PRELIMINARY

SigmaTel, Inc.

Integrating Mixed-Signal Solutions

STAC9705

Audio/Modem Codec for AC 97, 2.0

GENERAL DESCRIPTION:

SigmaTel's **STAC9705** is a general purpose 18-bit, full duplex, audio codec with integrated modem analog front end (AFE) that conforms to the analog component specification of AC 97 (Audio Codec 97 Component Specification rev. 2.0). The audio DACs, ADCs, and mixers are integrated with analog I/Os which include four analog line-level stereo inputs, two analog line-level mono inputs, and 5 output channels. The modem AFE includes a fully differential ADC and DAC along with 12 GPIOs for DAA interface. Also included are an extra audio ADC for hands free operation and an extra stereo line out for headphones or speaker amplifiers. The **STAC9705** communicates via the five wire AC Link to any digital component of AC 97 providing flexibility in the audio system design. Packaged in an AC 97 compliant 64-pin TQFP, the **STAC9705** can be placed on the motherboard, daughter boards, add-on cards, PCMCIA cards, or outside the main chassis such as in a speaker.

FEATURES:

- **High performance ΣΔ technology**
- **18-bit full duplex stereo A/D, D/A**
- **AC-link protocol compliance**
- **Additional audio A/D for MIC record**
- **AC 97 compliant mixer**
- **Energy saving power down modes**
- **Modem Analog Front End (AFE)**
- **Six analog line-level inputs**
- **Available in 64-pin TQFP**
- **Extra Stereo Line Out**

ORDERING INFORMATION:

PART NUMBER	PACKAGE	TEMPERATURE RANGE	SUPPLY RANGE
STAC9705T	64-pin TQFP 10mmx 10mm x 1.4mm	0^{O} C to $+70^{O}$ C	DVdd = 3.3V or 5V, AVdd = 5V

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Figure 1 - Package Outline

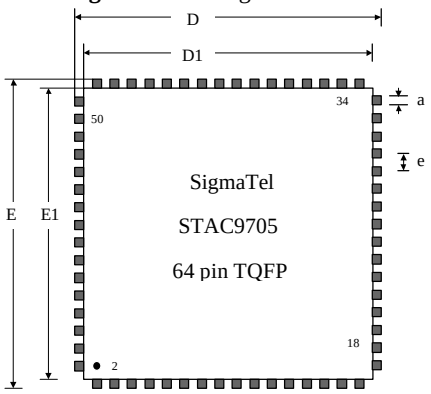


Table 1 - Package Dimensions

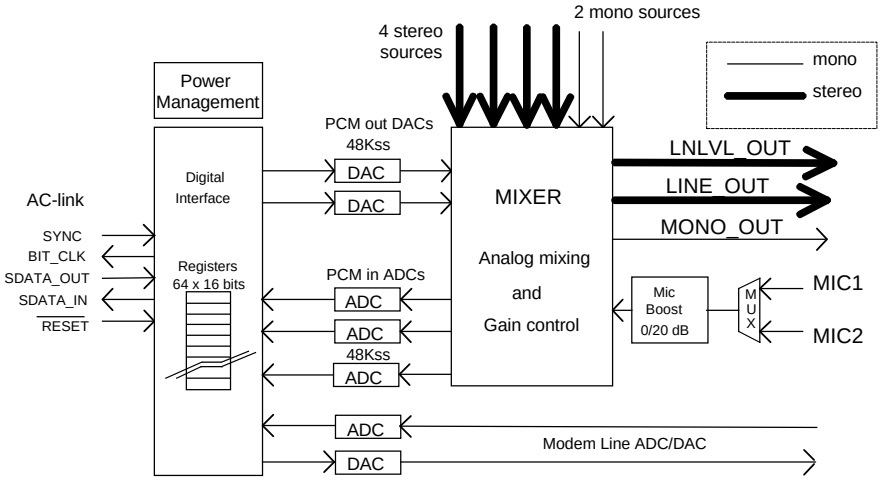
KEY	9701/3 DIMENSION LQFP
D	12.00 mm
D1	10.00 mm
E	12.00 mm
E1	10.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
thickness	1.4 mm

Table 2 - Pin Designation

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
1	GPIO0	*17*	AVss1	*33*	Vref	*49*	MONO_OUT
2	GPIO1	*18*	PC_BEEP	*34*	Vrefout	*50*	AVdd3
3	GPIO2	*19*	PHONE	*35*	AFILT1	*51*	LNLVL_OUT_L
4	GIPO3	*20*	AUX_L	*36*	AFILT2	*52*	NC
5	DVdd1	*21*	AUX_R	*37*	AFILT3	*53*	LNLVL_OUT_R
6	XTL_IN	*22*	VIDEO_L	*38*	CAP2	*54*	Avss3
7	XTL_OUT	*23*	VIDEO_R	*39*	CAP3	*55*	GPIO6
8	DVss1	*24*	CD_L	*40*	CAP4	*56*	GPIO7
9	SDATA_OUT	*25*	CD_GND	*41*	NC	*57*	TxAN
10	BIT_CLK	*26*	CD_R	*42*	NC	*58*	TxAP
11	DVss2	*27*	MIC1	*43*	NC	*59*	RxAN
12	SDATA_IN	*28*	MIC2	*44*	NC	*60*	RxAP
13	DVdd2	*29*	LINE_IN_L	*45*	LINE_OUT_L	*61*	GPIO8
14	SYNC	*30*	LINE_IN_R	*46*	LINE_OUT_R	*62*	GPIO9
15	RESET#	*31*	AVdd2	*47*	GPIO4	*63*	GPIO10
16	AVdd1	*32*	AVss2	*48*	GPIO5	*64*	GPIO11

# denotes active low

Figure 2. **STAC9705** Block Diagram

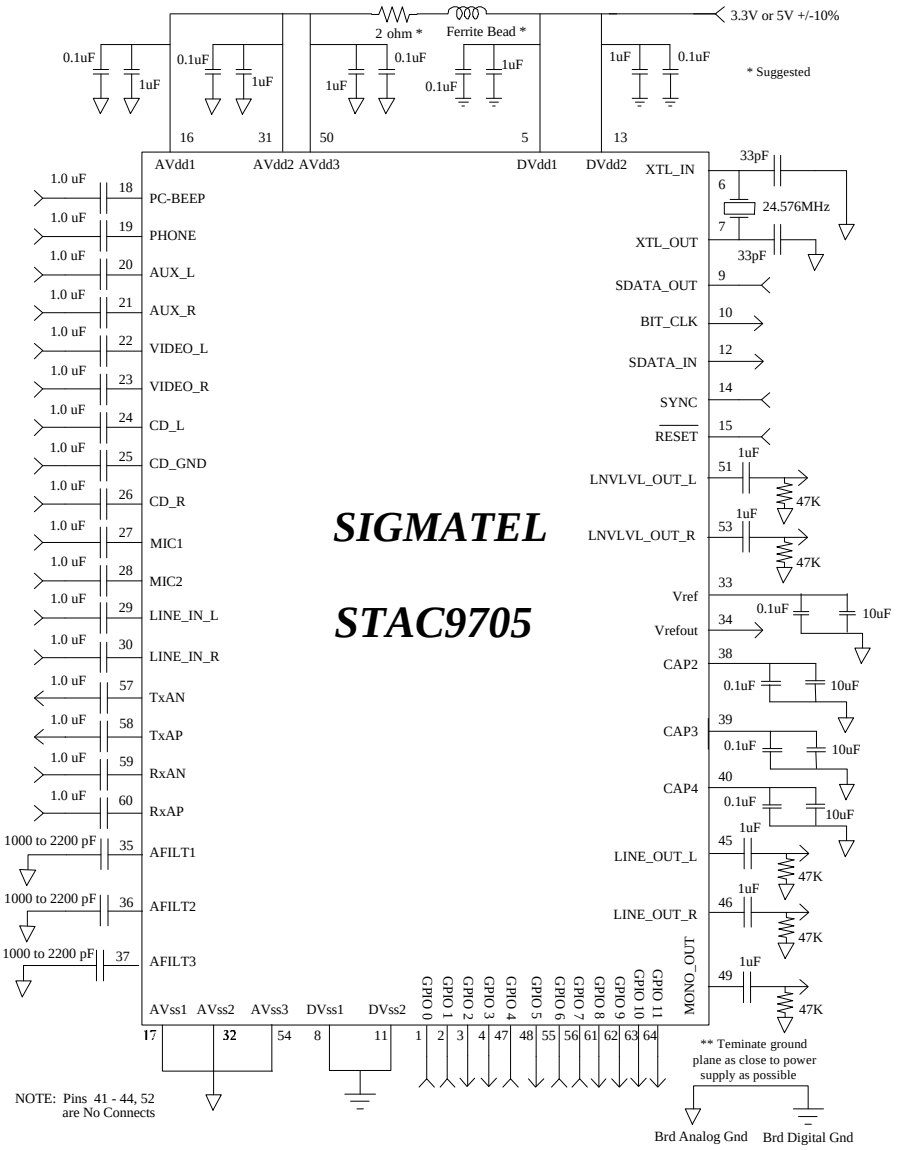


The **STAC9705** block diagram, above, illustrates its primary functional blocks. It performs fixed 48K sample rate D-A & A-D conversion, mixing, and analog processing. The digital interface communicates with the AC 97 controller via the five wire AC-link and contains the 64 word by 16-bit registers. Two fixed 48Kss DAC's support two stereo PCM-out channels which contain a mix generated in the AC 97 controller of all software sources, including the internal synthesizer and any other digital sources. The Mixer block mixes the PCM-out with any analog sources, then outputs to LINE_OUT and LN_LVL_OUT. The MONO_OUT delivers either mic only or a mono mix of sources from the mixer. The two fixed 48Ks ADC's take any mix of mono or stereo sources and convert it to a stereo PCM-in signal.

The **STAC9705** has a modem AFE which includes a fully differential ADC, DAC and associated loopback mode circuitry. The modem AFE supports all 6 required sample rates, and 4 optional sample rates from the AC97, Rev 2.0 specification. 12 GPIOs are also implemented to facilitate the DAA interface in modem applications.

Together with the logic component (controller) of AC 97, **STAC9705** can be SoundBlaster and Windows Sound System compatible. SoundBlaster is a registered trademark of Creative Labs. Windows is a registered trademark of Microsoft Corporation.

Figure 3 - Connection Diagram –
See Appendix A for an alternative connection diagram when using separate supplies



1. PIN/SIGNAL DESCRIPTIONS

1.1 Digital I/O

These signals connect the **STAC9705** to its AC 97 controller counterpart and an external crystal.

Table 3. Digital Signal List

SIGNAL NAME	TYPE	DESCRIPTION
RESET #	I	AC 97 Master H/W Reset
XTL_IN	I	24.576 MHz Crystal
XTL_OUT	O	24.576 MHz Crystal
SYNC	I	48 KHz fixed rate sample sync
BIT_CLK	O	12.288 MHz serial data clock
SDATA_OUT	I	Serial, time division multiplexed, AC 97 input stream
SDATA__IN	O	Serial, time division multiplexed, AC 97 output stream
GPIO 0,1,4,6,7	I	General Purpose I/O
GPIO 2,3,5,8-11	0	General Purpose I/O

# denotes active low

1.2 Analog I/O

These signals connect the **STAC9705** to analog sources and sinks, including microphones and speakers.

Table 4. Analog Signal List

SIGNAL NAME	TYPE	DESCRIPTION
PC-BEEP	I	PC Speaker beep pass through
PHONE	I	From telephony subsystem speakerphone (or DLP - Down Line Phone)
MIC1	I	Desktop Microphone Input
MIC2	I	Second Microphone Input
LINE-IN-L	I	Line In Left Channel
LINE-IN-R	I	Line In Right Channel
CD-L	I	CD Audio Left Channel
CD-GND	I	CD Audio analog ground
CD-R	I	CD Audio Right Channel
VIDEO-L	I	Video Audio Left Channel
VIDEO-R	I	Video Audio Right Channel
AUX-L	I	Aux Left Channel
AUX-R	I	Aux Right Channel
LINE-OUT-L	O	Line Out Left Channel
LINE-OUT-R	O	Line Out Right Channel
MONO-OUT	O	To telephony subsystem speakerphone (or DLP - Down Line Phone)

LNLVL_OUT_L	O	True Line Level Out Left Channel
LNLVL_OUT_R	O	True Line Level Out Right Channel
TxAN	O	Modem Transmit Out Negative
TxAP	O	Modem Transmit Out Positive
RxAN	I	Modem Receive Input Negative
RxAP	I	Modem Receive Input Positive

- Note: any unused input pins should have a capacitor (1 uF suggested) to ground.

1.3 Filter/References

These signals are connected to resistors, capacitors, or specific voltages.

Table 5. Filtering and Voltage References

SIGNAL NAME	TYPE	DESCRIPTION
Vref	O	Reference Voltage
Vrefout	O	Reference Voltage out 5mA drive (intended for mic bias)
AFILT1	O	Anti-Aliasing Filter Cap - ADC channel
AFILT2	O	Anti-Aliasing Filter Cap - ADC channel
AFILT3	O	Anti-Aliasing Filter Cap – MIC ADC
CAP2	O	ADC reference Cap
CAP3	O	Modem ADC Negative Input Anti-Alias Filter
CAP4	O	Modem ADC Positive Input Anti-Alias Filter

1.4 Power and Ground Signals

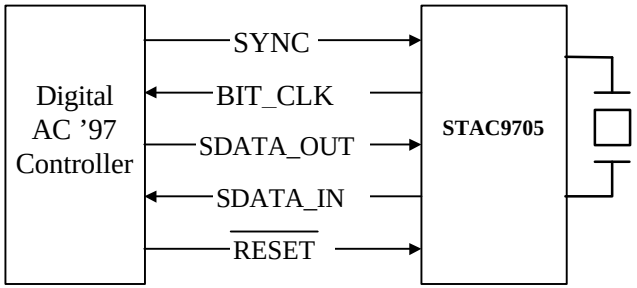
Table 6. Power Signal List **STAC9705**

SIGNAL NAME	TYPE	DESCRIPTION
AVdd1	I	Analog Vdd = 5.0V
AVdd2	I	Analog Vdd = 5.0V
AVss1	I	Analog Gnd
AVss2	I	Analog Gnd
AVdd3	I	Analog Vdd = 5.0V
AVss3	I	Analog Gnd
DVdd1	I	Digital Vdd = 5.0V or 3.3V
DVdd2	I	Digital Vdd = 5.0V or 3.3V
DVss1	I	Digital Gnd
DVss2	I	Digital Gnd

2. AC-LINK

Below is the figure of the AC-link point to point serial interconnect between the **STAC9705** and its companion controller. All digital audio streams and command/status information are communicated over this AC-link. Please refer to the "Digital Interface" section 3 for details and Appendix A for mixed supply operation..

Figure 4. **STAC9705's** AC97-link to its companion controller



2.1 Clocking

STAC9705 derives its clock internally from an externally connected 24.576 MHz crystal or an oscillator through the XTAL_IN pin. Synchronization with the AC 97 controller is achieved through the BIT_CLK pin at 12.288 MHz (half of crystal frequency).

The beginning of all audio sample packets, or "Audio Frames", transferred over AC-link is synchronized to the rising edge of the "SYNC" signal driven by the AC 97 controller. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled by the receiving side on each immediately following falling edge of BIT_CLK.

2.2 Reset

There are 3 types of resets as detailed under "Timing Characteristics".

1. a "cold" reset where all **STAC9705** logic is initialized to its default state

2. a "warm" reset where the contents of the **STAC9705** register set are left unaltered

3. a "register" reset which only initializes the **STAC9705** registers to their default states

After signaling a reset to the **STAC9705,** the AC 97 controller should not attempt to play or capture audio data until it has sampled a "Codec Ready" indication from the **STAC9705.**

In order for proper operation SDATA_OUT should be "0" during "cold" reset.

3. DIGITAL INTERFACE

3.1 AC-link Digital Serial Interface Protocol

The **STAC9705** communicates to the AC 97 controller via a 5 pin digital serial interface called AC-link which is a bi-directional, fixed rate, serial PCM digital stream. All digital audio streams, commands and status information are communicated over this point to point serial interconnect. This link handles multiple inputs, and output audio streams, as well as control register accesses using a time division multiplexed (TDM) scheme. The AC 97 controller synchronizes all AC-link data transaction. The following data streams are available on the **STAC9705:**

- **PCM Playback** **2 output slots** 2 Channel composite PCM output stream
- **PCM Record data** **2 input slots** 2 Channel composite PCM input stream

- **Control** **2 output slots** Control register write port
- **Status** **2 input slots** Control register read port
- **Modem AFE** **1 input / 1 output slot** Full duplex communication stream
- **GPIOs** **1 input / 1 output slot** General purpose I/O control streams
- **MIC Record data** **1 input slot** Microphone record input stream

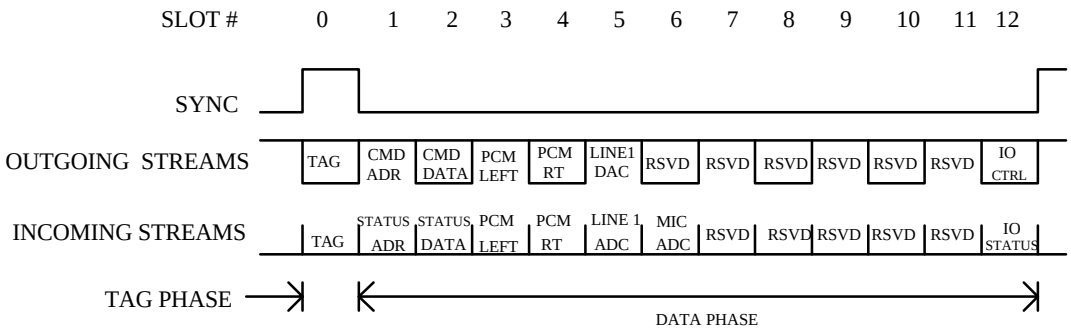
Synchronization of all AC-link data transactions is signaled by the AC 97 controller. The **STAC9705** drives the serial bit clock onto AC-link. The AC 97 controller then qualifies with a synchronization signal to construct audio frames.

SYNC, fixed at 48 KHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, **STAC9705** for outgoing data and AC 97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16-bit (13-bits defined, with 3 reserved trailing bit positions) time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A “1” in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is “tagged” invalid, it is the responsibility of the source of the data, (**STAC9705** for the input stream, AC 97 controller for the output stream), to stuff all bit positions with 0’s during that slot’s active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the “Tag Phase”. The remainder of the audio frame where SYNC is low is defined as the “Data Phase”.
Additionally, for power savings, all clock, sync, and data signals can be halted.

Figure 5. AC 97 Standard Bi-directional Audio Frame

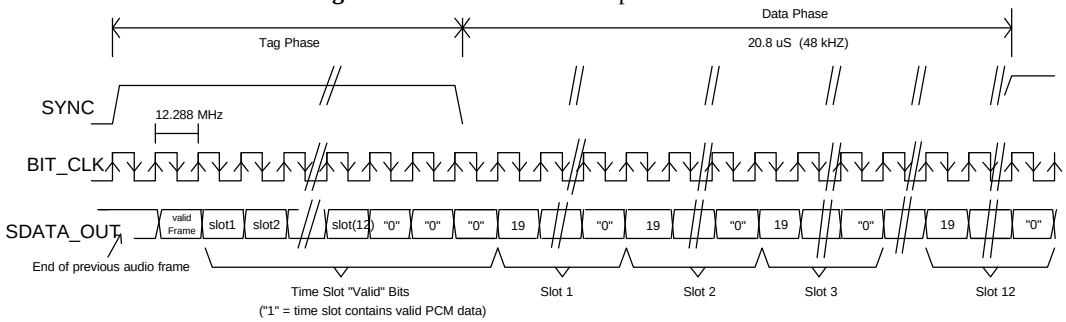


3.1.1 AC-link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the **STAC9705** DAC inputs, and control registers. Each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits which are used for AC-link protocol infrastructure.

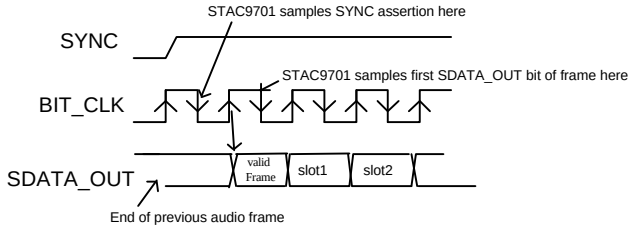
Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the “Valid Frame” bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by the **STAC9705** indicate which of the corresponding 12 times slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48KHz audio frame rate. The following diagram illustrates the time slot based AC-link protocol.

Figure 6. AC-link Audio Output Frame



A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the **STAC9705** samples the assertion of SYNC. This following edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the AC 97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the **STAC9705** on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 7: Start of an Audio Output Frame



SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions stuffed with 0's by the AC 97 controller.
When mono audio sample streams are sent from the AC 97 controller it is necessary that BOTH left and right sample stream time slots be filled with the same data.

3.1.1.1 Slot 1: Command Address Port

The command port is used to control features, and monitor status (see Audio Input Frame Slots I and 2) of the **STAC9705** functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid.

Audio output frame slot 1 communicates control register address, and write/read command information to the **STAC9705**.

Command Address Port bit assignments:

Bit (19) Read/Write command (1= read, 0=write)
Bit (18:12) Control Register Index (64 16-bit locations, addressed on even byte boundaries)
Bit (11:0) Reserved (Stuffed with 0's)

The first bit (MSB) sampled by **STAC9705** indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must he stuffed with 0's by the AC 97 controller.

3.1.1.2 Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (as indicated by Slot 1, bit 19)

Bit (19:4) Control Register Write Data (Stuffed with 0's if current operation is a read)
Bit (3 :0) Reserved (Stuffed with 0's)

If the current command port operation is a read then the entire slot time must be stuffed with 0's by the AC 97 controller.

3.1.1.3 Slot 3: PCM Playback Left Channel

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical “Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC 97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC 97 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

3.1.1.4 Slot 4: PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical “Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC 97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC 97 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

3.1.1.5 Slot 5: Modem Line1 DAC

Output frame slot 5 is the modem DAC output stream. This output channel drives a fully differential signal which connects to the DAA in modem applications. Modem DAC sample rate is controlled by the sample rate register, 40h, and level control via register 46h.

3.1.1.6 Slots 6-11: Reserved

Output frame slots 6-11 are used for multi channel outputs, second modem DAC, and additional headset DAC not supported by the **STAC9705.**

3.1.1.7 Slot 12: I/O Control

3.1.2 AC-link Audio Input Frame (SDATA_IN)

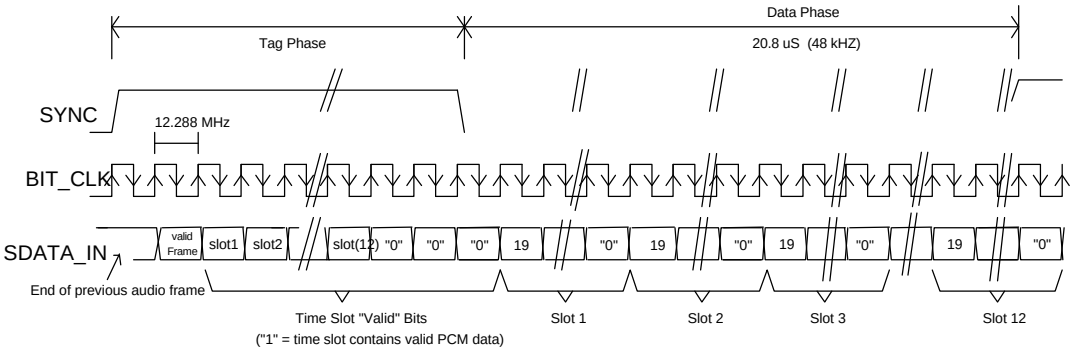
The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC 97 controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the **STAC9705** is in the "Codec Ready" state or not. If the “Codec Ready” bit is a 0, this indicates that **STAC9705** is not ready for normal operation. This condition is normal following the de-assertion of power on reset, for example, while **STAC9705**’s voltage references settle. When the AC-link "Codec Ready" indicator bit is a 1, it indicates that the AC-link and **STAC9705** control/status registers are in a fully operational state. The AC 97 controller must further probe the Powerdown Control Status Register (refer to Mixer Register section) to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting **STAC9705** into operation the AC 97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that **STAC9705** has become "Codec Ready". Once the **STAC9705** is sampled "Codec Ready", the next 12 bit positions sampled by the AC 97 controller indicate which of the corresponding 12 time slots are assigned to input data

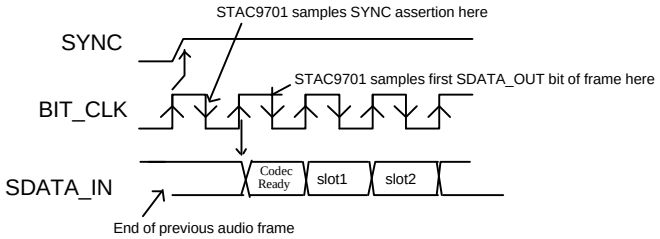
streams, and that they contain valid data. The following diagram illustrates the time slot based AC-link protocol.

Figure 8: **STAC9701** Audio Input Frame



A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, **STAC9705** samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the **STAC9705** transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK and subsequently sampled by the AC 97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 9: Start of an Audio Input Frame



SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0's by **STAC9705**. SDATA_IN data is sampled on the falling edges of BIT_CLK.

3.1.2.1 Slot 1: Status Address Port

The status port is used to monitor status for **STAC9705** functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by **STAC9705** during slot 0)

Status Address Port hit assignments:

Bit (19)	RESERVED	(Stuffed with 0)
Bit (18;12)	Control Register Index	(Echo of register index for which data is being returned)
Bit (11:0)	RESERVED	(Stuffed with 0's)

The first bit (MSB) generated by **STAC9705** is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, and the trailing 12 bit positions are stuffed with 0's by **STAC9705**.

3.1.2.2 Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Bit (19:4)	Control Register Read Data	(Stuffed with 0's if tagged "invalid")
Bit (3 :0)	RESERVED	(Stuffed with 0's)

If Slot 2 is tagged "invalid" by **STAC9705,** then the entire slot will be stuffed with 0's.

3.1.2.3 Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of **STAC9705** input MUX, post-ADC. **STAC9705** ADCs are implemented to support 18-bit resolution.

STAC9705 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

3.1.2.4 Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of **STAC9705** input MUX, post-ADC.

STAC9705 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

3.1.2.5 Slot 5: Modem Line 1 ADC

Input frame slot 5 is the modem ADC output stream. This input channel is converted from the differential input connected to the DAA in modem applications. Modem DAC/ADC sample rate is controlled by the sample rate register, 40h, and level control via register 46h.

3.1.2.6 Slot 6: MIC Record Channel

Audio input frame slot 6 is the MIC channel output of the **STAC9705** input MUX, post ADC.

3.1.2.7 Slots 7 – 11: Reserved

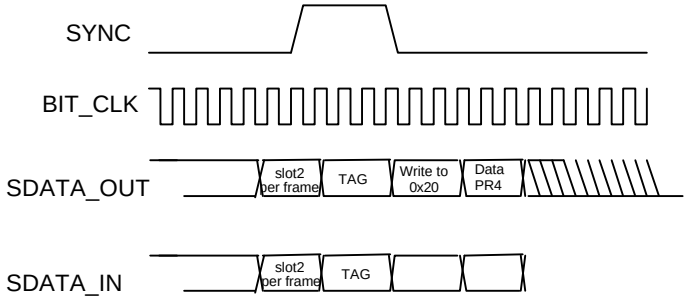
Input frame slots 7 – 11 are for reserved slots, second modem ADC and Headset DAC not supported by the **STAC9705.**

3.1.2.8 Slot 12: IO Status

3.2 AC-link Low Power Mode

The **STAC9705** can be placed in the low power mode by programming Register 26h to the appropriate value. Both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level. The AC 97 controller can wake up the **STAC9705** by providing the appropriate reset signals.

Figure 10. **STAC9705** Powerdown Timing



Note: BIT_CLK not to scale

BIT_CLK and SDATA_IN are transitioned low immediately (within the maximum specified time) following the decode of the write to the Powerdown Register (26h) with PR4. When the AC 97 controller driver is at the point where it is ready to program the AC-link into its low power mode, slots (1 and 2) are assumed to be the only valid stream in the audio output frame (all sources of audio input have been neutralized).

The AC 97 controller should also drive SYNC, and SDATA_OUT low after programming the **STAC9705** to this low power mode.

3.2.1 Waking up the AC-link

Once the **STAC9705** has halted BIT_CLK, there are only two ways to "wake up" the AC-link. Both methods must be activated by the AC 97 controller.

The AC-link protocol provides for a "Cold AC 97 Reset", and a "Warm AC 97 Reset". The current power down state would ultimately dictate which form of reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset register) is performed, wherein the AC 97 registers are initialized to their default values, registers are required to keep state during all power down modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

Cold Reset - a cold reset is achieved by asserting RESET# for the minimum specified time. By driving RESET# low, BIT_CLK, and SDATA_IN will be activated, or re-activated as the case may be, and all **STAC9705** control registers will be initialized to their default power on reset values.

Note: RESET# is an asynchronous input. # denotes active low

Warm Reset - a warm reset will re-activate the AC-link without altering the current **STAC9705** register values. A warm reset is signaled by driving SYNC high for a minimum of 1 uS in the absence of BIT_CLK.

Note: Within normal audio frames, SYNC is a synchronous input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the **STAC9705**.

4. STAC9705 MIXER

The **STAC9705** mixer is designed to the AC 97 specification to manage the playback and record of all digital and analog audio sources in the PC environment. These include:

- **System Audio**: digital PCM input and output for business, games and multimedia
- **CD/DVD**: analog CD/DVD-ROM Redbook audio with internal connections to Codec mixer
- **Mono microphone**: choice of desktop mic, with programmable boost and gain
- **Speakerphone**: use of system mic and speakers for telephone, DSVD, and video conferencing
- **Video**: TV tuner or video capture card with internal connections to Codec mixer
- **AUX/synth**: analog FM or wavetable synthesizer, or other internal source

Figure 11. **STAC9705** Mixer Functional Diagram

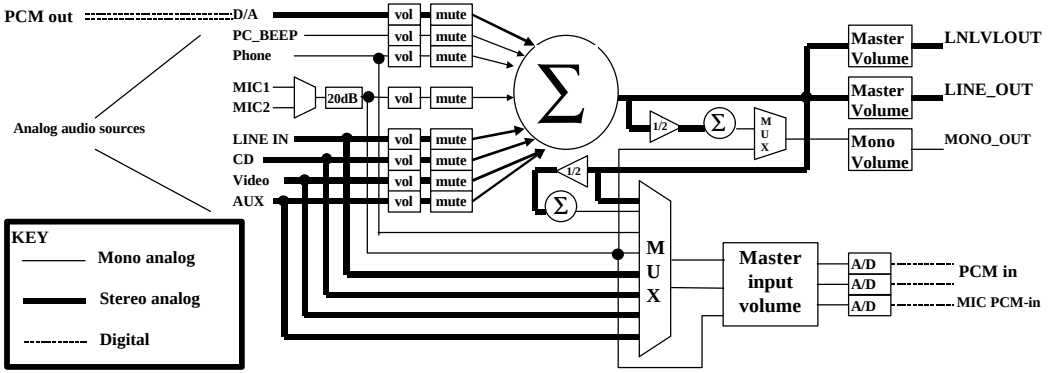


Table 7. Mixer functional connections

SOURCE	FUNCTION	CONNECTION
PC_Beep	PC beep pass thru	from PC beeper output
PHONE	speakerphone or DLP in	from telephony subsystem
MIC1	desktop microphone	from mic jack
MIC2	second microphone	from second mic jack
LINE_IN	external audio source	from line-in jack
CD	audio from CD-ROM	cable from CD-ROM
VIDEO	audio from TV tuner or video camera	cable from TV or VidCap card
AUX	upgrade synth or other external source	internal connector
PCM out	digital audio output from AC 97 Controller	AC-link
LINE_OUT	stereo mix of all sources	to output jack
LNLVL_OUT	Additional stereo mix of all sources	to output jack
MONO_OUT	mic or mix for speakerphone or DLP out	to telephony subsystem
MIC PCM in	Digital MIC input to AC 97 Controller	AC-link
PCM in	digital audio input to AC 97 Controller	AC-link

4.1 Mixer Input

The mixer provides recording and playback of any audio sources or output mix of all sources. The **STAC9705** supports the following input sources:

- any mono or stereo source
- mono or stereo mix of all sources
- 2-channel input w/mono output reference (mic + stereo mix)

Note: any unused input pins must have a capacitor (1 uF suggested) to ground.

4.2 Mixer Output

The mixer generates three distinct outputs:

- a stereo mix of all sources for output to the LINE_OUT
- a stereo mix of all sources for output to the LNLVL_OUT
- a mono, mic only or mix of all sources for MONO_OUT

  * Note: Mono output of stereo mix is attenuated by ½ .

4.3 PC Beep Implementation

PC Beep is active on power up and defaults to an unmuted state. The user should mute this input before using any other mixer input because the PC Beep input can contribute noise to the lineout during normal operation.

4.4 Mixer and Modem Registers:

Table 8. Mixer and Modem Registers

REG #	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DE FAULT
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	NA
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
04h	LNLVL Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	x000h
0Ch	Phone volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	AUX Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
1Eh	Record Gain Mic	Mute	X	X	X	X	X	X	X	X	X	X	X	GM3	GM2	GM1	GM0	8000h
20h	General Purpose	X	ST	X	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	000h
26h	Powerdown Ctrl/Stat	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	NA
2Ah	Ext'd Audio Ctrl/Stat	X	PRL	PRK	PRJ	PRI	X	MADC	LDAC	SDAC	CDAC	X	X	VRM	X	DRA	VRA	xxxxh
3Ch	Extended Modem ID	ID1	ID0	X	X	X	X	X	X	X	X	X	CID2	CID1	HSET	LIN2	LIN1	xxxxh
3Eh	Ext'd Modem Stat/Ctrl	PRH	PRG	PRF	PRE	PRD	PRC	PRB	PRA	HDAC	HADC	DAC2	ADC2	DAC1	ADC1	MREF	GPIO	xxxxh
40h	Line1 DAC/ADC Rate (IO slot 5)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
46h	Line 1 DAC/ADC Level	Mute	X	X	X	DAC3	DAC2	DAC1	DAC0	Mute	X	X	X	ADC3	ADC2	ADC1	ADC0	8080h
4Ah	Handset ADC level	X	X	X	X	X	X	X	X	Mute	X	X	X	ADC3	ADC2	ADC1	ADC0	8080h
4Ch	GPIO Pin Config (0=out, 1=in)	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	xxxxh

4Eh	GPIO Pin Polarity/Type (0=low,1=high)	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	FFFFh
50h	GPIO Pin Sticky (0=not sticky, 1=sticky)	GS15	GS14	GS13	GS12	GS11	GS10	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0	0000h
52h	GPIO Pin Wakeup (0=no, 1=yes int)	GW15	GW14	GW13	GW12	GW11	GW10	GW9	GW8	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0	0000h
54h	GPIO Pin Status (slot 12, bits 15-0)	GI15	GI 14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	xxxxh
56h	Misc. Modem AFE Stat/Ctrl	CID2	CID1	CIDR	X	X	HSB2	HSB1	HSB0	X	L2B2	L2B1	L2B0	X	L1B2	L1B1	L1B0	0000h
7Ch	Vendor ID1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	NA
7Eh	Vendor ID2	0	1	1	1	0	1	1	0	0	0	0	0	0	1	0	0	NA

Notes:

1. All registers not shown and bits containing an X are reserved.

2. Any reserved bits, marked X, can be written to but are don't care upon read back.

3. PC_BEEP default to 0000h, mute off.

4. If optional bits D13, D5 of register 02H or D5 of register 06H are set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 3fH as a value for this attenuation/gain block.

4.4.1 Reset Register (Index 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part.
All DACs operate at the same resolution. All ADCs operate at the same resolution.

4.4.2 Play Master Volume Registers (Index 02h, 04h, and 06h)

These registers manage the output signal volumes. Register 02h controls the stereo master volume (both right and left channels), register 04h controls the optional stereo true line level out, register 06h controls the mono volume output. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. ML5 through ML0 is for left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel.

The default value is 8000h (1000 0000 0000 0000), which corresponds to 0 dB attenuation with mute on.

Table 9: Play Master Volume Register

MUTE	MX5…MX0	FUNCTION	RANGE
0	00 0000	0dB Attenuation	Req.
0	01 1111	46.5 Attenuation	Req.
1	xx xxxx	∞ dB Attenuation	Req.

4.4.3 PC Beep Register (Index 0Ah)

This controls the level for the PC Beep input. Each step corresponds to approximately 3 dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. PC_BEEP supports motherboard implementations. The intention of routing PC_BEEP through the **STAC9705** mixer is to eliminate the requirement for an onboard speaker by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times. NOTE: the PC_BEEP is recommended to be routed to L & R Line outputs even when the **STAC9705** is in a RESET state. This is so that Power On Self Test (POST) codes can be heard by the user in case of a hardware problem with the PC. For further PC_BEEP implementation details please refer to the AC 97 Technical FAQ sheet. The default value can be 0000h or 8000h, which corresponds to 0 dB attenuation with mute off or on.

Table 10: PC_BEEP Register

MUTE	PV3…PV0	FUNCTION
0	0000	0 dB Attenuation
0	1111	45 dB Attenuation
1	xxxx	∞ dB Attenuation

4.4.4 Analog Mixer Input Gain Registers (Index 0Ch - 18h)

This controls the gain/attenuation for each of the analog inputs. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. Register 0Eh (Mic Volume Register) has an extra bit that is for a 20dB boost. When bit 6 is set to 1, the 20 dB boost is on. The default value is 8008, which corresponds to 0 dB gain with mute on. The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0 dB gain with mute on.

Table 11: Analog Mixer Input Gain Register

MUTE	GX4…GX0	FUNCTION
0	00000	+12 dB gain
0	01000	0 dB gain
0	11111	-34.5 dB gain
1	xxxxx	-∞ dB gain

4.4.5 Record Select Control Register (Index 1Ah)

Used to select the record source independently for right and left. The default value is 0000h, which corresponds to Mic in.

Table 12: Record Select Control Registers

SR2…SR0	RIGHT RECORD SOURCE
0	Mic
1	CD In (right)
2	Video In (right)
3	Aux In (right)

4	Line In (right)
5	Stereo Mix (right)
6	Mono Mix
7	Phone

SL2…SL0	LEFT RECORD SOURCE
0	Mic
1	CD In (L)
2	Video In (L)
3	Aux In (L)
4	Line In (L)
5	Stereo Mix (L)
6	Mono Mix
7	Phone

4.4.6 Record Gain Registers (Index 1Ch and 1Eh)

1Ch is for the stereo input and 1Eh is for the optional special purpose correlated audio mic channel. Each step corresponds to 1.5 dB. 22.5 dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at -∞ dB.

The default value is 8000h, which corresponds to 0 dB gain with mute on.

Table 13: Record Gain Registers

MUTE	GX3… GX0	FUNCTION
0	1111	+22.5 dB gain
0	0000	0 dB gain
1	xxxx	-∞ gain

4.4.7 General Purpose Register (Index 20h)

This register is used to control some miscellaneous functions. Below is a summary of each bit and its function. The MS bit controls the mic selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements.

Table 14: General Purpose Registers

BIT	FUNCTION
MIX	Mono output select 0 = Mix, 1= Mic
MS	Mic select 0 = Mic1, 1 = Mic2
LPBK	ADC/DAC loopback mode

4.4.8 Powerdown Control/Status Register (Index 26h)

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a "1" indicating that the subsection is "ready". *Ready* is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-link will have no effect on read only bits 0-7.

When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-link and AC 97 control and status registers are in a fully operational state. The AC 97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any are ready.

Table 15: Powerdown Status Registers

BIT	FUNCTION
REF	VREF's up to nominal level
ANL	Analog mixers, etc. ready
DAC	DAC section ready to playback data
ADC	ADC section ready to playback data

The power down modes are as per Table 16. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADC's and DAC's only. For modem AFE subsystem powerdown, see Section 4.5.2.

4.4.9 Extended Audio Control/Status Register (Index 2Ah)

The Extended Audio Status and Control Register is a *read/write* register that provides status and control of the extended audio features.

Bits D3-D0 are *read.write* controls that enable or disable the extended audio features

- VRA=1 enables Variable Rate Audio mode(sample rate control registers and SLOTREQ signaling)
- DRA=1 enables Double-Rate Audio mode
- VRM=1 enables Variable Rate Audio mode for the dedicated MIC ADC

The STAC9705 does not currently support the variable or double rate audio modes.

Bits D9-D6 are *read only* status of the extended audio feature readiness

- CDAC=1 indicates the PCM Center DAC is ready (6CH mode)
- SDAC=1 indicates the PCM Surround DACs are ready (6CH mode)
- LDAC=1 indicates the PCM LFE DAC is ready (6CH mode)
- MADC=1 indicates the MIC ADC is ready (new status for previously defined AC 97 feature)

The STAC9705 does not currently support the PCM Center, Surround, and LFE options.

Bits D14-D11 are read/write control of the extended audio feature power-down

- PRI=1 turns the PCM Center DAC off
- PRJ=1 turns the PCM Surround DACs off (6CH mode)
- PRK=1 turns the PCM LFE DACs off (6CH mode)
- PRL=1 turns the MIC ADC off (MIC ADC operation is independent of PR0 from 26h)

The STAC9705 does not currently support the PCM Center, Surround, LFE options.

4.5. Modem AFE Register Definitions

4.5.1. Extended Modem ID Register (Index 3Ch)

The extended modem ID is a *read/write* register that primarily identifies the enhanced codec's modem AFE capabilities. The default value will depend on features and hardware configuration. Writing any value to this register performs a warm modem AFE reset (register range 3C-56h), including GPIO (register range 4C-54h). The warm reset causes all affected registers to revert to their default values. Note: the audio and modem AFE are logically independent (writes to register 0h resets audio only).

- LIN1=1 indicates 1st line is supported
- LIN2=1 indicates 2nd line is supported
- HSET=1 indicates handset DAC/ADC is supported
- CID1=1 indicates that caller ID decode for line 1 is supported
- CID2=1 indicates that caller ID decode for line 2 is supported
- ID1, ID0 is a 2-bit field which indicates the codec configuration: Primary is 00; Secondary is 01, 10, or 11

Only the LIN1=1 (Single Modem AFE) is supported in the **STAC9705** indicating the codec is an AMC '97 and all modem functionality is implemented and controlled via the newly defined Extended AC 97 registers. In particular, the following functionality is NOT implemented as defined in the original AC 97 Component Specification:

- Reset Register (Index 0h) bit 1: Modem line codec support (ID1)
- Reset Register (Index 0h) bit 6-9 audio DAC and ADC resolution do not have any MAFE resolution info
- General Purpose Register (Index 20h) bits 10, 11: Local Loop Back (LLBK) and Remote Loop Back (RLBK)
- Modem Rate (Index 24h) Register
- Powerdown/Ctrl/Stat (Index 26h) bits 4 ,15: Modem Ready (MDM) and Modem DAC/ADC off (PR7)

4.5.2. Extended Modem Status and Control Register (Index 3Eh)

The Extended Modem Status and Control register functions similarly to the original AC 97 Powerdown Control/Status register, located at index 26h. The AMC '97 codec restricts modem and handset powerdown control/status to this register since all of the functions are provided here. Therefore, the AMC '97 codec (and DC '97 controller, of course) must ignore bits MDM and PR7 in register 26h and use what is included here. When

the GPIO section is powered down, all outputs are tri-stated and input slot 12 is marked invalid when the AC-link is active.

Bits 7-0 are *read only*, "1" indicate modem AFE subsystem readiness:

- GPIO=1 indicates GPIO ready
- MREF=1 indicates Modem Vref's up to nominal level
- ADC1=1 indicates Modem Line 1 ADC ready
- DAC1=1 indicates Modem Line 1 DAC ready
- ADC2=1 indicates Modem Line 2 ADC ready
- DAC2=1 indicates Modem Line 2 DAC ready
- HADC=1 indicates Handset ADC ready
- HDAC=1 indicates Handset DAC ready

The **STAC9705** does not support the optional Modem Line 2 ADC/DAC, or the Handset ADC/DAC

Bits 15-8 are *read/write* and control modem AFE subsystem powerdown. For AMC '97 implementations which use a common AREF and MREF, both powerdown bits must be low for disabling the reference.

- PRA=1 indicates GPIO powerdown
- PRB=1 indicates Modem Vref off
- PRC=1 indicates Modem Line 1 ADC off
- PRD=1 indicates Modem Line 1 DAC off
- PRE=1 indicates Modem Line 2 ADC off
- PRF=1 indicates Modem Line 2 DAC off
- PRG=1 indicates Handset ADC off
- PRH=1 indicates Handset DAC off

Bits 7-0 are *read only*, "1" indicate modem AFE subsystem readiness. Bits 15-8 are *read/write* and control modem AFE subsystem powerdown. For AMC '97 implementations which use a common AREF and MREF, both powerdown bits must be low for disabling the reference.

4.5.3. Modem Sample Rate Control Registers (Index 40h – 44h)

For modem AFE, each DAC/ADC pair is governed by a read/write modem sample rate control register which contains a 16-bit unsigned value between 0 and 65535, representing the rate of operation in Hz. Any number written over BB80h will cause the sample rate to be 48 kHz. For all rates, if the value written to the register is supported that value will be echoed back when read, otherwise the closest (higher in case of a tie) rate supported is returned.

Error! Reference source not found. defines the modem AFE sample rates supported in the **STAC9705,** with the required rates shown in **bold** typeface and the optional rates shown in *italics*. Although bit fields could be used to support the relatively few required and recommended sample rates, a full 16-bit register was chosen as the most flexible way to support future expandability.

Table 16. Sample Rates for Modem AFE (Hz)

Required and *recommended* sample rates for modem AFE (Hz)	
Sample rate	**D15-D0**
7200	*1C20*
8000	**1F40**
9000	*2328*
9600	**2580**
10285.71 (72000/7)	*282D*
13,714.28 (96000/7)	**3592**
16000	**3E80**
19200	*4B00*
24000	**5DC0**
48000	**BB80**

Note: In order to comply with ITU-T modem recommendations, sample rates must be generated to a tolerance of +/- 0.01%. This includes crystal tolerance, including variations over voltage, temperature, and age.

4.5.4. Modem DAC/ADC Level Control Registers (Index 46h-4Ah)

These *read/write* registers control the modem AFE DAC and ADC levels. DAC levels are defined to be the same as AC 97 Play Master Volume Register (2-6h minus 5th and 6th bits), ADC levels are defined to be the same as AC 97 Record Gain Registers (1C-1Eh).

The default value 8080h corresponds to 0dB DAC attenuation with mute on , 0dB ADC gain/attenuation with mute on.

4.5.5. GPIO Pin Configuration Register (Index 4Ch)

The GPIO Pin Configuration is a read/write register which specifies whether a GPIO pin is configured for input (“1”) or for output (“0”), and is accessed via the standard slot 1 and 2 command address/data protocols.

On reset (Cold or Warm), all pins are configured as inputs. The Status of all implemeted GPIO pins will initially read back "1" (via Slot 12 or reg 54h), any unimplemented GPIO pins will always read back "0". This scheme informs software as to how many GPIO pins have been implemented. It is up to the DC ‘97 controller to send the desired GPIO pin value over output slot 12 in the outgoing stream of the AC-link before configuring any of these bits for output.

4.5.6. GPIO Pin Polarity/Type Register (Index 4Eh)

The GPIO Pin Polarity/Type is a read/write register which defines GPIO Input Polarity (0=Low, 1=High active) when a GPIO pin is configured as an Input. It defines GPIO Output Type (0=CMOS, 1=OPEN-DRAIN) when a GPIO pin is configured as an Output.

On reset (Cold or Warm) this register defaults to all 1's. Unimplemented GPIO pins always return "1's".

4.5.7. GPIO Pin Sticky Register (Index 50h)

The GPIO Pin Sticky is a read/write register that defines GPIO Input Type (0=Not Sticky, 1=Sticky) when a GPIO pin is configured as an input. GPIO inputs configured as Sticky are cleared by writing a “0” to the corresponding bit of the GPIO Pin Status register 54h (see below), and by reset.

On reset (Cold or Warm) this register defaults to all "0's" specifying Non-Sticky. Unimplemented GPIO pins always return "0's". Sticky is defined as Edge sensitive, Non-Sticky as Level sensitive.

4.5.8. GPIO Pin Wakeup Mask Register (Index 52h)

The GPIO Pin Wakeup is a read/write register that provides a mask for determining if an input GPIO change will generate a wakeup or GPIO_INT (0=No, 1=Yes). When the AC-Link is powered down (Register 26h PR4 = 1 for Primary Codecs), a wakeup event will trigger the assertion of SDATA_IN (the AC-Link wakeup protocol is defined in Appendix C). When AC-link is powered up, a wakeup event will appear as GPIO_INT=1 on bit 0 of input slot 12.

On reset (Cold or Warm) this register defaults to all "0's" specifying no wakeup event. Unimplemented GPIO pins always returns "0's". An AC-Link wakeup Interrupt is defined as a "0" to "1" transition on SDATA_IN when the AC-Link is Powered down (Register 26h PR4="1"). GPIO bits which have been programmed as Inputs, Sticky and Pin Wakeup, upon transition either (high-to-low) or (low-to-high) depending on Pin polarity, will cause an AC-Link wakeup event (Transition of SDATA_IN from "0" to "1") if and only if the AC-Link was powered down.

4.5.9. GPIO Pin Status Register (Index 54h)

The GPIO Status is a read/write register that reflects the state of all GPIO pins (inputs and outputs) on slot 12. The value of all GPIO pin inputs and outputs comes in from the codec every frame on slot 12, but is also available for reading as GPIO Pin Status via the standard slot 1 and 2 command address/data protocols. GPIO inputs configured as Sticky are cleared by writing a “0” to the corresponding bit of this register 54h.

Bits corresponding to unimplemented GPIO pins should be forced to zero in this register and input slot 12.

Reset (Cold or Warm) does not affect value read. It is always the state of the GPIO pin. GPIO bits which have been programmed as Inputs and Sticky, upon transition either (high-to-low) or (low-to-high) depending on Pin

polarity, will cause the individual GI bit to go asserted "1", and remain asserted until a write of "0" to that bit. The only way to set the desired value of a GPIO output pin is to set the control bit in output slot 12.

4.5.10. Misc. Modem AFE Status and Control Register (Index 56h)

This *read/write* register defines the loop back modes available for the modem line and handset ADCs/DACs described in section 7

- L1B2-0 controls Line 1 loopback modes (or disabled)
- L2B2-0 controls Line 2 loopback modes (or disabled)
- HSB2-0 controls Handset loopback modes (or disabled)
- CID1=1 indicates caller ID decode for Line 1 is supported
- CID2=1 indicates caller ID decode for Line 2 is supported
- CIDR=1 indiocates that called ID data is “raw” (demodulated but not decoded; includes seizure, marks, etc.)

The **STAC9705** does not support Line 2 Modem, Handset ADC/DAC, or caller ID decode.

5. GPIO PIN DEFINITIONS

GPIO pins are programmable to have input/output functionality. The data values (status) for these pins are all in one register with input/output configuration in a separate register. Control of GPIO pins configured for output is achieved by setting the corresponding bit in output slot 12; status of GPIO pins configured for input is returned on input slot 12.

The codec constantly sets the GPIO pins that are configured for output, based upon the value of the corresponding bit position of the control slot 12. The codec ignores output slot 12 bits that correspond to GPIO control pins configured as inputs. The codec constantly updates status on input slot 12 based upon the logic level detected at each GPIO pin configured for input. A GPIO output pin value that is written via slot 12 in the current frame won’t affect the GPIO status that is returned in that particular write frame.

This slot 12 based control/status protocol minimizes the latency and complexity, especially for host based controllers and host data pump software, and provides high speed monitoring and control, above what could be achieved with command/status slots. For host based implementations most AC97 registers can be shadowed by the driver in order to provide immediate response when read by the CPU, and GPIO pins configured as inputs should be capable of triggering an interrupt upon a change of status.

The AC-link request for GPIO pin status is always delayed by at least one frame time. Read-Modify-Writes across the AC-link will thus incur latency issues and must be accounted for by the software driver or DC ‘97 controller firmware. PCI retries must be kept to a minimum wherever possible.

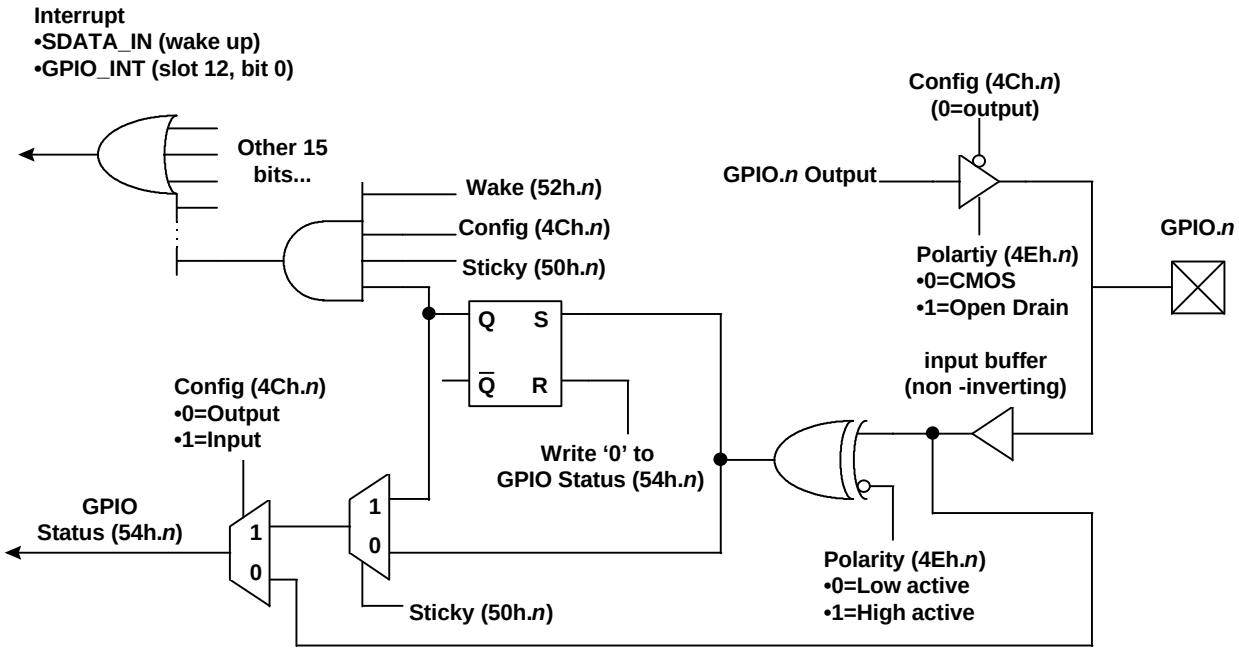
5.1. GPIO Pin Implementation

The **STAC9705** modem AFE contains 12 General Purpose Input/Outputs suitable for easy connection with minimal parts to a DAA circuit. The GPIOs, when configured as outputs, may not be able to directly drive a relay coil. The DC '97 controller has the responsibility to configure any GPIOs as outputs on power-up in order to drive transistors appropriately for DAA control.

When configured as an input, a GPIO functions as a CMOS Schmitt triggered input for a 3.3V power supply. Internal pull-ups or pull-downs should not be present in order to conserve power; the board designers are responsible for connecting unused pins to DVdd or DVss.

The GPIOs are tristated to a high impedance state on power-on or a cold reset. It is up to the DC '97 controller to first enable the output after setting it to the desired state. To prevent overdrive of any transistors, the outputs have slow rise and fall times. Typical values are 40 nsec for 10% to 90% of DVdd with a 50 pF load. In addition, the device will sink 2-4 mA at a maximum level of 0.4V and will source 2-4 mA at a minimum level of 2.4V.

Figure 12. "Conceptual" example of GPIO pin implementation



5.2. Recommended Slot 12 GPIO Bit Definitions

Table 17. Recommended Slot 12 GPIO bit definitions

Slot 12 (Input and Output): GPIO bits				
Bit	**GPIO**	**Name**	**Sense**	**Description**
19	GPIO15	LINE2_HL2R	out	opt GPIO / HANDSET_TO_LINE2 relay control (out)
18	GPIO14	LINE2_PULSE	in/out	opt GPIO / Line 2 pulse dial (out)
17	GPIO13	LINE2_LCS	in	Loop Current Sense Line 2
16	GPIO12	LINE2_CID	out	Caller ID path enable Line 2
15	GPIO11	LINE2_RI	in	Ring Detect Line 2
14	GPIO10	LINE2_OH	out	Off Hook Line 2
13	GPIO9	LINE12_RS	in/out	opt GPIO / International Bit 3 / Line 1/2 RS (out)
12	GPIO8	LINE12_DC	in/out	opt GPIO / International Bit 2 / Line 1/2 DC (out)
11	GPIO7	LINE12_AC	in/out	opt GPIO / International Bit 1 / Line 1/2 AC (out)
10	GPIO6	LINE1_HOHD	in/out	opt GPIO / HANDSET off hook detect (in)
9	GPIO5	LINE1_HL1R	in/out	opt GPIO / HANDSET to Line 1 relay control (out)
8	GPIO4	LINE1_PULSE	in/out	opt GPIO / Line 1 pulse dial (out)
7	GPIO3	LINE1_LCS	in	Loop Current Sense Line 1
6	GPIO2	LINE1_CID	out	Caller ID path enable Line 1
5	GPIO1	LINE1_RI	in	Ring Detect Line 1
4	GPIO0	LINE1_OH	out	Off Hook Line 1
1-3		Vendor rsrvd		vendor optional
0		GPIO_INT		GPIO_INT (uses same logic as wakeup event)

AC 97 2.0 makes no requirement on the number of GPIOs or their use, only that they be implemented as general purpose. Recommended bit definitions are provided for maximum interoperability, and should be followed wherever possible. The **STAC9705** only implements GPIO0 through GPIO11

The suggested use for the International Bits 1-3 is to implement LINE12_AC, LINE12_DC, and LINE12_RS, which, when set to one, adjust the DAA AC impedance, DC impedance, and Ring Detect sensitivity to alternate values more suitable for some non-North American countries. These outputs have effect on both Line 1 and Line 2 (i.e., it is assumed that both DAAs reside in the same country).

Outputs LINE1_PULSE and LINE2_PULSE control pulse dial relays, separate from the Off Hook relays, used in DAAs for some non-North American DAAs.

GPIO_INT has been added to leverage the logic that has already been implemented within the codec to detect a change in GPIO input state and trigger a wake up event. When the codec is NOT in powerdown mode any input

GPIO change can be enabled by the wake up mask to generate GPIO_INT=1 to indicate to the controller or driver that GPIO state has changed and should be updated in memory. The controller acknowledges and clears a wakeup event or GPIO_INT by writing a "0" to the corresponding bit in register 54h. This supports shadowing of codec registers in memory by potentially eliminating polling.

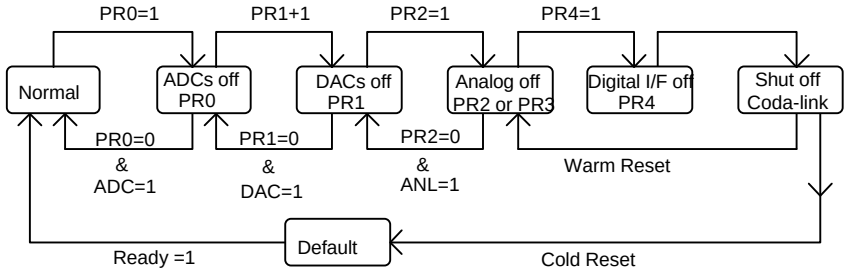
6. LOW POWER MODES

The **STAC9705** is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 7 commands of separate power down. See the table below for the different modes.

Table 18: Low Power Modes

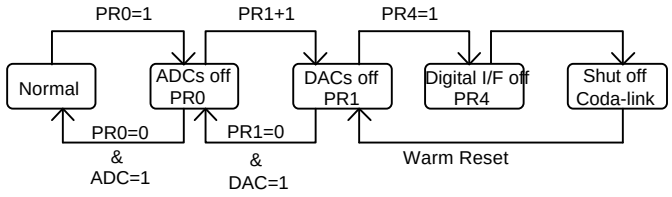
GRP BITS	FUNCTION
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (Vref still on)
PR3	Analog Mixer powerdown (Vref off)
PR4	Digital Interface (AC-link) powerdown (extnl clk off)
PR5	Internal Clk disable
PR6	Not implemented

Figure 13: Example of **STAC9705** Powerdown/Powerup flow



The above figure illustrates one example procedure to do a complete powerdown of **STAC9705**. From normal operation, sequential writes to the Powerdown Register are performed to power down **STAC9705** a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC-link. The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC 97 controller will send pulse on the sync line issuing a warm reset. This will restart AC-link (resetting PR4 to zero). The **STAC9705** can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers as a cold reset will reset them to their default states. When a section is powered back on, the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (stable) before attempting any operation that requires it.

Figure 14: STAC9705 Powerdown/Powerup flow with analog still alive



The above figure illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINE_IN source) through **STAC9705** to the speakers but have most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

6.1. Modem AFE Wake up and Power Management Event (PME#) Support

Ring and handset offhook detect are examples of events that might need to wake up a PC which has suspended into a low power state. Wake up on an audio event could eventually become practical.

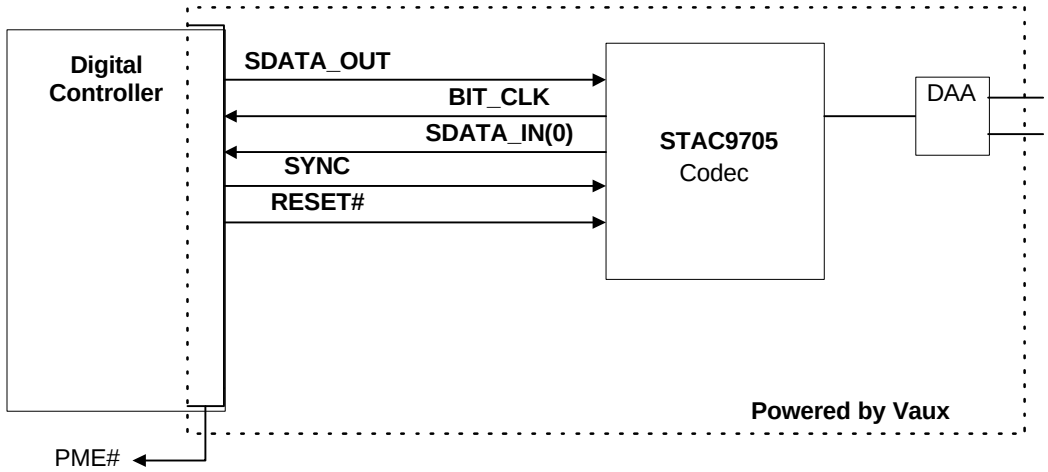
Revision 1.x AC 97 architecture enables fine granular power management of the AC-link and the individual subfunctions within the codec. However it does not support system wake requests triggered by external events. Power management, or wake, event support for a modem is a key feature of the 1998 Power Managed PC architecture and must be fully comprehended by the Extended AC 97 architecture. Support for wakeup must be comprehended for various configurations of AC 97 and AMC ‘97, be they single codec, or split partitioned primary/secondary codec implementations.

The 1998 Power Managed PC architecture specifies a Vaux supply that is designed to support specific “always active” functions while the majority of the PC is powered down. 5.0 V *and* 3.3 V Vaux supplies are available on the motherboard, and a 3.3 V Vaux supply pin is currently being added to the PCI slot definition. The cleanliness of the Vaux supply will depend on the power supply source.

6.1.1. Combined Audio/Modem AFE Codec (AMC '97)

For the **STAC9705** combined Audio/Modem AFE, the codec, AC-link and portions of the DC '97 controller all must be powered by Vaux as illustrated below:

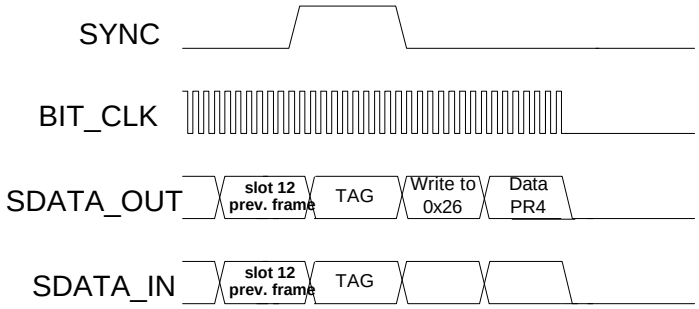
Figure 15. Combined Audio / Modem AFE Auxiliary Power Distribution



The codec and AC-link are programmed to a low power state (see Figure 16) and, upon detection of a power management event, are brought back to the active state by executing a warm reset sequence as detailed in Figure 17.

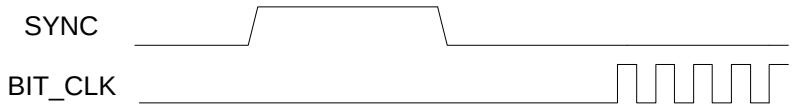
Figure 16 shows the DC '97 controller placing the AC-link into its lowest power state by programming the codec's Powerdown Control/Status register with bit(12) = 1 (PR4) .

Figure 16. AC-link Low Power Mode



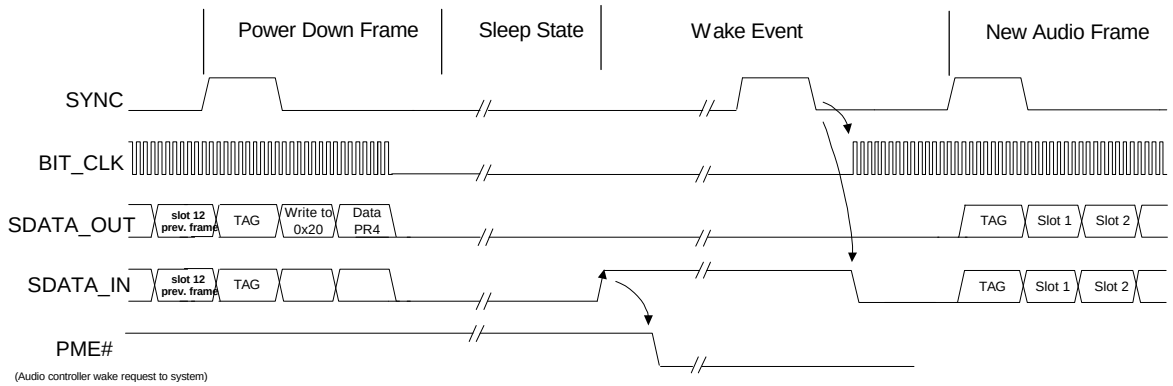
In response to this command BIT_CLK and SDATA_IN codec, and SDATA_OUT controller outputs go low and stay low .
AC-link when programmed to its low power mode, can only be reactivated by the device driver which can write to a DC '97 controller register causing it to signal a cold or warm reset on the AC-link. A warm reset, which will not alter the current AC 97 registers, is signaled by driving SYNC high for a minimum of 1uS in the absence of BIT_CLK.
Within normal audio frames SYNC is a synchronous codec input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used to signal a warm reset to the AC 97 codec.

Figure 17 AC-link Warm Reset



In an AMC'97 implementation, where the **STAC9705** codec and AC-link are both completely powered by Vaux, an enabled power management event detected at the modem interface causes the assertion of the PME# signal to the system. PME# assertion causes the system to resume so that the modem event can be serviced. The first thing that the device driver must do to reestablish communications with the codec is to command the DC'98 to execute a warm reset to the AC-link. The entire sequence is illustrated in Figure 18 below.

Figure 18. AC link Power down/up Sequence



The rising edge of SDATA_IN causes the DC '97 controller to assert its PME# to the system's ACPI controller. The AMC '97 codec must keep SDATA_IN high until it has sampled SYNC having gone high, and then low. PME# is cleared out in the DC '97 controller by system software, asynchronous to AC-link activity. The DC '97 controller must always monitor the codec's ready bit before sending data to it.

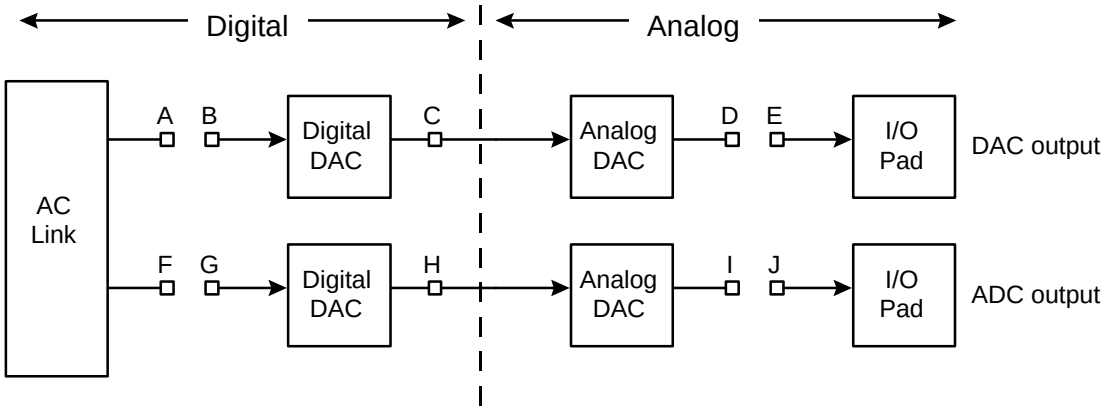
7. LOOPBACK MODES FOR TESTING

In Local Analog Loopback mode, the analog output from the DAC is connected to the analog input of the associated ADC. The DAC output pin(s) are muted and the ADC input pin(s) are ignored. In Remote Analog Loopback mode, The ADC input pin(s) are connected to the DAC pin(s) in addition to the ADC input. The DAC output is ignored.

Table 19. Modem Loopback Control Bit Definitions

Bit	Name	Function
2-0	L1B2-L1B0	Modem Line 1 Loop back enable 000 = Disabled (default) 001 = ADC Loop back 010 = Local Analog Loop back 011 = DAC Loop back 100 = Remote Analog Loop back 101 -111 = vendor optional
10-4		Modem Line 2 and Handset Loop back enable not supported in the **STAC9705**

Figure 19. Loopback Points



ADC LOOP BACK '001'
The ADC loop back takes the line input signal to the ADC and routes it back to the Line output. This loop includes the analog functions in the receive and transmit path.

LOCAL ANALOG LOOP BACK '010'
The appropriate outgoing slot of the AC-link is passed through the DAC and the analog filters, looped back through the ADC, then onto the appropriate incoming stream slot of the AC-link. This is commonly used in modem modes to troubleshoot problems.

DAC LOOP BACK '011'
This digital test loops back the digital transmit path (outgoing stream) to the digital receive path (incoming stream).

REMOTE ANALOG LOOP BACK '100'
The Line input signal is routed back to the Line output. This loop includes the analog receive functions, but no ADC or DAC.

8. TESTABILITY

The **STAC9705** has two test modes. One is for ATE in-circuit test and the other is restricted for ***SigmaTel's*** internal use. **STAC9705** enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. Once in the ATE test mode, the digital AC-link outputs (BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in-circuit testing of the AC 97 controller. This case will never occur during standard operating conditions.

9 AC TIMING CHARACTERISTICS

($T_{ambient}$ = 25 deg C, AVdd = DVdd = 5.0V or 3.3V +/- 10%, AVss=DVss+0V; 50pF external load)

9.1 Cold Reset

Figure 20: Cold Reset

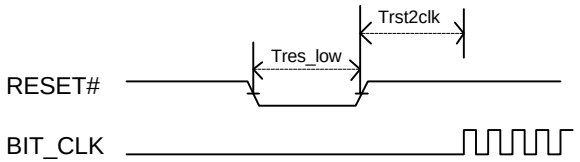


Table 20 : Cold Reset

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RESET# active low pulse width	Tres_low	1.0	-	-	us
RESET# inactive to BIT_CLK startup delay	Trst2clk	162.8	-	-	ns

# denotes active low.

9.2 Warm Reset

Figure 21: Warm Reset

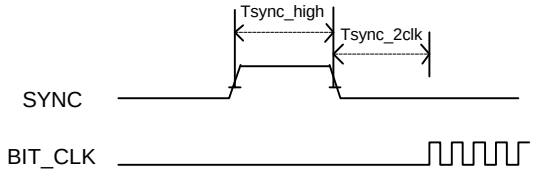


Table 21: Warm Reset

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SYNC active high pulse width	Tsync_high	-	1.3	-	us
SYNC inactive to BIT_CLK startup delay	Tsync2clk	162.8	-	-	ns

9.3 Clocks

Figure 22: Clocks

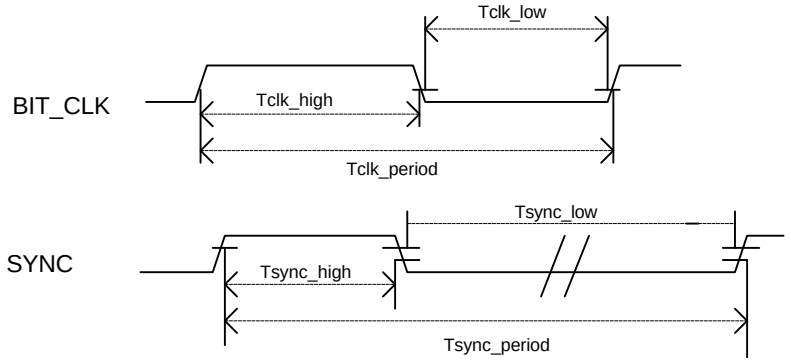


Table 22: Clocks

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BLT_CLK high pulsewidth (note 1)	Tclk_high	32.56	40.7	48.84	ns
BIT_CLK low pulse width (note 1)	Tclk_low	32.56	40.7	48.84	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	Tsync_period	-	20.8	-	us
SYNC high pulse width	Tsync_high	-	1.3	-	us
SYNC low_pulse width	Tsync_low	-	19.5	-	us

Notes: 1) Worst case duty cycle restricted to 40/60.

9.4 Data Setup and Hold (50pF external load)

Figure 23: Data Setup and Hold

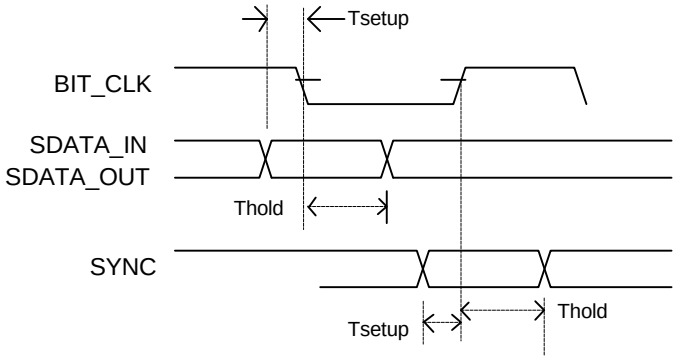


Table 23: Data Setup and Hold

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup to falling edge of BIT_CLK	Tsetup	15.0	-	-	ns
Hold from falling edge of BIT_CLK	Thold	5.0	-	-	ns

Note 1: Setup and hold time parameters for SDATA_IN are with respect to the AC 97 controller.

9.5 Signal Rise and Fall Times - (50pF external load; from 10% to 90% of Vdd)

Figure 24: Signal Rise and Fall Times

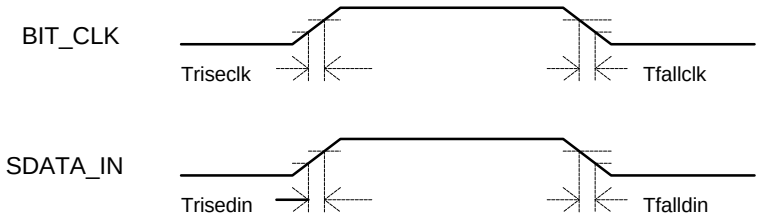


Table 24: Signal Rise and Fall Times

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
BIT_CLK rise time	Triseclk	2	-	6	ns
BIT_CLK fall time	Tfallclk	2	-	6	ns
SDATA_IN rise time	Trisedin	2	-	6	ns
SDATA_IN fall time	Tfalldin	2	-	6	ns

9.6 AC-link Low Power Mode Timing

Figure 25: AC-link Low Power Mode Timing

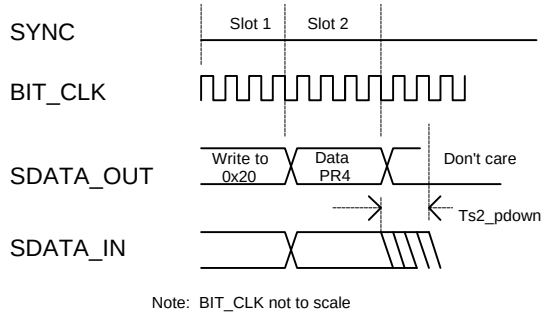


Table 25: AC-link Low Power Mode Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	us

9.7 ATE Test Mode

Figure 26: ATE Test Mode

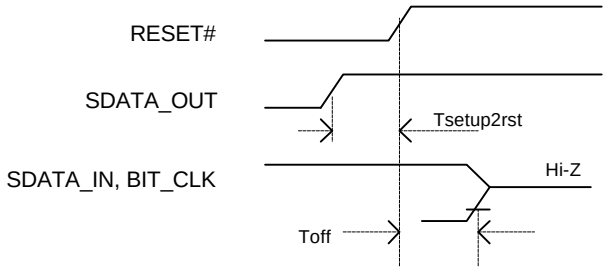


Table 26: ATE Test Mode

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup to trailing edge of RESET# (also applies to SYNC)	Toff	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

Notes:

1. All AC-link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes **STAC9705**'s AC-link outputs to go high impedance which is suitable for ATE in circuit testing.
2. Once either of the two test modes have been entered, the **STAC9705** must be issued another RESET# with all AC-link signals low to return to the normal operating mode.

 # denotes active low.

10. ELECTRICAL SPECIFICATIONS:

10.1 Absolute Maximum Ratings:

Voltage on any pin relative to Ground	-0.3V TO +6.0V
Operating Temperature	0^{o} TO 70^{o} C
Storage Temperature	-55^{o} TO $+125^{o}$ C
Soldering Temperature	260^{o} C FOR 10 SECONDS
Output Current per Pin	+/- 4 mA except Vrefout = +/- 5mA

10.2 Recommended Operating Conditions

Table 27. Operating Conditions

PARAMETER		MIN	TYP	MAX	UNITS
Power Supplies	+ 3.3v Digital	3.0	3.3	3.6	V
	+ 5v Digital	4.5	5	5.5	V
	+ 5v Analog	4.5	5	5.5	V
Ambient Temperature		0	-	70	^{O}C

10.3 Power Consumption

Table 28. Power Consumption

PARAMETER		MIN	TYP	MAX	UNITS
Digital Suppy Current	+ 5V Digital		TBD		mA
	+ 3.3v Digital		TBD		mA
Analog Supply Current	+ 5v Analog		TBD		mA
Power Down Status					
PR0 +5v Analog Supply Current			TBD		mA
PR1 +5v Analog Supply Current			TBD		mA
PR2 +5v Analog Supply Current			TBD		mA
PR3 +5v Analog Supply Current			TBD		mA
PR4 +3.3v Digital Supply Current			TBD		mA
PR5 +3.3v Digital Supply Current			TBD		mA
PR4 +5v Digital Supply Current			TBD		mA
PR5 +5v Digital Supply Current			TBD		mA

10.4 AC-link Static Digital Specifications

($T_{ambient}$ = 25 deg C, DVdd = 5.0V or 3.3V +/- 10%, AVss=DVss+0V; 50pF external load)

Table 29. AC-link Static Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Voltage Range	Vin	-0.30		DVdd + 0.30	V
Low level input range	Vil	-	-	0.30xDVdd	V
High level input voltage	Vih	0.40xDVdd	-	-	V
High level output voltage	Voh	0.50xDVdd	-	-	V
Low level output voltage	Vol	-	-		V
Input Leakage Current (AC-link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z'd AC-link outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	4		mA

10.5 STAC9705 Analog Performance Characteristics

($T_{ambient}$ = 25 deg C, AVdd = DVdd = 5.0V +/- 10%, AVss=DVss+0V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 Vrms, 10K ohm/ 50pF load, Testbench Characterization BW: 20 Hz – 20KHz, 0dB settings on all gain stages**)**

Table 30. Analog Performance Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage:				
Line Inputs	-	1.0	-	Vrms
Modem Input (Differential)	-	1.0	-	
Mic Inputs[1]	-	0.1	-	
Full Scale Output Voltage:				
Line Output	-	1.0	-	Vrms
Modem Output (Differential)	-	1.0	-	
Analog S/N:				
CD to LINE_OUT	90	95	-	dB
Other to LINE_OUT	-	95	-	
Analog Frequency Response[2]	20	-	20,000	Hz
Digital S/N[3]				
Audio D/A	85	95	-	dB
Audio A/D	75	88	-	
Modem D/A	85	98	-	
Modem A/D	80	85	-	
Total Harmonic Distortion:				
Line Output[4]	-	-	0.02	%
D/A & A/D Frequency Response[5]	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection[6]	+85	-	–	dB
Out-of-Band Rejection[7]	-	+40	–	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1KHz)	-	+40	–	dB
Crosstalk between Input channels	-	-	-70	dB
Spurious Tone Rejection	-	+100	–	dB

Attenuation, Gain Step Size	-	1.5	–	dB
Input Impedance	10	-	–	K Ohm
Input Capacitance	-	15	–	pF
Vrefout	-	0.41 x AVdd	–	V
Interchannel Gain Mismatch ADC			0.5	dB
Interchannel Gain Mismatch DAC		-	0.5	dB
Gain Drift		100		ppm/deg. C
DAC Offset Voltage		10	50	mV
Deviation from Linear Phase			1	degree
External Load Impedance	10			K ohm
Mute Attenuation (Vrms input)	90	96		dB

Notes:

1. With +20 dB Boost on, 1.0Vrms with Boost off
2. +/- 1 dB limits
3. The ratio of the rms output level with 1 KHz full scale input to the rms output level with all zeros into the digital input. Measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
4. 0 dB gain, 20 KHz BW, 48 KHz Sample Frequency
5. +/-0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

For more information, please contact:

SigmaTel, Inc.
6101 W. Courtyard Dr., Bldg. 1, Suite 100
Austin, Texas 78730
Tel (512) 343-6636 Ext. 11 Fax (512) 343-6199
email: alyman@sigmatel.com
Homepage: www.ccsi.com/~sigmatel