Codex 6030/6040 Series Intelligent Network Processor

Technical Manual

Reprinted August 1981

PROPRIETARY MATERIAL

PREFACE

This manual is directed to Codex overseas distributors, to Codex personnel, and to end users who will maintain their own systems.

It describes the 6030/6040 series INP's and tells how they process data. It gives diagnostics for detecting and identifying system failures and pinpointing the boards that are the cause of the failures, so that they may be replaced. In addition to on-site installation, the manual also identifies the causes of applications-oriented problems and recommends some corrective steps.

Appendixes contain collateral and reference material.

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part I5 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

06888

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont)

TABLE OF CONTENTS (Cont)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont)

LIST OF ILLUSTRATIONS (Cont)

LIST OF ILLUSTRATIONS (Cont)

LIST OF TABLES

LIST OF TABLES (Cont)

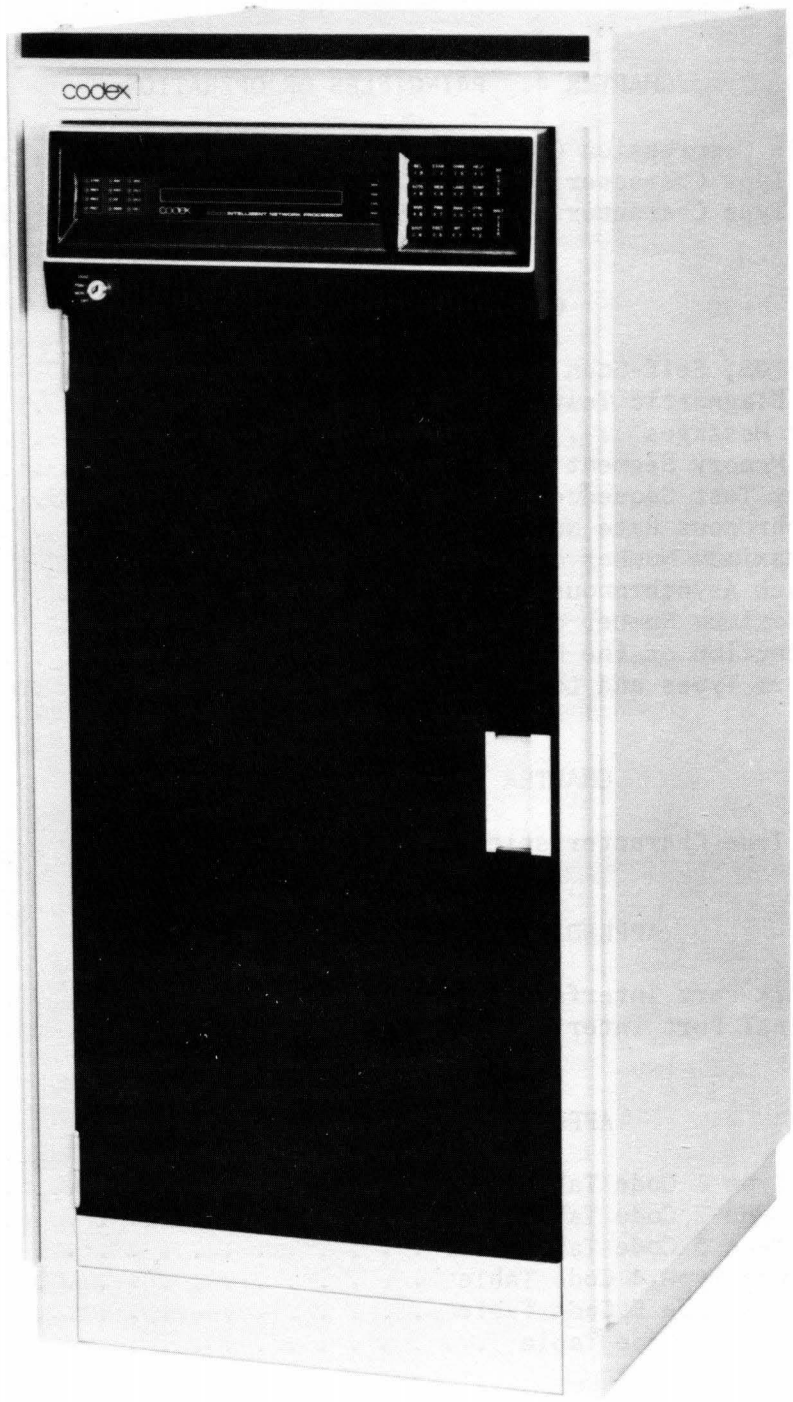


Figure 1-1. Codex Intelligent Network Processor

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW OF THE INP

The 6030/6040 Intelligent Network Processor (INP)™ shown in Figure 1-1, is a multi-microprocessor communications network controller. Essentially, the INP is a transparent communications system which can provide a point-to-point connection between any two ports on a two-node or multinode network. It makes use of statistical multiplexing and data compression to provide high bandwidth utilization on the network links. It guarantees error-free data between nodes by using a go-back-n ARQ scheme.

The INP also provides many other features, including:

- Autospeed recognition
- Statistics on network operation
- Real-time monitoring of critical functions and parameters
- Network control from either a control panel or a control terminal port
- Data compression
- Offline diagnostics of hardware functions

Tables 1-1 and 1-2 list the main features of all models of the 6030 and 6040 INP's. The options available with the 6030/6040 INP's are listed in Appendix B.

In its minimal (6030) configuration, an INP operates as a point-to-point system. This configuration is shown in general form in Figure 1-2. At each node the 6030 appears as a data communication equipment (DCE). Thus configured, the INP will pass both data and control signals transparently.

Data is received from the local terminals, processed within the node, and assembled into a message frame which is transmitted via the link to the adjacent node. This node receives the frame, disassembles it, verifies error-free transmission, and outputs the data to the destination terminal ports or CPU.

In a multinode (6040) version shown in Figure 1-3, some of the data from the frame may be processed and reassembled into another frame at an intermediate node for retransmission to a third node via a different network link.

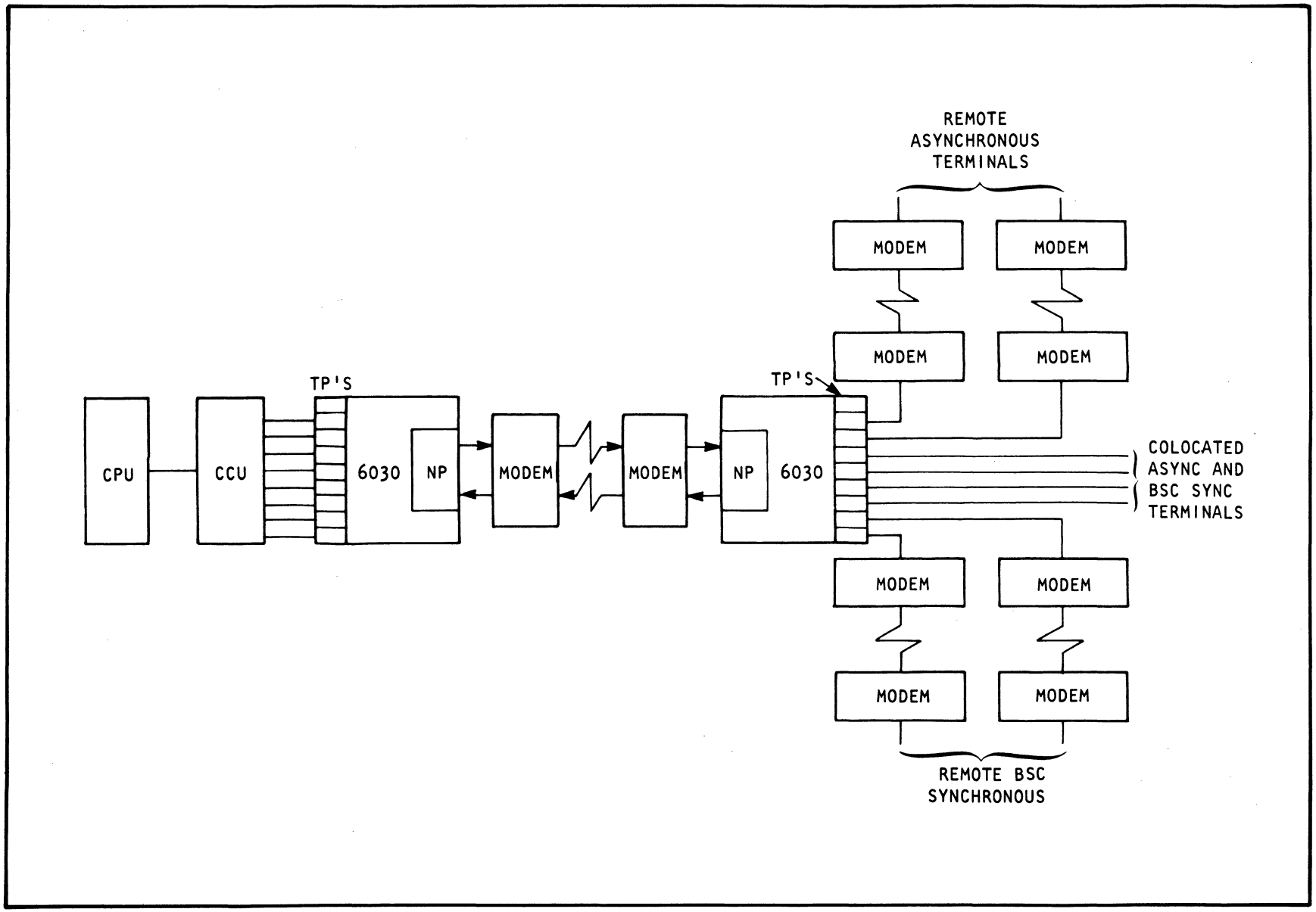


Figure 1-2. Codex 6030 Point-to-Point Configuration

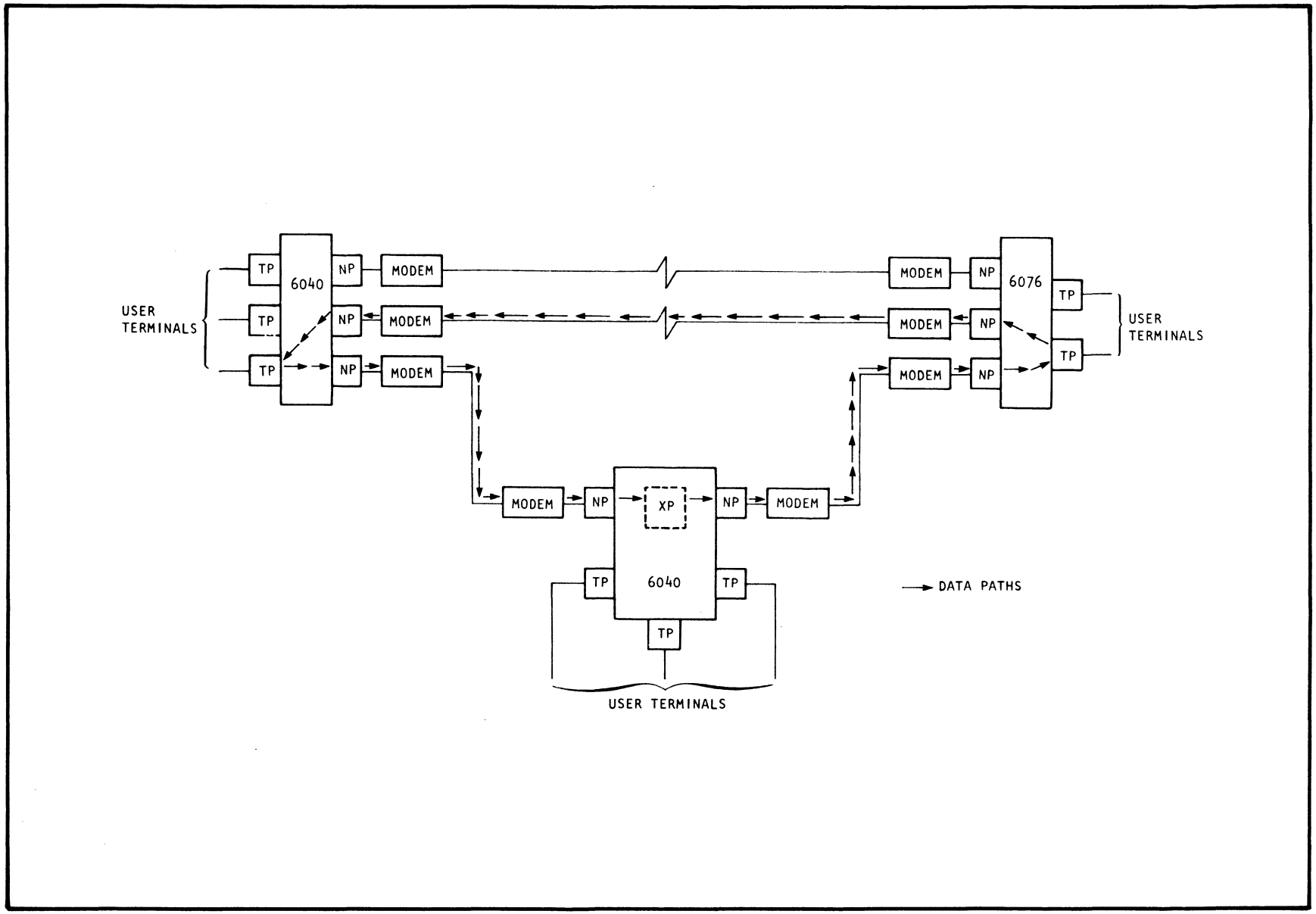


Figure 1-3. Codex 6040 Multinode System Configuration

TABLE 1-1. FEATURES OF 6030 SERIES INP's

Model	Feature
6030	Basic 6000 Intelligent Network Processor, tabletop enclosure with integral port nest. Includes buffer RAM and one nonvolatile configuration memory module for up to 28 ports (14 port modules).
6031	Basic 6000 Intelligent Network Processor, rack-mountable with one port nest. Includes buffer RAM and one nonvolatile configuration memory module for up to 28 ports (14 port modules).
6032	Basic 6000 Intelligent Network Processor, rack-mountable with two port nests. Includes buffer RAM and two nonvolatile configuration memory modules for up to 60 ports (30 port modules).
6033	Basic 6000 Intelligent Network Processor, rack-mountable with three port nests. Includes buffer RAM and three nonvolatile configuration memory modules for up to 92 ports (46 port modules).
6034	Basic 6000 Intelligent Network Processor, rack-mountable with four port nests. Includes buffer RAM and four nonvolatile configuration memory modules for up to 124 ports (62 port modules).

TABLE 1-2. FEATURES OF 6040 SERIES INP's

Model	Feature
6040	Basic 6000 Intelligent Network Processor, tabletop enclosure with integral port nest. Includes buffer RAM and nonvolatile configuration memory for up to 24 ports (12 port modules).
6041	Basic 6000 Intelligent Network Processor, rack-mountable with one port nest. Includes buffer RAM and nonvolatile configuration memory for up to 24 ports (12 port modules).
6042	Basic 6000 Intelligent Network Processor, rack-mountable with two port nests. Includes buffer RAM and nonvolatile configuration memory for up to 56 ports (28 port modules).
6043	Basic 6000 Intelligent Network Processor, rack-mountable with three port nests. Includes buffer RAM and nonvolatile configuration memory for up to 88 ports (44 port modules).
6044	Basic 6000 Intelligent Network Processor, rack-mountable with four port nests. Includes buffer RAM and nonvolatile configuration memory for up to 120 ports (60 port modules).
6045	Basic 6000 Intelligent Network Processor, rack-mountable with five port nests. Includes buffer RAM and nonvolatile configuration memory for up to 152 ports (76 port modules).

TABLE 1-2. FEATURES OF 6040 SERIES INP's (Cont)

Model	Feature
6046	Basic 6000 Intelligent Network Processor, rack-mountable with six port nests. Includes buffer RAM and nonvolatile configuration memory for up to 184 ports (92 port modules).
6047	Basic 6000 Intelligent Network Processor, rack-mountable with seven port nests. Includes buffer RAM and nonvolatile configuration memory for up to 216 ports (108 port modules).
6048	Basic 6000 Intelligent Network Processor, rack-mountable with eight port nests. Includes buffer RAM and nonvolatile configuration memory for up to 248 ports (124 port modules).

The logical communication paths between terminals and the communications control unit of a CPU constitutes the network topology. This topology is stored independently at each node, in a nonvolatile configuration memory (CMEM). The topology is defined by programming (loading) the memory via an operator's console or a control terminal port (CTP).

Like a TDM, the INP provides user transparency: that is, the remote terminal and the central processor unit (CPU) of the host computer communicate with each other "directly," just as though INP's were not present. End-to-end delay is minimal. Use of a 6030 or 6040 INP does not require modifying either hardware or software of the user's existing system.

What distinguishes the INP from a conventional TDM is its ability to provide higher throughput efficiency and error-free data transmission. The primary method used to achieve high throughput efficiency is statistical multiplexing. A typical TDM allocates a fixed portion of the high speed link's time to each port. If there is no data for this port to send, its portion of the time is unused. In contrast, the INP allocates the time dynamically. If a particular port has no data to transmit, a short place-holding character is sent for it and its unused time is assigned to the next port that does have data.

A second method that achieves throughput efficiency is data compression. To minimize the number of bits to be transmitted over a data link, the data is compressed by use of variable-length codes for characters and by bit-stripping.

Variable-length coding offers a significant improvement in compression. Short codes are used to represent frequently-used characters such as e, t, and space, and longer codes for the less frequent characters such as z and @. If a code of uniform length (8 bits, for example) is used for all characters, compression is not achieved. But the substitution of variable-length codes results in a saving of roughly 30 percent in the bit count. Even though the maximum number of bits in a code may be 14, the average is still only 6 bits. This method of data compression was developed in 1952 by D.A. Huffman. The Huffman method for constructing a code is described in simple form in Chapter 4.

Bit-stripping is the method commonly used by multiplexers. It consists of removing overhead information: start, stop, and parity bits from asynchronous data, and the idle and filler bits from BSC data.

Code conversion is also possible as a result of the data compression. Since the data must be converted back from its variable length code set to a fixed-length character code, the conversion may be performed simply by providing a table to be used for decoding into the new character set. Chapter 4 shows standard codes.

1.2 SPECIFICATIONS AND PHYSICAL CHARACTERISTICS

1.2.1 PERFORMANCE SPECIFICATIONS

The overall efficiency provided by the INP is dependent upon its specific application. The improvement in throughput offered by statistical multiplexing typically ranges from a factor of 2 to 4 over TDM efficiencies. Data compression will offer an additional improvement in throughput in the range of a factor of 1.2 to 1.5.

Since the 6000 node-to-node protocol utilizes variable-length frames, the node-to-node delay introduced by the 6000 will vary. For most applications it will be in the 35-50 ms range.

1.2.1.1 CLOCK ACCURACY. A 6030 or 6040:

a. Accepts clocks accurate to ±.10%.
b. Provides clocks accurate to ±.05%.

1.2.2 PHYSICAL SPECIFICATIONS

a. Environmental

Temperature: 0-50°C (32-122°F).

Relative Humidity: 0-95% (without condensation).

Altitude: 0-10,000 ft. (0-3 km).

b. Power Requirements

115/230 Vac ±10%.

47 to 63 Hz.

c. Terminal and Network Port Connectors

Cannon or Cinch DB-19604-43 or equivalent (25-pin).

d. Port Nest Space Availability and Allocation

First nest - 12 or 14 card slots.

Second through eighth nest - 16 card slots each.

One terminal port module provides interfaces for two terminals and occupies one card slot. Any of three types of terminal ports may be used.

One 6140 Network Port Module provides an additional trunk and occupies two card slots.

1.2.3 6030 DIMENSIONS AND WEIGHTS

	Width	Height	Length	Weight
6030	19" 48 cm	7" 18 cm	26" 66 cm	50 lbs 23 kg
6031	19" 48 cm	19"* 48 cm	19" 48 cm	50 lbs 23 kg
6032	19" 48 cm	30"* 76 cm	25" 64 cm	68 lbs 31 kg
6033	19" 48 cm	41"* 104 cm	25" 64 cm	76 lbs 35 kg
6034	19" 48 cm	52"* 132 cm	25" 64 cm	94 lbs 43 kg

*Overall vertical mounting space required.

1.2.4 6040 DIMENSIONS AND WEIGHTS

	Width	Height	Length	Weight
6040	19" 48 cm	7" 18 cm	26" 66 cm	50 lbs 23 kg
6041	19" 48 cm	19"* 48 cm	19" 48 cm	50 lbs 23 kg
6042	19" 48 cm	30"* 76 cm	25" 64 cm	68 lbs 31 kg
6043	19" 48 cm	41"* 104 cm	25" 64 cm	86 lbs 39 kg
6044	19" 48 cm	52"* 132 cm	25" 64 cm	94 lbs 43 kg
6045	19" 48 cm	63"* 160 cm	25" 64 cm	112 lbs 51 kg
6046	19" 48 cm	74"* 188 cm	25" 64 cm	120 lbs 55 kg
6047	19" 48 cm	85"* 216 cm	25" 64 cm	138 lbs 63 kg
6048	19" 48 cm	96"* 244 cm	25" 64 cm	146 lbs 67 kg

*Overall vertical mounting space required.

1.2.5 6030 POWER CONSUMPTION

6030	3.5 amps at 115 Vac, 2 amps at 220 Vac
6031	3.5 amps at 115 Vac, 2 amps at 220 Vac
6032	7.0 amps at 115 Vac, 4 amps at 220 Vac
6033	7.0 amps at 115 Vac, 4 amps at 220 Vac
6034	10.5 amps at 115 Vac, 6 amps at 220 Vac

1.2.6 6040 POWER CONSUMPTION

6040	3.5 amps at 115 Vac, 2 amps at 220 Vac
6041	3.5 amps at 115 Vac, 2 amps at 220 Vac
6042	7.0 amps at 115 Vac, 4 amps at 220 Vac
6043	10.5 amps at 115 Vac, 6 amps at 220 Vac
6044	10.5 amps at 115 Vac, 6 amps at 220 Vac
6045	14.0 amps at 115 Vac, 8 amps at 220 Vac
6046	14.0 amps at 115 Vac, 8 amps at 220 Vac
6047	17.5 amps at 115 Vac, 10 amps at 220 Vac
6048	17.5 amps at 115 Vac, 10 amps at 220 Vac

CHAPTER 2

HARDWARE DESCRIPTION

2.1 INTRODUCTION

A Codex 6030/6040 series Intelligent Network Processor, Figure 1-1, consists of an operator's console (or, alternately, a front panel), a mainframe, and one or more port nests, interconnected by an I/O bus, as diagrammed in Figure 2-1. Dc power for the logic and the EIA signals is furnished by one or more power supplies. Figure 2-2 shows the chassis of a rack-mounted 6031 INP with the major components identified. The console, mainframe, power supply, and port nest are mounted in one drawer of the rack, the port nest in another.

The 6030/6040 series INP's are modular in design. They offer a variety of options and capabilities that tailor them quite precisely to the needs of a given communication network. This modularity assures the customer of the services that are needed, but requires purchase of only the options that provide those services. If the system requirements change, the INP may be modified to match the new requirements.

Certain features are standard requirements, others are options. These options are classed as either hardware or firmware. In the following system description, the hardware components are described according to their physical locations in the INP.

2.2 OPERATOR'S CONSOLES AND FRONT PANEL

The operator's console is located on the face of the tabletop version of the INP, or in one of the top drawers of the face of any floor cabinet version (Figure 1-1). Every network must have at least one operator's console for configuring the network topology, monitoring system operation, gathering system operational statistics, and performing diagnostics of hardware operation. Only the operator's console can be used for performing diagnostics, although a control terminal port may perform the other operator's console functions.

If a 6030/6040 does not have an operator's console, it has instead a front panel, Figure 2-3, that contains an on/off POWER switch for the node, and a 50-pin connector.

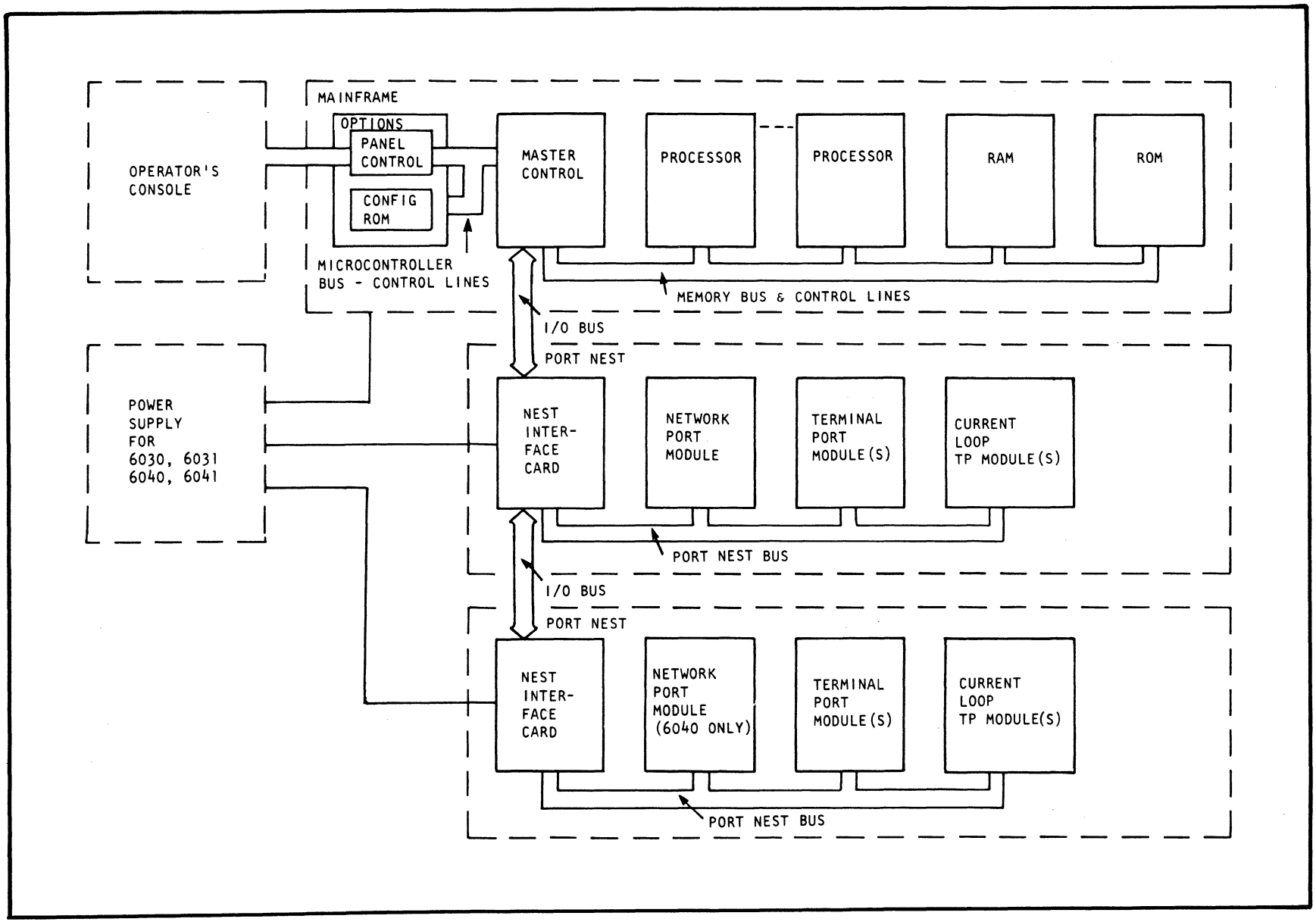


Figure 2-1. 6030/6040 Functional Block Diagram

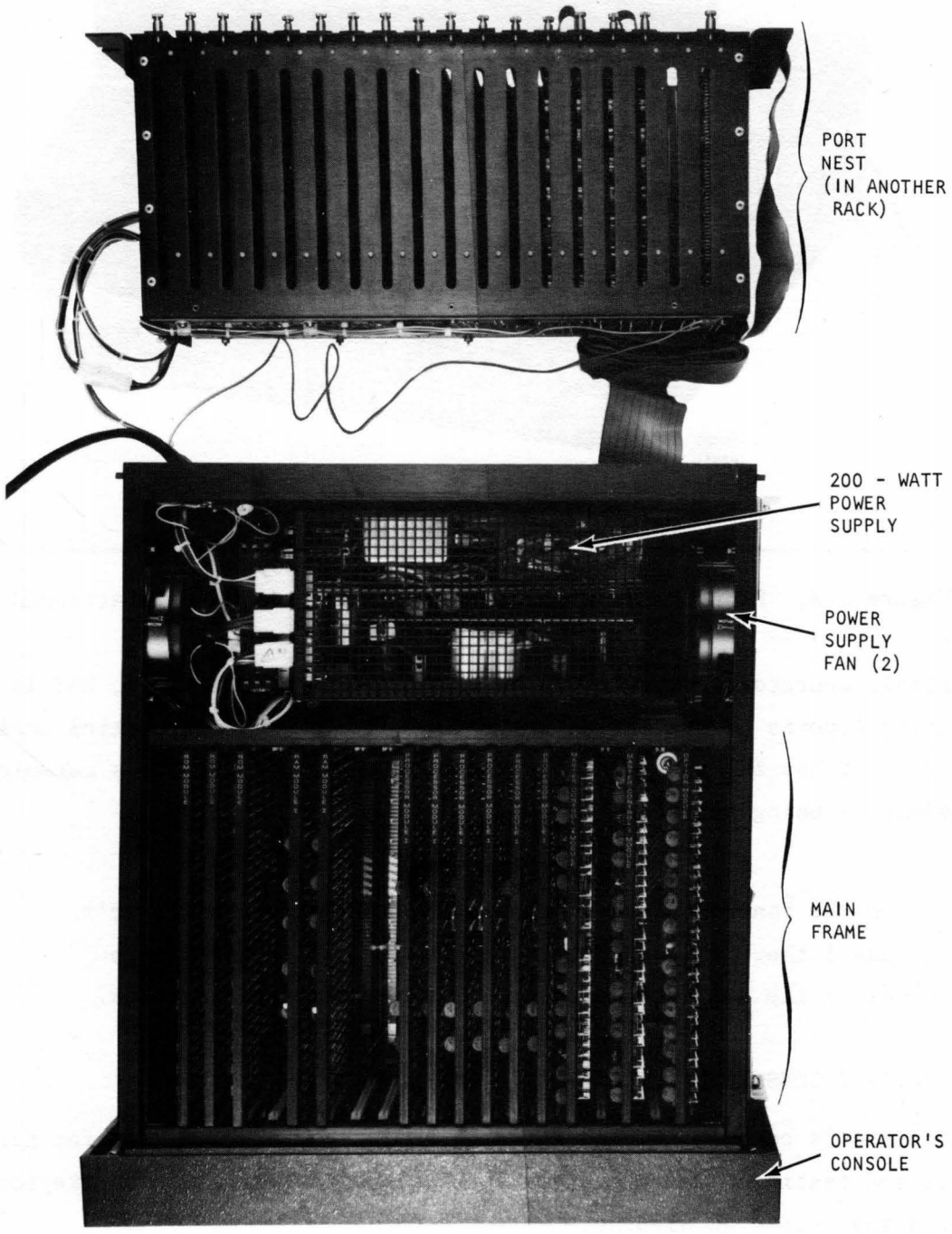


Figure 2-2. Chassis of Rack-Mounted 6031, Top View

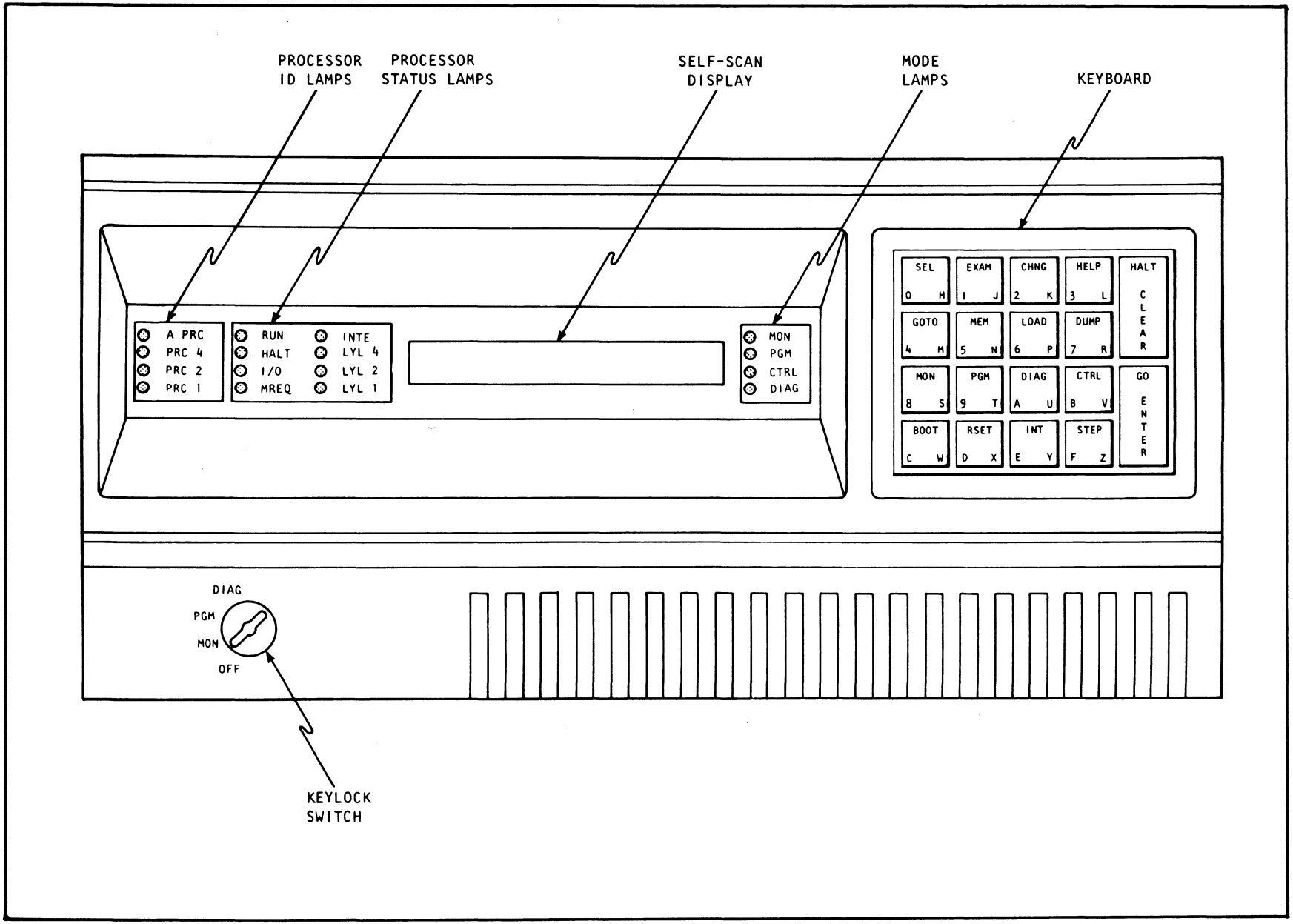


Figure 2-4. Codex 6030/6040 Series INP Operator Console

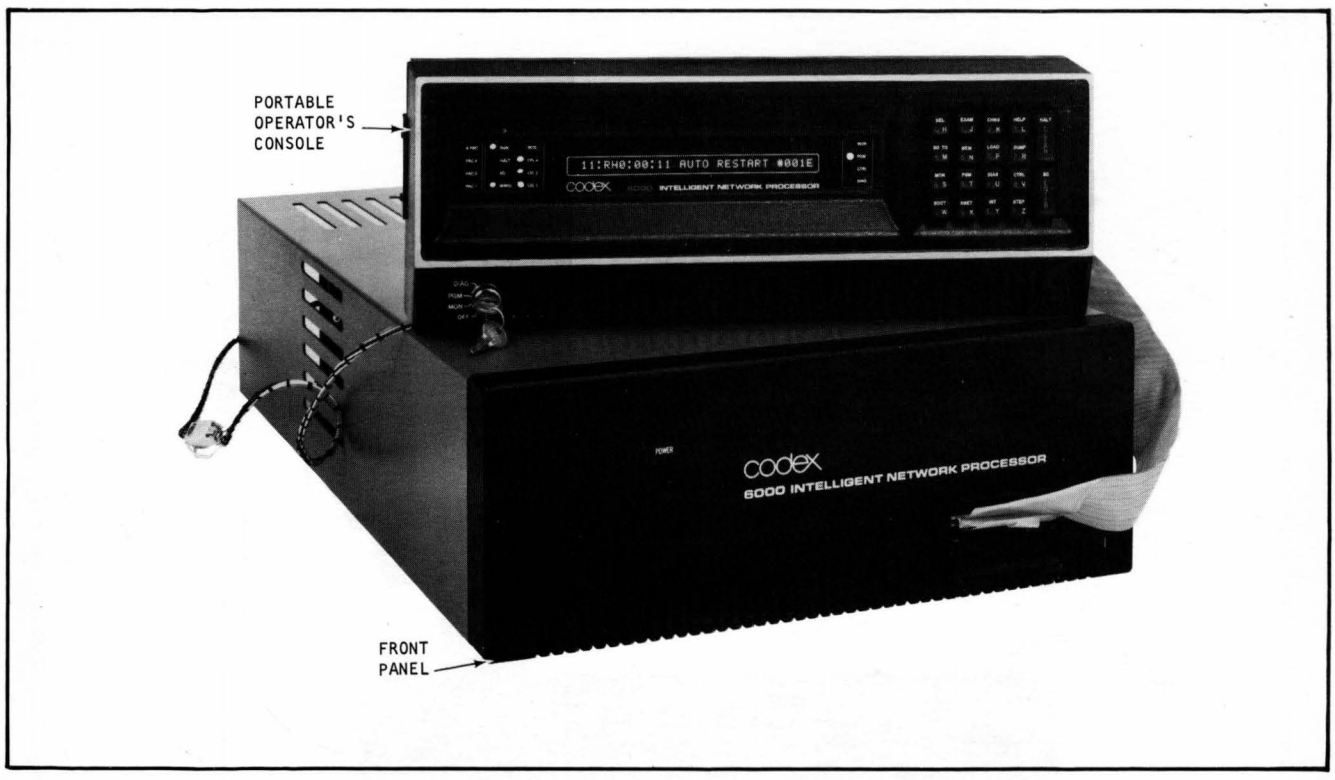


Figure 2-3. Front Panel with Portable Operator's Console Attached

A portable operator's console can be attached to the connector, and is used when operating reports or statistics are requested, or when diagnostics must be run for the node. It has the same controls and display as an operator's console, and differs mainly by being portable.

WARNING

On the inner surface of the logic card for the operator's panel there is a daughter card that supplies 250 Vdc to drive the self-scan display. This voltage is dangerous.

2.2.1 OPERATOR'S CONSOLE

The operator's console is used for programming and display, and for hardware diagnostics and testing. Operator inputs to the INP are made via the keyboard; outputs are via the self-scan display.

The face of an operator's console is shown in Figure 2-4. The console presents, from left to right, a row of processor ID lamps, two rows of processor status lamps, a 32-character 5x7 dot alphanumeric self-scan display, a row of operating mode

indicator lamps, and an 18-key keyboard. Below the processor ID lamps is a keylock power-function switch.

The functions of the controls and lamps are listed in Table 2-1.

The alphanumeric self-scan screen is used to display configuration information, commands, error conditions, and network statistics. (The small lights that form the characters are ionized gas, similar to neon tubes.) In Program and Monitor modes, character positions 2 through 6 of the self-scan screen continually display the currently-selected node number, configuration number, port type, and port number. This information may be displayed by the EXAM and CHNG commands. A sample format of this display is shown in Figure 2-5. Character position 1 contains an asterisk used to notify the operator when a system report is waiting to be displayed.

The remaining character positions (7 through 32) on the self-scan screen echo the input keystrokes for commands, and display error messages and the responses to commands.

NOTE

When a control terminal port (CTP) has been designated as the system report destination, messages or error reports are routed to the CTP; they are not displayed on the operator's console.

The keylock switch (see Figure 2-4) applies power to the INP and selects the mode of operation (these modes are described in the Operator Manual. The switch can be locked in any position by removing the key.

2.2.1.1 KEYBOARD. The keyboard consists of 18 pushbutton keys (see Figure 2-4). Each key has more than one function, depending upon the type of command being used, so each key has two or three different words or symbols printed on it. The keys are printed in this manner to provide many commands in a compact array.

In the lower left corner of each of the 16 square keys is a number or letter indicating the hexadecimal digits 0 to F. (See Figure 2-6.) Port numbers are in hexadecimal.

The mnemonic code key set consists of the alphabetic characters printed on the keys. (See Figure 2-7.) Note that the hexadecimal digits A through F double as alphabetic characters for the mnemonic code set. The character "O" doubles as the

TABLE 2-1. CONTROLS AND INDICATORS

Control/Indicator	Function
Processor ID Lamps	
A PRC lamp (green)	Indicates all processors in use.
PRC 4, PRC 2, PRC 1 lamps (yellow)	Indicates binary code of processor status being displayed.
Processor Status Lamps	
RUN lamp (green)	Indicates processor is running.
HALT lamp (red)	Indicates processor has halted.
I/O lamp (yellow)	Indicates input/output operation is in progress.
MREQ lamp (yellow)	Indicates memory request.
INTE lamp (green)	Indicates interrupt enabled.
LVL 4, LVL 2, LVL 1 lamps (yellow)	Indicates priority level in binary code.
Self-Scan Display	Displays alphanumeric data.
Mode Lamps	
MON lamp (green)	Indicates operator console is in monitor mode.
PGM lamp (yellow)	Indicates operator console is in program mode.
CTRL lamp (red)	Indicates operator console is in control mode.
DIAG lamp (red)	Indicates operator console is in diagnostic mode.
Keyboard	Used to enter commands (see paragraph 2.2.1.1).
Keylock Switch Position (See Figure 2-4)	
OFF	Shuts off power to system.
MON	Restricts operation to monitor mode only.
PGM	Allows only monitor, program, and control modes.
DIAG	Permits selection of any mode.

number "zero" and the letter "O," and the character "l" doubles as the number "one" and the letter "I."

The control character key set for monitor and program modes is shown in Figure 2-8(A). The additional control characters used for the control and diagnostic modes are shown in Figure 2-8(B).

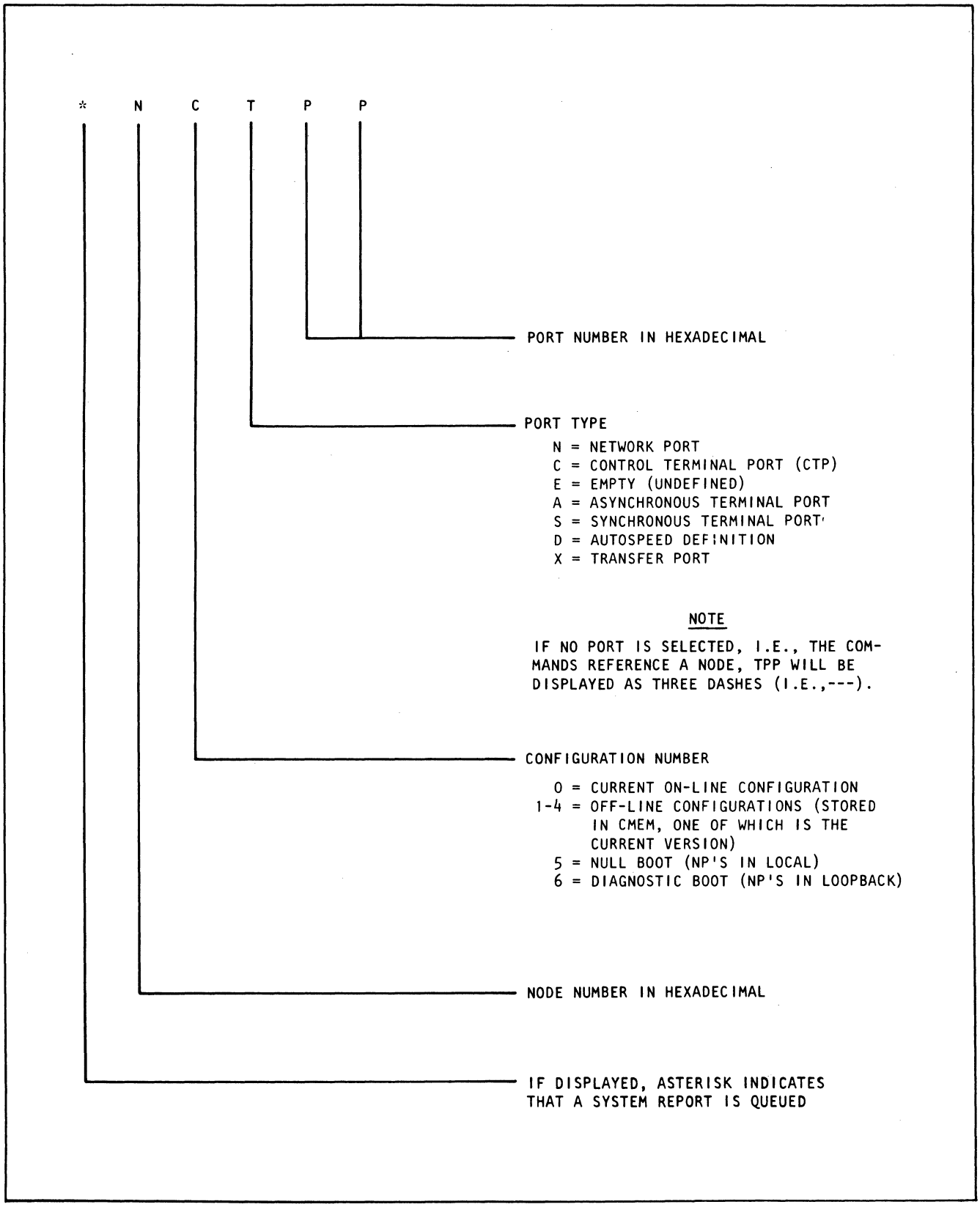


Figure 2-5. Display Format

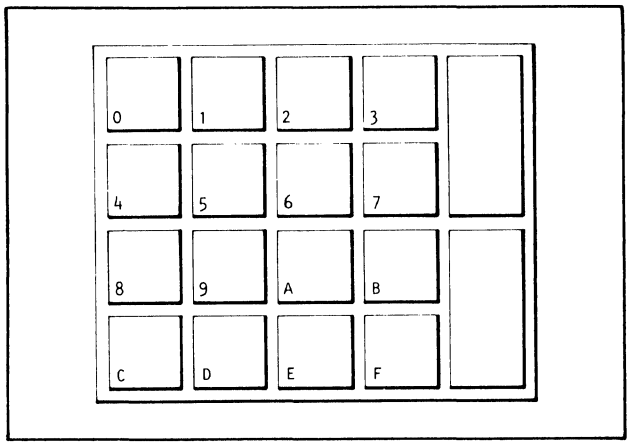


Figure 2-6. Hexadecimal Key Set

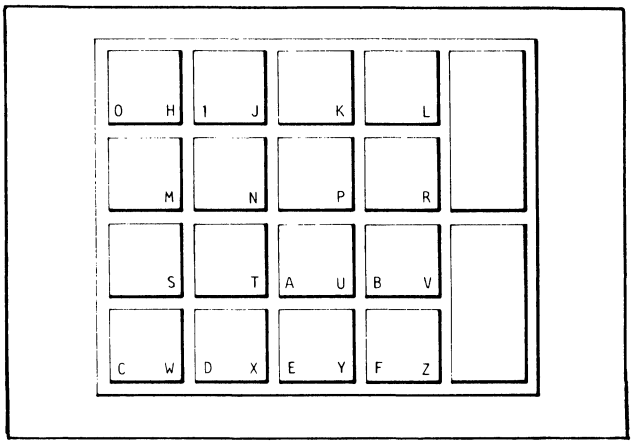


Figure 2-7. Mnemonic Code Set

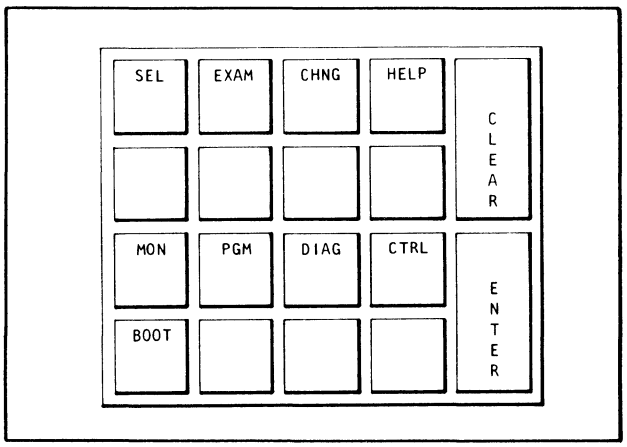


Figure 2-8(A). System Control Key Set, Monitor and Program Modes

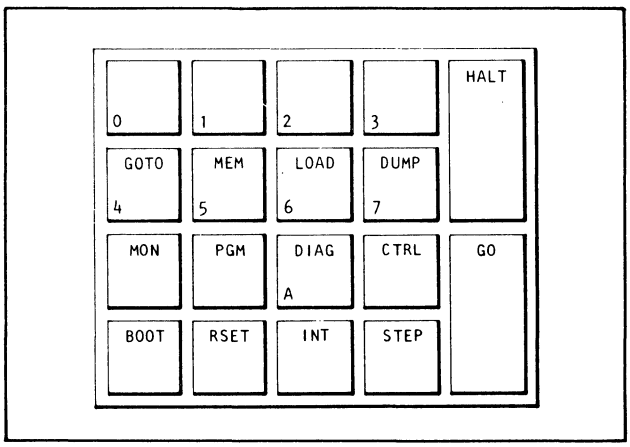


Figure 2-8(B). System Control Key Set, Control and Diagnostic Modes

2.2.2 FRONT PANEL

A front panel is used at a remote node that is usually unmanned. It can be used only to apply power to the node via an on/off POWER switch. A 50-pin connector allows attachment of a portable operator's console for test purposes (Figure 2-3).

2.2.3 PORTABLE OPERATOR'S CONSOLE

Since a front panel can be used only to power up a node, Codex Field Service Engineers carry a portable operator's console to give commands, query the system, and perform diagnostics at that node. This console is functionally the same as the

operator's console, and physically different only in that it is portable, with a protective rear cover. It is attached to the front panel 50-pin connector, with the power cord attached to power supply J2 or J3, as shown in Figure 2-3.

2.3 MAINFRAME

The mainframe, shown in Figure 2-9, is a card rack that is mounted directly behind the operator's console. It holds up to 17 circuit boards. These boards are of five types: an option module, 2 master control modules, up to 6 processor modules, and memory (ROM's and RAM's). They process data (processors), control operation of the system (master controllers), store software (ROM's) and configurations (RAM's), and contain the clocks to drive the logic and interfaces to other functional units of the INP. Master controller 1 (MC1) is the I/O controller. MC2 performs interface functions between MC1 and the processors and memories. The option card contains logic that interfaces the operator's console and the configuration memory with the MC1.

Logic diagrams for mainframe modules are shown in Appendix M.

The boards are edge-connected to the mainframe bus on a horizontal motherboard that is the floor of the mainframe. A 50-pin connector at the right rear edge of the motherboard terminates the I/O bus - a ribbon bus between the motherboard and the next interface card in the first port nest (see Figure 2-1).

A key on each edge connector on the motherboard allows only the correct type of module to be installed in each slot. The key engages a slot in the edge of the module.

2.3.1 MASTER CONTROLLER 1 (MC1)

MC1 performs the CPU functions for the master controller (see Figure 2-10). It contains the central processor (Intel 3000 series microcontroller), the firmware* program, local memory, and the pipeline registers, as well as the control and data interface for the port nest. It also contains the real-time clock and port clock generator. There is one MC1 per mainframe. The card rail of MC1's used with S49 software are marked "49."

*In the Codex INP's, "firmware" refers to the programmable ROM's on the MC1; they contain the programs for the Intel 3000 microcontroller. "Software" refers to the programs in the ROM cards.

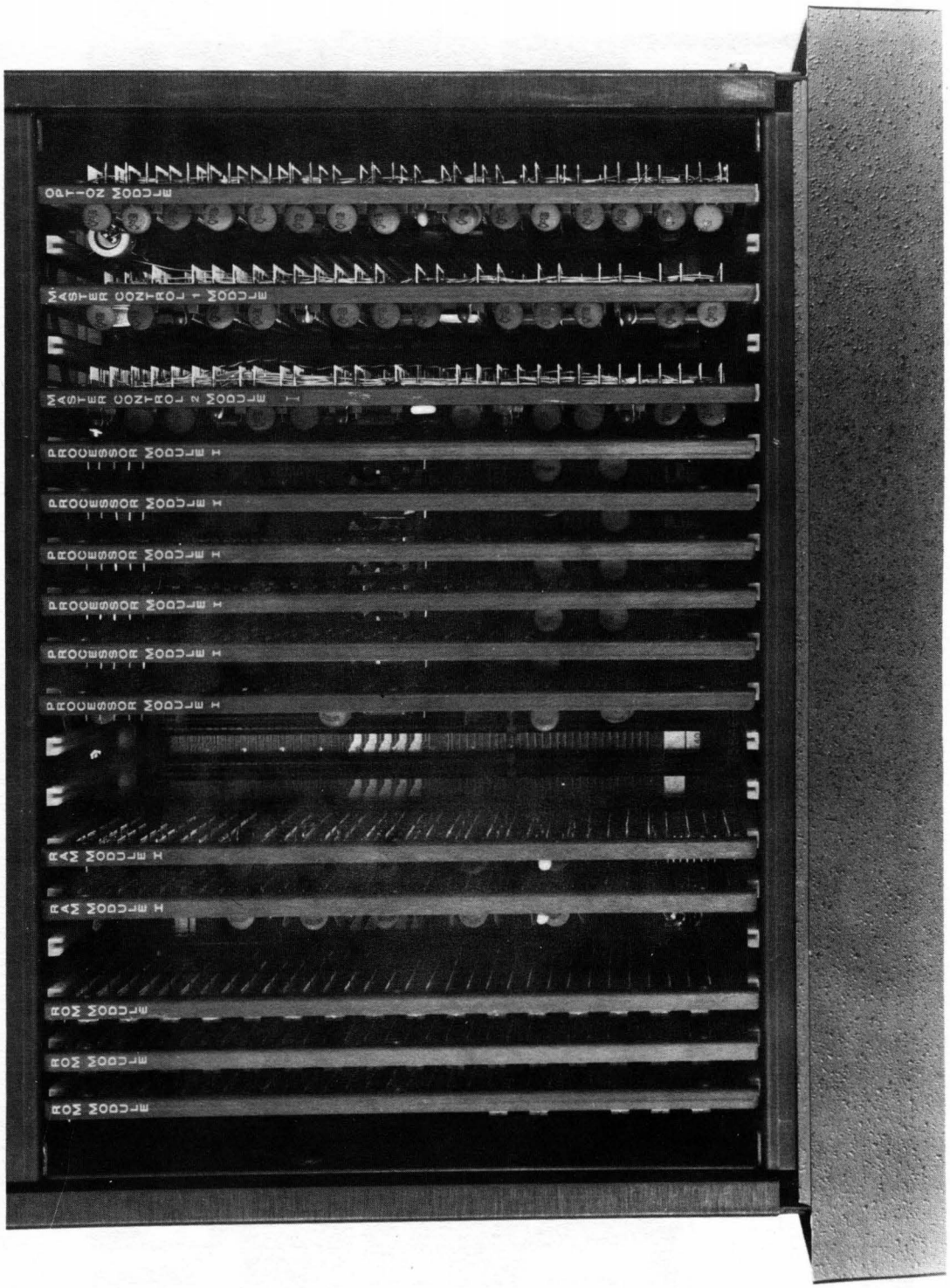


Figure 2-9. INP Mainframe

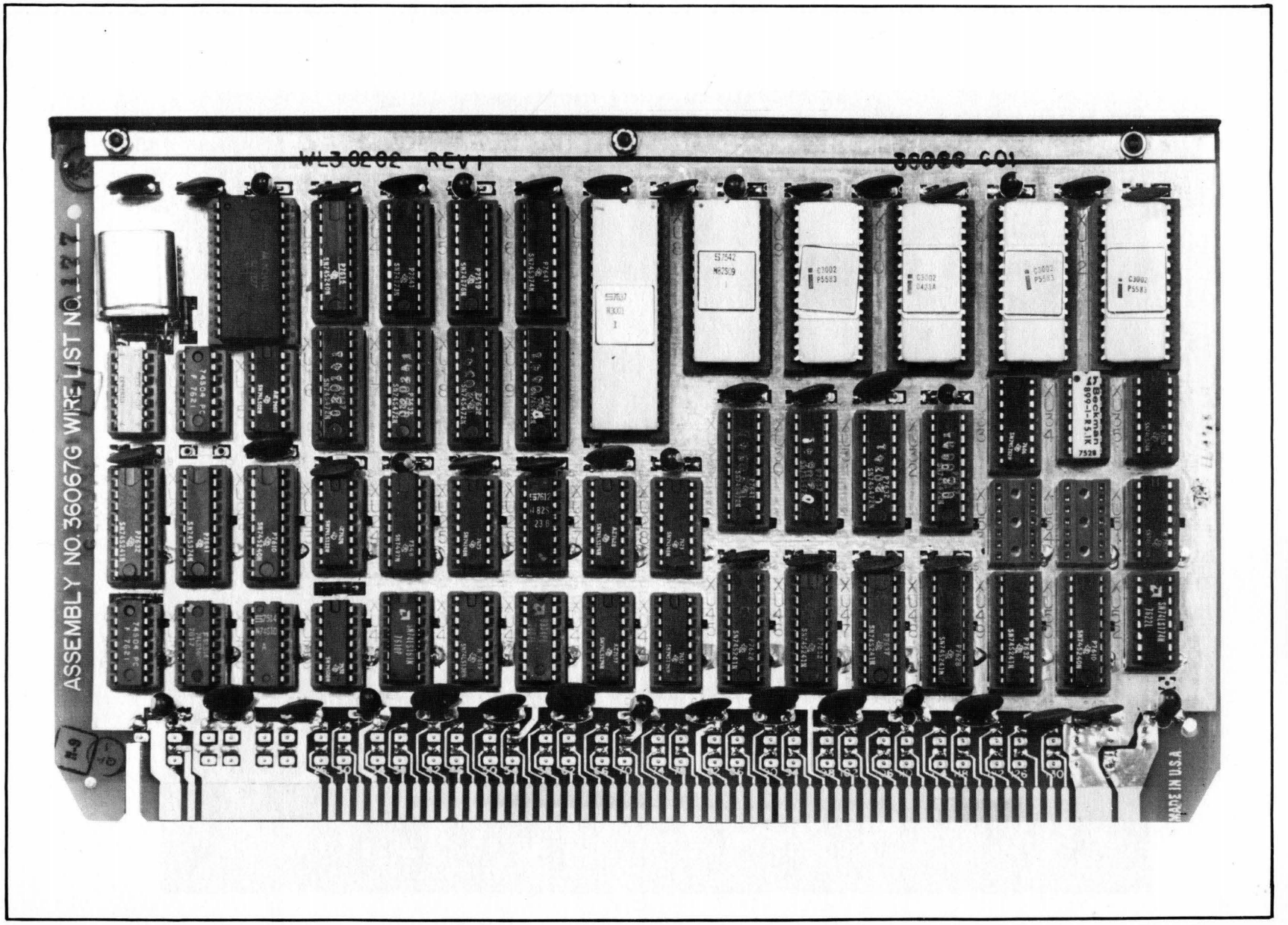
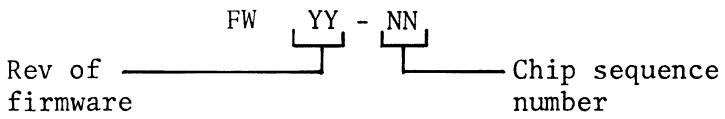


Figure 2-10. Master Controller 1 (MC1)

The MC1 firmware chips are marked as follows:



An MC1 is compatible with either a 4 MHz or a 5 MHz processor.

2.3.2 MASTER CONTROLLER 2 (MC2)

MC2 performs the interface functions between the master controller and the processors and memory (see Figure 2-11). MC2 also contains the system master clock generator, memory refresh control for the RAM's, and memory addressing and memory read/write. There is one MC2 per mainframe. MC2's that operate in a 5 MHz system are marked with 'I' on the rail. Those that are not so marked operate with 4 MHz.

MC2 has straps for controlling the size of the lock byte area and for the rate of the system clock. The lock byte area is physically on the RAM card, but is controlled from the MC2.

2.3.2.1 LOCK BYTE AREA. The lock byte area is common to all processors. It provides processors with temporarily exclusive access to 256-byte segments of RAM memory. This prevents interruption of a critical program by other processors. The key to each segment is an 8-bit "lock byte." When a processor addresses the byte and reads it, it clears the byte. Another processor addressing the same byte finds all 0's and retries at the cycle rate until the first processor has written the byte back.

Lock byte addresses are X'400' to X'500'; a total of 256 addresses. Each 32K of memory requires 128 lock bytes.

The size of the lock byte area is dependent on the INP model, and is selected by soldered straps on platform U40 of the MC2 board. These are shown in Figure 2-12.

2.3.3 PROCESSOR

The processor module performs processing of information passed between the terminal ports and the network ports.

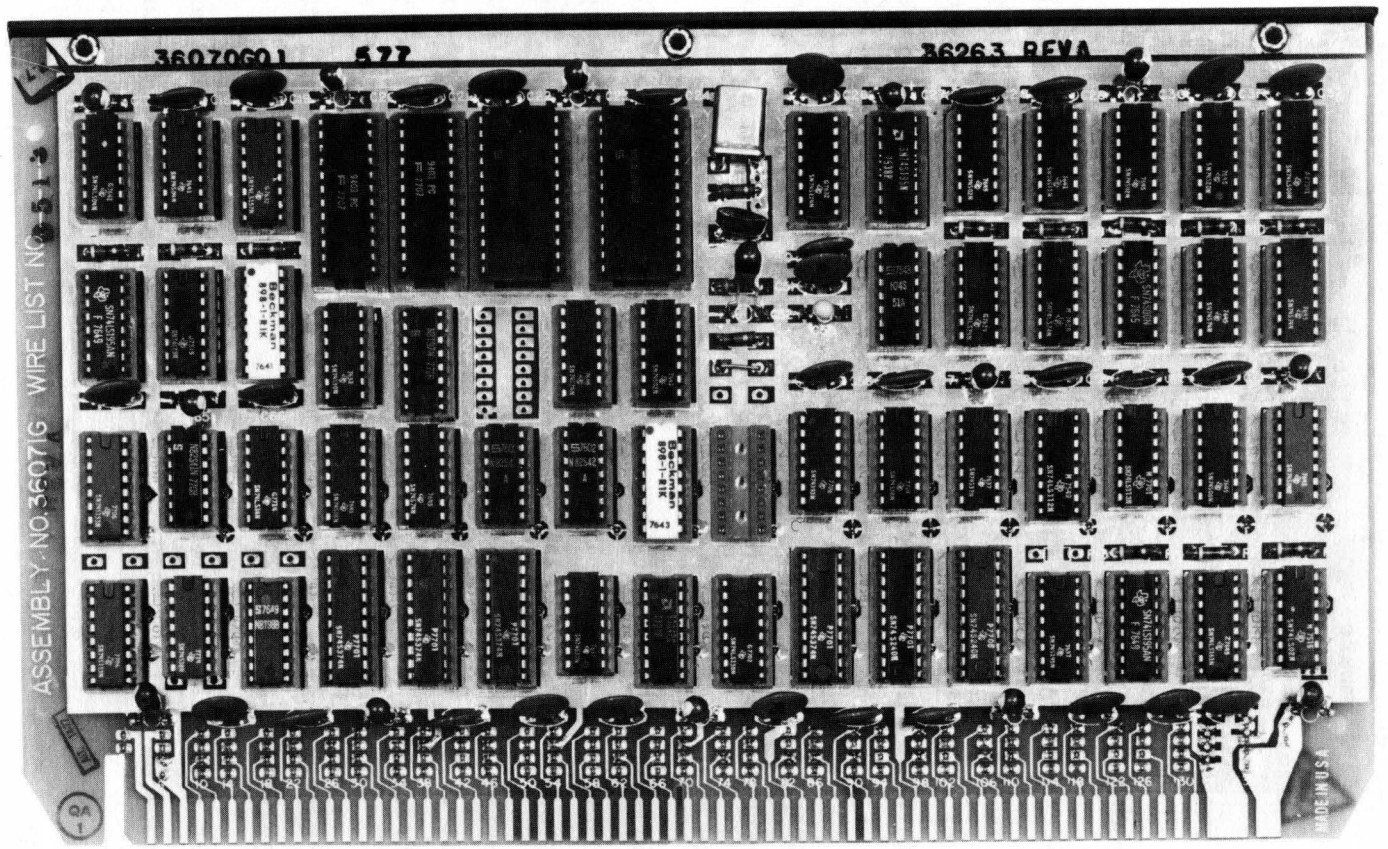


Figure 2-11. Master Controller 2 (MC2)

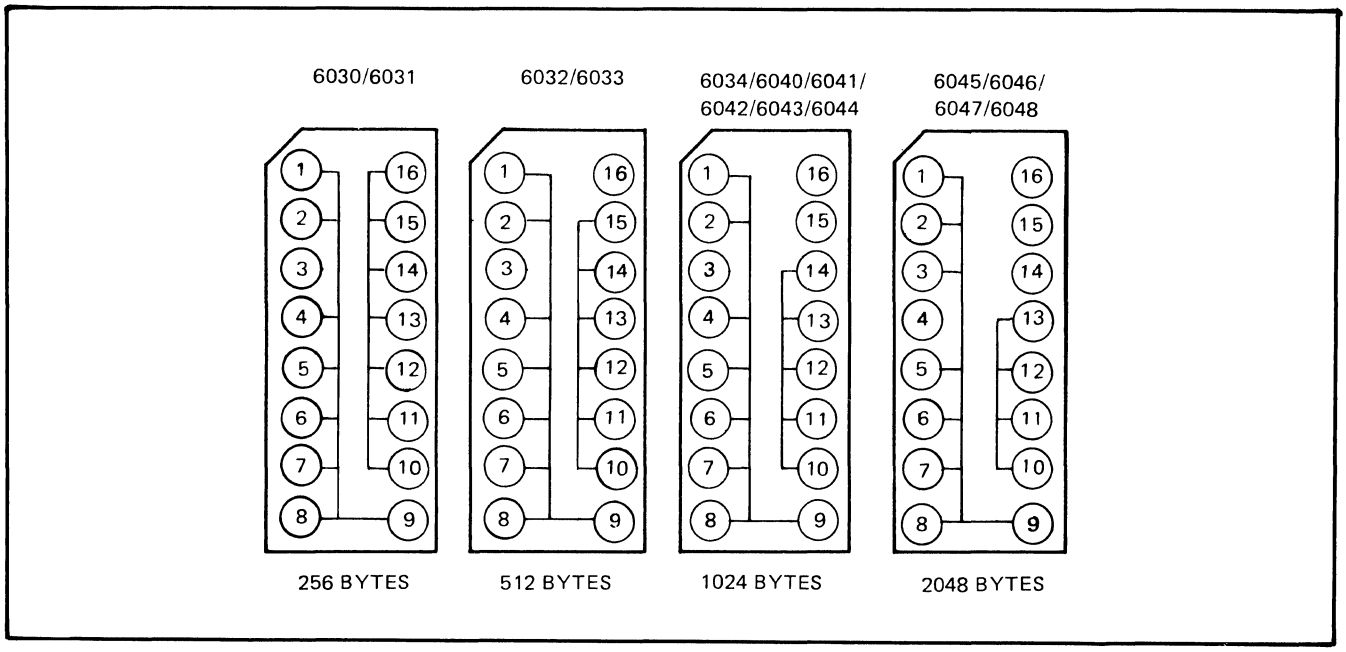


Figure 2-12. MC2 Lock Byte Platform U40

The processor (Figure 2-13) contains the Motorola M6800 microprocessor, associated bus and interrupt logic, and phase clock generation logic. There may be up to three processors in a 6030 mainframe or up to six in a 6040.

Processors that operate at 5 MHz are marked 'I' on the rail; those that are not so marked operate at 4 MHz.

Functionally, the processor is divided into four sections: phase clock generation, processor control logic, bus contention, and special addressing control, which can itself be divided into base register addressing, augmented processor register addressing, and I/O control and addressing.

A processor provides two areas of strapping. One of these, platform U34 (Figure 2-14) provides for "fast" or "slow" operation: a function of internal signal timing on the processor board. All current systems are strapped fast: U34-1 to -8, and -3 to -6. Some systems in the field may be strapped slow: U34-2 to -7, and -4 to -5; this would depend on user requirements.

The second area of strapping is in the upper right corner of the processor, just below U11: (see Figure 2-13). These connections are soldered staples (see Figure 2-15), and depend on the software used. For S46 and S47 software, the connections are across DV and 64K. For S49 they are across DV and 128K; it is the

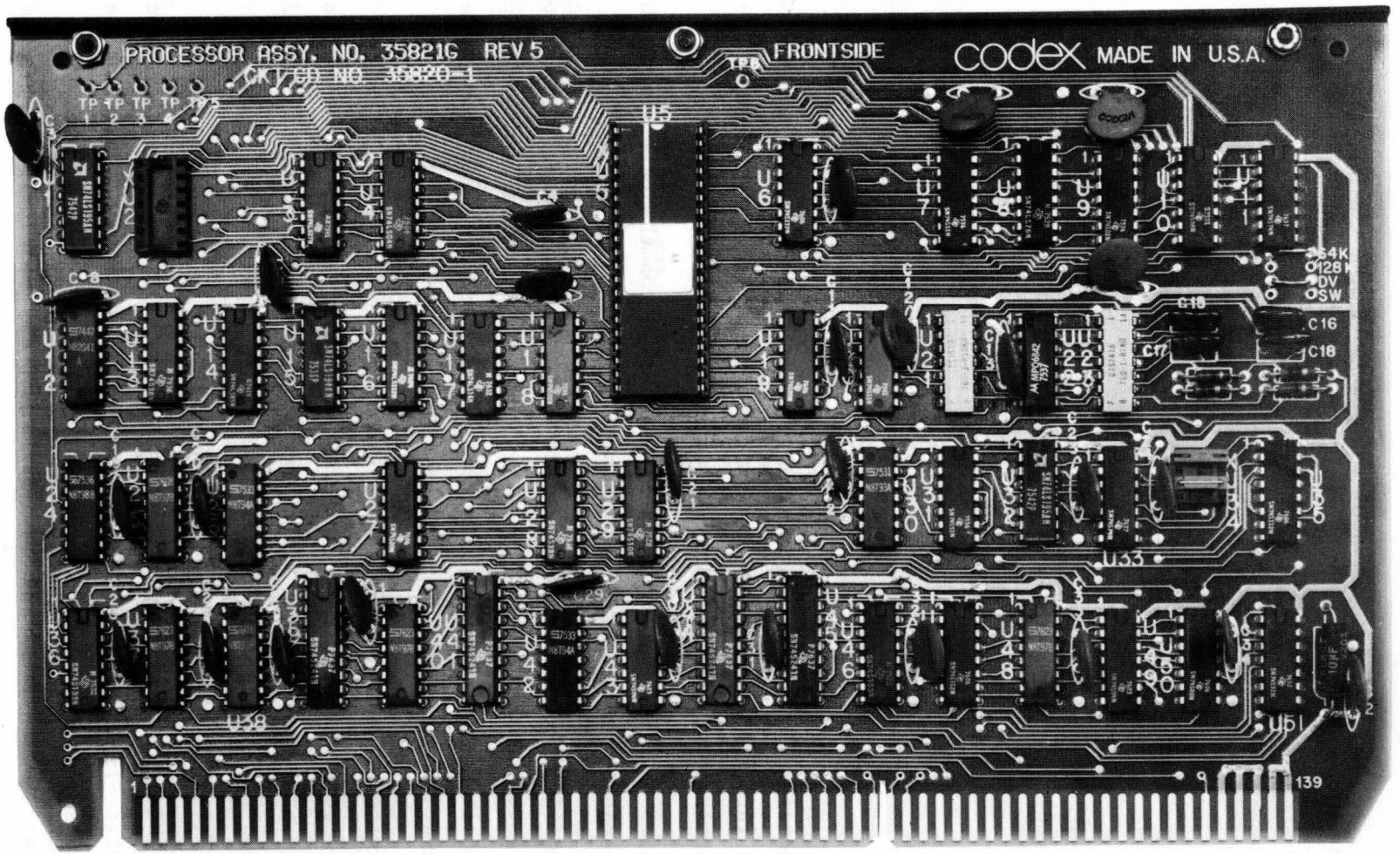


Figure 2-13. Processor

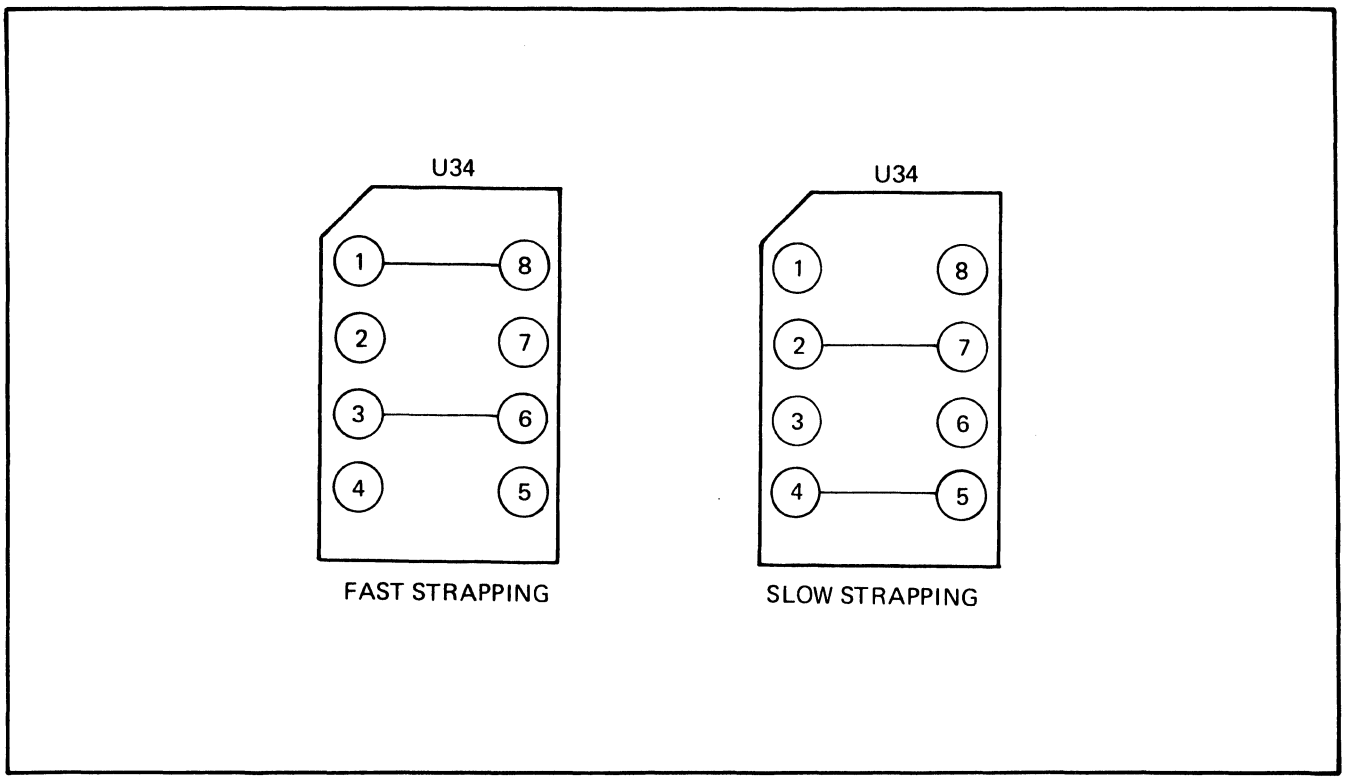


Figure 2-14. Processor Card Cycle Speed Strapping, Platform U34

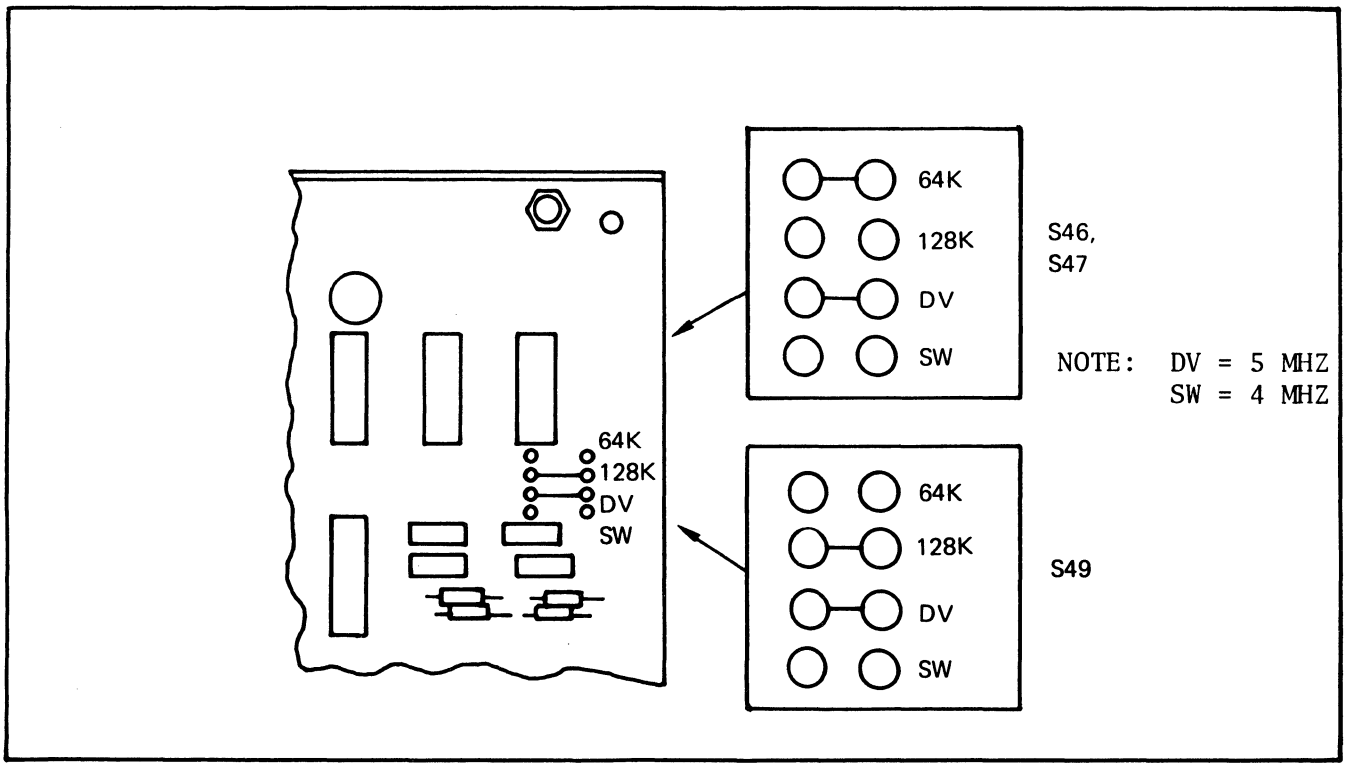


Figure 2-15. Processor Card Software Strapping

128K strap that permits addressing the third ROM (addresses 18000 to 18BFF) which holds some options available only with S49. This feature also requires firmware changes on the master control cards. The compatible MC1 can be identified by "S49" stamped on the rail.

2.3.4 16K PROM's (ROM's)

The ROM's provide software* storage to support software options ordered by the customer. These options are listed below and described in Appendix B.

Option No./ Product Code	Description
66301	Statistics and performance monitoring
66320	Operator console support
66321	Control terminal interface support
66322	Operator console and control terminal support
66323	Supervisory communications support
66324	Report logging control terminal support
66330	Asynchronous terminal support
66331	Autospeed
66332	Autoecho
66335	BSC terminal support
66344	Satellite link option
66345	Variable length ARQ option
66347	6030/6040 interface support

The software is contained on two or three ROM cards, depending on the options required. These cards must be mounted in the left-most slots in the mainframe (Figure 2-15). Each ROM has strapping on platform U52 (Figure 2-16) that addresses the software. Because this strapping defines the addresses, the sequence of the three cards in the mainframe is immaterial. The chips on the board are PROM's, programmed by Codex to provide the required memory.

*In these Codex INP's, "software" refers to the programs contained in the ROM cards; "firmware" refers to the PROM's on the MC1 module that contain the program for the Intel 3000 microcontroller.

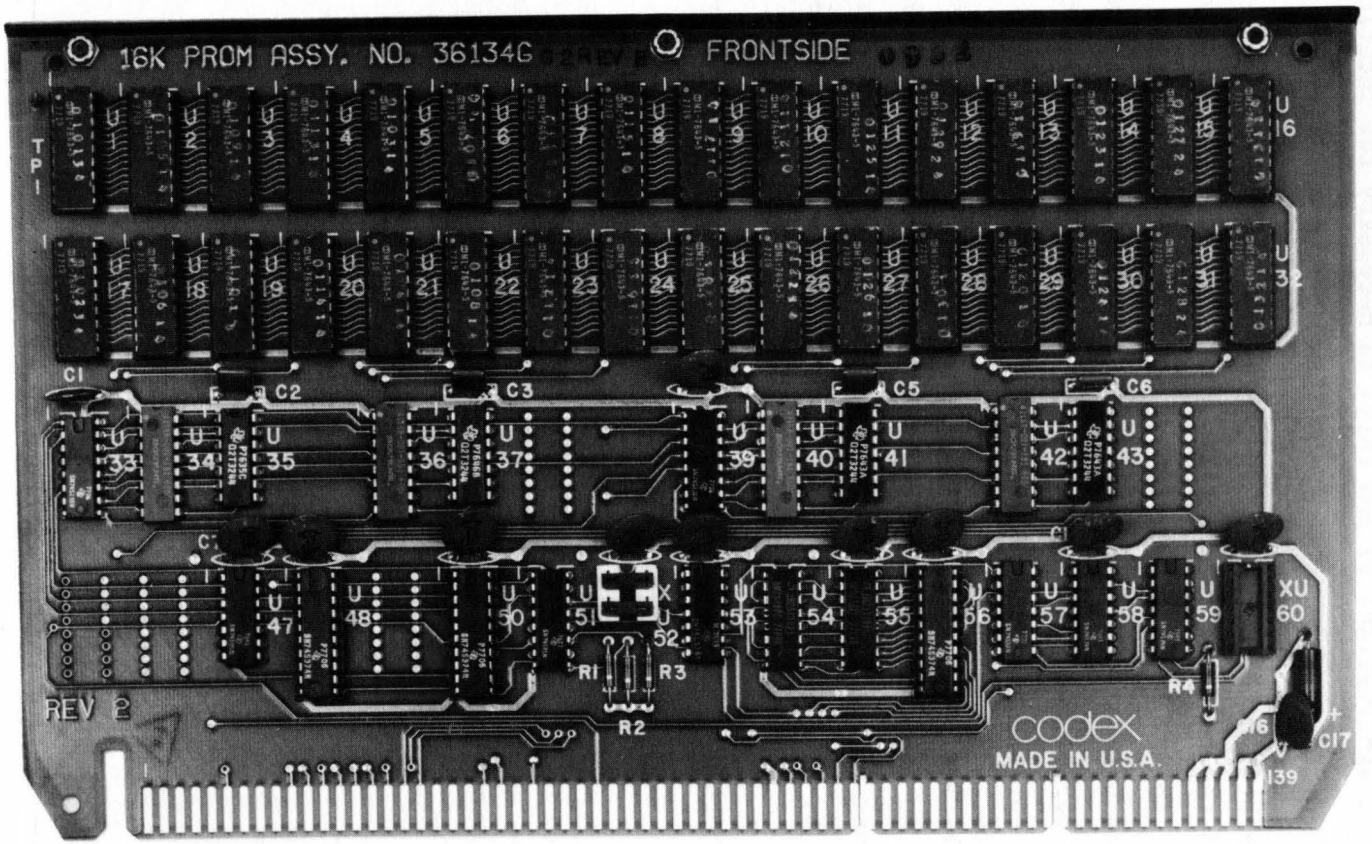


Figure 2-16. ROM (16K PROM)

The ROM's will run at either 4 MHz or 5 MHz, and are not identified for application.

2.3.4.1 ROM MEMORY MAP. The following information is included because knowledge of the addresses and applications of ROM chips is necessary for locating chips that have failed.

Figure 2-17 is an example of the address ranges used in an INP. The upper and lower limits of the code tables are fixed, but the address of the first byte of software is variable. It is a function of the Rev of the software. There may be some empty space between the top of the code tables and the lowest address of software; this may be used for "customer specials." The upper limit of software depends on the options needed by the user.

Physically, the ROM memory chips are laid out in two rows of 16 each. Each chip is 1K x 4 bits so two chips form an 8-bit byte. The odd numbered chips contain the least significant bits (0, 1, 2, 3); the even numbered chips contain the most significant bits (4, 5, 6, 7). Each chip is identified with a stamped six-digit number.

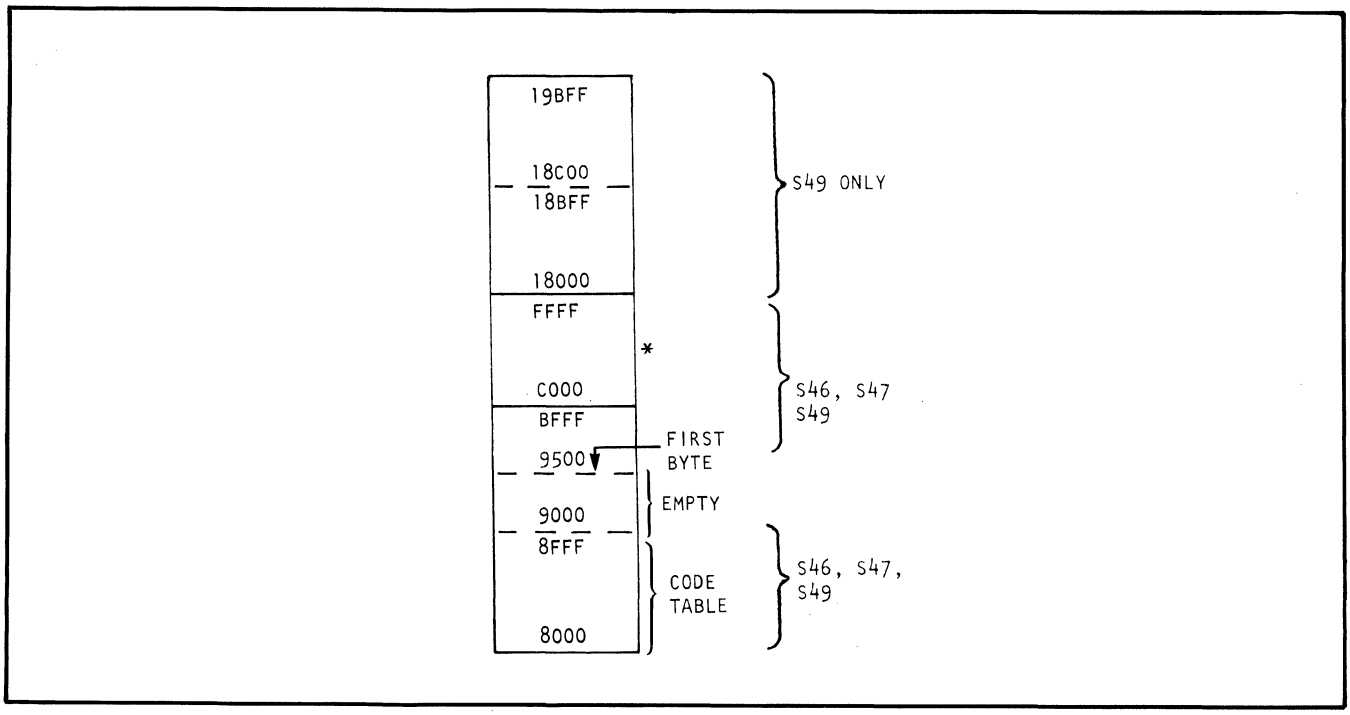
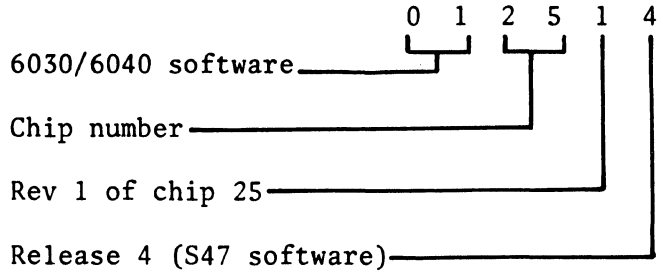


Figure 2-17. ROM Memory Map - S46, S47, and S49.06

*Locations FFF0 through FFF8 hold information on software Rev levels, checksums, and customer specials.

2.3.4.2 S47 ROM ADDRESSES. S47 software resides on two ROM cards. Addresses are shown in Tables 2-2 and 2-3.

ROM chips used with S47 software are identified with a number leaving the format:



NOTE

Chips used for the code tables start with the digits 04. These chips have the address range 8000 to 8FFF and replace chips number 57 to 64 inclusive.

Table 2-2 shows the chip addresses and sockets on the board that holds the first 32K of ROM. Figure 2-18 shows the address strapping on platform U52 of the cards.

TABLE 2-2. S47 ROM ADDRESSES AND SOCKETS - FIRST 32K

Address Range	Chip No.	Socket No.
8000 - 83FF	2, 1	U16, U32
8400 - 87FF	4, 3	U12, U28
8800 - 8BFF	6, 5	U15, U31
8C00 - 8FFF	8, 7	U11, U27
9000 - 93FF	55, 56	U14, U30
9400 - 97FF	53, 54	U10, U26
9800 - 9BFF	51, 52	U13, U29
9C00 - 9FFF	49, 50	U9, U25
A000 - A3FF	47, 48	U8, U24
A400 - A7FF	45, 46	U4, U20
A800 - ABFF	43, 44	U7, U23
AC00 - AFFF	41, 42	U3, U19
B000 - B3FF	39, 40	U6, U22
B400 - B7FF	37, 38	U2, U18
B800 - BBFF	35, 36	U5, U21
BC00 - BFFF	33, 34	U1, U17

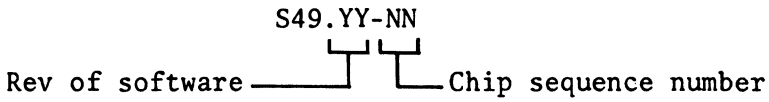
Table 2-3 shows ROM chip addresses and sockets on the board that holds the second 32K of memory.

TABLE 2-3. S47 ROM ADDRESSES AND SOCKETS - SECOND 32K

Address Range	Chip No.	Socket No.
C000 - C3FF	31, 32	U16, U32
C400 - C7FF	29, 30	U12, U28
C800 - CBFF	27, 28	U15, U31
CC00 - CFFF	25, 26	U11, U27
D000 - D3FF	23, 24	U14, U30
D400 - D7FF	21, 22	U10, U26
D800 - DBFF	19, 20	U13, U29
DC00 - DFFF	17, 18	U9, U25
E000 - E3FF	15, 16	U8, U24
E400 - E7FF	13, 14	U4, U20
E800 - EBFF	11, 12	U7, U23
EC00 - EFFF	9, 10	U3, U19
F000 - F3FF	7, 8	U6, U22
F400 - F7FF	5, 6	U2, U18
F800 - FBFF	3, 4	U5, U21
FC00 - FFFF	1, 2	U1, U17

2.3.4.3 S49 ROM ADDRESSES. S49 software is contained on three cards. The first contains address space 8000 to BFFF, the second contains C000 to FFFF, and the third (the high-order PROM) contains address space 18000 to 1BFFF, although addresses 19400 through 1BFFF are not yet used in S49.06. The strapping platform U52 on each is strapped as shown in Figure 2-19.

ROM chips that contain S49 software are marked:



ROM chips that contain the code tables are marked:

CT.YY-NN

where YY and NN have the same meanings as above.

Addresses and socket locations for the first two ROMs are the same as for S47. The complete address ranges for all chips on the third ROM are given in Table 2-4.

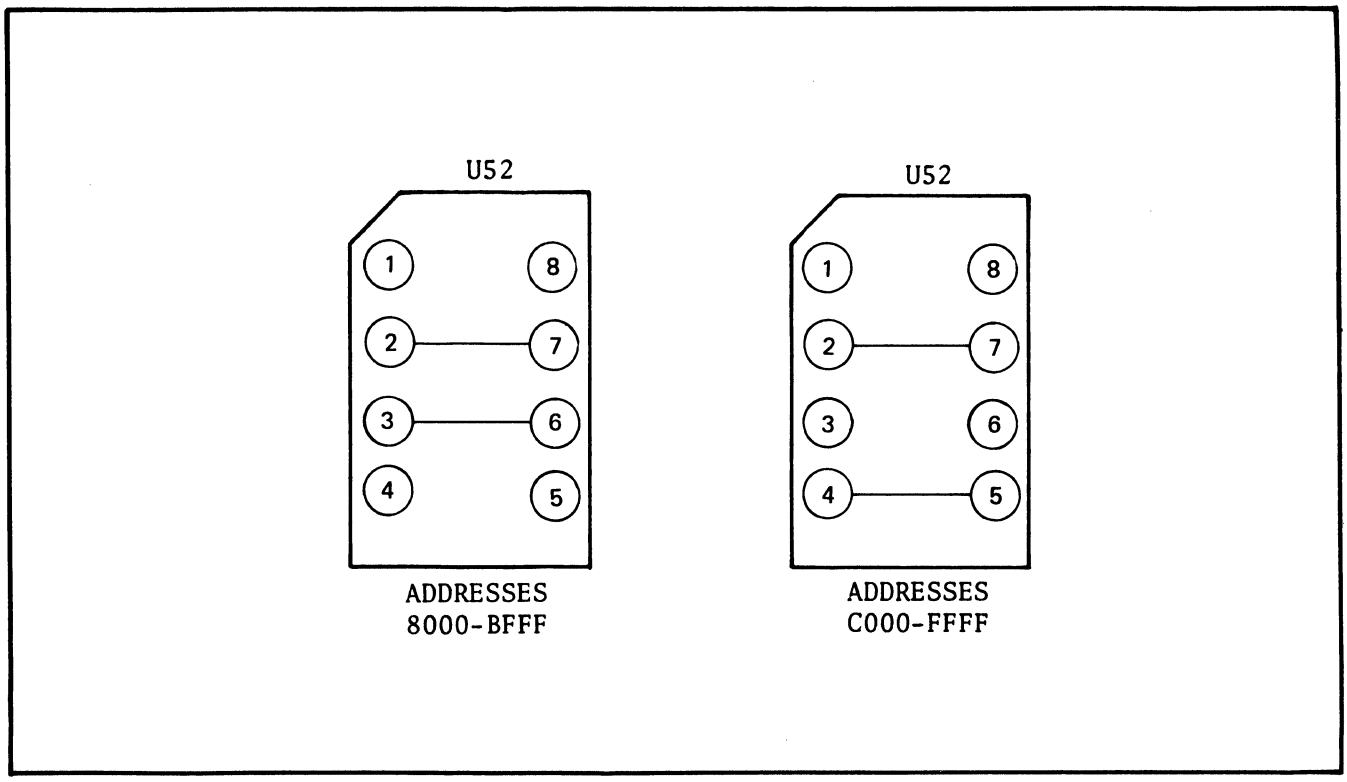


Figure 2-18. ROM Card S47 Address Strapping, Platform U52

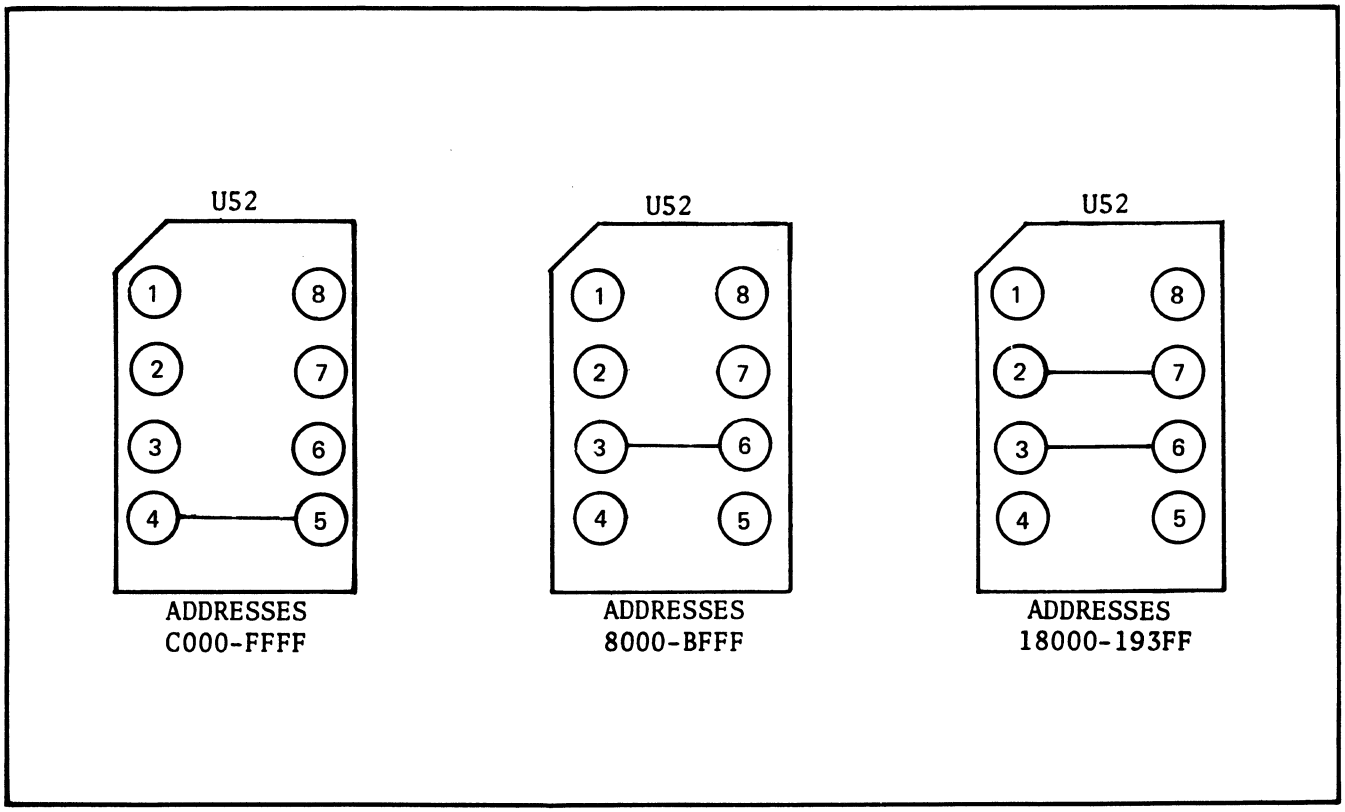


Figure 2-19. ROM Card S49 Address Strapping, Platform U52

TABLE 2-4. S49 ADDRESSES AND SOCKETS - HIGH BANK ROM

Address Range	Chip No.	Socket No.
18000 - 183FF	63, 64	U16, U32
18400 - 187FF	61, 62	U12, U28
18800 - 18BFF	59, 60	U15, U31
18C00 - 18FFF	57, 58	U11, U27
19000 - 193FF	55, 56	U14, U30
19400 - 197FF Unused	53, 54	U10, U26
19800 - 19BFF	51, 52	U13, U29
19C00 - 19FFF	49, 50	U9, U25
1A000 - 1A3FF	47, 48	U8, U24
1A400 - 1A7FF	45, 46	U4, U20
1A800 - 1ABFF	43, 44	U7, U23
1AC00 - 1AFFF	41, 42	U3, U19
1B000 - 1B3FF	39, 40	U6, U22
1B400 - 1B7FF	37, 38	U2, U18
1B800 - 1BBFF	35, 36	U5, U21
1BC00 - 1BFFF	33, 34	U1, U17

2.3.5 DIAGNOSTIC ROM - Options 6950 and 6951

The diagnostic ROM is a test board that is used for identifying hardware-caused operating problems and for isolating faulty boards. It does not test the system software. The test procedure is described in Chapter 5. Option 6950 is used for INP's that use software S47 and below; Option 6951 for S49.

Physically, the diagnostic ROM is a standard ROM board containing specially-programmed PROM's. To run diagnostics, the ROM boards are removed and the diagnostic ROM is inserted in any of the empty ROM slots. It is removed as soon as testing is completed.

2.3.6 RANDOM ACCESS MEMORY (RAM) MODULE

The 16K RAM module (see Figure 2-20) provides temporary storage for all data processing activities within the INP mainframe. The RAM interfaces with the processors and the MC2 via the mainframe bus to perform read, write, and read-write-modify functions. Additional logic circuitry provides all the control signals required by the RAM chips, as well as address multiplexing, address range decoding, and interleaving.

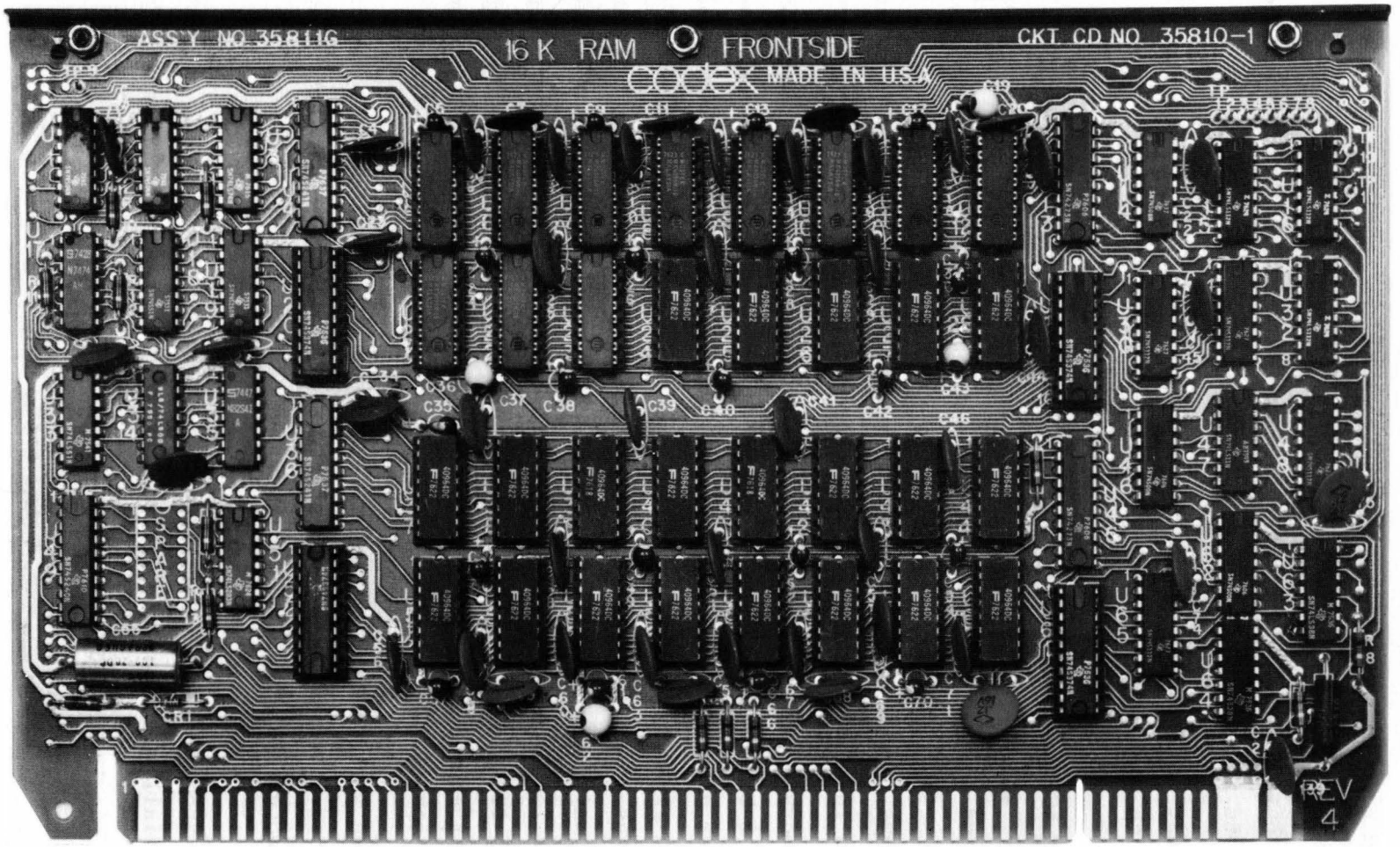


Figure 2-20. 16K RAM

The 16K memory is organized as four banks of 4K each, and consists of 32 4K x 1 dynamic random access chips. These chips are supported by refresh logic on the RAM card and on MC2.

RAM's that operate in a 5 MHz system are marked "I". Those that are not so marked operate in a 4 MHz system.

RAMs must be installed in consecutive slots in the mainframe (see Figure 2-2), beginning with the leftmost slot that is keyed for RAM cards.

2.3.6.1 RAM LOGIC. The RAM logic can be divided into four functional classes: memory array, address decoding and interleaving, control signal generation, I/O data interface, and address buffering.

2.3.6.2 MEMORY ARRAY. It is useful to understand the memory array and address decoding and interleaving in order to locate failed RAM chips for replacement.

The memory array for each RAM module consists of four selectable banks, each of which is 8 bits wide x 4K. The two upper banks hold the even addresses, while the two lower banks hold the odd addresses. Depending upon the method of interleaving (two-way or four-way) some of these banks will correspond to different address ranges as illustrated in Figures 2-21 and 2-22. For example, bank 1 for a two or four way interleaf corresponds to every fourth memory location below 16K beginning at location 0000, while bank 0 for a two way interleave corresponds to every fourth location below 16K beginning at 0002; however, for a four way interleave, it corresponds to every fourth location between 16K and 32K beginning at location x '4000'.

The even and odd banks are controlled separately and the data input/output lines are tied to separate drivers/receivers. This enables concurrent accesses by different processors or MC2 to the even and odd banks.

2.3.6.3 ADDRESS DECODING AND INTERLEAVING. The address decoding and interleave logic essentially decodes one of three conditions to select the bank being addressed:

1) a single 16K RAM (2 way interleave),
2) the first slot of a pair of RAMs (4 way interleave),
3) the second slot of a pair.

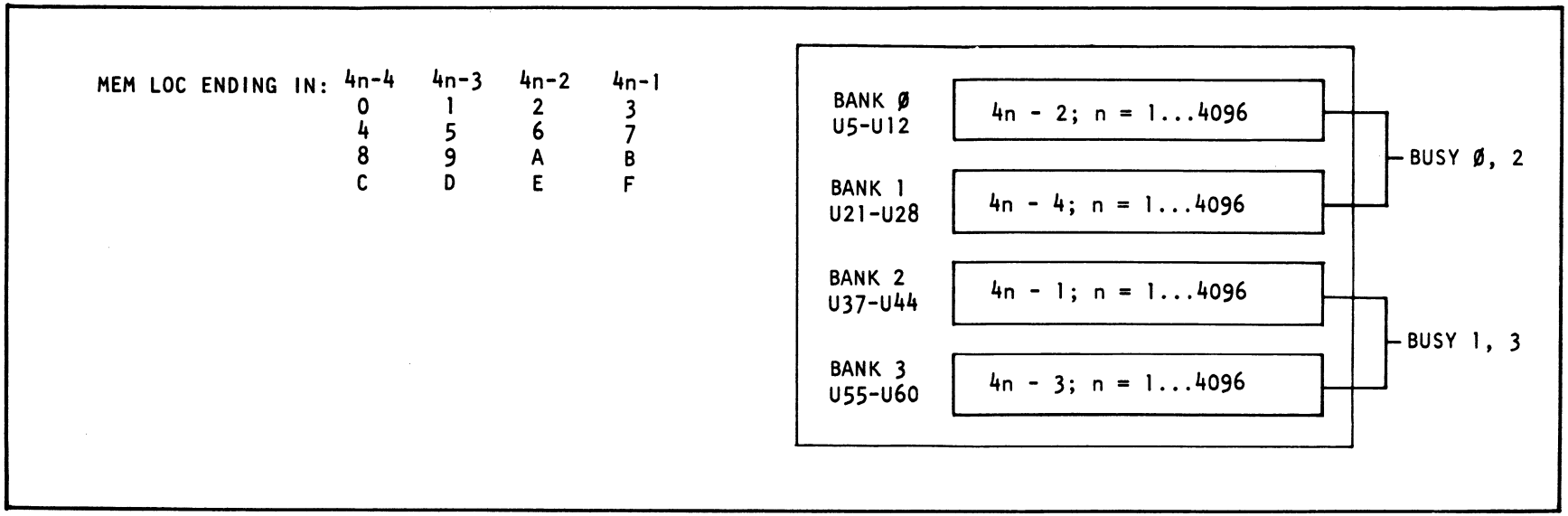


Figure 2-21. Two-Way Memory Interleave, 16K System

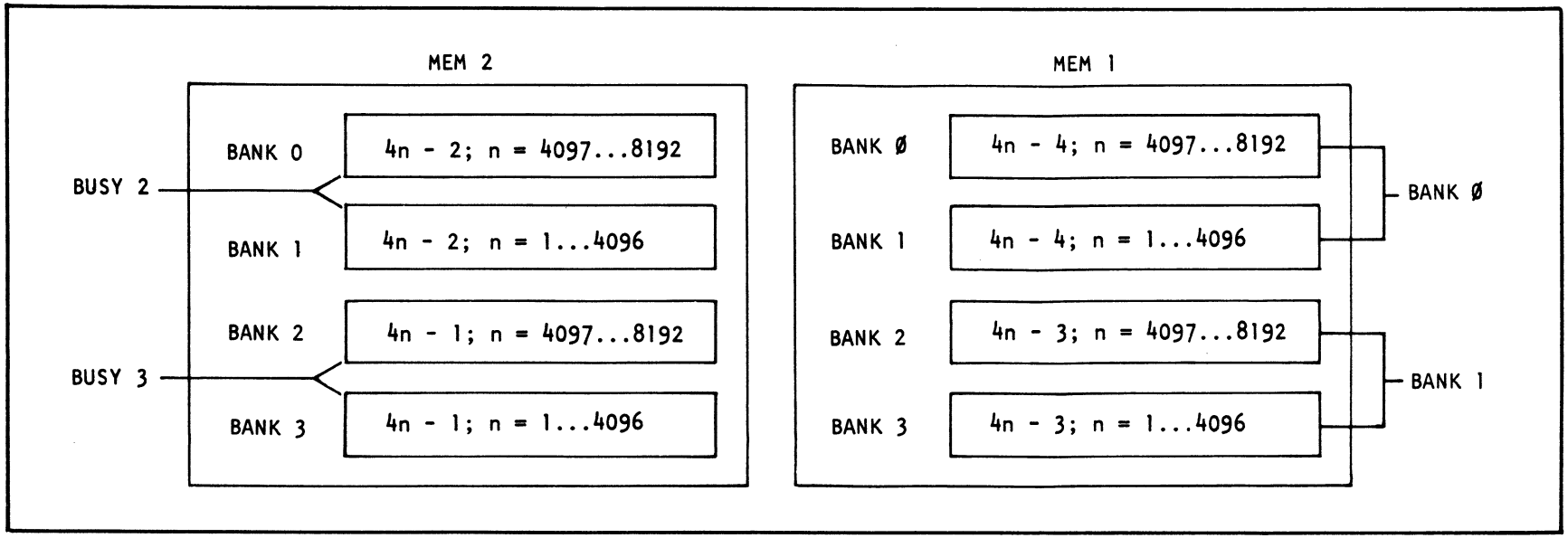


Figure 2-22. Four-Way Memory Interleave, 32K System

Since interleaving is limited to pairs of RAM modules, the decoding for a third and fourth, etc., is almost identical, differing only by the two most significant memory address lines used to decode 32K chunks of memory.

2.3.7 OPTION MODULE

The option module (Figure 2-23), holds information about the configuration of the customer's system. Its logic provides the interface between the master controller and 1) the operator's console and/or the control terminal port, and 2) the configuration memory. It also contains mainframe hardware reset logic and node number switching.

The configuration memory consists of up to 8 bytes of nonvolatile (battery backed up) CMOS RAMs with a manual write-protect switch. There are five 12 x 4-bit RAMs in each configuration.

CAUTION

It is possible to discharge the battery by wrapping the board in conductive packing material or by attaching a protective edge connector cover to the edge connector. Use only clear colorless polyethylene material for wrapping. Do not use an edge protector.

2.3.7.1 CONFIGURATION MEMORY LAYOUT. There are two versions of the option module: wire wrap and printed circuit. The wire wrap version consists of only one board, with the configuration memory chips laid out across the top of the board. The PC version consists of a mother board and a daughter board. The daughter board carries the configuration memory chips. There is only a PC version for Models 6046, 6047, and 6048; all others may have either PC or wire wrap boards (see Appendix J).

2.4 PORT NEST

A port nest is a card rack with connections for 18 PC cards (Figure 2-24). It contains one Nest Interface card (NIC) and up to 16 port cards, the types and quantities of which are application-dependent. The types of port cards are network ports (NP's) consisting of a set of two cards: an NP1 and an NP2; Terminal Ports (TP's), Activity Indicator Terminal Ports, and/or Current Loop Ports (CLP's). If

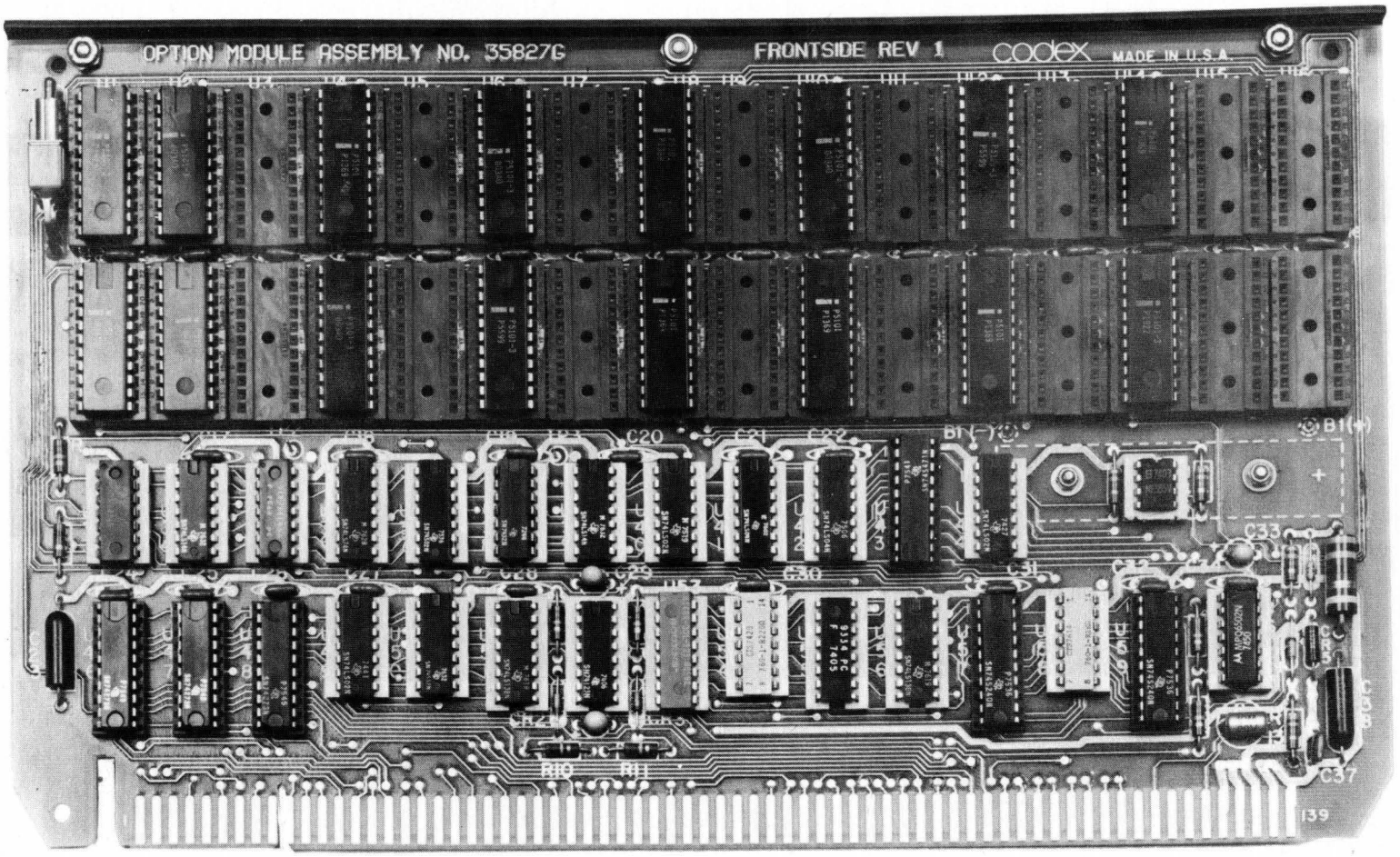


Figure 2-23. Option Module

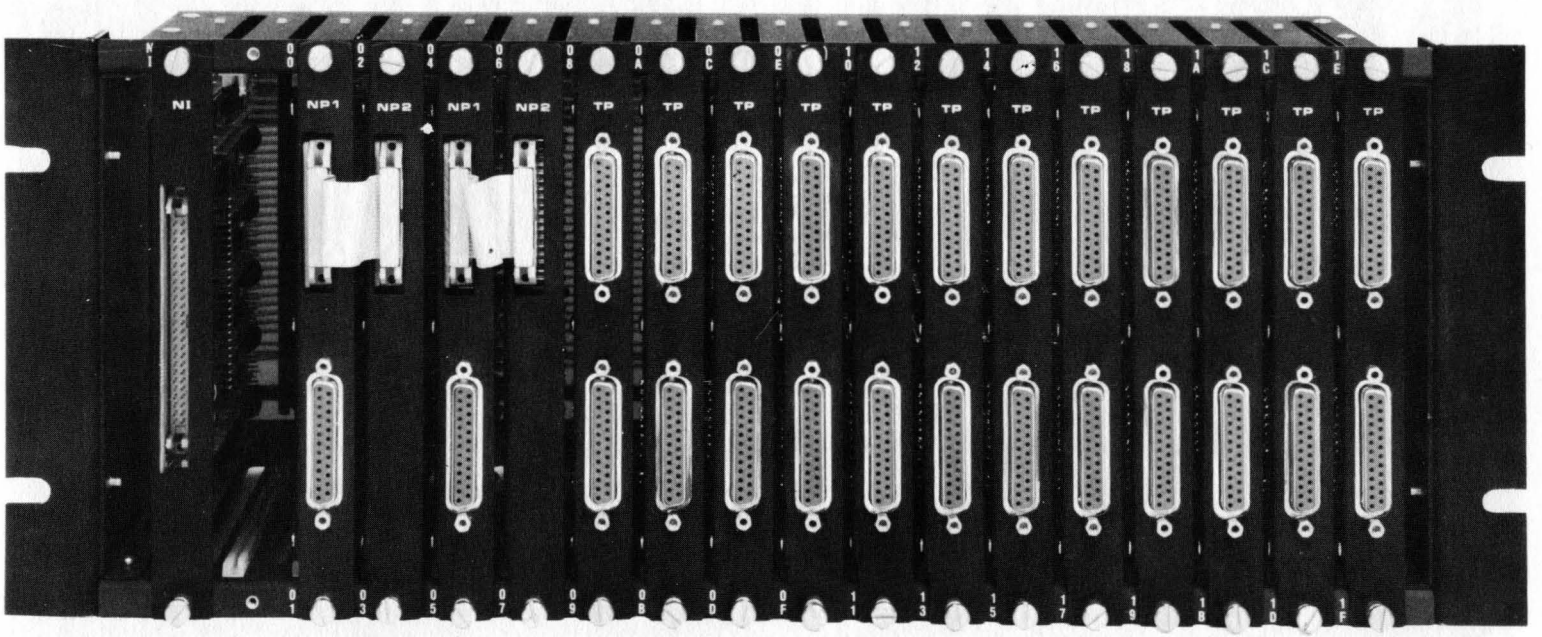


Figure 2-24. INP Port Nest

the INP has the Report Logging CTP option, a time-of-day module (TODM) is installed in slot 1E/1F. Port cards are connected to the nest interface card by a PC backplane port nest bus.

Every INP has as many port nests as needed to hold the required number of terminal port cards. Multiple port nests are cascaded from the mainframe by way of I/O busses in the form of 50-conductor ribbon cables between NIC's (see the block diagram, Figure 2-1).

2.4.1 PORT ADDRESSES AND PHYSICAL LOCATIONS

The nest interface card is mounted in the leftmost slot in the nest, marked "NI." It has no address. The next nest is empty, and also has no address. The two boards of the first network port are mounted in slots 00/01 and 02/03; the network port address is 02 - the first card is not addressed. A second network port (if present) is mounted in slots 04/05 and 06/07, and is addressed as 06. The locations and addresses for 8 port nests are shown in Figure 2-25. Terminal port cards have two channels each. The address of the J1 channel is the upper of the two addresses for the card, and the upper addresses are even. The address of the J2 channel is at the bottom which is an odd address.

2.4.2 INSTALLATION OF PORT CARDS

Terminal and network port cards that are located downstream of one empty slot in the port nest will operate normally because they are able to generate an interrupt. However, they cannot if they are downstream of two consecutive empty slots. For this reason it is good practice to insert cards in consecutive slots. This allows removal of a port card while the INP is running.

2.4.3 NEST INTERFACE CONTROL MODULE

The Nest Interface control (NI) module (Figure 2-26) in each port nest recognizes and passes I/O signals (from the mainframe or the adjacent upstream NI if there are two or more port nests) addressed in the I/O ports in its nest, as well as the adjacent downstream NI. Appendix C shows the signals on the 50 pins upstream, downstream (if applicable), and on the nest backplane to NP1 and NP2. The NI contains nest-selection logic, read-write controls, local chip select logic, interrupt service logic, clock buffers, a downstream address generator, and an 8-bit bidirectional Data Access Line (DAL) bus.

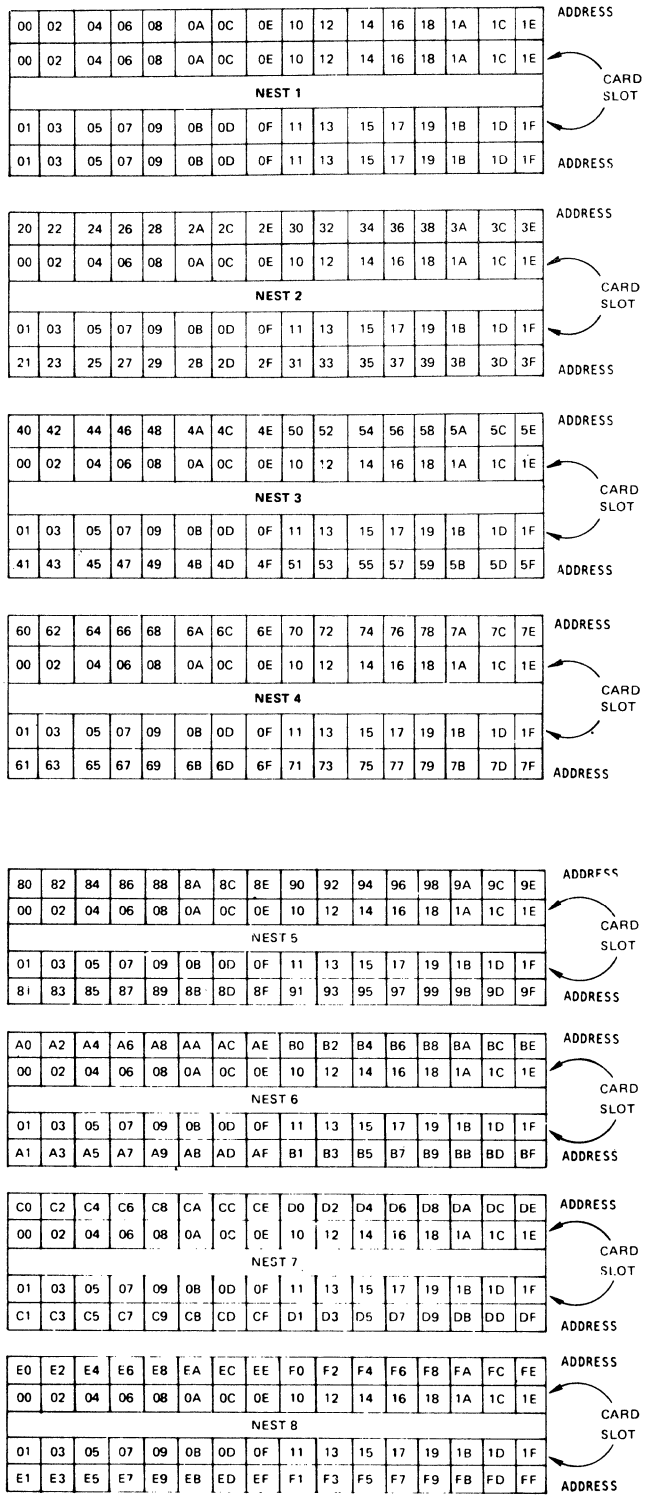


Figure 2-25. Physical Locations and Addresses - Port Nests

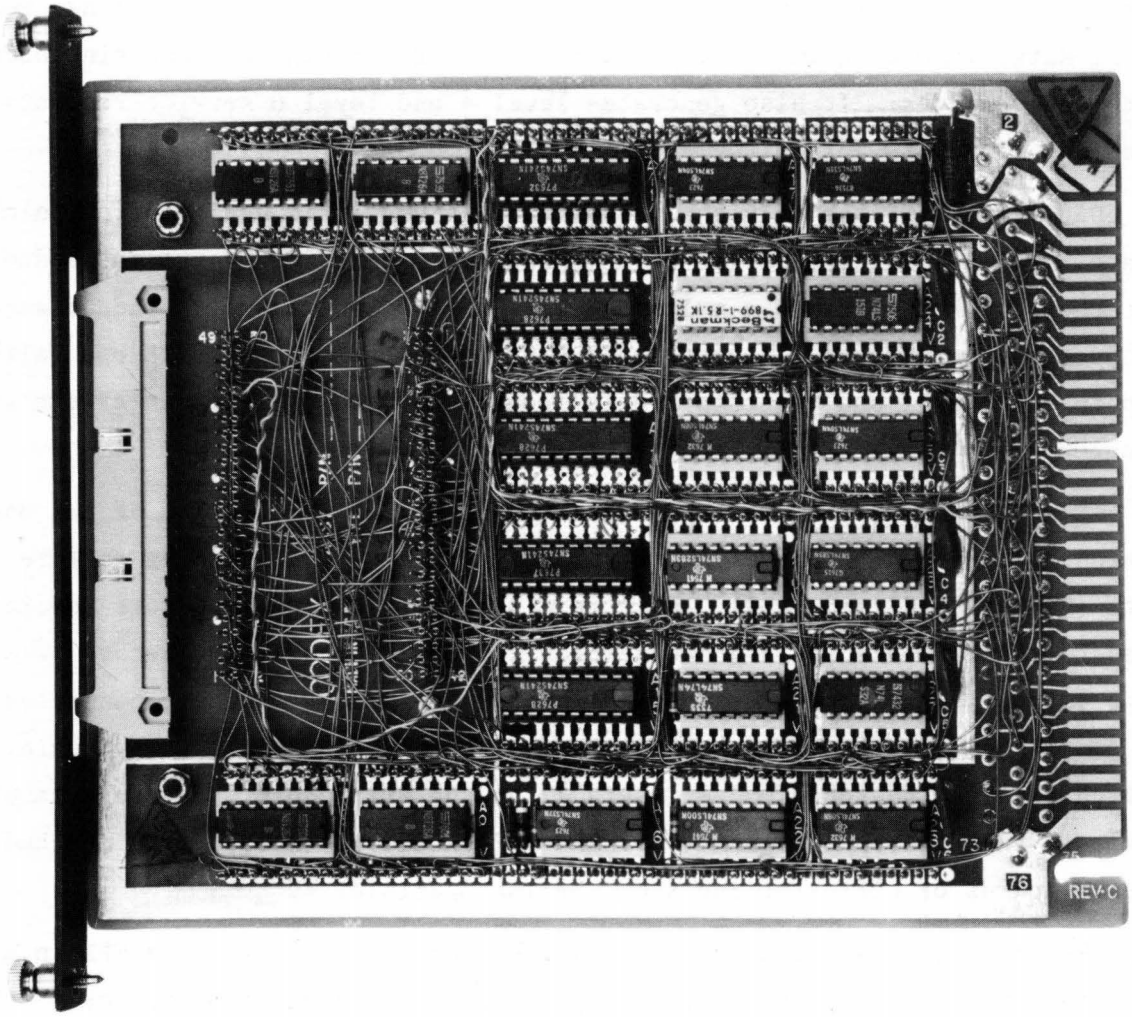


Figure 2-26. Nest Interface Control Module

As many as 8 nests can be daisy-chained via their respective NI modules and I/O busses.

2.4.4 NETWORK PORT

The network port is the node interface to the high speed trunk modem, and ultimately, to the INP at the remote node.

The network port performs the functions of serializing, deserializing, and buffering data; inserting and detecting flags; and generating and checking block error check sequences. It also generates level 4 and level 6 service requests and receives and transmits acknowledgments.

A 6030 series INP has only one network port since it is designed for point-to-point applications. A 6040 series INP has two or more network ports as needed to support the attached links in a multinode net. Network ports may be added according to system requirements. A port can operate at speeds up to 19.2K bps (although used up to 9600 bps), and presents a Data Terminal Equipment (DTE) interface at its EIA connector on NP1.

A network port, shown in block diagram in Figure 2-27, consists of two modules: NP1, which contains the transmit circuits, and NP2 which contains the receive circuits (Figures 2-28 and 2-29). Each is a highspeed synchronous port specially designed to handle variable-length codewords and to compute error checks. The two NP's are joined logically (daisy chained) by a ribbon cable I/O bus, connected to the J1 connector of each module. Removal of either NP breaks the daisy chain. Connection to the high-speed modem is via J2 on the NP1 module. J2 presents a DTE interface to the high-speed modem. NP1 and NP2 should be treated as a matched pair because two cards of different rev's may be incompatible.

The NP1 card is installed in slot 00/01 of the port nest and the NP2 in slot 02/03. The network port is addressed as port 02 for configuration purposes. Port addresses are hexadecimal.

2.4.4.1 NETWORK PORT SIGNALS.

Table 2-5 shows the signals on the NP interconnect cable, their sources, and their applications.

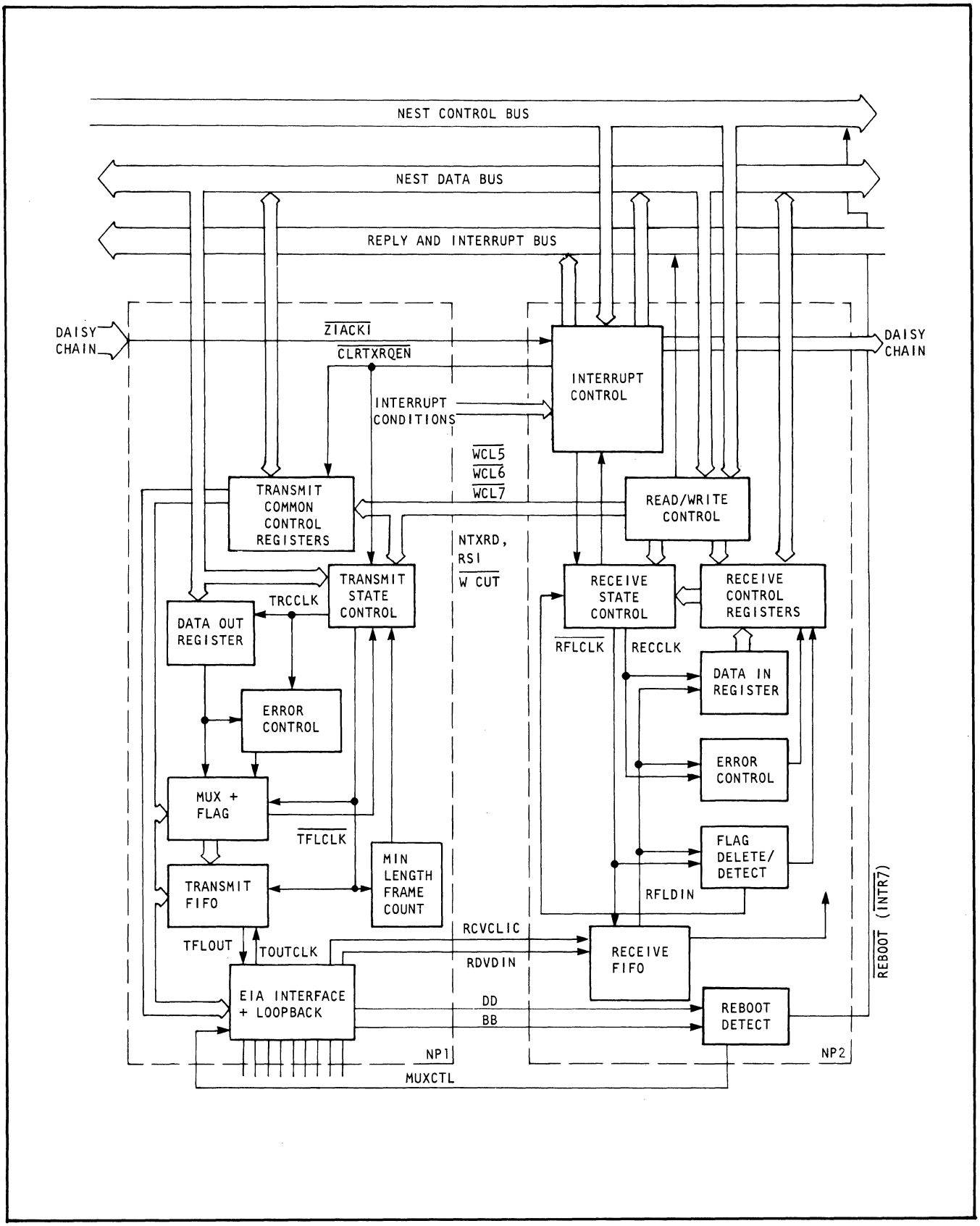


Figure 2-27. Network Port Block Diagram

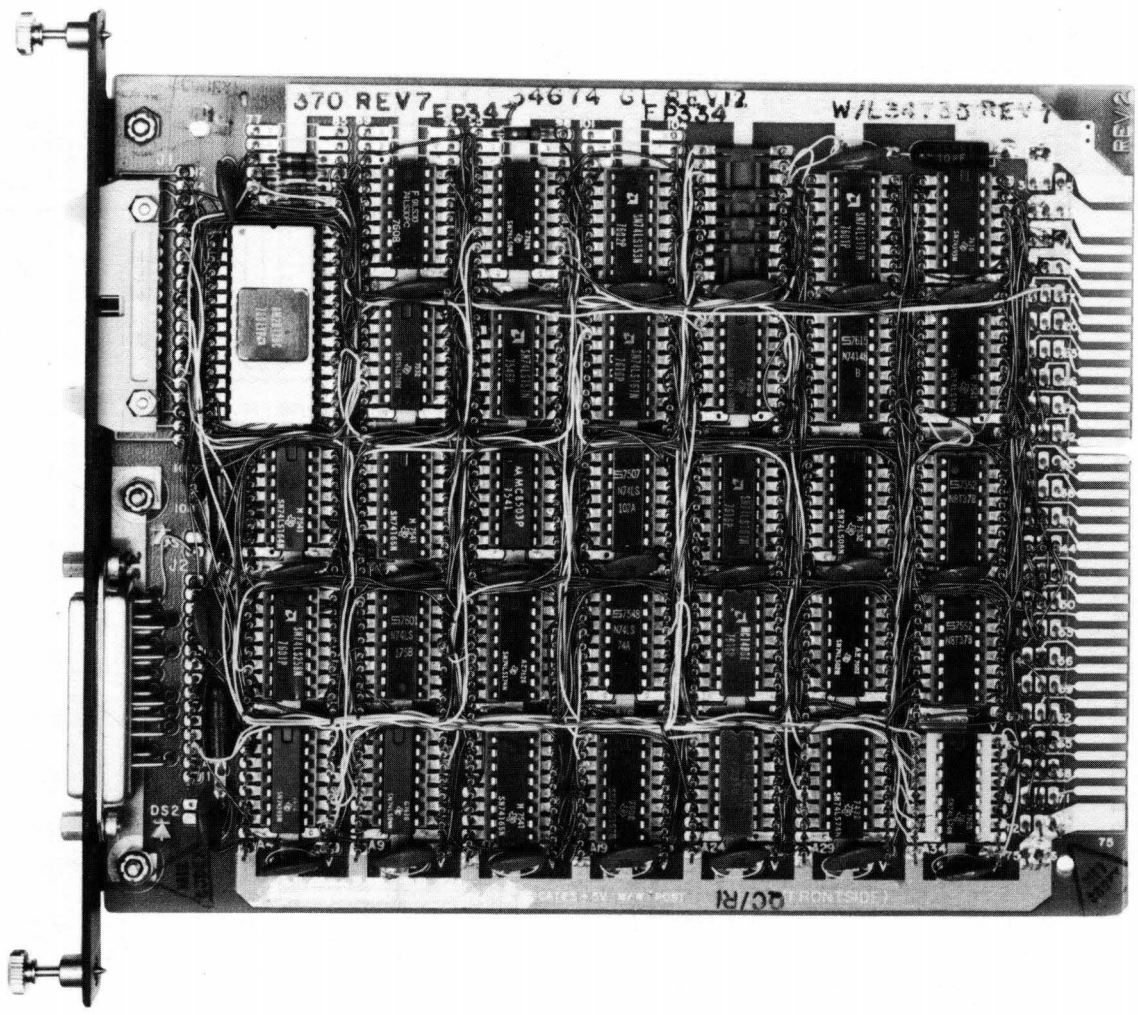


Figure 2-28. Network Port 1 Card (NP1)

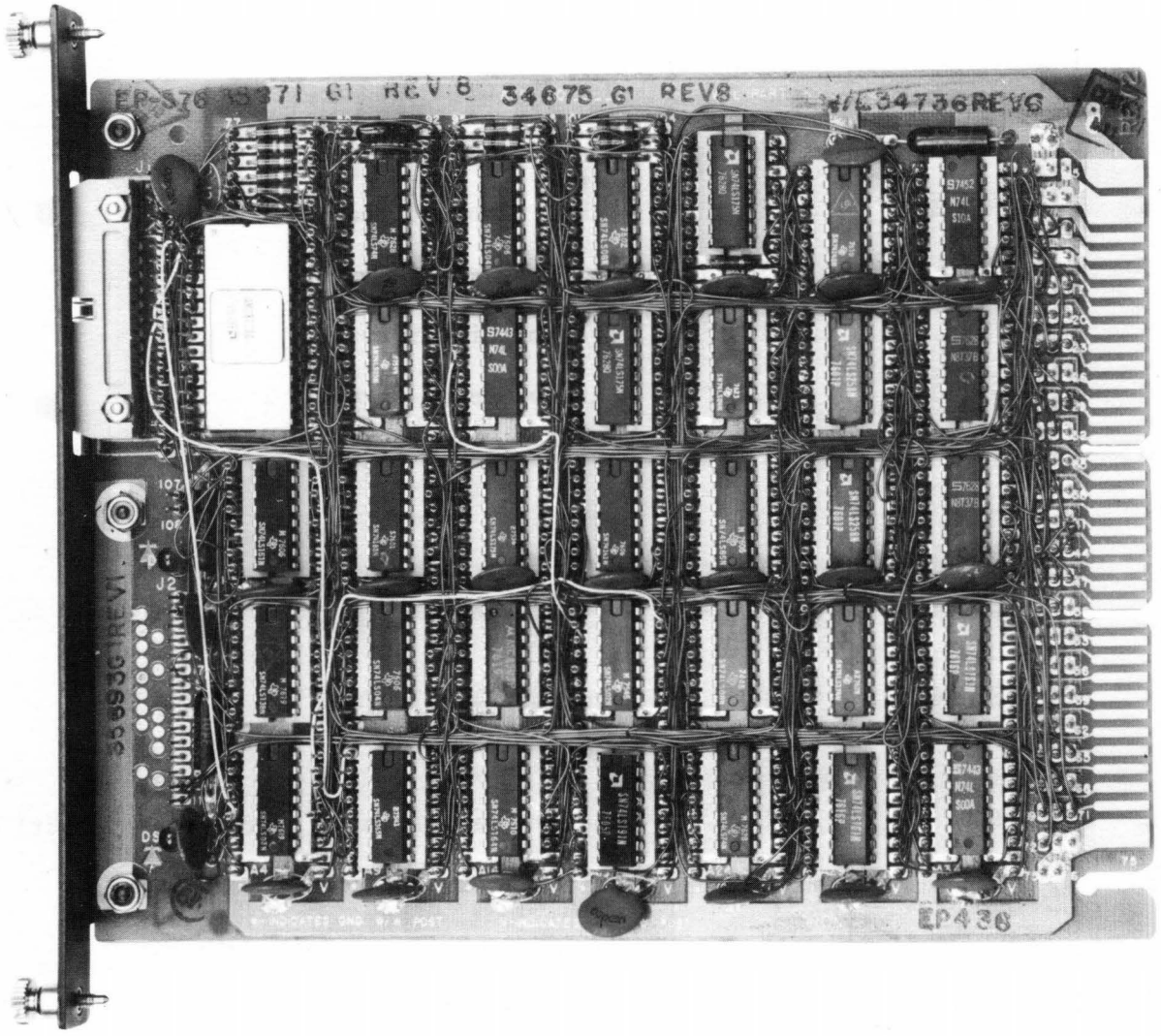


Figure 2-29. Network Port 2 Card (NP2)

TABLE 2-5. NETWORK PORT INTERCONNECT CABLE SIGNALS

J1 Pin	Signal Name	Source on NP_	Comments
1	$\overline{\text{PNDET}}$	1	Not used
2	$\overline{\text{WCL0}}$	2	Write clock, register select = 0
3	$\overline{\text{WCL4}}$	2	Not used
4	RCVDIN	1	Receive data in
5	$\overline{\text{RCVCLK}}$	1	Receive clock
6	$\overline{\text{CLRTXRQEN}}$	2	Clear transmit request enable
7	ZREPLY	2	Reply to poll*
8	$\overline{\text{TINT}}$	1	Transmit interrupt
9	$\overline{\text{LZREPLY}}$	-	Latched reply to poll*
10	$\overline{\text{WCL6}}$	2	Write clock, register select = 6
11	8ONES	2	Last 8 or more bits were 1
12	RS2	2	Register select 2 (middle bit)
13	-	-	Not used
14	TFFFLAG	1	Transmit $\geq$ half full
15	-	-	Not used
16	BBTTL	1	Receive data from BB (for reboot detect)
17	$\overline{\text{WCL5}}$	2	Write clock, register select = 5
18	$\overline{\text{RBDDTTL}}$	1	Buffered DD (for reboot detect)
19	MUXCTL	2	Disables loopback
20	$\overline{\text{WCL7}}$	2	Write clock, register select = 7

*Could be eliminated by additional latch on NP2.

2.4.5 DUAL UNIVERSAL TERMINAL PORT - Option 6130

This terminal port (TP) provides RS-232-C or CCITT V.24 interfaces between an Intelligent Network Processor and the data terminal attached to it. The TP module (Figure 2-30) contains two channels, each independently capable of full duplex operation in either asynchronous or BSC synchronous mode. (The mode is determined when the system is configured.) Each interface can appear as a modem (DCE) or as a data terminal (DTE), depending on the interface cable used to connect the terminal port channel to its I/O device. Terminal port interface signals and the interfaces for each type of cable are listed in Appendix C.

The TP contains hardware for generating and selecting clock rates, and selecting clock sources, EIA control signals, and signal delays. Two separate sets of clock rates are provided - one for asynchronous (low speed) terminals, the other for synchronous (high speed) terminals. Seven standard asynchronous clock rates are supplied: 75, 110, 134.5, 150, 300, 600, and 1200 bps. Other, customer-selected speeds are available via Option 6136, each at the sacrifice of one standard speed.

When operating in BSC synchronous mode, ASCII or EBCDIC codes are supported, as well as the transparent text mode. The following code-dependent functions are implemented: 1) character framing via SYN characters, 2) recognition of transparent/non-transparent text mode transitions, and 3) strip/insertion of idle time-fill characters.

Synchronous clocks are strap-selectable on the module. The terminal port (DCE) receive clock can be selected from the receive or the transmit clocks supplied by the Data Terminal Equipment (up to 9600 bps), or else from a set of six clocks supplied on the TP module itself: 1200, 2400, 3600, 4800, 7200, or 9600 bps. The terminal port transmit clock can be selected as the DTE transmit clock, or it can be the same as the terminal port receive clock. Output transmit and receive clocks are generated from the selected DCE receive clock.

2.4.5.1 TP MODULE LAYOUT.

When the TP card is plugged in the port nest, the upper connector is for the J1 channel, the lower for J2. Strapping locations and the ASTRO for each channel are illustrated in Figure 2-31. Strapping platform U5 is common to both channels; the clock sources and control signal delays for each channel are shown in Figure 2-32.

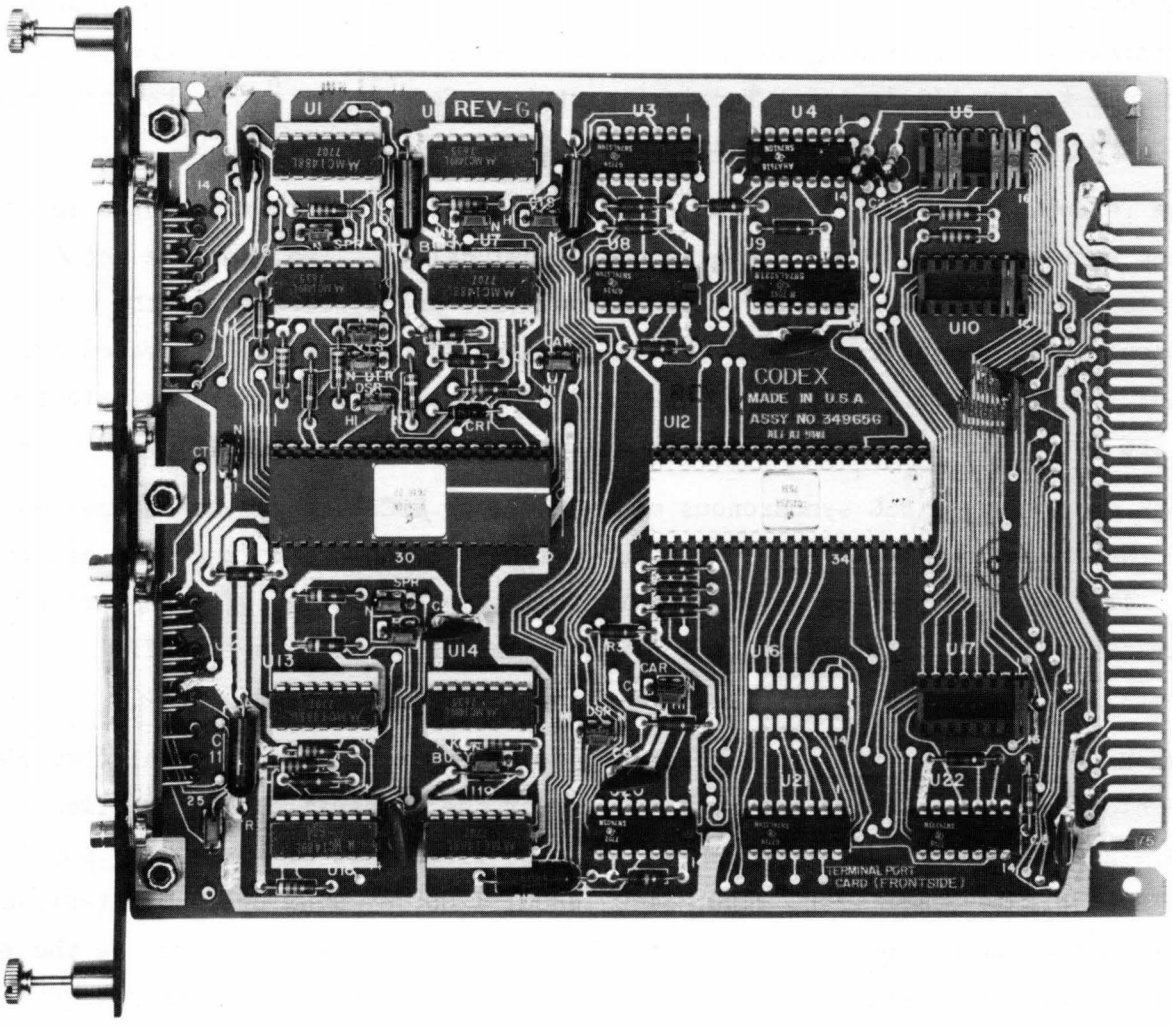


Figure 2-30. Standard (Dual Universal) Terminal Port Module

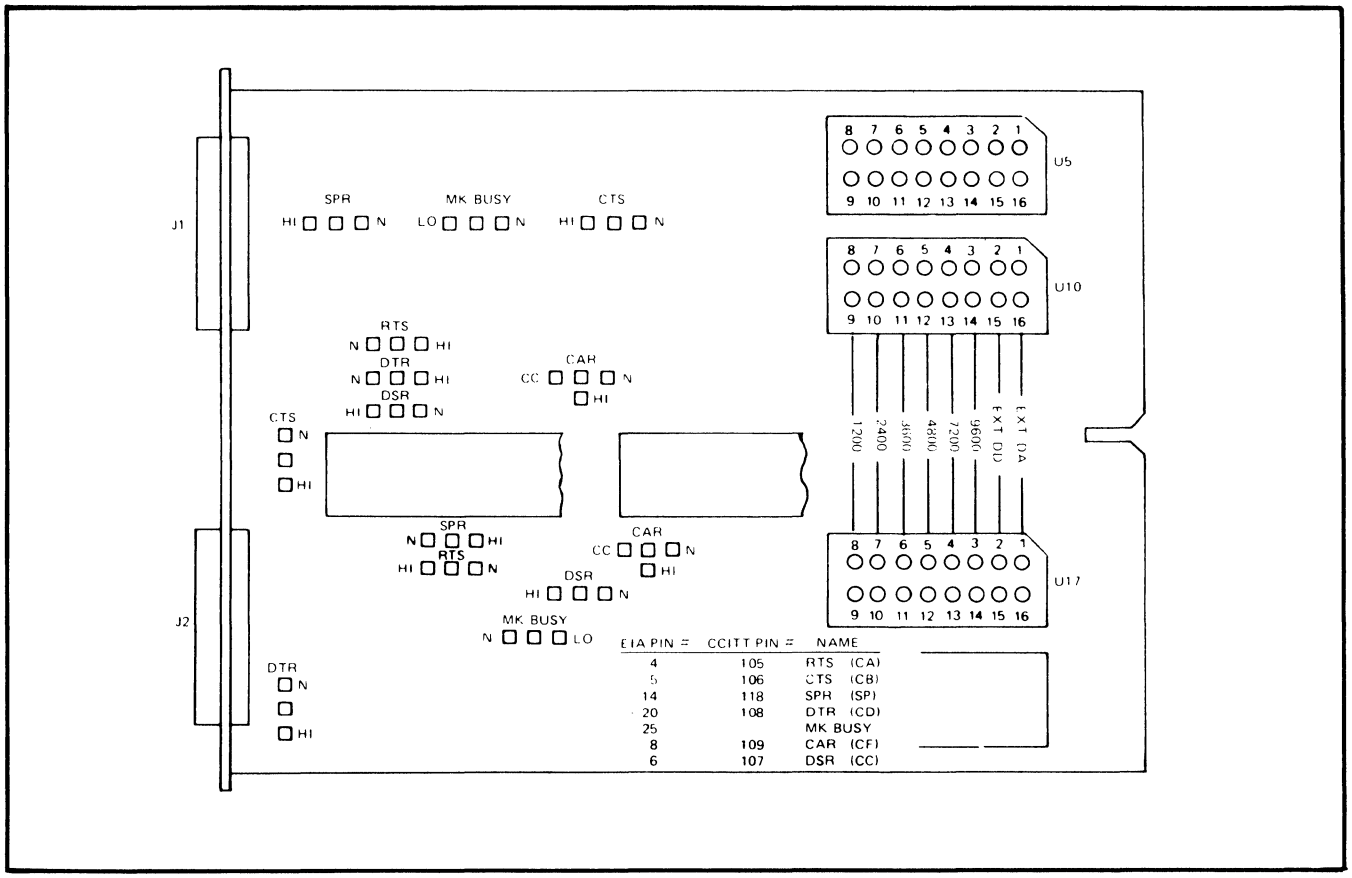


Figure 2-31. Terminal Port Strap Locations

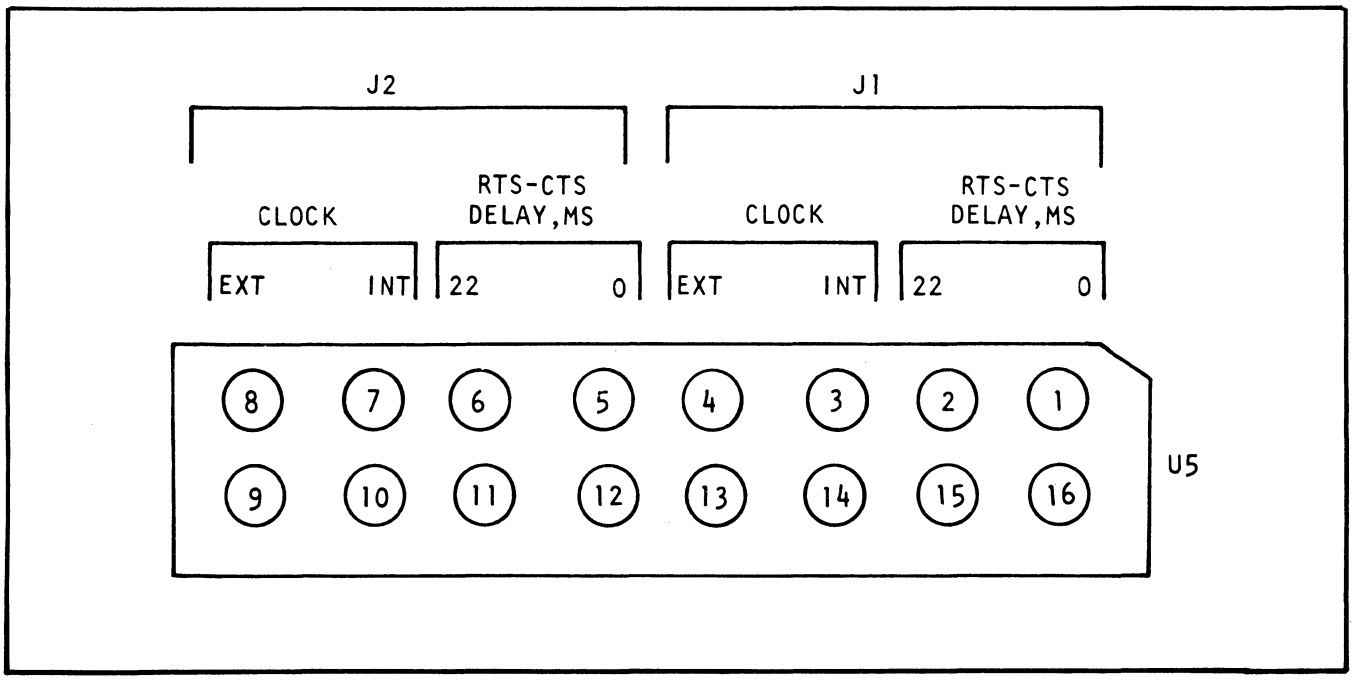


Figure 2-32. TP U5 Platform Strapping Points

2.4.5.2 CONTROL SIGNAL STRAPPING (See Figure 2-33). Two strapping positions are provided for all control signals except Carrier (CF), which has three positions.

2.4.5.2.1 Input Control Signals.

a) SPR (spare) may be strapped either Normal or HI. In the N position SPR is driven from pin 14 of the EIA interface; in the HI position SPR is held active.

b) MK BSY (busy in) may be strapped either Normal or LO. In the N position MK BSY is driven from pin 25 of the EIA interface; in the LO position it is inactive.

c) RTS (ready to send) may be strapped Normal or HI. In the N position it is driven from pin 4 of the EIA interface; in the HI position it is held active.

d) DTR (data terminal ready) may be strapped either Normal or HI. In the N position it is driven from pin 20 of the EIA interface; in the HI position it is held active.

2.4.5.2.2 Output Control Signals.

a) DSR (data set ready) may be strapped either Normal or HI. In the N position, pin 16 of the ASTRO drives pin 6 of the EIA interface. If DSR is in the HI position, pin 6 of the EIA interface is held active.

b) CAR (carrier detect) may be strapped in one of three positions: N, CC, or HI. If it is strapped N, pin 38 of the ASTRO drives pin 8 of the EIA interface; if it is strapped CC, pin 16 of the ASTRO drives pin 8 of the EIA interface. If it is strapped HI, pin 8 of the EIA interface is held active.

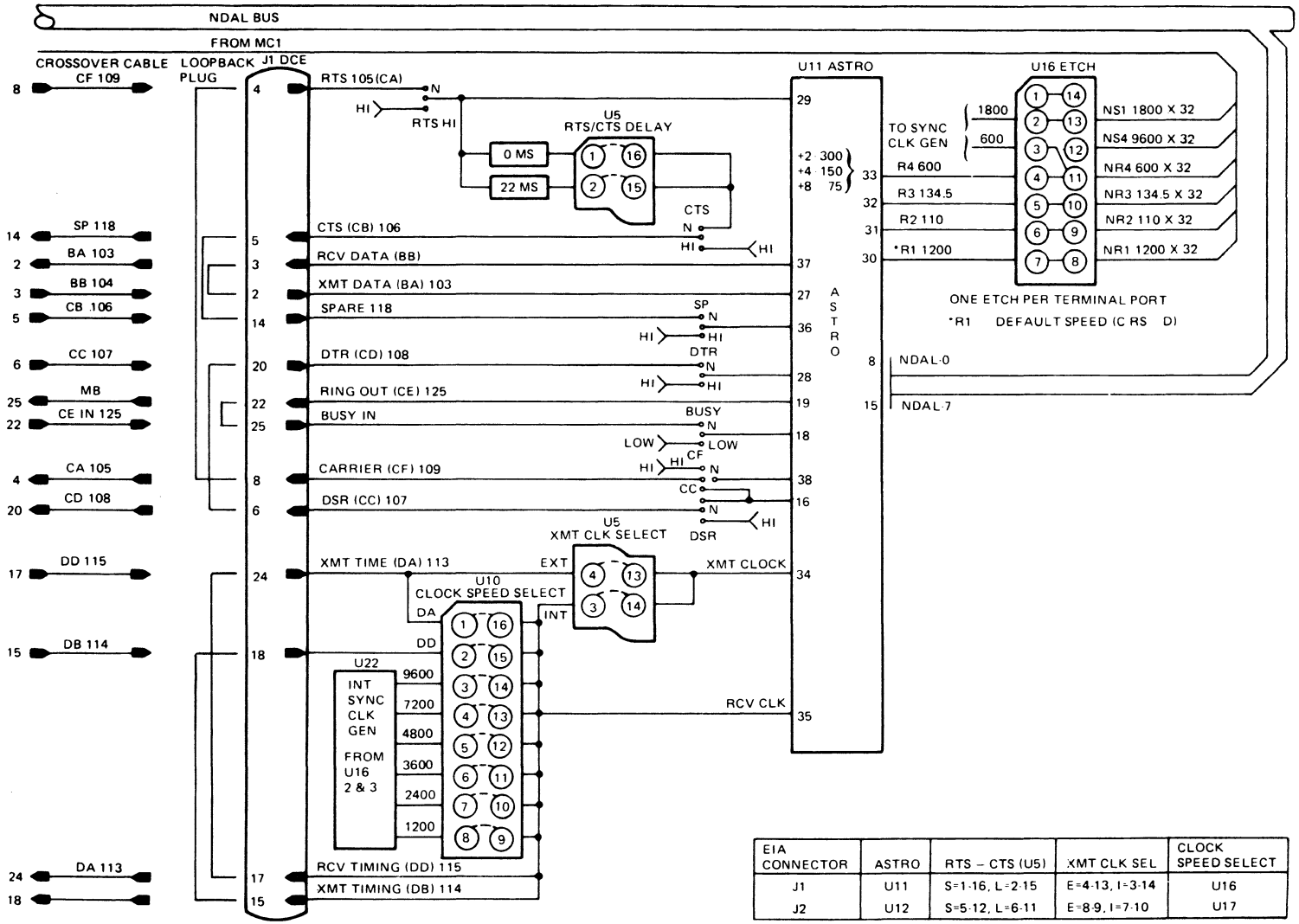
c) CTS (clear to send) may be strapped either Normal or HI. In the N position, pin 5 of the EIA interface is driven by pin 4 of the EIA interface, and CTS may be delayed. (The delay is described below.) In the HI position, pin 5 of the EIA interface is held active.

2.4.5.2.3 RTS/CTS Delay.

a) A 22-ms delay is introduced in the RTS/CTS turnaround if CTS is strapped N and U5-2 to -15 (for the J1 channel) or U5-6 to -11 (for the J2 channel).

b) No delay is introduced in the RTS/CTS turnaround if CTS is strapped N and U5-1 to -16 (for the J1 channel) or U5-5 to -12 (for the J2 channel).

2.4.5.3 CLOCK SPEED STRAPPING. System clock is supplied by the modem or by the sync clock generator. Figure 2-33 shows the strapping positions used to select the appropriate speeds.



EIA CONNECTOR	ASTRO	RTS – CTS (U5)	XMT CLK SEL	CLOCK SPEED SELECT
J1	U11	S=1-16, L=2-15	E=4-13, I=3-14	U16
J2	U12	S=5-12, L=6-11	E=8-9, I=7-10	U17

Figure 2-33. Dual Universal Terminal Port J1 Channel Signals

2.4.5.3.1 External Transmit Clock. Synchronous transmit clock speeds are supplied internally by the synchronous clock generator U22 on the port card. Figure 2-33 shows the strap positions to select the appropriate speeds. The J1 channel is strapped on platform U10, J2 on U17. The two channels are identical so the figure serves to illustrate both. The signal at ASTRO pin 35 also drives pins 15 and 17 of the EIA interface.

2.4.5.3.2 External Receive Clock.

a) Receive clock (DB) generated externally (usually by the modem) is provided to ASTRO pin 34 by strapping the J1 channel U5-4 to -13 and the J2 channel U5-8 to -9.

b) The signal at EIA pin 24 provides external transmit clock for the J1 channel by strapping U5-3 to -14 and for the J2 channel by strapping U5-8 to -9.

2.4.5.3.3 External Receive and Transmit Clock from EIA Pin 24.

a) Both receive and transmit clock are provided by J1 EIA pin 24 by removing the U10 strap and strapping U5-3 to -14 and U5-4 to -13.

b) Both receive and transmit clock are provided by J2 channel EIA pin 24 by removing the U17 strap and strapping U5-7 to -10 and U5-8 to -9.

2.4.6 ACTIVITY INDICATOR TERMINAL PORT - Option 6131

Option 6131 performs the same functions as the standard (dual universal) terminal port module.

2.4.6.1 FEATURES. The activity indicator terminal port incorporates the following enhancements:

- Four LEDs are mounted on the rail of the card. They show input and output signal activity for each channel on the card.
- Control signal strapping capabilities have been improved.
- The new board layout facilitates installation of small scale, customer-special circuitry. A three-DIP subassembly can be cleanly mounted on board and connected by wirewrap.
- The EIA drivers are supplied with ±9V instead of ±12V, which increases reliability and MTBF.

Like the standard (dual universal) terminal port, Option 6131 is strappable to select clock sources and rates and to activate control signals and associated delays.

2.4.6.2 MODULE LAYOUT. When the module is plugged into the port nest, the J1 connector is on top, J2 is below. All circuitry and strapping platforms for each channel are located on the associated (upper or lower) half of the board. Figure 2-34 is a photograph of the board; Figure 2-35 specifies the strapping locations.

2.4.6.3 CONTROL SIGNAL STRAPPING. Two strapping positions are provided for all control signals except Carrier (CF), which has three positions.

2.4.6.3.1 Input Control Signals.

a) SPR (spare) may be strapped either Normal or ON. In the N position SPR is driven from pin 14 of the EIA interface; in the ON position SPR is held active.

b) MK BSY (busy in) may be strapped either Normal or OFF. In the N position MK BSY is driven from pin 25 of the EIA interface; in the OFF position it is inactive.

c) RTS (ready to send) may be strapped Normal or ON. In the N position it is driven from pin 4 of the EIA interface; in the ON position it is held active.

d) DTR (data terminal ready) may be strapped either Normal or ON. In the N position it is driven from pin 20 of the EIA interface; in the ON position it is held active.

2.4.6.3.2 Output Control Signals.

a) DSR (data set ready) may be strapped either Normal or ON. In the N position, pin 16 of the ASTRO drives pin 6 of the EIA interface. If DSR is in the ON position, pin 6 of the EIA interface is held active.

b) CAR (carrier detect) may be strapped in one of three positions: N, CC, or ON. If it is strapped N, pin 38 of the ASTRO drives pin 8 of the EIA interface; if it is strapped CC, pin 16 of the ASTRO drives pin 8 of the EIA interface. If it is strapped ON, pin 8 of the EIA interface is held active.

c) CTS (clear to send) may be strapped either Normal or ON. In the N position, pin 5 of the EIA interface is driven by pin 4 of the EIA interface, and CTS may be delayed. (The delay is described below.) In the ON position, pin 5 of the EIA interface is held active.

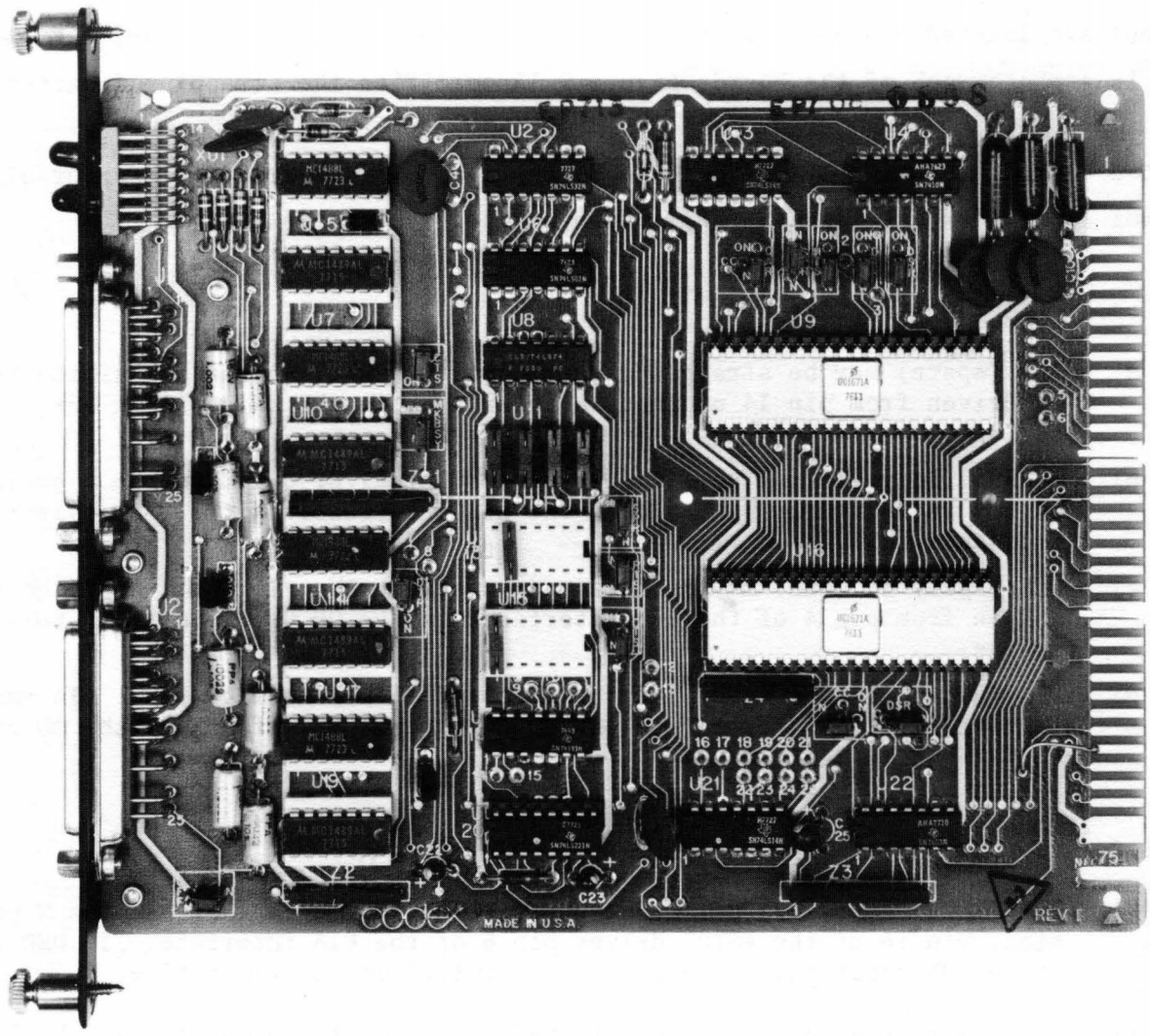


Figure 2-34. Activity Indicator Terminal Port

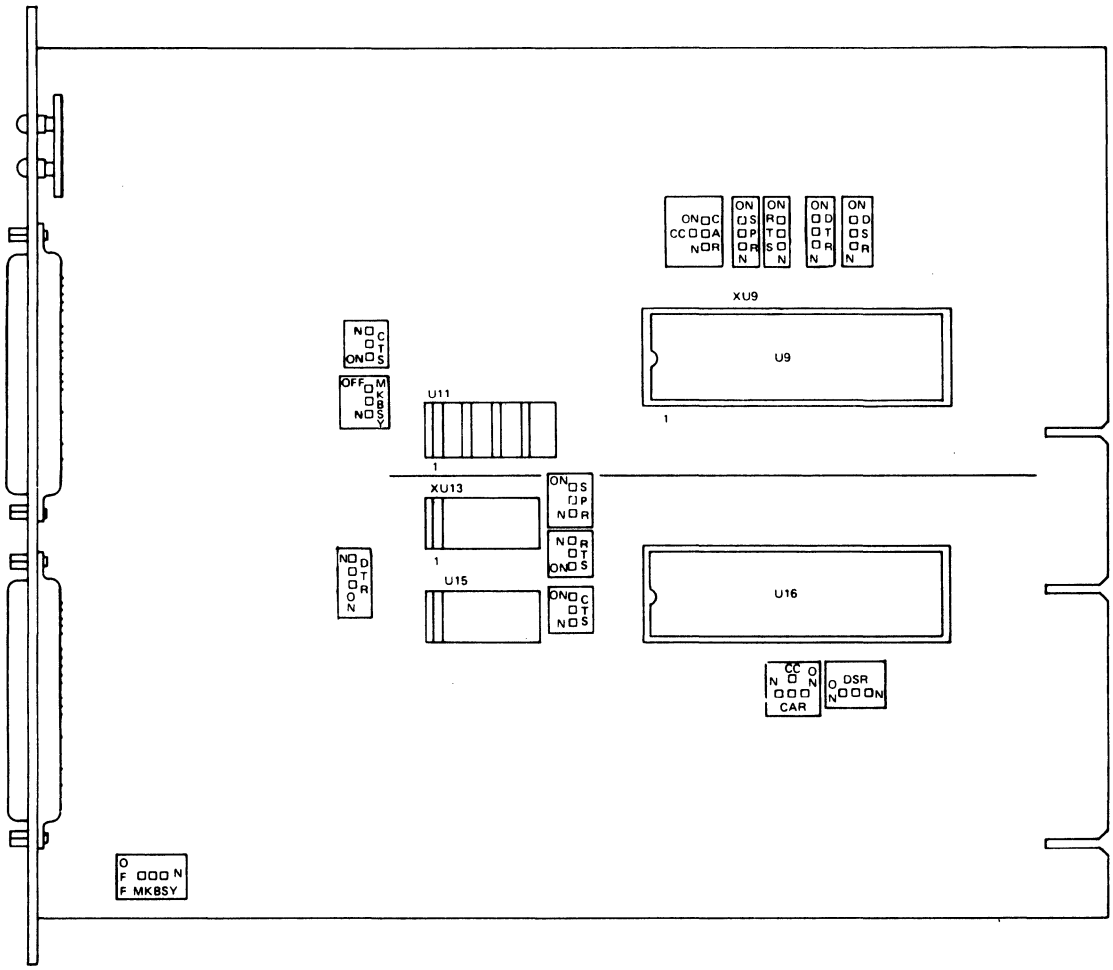


Figure 2-35. Activity Indicator Terminal Port Strap Locations

2.4.6.3.3 RTS/CTS Delay.

a) A 22-ms delay is introduced in the RTS/CTS turnaround if CTS is strapped N and U11 is strapped U11- 12 to -5 (for the J1 channel) or U11-1 to -16 (for the J2 channel).

b) No delay is introduced in the RTS/CTS turnaround if CTS is strapped N and U11 is strapped U11-6 to -11 (for the J1 channel) or U11-2 to -15 (for the J2 channel).

2.4.6.4 CLOCK SPEED STRAPPING. System clock is supplied by the modem or by the sync clock generator. Figure 2-36 shows the strapping positions used to select the appropriate speeds.

2.4.6.4.1 External Transmit Clock. Synchronous transmit clock speeds are supplied internally by the synchronous clock generator U22 on the port card. Figure 2-36 shows the strap positions to select the appropriate speeds. The J1 channel is strapped on platform U13, J2 on U15. The two channels are identical so the figure serves to illustrate both. The signal at ASTRO pin 35 also drives pins 15 and 17 of the EIA interface.

2.4.6.4.2 External Receive Clock.

a) Receive clock (DB) generated externally (usually by the modem) is provided to ASTRO pin 34 by strapping the J1 channel U11-8 to -9, and the J2 channel U11-4 to -1.

b) The signal at EIA pin 24 provides external transmit clock for the J1 channel by strapping U11-7 to -10, for the J2 channel by strapping U11-3 to -14.

2.4.6.4.3 External Receive and Transmit Clock from EIA Pin 24.

a) Both receive and transmit clock are provided by 1 channel EIA pin 24 by removing the U13 strap and strapping U11-7 to -10 and U11-8 to -9.

b) Both receive and transmit clock are provided by J2 channel EIA pin 24 by removing the U13 strap and strapping U11-3 to -14 and U11-4 to -13.

2.4.6.5 ACTIVITY INDICATOR LED DISPLAY. There are four LEDs mounted on the rail of each activity indicator terminal port module. The two LEDs on the left are associated with the J1 channel and the two on the right with the J2 channel. The top two LEDs indicate output activity and the bottom two indicate input activity.

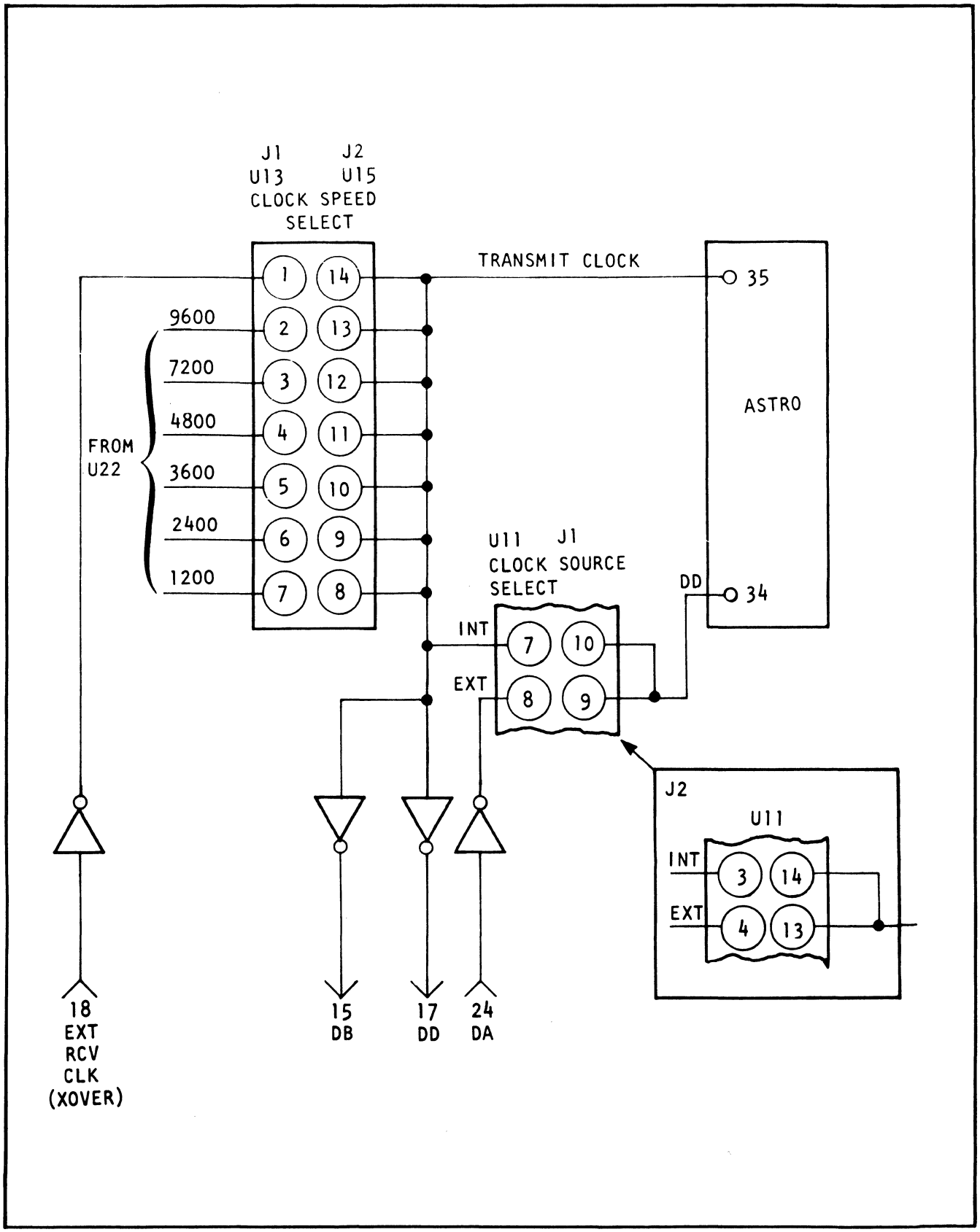


Figure 2-36. Clock Speed and Source Strap Locations

Table 2-6 summarizes the LED conditions. Each LED responds to three signals: a primary control signal, a secondary control signal, and a data signal. For an output indicator the primary control signal is DSR; the secondary control signal is CARRIER and the data signal is BB. For an input indicator the primary control signal is DTR, the secondary control signal is RTS, and the data signal is BA.

An LED will be ON if its primary control signal is active and its secondary control signal or its data signal is inactive. (A data signal is inactive if marking). An LED will be OFF if its primary control signal is inactive or if its primary control signal, secondary control signal, and data are all active. All control signals are detected at the ASTRO interface; not at the EIA interface. Under normal active conditions, a channel will have its primary and secondary control signals active while its data signal transitions between mark and space. The associated LED will blink on and off in this situation.

2.4.7 DUAL CURRENT LOOP PORT - Option 6150

The current loop terminal port module, Figure 2-37, provides two independent current loop interfaces to two current loop data terminals, such as send-receive teleprinters, at standard asynchronous speeds.

TABLE 2-6. LED CONDITIONS

	Primary Control Signal	Secondary Control Signal	Data Signal	LED State
Output	DSR	CAR	BB	
	Inactive	Don't care	Don't care	Off
	Active	Inactive	Don't care	On
	Active	Active	Space 0	Off
	Active	Active	Mark 1	On
Input	DTR	RTS	BA	
	Inactive	Don't care	Don't care	Off
	Active	Inactive	Don't care	On
	Active	Active	Space 0	Off
	Active	Active	Mark 1	On

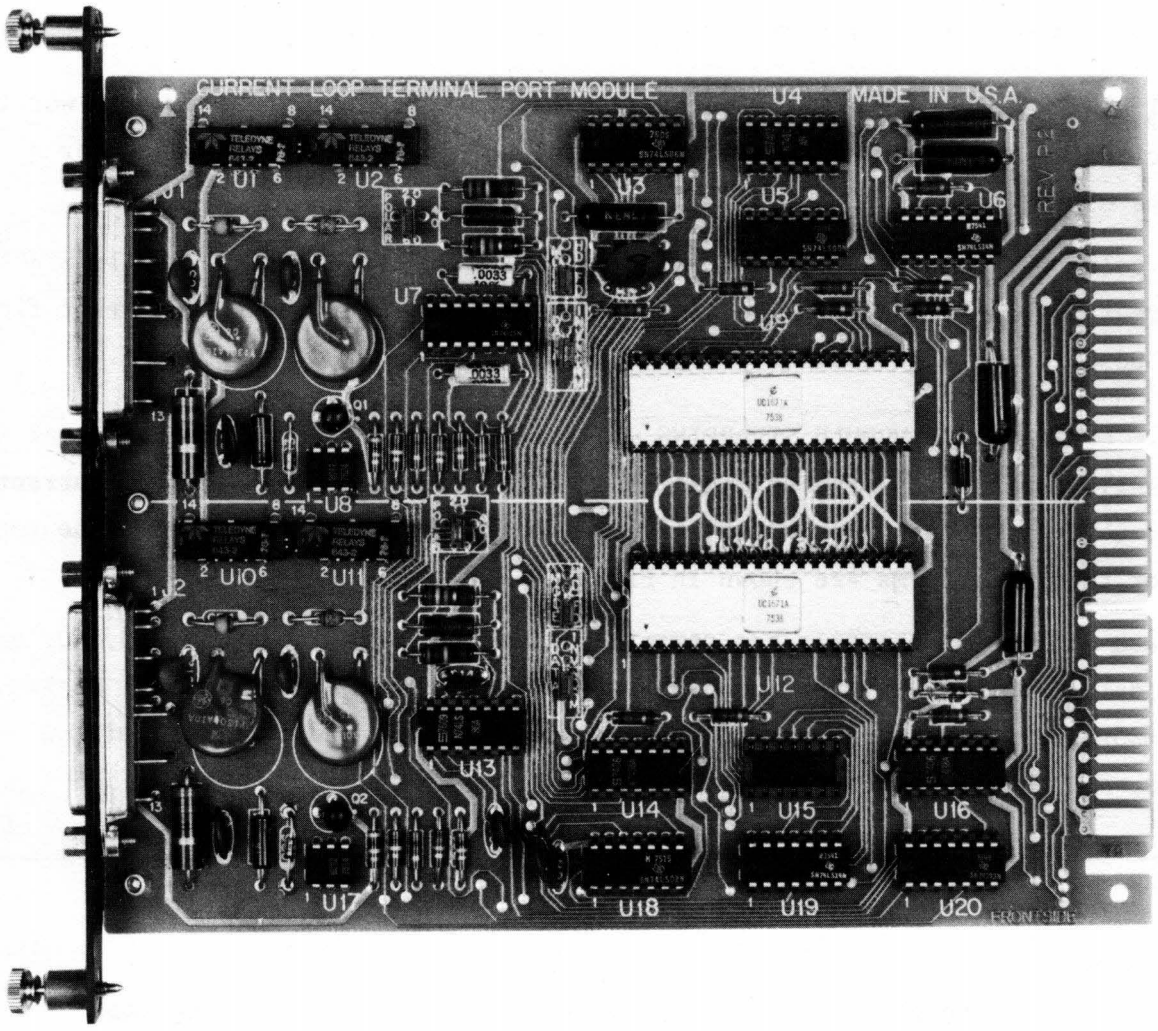


Figure 2-37. Current Loop Port

Such terminals are asynchronous and operate either half-duplex or full-duplex. The maximum voltage swing is 180 Vdc with neutral signaling or 85 Vdc with polar signaling, and the maximum standard current is 60 mA. The high voltage is used by common carriers and customers who need it to transmit over substantial distances, (over 1500 feet). The loop current compensates for resistance in the wire and the interface for the terminal equipment; it must provide 20 to 25 mA at the receiving terminal to minimize noise from the contacts in the terminal.

2.4.7.1 CURRENT LOOP SIGNALS. The signals may be either polar or neutral working, as required by the attached terminal. Neutral working signals may be either positive or negative.

In polar working signals, MARK is current flow in one direction, while SPACE is current flow in the other direction. In neutral working, MARK is current flow, either positive or negative, (see Figure 2-38) while SPACE is no current.

2.4.7.2 CURRENT LOOP MODULE STRAPPING. The accommodation to polar or neutral working signals generated by the terminal, and to the customer-provided loop current, is made by performing the appropriate strapping on platforms on the board. The locations of these platforms are shown in Figure 2-39.

Each of the two channels has strap positions for polar current: 20, 40, or 60 mA; data: normal or invert; and operating mode: half-duplex or full duplex. The common carrier normally provides the dc power source and current limiting devices.

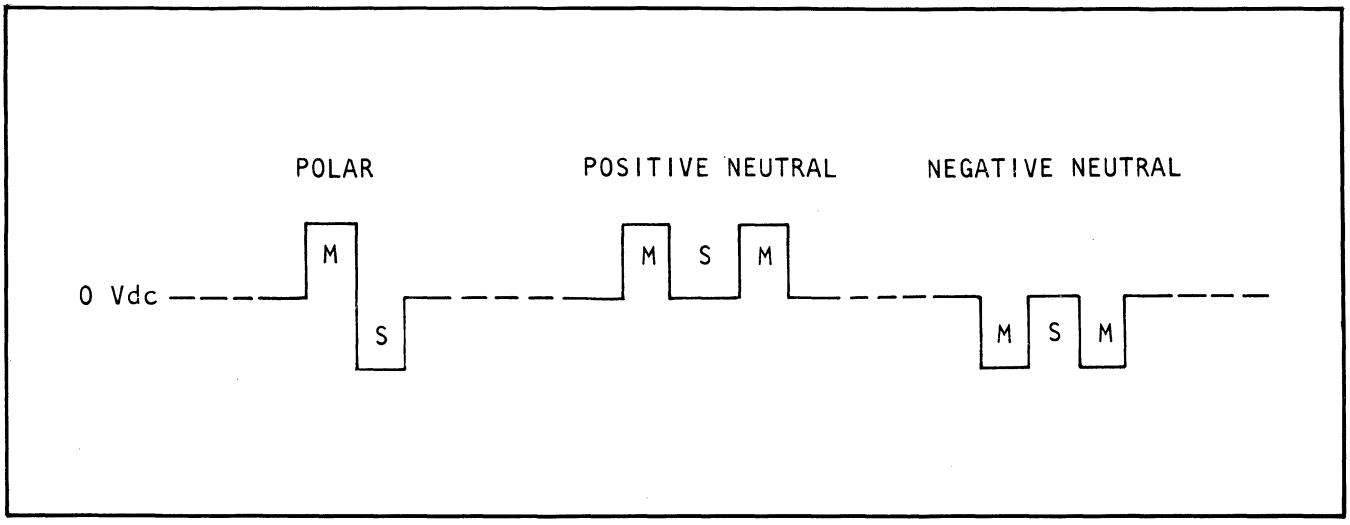


Figure 2-38. Current Loop Signals

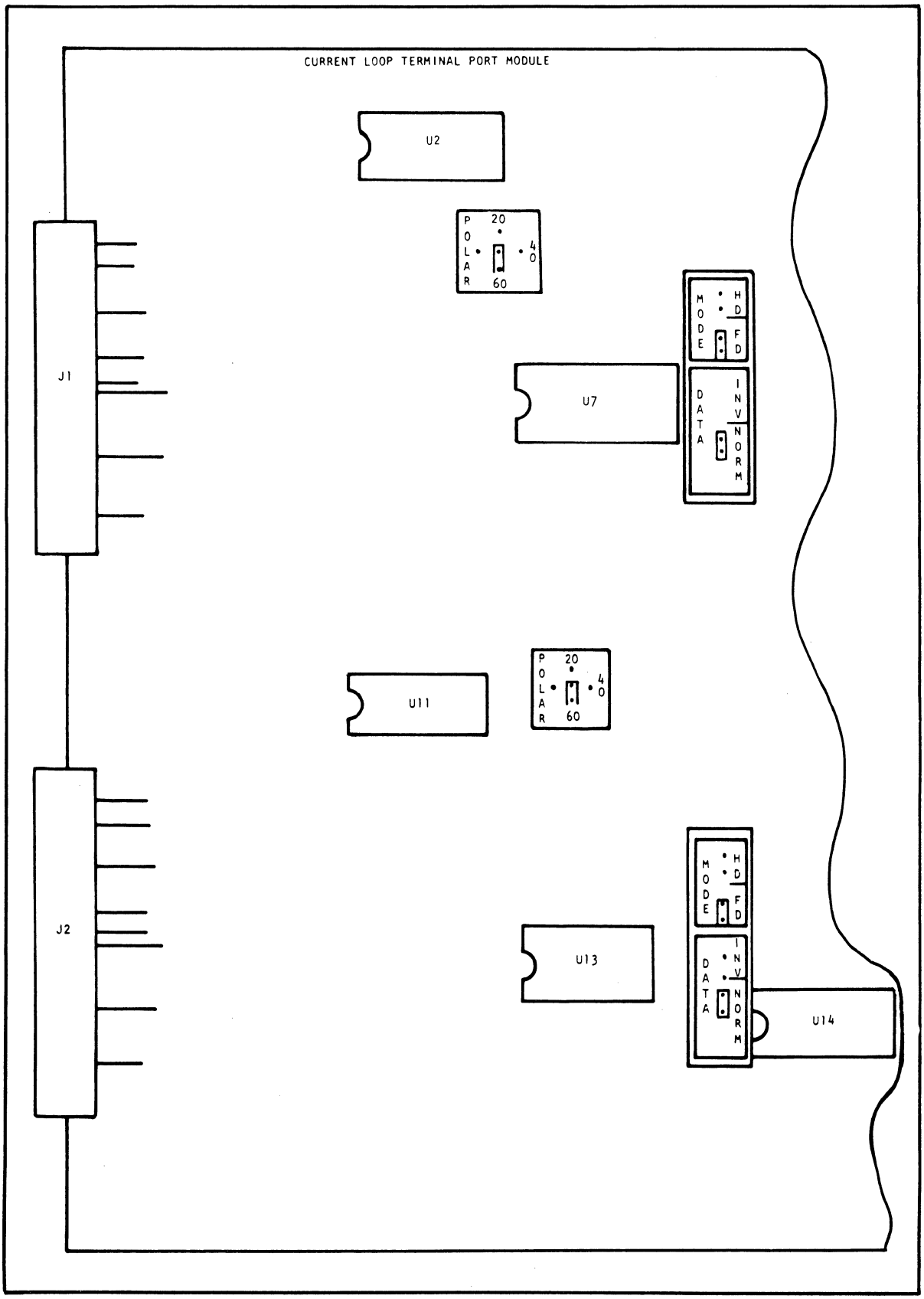


Figure 2-39. Current Loop Port Strapping Locations

2.4.7.2.1 Loop Current Strapping. The current loop module, when strapped for polar current, operates within ±15% of the nominal value strapped.

2.4.7.2.2 Data Strapping. Strapping data allows the module to accept either NORMal data or INVerted data. Normal data is shown in Figure 2-37; inverted data changes the current flow for MARK to zero, and the current flow for SPACE to flow in either direction.

2.4.7.2.3 Mode Strapping. This strapping allows the module to operate in the same mode as the attached terminal: full duplex or half-duplex.

2.4.7.3 ACCESSORIES. To prevent the mistake of connecting an EIA connector to a current loop port, the male and female connectors have been exchanged. The female is on the current loop cable, not on the card. The card connectors are male.

A 40-inch cable with a standard 25-pin EIA connector at one end, and a terminal block at the other end (Figure 2-40) is also available. The EIA connector (of which only 5 pins are active) plugs into the current loop port connector at the rear of the INP port nest. The terminal block at the other end of the cable mounts into a specially designed connector panel which is also available as an accessory.

The terminal block panel is designed to mount into vertical mounting rails at the rear of a rack cabinet. It contains 16 slots into which current loop terminal blocks may be mounted, allowing up to 16 current loop ports to be supported by one panel. Cabling of current loop DTE's to the current loop panel rather than the port nest will eliminate accidental connection of high current loop voltage to an EIA port module.

Upon completion of any current loop port installation, be sure to install the protective covers over the port nest backplane and terminal block panel. Each is used to protect operators and maintenance personnel from the high voltage present at the backplane etches and terminals.

The covers are held in place by a set of spacers and screws.

WARNING

Avoid contact with etches and terminals while installing the covers. Dangerous voltage is present on the terminals.

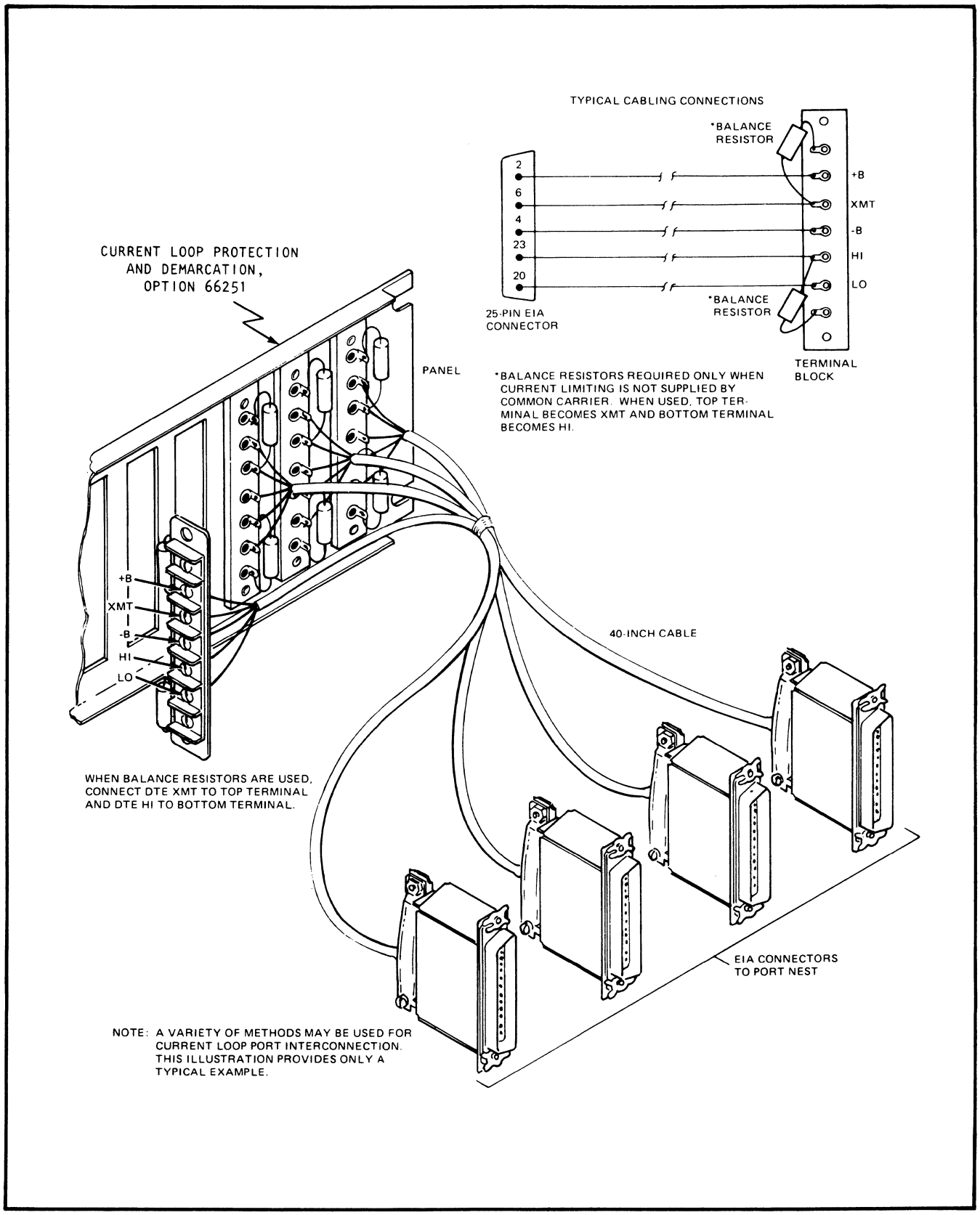
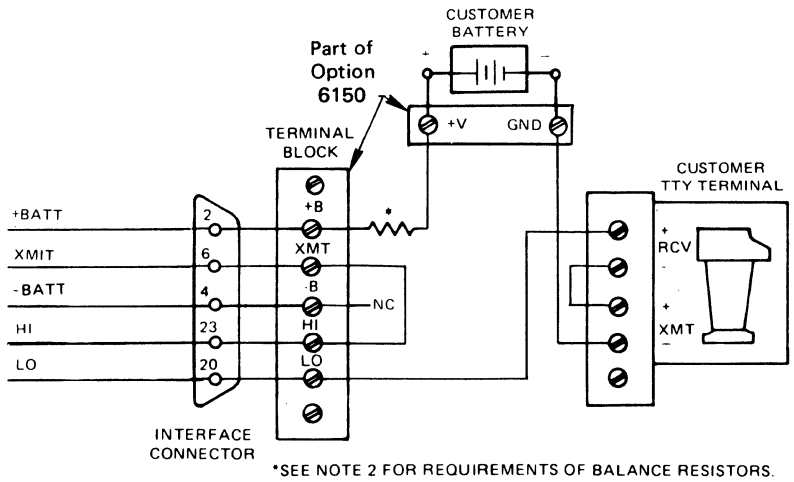


Figure 2-40. Current Loop Cabling Accessories

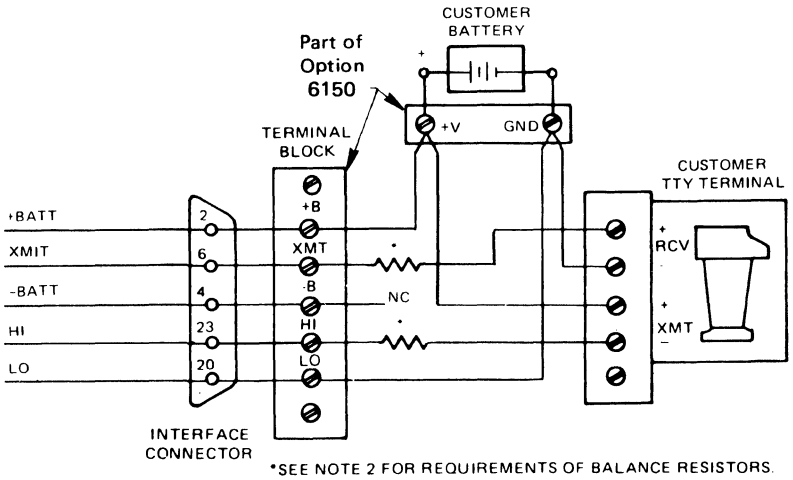
2.4.7.4 CONNECTION TO USER. Cabling between a current loop port module and associated data terminal can be connected in a variety of configurations according to customer requirements. Figures 2-41 through 2-43 show the more common configurations.

- Positive neutral loop, half duplex: see Figure 2-41.
- Positive neutral loop, full duplex: see Figure 2-42.
- Polar loop: see Figure 2-43.



NOTES:
1. SET NORMAL/INV DATA STRAPPING TO NORMAL.
2. BATTERY, CURRENT LIMITING, AND INDICATOR FUSES ARE NORMALLY PROVIDED BY COMMON CARRIER. IF NOT, A BALANCE RESISTOR MUST BE INSTALLED TO LIMIT CURRENT ACCORDING TO CUSTOMER REQUIREMENTS.
3. FD/HD STRAPPING TO HD.

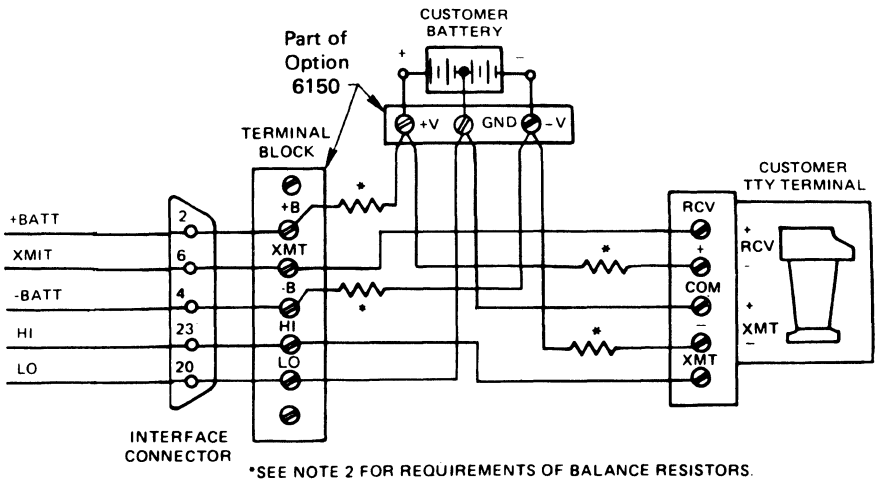
Figure 2-41. Positive Neutral Loop, Two Wire Half-Duplex Operation



NOTES:

1. SET NORMAL/INV DATA STRAPPING TO NORMAL.
2. BATTERY, CURRENT LIMITING, AND INDICATOR FUSES ARE NORMALLY PROVIDED BY COMMON CARRIER. IF NOT, BALANCE RESISTORS MUST BE INSTALLED TO LIMIT CURRENT ACCORDING TO CUSTOMER REQUIREMENTS.
3. FD/HD STRAPPING TO FD.

Figure 2-42. Positive Neutral Loop, Four Wire Full-Duplex Operation



NOTES:

1. SET NORMAL/INV DATA STRAPPING ACCORDING TO CUSTOMER EQUIPMENT. FOR NEGATIVE POLAR OPERATION, COMMON IN ENGLAND, AUSTRALIA AND ELSEWHERE, SET NORMAL/INV DATA TO INV
2. BATTERY, CURRENT LIMITING, AND INDICATOR FUSES ARE NORMALLY PROVIDED BY COMMON CARRIER. IF NOT, BALANCE RESISTORS MUST BE INSTALLED TO LIMIT CURRENT ACCORDING TO CUSTOMER REQUIREMENTS.
3. FD/HD STRAPPING TO FD.

Figure 2-43. Polar Loop Operation

CHAPTER 3

INP INSTALLATION

3.1 INTRODUCTION

Each model of a 6030/6040 INP has a basic physical configuration, described briefly in Chapter 1, with the components detailed in Chapter 2. Here we are concerned only with the mechanical and electrical requirements for interconnecting the components delivered by the Codex Corporation, and for assuring and verifying their proper operation.

The installation may be performed either by the customer's personnel or by Codex personnel, as determined when the equipment is ordered.

3.2 SITE PREPARATION

The 6030/6040 Series INP's should be installed within 5 feet (1.5 m) of a grounded ac outlet that has no other equipment on the line and is capable of furnishing the appropriate power specified in paragraphs 1.2.5 and 1.2.6. The installation area should be clean, well-lighted, and free from extremes of temperature, humidity, and vibration. One power outlet is required for each power supply in user-supplied racks. If Codex racks are used, only one outlet is required.

It is recommended that no other equipment (except modems) be driven from the electrical circuit used to power the INP.

3.3 INSTALLATION PROCEDURE

Personnel should become familiar with the following installation procedure for 6030/6040 Series INP's before attempting to install the equipment.

3.3.1 UNPACKING

After unpacking the equipment shipping crate, check the contents against the packing list. Inspect the equipment carefully for any damage that may have occurred in shipment.

If any damage is found, contact the shipper's agent. In the event of damage or a material shortage, contact the Codex Corporation, Marketing Operations, 15 Riverdale Avenue, Newton, MA 02195, for advice and assistance.

It is suggested that the shipping crate and packing material be retained for use in future repacking and shipping.

3.4 MECHANICAL ASSEMBLY

3.4.1 TABLETOP MODEL 6030 OR 6040

The only assembly required is the connecting of cabling (see section 3.5.1).

3.4.2 RACK-MOUNTED MODELS

Refer to Figure 3-1. Assembly of rack-mounted equipment is performed by installing the INP hardware in the appropriate racks, then connecting the port nest and power supply cables. Figure 3-2 shows the sequence of modules in the mainframe.

3.4.3 CUSTOMER-PROVIDED RACKS

Users who elect to install a 6030 or 6040 Series INP in their own racks must use installation techniques similar to those described in this manual. Codex Corporation may refuse to service locations where adequate provisions for accessibility, strain relief, and ventilation have not been provided.

3.5 ELECTRICAL ASSEMBLY

Electrical installation consists of connecting all cables according to drawings, verifying that boards in the mainframe and port nest are properly located and seated, and verifying the positions of moveable straps on the boards. Only then should power be applied to the system.

In the mainframe, the edge connectors on the motherboard are keyed to provide dedicated slots for boards, right to left, as follows: option card, MC1, MC2, 8 for processors, and 6 for RAM's and ROM's (see Figure 3-2).

Slots in the port nest are not keyed, but the placement of cards in the nest is subject to a few rules: The nest interface card occupies the leftmost slot, while the next slot is always open. The network port cards follow - NP1 in slot 00/01 and NP2

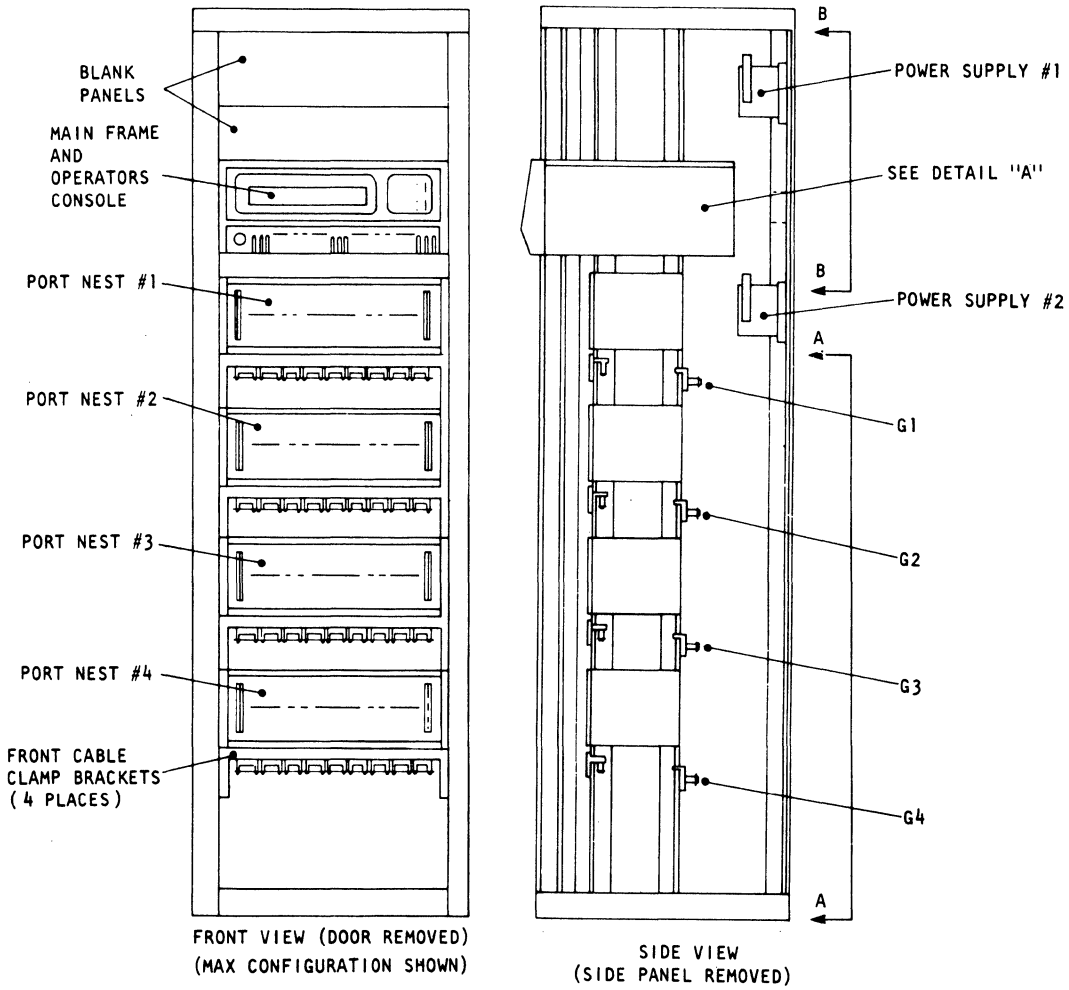


Figure 3-1A. Cabinet Installation

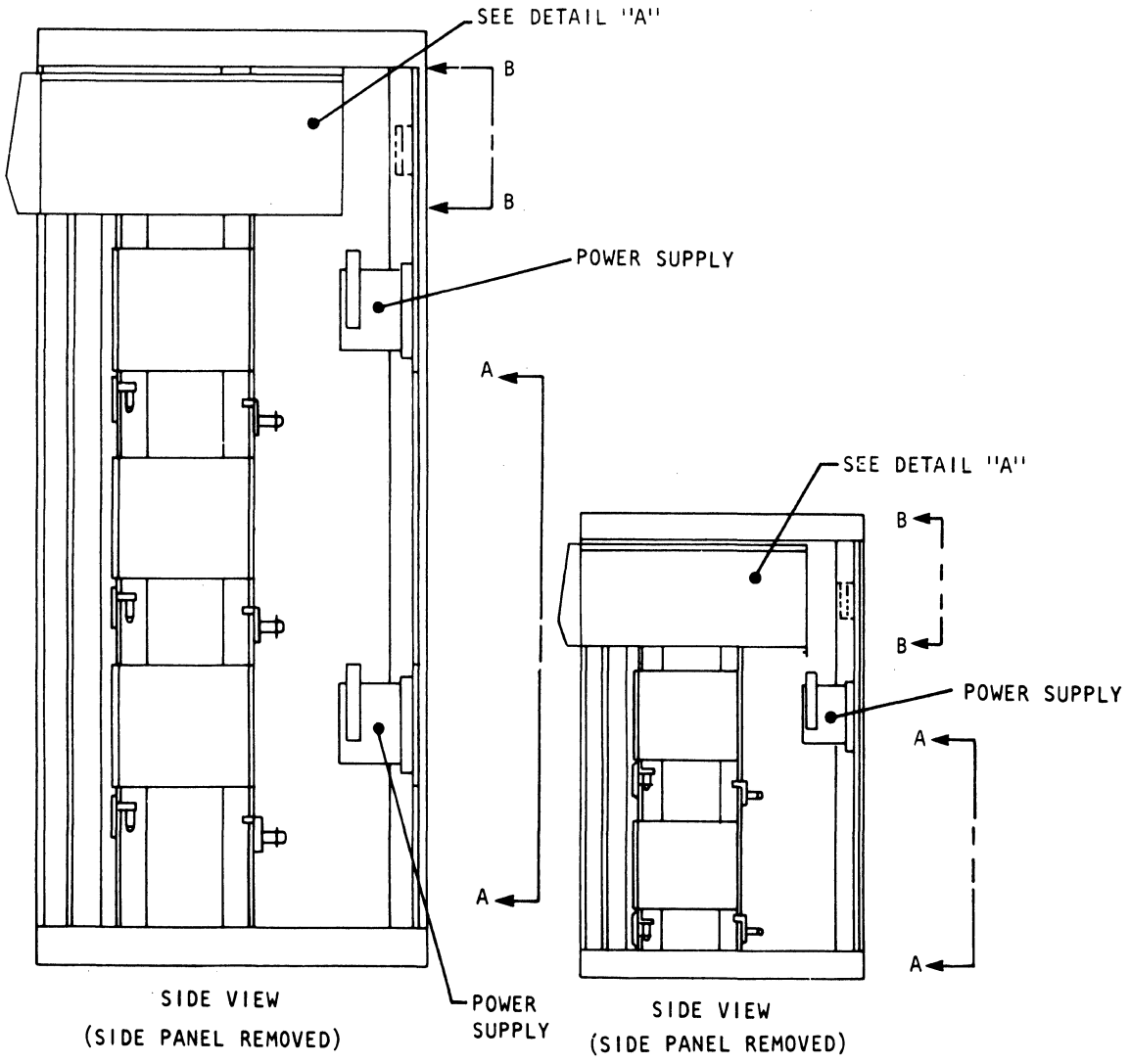


Figure 3-1B. Cabinet Installation

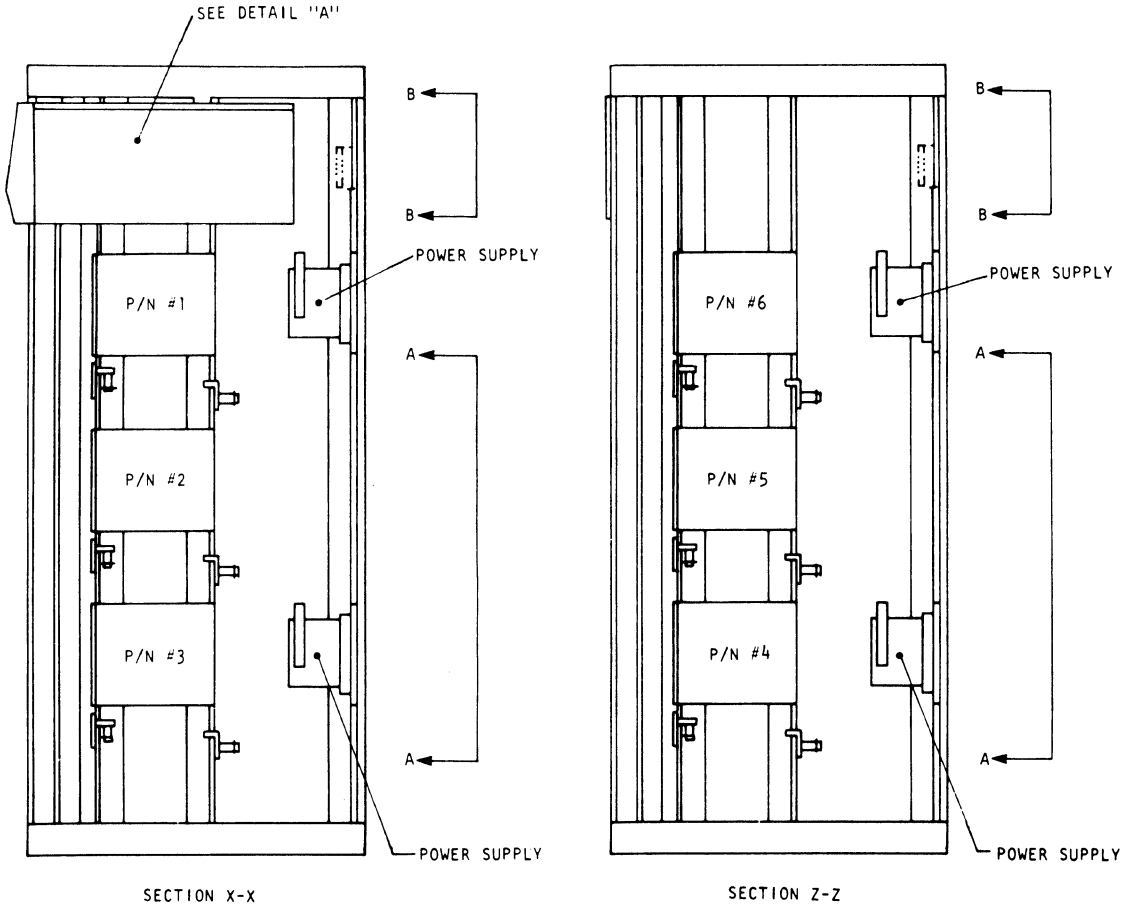


Figure 3-1C. Cabinet Installation

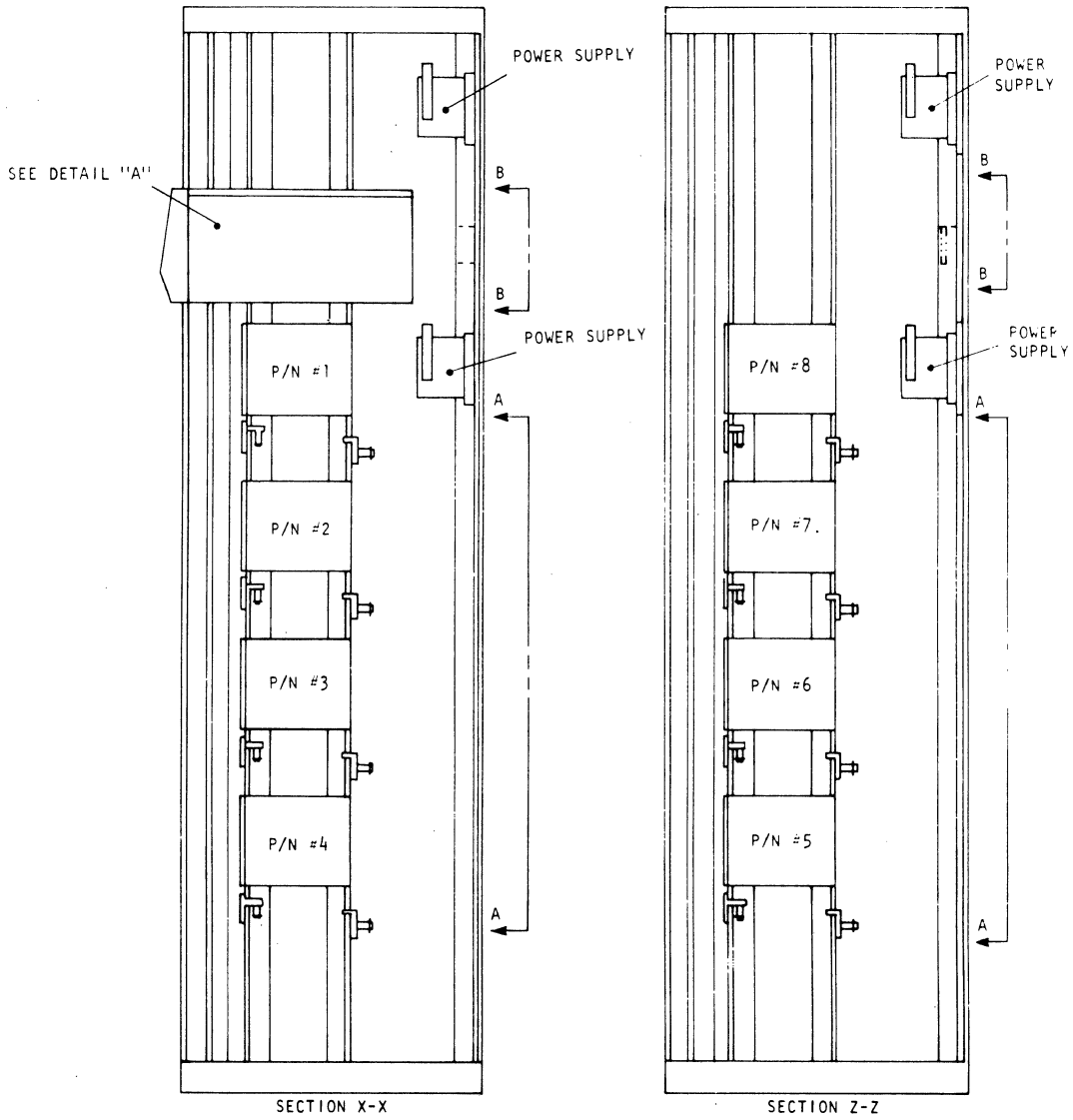
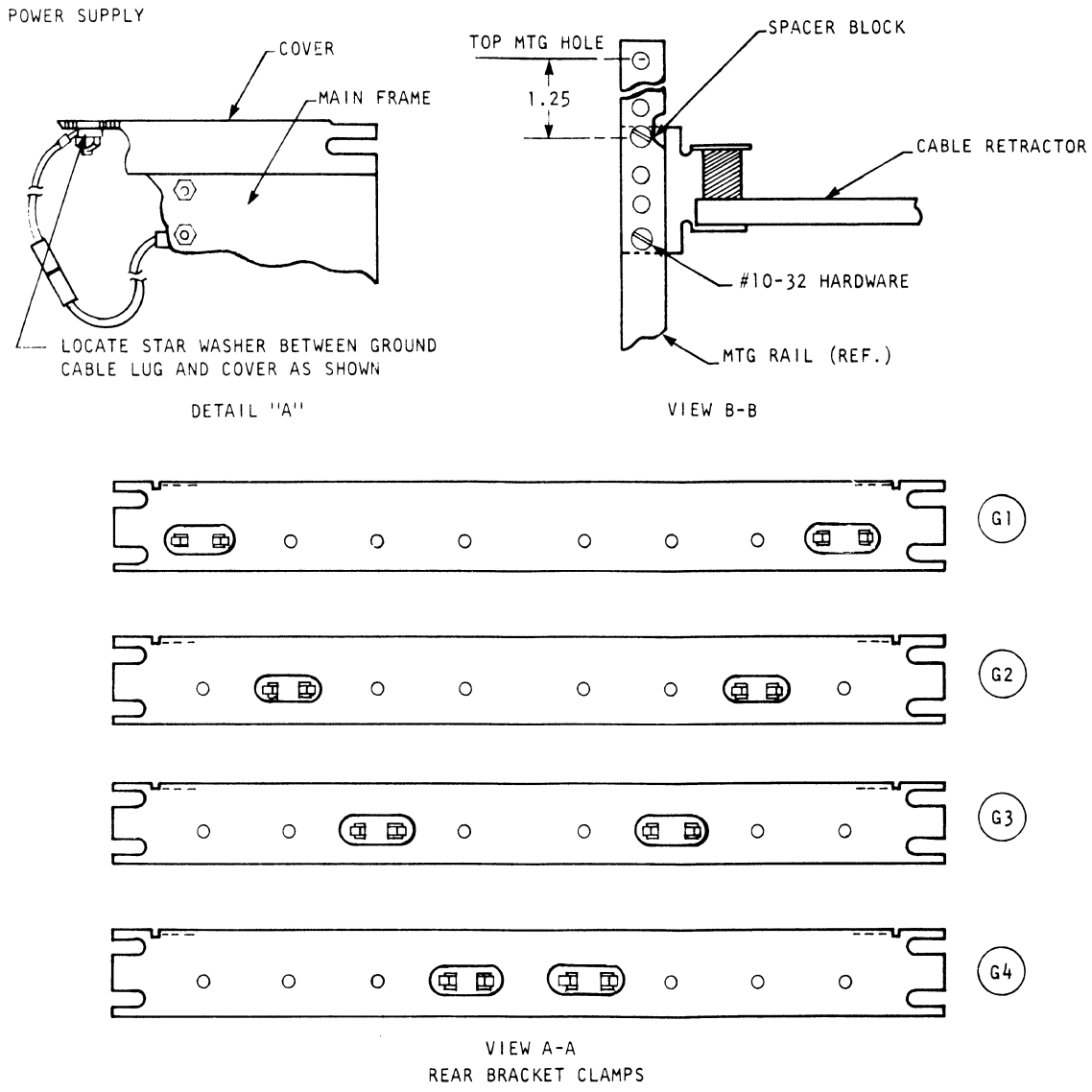


Figure 3-1D. Cabinet Installation



NOTE: It is important that the rear bracket clamps be used as shown to relieve strain on the cable connectors and the circuit boards.

Figure 3-1E. Cabinet Installation

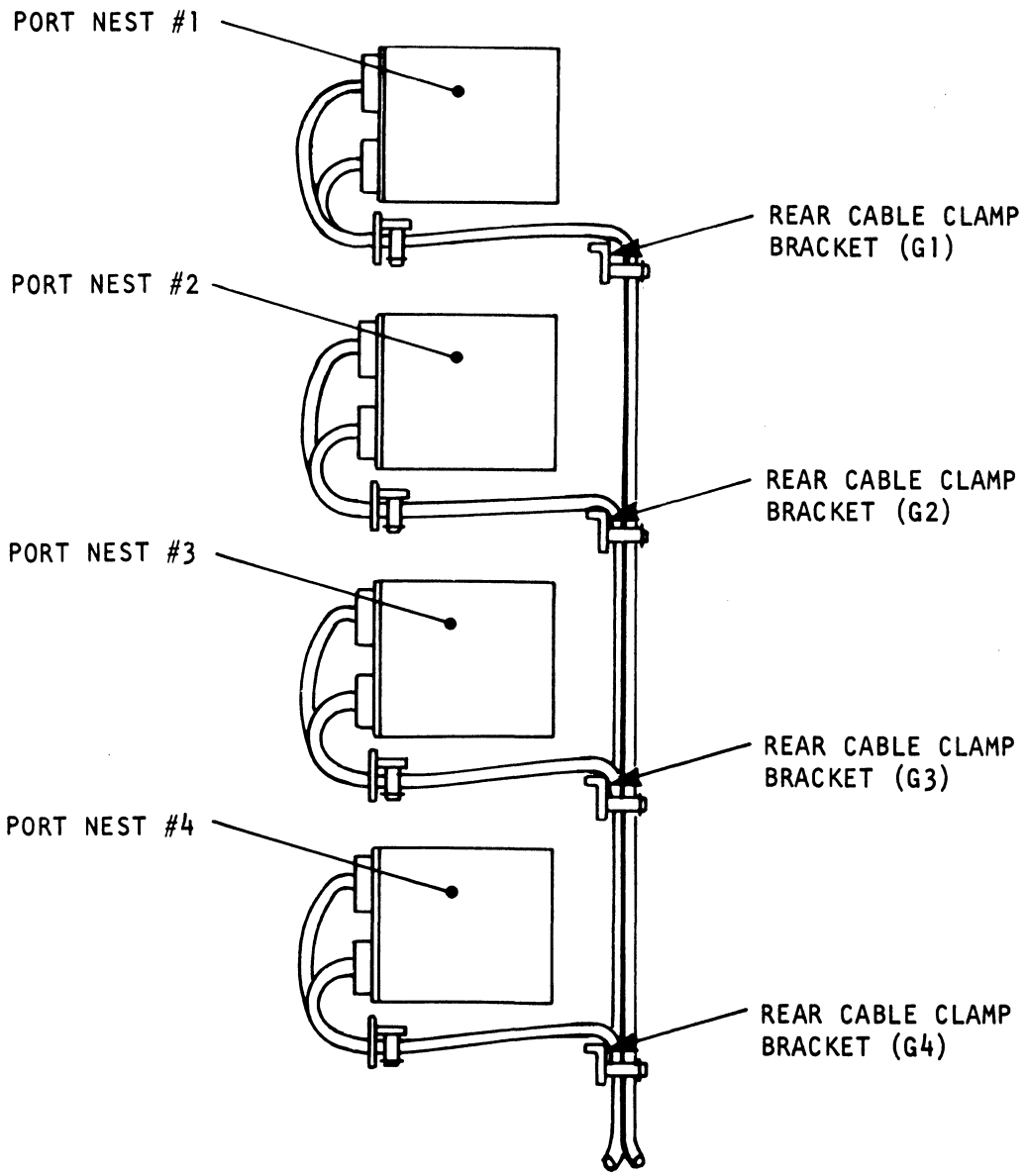


Figure 3-1F. Cabinet Installation

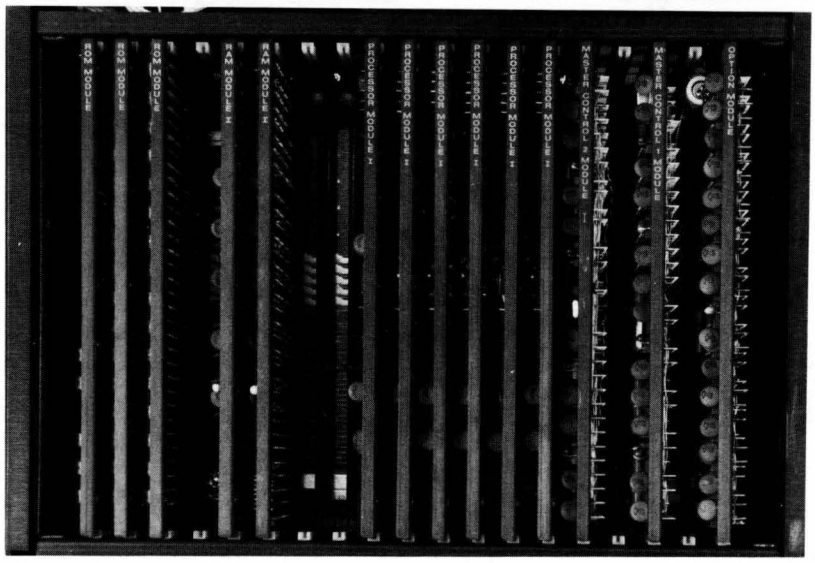


Figure 3-2. Mainframe Card Location

in slot 02/03, with other pairs of NPs, if any, in sequence. Terminal port cards follow in any type or order. If there is a time of day module (TODM) for a report logging CTP, it occupies slot 1E/1F.

3.5.1 CABLING

Figures 3-3 and 3-4 show the cables and connections used in installation of the various models of 6030 and 6040 INP's.

Figure 3-3 shows a 6030 (tabletop) or 6031 (rack-mounted) with one power supply. When a second port nest is added (Figure 3-4A), it is preferable to attach both port nests to the second power supply to equalize the loads on the power supplies. No more than two port nests should be attached to a 200W rack mounted power supply. With a 400W rack mounted supply, 2 units will supply up to 8 pin nests. (See Figure 3-4B.)

The equipment and cabling required for each model is indicated by the levels of the dashed lines at the left of the diagrams. For example, a 6030 or a 6040 consists of all equipment above the level of the dashed line: one operator's console, one

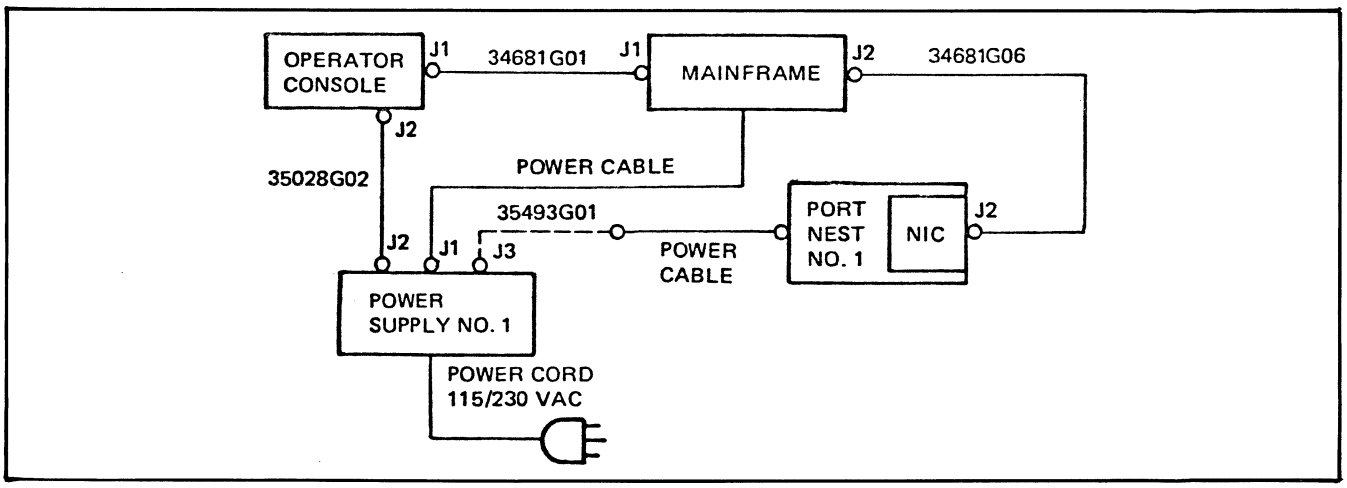


Figure 3-3. Cabling for 6030, 6031, 6040, and 6041 INP's

mainframe, and one port nest, with connecting cables. A 6032 or 6042 has a second port nest connected to the first port nest and driven by a second power supply, and so on.

The Codex part numbers given in Table 3-1 consist of two parts. The first five digits indicate the general application: e.g., crossover cable 35861, while the letter G and the last two digits indicate the specific applications: G01, G02, etc.

Customers should order parts by product code number.

In Figures 3-3 and 3-4, cable 35493G01, product 66938 (port nest to power supply) is shown as a dotted line. This cable is an extension to the port nest power cable, and is installed only if the added length is needed.

Use of the cable for the current loop terminal port (part number 37214G01) is described in Section

Figure 3-5 shows the cabling used on a port nest of a 6030 INP - it has only one network port. The product number of the cable from NP1 J2 to the high-speed modem depends on the length required (see Table 3-1).

Figure 3-6 shows the applications of INP to DTE direct cables, and INP to DCE crossover cables.

3.5.2 STRAPPING

When the mechanical installation and cabling connections have been completed, check the positions of the straps and switches on the printed circuit boards before applying power to the system.

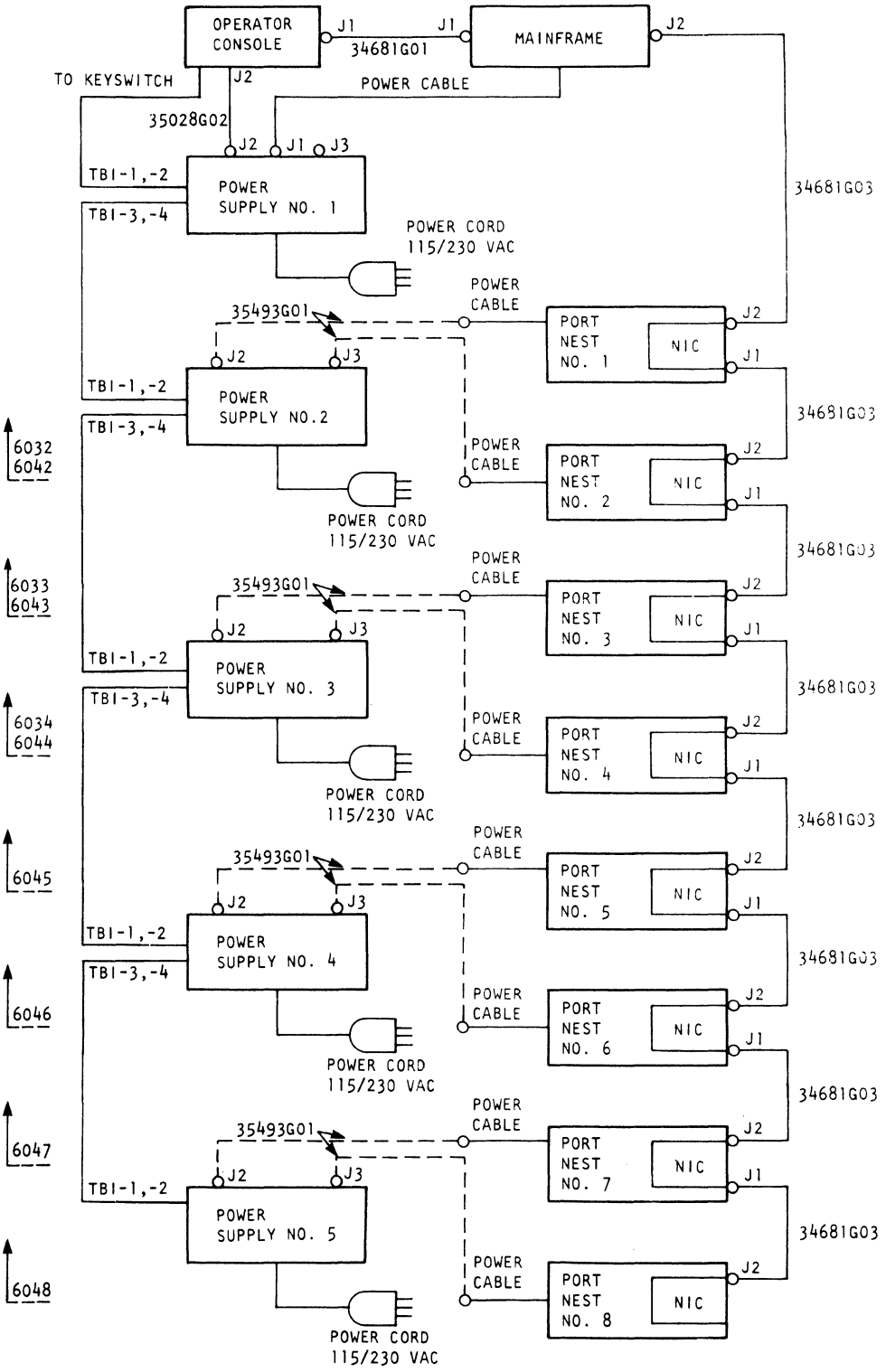


Figure 3-4A. Cabling and Connections for 6030/6040 Series INP's with 200 Watt Power Supplies

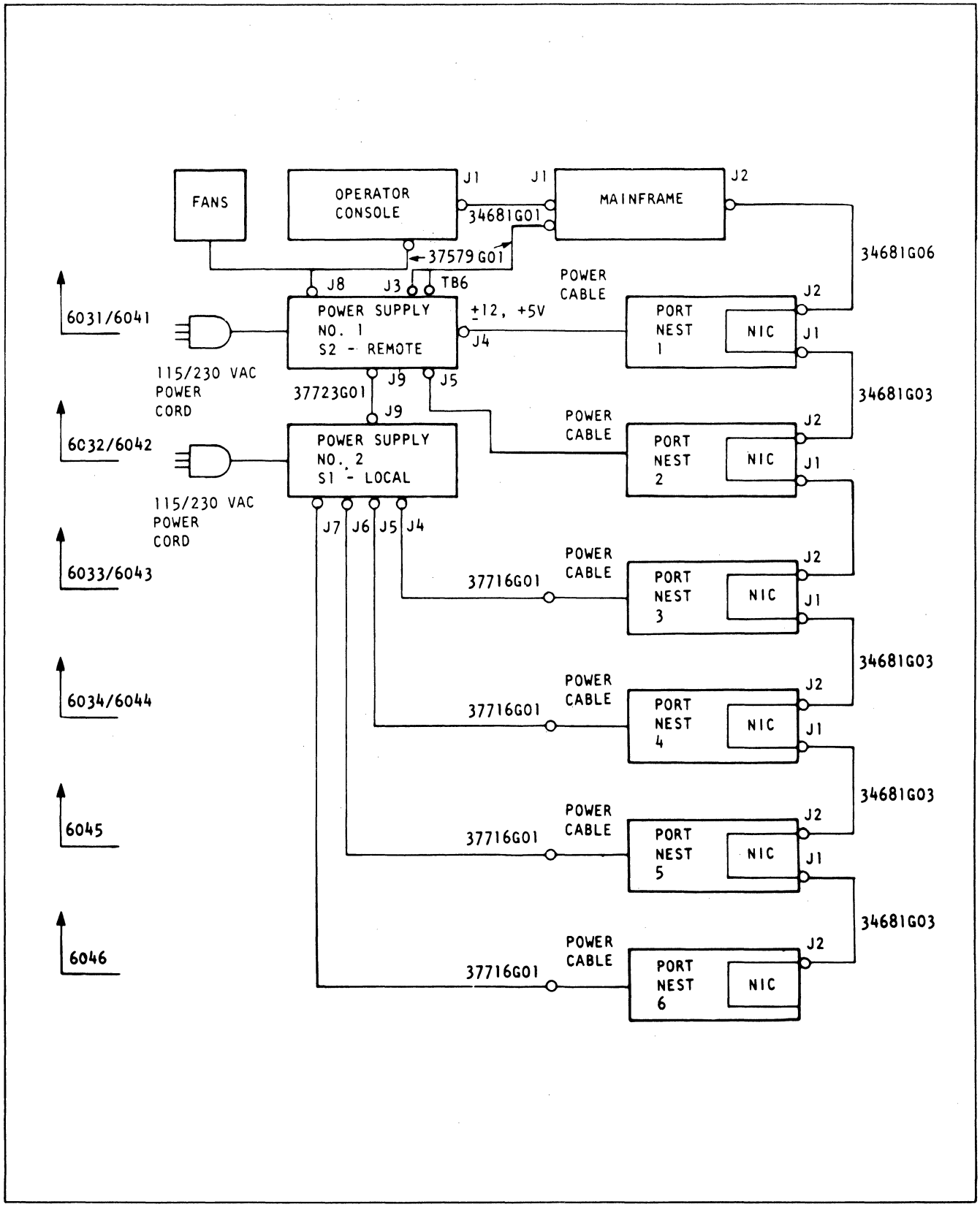


Figure 3-4B. Cabling and Connections for 6030/6040 Series INP's with 400 Watt Power Supplies

TABLE 3-1. CABLES FOR 6030/6040 SERIES INP's

Product Code	Part Number	Part Name	Part Description
66180	36795G01	15-ft EIA modem crossover cable	Male-male cable for connecting a terminal port to its modem (DCE).
66181	35795G02	30-ft EIA modem crossover cable	
66182	35795G03	50-ft EIA modem crossover cable	
66183	35861G01	15-ft EIA terminal cable	Male-female cable for connecting a terminal port to its terminal or CPU (DTE).
66184	35861G02	30-ft EIA terminal cable	
66185	35861G03	50-ft EIA terminal cable	
66186	34196G01	15-ft EIA network port cable	Male-male cable for connecting a 6000 network port (NP1 J2) to the high speed trunk modem.
66187	34196G02	30-ft EIA network port cable	
66188	34196G03	50-ft EIA network port cable	
66935	34681G06	180-in. interface cable	Connects mainframe to NIC between racks.
66937	34681G02	25-in. interface cable	Connects mainframe to port nest (desk model).
66938	35493G01	36-in. power cable	Connects port nest power cable to 200W power supply.
66939	34681G03	15-in. interface cable	Connects port nest to port nest.
66944	34681G01	5-in. interface cable	Connects console to mainframe.
66945	35028G02	25-in. power cable	Connects console J2 to 200W power supply J2.
66953	35028G01	28.5-in. power cable	Connects port nest J3 to 200W power supply, +5V, +12V ground.
66954	34681G04	58-in. interface cable	Connects mainframe to port (rack-mounted).
66955	34681G05	48-in. interface cable	Connects NIC to NIC between racks.

TABLE 3-1. CABLES FOR 6030/6040 SERIES INP's (Cont)

Product Code	Part Number	Part Name	Part Description
Part of Option 6150	37214G01	40-in. current loop cable	Current loop terminal port to connector panel.
-	37579G01	59-in. power cable	400W power supply to operators console, mainframe, and fans.
-	37723G01	24-in. power cable	400W power supply J9 to 400W power supply J9.
-	37716G01	72-in. power cable extension	400W power supply J1, J3, J4, J5, J6, J7 to port nest power.

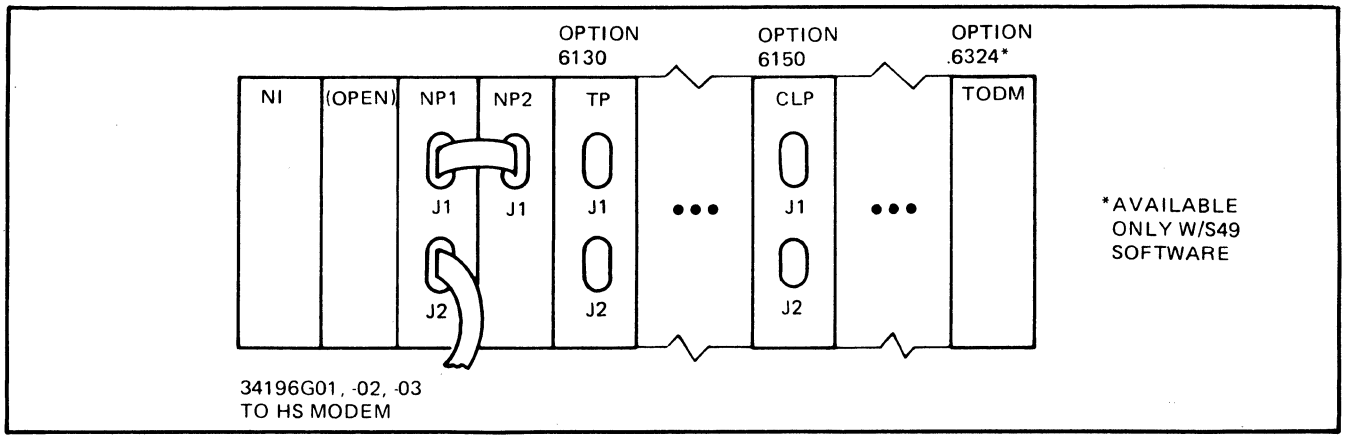


Figure 3-5. Port Nest Cabling

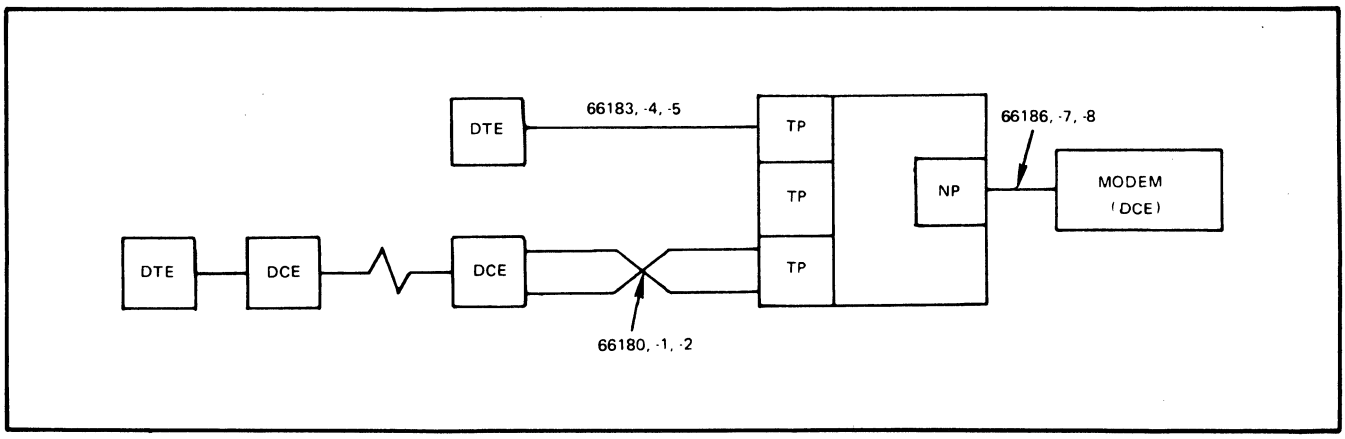


Figure 3-6. Cables from INP to DTE's and DCE's

Certain modules have strapping to be verified. In the mainframe: processors, MC2 card, and ROM's. In the port nests: network ports, terminal ports or activity indicator terminal ports, and current loop terminal ports (if any). In the power supply: the terminal board, all connectors, and possibly the switch and relay.

3.5.2.1 MASTER CONTROLLER 2 (MC2). The MC2 has straps for controlling the size of the lock byte area and for the rate of the system clock.

Soldered straps on the U40 platform control the size of the lock byte area (256 bytes to 2048 bytes). If an MC2 has insufficient lock byte area for the model of the INP, the error message IL (insufficient lock byte area) is displayed at BOOT time. Figure 3-7 shows the strapping for each model of the INP, and should be referred to if the cards are swapped.

System clock, either 5 MHz or 4 MHz, is solder-strapped at location DV or SW near the center of the board, just above U40.DV is 5 MHz, SW is 4 MHz.

NOTE

This speed must be the same as the speed of the processor module.

There are two versions of this board: one with a 40 MHz crystal, and one with a 32 MHz crystal.

3.5.2.2 PROCESSOR. There may be up to three processors in a 6030 series mainframe or up to six in a 6040. All processors in the same mainframe must be strapped for the same speed: 5 MHz or 4 MHz. The new boards operate at 5 MHz (strapped U34-1 to -8 and -3 to -6), but there are some 4 MHz processors in the field strapped U34-2 to -7, and -4 to -5 (see Figure 3-8).

S49 software takes advantage of an extended memory address technique. This technique requires that the strap in the upper right corner of the processor card, just below U11, be placed in the 128K position instead of the 64K position required by S46 and S47 (Figure 3-9). S49 also requires firmware changes on the Master Control cards. The compatible MC's are marked "S49" on the card rail.

3.5.2.3 16K PROM (ROM). ROM's for S47 software are treated as a set of two of the same release and revision number, so that if one fails, both are replaced. They are interchangeable in the two ROM slots in the mainframe because the addresses are

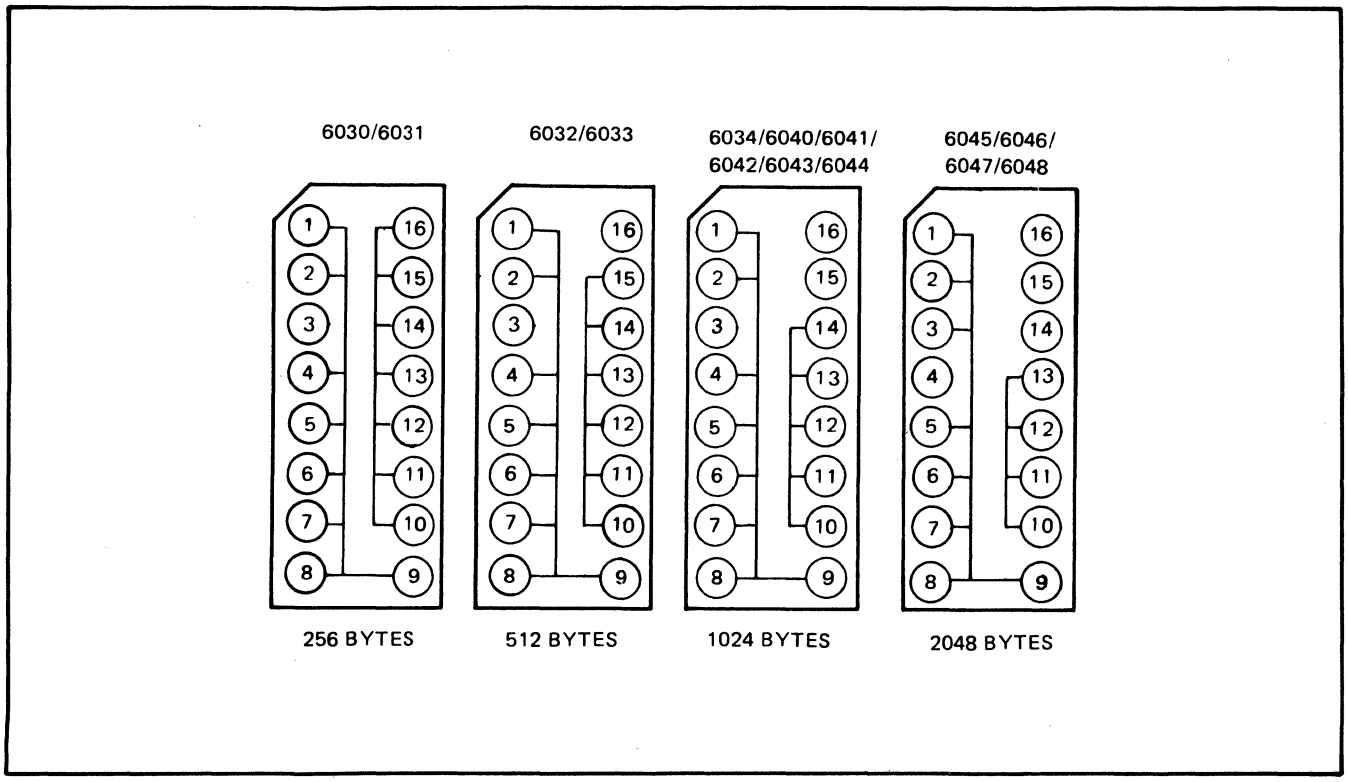


Figure 3-7. MC2 Lock Byte Platform U40

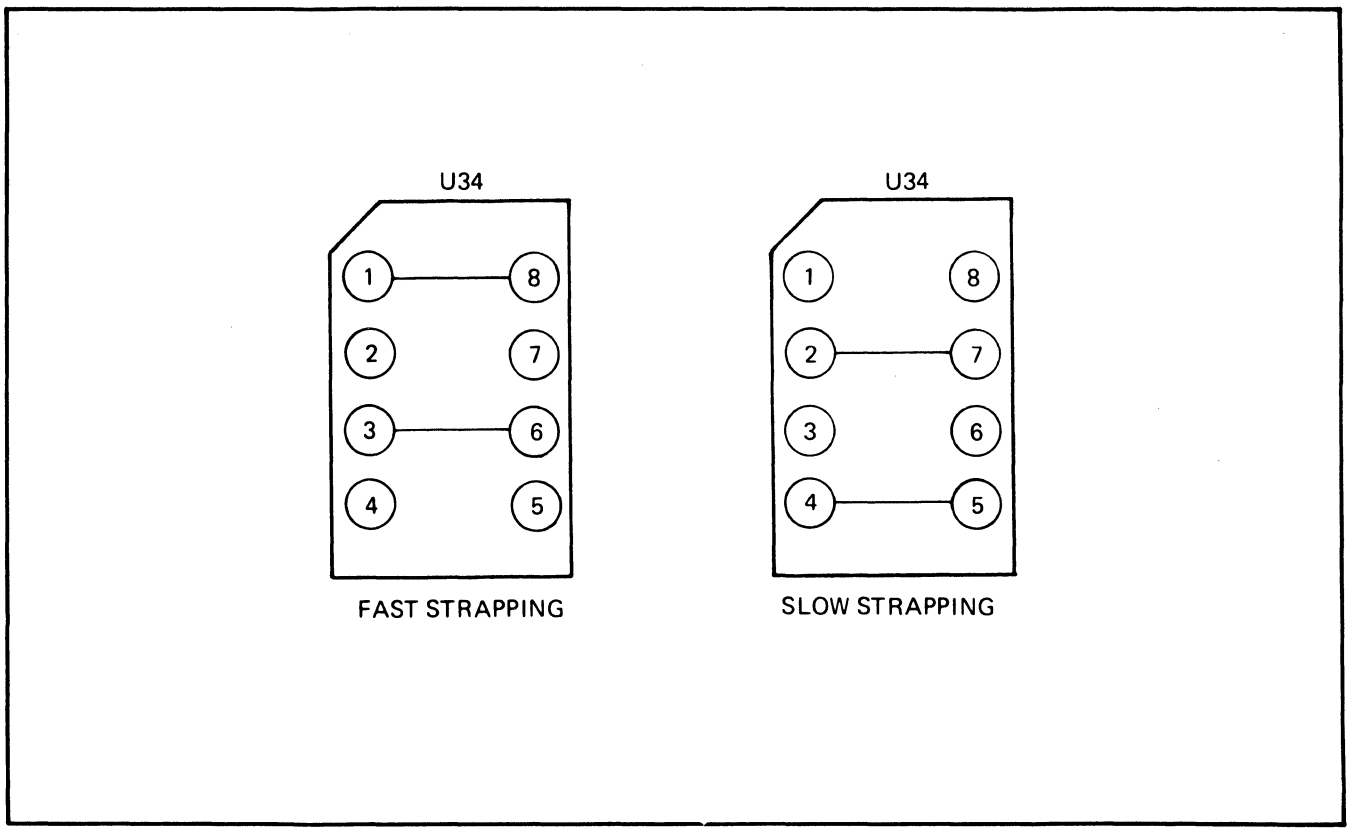


Figure 3-8. Processor Cycle Speed Strapping, Platform U34

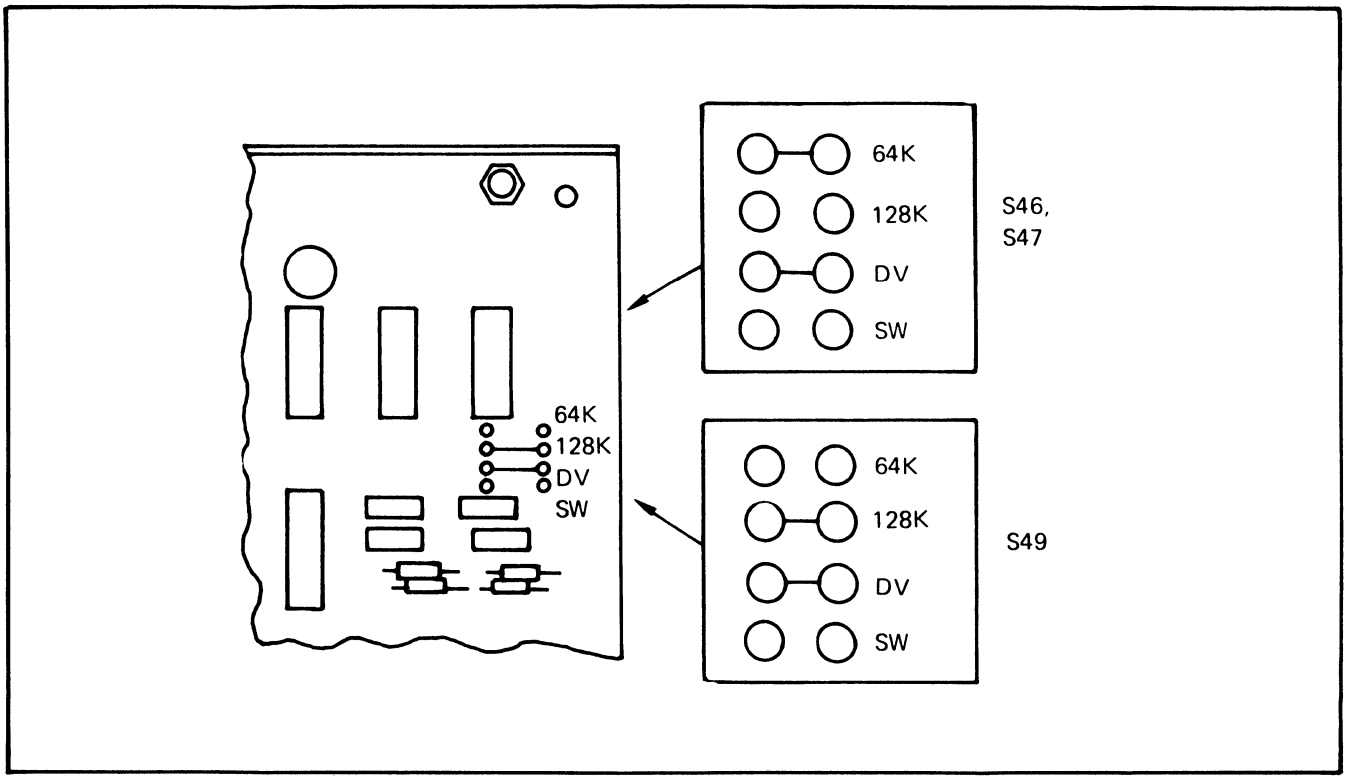


Figure 3-9. Processor Card Strapping, S46, S47 and S49

strapped on platform U52 as shown in Figure 3-10. If three ROMs are required for S49, they are strapped as shown in Figure 3-11. S49 ROMs are identified by "S49" printed on the rail.

3.5.2.4 NETWORK PORT 1 (NP1). NP1 is normably strapped for internal clock at 1800 bps on platform U20, from U20-1 to -20 (Figure 3-12). However, an option on the MC1 card provides a loopback clock at 7200 bps. Then, NP1 is strapped U20-2 to -19, or the modem clock can be looped back via NP1 U20-3 to -18 (Figure 3-13).

3.5.2.5 STANDARD (DUAL UNIVERSAL) TERMINAL PORT - Option 6130. The dual universal terminal port (Option 6130) has two channels, each of which can be configured independently to operate in either BSC or asynchronous mode. The mode is selected when the node is configured.

A number of signals must be strapped on the TP module: EIA control signals, clock rates, clock sources, and signal delays.

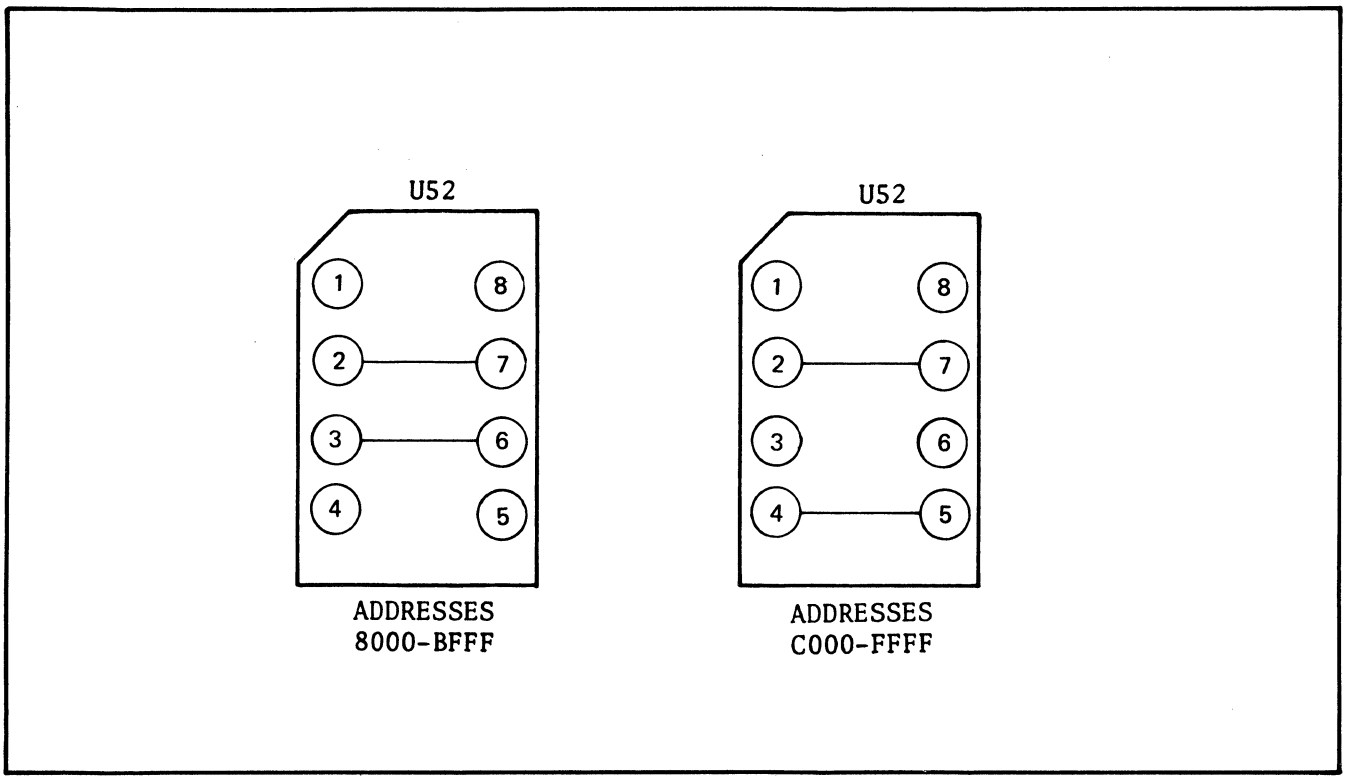


Figure 3-10. ROM Card S46 & S47 Address Strapping, Platform U52

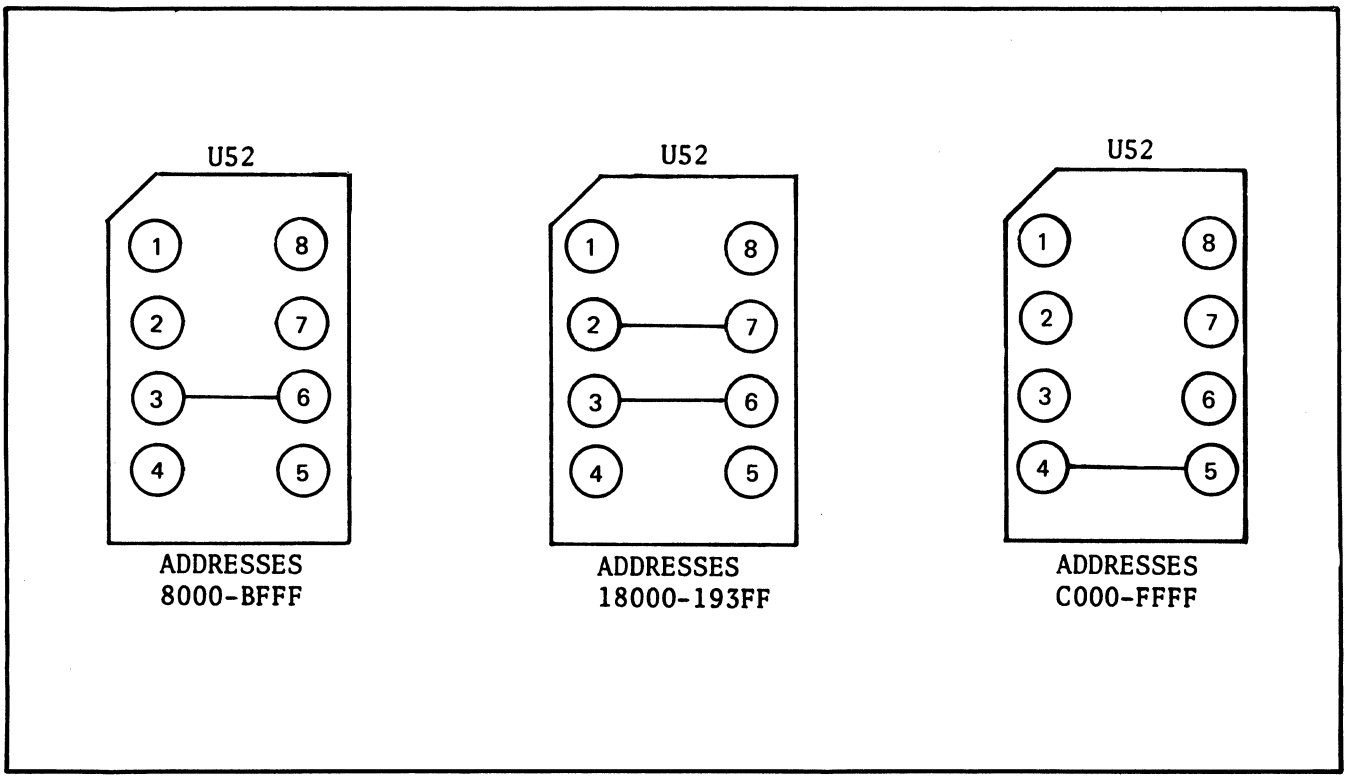


Figure 3-11. ROM Card S49 Address Strapping, Platform U52

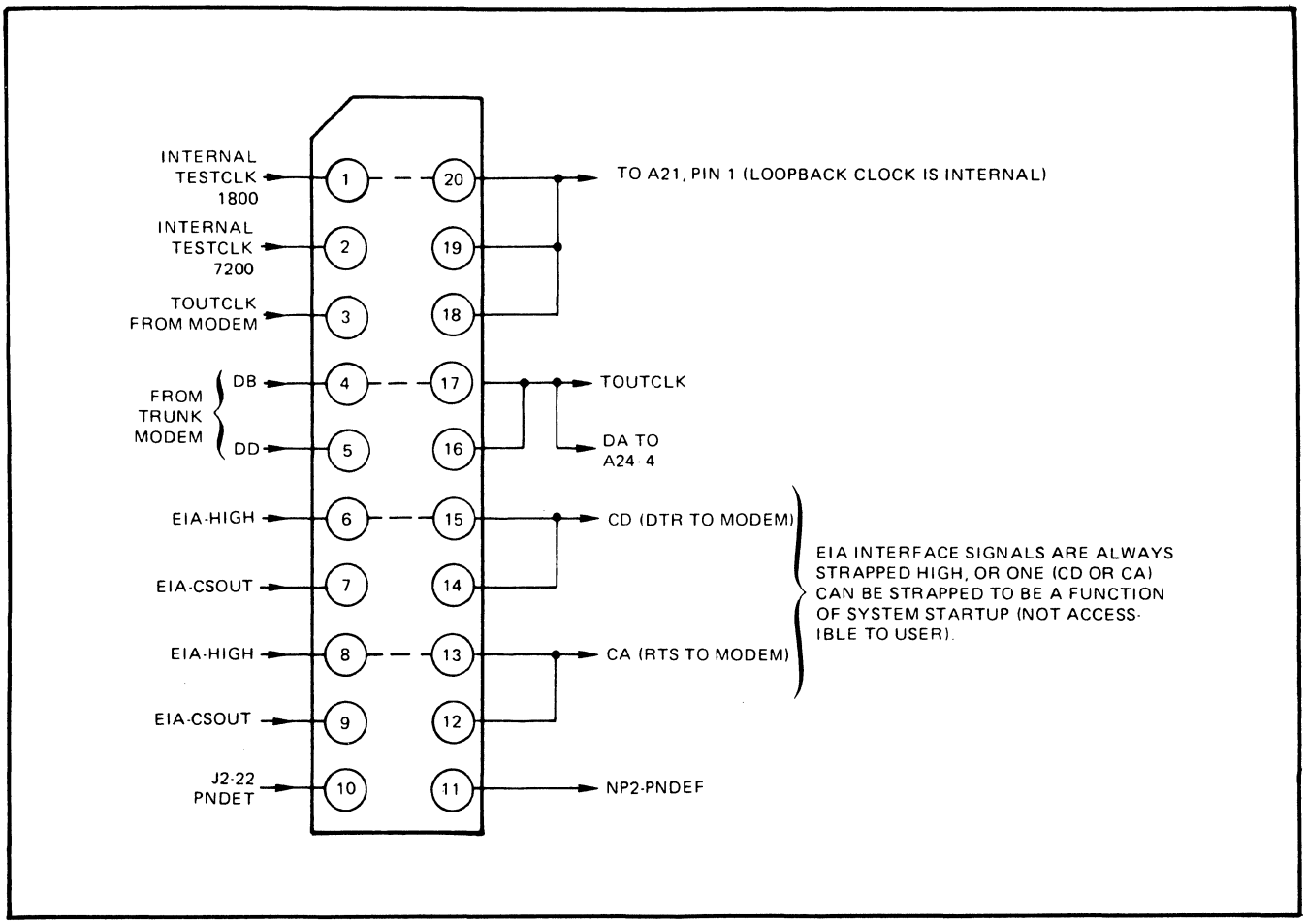


Figure 3-12. NP1 Platform U20, Normal Strapping

Figure 3-14 shows the strapping locations on the TP card. In the figure, a dashed dividing line, approximately across the middle of the board, separates components for the even channel (EIA connector J1) and odd channel (J2). Both J1 and J2 are wired as DCE interfaces. Platform U5, in the upper right corner of the board, is common to both channels. It is used to select internal and external clock sources as well as CTS delay. On U5, pins 1 to 4 and 13 to 16 serve the even channel, and 5 to 12 serve the odd channel.

Figure 3-15 is a schematic of the even (J1) channel on a TP. The schematic for the odd channel is identical except for the strapping points on U5 and the numbers of the ASTRO and clock speed select platform. These appear in Figure 3-14.

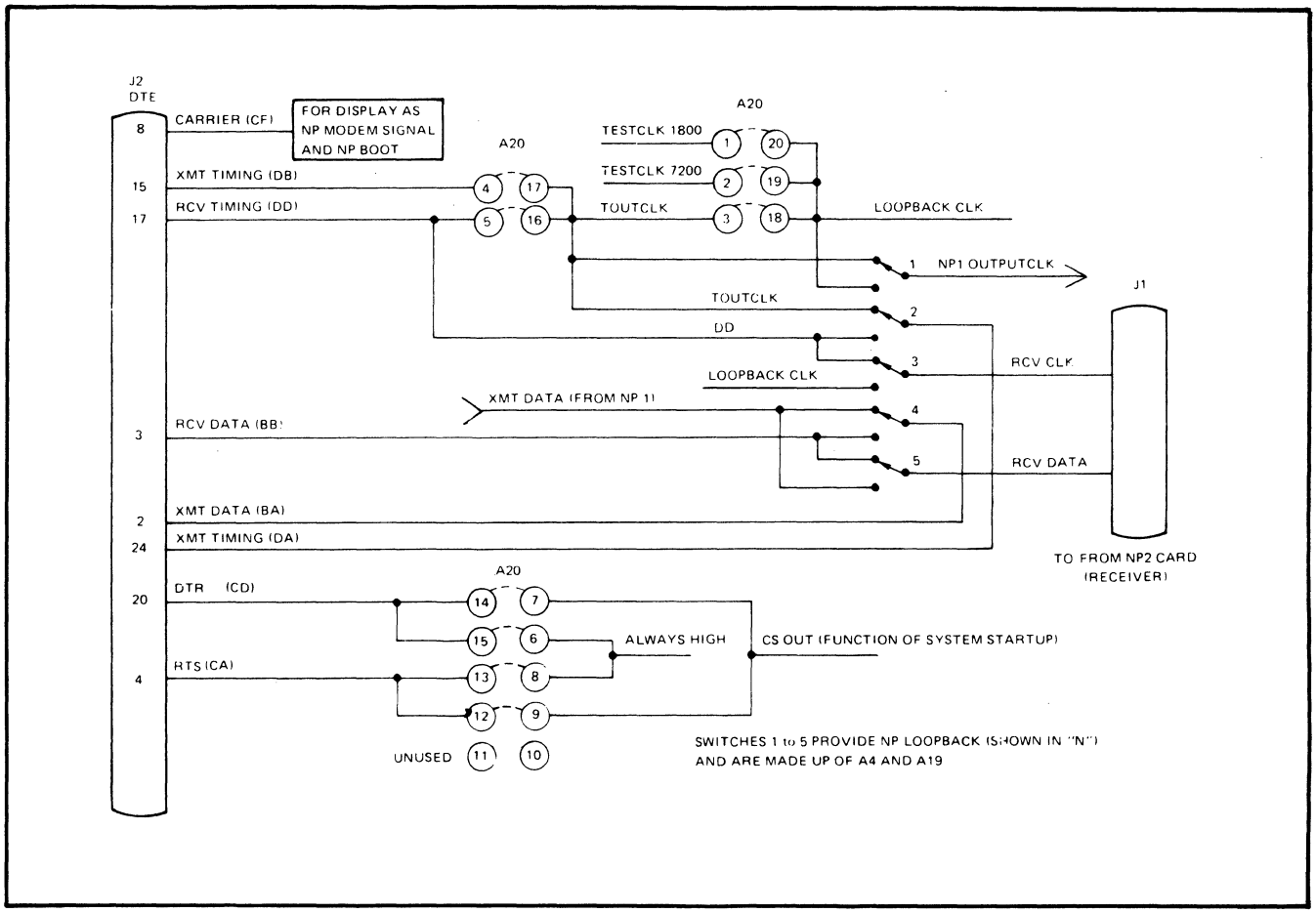


Figure 3-13. NP1 I/O Signals and Loopback Strapping

3.5.2.5.1 Clock Rates.

Platform U-10 and U-17 Straps (See Figure 3-16)

Strap 1-16 selects externally supplied clock from EIA pin 24 (connected to DCE).
2-15 selects externally supplied clock from EIA pin 18 (connected to DTE).
3-14 selects 9600 bps external receive clock.
4-13 selects 7200 bps external receive clock.
5-12 selects 4800 bps external receive clock.
6-11 selects 3600 bps external receive clock.
7-10 selects 2400 bps external receive clock.
8-9 selects 1200 bps external receive clock.

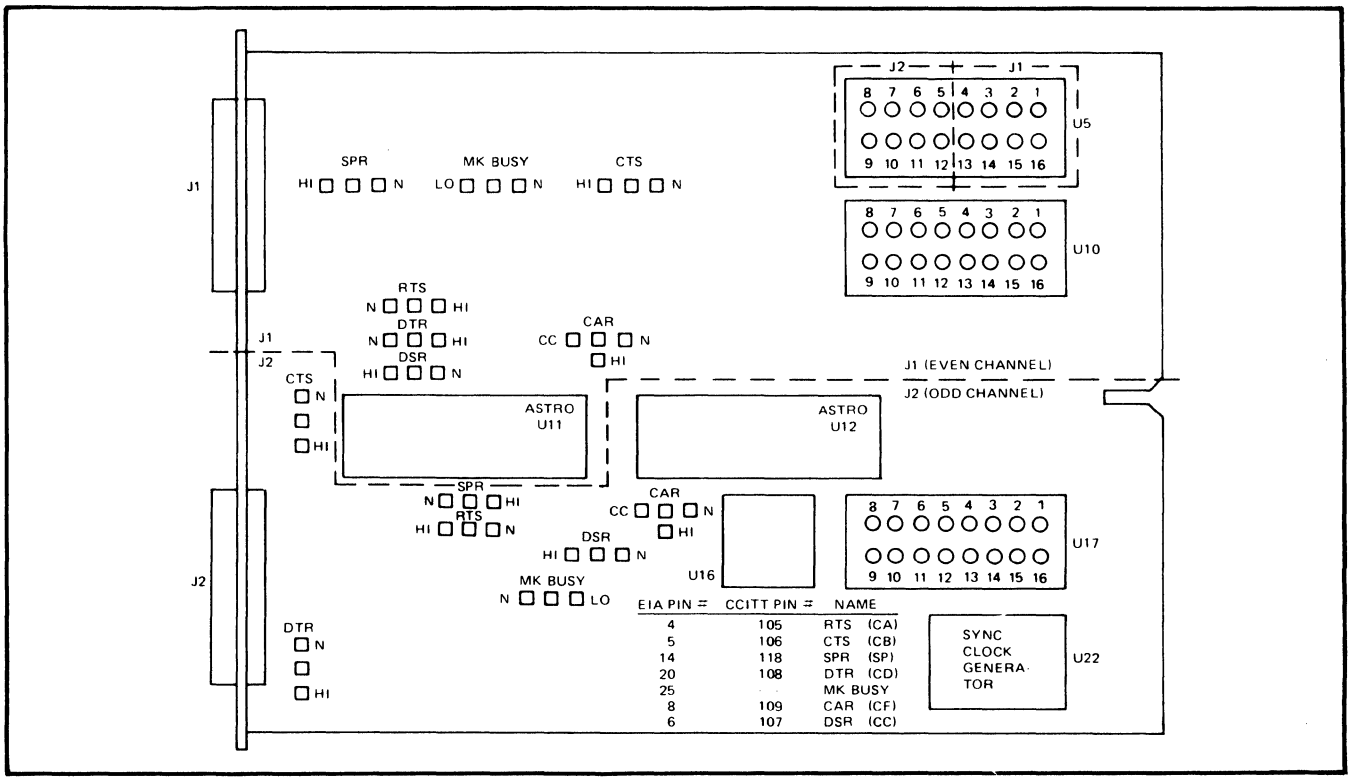


Figure 3-14. Standard TP Card Strap Locations

Platform U-5 Straps (See Figure 3-17)

Strap 1-16 Selects J1 port RTS (CA)/CTS(CB)
or 2-15 delay.

1-16 = no delay.
2-15 = delay, (approximately 22 ms).

3-14 Selects J1 port interface transmit clock
or 4-13 (only if External clocking is configured).

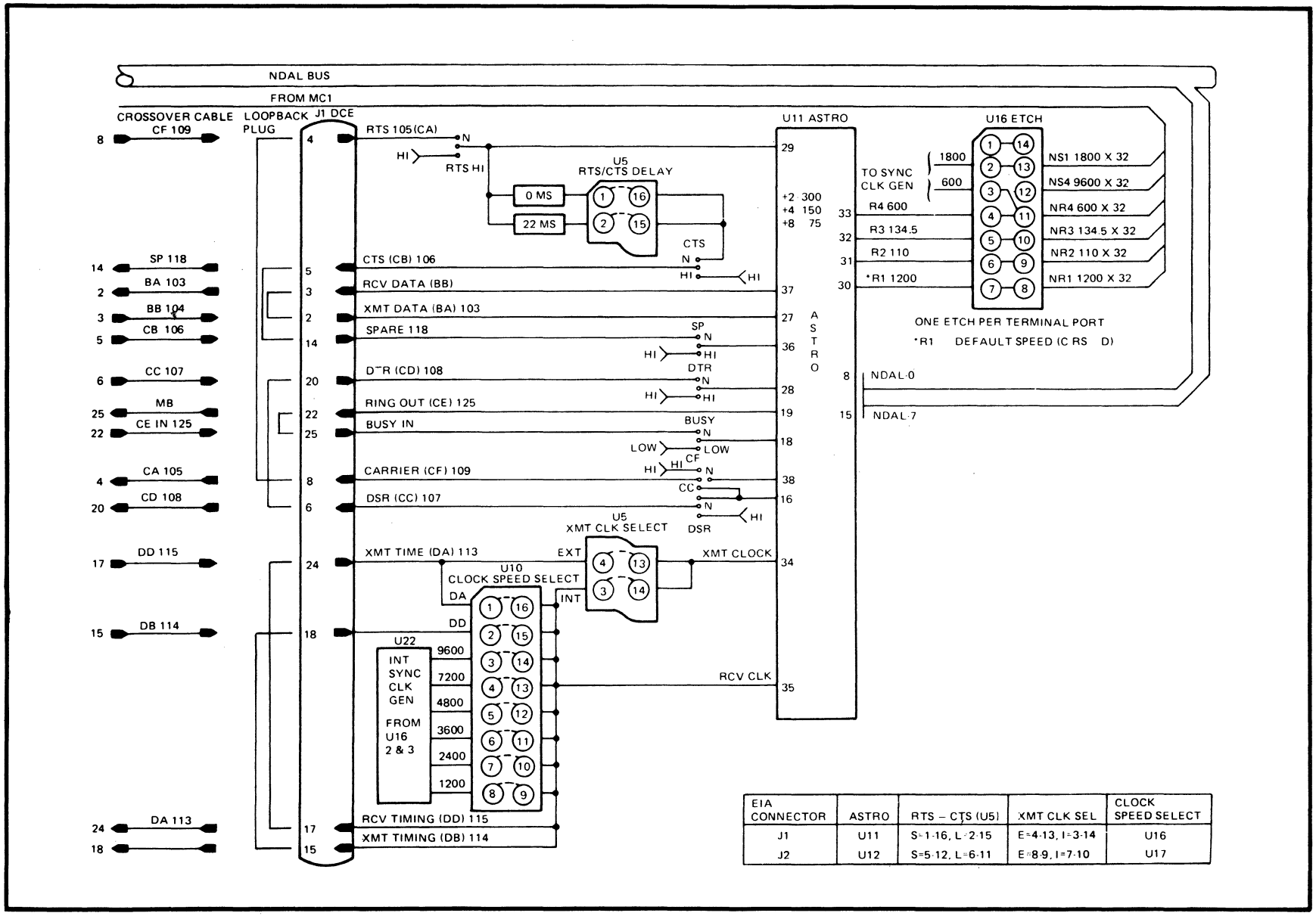
3-14 = same as receive clock.
4-13 = DA via EIA pin 24. DA = External transmit clock.

5-12 Selects J2 port RTS(CA)/CTS(CB)
or 6-11 delay.

5-12 = no delay.
6-11 = delay, (approximately 22 ms).

7-10 Selects J2 port interface
or 8-9 transmit clock.

7-10 = same as receive clock.
8-9 = DA via EIA pin 24. DA = External transmit clock.



EIA CONNECTOR	ASTRO	RTS – CTS (U5)	XMT CLK SEL	CLOCK SPEED SELECT
J1	U11	S-1-16, L-2-15	E-4-13, I-3-14	U16
J2	U12	S-5-12, L-6-11	E-8-9, I-7-10	U17

Figure 3-15. Terminal Port Even Channel (J1) Signals

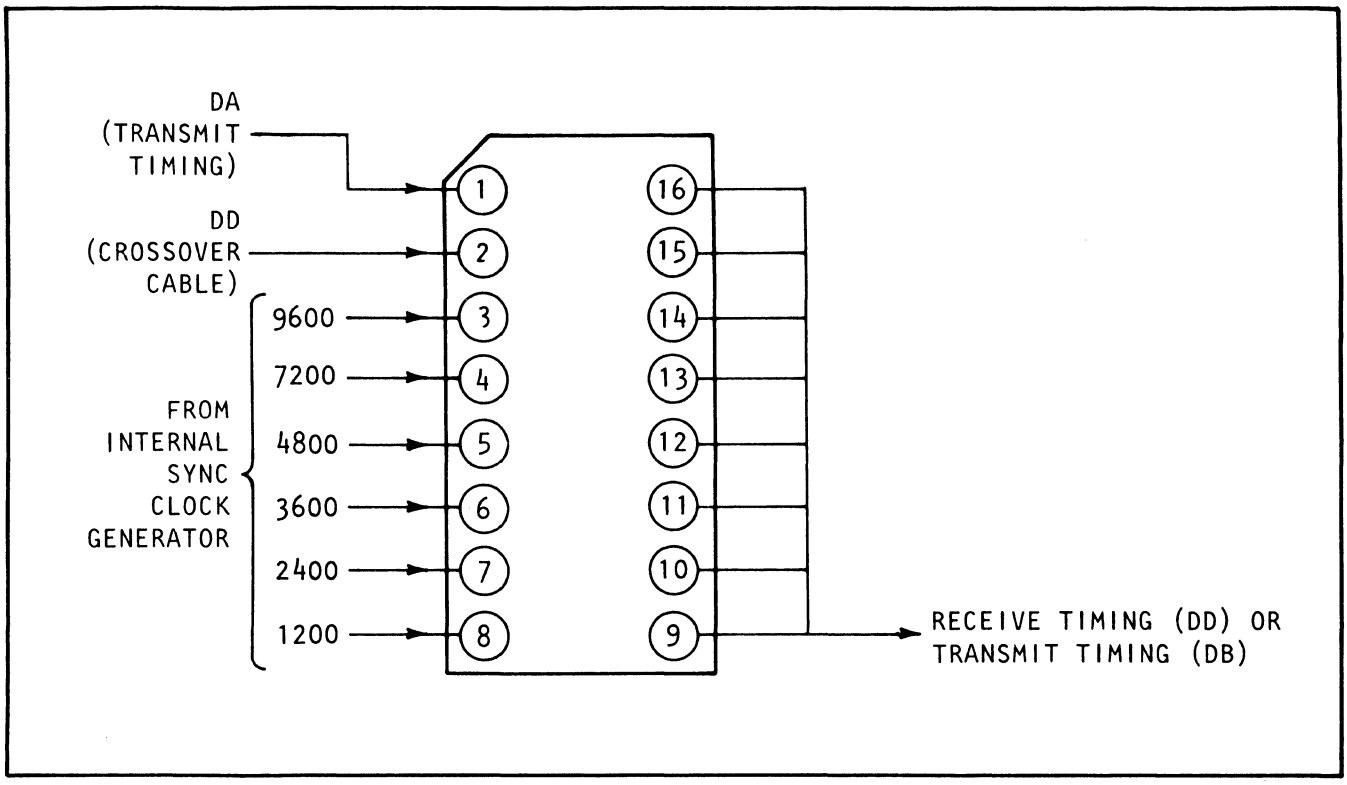


Figure 3-16. Platform U10 and U17 Straps

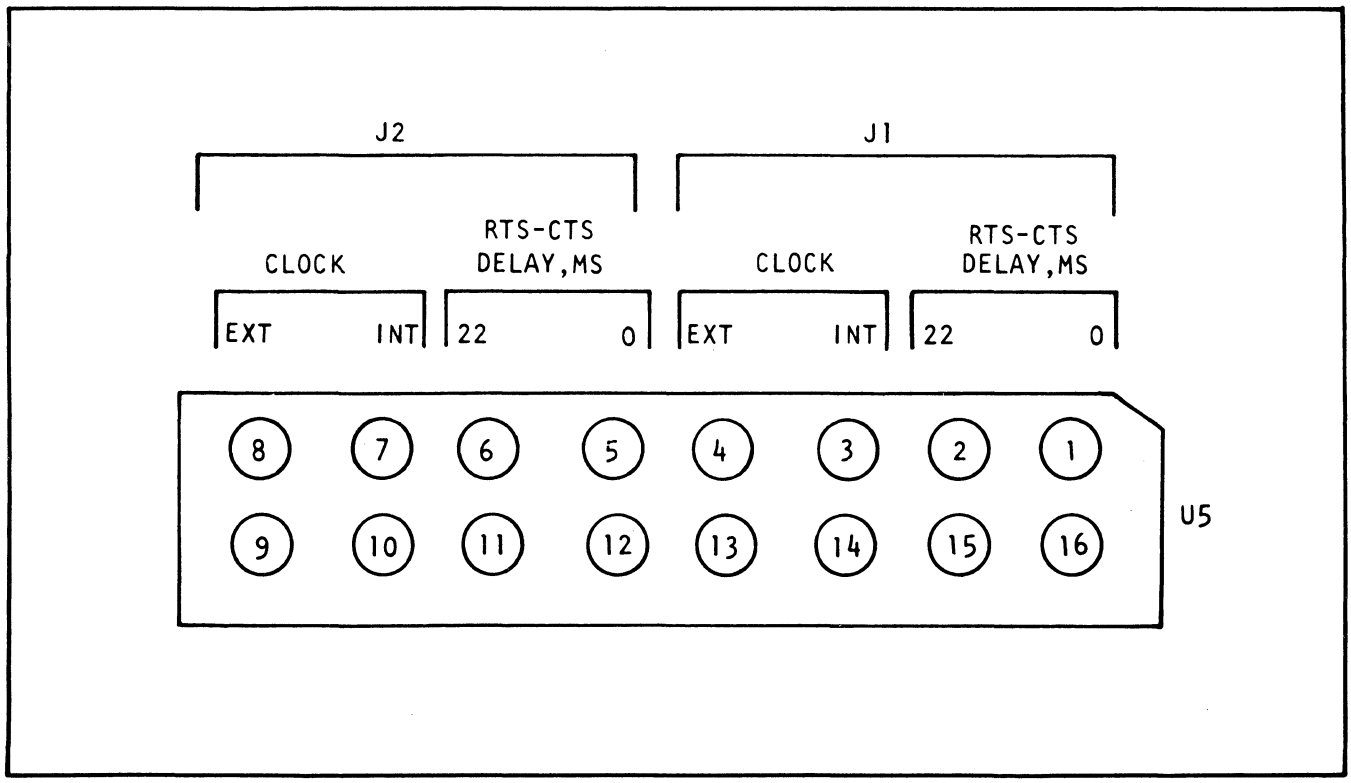


Figure 3-17. TP U5 Platform

Additional patches may be made to the TP card. This allows CB(CTS), CC(DSR), and CF(CAR) signals to be permanently in the ON or HI state. A strap combination also allows the bussing of CF to follow CC.

3.5.2.6 ACTIVITY INDICATOR TERMINAL PORT - Option 6131. Option 6131 performs the same functions as the standard (dual universal) terminal port module. Like the standard terminal port, it is strappable to select clock sources and rates and to activate control signals and associated delays.

3.5.2.6.1 Module Layout. When the module is plugged into the port nest, the J1 connector is on top, J2 is below. All circuitry and strapping platforms for each channel are located on the associated (upper or lower) half of the board. Figure 3-18 identifies the strapping locations.

3.5.2.6.2 Control Signal Strapping. Two strapping positions are provided for all control signals except Carrier (CF), which has three positions.

Input Control Signals.

a) SPR (spare) may be strapped either Normal or ON. In the N position SPR is driven from pin 14 of the EIA interface; in the ON position SPR is held active.

b) MK BSY (busy in) may be strapped either Normal or OFF. In the N position MK BSY is driven from pin 25 of the EIA interface; in the OFF position it is inactive.

c) RTS (ready to send) may be strapped Normal or ON. In the N position it is driven from pin 4 of the EIA interface; in the ON position it is held active.

d) DTR (data terminal ready) may be strapped either Normal or ON. In the N position it is driven from pin 20 of the EIA interface; in the ON position it is held active.

Output Control Signals.

a) DSR (data set ready) may be strapped either Normal or ON. In the N position, pin 16 of the ASTRO drives pin 6 of the EIA interface. If DSR is in the ON position, pin 6 of the EIA interface is held active.

b) CAR (carrier detect) may be strapped in one of three positions: N, CC, or ON. If it is strapped N, pin 38 of the ASTRO drives pin 8 of the EIA interface; if it is strapped CC, pin 16 of the ASTRO drives pin 8 of the EIA interface. If it is strapped ON, pin 8 of the EIA interface is held active.

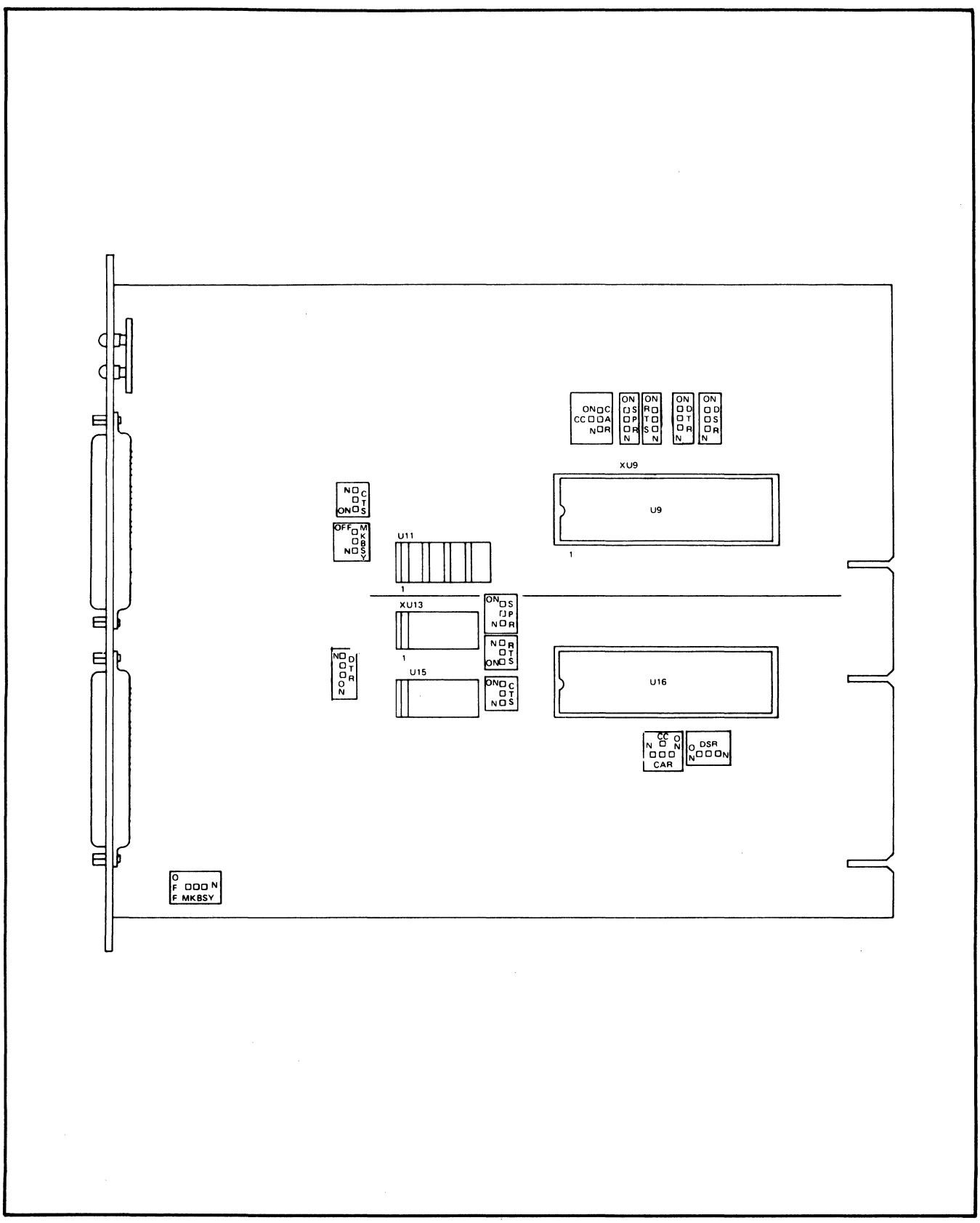


Figure 3-18. Activity Indicator Terminal Port Strap Locations

c) CTS (clear to send) may be strapped either Normal or ON. In the N position, pin 5 of the EIA interface is driven by pin 4 of the EIA interface, and CTS may be delayed. (The delay is described below.) In the ON position, pin 5 of the EIA interface is held active.

RTS/CTS Delay.

a) A 22-ms delay is introduced in the RTS/CTS turnaround if CTS is strapped N and U11 is strapped U11- 12 to -5 (for the J1 channel) of U11-1 to -16 (for the J2 channel).

b) No delay is introduced in the RTS/CTS turnaround if CTS is strapped N and U11 is strapped U11-6 to -11 (for the J1 channel) or U11-2 to -15 (for the J2 channel).

3.5.2.6.3 Clock Speed Strapping. System clock is supplied by the modem or by the sync clock generator. Figure 3-18 shows the strapping positions used to select the appropriate speeds.

External Transmit Clock.

a) Synchronous transmit clock speeds are supplied internally by the synchronous clock generator U22 on the port card. Figure 3-19 shows the strap positions to select the appropriate speeds.

b) The J1 channel is strapped on platform U13, J2 on U15. The two channels are identical so the figure serves to illustrate both. The signal at ASTRO pin 35 also drives pins 15 and 17 of the EIA interface.

External Receive Clock.

a) Receive clock (DB) generated externally (usually by the modem) is provided to ASTRO pin 34 by strapping the J1 channel U11-8 to -9, and the J2 channel U11-4 to -1.

b) The signal at EIA pin 24 provides external transmit clock for the J1 channel by strapping U11-7 to -10, for the J2 channel by strapping U11-3 to -14.

External Receive and Transmit Clock from EIA Pin 24.

a) Both receive and transmit clock are provided by 1 channel EIA pin 24 by removing the U13 strap and strapping U11-7 to -10 and U11-8 to -9.

b) Both receive and transmit clock are provided by J2 channel EIA pin 24 by removing the U13 strap and strapping U11-3 to -14 and U11-4 to -13.

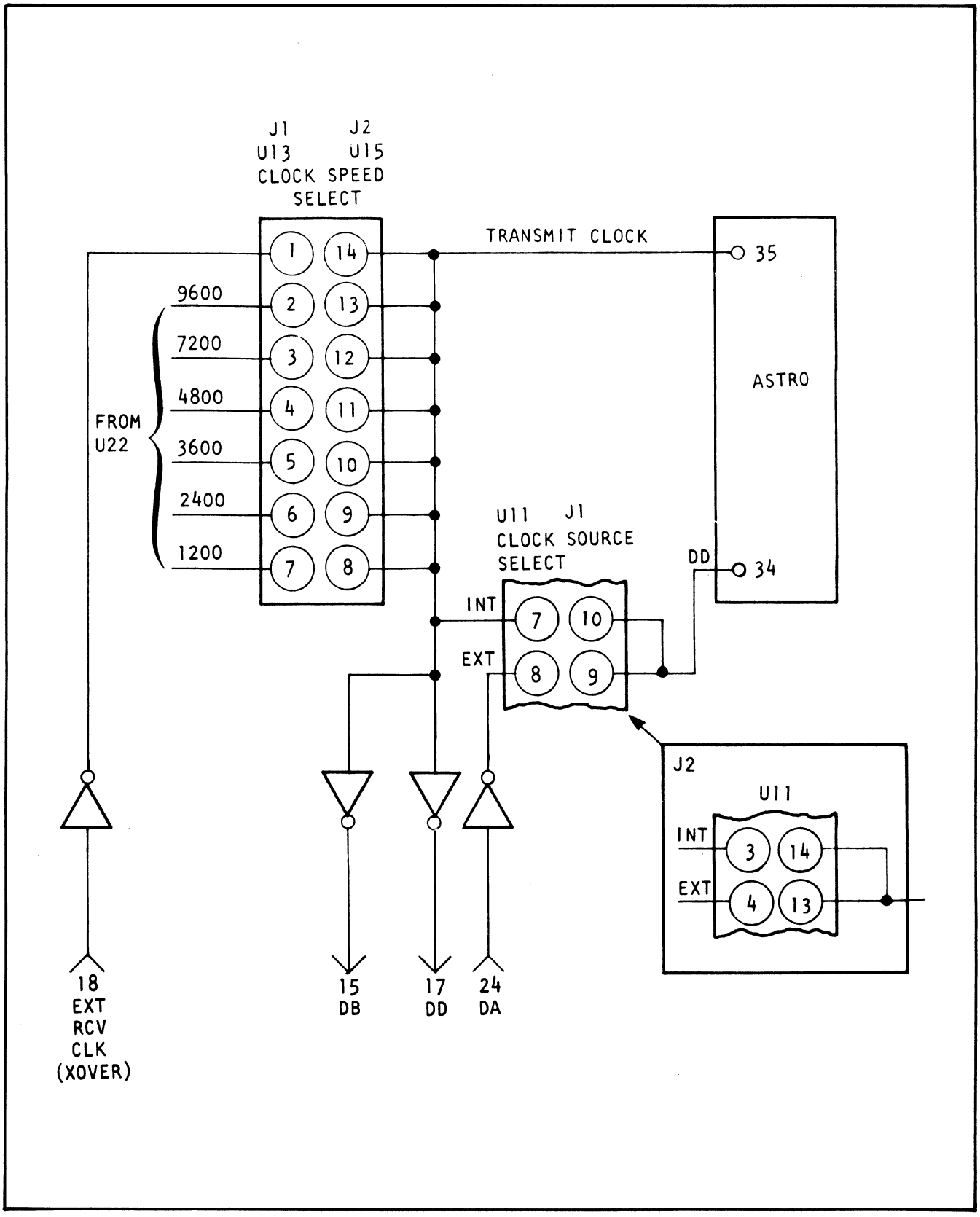


Figure 3-19. Clock Speed and Source Strap Locations

3.5.2.7 CURRENT LOOP TERMINAL PORT - Option 6150

WARNING

Dangerous high voltage may be present at all 6000 INP current loop port interfaces. INJURY TO SERVICE PERSONNEL AND DAMAGE TO EQUIPMENT may result unless the following precautionary procedures are followed during installation of any current loop port module.

3.5.2.7.1 Cabling Accessories. To prevent the mistake of connecting an EIA connector to a current loop port, the male and female connectors have been exchanged. The female is on the current loop cable, not on the card. The card connectors are male.

The 40-inch cable, with a standard 25-pin EIA female connector at one end and a terminal block at the other end, is shown in Figure 3-20. The EIA connector (of which only five pins are active) plugs into the current loop port. The terminal block at the other end of the cable mounts into a specially designed connector panel which is available as an accessory. The terminal block provides a means of user connection to the 6150.

The panel is designed to mount into vertical mounting rails at the rear of a rack cabinet. It contains 16 slots into which current loop terminal blocks may be mounted, allowing up to 16 current loop ports to be supported by one panel. Cabling of current loop DTE's to the current loop panel, rather than the port, will eliminate accidental connection of high current loop voltage to an EIA port.

3.5.2.7.2 Terminal Block Panel Covers.

WARNING

Install the protective cover over the terminal block panel upon completion of any current loop port installation. The cover protects operators and service personnel from the high voltage present at the terminals.

The cover is held in place by several plastic spacers. Avoid contact with terminals while installing the covers.

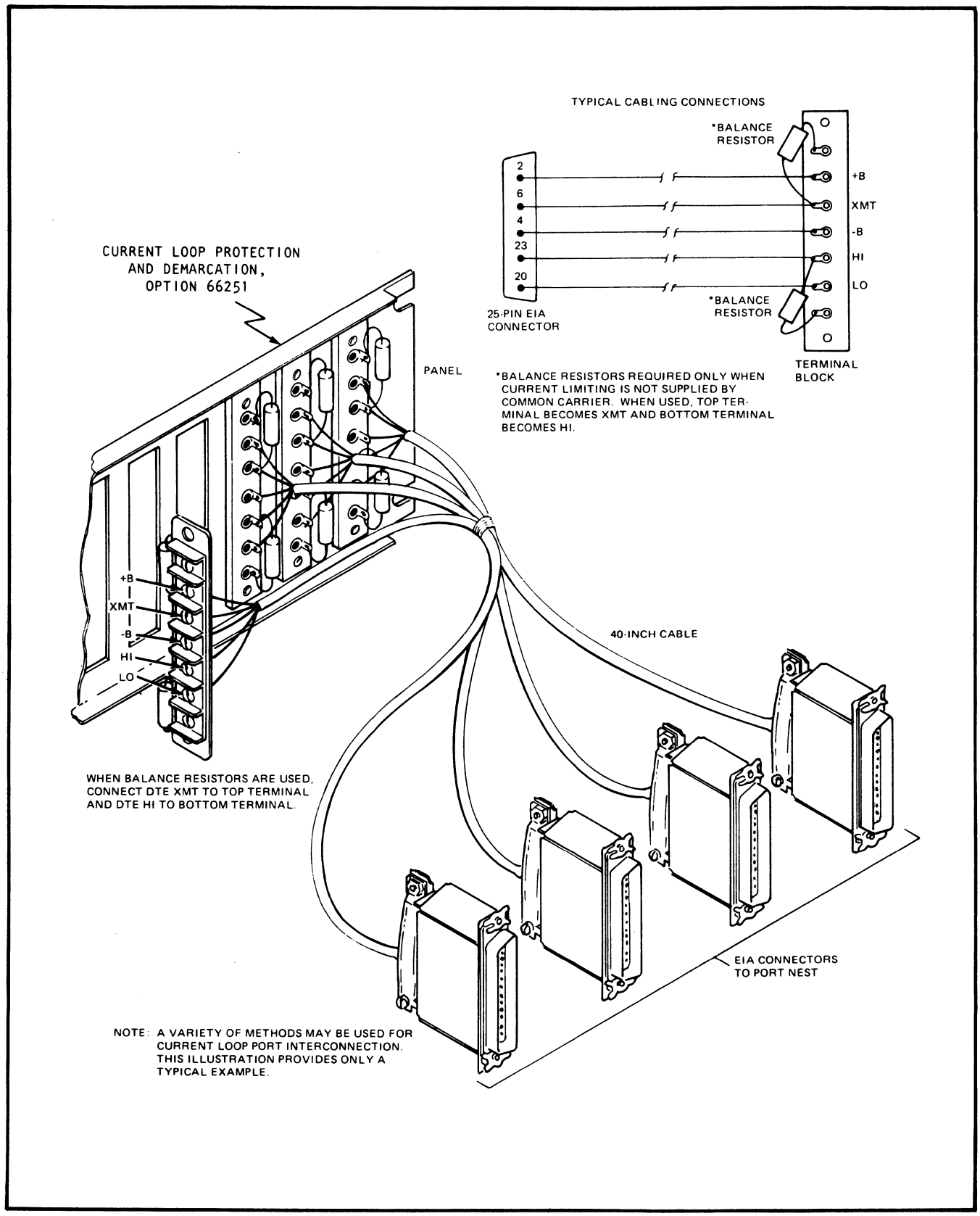


Figure 3-20. Current Loop Cabling Accessories

3.5.2.7.3 Strapping. Three jumpers per channel (see Figure 3-21) are located on the current loop port module to allow selection of various operational modes for the current loop channel. Each is described as follows:

One jumper is used to adapt the current loop module to the current that is being supplied to the channel by the customer. Normally, a channel will be adjusted for a 20, 40, 60 mA neutral loop or polar configuration; the customer provides the dc power source and current limiting devices to supply these specifications. The current loop module can be strapped to within +15% of any one of these parameters by positioning a jumper across the appropriate pins. The current loop module can be modified at the factory to accept any other "special" current between 10 and 60 mA. This accommodates customers which supply current different than the standards listed above. This "special" current loop module requires that the customer provide line balance to within 10% of the "special" current value.

The jumper labeled DATA allows the current loop module to accept either normal data (SPACE = OPEN loop and MARK = CLOSED loop) or INVerted data (SPACE = CLOSED loop and MARK = OPEN loop) from the data terminal.

The jumper labeled MODE is used to adapt the port module to either half-duplex (HD) or full-duplex (FD) operation, according to customer requirements.

3.5.2.7.4 Connection to User. Cabling between a current loop port module and associated data terminal can be connected in a variety of configurations according to customer requirements. Figures 3-22 through 3-24 show the more common configurations.

- Polar loop: see Figure 3-22
- Positive neutral loop, half duplex: see Figure 3-23
- Positive neutral loop, full duplex: see Figure 3-24

3.5.2.8 POWER SUPPLY STRAPPING AND CABLING. Figure 3-25 shows strapping and cabling for the 6030 series INP's (one power supply) and between multiple power supplies of the 6040 series. The terminal board shown has the ten connection points used in the supply that has two 4-Amp fuses.

In all versions of the power supply, the logic ground (TB1-6) and earth ground (TB1-7) are shipped strapped together, although the customer's application may require the strapping to be removed.

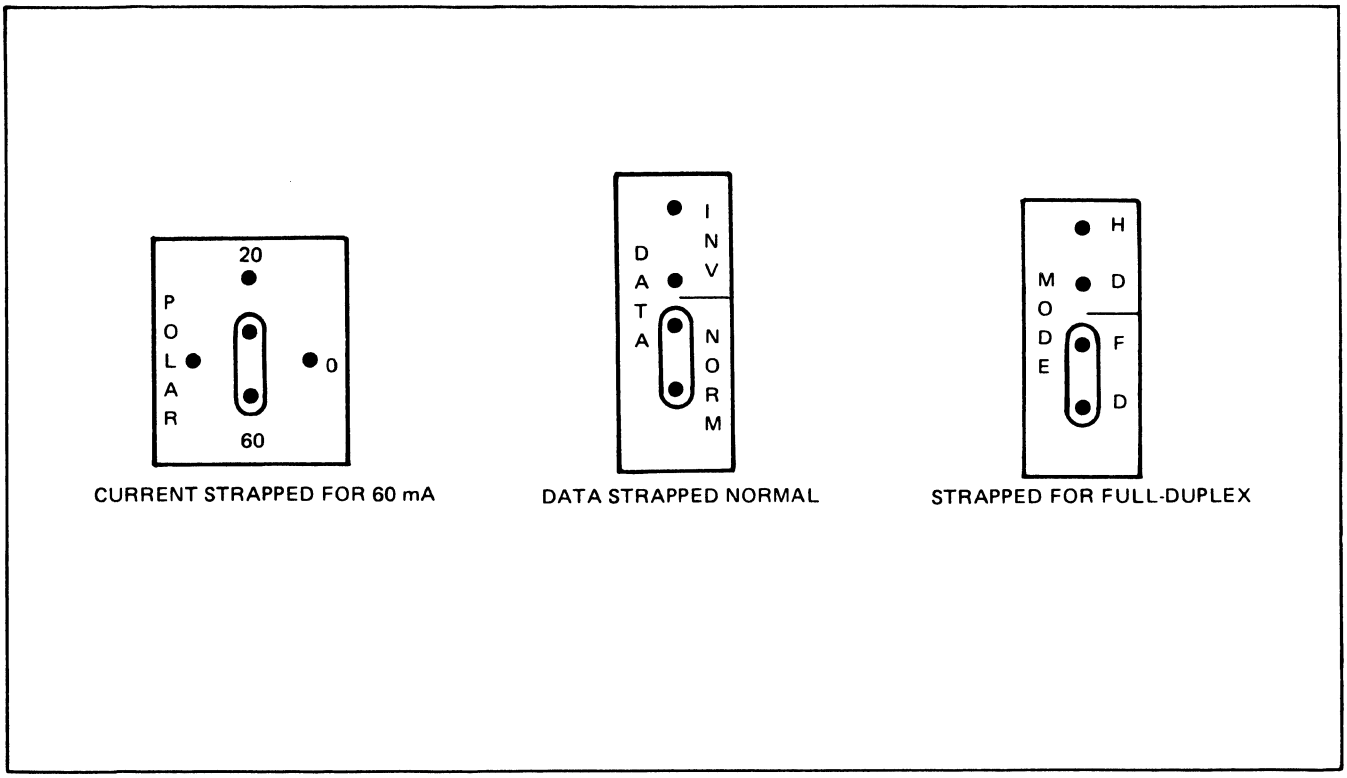
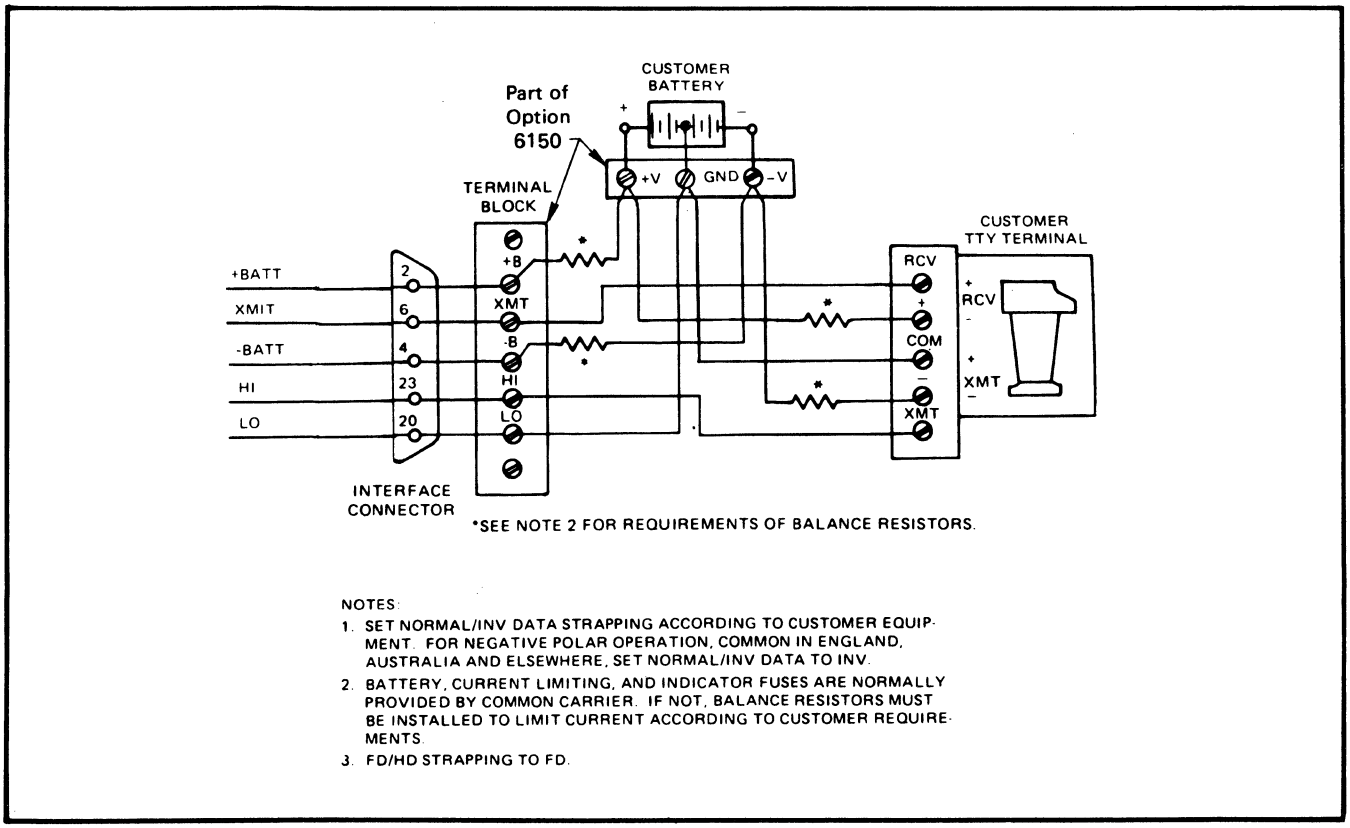


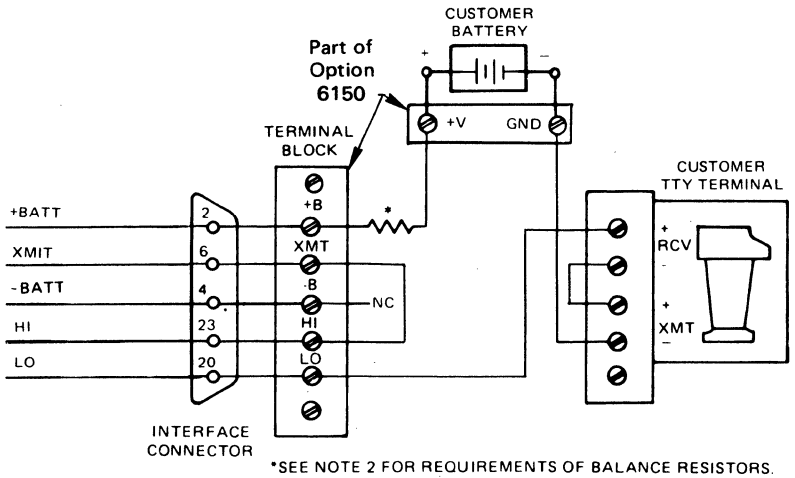
Figure 3-21. Strapping Diagram



NOTES:

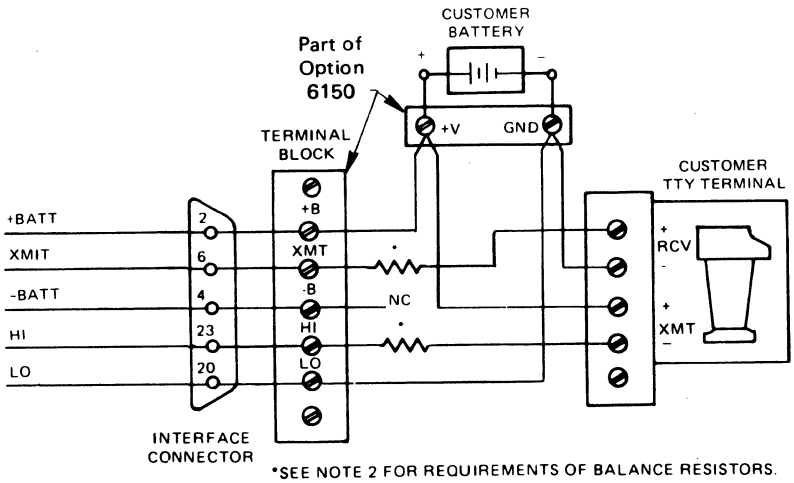
1. SET NORMAL/INV DATA STRAPPING ACCORDING TO CUSTOMER EQUIPMENT. FOR NEGATIVE POLAR OPERATION, COMMON IN ENGLAND, AUSTRALIA AND ELSEWHERE, SET NORMAL/INV DATA TO INV.
2. BATTERY, CURRENT LIMITING, AND INDICATOR FUSES ARE NORMALLY PROVIDED BY COMMON CARRIER. IF NOT, BALANCE RESISTORS MUST BE INSTALLED TO LIMIT CURRENT ACCORDING TO CUSTOMER REQUIREMENTS.
3. FD/HD STRAPPING TO FD.

Figure 3-22. Polar Loop Operation



NOTES:
1. SET NORMAL/INV DATA STRAPPING TO NORMAL.
2. BATTERY, CURRENT LIMITING, AND INDICATOR FUSES ARE NORMALLY PROVIDED BY COMMON CARRIER. IF NOT, A BALANCE RESISTOR MUST BE INSTALLED TO LIMIT CURRENT ACCORDING TO CUSTOMER REQUIREMENTS.
3. FD/HD STRAPPING TO HD.

Figure 3-23. Positive Neutral Loop, Two-Wire Half-Duplex Operation



NOTES:
1. SET NORMAL/INV DATA STRAPPING TO NORMAL.
2. BATTERY, CURRENT LIMITING, AND INDICATOR FUSES ARE NORMALLY PROVIDED BY COMMON CARRIER. IF NOT, BALANCE RESISTORS MUST BE INSTALLED TO LIMIT CURRENT ACCORDING TO CUSTOMER REQUIREMENTS.
3. FD/HD STRAPPING TO FD.

Figure 3-24. Positive Neutral Loop, Four-Wire Full-Duplex Operation

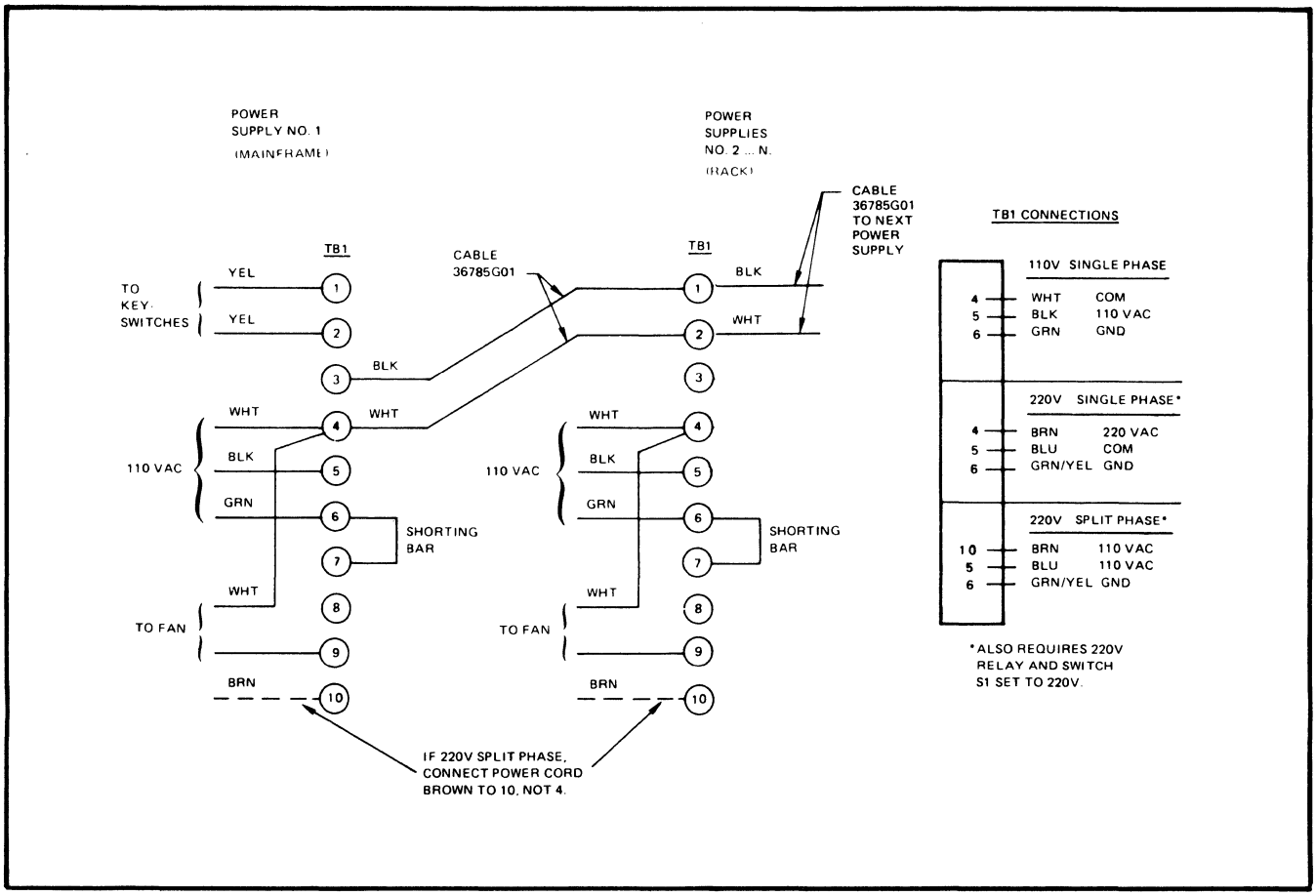


Figure 3-25. Connections on 200-Watt Power Supply with Two 4-Amp Fuses

3.5.2.8.1 Ground Strapping. Check to see whether the grounds AA and AB (EIA pins 1 and 7) are strapped together in the INP and also in the trunk modem. Both pieces of equipment are shipped with the straps in place because the straps are special and may be difficult to obtain in the field. Strap either the INP or the trunk modem, but not both.

3.6 INSTALLATION CHECKOUT PROCEDURES

After performing all internal cabling as shown in Figure 3-4A or 3-4B, verify that all strapping is correct for the network configuration. If the equipment is available, connect the network ports to the modems.

NOTE

Before applying power to the system, pause to consider that the firmware automatically boots the last booted configuration. Since the last configuration may not be known, the results may be unpredictable. It is better to boot the null configuration after powering up the system.

3.6.1 BOOTING THE SYSTEM

1. Turn the keylock to any position other than OFF and issue the command, BOOT 5 ENTER.

   An asterisk will appear on the self-scan display, indicating a message in the queue.

2. Issue the command, EXAM A R ENTER. The message that appears should be:

   CC (meaning configuration complete - this verifies communication capability from the INP to the modem and back).

3. If the message was CC, go to step 4. If the message was DN, the network port is down. Check all connections: NP cabling, NP and modem straps, and modems. Then reboot. If BOOT 5 ENTER is not successful, try BOOT 6 ENTER to check the internal operation of the 6000. If BOOT 6 ENTER is not successful, the problem is in the hardware, probably a TP. Call Codex Field Service.

4. When CC is displayed, call the next message by the command, ENTER. The display should be:

   FA (meaning framing acquired). The network link control is receiving good frames from adjacent nodes. Check the modem link, put remote modems into loopback, and recheck. When all messages in the queue have been displayed, the self-scan will display the message, EMPTY.

5. Once the system is running with BOOT 5, proceed to configure the network.

3.6.1.1 DIAGNOSTIC BOOT: BOOT 6 ENTER. The Diagnostic Boot causes the local node to load a null configuration with the local network port in local loopback. The response should be - CC and FA (or FA and CC).

Any other response, or the lack of a response, indicates a system failure. All cabling and strapping should be checked, then the Diagnostic Boot command reissued. If CC and FA messages are not received now, contact Codex Field Service.

A successful Diagnostic Boot permits configuration of the local node only, i.e., at the node at which the BOOT command was issued.

Once a configuration is loaded, checked, and booted successfully, diagnosing individual port problems can be performed.

In order to examine a port's EIA interface signals, select the appropriate node and port and issue the command:

(EXAM) (M) (ENTER)

This results in a display of all of the active EIA interface signals for the specified port.

If DTR (CD) and RTS (CA) are not active, the local port's receiver and the remote port's transmitter will not function. If DSR (CC) and CAR (CF) are not active, the local port's transmitter will not function. If DSR and CAR are not active, check the remote port's DTR and RTS signals. If they are not active, check the terminal and the cable for a bad connection.

If all of the interface signals appear to be correct and data does not pass correctly, check the system network configuration (characteristics, activity, transmit data path, and receive data path) for end-to-end compatibility and consistency with the terminals being used.

If further testing of a terminal port path is required, each terminal port can be placed in either local or remote loopback. Select the appropriate node, port, and configuration; then issue the following commands:

(CHNG) (A) (M) (ENTER)

(L) (ENTER)	For local loopback.
or	
(R) (ENTER)	For remote loopback.

3.6.2 REMOTE REBOOT OF THE SYSTEM

Setting the network port mode (M=) parameter to BT (boot) will cause the adjacent node to boot the configuration that is active at the node requesting the boot.

Setting the mode of the network port to BT permits N02 to reboot N01 (see Figure 3-26). An NB (network port boot) message will be displayed on the self-scan screen, and an NP boot sequence will be sent every 10 seconds as long as a framing lost (FL) condition exists. After the first NP boot sequence, the N02 mode parameter reverts to M=N (even though the NP boot sequences continue to be sent). N01 will then boot the configuration active at N02, which subsequently causes N02 to reboot the same configuration.

If a framing lost condition has occurred, set the adjacent NP's mode to BT. The system should reboot almost immediately, using the currently running configuration, e.g., the configuration at N02.

Example:

(SEL) (N) (#) (#) (ENTER)	(#) (#) = Number of the adjacent node.
(SEL) (P) (#) (#) (ENTER)	(#) (#) = Number of the network port.
(CHNG) (A) (M) (ENTER)	Change mode to BT.
(B) (T) (ENTER)	

If, Node 1 has established communication with itself, the NP boot sequence is sent only once since there is no FL (framing lost) condition (see Figure 3-27).

NOTE

Node 1 will NOT be rebooted by its own boot sequence.

N0 will boot the configuration that is active at N01, which subsequently causes N01 to reboot the same configuration.

If a frame lost condition has not occurred, but it is suspected that the content of C0 at one of the nodes is not correct, issue a BOOT 5 command, then set the local node's NP mode parameter to BT. This should cause the remote node to also boot C5. Once both nodes have C5 active, the content of the suspected incorrect configuration memory may be examined and/or changed, then booted.

Example:

(BOOT) (5) (ENTER)

(SEL) (N) (#) (ENTER) # = number of local node,

(SEL) (P) (#) (#) (ENTER) ## = number of NP.

(CHNG) (A) (M) (ENTER)

(B) (T) (ENTER)

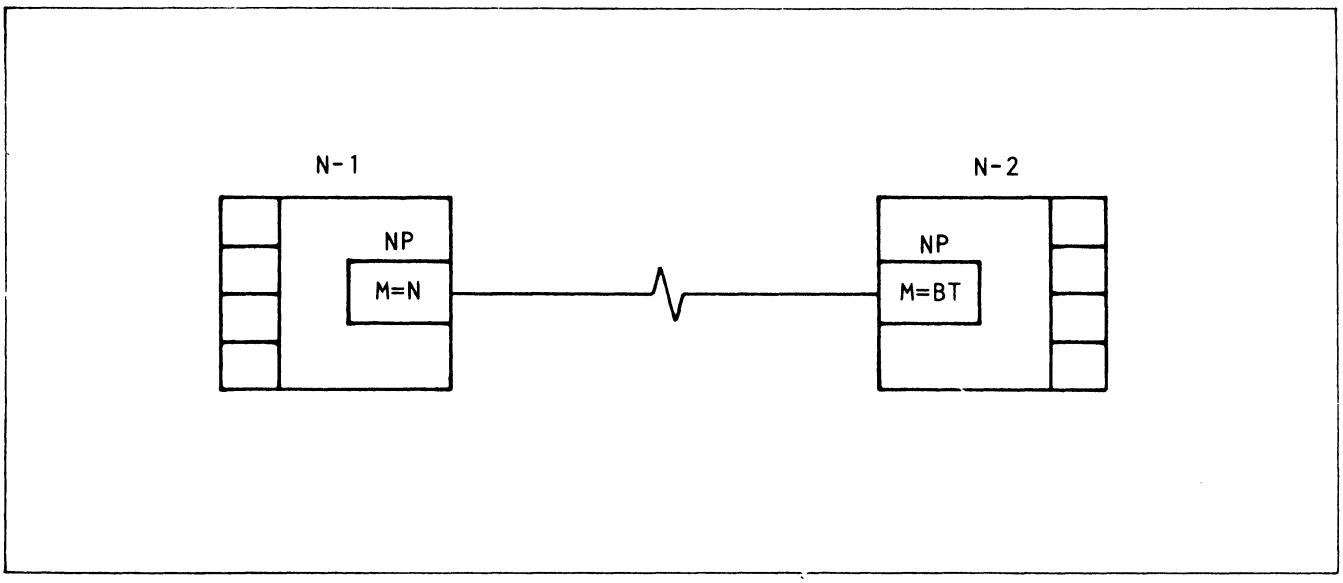


Figure 3-26. Network Port BT Mode (Remote Mode = N)

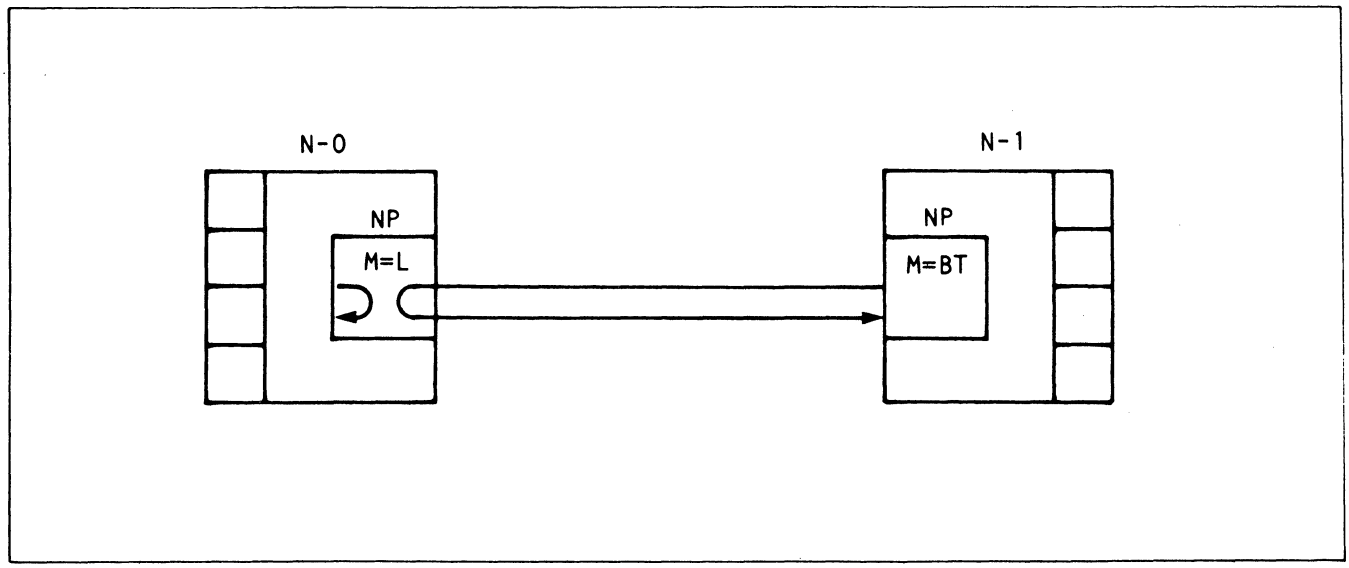


Figure 3-27. Network Port BT Mode (Remote Mode = L)

3.7 INSTALLATION HINTS

3.7.1 GROUNDING THE SYSTEM

To eliminate the possibility of establishing a ground loop potential, all communications equipment at each location should have both their signal grounds and chassis grounds connected in series except at one point in the system, normally host computer's the INP.

3.7.2 "DEAD" PORTS

In many cases a TP that fails to respond does not indicate a bad port. If the TP card is removed while the system is operating, the software will cease to recognize the port until a CHNG C S ENTER command is issued via the operator console or CTP.

3.7.3 PRE-CONFIGURATION ACTIVITY

Before attempting to configure a new system, make sure that all configuration parameters for that CMEM are "empty". Use the following procedure.

SEL C 1	Or whatever CMEM is to be configured
ENTER	Do it
CHNG E C E	Change configuration to empty
ENTER	Do it
1	Or whatever CMEM was selected above
ENTER	Do it.

CHAPTER 4

PRINCIPLES OF OPERATION

This chapter provides functional descriptions of both the software/firmware and hardware of the 6030/6040 Intelligent Network Processors. It contains nonproprietary background information of interest to persons who may perform maintenance/service on the equipment.

4.1 MOVEMENT OF DATA WITHIN THE INP

Two types of data are handled within the INP software system: (1) external data received from a terminal port, and (2) internal control information passed between software modules residing in the same or different nodes.

4.1.1 EXTERNAL DATA MOVEMENT

Movement of external data through the node from NP to TP or TP to NP, is bidirectional with each direction being processed independently. The processing performed for each direction is described below and the data movement is shown in Figure 4-1.

4.1.1.1 TERMINAL PORT TO NETWORK PORT. Processing of data for this direction begins when a character from the terminal is received by the terminal port, resulting in a hardware service request being generated.

When a processor becomes available, the hardware service request is picked up, and the processor dispatches the request to the terminal port driver. This software module processes the character according to the type of port. Checks are made for parity, overrun, and framing errors. Checks are also made for changes in control signals. The character or control signal change is then placed into the port's TP-to-NP buffer.

The transmit driver of the network port operates asynchronously with respect to the terminal port driver. When the network port's built-in FIFO requires more data, a hardware service request is generated. When a processor again becomes available, the service request is dispatched, this time to the software module that handles the network port, the network port control module (NPCM).

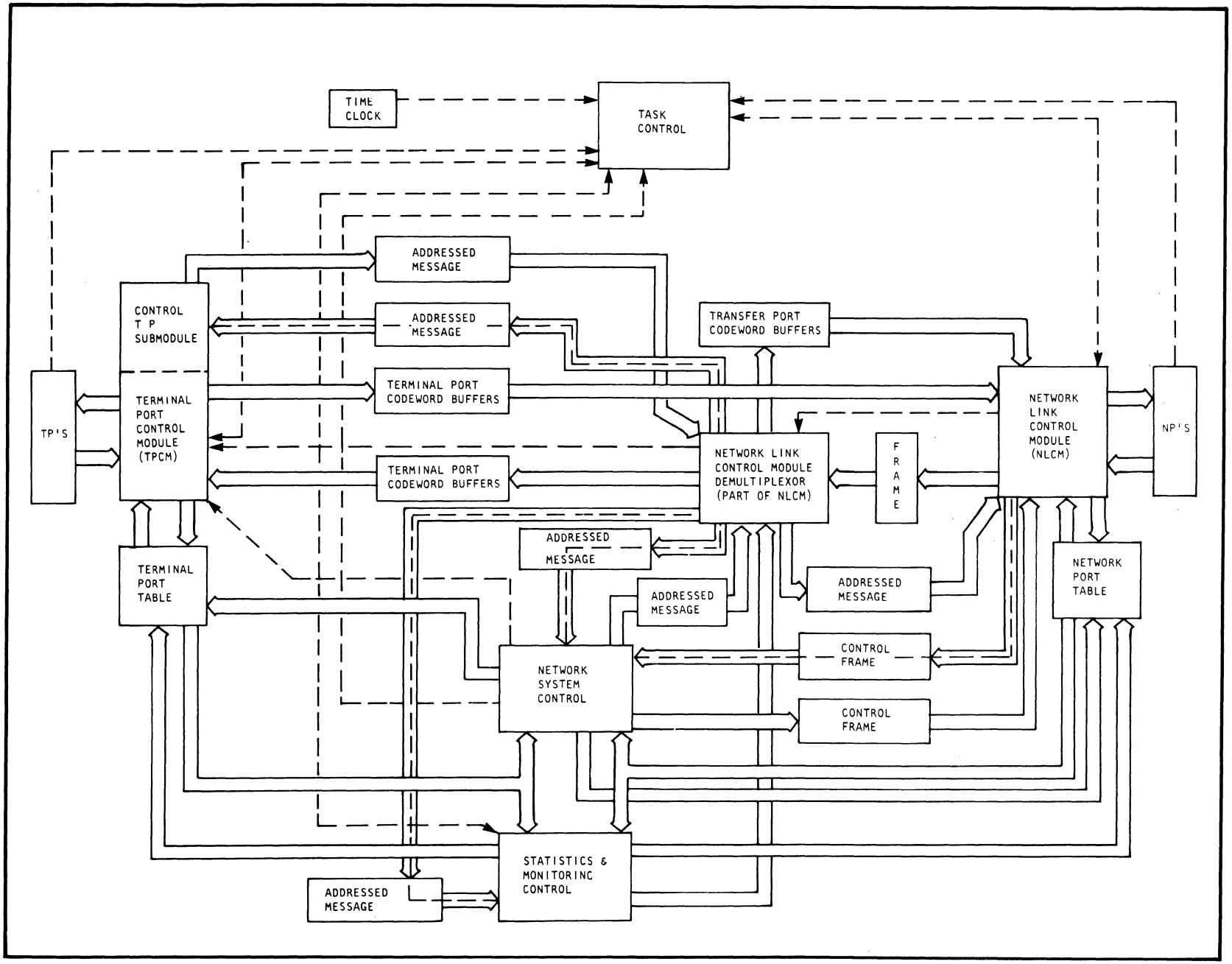


Figure 4-1. Movement of Data Within the INP

The software module continues to build and transmit frames. It also saves a copy of the frames queued-up in buffers in case retransmission is required. During the transmission of each frame, each of the terminal port buffers is checked to determine if it is empty. If a buffer is not empty, the data is removed one byte at a time, encoded, and transmitted. The maximum number of characters transferred for a particular terminal port is specified by the slot weight of the terminal port.

At the end of each frame the network port driver checks the ACK/NAK information received from the other node. It deletes any ACKed frames from its retransmit queue, but if a NAK indication is received it starts with the first frame in the retransmit queue and retransmits all of the frames on the queue before sending the next frame.

4.1.1.2 NETWORK PORT TO TERMINAL PORT. Processing of data in this direction begins when data from the frame enters the network port receiver FIFO buffer, causing a hardware service request to be generated. The hardware service request is dispatched to the network port receiver driver when a processor becomes available.

The network port receiver driver then removes the data from the FIFO and decodes it before placing it into a frame buffer. When the entire frame is received the error check code is checked to determine if an error occurred. If an error did occur, the frame is thrown away and a NAK indication is passed to the network port's transmit driver which will transmit it to the remote node in next frame sent. If no error occurred, the frame buffer is passed to the distribution module which is started (if it isn't already running).

The distribution module distributes the data to the proper NP-to-TP for each terminal port. It also starts the terminal port driver for each idle port for which it has data. Otherwise the driver will be started by a hardware service request from the terminal port when transmission of the current character is complete.

When a processor becomes available it picks up the terminal port's service request, removes one character from the buffer, and outputs it to the terminal port.

4.1.2 INTERNAL CONTROL INFORMATION

Because control information is distributed to many nodes throughout the network, a method is required to allow an operator to access any node from a single Operator's Console or Control Terminal Port. This is done using a built-in packet-switching system.

When a user requests information via the Operator's Console, a packet is built containing both a source address and destination address. Each address consists of a node number and the number of the software module that will process the packet at the destination node.

The packet system is designed to route the packets around links or nodes that have failed. Each frame transmitted by a network port has a slot reserved for the packet system. This slot may be empty or it may contain a packet. When the packet is received at the next node it is either routed to the terminal port in that node or forwarded to another node via another NP until the destination node is reached.

If the packet requires return information, a return packet is generated with the original source as the destination. When this packet is received, the information is then displayed for the user.

4.2 DATA COMPRESSION

Data is compressed to increase throughput by reducing the number of bits to be transmitted between nodes. This is done in two ways: (1) by converting uniform-length code characters (ASCII, EBCDIC, and Transcode) into variable-length codes that have shorter average lengths, and (2) by stripping overhead bits from the message. This section deals with the first method.

The basis for assigning a short or long code to a character is the frequency with which that character occurs in the text to be transmitted. In English text, characters such as space, e and t may be assigned 4-bit codes, while infrequently-used characters may have codes up to 14 bits in length.

Variable length coding leads to reductions of 50 to 60 percent in the link loading, although achieving them carries a penalty of extra processing steps at each end of the link: encoding at the transmitter to compress, and decoding at the receiver to restore them to standard characters.

Sending coded characters serially as a continuous stream of bits poses a problem of how the receiver can recognize the start of each character. This is achieved by the code structure. In it, no character can be the prefix of another character, so the beginning of each character is implicit in the code and no extra information is needed to separate the characters.

4.2.1 CODE SET WITH COMPRESSION AND PREFIX PROPERTY

As an example, consider a code set that has only four characters, A, B, C, and D, each of which has a known probability of occurrence, as shown in Table 4-1. Suppose half the characters actually transmitted were A's and one fourth B's, and one eighth were C's or D's. An appropriate variable-length code would map these characters into a code set as follows:

TABLE 4-1. SAMPLE COMPRESSION CODE

Character	Probability of Occurrence	Compression Code	Length, Bits
A	1/2	0	1
B	1/4	10	2
C	1/8	110	3
D	1/8	111	3

As a result, the average number of bits sent per character would be the sum of the products of character probabilities times the bit length for each character:

$$(1/2)\ 1 + (1/4)\ 2 + (1/8 + 1/8)3 = 1\text{-}3/4$$

which is 12.5% less than the 2 bits per character that would be obtained by uniform code. With larger alphabets and wider spreads of frequencies, greater savings can be obtained; 30% increases in efficiency are typical.

There is no problem in decoding such a code, despite the variable lengths, because the code has the prefix property that no codeword is the prefix (first part) of any other codeword. Thus, there is only one possible way that an arbitrary string of bits can be deciphered. The reader can verify that by writing a string of random 1's and 0's, and using the code table above to encode them. For example:

01100101111000... decodes as ACABDBAA..

A channel error may cause a short loss of synchronization as well as a character error, but in that case the error control system retransmits all the affected characters.

An additional advantage of the variable-length coding is that the transmitted characters are in a form which is extremely difficult to interpret without the applicable coding table, so a high degree of inherent data security and privacy is attained.

4.2.2 CODE TABLES

Two coding tables are provided as standard. Special coding tables for customers with unique applications can also be provided. A standard code table for typical ASCII terminals with parity allows compression of USASCII codes. Typically, compression ratios of 1.2:1 to 1.4:1 are obtained. A second code table is designed for 2741-type terminals. The third, obtainable as a special order, is for EBCDIC. The code table to be used for each port is specified by the operator as part of that port's configuration information.

An additional feature of the encoding process is that start/stop bits are stripped from asynchronous communication, providing an increase in efficiency of approximately 30%.

The compression efficiency statistic is defined as the number of bits input by the source terminal, divided by the number of bits transmitted to the adjacent node. Code type 3, ASCII code compression, results in an average compression efficiency of 7/5.2 = 1.3, while code type 5, 2741 Correspondence code compression, results in a compression efficiency of 6/5 = 1.2. Special compression tables should result in greater compression efficiencies.

For asynchronous traffic, compression efficiencies are the result of stripping start/stop bits, and of code compression. For ASCII, this results in a factor of (1.3) (1.3) = 1.7, and for 2741 correspondence a factor of (1.3) (1.3) = 1.7.

When using data compression, compression efficiency should be monitored via Option 6301, Network Monitoring and Statistics. A low value (near or at 100%) indicates a need for a different table.

The characteristics of codes used in systems running under S47 level software are shown in Table 4-2. The characteristics of codes used with S49 software are identical except for Code 5, which no longer is used for 2741 Correspondence. S49-applicable codes are shown in Table 4-3. Note that only code types 3 and 5 have non-uniform codeword lengths.

The following are comments on Table 4-2, codes used with S46 and S47 software.

Code Types 0 and 1 contain 256 different combinations and may be used for codes with 8 data bits including parity which is stripped/inserted at the TP.

Code Types 2 and 3 contain 128 different combinations and may be used for codes with 7 or 8 data bits including parity which is stripped/inserted at the TP.

TABLE 4-2. CODE TYPE CHARACTERISTICS (S47 SOFTWARE)

Code Type	Uses	Compression	No. of Data Bits (including parity* if any)	Control Char List (applicable only to BSC terminals)
0	a. BSC ASCII b. Any S/S terminal with 8 or less data bits c. Autospeed terminal if it cannot use 2	None	8 or less	ASCII
1	BSC EBCDIC	None	8	EBCDIC
2	a. BSC ASCII with no transparency b. Any S/S terminal using 8 data bits with parity, e.g., ASCII c. Any S/S terminal using 7 or less data bits d. Autospeed terminal with 2b 2c characteristics	None	8 with parity, otherwise 7 or less	ASCII
3	ASCII with parity (S/S or BSC with no transparency)	Standard	8 with parity	ASCII
4	a. BSC Transcode b. Any S/S terminal using 7 data bits with parity, e.g., 2731 c. Any S/S terminal using 6 or less data bits	None	7 with parity otherwise 6 or less	Transcode
5	2741 Correspondence	Standard	7 with parity	
6	a. Any S/S terminal using 6 data bits with parity b. Any S/S terminal using 5 or less data bits, e.g. Baudot	None	6 with parity otherwise 5 or less	
7 on	Custom Applications	As specified	As Specified	As Specified

*Parity odd even mark none or space for AP; odd even none or space for SP

TABLE 4-3. CODE TYPE CHARACTERISTICS (S49 SOFTWARE)

Code Type	Uses	Compression	No. of Data Bits (including parity* if any)	Control Char List (applicable only to BSC terminals)**
0	a. BSC ASCII b. Any S/S terminal with 8 or less data bits c. Autospeed terminal if cannot use 2	None	8 or less	ASCII
1	a. BSC EBCDIC	None	8	EBCDIC
2	a. BSC ASCII with no transparency b. Any S/S terminal using 8 data bits with parity, e.g., ASCII c. Any S/S terminal using 7 or less data bits d. Autospeed terminal with 2b/2c characteristics	None	8 with parity; otherwise, 7 or less	ASCII
3	ASCII with parity (S/S or BSC with no transparency)	Standard	8 with parity	ASCII
4	a. BSC Transcode b. Any S/S terminal using 7 data bits with parity c. Any S/S terminal using 6 or less data bits	None	7 with parity; otherwise 6 or less	Transcode
5	a. Any S/S terminal using 7 data bits with parity b. Any S/S terminal using 6 or less data bits	None	7 with parity	

TABLE 4-3. CODE TYPE CHARACTERISTICS (S49 SOFTWARE) (CONT)

Code Type	Uses	Conpression	No. of Data Bits (including parity* if any)	Control Char List (applicable only to BSC terminals)**
6	a. Any S/S terminal using 6 data bits with parity b. Any S/S terminal using 5 or less data bits, e.g., Baudot	None	6 with parity; otherwise, 5 or less	
7 on	Custom Applications	As specified	As specified	As specified

*Parity = odd/even/mark/none or space for AP; odd/even/none or space for SP.
**Garble characters produced by incorrect parity are " (ASCII); X or x (2741 Correspondence); ? or / (2740 EBCD).

Code Type 3 is the standard ASCII compression table. This table has the following Huffman code length distribution:

1 3-bit codeword, 14 5-bit codewords, 33 7-bit codewords, 2 8-bit codewords and 87 9-bit codewords

Code Type 4 contains 64 different combinations and may be used for codes with 6 or 7 data bits including parity which is stripped/inserted at the TP.

Code Type 5 contains 64 different combinations, and is used with 7 data bits including parity. The parity bit is stripped/inserted at the TP.

Code Type 6 contains 32 different combinations and is used for Baudot code of 5 data bits or other codes with 6 data bits including parity which is stripped/inserted at the TP.

Appendix E contains listings of the character sets for the codes, the hex codes for the characters, and the length in bits.

4.2.3 GARBLE CHARACTER

The garble character provides a primitive form of error detection when a start/stop terminal inputs a character with an error. The garble character is generated in the transmitting node when one of the following three errors occurs: (1) If there is a framing error because no stop bit is input at the end of a character, (2) if there is an overrun error because a new character is input before the terminal port has processed the previous character, or (3) if there is a parity error because the parity for a character does not match the parity for the configured code type.

When an error occurs, the terminal port throws away the bad character and replaces it with the garble character. The garble character is a valid data character, so it is passed over the link and through the destination node to the terminal.

The garble character sent is: " for ASCII,
X or x for 2740 Correspondence, or
? or / for 2740 EBCDIC.

When the destination terminal receives a garble character, the operator there must observe it and manually ask the transmitting terminal for a retransmission, using Option 6323, Supervisory Communication Support, if available.

4.2.4 CUSTOM DATA COMPRESSION TABLES

Codex provides special data compression tables for customers whose messages use a unique character set or whose standard character set has a nonstandard frequency distribution.

Special tables are handled on a RPQ basis. The customer must provide a listing of his character set and the associated frequency distribution of its characters.

To facilitate the processing of customer-provided information in generating custom compression tables, the following standard format is used for the customer-submitted data: The code (ASCII, EBCDIC) is listed in ascending order (00 through FF), with the corresponding probability of occurrence of each character calculated to 4 decimal places.

Any other information such as raw character counts and printable graphics is helpful, but not required.

4.2.5 TRANSMIT FRAME CONSTRUCTION

Figure 4-2 represents the construction of a transmit frame by the software module called the network link control module. Four terminals generate characters and input them to terminal port buffers. At the moment depicted, terminals 1 and 4 are inputting at a rate that keeps their buffers nearly full. Terminal 2 is inputting slowly and terminal 3 is temporarily inactive so that no buffer space is assigned to it.

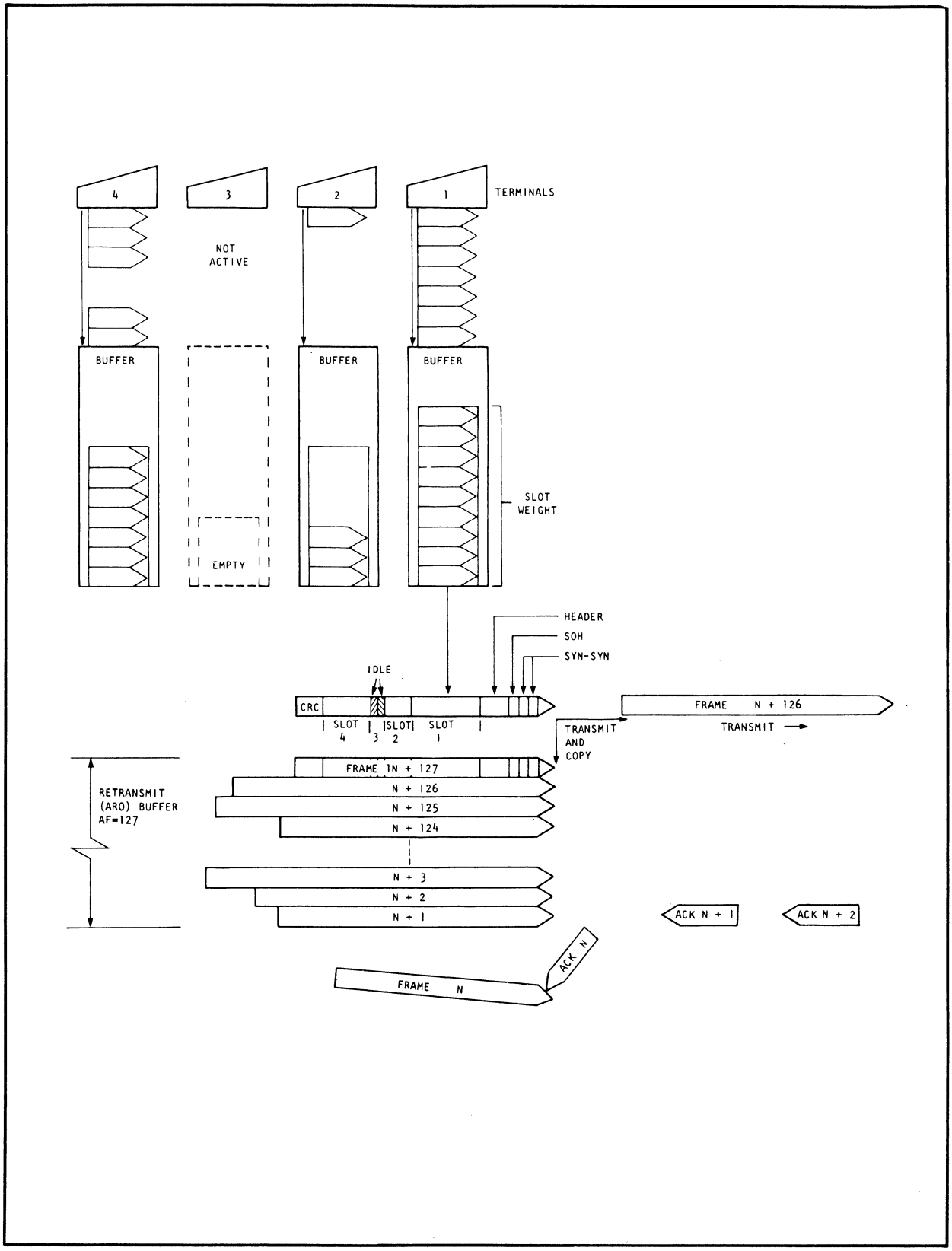


Figure 4-2. Frame Construction and Buffering

When the network port needs data for transmission, the network link control module takes uniform-length characters from the buffers, processes and code-compresses them, and proceeds to construct a transmit frame with them. It cycles in sequence through the terminal buffers, removes from each buffer the maximum number of characters allowed, and places those characters in a dedicated slot in the frame. The maximum number of characters that may be taken from any buffer is called the slot weight, and is a definable characteristic of the terminal.

In the figure, the slot weight is represented by an opening in each buffer, through which the allowed number of characters is removed. The characters are removed one byte at a time, encoded, and then simultaneously are transmitted and copied to a retransmit buffer for possible later transmission.

Compression of uniform-length characters is represented by the shortened (variable-length) codes in the transmit frame. A short idle code fills the slot assigned to the inactive terminal, and another terminates the partially-filled slot for terminal 2.

Frames in the transmit buffer are of varying lengths. At the bottom of this buffer a returned acknowledgement causes the dropping of the corresponding frame from the buffer. If there are previously transmitted but unacknowledged frames in the buffer, they are dropped too.

CHAPTER 5

DIAGNOSTICS

5.1 INTRODUCTION

The procedure followed in troubleshooting and diagnostics of hardware failure is to verify that a fault is not in the operating procedure, therefore it must be in the hardware. The next move is to isolate the problem to a specific board, to replace the faulty board, and to verify satisfactory operation. The diagnostics do not verify or check operation of the software.

Apart from the simple external problem arising from failure to apply line power to the INP, most hardware failures can be pinpointed by use of the diagnostic ROM. This is a standard INP ROM with specially-designed chips for testing hardware that operates under any software release up through S47 (Option 6450) or S49 (Option 6451).

The diagnostic ROM is installed in either of the ROM slots in the mainframe, after both standard ROMs are removed. It checks only the hardware of the node in which it is installed.

The tests fall into two groups: (1) preliminary, which run automatically when the INP is started up, and (2) the main diagnostics, which must be called for specifically, either by individual test or by groups or families of tests that check the various functions of a particular type of module.

All communications with the INP employ the operator's control panel. Inputs are made on the keypad and outputs are displayed on the self-scan and/or the mode lamps, the processor ID lamps, and the processor status lamps. The diagnostics cannot be executed from a control terminal port (CTP).

Hardware failures are indicated by either an error message on the self-scan or by abnormal termination of a diagnostic test. In either case, the card under test is identified as "suspect". Where there are multiple cards of a type, the failure can be pinpointed to a specific card by card swapping.

A recommended troubleshooting sequence is to get the mainframe going first, then the port nests. In checking the mainframe, start with the option card and one processor, MC1 and MC2, one RAM, and the diagnostic ROM.

5.2 OPERATION

This section presents the operating procedures step by step. A summary of the procedures appears in Section 5.2.8.

5.2.1 STARTUP PROCEDURES

The startup procedures for INPs with and without operators consoles differ only slightly.

5.2.1.1 6000's WITH OPERATOR CONSOLE

a. Turn off the ac power.
b. Remove all ROM boards (see Figure 5-1).
c. Install diagnostic ROM card in any of the ROM slots.
d. Verify that the RAM cards are in slots adjacent to each other.
e. Turn keylock to DIAG. The self-scan display momentarily displays:

0-:SH2:00:01 DIAGNOSTICS REV:11

and the sequence described in Paragraph 5.2 follows immediately.

NOTE

If the machine starts up normally, but will not start with the diagnostic ROM in place, there may be a defective RAM chip. Section 5.6 describes this problem and its solution.

5.2.1.2 6000's WITHOUT OPERATOR CONSOLE

a. Turn off the ac power.
b. Connect the portable operator console as follows:
   1. Insert the ribbon cable into the receptacle behind the flip-up door on the front panel.
   2. Connect the dc power cable to either connector or the power supply.
c. Remove all ROM cards (see Figure 5-1).
d. Install the diagnostic ROM card in any of the ROM slots.
e. Verify that the RAM cards are in slots adjacent to each other.

0-:SH2:00:01 DIAGNOSTICS REV:11

and the sequence described below follows immediately.

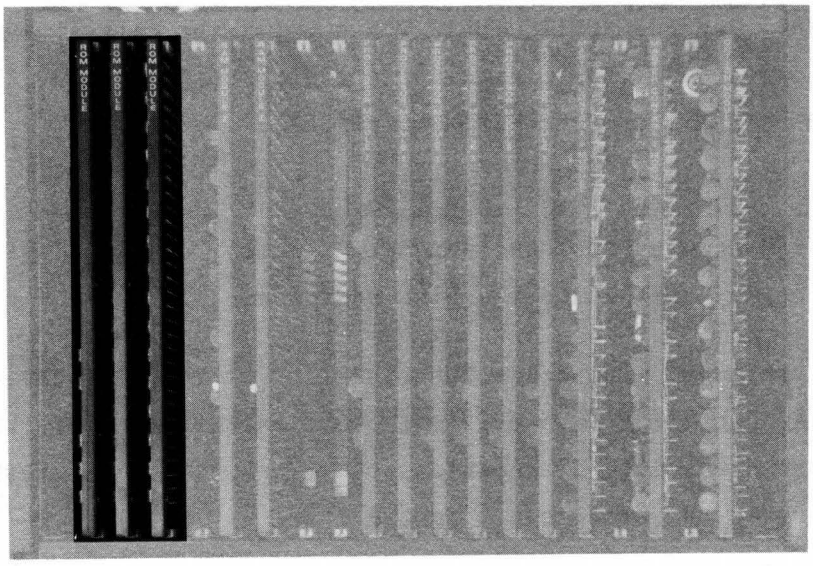


Figure 5-1. ROM Card Location

5.2.2 PRELIMINARY DIAGNOSTIC TESTS

A sequence of preliminary diagnostic programs is executed automatically after a power up or a preemptive BOOT has been entered by the operator. These programs must run to completion to ensure minimum functionality of the INP. If necessary, replace defective boards until this point has been reached.

The preliminary tests are described in the next five paragraphs.

5.2.2.1 PRELIMINARY ROM TEST (TSC = 01). The contents of the diagnostic ROM card are checksummed and compared to the prestored correct value.

5.2.2.2 PRELIMINARY PROCESSOR RUN-HALT TEST (TSC = 02). The master controller verifies that all processors except processor 0 are halted. The number of processors which can be selected is displayed for operator verification. If the number of processors is incorrect, the processors that can be counted can be found by displaying

location E3. To do this, use the MEM preemptive function (see Section 5.2.5). A bit is set in that byte corresponding to each processor that is present; e.g., location E3 = 5 means processors 0 and 2 are present. Press GO to continue.

5.2.2.3 PRELIMINARY RAM DIAGNOSTIC TEST (TSC = 03). The highest memory location which responds is located and displayed for operator verification. The display for 16K memory should be 3FFF; and for 32K memory, 7FFF.

CAUTION

The RAM modules must be in adjacent slots, or the diagnostic may not locate the high addresses.

Press GO to continue. The basic functionality of memory locations X'20' through X'2F' and X'80' through X'7FF' is verified. More extensive memory testing is performed by programs in the main diagnostic system. While the RAM test is running, random text appears on the self-scan. Ignore it.

5.2.2.4 TP AND NP COUNT VERIFICATIONS (TSC = 04). The operator is asked if TP tests will be executed with any TP's running at a special speed. Press ENTER if no, press CLEAR if yes. If the response is yes, further information will be asked at the beginning of the first applicable TP test that is executed.

Next, the number of NP's that respond is displayed: Press GO to continue.
Then, the number of TP's that respond is displayed: Press GO to continue.

The NP's and TP's that respond can be determined by examining, with the MEM preemptive function, the I/O map that begins at location 1000. Location 1000 plus the TP address will equal 1 if a TP is present. Location 1000 plus the NP address plus 2 will equal 2 if an NP is present.

5.2.2.5 PRELIMINARY FRONT PANEL DIAGNOSTIC TEST (TSC = 05). Test TSC = 05 requires operator intervention to complete. Check the text displayed on the right half of the self-scan (see Table 5-1) and push the CLEAR key to continue the test.

Next press all 18 keys in the sequence 0, 1, - - -, E, F, ENTER, CLEAR. The keys are echoed back to the self-scan as they are pressed, with [ENTER] being echoed for ENTER. If the correct sequence is not followed, no character will be echoed and the diagnostic program will wait for the expected key to be pressed.

TABLE 5-1. TSC = 05, SELF-SCAN DISPLAYS

Text Displayed and To Be Checked	Operator Action
@ A B C D E F G H I J K L M N O	Press CLEAR
P Q R S T U V W X Y Z [~]	Press CLEAR
! " # $ % ¢ ' ( ) * + , - ° /	Press CLEAR
0 1 2 3 4 5 6 7 8 9 : ; < = >	Press CLEAR

When the front panel test is thus completed, the display is:

0-:SH2:00 TSC(1): 7F/

5.2.3 SELECTION OF TEST SEQUENCE CODE (TSC)

The TSC(1):7F/ display signifies that the system is in the "command mode", which allows selection of the test sequence(s) the system will execute, as defined by the Test Sequence Code (TSC). The diagnostics will execute all defined test sequences, in order. When control is returned to the operator, all test sequence definitions, except TSC(1), are erased if the preemptive control mode interrupt is used.

The diagnostics permit programming of up to 15 test sequences defined by TSC(1), TSC(2), - - - TSC(F). Each TSC may define:

a. A single test; e.g., enter digits 1 and 2 for test No. 12.

b. A group of tests; e.g., enter hex digits 1 and F, whereby F indicates all tests in group 1-. (Section 5.2.8 shows tests singly and by groups.)

c. All groups, all tests: enter hex digits FF, where the first F indicates all groups and the second F all tests within each group.

d. All tests No. 1 in all groups: enter hex digits F and 1. This is a quick test of the basic functions of all groups.

NOTE

All the following tests must be selected separately:

1. Off-line configuration memory tests 37, 38, 44, and 45. (Tests 37, 38, and 44 may change CMEM; Test 45 will change CMEM.)
2. TP tests in the 7F and 8F series.
3. NP reboot test 67.

To define a TSC the operator inputs:

Hex digit Hex digit ENTER

See Section 5.2.8 for the list of main diagnostic tests. The self-scan echoes the two digits. Pressing the ENTER key causes the diagnostics to accept the next TSC; the display will be:

TSC(2):00/

If no more TSC selections are required, pressing the CLEAR key once causes the self-scan to indicate TSC(1):nn/, where nn is the TSC(1) mode. The remainder of the programmed TSC's may be checked by repeated use of the ENTER key. A TSC definition can still be changed at this time. Pressing the CLEAR key in the TSC(1) mode causes a transition to the TCC mode. The self-scan will be:

INPUT TCC:

5.2.4 SELECTION OF TEST CONTROL CODE (TCC)

The test control code consists of three characters which specify the action to be taken at the end of the test sequence or when an error is detected, followed by an ENTER.

a. Character 1: Specifies the action to be taken during and at the end of the test sequence. Three codes are acceptable:

R - At the end, restart the test sequence again.

S - At the end, stop and return to operator control.

W - At the end of each individual test wait; continue when GO key is pressed.

At the end of the entire test sequence, stop and return control to the operator.

The test control return messages depend on the choice of character 1.

R - The self-scan displays (in hexadecimal) the number of auto restarts that have occurred.

AUTO RESTART #0001

S - The diagnostics return control to the operator after the previously selected test sequences are completed and displays:

TSC(1):nn/

W - The system waits after each test and displays:

** CTRL WAIT **

This display remains on the self-scan during all tests following the first selected test. If CTRL WAIT is displayed while the PGM mode indicator is lit, the test sequence is still in progress. The end of the test sequence is indicated by a lit MON mode indicator. Now, pressing the GO key causes control of the diagnostics to return to the operator. The WAIT function allows the operator to examine the results of the test internally by using the MEM command.

b. Character 2: Specifies whether a test should halt or not when an error is detected. Two codes are acceptable:

H - Halt (pushing GO key resumes running).

N - No Halt (except for error message 990 - spurious processor restart).

c. Character 3: Specifies how to resume testing after an error is detected. Eight codes are currently acceptable:

0 - Continue with test.

1 - Go into tight loop around that portion of the diagnostic program which failed. It will continue to loop as long as the error is detected.

2 - Rerun the diagnostic test that failed (after ENTER is pressed).

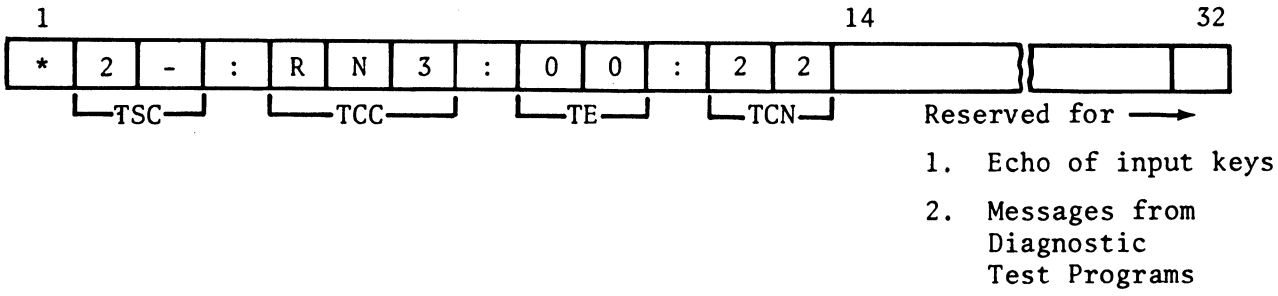
3 - Rerun the complete test sequence (after ENTER is pressed).

4 - Run the next test in sequence (after ENTER is pressed).

5 - File the error data and continue the test. (Used only with RN5.)

6, 7 - Return to operator control

When the TCC selection has been completed, the diagnostics immediately execute the selected test sequences. The left 14 positions of the self-scan indicate the current state of the diagnostics, formatted as follows:



NOTE

Hex F displays as - .

* Message waiting flag. The asterisk will be displayed when two or more processors have a message to be displayed. Pressing the ENTER key clears one message and causes the next message to be displayed. When the last message is displayed, the asterisk will disappear and the word EMPTY will appear.

TSC Currently executing Test Sequence Code.

TCC Test Control Code.

NOTE

When inputting TCC, if the operator wishes to use the TCC that is displayed, ENTER is pushed.

TE Total number of errors detected during the current (or last) test sequence. (2 digit hexadecimal counter which overflows to a count of X'F0'.)

TCN Number of the test which is currently running.

5.2.5 PREEMPTIVE CONTROL MODE

The preemptive control mode allows the operator to interrupt the diagnostics to change the test sequence in progress, or to examine or change the contents of memory.

The preemptive control mode is entered by performing the following actions:

a. With the keylock switch in MON or PGM position, press any key.

b. Turn the keylock switch to DIAG.

c. Press the desired preemptive function key.

The preemptive functions that can be activated are:

Key	Action
BOOT	Reboot diagnostics - reexecutes preliminary diagnostics (TSC = 01 through 05).
CTRL	Terminate current test and return control to the test operator. (This skips preliminary diagnostics.)
STEP	Terminate current test and proceed to the next test in the current test sequence.
HELP	Display current program counter and current stack pointer. Add X'17' to the stack pointer to get the program stack pointer. When CLEAR key is pressed, proceed to the MEM preemptive control function.
MEM	Examine, and optionally change, the contents of a memory location. ADR: = Prompt for address ADR: nnnn mm/ = Prompt for change nnnn = memory address (in hex) mm = contents of memory (in hex) CLEAR key = Terminate and proceed to the GOTO preemptive control function or enter new address or enter new value.

GOTO — Start execution at the address provided by the operator via the keyboard. If no address is entered (e.g., CLEAR key is pressed), resume previous state before entering the preemptive control mode.

EXAM — Examine (and optionally change) the off-line configuration memory. Examine the option PROM. (Functions similarly to MEM above.)

DIAG — Examine the error file created if in RN5 TCC mode. The error file display is as follows:

RECORD No./ERR(error) No./X REG/A REG/B REG/RST(restart)No./TEST No.

Press ENTER to examine the next file entry. The record number will not advance if the present record number is the last.

Press any key except ENTER or CLEAR, then press ENTER to examine the previous record.

Press CLEAR to continue the test that was interrupted.

For TP and NP errors, the lower two digits of the X register are the address of the failed port. A preemptive BOOT or CTRL clears the error file.

SEL — Selects the next processor for panel display. Used in special data-gathering procedures.

5.2.6 RETURN TO NORMAL OPERATION

When all diagnostic tests run with no failures indicated, return to normal operation. Turn off the ac power, then remove the diagnostic ROM card and replace all firmware ROM cards. The ROM cards can be placed interchangeably in the access ROM card slots. Then turn on the ac power.

5.2.7 S46 AND S47 CHECKSUMS

One last item remains to be verified: the checksum of the firmware on the ROM cards. The checksum procedure verifies that the contents of the installed firmware agrees with that installed initially by Codex. The procedure for obtaining the checksum is:

	Operator Action	Resultant Display
a.	Press any key when system is in PGM or MON mode	-
b.	Turn keylock switch to DIAG	-
c.	Press CTRL key	CTRL
d.	Press RSET key	CKSM FROM
e.	Enter: 8000 ENTER	CKSM FROM 8000 TO
f.	Enter: FFFF ENTER	CKSM FROM 8000 to FFFF

After a few seconds delay	CKSM FROM 8000 TO FFFF XXXX (where XXXX represents the checksum in hexadecimal)

The correct checksums for software currently in the fild are:

Release: Revision	8000 to FFFF	8000 to BFFF	C000 to FFFF
46.02	C0C5	32D3	8DF2
46.03	A409	2988	7B51
46.04	94B6	2988	6B2E
47.02	9E42	D31D	CB24
47.03	6A76	D630	9445
47.05	3CC5	D377	694D

If the checksum obtained in the test is not correct, replace one or both firmware ROM cards until it is correct.

5.2.8 S49 CHECKSUMS

There are four ways the S49 checksums can be computed and displayed: (1) compute and display the main software area once, (2) same as 1, plus compute and display continuously, (3) compute and display the specified area checksum once, and (4) same as 3, plus compute and display continuously. The procedure for each is presented below.

NOTES ON THE DISPLAYS

1. Addresses are 5-digit hex numbers. If a 4-digit number is entered, pressing ENTER will prefix 0 to the address.
2. TO in an address range is abbreviated to "T".
3. If a continuous display is ordered, the machine is deaf to commands while it is computing, so CLEAR has no effect unless pressed between computations.

The following specific addresses will display a checksum of 0000:

Address	Contents
8000 to 8FFF	Code table.
18000 to 193FF	High bank ROM, including both of below.
18000 to 18BFF	Supervisory control port.
19000 to 193FF	Logging control terminal port.

as will the following general form:

RSET, ENTER, ENTER or RSET, ENTER, C, ENTER

which addresses the software area between the variable low address and the high address BFFF. This is a convenient form that eliminates the need for knowing the low address for each system configuration.

Any other specific address will display a hex 5-digit address.

If the checksum obtained in the test is not correct, replace on or more ROM boards until it is.

5.2.8.1 ONE-TIME DISPLAY OF MAIN AREA CHECKSUM

Operator Action	Resultant Display
Turn keylock to PGM.	PGM light on.
Press SEL, CTRL, ENTER.	CTRL
Press RSET, ENTER, ENTER.	Computed main area (less code table) checksum displayed once. If there is no error, the checksum is 0.

5.2.8.2 CONTINUOUS DISPLAY OF MAIN AREA CHECKSUM

Operator Action	Resultant Display
Turn keylock to PGM.	PGM light on.
Press SEL, CTRL, ENTER.	CTRL
Press RSET, ENTER, C, ENTER.	Computed main area (less code table) checksum is displayed, and a continuously computed checksum is displayed beside original checksum. If there is no error, the checksum is 0.

The process stops if the checksum is ever found to change, or if the user presses CLEAR.

5.2.8.3 ONE-TIME DISPLAY OF SPECIFIED AREA CHECKSUM

Operator Action	Resultant Display
Turn keylock to PGM.	PGM light on.
Press SEL, CTRL, ENTER.	CTRL
Press RSET.	CKSUM FROM
Press AAAA, ENTER.	CKSUM FROM AAAA TO
Press BBBB, ENTER.	CKSUM FROM AAAA TO BBBB - value.

5.2.8.4 CONTINUOUS DISPLAY OF SPECIFIED AREA CHECKSUM

Operator Action	Resultant Display
Turn keylock to PGM.	PGM light on.
Press SEL, CTRL, ENTER.	CTRL light on.
Press RSET.	CKSUM FROM
Press AAAA, ENTER.	CKSUM FROM AAAA TO
Press BBBB, ENTER.	CKSUM FROM AAAA TO BBBB - value. The first-computed checksum is displayed. It should agree with the value in the checksum listing.
C ENTER.	CKSUM FROM AAAA TO BBBB - value - value. The checksum is computed continuously and displayed beside the original.

The process stops if the checksum is ever found to change, or if the user presses CLEAR.

5.2.9 SUMMARY OF DIAGNOSTIC OPERATION

1. Install diagnostic ROM module in place of customer's ROM's.
2. Preliminary Tests.
   a. Initiated by power up of system.
   b. TSC = 01, Preliminary ROM Test.
   c. TSC = 02, Preliminary Processor Run-Halt Test: verification of number of processors.
   d. TSC = 03, Preliminary RAM Diagnostic.
   e. TSC = 04, TP and NP verification.
   f. TSC = 05, Front Panel Diagnostic.
      1. Text displayed @ ABCDEFGHIJKLMNO CLEAR
      2. Text displayed PQRSTUVWXYZ[~]{} CLEAR

3. Text displayed !"#$%&()*+,-./ CLEAR

4. Text displayed 0123456789:;<=>? CLEAR

5. Text displayed 04:SH2:00:04 Keys =
   Press keys in sequence 0 → F ENTER CLEAR

3. Select Test Sequence Code.

In the following, Kn means the nth digit to be displayed or entered.

Display: 0-SH2:00 TSC(1):nn/

Action: K1 K2 ENTER

K1 = Test Group K2 = Test within group

F entered will display as - (dash); it means all tests are to be run.

(FF = all groups, all tests)

4. Select Test Control Code.

Display: K1 K2 :SH2:00 Input TCC:

Action: K3 K4 K5 ENTER

K3 = action taken at end of test

K4 = action on receipt of error

K5 = mode of continued execution after error

Pressing ENTER initiates execution of selected test:

Display: K1 K2 : K3 K4 K5 :00:XX

XX = current test being executed

5. Preemptive Control Mode: entered if transition to diagnostic mode is detected.

Action: a. Turn keylock switch to MON or PGM, press any key.

b. Turn keylock switch to DIAG, press a functional key:

BOOT - Reboot diagnostic system.

CTRL - Terminate current test and return to controller.

STEP - End current test, advance to next test.

HELP - Display current program counter and stack pointer.

MEM - Examine, and optionally change, contents of memory location.

GOTO - Start execution at address entered via the keyboard.

EXAM - Examine, and optionally change, contents of locations in the off-line configuration memory.

DIAG - Examine the error file if in RN5 TCC mode.

SEL - Select the next processor for the panel display.

5.2.10 MAIN DIAGNOSTIC TESTS

Table 5-2 shows the main groups of diagnostic tests used with both S46 and S47, and also S49 software. Tests that do not apply to all are marked † for S46 and S47 only, or * for S49 only.

TABLE 5-2. MAIN DIAGNOSTIC TESTS

1-	RAM Group Diagnostics	Approx. Run Time, sec.	Remarks
11	Random data	18	Per 16K RAM
12	Random address	32	Per 16K RAM
13	Lock byte	5	
14	Base register, base register select, data spaces	4	
15	Base register, base register select, data spaces	4	
*16	Memory refresh	-	
*17	Level queues	12	
*18	Level queues	2	
2-	M6800 Processor Group Diagnostics		
21	Run-hault-reset	2	Per processor
23	Base register, base register select, data spaces	5	Per processor
24	Task dispatches and suspends	10	Per processor
25	Multiprocessor start	3	
*26	Queued task interrupts	28	
*27	Real-time clock	66	
3-	Master Controller Group Diagnostics		
31	Run-halt-reset	3	Per processor
32	Real-time clock	66	Per processor
33	Queued task interrupts	27	Per processor
†34	RPL and RNR instructions	2	
35	Base register, base register select, data spaces, each processor test 14	5	Per processor

* S49 only.
† S46 and S47 only.

TABLE 5-2. MAIN DIAGNOSTIC TESTS (Cont)

3-	Master Controller Group Diagnostics	Approx. Run Time, sec.	Remarks
36	Base register, base register select, data spaces, test 15	4	Per processor
37[1]	ROM and WOM (off-line memory)	2.5	Per option card memory chip
38[1]	Off-line memory - write-protect key	7	Per option card memory chip
4-	Multiprocessor (MP) Group Diagnostics		
41	MP RAM	11	
42	MP Augmented Register	2	
43	MP Base Register	4	
44[1]	MP Off-line memory	3	Per K of memory
45[1]	MP Off-line memory	-	Continuous
5-	Terminal Port Group Diagnostics - Internal Loopback Mode		
51	RSET, then read/write test all TP's singly.	<1	
52	RSET, then read/write test all TP's simultaneously.	2	
53[2]	Single TP interrupt	<1	
54[2]	Multiple TP interrupt	<1	
55	Single TP async function	38	Per TP
56	Multiple TP async function	120	30 seconds per TP
57	Single TP sync function	92	Per TP (Total: 6 min 8 sec.)

[1] Tests 37, 38, and 44 must be requested specifically because the tests may change configuration memory, and test 45 because it will change configuration memory. Selection of all tests in Group 3 or Group 4 will skip over these tests.
[2] See Section 5-3.

TABLE 5-2. MAIN DIAGNOSTIC TESTS (Cont)

6-	Network Port Group Diagnostics - Internal Loopback Mode	Approx. Run Time, sec.		Remarks
			NP1 Strap Speed	
		7200	1800	
61	Single NP R/W	<1		
62	Multiple NP R/W	2		
63[3]	Single NP interrupt	20		Per NP
64[3]	Multiple NP interrupt	5		
65	Single NP XMT/RCV function	12	35	Per NP
66	Multiple NP XMT/RCV function	23	70	Per NP
†67	NP reboot test	-		
7-[4]	Terminal Port Group Diagnostics - External Loopback Mode			
75	Single NP async function	38		Per TP
76	Multiple TP async function	31		Per TP
77	Single TP sync function	12		Per TP
78[5]	Multiple TP sync function at 1200 bps	8		For N ≥10
8-[4]	Terminal Port Group Diagnostics - External Loopback Mode - Operator Selection			
85	Single TP async function	39		Per TP
86	Multiple TP Async Function	120		For all TP's
87	Single TP sync function	12		Per TP
88[5]	Multiple TP sync function	2 min. 26 sec.		For 12 TP's

[3] If the MC1 card is Rev 5 or earlier with a DMCLK rate of 900 bps, Tests 63 and 64 will produce an error message. Move the internal loopback clock from 1800 (U20-1 to U20-20) to 7200 bps (U20-2 to U20-19) for tests 63 and 64 only.
[4] Each test in this series must be specifically selected.
[5] All TP cards must be strapped for an external clock. This test must be specifically selected.

† S46 and S47 only.

5.2.11 ERROR MESSAGES

If an error occurs while testing in the HALT mode, an error message is displayed in the right half of the self-scan in the general format:

E:MMM.N XXXX AA BB

where MMM is the error number

N is the number of the processor that is reporting the error, and

XXXX, AA, and BB are additional digits of error data.

These digits come from three internal processor registers: X, A, and B. Depending on the error, some or all of the digits are displayed as shown below. Note that in the error file display (RN5 mode) that all the digits from the three registers are displayed. The relevant data from the display can be found in Table 5-3.

TABLE 5-3. ERROR MESSAGES

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
E:001.#	A XXXX	Processor number, address of routine calling PNL$(*).	Panel lock byte inconsistency (ignore this message if it occurs after a preemptive function. If persistent, check preliminary tests with BOOT for program checksum, and run tests FF).
E:002.#	A XXXX	Same.	
E:003.#	A XXXX	Same.	
E:040.#	AABB XXXX	Checksum calculated, expected.	Preliminary diagnostic ROM checksum error.
*E:041.#	AA	REQLVL (bits set at level outstanding).	Interrupt requests outstanding at power-up or software restart.
*E:042.#			No software restart.
†E:070.#		Processor number	A processor that should be bolted is running.
*E:071.#	AA BB	Processor control register, processor number.	Processor halt bit not set.

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (Cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
*E:072.#	AA BB	Processor control register, processor number.	Processor GO bit not set.
*E:075.#	AA BB	Processor control register, processor number.	Can't clear interrupt bit.
*E:076.#	AA	RPS value.	RPS enable bit not clear.
*E:077.#	AA	RPS value.	RPS enable bit not clear.
*E:078.#			RPS Enable bit not set after suspending a queued task.
*E:079.#	AA BB	Level expected, actual.	Incorrect level returned from queue with 32 tasks.
*E:080.#	AA BB	DSN expected, actual.	Incorrect DSN returned from queue with tasks.
E:100.#	XXXX AA BB	Address, data expected, actual.	Read-after-write memory error.
*E:101.#			No memory above 8K and location X'1FFF' doesn't respond.
†E:101.#		Processor number.	No memory above 16K and location X'3FFF' doesn't respond.
E:110.#	XXXX AA BB	Address, data expected, actual.	Unexpected interference in memory.
E:130.#	XXXX		Lock byte memory size not a multiple of X'100'. X-reg = address of top of lock byte area.
E:140.#	XXXX AA BB	Address, value before read, value after read.	Lock byte memory cell did not clear after reading.
E:150.#	XXXX AA BB	Address, data expected, actual.	Data space read-write error. Write with BRB mode. If index register < X'20' the read error was in BRB mode. If index register > X'20' the read error was in index mode.

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (Cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
*E:152.#	AA BB	DSN expected, actual.	Incorrect DSN returned by RPS.
*E:153.#	AA BB	Queue block expected, actual.	Incorrect queue block in firmware memory.
*E:154.#	XXXX AA BB	Address expected, actual.	DSN queued in memory is no good.
*E:155.#	XXXX AA BB	Absolute address for data space #2, value expected, actual.	Data error BRB addressing.
*E:156.#	XXXX AA BB	Absolute address for data space #3, value expected, actual.	Data error BRB addressing.
*E:157.#	XXXX AA BB	Absolute address for data space #4, value expected, actual.	Data error BRB addressing.
†E:160.#		BRH:BRL/BRB	Error in converting format from BRH/BRL to BRB.
†E:170.#		Data written/data read.	Error writing BRB register.
†E:180.#		BRH:BRL/BRB.	Error converting from BRB format to BRH-BRL format.
†E:190.#		Address/data written/ data read.	Base register read error.
†E:200.#		Address/data written/ data read.	Base register write error.
E:211.#	BB	Processor number.	Processor did not start when called by UTIL$6.
E:212.#	BB	Processor number.	Processor started which was not mapped by UTIL$3.
*E:213.#	AA BB	Number expected, actual.	Incorrect processor select number in firmware memory.
E:220.#			Q bit not set in fork or suspend.

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (Cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
*E:221.#	AA BB	Level expected, actual.	Incorrect level.
*E:222.#	AA BB	Level bits expected, actual.	Incorrect RPS level.
*E:223.#	AA BB	DSN expected, actual.	Incorrect DSN.
*E:224.#	AA BB	Level expected, actual.	Incorrect level after interrupt.
*E:225.#	AA BB	Level expected, actual.	Incorrect level change.
†E:240.#		Number of ms early.	
*E:241.#	AA	REQLVL value.	RTC task not cleared from REQLVL.
†E:250.#		Number of ms remaining for check.	Real time clock timed out (interrupted) early.
*E:258.#	AA	REQLVL value.	Display can't clear queued tasks from REQLVL.
*E:259.#	AA	REQLVL value.	Suspend. Can't clear queued tasks from REQLVL.
*E:260.#	AA	REQLVL value.	Can't clear queued tasks from REQLVL - UTIL$D.
†E:260.#		Queue level*2/actual pointer/expected pointer.	Real time clock did not time out within expected time window.
*E:261.#	AA	RPS value.	RPS interrupt bit not set.
*E:262.#	AA	RPS value.	RPS interrupt bit not cleared.
*E:263.#	AA BB	Level to be interrupted. highest outstanding level.	No software interrupt.
*E:265.#	AA BB	Level expected, actual.	Incorrect level interrupted - RPS.
*E:268.#			Q bit set on hardware interrupt.
†E:270.#		Queue level*2/actual pointer (should be 28).	WSF error, linked list inconsistent.

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (Cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
*E:274.#	AABB XXXX	Initial RTC count, RTC count at error time.	No real time clock interrupt.
+E:280.#		Queue level*2/actual DR$/expected DR$.	WSF error, rear queue pointer inconsistent.
†E:290.#		Queue level*2/actual (data space pointer) DR$/expected DR$.	RSF error (de-queuing). A nonempty queue was found to be empty.
			RSF error, wrong data space dequeued.
E:294.#	AA	RPS value.	Interrupt bit not set - RPS.
E:295.#	AA	ENQ$ IO$DR.	Incorrect interrupt level - ENQ.
E:300.#			Processor control instruction did not restart system.
E:301.#			Processor # 0 did not restart.
†E:306.#		Queue level*2/actual DR$/expected DR$.	RSF error: hardware request serviced before the hardware request, or hardware request not serviced after a software request.
E:310.#			Operator presses a key but level 1 interrupt not received within 10 seconds.
*E:311.#	AA	IO$DR (ENQ).	Incorrect level response to key interrupt.
*E:312.#	AA	Status byte.	Key flag not set in status byte.
*E:313.#			Interrupts enabled after key interrupt.
†E:320.#		Actual DR$/expected DR$.	RPL error, unexpected DR$ level returned.
†E:330.#		Actual AR$/expected DR$.	RNR error, unexpected DR$ level returned in servicing a software request.

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (Cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
†E:340.#		Actual DR$/expected DR$.	RNR error, wrong data space dequeued.
†E:350.#		Actual RD$/expected DR$.	RPL error, RTC hardware request not recognized after RNR software request.
†E:360.#		Level*2/actual data/ expected data.	RNR error, wrong data space dequeued from free level queue.
†E:370.#		Level*2/actualdata/ expected data.	RNR error, wrong data dequeued from free-level queue.
E:381.#	XXXX AA BB	RAM address, value expected, actual.	Cannot copy AROM data into RAM. RAM read-write error.
E:382.#	XXXX AA	AROM address, actual value, expected value.	First byte of AROM memory not at beginning of a segment.
E:383.#	XXXX AA	AROM address, actual value read (expected 0).	First byte of an AROM memory segment found not at beginning of a segment.
E:384.#	XXXX AA	AROM address, actual value read (expected 0).	Byte in an AROM segment did not read back.
E:385.#	XXXX AA BB	AROM address, value expected, actual.	Byte no properly reloaded into AROM OK.
E:386.#	XXXX AA BB	Test #37: Write-protect key failure. Test #38: AROM write-read failure. Test #44: AROM write-read failure.	AROM write-read error.
E:387.#	XXXX AA BB	Address, expected, actual.	AROM high-speed read error.
E:390.#	AA	Processor number.	Multiprocessor test time out.
E:400.#			No terminal port found by the I/O map routine (UTIL$M).
*E:401.#	XX	Port address.	No port response to TPRT$.
*E:402.#			No tasks present.

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (Cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
*E:403.#			No task returned by ENQ after an interrupt.
*E:404.#			A queued task interrupted.
*E:405.#			No tasks in REQLVL at interrupt to module HDI.
E:420	XX AA B		TP register not clear after a master I/O reset. X-Reg = TP address. A-Reg = contents of TP register. B-Reg = register number. (0_RSTD$, 1_RDT1$).
E:430.#	XX AA BB	TP number, data written, read.	Read-after-write check error on TP register #1.
E:431.#	XX AA BB	TP number, data written, read.	Read-after-write check error on TP register #2.
E:440.#	XX AA BB	TP number, data expected, actual.	TP register 1 interference error.
†E:450.#			
†E:460.#			
†E:470.#		- - -	TP interrupt service cycle error, AR$ incorrect after an RNR.
†E:490.#		TP address/actual SR$/ expected SR$.	TP status register incorrect.
*E:500.#	XX AA BB	TP address, DR$, SR$ (ENQ$).	Invalid TP address interrupted.
†E:500.#		AR$/DR$/SR$.	Spurious interrupt at TP interrupt level - no TP response to RNR.
E:520.#	XX AA	TP number, status register.	Unexpected data set change receiver interrupt (TP status bit 7) or incorrect status register after carrier loss.

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (Cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
E:530.#	XX AA	TP number, status register.	Error flag set in terminal port status register.
E:540.#	XX AA BB	TP number, character expected, actual.	Character received in error, but no error flag set in TP status register.
E:550.#	XX A	TP number, counter state. State: 0 — XMT counter =0, RCV counter =0 1 — XMT counter =0, RCV counter >0 2 — XMT counter >0, RCV counter >0	Terminal port diagnostic test time out.
E:560.#	XX AA BB	AR$, DR$, SR$ for ENQ instruction.	Interrupt not at TP level.
*E:561.#	XXXX AA BB (see note)	Interrupt number/TP address DR$ expected, actual (ENQ$). Interrupt number = 10 - carrier detect 20 - XMT hold register empty 30 - carrier loss	Interrupt not at TP level-Test 53, 54.
*E:562.#	XXXX AA	Correct TP address, TP address returned in AR$. Interrupt number = 10 - carrier detect 20 - XMT hold register empty 30 - carrier loss	Wrong TP address interrupted - Test 53, 54.
*E:563.#	XXXX AA BB	TP address, status expected, actual. Interrupt number = 10 - carrier detect 20 - XMT hold register empty 30 - carrier loss	Unexpected TP status register contents.

Note: First XX = interrupt number
Second XX = TP address

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (Cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
*E:564.#	XXXX (see note)	Interrupt number/TP address. Interrupt number = 10 - carrier detect 20 - XMT hold register empty 30 - carrier loss	Terminal port interrupt failed to occur - Test 53, 54.
E:570.#	AA BB	Last TP found, RTN from FIND_PREV_TP.	TP search problem.
*E:600.#			No network ports found by the I/O map routine (UTIL$M).
*E:601.#	AA	First port address + 2.	NP port not in slot 0 MOD4.
E:620.#	XX AA B	NP address, status register, register number. Reg. No. — Expected Reg. Value 0 — X'10' 2 — X'04' 6 — X'80'	NP status register not initialized correctly after a master I/O reset.
E:640.#	XX AA BB	NP address, data expected, actual. NOTE Data bits 7,6 correspond to bits 7,6 in NPCC (NP register). Data bits 5,4 correspond to bits 6,5 in NPCI (NP register). Data bit 2 corresponds to bit 5 in NPCO (NP register).	Network port status/control registers read-after-write error.
E:650.#	XX AA BB	NP address, data expected, actual.	Network port register interference found (test work format same as ER$640).

Note: First XX = interrupt number
Second XX = TP address

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (Cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
E:660.#	XX	NP address.	Network port XMT interrupt failed to occur when expected (TXRQEN=1 &TXRQ=1).
E:661.#	AA	Status out.	NP status out: XMT ready-to-receive-new-data bit not set (bit 7).
E:670.#	XX AA BB	NP address, DR$ expected, actual.	Unexpected DR$ after ENQ$ with an interrupting network port (XMT).
E:680.#	XX AA	NP address expected, actual.	AR$ incorrect after an ENQ$ with an interrupting network port (XMT).
E:690.#	XX AA BB	NP address, expected NPSO$, actual IO$SR.	Unexpected SR$ after an ENQ$ with an interrupting network port (XMT).
E:700.#	XX AA BB	NP address NPSO$ expected, actual.	Unexpected NPSO$ after an XMT network port interrupt.
†E:701.#		Flag type/number of flags received.	No NP reboot - time-out error. NOTE: Flag type = 3, 7, F, 1F, ..., FF correspond to flags of 9, 10, 11, ..., 15 1's.
†E:702.#		Port address/DR$/SR$.	NP transmit instead of receive interrupt.
†E:703.#		Port address/DR$/SR$.	No NP reboot after receiving 9 flags.
†E:704.#		Flag type/number of flags received.	NP reboot, but after time out.
†E:705.#		Flag type/number of flags received.	NP reboot on incorrect number of flags received.
†E:706.#			NP interrupt caused by incorrect flag sequence.
†E:707.#		Port address/DR$/SR$.	NP flag interrupt with flag detected bit not set.

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (Cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
*E:710.#	XX	NP address.	Network port RCV interrupt occurred instead of XMT interrupt.
†E:710.#		NP address.	NP receive interrupt failed to occur.
E:711.#	AA BB	NP address, status in.	NP status in: data ready-to-be-read bit not set (bit 7).
E:720.#	XX AA BB	NP address DR$ expected, actual.	Incorrect DR$ after ENQ$ with an interrupting network port (RCV).
E:730.#	XX AA	NP address AR$ expected, actual.	Incorrect AR$ after an ENQ$ with an interrupting network port (RCV).
E:740.#	XX AA BB	NP address, NPSI$ expected, IO$SR actual.	Incorrect SR$ after an ENQ$ with an interrupting network port (RCV).
E:750.#	XX AA BB	NP address NPSI$ expected, actual.	Incorrect NPSI$ after an RCV network port interrupt.
E:760.#	XX AA BB	AR$, DR$, SR$.	Spurious interrupt at a network port request level.
E:761.#	XX AA BB	AR$-responding address, DR$, SR$. If SR$ even = receive. If SR$ odd = transmit.	Port with wrong address responded.
E:770.#	XX AA	NP address, SR$.	Unexpected XMT interrupt, XMT sequence should be complete.
E:780.#	XX AA	NP address, SR$.	Unexpected RCV interrupt, RCV sequence should be complete.
E:785.#	XX AA BB	NP address, data expected, actual.	NP RCV data error.
E:790.#	XX AA	NP address, SR$ after ECC shifted in from FIFO.	Network port receiver ECC checkerror.

* S49 only.
† S46 and S47 only.

TABLE 5-3. ERROR MESSAGES (cont)

Display		Data Identification	Probable Cause of Error
Error Number	Error Data		
E:800.#	XX	NP address.	Network prot diagnostic test time out.
E:940.#			No active I/O ports could be found in system.
E:950.#			Self-halted processor unexpectedly restarted (run flag turned on).
E:960.#	XXXX	Address where SWI was executed.	Unexpected SWI interrupt.
E:970.#	XX AA BB	Address, Q level, status.	Unexpected hardware interrupt.
†E:975.#		Port address/DR$/SR$.	IRQ interrupt received with no valid request pending.
E:976.#			No free data space.
E:980.#	AA	Key code.	Undefined NMI interrupt.
E:990.#			Spurious reset given to processor.

* S49 only.
† S46 and S47 only.

5.2.12 TEST OPERATION INSTRUCTIONS

5.2.12.1 OFF-LINE MEMORY DIAGNOSTIC (TSC = 37). The test can be called only by specifying TSC = 37. This test only allows Test Control Codes (TCC) of SH0, SH1, SN0, or SN1.

This test first stores the current contents of AROM in RAM. If the test is successfully completed, the original contents of AROM are restored. If there is any error, the original contents should be considered as lost.

The test counts the number of memory segments (blocks of 256 bytes) which respond normally, and asks the operator to verify the number (in hex) of memory chips on the option board. (The number of chips is twice the number of segments.) If the number is correct, press ENTER; otherwise terminate the test.

If the number of chips is incorrect, the chips which responded correctly can be determined by reading a table beginning at location X'1000'. (See Table 5-4.)

TABLE 5-4. AROM MEMORY SEGMENT ADDRESSES

RAM Location	Description
X'1000'	Location of the address of the last segment in the table.
X'1002'	Beginning address of segment 1.
X'1004'	Beginning address of segment 2.
.	
.	
.	
X'1000 + 2*n'	

The memory test writes to all of memory and then reads from all of memory each of the data patterns described in Table 5-5.

This sequence is repeated several times per processor. The number of repeats is less if there are more processors, so the running time of the test is independent of the number of processors.

If memory fails in this part of the test, the error number is 386; check that the write-protect switch is in the write position. If the error is not a switch

TABLE 5-5. MEMORY TEST SEQUENCES

Pattern	Sequence Pointer
Constant 0's	X'00'
Constant X'FF'	X'03'
Constant 0	X'06'
Cycle 1 to left	X'09'
Cycle X'7F' to right	X'0B'
Slide X'FF' to right	X'0F'
Cycle X'AA' to left	X'12'
Cycle X'5A' to left	X'15'
Random Sequence	X'18'

error, read the data with the preemptive MEM function called for in the error data sheet for error 386, memory test 37 (Figure 5-2). The sequence pointer specifies which data sequence was being written and read. (See Table 5-5.)

To continue the test in looping or nonlooping mode, press CLEAR, then press CLEAR again, and then press ENTER.

In looping mode, the test rewrites and rereads the same data pattern for all of memory. During the read-verify sequence, the complement of what was read is written back to each location. In this way intermittent write errors during looping will be found.

The write-protect switch can be tested by throwing the switch to the protect position while the main memory test is running. Error 386 should occur.

5.2.12.2 OFF-LINE MEMORY WRITE-PROTECT KEY DIAGNOSTIC (TSC = 38). The test can be called only by specifying TSC = 38. This test only allows Test Control Codes (TCC) of SH0, SH1, SN0, or SN1.

This test first stores the current contents of AROM in RAM. If the test is successfully completed, the original contents of AROM are restored. If there is any error, the original contents should be considered as lost.

The test counts the number of memory segments (blocks of 256 bytes) which respond normally, and asks the operator to verify the number (in hex) of memory chips on the option board. (The number of chips is twice the number of segments.) If the number is correct, press ENTER; otherwise terminate the test.

ERROR DATA SHEET FIRMWARE DIAGNOSTICS - REV. 12

ERROR #386

TEST #37 - OFF-LINE MEMORY

FAILED PROCESSOR #_____ AROM ADDR EXPECTED ACTUAL
ERROR MESSAGE DATA: X = _____ A = _____ B = _____

PROCESSOR DATA:

Ø		1		2		3		4		5		6		7		
3FB		3A4		34B		2F2		299		240		1E7		18E		} COUNT
3FC		3A5		34C		2F3		29A		241		1E8		18F		}
3FD		3A6		34D		2F4		29B		242		1E9		190		SEQ PTR

Figure 5-2. Data Sheet - TSC = 37, ERROR = 386

The test next tests the write-protect key and the write-protect control register (27) for processor 00. Data is written to memory for every value except the correct key value in memory location 27. If the memory write is successful, error message 386 is displayed.

Error looping (SH1 or SN1) for this error attempts to rewrite and check the entire memory with the current key value in memory location 27. The loop will continue until interrupted by the operator.

5.2.12.3 MULTIPROCESSOR OFF-LINE MEMORY DIAGNOSTIC (TSC = 44). The test can be called only by specifying TSC = 44. This test only allows Test Control Codes (TCC) SH0, SH1, SN0, or SN1.

The test initially stores the current contents of AROM in RAM. If the test is successfully completed, the original contents of AROM are restored. If there is any error, the original contents should be considered lost.

Next, the test establishes which memory segments (blocks of 256 bytes) respond normally, and creates a table beginning at location X'1000'. If there are inexplicable problems, this table should be checked. (See Table 5-2.)

During the main part of the test, each processor writes and reads, segment by segment, the data patterns described in Table 5-3. All of memory is scanned with each pattern. Then the next pattern is used, etc. Contention for memory segments is controlled by lock bytes which begin at location X'404'. Program activity is indicated by an incrementing level count and incrementing digits in the first position of the screen. During error looping the digits increment but the level lights do not.

Error 386 is a write-read error. For the SH0 mode, all processors except the failed processor are halted within 38 instructions of the detection of the error; and the test cannot be continued. For the modes SH1, SN0, and SN1, the processors are not halted. After error data collection for mode SH1, the test may be continued by pressing CLEAR, then pressing CLEAR again, and then pressing ENTER.

Error data collection for error 386 is indicated on the error data sheet for error 386, test 44 (Figure 5-3). Collect the data for the processor which failed. Then if in SH1 mode, press CLEAR, then press CLEAR again, and then press ENTER. The message ERROR LOOPING should appear. If in SH0 mode, select the next processor for the panel by executing the SEL preemptive mode. Then go into the MEM preemptive mode and collect the data for that processor. Repeat for all processors.

The error data shows which patterns were tested in which segments when the error occurred. The sequence pointer refers to Table 5-3 and indicates the pattern. The AROM pointer is the last address being tested. The other data should be consistent; the lock bytes should be X'404' plus the segment number; the table segment pointer should be between X'1002', and the value at location X'1000', etc. If this data is not consistent, then the error is not an AROM problem.

For error looping, a flag is set which sets all processors to looping with write-reads in the segments which were being tested when the error was detected. During the read sequence the complement of the value read is written back to each location. In this way intermittent write errors during looping will be found. The loops will continue until interrupted by the operator.

5.2.12.4 MULTIPROCESSOR OFF-LINE MEMORY DIAGNOSTIC (TSC = 45). This test is similar to test 44 except that it does not terminate. The original contents of the off-line memory are lost.

5.2.12.5 SINGLE-TP, INTERNAL-LOOPBACK, ASYNCHRONOUS DIAGNOSTIC (TSC = 55). This test exercises each TP asynchronously in internal loopback mode for the rates shown in Table 5-6 below and for character lengths 5 through 8.

TABLE 5-6. ASYNCHRONOUS RATE NUMBERS AND SPEEDS

Rate Number	Rate, bps	Rate Number	Rate, bps
1	1200	5	300
2	110	6	150
3	134.5	7	75
4	600		

The TP being tested is displayed in the right half of the self-scan.

If there is an error and the current test rate and character lengths are needed, use the MEM preemptive function to examine the following locations in memory:

ERROR DATA SHEET FIRMWARE DIAGNOSTICS - REV. 12

ERROR #386 Date_____ Time_____

TEST #44 - MULTIPROCESSOR OFF-LINE MEMORY Machine Operator_____

FAILED PROCESSOR #_____ AROM ADDR EXPECTED ACTUAL
ERROR MESSAGE DATA: X = _____ A = _____ B = _____

PROCESSOR DATA: (MODE SH0 - Collect data for all processors. To go to next processor, use the SEL preemptive function. MODE SH1 - Collect data for processors which failed. Begin looping by pressing CLEAR, pressing CLEAR, pressing ENTER. The message ERROR LOOPING should appear.

	0		1		2		3		4		5		6		7		
	28		28		28		28		28		28		28		28		AROM PTR
	29		29		29		29		29		29		29		29		
	2A		2A		2A		2A		2A		2A		2A		2A		LOCK BYTE
	2B		2B		2B		2B		2B		2B		2B		2B		
	2C		2C		2C		2C		2C		2C		2C		2C		TABLE SEG PTR
	2D		2D		2D		2D		2D		2D		2D		2D		
	2E		2E		2E		2E		2E		2E		2E		2E		SEQ ENTRY PTR
	2F		2F		2F		2F		2F		2F		2F		2F		
ONLY FOR PROCESSOR WHICH FAILED	3EE		397		33E		2E5		28C		233		1DA		181		SEQ ENTRY PTR
	3EF		398		33F		2E6		28D		234		1DB		182		
	3F0		399		340		2E7		28E		235		1DC		183		TABLE SEG PTR
	3F1		39A		341		2E8		28F		236		1DD		184		
	3F2		39B		342		2E9		290		237		1DE		185		MEM LOCK BYTE
	3F3		39C		343		2EA		291		238		1DF		186		
	3F4		39D		344		2EB		292		239		1E0		187		AROM PTR
	3F5		39E		345		2EC		293		23A		1E1		188		
	3FA		3A3		34A		2F1		298		23F		1E6		18D		SEG 1ST NO.
	3FB		3A4		34B		2F2		299		240		1E7		18E		COUNT
	3FC		3A5		34C		2F3		29A		241		1E8		18F		
	3FD		3A6		34D		2F4		29B		242		1E9		190		SEQ PTR
	3FE																
	3FF																

Figure 5-3. Data Sheet - TSC = 44, ERROR = 386

Memory Location	Memory Contents
3FC	Rate number 1⟶7
3FD	Character length: 0 = length 8
	40 = length 7
	80 = length 6
	C0 = length 5

5.2.12.6 MULTIPLE-TP, INTERNAL-LOOPBACK ASYNCHRONOUS DIAGNOSTIC (TSC = 56). This test exercises a multiple number of TP's simultaneously in internal loopback mode. The test verifies the ability of the system to handle a moderate total data rate. The maximum number of TP's tested at one time depends on the rate being tested, and is determined automatically by the test program from Table 5-7 below.

TABLE 5-7. THE MAXIMUM NUMBER OF TP's TESTED FOR EACH ASYNCHRONOUS RATE

Rate Number	Rate, bps	Maximum Number of TP's in Test Subset	Maximum Total Data Rate, bps
1	1200	12	28,800
2	110	130	28,600
3	134.5	107	28,783
4	600	24	28,000
5	300	48	28,000
6	150	96	28,000
7	75	192	28,000

The maximum number of TP's tested can be changed by doing a preemptive BOOT command and answering YES (press the CLEAR key) to the question "SPECIAL SPEEDS?". Then when test 56 (or tests 58, 76, 78, 86, 88) is initiated the operator will be asked to enter new maximum of TP's for rates 0-7. (Rate 0 is used for synchronous tests 58, 78, and 88.) Once these questions have been answered they will not be asked again until test control has been returned to the operator and one of the tests 56, 58, 76, 78, or 88 is initiated. To terminate this prompting and return to the numbers used in Table 5-8 do a preemptive BOOT and answer NO (press the ENTER key) to the question "SPECIAL SPEEDS?".

The subsets of TP's to be tested are chosen automatically and are displayed in the form:

TP = [W,X],[Y,Z]

This means that all TP's W through X, inclusive, and Y through Z inclusive, are being tested. Initially the TP's within the first bracket are at the lowest addresses and the TP's within the second bracket are at the highest addresses. After one data cycle the numbers W and X increment to the next TP address and the numbers Y and Z decrement to the next TP address. When X and Y represent adjacent TP's testing begins with another data sequence and the initial subset. After seven data sequences have been tested the next rate is tested in the above manner. Only 8-bit characters are tested.

In the event of an error, if the rate is needed, use the preemptive MEM function to examine location 3FC which contains the rate number.

5.2.12.7 SINGLE-TP, INTERNAL-LOOPBACK, SYNCHRONOUS DIAGNOSTIC (TSC = 57). This test is functionally the same as test 55 except that the TP's are in synchronous mode. There is a delay in this test so the running time is longer than for test 55. (See Table 5-2.)

5.2.12.8 TP EXTERNAL-LOOPBACK DIAGNOSTIC (TSC = 75 THROUGH 78). Tests 75-77 are the same as tests 55-57 except that the TP's are in external loopback mode and hence require loopback plugs such as illustrated in Figure 5-4. One further exception is that test 77 tests only rate 1. Test 78 tests subsets of TP's in synchronous mode at rate 0 (the 1x external clock) so all TP's must be strapped according to Figure 5-5.

The maximum number of TP's in a subset is computed automatically from Table 5-8. To change these maximum numbers, answer YES to the question "SPECIAL SPEEDS?" in the BOOT sequence (see Section 5.2.10.6 for details).

5.2.12.9 TP EXTERNAL LOOPBACK, OPERATOR-SELECT DIAGNOSTIC (TSC = 85 THROUGH 88). These tests are the same as tests 75-78, except that only TP's which the operator selects via the operator's console are tested.

At the beginning of any test 85-88 the display prompts for a TP address entry with the display, TP =. Enter a TP address and press ENTER. If the address entered

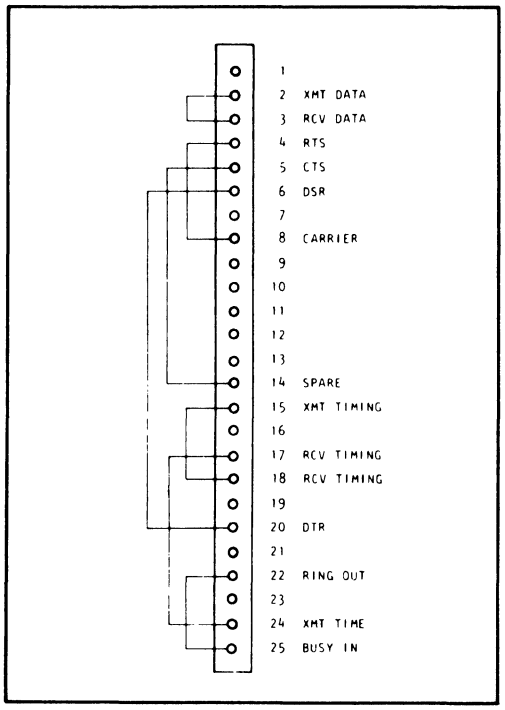


Figure 5-4. External Loopback Plug Connections for Diagnostic Tests 75-78, 85-88

TABLE 5-8. THE MAXIMUM NUMBER OF TP's TESTED AT RATE 0 AS A FUNCTION OF THE NUMBER OF PROCESSORS

Number of Processors	Maximum Number of TP's in Test Subset
1	4
2	8
3 or more	10

To test a few TP's for simultaneous synchronous operation it may be easier to use test 88

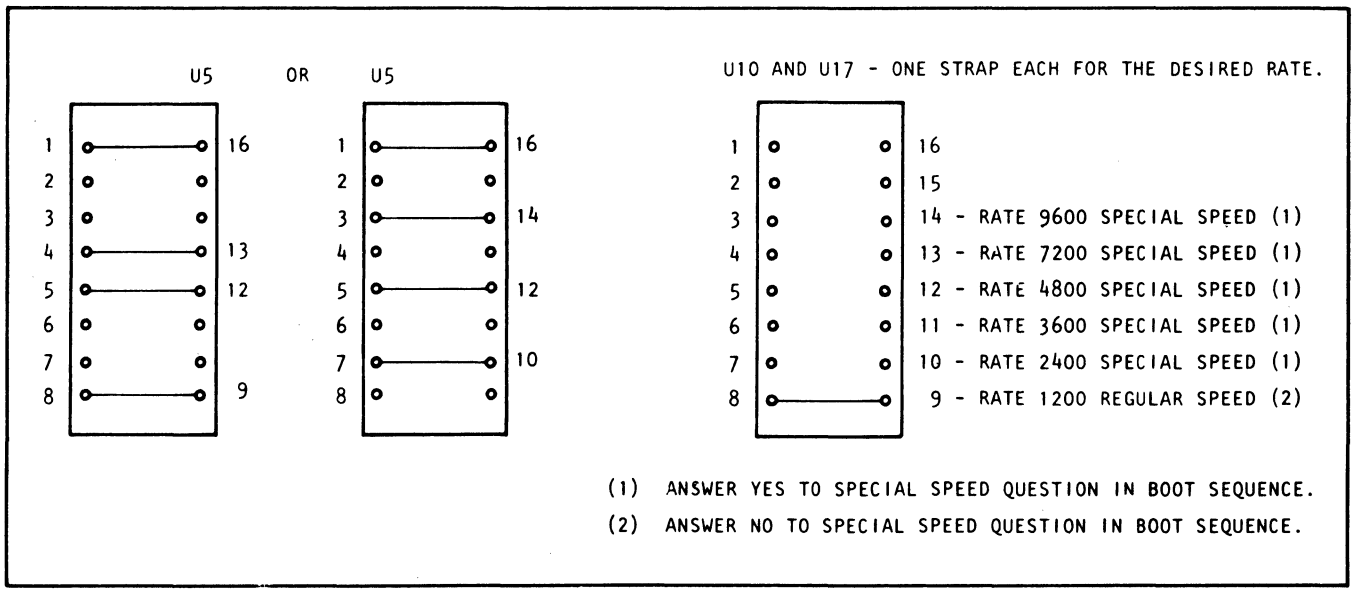


Figure 5-5. TP Strapping For Synchronous Tests 78 and 88

is valid, the data is stored and the display asks for another TP. To terminate this input sequence enter CLEAR and the test will begin. If an entered address is incorrect an error message !!ERROR!! is displayed, the data is rejected, and another TP request is made.

5.3 ISOLATING PORT AND NEST PROBLEMS

If port or port nest problems are suspected, first ascertain that the correct number of NP's and TP's respond: Do a BOOT or power-up and verify this in the preliminary tests. Then run the diagnostics with test sequence codes (TSC) of 5F and a test control code (TCC) of RHO (R = at the end, restart the test sequence. H = halt on error, GO resumes operation. 0 = continue with test).

If the tests cycle through once, the port nest(s) are probably operating correctly.

Next do more exhaustive testing by testing all the TP's, or selected TP's, with external loopback plugs, (Figure 5-4) and tests in the 7F or 8F series. Unless all TP's are strapped for synchronous (1X) clock, the synchronous TP's must be tested individually with tests 87 and/or 88.

Most problems will show up as errors when running tests 51 through 54. If an error is detected, execute only the failing test while swapping cards, then retest with TSC of 5F.

If tests 51 and 52 run successfully but 53 or 54 fails, the problem is probably the interrupt acknowledge logic.

NOTE

> The error message will display a port address that is probably NOT the port with the problem. The failing port is usually one or two ports to the left (lower port address) than that indicated by the diagnostic.

The quickest way to isolate a port which fails tests 51-54 is to run the failing test with a TCC = RNO. Executing the diagnostics in this manner will cause the error counter on the self-scan to increment when an error is encountered. When the failing card is removed, the error counter will stop counting. One way to run these tests is

to loosen all port cards, then plug them in one at a time (there may be a short burst of errors when each card is first plugged in, but then the count should stop).

5.4 MC1 AND MC2 PROBLEMS

If any test in 3F series fails, suspect a bad MC1 or MC2; however, if 37 fails suspect a bad option card.

If tests 41 or 42 fail, suspect a bad MC1 or MC2.

If test 44 fails, suspect a bad ROM or WOM.

5.5 LOCATING A FAILED RAM CHIP

The location of a failed RAM chip can be pinpointed by running the diagnostic TSC = IF, TCC = RHO, and reading the error message. The format of the message is

AAAA EE RR

where AAAA = address where the error occurred
EE = expected data or written data
RR = data read

As an example, take the error message

0137 AC AB

If there is one RAM in the mainframe (2-way interleaved), the last character of the address shows the row in which the bad chip resides (Figure 5-6). Since the last digit of the address is 7, the bad chip is in the third row (as it would be if the last digit were 3, B, or F). To determine which chip in the third row is bad, read the hex values for data expected/data read, and convert the hex to binary:

Expected		Read	
A	C	A	B
1010	1100	1010	1000

MSB — FAULT — LSB

It is evident that the difference lies in data bit 2 of data bits 0-7.

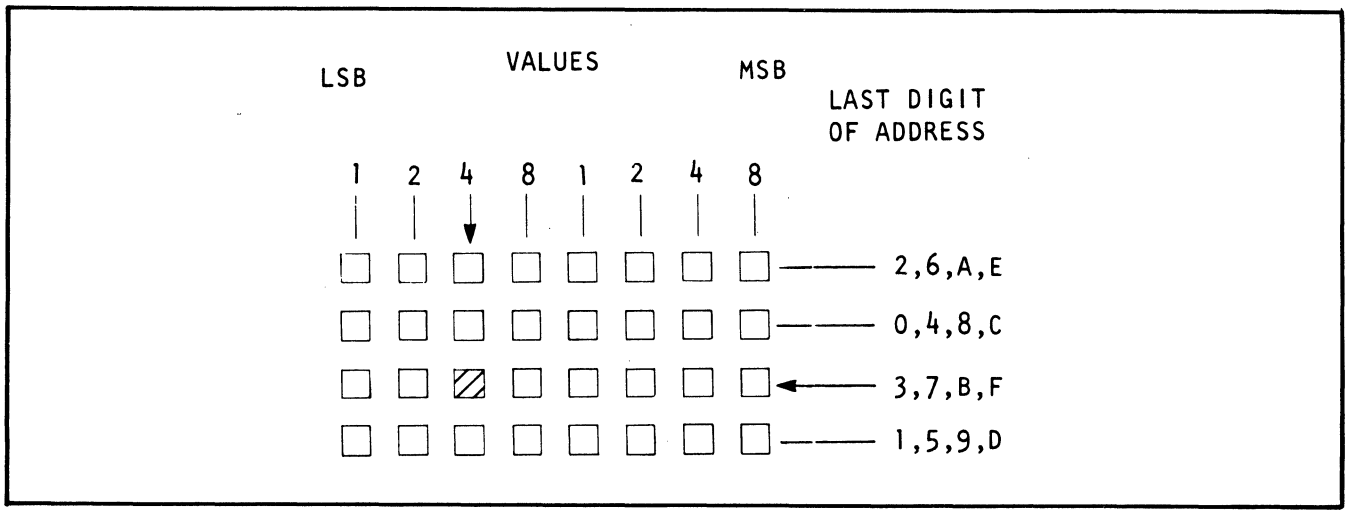


Figure 5-6. RAM Chip Layout

Now refer to the chip side of the RAM card or to the chip layout shown above. The chip that holds the least significant bit (0) is on the left, with the MSB (7) on the right. (This is the reverse of the way the numbers are written normally.) Therefore, the failed chip is the third from the left in row 3, and should be replaced.

5.6 WHEN THE INP WILL NOT START

A problem arises when it is not possible to get the INP running with one RAM in place. This happens because the diagnostics use the lower 2K of memory to start up.

If two known good RAMs are available, it will be possible to pinpoint the failed chip as in 5.5. Install both good RAMs in place, with the suspect RAM in the next slot to the left of them. The diagnostics will indicate memory from 0000 to BFFF, and the bad chip will be in the range 8000 to BFFF. This will afford a two-way interleave and allow using the single RAM method of locating the failed chip.

If only one known good RAM is available, pair it with the suspect RAM. (This will make a four-way interleave memory.) Pairing RAMs in this fashion allows narrowing the search to two chips, which can be replaced one at a time to locate the faulty chip. Figure 5-7 below shows the addressing scheme. The pair of RAMs will cover an address range from 0000 to 7FFF (32K).

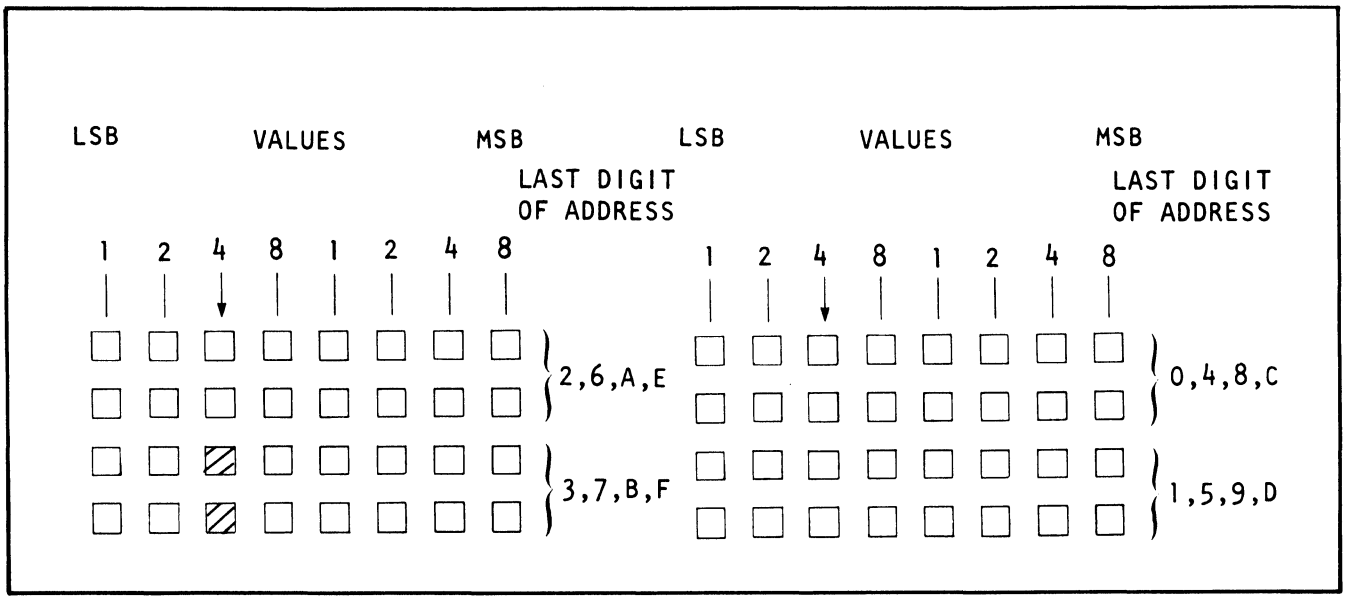


Figure 5-7. Chip Layout for Paired RAM's

5.7 USE OF BREAKOUT BOX TO CHECK TP DRIVERS

5.7.1 STANDARD (DUAL UNIVERSAL) TERMINAL PORT

A dual universal terminal port has two transmitter drivers (U1 and U7 or U13 and U19) and two receiver drivers (U2 and U6 or U14 and U18) that are not checked by the Rev 11 or Rev 12 diagnostics unless tests are run to external loop (TSC = 75 through 78). It is possible to check whether these drivers are on or off by use of the EXAM M function on the TP. The function is monitored by an attached breakout panel. Comparison of the EXAM M for a port with the status observed on the breakout panel can show which EM driver is defective. Figure 5-8 shows the pins and signals for each dip in each channel. Loss of an EIA signal indicates failure of the associated dip, and need for dip replacement.

5.7.2 ACTIVITY INDICATOR TERMINAL PORT

Rev 11 and Rev 12 diagnostics do not check the two transmitter or two receiver drivers of the activity indicator terminal port unless tests are run to external loop. Again, the breakout box can be used to check the signals, as in Section 5.7.1. Figure 5-9 shows the pins and signals for each dip in each channel.

5.8 USE OF BREAKOUT BOX TO CHECK CONTROL SIGNALS

It is possible to identify and isolate the specific chip causing a failure in a TP module by using a breakout box.

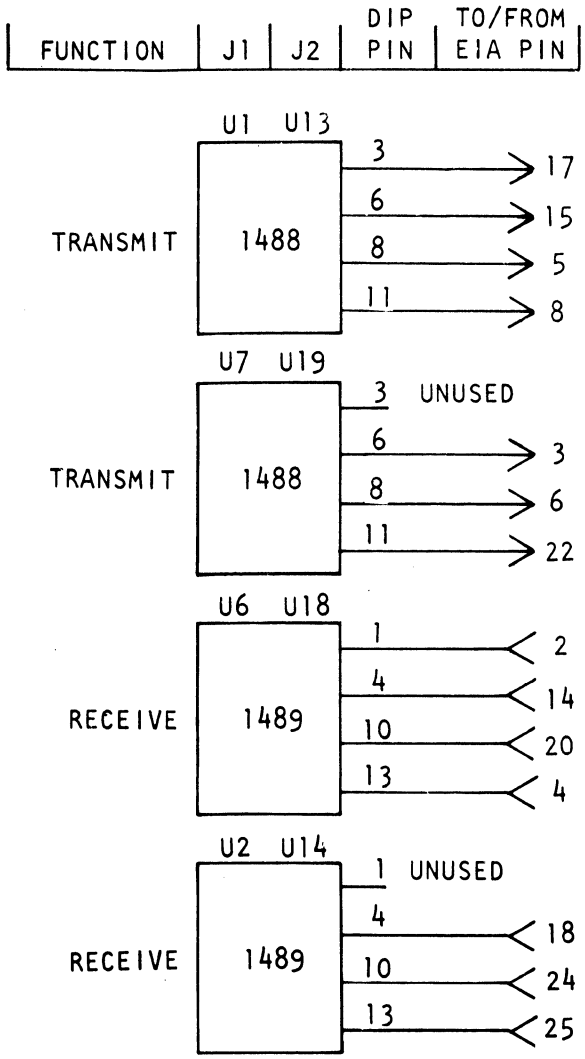


Figure 5-8. Signals on Standard TP Drivers

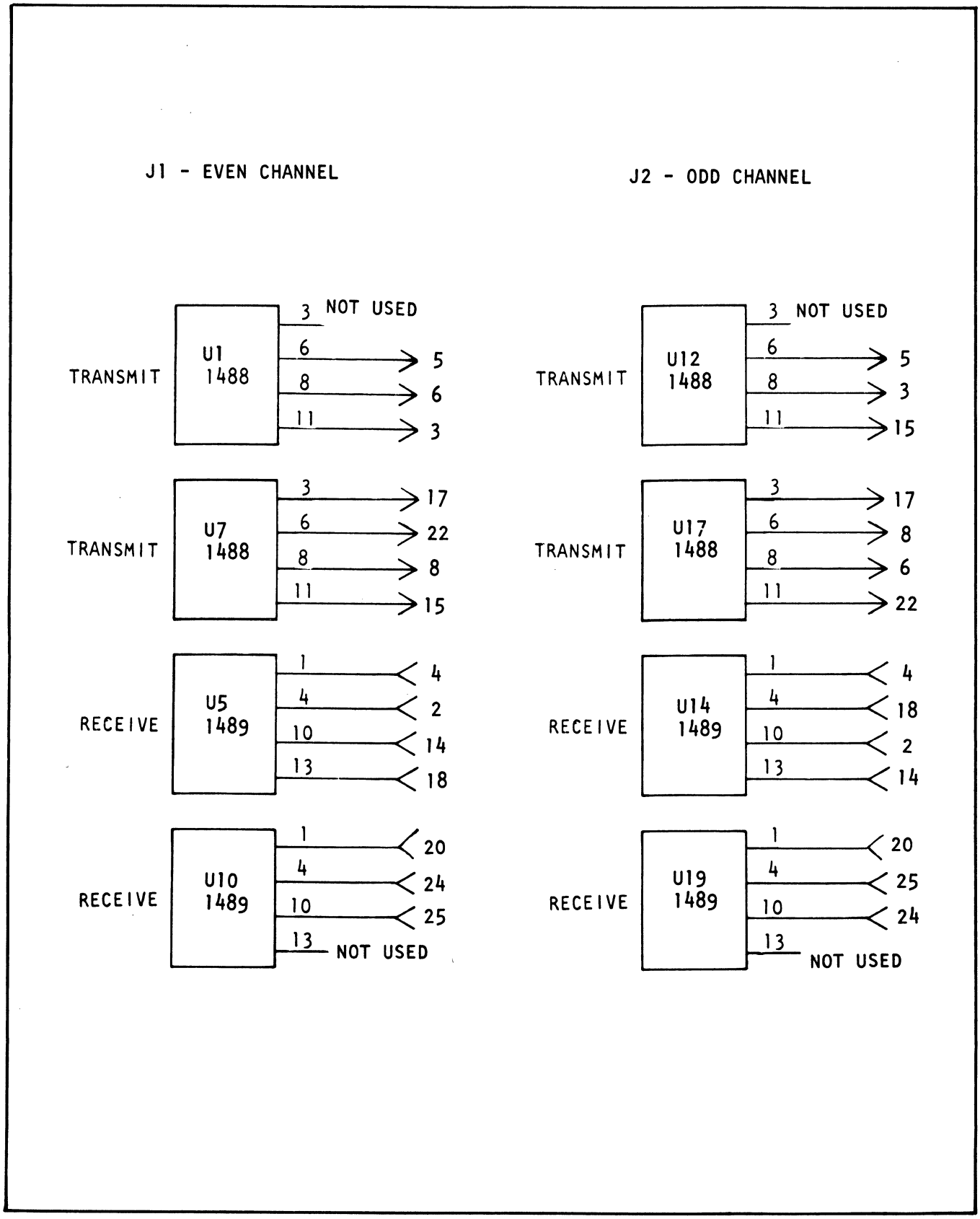


Figure 5-9. Signals on Activity Indicator Port Drivers

A breakout box is a pocket-sized item of test equipment used to check out timing and control signals and verify + or -3V potential on an EIA interface.

It consists of the following, connected in series, (Figure 5-10): a 25-pin EIA female connector, an array of 24 test-point pins and 24 rocker switches (pin 1, chassis ground - AA, has no pin or switch), 25 pins used for cross-patching with jumpers, and 14 LED indicator lamps. Two of these lamps are located below the row of switches and indicate positive or negative voltage levels in excess of 3V. These may be patched to monitor any line. The connection terminate on the right with an EIA male connector at the end of a short ribbon cable. The LED's are powered by two pen light batteries mounted in the cover of the box. The box is 3.75 in. W x 5 in. H x 1.75 in. D. The figure shows an International Data Sciences, Inc. Model 60 Breakout Panel.

Figure 5-11 shows four uses for the box. It can be connected between an NP and its high-speed modem, between a TP and a terminal, between a TP and an external loopback plug, or between a terminal and the high-speed modem.

5.9 ISOLATING TERMINAL PORT "BX" ERRORS

The term 'BX error' is used to describe any of the events leading to an overflow of the buffer attached to the output side of a terminal port. BX errors are caused by any of the several sequences of events listed in Table - . There are normal and abnormal BX errors. Once there is a distinction between them, the causes of abnormal errors can be isolated.

The main cause of severe, recurrent BX errors is a bad 7403 IC in the interrupt acknowledge logic of a terminal port, socket U22. The terminal port containing the failed 7403 will have a lower address than the port or ports getting the BX errors. The interrupt acknowledge propagates from card to card through the ASTRO's, through logic which detects an empty slot in the next card position and through logic which separates acknowledges for the terminal ports from acknowledges for the network ports. The 7403's are part of the circuit which bypasses the next slot if it is empty. 7403's which have failed will erroneously detect an empty slot and send a spurious acknowledge to the second following terminal port card or they will continuously send an acknowledgement signal to downstream ports.

The odd thing about BX errors which are caused by solidly failed 7403's is that they do not occur continuously. The exact pattern is complex and not fully

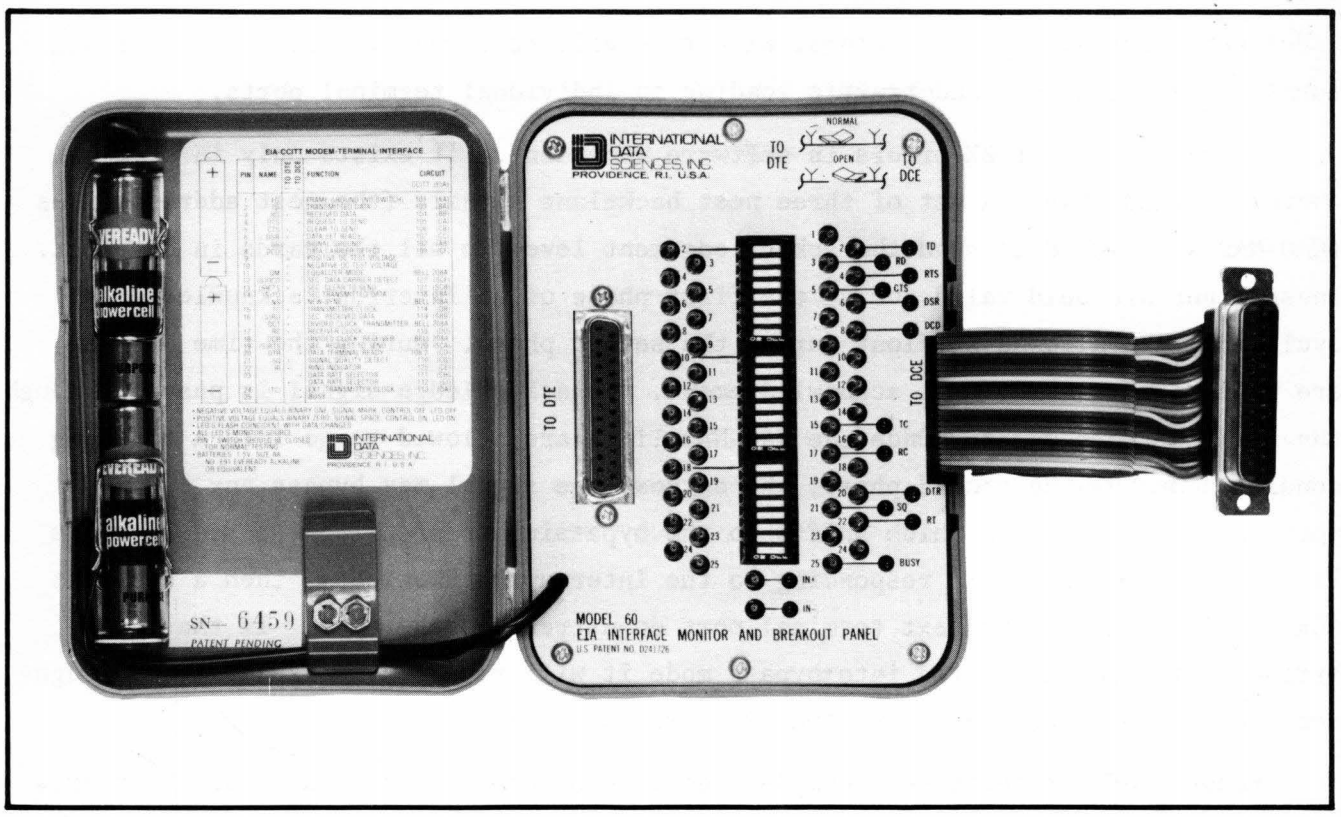


Figure 5-10. Breakout Box

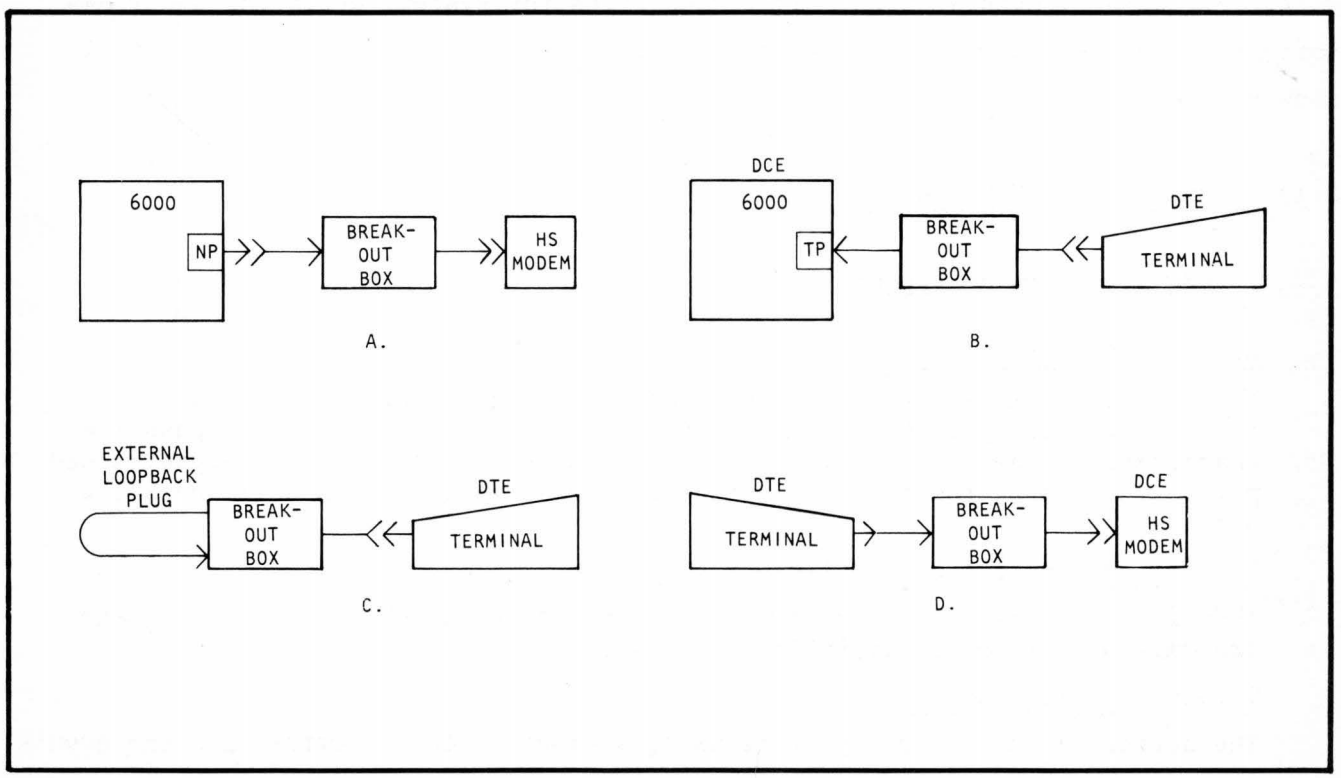


Figure 5-11. Breakout Box Applications

understood, but among other things, BX errors will be a function of card position, total traffic loading, and traffic loading on individual terminal ports.

Another cause of BX errors is software dependent. It exists only in systems operating under S49. A set of three nest backplane signals (the nest address lines (NA0-NA2)) are used to send the acknowledgement level to all the cards in the nest. These lines are held valid during the first phase of an interrupt acknowledgement cycle, but are allowed to float during the second phase. During the time NA0-NA2 are valid for terminal port acknowledgement, the acknowledge signal is passed through the terminal port cards. Once the NA0-NA2 lines are allowed to go into a floating condition during the second phase, the acknowledge signal may bypass any terminal port card. If the card which shifts to the bypassing mode during the second phase is the same card which is responding to the interrupt acknowledge, then a spurious ACK will be sent to the next terminal port downstream in the nest. If that downstream port has not shifted into bypass mode it will receive the faulty acknowledgement and either generate an eventual BX error or an overrun error.

Because of the relatively complex sequence of events and because of the narrow time window for the sequence to occur, the resulting BX errors and overruns occur quite infrequently even at high traffic densities for systems operating under S49 software. Systems operating under S46 and S47 are even less liable, due to their slower speed.

5.10 CAUSES OF BX OVERFLOW

5.10.1 NORMAL BUFFER OVERFLOWS

Dissimilar Terminal Port Speed

The slower terminal port will not be able to output characters as fast as the higher speed port can input characters. The network link will pass the characters as they become available from the receive side of the higher speed port. Therefore, the transmit buffer will gradually fill up until overflow occurs.

Dissimilar Stop Bit Quantities

When incoming characters use 1 stop bit, but outgoing characters use 2, the transmit buffer gradually fills, as above.

Terminal Device Too Fast

The device connected to a port is using a clock which is faster than the 6000's internal clock, but not so much faster that character errors occur. The traffic must be continuous. The results are the same as above.

Continuous Space in an Incoming Data Line

When either a tail circuit or a local terminal outputs spaces, and the attached modem is strapped for SPACE hold, the modem outputs SPACE continually. Since SPACE is a character, the continuous SPACES transmitted to the remote INP cause a BX overflow. The cure is to strap the modem to MARK hold.

5.10.2 ABNORMAL BUFFER OVERFLOWS

A terminal port which is requesting service receives an interrupt acknowledge which is spurious and not generated by the master controller. The interrupt request is cleared because of the spurious acknowledge but no servicing of the interrupt request by the master controller takes place. If the spurious acknowledge clears a transmit request, there will be no further transmit request and a BX error will occur. If the spurious acknowledge clears a receive request the next received character will create an overrun condition at the port.

5.11 LOOPBACK TESTING

Terminal ports and network ports are tested in remote and local mode.

5.11.1 TERMINAL PORT LOOPBACKS

Loops at the TP level are single-ended loops (Figure 5-12). They are caused by setting the mode (M =) parameter to either L or R.

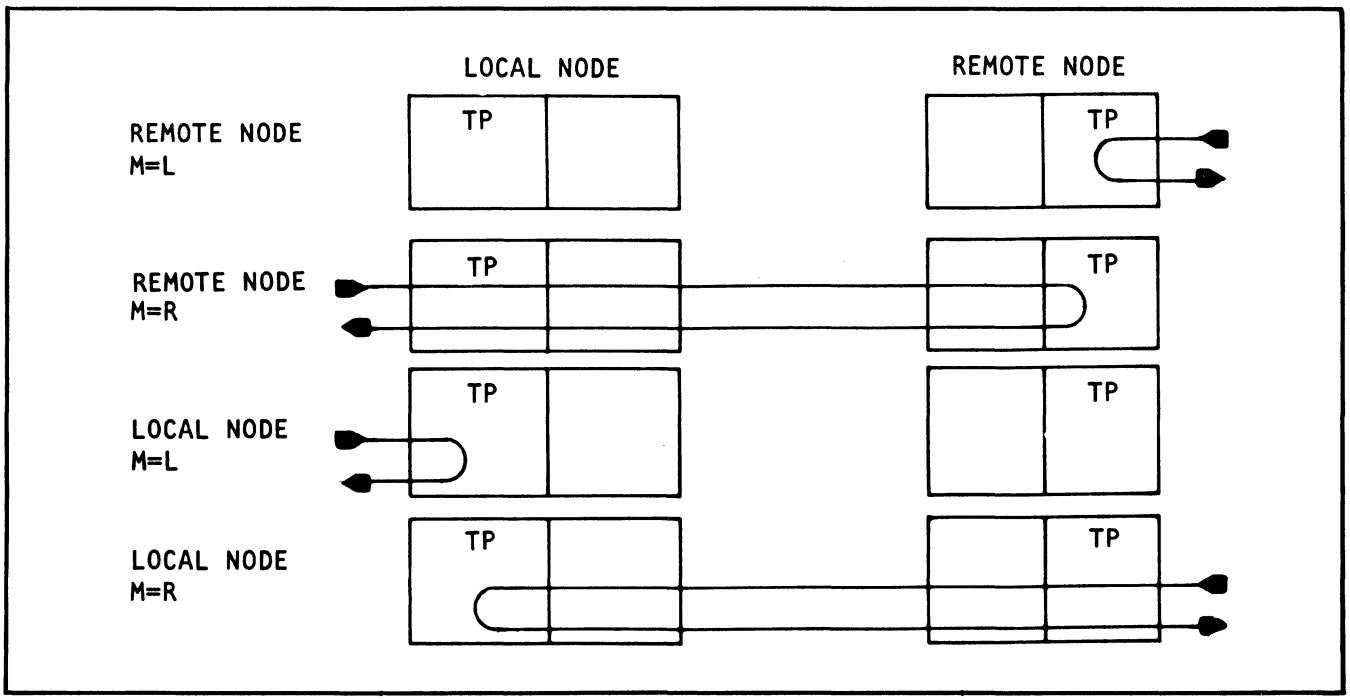


Figure 5-12. Terminal Port Testing

5.11.2 NETWORK PORT LOOPBACKS

Loops at the NP level are bidirectional loops (Figure 5-13). They are caused by setting the mode (M =) parameter to L (loop). When placing a network port in L (loop) the adjacent node is the node containing the network port.

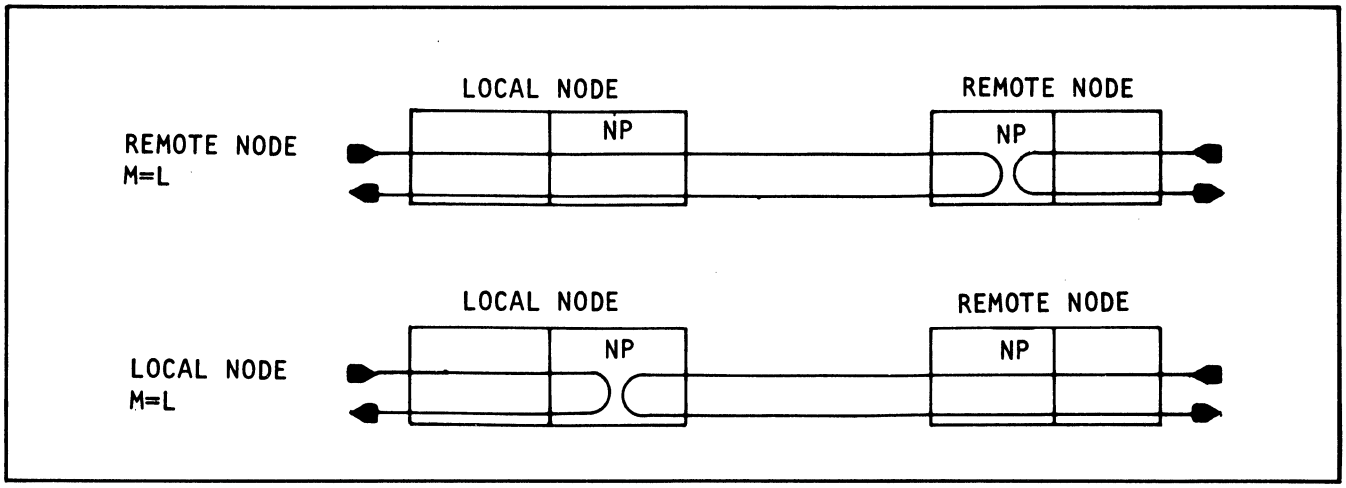


Figure 5-13. Network Port Testing

The process of port loopback testing can be used to isolate the most likely source of transmission failures. Table 5-9 summarizes and locates the failures.

TABLE 5-9. FAILURE TYPES AND LOCATIONS

Type of Loopback Failure	Probable Location of Failure
Local TP, local loopback	Terminal/DTE interface
Remote TP, local loopback	DCE interface
Local TP, remote loopback	
Remote TP, remote loopback	
Local NP, local loopback	
Local NP, remote loopback	
Remote NP, local loopback	Local operator error
Remote NP, remote loopback	Reboot system to recover

The following examples illustrate the commands necessary to perform the loopbacks.

```
SELN (remote node no.) ENTER
SELP (remote TP no.) ENTER
CHNGA M ENTER
  R  ENTER                          Remote loopback of remote TP
     or
  L  ENTER                          Local loopback of remote TP

SELN Local Node # ENTER
SELP Local Port (TP) # ENTER
CHNGA M ENTER
  R  ENTER                          Remote loopback of local TP
     or
  L  ENTER                          Local loopback of local TP

SELN hex hex ENTER                  node number in hex
SELP 2 ENTER                        or other NP port number
CHNGA M ENTER
  R  ENTER                          Remote loopback of local NP
     or
  L  ENTER                          Local loopback of local NP
```

CHAPTER 6

APPLICATION NOTES

6.1 INTRA-NODE COMMUNICATION

Intra-node communication can be verified by utilizing a local network port operating in local loopback. (See Figure 6-1.)

In Figure 6-1,

NP-2E has its mode parameter defined as: M = L

TP-0A has its transmit data path defined as: AN = 3, AP = 0B

TP-0B has its transmit data path defined as: AN = 3, AP = 0A

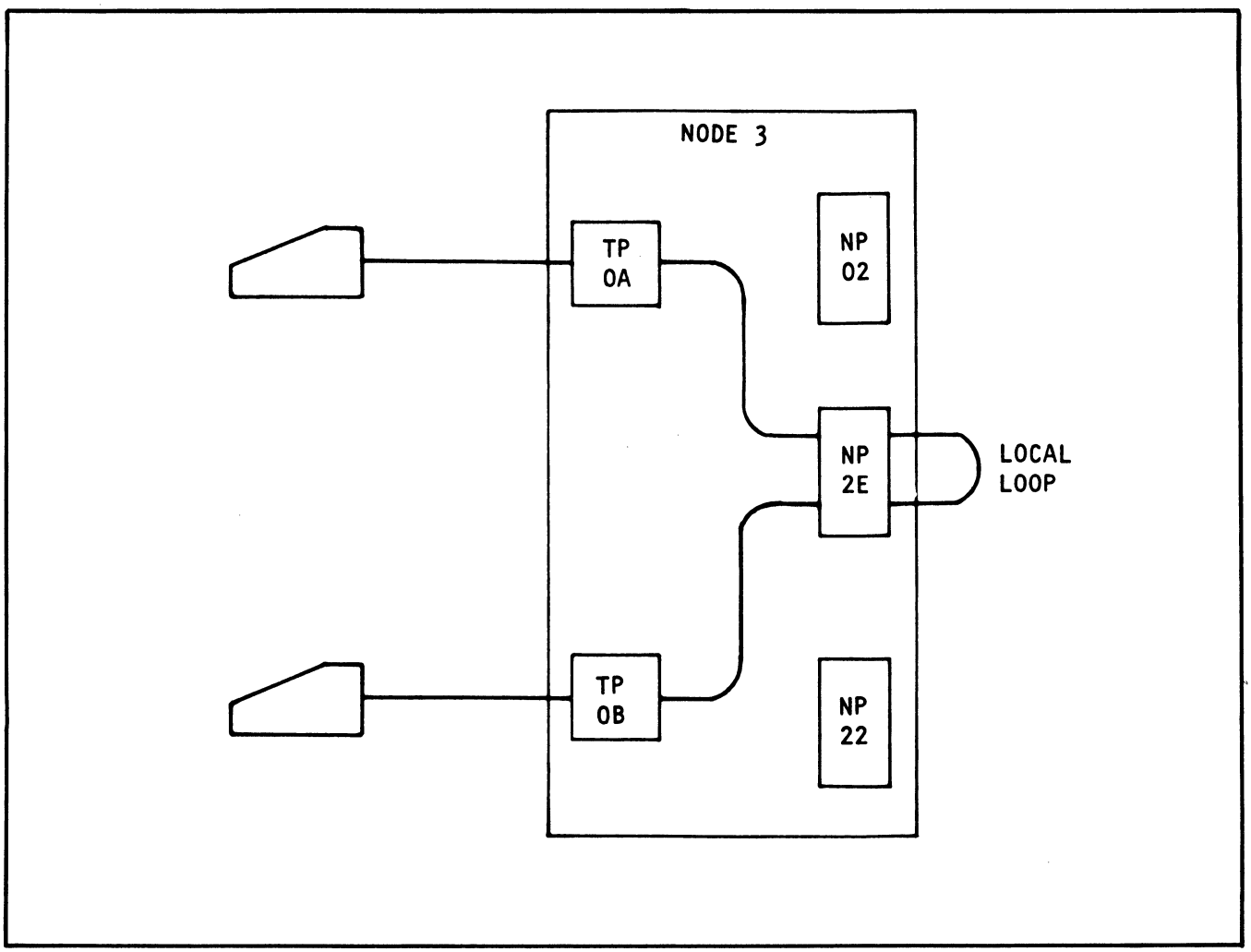


Figure 6-1. Intra-node Communication

6.2 FINE TUNING THE SYSTEM

6.2.1 CODE TYPE

The selection of the code type is based on the number of information bits from the terminal with start, stop, and parity bits removed. Other considerations are:

a. All terminal data placed in the network frame is Hoffman coded (variable length prefix code)

b. Compression available with code types 3 and 5 means non-uniform weighting of the characters in the code set based upon the frequency of utilization of the character.

c. The code type selects the number of data bits from the user terminal that will be code converted. See Table 6-1.

The following examples illustrate the relationship between code type and word length:

Example 1:

If the user terminal is ASCII without parity, use code type 0 because all eight bits could be used to form characters (required for a graphics terminal).

Example 2:

For an ASCII terminal with even parity, use code type 2 or 3. Since the parity bit is externally supplied by the Astro, the 7 information bits from the code set need to be converted. The choice of code type 2 or 3 would depend upon the actual data and whether compression is needed.

TABLE 6-1. CODE TYPE CHARACTERISTICS

Code Type	Number of Data Bits	Characters Possible
0	8	256
1	8	256
2	7	128
3	7	128
4	6	64
5	6	64
6	5	32

6.2.2 ARQ FRAME SIZE/FIFO LENGTH

The ARQ frame size is the number of frames that are buffered for retransmission in case a NAK is returned. The value is a characteristic of the network port, and is selectable as 7, 15, 31, 63, or 127 frames. It must exceed the expected round-trip path delay for the link attached to the NP. The standard (default) ARQ size is 7, which is sufficient for land lines, but the expected path delay for satellite links may require up to 127.

The FIFO size can also be set, at 32, 64, 128 or 256 bits in length.

ARQ frame size and FIFO length are related: The FIFO size fixes the minimum frame length and the ARQ size fixes the maximum number of frames to be buffered. Therefore, the product of the two is the minimum number of bits of network data that will be buffered. For error-free transmission, this product must be greater than the total number of bits of round trip-path delay.

As an example, assume a speed of 9600 bps and a round-trip path delay of 0.120 sec. The round-trip delay in bits is

9600 x .120 = 1152 bits

If the FIFO size (F) is 64 bits the ARQ frame size (AF) must be greater than 1152/64 = 18. The next frame size larger than 18 is 31, which will ensure an adequate buffer for the delay path length.

So, for this configuration, F = 64 and AF = 31.

6.2.3 OPERATION MODE

6.2.3.1 S46 AND S47 OPERATION. For most observed applications modes 2 and 6 seem to be the most useable. If the terminal protocol is polling and addressing as with the 3270, Op mode 6 is required to minimize the risk of sync fill during an address cycle. If mid-message sync fill is not a real problem, then mode 2 should be used. This would be for higher volume like a remote print on RJE application.

6.2.3.2 S49 OPERATION. Operation modes 4A and 6A appear to be the most useable for most observed applications. If the protocol is polling and addressed as with the 3270, Op mode prevents the insertion of a SYN fill at the beginning of a BSC message block. If OM3 = 0, the receive data output (BB, pin 3) will be delayed by the

quantity of characters specified in decimal by the characteristic CD. If OM3 = 1, the delay will be for the number of frames specified by CD.

If start of message or mid-message SYN fill poses no problem (as with high-volume remote print on RJE application) Op mode 1 with OM1 = 1 should be set.

6.2.3.3 ANALYSIS OF BUFFER OVERFLOW PROBLEMS. Problem 1: Buffer overflow usually occurs during bursts of data. For example, if the slot weight is 6 and the terminal input rate is 7 characters per frame, data will build up in the buffer at the rate of one character per frame. If this situation continues, eventually the buffer will overflow, and the error message BR will be displayed on the self-scan.

The rate of buildup of asynchronous data can be tested with an IDS Model 1300 TDM-Modem Test Set. With the remote node in remote loop, connect the 1300 with settings as follows: DTR and RTS at OFF, PATTERN at MARK, and CODE LEVEL at infinity and power on. Next, raise DTR, raise RTS, set CODE LEVEL to the proper value, and set PATTERN to 63. Select proper PARITY and STOP BITS settings. The preceding steps will assure that the code word buffers are freed from the port.

For high-density synchronous traffic, such as that between two computers, the following test will disclose a potential problem.

Again use the IDS 1300.

With the IDS in sync, raise the TX error switch and observe the time interval until the display starts clocking errors. Wait about 3-5 minutes, then raise the TX error switch and see if the interval has substantially increased. If it has, the slot weight for the port is too low.

Problem 2: Buffer Overflow (BR). Monitor the Error Density factors for the node. This will indicate the frame retransmission rate and will cause buffer overflow due to the reduced throughput and buffer buildup. The larger the value of slot weight, the better the burst data protection in a high error rate situation. Also, longer network outages can occur before losing data.

Buffer Multiplier: With one RAM module, a system has about 720 code word buffers that can be allocated for storage of TP data. Each buffer can hold 7 to 14 characters (depending on encoded data length).

The buffer multiplier should be set to a value that will allow use of all the buffers. To calculate this the following formula can be used:

$$\sum_{0}^{N} SW \times B > 720$$

The sum of all slot weights from port 04 to N (highest number) times the buffer multiplier should be greater than 720.

Example: Ten ports

04 = 7200 bsc Sw = 48

05 = 2400 bsc Sw = 12

06 = 300 s/s Sw = 4

↓ ↓ ↓

0D 300 s/s Sw = 4

Sum of Sw = 48 + 12 + 8 x 4 = 92

If the Buffer Multiplier is set to 3, then the maximum number of buffers that could be used would be:

92 x 3 = 276.

Over 445 buffers in the pool would be unused, and yet the system would be "out" of buffers.

This now raises the question: raise the slot weight or the Buffer Multiplier? The answer is to do both. The two BSC channels may suffer from excessive delay. In this case, their slot weight would be increased. Then, after that change, the Buffer Multiplier should be raised so that the product of the sum of the slot weights and the buffer multiplier is greater than 720.

In summary, there is no table of values to use for all situations. With the 6000, the more that is known about the user's data, the better his system can be tuned to handle his operation.

6.2.4 TP SLOT WEIGHT/BUFFER MULTIPLIER

The slot weight is the maximum number of characters one port can insert into one network frame. The Buffer Multiplier is the factor applied to the slot weight that determines the maximum number of code word buffers the port can take from the system buffer pool:

The Operation Manual gives some suggested values to be used for both factors. These were arrived at as average useage. Since no system or terminal is average, observation of the effect that variation of these parameters has on system operation will finally determine their final values.

Increasing the value of the slot weight usually presents no problem. The problem normally arises when it is set too low.

6.2.5 THRESHOLDS

There is another area where there are no fixed answers. In practice, the alert messages should only be sent to alert the operator to a problem. Frequency messages reduce the value of the report system.

Threshold alarms (alert messages) are Monitor functions. These differ from the statistic display in that they are an instantaneous measurement against a limit, rather than a time-averaged element. An alert message for Error Density could be received and examination of the statistic would reveal that the parameter is way below the set threshold. The statistics displayed are time averaged against the system time-constant and reflect the long term measure of the element.

With the above in mind, what we should consider is when will intervention be required. These points should be evaluated and they would set out thresholds. For example:

1. Error Density = $\frac{\text{NAKS R X}}{\text{Frames TX}}$ x 100%

   With an error density of say 5% let's see what the bit error rate would be. Assume FIFO is 256 and we are using a minimum frame length.

   $$\frac{5\ \text{Naks}}{100\ \text{Frames}} \text{ or } \frac{1\ \text{Nak}}{20\ \text{Rrames}} \text{ or } \frac{1\ \text{Nak}}{20 \times 256} \text{ or } \frac{1\ \text{Nak}}{5120\ \text{Bits}}$$

   If we further assume single bit errors, it would mean 1 error per 5120 bits or a bit error rate of 1 part in 5×10^3. Relating this to the Codex 9600 modes, it would mean the good data lamp out and the marginal circuit lamp on "solid".

In thinking of communications, the above may or may not be a problem. A single hig or modem retrain could cause the error density to exceed the threshold. It would also be necessary to examine the statistic to see if any long term problems exist.

Again the numbers in the book are only guidelines and each system may be different.

6.2.6 POWER SUPPLY ADJUSTMENT

The outputs of the 200W power supply are adjusted at the factory and rarely need adjustment in the field. To check the outputs, use a portable multimeter. The most rugged for field use is a 3-1/2 digit portable digital multimeter, of which there are several on the market. A Fluke model 8020A is satisfactory, with an accuracy within 0.25% of actual, ±1 digit.

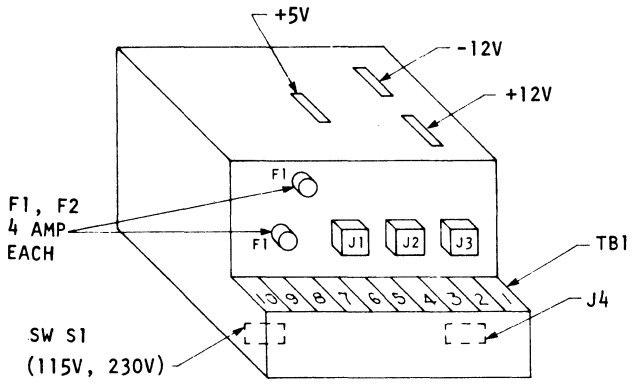
Measure +5Vdc on the top of the MC1 card, across one of the filter capacitors. It must read +5V ± 0.10Vdc.

Measure the +12 and -12Vdc on TB1 of the power supply: +12 at TB1-7 and -12 at TB1-8. They must be nominal ±0.2Vdc.

Figure 6-2 shows the locations of the adjustment pots on the three power supplies that may be encountered in the field. Identify the models by the presence or absence of heat sinks on the end of the unit and the layout of the boards as shown in the figure.

NOTE

The 400W power supply is not adjustable.

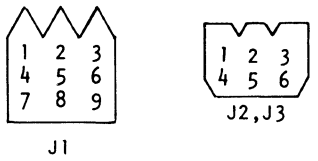


J1

1	SIGNAL GND	Y
2		Y
3		BN,GY
4	+5VDC	BN,WH
5		BK
6		GN,Y
7	+12VDC	
8	-12VDC	
9	SENSE	

J2,J3

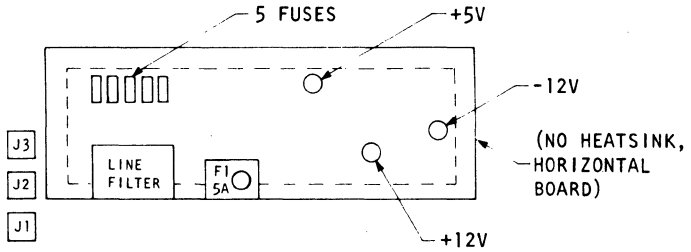
1	SIG GND	BK
2	+5VDC	RD
3	+12VDC	OR
4	SIG GND	BK
5	+5VDC	RD
6	-12VDC	BLU



0 10	0 9	0 8	0 7	0 6	0 5	0 4	0 3	0 2	0 1
BRN		-	-	GRN	BK	WH	-	BK	WH

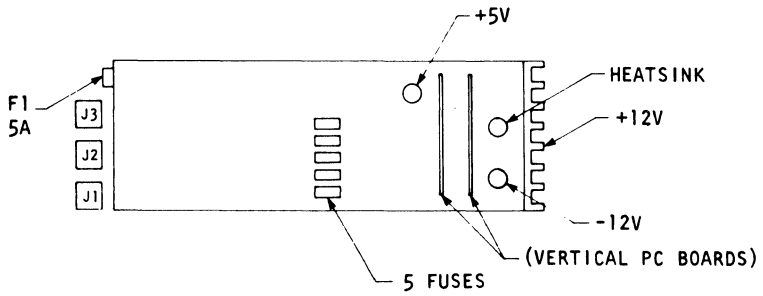
6000 MAINFRAME AND AUXILIARY.
ONE FAN ON DS, AIR FLOW FROM FRONT OF MAINFRAME - OUT PAST PS

20 AMP POWER SUPPLY - MAINFRAME & AUXILIARY RACK



TWO FANS IN MAINFRAME - AIR FLOW IN TOWARD POWER SUPPLY

20 AMP POWER SUPPLY - MAINFRAME ONLY



2 FANS IN MAINFRAME - AIR FLOW TOWARD POWER SUPPLY

Figure 6-2. Adjustment Points on 200W Power Supplies

APPENDIX A

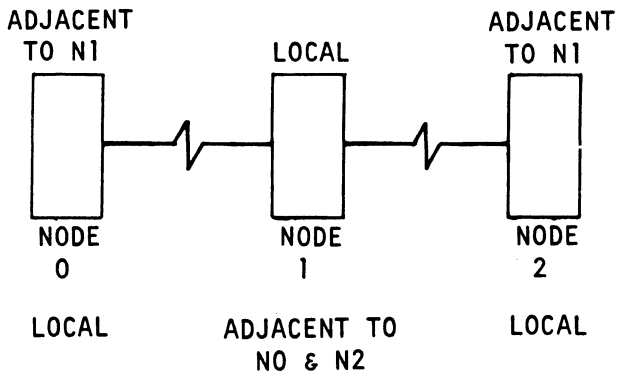
GLOSSARY

This glossary defines terms as used in manuals about the 6030/6040 series of Intelligent Network Processors.

For convenience and brevity, the 6030 and 6040 series of intelligent network processors are referred to collectively as the 6000 INP's, or even more simply, INP.

ACK — Affirmative acknowledgement sent by a receiver to a transmitter that a message frame was received intact.

ADJACENT NODE — The next node logically in the communications link.



ADJACENT PORT — The port in an adjacent node to which a port in the local node is connected.

ARQ — Automatic Repeat Request. In the 6000, an error-detection scheme is employed so that the reception of erroneous data initiates a request for retransmission of all frames following the last frame received intact.

AUTOECHO — Automatic serial loopback of data received in asynchronous mode from a local TP.

AUTOSPEED — Automatic determination of the baud rate of incoming data. The rate is defined by the first character - the control character - sent by the terminal. The local 6000 transmits this to the receiving node, which converts it to the ASCII or EBCDIC hex equivalent that can be read by the receiving host computer.

BSC	Binary Synchronous Communication. An IBM synchronous half-duplex line protocol, and hardware interface specification. Three code sets will be used: EBCDIC, USASCII, and 6-bit Transcode.
BUFFER	Temporary memory storage for data.
BUFFER MULTIPLIER	A nodal parameter to limit the maximum number of data buffers that any port can use at a given node. The maximum number is proportional to a port's slot weight times the buffer multiplifer. A buffer multiplier of 5 is recommended for standard systems.
CONFIGURATION MEMORY (CMEM)	A non-volatile memory used to maintain off-line configuration information. Modified when the configuration is changed via control terminal port or operator console.
CONTROL TERMINAL PORT	A standard terminal port that (1) is asynchronous, (2) has an ASCII, start/stop asynchronous terminal attached, and (3) is designated as a Control Terminal Port when the network is configured. It communicates interactivity with the 6000 in half-duplicates. The attached terminal can be used in place of an Operator's Console to configure the network and perform all the other functions of an Operator's Console in the Program and Monitor modes. However, it cannot be used for diagnostics. The attached terminal may be the terminal control unit of a host computer.
ENTROPY	The theoretical average minimum number of bits required to represent all characters of a code.
FRONT END	A processor attached locally to a host computer through a terminal handler. It assumes management of the telecommunications network and presents error-free data from the net to the host computer, in a defined, constant format from a single source.
GO-BACK-N-ARQ	An automatic repeat request that compensates for path delays in satellite circuits. Frames are transmitted continuously with no wait for an ACK, until a NACK is received. Then the transmitter goes back n frames to the beginning of its buffer, and retransmits. The value of n is set to account for path delay.
LOCK BYTE	An addressable byte used to control access to a common area of RAM (a lock byte area) that is used by all processors, so that a processor cannot access the area if another processor is using it. The purpose is to protect critical programs that are running.
LOCK BYTE AREA	An area of memory that is common to all processors. It provides processors with exclusive access to 256-byte segments of RAM. This prevents interruption of a critical program by other processors. The key to each segment is an 8-bit "lock byte." When a processor addresses the byte and reads it, it

clears the byte to all 0's. Another processor addressing the same byte finds all 0's and retries at the cycle rate until the first processor has written the byte back.

NACK — Negative Acknowledgement. A message sent by a receiver to a transmitter that an incomplete or garbled frame was received.

NEST INTERFACE CARD — A hardware module used to terminate the incoming bus from the mainframe, drive the port nest I/O bus, and redrive the mainframe I/O bus to the next port nest.

NETWORK PORT — A physical port through which data is transferred to and from a communication link to another INP.

NIC — See Nest Interface Card.

NODE — A point in a communication network where an INP resides.

NP — See Network Port.

NP BOOT — The NP BOOT function, which is automatically implemented, causes the adjacent node to reload the last booted configuration. The NP BOOT occurs when the local node does not receive any response to the frames sent as governed by the AF = (ARQ Frame size) parameter.

The following chart lists the timeouts before the first NP BOOT occurs:

ARQ SIZE	TIME
7	40 sec.
15	90 sec.
31	135 sec.
63	185 sec.
127	240 sec.

After the first NP BOOT occurs, an NP BOOT is sent every 10 seconds. During the 10-second period, any queued frames are transmitted.

If the carrier signal from the trunk modem is low, the NP BOOT function is not allowed.

PORT — A logical or physical communication entity, through which data enters and leaves the 6040.

PORT NEST — A chassis containing a nest control card, network ports, and terminal ports.

PROCESSOR — A hardware module (card) containing a microprocessor.

RAM — Random Access Memory.

ROM — Read-Only Memory

SLOT WEIGHT — A value used to control the maximum rate of service for a terminal port. For uniformly proportional servicing, the following formula can be used:

$$\frac{\text{terminal speed}}{300} = \text{slot weight}$$ (rounded to nearest integer, but at least one)

TAIL CIRCUIT	A point-to-point circuit that connects a remote terminal to a port in a local node. Since the terminal is remote, the connecting communication link requires a modem at each end to assure error-free data reception. A special crossover cable connects the local modem to the net port.
TERMINAL PORT	A physical port through which data is transferred to and from a local user terminal. Two ports reside on one terminal port card. There is one terminal port for each terminal; multidupped terminals are connected to a terminal handler which functions as a single-terminal in the net.
TP	See Terminal Port.
TRANSFER PORT	A unidirectional intermediate port in a multinode terminal port transmit or receive data path.
UNIVERSAL TERMINAL PORT	See Terminal Port.
XP	See Transfer Port.
TERMINAL PORT BUFFER	Storage for character received from the terminal port. Each terminal port is allocated an emitted amount of buffer space. The limit is defined by the buffer multiplier.

APPENDIX B

6030/6040 SYSTEM OPTIONS

B.1 HARDWARE OPTIONS

Both hardware and firmware options are available to interface the communications processing capabilities of the 6030/6040 series INP's. Brief descriptions of the options follow.

6103 Processor Module

This option is a plug-in assembly that provides the 6040 series with an additional processor for incremental processing and throughput capabilities.

6114 Buffer Memory

This option is a plug-in assembly that provides an additional 16K byte increment of RAM buffer storage.

6120 Operator Console

An Operator Console is available to select, examine, and modify configuration, status, and performance data anywhere in the network. It also serves as a hardware diagnostic/test panel during installation and maintenance.

The Operator Console contains a self-scan alphanumeric 32-character (5 x 7 dot) display, an 18-key multifunction keyboard, indicators, and a locking power/function switch.

Alternately, using the Control Terminal Port Support Option 6321, any unassigned terminal port can be designated a control terminal port, enabling most asynchronous terminals or a host computer to perform the tasks of monitoring, interrogation, and reconfiguration.

6122 Configuration Memory Expansion

This option provides additional non-volatile configuration memory for up to 32 ports. The incorporation of this option provides the 6040 with the capability of storing alternate network topologies having different characteristics. This is particularly useful in day/night operations where different types of terminals are used or when a fall-back configuration or alternate network topology is desired.

6130 Dual Universal Terminal Port Module

The 6130 is a single plug-in module that provides two independent RS-232-C or CCITT V.24 terminal interfaces. Each interface may be asynchronous or BSC synchronous and can appear as a modem (DCE) or as a data terminal (DTE) depending upon the interface cable used to connect the port module to its input/output device.

A port is configured by entering its characteristics (type, speed, code, data bits, parity, etc.) and other parameters into memory via the Operator Console or Control Terminal Port.

Up to three control signals may be passed end-to-end bidirectionally. Clear to Send is looped back locally from Request to Send with a switch selectable delay. The port module also recognizes and passes "break" and provides a loop control feature to appropriately loop data and control signals.

The standard asynchronous speeds supported include 75, 110, 134.5, 150, 300, 600, and 1200 bps.

When operating in the BSC synchronous mode, ASCII or EBCDIC codes are supported as well as the transparent text mode. The following code dependent functions are implemented:

- Character framing via SYN characters.
- Recognition of transparent/non-transparent text mode transitions.
- Strip/insertion of idle time fill characters.

Clocks are strap selectable on the Terminal Port Module. The terminal port (DCE) receive clock can be selected from the receive or transmit clocks supplied by the Data Terminal Equipment (up to 9600 bps), or from a set of clocks supplied on the Terminal Port Module (1200, 2400, 3600, 4800, 7200 or 9600 bps). The terminal port (DCE) transmit clock can be selected as the DTE transmit clock or can be the same as the terminal port receive clock. Output transmit and receive clocks are generated from the selected DCE receive clock.

6131 Activity Indicator Terminal Port

Option 6131 is a single plug-in module that performs the same functions as the standard (dual universal) terminal port module. The activity indicator terminal port incorporates the following enhancements:

- Four LEDs are mounted on the rail of the card. They show input and output signal activity for each channel on the card.

- Control signal strapping capabilities have been improved.
- The new board layout facilitates installation of small scale, customer-special circuitry. A three-DIP subassembly can be cleanly mounted on board and connected by wire wrap.
- The EIA drivers are supplied with $\pm$9V instead of $\pm$12V, which increases reliability and MTBF.

The option supports the same standard asynchronous speeds as Option 6130, and provides the same clock speeds and sources.

6136 Non-Standard Data Rates

This option provides non-standard terminal port data rates for those applications which require other than standard Codex-supported data rates. Each non-standard rate replaces any one of the following standard rates:

Asynchronous 75, 110, 134.5, 150, 300, 600, 1200 bps
Synchronous 1200, 2400, 3600, 4800, 7200, 9600 bps

6140 Network Port Module

This option consists of two plug-in assemblies that provide an additional high-speed output port. Each 6040 base unit includes two 6140 modules and will accommodate additional network ports as a function of its processing capabilities, throughput requirements and the trunk utilization. The network port will operate at speeds up to 19.2 Kbps and presents a Data Terminal Equipment Interface (DTE) at its EIA type port connector.

6150 Dual Current Loop Terminal Port Module

The 6150 is a single plug-in module that provides two independent high level current interfaces to current loop Data Terminal Equipment at standard asynchronous speeds. The voltage swing may be up to 170V with neutral signaling on 85V with polar signaling at 20 to 60 ma. The current loop interface is provided on the port module 25-pin connector.

Pin	Signal
2	+Batt
4	-Batt
6	Xmit
23	Hi
20	Lo

The 6150 may be field strapped to provide any of the following operations:

Polarity	Current
Positive neutral	20, 40 or 60 ma.
Positive polar	20, 40 or 60 ma.
Negative neutral	20, 40 or 60 ma.
Negative polar	20, 40 or 60 ma.
Half-duplex neutral	20, 40 or 60 ma.

6153 Current Loop Terminal Port

The current loop converter module provides a high-level conversion for neutral or polar current signaling.

The option provides for asynchronous type data flow in the same manner as standard asynchronous data. However, no EIA control information is passed, and if the loop is broken, constant break characters (continuous space) is sent to the remote end.

6161-6166 MIL-STD-188C Port Modules

This series of modules provide EIA to MIL-STD-188 level conversion between the 6130 Terminal Port Module and Data Terminal Equipment or Data Communications Equipment at speeds up to 9600 bps. The 6160 universal option nest is used to house up to 16 of the MIL-STD-188C modules. Two 25-pin female connectors (wired as DCE) are provided on each module. One provides the EIA connection to the 6040 port module via a cross-over cable included with the option. The other connector provides the MIL-STD-188 interface to customer equipment.

Model Number	Provides Level Conversion Between	Speed
6161	Terminal Port and Terminal	to 2400 bps
6162	Terminal Port and Terminal	over 2400 bps to 9600 bps
6163	Terminal Port and Modem	to 2400 bps
6164	Terminal Port and Modem	over 2400 bps to 9600 bps
6166	Network Port Trunk Modem	to 9600 bps

6155 220 Volt Power Option

This option provides for the necessary conversion from 110 volt operation to 220 volt operation.

6156 Rack-Mountable Power Supply

This option provides a rack-mountable power supply for use with the 6161-6166 MIL-STD-188C converter modules.

B.2 FIRMWARE OPTIONS

Non-standard Firmware Modules. The following optional 6030 modules are included with the basic 6040.

6301 Statistics and Performance Monitoring Package

The Statistics and Performance Monitoring Option provides an on-line facility for the collection, computation and reporting of statistical measures of network performance. Additionally, it reports when abnormal conditions occur or user-preset threshold levels are exceeded. Information is reported via the Operator Console or a Control Terminal Port.

This option provides a two part facility: statistics gathering for network and terminal ports, and the monitoring of certain crucial information (i.e., abnormal or critical system conditions). The monitoring function is a background activity and is always enabled. Statistics gathering is performed in real time and can be selectively enabled/disabled on an individual port basis by operator command, in order to prevent unnecessary loading of the 6000 processor. Statistics gathering is concerned with long-term averages, while monitoring functions deal with real-time conditions.

6330 Asynchronous Terminal Support

The 6330 option provides the necessary firmware to support asynchronous communications at seven standard speeds (75, 110, 134.5, 150, 300, 600 and 1200 bps) with corresponding code/data bit/stop bit format. Up to three control signals are passed bidirectionally (DSR, CAR, RNG, or DTR, RTS and Spare).

6335 BSC Synchronous Terminal Support

The 6335 option provides the necessary firmware to support IBM Binary Synchronous Communications with ASCII or EBCDIC codes, including the transparent text mode of operation.

In addition, the 6040 includes as standard firmware functions: Basic Multinode Support, which allows implementation of multinode networks, including transfer ports; ASCII and 2741 Data Compression, which provide coding tables which compress typical ASCII or 2741 source data using variable-length (Huffman) codes.

B.3 OPTIONAL FIRMWARE MODULES

6320 Operator Console Support

This option provides the necessary firmware to support the 6120 Operator Console.

6321 Control Terminal Port Support

This option provides the necessary firmware to support any specifically designated asynchronous ports as a Control Terminal Port. Any start/stop ASCII terminal, or CPU port, may be attached to the CTP and thereby provide the capabilities equivalent to the program and monitor modes of the Operator's Console.

6322 Operator Console and Control Terminal Support

This option combines the features of 6320 and 6321 into one firmware package.

6323 Supervisory Communication Support

Supervisory Communication Support (SCS) is a firmware option that provides users of the 6000 INP with the capability to send addressed messages (datagrams) between Supervisory Communications Ports (SCP's) in a 6000 network.

An SCP is an asynchronous ASCII terminal which connects to the 6000 through an EIA terminal port (TP) interface. The SCP is configured as a control terminal port (CTP) with subtype 2. Messages consist of a decimal message sequence number supplied by the 6000, and destination address(es) and text body supplied by the user. Messages are transmitted using the address packet system currently implemented in the 6000. At an SCP, received messages are identified by node of origin and the message sequence number. Since SCP's use a half-duplex protocol, messages are buffered at the output so that received messages will not be lost while the SCP is inputting. Both flow control and error control procedures are used to deliver messages efficiently without significantly impacting normal system performance.

No new hardware is required for the SCS option.

6324 Report Logging Control Terminal Port

The Report Logging Control Terminal Port (RL/CTP), provides the 6030 and 6040 INPs with the capability of presenting system reports to attached Data Terminal Equipment. Reports may be output as they occur, or may be queued and output on a time interval basis. A date and time stamp is generated when the report is output.

The option provides:

- Centralized logging of all system reports generated by all network nodes
- User selectable reporting interval

- Useable in conjunction with any asynchronous ASCII terminal equipment
- Provides standard control terminal function in addition to report logging.

The Report Logging Control Terminal option consists of a firmware module and a Time of Day Module which incorporates all of the logic necessary to generate the time stamp data. It is installed in the 6000 INP port nest and occupies one nest slot. The module is battery protected to assure no information is lost in the event of a power failure.

The user interface to the report logging function is via a standard 66130, 66131, or 66150 Terminal Port module. This port is configured as a RL/CTP by setting the appropriate port characteristics and parameters. The date, time, and logging interval are also configurable node parameters. The RL/CTP must be configured from the node which it is attached.

The logging interval is specified in tenths of hours from 0 to 240. A value of 0 results in report logging as system reports occur. For values other than 0, reports will be queued and output with a single time and date stamp when the time interval lapses. If there are no reports in the queue, the RL/CTP outputs "EMPTY".

6331 Autospeed

The 6331 autospeed option provides the 6040 Intelligent Network Processor with the ability to automatically determine the speed and character format of asynchronous data and thereby dynamically configure the terminal ports for this rate. This feature permits a single terminal port to support a variety of asynchronous terminal speeds without requiring that an operator manually modify configuration information. Note: This option requires that the host computer connected to the local 6040 Series INP also have autospeed capability, since output data will be reconverted to the original speed.

This feature is particularly advantageous in systems where a variety of terminals, operating at different speeds, all have access to a terminal port through a dial network. With this option, the necessity of fragmenting incoming communications lines into 2 or 3 or 4 speed groups is eliminated. Thus, the minimum number of lines required to support a pool of terminals is more easily achieved. Furthermore, the statistical multiplexing capability of the 6040 Series allows the 6040 to dynamically allocate high speed bandwidth as a function of the specific terminal speed (in contrast to TDM schemes), thereby optimizing data throughput.

6332 Autoecho

Autoecho allows the 6000 INP to serially echo received data on an asynchronous terminal port, thereby providing a primitive form of error control. Autoecho is selectively enabled or disabled on a port by port basis.

6344 Satellite Link Option

The 6344 option alters the GO-BACK-N ARQ scheme from the standard N = 7 to N = 15, 31, 63, or 127, thus permitting additional frame buffering to accommodate the delays introduced in single-hop satellite circuits.

6347 6030/6040 Interface Support

The 6030/6040 interface support allows a 6030 to be connected to a 6040 via a communications link. This provides a "tail circuit" capability to a 6040 communications network.

6950 Diagnostic ROM, Rev 11/6951 Diagnostic ROM, Rev 12

The diagnostic ROM is a special ROM board used to perform diagnostics of hardware faults.

APPENDIX C

INTERFACE SIGNAL LISTS

TABLE C.1 NETWORK PORT INTERFACE SIGNAL LISTS

EIA RS232C	CCITT V.24	Pin	Name	Description
AA	101	1	Protective Ground	Chassis ground.
AB	102	7	Signal Ground	Common signal and dc power supply ground.
BA	103	2	Transmit Input Data	Serial digital data from a data terminal or other digital data source. If accompanied by an external data rate clock (DA), data transitions must occur on positive-going transitions of the external transmit input clock.
BB	104	3	Receive Output Data	Serial digital data at the output of the modem receiver. The data is accompanied by an internal data rate clock (DD) whose positive-going transitions occur on the data transitions.
CA	105	4	Request to Send	A positive level to the modem when data transmission is desired.
CB	106	5	Clear to Send	A positive level from the modem with a selectable delay, after receipt of Request to Send (CA) and when the modem is ready to transmit; i.e., not in the Test mode. CB is low during training or when CA is low.
CC	107	6	Data Set Ready	A positive level to the INP when not in the Test mode.
CF	109	8	Received Line Signal Detector	A positive level from the modem except when a loss of the received input signal is detected.
CD	108.2	20	Data Terminal Ready	A positive level from the terminal indicating the system is powered up and ready to receive.

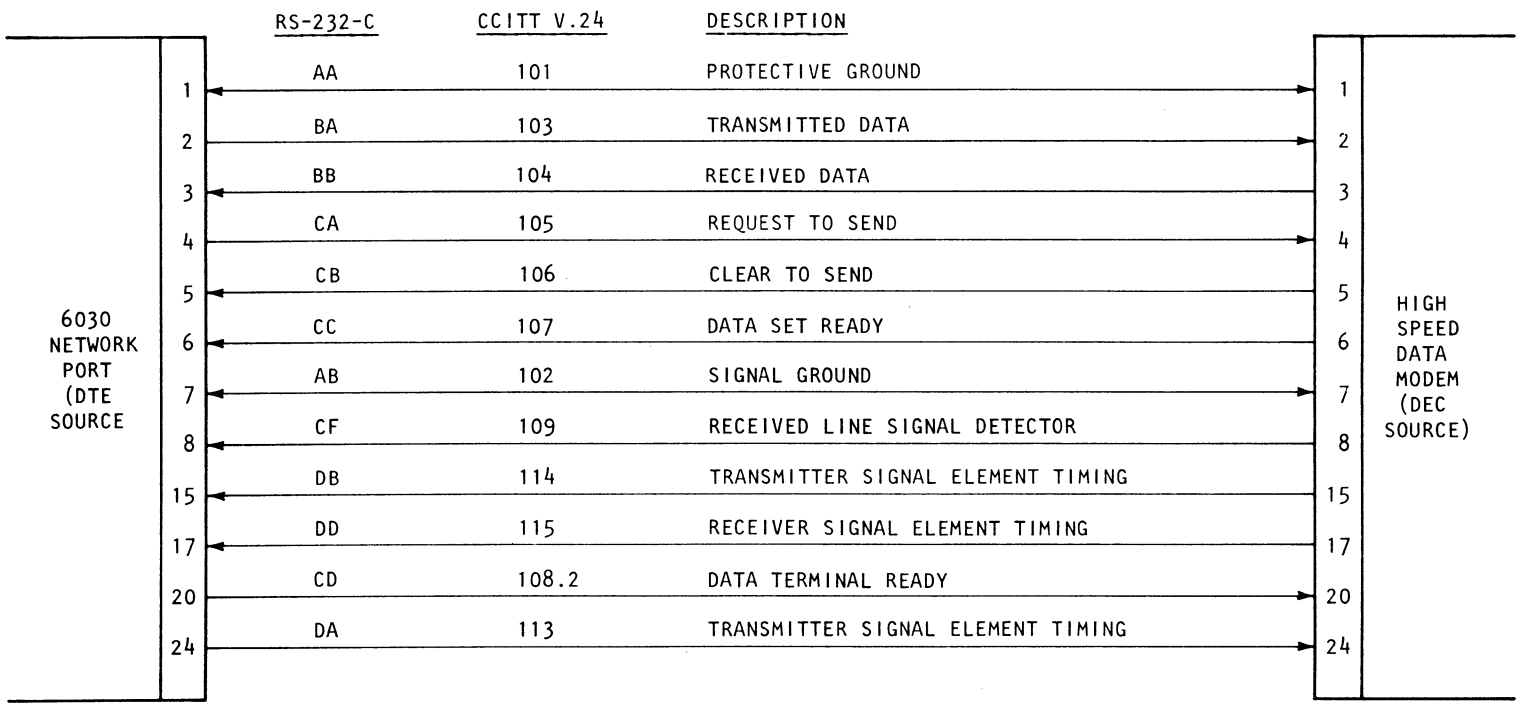


Figure C-1. Network Port to Trunk Modem Interface

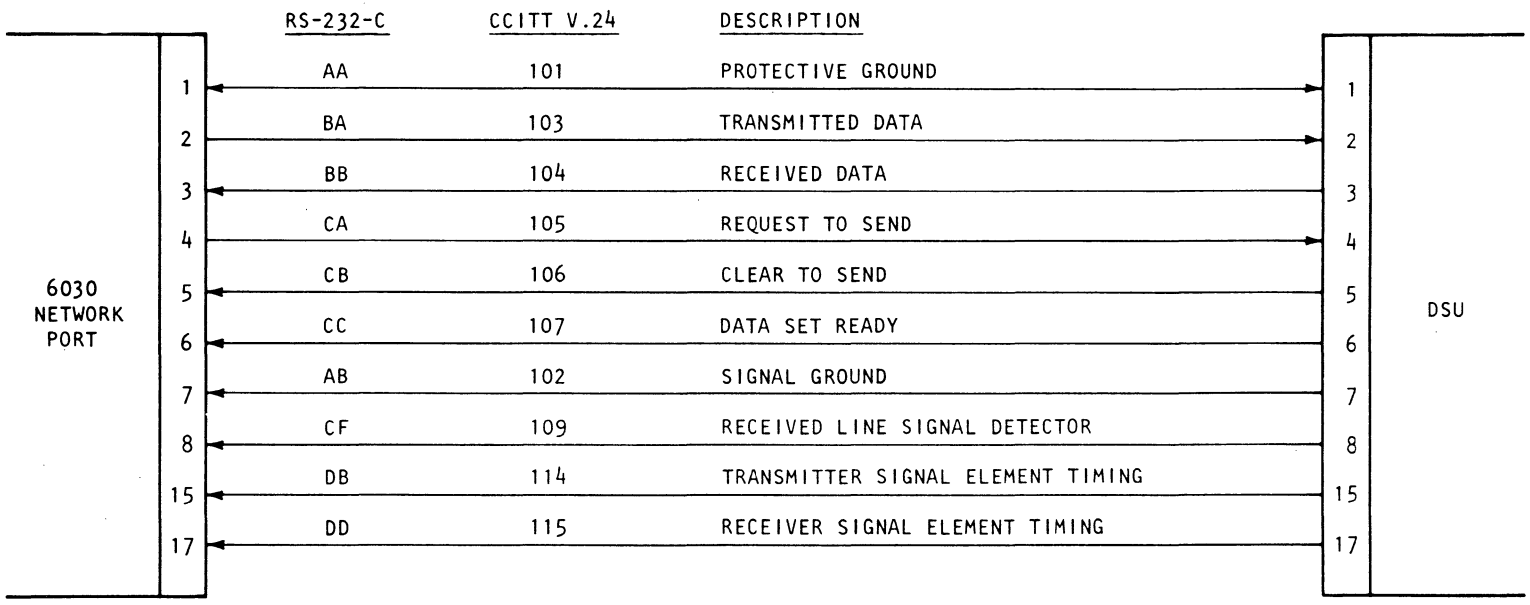


Figure C-2. Network Port to Digital Network Interface via a Data Service Unit for 2400, 4800 and 9600 bps Transmission Rates

TABLE C.1 NETWORK PORT INTERFACE SIGNAL LIST (Cont)

EIA RS232C	CCITT V.24	Pin	Name	Description
DA	113	24	External Transmit Serial Clock	A serial data rate clock input from the data source. Positive clock transitions correspond to data transitions.
DB	114	15	Transmit Signal Element Timing	DCE Source Transmit Clock.
DD	115	17	Receiver Signal Element Timing	A receive data rate clock output for use by the external data sink. Positive clock transitions correspond to data transitions.

TABLE C.2 TERMINAL PORT INTERFACE SIGNAL DESCRIPTIONS

EIA RS232C	CCITT V.24	Pin	Name	Description
AA	101	1	Protective Ground (Earth)	Chassis ground.
AB	102	7	Signal Ground Common Return	Common signal and dc power ground.
BA	103	2	Transmitted Data	Serial digital data from a data terminal or other digital data source.
BB	104	3	Received Data	Serial digital data at the output of the INP (received from a remote end).
CA	105	4	Request to Send	A positive level from the terminal to the INP when data transmission is desired.
CB	106	5	Clear to Send	A positive level from the INP port module to the terminal after receipt of Request to Send (CA), indicating the INP is ready to transmit.

TABLE C.2 TERMINAL PORT INTERFACE SIGNAL DESCRIPTIONS (Cont)

EIA RS232C	CCITT V.24	Pin	Name	Description
CC	107	6	Data Set Ready	An output signal controlled from the remote TP interface (pin 20). Data Set Ready for a modem, Data Terminal Ready for a terminal.
CF	109	8	Received Line Signal Detector	An output signal controlled from the remote TP interface (pin 4). Carrier Detect for a modem, Request To Send for a terminal.
SPARE	---	14	Spare	
DB	114	15	Transmitter Signal Element Timing	A transmit data clock output for use by an external data source. An external source to supply data on data transitions (external only).
DD	115	17	Receiver Signal Element Timing	A receive data rate clock output for use by the external data sink. Positive clock transitions correspond to data transitions (external only).
--	---	18	External Receive Clock	Accepts an external DB for transmission to DCE from crossover cable.
DA	113	24	Transmitter Signal Element Timing	A serial data rate clock input from the data source. Positive clock transitions correspond to data transitions (external only).
CD	108	20	Data Terminal Ready	A positive level from the terminal indicating the system is powered up and ready to receive.
CE OUT	125	22	Ring Indicator	A positive level indicates a ring is being detected.
MB	---	25	Make Busy	

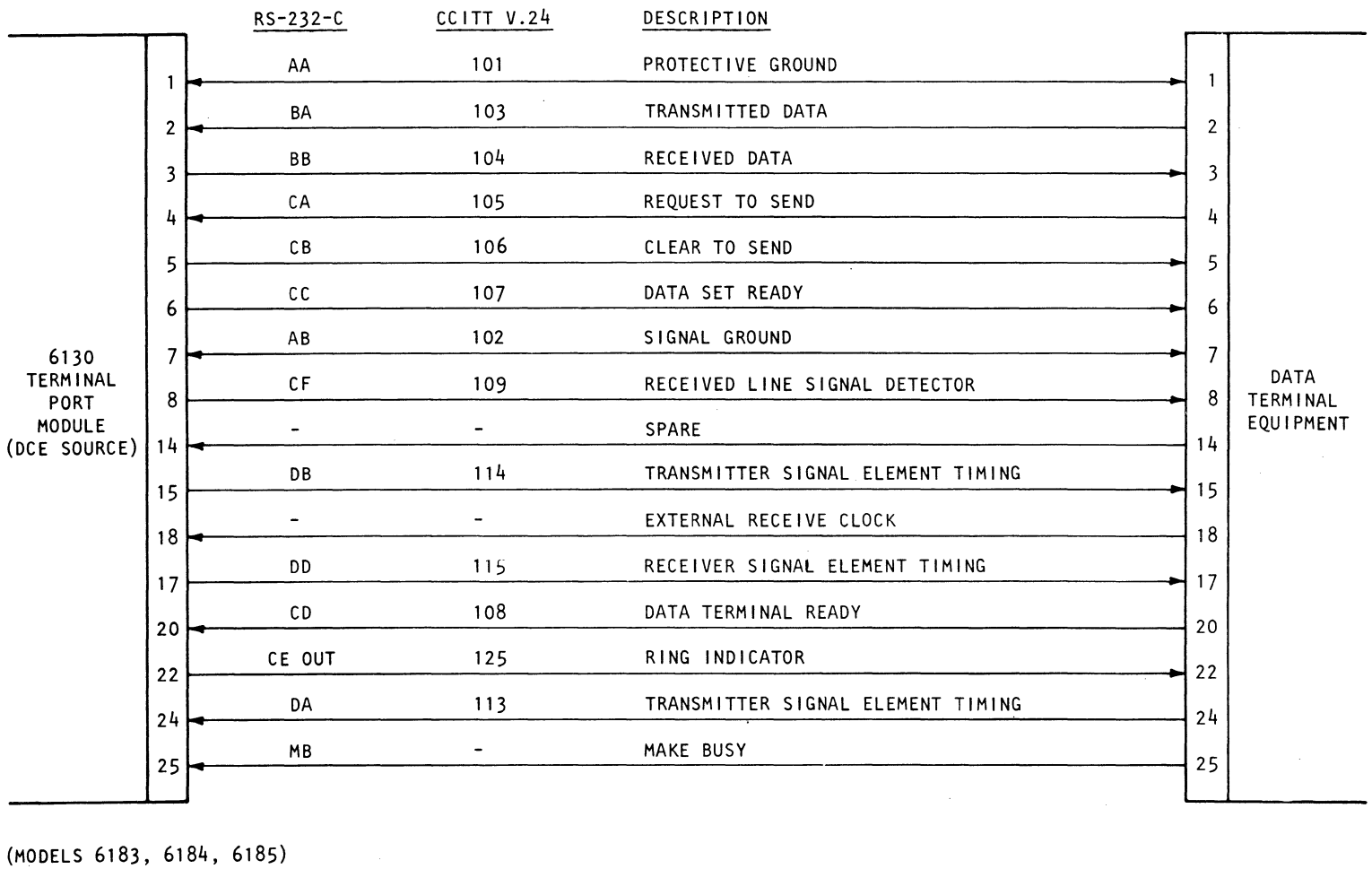


Figure C-3. 6130 Terminal Port Module Attached to Data Terminal Equipment

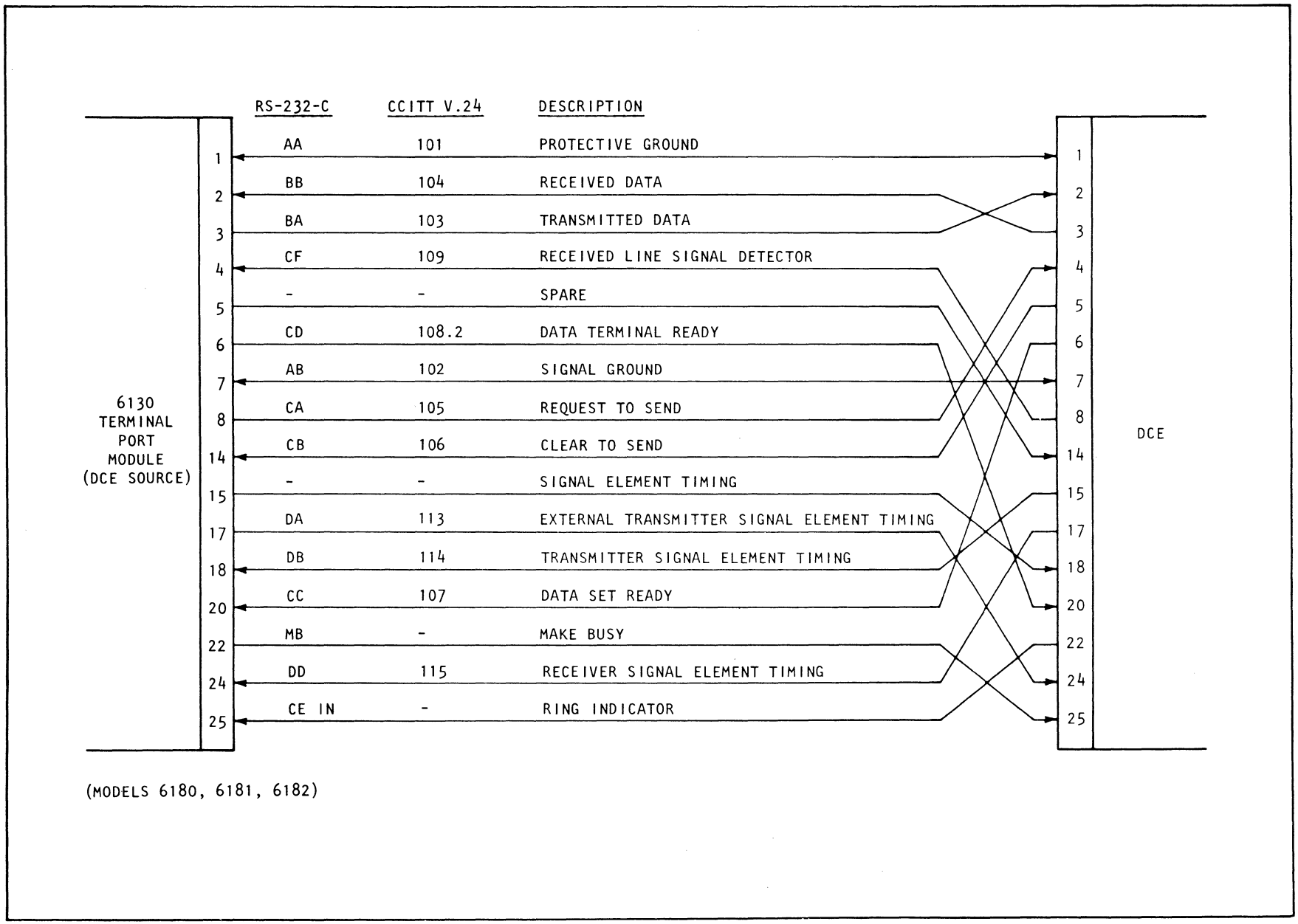


Figure C-4. 6130 Terminal Port Module Interface Signal Crossover Attached to Data Communications Equipment

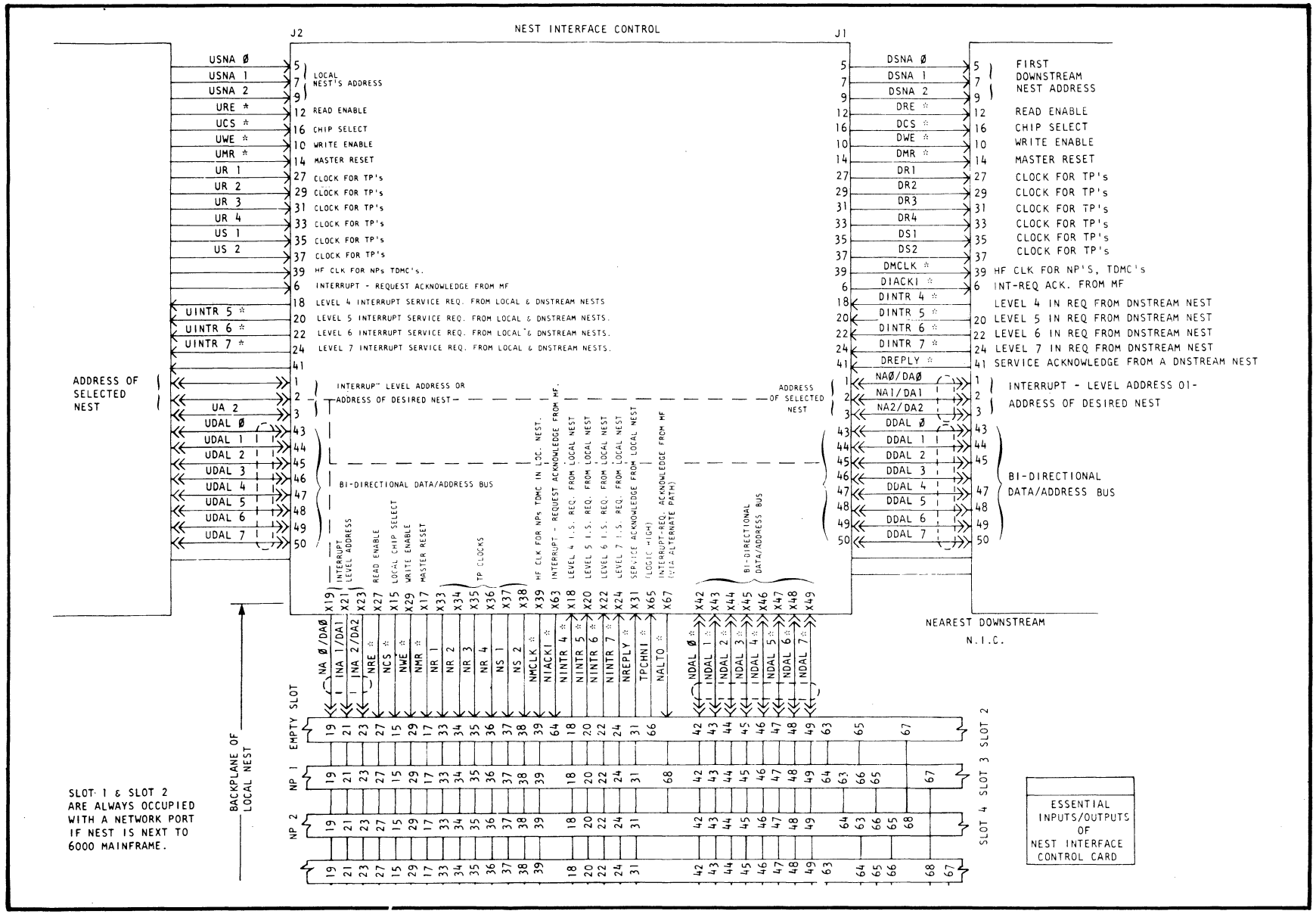


Figure C-5. Nest Interface Control Module Signals

APPENDIX D

UNIVERSAL CODE CHART

This appendix contains tables of codes: 1) Character-to binary and hex, and 2) hex-to-character, for all commonly-used data communications codes.

UNIVERSAL CODE CHART FOR DATA COMMUNICATIONS

8 BIT ASCII			7 BIT ASCII			EVEN PARITY ASCII			ODD PARITY ASCII			EBCDIC			6 BIT TRANSCODE			6 BIT TYPESETTER			EBCD			SELECTRIC			FIELD DATA			BAUDOT		
	BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY C 1248 A8	HEX		BINARY C 1248 A8	HEX		BINARY	HEX		BINARY	HEX
A	11 000 001	C1	A	1 000 001	41	A	01 000 001	41	A	11 000 001	C1	A	11 000 001	C1	A	000 001	01	A	000 011	03	A	0 100 011	23	A	1 111 001	79	A	000 110	06	A	00 011	03
B	11 000 010	C2	B	1 000 010	42	B	01 000 010	42	B	11 000 010	C2	B	11 000 010	C2	B	000 010	02	B	011 001	19	B	0 010 011	13	B	1 110 110	76	B	000 111	07	B	11 001	19
C	11 000 011	C3	C	1 000 011	43	C	11 000 011	C3	C	01 000 011	43	C	11 000 011	C3	C	000 011	03	C	001 110	0E	C	1 110 011	73	C	1 111 010	7A	C	001 000	08	C	01 110	0E
D	11 000 100	C4	D	1 000 100	44	D	01 000 100	44	D	11 000 100	C4	D	11 000 100	C4	D	000 100	04	D	001 001	09	D	0 001 011	0B	D	0 101 010	2A	D	001 001	09	D	$ 01 001	09
E	11 000 101	C5	E	1 000 101	45	E	11 000 101	C5	E	01 000 101	45	E	11 000 101	C5	E	000 101	05	E	000 001	01	E	1 101 011	6B	E	1 001 010	4A	E	001 010	0A	E	3 00 001	01
F	11 000 110	C6	F	1 000 110	46	F	11 000 110	C6	F	01 000 110	46	F	11 000 110	C6	F	000 110	06	F	001 101	0D	F	1 011 011	5B	F	1 110 011	73	F	001 011	0B	F	! 01 101	0D
G	11 000 111	C7	G	1 000 111	47	G	01 000 111	47	G	11 000 111	C7	G	11 000 111	C7	G	000 111	07	G	011 010	1A	G	0 111 011	3B	G	0 100 011	23	G	001 100	0C	G	& 11 010	1A
H	11 001 000	C8	H	1 001 000	48	H	01 001 000	48	H	11 001 000	C8	H	11 001 000	C8	H	001 000	08	H	010 100	14	H	0 000 111	07	H	0 100 110	26	H	001 101	0D	H	= 10 100	14
I	11 001 001	C9	I	1 001 001	49	I	11 001 001	C9	I	01 001 001	49	I	11 001 001	C9	I	001 001	09	I	000 110	06	I	1 100 111	67	I	0 011 001	19	I	001 110	0E	I	8 00 110	06
J	11 001 010	CA	J	1 001 010	4A	J	11 001 010	CA	J	01 001 010	4A	J	11 010 001	D1	J	010 001	11	J	001 011	0B	J	1 100 011	63	J	1 000 011	43	J	001 111	0F	J	. 01 011	0B
K	11 001 011	CB	K	1 001 011	4B	K	01 001 011	4B	K	11 001 011	CB	K	11 010 010	D2	K	010 010	12	K	001 111	0F	K	1 010 001	51	K	0 011 010	1A	K	010 000	10	K	(01 111	0F
L	11 001 100	CC	L	1 001 100	4C	L	11 001 100	CC	L	01 001 100	4C	L	11 010 011	D3	L	010 011	13	L	010 010	12	L	0 110 001	31	L	1 000 110	46	L	010 001	11	L	) 10 010	12
M	11 001 101	CD	M	1 001 101	4D	M	01 001 101	4D	M	11 001 101	CD	M	11 010 100	D4	M	010 100	14	M	011 100	1C	M	1 001 001	49	M	1 100 001	61	M	010 010	12	M	. 11 100	1C
N	11 001 110	CE	N	1 001 110	4E	N	01 001 110	4E	N	11 001 110	CE	N	11 010 101	D5	N	010 101	15	N	001 100	0C	N	0 101 001	29	N	1 010 010	52	N	010 011	13	N	. 01 100	0C
O	11 001 111	CF	O	1 001 111	4F	O	01 001 111	CF	O	01 001 111	4F	O	11 010 110	D6	O	010 110	16	O	011 000	18	O	u 011 001	19	O	1 000 101	45	O	010 100	14	O	9 11 000	18
P	11 010 000	D0	P	1 010 000	50	P	01 010 000	50	P	11 010 000	D0	P	11 010 111	D7	P	010 111	17	P	010 110	16	P	1 111 001	79	P	0 001 011	0B	P	010 101	15	P	0 10 110	16
Q	11 010 001	D1	Q	1 010 001	51	Q	11 010 001	D1	Q	01 010 001	51	Q	11 011 000	D8	Q	011 000	18	Q	010 111	17	Q	1 000 101	45	Q	1 011 011	5B	Q	010 110	16	Q	1 10 111	17
R	11 010 010	D2	R	1 010 010	52	R	11 010 010	D2	R	01 010 010	52	R	11 011 001	D9	R	011 001	19	R	001 010	0A	R	0 101 001	29	R	0 101 001	29	R	010 111	17	R	4 01 010	0A
S	11 010 011	D3	S	1 010 011	53	S	01 010 011	53	S	11 010 011	D3	S	11 100 010	E2	S	100 010	22	S	000 101	05	S	1 010 010	52	S	0 100 101	25	S	011 000	18	S	Bell 00 101	05
T	11 010 100	D4	T	1 010 100	54	T	11 010 100	D4	T	01 010 100	54	T	11 100 011	E3	T	100 011	23	T	010 000	10	T	0 110 010	32	T	0 000 010	02	T	011 001	19	T	5 10 000	10
U	11 010 101	D5	U	1 010 101	55	U	01 010 101	55	U	11 010 101	D5	U	11 100 100	E4	U	100 100	24	U	000 111	07	U	1 001 010	4A	U	0 110 010	32	U	011 010	1A	U	7 00 111	07
V	11 010 110	D6	V	1 010 110	56	V	01 010 110	56	V	11 010 110	D6	V	11 100 101	E5	V	100 101	25	V	011 110	1E	V	0 101 010	2A	V	0 110 001	31	V	011 011	1B	V	; 11 110	1E
W	11 010 111	D7	W	1 010 111	57	W	01 010 111	57	W	11 010 111	D7	W	11 100 110	E6	W	100 110	26	W	010 011	13	W	0 011 010	1A	W	1 110 101	75	W	011 100	1C	W	2 10 011	13
X	11 011 000	D8	X	1 011 000	58	X	11 011 000	D8	X	01 011 000	58	X	11 100 111	E7	X	100 111	27	X	011 101	1D	X	1 111 010	7A	X	1 100 010	62	X	011 101	1D	X	/ 11 101	1D
Y	11 011 001	D9	Y	1 011 001	59	Y	01 011 001	59	Y	11 011 001	D9	Y	11 101 000	E8	Y	101 000	28	Y	010 101	15	Y	1 000 110	46	Y	1 100 111	67	Y	011 110	1E	Y	6 10 101	15
Z	11 011 010	DA	Z	1 011 010	5A	Z	01 011 010	5A	Z	11 011 010	DA	Z	11 101 001	E9	Z	101 001	29	Z	010 001	11	Z	0 100 110	26	Z	1 010 100	54	Z	011 111	1F	Z	" 10 001	11
a	11 100 001	E1	a	1 100 001	61	a	11 100 001	E1	a	01 100 001	61	a	10 000 001	81																			
b	11 100 010	E2	b	1 100 010	62	b	11 100 010	E2	b	01 100 010	62	b	10 000 010	82																	(NO LOWER CASE)		
c	11 100 011	E3	c	1 100 011	63	c	01 100 011	63	c	11 100 011	E3	c	10 000 011	83	(NO LOWER CASE)			CAPS = "SHIFT" LC = "UNSHIFT" UNSHIFT 011 111 1F SHIFT 011 011 1B			CAPS = "UC" LC = "LC" LC 00 011 111 1F UC 00 011 100 1C			CAPS = "UC" LC = "LC" LC 00 011 111 1F UC 00 011 100 1C			(NO LOWER CASE)			"LETTERS" 11 111 1F "FIGURES" 11 011 1B		
d	11 100 100	E4	d	1 100 100	64	d	11 100 100	E4	d	01 100 100	64	d	10 000 100	84																			
e	11 100 101	E5	e	1 100 101	65	e	01 100 101	65	e	11 100 101	E5	e	10 000 101	85																			
f	11 100 110	E6	f	1 100 110	66	f	01 100 110	66	f	11 100 110	E6	f	10 000 110	86																			
g	11 100 111	E7	g	1 100 111	67	g	11 100 111	E7	g	01 100 111	67	g	10 000 111	87																			
h	11 101 000	E8	h	1 101 000	68	h	11 101 000	E8	h	01 101 000	68	h	10 001 000	88																			
i	11 101 001	E9	i	1 101 001	69	i	01 101 001	69	i	11 101 001	E9	i	10 001 001	89																			
j	11 101 010	EA	j	1 101 010	6A	j	01 101 010	6A	j	11 101 010	EA	j	10 010 001	91																			
k	11 101 011	EB	k	1 101 011	6B	k	11 101 011	EB	k	01 101 011	6B	k	10 010 010	92																			
l	11 101 100	EC	l	1 101 100	6C	l	01 101 100	6C	l	11 101 100	EC	l	10 010 011	93																			
m	11 101 101	ED	m	1 101 101	6D	m	11 101 101	ED	m	01 101 101	6D	m	10 010 100	94																			
n	11 101 110	EE	n	1 101 110	6E	n	11 101 110	EE	n	01 101 110	6E	n	10 010 101	95																			
o	11 101 111	EF	o	1 101 111	6F	o	01 101 111	6F	o	11 101 111	EF	o	10 010 110	96																			
p	11 110 000	F0	p	1 110 000	70	p	11 110 000	F0	p	01 110 000	70	p	10 010 111	97																			
q	11 110 001	F1	q	1 110 001	71	q	01 110 001	71	q	11 110 001	F1	q	10 011 000	98																			
r	11 110 010	F2	r	1 110 010	72	r	01 110 010	72	r	11 110 010	F2	r	10 011 001	99																			
s	11 110 011	F3	s	1 110 011	73	s	01 110 011	F3	s	11 110 011	F3	s	01 110 011	73																			
t	11 110 100	F4	t	1 110 100	74	t	01 110 100	74	t	11 110 100	F4	t	11 110 100	F4	t	10 100 011	A3																
u	11 110 101	F5	u	1 110 101	75	u	11 110 101	F5	u	01 110 101	75	u	10 100 100	A4							UPPER CASE (U) LOWER CASE (L) EITHER (*)			UPPER CASE (U) LOWER CASE (L) EITHER (*)								
v	11 110 110	F6	v	1 110 110	76	v	11 110 110	F6	v	01 110 110	76	v	10 100 101	A5																			
w	11 110 111	F7	w	1 110 111	77	w	01 110 111	77	w	11 110 111	F7	w	10 100 110	A6																			
x	11 111 000	F8	x	1 111 000	78	x	01 111 000	78	x	11 111 000	F8	x	10 100 111	A7																			
y	11 111 001	F9	y	1 111 001	79	y	11 111 001	F9	y	01 111 001	79	y	10 101 000	A8																			
z	11 111 010	FA	z	1 111 010	7A	z	11 111 010	FA	z	01 111 010	7A	z	10 101 001	A9																			
0	10 110 000	B0	0	0 110 000	30	0	00 110 000	30	0	10 110 000	B0	0	11 110 000	F0	0	110 000	30	0	110 110 U	36	0	01 010 100 L	54	0	01 100 100 L	64	0	110 000	30	0	10 110 F	16
1	10 110 001	B1	1	0 110 001	31	1	10 110 001	B1	1	00 110 001	31	1	11 110 001	F1	1	110 001	31	1	111 101 U	3D	1	00 100 000 L	20	1	00 100 000 L	20	1	110 001	31	1	10 111 F	17
2	10 110 010	B2	2	0 110 010	32	2	10 110 010	B2	2	00 110 010	32	2	11 110 010	F2	2	110 010	32	2	110 011 U	33	2	00 010 000 L	10	2	00 010 000 L	10	2	110 010	32	2	10 011 F	13
3	10 110 011	B3	3	0 110 011	33	3	00 110 011	33	3	10 110 011	B3	3	11 110 011	F3	3	110 011	33	3	100 001 U	21	3	00 110 000 L	30	3	01 110 000 L	70	3	110 011	33	3	00 001 F	01
4	10 110 100	B4	4	0 110 100	34	4	10 110 100	B4	4	00 110 100	34	4	11 110 100	F4	4	110 100	34	4	101 010 U	2A	4	00 001 000 L	08	4	00 000 100 L	04	4	110 100	34	4	01 010 F	0A
5	10 110 101	B5	5	0 110 101	35	5	00 110 101	35	5	10 110 101	B5	5	11 110 101	F5	5	110 101	35	5	110 000 U	30	5	01 001 000 L	48	5	00 001 000 L	08	5	110 101	35	5	10 000 F	10
6	10 110 110	B6	6	0 110 110	36	6	00 110 110	36	6	10 110 110	B6	6	11 110 110	F6	6	110 110	36	6	110 101 U	35	6	01 011 000 L	58	6	01 011 000 L	58	6	110 110	36	6	10 101 F	15
7	10 110 111	B7	7	0 110 111	37	7	10 110 111	B7	7	00 110 111	37	7	11 110 111	F7	7	110 111	37	7	100 111 U	27	7	00 111 000 L	38	7	01 101 000 L	68	7	110 111	37	7	00 111 F	07
8	10 111 000	B8	8	0 111 000	38	8	10 111 000	B8	8	00 111 000	38	8	11 111 000	F8	8	111 000	38	8	100 110 U	26	8	00 000 100 L	04	8	00 111 000 L	38	8	111 000	38	8	11 010 F	1A
9	10 111 001	B9	9	0 111 001	39	9	00 111 001	39	9	10 111 001	B9	9	11 111 001	F9	9	111 001	39	9	111 000 U	38	9	01 100 100 L	64	9	00 110 100 L	34	9	111 001	39	9	11 000 F	18
SP	10 100 000	A0	SP	0 100 000	20	SP	10 100 000	A0	SP	00 100 000	20	SP	01 000 000	40	SP	011 010	1A	SP	000 100 S/U	04	SP	01 000 000 -	40	SP	01 000 000 -	40	SP	000 101	05	SP	00 100	04
!	10 100 001	A1	!	0 100 001	21	!	00 100 001	A1	!	10 100 001	A1	!	01 011 010	5A	!			!	100 011 S	23	!	01 110 101 U	75	!	60 000 001 L	01	!	101 101	2D	!	01 101 F	0D
"	10 100 010	A2	"	0 100 010	22	"	00 100 010	22	"	10 100 010	A2	"	01 111 111	7F				'			'	00 110 100 U	34	"	01 001 001 U	49	"			"	10 001 F	11
#	10 100 011	A3	#	0 100 011	A3	#	00 100 011	23	#	00 100 011	23	#	01 111 011	7B	=	111 011	3B				=	00 110 000 U	70	=	01 110 000 U	70	=	100 110	26	=	10 100 F	14
$	10 100 100	A4	$	0 100 100	24	$	00 100 100	24	$	10 100 100	A4	$	01 011 011	5B	$	011 011	1B	$	100 011 U	23	$	01 110 101 L	75	$	00 000 100 U	04	$	100 111	27	$	01 001 F	09
%	10 100 101	A5	%	0 100 101	25	%	10 100 101	A5	%	00 100 101	25	%	01 101 100	6C	%	101 100	2C				%	01 101 000 U	68	%	00 001 000 U	08	%	101 010	2A			
&	10 100 110	A6	&	0 100 110	26	&	10 100 110	A6	&	00 100 110	26	&	01 010 000	50	&	010 000	10	&	111 000 S	38	&	01 001 011 L	43	&	01 101 000 U	68	&	000 001	01			
'	10 100 111	A7	'	0 100 111	27	'	00 100 111	27	'	10 100 111	A7	'	01 111 101	7D				'			'	01 011 000 U	58	'	01 001 001 L	49		111 010	3A	'	01 011 F	0B
(	10 101 000	A8	(	0 101 000	28	(	00 101 000	28	(	10 101 000	A8	(	01 001 101	4D				(	110 001 S	31	(	01 100 100 U	64	(	00 110 100 U	34	:	101 001	29	(	01 111 F	0F
)	10 101 001	A9	)	0 101 001	29	)	10 101 001	A9	)	00 101 001	29	)	01 011 101	5D				)	110 001 U	31	)	00 100 100 U	54	)	01 100 100 U	64	)	100 000	20	)	10 010 F	12
*	10 101 010	AA	*	0 101 010	2A	*	10 101 010	AA	*	00 101 010	2A	*	01 011 100	5C	*	011 100	1C				*	00 000 100 U	04	*	00 111 000 U	38	*	101 000	28			
+	10 101 011	AB	+	0 101 011	2B	+	00 101 011	2B	+	10 101 011	AB	+	01 001 110	4E							+	01 000 011 U	43	+	00 010 011 U	13	,	100 001	22			
,	10 101 100	AC	,	0 101 100	2C	,	10 101 100	AC	,	00 101 100	2C	,	01 101 011	6B		101 011	2B				,	01 110 110 L	76	,	00 111 011 *	3B	.	101 110	2E	,	01 100 F	0C
.	10 101 101	AD	.	0 101 101	2D	.	00 101 101	2D	.	10 101 101	AD	.	01 000 000	60		100 000	20		101 001 U	29	.	00 111 111 L	37	.	00 110 111 L	37	-	100 001	21	.	00 011 F	03
/	10 101 110	AE	/	0 101 110	2E	/	00 101 110	2E	/	10 101 110	AE	/	01 001 011	4B		001 011	0B		111 100 S/U	3C	/	00 110 111 L	37	/	01 010 001 *	51	/	111 101	3D	/	11 100 F	1C
	10 101 111	AF		0 101 111	2F		10 101 111	AF		00 101 111	2F		01 100 001	61		100 001	21					01 100 010 L	62		00 000 111 L	07		111 100	3C		11 101 F	1D

8-BIT ASCII			7-BIT ASCII			EVEN PARITY ASCII			ODD PARITY ASCII			EBCDIC			6-BIT TRANSCODE			6-BIT TYPESETTER			EBCD			SELECTRIC			FIELD DATA			BAUDOT		
	BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY C 12 4 8 A 8		HEX		BINARY C 12 4 8 A 8		HEX		BINARY	HEX		BINARY	HEX
:	10 111 010	BA	:	0 111 010	3A	:	00 111 010	3A	:	10 111 010	BA	:	01 111 010	7A				:	111 010	S	3A	:	00 001 000	U	08	:	01 101 011	U	0B	:	101 011	2B	:	01 110	F	0E
;	10 111 011	BB	;	0 111 011	3B	;	10 111 011	BB	;	00 111 011	3B	;	01 011 110	5E				;	111 010	U	3A	;	00 110 000	U	30	;	01 101 011	L	0B	;	111 011	3B	;	11 110	F	1E
<	10 111 100	BC	<	0 111 100	3C	<	00 111 100	3C	<	10 111 100	BC	<	01 001 100	4C	<	001 100	0C					<	00 010 000	U	10					<	100 011	23				
=	10 111 101	BD	=	0 111 101	3D	=	10 111 101	BD	=	00 111 101	3D	=	01 111 110	7E								=	00 100 000	U	20	=	00 010 011	L	13	=	100 100	24				
>	10 111 110	BE	>	0 111 110	3E	>	10 111 110	BE	>	00 111 110	3E	>	01 101 110	6E								>	00 111 000	U	38					>	100 101	25				
?	10 111 111	BF	?	0 111 111	3F	?	00 111 111	3F	?	10 111 111	BF	?	01 101 111	6F				?	110 110	S	36	?	01 100 010	U	62	?	00 000 111	U	07	?	101 100	2C	?	11 001	F	19
@	11 000 000	C0	@	1 000 000	40	@	11 000 000	C0	@	01 000 000	40	@	01 111 100	7C	@	111 100	3C	@	101 001	S	29	@	00 000 010	L	02	@	00 010 000	U	10	@	101 111	2F				
[	11 011 011	DB	[	1 011 011	5B	[	11 011 011	DB	[	01 011 011	5B														[	00 100 000	U	20	[	000 011	03				
\	11 011 100	DC	\	1 011 100	5C	\	01 011 100	5C	\	11 011 100	DC	\	11 100 000	E0																				
]	11 011 101	DD	]	1 011 101	5D	]	11 011 101	DD	]	01 011 101	5D														]	00 100 000	L	20	]	000 100	04				
^	11 011 110	DE	^	1 011 110	5E	^	11 011 110	DE	^	01 011 110	5E																		^	000 010	02				
_	11 011 111	DF	_	1 011 111	5F	_	01 011 111	5F	_	11 011 111	DF	_	01 101 101	6D											_	00 110 111	U	37							
`			`	1 100 000	60	`	01 100 000	60	`	11 100 000	E0	`	01 111 001	79																				
|	11 111 011	FB	|	1 111 011	7B	|	01 111 011	7B	|	11 111 011	FB	|	11 000 000	C0																				
:	11 111 100	FC	:	1 111 100	7C	:	11 111 100	FC	:	01 111 100	7C	:	01 101 010	6A																				
}	11 111 101	FD	}	1 111 101	7D	}	01 111 101	7D	}	11 111 101	FD	}	11 010 000	D0																				
~	11 111 110	FE	~	1 111 110	7E	~	01 111 101	7E	~	11 111 110	FE	~	10 100 001	A1																				
												¢	01 001 010	4A								¢	00 000 010	U	02	¢	01 011 000	U	58						
¬												¬	01 011 111	5F								¬	00 110 111	U	37										
|												|	01 001 111	4F								|	01 110 110	U	76										
																									±	00 100 000	U	20							
																										00 000 001	U	01							
ACK	10 000 110	86	ACK	0 000 110	06	ACK	00 000 110	06	ACK	10 000 110	86	ACK	00 101 110	2E																				
BEL	10 000 111	87	BEL	0 000 111	07	BEL	10 000 111	07	BEL	00 000 111	07	BEL	00 101 111	2F	BEL	001 101	0D	BEL	101 011		2B													
BS	10 001 000	88	BS	0 001 000	08	BS	10 001 000	08	BS	00 001 000	08	BS	00 010 110	16								BS	01 011 101		5D	BS	01 011 101		5D						
												BYP	00 100 100	24								BYP	00 001 110		0E	BY	00 001 110		0E						
CAN	10 011 000	98	CAN	0 011 000	18	CAN	00 011 000	18	CAN	10 011 000	98	CAN	00 011 000	18																				
												CC	00 011 010	1A																				
CR	10 001 101	8D	CR	0 001 101	0D	CR	10 001 101	8D	CR	00 001 101	0D	CR	00 001 101	0D				RET	001 000		08								CR	111 111	3F	CR	01 000		08
DC1	10 010 001	91	DC1	0 010 001	11	DC1	00 010 001	11	DC1	10 001 001	91	DC1	00 010 001	11																				
DC2	10 010 010	92	DC2	0 010 010	12	DC2	00 010 010	12	DC2	10 010 010	92	DC2	00 010 010	12																				
DC3	10 010 011	93	DC3	0 010 011	13	DC3	10 010 011	93	DC3	00 010 011	13	DC3	00 010 011	13																				
DC4	10 010 100	94	DC4	0 010 100	14	DC4	00 010 100	14	DC4	10 010 100	94	DC4	00 011 100	3C																				
DEL	11 111 111	FF	DEL	1 111 111	7F	DEL	11 111 111	FF	DEL	01 111 111	7F	DEL	00 000 111	07	DEL	111 111	3F	RUBOUT	111 111		3F	DEL	01 111 111		7F	DEL	01 111 111		7F						
DLE	10 010 000	90	DLE	0 010 000	10	DLE	10 010 000	90	DLE	00 010 000	10	DLE	00 010 000	10	DLE	011 111	1F																	
												DS	00 100 000	20				ELEVATE	000 010		02													
EM	10 011 001	99	EM	0 011 001	19	EM	10 011 001	99	EM	00 011 001	19	EM	00 011 001	19	EM	111 110	3E	THIN SP	100 000		20													
ENQ	10 000 101	85	ENQ	0 000 101	05	ENQ	00 000 101	05	ENQ	10 000 101	85	ENQ	00 101 101	2D	ENQ	101 101	2D	ADD TH SP	100 100		24													
												EOB	00 100 110	26				EM SP	100 101		25	EOB	01 011 110		5E	EOB	01 011 110		5E						
EOT	10 000 100	84	EOT	0 000 100	04	EOT	10 000 100	84	EOT	00 000 100	04	EOT	00 110 111	37	EOT	011 110	1E	EN SP	101 110		2E	EOT	01 111 100		7C	EOT	01 111 100		7C						
ESC	10 011 011	9B	ESC	0 011 011	1B	ESC	00 011 011	1B	ESC	10 011 011	9B	ESC	00 100 111	27	ESC	101 010	2A	QR	101 111		2F													
ETB	10 010 111	97	ETB	0 010 111	17	ETB	00 010 111	17	ETB	10 010 111	97	ETB	00 100 110	26	ETB	001 111	0F	V RULE	110 010		32													
ETX	10 000 011	83	ETX	0 000 011	03	ETX	00 000 011	03	ETX	10 000 011	83	ETX	00 000 011	03	ETX	101 110	2E	EM LEAD	110 100		34													
FF	10 001 100	8C	FF	0 001 100	0C	FF	00 001 100	0C	FF	10 001 100	8C	FF	00 001 100	0C				EN LEAD	110 111		37								FF	111 110	3E				
FS	10 011 100	9C	FS	0 011 100	1C	FS	10 011 100	9C	FS	00 011 100	1C	FS	00 100 010	22				U RAIL	111 001		39													
GS	10 011 101	9D	GS	0 011 101	1D	GS	00 011 101	1D	GS	10 011 101	9D							L RAIL	111 011		3B													
HT	10 001 001	89	HT	0 001 001	09	HT	00 001 001	09	HT	10 001 001	89	HT	00 000 101	05	HT	101 111	2F	Q CENT	111 110		3E	HT	00 101 111		2F	HT	00 101 111		2F						
												IFS	00 011 100	1C																				
												IGS	00 011 101	1D																				
												IL	00 010 111	17								IL	00 111 101		3D	IL	00 111 101		3D						
												IRS	00 011 110	1E																				
												IUS	00 011 111	1F																				
												LC	00 000 110	06								LC	00 011 111		1F	LC	00 011 111		1F						
LF	10 001 010	8A	LF	0 001 010	0A	LF	00 001 010	0A	LF	10 001 010	8A	LF	00 100 101	25								LF	01 101 110		6E	LF	01 101 110		6E				LF	00 010		02
NAK	10 010 101	95	NAK	0 010 101	15	NAK	10 010 101	95	NAK	00 010 101	15	NAK	00 111 101	3D	NAK	111 101	3D																	
												NL	00 010 101	15								NL	01 101 101		6D	NL	01 101 101		6D						
NUL	10 000 000	80	NUL	0 000 000	00	NUL	00 000 000	00	NUL	10 000 000	80	NUL	00 000 000	00															PER	111 101	3D				
												PF	00 000 100	04				PF	100 010		22	PF	01 001 111		4F	PF	01 001 111		4F						
												PN	00 110 100	34								PN	01 001 100		4C	PN	01 001 100		4C						
												PRE	00 100 111	27								PRE	00 111 110		3E	PRE	00 111 110		3E						
												RES	00 010 100	14								RES	00 001 101		0D	RES	00 001 101		0D						
												RLF	00 001 001	09																				
RS	10 011 110	9E	RS	0 011 110	1E	RS	00 011 110	1E	RS	10 011 110	9E	RS	00 110 101	35								RS	00 101 100		2C	RS	00 101 100		2C						
SI	10 001 111	8F	SI	0 001 111	0F	SI	00 001 111	0F	SI	10 001 111	8F	SI	00 001 111	0F																				
												SM	00 101 010	2A																				
												SMM	00 001 010	0A																				
SO	10 001 110	8E	SO	0 001 110	0E	SO	00 001 110	0E	SO	10 001 110	8E	SO	00 001 110	0E																				
SOH	10 000 001	81	SOH	0 000 001	01	SOH	00 000 001	01	SOH	10 000 001	81	SOH	00 000 001	01	SOH	000 000	00																	
												SOS	00 100 001	21																				
STX	10 000 010	82	STX	0 000 010	02	STX	00 000 010	02	STX	10 000 010	82	STX	00 000 010	02	STX	001 010	0A																	
SUB	10 011 010	9A	SUB	0 011 010	1A	SUB	00 011 010	1A	SUB	10 011 010	9A	SUB	00 111 111	3F	SUB	001 110	0E																	
SYN	10 010 110	96	SYN	0 010 110	16	SYN	00 010 110	16	SYN	10 010 110	96	SYN	00 110 010	32	SYN	111 010	3A																	
												UC	00 110 110	36								UC	00 011 100		1C	UC	00 011 100		1C						
US	10 011 111	9F	US	0 011 111	1F	US	00 011 111	1F	US	10 011 111	9F				US	011 101	1D																	
VT	10 001 011	8B	VT	0 001 011	0B	VT	00 001 011	0B	VT	10 001 011	8B	VT	00 001 011	0B																				

UPPER CASE (U)
LOWER CASE (L)
EITHER (*)

UNSHIFT 011 111 1F
SHIFT 011 011 1B

UC 00 011 100 1C
LC 00 011 111 1F

FIGS 11 011 1B
LTRS 11 111 1F

HEX TO CHARACTER CODE FOR DATA COMMUNICATIONS

EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	7-BIT ASCII	EBCD UC	EBCD LC	SELECTRIC UC	SELECTRIC LC	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	7-BIT ASCII	EBCD UC	EBCD LC	SELECTRIC UC	SELECTRIC LC
00 NUL	NUL		00 NUL					40 SP		@	40 @	SP		SP	
01 SOH		SOH	01 SOH			O	!	41	A		41 A				
02 STX		STX	02 STX	¢	@	T	t	42	B		42 B				
03 ETX	ETX		03 ETX					43		C	43 C	+	&	J	j
04 PF		EOT	04 EOT	•	8	$	4	44	D		44 D				
05 HT	ENQ		05 ENQ					45		E	45 E	Q	q	O	o
06 LC	ACK		06 ACK					46		F	46 F	Y	y	L	l
07 DEL		BEL	07 BEL	H	h	?	1	47	G		47 G				
08		BS	08 BS	:	4	%	5	48	H		48 H				
09 RLF	HT		09 HT					49		I	49 I	M	m		
0A SMM	LF		0A LF					4A ¢		J	4A J			E	e
0B VT		VT	0B VT	D	d	P	p	4B •	K		4B K	U	u		
0C FF	FF		0C FF					4C <		L	4C L	PN		PN	
0D CR		CR	0D CR	RES		RES		4D (	M		4D M				
0E SO		SO	0E SO	BYP		BY		4E +	N		4E N				
0F SI	SI		0F SI					4F !		O	4F O	PF		PF	
10 DLE		DLE	10 DLE	<	2	@	2	50 &	P		50 P				
11 DC1	DC1		11 DC1					51		Q	51 Q	K	k	•	•
12 DC2	DC2		12 DC2					52		R	52 R	S	s	N	n
13 DC3		DC3	13 DC3	B	b	+	=	53	S		53 S				
14 RES	DC4		14 DC4					54		T	54 T	)	0	Z	z
15 NL		NAK	15 NAK					55	U		55 U				
16 BS		SYN	16 SYN					56	V		56 V				
17 IL	ETB		17 ETB					57		W	57 W				
18 CAN	CAN		18 CAN					58		X	58 X		6	¢	6
19 EM		Em	19 EM	O	o	I	i	59	Y		59 Y				
1A CC		SUB	1A SUB	W	w	K	k	5A !	Z		5A Z				
1B	ESC		1B ESC					5B $		[	5B [	F	f	Q	q
1C IFS		FS	1C FS	UPPER CASE		UPPER CASE		5C *	\	\	5C \				
1D IGS	GS		1D GS					5D)		]	5D]	BS		BS	
1E IRS	RS		1E RS					5E ;		^	5E ^	EOB		EOB	
1F IUS		US	1F US	LOWER CASE		LOWER CASE		5F ¬	—		5F —				
20 DS		SP	20 SP	=	1	[:]	1	60 -	`		60 `				
21 SOS	!		21 !					61 /		a	61 a	J	j	M	m
22 FS	"		22 "					62		b	62 b	?	/	X	x
23		=	23 =	A	a	G	g	63	c		63 c				
24 BYP	$		24 $					64		d	64 d	(	9	)	0
25 LF		%	25 %	R	r	S	s	65	e		65 e				
26 EOB/ETB		&	26 &	Z	z	H	h	66	f		66 f				
27 ESC/PRE			27 '					67		g	67 g	I	i	Y	y
28	(		28 (					68		h	68 h	%	5	&	7
29		)	29)	N	n	R	r	69	i		69 i				
2A SM		*	2A *	V	v	D	d	6A ¦	j		6A j				
2B	+		2B +					6B .		k	6B k	E	e	:	;
2C			2C ,	RS		RS		6C %	l		6C l				
2D ENQ	—		2D —					6D —		m	6D m	NL		NL	
2E ACK			2E					6E >		n	6E n	LF		LF	
2F BEL		/	2F /	HT		HT		6F ?	o		6F o				
30	0		30 0	;	3			70		p	70 p			=	3
31		1	31 1	L	l	V	v	71	q		71 q				
32 SYN		2	32 2	T	t	U	u	72	r		72 r				
33	3		33 3					73		s	73 s	C	c	F	f
34 PN		4	34 4	"	#	(	9	74	t		74 t				
35 RS	5		35 5					75		u	75 u	!	$	W	w
36 UC	6		36 6					76		v	76 v	'	.	B	b
37 EOT		7	37 7	¬		—	-	77	w		77 w				
38		8	38 8	>	7	*	8	78	x		78 x				
39	9		39 9					79 \		y	79 y	P	p	A	a
3A	:		3A :					7A :		z	7A z	X	x	C	c
3B		;	3B ;	G	g			7B =	{		7B {				
3C DC4	<		3C <					7C @			7C	EOT		EOT	
3D NAK		=	3D =	IL		IL		7D '	}		7D }				
3E		>	3E >	PRE		PRE		7E =	~		7E ~				
3F SUB	?		3F ?					7F "		DEL	7F DEL	DEL		DEL	

EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	8-BIT ASCII	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	8-BIT ASCII		FIELD DATA	6-BIT TYPESETTER SHIFT	6-BIT TYPESETTER UNSHIFT	6-BIT TRANSCODE	BAUDOT LTRS	BAUDOT FIGS
80		NUL	NUL	C0 {	@		@		00			SOH		
81 a	SOH		SOH	C1 A		A	A		01 &	E	e	A	E	3
82 b	STX		STX	C2 B		B	B		02 ^	ELEVATE		B	LF	
83 c		ETX	ETX	C3 C	C		C		03 [	A	a	C	A	
84 d	EOT		EOT	C4 D		D	D		04]	SPACE		D	SP	
85 e		ENQ	ENQ	C5 E	E		E		05 SP	S	s	E	S	BEL
86 f		ACK	ACK	C6 F	F		F		06 A	I	i	F	I	8
87 g	BEL		BEL	C7 G		G	G		07 B	U	u	G	U	7
88 h	BS		BS	C8 H		H	H		08 C	RETURN		H	CR	
89 i		HT	HT	C9 I	I		I		09 D	D	d	I	D	$
8A		LF	LF	CA	J		J		0A E	R	r	STX	R	4
8B	VT		VT	CB		K	K		0B F	J	j	.	J	'
8C		FF	FF	CC	L		L		0C G	N	n	<	N	,
8D	CR		CR	CD		M	M		0D H	F	f	BELL	F	!
8E	SO		SO	CE		N	N		0E I	C	c	SUB	C	:
8F		SI	SI	CF	O		O		0F J	K	k	ETB	K	(
90	DLE		DLE	D0 }		P	P		10 K	T	t	&	T	5
91 j		DC1	DC1	D1 J	Q		Q		11 L	Z	z	J	Z	"
92 k		DC2	DC2	D2 K	R		R		12 M	L	l	K	L	)
93 l	DC3		DC3	D3 L		S	S		13 N	W	w	L	W	2
94 m		DC4	DC4	D4 M	T		T		14 O	H	h	M	H	#
95 n	NAK		NAK	D5 N		U	U		15 P	Y	y	N	Y	6
96 o	SYN		SYN	D6 O		V	V		16 Q	P	p	O	P	0
97 p		ETB	ETB	D7 P	W		W		17 R	Q	q	P	Q	1
98 q		CAN	CAN	D8 Q	X		X		18 S	O	o	Q	O	9
99 r	EM		EM	D9 R		Y	Y		19 T	B	b	R	B	?
9A	SUB		SUB	DA		Z	Z		1A U	G	g	SPACE	G	8
9B		ESC	ESC	DB	[		[		1B V	SHIFT		$	FIGS	
9C	FS		FS	DC	\		\		1C W	M	m	%	M	.
9D		GS	GS	DD	]		]		1D X	X	x	US	X	/
9E		RS	RS	DE	^		^		1E Y	V	v	EOT	V	;
9F	US		US	DF			–		1F Z	UNSHIFT		DLE	LTRS	
A0	SP		SP	E0 \					20)	THIN SPACE		–		
A1 ~		!	!	E1	a		a		21 –		3	/		
A2 s		"	"	E2 S	b		b		22 +	PF		S		
A3 t	=		=	E3 T		c	c		23 <	!	$	T		
A4 u		$	$	E4 U	d		d		24 =	ADD THIN SPACE		U		
A5 v	%		%	E5 V		e	e		25 >	EM SPACE		V		
A6 w	&		&	E6 W		f	f		26 #		8	W		
A7 x	'		'	E7 X	g		g		27 $		7	X		
A8 y		(	(	E8 Y	h		h		28 *	∨	∨	Y		
A9 z	)		)	E9 Z		i	i		29 (	@	–	Z		
AA	*		*	EA		j	j		2A %		4	ESC		
AB		+	+	EB	k		k		2B :	BELL		.		
AC	,		,	EC		l	l		2C ?			%		
AD		–	–	ED	m		m		2D !	.	.	ENQ		
AE	.		.	EE	n		n		2E .	EN SPACE		ETX		
AF	/		/	EF		o	o		2F @	QR		HT		
B0		0	0	F0 0	p		p		30 0		5	0		
B1	1		1	F1 1		q	q		31 1	(	)	1		
B2	2		2	F2 2	r		r		32 2	V RULE		2		
B3		3	3	F3 3	s		s		33 3		2	3		
B4	4		4	F4 4		t	t		34 4	EM LEADER		4		
B5		5	5	F5 5	u		u		35 5		6	5		
B6		6	6	F6 6	v		v		36 6	?	0	6		
B7	7		7	F7 7		w	w		37 7	EN LEADER		7		
B8	8		8	F8 8	x		x		38 8	&	9	8		
B9		9	9	F9 9	y		y		39 9	UPPER RAIL		9		
BA		:	:	FA	z		z		3A '	:	;	SYN		
BB	;		;	FB		{	{		3B ;	LOWER RAIL		#		
BC		<	<	FC	!		!		3C /	.	.	@		
BD	=		=	FD		}	}		3D .		1	NAK		
BE	>		>	FE		~	~		3E FF	QUAD CENTER		EM		
BF		?	?	FF	DEL		DEL		3F CR	RUBOUT		DEL		

APPENDIX E

DATA COMPRESSION

This appendix contains a series of listings - one code for Code Types 1 through 6 - showing the character set, the hex code for each character, and the code length in bits after compression. (See Tables E1 through E6.) Values are given for the entropy for the character set, and for the character set plus idle and control characters. Entropy is the theoretical minimum average number of bits required to represent the entire character set.

TABLE E-1. CODE TYPE 1 CODE TABLE

BSC EBCDIC

Character	Hex Code	Length, Bits
IDLE	100	6
FF	FF	8
FE	FE	8
FD	FD	8
FC	FC	8
Fb	FB	8
FA	FA	8
9	F9	8
8	F8	8
7	F7	8
6	F6	8
5	F5	8
4	F4	8
3	F3	8
2	F2	8
1	F1	8
0	F0	8
EF	EF	8
EE	EE	8
ED	ED	8
EC	EC	8
EB	EB	8
EA	EA	8
Z	E9	8
Y	E8	8
X	E7	8
Q	E6	8
V	E5	8
U	E4	8
T	E3	8
S	E2	8
E1	E1	8
\	E0	8
DF	DF	8
DE	DE	8
DD	DD	8
DC	DC	8
DB	DB	8

Character	Hex Code	Length, Bits
DA	DA	8
R	D9	8
Q	D8	8
P	D7	8
O	D6	8
N	D5	8
M	D4	8
L	D3	8
K	D2	8
J	D1	8
}	D0	8
CF	CF	8
CE	CE	8
CD	CD	8
CC	CC	8
CB	CB	8
CA	CA	8
I	C9	8
H	C8	8
G	C7	8
F	C6	8
E	C5	8
D	C4	8
C	C3	8
B	C2	8
A	C1	8
{	C0	8
BF	BF	8
B9	69	8
B8	68	8
B7	67	8
B6	66	8
B5	67	8
B4	64	8
B3	63	8
B2	62	8
B1	61	8
B0	60	8
z	A9	8

TABLE E-1. CODE TYPE 1 CODE TABLE (Cont)

BSC EBCDIC

Character	Hex Code	Length, Bits
y	A8	8
x	A7	8
w	A6	8
v	A5	8
u	A4	8
t	A3	8
s	A2	8
-	A1	8
A0	A0	8
r	99	8
q	98	8
p	97	8
o	96	8
n	95	8
m	94	8
L	93	8
k	92	8
j	91	8
90	90	8
8F	8F	8
8E	8E	8
8D	8D	8
8C	8C	8
8B	8B	8
8A	8A	8
i	89	8
h	88	8
g	87	8
f	86	8
e	85	8
d	84	8
c	83	8
b	82	8
a	81	8
80	80	8
"	7F	8
=	7E	8
'	7D	8
@	7C	8

Character	Hex Code	Length, Bits
#	7B	8
:	7A	8
\	79	8
78	78	8
77	77	8
76	76	8
75	75	8
74	74	8
73	73	8
72	72	8
71	71	8
70	70	8
?	6F	8
>	6E	8
_	6D	8
%	6C	8
,	6B	8
|	6A	8
69	69	8
68	68	8
67	67	8
66	66	8
65	65	8
64	64	8
63	63	8
62	62	8
61	61	8
-	60	8
NOT	5F	8
;	5E	8
)	5D	8
*	5C	8
$	5B	8
!	5A	8
59	59	8
58	58	8
57	57	8
56	56	8
55	55	8

TABLE E-1. CODE TYPE 1 CODE TABLE (Cont)

BSC EBCDIC

Character	Hex Code	Length, Bits
54	54	8
53	53	8
52	52	8
51	51	8
&	50	8
}	4F	8
+	4E	8
(	4D	8
<	4C	8
.	4B	8
CENT	4A	8
49	49	8
48	48	8
47	47	8
46	46	8
45	45	8
44	44	8
43	43	8
42	42	8
41	41	8
SP	40	8
SUB	3F	8
3E	3E	8
NAK	3D	8
DC4	3C	8
3B	3B	8
3A	3A	8
39	39	8
38	38	8
EOT	37	8
UC	36	8
RS	35	8
PN	34	8
33	33	8
SYN	32	8
31	31	8
30	30	8
BEL	2F	8
ACK	2E	8

Character	Hex Code	Length, Bits
ENQ	2D	8
2C	2C	8
2B	2B	8
SM	2A	8
29	29	8
28	28	8
PRE	27	8
EOB	26	8
LF	25	8
BYP	24	8
23	23	8
FS	22	8
SOS	21	8
DS	20	8
IUS	1F	8
IRS	1E	8
IGS	1D	8
IFS	1C	8
1B	1B	8
CC	1A	8
E"	19	8
CAN	18	8
IL	17	8
HS	16	8
NL	15	8
RES	14	8
DC3	13	8
DC2	12	8
DC1	11	8
DLE	10	8
SI	F	8
SO	E	8
CR	D	8
FF	C	8
VT	B	8
SMM	A	8
RLF	9	8
08	8	8
DEL	7	8

TABLE E-1. CODE TYPE 1 CODE TABLE (Cont)

BSC EBCDIC

Character	Hex Code	Length, Bits
LC	6	8
HT	5	8
PF	4	8
ETX	3	8
STX	2	8
SOH	1	8
NUL	0	8
BE	BE	9
BD	BD	9
BC	BC	9
BB	BB	9
BA	BA	9
AF	AF	9
AE	AE	9
AD	AD	9

Character	Hex Code	Length, Bits
AC	AC	9
AB	AB	9
9F	9F	9
9E	9E	9
9D	9D	9
9C	9C	9
9B	9B	9
9A	9A	9
AA	AA	9
GRB		9
/BRK		9
BRK		9
/RNG		9
RNG		9
/CAR		9
CAR		9
/DSR		9
DSR		9

ENTROPY = 8.0

WITH IDLE AND CONTROL CHARACTERS:

ENTROPY = 8.022
COMPRESSION RATIO = -0.83

AVERAGE CODE LENGTH = 8.07

TABLE E-2. CODE TYPE 2 CODE TABLE

BSC ASCII

Character	Hex Code	Length, Bits
IDLE	80	2
z	7A	7
y	79	7
x	78	7
w	77	7
v	76	7
u	75	7
t	74	7
s	73	7
r	72	7
q	71	7
p	70	7
o	6F	7
n	6E	7
m	6D	7
L	6C	7
k	6B	7
j	6A	7
i	69	7
h	68	7
g	67	7
f	66	7
e	65	7
d	64	7
c	63	7
b	62	7
a	61	7
Y	59	7
X	58	7
V	56	7
U	55	7
T	54	7
S	53	7
R	52	7
P	50	7
O	4F	7
N	4E	7
M	4D	7

Character	Hex Code	Length, Bits
L	4C	7
K	4B	7
J	4A	7
I	49	7
H	48	7
G	47	7
F	46	7
E	45	7
D	44	7
C	43	7
B	42	7
A	41	7
@	40	7
?	3F	7
=	3D	7
;	3B	7
:	3A	7
9	39	7
8	38	7
7	37	7
6	36	7
5	35	7
4	34	7
3	33	7
2	32	7
1	31	7
0	30	7
/	2F	7
.	2E	7
-	2D	7
,	2C	7
+	2B	7
*	2A	7
)	29	7
(	28	7
'	27	7
&	26	7
%	25	7
$	24	7

TABLE E-2. CODE TYPE 2 CODE TABLE (Cont)

BSC ASCII

Character	Hex Code	Length, Bits
#	23	7
"	22	7
!	21	7
SP	20	7
CR	D	7
LF	A	7
Z	5A	8
<	3C	9
-	7E	9
}	7D	9
W	57	9
|	7C	9
{	7B	9
DEL	7F	9
`	60	9
	5F	9
$\overline{Q}$	51	9
NOT	5E	9
]	5D	9
\	5C	9
US	1F	9
RS	1E	9
GS	1D	9
FS	1C	9
ESC	1B	9
SUB	1A	9
EM	19	9
CAN	18	9
ETB	17	9
SYN	16	9

Character	Hex Code	Length, Bits
NAK	15	9
DC4	14	9
DC3	13	9
DC2	12	9
DC1	11	9
DLE	10	9
SI	F	9
SO	E	9
[	D	9
FF	C	9
VT	B	9
>	A	9
HT	9	9
BS	8	9
BEL	7	9
ACK	6	9
ENQ	5	9
EOT	4	9
ETX	3	9
STX	2	9
SOH	1	9
NUL	0	9
GRB		9
/BRK		9
BRK		9
/RNG		9
RNG		9
/CAR		9
CAR		9
/DSR		9
DSR		9

ENTROPY = 7.00

WITH IDLE AND CONTROL CHARACTERS:

ENTROPY = 7.42

COMPRESSION RATIO = -10.15

AVERAGE CODE LENGTH = 7.71

TABLE E-3. CODE TYPE 3 CODE TABLE

ASCII WITH PARITY

Character	Hex Code	Length, Bits
IDLE	80	3
T	54	5
S	53	5
R	52	5
O	4F	5
N	4E	5
M	4D	5
L	4C	5
|	49	5
[	45	5
C	43	5
A	41	5
SF	20	5
CS	D	5
IF	A	5
Y	59	7
X	58	7
U	55	7
DFL	7F	7
P	50	7
K	4B	7
J	4A	7
H	48	7
G	47	7
F	46	7
D	44	7
B	42	7
9	39	7
8	38	7
7	37	7
6	36	7
5	35	7
4	34	7
3	33	7
2	32	7
1	31	7
0	30	7
.	2E	7

Character	Hex Code	Length, Bits
-	2D	7
,	2C	7
)	29	7
(	28	7
US	1F	7
ETB	17	7
SYN	16	7
DLE	10	7
ETX	3	7
NUL	0	7
M	6D	8
|	7C	8
{	7B	9
z	7A	9
y	79	9
l	6C	9
k	6B	9
x	78	9
j	6A	9
i	69	9
h	68	9
w	77	9
c	67	9
v	76	9
}	66	9
u	75	9
@	40	9
?	3F	9
>	3E	9
=	3D	9
<	3C	9
;	3B	9
:	3A	9
e	65	9
d	64	9
c	63	9
b	62	9
a	61	9
`	60	9

TABLE E-3. CODE TYPE 3 CODE TABLE (Cont)

ASCII WITH PARITY

Character	Hex Code	Length, Bits
	5F	9
NOT	5E	9
]	5D	9
\	5C	9
/	2F	9
[	5B	9
Z	5A	9
q	71	9
+	2B	9
*	2A	9
p	70	9
W	57	9
'	27	9
&	26	9
%	25	9
|	24	9
#	23	9
"	22	9
!	21	9
t	74	9
V	56	9
BS	1E	9
GS	1D	9
FS	1C	9
ESC	1B	9
SUB	1A	9
EM	19	9
CAN	18	9
o	6F	9
n	6E	9

Character	Hex Code	Length, Bits
NAK	15	9
DC4	14	9
DC3	13	9
DC2	12	9
DC1	11	9
-	7E	9
SI	F	9
SO	E	9
s	73	9
FF	C	9
VI	B	9
r	72	9
HI	9	9
BS	8	9
BEL	7	9
ACK	6	9
ENQ	5	9
EOT	4	9
}	7D	9
STX	2	9
SOH	1	9
Q	51	9
GRB		9
/BRK		9
BRK		9
/RNG		9
RNG		9
/CAR		9
CAR		9
/DSR		9
DSR		9

ENTROPY = 7.00

WITH IDLE AND CONTROL CHARACTERS:

ENTROPY = 7.19

COMPRESSION RATIO = -14.73

AVERAGE CODE LENGTH = 8.03

TABLE E-4. S49 CODE TYPE 4 CODE TABLE

BSC TRANSCODE

Character	Hex Code	Length, Bits
IDLE	40	2
DEL	3F	6
EM	3E	6
NAK	3D	6
@	3C	6
#	3B	6
SYN	3A	6
9	39	6
8	38	6
7	37	6
6	36	6
5	35	6
4	34	6
3	33	6
2	32	6
1	31	6
0	30	6
HT	2F	6
ETX	2E	6
ENQ	2D	6
%	2C	6
,	2B	6
ESC	2A	6
Z	29	6
Y	28	7
X	27	7
W	26	7
V	25	7
U	24	7
T	23	7
S	22	7
/	21	7
-	20	7
DLE	1F	7
EOT	1E	7

Character	Hex Code	Length, Bits
US	1D	7
*	1C	7
$	1B	7
SPACE	1A	7
R	19	7
Q	18	7
P	17	7
O	16	7
N	15	7
M	14	7
L	13	7
K	12	7
J	11	7
&	10	7
ETB	F	7
SUB	E	7
BELL	D	7
<	C	7
.	B	7
STX	A	7
I	9	7
H	8	7
G	7	7
F	6	7
E	5	7
D	4	7
C	3	7
B	2	7
A	1	7
SOH	0	7
GRB		7
/BRK		7
BRK		7
/RNG		7
RNG		7
/CAR		7
CAR		7
/DSR		7
DSR		7

ENTROPY = 6.00

WITH IDLE AND CONTROL CHARACTERS:
ENTROPY = 6.42
COMPRESSION RATIO = -10.68

AVERAGE CODE LENGTH = 6.64

TABLE E-5. S49 CODE TYPE 5 CODE TABLE

ASYNC

Character	Hex Code	Length, Bits
IDLE	40	2
CTL-C	3C	4
(9 D	34	5
LOWER	1F	5
CTL-B	1E	5
UPPER	1C	5
SPACE	00	5
A a	39	6
* 8	38	7
_ -	37	7
B̄ b S	36	7
W w	35	7
PRFIX	3E	7
F f	33	7
U u	32	7
V v	31	7
# 3	30	7
TAB	2F	7
LF	2E	7
NL	2D	7
RDRSTP	2C	7
: ;	2B	7
D d	2A	7
R r	29	7
& 7	28	7
Y y	27	7
H h	26	7
S s	25	7
) 0	24	7
G g	23	7
X x	22	7
M m	21	7
[ ]	20	7
IDLE	3D	7
DEL	3F	7

Character	Hex Code	Length, Bits
BS	1D	7
' '	3B	7
Q q	1B	7
K k	1A	7
I i	19	7
6	18	7
X'17'	17	7
X'16'	16	7
X'15'	15	7
Z z	14	7
+ =	13	7
N n	12	7
. .	11	7
@ 2	10	7
PNHOFF	0F	7
BYPAS	0E	7
RSTRE	0D	7
PNHON	0C	7
P p	0B	7
E e	0A	7
" '	09	7
% 5	08	7
? /	07	7
L 1	06	7
O o	08	7
$ 4	04	7
J j	03	7
T t	02	7
0 !	01	7
C c	3A	7
GRB	9	7
/BRK	8	7
BRK	7	7
/RNG	6	7
RNG	5	7
/CAR	4	7
CAR	3	7
/DSP	2	7
DSR	1	7

ENTROPY = 6.00

WITH IDLE AND CONTROL CHARACTERS:
ENTROPY = 6.42
COMPRESSION RATIO = -13.02

AVERAGE CODE LENGTH = 6.781

TABLE E-6. CODE TYPE 6 CODE TABLE

ASYNC

Character	Hex Code	Length, Bits
IDLE	20	2
LTRS	1F	5
V ;	1E	5
X /	1D	5
M .	1C	5
FIGS	1B	5
G 8	1A	5
B ?	19	5
O 9	18	6
Q 1	17	6
P 0	16	6
Y 6	15	6
H #	14	6
W 2	13	6
L)	12	6
Z "	11	6
T 5	10	6
K (	F	6
C :	E	6
F !	D	6

Character	Hex Code	Length, Bits
N ,	C	6
J '	B	6
R 4	A	6
D $	9	6
CR	8	6
U 7	7	6
I 8	6	6
S BEL	5	6
SP	4	6
A	3	6
LF	2	6
E 3	1	6
	0	6
GRB	9	6
/BRK	8	6
BRK	7	6
/RNG	6	6
RNG	5	6
/CAR	4	6
CAR	3	6
/DSR	2	6
DSR	1	6

ENTROPY = 5.00
WITH IDLE AND CONTROL CHARACTERS:
ENTROPY = 5.42

COMPRESSION RATIO = -15.63
AVERAGE CODE LENGTH = 5.78

APPENDIX F
BINARY SYNCHRONOUS COMMUNICATION

F.1 PROTOCOL

Binary synchronous communication (BSC) protocol is a set of rules for transmitting binary-coded data from point to point. BSC accommodates three standard transmission codes: ASCII, which is the most common for terminals; EBCDIC, or Transcode. BSC also provides transparency, which allows the transmission of control characters as data. These features permit use of a wide range of high-speed and medium speed terminals and transmission equipment.

Under BSC protocol, data is transmitted synchronously as a continuous stream of bits in one direction at a time. Synchronization is achieved by the transmission of a unique bit pattern - the sync signal - that is recognized by any receiver and used to time the receiver to operate in step (synchronously) with the transmitter.

The communications systems that use BSC may operate via leased or switched lines in either a point-to-point or a multinode configuration. In a point-to-point configuration the nodes contend for use of the line; the node that persists or that is fortunate in timing wins the line.

In a multinode configuration, one node is typically the control node. It controls all transmissions in the net by either polling it tributary stations or by selection of one. Selection is by request to receive; the control node designates both the transmitting and receiving nodes by address. An address is unique, and may consist of one to seven characters, the first of which identifies the node, while the remainder identify the terminals attached to the node.

F.2 MESSAGE CONTENT

A BSC message block consists of data plus control characters. The data is the contents of the message that is to be transmitted; the control characters provide message identification, addressing, error checking, etc., and show the limits of the functional portions of the transmission block. It should be noted that in transparent text, the control characters are passed as data.

BSC messages are divided into blocks to provide tight error control, and each block in turn is divided into functional segments marked SOH, ETX, ITB, and ETB, as well as error-checking characters. These are all explained below.

F.3 ERROR CHECKING

Error checking is performed in a variety of ways depending on the transmission code used. ASCII with odd parity employs a vertical redundancy check (VRC) that checks the message character-by-character as it is received.

Longitudinal redundancy checking (LRC) checks the entire received block, in the following manner: all data and control characters (except sync's) are accumulated independently at both the transmitter and receiver to form a block check character (BCC) that is transmitted after ETB, ETX, or ITB. The BCC sent by the transmitter is compared at the receiver with the BCC accumulated there; if the BCC's match, the transmission is error-free.

The control signals STX (start of text) or SOH (start of header) mark the beginning of a new message block; they reset the LRC and a new BCC is started.

When a receiver has gotten an error-free message block it sends back an ACK0 or ACK1 to the transmitter to mark the event. ACK0 and ACK1 are sent in response to alternate blocks; they identify the block being ACK'd.

When a receiver detects an error in transmission it sends a NAK to the transmitter, which then retransmits the previous block.

If an ACK or NAK is garbled, the transmitter sends ENQ (enquiry) to the receiver, which then retransmits the acknowledgement.

Cyclical redundancy checking (CRC) for error control may have two forms: CRC 12 used for six-bit codes, or CRC 16 used for eight-bit codes. Like the LRC, the CRC is computed at both transmitter and receiver.

Appendix D contains the binary and hex codes for keyboard characters.

F.3.1 EOT/NAK PAD FORMAT CHECK

BSC stations add eight one's to EOT or NAK as trailing pad bits. This assures accurate reception of these characters as data. Without the pads they might be

interpreted as control characters if timing variations resulted in clipping some bits from them. The receiver actually needs only four one's; the rest provide insurance.

In the Codex 6030/6040, this is expanded so that pads are added to any character that turns the line around.

F.4 DATA LINK CONTROL

The data link is controlled by the control characters and sequences described below. There are several variations in the code sets (ASCII, EBDCIC, and Transcode). These variations are shown in the character conversion chart shown in Figure 1.

SYN - synchronous idle. Used to establish and maintain synchronization, and as a time fill in the absence of data or any control character. Two contiguous SYN's start each transmission. (They are represented by 0 in the accompanying figures and format examples.)

SOH - Start of heading. Precedes a block of heading characters that identify routing and priority and are necessary to process the text of the message. Initiates the accumulation of the BCC, but an initial SOH is not part of the accumulation

STX - start of text. Text is a block of characters that are transmitted through to the ultimate destination without change. STX also terminates a heading.

ETB - end of transmission block. ETB terminates a block of characters starting with SOH or STX. (This transmission block is not necessarily related to the processing format.) ETB is followed immediately by the block check character. ETB requires an acknowledgement: ACK0, ACK1, NAK or WACK or RVI.

ITB - end of intermediate transmission block. Divides a message for error checking purposes without causing a turnaround. ITB is followed by a BCC and resets the block check count. After ITB, successive intermediate blocks need not be preceded by STX or SOH. (For transparent data, each successive intermediate block begins with DLE STX.) However, if one intermediate block is data and the next is text, STX begins the text block.

The last intermediate block is terminated by ETB or ETX (DLE ETB or DLE ETX for transparency). The receiver acknowledges the entire transmission, but if an error is detected in any intermediate block, a NAK is sent for that block, and it and all subsequent blocks are retransmitted.

All BSC stations must be able to receive ITB and its BCC, but the ability to transmit ITB is optional.

Some stations permit ITB's in transparent data at predetermined, fixed intervals in the transparent text. The receiver must be aware of the interval length.

ETX - end of text. ETX terminates a block that begins with STX or SOH and is transmitted as an entity. ETX is followed immediately by the BCC, and requires an acknowledgement.

EOT - end of transmission. The transmission may contain one or more blocks, including text and associated headings. EOT causes reset of error check at all stations. EOT is also used as:

1. A response to a poll when the polled station has nothing to transmit.
2. An abort signal that indicates that the transmitter can no longer transmit due to a system malfunction or an operational difficulty.

ENQ - enquiry. ENQ is used to:

1. Obtain a transmission of a ACK or NAK that was garbled or not receive when expected.
2. Bid for the line in point-to-point transmission.
3. Indicate the end of a poll or selection sequence.

ACK0/ACK1 - affirmative acknowledgement. Used to indicate that the last block was received without error and the receiver is ready for the next block. ACK0 is sent first, and alternates with ACK1. ACK0 is also the positive response to selection (multipoint) or line bid (point-to-point) to provide a sequential check for a series of acknowledgements.

WACK - wait acknowledge. Receiver temporarily not ready to receive. WACK is sent in response to text, heading block, line bid or selection sequence, or, in a switched net, to an identification (ID) line bid. WACK is positive acknowledgement of the received data block, or of selection.

The transmitter's response to WACK is ENQ, but EOT and DLE EOT are also valid. If ENQ is received, the receiver continues to reply WACK until ready to continue.

All BSC stations must be able to receive WACK, but the ability to send it is optional.

NAK - negative acknowledgement. Indicates that the previous block was received in error, and should be retransmitted. NAK is also sent in response to station selection or line bid, if not ready to receive.

DLE - data link escape. Used only with line control characters, or transparent mode control characters, as follows:

DLE STX, DLE ETX, DLE ITB, DLE ETB	Initiate and terminate transparent text
DLE ENQ, DLE DLE, DLE EOT	Active control characters within transparent text
DLE SYN	Inserted in heading and text data at 1-second intervals to maintain sync. Cannot establish phase

RVI - reverse interrupt. If sent by a receiver in place of ACK0 or ACK1, RVI requests termination of current transmission so receiver can send high priority message to transmitter. Also, in multipoint net, sent by control station that is receiving, so that it can send message to any station in the network. Successive RVI's cannot be sent, except in response to ENQ.

The sending station treats RVI as ACK, and transmits all data that prevents it from receiving (i.e., empties its buffers). More than one block transmission may be required.

BSC stations must be able to receive RVI. The ability to transmit RVI is optional.

TTD - temporary text delay. If a transmitter has a line and wishes to retain it, but is not ready to transmit within two seconds, it sends TTD. This two-second timeout avoids the nominal three-second receive timeout at the receiver.

The response to TTD is NAK. If the sender is still not ready to transmit, TTD can be repeated one or more times.

TTD is used when the sender's buffer is not full due to intrinsic machine timing, and also to abort the current transmission when the sender is in message transfer mode. After receiving NAK to the TTD sequences, the sender sends EOT, resetting the stations to control mode (forward abort).

DLE EOT - disconnect for a switched line. DLE EOT is sent by either the calling or the called station, to indicate that the sender is going "on hook" (usually after all message exchanges are complete). It may be used optionally in place of EOT.

ID - Identification. Line bid for a switched network.

APPENDIX G

DIAGNOSTIC OPERATION - SUMMARY

1. Install diagnostic ROM module in place of customer's ROM's.

2. Preliminary Tests.
   a. Initiated by power up of system.
   b. TSC = 01, Preliminary ROM Test.
   c. TSC = 02, Preliminary Processor Run-Halt Test: verification of number of processors.
   d. TSC = 03, Preliminary RAM Diagnostic.
   e. TSC = 04, TP and NP verification.
   f. TSC = 05, Front Panel Diagnostic.
      1. Text displayed @ ABCDEFGHIJKLMNO CLEAR
      2. Text displayed PQRSTUVWXYZ[~]{} CLEAR
      3. Text displayed !"#$%&()*+,-./ CLEAR
      4. Text displayed Ø123456789:;<=>? CLEAR
      5. Text displayed Ø4:SH2:ØØ:Ø4 Keys =
         Press keys in sequence 0 ⟶ F ENTER CLEAR

3. Select Test Sequence Code.
   In the following, Kn means the nth digit to be displayed or entered.
   Display: Ø-SH2:ØØ TSC(1):nn/
   Action: K1 K2 ENTER
   K1 = Test Group K2 = Test within group
   F entered will display as - (dash); it means all tests are to be run.
   (FF = all groups, all tests)

4. Select Test Control Code.
   Display: K1 K2 :SH2:ØØ Input TCC:
   Action: K3 K4 K5 ENTER
   K3 = action taken at end of test
   K4 = action on receipt of error
   K5 = mode of continued execution after error

Pressing ENTER initiates execution of selected test.

Display: K1 K2 : K3 K4 K5 :ØØ:XX

XX = current test being executed

5. Preemptive Control Mode: entered if transition to diagnostic mode is detected.

Action: a. Turn keylock switch to MON or PGM, press any key.

b. Turn keylock switch to DIAG, press a functional key:

BOOT - Reboot diagnostic system.

CTRL - Terminate current test and return to controller.

STEP - End current test, advance to next test.

HELP - Display current program counter and stack pointer.

MEM - Examine, and optionally change, contents of memory location.

GOTO - Start execution at address entered via the keyboard.

EXAM - Examine, and optionally change, contents of locations in the off-line configuration memory.

DIAG - Examine the error file if in RN5 TCC mode.

SEL - Select the next processor for the panel display.

APPENDIX H

EXTERNAL LOOPBACK PLUG WIRING

H.1 TP EXTERNAL LOOPBACK PLUG

A user can make an external loopback test plug by wiring a 25-pin EIA male connector as shown in Figure H-1. It is quicker and less expensive for a customer to make one than to order one from Codex, hence it is not a standard spare.

The figure is also a key to the locations of pins on the connector. The numbers are embossed on the insulator body, but are small and difficult to read in low-level light.

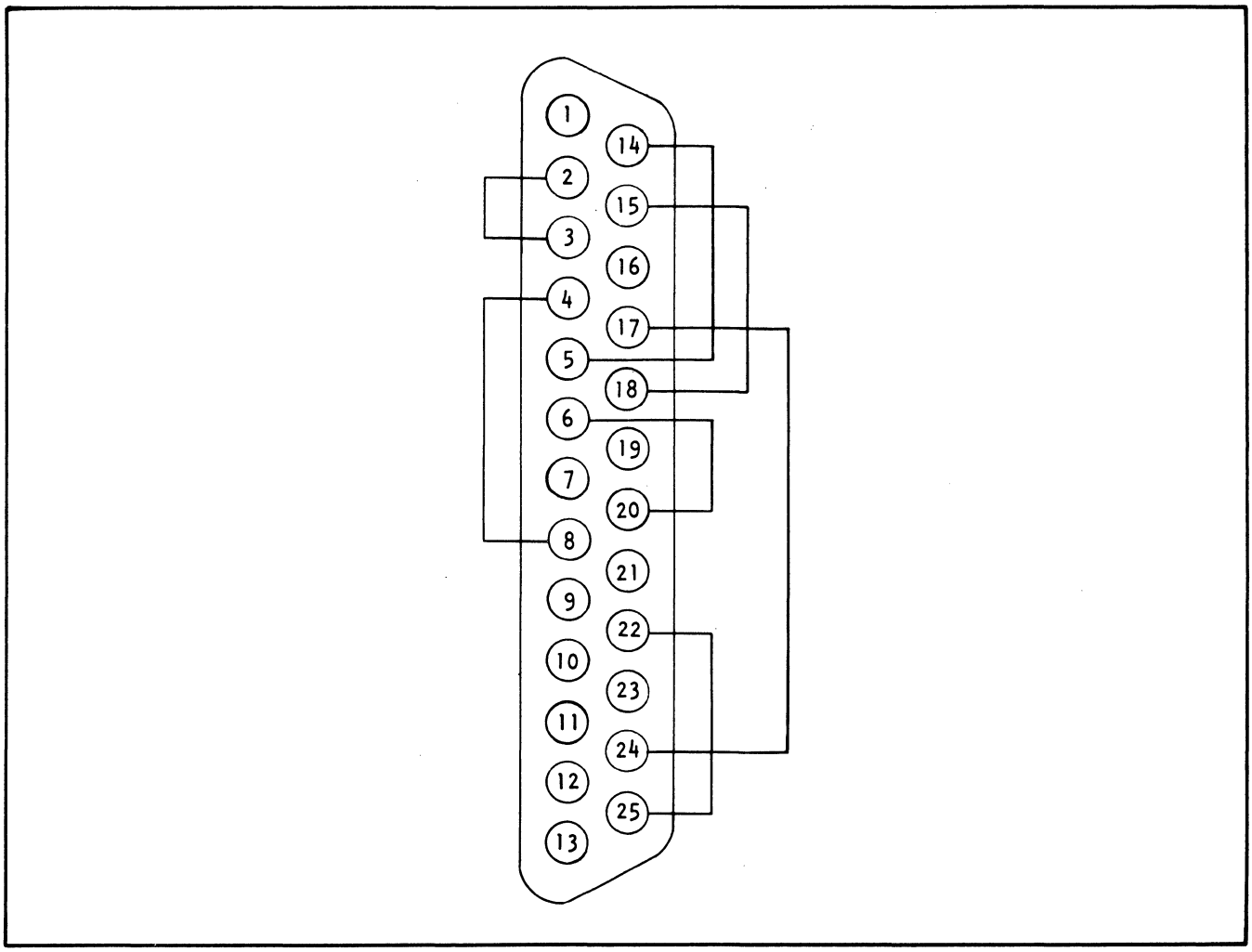


Figure H-1. TP External Loopback Plug Connections

H.2 NP EXTERNAL LOOPBACK WITH INTERNAL CLOCK SOURCE

If it is necessary to test a network port when the trunk modem is either not present or not working, the user can get internal clock from the TP by making a pair of test plugs. Figure H-2 shows the wiring for these plugs.

The TP must also be strapped for the desired speed on platform U10 or U17, as applicable. Platform U5 is strapped for internal clock on the appropriate channel (U5-3 to -14 for J1, U5-7 to -10 for J2). The strapping locations are shown in Figure for the J1 channel. J2 is identical.

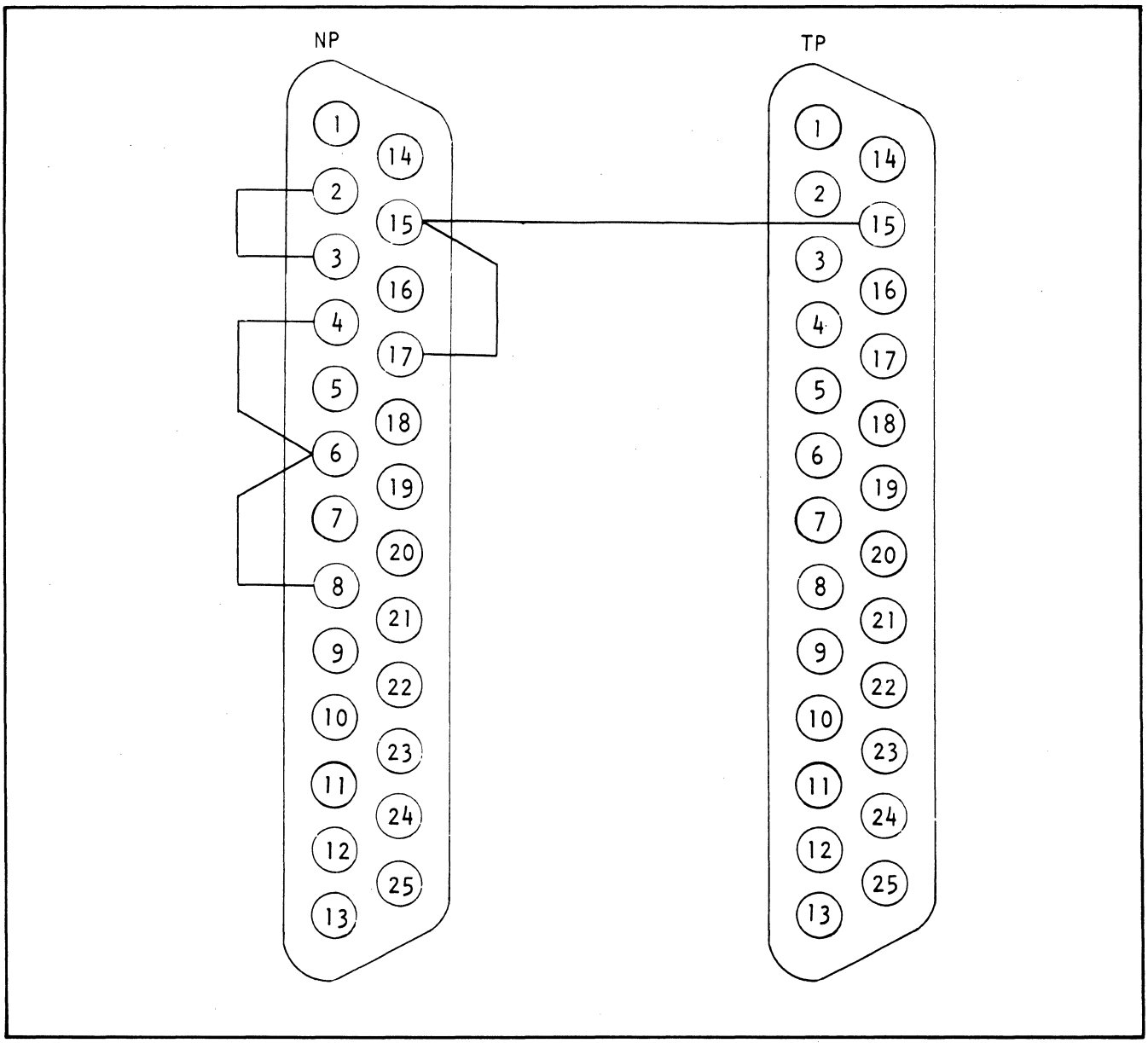


Figure H-2. NP External Loopback Plug Connections - Internal Clock from TP

APPENDIX I

SYSTEM CALCULATIONS

I.1 SYSTEM THROUGHPUT

To calculate system throughput for 6000 networks, the following formula should be used:

operations = Σ average traffic into buffers + Σ average traffic out of buffers + 5 Σ frames received + 5 Σ frames transmitted + Σ idle codes received + Σ idle codes transmitted

Idle codes are calculated based on one idle code per frame per port during the portion of time a terminal is idle.

I.2 SYSTEM OUTAGE DURATIONS

The following chart illustrates the relationship between slot-weights and buffer multiplier values which result in approximate outage duration times.

		A	B	C = Bx5	D = Cx14	$C = \frac{D}{A}$
	Speed	CPS	Slot Weight	Buffers	Approximate Number of Buffered Char.	Outage Duration In Seconds
	75	10	1	5	70	7
A	110	10	1	5	70	7
S	134.5	15	1	5	70	4.6
Y	150	15	1	5	70	4.6
N	300	30	2	10	140	4.6
C	600	60	3	15	210	3.5
	1200	120	6	30	420	3.5
	1200	150	8	40	560	3.7
S	2000	250	14	70	980	3.9
Y	2400	300	16	80	1120	3.7
N	3600	450	24	120	1680	3.7
C	4800	600	32	160	2240	3.7
	7200	900	48	240	3360	3.7
	9600	1200	64	320	4480	3.7

I.3 RAM BUFFER POOL SIZE

The following chart may be used to calculate the approximate (±5%) size of the RAM buffer pool.

	RAM Bytes Required	Lock Bytes Required
Node	350	16
Each Code Table	62	--
Each TP	68	6
Each NP	63	11
Each XP	52	2
Each CTP	28	6
Each Autospeed Definition	6	--
Lock Byte Area	256, 512, or 1024	

For example, consider a 6040 with 512 bytes available for the lock byte area and the following:

Node	350	16
7 Code Tables	434	--
2 NP's	126	22
30 TP's	2040	180
20 XP's	1040	40
1 CTP	28	6
5 AD's	30	
	Total RAM = 4048	Total Lock byte = 248

The total RAM area required is 4048 + 512 (of which only 248 are used) = 4560 bytes. Each RAM has a capacity of 16,384 bytes. If only 4560 are used, 11,824 remain available for buffers. If each buffer requires 16 bytes, then approximately 739 buffers are available.

I.4 CHARACTER DELAY

Figure I-1 shows character delay through an INP as a function of traffic density. Two line speeds are assumed, 4800 and 7200 bps, with 23 terminals.

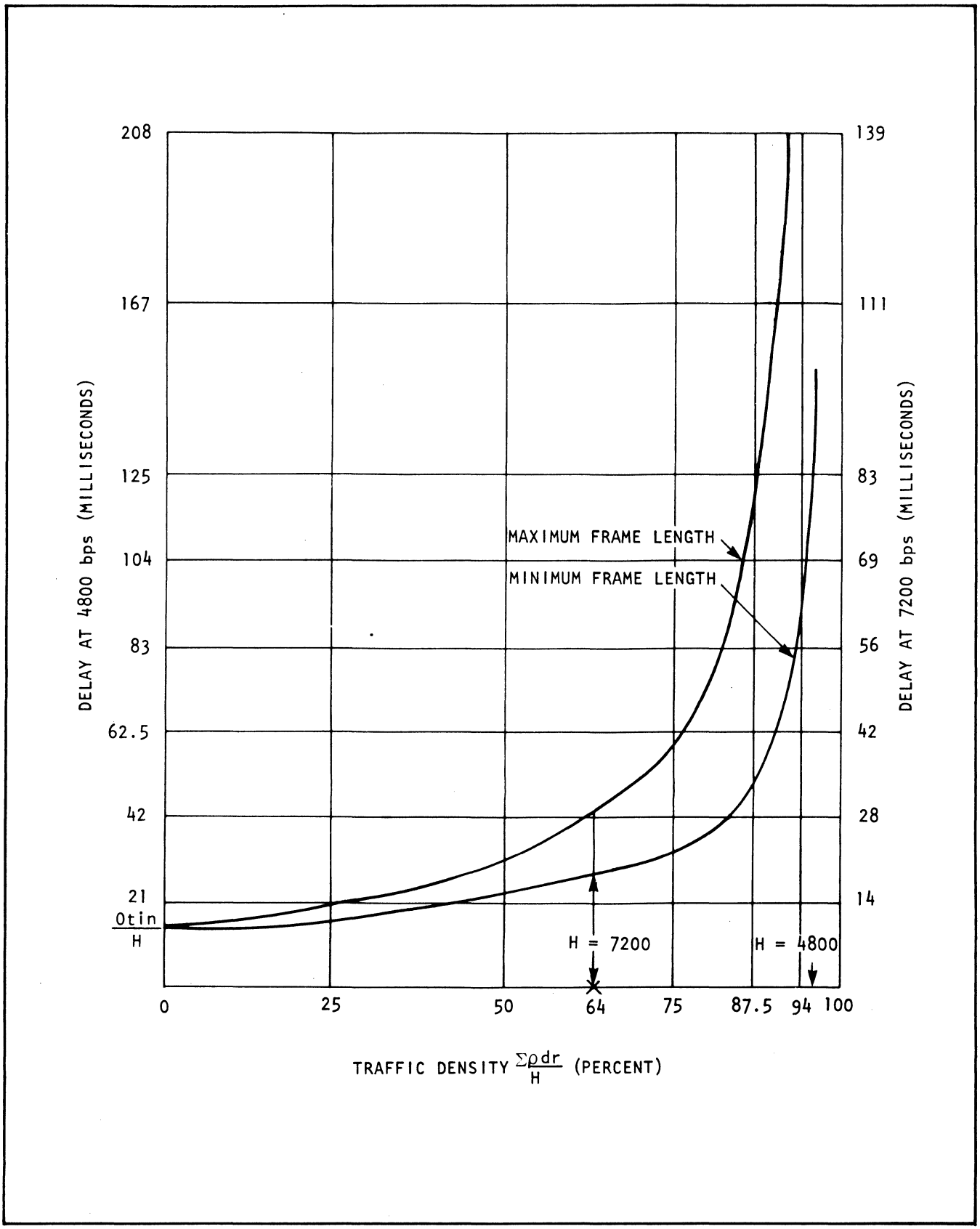


Figure I-1. Character Delay Thru 6000 as a Function of Traffic Density

I.5 AVERAGE FRAME LENGTH

The average 6000 Series frame length can be calculated from the following formula (which assumes no idle codewords).

$$\text{Average Frame size} = \frac{27 - \text{ARQ size}}{100 - \text{Traffic Density}} \times 100$$

I.6 BUFFER MULTIPLIER VALUE

$$\text{Buffer Multiplier} = \frac{720}{\sum_{4}^{N} \text{Slot weight}}$$

where 720 = approximate number of buffers per RAM

Example:

10 terminals, each with a speec of 1200, and a slot weight = 12.

Then: $BM = \frac{720}{10 \times 12} = \frac{720}{120}$

$BM = 6$

I.7 CALCULATING AVERAGE FRAME LENGTH

$$\text{AVG. FR. LEN.} = \frac{\text{FR. OVHD} + \sum_{4}^{N} \text{IDLE CODE LEN.} \times \text{NO. OF TERM.}}{H - \sum_{4} p\, d\, r} \times H$$

Where:

H = high speed line rate

p = terminal utilization factor

d = data compression factor

r = terminal speed

Example:

10 terminals

p = 50%

d = .7

r = 1200

Idle code length = 2 bits

Then:

$$\text{Avg. fr. len.} = \frac{30 + 20}{9600 - 10 \times .50 \times .7 \times 1200} \times 9600$$

$$= \frac{50}{9600 - 4200} \times 9600$$

$$= \frac{50}{5400} \times 9600$$

$$= .009 \times 9600$$

$$= 89 \text{ bits}$$

NOTE: p X d = CL (compressed loading)
CL X speed = pdr

I.8 CALCULATING MINIMUM FRAME TIME

Minimum frame time = FIFO size

Example:

trunk speed = 9600 BPS

FIFO size = 256

Then:

256 = number of bits per frame

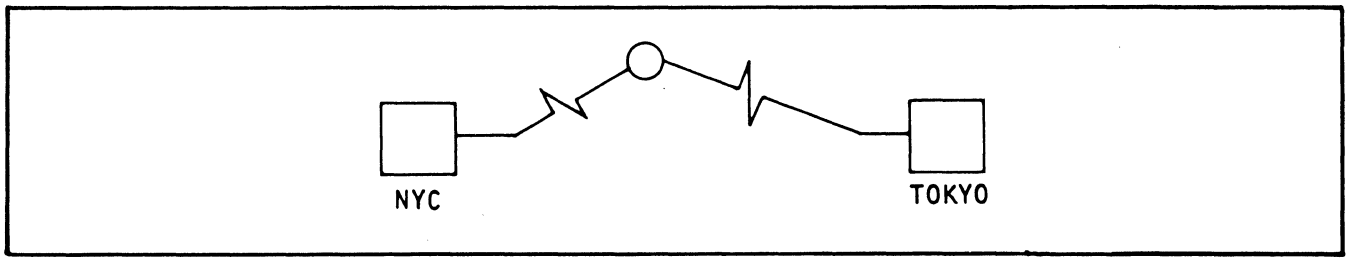
At 9600 BPS, each bit takes 104 μsec to transmit

256 x 104 μsec = 26 Msec per frame

I.9 CALCULATING ARQ SIZE

Example:

Consider a 6000 network operating between NYC and Tokyo, operating over a satellite.



ASSUME: one-way path delay = 350 Msec
round trip path delay = 700 Msec
trunk speed = 9600
FIFO = 256

FIRST: calculate the MINIMUM frame time

256 bits

At 9600 BPS, each bit takes 104 μsec to transmit

256 bits per frame x 104 µsec per bit
= 26 Msec per frame

THEN: calculate the ARQ value

```
   26
26/700
  52
  180
  156
   24
```

= number of frames transmitted before first ACK received (path delay)

THEREFORE: the calculated size is 26 but the valid parameters are 7, 15, 31, 63, 127.

So the parameter would be set to 31.

I.10 FRAME TRANSMISSION TIME

$$\text{Frame Transmission Time} = \frac{\text{frame length}}{\text{line speed}}$$

Frame length = ΣSW * 8 bits + overhead

Overhead = 29 bits per frame

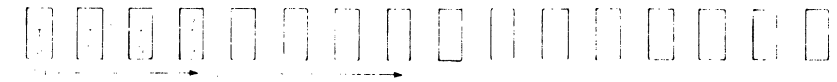
APPENDIX J

CONFIGURATION MEMORY LAYOUTS

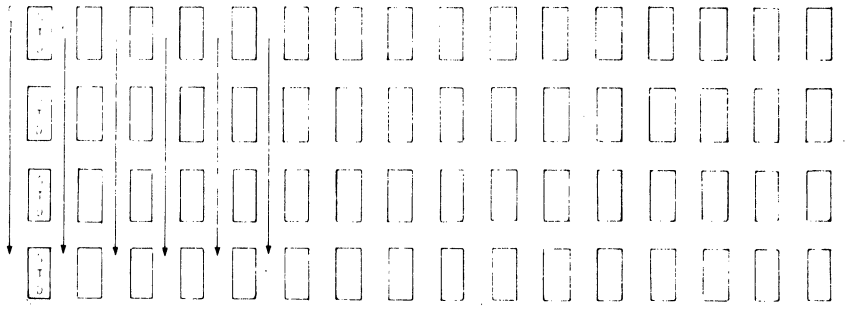
Figure J-1 shows the layout of configuration memory for every model of the 6030/6040 Intelligent Network Processor. There are two versions of the option module; wire wrap and printed circuit. Layouts for both are shown for each applicable model, but there is only a PC version of Models 6046, 6047, and 6048.

MODEL 6030-6031

WIRE WRAP



PRINTED CIRCUIT



MODEL 6032

WIRE WRAP

PRINTED CIRCUIT

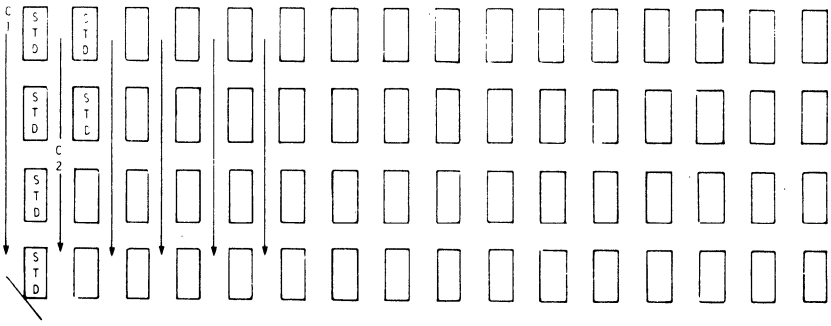
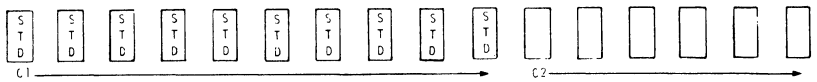


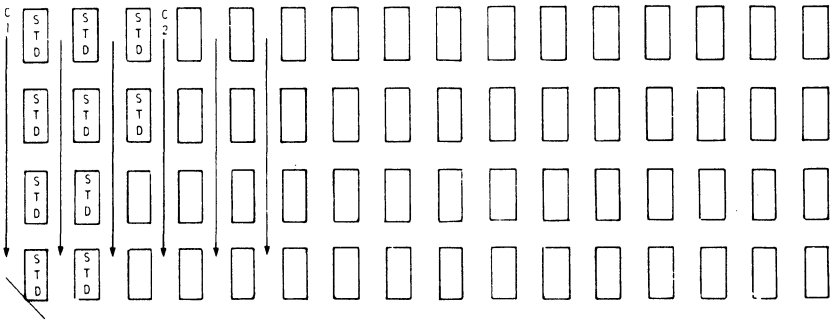
Figure J-1. Configuration Memory Chip Layout

MODEL 6033

WIRE WRAP

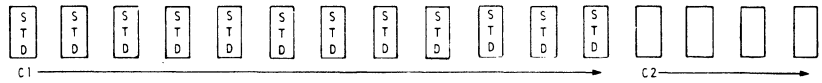


PRINTED CIRCUIT



MODEL 6034

WIRE WRAP



PRINTED CIRCUIT

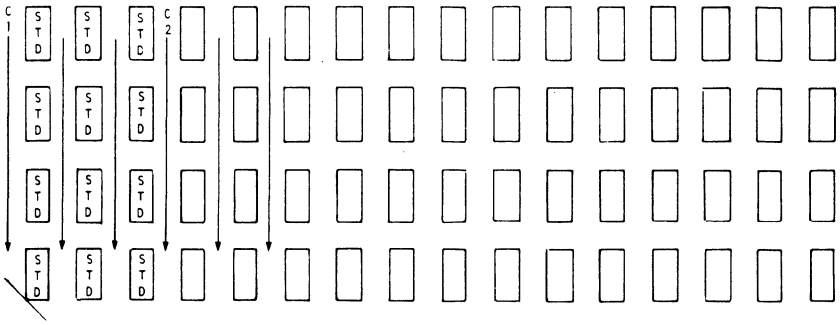
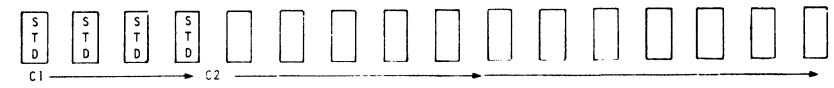


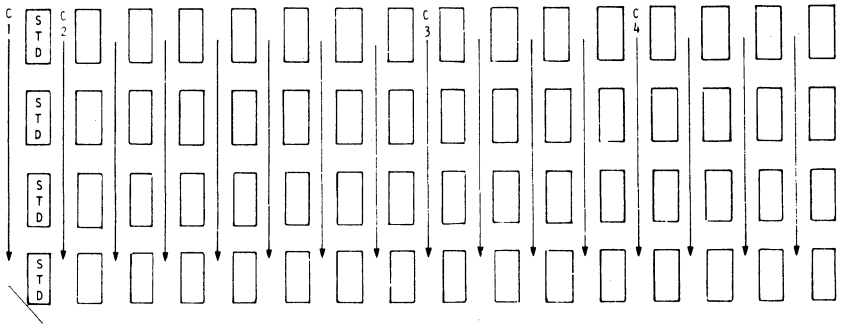
Figure J-1. Configuration Memory Chip Layout (Cont)

MODEL 6040-6041

WIRE WRAP

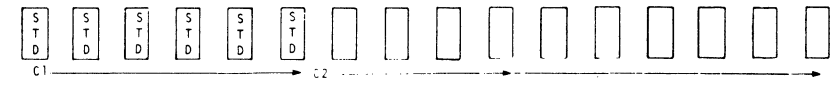


PRINTED CIRCUIT



MODEL 6042

WIRE WRAP



PRINTED CIRCUIT

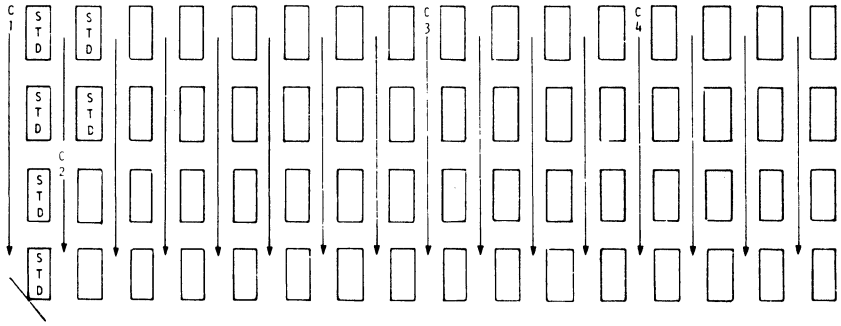
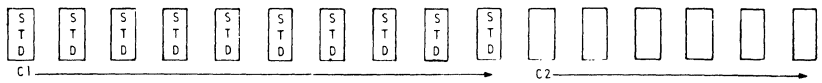


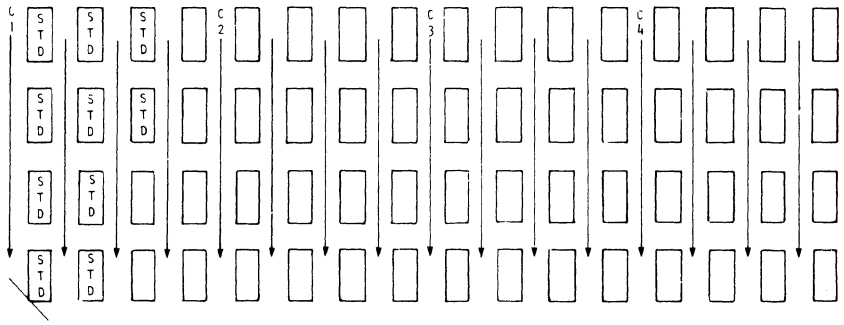
Figure J-1. Configuration Memory Chip Layout (Cont)

MODEL 6043

WIRE WRAP

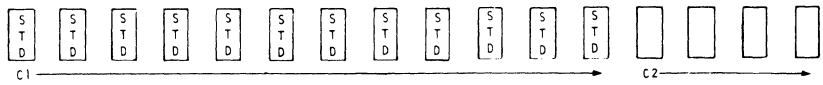


PRINTED CIRCUIT



MODEL 6044

WIRE WRAP



PRINTED CIRCUIT

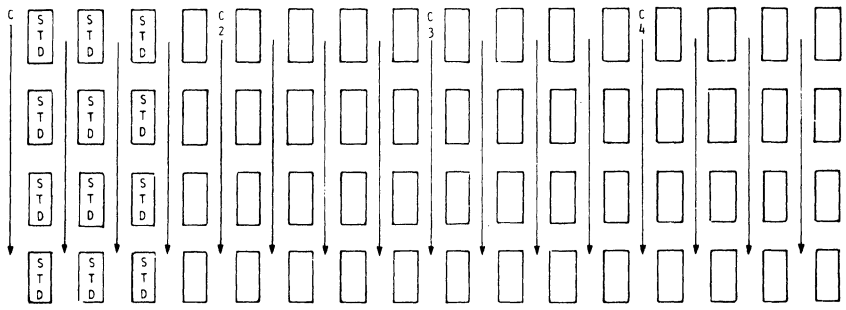
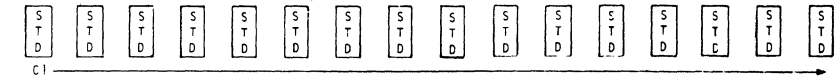


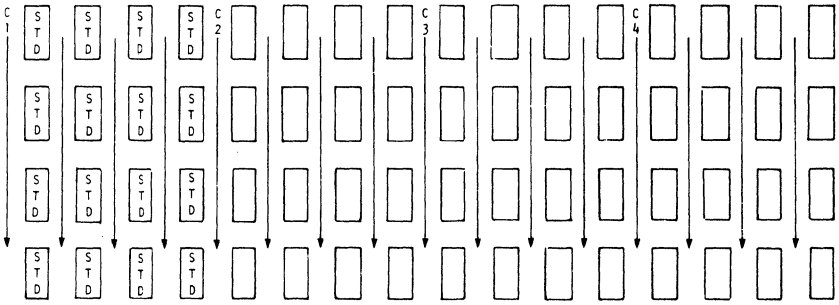
Figure J-1. Configuration Memory Chip Layout (Cont)

MODEL 6045

WIRE WRAP



PRINTED CIRCUIT



MODEL 6046

PRINTED CIRCUIT

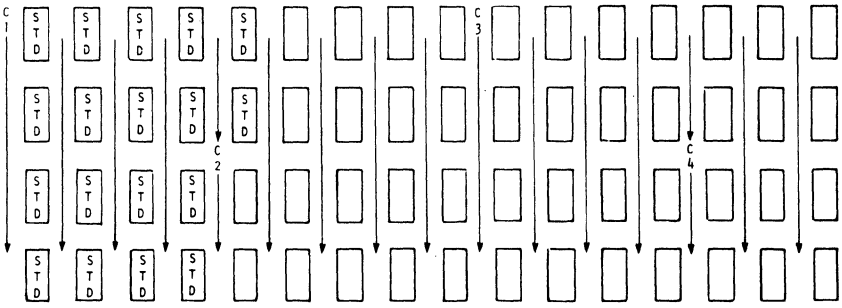
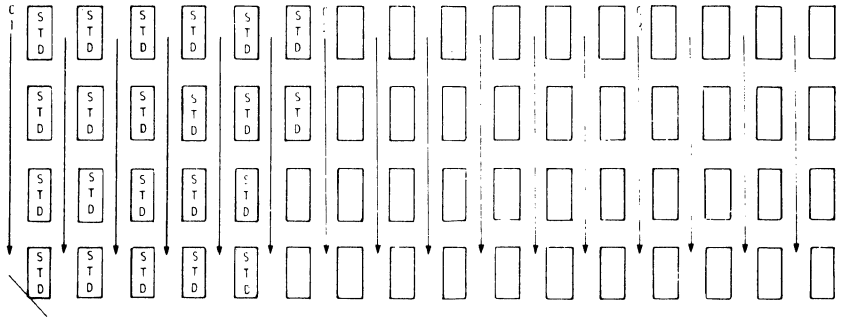


Figure J-1. Configuration Memory Chip Layout (Cont)

MODEL 6047

PRINTED CIRCUIT



MODEL 6048

PRINTED CIRCUIT

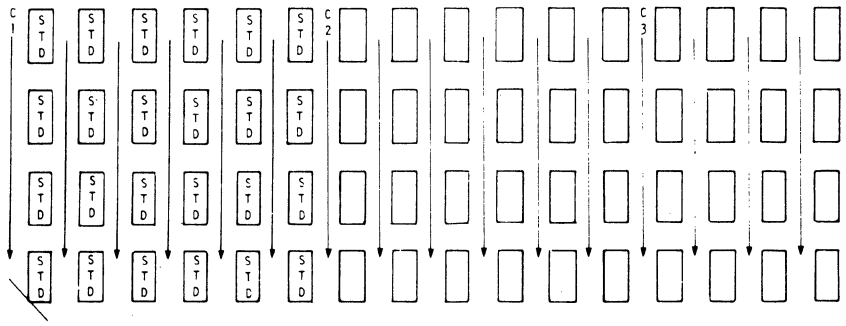


Figure J-1. Configuration Memory Chip Layout (Cont)

APPENDIX K

CHIP IDENTIFICATION

K.1 CHIP IDENTIFICATION

Each chip on circuit boards used specifically for S49 software is marked uniquely in white ink. The identification numbers are analyzed and defined in Table K-1. The general format for the identification is as follows:

Use . Release number - Chip sequence number

TABLE K-1. CHIP IDENTIFICATION

Use	Use Identification		Release Number		Chip Sequence Number
Diagnostic Rev 12	D12	.	RR	-	CC
Code Table	CT	.	RR	-	CC
Firmware	FW	.	RR	-	CC
Software	S49	.	RR	-	CC

APPENDIX L

RETURN OF DEFECTIVE MATERIALS

Field repair of defective modules or units to the component level is not recommended Replacing whole modules known to be defective is, however, recommended as a means of quickly returning the unit to on-line service.

Defective units or modules should have tags attached indicating the malfunction or diagnostic test which failed and the address to which the repaired module/unit should be returned. Do not mark the equipment itself. Failure symptoms should include the name of the test failed, the error message displayed, and the error indicator displayed. This information will expedite analysis and correction of the defect.

Enclose within each package a shipping list, identifying each item by serial/part number and failure symptoms. Also include, where possible, a purchase order number for billing purposes. After securely packaging the defective materials, ship them prepaid to:

Codex Corporation
Attn: Dept. ERR
665 West Street
Mansfield, Massachusetts 02048

Always refer to the latest Codex Installation and Maintenance Price Schedule (Form Number 98786) for repair/replacement cost.

APPENDIX M

LOGIC DIAGRAMS

This appendix contains logic diagrams for the Intelligent Network Processor.

(to be supplied)

6030/6040 SERIES

S49 SOFTWARE NODE WORKSHEET

Page _____ of _____

NODE # _______ CONFIGURATION # _______

CIRCUIT CROSS REFERENCE			CHARACTERISTICS C															ACTIVITY A =			TRANSMIT DATA PATH X =			RECEIVE DATA PATH R =	
		PORT NO	PORT TYPE	SUB TYPE	TRANSMIT SPEED	CODE TYPE	DATA BITS	PAR	STOP BITS	AUTO ECHO	RECEIVE SPEED	OP MODE	CHAR DELAY	FLY BACK	AUTOSPEED RECOG CHAR	AUTOSPEED SUB CHAR	FIFO SIZE	STAT	MODE	ARQ FRAME	ADJ NODE	ADJ PORT	SLOT WT	ADJ NODE	ADJ PORT
PAGE NO	LINE NO		T	ST	S	C	DB	P	SB	E	RS	OM	CD	FB	AR	AS	F	S	M =	AF =	AN =	AP =	SW =	AN =	AP =

6040 ONLY (PAGE NO, LINE NO)

PARAMETERS REQUIRED TO CONFIGURE THE VARIOUS PORT TYPES. (● = REQUIRED)

	PORT TYPE	SUB TYPE	TRANSMIT SPEED	CODE TYPE	DATA BITS	PAR	STOP BITS	AUTO ECHO	RECEIVE SPEED	OP MODE	CHAR DELAY	FLY BACK	RECOG CHAR	SUB CHAR	FIFO SIZE	STAT	MODE	ARQ FRAME	ADJ NODE	ADJ PORT	SLOT WT	ADJ NODE	ADJ PORT
	NP		●												●	●	●	●					
	AP	●	●	●	●	●	●	●	●	●		●				●	●		●	●	●		
	SP	●	●	●	●	●				●	●					●	●		●	●	●		
	C	●	●		●	●	●	●	●		●												
	E																						
	AD		●	●	●	●	●	●	●	●			●	●									
	XP			●															●	●	●	●	●

6040 ONLY (RECEIVE DATA PATH)

ENTRY DESCRIPTIONS FOR NODAL PARAMETERS CAN BE FOUND ON REVERSE SIDE

REV-B
CODEX PN 04739
Printed in U.S.A.

6030/6040 SERIES

S49 SOFTWARE NODE WORKSHEET

SUGGESTED STARTING VALUES

NODE NO. _____ CONFIGURATION _____

1 PORT TYPES

NP = NETWORK PORT
AP = ASYNCHRONOUS TERMINAL PORT
SP = SYNCHRONOUS TERMINAL PORT
C = CONTROL TERMINAL PORT
E = EMPTY PORT
AD = AUTOSPEED DEFINITION
XP = TRANSFER PORT

2 SUBTYPES

FOR AP: 1 = START/STOP
2 = AUTOSPEED
FOR SP: 1 = BSC
FOR C: 1 = CONTROL TERMINAL PORT
2 = SUPERVISORY COMMUNICATIONS PORT
3 = LOGGING CONTROL TERMINAL PORT
NOTE: 0 IS AN ILLEGAL VALUE

3 TRANSMIT SPEED

AP = 75, 110, 135, 150, 300, 600, 1200
SP = 1200, 2400, 3600, 4800, 7200, 9600

5 DATA BITS

ACTUAL VALUE INCLUDING PARITY

6 PARITY

FOR AP: O = ODD, E = EVEN, N = NONE
FOR SP: 0 = ODD, E = EVEN, N = NONE

4 CODE TYPE CHARACTERISTICS

NO. BITS	USES	NO. OF DATA BITS	HEX SYNC CHAR	BSC CONTROL CHAR	IDLE CODE BITS	COMPRESSION	CODE TYPE
8	BSC ASCII	8 or less no parity	16	ASCII	6	NO	0
	Any S/S Terminal	8 or less no parity	n/a	n/a	6	NO	0
	EBCDIC	8, no parity	32	EBCDIC	4	YES	7
	Autospeed not supported by CT2				6	NO	0
	BSC EBCDIC	8, no parity	32	EBCDIC	6	NO	1
	BSC ASCII	8 or less with parity	E = 96 0 = 16	ASCII	2	NO	2
	Any S/S Terminal	8 or less with parity	n/a	n/a	2	NO	2
	ASCII	8 with parity	E = 96 0 = 16	ASCII	3	YES	3
7	BSC Transcode	7 with parity	n/a	Transcode	2	NO	4
6	Any S/S Terminal	6 with parity	n/a	n/a	2	NO	6
5	Baudot	5, no parity	n/a	Baudot	2	NO	6
	Custom Applications						8

7 STOP BITS

1 or 2 NOTE: DB = 5 WITH 2 STOP BITS DEFAULTS TO 1.5 STOP BITS.

8 AUTOECHO

E = ENABLED D = DISABLED

9 RECEIVE SPEED

T = SAME AS TRANSMIT SPEED
D = DEFAULT TO AN INTERNAL CLOCK VALUE (1200 BPS)

10 OPERATION MODE

OPERATION MODE IS TWO HEX CHARACTERS (C_1 AND C_2), EACH OF WHICH IS FOUR BITS.

OM = C_1 (b_7 b_6 b_5 b_4) C_2 (b_3 b_2 b_1 b_0)

FOR ASYNCHRONOUS APPLICATIONS:
OM = 00 IF NO FLYBACK (FB) IS USED
OM = 10 IF FLYBACK (FB) IS USED.

FOR ASYCHRONOUS APPLICATIONS:
b0 = 1 PREVENTS ECHO OF DATA COMMON TO 201 MODEM IN DIAL UP.
b1 = 1 PREVENTS SYN INSERTION BETWEEN BSC MESSAGE BLOCKS.
b2 = NOT USED
b3 = 1 PREVENTS SYN INSERTION IN QUANTITY OF BSC *CHARACTERS* SPECIFIED BY CD.
b3 = 0 PREVENTS SYN INSERTION IN THE QUANTITY OF NETWORK PORT *FRAMES* SPECIFIED BY CD

10 OPERATION MODE *(continued)*

b4 = 1 STRIPS LEADING SYN FROM MESSAGE BLOCKS.
b5 = 1 FOR ADJACENT PORTS, PREVENTS DUPLICATE MESSAGE BLOCKS (NOT FOR PROTOCOLS SENDING CONSECUTIVE BLOCKS.)
b6 = 1 FOR ADJACENT PORTS, STRIPS PAD CHARACTERS AT TRANSMITTING PORT AND RESTORES THEM AT RECEIVING PORT.
b7 = NOT USED

11 CHARACTER DELAY

ACTUAL VALUE IS 0-255

12 FLYBACK

TWO HEX CHARACTERS CORRESPONDING TO CARRIAGE RETURN AS FOLLOWS:
0D = EBCDIC, ODD-PARITY ASCII, 7-BIT ASCII
8D = EVEN-PARITY ASCII, 8-BIT ASCII
6D = SELECTRIC, EBCD
08 = BAUDOT, 6-BIT TYPESETTER

13 AUTOSPEED RECOGNITION CHARACTER

SEE 6030/6040 OPERATION MANUAL FOR LIST.

14 AUTOSPEED SUBSTITUTION CHARACTER

ANY CHARACTER IN HEX CODE.

15 FIFO-SIZE

TRUNK SPEED	FIFO VALUE
1200	32
2400	64
4800	128
9600	256

16 STATISTICS

E = ENABLED D = DISABLED

17 MODE

N = NORMAL (FDX)
L = LOCAL LOOPBACK
R = REMOTE LOOPBACK

18 ARQ FRAMES

ACTUAL VALUES ARE 7, 15, 31, 63, 127

19 ADJACENT NODE

ACTUAL NUMBER OF ADJACENT NODE TO WHICH DATA IS TRANSMITTED

20 ADJACENT PORT

ACTUAL NUMBER OF ADJACENT PORT TO WHICH DATA IS TRANSMITTED

21 SLOT WEIGHT

TERMINAL SPEED	SLOT WEIGHT
150 BPS OR LESS	1
300 BPS	2
600 BPS	3
1200 BPS	6

21 SLOT WEIGHT *(continued)*

2400 BPS (ASYNC)	12
(SYNC)	16
4800 BPS (SYNC)	32
9600 BPS (SYNC)	64

22 ADJACENT NODE

ACTUAL NUMBER OF ADJACENT NODE FROM WHICH DATA IS RECEIVED

23 ADJACENT PORT

ACTUAL NUMBER OF ADJACENT PORT FROM WHICH DATA IS RECEIVED

NODAL PARAMETERS

ACTIVITY A =		
TIME CONSTANT (1-240)	T =	
REPORT DESTINATION NODE (# #)	RN =	
REPORT DESTINATION PORT (# #)	RP =	
BUFFER MULTIPLIER	B =	

SUGGESTED VALUES:
T 1
RP 0
B 5
NOTE: FOR RP, 0 = OPERATOR'S CONSOLE

THRESHOLDS (%) T =		
NETWORK PORT ERROR DENSITY	ED =	
TERMINAL PORT COMPRESSION EFFICIENCY	CE =	
TERMINAL PORT CHARACTER ERROR RATE	ER =	
BUFFER UTILIZATION	BU =	
PROCESSOR LOADING	PL =	
RETRANSMISSION RATE, FRAMES/SEC	RR =	

SUGGESTED THRESHOLDS:
ED 3%
CE 100%
ER 3%
BU 90%
PL 90%
RR 7 FRAMES/SEC

ADDENDUM A

6030/6040 POWER SUPPLY ASSEMBLIES

AD.1 GENERAL

The external power supply shown in Figure AD-1 provides both ac and dc power requirements for the 6030/6040 Series INPs. It consists of a rack-mounted chassis that includes a power supply module, ac and dc distribution brackets, a transformer, and a relay.

Two models of the power supply are available: the dual +5 Vdc output assembly 37317G01 and the single +5 Vdc output assembly 37317G02. Both models are capable of meeting the power requirements of the 6030/6040 mainframe and two port nests. An auxiliary power supply is required for additional port nests: 37317G01 supports up to six port nests; 37317G02 provides power for up to four.

The assembly is installed in the rear of the equipment rack which must be equipped with intermediate rails to meet the mounting requirements of the power supply (refer to Figure AD-5). All Codex-supplied cabinets with 6030/6040 equipment have the required rails for the 6030/6040 mainframe, port nests, and external power supply. Equipment racks not having adjustable rails are not recommended. In the event that a cabinet must have intermediate rails installed, consult a Codex Applications Engineer about retrofitting.

AD.2 DESCRIPTION

The power supply assembly is made up of two parts, an ac distribution section and a dc distribution section, which are described separately in the following paragraphs.

AD.2.1 AC DISTRIBUTION

The ac power distribution consists of a transformer, relay, and an ac distribution bracket. The transformer is used to supply the low voltage for remote turn-on and to support the 115V fans for both 115 and 230 Vrms operation. The relay is a 4-pole, normally open, 24 Vac solenoid in which three of the four contacts are used; one for the power supply, and the other two for the fans.

The ac distribution bracket shown in Figure AD-2 contains three connectors (J8, J9, and J10), a 2-position slide switch (S2), a fuse (F1), a terminal board

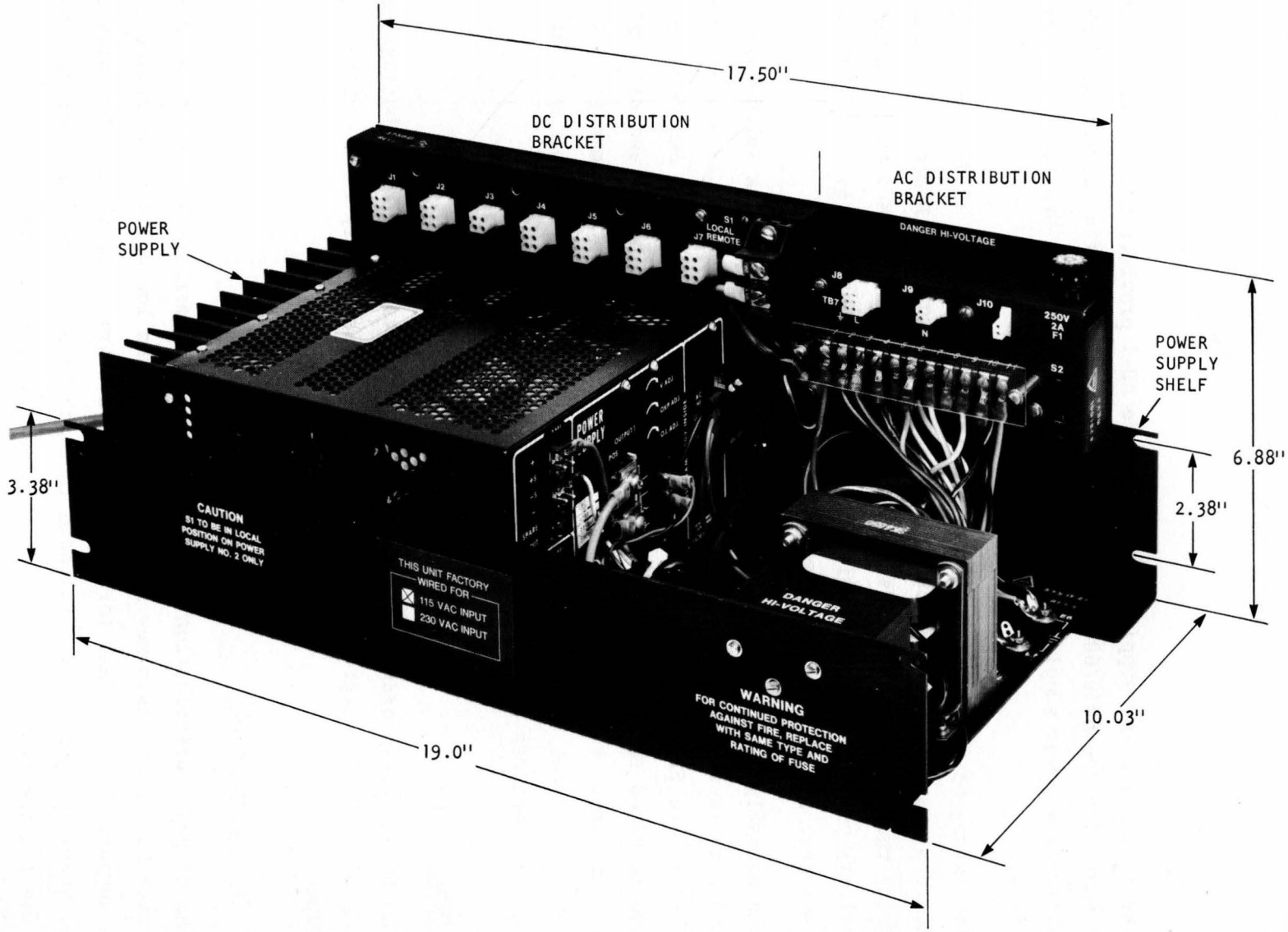


Figure AD-1. 6030/6040 Series INP's External Power Supply Assembly

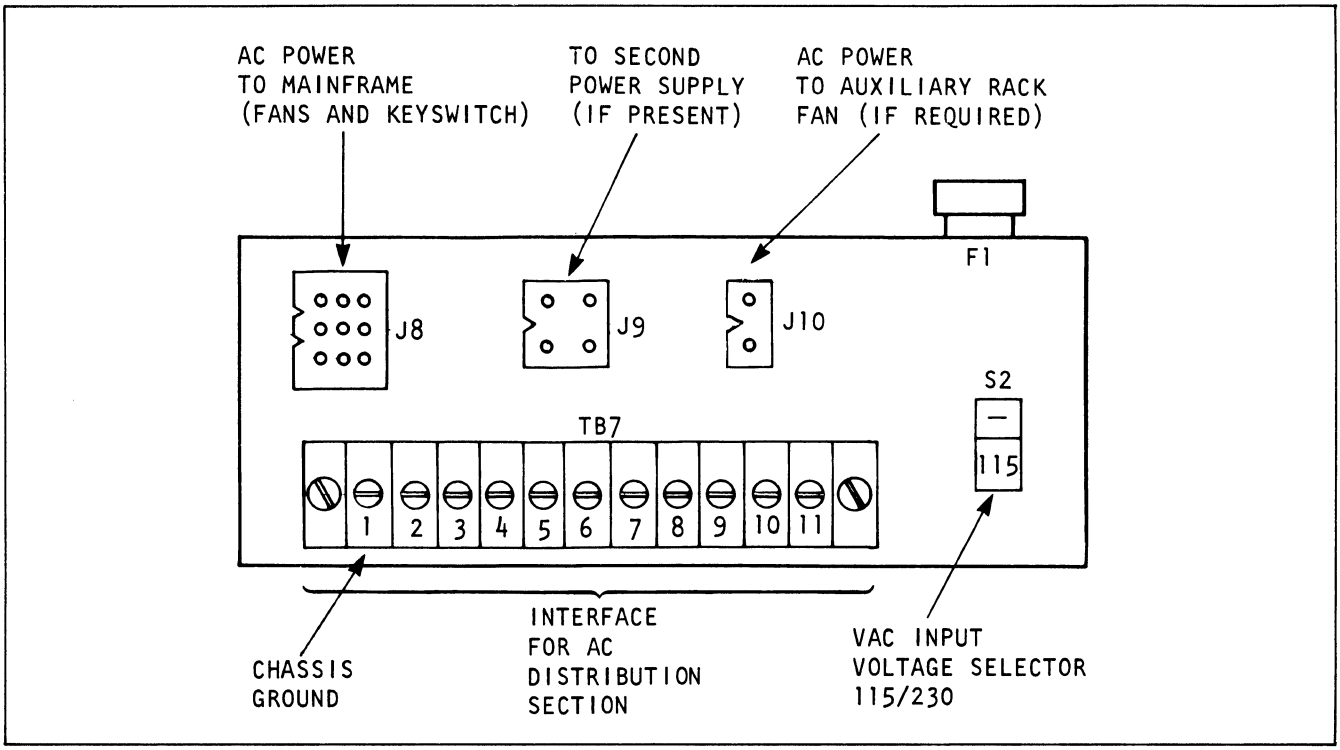


Figure AD-2
Ac Distribution Bracket

(TB7, and an isolated terminal (E5). Connector J8 is used to supply ac power to the fans in the mainframe and to the solenoid for the remote turn-on switch. J9 is used to connect a second power supply assembly's relay control winding in parallel with the primary power supply assembly so that both may be controlled by the remote turn-on switch. Connector J10 supplies 115 Vrms to power a rear-mounted fan assembly (if required).

The fuse on the ac distribution bracket provides protection for the transformer and cooling fans. Slide switch S2 selects the transformer's primary wiring configuration for either 115 or 230 Vrms operation.

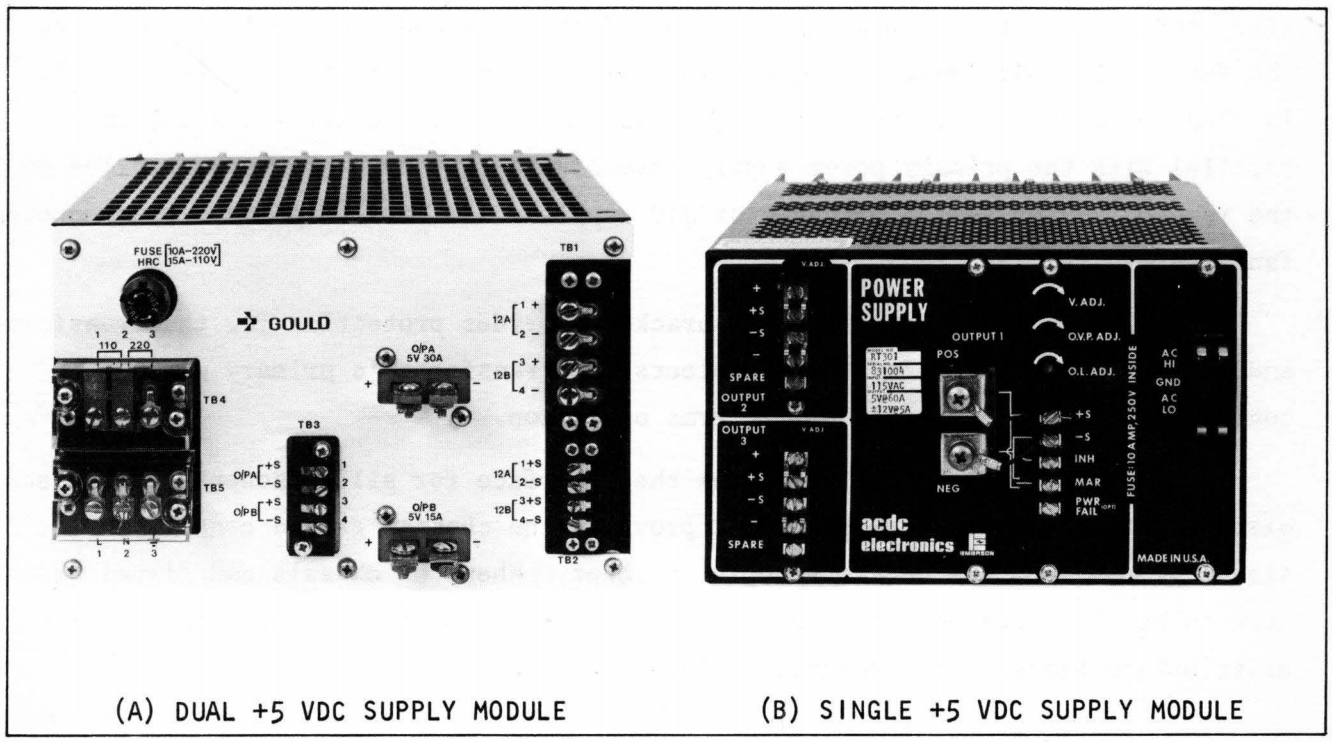
The terminal board (TB7) provides the interface for all components of the ac distribution section. Terminal TB7-1 provides the chassis ground connection for signal ground from the dc distribution bracket. When the chassis and signal grounds need to be tied together, a green wire with a yellow stripe coming from the dc distribution bracket is connected to TB7-1.

If the chassis and signal grounds must be isolated, then the wire is connected to E5 which is insulated from chassis ground. Terminals E6 and E7 are chassis ground connections for the entire power supply assembly.

AD.2.2 DC DISTRIBUTION

The dc power distribution consists of a purchased power supply module and a dc distribution bracket. Two types of power supply modules are available, based on the power requirements of the model 6030/6040 INP ordered. They include a dual +5 Vdc output and a single +5 Vdc output module (see Figure AD-3).

When used as the primary power supply, the dual +5 Vdc output assembly (37317G01) provides a +5 Vdc supply for the mainframe and another +5 Vdc output supply for two port nests. When 37317G01 is used as a second supply, the +5 Vdc output used for the mainframe can support up to four port nests (connectors J4-J7). These connectors must be used first, before connectors J1 and J2 can be connected to port nests 5 and 6. Two +12 Vdc outputs support additional system power requirements.



(A) DUAL +5 VDC SUPPLY MODULE (B) SINGLE +5 VDC SUPPLY MODULE

Figure AD-3. Types of Power Supply Modules

The single +5 Vdc output power supply assembly (37317G02) provides just +5 Vdc supply to support the mainframe and two port nests. When used as a second supply, a maximum of four port nests can be supported. Two +12 Vdc outputs are also provided for additional system support.

The dc distribution bracket shown in Figure AD-4 contains seven connectors (J1 through J7), a terminal board (TB6), and a 2-position slide switch (S1). For 37317G01, connectors J1, J2, J4, J5, J6, and J7 supply power to the port nest when the power supply assembly is used as a second supply. For 37317G02, connectors J1 and J2 do not have +5 Vdc connected, and therefore cannot be used for port nest support. In both assemblies, connector J3 contains both the positive and negative 12-volt supply and the remote sense for the +5 volts to the mainframe.

CAUTION

For 37317G01, J1 and J2 port nest connections should be used when the mainframe is connected to the power supply assembly. For 37317G02, J4 and J5 are port nest connections when the mainframe is connected.

Terminal board (TB6) provides the interface for +5 Vdc to the mainframe (the red lead supplies +5 Vdc).

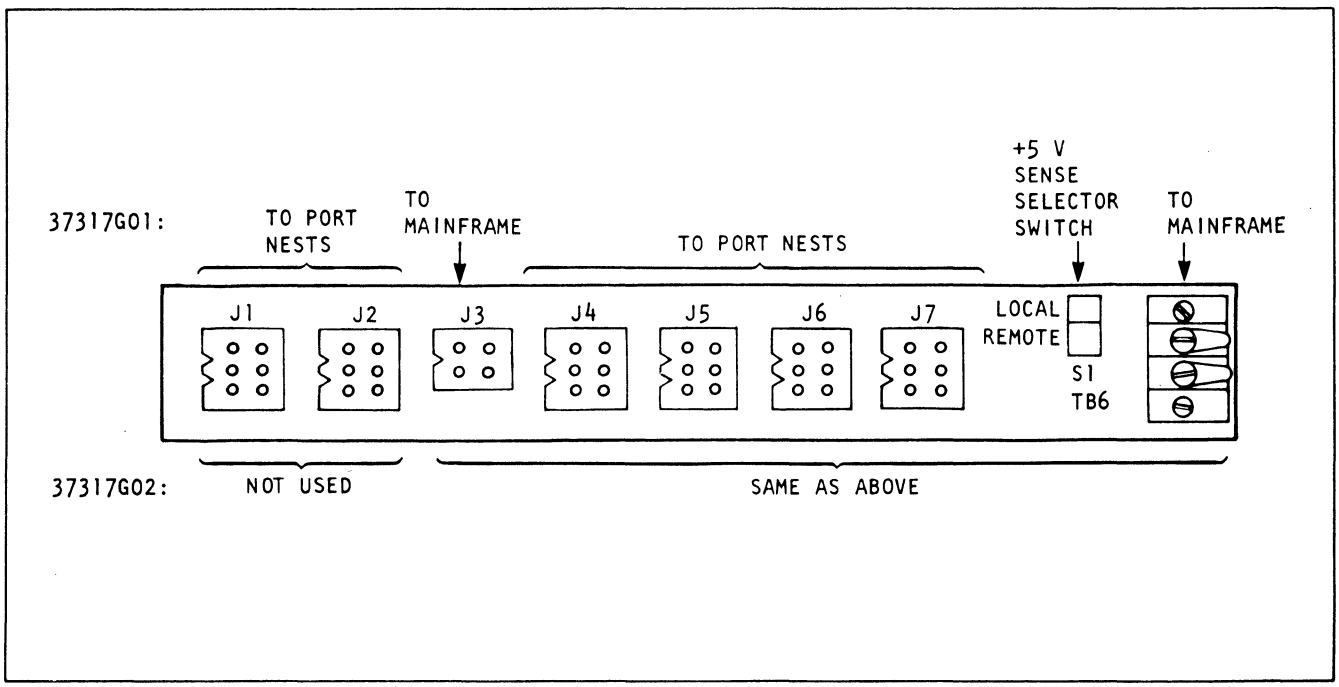


Figure AD-4. DC Distribution Bracket

The 2-position slide switch (S1) selects the location of the +5 V sense. In the remote position, the 5 volts are sensed in the mainframe. In the local position, the 5 volts are sensed at connectors J4 through J7.

AD.3 INSTALLATION

Installation of the power supply assembly is accomplished by positioning the unit in place, and then connecting the appropriate cables. This section provides the information required to plan and accomplish the mechanical and electrical installation of the assembly. Service personnel should become familiar with the complete installation procedure before attempting to install the unit.

AD3.1 TOOLS/EQUIPMENT/MATERIAL REQUIRED

The following tools and equipment should be available for use during installation.

a. Standard field service tool kit.
b. Digital voltmeter.

AD.3.2 MECHANICAL INSTALLATION

The power supply assembly is designed for installation in the rear of a 19-inch Codex-supplied equipment that has intermediate rails (see Figure AD-5). Users who already have 6030/6040 equipment installed in a Codex rack with these rails meet the mounting requirements of the external power supply. For a cabinet that must have intermediate rails installed, consult a Codex Applications Engineer about retrofitting.

Mechanical installation is illustrated in Figure AD-6 and accomplished as follows:

NOTE

The external power supply and its shelf is secured to the rails by the following pieces of equipment normally found in the rack cabinet.

Speed Nuts: P/N 02502
Screws: P/N 04355
or
Black Screws: P/N 34645-01
Black Washers: P/N 03145

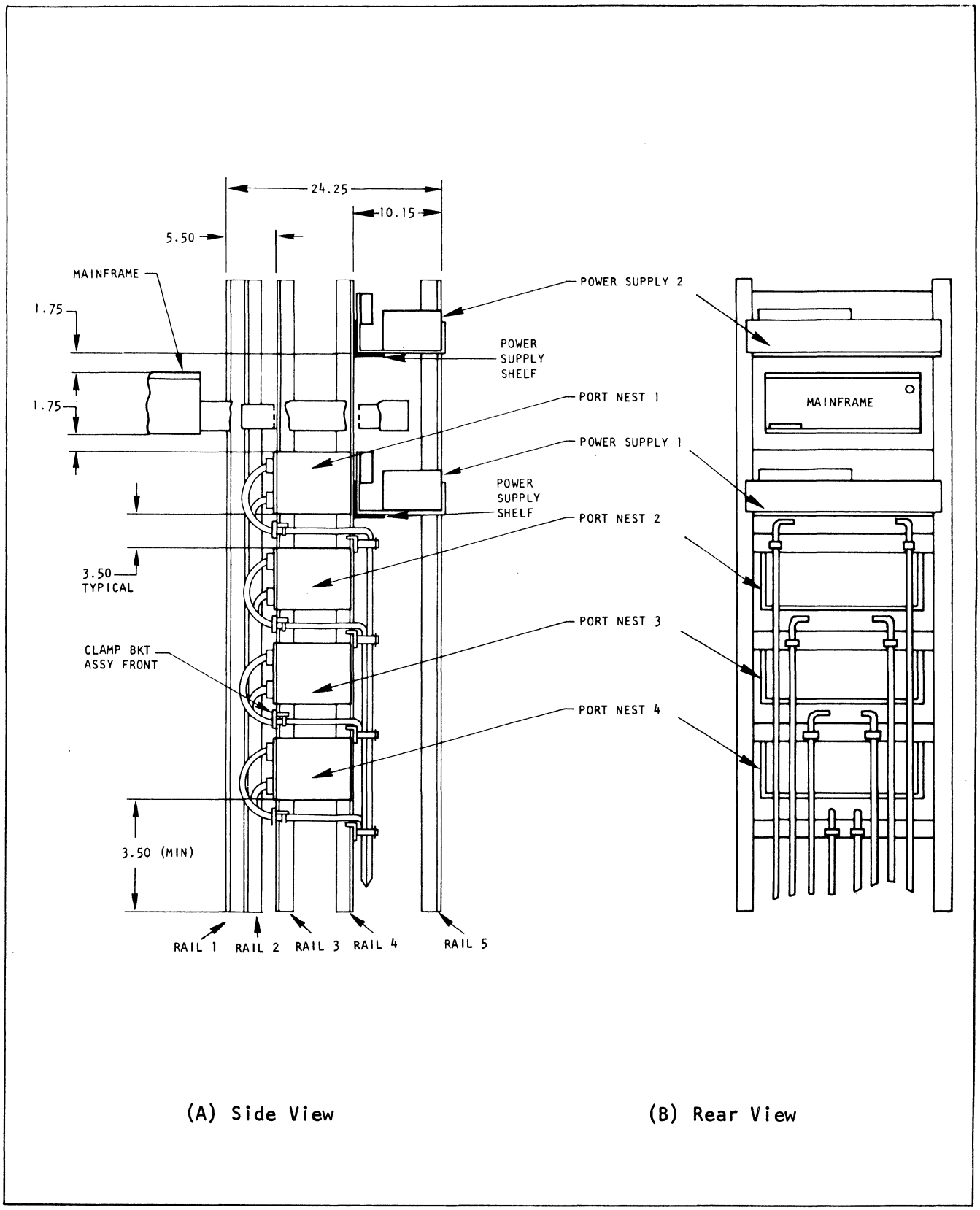


Figure AD-5. Typical Rack Configuration

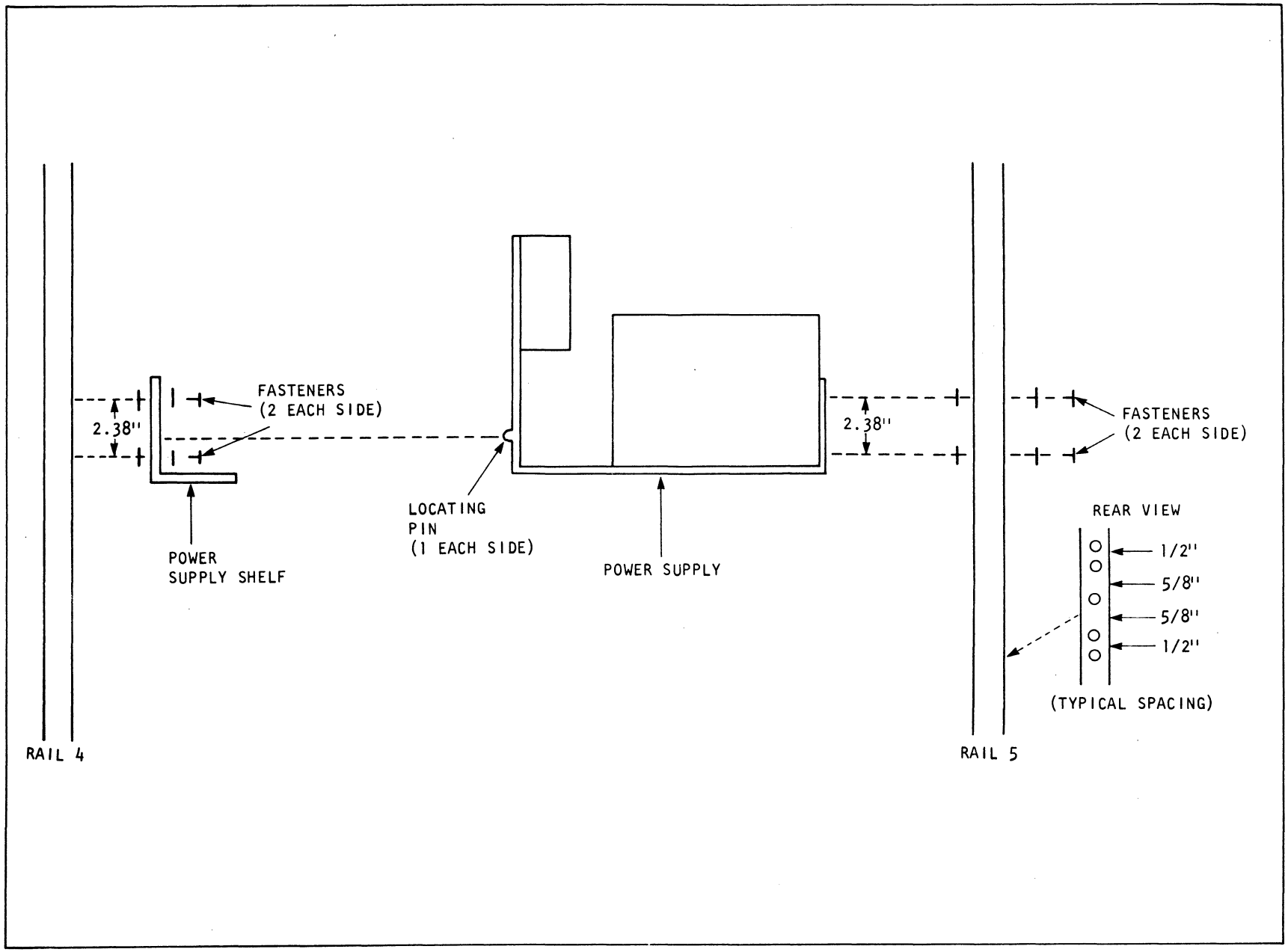


Figure AD-6. Mechanical Installation, Side View

a. Secure the power supply shelf bracket to rail pair #4 of the equipment rack by four speed nuts, washers, and screws in the angle brackets in the following positions:

1. For Power Supply 1 (located behind Port Nest 1): the bottom of the shelf should be flush with the bottom of Port Nest 1.

NOTE

This power supply furnishes power for the mainframe and two port nests.

2. For Power Supply 2 (located at the top of the rack): the bottom of the shelf should be 1.75" (4.45 cm) higher than the mainframe's top cover.

NOTE

A 37317G01 supply furnishes power for up to 6 additional port nests.
A 37317G02 supply furnishes power for up to 4 additional port nests.

b. Place the external power supply assembly on the support shelf, using the locating pins on the back of the power supply to ensure proper positioning.

c. Secure the power supply to rail pair #5 by fasteners in the angle brackets.

AD.3.3 ELECTRICAL INSTALLATION

Electrical installation consists of connecting all cables and wires to the appropriate connectors. Figures AD-7 and AD-8 depict the cabling configuration for power supply assembly 37317G01 and 37317G02, respectively (see Table AD-1). Connectors J1 through J5 support different functions based on the power supply assemblies unless otherwise specified.

NOTE

For 37317G01, connectors J1 and J2 support port nests when the power supply assembly is connected to a mainframe. For 37317G02, J4 and J5 provide support for port nests when the power supply assembly is connected to a mainframe.

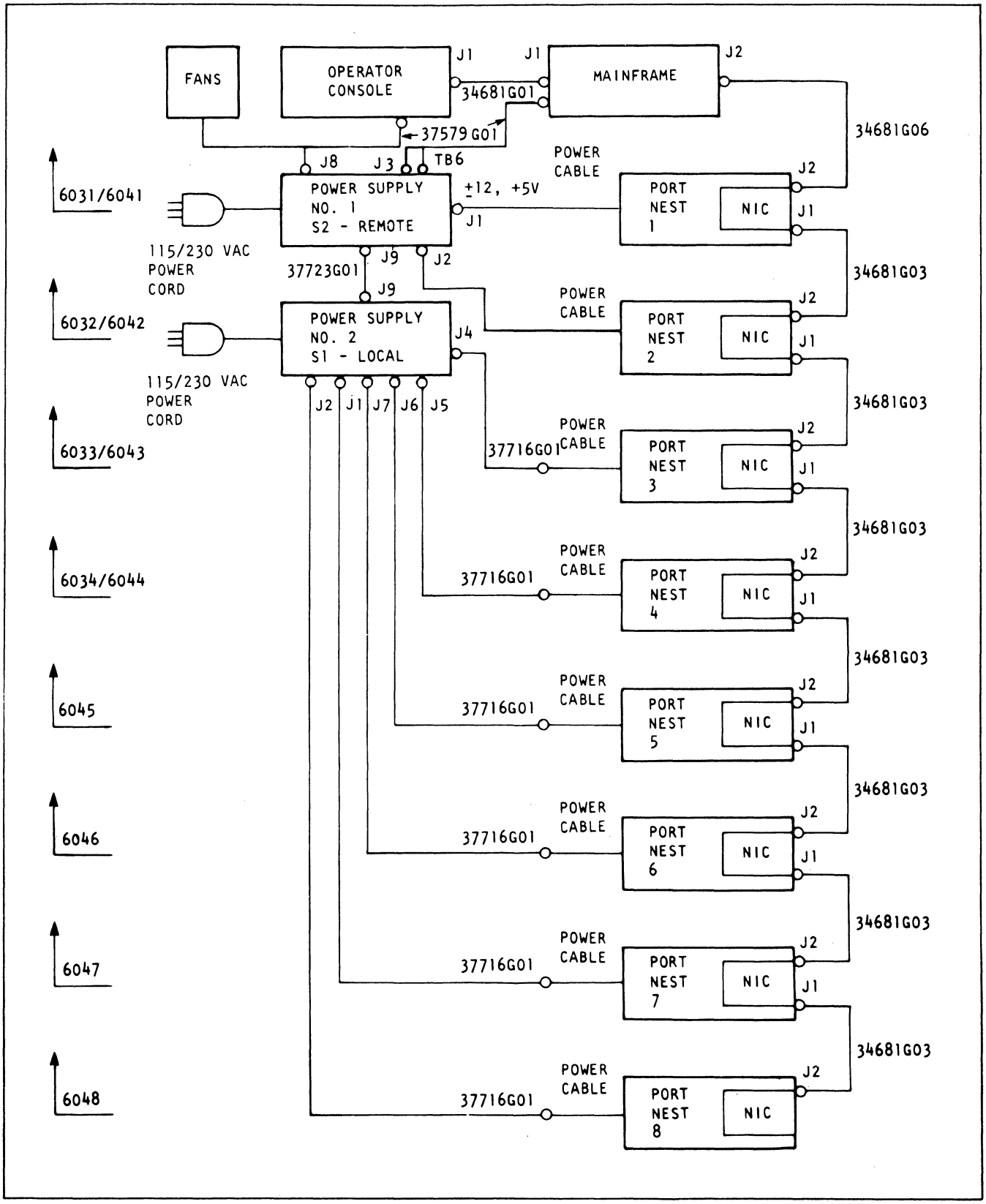


Figure AD-7. Cabling and Connections for 6030/6040 Series INP's with Power Supply Assembly (37317G01)

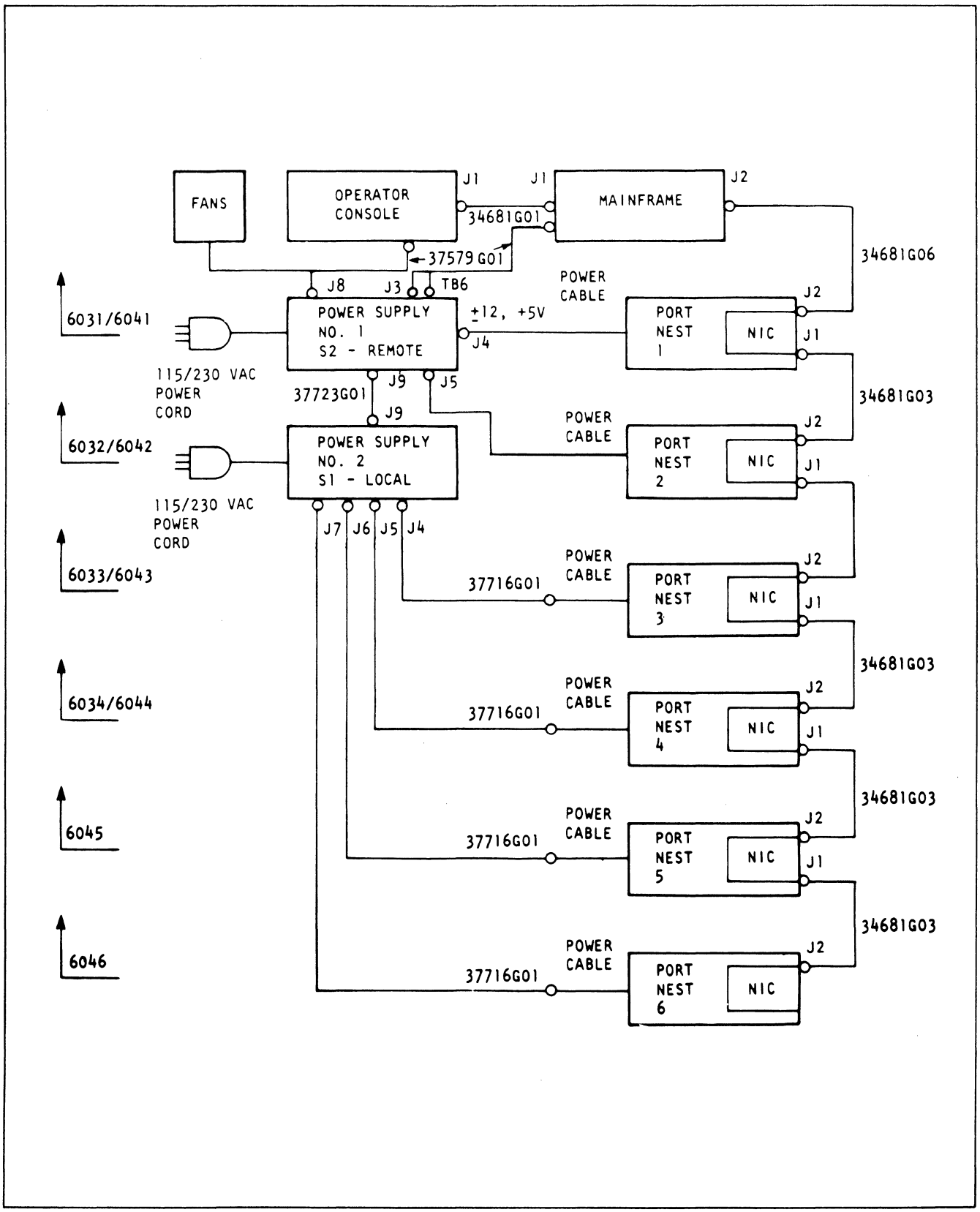


Figure AD-8. Cabling and Connections for 6030/6040 Series INP's with Power Supply Assembly (37317G02)

TABLE AD-1. INTERCONNECT GUIDE

Connector	Function
J1	Supports port nest for 37317G01; for 37317G02, this connector is not used.
J2	Supports port nest for 37317G01; for 37317G02, this connector is not used.
J3	Supports mainframe dc voltage requirements for both the 37317G01 and 37317G02.
J4	Supports port nest when 37317G01 is used as a second supply; for 37317G02, this connector supports a port nest.
J5	Supports port nest when 37317G01 is used as a second supply; for 37317G02, this connector supports a port nest.
J6	Supports port nest when used as a second supply.
J7	Supports port nest when used as a second supply.
J8	Supports mainframe ac voltage requirements.
J9	Used to interconnect two power supply assemblies.
J10	Supports an auxiliary rack fan (if required).
TB4	110/220 Vrms straps on the dc supply module (37317G01 only).
TB6	+5 Vdc interface to mainframe.
TB7	Interface for ac distribution throughout assembly.
E5	Insulated terminal for signal gound at the ac distribution bracket.
E6	Chassis (earth) ground.
E7	Chassis (earth) ground.

To configure the power supply assembly for either 115 or 230 Vac power input, set switch S2 on the ac distribution bracket and the external strap TB4 for 37317G01 or the internal strap for 37317G02 to the proper position. Connectors J3, J8 and TB6 support the mainframe and J1 and J2 of 37317G01 or J4 and J5 of 37317G02 support the two port nests.

NOTE

When connecting mainframe cable 37579G01 to the power supply, clamp the cable as shown in Figure AD-9 using the clamp assembly.

CAUTION

When 37317G01 is used as a second supply, connectors J4 through J7 must be used first, with J1 and J2 used only for connection to port nests 5 and 6.

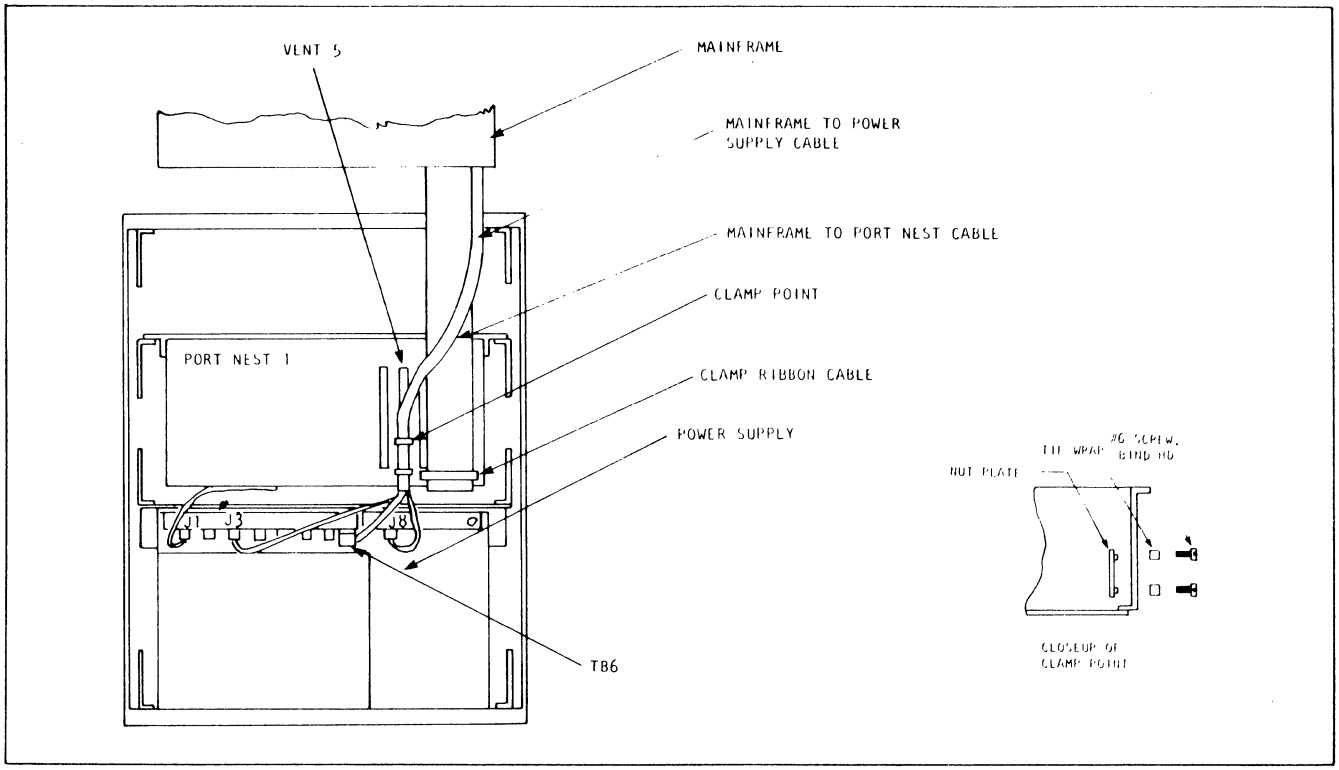


Figure AD-9. Mainframe Cable Routing

When used as a second supply, 37317G01 will support a maximum of six port nests and 37317G02 will support a maximum of four nests. Connector J9 is cabled to J9 of the first supply and switch S1 on the dc distribution bracket should be set to the LOCAL position. If this switch is not in the LOCAL position, the +5 Vdc supply for connectors J4 through J7 will not be regulated. Port nests are connected to J4 through J7, J1, and J2 for 37317G01 and to J4 through J7 for 37317G02.

AD.4 MAINTENANCE

The power supply assembly requires no special maintenance to keep it in good working order when operated in an environment free from extremes of temperature, humidity, appreciable shock, and vibration. However, the operator can perform routine inspections at varied intervals to ensure that the ac line cord and interconnect cabling are free of cuts, cracks, or any other damage. He should also inspect each terminal board connection for signs of corrosion.

AD.4.1 FIELD SERVICE REPAIR/REPLACEMENT

Field repair of defective power supply assemblies to the component level is not recommended. The major objective of effective maintenance is to restore the system to operational status as soon as possible; therefore, it is recommended that faulty power supply assemblies be entirely replaced with a spare unit.

AD.4.2 RETURN OF UNITS

Defective units must be returned to Codex Corporation, Department ERR, 100 Hampshire St., Mansfield, Massachusetts 02048, for repair. An equipment repair tag, indicating the type of failure, part number, etc., should be attached to each returned unit (see Figure AD-10).

codex corporation

EQUIPMENT REPAIR TAG

CUSTOMER _____

PART DESCRIPTION _____ REV. _____ I.D. NUMBER _____

DATE ____/____/____ P.S.O. _____ ENG. EVALUATION _____

FAILURE SYMPTOMS _____

_____

_____

FIELD SERVICE ENG. _____

EQUIPMENT ORDER TYPE _____ NUMBER _____

DEFECT _____

DATE ____/____/____ TECHNICIAN _____

C206 8-78 10M SB

Figure AD-10. Equipment Repair Tag

codex
corporation

CODEX CORPORATION
20 Cabot Blvd., Mansfield, MA 02048
Tel: (617) 364-2000 - Telex: 92-2443

CODEX INTELLIGENT TERMINAL SYSTEMS OPERATION
Tempe, Arizona

CODEX EUROPE S.A.
Brussels, Belgium

CODEX (U.K.) LTD.
Croydon, England

CODEX FAR EAST
Tokyo, Japan

ESE LIMITED
Rexdale, Ontario

member of
IDCMA
PRINTED IN U.S.A.