EXOS 201

Intelligent Ethernet Controller For Multibus Systems

Reference Manual

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EXOS 201
Intelligent Ethernet Controller
For Multibus Systems
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MANUAL REVISION HISTORY

MANUAL REVISION	DATE	SUMMARY OF CHANGES
A	02-08-85	Initial Release. EXOS 201 Ethernet Front-End Processor For Multibus Systems Reference Manual Publication No. 4200006-00
B	03-12-85	Reprint of Manual Revision A using laser printer.
C	06-05-86	Manual Revision C Release. Several technical and editorial changes. Changed product name to EXOS 201 Intelligent Ethernet Controller. Restructured the manual to include predominantly hardware information, which remains unchanged. NX 200 firmware information moved to a separate manual.

PREFACE

This manual describes the EXOS 201 Intelligent Ethernet Controller board. It covers information necessary to integrate the EXOS 201 board in a Multibus system. The manual is intended to be used only as a reference manual and does not undertake to explain the product's design philosophy.

The Ethernet and Multibus standards are described in readily available documents; this manual makes no special effort to explain them.

Excelan supplies several TCP/IP protocol software packages (suitable for use with different operating systems) that can execute on EXOS 201. Alternatively, users can design their own protocol and applications software.

For users who wish to design their own software, EXOS 201 provides the on-board, EPROM-resident NX 200 Network Executive, which includes a dedicated operating system kernel and a network services manager. By design, NX 200 insulates user protocol software from hardware implementation details. This approach simplifies software design and facilitates portability to future products, which will take advantage of latest hardware technologies.

Detailed documentation for the NX 200 Network Executive is available from Excelan, Inc. See [7] below.

The documents listed below provide related reference and study material for EXOS 201 users.

EXOS 201 conforms to the following specification:

[1] *The Ethernet: A Local Area Network: Data Link Layer and Physical Layer Specifications*, DEC, Intel, and Xerox Corporations, 1980.

[2] *The Ethernet: A Local Area Network: Data Link Layer and Physical Layer Specifications, Version 2.0*, DEC, Intel, and Xerox Corporations, 1982.

[3] *Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications (Standard 802.3-1985/International Standard 8802/3)*,
The Institute of Electrical and Electronics Engineers, Inc., 1985.

EXOS 201 conforms to the Multibus specifications, which are described in the following document:

[4] *Intel Multibus Specifications Manual*, Order Number 9800683-04, Intel Corporation, 1982.

EXOS 201 uses the Intel 82586 LAN Coprocessor for implementation of Ethernet Data Link protocol. This coprocessor is described in the following document:

[5] *LAN Components User's Manual*, Document No. 230814-001, Intel Corporation, 1984.

EXOS 201 supports front-end processing of user-written higher-level protocols, which executes on an Intel 80186 CPU. This CPU is described in the following manual:

[6] *iAPX 86/88, 186/188 User's Manual*, Document No. 210911-001, Intel Corporation, 1983.

User-written protocol software must use the on-board, EPROM-resident NX 200 Network Executive, which is described in the following manual:

[7] *NX 200 Network Executive, Reference Manual*, Publication No. 4200036-00, Excelan, Inc., 1986

The following reference describes the C language, which is used for procedural specifications in this manual:

[8] Kernighan, B.W. and Ritchie, D.M, *The C Programming Language*, Prentice-Hall, Englewood Cliffs, New Jersey, 1978.

The following reference describes the ISO Open Systems Model:

[9] *Reference Model of Open Systems Interconnection*, Document no. ISO/TC97/SC16 N227, International Organization for Standardization (ISO), 1979.

For optimum accuracy, this manual should be used in conjunction with the Release Notes supplied with the product described in this manual.

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Chapter 1
INTRODUCTION

1.1. INTRODUCTION

The EXOS 201 Intelligent Ethernet Controller is a high-performance, front-end communications processor board that connects a Multibus system to an Ethernet* or IEEE 802.3 local area network. It implements the complete Ethernet Data Link Layer interface, with significant functional extensions, on a single Multibus board.

The EXOS 201 board can be used both as an intelligent front-end processor and as a link-level controller. When used as a front-end processor, it executes the high-level network protocols on the board, thereby offloading this burden from the host CPU. When used as link-level controller, it provides the standard Ethernet Data Link interface to the host system. Sections 1.1.1 and 1.1.2 briefly describe the two modes.

The EXOS 201 board is designed around three major on-board hardware components and one firmware component. The hardware components are an Intel 80186 CPU, an Intel 82586 LAN Coprocessor, and dual-port RAM (either 128, 256, or 512 Kbytes). The firmware component is the EPROM-resident NX 200 Network Executive, also referred to as the NX 200 firmware.

The 80186 CPU executes the protocol software, which is downloaded to the board, and the on-board NX 200 firmware. The 82586 LAN Coprocessor implements part of the Data Link layer. The RAM provides space for downloading protocol software and for buffering packets. The NX 200 firmware provides diagnostics, interfaces to host memory and the LAN coprocessor, and operating system environment for execution of the downloaded protocol software. The NX 200 firmware also provides link-level controller functions.

The host Multibus system and the EXOS 201 board primarily communicate through command and reply messages located in host memory, which is accessible from the Multibus. The NX 200 firmware interprets the command messages and generates the replies.

1.1.1. EXOS 201 in Front-End Mode

In the front-end processor mode, the host system downloads protocol software to EXOS 201 at initialization time (or EXOS 201 bootstraps itself from the Ethernet). This software then uses NX 200's real-time, multitasking process management services and I/O drivers to control EXOS 201's Ethernet interface and to manage communications with the host system.

Standard protocol modules for EXOS 201, such as the DARPA TCP/IP protocols, are available from Excelan. Figure 1-1 shows the relationship between these modules and the Open Systems Interconnection (OSI) reference model of the International Standards Organization (ISO).

Alternatively, users can develop or port their own protocols to run on EXOS 201 under NX 200.

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*Please note that in this manual the term Ethernet refers to both Ethernet and IEEE 802.3.

Programming information required to write protocol software that runs on the EXOS 201 board is detailed in the *NX 200 Network Executive Reference Manual.*

1.1.2. EXOS 201 in Link-Level Mode

In the link-level mode, the NX 200 firmware brings EXOS 201's Data Link controller functions to the host interface. The host system obtains Data Link services through standard request/reply messages. In this mode, EXOS 201's RAM is entirely available for buffering packets. The link-level controller mode is useful for applications where host-resident protocol software has already been developed or where it is otherwise not feasible to download high-level protocols to run on the EXOS 201 board.

Programming information required to write I/O drivers to interface host-resident protocol software to the NX 200 Data Link functions is detailed in the *NX 200 Network Executive Reference Manual.*

1.1.3. Manual Organization

This manual is organized as follows:

Chapter 1, Introduction, provides an overview of the EXOS 201 features and functions.

Chapter 2, Hardware Reference, describes the architecture of the EXOS 201 board and the functions of various on-board components.

Chapter 3, Installation, discusses how to install the EXOS 201 board in a generic Multibus system and then connect the system to a network.

Chapter 4, Service Information, details procedures on how to obtain factory service for the EXOS 201 boards.

Appendices A through C provide Component and Jumper Layout, Schematics, and Transceiver Pin-outs, respectively.

1.2. EXOS 201 HARDWARE

Figure 1-2 shows a block diagram of EXOS 201. Architecturally, EXOS 201 consists of two loosely coupled elements: an Ethernet Data Link Layer controller, and a microprocessor-based protocol processing engine. These components communicate with each other through an internal bus and 128, 256, or 512 Kbytes of dual-port RAM.

EXOS 201 implements the Ethernet Data Link protocol using the Intel 82586 LAN Coprocessor. Functions such as address recognition, CRC check, and buffer chaining are managed in hardware, leaving the 80186 CPU fully available for front-end processing applications. The protocol-processing engine is supported by 128, 256, or 512 Kbytes of RAM. Two 16-Kbyte EPROMs contain Excelan's NX 200 firmware, which includes self-diagnostic tests, an operating system kernel, host and network interfaces, and network bootstrap code.

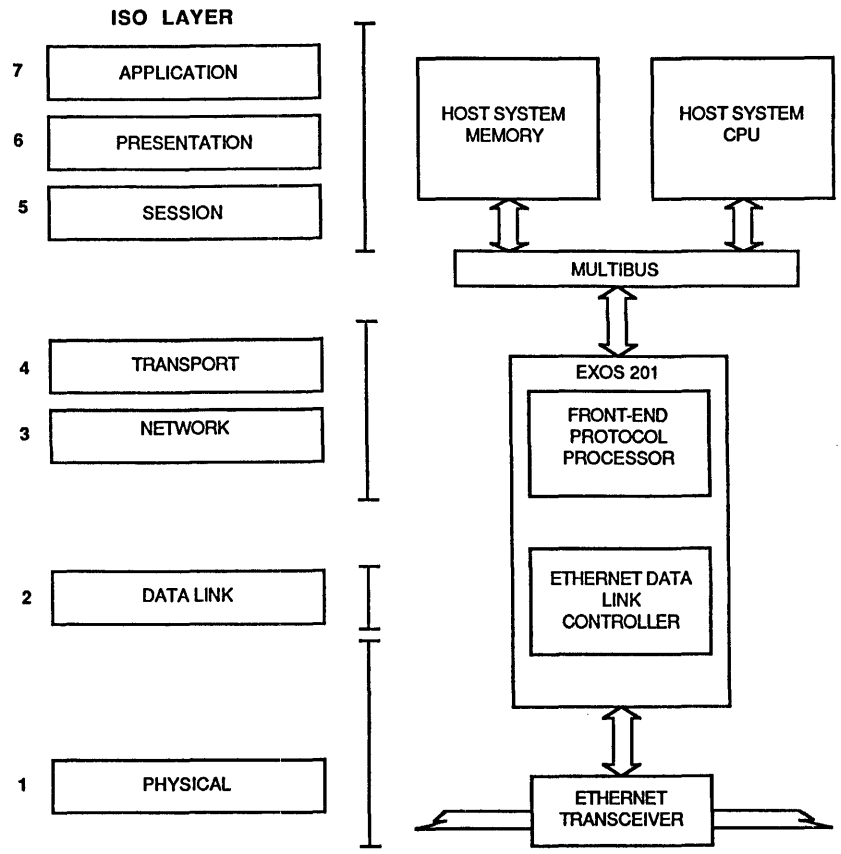


Figure 1-1: The EXOS 201 Front-End Mode Implementation and ISO/OSI

1.2.1. Principal Hardware Features

The following are the salient features of the EXOS 201 board.

- Single 6.75" by 12" Multibus board, which requires just one Multibus slot.
- On-board Intel 80186 microprocessor running at 8 MHz and 128 Kbytes of RAM on Model 2, 256 Kbytes on Model 3, or 512 Kbytes on Model 4 support high-level network protocols on-board.
- Dual-port memory allows concurrent, full-speed access by the on-board CPU and the on-board LAN coprocessor.
- Sockets for two 32-Kbyte user EPROMs allows for installing user-written code on the board.

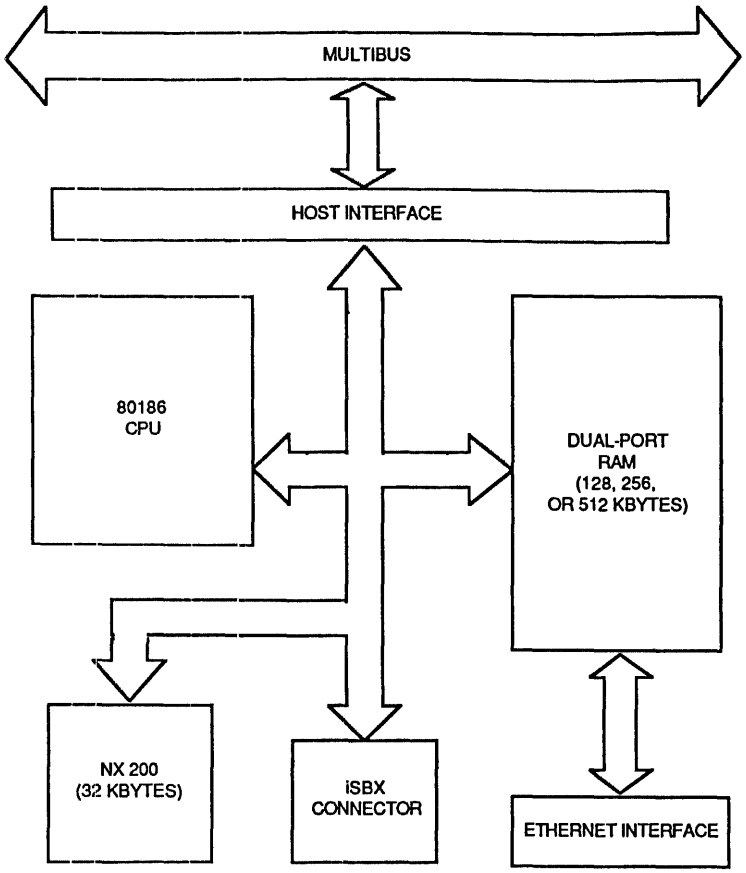


Figure 1-2: EXOS 201 Block Diagram

- Can receive successive frames with minimum interframe spacing (9.6 microseconds). Can receive immediately after transmitting, or vice versa, with minimum interframe spacing and without losing data.
- Hardware recognition of physical, broadcast, and multiple multicast addresses, in addition to promiscuous mode.
- Hardware-supported buffer chaining allows buffering of an arbitrary number of received frames without any CPU intervention. Allocation of buffers, both location and size, is completely under software control.

1.2.2. Ethernet Compatibility

EXOS 201 is fully compliant with the IEEE 802.3 standard as well as with Ethernet specifications Versions 1.0 and 2.0. Used with a standard IEEE 802.3 or Ethernet transceiver, EXOS 201 provides all Data Link and Physical layer services.

1.2.3. Multibus Compatibility

EXOS 201 conforms with Multibus/IEEE 796 specifications as a 16-bit master. Compliance is D16 M24 I16 VO L (16-bit transfers, 24-bit addressing, and non-bus-vectored interrupts).

1.2.4. Multibus Interface

EXOS 201 can access the entire Multibus system memory space (16 Mbytes) and the full 64 Kbytes of I/O space as a 16-bit bus master. An additional one-byte communication path is provided from the Multibus to the EXOS processor via an I/O port. This is used during initialization to transmit the address of a communication area in the shared Multibus memory.

EXOS 201 and host processors can interrupt each other. The board generates non-bus-vectored interrupts to interrupt the host. Interrupt priority can be set via jumper selection. EXOS 201 provides a status bit, in case interrupt polling is required. The host can interrupt the EXOS 201 processor by writing to an I/O port.

1.2.5. Ethernet Functions

EXOS 201 performs all Physical and Link Layer Ethernet functions except for transceiver functions. These include the following:

- Serial-to-parallel and parallel-to-serial conversions
- Address recognition
- Framing and unframing of messages
- Manchester encoding and decoding
- Preamble generation and removal
- Carrier sense and deference
- Collision detection and enforcement, including jamming, backoff timing, and retry
- FCS (CRC) generation and verification
- Error detection and handling

1.2.6. Address Recognition

Each board has a unique 48-bit Ethernet address, which is stored in a PROM. (The host software can override this address at run time.) Recognition of physical, broadcast, and multicast addresses is fully supported. Up to 252 multicast addresses can be assigned to a station; a very efficient filtering scheme reduces processing overhead. EXOS 201 also provides a promiscuous mode, in which it accepts all addresses.

1.2.7. Frame Format

Link-level frames are formatted as per the Ethernet specification: preamble (64 bits of synchronizing sequence), destination address (48 bits), source address (48 bits), message type (16 bits), data (46 to 1500 bytes) and FCS (32 bits). The preamble is generated and removed in hardware. Generation and checking of the Frame Check Sequence (FCS) is also handled in hardware.

1.2.8. Error Handling

EXOS 201 handles all Ethernet error conditions, including CRC, alignment, and length errors. Packets containing these errors can optionally be received.

1.2.9. High-level Protocol Support

On-board processing power supports execution of higher level communications protocols, above the Ethernet link layer. The elements of this protocol execution environment are the following:

- Intel 80186 CPU, with on-chip clock timer and interrupt controller, operating at 8 MHz
- 128, 256, or 512 Kbytes of dual-port RAM
- 32 Kbytes of EPROM containing the NX 200 Network Executive code

The on-board firmware (the NX 200 Network Executive) provides simplified Ethernet and host interface device drivers, and a multitasking environment for high-level network protocols.

1.3. NX 200 FIRMWARE – THE NETWORK EXECUTIVE

The NX 200 Network Executive, an EPROM-resident set of modules, is an integral part of EXOS 201. It contains board diagnostics, an operating system kernel, interfaces to the host and the Ethernet, and network bootstrap code. When EXOS 201 is used in front-end mode, NX 200 provides the operating system environment for the downloaded protocol software that runs on the board. When EXOS 201 is used in link-level mode, NX 200 provides the Data Link Controller functions for the protocol software that runs on the host system.

NX 200 resides in EPROM memory, which appears at the high end of the 1 Mbyte address space of the 80186 CPU. NX 200 data structures use 4 Kbytes of the RAM; the rest is available for higher-level software. Figure 1-3 provides a graphic representation of the NX 200 software architecture.

For users who use prepackaged software, such as Excelan's EXOS Series 8000 TCP/IP Network Software, existence of NX 200 is transparent. Accordingly, they need not concern themselves with the internals of NX 200.

For users who plan to write their own protocol software or link-level drivers, it is necessary to understand the NX 200 internals. A summary of NX 200 features is given in the following sections. Refer to the *NX 200 Network Executive Reference Manual* for further details.

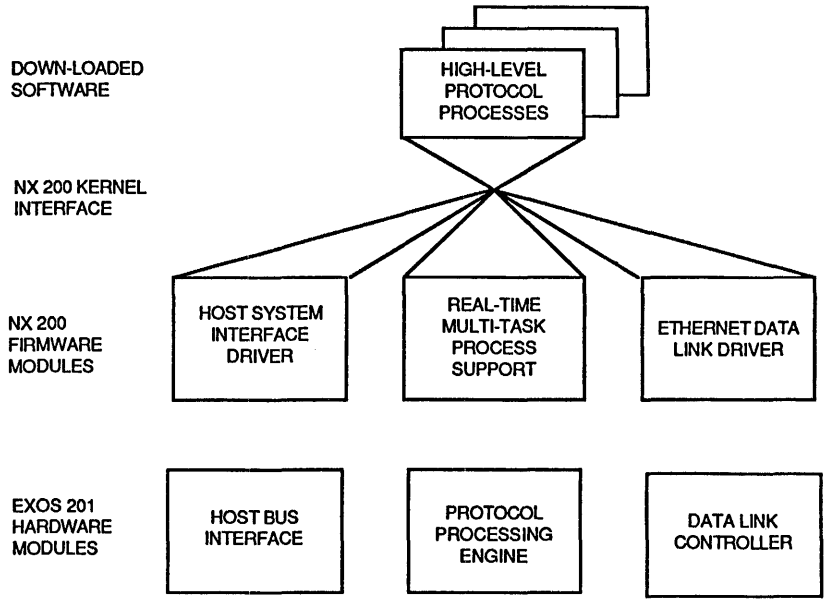


Figure 1-3: NX 200 Software Architecture

1.3.1. Principal Features of NX 200

The following is a list of the main features of the NX 200:

- Self-diagnostics for testing the integrity of the EXOS 201 hardware.
- Booting process that allows higher-level software to be downloaded either from the host or from the network.
- Real-time kernel that provides a multiasking environment, enabling the protocol software to be constructed in a structured manner as a set of cooperating processes.
- Device drivers for the Ethernet controller and host computer interface. Access through message queues simplifies pipelined communications.

- Supports network management functions by collecting network statistics.
- Allows EXOS 201 to be used as a simple Data Link controller, giving direct access to the network without downloading any software.

1.3.2. Initialization

On reset the NX 200 firmware performs a series of self tests that confirm the integrity of the hardware. In case of failure, the firmware communicates diagnostic codes through an LED display. After successful completion of the tests, EXOS 201 either boots itself from the Ethernet or awaits initialization by the host system, depending on the jumper option selected on the board.

If the jumper selects initialization by a host system, the host then uses a configuration message to select NX 200's mode of operation and specify several other parameters. It can download software directly, direct NX 200 to boot itself from the Ethernet, or select link-level controller mode. If initialization includes downloading software, then NX 200 spawns a process and enters the front-end processor mode of operation.

1.4. INSTALLATION

Installing the EXOS 201 board is a relatively simple task. In a typical Multibus system, it consists of turning off the power, accessing the card cage, inserting the board, and establishing the required connection through appropriate cables and connectors. In general, the complexity of installation procedure depends on the physical design of the host machine rather than on the design of the EXOS 201 board.

1.5. CUSTOMER SERVICE

All EXOS 201 boards, like all other Excelan products, must pass very rigorous quality control procedures before they are shipped to customers. Even so, some problems and questions are bound to come up in actual applications. Excelan maintains a highly qualified and trained customer service staff who resolve technical problems related to Excelan products and advise on procedures for shipping the product back to factory for service.

Chapter 2
HARDWARE REFERENCE

2.1. INTRODUCTION

Most of the hardware-dependent aspects of the EXOS 201 implementation are hidden by the NX 200 firmware. Therefore, this chapter discusses only those aspects which are "visible" to and are of concern to most users. These aspects include issues related to Multibus, Ethernet, on-board processing, NX 200 firmware, and jumper-selectable options. This chapter discusses these issues in detail. However, theory of operation is deliberately omitted. The schematics included in Appendix B may be referred to for further understanding of the board functions.

Multibus-related issues discussed in this chapter include bus interface, compliance, memory access, I/O access, interrupt configuration, and priority resolution.

Ethernet-related issues discussed include Ethernet interface, compliance, functions, address recognition, operation timing, packet buffering, error handling, and network connections.

The on-board processing issues encompass the resources available for high-level and link-level protocol processing.

The NX 200 firmware issues include firmware configuration, self-test, and diagnostics.

2.2. EXOS 201 COMPONENT LAYOUT

Physical layout of the EXOS 201 board, as seen from the component side, is shown in Figure A-1 in Appendix A. This figure also shows the location of various jumpers. For development purposes, the following components are socketed:

- 80186 CPU
- Two 16-Kbyte EPROMs

Note that except for the jumpers and the socketed components mentioned above, all other components are not serviceable by the user. If any operational problems are encountered, you should obtain authorized service as described in Chapter 4.

EXOS 201 provides several jumpers for selecting various options. The jumper-selectable options are described in detail in subsequent sections. Table 2-1 provides a quick reference to jumper-selectable options. (For convenience, this table is also included in Appendix A.)

EXOS 201 includes three Light Emitting Diodes (LEDs) to communicate status information. The LEDs are located in adjacent positions at the top of the board; they can easily be seen while the board is installed. Figure 2-1 shows their relative locations and functions. Subsequent sections describe the LEDs in more detail.

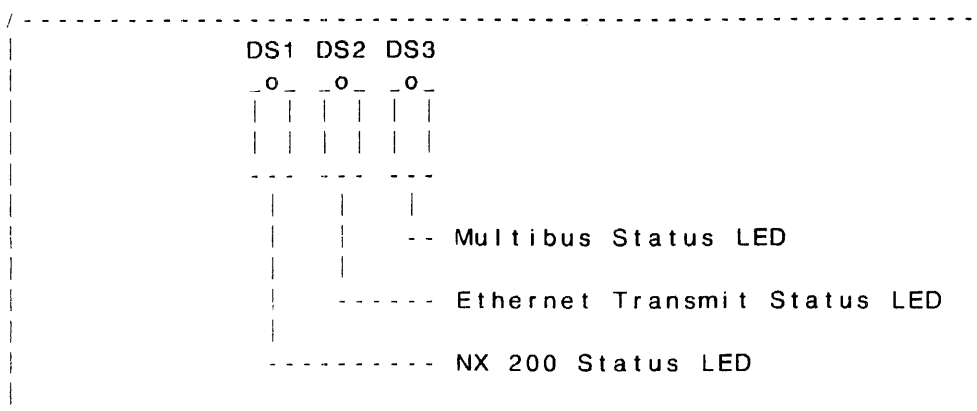


Figure 2-1: EXOS 201 Status LEDs

2.3. MULTIBUS INTERFACE

The EXOS 201 Intelligent Ethernet Controller is built on a single 6.75" by 12" Multibus board. It presents one TTL (LS) load on the Multibus.

2.3.1. Multibus Compliance

The EXOS 201 conforms to Multibus specifications as a 16-bit bus master. IEEE 796 compliance is MASTER D16 M24 I16 V0 L:

- 8-bit or 16-bit transfers
- 24-bit addressing
- Non-bus-vectored interrupts

2.3.2. Multibus Memory Access

EXOS 201 generates 24-bit memory addresses to access the entire 16 Mbytes of Multibus memory.

Note that EXOS 201's own memory is not accessible from the Multibus.

Table 2-1: EXOS 201 Jumpers

Jumper	Function (when jumper is installed)	Factory Setting
J2	Reserved	Installed
J3	Reserved	Absent
J4	512 Kbyte Memory (Model 4)	Absent
J5	Disable Carrier Sense	Absent
J6	Boot from network	Absent
J7	256 Kbyte Memory (Model 3)	Absent
J9	Reserved	Absent
J10	Reserved	Installed
J11	Disable SQE (Heartbeat) check, Ethernet Version 1.0 mode	Installed
J12	Reserved	Absent
J13	Ground IRO from iSBX	Absent
J14	Ground IRO from iSBX	Absent
J15	Enable Watchdog Timer	Absent
J50	Enable 16-bit address decode	Installed
J51	Enable 8-bit address decode	Absent
J52	(7 jumpers) Bits 1-7 of I/O port address	All absent (0)
J53	(8 jumpers) Bits 8-15 of I/O port address	All absent (0)
J54	(8 jumpers) Interrupt levels 0-7	Level 5
J55	27128 user EPROMs	Absent
J56	27256 user EPROMs	Absent
J57	Enable /BPRO output	Installed
J58	Enable response to /CBRQ	Absent
J59	Respond as if /CBRQ always active	Installed
J60	Drive /CCLK and /BCLK lines	Absent
J61	Reserved	Installed

2.3.3. Multibus I/O (Slave) Access

The EXOS 201 can access the full 64 Kbyte Multibus I/O address space. However, it does not generate any I/O commands unless requested by user software.

EXOS 201 presents two read/write host memory-mapped I/O ports – ports A and B – to the Multibus. The host can actively access EXOS 201 only through these ports. These ports are accessed over the Multibus; they can be both written to and read from. Port A's address is jumper-selectable; port B's address is the address of port A plus 1.

(Note that 68000 CPU boards, such as the SUN design, typically invert the least significant address bit so that ports A and B are logically reversed as seen by host system software.)

The effects of reading and writing ports A and B are summarized below:

Read A: Resets the EXOS 201 board

Read B: Returns the EXOS 201 status byte:

Bit 0: (Error Bit) when 0, indicates a fatal error in EXOS 201. When EXOS 201 is reset, this bit is 0

but will be set to 1 if the self-test completes successfully. If this bit is not set within 3 seconds, then EXOS 201 has failed the self diagnostics.

Bit 1: (Interrupt Bit) is set whenever EXOS 201 asserts a Multibus level interrupt. This is useful when an interrupt line is shared and polling is required. An I/O write to port A clears this bit. The interrupt bit is defined only when level interrupts are selected.

Bit 2: Undefined.

Bit 3: (Ready Bit) when 0, indicates that EXOS 201 is ready to accept a byte written to port B. When 1, EXOS 201 has not yet read the byte last written to port B.

Bits 4,5:
Undefined.

Bit 6: (Loopback Test Bit) when 0, indicates transceiver loopback test passed. When 1, indicates loopback test failed, possibly due to faulty transceiver or faulty transceiver cable.

Bits 7: Undefined.

Write A: Causes EXOS 201 to drop the interrupt line when it has asserted a non-bus-vectored interrupt on the Multibus. This also clears the interrupt bit in port B. The value written is arbitrary and is not accessible to software on the EXOS 201 board.

Write B: Interrupts the EXOS 201 CPU and communicates a 1-byte value. This is the only way to communicate a value to the EXOS 201 other than through shared memory.

As shipped from the factory, the default addresses for ports A and B are 0000H and 0001H, respectively.

The EXOS 201 board allows selecting of 16-bit addressing or 8-bit addressing. Jumper J50, when installed, selects 16-bit addressing; jumper J51, when installed, selects 8-bit addressing. However, one and only one of these jumpers must be installed.

For selecting a 16-bit address, each of the 7 jumpers in J52 and each of the 8 jumpers in J53 must be appropriately selected. For selecting an 8-bit address, only the 7 jumpers in J52 should be selected. Various address bits are jumper-selectable as follows:

Bits 8-15: Jumpers 1 through 8, respectively, in J53 select these bits.

Bits 1-7: Jumpers 1 through 7, respectively, in J52 select these bits.

Absent jumper=0; installed jumper=1.
(Factory setting is all jumpers absent, that is, each bit is a 0.)

Bit 0: Always decoded as a 0 for port A and as a 1 for port B.

2.3.4. Multibus Interrupt Access

EXOS 201 can assert non-bus-vectored interrupts on the Multibus. Interrupt priority is jumper-selectable in the range INT0 to INT7. Only one interrupt level should be selected, or malfunction will result. The jumpers in J54 select the interrupt levels as illustrated below:

J54 Jumper number	1	2	3	4	5	6	7	8
Interrupt level	7	6	5	4	3	2	1	0

As shipped from the factory, interrupt level 5 is selected.

EXOS 201 can also be initialized to generate memory-mapped interrupts to the host. The host interrupts the EXOS 201 board by writing to an I/O port. Refer to Section 2.3.3.

2.3.5. Multibus Priority Resolution

EXOS 201 is an Option RWD (Release-When-Done) Requestor. As a bus master, EXOS 201 requests and releases the bus for each command. It executes the command immediately upon obtaining the bus and releases the bus immediately upon the command's completion. Therefore its bus load is dependent only on the performance of the Multibus slave being accessed (typically host memory).

EXOS 201 is compatible with either parallel or serial priority resolution schemes. Some Multibus implementations require disconnection of the BPRO/ line when parallel resolution is used. Jumper J57 on the EXOS 201 board, which connects the BPRO/ line to the bus interface, can be removed if required.

As shipped from the factory, jumper J57 is installed.

2.3.6. Multibus Cycle Status LED

The Light Emitting Diode (LED) in position DS3 on the EXOS 201 board, when lit, indicates that a Multibus cycle is in progress. If lit steadily, then EXOS 201 has probably attempted to access a non-existent or bad memory address on the Multibus. In general, this condition points toward a user software bug. Note that this applies only if the bus timeout feature is not selected by jumper J15.

2.4. ETHERNET INTERFACE

Integrated with a standard Ethernet transceiver, EXOS 201 performs all specified Ethernet Physical and Link layer functions.

2.4.1. Ethernet Compliance

EXOS 201 conforms fully to the IEEE 802.3 standard as well as to Ethernet specification, Versions 1.0 or 2.0.

As shipped from the factory, EXOS 201 is configured for Ethernet Version 1.0 use; for IEEE 802.3 and Version 2.0 use, jumper J11 must be removed.

2.4.2. Ethernet Functions

Ethernet functions implemented on the EXOS 201 board include the following:

- Serial/parallel and parallel/serial conversion
- Physical and multicast address recognition
- Packet framing and unframing
- Manchester encoding and decoding
- Preamble generation and removal
- Carrier sense and deference
- Collision detection and enforcement.
- Backoff and retry timing
- Frame check sequence (CRC) generation and verification
- Alignment and length error detection and handling

2.4.3. Ethernet Address Recognition

EXOS 201 recognizes physical, multicast, and broadcast addresses without user software intervention. A very efficient multicast address filter, implemented in hardware, greatly reduces the overhead of multicast address recognition. The multicast address filter can be disabled so that all multicast addresses are accepted. EXOS 201 also provides a promiscuous mode, in which it accepts all addresses.

Each EXOS 201 board has a unique 48-bit Ethernet address, stored in a PROM. This is the board's physical address by default, but the effective physical address resides in RAM and can be modified by user software.

2.4.4. Ethernet Operation Timing

EXOS 201 can receive successive frames with minimum interframe spacing (9.6 microseconds). It can also receive immediately after transmitting, or vice versa, with minimum interframe spacing and without losing data.

2.4.5. Ethernet Packet Buffering

In the front-end mode, under NX 200 firmware control, EXOS 201 can buffer an arbitrary number of both receive and transmit packets. The actual number of available buffers depends on the application criteria. User software can select both buffer size and location, which can be anywhere between 01000H and 1FFFFH in EXOS 201's dual-ported memory.

In the link-level mode, EXOS 201 can chain up to 32 receive packet buffers, and receive as many packets, without CPU intervention. Transmit packets are chained by NX 200 firmware and transmitted with minimal delay.

2.4.6. Ethernet Error Handling

EXOS 201 can be selectively enabled to receive packets normally rejected due to CRC and alignment errors.

2.4.7. Ethernet Transmit Status LED

EXOS 201 lights an LED at position DS2 while transmitting on the Ethernet.

2.4.8. Ethernet Transceiver Connector

EXOS 201 board's Ethernet connector is a 16-pin IDH type which mates with a 16 pin IDC type connector. The connectors are keyed, and pin number 1 can also be identified by an arrow on the connector. Note that it is still possible to insert the connector backwards.

2.4.9. Pin Definition of Ethernet Connector

The Ethernet connector (P3) on EXOS 201 is a 16-pin dual-row connector with latches. This connector accepts normal, flat-cable connectors that have a 16-pin on one end and a 15-pin D-Sub connector on the other. The flat-cable connector connects to EXOS 201 and the D-Sub connector connects to the standard Ethernet transceiver cable. Note that the numbering system is different for the two types of connectors.

The pin-out for the P3 connector, using "flat cable numbering scheme," is given below.

Table 2-2: Ethernet Connector (P3) Pin Definition

Pin #	Function	Polarity
2	Collision	(–)
3	Collision	(+)
4	Transmit	(–)
5	Transmit	(+)
7	Signal	Gnd
8	Receive	(–)
9	Receive	(+)
10	Power	+12V
11	Power	Gnd
1,6,12-16	Not used	

2.5. ON-BOARD PROCESSING CAPABILITIES

EXOS 201 is designed to facilitate the implementation of higher-level communications protocols on its own processor. The following are the major elements of this intelligent Ethernet controller:

- An 8-MHz 80186 CPU, clock speed 8 MHz
- 128 Kbytes of dual-ported RAM (Model 2), 256 Kbytes of dual-ported RAM (Model 3), or 512 Kbytes of dual-port RAM (Model 4). (On all models, all but 4 Kbytes of RAM is available for user software.)
- NX 200 operating system kernel, residing in two 16-Kbyte EPROMs.
- Sockets for two 32-Kbyte EPROMs for installing user-coded firmware.

The NX 200 operating system kernel provides a real-time, multitasking environment for the implementation of higher level protocols on EXOS 201. NX 200 implements consistent and portable access methods for the Ethernet and host interfaces. In addition, it executes self-diagnostics and can optionally drive the EXOS 201 board as an intelligent link-level controller, in which case the user is not required to download protocol software.

The two 32-Kbyte user EPROMs can be used to install user-coded firmware on the board. These EPROMs are mapped to addresses C0000H to CFFFFH. Users can include their own protocols, programs, or routines in these EPROMs. This feature can be very useful for users who write their own network software.

2.6. FIRMWARE CONFIGURATION OPTIONS

Jumper J6 selects NX 200 firmware options. If J6 is installed, EXOS 201 attempts to download software from the Ethernet after the self-test is complete. If the jumper is not installed, EXOS 201 awaits initialization from the host after the self-test is complete.

Jumper J11 when installed (default) disables the SQE check that is performed after each transmit. This provides an Ethernet Version 1.0 compatible transceiver connection. Note that if a Version 2.0 or an IEEE 802.3 transceiver is to be used, Jumper J11 should be removed.

It may be necessary to install jumper J5, that is, disable the Carrier Sense function, when a broad-band transceiver is used. This requirement is indicated by a 20H Return Code described in Section 6.3.4 of the *NX 200 Network Executive Reference Manual.*

2.7. iSBX CONNECTIONS

A 44-pin iSBX connector, which meets the IEEE P969 specifications, is provided for adding daughter boards (such as, a serial communications board). Two jumper-selectable interrupt lines (J13 and J14) are provided. These lines are active high. Therefore, if either one of these lines is used, then the other must be grounded. Unless a software driver is installed, both jumpers should be left open.

2.8. SELF-TEST OPERATION

The NX 200 firmware performs a series of tests which exercise the hardware and software components of the EXOS 201 Intelligent Ethernet Controller. In addition to ensuring the EXOS 201 is functioning properly, the tests can be used to isolate specific software or hardware problems associated with configuration or operation. The errors are reported via an LED making it possible for them to be identified and corrected.

When the EXOS 201 board is reset by the Multibus INIT/ line or by host software, NX 200 firmware runs comprehensive diagnostic tests on the EXOS 201 components. These tests complete within three seconds, after which the board is ready to be configured. If the tests fail, this is reported to the host via an I/O port. Refer to the "Initialization and Host Interface" chapter of the *NX 200 Network Executive Reference Manual.*

2.8.1. NX 200 Status LED

Test progress and status are also reported via an LED at position DS1. On EXOS 201 reset, this LED is lit, and it remains lit constantly while the self-tests are in progress. When the self-tests are complete, the LED flashes evenly until EXOS 201 is initialized by the host or from the Ethernet. After initialization, LED DS1 turns off.

If the diagnostics encounter a hardware problem, then the LED will be lit constantly or will communicate an error code by flashing long and short pulses.

Software errors that occur during the process of configuration can also result in the display of an error. Error codes are 8-bit numbers, and are presented bit-by-bit, starting with the most significant bit. A long pulse is a "1" bit, and a short pulse is a "0" bit. The error code is continuously repeated, with a pause in between to demarcate the starting point. Table 2-3 specifies all defined error codes for the EXOS 201.

2.8.2. Error Handling

As stated earlier, NX 200 handles all Ethernet error conditions, including user software configuration, and native hardware errors. Additionally, NX 200 also monitors for fatal hardware and software errors that may occur during general network operation.

2.9. ERROR CATEGORIES

The errors are logically categorized into three groups.

- A0H-AFH: Fatal software configuration errors
- B0H-BFH: Fatal hardware errors
- C0H-CFH: Fatal errors, either software or hardware, which occur during the course of normal operation

2.9.1. Fatal Software Errors

Although software configuration errors generally occur from entering inappropriate values for system configuration, on rare occasions, they can result from a bad bit in a memory chip being interpreted by NX 200 as an invalid value returned. The software generated error codes are also available and useful for debugging user software written to configure the Ethernet utilizing non-EXOS, user proprietary protocols.

An exception to this is error **AFH - Net Boot Failed** which results from utilizing the network bootstrap procedures for diskless workstations. This function, associated with an EXOS Intelligent Ethernet Controller jumper option, is not currently implemented in the NX 200 operating system kernel.

Table 2-3: Self-Diagnostic and Configuration Error Codes

Hex Code	Pulse Code	Explanation of Error Code
Software-generated Errors		
A0H	-.-.	Invalid address for configuration message.
A4H	-.-. .-..	Invalid operation mode parameter.
A5H	-.-. .-.-	Invalid host data format test pattern.
A7H	-.-. .---	Invalid configuration message format.
A8H	-.-. -...	Invalid movable data block parameter.
A9H	-.-. -..-	Invalid number of processes parameter.
AAH	-.-. -.-.	Invalid number of mailboxes parameter.
ABH	-.-. -.--	Invalid number of address slots parameter.
ACH	-.-. --..	Invalid number of hosts parameter.
ADH	-.-. --.-	Invalid host queue parameter.
AEH	-.-. ---.	Improper objects allocation.
AFH	-.-. ----	Net boot failed.
Hardware-generated Errors		
B0H	-.--	Checksum on NX 200 EPROM failed.
B1H	-.-- ...-	Memory test failed for 0-128K.
B2H	-.-- ..-.	Memory test failed for 128K up to the highest address.
B3H	-.-- ..--	Counter test failed.
B4H	-.-- .-..	Interrupts test failed.
B5H	-.-- .-.-	Transmission test failed.
B6H	-.-- .--.	Receive test failed.
B7H	-.-- .---	Local loopback data path test failed.
B8H	-.-- -...	CRC test failed.
B9H	-.-- -..-	Checksum on physical address EPROM failed.
BAH	-.-- -.-.	Bus timeout.
BBH	-.-- -.--	Ethernet chip initialization failed.
BCH	-.-- --..	Ethernet chip self-test failed.
BDH	-.-- --.-	Ethernet chip resource counter failed.
BEH	-.-- ---.	External loop-back test alignment error.
BFH	-.-- ----	iSBX board not in place.
Operation-generated Errors		
C0H	--..	Specified time exhausted.
C1H	--.. ...-	Host memory read/write test failed.
C8H	--.. -...	Parity hardware logic failed.
C9H	--.. -..-	NMI interrupt for bus timeout failed.
CAH	--.. -.-.	Host interrupt test failed.
CBH	--.. -.--	Command unit test failed.
CCH	--.. --..	Divide error exception.
CDH	--.. --.-	Undefined interrupt type.
CEH	--.. ---.	Command not executed by the CU of the 82586.
CFH	--.. ----	Command block sync failed between h/w and s/w.

2.9.2. Fatal Hardware Errors

Fatal hardware errors generally occur when NX 200 encounters specific EXOS hardware failure. However, the following three errors can be exceptions to this case, and may be due to incorrectly seated or installed cabling. In the event these errors occur, check and reconnect the cables, then reset the system. If this does not correct the condition and the error continues to occur, refer to Chapter 4 for service information.

BBH - Transmission test failed
BCH - Receive test failed
BDH - Local loopback data path test failed

The third and final category is directly associated with fatal errors that occur during normal operation, and are not usually encountered upon executing a reset and standard self-test. These errors can be produced by either software, hardware, or a combination of both. The software errors may be intermittent, while the hardware errors may be misconnections between the host and the network, or host and the EXOS 201 board.

The five errors listed below are generally associated with the physical interface between the host and the EXOS 201 board.

C1H - Host memory read/write test failed
C9H - NMI interrupt for bus timeout failed
CAH - Host interrupt test failed
CCH - Divide error exception
CDH - Undefined interrupt type

One error, **CBH - Command Unit Test Failed**, can occur between the host and the network if the transceiver malfunctions or is physically not connected to the network. If such is the case reconnect the host to the network and reboot. repetition of the error code will usually indicate a transceiver malfunction.

2.10. GENERAL SPECIFICATIONS

The following are general specifications for the EXOS 201 Intelligent Ethernet Controller:

Power Requirement:	+5VDC @ 4.5 Amp Max +12VDC @ 0.5 Amp Max (for transceiver and iSBX connector) –12VDC @ 0.05 Amp Max (for iSBX connector only)
Operating Environment:	Temperature: 5°C to 50°C Humidity: 0% to 90% non-condensing
I/O Register Addresses:	Jumper-selectable (from 0 to FFFF) Factory setting: Port A: 0000H; Port B: 0001H
Interrupt Vector Address:	Software programmable
Interrupt Priority Level:	Jumper selectable, one from 8 levels (INT0-INT7)
Multibus Timeout:	30 milliseconds (jumper selectable)
Physical Size:	6.75" by 12"; 6-layer single PCB

Chapter 3
INSTALLATION

3.1. INTRODUCTION

The EXOS 201 Intelligent Ethernet Controller is designed for use in Multibus-based computer systems, such as Intel System 286/310, NCR Tower, and systems from Altos, Arete, Masscomp, Silicon Graphics, and others. Prior to its installation, the EXOS 201 board must be jumper-configured to be compatible with the host system's configuration. Following the installation, the board must be connected to the Ethernet network using a transceiver cable and a transceiver.

Once the EXOS 201 board has been installed and the system connected to the network, appropriate network software, such as Excelan's 8000 Series network software, can be installed on the host system. The host system can then communicate with other hosts on the network.

3.2. CONFIGURING EXOS 201

The configuration of EXOS 201, as applicable to its installation in a host system, involves selecting I/O port addresses and a Multibus interrupt level by setting various jumpers.

3.2.1. Assigning System Addresses (I/O Ports) for EXOS 201

The EXOS 201 uses two consecutive one-byte words of I/O address space in the host system memory. The factory-set default for these is 00H and 01H. Therefore, addresses 00H and 01H should not be used by any other device in the system. However, if there should be any contention for this address space, different addresses can be jumper-selected for the EXOS 201.

EXOS 201 allows selection of either 8-bit or 16-bit addresses for these ports via jumpers J50 and J51. Refer to Section 2.3.3 for details.

Note that if EXOS 201 is assigned new I/O port addresses, they must be supplied to the EXOS I/O driver at the time the driver is built during the EXOS 8000 Series network software installation.

3.2.2. Selecting Bus Interrupt Level

As shipped from the factory, bus interrupt level 5 is selected for EXOS 201. This is the level used by EXOS 8000 Series network software. However, if there is contention for this interrupt level, any other interrupt level from INT0 to INT7 can be selected by appropriately reconfiguring the jumper J54. Refer to Section 2.3.4 for details.

Note that if a new interrupt level is selected, it must be supplied to the EXOS I/O driver at the time the driver is built during the EXOS 8000 Series network software installation.

3.3. INSTALLING EXOS 201

The procedure for physical installation of the board depends on the design of the mechanical enclosure and card cage accessibility of the host system. You should consult the hardware reference manual for the host computer system and follow the specified procedure to install a board.

In general, a typical installation procedure includes the following steps. Steps for connecting the system to the network are also included.

1. Make sure that the system I/O port addresses selected for EXOS 201 (check jumpers J50 an J51) are not used by any other device. If necessary, select different I/O port addresses.
2. Make sure that there is no contention for the bus interrupt level selected for EXOS 201 (check jumper J54). If necessary, select a different interrupt level.
3. Shut down the system by following the procedure specified for your system.
4. Switch off the power.
5. Remove the card cage cover(s).
6. Insert and slide the EXOS 201 board into an empty slot until properly seated.
7. Plug the male end of the EXOS 1212 Board Cable or equivalent into the 16-pin IDH connector on EXOS 201. (The board cable is not supplied with the EXOS 201 board; it must be ordered separately.) Make sure that the latches on the board have seated properly; this prevents the cable from being pulled out accidentally.
8. Route the board cable to the back of the computer cabinet.
9. Knock out the prepunched plate in the computer I/O panel to receive the 15-pin subminiature D-type connector on the other end of the EXOS board cable.
10. Bolt the D-type connector in place ensuring that the slide latch operates correctly.
11. Ensure that enough +12 volt power is available for the transceiver. (Normally, the transceiver gets power for itself through the EXOS 201 board. However, you should consult the applicable transceiver documentation for specifics. Insufficient power for the transceiver can cause your computer to crash.)
12. Connect the system to the network by plugging one end of the transceiver cable into the D-type connector and the other into the transceiver, which must have already been installed on the Ethernet media.
13. Turn on the power.

Following Step 13, you can install the network software, such as the EXOS 8000 Series, as described in the applicable network software manual.

Chapter 4
SERVICE INFORMATION

4.1. INTRODUCTION

Prior to shipping, each EXOS 201 Ethernet Intelligent Ethernet Controller board is thoroughly tested and exercised both at the component and system level. However, since it is not possible to simulate every possible situation that might exist on the network, occasionally you might encounter operational problems with the EXOS 201 board. For such rare cases, Excelan provides prompt technical service assistance. After hearing from you, our technical support personnel will discuss the problem with you over the telephone. Quite often, the problem is a simple one and can be resolved during such discussions. At other times, it may be necessary for you to ship the board back to factory for repair or replacement.

This chapter provides information on how to obtain service assistance. Note that when communicating with Excelan Service Center, you might need to provide or refer to information included in Appendixes A and B of this manual.

Appendix A presents an assembly diagram of the EXOS 201 board that shows the locations of the EXOS 201 serial number, assembly or part number, board revision level, various components, and jumpers. The appendix also contains a jumper table that shows functions of various jumpers.

Appendix B provides a set of EXOS 201 schematic diagrams.

4.2. HOW TO USE SERVICE ASSISTANCE

The following is a summary of procedure for using Excelan's service assistance. For detailed information, please refer to the "Warranty/Service Information" document shipped with your EXOS 201.

If you encounter any problem with your EXOS 201 and you or your system administrator cannot resolve it, please contact

Customer Service Center
Excelan, Inc.
2180 Fortune Drive
San Jose, CA 95131
(408) 434-2285

For prompt assistance the Service Center will require the following information. Please have it ready.

- Your company name
- Technical contact
- Company address
- Telephone number
- Product name, part number, and serial number
- Your purchase order number or service contract number

The Customer Service staff will then discuss the problem you are experiencing with EXOS 201. They will assist you in isolating the fault and fixing it, if possible.

If the problem cannot be resolved, the service staff will provide you with a Return Material Authorization (RMA) number. You should then securely pack the unit in its original or similar packing and return it to to Excelan at the address given above. Please refer to the "Warranty/Service Information" document for detailed service terms.

At this point, depending on whether or not the unit is under warranty or extended warranty, the service staff will be able to advise you of any applicable charges for the service.

Appendix A
COMPONENT LOCATION

A.1. INTRODUCTION

Figure A-1 show the location of main components and various jumpers on the EXOS 201 board. Table A-1 lists the function of various jumpers.

Table A-1: EXOS 201 Jumpers

Jumper	Function (when jumper is installed)	Factory Setting
J2	Reserved	Installed
J3	Reserved	Absent
J4	512 Kbyte Memory (Model 4)	Absent
J5	Disable Carrier Sense	Absent
J6	Boot from network	Absent
J7	256 Kbyte Memory (Model 3)	Absent
J9	Reserved	Absent
J10	Reserved	Installed
J11	Disable SQE (Heartbeat) check, Ethernet Version 1.0 mode	Installed
J12	Reserved	Absent
J13	Ground IRO from SBX	Absent
J14	Ground IRO from SBX	Absent
J15	Enable Watchdog Timer	Absent
J50	Enable 16-bit address decode	Installed
J51	Enable 8-bit address decode	Absent
J52	(7 jumpers) Bits 1-7 of I/O port address	All absent (0)
J53	(8 jumpers) Bits 8-15 of I/O port address	All absent (0)
J54	(8 jumpers) Interrupt levels 0-7	Level 5
J55	27128 user EPROMs	Absent
J56	27256 user EPROMs	Absent
J57	Enable /BPRO output	Installed
J58	Enable response to /CBRQ	Absent
J59	Respond as if /CBRQ always active	Installed
J60	Drive /CCLK and /BCLK lines	Absent
J61	Reserved	Installed

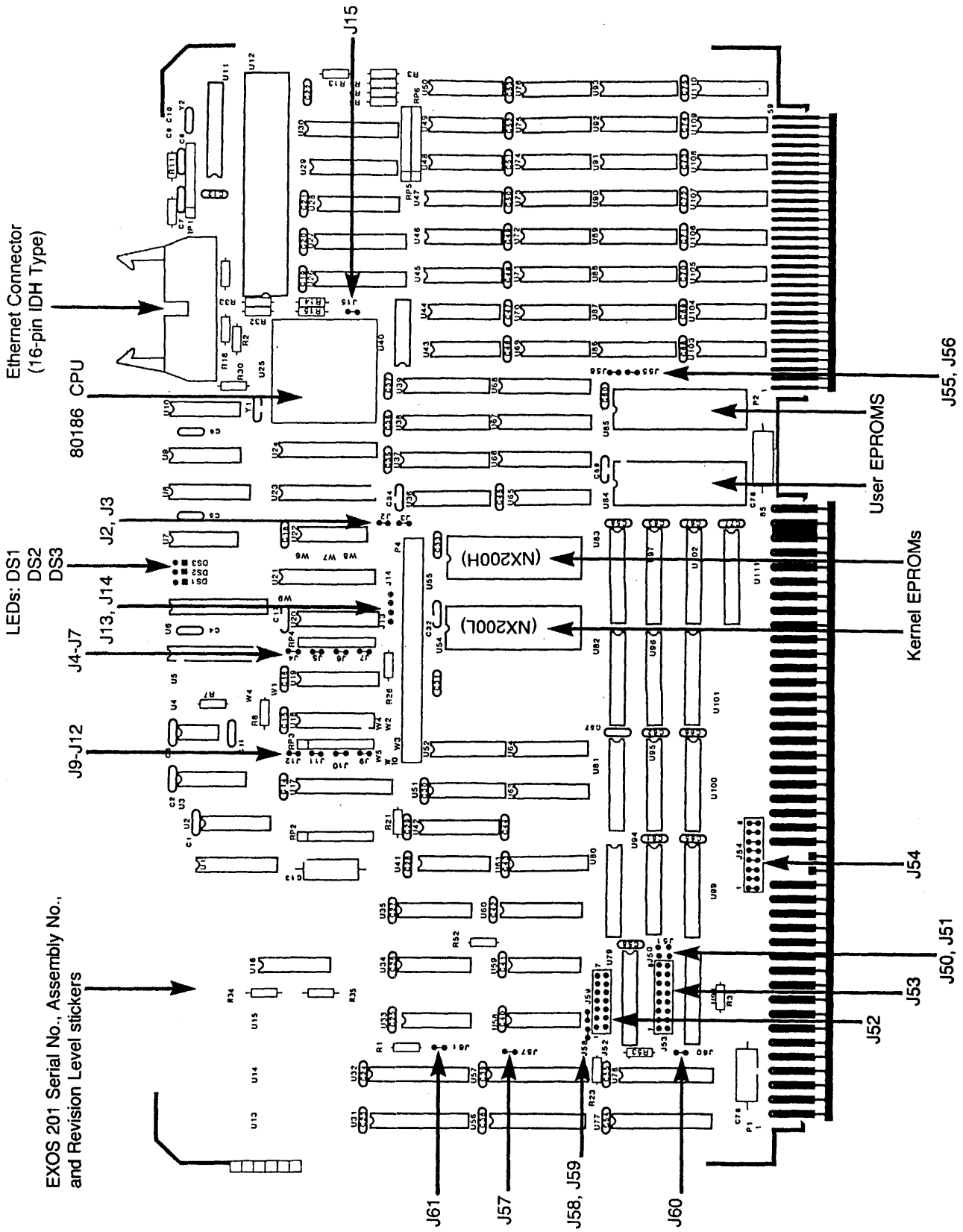
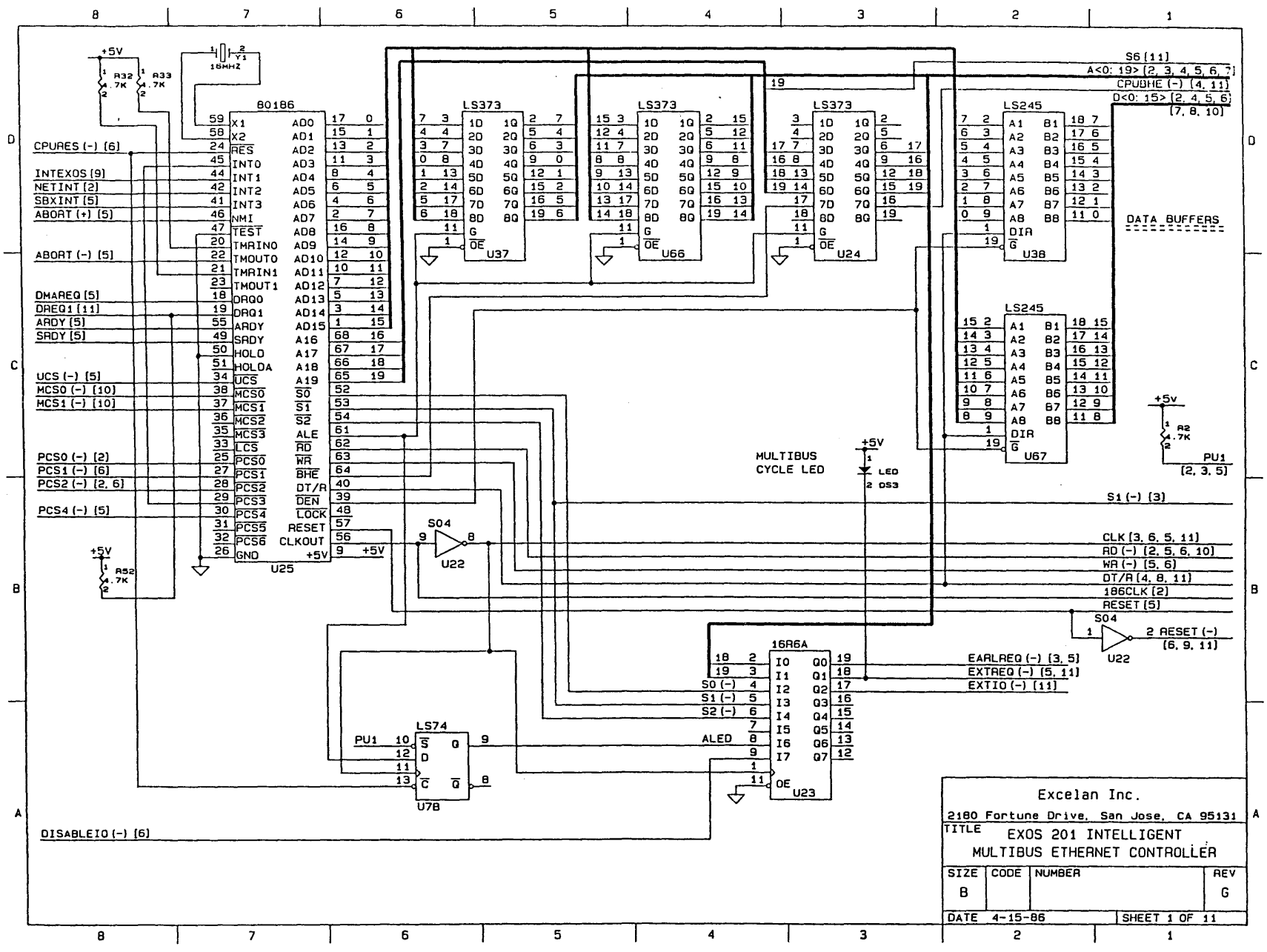


Figure A-1: EXOS 201 Component Layout

Appendix B
EXOS 201 SCHEMATICS

B.1. INTRODUCTION

The schematics for the EXOS 201 Intelligent Ethernet Controller are shown on the following pages.


80186
LS373
LS245
16R6A
LS74
S04
+5V
R32 4.7K
R33 4.7K
R52 4.7K
R2 4.7K
15MHZ
Y1
U25
U37
U66
U24
U38
U67
U22
U23
U78
PU1
LED
DS3
DATA BUFFERS
MULTIBUS CYCLE LED
CPUBHE (-) [4, 11]
A<0: 19> [2, 3, 4, 5, 6, 7]
D<0: 15> [2, 4, 5, 6] [7, 8, 10]
S6 [11]
CPUAES (-) [6]
INTEXOS [9]
NETINT [2]
SBXINT [5]
ABORT (+) [5]
ABORT (-) [5]
DMAREQ [5]
DREQ1 [11]
ARDY [5]
SRDY [5]
UCS (-) [5]
MCS0 (-) [10]
MCS1 (-) [10]
PCS0 (-) [2]
PCS1 (-) [6]
PCS2 (-) [2, 6]
PCS4 (-) [5]
S1 (-) [3]
CLK [3, 6, 5, 11]
RD (-) [2, 5, 6, 10]
WR (-) [5, 6]
DT/R [4, 8, 11]
186CLK [2]
RESET [5]
2 RESET (-) [6, 9, 11]
EARLREQ (-) [3, 5]
EXTREQ (-) [5, 11]
EXTIO (-) [11]
DISABLEIO (-) [6]
Excelan Inc.
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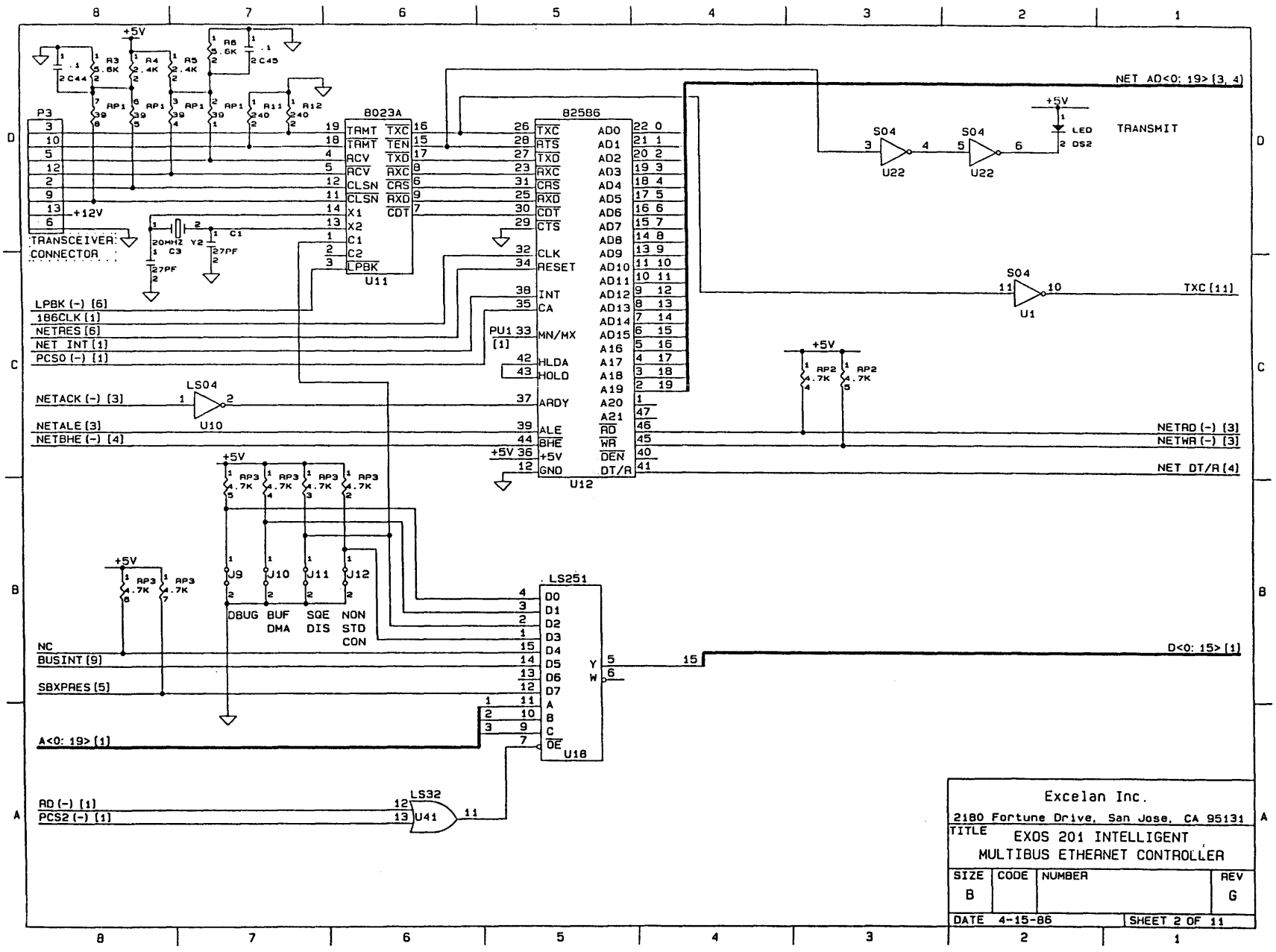
TITLE
EXOS 201 INTELLIGENT MULTIBUS ETHERNET CONTROLLER
SIZE B
CODE
NUMBER
REV G
DATE 4-15-86
SHEET 1 OF 11


8 7 6 5 4 3 2 1
+5V
+12V
P3
TRANSCEIVER CONNECTOR
8023A
82586
U11
U12
20MHZ Y2
C1 C2 C3
27PF
LPBK (-) [6]
186CLK [1]
NETRES [6]
NET INT [1]
PCS0 (-) [1]
NETACK (-) [3]
NETALE [3]
NETBHE (-) [4]
LS04
U10
PU1 [1]
NET AD<0: 19> [3, 4]
S04
U22
LED DS2
TRANSMIT
U1
TXC [11]
NETRD (-) [3]
NETWR (-) [3]
NET DT/R [4]
RP2 4.7K
RP3 4.7K
LS251
U18
DBUG
BUF DMA
SQE DIS
NON STD CON
NC
BUSINT [9]
SBXPRES [5]
A<0: 19> [1]
D<0: 15> [1]
LS32
U41
AD (-) [1]
PCS2 (-) [1]
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EXOS 201 INTELLIGENT
MULTIBUS ETHERNET CONTROLLER
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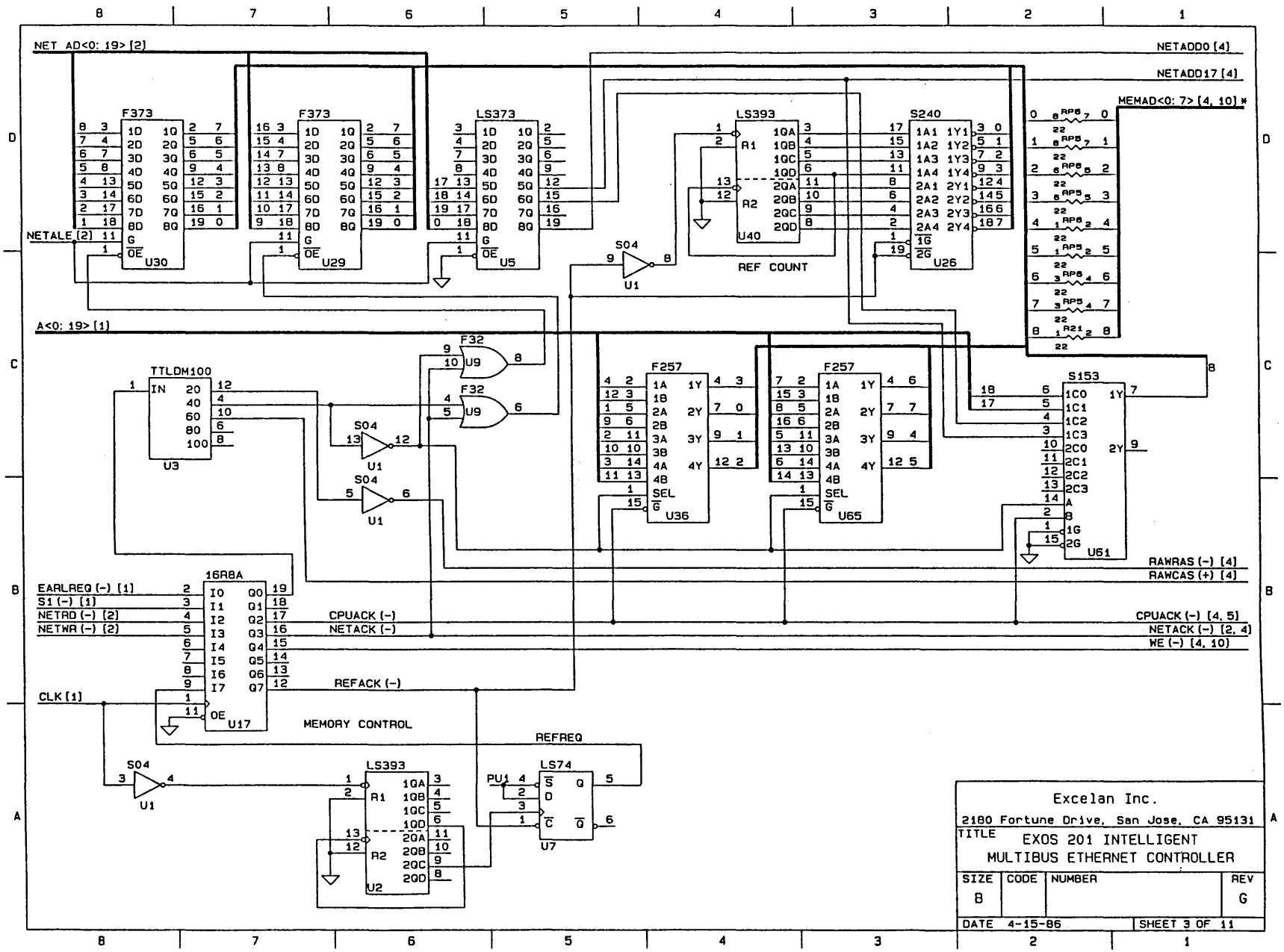
NET AD<0: 19> [2]
NETADD0 [4]
NETADD17 [4]
MEMAD<0: 7> [4, 10] *
NETALE [2]
A<0: 19> [1]
F373
U30
U29
LS373
U5
LS393
U40
REF COUNT
S240
U26
S04
U1
F32
U9
TTLDM100
U3
F257
U36
U65
S153
U61
16R8A
U17
MEMORY CONTROL
EARLREQ (-) [1]
S1 (-) [1]
NETRD (-) [2]
NETWR (-) [2]
CLK [1]
CPUACK (-)
NETACK (-)
REFACK (-)
RAWRAS (-) [4]
RAWCAS (+) [4]
CPUACK (-) [4, 5]
NETACK (-) [2, 4]
WE (-) [4, 10]
REFREQ
LS74
U7
U2
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EXOS 201 INTELLIGENT
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SIZE
B
CODE
NUMBER
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G
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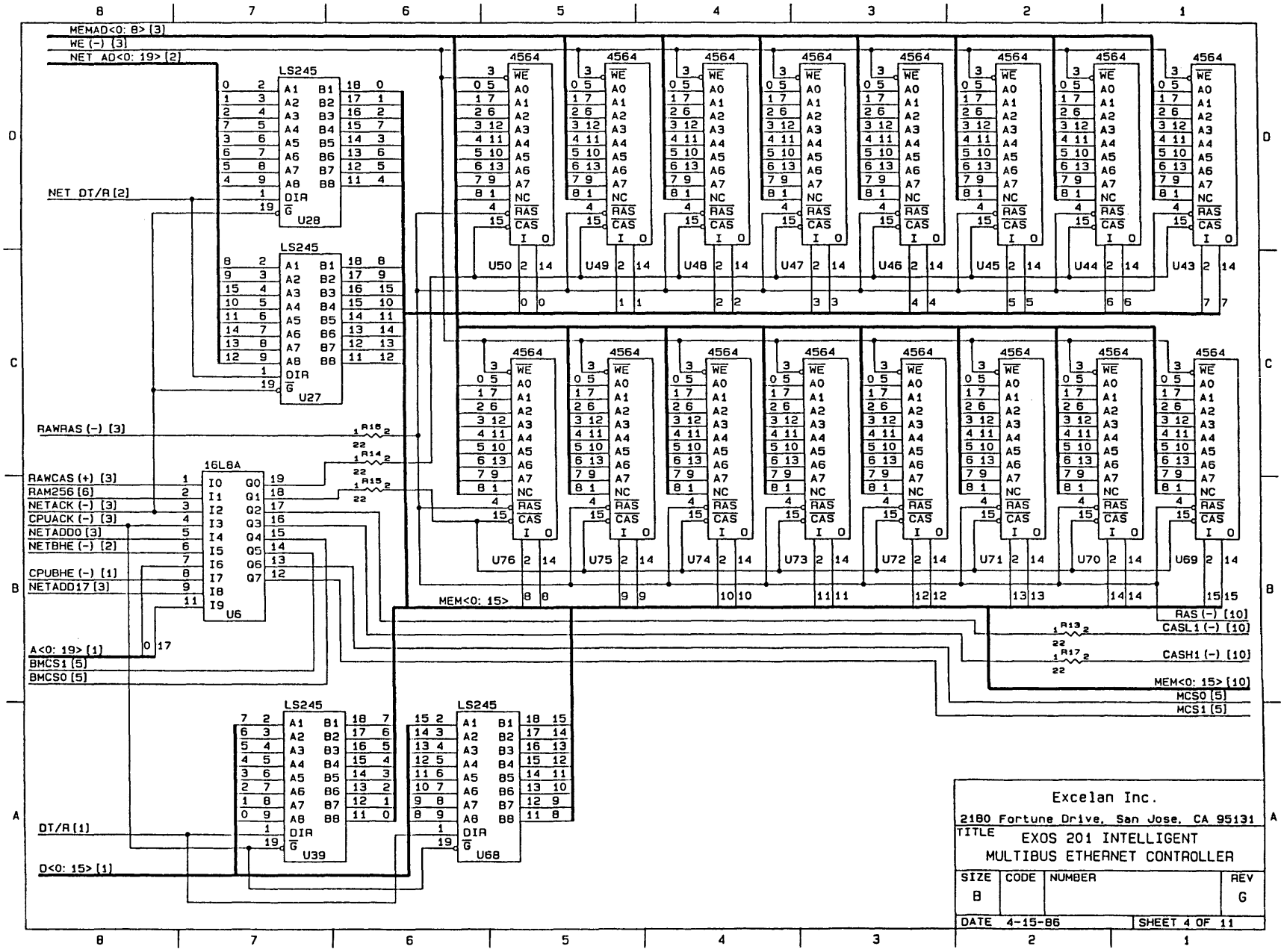
SHEET 3 OF 11


MEMAD<0: 8> [3]
WE (-) [3]
NET AD<0: 19> [2]
NET DT/R [2]
RAWRAS (-) [3]
RAWCAS (+) [3]
RAM256 [6]
NETACK (-) [3]
CPUACK (-) [3]
NETADD0 [3]
NETBHE (-) [2]
CPUBHE (-) [1]
NETADD17 [3]
A<0: 19> [1]
BMCS1 [5]
BMCS0 [5]
DT/R [1]
D<0: 15> [1]
MEM<0: 15>
RAS (-) [10]
CASL1 (-) [10]
CASH1 (-) [10]
MEM<0: 15> [10]
MCS0 [5]
MCS1 [5]
LS245
U28
U27
U39
U68
16L8A
U6
4564
U50
U49
U48
U47
U46
U45
U44
U43
U76
U75
U74
U73
U72
U71
U70
U69
R16
R14
R15
R13
R17
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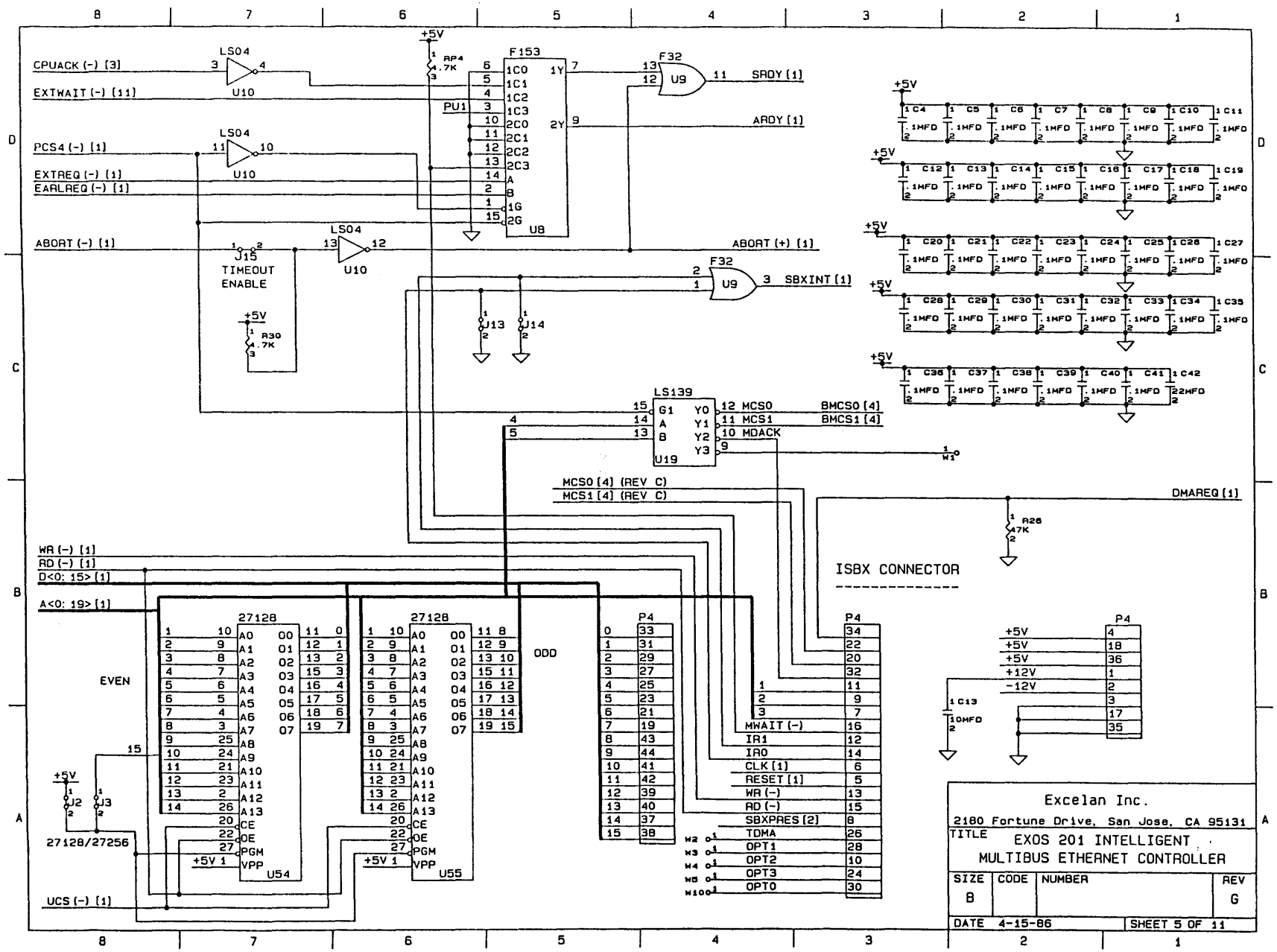
EXOS 201 INTELLIGENT
MULTIBUS ETHERNET CONTROLLER
SIZE
B
CODE
NUMBER
REV
G
DATE 4-15-86
SHEET 4 OF 11


CPUACK (-) [3]
EXTWAIT (-) [11]
PCS4 (-) [1]
EXTREQ (-) [1]
EARLREQ (-) [1]
ABORT (-) [1]
ABORT (+) [1]
SRDY [1]
ARDY [1]
SBXINT [1]
J15
TIMEOUT
ENABLE
LS04
U10
F153
U8
F32
U9
LS139
U19
BMCS0 [4]
BMCS1 [4]
MDACK
MCS0 [4] (REV C)
MCS1 [4] (REV C)
DMAREQ [1]
R26
47K
ISBX CONNECTOR
WR (-) [1]
RD (-) [1]
D<0: 15> [1]
A<0: 19> [1]
EVEN
ODD
27128
U54
U55
27128/27256
UCS (-) [1]
MWAIT (-)
IR1
IR0
CLK [1]
RESET [1]
WR (-)
RD (-)
SBXPRES [2]
TDMA
OPT1
OPT2
OPT3
OPT0
P4
+5V
+12V
-12V
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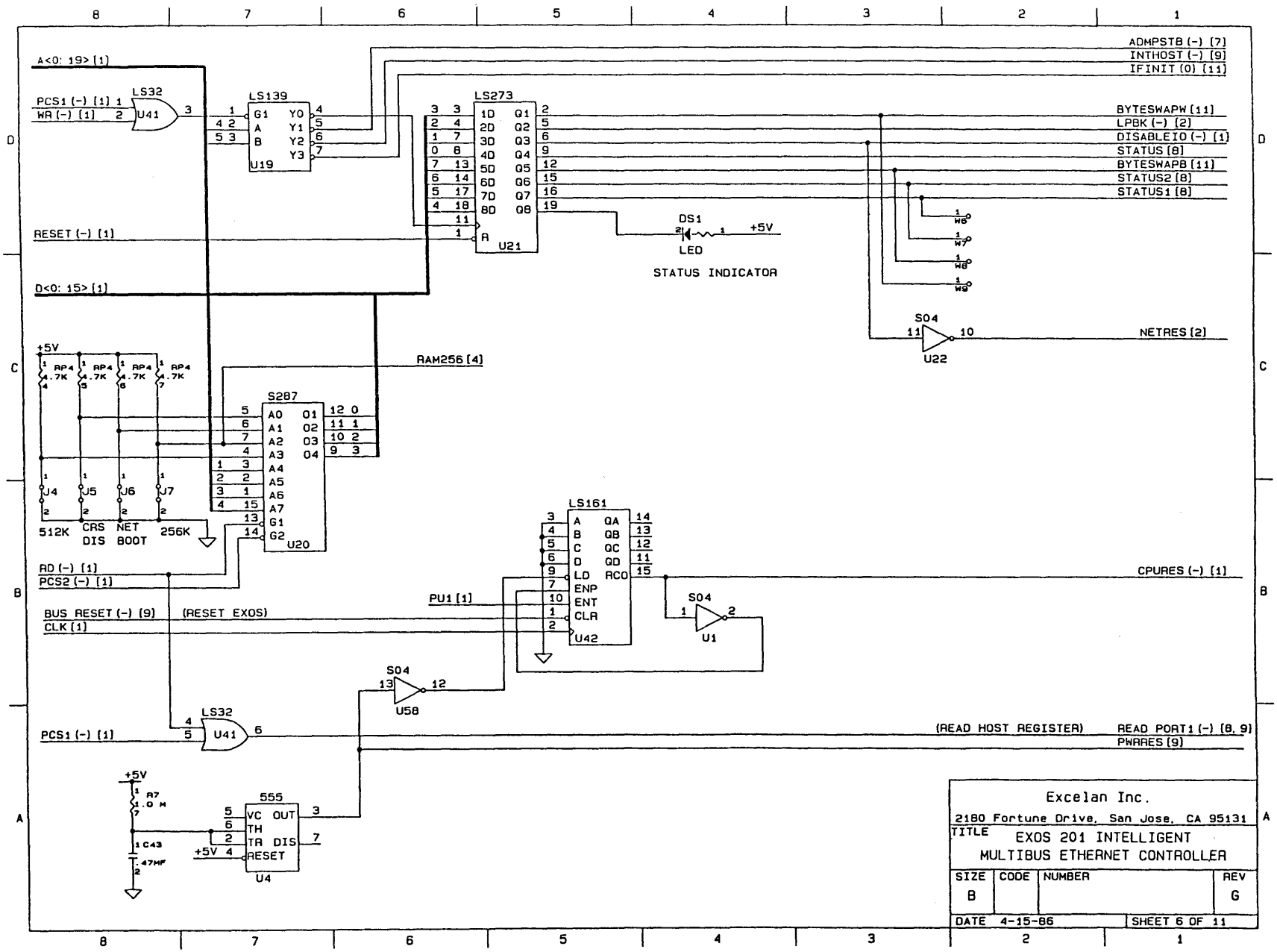
TITLE
EXOS 201 INTELLIGENT
MULTIBUS ETHERNET CONTROLLER
SIZE
B
CODE
NUMBER
REV
G
DATE 4-15-86
SHEET 5 OF 11


A<0: 19> [1]
PCS1 (-) [1]
WR (-) [1]
LS32
U41
LS139
U19
LS273
U21
ADMPSTB (-) [7]
INTHOST (-) [9]
IFINIT (0) [11]
BYTESWAPW [11]
LPBK (-) [2]
DISABLEIO (-) [1]
STATUS [8]
BYTESWAPB [11]
STATUS2 [8]
STATUS1 [8]
RESET (-) [1]
DS1
LED
+5V
STATUS INDICATOR
D<0: 15> [1]
S04
U22
NETRES [2]
RAM256 [4]
S287
U20
RP4 4.7K
U4
U5
U6
U7
512K
CRS DIS
NET BOOT
256K
AD (-) [1]
PCS2 (-) [1]
LS161
U42
PU1 [1]
BUS RESET (-) [9]
(RESET EXOS)
CLK [1]
U1
U58
CPURES (-) [1]
(READ HOST REGISTER)
READ PORT1 (-) [8, 9]
PWRRES [9]
555
U4
R7 1.0 M
C43 .47MF
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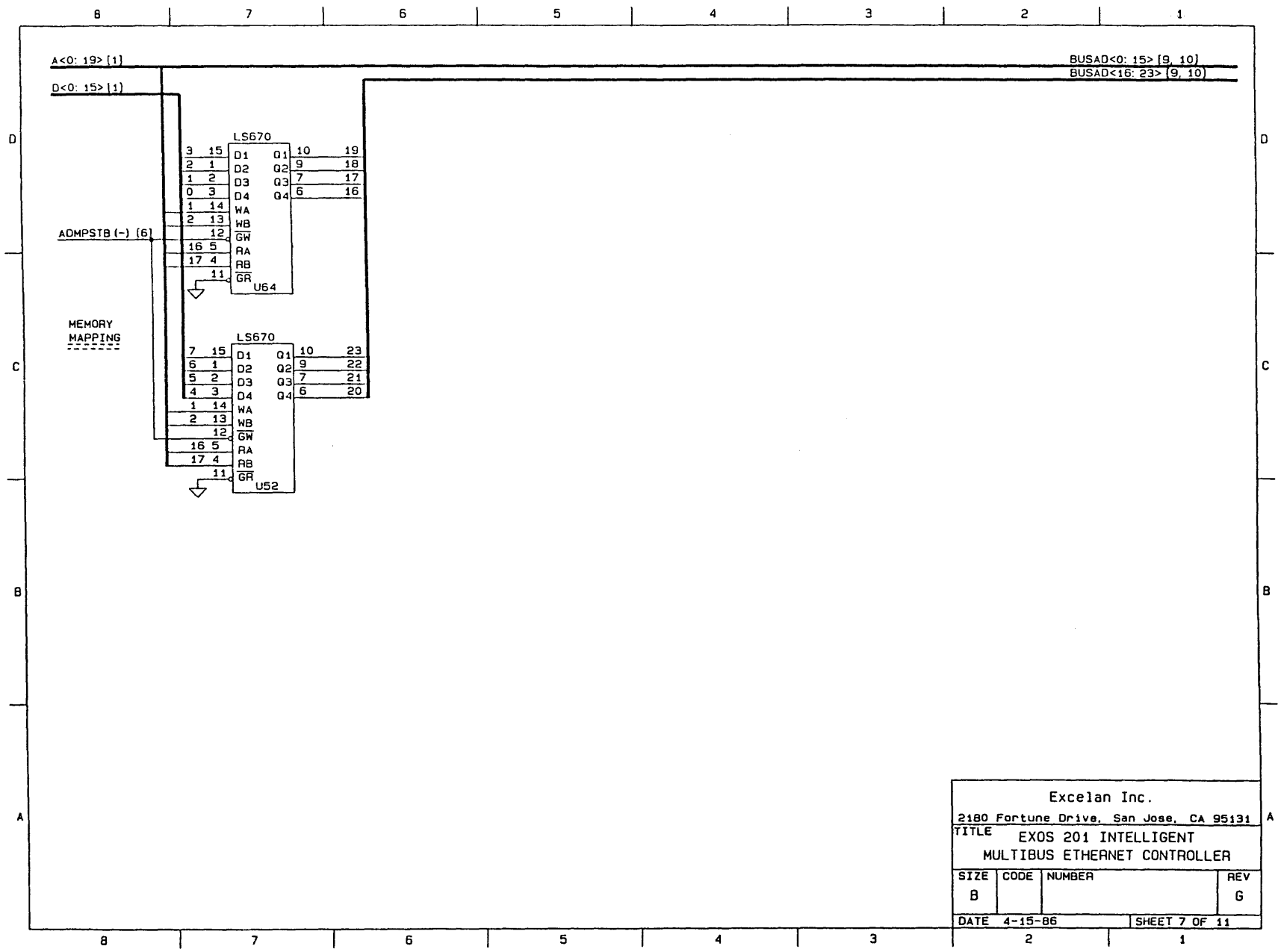
EXOS 201 INTELLIGENT
MULTIBUS ETHERNET CONTROLLER
SIZE B
CODE
NUMBER
REV G
DATE 4-15-86
SHEET 6 OF 11


A<0: 19> [1]
D<0: 15> [1]
BUSAD<0: 15> [9, 10]
BUSAD<16: 23> [9, 10]
ADMPSTB (-) [6]
MEMORY MAPPING
LS670
U64
LS670
U52
D1
D2
D3
D4
Q1
Q2
Q3
Q4
WA
WB
GW
RA
RB
GR
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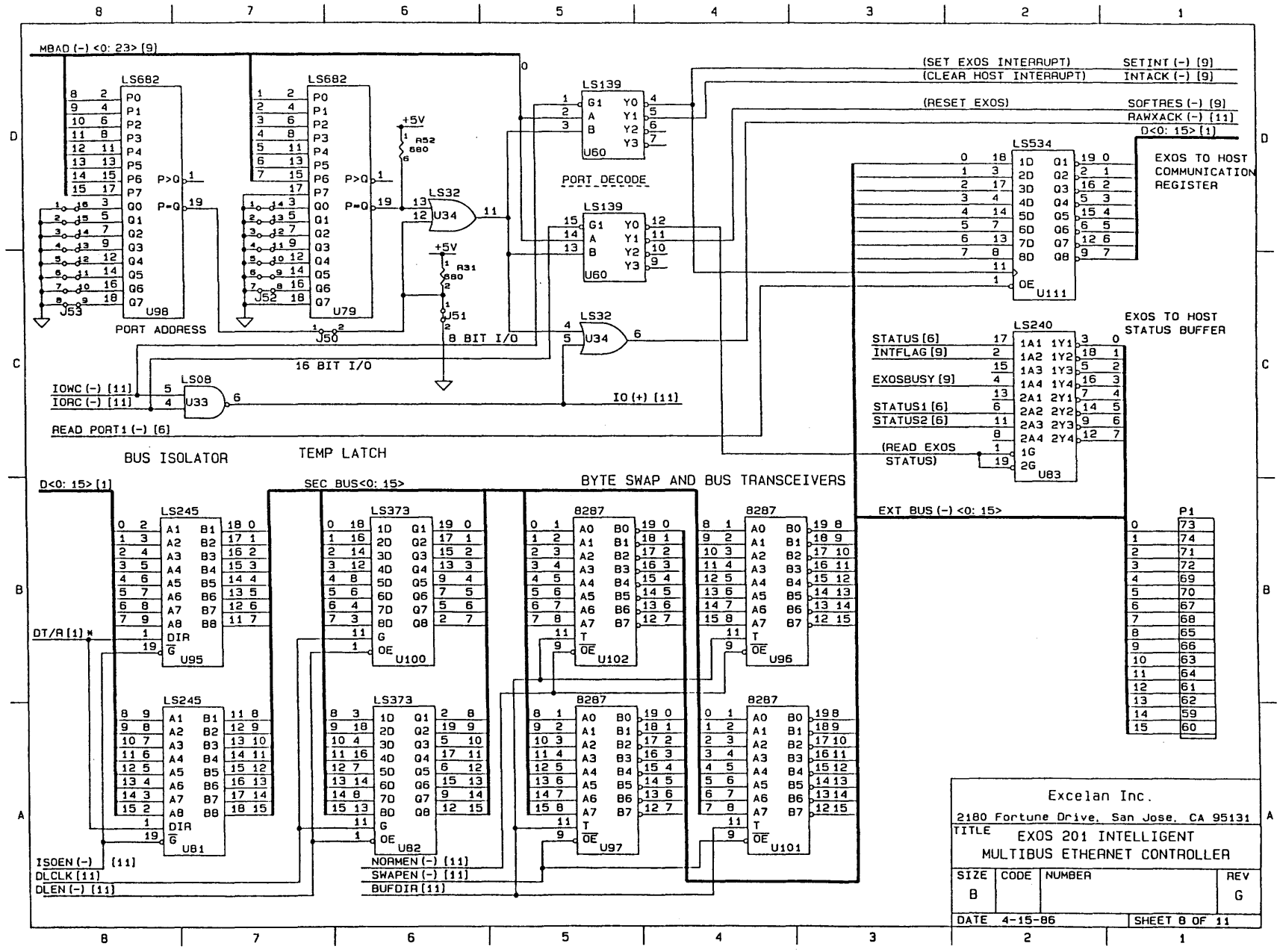
MBAD (-) <0: 23> [9]
LS682
U98
U79
PORT ADDRESS
J53
J52
J50
J51
8 BIT I/O
16 BIT I/O
+5V
R52 680
R31 680
LS32
U34
LS139
U60
PORT DECODE
(SET EXOS INTERRUPT)
(CLEAR HOST INTERRUPT)
SETINT (-) [9]
INTACK (-) [9]
(RESET EXOS)
SOFTRES (-) [9]
RAWXACK (-) [11]
D<0: 15> [1]
LS534
U111
EXOS TO HOST COMMUNICATION REGISTER
LS240
U83
EXOS TO HOST STATUS BUFFER
STATUS [6]
INTFLAG [9]
EXOSBUSY [9]
STATUS1 [6]
STATUS2 [6]
(READ EXOS STATUS)
EXT BUS (-) <0: 15>
P1
IOWC (-) [11]
IORC (-) [11]
LS08
U33
IO (+) [11]
READ PORT1 (-) [6]
BUS ISOLATOR
TEMP LATCH
BYTE SWAP AND BUS TRANSCEIVERS
D<0: 15> [1]
SEC BUS<0: 15>
LS245
U95
U81
LS373
U100
U82
8287
U102
U97
U96
U101
DT/R [1]
ISOEN (-) [11]
DLCLK [11]
DLEN (-) [11]
NORMEN (-) [11]
SWAPEN (-) [11]
BUFDIR [11]
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EXOS 201 INTELLIGENT MULTIBUS ETHERNET CONTROLLER
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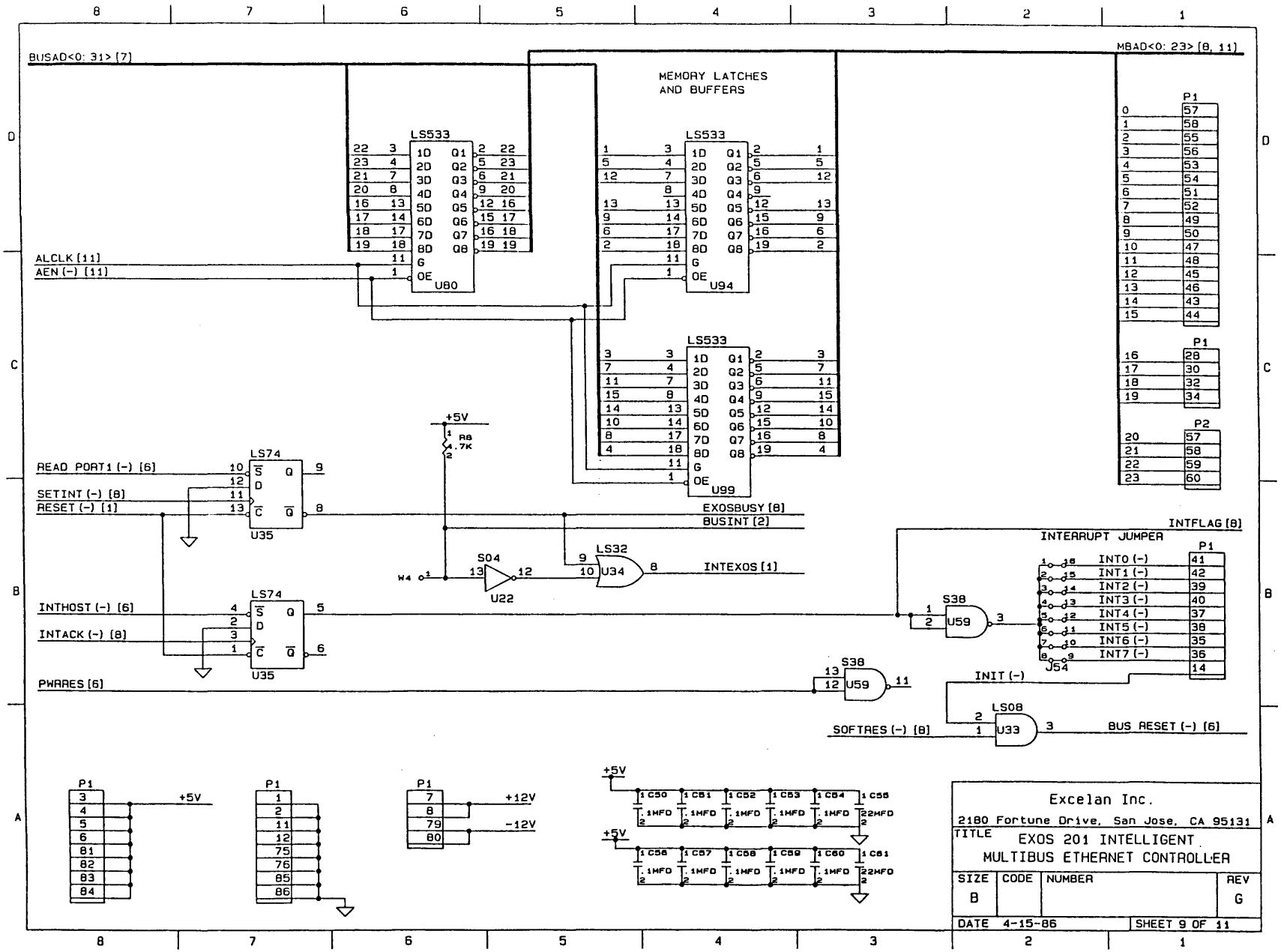
BUSAD<0: 31> [7]
MBAD<0: 23> [8, 11]
MEMORY LATCHES
AND BUFFERS
LS533
U80
U94
U99
ALCLK [11]
AEN (-) [11]
P1
P2
LS74
U35
READ PORT1 (-) [6]
SETINT (-) [8]
RESET (-) [1]
+5V
R8
4.7K
EXOSBUSY [8]
BUSINT [2]
INTFLAG [8]
INTERRUPT JUMPER
LS32
U34
S04
U22
INTEXOS [1]
INTHOST (-) [6]
INTACK (-) [8]
S38
U59
J54
INT0 (-)
INT1 (-)
INT2 (-)
INT3 (-)
INT4 (-)
INT5 (-)
INT6 (-)
INT7 (-)
PWRRES [6]
INIT (-)
LS08
U33
SOFTRES (-) [8]
BUS RESET (-) [6]
+12V
-12V
.1MFD
22MFD
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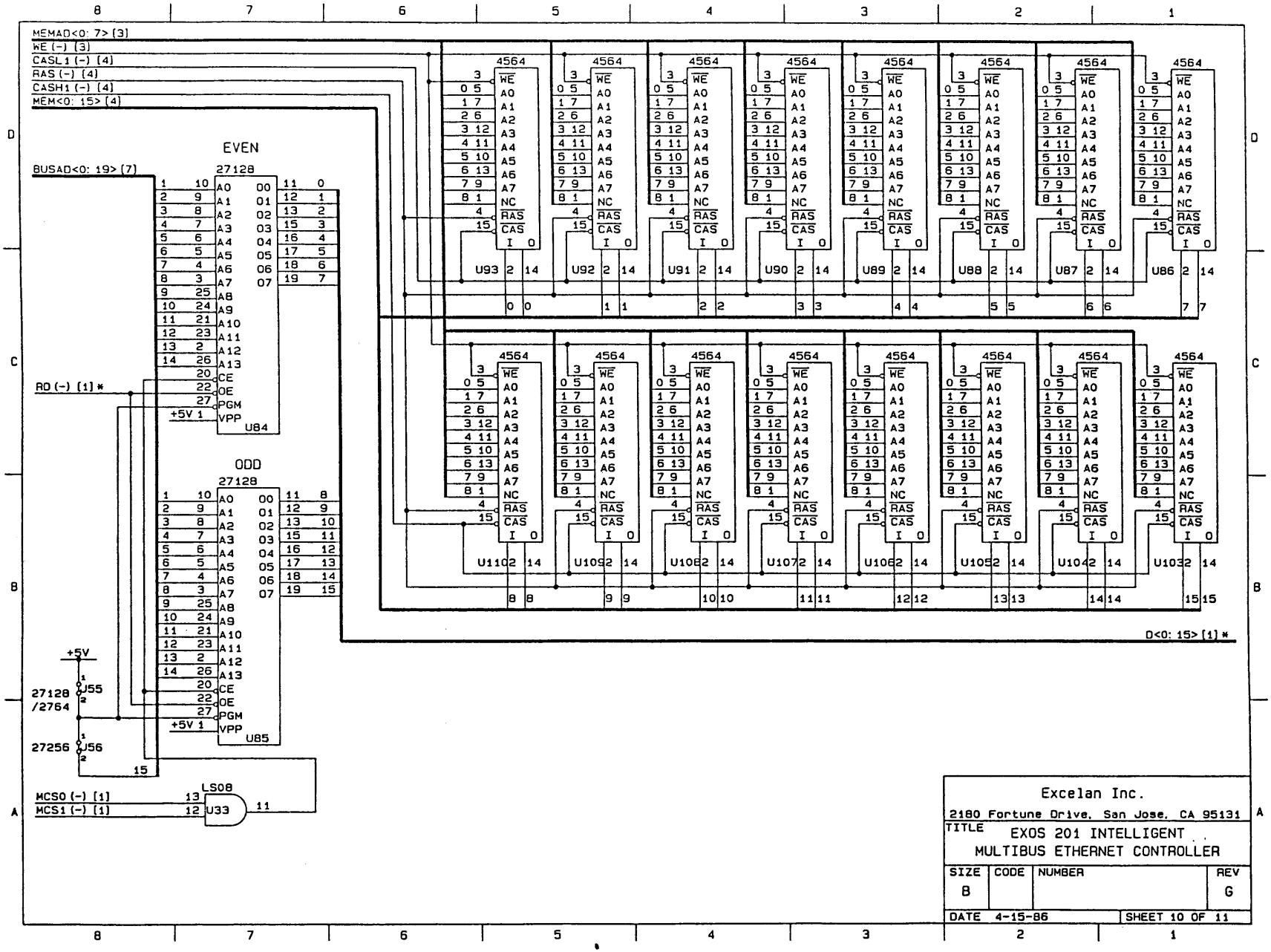
MEMAD<0: 7> [3]
WE (-) [3]
CASL1 (-) [4]
RAS (-) [4]
CASH1 (-) [4]
MEM<0: 15> [4]
EVEN
BUSAD<0: 19> [7]
27128
U84
RD (-) [1] *
+5V 1
ODD
27128
U85
+5V
27128 /2764
U55
27256
U56
MCS0 (-) [1]
MCS1 (-) [1]
LS08
U33
4564
U93
U92
U91
U90
U89
U88
U87
U86
U1102
U1092
U1082
U1072
U1062
U1052
U1042
U1032
D<0: 15> [1] *
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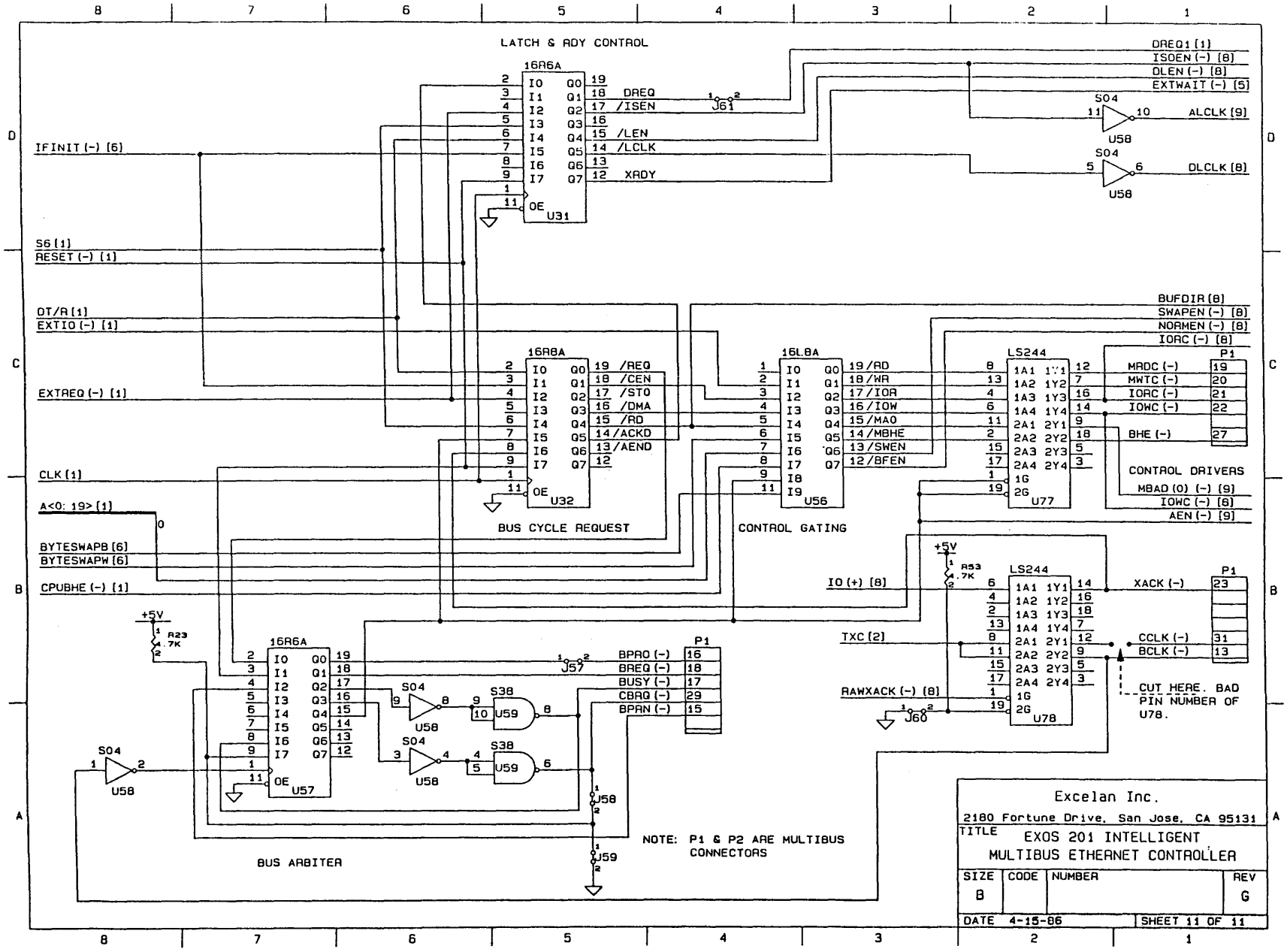
LATCH & RDY CONTROL
16R6A
U31
IFINIT(-) [6]
S6 [1]
RESET(-) [1]
DT/R [1]
EXTIO(-) [1]
EXTREQ(-) [1]
CLK [1]
A<0:19> [1]
BYTESWAPB [6]
BYTESWAPW [6]
CPUBHE(-) [1]
DREQ
/ISEN
/LEN
/LCLK
XRDY
DREQ1 [1]
ISOEN(-) [8]
DLEN(-) [8]
EXTWAIT(-) [5]
ALCLK [9]
DLCLK [8]
S04
U58
J61
16R8A
U32
/REQ
/CEN
/STO
/DMA
/RD
/ACKD
/AEND
BUS CYCLE REQUEST
16L8A
U56
/RD
/WR
/IOR
/IOW
/MAO
/MBHE
/SWEN
/BFEN
CONTROL GATING
LS244
U77
U78
BUFDIR [8]
SWAPEN(-) [8]
NORMEN(-) [8]
IORC(-) [8]
P1
MRDC(-)
MWTC(-)
IORC(-)
IOWC(-)
BHE(-)
CONTROL DRIVERS
MBAD(0) (-) [9]
IOWC(-) [8]
AEN(-) [9]
+5V
R53
4.7K
IO(+) [8]
XACK(-)
TXC [2]
CCLK(-)
BCLK(-)
RAWXACK(-) [8]
J60
CUT HERE. BAD PIN NUMBER OF U78.
R23
4.7K
16R6A
U57
J57
BPRQ(-)
BREQ(-)
BUSY(-)
CBRQ(-)
BPAN(-)
S38
U59
J58
J59
BUS ARBITER
NOTE: P1 & P2 ARE MULTIBUS CONNECTORS
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EXOS 201 INTELLIGENT MULTIBUS ETHERNET CONTROLLER
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Appendix C
TRANSCEIVER CABLE CONNECTOR PIN-OUT

C.1. INTRODUCTION

The EXOS 201 board is compatible with IEEE 802.3 and Ethernet (Version 1.0 and 2.0) transceivers. Therefore, all standard transceiver cables available commercially are suitable for use with the EXOS 201 board.

For reference, the pin assignment for the cable connector on the EXOS 201 board is shown in Table C-1; the pin numbers are illustrated in Figure C-1.

Table C-1: EXOS 201 Pin Assignment for the Transceiver Cable Connector

Pin #	Function	Polarity
2	Collision	(–)
3	Collision	(+)
4	Transmit	(–)
5	Transmit	(+)
7	Signal	Gnd
8	Receive	(–)
9	Receive	(+)
10	Power	+12V
11	Power	Gnd
1,6,12-16	Not used	

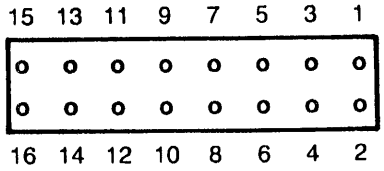

Figure C-1: Pin Layout for Transceiver Connector on EXOS 201

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TELEX 176610

January 29, 1986

RELEASE NOTES
EXOS 201 Ethernet Front-End Processor
ECN #1283 or Higher

You should read this entire release note before installing and using the EXOS 201 board. Refer to the *EXOS 201 Ethernet Front-End Processor Reference Manual* for details on installing and using the EXOS 201.

If you should have any questions, comments, or suggestions, please contact

Product Engineering
Excelan, Inc.
2180 Fortune Drive
San Jose, CA 95131
(408) 434-2285

COMPONENTS

ECN 1283 or higher versions of the EXOS 201 front-end processor consists of the following components:

- This release note (Part No. 4230107-00 Rev. B)
- One EXOS 201 board
- The *EXOS 201 Ethernet Front-End Processor Reference Manual* (Publication No. 4200006-00, Rev. A).

COMPATIBILITY

The EXOS 201 provides full IEEE 802.3 compliance when jumper J11 is removed. In this condition the output to the transceiver is AC-coupled and the SQE test is performed at the end of every transmission.

When jumper J11 is inserted (the factory setting), the EXOS 201 will have a DC-coupled output and the SQE test will not be performed. The board then meets the Ethernet Version 1.0 standard. In this condition the board functions correctly with all transceivers that Excelan has tested.

The EXOS 201 has been tested and is compatible with the following transceivers:

- EXOS 1110
- EXOS 1111
- 3Com 3C100
- TCL 2010E
- TCL 2010EB
- TCL 2010IS
- DEC H4000
- Interlan NT10
- Interlan NT100

The EXOS 201 is compatible with the following transceivers/fan-out units (transceivers/MUXs):

- EXOS 1130
- DEC DELNI
- TCL 2110

June 2, 1986

RELEASE NOTES
NX 200
Release 5.3

These release notes apply to NX 200, Release 5.3. It describes the features of Release 5.3 and list the enhancements and fixes that have been made since previous releases. NX 200 is described in the *Intelligent Ethernet Controller Reference Manual* for your EXOS 200 Series board.

If you should have any questions, comments, or suggestions, please contact

Customer Service Center
Excelan, Inc.
2180 Fortune Drive
San Jose, CA 95131
(408) 434-2285

FEEDBACK

Your feedback on this firmware is appreciated. An overall evaluation form, as well as a problem report form, are included at the end of these release notes. Please complete them and return them to Excelan.

BUG FIXES AND ENHANCEMENTS IN THIS RELEASE

The following problems in Release 5.0 have been corrected in Release 5.3:

- Disabling carrier sense detection. Carrier sense fault checking is disabled in the EXOS 200 Series boards when the indicated jumper is inserted. This allows for proper operation with DEC DECOM broadband transceivers.
  - EXOS 201: Jumper J5
  - EXOS 202: Jumper J5
  - EXOS 203: Jumper J11
  - EXOS 204: Jumper J8
- Intel 82501 support. Intel 82501 chips (Ethernet Serial Interface) can be used interchangeably with the Seeq 8023A. The new firmware accommodates the unique characteristics of the Intel 82501.
- Avoidance of infinite loops. If the Intel 82586 (Ethernet coprocessor) malfunctions, NX will continue normal operation.
- Oversized packets (link-level mode only). In previous releases of NX, packets composed of fragmented blocks might be transmitted incorrectly. If the cumulative length of the blocks exceeded the maximum packet size, the blocks beyond the maximum length would not get transmitted. Instead, random blocks were incorrectly transmitted in their place.

In the current release, no blocks over the maximum allowable length will be transmitted. Instead, the packet size is reduced to accommodate the blocks whose total size is below or equal to the limit.

For example, if NX has been initialized for a maximum length of 1514 byte and the host wants to transmit blocks with the fragment sizes

200 200 200 200 200 200 200 200

NX will transmit only the first seven blocks (1400 bytes). The message length will be 1404 (the last 4 bytes are the CRC checksum).

- Enhanced performance. In the current release, arming and disarming a timer take about 100 microseconds less per packet than in previous releases.

The following problems in Release 4.4 were corrected in Release 5.0:

- If the cable/transceiver is not correctly installed, an error code will be sent to the user.
- When more than one multicast address is programmed, all slots are now recognized.
- The TRANSMIT request return codes have been corrected.
- All REQUESTS now return packet lengths that include the CRC. This ensures plug-in compatibility between the EXOS 101 and 201 boards.
- EXOS boards can now transmit and receive simultaneously.
- Ethernet packets can now be located anywhere in NX memory.
- When using the EXOS boards in memory-mapped interrupt mode, the extended addressing mapping registers are now guarded from corruption.
- Host-to-EXOS common data structures can now cross physical 64-Kbyte boundaries.