Preliminary

Napalm®

HIGH PERFORMANCE

GRAPHICS ENGINE

FOR

3D GAME ACCELERATION

Revision 1.12

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1 Introduction

1.1 Scope of Document

This is the Data Book for Napalm. This document includes a device overview, pin descriptions, DC and AC parameters, and additional information necessary to design with Napalm.

1.2 Document History

Table 1.1 Document History

Version	Date	Change from previous version
1.0	June 22, 1999	Initial Release
1.1	June 29, 1999	See change bars in Chap 11, Chap 10, Pin Descriptions
1.2	Aug 9, 1999	TV_DATA6, GPIO, Physical Dimensions
1.3	Aug 9, 1999	Added pullup/down to sli/aa pin descriptions
1.4	Aug 18, 1999	No more OD outputs, update pin C4
1.5	Aug 25, 1999	Add strapping notes to memory configuration tables.
1.6	October 5, 1999	Added pins to strapping tables, fixed PD/HP in gpio table Added internal pull-up notes. Corrected AGP_BAL_H/L.
1.7	Nov 8, 1999	Swapped unscrambled TV-out data bits
1.8	Jan 26, 2000	Updated serial port use notes.
1.9	Feb 1, 2000	Fixed AGP_BAL_H/L connections
1.10	Feb 10, 2000	Swap pins: PCI_CLK and SLI_SYNC_IN
1.11	March 13, 2000	Moved pins: DEVICE_ID, PCI_CLK_OUT, KELVIN
1.12	March 29, 2000	Add TV_DATA_10 Strapping

1.3 Devices Covered

This document covers the production version(s). Note that A0 silicon had pins E12 and B16 swapped.

1.4 Audience

This document is tailored to a knowledgeable audience. It is assumed that the reader is familiar with assembly language programming of Pentium® CPU and has a good foundation in computer-generated graphics, especially 3D.
Hardware designers intending to use Napalm should have experience in the design of mixed analog-digital devices with very high bandwidth buses. Some signals have fast edge rates and will behave as transmission lines, requiring controlled impedance traces and short, direct connections. Experience with SGRAM/SDRAM arrays and the PCI/AGP bus will be valuable. Designers are encouraged to study the layout guidelines available from 3dfx Interactive, Inc., as well as the reference designs.

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1.5 Conventions

1.5.1 Acronyms

The first appearance of each TLA (Three Letter Acronym) is followed immediately by the definition in parentheses.

1.5.2 Number Base

Hexadecimal (base 16) numbers use upper case letters ABCDEF. Hexadecimal numbers have a prepended ‘0x’ or an appended ‘h’. The following are examples of hexadecimal numbers: 0x00, 0x3DF, 3DFh, 0x1234, 0x2A. Eight-digit hexadecimal numbers typically contain a space in the middle. For example 0x0123 4567 is an eight-digit hexadecimal number.
Decimal (base 10) numbers have no special indicator. The following are examples of decimal numbers: 1234, 2380, 42.
Binary (base 2) have an appended ‘b’. The following are examples of binary numbers: 00b, 01b, 101010b.
Octal (base 8) numbers are not used in this document.
The value zero is often written as 0, without any quotes and without indication as to size or base.

1.5.3 Object Grouping

Objects that are grouped together are listed in descending order. A range is indicated with surrounding square brackets and a colon between the highest and the lowest in the range. A[7:0] means A7, A6, A5, A4, A3, A2, A1, A0. This convention is used for bits in a register (for example, CR2[7:0]) and for signal pins (for example, PCI_AD[31:0]).

1.5.4 Abbreviations

The following abbreviations are used in this document.

Table 1.2 Abbreviations

Abbreviation	Meaning	Note
kbyte	1024 bytes	
Mbyte	1,048,576 bytes	1024 kbytes
Gbyte	1,073,741,824 bytes	1024 Mbytes
Hz	Hertz	frequency
kHz	1000 Hertz	
MHz	1,000,000 Hertz	
ms	10^{-3} second	period
us	10^{-6} second	
ns	10^{-9} second	
mA	10^{-3} Ampere	current
uA	10^{-6} Ampere	
uF	10^{-6} Farad	capacitance
pF	10^{-12} Farad	

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Table 1.2 Abbreviations *(cont.)*

Abbreviation	Meaning	Note
tbd, na	To Be Determined, Not Available	used interchangeably
Mpixel	1,000,000 pixels	

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2 Product Overview

2.1 Introduction

The 3dfx Interactive, Inc. Napalm graphics accelerator integrates powerful new 3D features with 2D and video capabilities. Fully forward-compatible with Voodoo3 driver software, Napalm incorporates 3dfx's T-buffer™ technology to provide stunning image-quality features such as full-screen antialiasing, motion blur, and depth of field blur. Scalability through scanline interleave allows multi-chip configurations to offer industry-leading 3D fill rates, while 4X AGP support ensures the highest possible host -bandwidth available on the PC platform. Up to 64 MB frame buffer support means that Napalm can manage huge volumes of texture data from the most demanding 3D applications. Napalm provides a unique combination of full Voodoo compatibility, standard-setting image quality features, scalable performance, and unparalleled 3D API compatibility.

2.1.1 Voodoo Graphics Glide 2.X and 3.X Compatibility

Since Napalm is upward compatible with Voodoo® 3D, hundreds of 3D titles that have been optimized for acceleration on Voodoo Graphics, Voodoo Rush, Voodoo^2, Voodoo Banshee, and Voodoo3 will run on Napalm without modification. Of course, to take full advantage of the Napalm enhanced features, it will be necessary make changes.

2.1.2 3D Performance and Quality

3dfx Interactive, Inc. is the industry leader in delivering 3D technology for the PC consumer market. Napalm will continue this heritage, delivering 400 Mpix/sec and over 10 million triangles per second single-cycle multi-texturing 3D performance. The design philosophy behind all products of 3dfx Interactive, Inc. is to provide advanced 3D features with the universal requirement of all serious game developers: **no degradation in performance and quality**.

2.1.3 Optimized for Pentium® III, AMD K7®, and AGP-4X Platform

Napalm fully exploits the processing power of Pentium® III or AMD K7®, including direct hardware handling of out-of-order writes. From the very beginning, Napalm was designed to maximize the performance of Pentium I/O architecture. The AGP interface is tuned for optimal 3D performance, and supports sideband addressing for very fast texture downloading and full 4X 266 MHz AGP bus operation.

2.1.4 Windows® GUI/Video Acceleration

Napalm is a full 128-bit graphics accelerator with 128-bit frame buffer interface. Even the VGA core is 128 bits. The design philosophy has been to implement the Microsoft GDI (Graphics Device Interface) in hardware for outstanding windows acceleration. Napalm supports the new features of Windows98 (for example, multi-monitor support) and is PC99a compliant.

2.1.5 DVD Acceleration

The video architecture of Napalm is optimized for software DVD acceleration. This optimization includes large FIFOs, YUV 4:2:0 planar to packed pixel conversion with AGP bus-mastering, automatic double-buffering, and alpha blending for sub-picture support.

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2.2 Feature List

2.2.1 General Features

- Fully integrated 128-bit VGA/2D/3D/Video Accelerator
- Ultimate 3D experience with 400 Mpixels/sec and 10 million triangles/sec
- T-buffer™ antialiasing technology
  - Spatial: full-scene 2-, 4-, or 8-sample antialiasing
  - Focus: Depth of field blur
  - Motion: Motion blur
- 2-way and 4-way SLI scalability
- 4X AGP with full sideband support
- 8 MB to 64 MB frame buffer support (128-bit bus)
- 32-bit rendering
- 24-bit floating point depth buffer (Z or W)
- 8-bit stencil buffer
- 32-bit textures
- 2K x 2K maximum texture size
- Industry-standard and proprietary texture compression
- Fully software-compatible with 3dfx Voodoo3

2.2.2 3D Acceleration

- 32-bit rendering
- Dual pixel pipeline: 2 pixels/clock (single texture) or 2 textures/clock (single pixel)
- Full-screen antialiasing in hardware
  - One chip: 2-sample antialiasing
  - Two chips: 4-sample antialiasing
  - Four chips: 8-sample antialiasing
- Full hardware setup of triangle parameters
- Supports multi-triangle strips and fans
- 24-bit floating-point depth buffer (Z or W)
- 8-bit stencil buffer
- Transparency and chroma-key with dedicated color mask
- Alpha blending of source and destination pixels
- Sub-pixel and sub-texel correction to 0.4 x 0.4 resolution
- Per-pixel atmospheric fog with programmable fog zones
- Full-scene polygon-based edge anti-aliasing
- Dynamic environment mapping
- Perspective correct (true divide-per-pixel) 3D texture mapping and Gouraud shading
- Single-cycle bump mapping
- Single-cycle Trilinear Mip-mapping
- True per-pixel LOD (level-of-detail) MIP mapping with biasing and clamping
- RGB modulation combines textures and shaded pixels
- Texture compositing for multi-texture special effects
  - All DX7 and OpenGL 1.2 texture blends
- Support for 14 different texture map formats
- 8-bit palletized textures with full bilinear filtering
- Four-bit per texel texture compression through Microsoft Direct X and 3dfx proprietary algorithms

2.2.3 2D Acceleration

- 128-bit VGA
- 128-bit Windows GUI acceleration
- Fully-featured 128-bit BitBlt Engine: Windows GDI in hardware
- Acceleration for Bresenham line draw, polygon fill, 256 ROP, scissor/rectangle clippers
- SGRAM function support: color expansion, block write

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2.2.4 Video Acceleration and Features

- Planar to packed-pixel digital video format conversion
- Digital video port for NTSC/PAL TV-out
- Full VMI 1.4 video port support with CCIR 656 extension
- Direct connection to TMDS transmitter for DVI, DFP, and P&D flat panel support
- 350 MHz RAMDAC for 2048 x 1536 85 Hz display support

2.2.5 Host Interface

- AGP 4X includes optimized support for sideband addressing
- FIFO optimized for high speed bursting of geometry and texture data
- Bi-endian byte ordering support
- Hardware support for Pentium II out of order writes

2.2.6 Memory System

- Supports x 16 and x 32 SDR SDRAM and SGRAM
- 128-bit configurations from 8 MB to 64 MB
- Up to 200 MHz memory clock

2.2.7 Process and Package Technology

- Custom IC fabricated in 0.25 micron, 5 metal layer CMOS
- 548-lead plastic BGA (PBGA) package
- 2.5 volt core, 3.3 volt I/O, 3.3/1.5 volt AGP interface
- Full scan to ensure > 95% fault coverage for extremely high reliability

2.2.8 Software

- Forward-compatible with Voodoo3 driver
- Backward-compatible driver available for Voodoo3
- Windows9X, Win2K, Win NT4.0 device drivers
- World's most comprehensive 3D API support: Microsoft DirectX, OpenGL, Glide 2.X and 3.X
- MPEG2: Support for hardware and software MPEG2 encoders and decoders from leading suppliers

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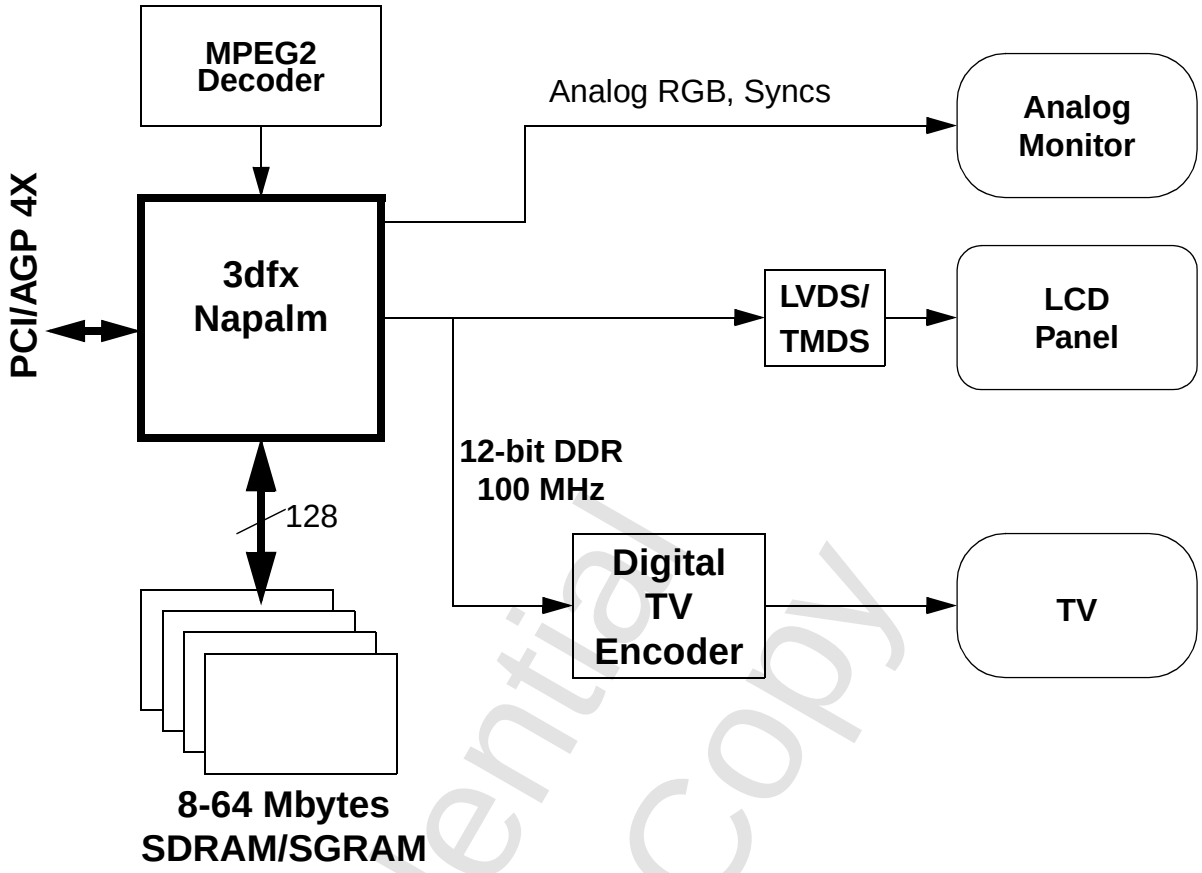

Figure 2.1 System Block Diagram

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3 Pins

3.1 Introduction

The Napalm pins are described in this chapter. Included are pin diagrams, pin tables, and detailed pin descriptions. Where appropriate, the detailed pin descriptions include board design notes.

3.2 Pin Diagrams

Napalm is available in a 548-lead PBGA. Figure 3.1 is a high-level diagram showing the location of the buses for reference only. Table 3.1 is the detailed pin diagram.

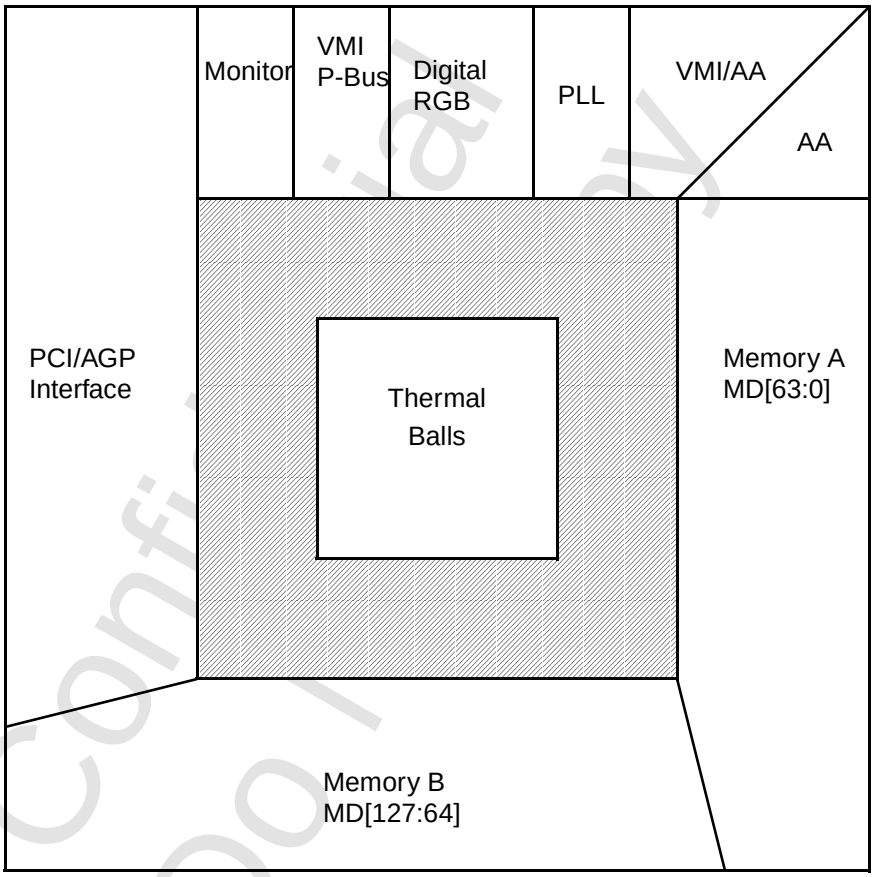

Figure 3.1 Bus Diagram

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Table 3.1 Pin Diagram: Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND	GND	PCOS	TEN	HSYNC	DAVDD	DCSRC	BLUE	GND	VPD7	VPD3	TICLK	TVSNC	TVD8	TVD3	SSOUT	GND	PAVDD0	PAVSS1	GPIO2	ROMWE	VRST	VHD6	VHD5	GND	GND
B	GND	GND	DIDL	IDDQ	VSYNC	DCS0	DRSET	GREEN	VBLNK	VPD6	VPD2	TBLNK	THSNC	TVD7	TVD2	PCLKI	AAVDD	XOUT	PAVDD1	GPIO1	ROMOE	VHA3	VHD7	VHD4	GND	GND
C	TYPE	BAL_L	BAL_H	VARBF	RDRDY	DCS1	VDDIO	RED	VVSNC	VPD5	VPD1	TCLKO	TVD11	TVD6	TVD1	SCLKI	PAVSS0	VDDIO	SDA0	GPIO0	VINT	VHA2	VHA0	VHD3	VHD2	VHD1
D	PGNT	RST	INTA	RBF	FSTALL	DVSSR	DAVSS	DAVDDI	VHSNC	VPD4	VPD0	TRST	TVD10	TVD5	TVD0	AAVSS	VPLLLF	XIN	SDC0	VSREF	VRDY	VHA1	VHD0	AACLK	AAVAL	AAD11
E	SBA1	SBA0	ST2	ST1	ST0	SCKOT	DCS2	VBG	PD	VPCLK	PCLK0	SSIN	TVD9	TVD4	HPLUG	SYCFB	SDA1	SDC1	ROMCS	VDS	VCS	VRW	AAD10	AAD9	AAD8	AAD7
F	SBA3	VDDQ	GT	VDDQ	SBA2	VDDIO	VDDIO	VDDIO	VDDIO									VDDIO	VDDIO	VDDIO	VDDC	AAD5	AAD4	AAD3	AAD2	AAD1
G	SBA5	SBA4	GT	SBSTN	SBSTB	VDDIO														(G20)	VDDIO	AAD6	AAD0	MD22	MD21	MD19
H	GND	PAD31	SBA7	SBA6	GND	VDDIO														(H)	VDDIO	MD23	MD17	MD16	MDM2	MDM0
J	PAD28	VDDQ	PAD29	VDDQ	PAD30	VDDC			VDDC	VDDC	VDDC	VDDC	GND	GND	VDDC	VDDC	VDDC	VDDC		(J)	VDDIO	MD20	MD7	MD6	MD5	GND
K	GT	PAD24	PAD25	PAD26	PAD27				VDDC	GND	GND	GND	GND	GND	GND	GND	GND	VDDC		(K)		MD18	MD2	VDDIO	MD3	MD4
L	PAD23	CBE3	GT	ADS1N	ADST1				VDDC	GND	GND	GND	GND	GND	GND	GND	GND	VDDC		(L)		MD1	MD13	MD14	MD15	MD0
M	PAD19	VDDQ	PAD22	VDDQ	PAD21				VDDC	GND	GND	GND	GND	GND	GND	GND	GND	VDDC		(M)		MD12	MDM1	MD9	MD10	MD11
N	PAD20	PAD17	PAD18	PAD16	GT				GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		(N)		MD8	MD29	MD30	MD31	MDM3
P	GND	AVR15	AVR30	GT	IDSEL				GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		(P)		MD28	MD24	MD25	MD26	MD27
R	IRDY	FRAME	VDDQ	CBE2	CBE1				VDDC	GND	GND	GND	GND	GND	GND	GND	GND	VDDC		(R)		MD55	MD51	MD52	MD53	MD54
T	DEVSEL	TRDY	STOP	PAR	PAD13				VDDC	GND	GND	GND	GND	GND	GND	GND	GND	VDDC		(T)		MD48	MDM4	VDDIO	MD49	MD50
U	PAD15	VDDQ	PAD14	VDDQ	GND				VDDC	GND	GND	GND	GND	GND	GND	GND	GND	VDDC		(U)		MDM6	MD35	MD36	MD37	MD39
V	GND	PAD12	PAD11	PAD10	ADST0	VDDC			VDDC	VDDC	VDDC	VDDC	GND	GND	VDDC	VDDC	VDDC	VDDC		(V)	VDDIO	MD38	MD32	MD33	MD34	GND
W	PAD9	PAD8	CBE0	GT	ADS0N	VDDIO														(W)	VDDIO	MCLKAI	MD45	MCLKA	MD46	MD47
Y	GT	VDDQ	PAD7	VDDQ	PAD2	VDDIO	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	(Y20)	VDDIO	MDM7	MD43	MD44	MD42	MD41
AA	PAD6	PAD5	PAD4	PAD3	PAD1	VDDIO	VDDIO	VDDIO	VDDIO									VDDIO	VDDIO	VDDIO	VDDC	MA_A11	MD63	MDM5	MD40	MD62
AB	PAD0	MDSFB	MWEB	MCASB	MRASB	MD122	MD123	MD105	MD97	MD103	MDM12	MCLKBI	MD117	MD90	MD95	MD66	MD80	MD81	MD84	MCS0	MCACA	MD61	MD57	MD58	MD59	MD60
AC	MA_B0	MA_B1	MA_B2	MA_B3	MBA_B1	MD125	MD106	MD107	MD111	MD99	MDM14	MD113	MD118	MD91	MDM11	MD74	MD78	MD68	MDM8	MD85	MRASA	MA_A1	MA_A5	MBA_A1	MBA_A0	MD56
AD	MA_B4	MA_B5	MA_B6	MA_B9	MBA_B0	MD126	MD104	MD108	MD96	MD100	VDDIO	MD114	MD119	MD92	MDM9	MD75	VDDIO	MD67	MD71	MD83	MCS1	MA_A0	MA_A4	MA_A8	MA_A9	MA_A10
AE	GND	GND	MA_B7	MA_B11	MD120	MD127	MDM13	MD109	MD98	MD101	MD112	MD115	MD88	MD93	MD72	MD76	MD79	MD65	MD70	MD82	MD87	MDSFA	MA_A3	MA_A7	GND	GND
AF	GND	GND	MA_B8	MA_B10	MD121	MD124	MDM15	MD110	GND	MD102	MCLKB	MD116	MD89	MD94	MD73	MD77	MD64	GND	MD69	MDM10	MD86	MWEA	MA_A2	MA_A6	GND	GND

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3.3 Pin Tables

The following tables contain pin names, pin number, pin type, and a brief description. The pins are organized into the groups shown in Table 3.2.
Within each group, the pins are listed in alphabetical order, higher number first. Because of space limitations in the pin diagram (Table 3.1), it was necessary to abbreviate some pin names. The abbreviated names are in the second column of each table.

Table 3.2 Pin Table Summary

Group	Table	Link
PCI Interface	Table 3.4	Section 3.4.1
AGP Interface	Table 3.5	Section 3.4.2
Frame Buffer Memory	Table 3.6	Section 3.4.3
PLL	Table 3.7	Section 3.4.4
Monitor Interface	Table 3.8	Section 3.4.5
VMI Interface	Table 3.9	Section 3.4.6
Digital RGB Out	Table 3.10	Section 3.4.7
Miscellaneous	Table 3.11	Section 3.4.8
SLI/AA Interface	Table 3.12	Section 3.4.9
Power and Ground	Table 3.13	Section 3.4.10

The following abbreviations are used in the type column in the tables that follow.

Table 3.3 Type Column Key

Type	Description	Note
Ground	Ground Reference	
Input	Always an input	
I or O	Input or output	Depending on how the part is programmed
I or O: PU	I or O with a pullup	(Internal pullup)
I/O	Bidirectional I/O	
I/O: PU	Bidi I/O with a pullup	The (internal) pullup is for power-on configuration.
Out	Always an output	
Out: PU	Output with a pullup	Always an output. The (internal) pullup is for power-on configuration.
Power	Power supply	See description for power level
Wire	No buffer	AGP impedance matching pins, AGP guard traces

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Table 3.4 PCI Interface Pins

Name	Abbr. Name	Position	Type	Description
PCI_AD31	PAD31	H2	I/O	PCI Address and Data Bus
PCI_AD30	PAD30	J5	I/O	PCI Address and Data Bus
PCI_AD29	PAD29	J3	I/O	PCI Address and Data Bus
PCI_AD28	PAD28	J1	I/O	PCI Address and Data Bus
PCI_AD27	PAD27	K5	I/O	PCI Address and Data Bus
PCI_AD26	PAD26	K4	I/O	PCI Address and Data Bus
PCI_AD25	PAD25	K3	I/O	PCI Address and Data Bus
PCI_AD24	PAD24	K2	I/O	PCI Address and Data Bus
PCI_AD23	PAD23	L1	I/O	PCI Address and Data Bus
PCI_AD22	PAD22	M3	I/O	PCI Address and Data Bus
PCI_AD21	PAD21	M5	I/O	PCI Address and Data Bus
PCI_AD20	PAD20	N1	I/O	PCI Address and Data Bus
PCI_AD19	PAD19	M1	I/O	PCI Address and Data Bus
PCI_AD18	PAD18	N3	I/O	PCI Address and Data Bus
PCI_AD17	PAD17	N2	I/O	PCI Address and Data Bus
PCI_AD16	PAD16	N4	I/O	PCI Address and Data Bus
PCI_AD15	PAD15	U1	I/O	PCI Address and Data Bus
PCI_AD14	PAD14	U3	I/O	PCI Address and Data Bus
PCI_AD13	PAD13	T5	I/O	PCI Address and Data Bus
PCI_AD12	PAD12	V2	I/O	PCI Address and Data Bus
PCI_AD11	PAD11	V3	I/O	PCI Address and Data Bus
PCI_AD10	PAD10	V4	I/O	PCI Address and Data Bus
PCI_AD9	PAD9	W1	I/O	PCI Address and Data Bus
PCI_AD8	PAD8	W2	I/O	PCI Address and Data Bus
PCI_AD7	PAD7	Y3	I/O	PCI Address and Data Bus
PCI_AD6	PAD6	AA1	I/O	PCI Address and Data Bus
PCI_AD5	PAD5	AA2	I/O	PCI Address and Data Bus

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Table 3.4 PCI Interface Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
PCI_AD4	PAD4	AA3	I/O	PCI Address and Data Bus
PCI_AD3	PAD3	AA4	I/O	PCI Address and Data Bus
PCI_AD2	PAD2	Y5	I/O	PCI Address and Data Bus
PCI_AD1	PAD1	AA5	I/O	PCI Address and Data Bus
PCI_AD0	PAD0	AB1	I/O	PCI Address and Data Bus
PCI_CBE3	CBE3	L2	Input	PCI Command and Byte Enables
PCI_CBE2	CBE2	R4	Input	PCI Command and Byte Enables
PCI_CBE1	CBE1	R5	Input	PCI Command and Byte Enables
PCI_CBE0	CBE0	W3	Input	PCI Command and Byte Enables
PCI_CLK_IN	PCLKI	B16	Input	PCI Clock In (was E12 on A0 Si)
PCI_CLK_OUT	PCLKO	E11	Input	PCI Clock Out
PCI_DEVSEL	DEVSEL	T1	I/O	PCI Device Select
PCI_FRAME	FRAME	R2	Input	PCI Transfer Frame
PCI_GNT_N	PGNT	D1	Input	PCI Bus Grant
PCI_IDSEL	IDSEL	P5	Input	PCI Initialization Device Select
PCI_INTA_N	INTA	D3	Out	PCI Interrupt Request
PCI_IRDY_N	IRDY	R1	Input	PCI Initiator Ready
PCI_PAR	PAR	T4	I/O	PCI Bus Parity
PCI_RESET_N	RST	D2	Input	PCI System Reset
PCI_STOP_N	STOP	T3	Out	PCI Transfer Stop
PCI_TRDY_N	TRDY	T2	I/O	PCI Target Ready

Table 3.5 AGP Interface Pins

Name	Abbr. Name	Position	Type	Description
AGP_AD_STB1	ADST1	L5	Input	AD Bus Strobe 1
AGP_AD_STB1_N	ADS1N	L4	Input	AD Bus Strobe 1 Complement

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Table 3.5 AGP Interface Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
AGP_AD_STB0	ADST0	V5	Input	AD Bus Strobe 0
AGP_AD_STB0_N	ADS0N	W5	Input	AD Bus Strobe 0 Complement
AGP_BAL_H	BAL_H	C3	Wire	AGP Impedance Matching High
AGP_BAL_L	BAL_L	C2	Wire	AGP Impedance Matching Low
AGP_RBF_N	RBF	D4	Out	AGP Read Buffer Full
AGP_SB_STB	SBSTB	G5	Out	AGP Sideband Strobe
AGP_SB_STB_N	SBSTN	G4	Out	AGP Sideband Strobe Complemnt
AGP_SBA7	SBA7	H3	Out	AGP Sideband Address Bus
AGP_SBA6	SBA6	H4	Out	AGP Sideband Address Bus
AGP_SBA5	SBA5	G1	Out	AGP Sideband Address Bus
APG_SBA4	SBA4	G2	Out	AGP Sideband Address Bus
AGP_SBA3	SBA3	F1	Out	AGP Sideband Address Bus
AGP_SBA2	SBA2	F5	Out	AGP Sideband Address Bus
AGP_SBA1	SBA1	E1	Out	AGP Sideband Address Bus
AGP_SBA0	SBA0	E2	Out	AGP Sideband Address Bus
AGP_ST2	ST2	E3	Input	AGP Status Bus
AGP_ST1	ST1	E4	Input	AGP Status Bus
AGP_ST0	ST0	E5	Input	AGP Status Bus
TYPEDET	TYPE	C1	Input	AGP Signaling Level Indicator
AGP_VREF_1_5V	AVR15	P2	Wire	AGP Voltage Reference
AGP_VREF_3V	AVR30	P3	Wire	AGP Voltage Reference
GND_AGP_G	GT	F3	Wire	AGP Guard Trace: SB_STB/_N
GND_AGP_G	GT	G3	Wire	AGP Guard Trace: SB_STB/_N
GND_AGP_G	GT	K1	Wire	AGP Guard Trace: AD_STB1/_N
GND_AGP_G	GT	L3	Wire	AGP Guard Trace: AD_STB1/_N
GND_AGP_G	GT	N5	Wire	AGP Guard Trace: VREF
GND_AGP_G	GT	P4	Wire	AGP Guard Trace: VREF
GND_AGP_G	GT	W4	Wire	AGP Guard Trace: AD_STB0/_N

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Table 3.5 AGP Interface Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
GND_AGP_G	GT	Y1	Wire	AGP Guard Trace: AD_STB0/_N

Table 3.6 Frame Buffer Interface Pins

Name	Abbr. Name	Position	Type	Description
MA_A11	MA_A11	AA22	Out	Frame Buffer Port A Address
MA_A10	MA_A10	AD26	Out	Frame Buffer Port A Address
MA_A9	MA_A9	AD25	Out	Frame Buffer Port A Address
MA_A8	MA_A8	AD24	Out	Frame Buffer Port A Address
MA_A7	MA_A7	AE24	Out	Frame Buffer Port A Address
MA_A6	MA_A6	AF24	Out	Frame Buffer Port A Address
MA_A5	MA_A5	AC23	Out	Frame Buffer Port A Address
MA_A4	MA_A4	AD23	Out	Frame Buffer Port A Address
MA_A3	MA_A3	AE23	Out	Frame Buffer Port A Address
MA_A2	MA_A2	AF23	Out	Frame Buffer Port A Address
MA_A1	MA_A1	AC22	Out	Frame Buffer Port A Address
MA_A0	MA_A0	AD22	Out	Frame Buffer Port A Address
MA_B11	MA_B11	AE4	Out	Frame Buffer Port B Address
MA_B10	MA_B10	AF4	Out	Frame Buffer Port B Address
MA_B9	MA_B9	AD4	Out	Frame Buffer Port B Address
MA_B8	MA_B8	AF3	Out	Frame Buffer Port B Address
MA_B7	MA_B7	AE3	Out	Frame Buffer Port B Address
MA_B6	MA_B6	AD3	Out	Frame Buffer Port B Address
MA_B5	MA_B5	AD2	Out	Frame Buffer Port B Address
MA_B4	MA_B4	AD1	Out	Frame Buffer Port B Address
MA_B3	MA_B3	AC4	Out	Frame Buffer Port B Address
MA_B2	MA_B2	AC3	Out	Frame Buffer Port B Address

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Table 3.6 Frame Buffer Interface Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
MA_B1	MA_B1	AC2	Out	Frame Buffer Port B Address
MA_B0	MA_B0	AC1	Out	Frame Buffer Port B Address
MBA_A1	MB_A1	AC24	Out	Frame Buffer Port A Bank Address
MBA_A0	MB_A0	AC25	Out	Frame Buffer Port A Bank Address
MBA_B1	MB_B1	AC5	Out	Frame Buffer Port B Bank Address
MBA_B0	MB_B0	AD5	Out	Frame Buffer Port B Bank Address
MCAS_A	MCACA	AB21	Out	Frame Buffer Port A CAS
MCAS_B	MCASB	AB4	Out	Frame Buffer Port B CAS
MCLKA	MCLKA	W24	Out	Frame Buffer Port A Clock Out
MCLKA_IN	MCLKAI	W22	Input	Frame Buffer Port A Clock Feedback
MCLKB	MCLKB	AF11	Out	Frame Buffer Port B Clock Out
MCLKB_IN	MCLKBI	AB12	Input	Frame Buffer Port B Clock Feedback
MCS_1	MCS1	AD21	Out	Frame Buffer Bank 1 Chip Select
MSC_0	MCS0	AB20	Out	Frame Buffer Bank 0 Chip Select
MD127	MD127	AE6	I/O	Frame Buffer Data Bus
MD126	MD126	AD6	I/O	Frame Buffer Data Bus
MD125	MD125	AC6	I/O	Frame Buffer Data Bus
MD124	MD124	AF6	I/O	Frame Buffer Data Bus
MD123	MD123	AB7	I/O	Frame Buffer Data Bus
MD122	MD122	AB6	I/O	Frame Buffer Data Bus
MD121	MD121	AF5	I/O	Frame Buffer Data Bus
MD120	MD120	AE5	I/O	Frame Buffer Data Bus
MD119	MD119	AD13	I/O	Frame Buffer Data Bus
MD118	MD118	AC13	I/O	Frame Buffer Data Bus
MD117	MD117	AB13	I/O	Frame Buffer Data Bus
MD116	MD116	AF12	I/O	Frame Buffer Data Bus
MD115	MD115	AE12	I/O	Frame Buffer Data Bus
MD114	MD114	AD12	I/O	Frame Buffer Data Bus

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Table 3.6 Frame Buffer Interface Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
MD113	MD113	AC12	I/O	Frame Buffer Data Bus
MD112	MD112	AE11	I/O	Frame Buffer Data Bus
MD111	MD111	AC9	I/O	Frame Buffer Data Bus
MD110	MD110	AF8	I/O	Frame Buffer Data Bus
MD109	MD109	AE8	I/O	Frame Buffer Data Bus
MD108	MD108	AD8	I/O	Frame Buffer Data Bus
MD107	MD107	AC8	I/O	Frame Buffer Data Bus
MD106	MD106	AC7	I/O	Frame Buffer Data Bus
MD105	MD105	AB8	I/O	Frame Buffer Data Bus
MD104	MD104	AD7	I/O	Frame Buffer Data Bus
MD103	MD103	AB10	I/O	Frame Buffer Data Bus
MD102	MD102	AF10	I/O	Frame Buffer Data Bus
MD101	MD101	AE10	I/O	Frame Buffer Data Bus
MD100	MD100	AD10	I/O	Frame Buffer Data Bus
MD99	MD99	AC10	I/O	Frame Buffer Data Bus
MD98	MD98	AE9	I/O	Frame Buffer Data Bus
MD97	MD97	AB9	I/O	Frame Buffer Data Bus
MD96	MD96	AD9	I/O	Frame Buffer Data Bus
MD95	MD95	AB15	I/O	Frame Buffer Data Bus
MD94	MD94	AF14	I/O	Frame Buffer Data Bus
MD93	MD93	AE14	I/O	Frame Buffer Data Bus
MD92	MD92	AD14	I/O	Frame Buffer Data Bus
MD91	MD91	AC14	I/O	Frame Buffer Data Bus
MD90	MD90	AB14	I/O	Frame Buffer Data Bus
MD89	MD89	AF13	I/O	Frame Buffer Data Bus
MD88	MD88	AE13	I/O	Frame Buffer Data Bus
MD87	MD87	AE21	I/O	Frame Buffer Data Bus
MD86	MD86	AF21	I/O	Frame Buffer Data Bus

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Table 3.6 Frame Buffer Interface Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
MD85	MD85	AC20	I/O	Frame Buffer Data Bus
MD84	MD84	AB19	I/O	Frame Buffer Data Bus
MD83	MD83	AD20	I/O	Frame Buffer Data Bus
MD82	MD82	AE20	I/O	Frame Buffer Data Bus
MD81	MD81	AB18	I/O	Frame Buffer Data Bus
MD80	MD80	AB17	I/O	Frame Buffer Data Bus
MD79	MD79	AE17	I/O	Frame Buffer Data Bus
MD78	MD78	AC17	I/O	Frame Buffer Data Bus
MD77	MD77	AF16	I/O	Frame Buffer Data Bus
MD76	MD76	AE16	I/O	Frame Buffer Data Bus
MD75	MD75	AD16	I/O	Frame Buffer Data Bus
MD74	MD74	AC16	I/O	Frame Buffer Data Bus
MD73	MD73	AF15	I/O	Frame Buffer Data Bus
MD72	MD72	AE15	I/O	Frame Buffer Data Bus
MD71	MD71	AD19	I/O	Frame Buffer Data Bus
MD70	MD70	AE19	I/O	Frame Buffer Data Bus
MD69	MD69	AF19	I/O	Frame Buffer Data Bus
MD68	MD68	AC18	I/O	Frame Buffer Data Bus
MD67	MD67	AD18	I/O	Frame Buffer Data Bus
MD66	MD66	AB16	I/O	Frame Buffer Data Bus
MD65	MD65	AE18	I/O	Frame Buffer Data Bus
MD64	MD64	AF17	I/O	Frame Buffer Data Bus
MD63	MD63	AA23	I/O	Frame Buffer Data Bus
MD62	MD62	AA26	I/O	Frame Buffer Data Bus
MD61	MD61	AB22	I/O	Frame Buffer Data Bus
MD60	MD60	AB26	I/O	Frame Buffer Data Bus
MD59	MD59	AB25	I/O	Frame Buffer Data Bus
MD58	MD58	AB24	I/O	Frame Buffer Data Bus

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Table 3.6 Frame Buffer Interface Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
MD57	MD57	AB23	I/O	Frame Buffer Data Bus
MD56	MD56	AC26	I/O	Frame Buffer Data Bus
MD55	MD55	R22	I/O	Frame Buffer Data Bus
MD54	MD54	R26	I/O	Frame Buffer Data Bus
MD53	MD53	R25	I/O	Frame Buffer Data Bus
MD52	MD52	R24	I/O	Frame Buffer Data Bus
MD51	MD51	R23	I/O	Frame Buffer Data Bus
MD50	MD50	T26	I/O	Frame Buffer Data Bus
MD49	MD49	T25	I/O	Frame Buffer Data Bus
MD48	MD48	T22	I/O	Frame Buffer Data Bus
MD47	MD47	W26	I/O	Frame Buffer Data Bus
MD46	MD46	W25	I/O	Frame Buffer Data Bus
MD45	MD45	W23	I/O	Frame Buffer Data Bus
MD44	MD44	Y24	I/O	Frame Buffer Data Bus
MD43	MD43	Y23	I/O	Frame Buffer Data Bus
MD42	MD42	Y25	I/O	Frame Buffer Data Bus
MD41	MD41	Y26	I/O	Frame Buffer Data Bus
MD40	MD40	AA25	I/O	Frame Buffer Data Bus
MD39	MD39	U26	I/O	Frame Buffer Data Bus
MD38	MD38	V22	I/O	Frame Buffer Data Bus
MD37	MD37	U25	I/O	Frame Buffer Data Bus
MD36	MD36	U24	I/O	Frame Buffer Data Bus
MD35	MD35	U23	I/O	Frame Buffer Data Bus
MD34	MD34	V25	I/O	Frame Buffer Data Bus
MD33	MD33	V24	I/O	Frame Buffer Data Bus
MD32	MD32	V23	I/O	Frame Buffer Data Bus
MD31	MD31	N25	I/O	Frame Buffer Data Bus
MD30	MD30	N24	I/O	Frame Buffer Data Bus

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Table 3.6 Frame Buffer Interface Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
MD29	MD29	N23	I/O	Frame Buffer Data Bus
MD28	MD28	P22	I/O	Frame Buffer Data Bus
MD27	MD27	P26	I/O	Frame Buffer Data Bus
MD26	MD26	P25	I/O	Frame Buffer Data Bus
MD25	MD25	P24	I/O	Frame Buffer Data Bus
MD24	MD24	P23	I/O	Frame Buffer Data Bus
MD23	MD23	H22	I/O: PU	Frame Buffer Data Bus
MD22	MD22	G24	I/O: PU	Frame Buffer Data Bus
MD21	MD21	G25	I/O: PU	Frame Buffer Data Bus
MD20	MD20	J22	I/O: PU	Frame Buffer Data Bus
MD19	MD19	G26	I/O: PU	Frame Buffer Data Bus
MD18	MD18	K22	I/O: PU	Frame Buffer Data Bus
MD17	MD17	H23	I/O: PU	Frame Buffer Data Bus
MD16	MD16	H24	I/O: PU	Frame Buffer Data Bus
MD15	MD15	L25	I/O: PU	Frame Buffer Data Bus
MD14	MD14	L24	I/O: PU	Frame Buffer Data Bus
MD13	MD13	L23	I/O: PU	Frame Buffer Data Bus
MD12	MD12	M22	I/O: PU	Frame Buffer Data Bus
MD11	MD11	M26	I/O: PU	Frame Buffer Data Bus
MD10	MD10	M25	I/O: PU	Frame Buffer Data Bus
MD9	MD9	M24	I/O: PU	Frame Buffer Data Bus
MD8	MD8	N22	I/O: PU	Frame Buffer Data Bus
MD7	MD7	J23	I/O: PU	Frame Buffer Data Bus
MD6	MD6	J24	I/O: PU	Frame Buffer Data Bus
MD5	MD5	J25	I/O: PU	Frame Buffer Data Bus
MD4	MD4	K26	I/O: PU	Frame Buffer Data Bus
MD3	MD3	K25	I/O: PU	Frame Buffer Data Bus
MD2	MD2	K23	I/O: PU	Frame Buffer Data Bus

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Table 3.6 Frame Buffer Interface Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
MD1	MD1	L22	I/O: PU	Frame Buffer Data Bus
MD0	MD0	L26	I/O: PU	Frame Buffer Data Bus
MDM15	MDM15	AF7	Out	Frame Buffer Data Bus Mask
MDM14	MDM14	AC11	Out	Frame Buffer Data Bus Mask
MDM13	MDM13	AE7	Out	Frame Buffer Data Bus Mask
MDM12	MDM12	AB11	Out	Frame Buffer Data Bus Mask
MDM11	MDM11	AC15	Out	Frame Buffer Data Bus Mask
MDM10	MDM10	AF20	Out	Frame Buffer Data Bus Mask
MDM9	MDM9	AD15	Out	Frame Buffer Data Bus Mask
MDM8	MDM8	AC19	Out	Frame Buffer Data Bus Mask
MDM7	MDM7	Y22	Out	Frame Buffer Data Bus Mask
MDM6	MDM6	U22	Out	Frame Buffer Data Bus Mask
MDM5	MDM5	AA24	Out	Frame Buffer Data Bus Mask
MDM4	MDM4	T23	Out	Frame Buffer Data Bus Mask
MDM3	MDM3	N26	Out	Frame Buffer Data Bus Mask
MDM2	MDM2	H25	Out	Frame Buffer Data Bus Mask
MDM1	MDM1	M23	Out	Frame Buffer Data Bus Mask
MDM0	MDM0	H26	Out	Frame Buffer Data Bus Mask
MDSF_A	MDSFA	AE22	Out	Frame Buffer A Special Function
MSDF_B	MDSFB	AB2	Out	Frame Buffer B Special Function
MRAS_A	MRASA	AC21	Out	Frame Buffer Port A RAS
MRAS_B	MRASB	AB5	Out	Frame Buffer Port B RAS
MWE_A	MWEA	AF22	Out	Frame Buffer Port A Write Enable
MWE_B	MWEB	AB3	Out	Frame Buffer Port B Write Enable

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Table 3.7 PLL Interface Pins

Name	Abbr. Name	Position	Type	Description
AGP_PLL_VDD	AAVDD	B17	Power	AGP Phase Locked Loop Power
PLL_AVDD1	PAVDD1	B19	Power	Phase Locked Loop Power
PLL_AVDD0	PAVDD0	A18	Power	Phase Locked Loop Power
AGP_PLL_VSS	AAVSS	D16	Power	AGP Phase Locked Loop Ground
PLL_AVSS1	PAVSS1	A19	Power	Phase Locked Loop Ground
PLL_AVSS0	PAVSS0	C17	Power	Phase Locked Loop Ground
VPLL_LF	VPLLLF	D17	Wire	Video PLL Loop Filter (test point)

Table 3.8 Monitor, DAC Pins

Name	Abbr. Name	Position	Type	Description
BLUE	BLUE	A8	Out	DAC Analog Blue
DAC_AVDD	DAVDD	A6	Power	DAC Power
DAC_AVDD_I	DAVDDI	D8	Power	DAC Power
DAC_AVSS	DAVSS	D7	Ground	DAC Ground
DAC_AVSS_R	DVSSR	D6	Ground	DAC Ground
DAC_RSET	DRSET	B7	Wire	DAC Full Scale Set
GREEN	GREEN	B8	Out	DAC Analog Green
HSYNC	HSYNC	A5	Out	Horizontal Sync to Monitor
RED	RED	C8	Out	DAC Analog Red
VSYNC	VSYNC	B5	Out	Vertical Sync to Monitor

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Table 3.9 VMI Pins

Name	Abbr. Name	Position	Type	Description
VMI_BLANK	VBLNK	B9	I/O	External VMI Blank Signal
VMI_CS_N	VCS	E21	I/O	External VMI Chip Select
VMI_DS_N	VDS	E20	I/O	External VMI Data Strobe
VMI_HA3	VHA3	B22	Out: PU	VMI Host Port Address Bus
VMI_HA2	VHA2	C22	Out: PU	VMI Host Port Address Bus
VMI_HA1	VHA1	D22	Out: PU	VMI Host Port Address Bus
VMI_HA0	VHA0	C23	Out: PU	VMI Host Port Address Bus
VMI_HD7	VHD7	B23	I/O: PU	VMI Host Port Data Bus
VMI_HD6	VHD6	A23	I/O: PU	VMI Host Port Data Bus
VMI_HD5	VHD5	A24	I/O: PU	VMI Host Port Data Bus
VMI_HD4	VHD4	B24	I/O: PU	VMI Host Port Data Bus
VMI_HD3	VHD3	C24	I/O: PU	VMI Host Port Data Bus
VMI_HD2	VHD2	C25	I/O: PU	VMI Host Port Data Bus
VMI_HD1	VHD1	C26	I/O: PU	VMI Host Port Data Bus
VMI_HD0	VHD0	D23	I/O: PU	VMI Host Port Data Bus
VMI_HSYNC	VHSNC	D9	I/O	VMI Horizontal Sync
VMI_INT_N	VINT	C21	In?	VMI Interrupt: *Verify direction*
VMI_PCLK	VPCLK	E10	I/O	VMI Pixel Clock
VMI_PD7	VPD7	A10	I/O	VMI Pixel Bus
VMI_PD6	VPD6	B10	I/O	VMI Pixel Bus
VMI_PD5	VPD5	C10	I/O	VMI Pixel Bus
VMI_PD4	VPD4	D10	I/O	VMI Pixel Bus
VMI_PD3	VPD3	A11	I/O	VMI Pixel Bus
VMI_PD2	VPD2	B11	I/O	VMI Pixel Bus
VMI_PD1	VPD1	C11	I/O	VMI Pixel Bus
VMI_PD0	VPD0	D11	I/O	VMI Pixel Bus
VMI_RDY_N	VRDY	D21	I/O	VMI Ready

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Table 3.9 VMI Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
VMI_RESET_N	VRST	A22	I/O	VMI Reset
VMI_RW_N	VRW	E22	I/O	VMI Host Port Read/Write
VMI_VSYNC	VVSYNC	C9	I/O	VMI Vertical Sync

Table 3.10 Digital RGB Interface Pins

Name	Abbr. Name	Position	Type	Description
HOT_PLUG	HPLUG	E15	I/O: PU	Digital Input
PD	PD	E9	I/O: PU	Digital Out
TV_BLANK	TBLNK	B12	I/O: PU	Digital RGB Blank
TV_CLK_OUT	TCLKO	C12	I/O	Digital RGB Clock Out
TV_DATA11	TVD11	C13	I/O: PU	Digital RGB Data Bus
TV_DATA10	TVD10	D13	I/O: PU	Digital RGB Data Bus
TV_DATA9	TVD9	E13	I/O: PU	Digital RGB Data Bus
TV_DATA8	TVD8	A14	I/O: PU	Digital RGB Data Bus
TV_DATA7	TVD7	B14	I/O: PU	Digital RGB Data Bus
TV_DATA6	TVD6	C14	I/O: PU	Digital RGB Data Bus
TV_DATA5	TVD5	D14	I/O: PU	Digital RGB Data Bus
TV_DATA4	TVD4	E14	I/O: PU	Digital RGB Data Bus
TV_DATA3	TVD3	A15	I/O: PU	Digital RGB Data Bus
TV_DATA2	TVD2	B15	I/O: PU	Digital RGB Data Bus
TV_DATA1	TVD1	C15	I/O: PU	Digital RGB Data Bus
TV_DATA0	TVD0	D15	I/O: PU	Digital RGB Data Bus
TV_HSYNC	THSNC	B13	I/O: PU	Digital RGB HSYNC
TV_INCLK	TICLK	A12	Input	Digital RGB Clock In
TV_RESET	TRST	D12	I/O: PU	Digital RGB Reset
TV_VSYNC	TVSNC	A13	I/O: PU	Digital RGB VSYNC

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Table 3.11 Miscellaneous Pins

Name	Abbr. Name	Position	Type	Description
DEVICE_ID_LSB_N	DIDL	B3	Input	Device ID LSB (PCI00)
GPIO_2	GPIO2	A20	Input	‘GPIO’ (Input Only)
GPIO_1	GPIO1	B20	Out	‘GPIO’ (Output Only)
GPIO_0	GPIO0	C20	Out	‘GPIO’ (ROM Decode: Output)
PCI_CLK_OUT_SEL	PCOS	A3	Input	Factory Testing
ROM_CS_N	ROMCS	E19	Out	ROM Chip Select
ROM_OE_N	ROMOE	B21	Out	ROM Output Enable
ROM_WE_N	ROMWE	A21	Out	ROM Write Enable
SDA1	SDA1	E17	I/O	VMI (Feature Connector)
SDA0	SDA0	C19	I/O	DDC (Monitor Connector)
SDC1	SDC1	E18	I/O	VMI (Feature Connector)
SDC0	SDC0	D19	I/O	DDC (Monitor Connector)
TEST_ENABLE	TEN	A4	Input	Factory Testing
XIN	XIN	D18	Wire	Crystal In
XOUT	XOUT	B18	Wire	Crystal Out

Table 3.12 SLI/AA Dedicated Pins

Name	Abbr. Name	Position	Type	Description
AA_CLK	AACLK	D24	I or O: PU	SLI/AA Data Clock
AA_DATA_11	AAD11	D26	I or O: PU	AA Data Bus
AA_DATA_10	AAD10	E23	I or O: PU	AA Data Bus
AA_DATA_9	AAD9	E24	I or O: PU	AA Data Bus
AA_DATA_8	AAD8	E25	I or O: PU	AA Data Bus
AA_DATA_7	AAD7	E26	I or O: PU	AA Data Bus
AA_DATA_6	AAD6	G22	I or O: PU	AA Data Bus

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Table 3.12 SLI/AA Dedicated Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
AA_DATA_5	AAD5	F22	I or O: PU	AA Data Bus
AA_DATA_4	AAD4	F23	I or O: PU	AA Data Bus
AA_DATA_3	AAD3	F24	I or O: PU	AA Data Bus
AA_DATA_2	AAD2	F25	I or O: PU	AA Data Bus
AA_DATA_1	AAD1	F26	I or O: PU	AA Data Bus
AA_DATA_0	AAD0	G23	I or O: PU	AA Data Bus
AA_VALID	AAVAL	D25	I or O: PU	AA Data Valid
DAC_CUR_SINK2	DCS0	E7	I or O	DAC Reference Out
DAC_CUR_SINK1	DCS1	C6	I or O	DAC Reference Out
DAC_CUR_SINK0	DCS2	B6	I or O	DAC Reference Out
DAC_CUR_SRC	DCSRC	A7	I or O	DAC Reference In
PCI_FIFO_ST	FSTALL	D5	I or O	PCI FIFO Stall
PCI_RDRDY	RDRY	C5	I or O	Used for CPU reads of AA data
SLI_SYNC_IN	SSIN	E12	Input	Used for CPU writes of AA data (was B16 on A0 Si)
SLI_SYNC_OUT	SSOUT	A16	Out: PU	SLI Sync Chain
SYNC_CLK_FB	SYCFB	E16	Input	SLI Sync Clock Feedback
SYNC_CLK_IN	SCLKI	C16	Input	SLI Sync Clock Input
SYNC_CLK_OUT	SCKOT	E6	Out	SLI Sync Clock Output
VSYNC_REF	VSREF	D20	I or O	SLI Vertical Sync Reference

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Table 3.13 Power and Ground Pins

Name	Abbr. Name	Position	Type	Description
GND	GND	A1	Ground	Ground
GND	GND	A2	Ground	Ground
GND	GND	A9	Ground	Ground
GND	GND	A17	Ground	Ground
GND	GND	A25	Ground	Ground
GND	GND	A26	Ground	Ground
GND	GND	B1	Ground	Ground
GND	GND	B2	Ground	Ground
GND	GND	B25	Ground	Ground
GND	GND	B26	Ground	Ground
GND	GND	H1	Ground	Ground
GND	GND	H5	Ground	Ground
GND	GND	J26	Ground	Ground
GND	GND	P1	Ground	Ground
GND	GND	U5	Ground	Ground
GND	GND	V1	Ground	Ground
GND	GND	V26	Ground	Ground
GND	GND	AE1	Ground	Ground
GND	GND	AE2	Ground	Ground
GND	GND	AE25	Ground	Ground
GND	GND	AE26	Ground	Ground
GND	GND	AF1	Ground	Ground
GND	GND	AF2	Ground	Ground
GND	GND	AF9	Ground	Ground
GND	GND	AF18	Ground	Ground
GND	GND	AF25	Ground	Ground
GND	GND	AF26	Ground	Ground

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Table 3.13 Power and Ground Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
IDDQ	IDDQ	B4		
Thermal Balls	T_BALL	J13, J14 {K:M}{10:17} {N:P}{9:18} {R:U}{10:17} V13, V14	Ground	Thermal Control (72 pins)
VBG	VBG	E8		
VDD_AGP_RBF	VARBF	C4	Power	RBF Pin Power?
VDD_CORE2.5	VDDC	F21	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	J6	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	J9	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	J10	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	J11	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	J12	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	J15	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	J16	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	J17	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	J18	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	K9	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	K18	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	L9	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	L18	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	M9	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	M18	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	R9	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	R18	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	T9	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	T18	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	U9	Power	Digital Power: Nominally 2.5V

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Table 3.13 Power and Ground Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
VDD_CORE2.5	VDDC	U18	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	V6	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	V9	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	V10	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	V11	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	V12	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	V15	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	V16	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	V17	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	V18	Power	Digital Power: Nominally 2.5V
VDD_CORE2.5	VDDC	AA21	Power	Digital Power: Nominally 2.5V
VDDIO3.3	VDDIO	C7	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	C18	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	F6	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	F7	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	F8	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	F9	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	F18	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	F19	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	F20	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	G6	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	G21	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	H6	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	H21	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	J21	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	K24	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	T24	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	V21	Power	I/O Pad: Nominally 3.3V

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Table 3.13 Power and Ground Pins *(cont.)*

Name	Abbr. Name	Position	Type	Description
VDDIO3.3	VDDIO	W6	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	W21	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	Y6	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	Y21	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	AA6	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	AA7	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	AA8	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	AA9	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	AA18	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	AA19	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	AA20	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	AD11	Power	I/O Pad: Nominally 3.3V
VDDIO3.3	VDDIO	AD17	Power	I/O Pad: Nominally 3.3V
VDDQ3.3/1.5	VDDQ	F2	Power	PCI/AGP IO: 3.3V or 1.5V
VDDQ3.3/1.5	VDDQ	F4	Power	PCI/AGP IO: 3.3V or 1.5V
VDDQ3.3/1.5	VDDQ	J2	Power	PCI/AGP IO: 3.3V or 1.5V
VDDQ3.3/1.5	VDDQ	J4	Power	PCI/AGP IO: 3.3V or 1.5V
VDDQ3.3/1.5	VDDQ	M2	Power	PCI/AGP IO: 3.3V or 1.5V
VDDQ3.3/1.5	VDDQ	M4	Power	PCI/AGP IO: 3.3V or 1.5V
VDDQ3.3/1.5	VDDQ	R3	Power	PCI/AGP IO: 3.3V or 1.5V
VDDQ3.3/1.5	VDDQ	U2	Power	PCI/AGP IO: 3.3V or 1.5V
VDDQ3.3/1.5	VDDQ	U4	Power	PCI/AGP IO: 3.3V or 1.5V
VDDQ3.3/1.5	VDDQ	Y2	Power	PCI/AGP IO: 3.3V or 1.5V
VDDQ3.3/1.5	VDDQ	Y4	Power	PCI/AGP IO: 3.3V or 1.5V

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3.4 Pin Descriptions

The following sections are the detailed, formal pin descriptions. These descriptions are organized exactly the same as the tables.

3.4.1 PCI Interface

The pins on the PCI interface connect directly to the corresponding pins on the PCI bus. These pins are organized so that short, direct traces can be run to the connector.

Name	Description
PCI_AD[31:0]	**PCI Address and Data:** This multiplexed, bidirectional bus transfers address and data during any memory or I/O transaction. The address is on the bus during the clock phase in which PCI_FRAME is active. For I/O, this is a byte address; for configuration and memory transactions, this is a DWORD address. During the data phase(s), PCI_AD[7:0] contain the least significant byte and PCI_AD[31:24] contain the most significant byte. Write data is stable and valid when PCI_IRDY_N is asserted and read data is stable and valid when PCI_TRDY_N is asserted. Data is transferred during those clocks in which both PCI_IRDY_N and PCI_TRDY_N are asserted.
PCI_CBE[3:0]	**PCI Bus Command and Byte Enables:** These multiplexed pins transfer the bus command and byte enables for any transaction. During the address phase, these pins are driven by the initiator with the bus command. During data phase(s) these pins are used as byte enables. Byte Enables are valid for the entire data cycle and specify the byte lanes that carry meaningful data. PCI_CBE0 is associated with PCI_AD[7:0]; PCI_CBE3 is associated with PCI_AD[31:24].
PCI_CLK_IN	**PCI Clock:** The clock provides timing for all transactions on PCI. All PCI timing is defined with respect to the rising edge of this clock. Napalm supports 66 MHz PCI Clock.
PCI_CLK_OUT	**PCI Clock Out:** Either of two internal clocks can be driven onto this pin, according to the table. This output is for factory testing and should be a no connect in any production application. This pin is connected to a test point on the reference design.

PCI_CLK_OUT_SEL	Output	Comment
0	pci_66_clk_mon	output of agpsynchro, at the source of the clock tree
1	pci_clk	..from middle of clock tree

PCI_DEVSEL	**PCI Bus Device Select:** When a device drives this signal active, it indicates the device has decoded the address on the bus as belonging to itself. This signal is a sustained Tri-State output as defined in the PCI specification.
PCI_FRAME	**PCI Bus Cycle Frame:** This signal is driven by the initiator to indicate the beginning and duration of an access. PCI_FRAME is asserted to indicate a bus transaction is beginning. While PCI_FRAME is active, data transfers continue. When PCI_FRAME is deasserted, the transaction is in the final data phase.

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3.4.1 PCI Interface *(cont)*

Name	Description
PCI_GNT_N	**PCI Bus Grant:** This input indicates to the agent that bus access is granted. This is a point-to-point signal; each master has its own GNT. This pin is used without PCI bus request (REQ#) for AGP. This pin must be pulled down on chips that are configured as SLI slaves, or are on a PCI card, or both.
PCI_IDSEL	**PCI Bus Initialization Device Select:** This input is a chip select in lieu of the upper 24 address lines during configuration read and write cycles. This signal is replaced with AD16 when Napalm is configured for AGP.
PCI_INTA_N	**PCI Bus Interrupt Request:** This open-collector output is driven low when Napalm is requesting an interrupt. This pin is always connected to INTA#.
PCI_IRDY_N	**PCI Bus Initiator Ready:** This active-low signal indicates the initiating agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock during which both PCI_IRDY_N and PCI_TRDY_N are sampled active. During a write, PCI_IRDY_N indicates that valid data is present on PCI_AD[31:0]. During a read, PCI_IRDY_N indicates the bus master is ready to accept data. Wait cycles are inserted until both PCI_IRDY_N and PCI_TRDY_N are asserted together.
PCI_PAR	**PCI Bus Parity:** This signal provides even parity across PCI_AD[31:0] and PCI_CBE[3:0]. Parity generation is required for all PCI agents. Napalm does not check parity.
PCI_RESET_N	**PCI Reset:** This active-low signal initializes the Napalm to a known state. On the rising edge of PCI_RESET_N, the chip reads configuration information from the VMI address and data buses. See Chapter 4. Also, subsystem and subsystem vendor information is loaded from four bytes of the ROM into PCI2C. See the description of register PCI2C in the Programming Guide.
PCI_STOP_N	**PCI Bus Stop Request:** This active-low signal indicates the target is requesting the master to stop the current transaction. This signal is a sustained Tri-State output as defined in the PCI specification.
PCI_TRDY_N	**PCI Bus Target Ready:** This active-low signal indicates the target's ability to complete the current data phase of the transaction. A data phase is completed on any clock during which both PCI_IRDY_N and PCI_TRDY_N are sampled active. During a write, PCI_TRDY_N indicates that the target is ready to accept data. During a read, PCI_TRDY_N indicates valid data is present on PCI_AD[31:0]. Wait cycles are inserted until both PCI_IRDY_N and PCI_TRDY_N are asserted together. This signal is a sustained Tri-State output as defined in the PCI specification.

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3.4.2 AGP Interface

The pins on the AGP interface connect directly to the corresponding pins on the AGP bus. These pins are organized so that short, direct traces can be run to the connector.

Name	Description
AGP_AD_STB1	**AGP AD Bus Strobe 1:** This input provides timing for 2X data transfer mode on AD[31:16]. This pin must be pulled up on chips that are configured as SLI slaves, or are on a PCI card, or both.
AGP_AD_STB1_N	**AGP AD Bus Strobe 1 Complement:** This input is used in conjunction with AGP_AD_STB1 to provide timing for 4X data transfer mode on AD[31:16]. This pin must be pulled down on chips that are configured as SLI slaves, or are on a PCI card, or both.
AGP_AD_STB0	**AGP AD Bus Strobe 0:** This input provides timing for 2X data transfer mode on AD[15:0]. This pin must be pulled up on chips that are configured as SLI slaves, or are on a PCI card, or both.
AGP_AD_STB0_N	**AGP AD Bus Strobe 0 Complement:** This input is used in conjunction with AGP_AD_STB0 to provide timing for 4X data transfer mode on AD[15:0]. This pin must be pulled down on chips that are configured as SLI slaves, or are on a PCI card, or both.
AGP_BAL_H	**AGP Impedance Matching High:** This output is used to dynamically measure the impedance to ground. This output must be connected to a 56 ohm resistor returned to ground. The resistor must be ? mm from the pin and the trace must have the same dimensions as the traces connecting to the AGP interface? Because of power dissipation, the resistor must be at least an 0805 package for AGP 4X designs but may be 0603 for all other designs. The resistor must be present for a PCI card as well as AGP card. See the definition of the iMatchCtrl register in the Programming Guide.
AGP_BAL_L	**AGP Impedance Matching Low:** See above. This pin must be connected to a 56 ohm resistor returned to VDDQ3.3/1.5. Because of power dissipation, the resistor must be at least an 0805 package. The resistor must be present for a PCI card as well as AGP card.
AGP_RBF_N	**AGP Bus Read Buffer Full:** When this active-low output is asserted, the arbiter is not allowed to initiate the return of low priority read data to the master.
AGP_SB_STB:	**AGP Sideband Strobe:** This output provides timing for SBA[7:0] and is always driven by the AGP master. When the Sideband Strobes have been idle, a synchronization cycle must be performed before a request can be enqueued. This pin must be pulled up on chips that are configured as SLI slaves, or are on a PCI card, or both.
AGP_SB_STB_N	**AGP Sideband Strobe Complement:** This output is used in conjunction with AGP_SB_STB to provide timing for SBA[7:0] when 4X timing is supported. This pin must be pulled down on chips that are configured as SLI slaves, or are on a PCI card, or both.
AGP_SBA[7:0]	**AGP Bus Sideband Address Port:** This bus provides an additional bus to pass address and command from the master to the target. Each pin must be pulled up on chips that are configured as SLI slaves, or are on a PCI card, or both.
AGP_ST[2:0]	**AGP Bus Status:** This bus provides information from the arbiter to the Napalm on what it may do. This bus has meaning only when PCI_GNT_N is asserted.

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3.4.2 AGP Interface *(cont)*

Pin	Description
TYPEDET	**AGP Signaling Level Indicator:** If this input is open, the AGP interface uses 3.3 volt signaling. If this input is shorted to ground, the AGP interface uses 1.5 volt signaling. On the evaluation board, this input is connected to a resistor network consisting of a 4.7 kohm resistor to 3.3V and a 100 ohm resistor to ground. This pin should be pulled up on PCI cards.
AGP_VREF_1_5V	**AGP Voltage Reference:** This input supplies the switching threshold for the AGP recievers for the 1.5V case. This is derived from a resistor network consisting of a 210 ohm 1% resistor to VDDQ and a 158 ohm 1% resistor to ground. There is a 0.1 uF capacitor in parallel with the resistor to ground.
AGP_VREF_3V	**AGP Voltage Reference:** This input supplies the switching threshold for the AGP recievers for the 1.5V case. This is derived from a resistor network consisting of a 210 ohm 1% resistor to VDDQ and a 158 ohm 1% resistor to ground. A second RC network cocnsists of a 210 ohm 1% resistor in series with a 560 pF cap to VDDQ and a 158 ohm 1% resistor in series with a 560 pF cap to ground. This is total of four resistors and two caps.
GND_AGP_G	**GND_AGP_Guard:** These four pairs of pins connect to ground traces that shield four signal pairs from cross talk. The four signal pairs are shown in the table. The reference designs may be studied to see how the traces should be routed.

Signal Pair	Guard Balls
AGP_SB_STB/_N	F3, G3
AGP_AD_STB0/_N	W4, Y1
AGP_AD_STB1/_N	K1, L3
VREF0/1	N5, P4

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3.4.3 Frame Buffer Pins

This group of pins provide the interface to the SGRAM/SDRAM frame buffer. The A and B ports connect to the SGRAM/SDRAMs providing MD[63:0] and MD[127:64], respectively. Doubling up on control lines reduces the loading and makes for a tighter layout. MCS0 and MCS1 connect to two banks of four devices each.

Name	Description
MA_A[11:0]	**Memory Address A Bus:** This multiplexed bus supplies the address to the SGRAM/SDRAMs providing MD[63:0]. The exact connections of the MA, MBA, and MCS lines to the SGRAM/SDRAM inputs depends on the memory configuration. See Chapter 5 for details.
MA_B[11:0]	**Memory Address B Bus:** This multiplexed bus supplies the address to the SGRAM/SDRAMs providing MD[127:64]. See the description of MA_A[11:0] for connection details.
MBA_A[1:0]	**Memory Bank Address A[1:0]:** These outputs supply the bank address to the SGRAM/SDRAMs providing MD[63:0].
MBA_B[1:0]	**Memory Bank Address B[1:0]:** These outputs supply the bank address to the SGRAM/SDRAMs providing MD[127:64].
MCAS_A	**Memory Column Address Strobe A:** This signal supplies CAS to the SGRAM/SDRAMs providing MD[63:0].
MCAS_B	**Memory Column Address Strobe B:** This signal supplies CAS to the SGRAM/SDRAMs providing MD[127:64].
MCLKA	**Memory Clock A:** This signal supplies the clock to the SGRAM/SDRAMs providing MD[63:0]. This signal requires one series termination resistor placed as close to the pin as possible for every two SGRAM/SDRAMs. The evaluation board uses 22 ohms. In addition, this pin drives MCLKA_IN through a 22 ohm resistor. This minimizes clock skew when the SGRAM/SDRAMs are supplying data to Napalm.
MCLKA_IN	**Memory Clock A Feedback:** This input supplies the clock which latches read data from the SGRAM/SDRAMs providing MD[63:0]. This input must be driven from MCLKA.
MCLKB	**Memory Clock B:** This signal supplies the clock to the SGRAM/SDRAMs providing MD[127:64]. This signal requires one series termination resistor placed as close to the pin as possible for every two SGRAM/SDRAMs. The evaluation board uses 22 ohms. In addition, this pin drives MCLKB_IN through a 22 ohm resistor. This minimizes clock skew when the SGRAM/SDRAMs are supplying data to Napalm.
MCLKB_IN	**Memory Clock B Feedback:** This input supplies the clock which latches read data from the SGRAM/SDRAMs providing MD[127:64]. This input must be driven from MCLKB.
MCS_1	**Memory Chip Select 1:** This output connects to an optional second bank of SGRAMs.
MCS_0	**Memory Chip Select 0:** This output connects to the first bank of four SGRAM/SDRAMs.

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3.4.3 Frame Buffer Pins *(cont)*

Pin	Description
MD[127:0]	**Memory Data Bus:** This is a 128-bit bidirectional data bus. MD[23:0] are also used as configuration input and have internal pullup resistors.
MDM[15:0]	**Frame Buffer Data Mask:** This bus provides the byte-write mask for the 128-bit data. MDM0 is associated with MD[7:0].
MDSF_A	**Frame Buffer Special Function A:** This pin supplies the special function control for the SGRAMs providing MD[63:0]. This is a no-connect in a SDRAM array.
MDSF_B	**Frame Buffer Special Function B:** This pin supplies the special function control for the SGRAMs providing MD[127:64]. This is no-connect in a SDRAM array.
MRAS_A	**Frame Buffer Row Address Strobe A:** This pin supplies RAS for the SGRAM/SDRAMs providing MD[63:0].
MRAS_B	**Frame Buffer Row Address Strobe B:** This pin supplies RAS for the SGRAM/SDRAMs providing MD[127:64].
MWE_A	**Frame Buffer Write Enable A:** This pin supplies write enable for the SGRAM/SDRAMs providing MD[63:0].
MWE_B	**Frame Buffer Write Enable B:** This pin supplies write enable for the SGRAM/SDRAMs providing MD[127:64].

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3.4.4 PLL

These are the power and ground pins for the phase-locked-loops, as well as the loop filter monitor pin for video PLL.

Bit	Description
AGP_PLL_VDD	**AGP_PLL Power:** This pin supplies power to the AGP PLL. This supply is decoupled from V2_5 (2.5V supply) with a bead and then four capacitors: 10 uF, 0.1 uF, 0.01 uF, and 1000 pF. The filters should be close to the pin.
PLL_AVDD[1:0]	**PLL Power:** These two pins supply power to the video PLL.This supply is decoupled from V2_5 (2.5V supply) with a bead and then four capacitors: 10 uF, 0.1 uF, 0.01 uF, and 1000 pF. The filters should be close to the pins.
AGP_PLL_VSS	**AGP_PLL Ground Reference:** This pin supplies ground reference to the AGP PLL. It must be connected directly to the ground plane.
PLL_AVSS[1:0]	**PLL Ground Reference:** These two pins supply ground reference to the video PLL. These pins must be connected directly to the ground plane.
VPLL_LF	**Video Loop Filter:** This pin can be used to monitor the video PLL loop filter. This pin is for testing purposes only and should be a no-connect for production applications.

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3.4.5 Monitor

These pins are the monitor interface.

Bit	Description
BLUE	**Pixel Blue Content:** This analog output supplies current corresponding to the blue content of the pixel being refreshed. This output should have a 75 ohm resistor returned to DAC_VSS placed as close to the pin as possible. The monitor should supply a 75 ohm parallel termination for a net impedance of 37.5 ohms. The evaluation board has surge suppression diodes to VCC and ground and a low-pass filter consisting of a bead and 22 pF capacitor close to the DB-15 connector.
DAC_AVDD/I	**DAC Power:** These two pins supply power to the DACs. They are adjacent on the package. This supply is decoupled from tjhe 2.5V supply with a bead and then four capacitors: 10 uF, 0.1 uF, 0.01 uF, and 1000 pF. The filters should be close to the pin.
DAC_AVSS/R	**DAC Ground Reference:** These two pins supply ground reference to the DACs. They must be connected directly to the ground plane.
DAC_RSET	**Video DAC RSET:** This pin is used to set the full scale DAC output current. A resistor must be connected between this pin and ground. On the evaluation board, this is 61.9 ohms, 1% tolerance.
GREEN	**Pixel Green Content:** This analog output supplies current corresponding to the green content of the pixel being refreshed. This output should have a 75 ohm resistor returned to DAC_VSS placed as close to the pin as possible. The monitor should supply a 75 ohm parallel termination for a net impedance of 37.5 ohms. The evaluation board has surge suppression diodes to VCC and ground and a low-pass filter consisting of a bead and 22 pF capacitor close to the DB-15 connector.
HSYNC	**Horizontal Sync:** This output supplies horizontal sync to the monitor. This output should have a series termination resistor placed as close to the pin as possible. The evaluation board uses 47 ohms. The evaluation board has a low-pass filter consisting of a bead and 100 pF capacitor close to the DB-15 connector. Multi-chip configurations require a pull-up on this pin.
RED	**Pixel Red Content:** This analog output supplies current corresponding to the red content of the pixel being refreshed. This output should have a 75 ohm resistor returned to DAC_VSS placed as close to the pin as possible. The monitor should supply a 75 ohm parallel termination for a net impedance of 37.5 ohms. The evaluation board has surge suppression diodes to VCC and ground and a low-pass filter consisting of a bead and 22 pF capacitor close to the DB-15 connector.
VSYNC	**Vertical Sync:** This output supplies vertical sync to the monitor. This output should have a series termination resistor placed as close to the pin as possible. The evaluation board uses 47 ohms. The evaluation board has a low-pass filter consisting of a bead and 100 pF capacitor close to the DB-15 connector.

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3.4.6 VMI Interface

Bit	Description
VMI_BLANK	**VMI VACTIVE:** This input indicates that valid pixel data is being transmitted on VMI_PD[7:0]. Although transitions in VACTIVE are allowed to support common HREF/ VREF systems, VACTIVE is intended to allow a hardware mechanism for cropping data.
VMI_CS_N	**VMI Chip Select:** This output supplies the chip select for the VMI Host interface.
VMI_DS_N	**VMI Data Strobe:** When the VMI interface is configured for mode A, this is an active-low data strobe. When the VMI interface is configured for mode B, this is an active-low read command. This pin also supplies ROM address bit 15. This pin also supplies AA/SLI data bit 25.
VMI_HA[3:0]	**VMI Host Port Address Bus:** This bus supplies the address for the VMI host interface port. This bus also supplies ROM address bits [11:8]. This bus also supplies AA/SLI data bits [11:8]. These are configuration inputs and have internal pullups.
VMI_HD[7:0]	**VMI Host Port Data Bus:** This bidirectional bus transfers data across the VMI host interface port. This bus is also used as the ROM data bus. This bus also supplies AA/SLI data bits [7:0]. These are configuration inputs and have internal pullups.
VMI_HSYNC	**VMI HREF:** This input is the horizontal reference from the VMI video port.
VMI_INT_N	**VMI INTREQ#:** This active input is the interrupt request from the VMI interface. This pin also supplies ROM address bit 13.
VMI_PCLK	**VMI PIXCLK:** This input is the pixel clock from the VMI video port.
VMI_PD[7:0]	**VMI YUV Video Data Bus:** This input bus is the pixel data from the VMI video port. This bus is also the low order eight bits of the ROM address bus.
VMI_RDY_N	**VMI DTACK#/READY:** When the VMI interface is configured for mode A, this is active DTACK# (extend transaction). When the VMI interface is configured for mode B, this is active high READY. This pin also supplies ROM address bit 12. This pin also supplies AA/ SLI data bit 26.
VMI_RESET_N	**VMI RESET:** This active low signal resets the VMI interface and/or devices to a known condition.
VMI_RW_N	**VMI R/W# WR#:** When the VMI interface is configured for mode A, this is the read/write indicator. When the VMI interface is configured for mode B, this is an active low write command. This pin also supplies ROM address bit 14. This pin also supplies AA/SLI data bit 24.
VMI_VSYNC	**VMI VREF:** This input is the vertical reference from the VMI video port.

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3.4.7 Digital RGB Interface Signals

This interface supplies digital RGB. It is typically used to drive an LCD encoder or TV encoder, but could be used for any other application requiring digital RGB.

Pin	Description
HOT_PLUG	**Hot Plug:** This input is connected to the panel hotplug pin. See Table 9.1 for programming notes. This has an internal pullup resistor.
PD	**Power Down:** This output is used to control power to the panel. See Table 9.1 for programming notes. This has an internal pullup resistor.
TV_BLANK	**TV_BLANK_N:** This active low output is the blank signal for the digital RGB out port. This has an internal pullup resistor.
TV_CLK_OUT	**TV Clock Out:** This output supplies the clock for the digital RGB out port.
TV_DATA[11:0]	**TV Data Out:** This 12-bit bus supplies digital RGB data for the digital RGB out port. These are configuration inputs and each has an internal pullup resistor.
TV_HSYNC	**TV_HSYNC:** This pin supplies horizontal sync for the digital RGB out port. This has an internal pullup resistor.
TV_INCLK	**TV Clock In:** This input is the clock for the digital RGB out port for slave mode.
TV_RESET	**TV_RESET_N:** This is a reset for the digital RGB out port. This has an internal pullup resistor.
TV_VSYNC	**TV_VSYNC:** This pin supplies vertical sync for the digital RGB out port. This has an internal pullup resistor.

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3.4.8 Miscellaneous Pins

The following pins didn't fall into any of the other groups.

Pin	Description
DEVICE_ID_LSB_N	**Device ID LSB:** This active-low input specifies the least significant bit of the Device ID (PCI00).
GPIO_[2:0]	**General Purpose I/O[2:0]:** These pins are dedicated for general purpose I/O. The table indicates how they are assigned on the evaluation board. See Chapter 9 for register assignments and whatever else we decide to put there.

Name	Pin	Signal Label	Purpose
GPIO_2	A20	ROM_ACTIVE	Controls buffer for VMI pixel data
GPIO_1	B20	(no name)	Controls select for DDC data, clock
GPIO_0	C20	GPIO_2	Unused input (pulled up)

PCI_CLK_OUT_SEL	**PCI Clock Out Select:** This input controls the multiplexer for the source of the PCI Clock Out. This pin is a no connect on the reference design just now.
ROM_CS_N	**ROM Chip Select:** This output connects to the CE pin of the ROM. This pin requires a pull-up resistor.
ROM_OE_N	**ROM Output Enable:** This output connects to the OE pin of the ROM. This pin is active with ROM_CS_N to read the ROM.
ROM_WE_N	**ROM Write Enable:** This output connects to the WE pin of the ROM. This pin is active with ROM_CS_N for ROM writes (for updating the BIOS).
SDA[1:0]	**Serial Data[1:0]:** These are the data pins of the two I^2C interfaces. See Chapter 10.
SDC[1:0]	**Serial Clock[1:0]:** These are the clock pins of the two I^2C interfaces. See Chapter 10.
TEN	**Test Enable:** This input is pulled up to VDDIO on the reference design. This pin requires a pulldown resistor.
XIN	**Crystal In:** This pin connects to one side of the reference oscillator crystal. No external resistor or capacitors are required. Napalm has internal capacitors. The oscillator is designed for a 18 pF, parallel resonant crystal. 3dfx Interactive, Inc. recommends a tolerance of 50 ppm.
XOUT	**Crystal Out:** This pin connects to one side of the reference oscillator crystal.

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3.4.9 SLI/AA InterfacePins

The following pins are to used for scanline interlacing/anti-aliasing. See the application note on SLI/AA for addition information.

Pin	Description
AA_CLK	**AA Clock:** This pin is used to clock data from the SLI/AA slave to the SLI/AA master. It is driven by the slave and recieved by the master. This has an internal pullup resistor.
AA_DATA[11:0]	**AA Data:** This bus is used to transmit data from the SLI/AA slave to the SLI/AA master. It is driven by the slave and recieved by the master. Each pin has an internal pullup resistor.
AA_VALID	**AA Valid:** This pin is used to indicate when SLI/AA data is available on the bus. It is driven by the slave and recieved by the master. This pin requires a pull-down. This pin has an internal pullup resistor.
DAC_CUR_SINK[2:0]	**DAC Current Sink:** These pins are used to specify the full scale DAC current level. Each is connected to the DAC_CUR_SRC input of one slave. If there are less than three slaves, the unused pins (on the master) are not connected. On slaves, these pins are not connected.
DAC_CUR_SRC	**DAC Current Source:** This pin is a no-connect on the master. On a slave, it connects to the one of the three DAC_CUR_SINK[2:0] pins on the master.
PCI_FIFO_ST	**PCI Bus FIFO Stall:** This is an output on SLI slaves and an input on the SLI master. The slaves can activate this signal to slow down the master when the slave FIFO is nearly full (the slave is bus snooping and cannot make TRDY active). This pin requires a pull-down resistor.
PCI_RDRDY	**PCI Bus Read Ready:** This is an output on SLI slaves and an input on the SLI master. The slaves can activate this signal to indicate that data is not available for reads of AA data (all the slaves have to have data ready before the read can complete) or SLI data. This pin requires a pull-down resistor.
SLI_SYNC_IN	**SLI Sync In:** This input connects to the SLI_SYNC_OUT pin of the previous chip in an SLI chain. This pin requires a pull-down resistor.
SLI_SYNCOUT	**SLI Sync Out:** This output connects to the SLI_SYNC_IN pin of the next chip in an SLI chain. This pin requires a pull-down resistor.
SYNC_CLK_FB	**SLI Sync Clock Feedback:** On the SLI master, this pin is grounded. On each SLI slave, this pin connects to the SYNC_CLK_OUT pin of the same chip through a trace that is the same length as the trace from the master's SYNC_CLK_OUT.
SYNC_CLK_IN	**SLI Sync Clock In:** On the SLI master, this pin is grounded. On each SLI slave, this pin is driven from the master's SYNC_CLK_OUT.
SYNC_CLK_OUT	**SLI Sync Clock Out:** On the SLI master, this pin is connected to the SYNC_CLK_IN pin of each SLI slave. This is a 12 mA driver and will very likely need a damping resistor very close to the pin. On each SLI slave, this pin is connected to the SYNC_CLK_FB of the same chip. This trace length should be the same as the trace length from the master's SYNC_CLK_OUT.
VSYNC_REF	**Vertical Sync Reference:** This pin supplies a vertical sync reference from the SLI master to the SLI slaves. This is a 12 mA driver.

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3.4.10 Power and Ground

These are the power and ground pins. The power and ground pins for the PLLs are described in Section 3.4.4. The power and ground pins for the DACs are described in Section 3.4.5.

Bit	Description
GND	**Digital Ground Reference:** These pins supply ground reference to the chip. Each pin must be connected directly to the ground plane. There are 27 ground pins, not counting the thermal pads or the guard trace pins.
Thermal(GND)[72:1]	**Thermal Ground Pads:** These pins supply ground reference to the chip. Each pin must be connected directly to the ground plane. These pins are 72 of the 100 in the square array of pins at the center of the package footprint. These pins provide a good deal of the thermal path which gets heat out of the package. They should have as large a via and as little thermal relief to the ground plane as permitted by the local design rules.
VGB	This pin is connected to a test point and a capacitor to ground on the reference design.
VDD_AGP_RBF	**Power:** This pin is connected to the VDDQ supply.
VDD_CORE2.5	**Digital Power:** These pins supply 2.5V power. Each pin must connect directly to the 2.5V power plane. These pins must be well bypassed to ground. Twenty-eight of these pins are in the thermal array at the center of the package footprint. There are four additional pins for a total of 32. This supply is generated with a regulator on the reference design.
VDD_IO3.3	**I/O Power:** These pins supply 3.3V power to the I/O buffers. Each pin must connect directly to the 3.3V power plane. These pins must be well bypassed to ground. There are 30 of these pins.
VDDQ3.3/1.5	**AGP Power:** These pins supply power to the AGP interface buffers. Each must be connected directly to the VDDQ power plane. These pins must be well bypassed. There are 11 of these pins.

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4 Configuration Options

Napalm reads the levels on a number of pins during power-on. This information is used to set some fundamental configuration. Each configuration input has a nominal 82kOhm pullup resistor in the pad. If the required configuration is ’1’, no external resistor is needed. If the required configured configuration is 0, an external resistor to ground must be supplied. The suggested value for a pulldown is 4.7 kOhm, although a stiffer pulldown can be used.
The strapping information can be determined by reading strapInfo0 and strapInfo1.

Table 4.1 Configuration Strapping: strapInfo0

strapInfo0 Bit	Pin		Description	Strapping
	Name	Ball		
31:24	Reserved			
23	TV_DATA11	C13	Unused	Unused
22	TV_DATA10	D13	Revision ID	0: Indicates A2 Silicon 1: Indicates A1 Silicon
21	TV_DATA9	E13	Unused	Unused
20	TV_DATA8	A14	Unused	Unused
19	TV_DATA7	B14	Unused	Unused
18	TV_DATA6	C14	Device_ID (PCI00)	0: Returns 6 or 7 1: Returns 8 or 9
17	TV_DATA5	D14	pci_strapinfo1_zero	0: Load strapinfo1 from MDs 1: Force strapinfo1 to 0
16	TV_DATA4	E14	mctl_num_banks dramInit0[30]	0: Two Internal banks 1: Four Internal banks
15	TV_DATA3	A15	Device Size MSB dramInit0[29]	(See VMI_DATA_6)
14	TV_DATA2	B15	Device Size dramInit0[28]	(see VMI_DATA_6)
13	TV_DATA1	C15	AGP 4X Enable	0: AGP 4X not enabled 1: AGP 4X enabled
12	TV_DATA0	D15	AGP 2X Enable	0: AGP 2X not enabled 1: AGP 2X enabled
11	VMI_HA3	B22	pll_bypass	0: Normal Operation 1: Bypass
10	VMI_HA2	C22	mctl_type_sdram dramInit1[30]	0: SGRAM 1: SDRAM

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Table 4.1 Configuration Strapping: strapInfo0 *(cont.)*

strapInfo0 Bit	Pin		Description	Strapping
	Name	Ball		
9	VMI_HA1	D22	mctl_short_power_on	0: Normal Operation 1: For simulation only
8	VMI_HA0	C23	re-map IDSEL	0: Use IDSEL 1: Use PCI_AD_16
7	VMI_HD7	B23	Disable PCI IRQ register	0: Enable register 1: Disable register
6	VMI_HD6	A23	Device Size LSB dramInit0[27] Used with TV_DATA_3 (msb) and TV_DATA_2	000: 8 Mbit[a] 001: 16 Mbit 010: 32 Mbit 011: 64 Mbit 100: 128 Mbit 101: 110: 111:
5	VMI_HD5	A24	Number Chipsets dramInit0[26]	0: One chipset 1: Two chipsets
4	VMI_HD4	B24	PCI Device Type	0: VGA 1: Other multimedia
3	VMI_HD3	C24	AGP Enable	0: AGP Disabled 1: AGP Enabled
2	VMI_HD2	C25	PCI 66 MHz	0: 33 MHz 1: 66 MHz
1	VMI_HD1	C26	BIOS Size	0: 32K 1: 64K
0	VMI_HD0	D23	PCI DEVSEL	0: Medium 1: Fast

a. When the design is using x16 memory devices, Napalm sees two devices as a single x32 device. In this case, the strapping has to be set to indicate the capacity of the logical x32 device; that is, twice the capacity of the x16 device. In Table 5.3, 16Mbit x16 devices are reported as 32 Mbit and in Table 5.6, 64Mbit x 16 devices are reported as 128M.

When TV_DATA5 is strapped high, strapInfo1 is forced to all zeroes. When TV_DATA5 is strapped low,

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strapInfo1 is loaded from memory data lines as indicated in the following table.

Table 4.2 Configuration Strapping: strapInfo1

strapInfo1 Bit	Pin		Description	Strapping
	Name	Ball		
31:24	Reserved			
23	MD23	H22	vga_valid_disable	default vgaInit0[3]
22	MD22	G24	vga_legacy_addr_disable	default vgaInit0[10:9]
21	MD21	G25	vga_disable	default vgaInit0[1]
20	MD20	J22	pci_multi_fctn_mmedia	
19	MD19	G26	pci_multi_fctn_device	default cfgInitEnable[28]
18	MD18	K22	pci_disable_fctn_zero	
17	MD17	H23	pci_fctn_number[2]	These three bits specify the function number for a PCI multi-function device.
16	MD16	H24	pci_fctn_number[1]	
15	MD15	L25	pci_fctn_number[0]	
14	MD14	L24	chip ID [4]	These six bits specify a unique chip ID for multi-chip configurations. See
13	MD13	L23	chip ID [3]	
12	MD12	M22	chip ID [2]	
11	MD11	M26	chip ID [1]	
10	MD10	M25	chip ID [0]	
9	MD9	M24	pci_iobase_alloc[1]	These two bits set the space claimed in iobase.
8	MD8	N22	pci_iobase_alloc[0]	
7	MD7	J23	pci_membase1_alloc[3]	These four bits set the memory claimed in membase1 (PCI14).
6	MD6	J24	pci_membase1_alloc[2]	
5	MD5	J25	pci_membase1_alloc[1]	
4	MD4	K26	pci_membase1_alloc[0]	
3	MD3	K25	pci_membase0_alloc[3]	These four bits set the memory claimed in membase0 (PCI10).
2	MD2	K23	pci_membase0_alloc[2]	
1	MD1	L22	pci_membase0_alloc[1]	
0	MD0	L26	pci_membase0_alloc[0]	

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5 Frame Buffer Connections

The following tables shows the specific connections for every memory configuration thought to be practical with Napalm. Each column describes the array and connections for a specific memory type. The column heading describes the memory type, including the number of internal banks in each memory chip. The first row in the table body specifies the specifies the number of chipsets in the array (basically whether chip select needs to be used). The term chipset is used here to avoid confusion with the number of internal banks in each device.
The tables also contain rows indicating the required programming for fields in dramInit0 and dramInit1.
The tables also contain rows indicated the required strapping. As always, strap low for a 0, strap high for a '1'. There are brief strapping notes in the right-most column of Table 5.1. In addition, see Chapter 4 for complete strapping information.

Table 5.1 4 MByte Memory Configurations

Item	8 Mbit SGRAM x32 (2 bank)	Strapping Note
Number Chipsets	1	-
Total Number Devices	4	-
Address	MA_A/B[8:0]	-
Bank Select	MBA_A/B[0]	-
Chip Select	(tie low)	-
dramInit0[30:26]	00000b	-
dramInit1[30]	0b	-
TV_DATA4	0	Internal Banks
TV_DATA[3:2] VMI_HD6	000	Memory Size
VMI_HA2	0	SGRAM/SDRAM
VMI_HD5	0	Number Chipsets

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Table 5.2 8 MByte Memory Configurations

Item	16 Mbit SGRAM x32 (2 bank)	8 Mbit SGRAM x32 (2 bank)
Number Chipsets	1	2
Total Number Devices	4	8
Address	MA_A/B[9:0]	MA_A/B[8:0]
Bank Select	MBA_A/B[0]	MBA_A/B[0]
Chip Select	(tie low)	MCS[1:0]
dramInit0[30:26]	00010b	00001b
dramInit1[30]	0b	0b
TV_DATA4	0	0
TV_DATA[3:2] VMI_HD6	001	000
VMI_HA2	0	0
VMI_HD5	0	1

Table 5.3 16 MByte Memory Configurations

Item	16 Mbit SDRAM x16 (2 bank)	32 Mbit SGRAM x32 (2 bank)	16 Mbit SGRAM x32 (2 bank)
Number Chipsets	1	1	2
Total Number Devices	8	4	8
Address	MA_A/B[10:0]	MA_A/B[10:0]	MA_A/B[9:0]
Bank Select	MBA_A/B[0]	MBA_A/B[0]	MBA_A/B[0]
Chip Select	(tie low)	(tie low)	MCS[1:0]
dramInit0[30:26]	00100b	00100b	00011b
dramInit1[30]	1b	0b	0b
TV_DATA4	0	0	0
TV_DATA[3:2] VMI_HD6	010	010	001
VMI_HA2	1	0	0
VMI_HD5	0	0	1

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Table 5.4 32 MByte Memory Configurations: SDRAM[a]

Item	64 Mbit SDRAM x32, 2 bank	64 Mbit SDRAM x32, 4 bank
Number Chipsets	1	1
Total Number Devices	4	4
Address	MA_A/B[11:0]	MA_A/B[10:0]
Bank Select	MBA_A/B[0]	MBA_A/B[1:0]
Chip Select	(tie low)	(tie low)
dramInit0[30:26]	00110b	10110b
dramInit1[30]	1b	1b
TV_DATA4	0	1
TV_DATA[3:2] VMI_HD6	011	011
VMI_HA2	1	1
VMI_HD5	0	0

a. A configuration with 16 pieces of 16 Mbit SDRAM is not shown because of loading considerations.

Table 5.5 32 MByte Memory Configurations: SGRAM

Item	64 Mbit SGRAM x32, 2 bank	64 Mbit SGRAM x32, 4 bank	32 Mbit SGRAM x32, (2 bank)
Number Chipsets	1	1	2
Total Number Devices	4	4	8
Address	MA_A/B[11:0]	MA_A/B[10:0]	MA_A/B[10:0]
Bank Select	MBA_A/B[0]	MBA_A/B[1:0]	MBA_A/B[0]
Chip Select	(tie low)	(tie low)	MCS[1:0]
dramInit0[30:26]	00110b	10110b	00101b
dramInit1[30]	0b	0b	0b
TV_DATA4	0	1	0
TV_DATA[3:2] VMI_HD6	011	011	010

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Table 5.5 32 MByte Memory Configurations: SGRAM

Item	64 Mbit SGRAM x32, 2 bank	64 Mbit SGRAM x32, 4 bank	32 Mbit SGRAM x32, (2 bank)
VMI_HA2	0	0	0
VMI_HD5	0	0	1

Table 5.6 64 MByte Memory Configurations: SDRAM, Part 1

Item	64 Mbit SDRAM x16, 2 bank	64 Mbit SDRAM x16, 4 bank	128 Mbit SDRAM x32, 2 bank
Number Chipsets	1	1	1
Total Number Devices	8	8	4
Address	MBA_A/B[1], MA_A/B[11:0]	MA_A/B[11:0]	MBA_A/B[1], MA_A/B[11:0]
Bank Select	MBA_A/B[0]	MBA_A/B[1:0]	MBA_A/B[0]
Chip Select	(tie low)	(tie low)	(tie low)
dramInit0[30:26]	0100b	11000b	01000b
dramInit1[30]	1b	1b	1b
TV_DATA4	0	1	0
TV_DATA[3:2] VMI_HD6	100	100	100
VMI_HA2	1	1	1
VMI_HD5	0	0	0

Table 5.7 64 MByte Memory Configurations: SDRAM, Part 2

Item	128 Mbit SDRAM x32, 4 bank	64 Mbit SDRAM x32, 2 bank	64 Mbit SDRAM x32, 4 bank
Number Chipsets	1	2	2
Total Number Devices	4	8	8
Address	MA_A/B[11:0]	MA_A/B[11:0]	MA_A/B[10:0]
Bank Select	MBA_A/B[1:0]	MBA_A/B[0]	MBA_A/B[1:0]
Chip Select	(tie low)	MCS[1:0]	MCS[1:0]

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Table 5.7 64 MByte Memory Configurations: SDRAM, Part 2 *(cont.)*

Item	128 Mbit SDRAM x32, 4 bank	64 Mbit SDRAM x32, 2 bank	64 Mbit SDRAM x32, 4 bank
dramInit0[30:26]	11000b	00111b	10111b
dramInit1[30]	1b	1b	1b
TV_DATA4	1	0	1
TV_DATA[3:2] VMI_HD6	100	011	011
VMI_HA2	1	1	1
VMI_HD5	0	1	1

Table 5.8 64 MByte Memory Configurations: SGRAM

Item	64 Mbit SGRAM x32, 2 bank	64 Mbit SGRAM x32, 4 bank
Number Chipsets	2	2
Total Number Devices	8	8
Address	MA_A/B[11:0]	MA_A/B[10:0]
Bank Select	MBA_A/B[0]	MBA_A/B[1:0]
Chip Select	MCS[1:0]	MCS[1:0]
dramInit0[30:26]	00111b	10111b
dramInit1[30]	0b	0b
TV_DATA4	0	1
TV_DATA[3:2] VMI_HD6	011	011
VMI_HA2	0	0
VMI_HD5	1	1

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6 Digital RGB Data Formats

Digital RGB data is clocked on both edges of the clock. Which bit is clocked on each edge is controlled by vidInFormat[8] and vidInFormat[22]. See the following table.

Table 6.1 Digital RGB Data Formats

Pin	Scramble Enabled (vidInFormat[22] = 0)				Scramble Disabled (vinInFormat[22] = '1')			
	vidInFormat[8] = 0 Chrontel Encoder		vidInFormat[8] = 1 Brooktree Encoder		vidInFormat[8] = 0		vidInFormat[8] = 1	
	Rising	Falling	Rising	Falling	Rising	Falling	Rising	Falling
TV_DATA[11]	G4	R7	R7	G4	G3	R7	R7	G3
TV_DATA[10]	G3	R6	R6	G3	G2	R6	R6	G2
TV_DATA[9]	G2	R5	R5	G2	G1	R5	R5	G1
TV_DATA[8]	B7	R4	R4	B7	G0	R4	R4	G0
TV_DATA[7]	B6	R3	R3	B6	B7	R3	R3	B7
TV_DATA[6]	B5	G7	G7	B5	B6	R2	R2	B6
TV_DATA[5]	B4	G6	G6	B4	B5	R1	R1	B5
TV_DATA[4]	B3	G5	G5	B3	B4	R0	R0	B4
TV_DATA[3]	G0	R2	R2	G0	B3	G7	G7	B3
TV_DATA[2]	B2	R1	R1	B2	B2	G6	G6	B2
TV_DATA[1]	B1	R0	R0	B1	B1	G5	G5	B1
TV_DATA[0]	B0	G1	G1	B0	B0	G4	G4	B0

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7 Shared Pins

A number of pins are shared between the VMI, ROM and SLI/AA interfaces. Table 7.1 shows these pins.

Table 7.1 VMI/ROM Pins

Pin		ROM Access		VMI Access		SLI/AA	
Name	Ball	Function	I/O	Function	I/O	Function	I/O
VMI_PD0	D11	A0	out	Y0/Cr0/Cb0[a]	in	-	
VMI_PD1	C11	A1	out	Y1/Cr1/Cb1[a]	in	-	
VMI_PD2	B11	A2	out	Y2/Cr2/Cb2[a]	in	-	
VMI_PD3	A11	A3	out	Y3/Cr3/Cb3[a]	in	-	
VMI_PD4	D10	A4	out	Y4/Cr4/Cb4[a]	in	-	
VMI_PD5	C10	A5	out	Y5/Cr5/Cb5[a]	in	-	
VMI_PD6	B10	A6	out	Y6/Cr6/Cb6[a]	in	-	
VMI_PD7	A10	A7	out	Y7/Cr7/Cb7[a]	in	-	
VMI_HA0	C23	A8	out	vaddr0	out	SLI/AA Data 8	I O
VMI_HA1	D22	A9	out	vaddr1	out	SLI/AA Data 9	I O
VMI_HA2	C22	A10	out	vaddr2	out	SLI/AA Data 10	I O
VMI_HA3	B22	A11	out	vaddr3	out	SLI/AA Data 11	I O
VMI_RW_N	E22	A14	out	vmi_rw	out	SLI/AA Data 24	I O
VMI_DS_N	E20	A15	out	vmi_ds	out	SLI/AA Data 25	I O
VMI_RDY_N	D21	A12	out	vmi_rdy[a]	in	SLI/AA Data 26	I O
VMI_HD0	D23	D0	i/o	vmi_hd_0	i/o	SLI/AA Data 0	I O
VMI_HD1	C26	D1	i/o	vmi_hd_1	i/o	SLI/AA Data 1	I O
VMI_HD2	C25	D2	i/o	vmi_hd_2	i/o	SLI/AA Data 2	I O
VMI_HD3	C24	D3	i/o	vmi_hd_3	i/o	SLI/AA Data 3	I O
VMI_HD4	B24	D4	i/o	vmi_hd_4	i/o	SLI/AA Data 4	I O
VMI_HD5	A24	D5	i/o	vmi_hd_5	i/o	SLI/AA Data 5	I O
VMI_HD6	A23	D6	i/o	vmi_hd_6	i/o	SLI/AA Data 6	I O
VMI_HD7	B23	D7	i/o	vmi_hd_7	i/o	SLI/AA Data 7	I O
VMI_INT_N	C21	A13	out	vmi_int_n[a]	in	-	

a. These pins must be isolated from the VMI with a buffer controlled with GPIO[0].

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8 VMI Host Interface

Transactions on the VMI host interface are generated by programming each control bit explicitly. This is unlike some graphics chips incorporating state machines that translate writes or reads to an address range into VMI host interface writes or reads.

8.1 Manual Transactions: Bit Assignments

The bits that control the VMI host are in vidSerialParallelPort. The VideoIn Interface Configuration field (vidInFormat[15:14]) must be programmed to 01b. Table 8.1 shows the bit assignments.

Table 8.1 VMI Host Interface Explicit Control Bits: vidSerialParallelPort

Field	Description	Note
17:14	VMI Address	This field is driven onto VMI_HA[3:0]
13:6	VMI Data	Bidirectional data on VMI_HD[7:0]
5	VMI Data Output Enable	Active low enable for VMI_HD[7:0]
4	VMI_RDY_N	DTACK_N for mode A, READY for mode B
3	VMI_RW_N	R/W# for mode A, WR# for mode B
2	VMI_DS_N	DS# for mode A, RD# for mode B
1	VMI_CS_N	Active low chip select
0	VMI Host Port Enable	Active low enables for control pins

8.2 Automatic Transactions

On Napalm, these transactions can be generated by a state machine. When the host writes to the linear frame buffer using format 9, each 32-bit write will generate a single 8-bit write on the VMI port if miscInit0[31] is '1'. The host port data, address, mode, and sense of the read/write and chip signals are all imbedded in the 32-bit word.

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9 General Purpose I/O

Napalm has three pins dedicated to general purpose I/O (these should not really be called GPIO since they have dedicated directions), and two addition pins that are intended for panel control and really are GPIOs. These are summarized in Table 9.1.

Table 9.1 General Purpose I/O Pins

Name	Ball	Direction	Register Bit
GPIO0	C20	Output	(Address Decode)
GPIO1	B20	Output	vidSerialParallelPort[29]
GPIO2	A20	Input	vidSerialParallelPort[30]
HOT_PLUG	E15	I/O	cfgSliAAMisc[11:9]
PD	E9	I/O	miscInit[31:29]

10 Serial I/O

There are two serial I/O ports on Napalm. Each port comprises two open-drain outputs that can be controlled and sensed with register bits. These ports are similar to I2C.
By convention, Serial Port 0 is used for the analog monitor and the flag panel. Since these two devices often argue with each other, an analog multiplexor controlled by GPIO1 connects one or the other to port. See the board schematics.
Serial Port 1 is used for VMI (it is wired to the Feature Connector), and encoders. This includes the TV encoder and the flat panel encoder (as opposed to the flag panel itself).
The following table shows the pin and register bit assignments for the two serial ports.

Table 10.1 Serial I/O Assignments

Signal Name	Function	Pin	vidSerialParallelPort Bits		
			Enable	In	Out
SDA1	Data	E17	23	27	25
SDC1	Clock	E18	23	26	24
SDA0	Data	C19	18	22	20
SDC0	Clock	D19	18	21	19

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11 cfgVideoCtrl Register Notes

Napalm incorporates three registers that control scanline interleave and anti-aliasing. Bits in these registers can control the output enables on a number of I/Os, as indicated in the following notes.

11.1 dac_vsync (VSYNC) Controls

If dac_vsync_float (cfgVideoCtrl0[24]) is '1', then dac_vsync (VSYNC) is tri-stated regardless of any other controls.
If dac_vsync_float is 0 and enhanced_video_en (cfgVideoCtrl0[0]) is '1', then dac_vsync is controlled by enhanced_video_slv (cfgVideoCtrl0[1]). In particular, if enhanced_video_slv is 0, dac_vsync is driven; if enhanced_video_slv is '1', dac_vsync is tri-stated.
If both dac_vsync_float is 0 and enhanced_video_en is 0, then dac_vsync is controlled as on previous products.

Table 11.1 dac_vsync

dac_vsync_float	enhanced_video_enable	enhanced_ video_slv	output
'1'	d/c	d/c	disabled
0	'1'	0	enabled
0	'1'	'1'	tri-stated
0	0	d/c	previous

11.2 dac_hsync (HSYNC) Controls

If dac_hsync_float (cfgVideoCtrl0[25]) is '1', then dac_hsync (HSYNC) is tri-stated regardless of any other controls.
If dac_hsync_float is 0 and enhanced_video_en (cfgVideoCtrl0[0]) is '1', then dac_hsync is controlled according to the following equation:
(((scanline[7:0] & sli_rendermask_crt) == sli_compareMask_crt) ^ sli_crt_compare_invert)
If the equation is true, dac_hsync is driven; if the equation is false, dac_hsync is tri-stated. The chip drives HSYNC for the scanlines it is responsible for.
If both dac_hsync_float is 0 and enhanced_video_en is 0, then dac_hsync is controlled as on previous products.

Table 11.2 dac_hsync

dac_hsync_float	enhanced_video_enable	(equation)	output
'1'	d/c	d/c	disabled
0	'1'	true	enabled
0	'1'	false	tri-stated
0	0	d/c	previous

11.3 TV Control Signals Controls

The TV control signals are tv_clk_out, tv_hsync, tv_vsync, and tv_blank. If video_tv_output_en (cfgVideoCtrl0[2]) is '1', then these outputs are enabled regardless of any other setting.

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If video_tv_output_en is 0 and enhanced_video_en is ‘1’, then these outputs are controlled by enhanced_video_slv. In particular, these outputs are driven if enhanced_video_slv is 0; if enhanced_video_slv is ‘1’, then these outputs are tri-stated.
If both video_tv_output_en is 0 and enhanced_video_en is 0, then these outputs are controlled as on previous products.

Table 11.3 TV Controls

video_tv_ output_en	enhanced_video_enable	enhanced_ video_slv	outputs
‘1’	d/c	d/c	disabled
0	‘1’	0	enabled
0	‘1’	‘1’	tri-stated
0	0	d/c	previous

11.4 tv_data[11:0] Controls

If video_tv_output_en (cfgVideoCtrl0[2]) is ‘1’, then these outputs are driven, regardless of all other controls.
If video_tv_output_en is 0 and enhanced_video_en is ‘1’, then the following equation is used to determine whether these outputs are driven.
(((scanline[7:0] & sli_rendermask_crt) == sli_compareMask_crt) ^ sli_crt_compare_invert).

Table 11.4 tv_data[11:0]

video_tv_ output_en	enhanced_video_enable	(equation)	output
‘1’	d/c	d/c	disabled
0	‘1’	true	enabled
0	‘1’	false	tri-stated
0	0	d/c	previous

11.5 Digital Anti-aliasing Signals

The digital anti-aliasing signals are aa_vid, aa_clk, aa_data[11:0], vmi_addr[3:0], vmi_data[7:0], vmi_rw, vmi_ds_n, and vmi_rdy.
If enhanced_video_en (cfgVideoCtrl0[0]) is ‘1’ and enhanced_video_slv (cfgVideoCtrl0[1]) is ‘1’, then the following equation is used to determine whether these signals are driven:

(((scanline[7:0] & sli_rendermask_aafifo) == sli_compareMask_aafifo) ^ sli_aafifo_compare_invert)
If the equation is true, the outputs are enabled; if the equation is false, then outputs are disabled.
If enhanced_video_en is false, then the vmi outputs are controlled with the normal VMI control signals.
Valid data is only transferred on the digital AA signals when enhanced_video_en is ‘1’ and the above equation is true. Otherwise aa_vld is tristated and no valid data is transferred across the digital AA bus.

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12 DC Specifications

12.1 Absolute Maximum Ratings

Stresses above those listed in Table 12.1 may cause permanent damage to system components. These are stress ratings only and functional operation at these or any conditions outside those indicated in Table 12.3 through Table 12.8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 12.1 Absolute Maximum Ratings

Symbol	Description	Rating
T_{STG}	Storage Temperature	-40 to 125 degrees C
V_{IN}	Input Voltage on any pin	-0.5 V to V_{CC} + 0.5 V
VDDIO3.3	Power Supply Voltage	3.60 V
VDD_CORE2.5	Power Supply Voltage	tbd
VDDQ3.3/1.5	Power Supply Voltage	tbd
I_{OUT}	DC output current (per pin)	tbd

12.2 DC Characteristics and Recommended Operating Conditions

Napalm uses a number of power supplies and supports a number of signaling levels. There is a table for each supply level, as well as tables that specify conditions common to all. Table 12.2 is an index.

Table 12.2 DC Tables Summary

Title	Link	Note
DC Characteristics: VDDIO3.3	Table 12.3	
DC Characteristics: VDD_CORE2.5	Table 12.4	(no buffer specs needed?)
DC Characteristics: VDDQ3.3	Table 12.5	
DC: Characteristics: VDDQ1.5	Table 12.6	
Thermal Characteristics	Table 12.7	
Environmental Operating Conditions	Table 12.8	
Pin Capacitance	Table 12.9	
DAC Characteristics	Table 12.10	

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Table 12.3 DC Characteristics: VDDIO3.3

Symbol	Description	Test Conditions		
			Min	Max
V_{CC}	Power Supply Voltage	-	3.15	3.45
$I_{DDIO3.3}$	Supply Current	V_{DD} = 3.15	-	tbd
		V_{DD} = 3.3V	-	tbd
		V_{DD} = 3.45	-	tbd
V_{IH}	Input High Voltage	V_{DD} =	tbd	-
V_{IL}	Input Low Voltage	V_{DD} =	-	tbd
I_{IH}	Input High Current	$V_I = V_{DD}$	-	10 uA
I_{IL}	Input Low Current	V_I =	-10 uA	-
V_{OH}	Output High Voltage	I_{OH} =	0.9 * V_{DD}	-
V_{OL}	Output Low Voltage	I_{OL} =	-	0.4 V
I_{OL}	Output Leakage Current	$0V \le V_{IN} \le V_{DD}$	-10 uA	10 uA

Table 12.4 DC Characteristics: VDDC2.5

Symbol	Description	Test Conditions		
			Min	Max
V_{CC}	Power Supply Voltage	-	tbd	tbd
$I_{DDIO3.3}$	Supply Current	V_{DD} =	-	tbd
		V_{DD} = 2.5V	-	tbd
		V_{DD} =	-	tbd
V_{IH}	Input High Voltage	V_{DD} =	tbd	-
V_{IL}	Input Low Voltage	V_{DD} =	-	tbd
I_{IH}	Input High Current	$V_I = V_{DD}$	-	10 uA
I_{IL}	Input Low Current	V_I =	-10 uA	-

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Table 12.4 DC Characteristics: VDDC2.5 *(cont.)*

Symbol	Description	Test Conditions		
			Min	Max
V_{OH}	Output High Voltage	I_{OH} =	0.9 * V_{CC}	-
V_{OL}	Output Low Voltage	I_{OL} =	-	0.4 V
I_{OL}	Output Leakage Current	$0V \le V_{IN} \le V_{DD}$	-10 uA	10 uA

Table 12.5 DC Characteristics: VDDQ 3.3V Signaling

Symbol	Description	Test Conditions	Min	Max
V_{DD}	Power Supply Voltage	-	3.15	3.45
V_{ref}	Input Reference Voltage	-	0.39 Vddq	0.41 Vddq
$I_{DDIO3.3}$	Supply Current	V_{DD} = 3.15	-	tbd
		V_{DD} = 3.3	-	tbd
		V_{DD} = 3.45	-	tbd
V_{IH}	Input High Voltage	V_{DD} =	0.5 Vddq	Vddq+0.5V
V_{IL}	Input Low Voltage	V_{DD} =	-0.5V	0.3 Vddq
I_{IL}	Input Leakage Current	$0 < V_{In} <$ Vddq	-	+-10 uA
V_{OH}	Output High Voltage	I_{OH} = -500 uA	.9 Vddq	-
V_{OL}	Output Low Voltage	I_{OL} = 1500 uA	.1 Vddq	
C_{in}	Input Pin Capacitance			8 pF
C_{clk}	CLK Pin Capacitance		5 pF	12 pF

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Table 12.6 DC Characteristics: VDDQ 1.5V Signaling

Symbol	Description	Test Conditions	Min	Max
V_{DD}	Power Supply Voltage	-	1.425	1.575
V_{ref}	Input Reference Voltage	-	0.48 Vddq	0.52 Vddq
$I_{DDIO1.5}$	Supply Current	V_{DD} = 1.425	-	tbd
		V_{DD} = 1.5	-	tbd
		V_{DD} = 1.575	-	tbd
V_{IH}	Input High Voltage	V_{DD} =	0.6 Vddq	Vddq+0.5V
V_{IL}	Input Low Voltage	V_{DD} =	-0.5V	0.4 Vddq
I_{IL}	Input Leakage Current	0 < V_{In} < Vddq	-	+-10 uA
V_{OH}	Output High Voltage	I_{OH} = -200 uA	.85 Vddq	-
V_{OL}	Output Low Voltage	I_{OL} = 1000 uA	.15 Vddq	
C_{in}	Input Pin Capacitance			8 pF
C_{clk}	CLK Pin Capacitance		5 pF	12 pF

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Table 12.7 Thermal Characteristics

Parameter	Conditions	Degrees C / watt
θJC	-	tbd
θJA	Free Air[a]	tbd

a. This is for the package alone. It does not take into account heat conducted into the printed circuit board. 3dfx Interactive, Inc. plans an application note that covers thermal considerations.

Table 12.8 Environmental Operationing Condition

Symbol	Description	Test Conditions		
			Min	Max
T_C	Case Temperature	Operating	0 ° C	95° C

Table 12.9 Pin Capacitance

Symbol	Description	Pins	Min	Nominal	Max
C_{IN}	Input Capacitance	All except XIN, XOUT	-	-	10 pF
C_{INX}	Input Capacitance	XIN, XOUT	tbd	tbd	tbd
C_{OUT}	Output Capacitance	-	-	-	10 pF

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12.3 DAC Characteristics

Table 12.10 DAC Characteristics

Symbol	Parameter	MAX	Units	Conditions	Notes
R	Resolution	8	bits		
IO	Output current	tbd	mA	VO < 1V	
TR	Analog output rise/full time	tbd	ns	10% to 90% full scale	a b
TS	Analog output settling time	tbd	ns	50% FS change to remaining within 2%	a b
TSK	Analog output skew	tbd	ns		a b c d
FDT	DAC-to-DAC correlation	tbd	%		a b c d
GI	Glitch impulse	tbd	pV/sec		b
IL	Integral linearity	tbd	LSB		
DL	Differential linearity	tbd	LSB		b

a. Load is 50 ohms and 30 pF per analog output.
b. RSET = 147 ohms
c. Outputs loaded identically.
d. About the mid-point of the distribution of the three DAC's measured at full-scale output.

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13 AC Specifications

In general, these waveforms and tables very closely follow those of the respective specifications.

13.1 Clock Input Timing

Figure 13.1 shows the level definitions of incoming clocks.

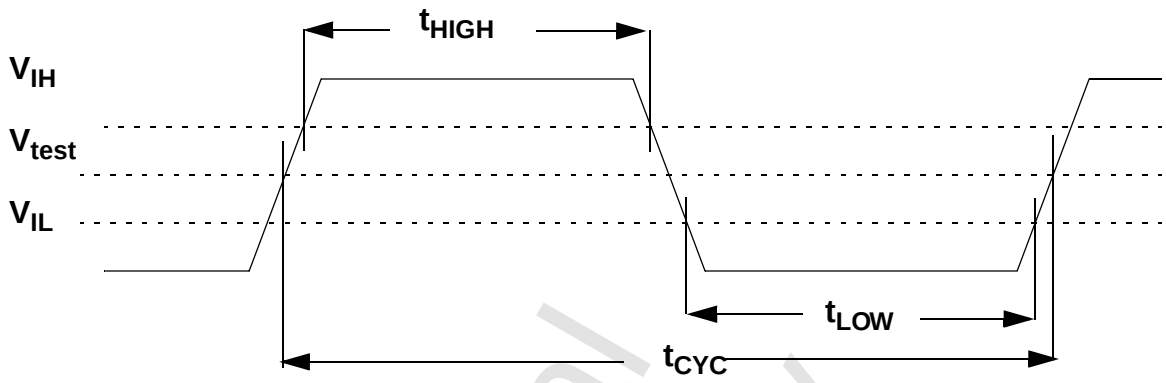

Figure 13.1 Clock Input Measurement Conditions

Table 13.1 PCI_CLK Timing

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	15	30	ns
t_{HIGH}	CLK high time	6	-	ns
t_{LOW}	CLK low time	6	-	ns
-	CLK slew rate	1.0	4	V/ns

Table 13.2 VMI_PCLK (VMI Video Capture Mode) Timing

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	35	-	ns

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Table 13.3 TV_INCLK (TV out Mode) Timing

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	tbd	tbd	ns
t_{HIGH}	CLK high time	tbd	-	ns
t_{LOW}	CLK low time	tbd	-	ns

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13.2 Clock Out Timing

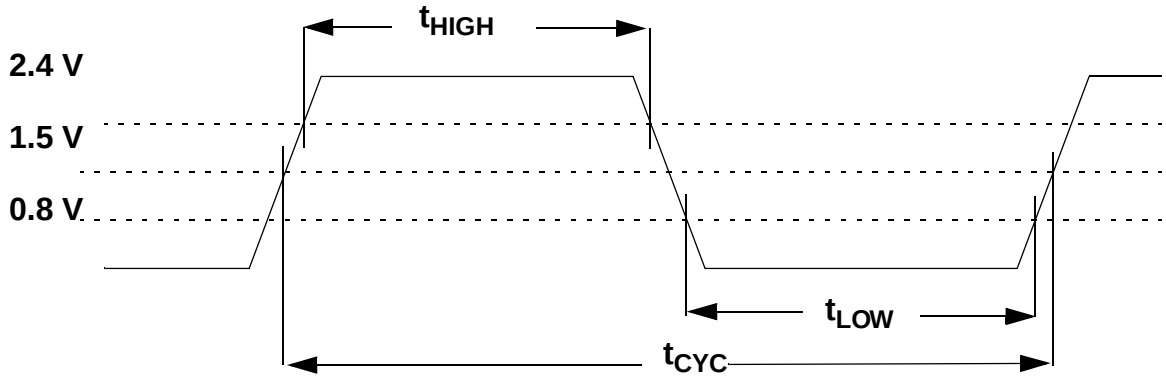

Figure 13.2 Clock Out Waveform

Table 13.4 MCLKA/MCLKB Timing

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	8.6	-	ns
t_{HIGH}	CLK high time	4	-	ns
t_{LOW}	CLK low time	4	-	ns

Table 13.5 TV_CLK_OUT Timing: TV Out Mode

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	10	-	ns
t_{HIGH}	CLK high time	5	-	ns
t_{LOW}	CLK low time	5	-	ns

Table 13.6 TV_CLK_OUT Timing: LCD Out Mode

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	10	-	ns
t_{HIGH}	CLK high time	5	-	ns
t_{LOW}	CLK low time	5	-	ns

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13.3 Reset Timing

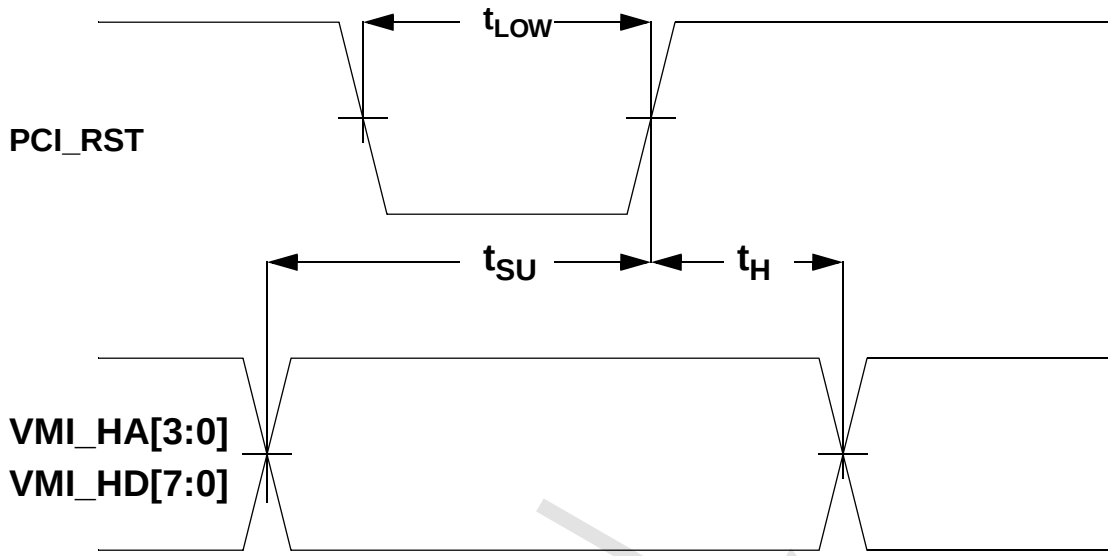

Figure 13.3 Reset Waveforms

Table 13.7 Reset Timing

Symbol	Parameter	Min	Max	Units
t_{LOW}	PCI_RST pulse width	tbd	-	PCI_CLK
t_{SU}	Strapping Resistor Setup	20	-	ns
t_H	Strapping Resistor Hold	20	-	ns

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13.4 PCI/AGP Transmitter (output) Timing: 1X

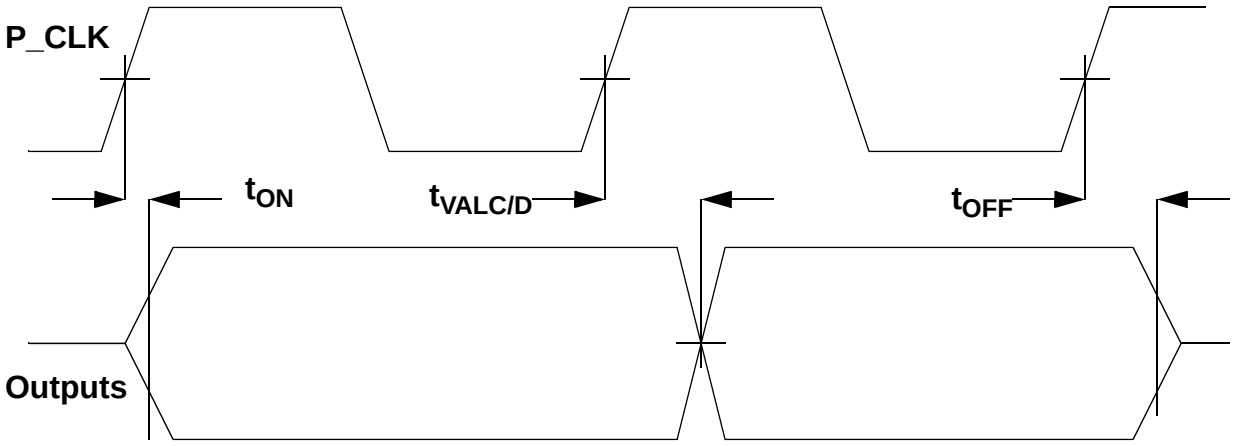

Figure 13.4 PCI/AGP Transmitter Waveforms: 1X

Table 13.8 PCI/AGP Transmitter (output) Timing: AGP 1X

Symbol	Parameter	Min	Max	Units
t_{VALC}	CLK to control signal valid delay	1.0	5.5	ns
t_{VALD}	CLK to data valid delay	1.0	6.0	ns
t_{ON}	Float to active delay	1.0	6	ns
t_{OFF}	Active to float delay	1	14	ns
	Output slew rate	1.5	4	V/ns

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13.5 PCI/AGP Receiver (input) Timing: 1X

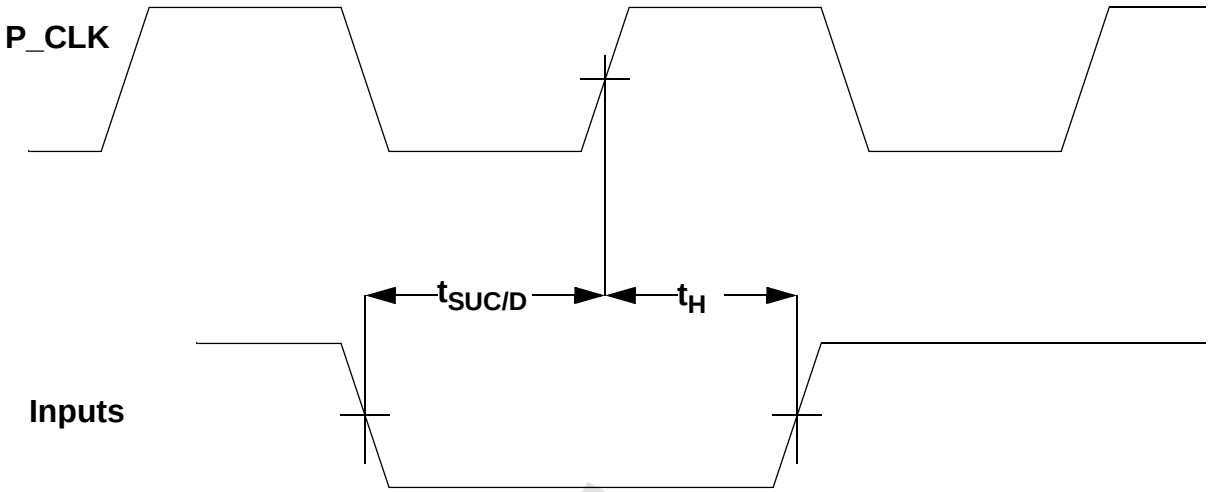

Figure 13.5 PCI/AGP Receiver Waveforms: 1X

Table 13.9 PCI/AGP Receiver (input) Timing: AGP 1X

Symbol	Parameter	Min	Max	Units
t_{SUC}	Control signals setup time to CLK	6.0	-	ns
t_{SUD}	Data setup time to CLK	5.5	-	ns
t_H	Control signals hold time to CLK	0.0	-	ns

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13.6 PCI/AGP Receiver (input) Timing: 2X

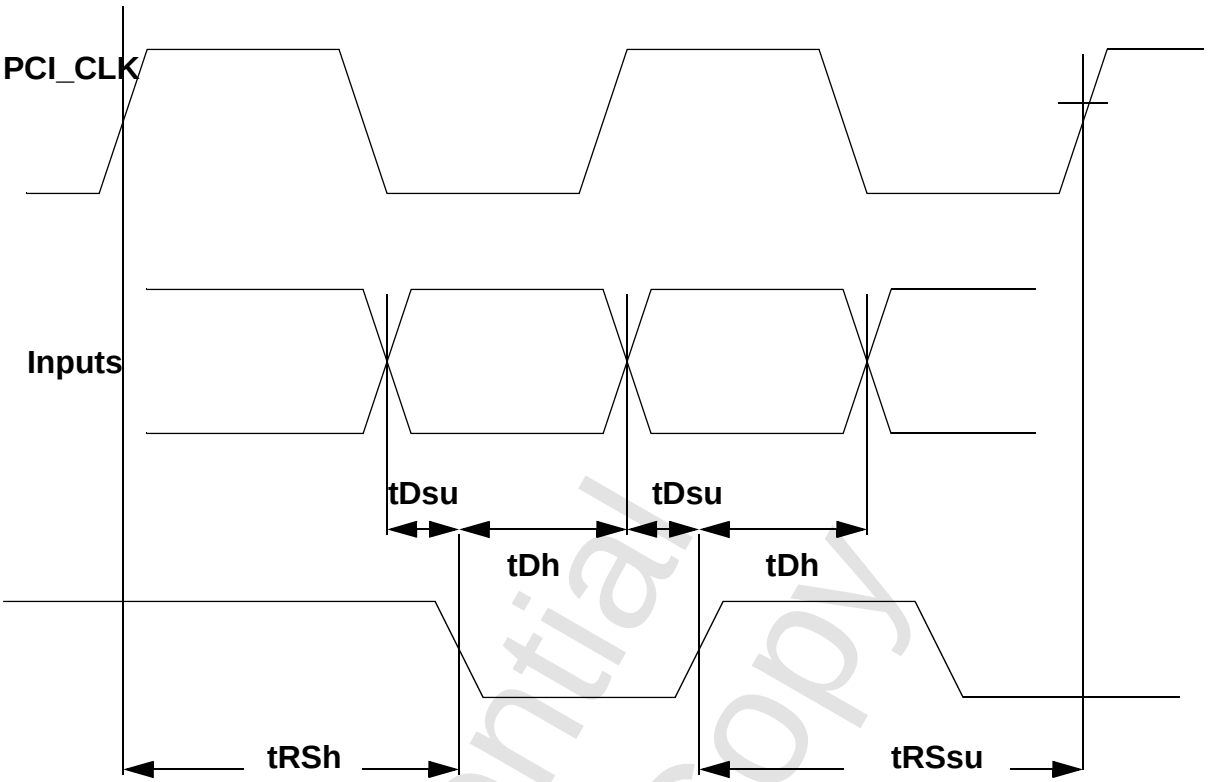

Figure 13.6 PCI/AGP Receiver Waveforms: 2X

Table 13.10 PCI/AGP Receiver (input) Timing: AGP 2X

Symbol	Parameter	Min	Max	Units
tR_{Ssu}	Receive strobe setup time to CLK	6	-	ns
t_{RSh}	Receive strobe setup hold time from CLK	1	-	ns
t_{Dsu}	Data to strobe setup time	1	-	ns
t_{Dh}	Strobe to data hold time	1	-	ns

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13.7 PCI/AGP Receiver (input) Timing: 4X

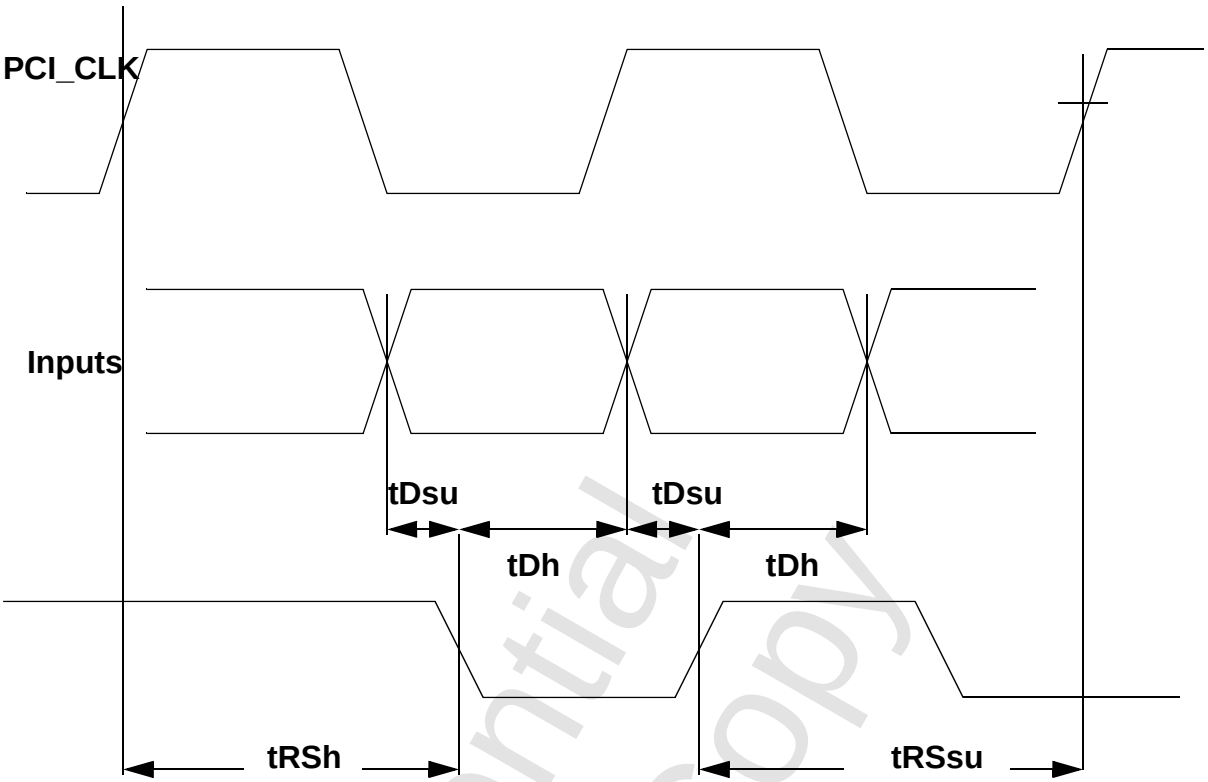

Figure 13.7 PCI/AGP Receiver Waveforms: 4X

Table 13.11 PCI/AGP Receiver (input) Timing: AGP 4X

Symbol	Parameter	Min	Max	Units
tR_{Ssu}	Receive strobe setup time to CLK	6	-	ns
t_{RSh}	Receive strobe setup hold time from CLK	0.5	-	ns
t_{Dsu}	Data to strobe setup time	0.40	-	ns
t_{Dh}	Strobe to data hold time	0.70	-	ns

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13.8 Frame Buffer Output Timing

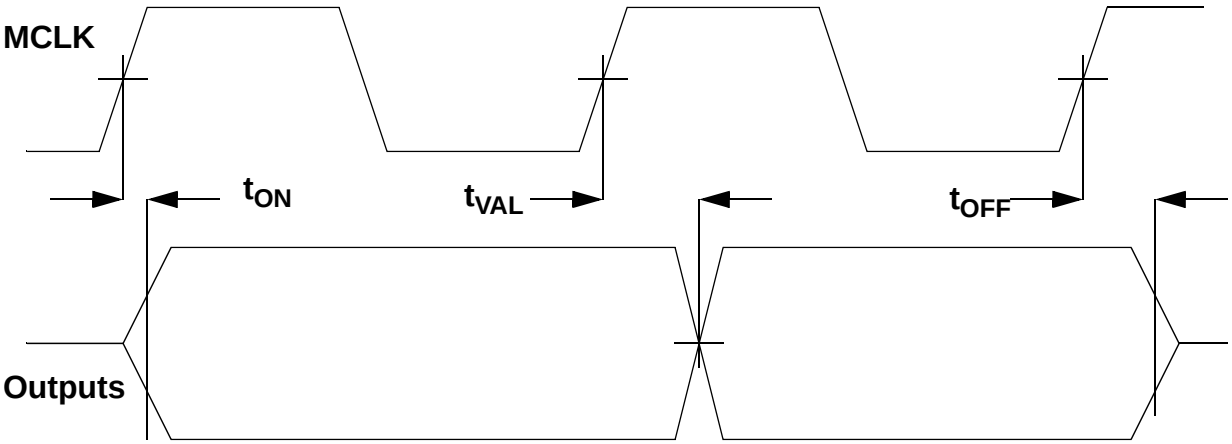

Figure 13.8 Frame Buffer Output Waveforms

Table 13.12 Frame Buffer Output Timing[a]

Symbol	Parameter	Min	Max	Units
t_{ON}	Float to active delay (MD[127:0])	tbd	tbd	ns
t_{VAL}	CLK to control signal valid delay	-	tbd	ns
t_{VAL}	CLK to address valid delay	-	tbd	ns
t_{VAL}	CLK to MD valid delay	-	tbd	ns
t_{OFF}	Active to float delay (MD[127:0])	tbd	tbd	ns

a. 115 MHz MCLK, standard BIOS programming.

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13.9 Frame Buffer Input Timing

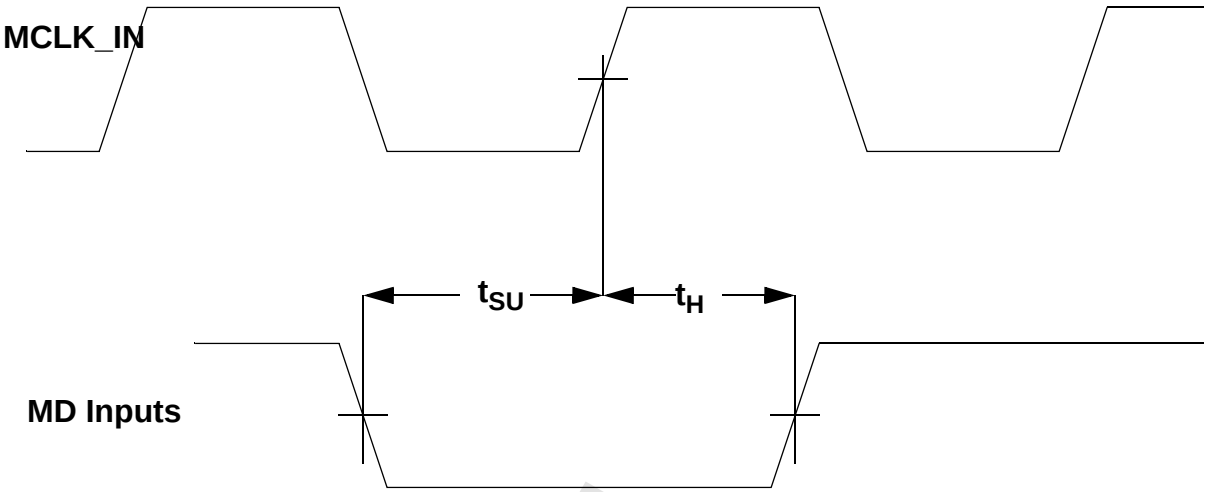

Figure 13.9 Frame Buffer Input Waveforms

Table 13.13 Frame Buffer Input Timing

Symbol	Parameter	Min	Max	Units
t_{SU}	MD setup time to MCLK_IN	tbd	-	ns
t_H	MD hold time to MCLK_IN	tbd	-	ns

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13.10 SLI/AA Output Timing

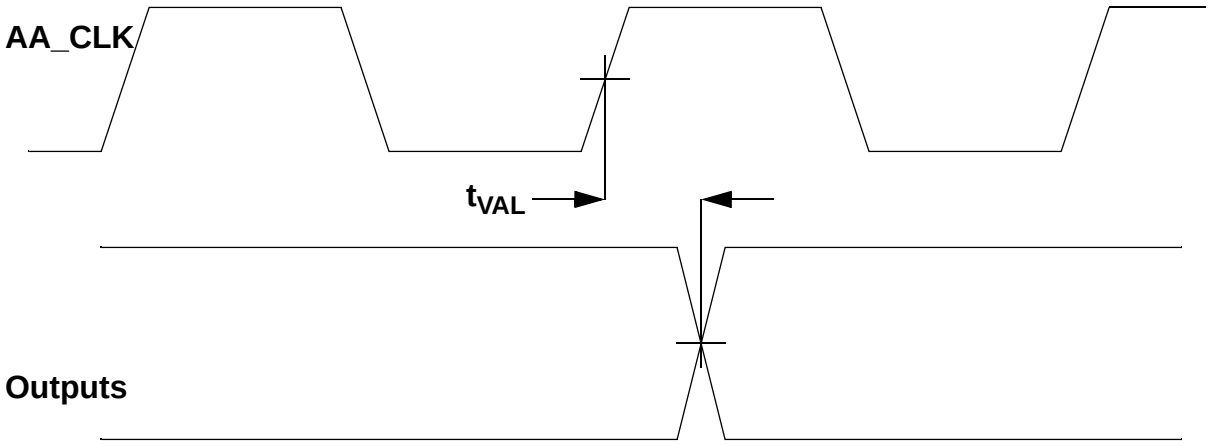

Figure 13.10 SLI/AA Output Waveforms

Table 13.14 SLI/AA Output Timing

Symbol	Parameter	Min	Max	Units
t_{VAL}	CLK to control signal valid delay	-	tbd	ns
t_{VAL}	CLK to data valid delay	-	tbd	ns

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13.11 SLI/AA Input Timing

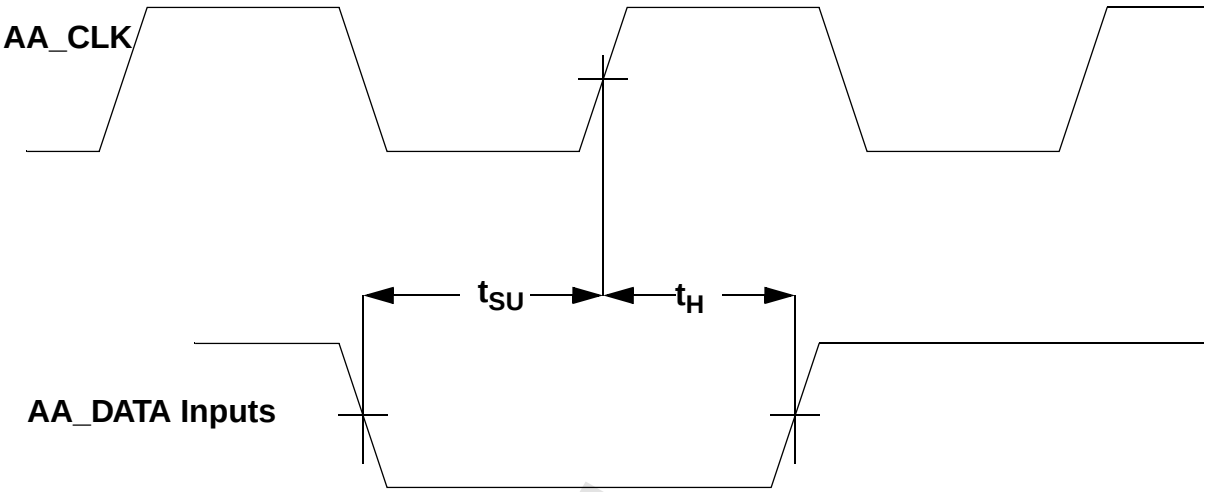

Figure 13.11 SLI/AA Input Waveforms

Table 13.15 SLI/AA Input Timing

Symbol	Parameter	Min	Max	Units
t_{SU}	MD setup time to MCLK_IN	tbd	-	ns
t_H	MD hold time to MCLK_IN	tbd	-	ns

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13.12 VMI Host Interface Mode A Timing: Manual

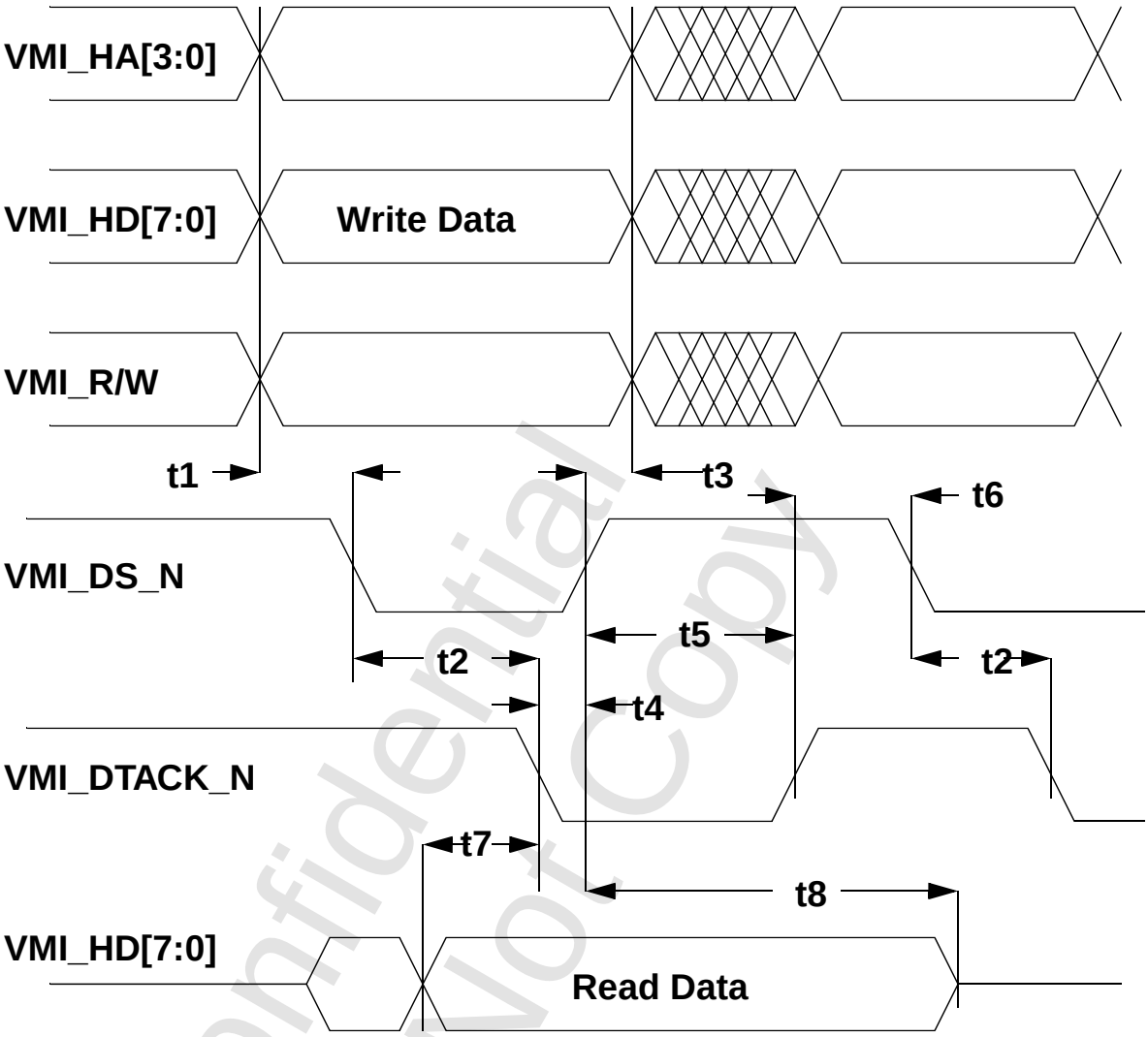

Figure 13.12 VMI Host Interface Mode A Waveforms: Manual

Table 13.16 VMI Host Interface Mode A Timing: Manual [a]

Symbol	Parameter	Min	Max	Units
t1	HA, HD, R/W# setup to DS# low	5	-	ns
t2	Delay DTACK# low after DS# low	0	13000	ns
t3	HA, HD R/W# hold after DS# high	5	-	ns
t4	Delay DS# high after DTACK# low	5	-	ns

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Table 13.16 VMI Host Interface Mode A Timing: Manual *(cont.)*[a]

Symbol	Parameter	Min	Max	Units
t5	Delay DTACK# high after DS# high	0	52	ns
t6	Delay DS# low (next cycle) after DTACK# high	5	-	ns
t7	(Read cycle) HD setup until DTACK# low	10	-	ns
t8	(Read cycle) HD hold after DS# high	0	-	ns

a. The timing parameters of VMI interface host cycles are explicitly controlled by bits in the vidSerialParallelPort register. The timing diagrams and tables are from the VMI specification and are included here for convenience.

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13.13 VMI Host Interface Mode A Timing: State Machine

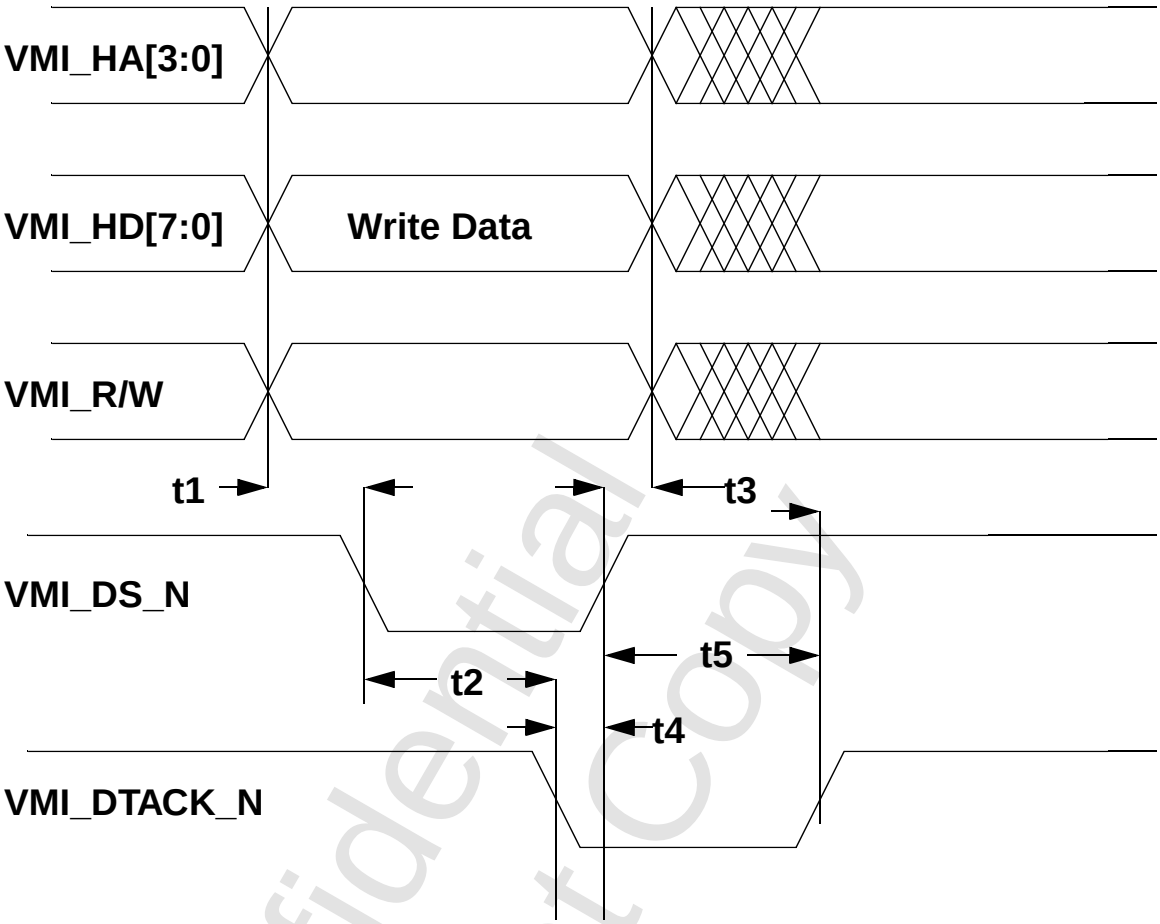

Figure 13.13 VMI Host Interface Mode A Waveforms: State Machine

Table 13.17 VMI Host Interface Mode A Timing: State Machine

Symbol	Parameter	Min	Max	Units
t1	HA, HD, R/W# setup to DS# low	tbd	-	cycles
t2	Delay DTACK# low after DS# low	0	13000	ns
t3	HA, HD R/W# hold after DS# high	tbd	-	cycles
t4	Delay DS# high after DTACK# low	tbd	-	cycles
t5	Delay DTACK# high after DS# high	0	52	ns

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13.14 VMI Host Interface Mode B Timing: Manual

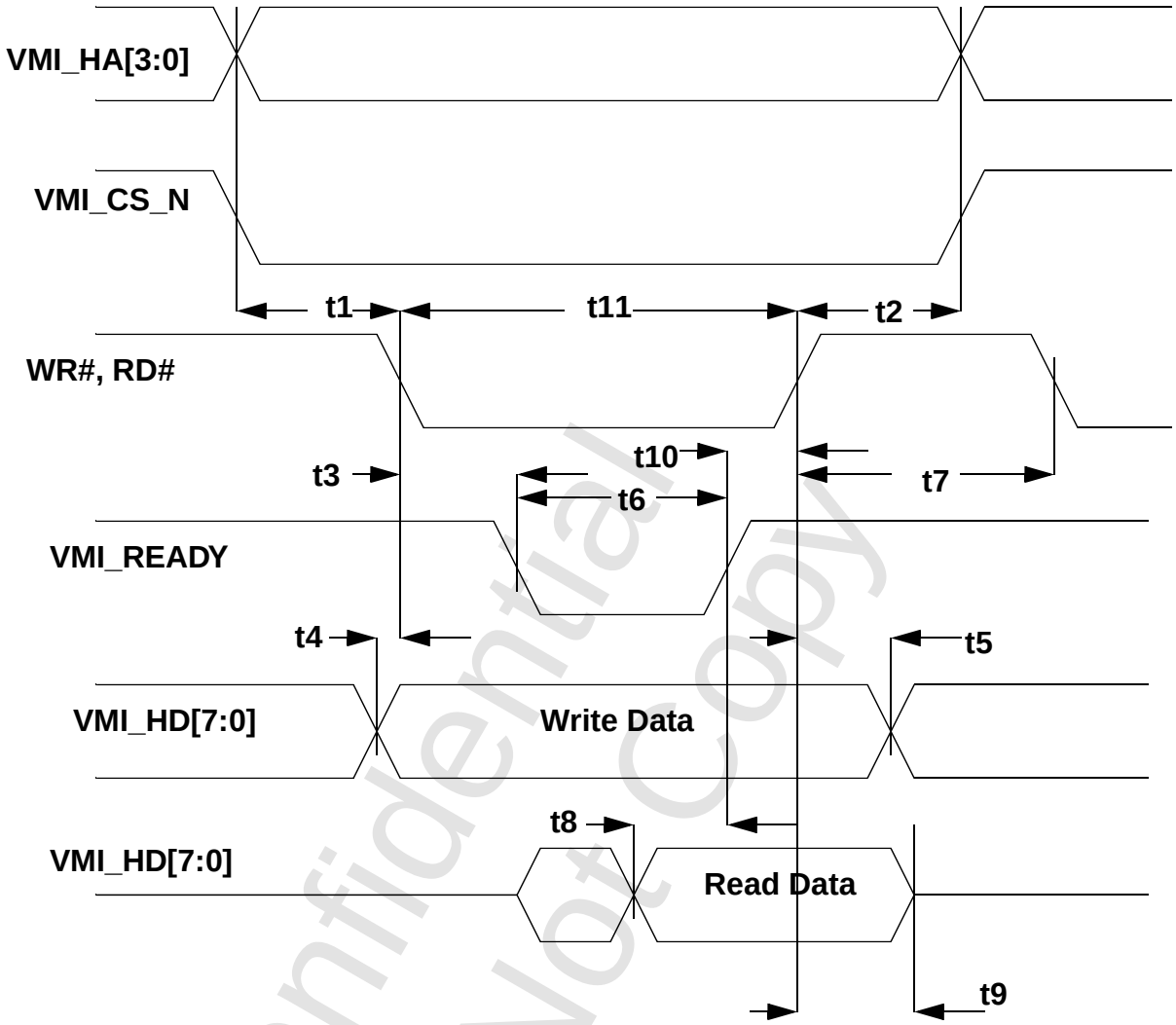

Figure 13.14 VMI Host Interface Mode B Waveforms: Manual

Table 13.18 VMI Host Interface Mode B Timing: Manual [a]

Symbol	Parameter	Min	Max	Units
t1	HA, CS# setup until WR# or RD# low	10	-	ns
t2	HA, CS# hold after WR# or RD# high	0	-	ns
t3	Delay READY low after WR# or RD# low	-	28	ns
t4	HD setup until WR# low (write cycle)	5	-	ns
t5	HD hold after WR# high (write cycle	10	-	ns

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Table 13.18 VMI Host Interface Mode B Timing: Manual *(cont.)*[a]

Symbol	Parameter	Min	Max	Units
t6	READY pulse width	0	-	ns
t7	WR# high until any command	38	-	ns
t8	HD setup until READY active (read cycle)	0	-	ns
t9	HD hold after RD# inactive (read cycle)	0	15	ns
t10	Delay WR# or RD# high after READY high	0	100	ns
t11	Read/Write command pulse width	40	-	ns

a. The timing parameters of VMI interface host cycles are explicitly controlled by bits in the vidSerialParallelPort register. The timing diagrams and tables are from the VMI specification and are included here for convenience.

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13.15 VMI Host Interface Mode B Timing: State Machinel

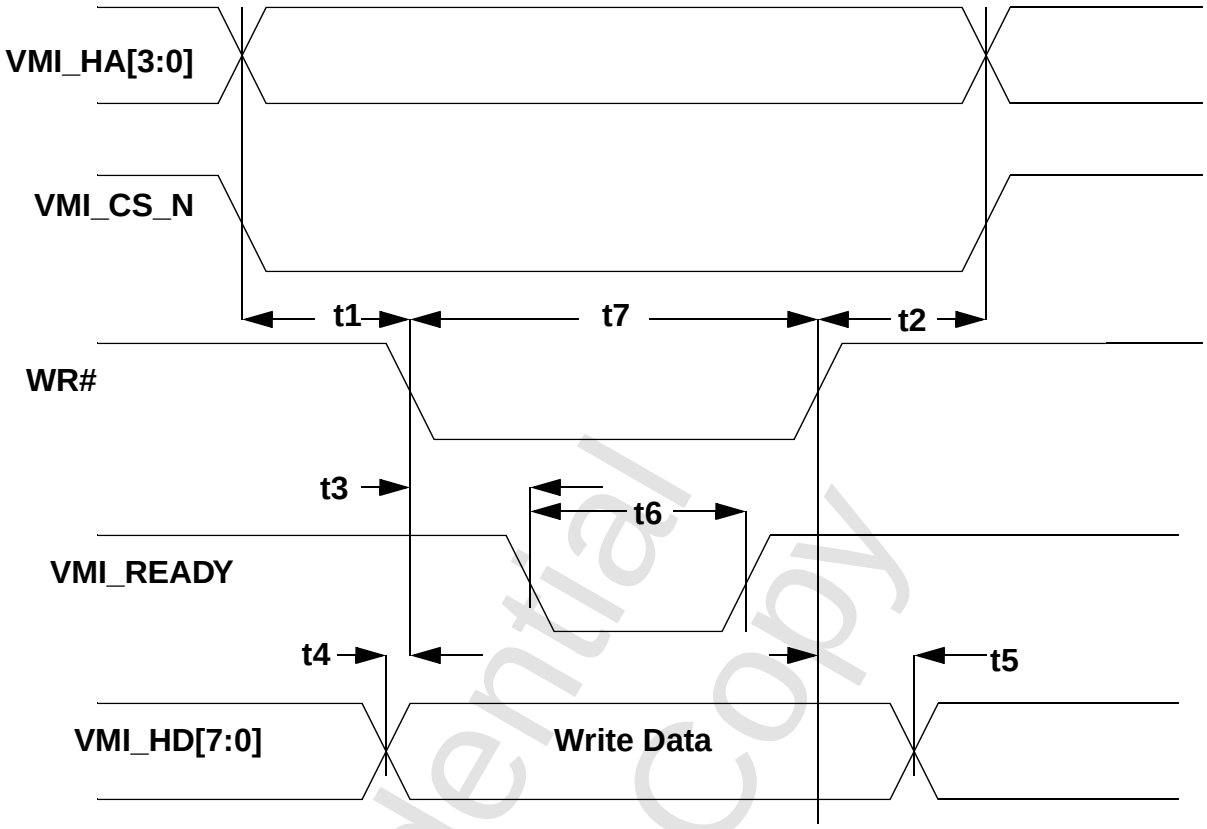

Figure 13.15 VMI Host Interface Mode B Waveforms: State Machine

Table 13.19 VMI Host Interface Mode B Timing: State Machine

Symbol	Parameter	Min	Max	Units
t1	HA, CS# setup until WR# low	tbd	-	cycles
t2	HA, CS# hold after WR# high	0	-	ns
t3	Delay READY low after WR# low	-	tbd	cycles
t4	HD setup until WR# low	tbd	-	cycles
t5	HD hold after WR# high	tbd	-	cycles
t6	READY pulse width	0	-	ns
t7	WR# command pulse width	tbd	-	cycles

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13.16 VMI Video In Timing

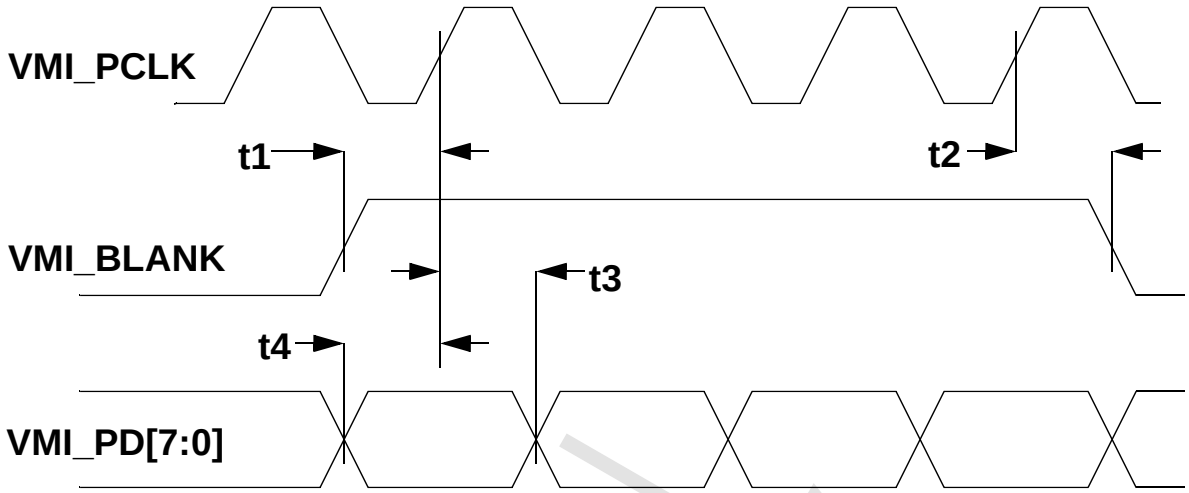

Figure 13.16 VMI Video In Waveforms

Table 13.20 VMI Video In Timing

Symbol	Parameter	Min	Max	Units
t1	VMI_BLANK (VACTIVE) setup to VMI_PCLK high	5	-	ns
t2	VMI_BLANK hold after VMI_PCLK high	0	-	ns
t3	VMI_PD[7:0] hold after VMI_PCLK high	0	-	ns
t4	VMI_PC[7:0] setup to MVI_PCLK high	5	-	ns

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13.17 Digital RGB Out Timing

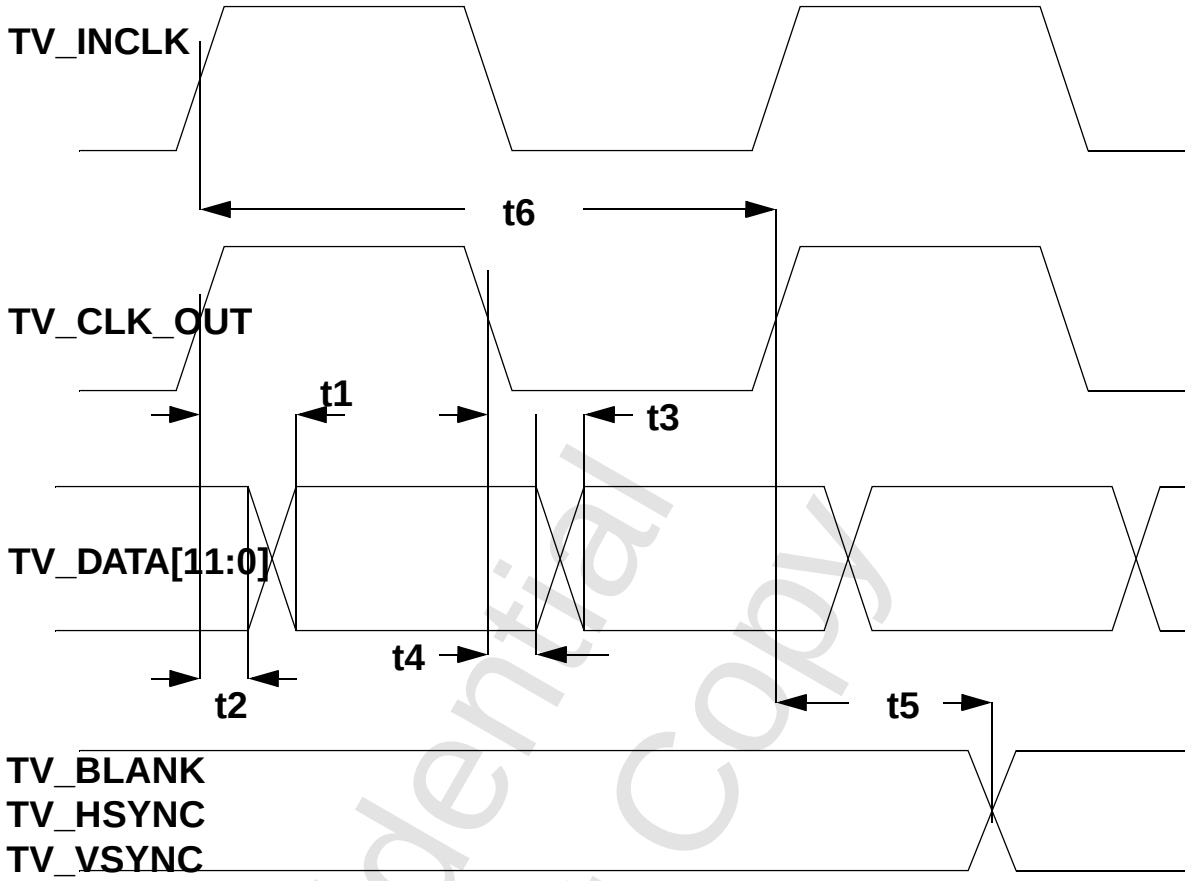

Figure 13.17 Digital RGB Out Waveforms

Table 13.21 Digital RGB Out Timing

Symbol	Parameter	Min	Max	Units
t1	Positive Clock Out to next Digital Data valid	-	tbd	ns
t2	Positive Clock Out to current Digital Data invalid	tbd	-	ns
t3	Negative Clock Out to next Digital Data valid	-	tbd	ns
t4	Negative Clock Out to current Digital Data invalid	tbd	-	ns
t5	Clock to Controls delay	-	tbd	ns
t6	Relationship between TV_INCLK and TV_CLK_OUT (Slave Mode only)	tbd	tbd	ns

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13.18 ROM Read Cycle

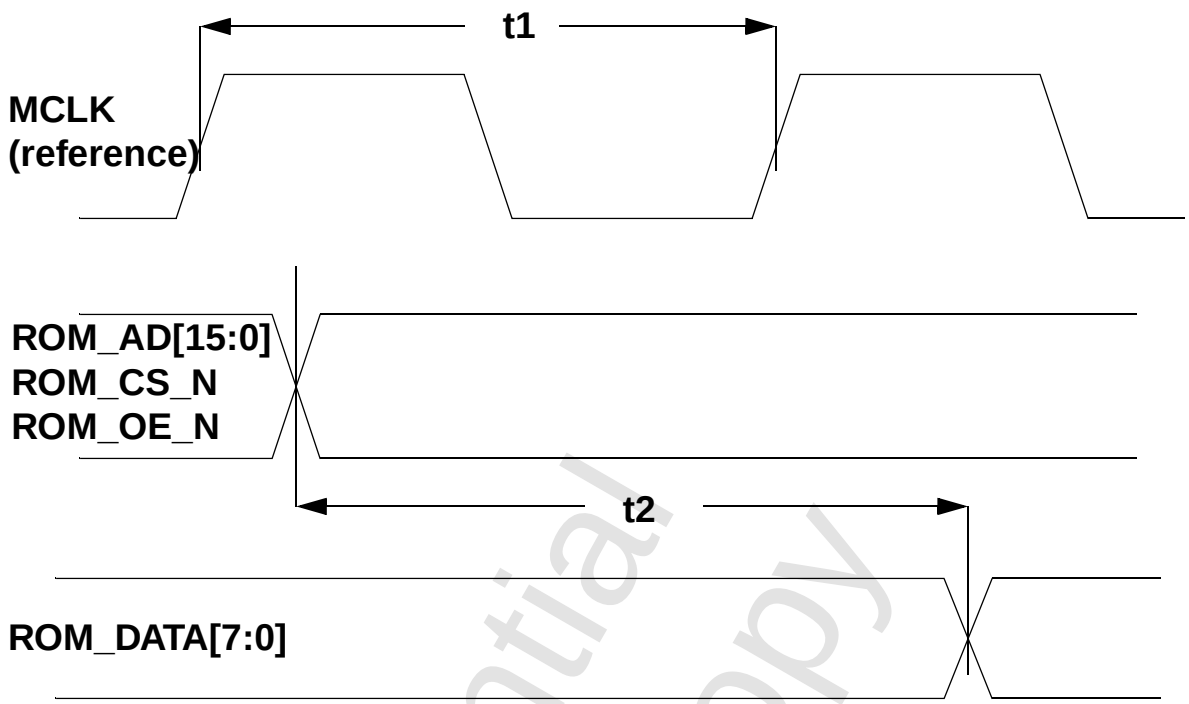

Figure 13.18 ROM Read Cycle Waveforms

Table 13.22 ROM Read Cycle

Symbol	Parameter	Min	Max	Units
t1	MCLK Period (Reference)	-	-	ns
t2	ROM_AD[15:0] to Data Valid	-	tbd	t1
t2	ROM_CS_N to Data Valid	-	tbd	t1
t2	ROM_OE_N to Data Valid	-	tbd	t1

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13.19 ROM Write Cycle

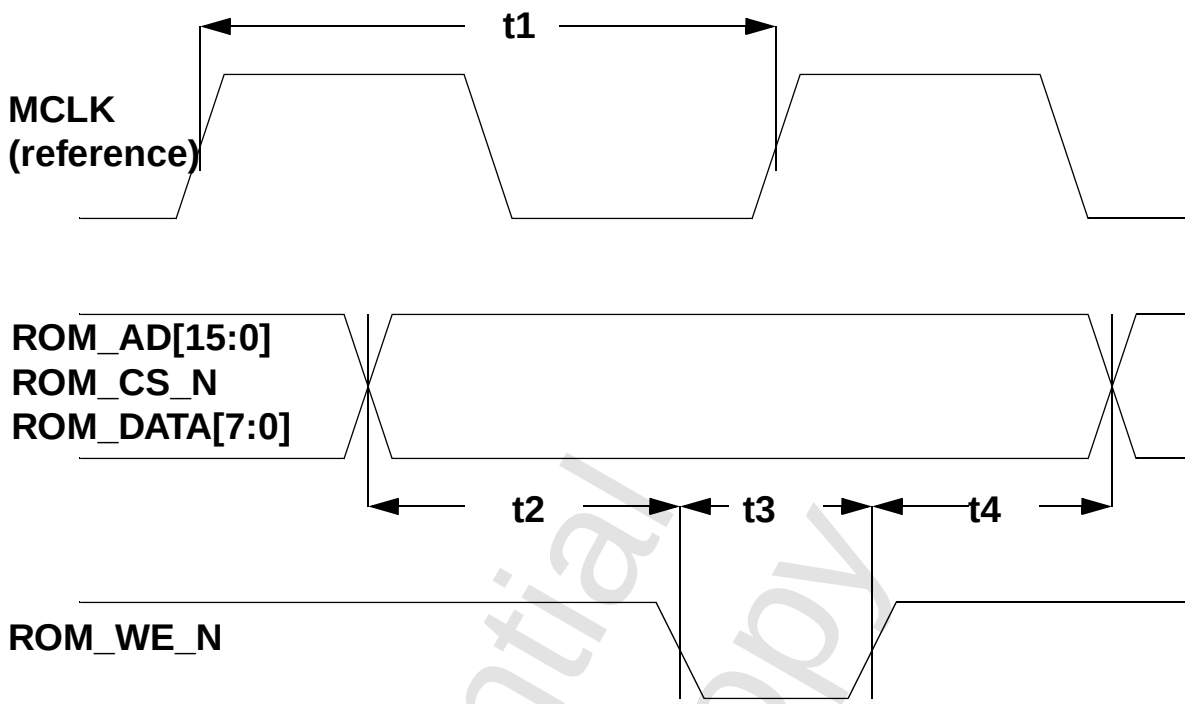

Figure 13.19 ROM Write Cycle Waveforms

Table 13.23 ROM Write Cycle

Symbol	Parameter	Min	Max	Units
t1	MCLK Period (Reference)	-	-	ns
t2	ROM_AD[15:0] to ROM_WE_N active	-	tbd	t1
t2	ROM_CS_N to ROM_WE_N active	-	tbd	t1
t2	ROM_DATA[7:0] to ROM_WE_N_active	-	tbd	t1
t3	ROM_WE_N Active low pulse width	-	tbd	t1
t4	ROM_AD[15:0] hold from ROM_WE_N inactive	-	tbd	t1
t4	ROM_CS_N hold from ROM_WE_N inactive	-	tbd	t1
t4	ROM_DATA[7:0] hold from ROM_WE_N inactive	-	tbd	t1

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14 Package

14.1 Physical Dimensions

The Napalm is supplied in a 348-pin 35-mm BGA package.

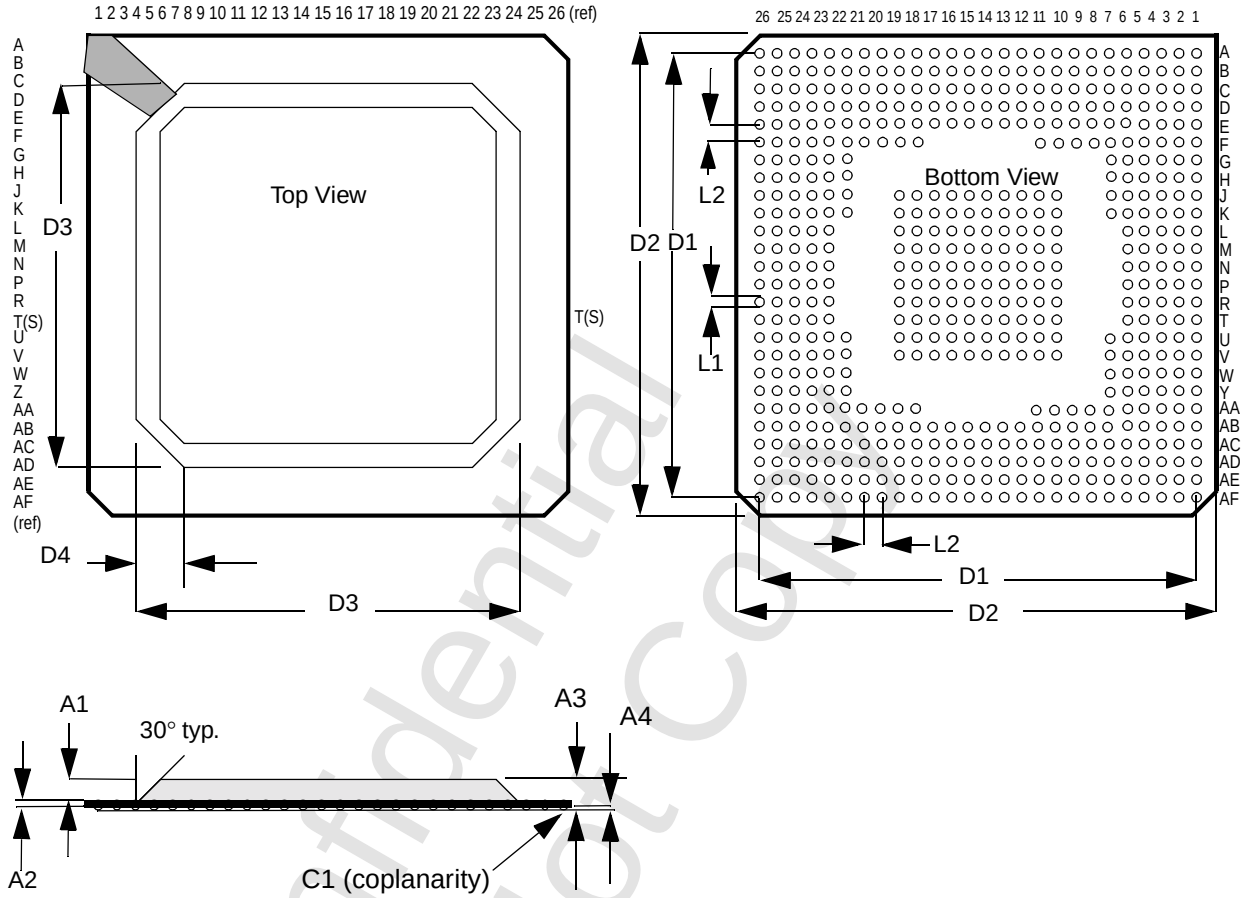

Figure 14.1 Physical Dimensions (mm)

Symbol	Minimum	Nominal	Maximum	B548-SW1
A1	1.12	1.17	1.22	A2
A2	.051	0.56	.061	c
A3	2.20	2.33	2.50	A
A4	-	0.60	-	A1
C1	-	-	0.15	ddd
D1	-	31.75	-	D1
D2	34.80	35.00	35.20	D
D3	-	30.00 ref	-	D2
D4	-	4.00	-	
L1	-	0.75	-	b
L2	-	1.27	-	e

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14.2 Pad Layout

Pads on the PC board may be placed as shown in Figure 14.2.

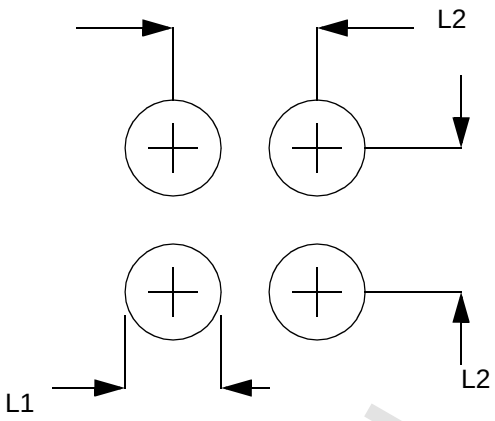

Figure 14.2 Pad Layout

Symbol	Minimum (mm)	Nominal (mm)	Maximum (mm)
L1		0.71	
L2		1.27	

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