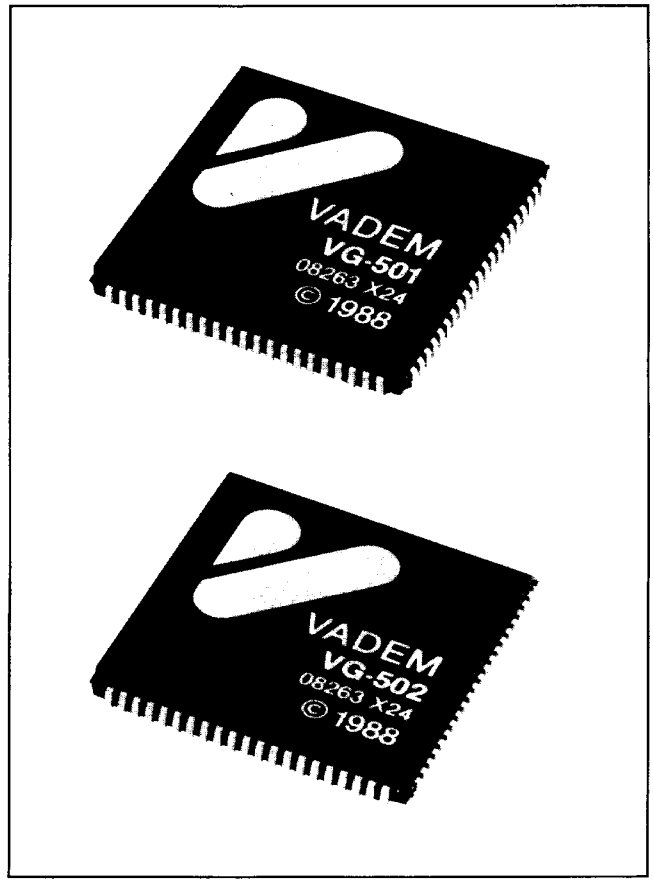
VADEM

VG-501 AND VG-502
PS/2 MODEL 30 AND PC/XT CHIP SET
FOR THE INTEL 80C186 PROCESSOR

June 1989

FEATURES

- ☐ Provides PC/XT and PS/2 Model 30 compatibility
- ☐ Low power 1.5 micron CMOS technology
- ☐ Functionality includes
  - — Model 30 Keyboard and mouse interface
  - — 8/16 bit bus conversion logic
  - — Speaker control logic
  - — Model 30 planar register
  - — Parity logic including parity generator
  - — DRAM controller and refresh logic
  - — Memory address decoder
  - — EMS 4.0 logic support to 32 MB capacity
  - — Timer clock generator
  - — Bus cycle generator logic
- ☐ Minimum component count for PS/2 Model 30 implementation
- ☐ Takes full advantage of on-board 80C186 peripherals
- ☐ Operation to 16 Mhz with zero wait states
- ☐ When used with VG-603, provides
  - — Parallel port
  - — Real time clock
  - — RS-232 Port
  - — ROM-DISK, when used with Vadem BIOS
- ☐ Each chip available in 84-pin PLCC (JEDEC STD)

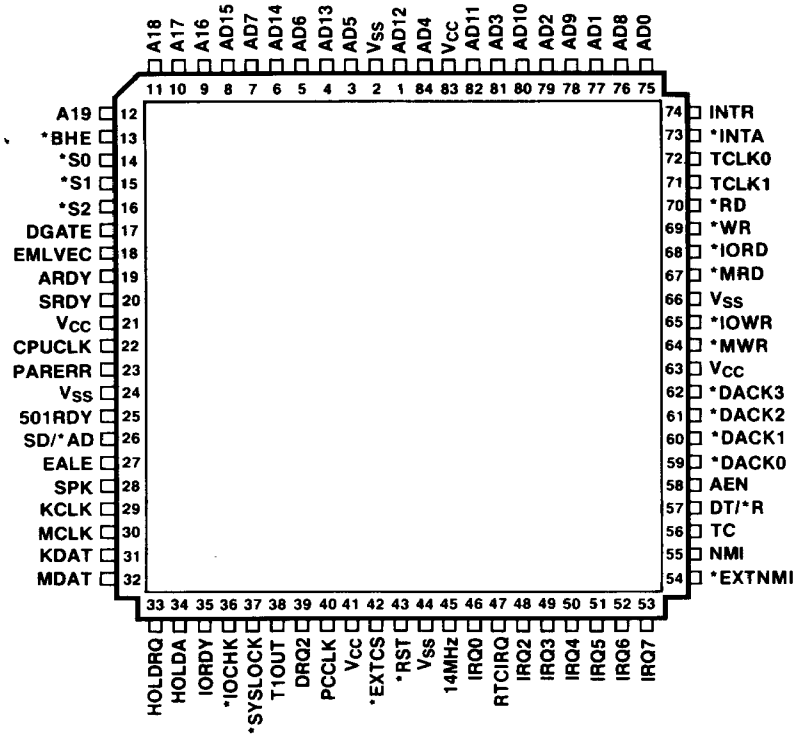


DESCRIPTION

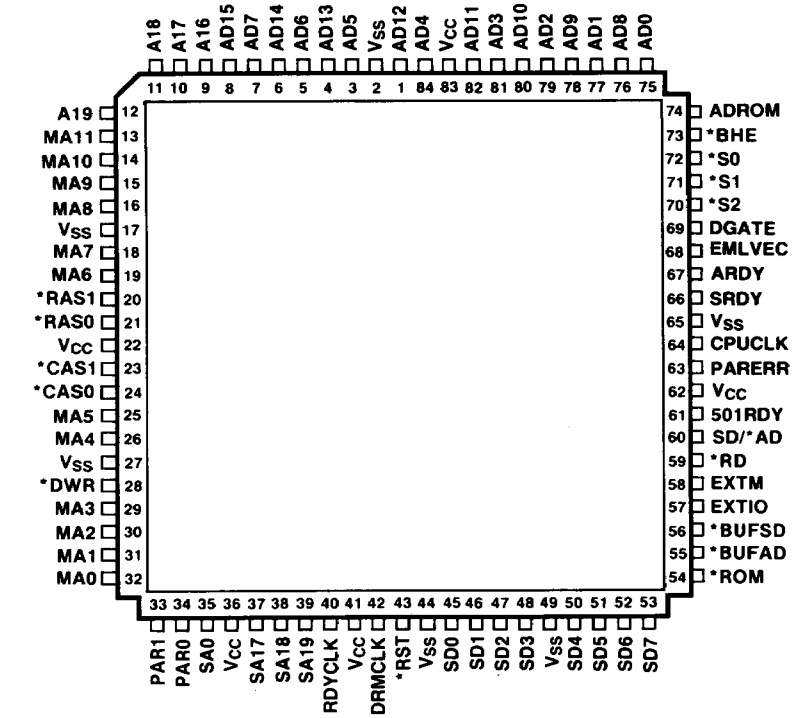
The Vadem VG-501 and VG-502 constitute a powerful two-chip set that, together with the Intel 80C186 processor, enables OEMs and system designers to build high performance, compact PS/2 Model 30 or PC/XT compatible systems with a minimum component count and hence, minimum size and cost. The VG-501/502 are ideal for embedded or dedicated PC applications because of their low power requirements, minimum component count, and their unique ability to work with Vadem's ROM DISK architecture enabling the easy design of a diskless PC environment.

The VG-501/502 are structured to provide Model 30 compatibility for the 80C186 CPU in the areas of DMA control, interrupt control, I/O control, speaker interface, parallel printer port and RAM memory control and timing.

VG-501 PIN CONFIGURATION



VG-502 PIN CONFIGURATION



VG-501 PIN DESCRIPTION

NAME	PIN	I/O	FUNCTION
AD[0:15]	1, 3–8; 75–82; 84	I/O	CPU resident multiplexed address/data bus.
A[16:19]	9–12	I/O	4 MSB of CPU resident address bus.
*S[0:2]	14–16	I/O	CPU resident bus status.
KDAT	31	I/O	Keyboard channel A data.
MDAT	32	I/O	Keyboard channel B data.
KCLK	29	I/O	Keyboard channel A clock.
MCLK	30	I/O	Keyboard channel B clock.
TCLK0	72	I/O	1.19 MHz clock to the 80C186 channel 0. At reset the output driver is off and the level of this pin is latched. This pin is used as SW5. A 10K pull up/down should be used.
TCLK1	71	I/O	1.19 MHz clock to the 80C186 channel 1. It is gated in the VG-501. At reset the output driver is off and the level of this pin is latched. This pin is used as SW6. A 10K pull up/down should be used.
*BHE	13	I/O	CPU resident bus high byte enable signal.
IRQ0	46	I	Input to VG-501 interrupt controller.
IRQ[2:7]	48–53	I	Inputs to VG-501 interrupt controller.
*INTA	73	I	Interrupt acknowledge from 80C186.
DRQ2	39	I	DMA channel 2 request to internal DMA controller.
HOLDA	34	I	Hold acknowledge from 80C186.
*IOCHK	36	I	I/O channel check signal.
T1OUT	38	I	Speaker timer. From 80C186.
14MHz	45	I	14.31818MHz clock input.
CPUCLK	22	I	80C186 CPU clock.
*RST	41	I	System reset.
IORDY	35	I	I/O channel ready signal.
SD/*AD	26	I	Indicates location of the addressed device. Low is on the AD bus and high is on the 8-bit system bus.
PARERR	23	I	DRAM parity error signal.
*EXTNMI	54	I	External input to I/O trapping logic.
ARDY	19	I	CPU resident bus asynchronous ready signal.
SRDY	20	I	CPU resident bus synchronous ready signal.
*EXTCS	42	O	Chip select output for address FC40–3. This is a tri-stated output that requires a pull-up. It must be qualified with a control signal and the device must be on the 8-bit data bus.
RTCIRQ	47	I	IRQ from optional Real Time Clock.
*SYSLOCK	37	I	Input from front panel key.
DT/*R	57	O	Latched *S1.
INTR	74	O	Interrupt request to 80C186.
TC	56	O	I/O channel DMA terminal count signal.
NMI	55	O	Non-maskable interrupt to 80C186.
SPK	28	O	Speaker data. Buffering required.
*IORD/WR *MRD/WR	68, 65 67, 64	O	I/O channel read/write signals.
*DACK[0:3]	59–62	O	I/O channel DMA acknowledge signals.
AEN	58	O	DMA address enable signal.
HOLDRQ	33	O	Hold request to 80C186.
DGATE	17	O	Timing signal to VG-502.
EMLVEC	18	O	Timing signal to VG-502.
PCCLK	40	O	I/O channel system clock signal.
EALE	27	O	Address Latch Enable.
501RDY	25	O	VG-501 ready signal to VG-502.
*RD	70	O	Tri-stated output. Active during DMA cycles as initiated by DRQ0 and DRQ2.
*WR	69	O	Tri-stated output. Active during DMA cycles as initiated by DRQ0 and DRQ2.

VG-502 PIN DESCRIPTION

NAME	PIN	I/O	FUNCTION
CPUCLK	64	I	80C186 CPU clock. CMOS input.
*RST	43	I	System reset.
*S[0:2]	70–72	I	CPU resident bus status.
AD[0:15]	75–82; 84–1; 3–8	I/O	CPU resident multiplexed address/data bus.
A[16:19]	9–12	I	4 MSB of the CPU resident address bus.
*BHE	73	I	CPU resident bus high byte enable.
*RD	59	I	CPU resident bus read signal.
SRDY	66	O	CPU resident bus synchronous ready signal.
ARDY	67	O	CPU resident bus asynchronous ready signal.
RDYCLK	40	I	Clock used to time ARDY signal. CMOS input.
501RDY	61	I	VG-501 ready signal. CMOS input.
SA0	35	O	LSB of the system address bus. CMOS input.
SA[17:19]	37–39	O	3 MSB of system address bus.
SD[0:7]	45–48; 50–53	O	System data bus.
DGATE	69	I	Timing signal generated by VG-501. CMOS input.
SD/*AD	60	I/O	Indicator of addressed device data bus.
DRMCLK	42	I	Clock used to time DRAM control signals. CMOS input.
MA[0:11]	13–16; 18–19; 25–26; 29–32	O	DRAM multiplexed address bus.
RAS[0:1]	20–21	O	Even and odd byte DRAM RAS signals.
CAS[0:1]	23–24	O	Even and odd bank DRAM CAS signals.
*DWR	28	O	DRAM write signal.
*BUFAD	55	O	DRAM data bus buffer enable.
PAR[0:1]	33–34	I/O	Even and odd byte DRAM parity bits.
PARERR	63	O	DRAM parity error signal.
*ROM	54	O	System ROM chip select signal.
EMLVEC	68	I	Timing signal generated by VG-501. CMOS input.
ADROM	74	I	Enable shadow BIOS ROM option.
*BUFSD	56	O	System data bus buffer enable.
EXTM	58	I/O	High indicates addressed memory is on the external 8-bit data bus.
EXTIO	57	I/O	High indicates addressed I/O and/or DMA devices are on the external 8-bit data bus.

VG-501 FUNCTIONAL DESCRIPTION

INTERRUPT CONTROLLER

The VG-501 interrupt controller has 8 channels, 7 external and one internal. The internal channel is connected to the VG-501 keyboard/mouse controller. The interrupt controller is compatible with the Intel 8259A. The output of the interrupt controller is connected to the INTO input of the C186. When the C186 receives an interrupt and does a INTACK cycle the VG-501 responds in the same way as the 8259A. This means that software interrupt routines will run without change.

DMA/REFRESH CONTROLLER

The DMA controller in the VG-501 provides two channels. One channel is intended for floppy disk transfers and is programmable. This channel operates in single transfer mode (Intel 8237A) and provides only the features and compatibility needed for use with floppy disk controllers. The second channel is for refresh and is not programmable. It has a fixed frequency derived from the 14MHz clock.

The controller uses the hold request/acknowledge feature of the C186. When the controller is ready to do a transfer it issues a hold request. Once the C186 releases the bus and returns a hold acknowledge the VG-501 becomes a bus master (looks like a C186). In the case of a floppy transfer, the DMA cycle is comprised of two bus cycles. The first is a read and the second is a write (except for a verify cycle which is a single I/O cycle). Both cycles are 8 bits wide. a DACK is generated during the I/O portion of the DMA cycle. If the DMA cycle is a refresh cycle then the VG-501 does one bus cycle which is a memory read. During a refresh cycle AD[0:11] will have the refresh address, AD[12:15] and A[16:19] are driven low. The DMA section contains circuitry that generates a DACK for each of the four channels used in a PC. There is also circuitry that counts DMA cycles for each channel and generates a TC during the I/O portion of the last cycle (count is set by the software).

KEYBOARD/MOUSE

The keyboard/mouse section of the VG-501 consists of two identical transmit and receive channels. There are additional inputs for a Real Time Clock interrupt and a "system locked" signal from a key in the front panel. The architecture for this controller is a sub-set of the Model 30 keyboard controller and is compatible at the BIOS level with the Model 30. Both channels works with a bi-directional keyboard or PS/2 mouse. The RTC interrupt is OR'ed with the interrupts from the two keyboard/mouse channels. This OR'ed interrupt is then connected internally to IRQ1 of the VG-501 interrupt controller. Both the source of the interrupt and the status of the front panel key are read from an internal I/O port.

TIMER

The timer section has one input and generates two outputs. The input is a 14MHz clock. The two outputs are equivalent to timer channels 1 and 2 of the PC. These outputs are connected to the timer inputs of the C186. Channel 1 is the 14MHz clock divided by 12 which is used as the clock source for the system timer. Channel 2 is gated in the VG-501 before going to the C186. This is done to emulate the gate feature of the 8253 that is used as a PC. Channel 2 is the clock source for the speaker clock. The speaker clock that comes from the C186 goes into the VG-501 where it is gated by the speaker data before driving a speaker through a buffer circuit.

BUS CYCLE GENERATOR

The PCCLK, *MRD, *MWR, *IORD, *IOWR, *DACK[0:3], AEN and TC IO Channel control signals are generated in the Bus Cycle Generator (BCG). PCCLK may be chosen to be ½, ⅓ or ¼ of the frequency of CPUCLK. The frequency divisor is chosen so that the frequency of PCCLK does not exceed 4.77 MHz. *MRD, *MWR, *IORD, *IOWR, *DACK[0:3], AEN and TC are all clocked by PCCLK. The BCG produces the following types of cycles:

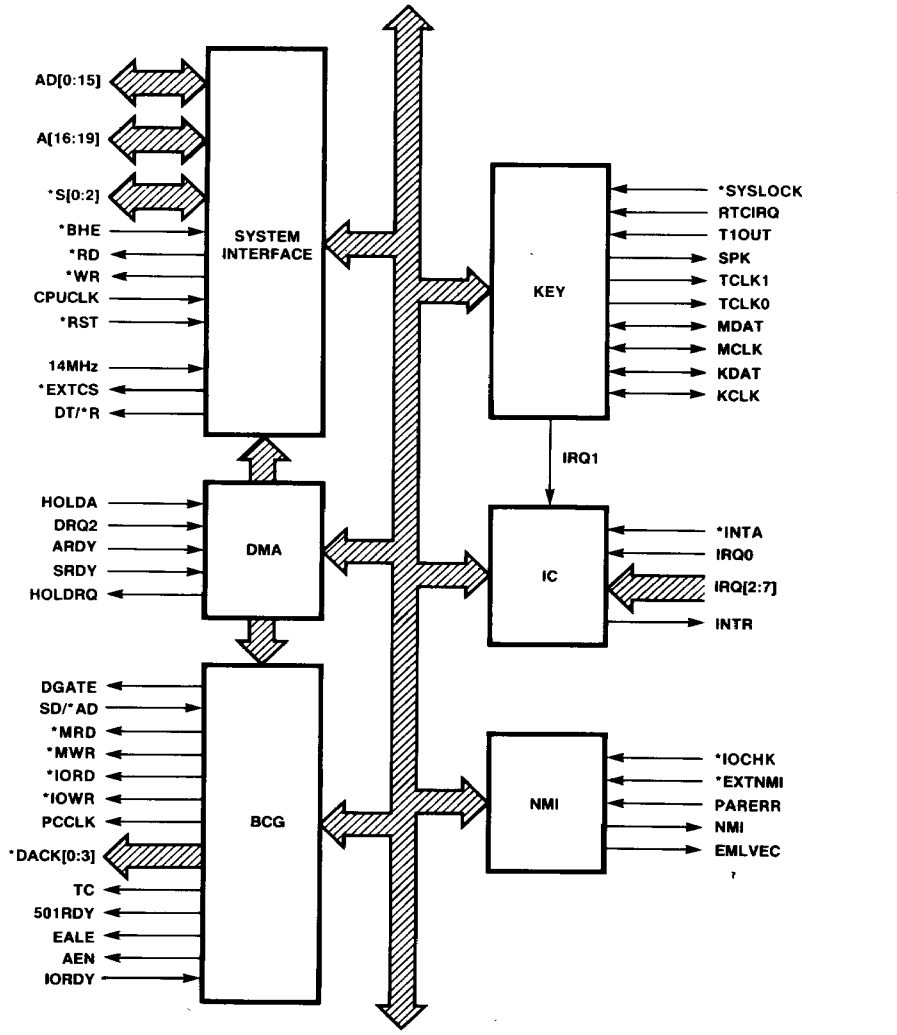
1. non-DMA memory read cycles;
2. non-DMA memory write cycles;
3. non-DMA IO read cycles;
4. non-DMA IO write cycles;
5. DMA memory read cycles;
6. DMA memory write cycles;
7. DMA IO read cycles;
8. DMA IO write cycles; and
9. refresh cycles.

Normally, non-DMA memory read and write cycles and refresh cycles have no IO Channel wait states. The remaining types of cycles normally have one IO Channel wait state. IORDY may be used to insert additional wait states. IORDY is tested by sampling on both the rising edge and then the falling edge of PCCLK. If both samples are set, the cycle is ended two IO Channel T-states later. If either sample is reset, then the cycle is extended one additional IO Channel wait state, and IORDY is again tested during the next IO Channel T-state. For non-DMA memory read and write cycles and for refresh cycles, IORDY is first tested during the IO Channel T2 state. For other cycles, IORDY is first tested during the IO Channel T3 state.

PARITY

The parity section accepts inputs from two PC compatible sources. One is the IOCHK signal from the expansion bus. The second source is the parity checker in the VG-502. This parity checker handles parity for any local DRAM. Both these parity sources generate an NMI and the keyboard has a compatible port to read that indicates the source of the NMI.

VG-501 BLOCK DIAGRAM



VG-502 FUNCTIONAL DESCRIPTION

CONTROL LOGIC

The CPUCLK, *S[0:2], *BHE, *RD, *RST, DGATE and SD/*AD signals are used for control throughout the VG-502. CPUCLK, *S[0:2], *BHE and *RD are connected to the corresponding 80C186 bus signals. *RST is the active low system wide reset signal. DGATE is a timing signal driven by the VG-501.

SD/*AD is a bidirectional open-drain signal. It should be connected to an external 2.2K pullup resistor and to the corresponding input pin of the VG-501. During a cycle, the value of SD/*AD determines the data bus (SD or AD) of the accessed device. The VG-502 needs this information to correctly route data during the cycle. The VG-501 bus cycle generator needs this information to determine if a SD bus cycle should be generated. The VG-502 resets SD/*AD when the following AD bus devices are accessed:

1. System DRAM
2. System ROM
3. 80C186 internal IO
4. VG-501 internal IO
5. VG-502 internal IO
6. Coprocessor IO

If the application requires other AD bus devices, these devices must reset SD/*AD with open drain signals whenever they are accessed. These devices should not reset SD/*AD during refresh cycles. SD bus devices should not drive SD/*AD.

IO channel refresh cycles use 5.6% of the system time. In many situations, only system DRAM needs to be refreshed. The VG-502 may be programmed so as to disable IO channel refresh. If this is done, system DRAM refresh uses only 2.1% of the system time when CPUCLK frequency is 16 MHz.

AD BUFFER, BUS CONVERTER AND SD BUFFER

These sections of the VG-502 are responsible for routing data between the 16-bit AD bus and the 8-bit SD bus during cycles. The AD buffer drives the VG-502 internal data bus. The bus converter routes data between the SD bus and either the low byte or the high byte of the AD bus. During an even addressed word access of an SD bus device, a double cycle occurs. The first cycle performs an even address byte transfer; the second cycle performs an odd address byte transfer.

EXTERNAL SD BUS CONTROL

If the application requires driving a large SD bus capacitive load, the *BUFSD signal of the VG-502 and the DT/*R signal of the VG-501 may be used to drive the active low enable and the direction controls of an external bidirectional SD bus buffer.

EXTM and EXTIO are bidirectional open drain signals. If no external SD buffer is used, EXTM and EXTIO should be grounded. If an external SD buffer is used, EXTM and EXTIO should be connected to external 10K pullup resistors. EXTM and EXTIO are used to determine the data bus (internal or external) of accessed SD bus devices. External SD bus devices should not drive EXTM or EXTIO.

When an external SD buffer is used, EXTM and EXTIO must be driven by internal SD bus devices with open drain drivers. When an internal SD bus memory device is addressed by the SA bus during a non-refresh cycle (*DACK0 = 1), it should reset EXTM. EXTM is ignored when SD bus system ROM is accessed. When an internal SD bus IO device is addressed by the SA bus during a non-DMA cycle (AEN = 0), it should reset EXTIO. When an internal SD bus DMA device is addressed by the *DACK[1:3] signals, it should reset EXTIO.

The VG-603 may be used to control a number of SD bus devices. The EXTM and EXTIO signals for the VG-603 controlled devices, are driven by the VG-603.

ADDRESS LATCH

The address latch is used to capture the 20-bit 80C186 bus address. The output of this latch drives the VG-502 internal address bus.

EMS ADDRESS MAPPER

The VG-502 provides memory mapping for Version 4.0 EMS. Up to 2048, 16 Kbyte mappable segments (32 Mbytes) of system DRAM may be mapped into 60, 16-Kbyte physical pages of 80C186 memory address space (00000H-EFFFFH). Since system

BIOS is always active, no mapping may occur in the address space, F0000H-FFFFFH. The VG-502 provides one regular mapping register set of 60, 12-bit registers. If the application requires EMS, the VADEM EMS driver must be used.

PLANAR RAM CONTROL STATUS REGISTER

The VG-502 implements a Model 30 compatible planar RAM control status register (PRCS).

ADDRESS MULTIPLEXER

The address multiplexer routes the VG-502 internal address bus and the EMS mapper output to the SA and MA address busses. SA0 and SA[17:19] are driven by the VG-502. SA[1:16] are driven by two external octal latches. AD[1:16] are the inputs to these latches and the ALE signal of the VG-501 is the gate for these latches.

The row and column system DRAM addresses are routed to the MA bus. MA address multiplexing supports DRAM arrays with banks of 256K x 16, 1M x 16, and 4M x 16.

SYSTEM DRAM CONTROL

The VG-502 provides control signals for various DRAM arrays. The DRAM control signals are *RAS[0:1], *CAS[0:1], *DWR and *BUFAD. The DRAM array is 16 bits wide. *RAS0 drives the even byte DRAM *RAS signals; *RAS1 drives the odd byte DRAM *RAS signals. *DWR drives the DRAM *WE signals.

If the capacitive load of the AD bus is not too great, the DRAM array data bus may directly drive the AD bus. Otherwise, the *BUFAD signal of the VG-502 and the DT/*R signal of the VG-501 may be used to drive the active low enable and the direction controls of an external system DRAM bidirectional buffer.

There may be any number of 16-bit wide banks. When an even bank is selected, *CAS0 is asserted; when an odd bank is selected, *CAS1 is asserted. If there is one bank, *CAS0 directly drives all DRAM *CAS signals. If there are only two banks, *CAS0 directly drives DRAM bank 0 *CAS signals and *CAS1 directly drives DRAM bank 1 *CAS signals. If there are more than two banks, then *CAS0 and *CAS1 are demultiplexed to provide a separate *CAS signal for each bank. The upper MA bus bits control which *CAS bank signal to assert.

BANK SIZE	MAX # BANKS	MAX SIZE
256K x 16	16	8 Mbytes
1M x 16	8	16 Mbytes
4M x 16	4	32 Mbytes

BANK SIZE	MA11	MA10	MA9	*CAS0	*CAS1	DRAM BANK	ADDRESS
256K x 16	0	0	0	0	1	0	0000000
256K x 16	0	0	0	1	0	1	0080000
256K x 16	0	0	1	0	1	2	0100000
256K x 16	0	0	1	1	0	3	0180000
256K x 16	0	1	0	0	1	4	0200000
256K x 16	0	1	0	1	0	5	0280000
256K x 16	0	1	1	0	1	6	0300000
256K x 16	0	1	1	1	0	7	0380000
256K x 16	1	0	0	0	1	8	0400000
256K x 16	1	0	0	1	0	9	0480000
256K x 16	1	0	1	0	1	A	0500000
256K x 16	1	0	1	1	0	B	0580000
256K x 16	1	1	0	0	1	C	0600000
256K x 16	1	1	0	1	0	D	0680000
256K x 16	1	1	1	0	1	E	0700000
256K x 16	1	1	1	1	0	F	0780000

BANK SIZE	MA11	MA10	*CAS0	*CAS1	DRAM BANK	ADDRESS
1M x 16	0	0	0	1	0	0000000
1M x 16	0	0	1	0	1	0200000
1M x 16	0	1	0	1	2	0400000
1M x 16	0	1	1	0	3	0600000
1M x 16	1	0	0	1	4	0800000
1M x 16	1	0	1	0	5	0A00000
1M x 16	1	1	0	1	6	0C00000
1M x 16	1	1	1	0	7	0E00000

BANK SIZE	MA11	*CAS0	*CAS1	DRAM BANK	ADDRESS
4M x 16	0	0	1	0	0000000
4M x 16	0	1	0	1	0800000
4M x 16	1	0	1	2	1000000
4M x 16	1	1	0	3	1800000

DRMCLK is used to clock the DRAM control signals. If the 80C186 data valid setup requirement is met, DRMCLK may be driven by CPUCLK. Otherwise DRMCLK must be driven by an advanced CPUCLK. In this case an external delay line, driven by CPUCLK, should be used to generate DRMCLK. This is necessary in order to satisfy 80C186 data bus setup time requirements during system DRAM read cycles. System DRAM accesses may be programmed to take either 4 or 5 80C186 T-cycles.

PARITY LOGIC

The VG-502 provides parity generation and checking for system DRAM. PAR1 is the odd byte parity signal; PAR0 is the even byte parity signal. During write cycles, PAR[0:1] are generated and output. During system DRAM odd byte read cycles, PAR1 is input and checked. During system DRAM even byte read cycles, PAR0 is input and checked. During system DRAM word read cycles, PAR[0:1] are input and checked. Parity errors are reported by the PARERR signal. PARERR is connected to the corresponding VG-501 input.

SYSTEM CONTROL ROM

The VG-502 *ROM output signal drives the *CE input of the system ROM. The 80C186 bus *RD signal drives the *OE input of the system ROM.

The SA bus drives the address inputs of the system ROM. The VG-502 allows the data bus of the system ROM to be either the AD bus or the SD bus. The ADROM input signal is used by the VG-502 to determine the position of the system ROM. ADROM is internally pulled up.

If the data bus of the system ROM is the 16-bit AD bus, then ADROM should not be connected. In this case, two 32 Kbyte ROMs are necessary. An AD bus system ROM word read cycle may be programmed to take either 4 or 6 80C186 T-cycles (250 ns or 375 ns, for a 16 MHz CPUCLK).

If the data bus of the system ROM is the 8-bit SD bus, then ADROM should be grounded. In this case a single 64 Kbyte ROM is necessary. A SD bus system ROM word read cycle takes 8 IO channel T-cycles (about 1680 ns).

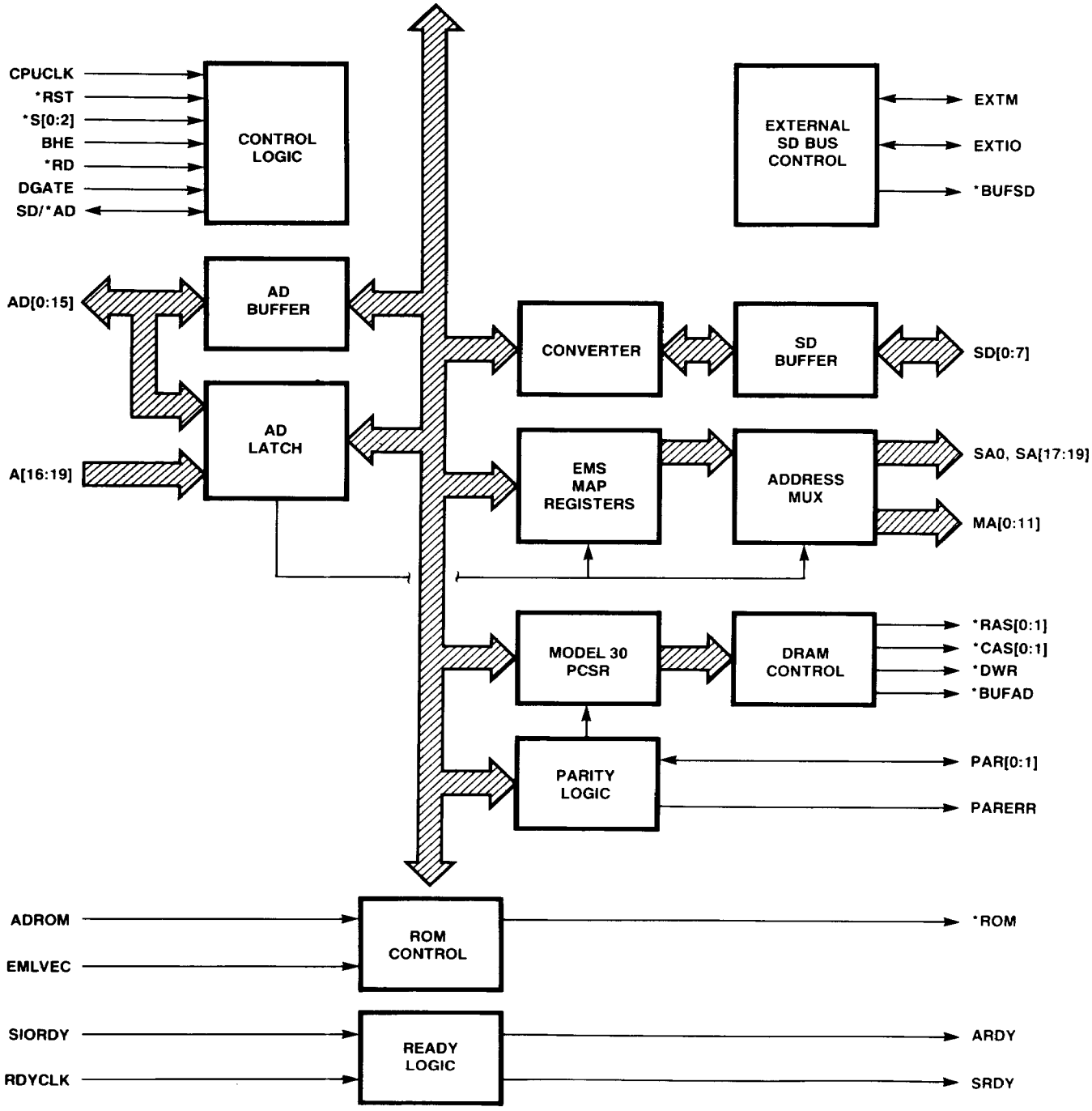
System ROM contents may be shadowed in system DRAM. In this case, accesses in the memory address range, F0000H–FFFFFH, are directed to the shadowed DRAM. A word read of shadowed DRAM may be programmed to take either 4 or 5 80C186 T-cycles (250 ns or 312.5 ns for a 16 MHz CPUCLK). DRAM array size must be at least 1 Mbyte for shadowing to be enabled. 64 Kbytes of system DRAM is used by shadow DRAM.

EMLVEC input signal is driven by the VG-501. EMLVEC causes system ROM to respond to certain cycles used in IO emulation.

READY LOGIC

The VG-502 generates the 80C186 bus signals, ARDY and SRDY. 501RDY is driven by the VG-501. It is used in certain cycles to determine ARDY and SRDY. ARDY is clocked on falling edges of RDYCLK. If the 80C186 ARDY setup time requirement is met, RDYCLK may be driven by CPUCLK. Otherwise RDYCLK must be driven by an advanced CPUCLK. In this case, an external delay line, driven by CPUCLK should be used to generate RDYCLK.

VG-502 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{CC}	—	7.0	V
Input voltage	V_I	-0.5	5.5	V
Output current	V_O	-0.5	5.5	V
Operating temperature range	T_{op}	-25	85	°C
Storage temperature range	T_{stg}	-40	125	°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Limits		Unit
		Interfacing with TTL		
		Min	Max	
Power Supply Voltage	V_{CC}	4.75	5.25	V
Operating Temperature	T_{opt}	0	70	°C
Low-level Input Voltage (TTL)	V_{IL}	-0.5	0.8	V
High-level Input Voltage (TTL)	V_{IH}	2.0	5.5	V
Low-level Input Voltage (CMOS)	V_{IL_C}	-0.5	0.8	V
High-level Input Voltage (CMOS)	V_{IH_C}	3.0	5.5	V
Positive Schmitt Trigger Voltage	V_P	1.4	2.2	V
Negative Schmitt Trigger Voltage	V_N	0.8	—	V
Hysteresis	V_H	0.4	0.5	V
Rise/Fall Time	t_r/t_f	1	3	ns

DC CHARACTERISTICS

Parameter	Symbol	Limits			Unit	Comments
		Min	Typ	Max		
Quiescent Current	I_{Q1}			1	mA	@ CMOS high or low levels (V_{CC} or GND)
Quiescent Current	I_{Q2}			15	mA	@ TTL
Output Hi-Z Leakage Current	I_{OZ}	-200		200	A	
Off-state Output Leakage Current	I_{OLK}			0.01	mA	@ TTL high or low levels (2.4V or 0.8V)
Operating Current	I_{CC}		100		mA	
Input Current	I_{IN}			0.01	mA	
Low-level Output Current (Note 1)	I_{OL}	2		12	mA	See below
High-level Output Current (Note 2)	I_{OH}	2		12	mA	See below
Low-level Output Voltage	V_{OL}	0		0.45	V	@ I_{OL} as specified
High-level Output Voltage	V_{OH}	2.4		V_{CC}	V	@ I_{OH} as specified

Notes:
(1) $V_{OL}=0.4V$
(2) $V_{OH}=2.4V$

VG-501/502 INPUT LOADING

All inputs have input capacitance no greater than 8 pF.

VG-501
OUTPUT CURRENT DRIVING CAPABILITIES/LOAD[1]

Pin Name	Pin No.	I_{OL} (mA)	I_{OH} (mA)	Max Load (pF)
AD[0:15]	1, 3-9, 75-82, 84	8	4	100
A[16:19]	9-12	8	4	100
*BHE	13	8	4	100
KCLK	29	8	4	100
KDAT	31	8	4	100
MCLK	30	8	4	100
MDAT	32	8	4	100
*S[0:2]	14-16	8	4	100
TCLK0	72	4	4	50
TCLK1	71	4	4	50
*EXTCS	42	2	2	50
501RDY	25	4	2	50
AEN	58	12	12	200
*DACK[0:3]	59-62	12	12	200
DT/*R	57	8	4	100
EALE	27	8	4	50
EMLVEC	18	4	2	50
DGATE	17	4	2	50
HOLDRQ	33	4	2	50
INTR	74	4	2	50
*IORD	68	12	12	200
*IOWR	65	12	12	200
*MRD	67	12	12	200
*MWR	64	12	12	200
NMI	55	4	2	50
PCCLK	40	12	12	200
SPK	28	4	2	50
TC	56	12	12	200
*RD	70	4	4	75
*WR	69	4	4	75

VG-502
OUTPUT CURRENT DRIVING CAPABILITIES/LOAD[1]

Pin Name	Pin No.	I_{OL} (mA)	I_{OH} (mA)	Max Load (pF)
AD[0:15]	1, 3-8, 75-82, 84	8	4	100
EXTIO	57	4	2	50
EXTM	58	4	2	50
PAR[0:1]	33-34	4	2	50
SD[0:7]	45-48, 50-53	12	12	100
SD/*AD	60	4	2	50
ARDY	67	4	2	50
*BUFSD	56	4	2	50
*BUFAD	55	4	2	100
*CAS[0:1]	23-24	8	4	200
*DWR	28	12	12	200
MA[0:11]	13-16, 18-19, 25-26, 29-32	12	12	200
PARERR	63	4	2	50
*RAS[0:1]	20-21	12	12	100
*ROM	54	4	2	50
SA0	35	12	12	100
SA[17:19]	37-39	12	12	100
SRDY	66	4	2	50

Note 1: These maximum output loading satisfied all timing specifications. Actual output loading can exceed C_{LOAD} (MAX) at design's risk if timing specifications are *not* observed.

VG-501 TIMING CHARACTERISTICS

Parameter	Symbol	Limits Min	Limits Max	Unit
*S0:2 to EALE high	T101		20	ns
*S0:2 valid to CPUCLK ↑	T102		25	ns
Address valid to *EXTCS valid	T103		40	ns
EMLVEC high from NMI ↑	T104		45	ns
EALE to DT/R valid	T105		30	ns
Data valid from CPUCLK ↓	T106		60	ns
Data hold from CPUCLK ↓	T107	10		ns
Data available before CPUCLK ↑	T108	40		ns
Data held after CPUCLK ↑	T109	40		ns
Outputs valid from CPUCLK ↑	T110		100	ns
CPUCLK ↑ to EALE low	T111	15	30	ns
CPUCLK ↓ to HOLDRQ high	T112	35		ns
HOLDA setup to CPUCLK ↑	T113	15		ns
*S0:2 high from CPUCLK ↑	T114		40	ns
AD16:19 valid from CPUCLK ↑	T115		30	ns
*S0:2 valid from CPUCLK ↑	T116		25	ns
AD0:15 valid from CPUCLK ↓	T117		40	ns
*S0:2 high from CPUCLK ↓	T118		30	ns
HOLDRQ low from CPUCLK ↓	T119	4	35	ns
AD0:15 float from CPUCLK ↑	T120		40	ns
AD16:19 float from CPUCLK ↓	T121		40	ns
Address hold time from CPUCLK ↓	T122		5	ns
Data setup for DMA read	T123	20	ns	
Data hold for DMA read	T124	8	ns	
ARDY setup to CPUCLK ↑	T126	15		ns
ARDY hold from CPUCLK ↑	T127	15		ns
SRDY setup to CPUCLK ↓	T128	15		ns
SRDY hold from CPUCLK ↓	T129	15		ns
*RD/*WR low from CPUCLK ↓	T130	5	30	ns
*RD/*WR high from CPUCLK ↓	T131	5	30	ns
Data valid from CPUCLK ↓	T133		35	ns
Data hold from CPUCLK ↑	T134	5		ns
INTR high from IRQX	T135		100	ns
INTR low from *INTA ↓	T136		40	ns
AD0:15 valid from *INTA ↓	T137		60	ns
AD0:15 hold from *INTA ↑	T138	10		ns
TCLK valid from 14MHz ↑	T139		50	ns
*DACK low from PCCLK ↓	T140		25	ns
*DACK high from PCCLK ↓	T141		25	ns
AEN high from PCCLK ↓	T142		25	ns
AEN low from PCCLK ↓	T143		25	ns
*MRD/*IORD low from PCCLK ↓	T144	10	35	ns
*MRD/*IORD high from PCCLK ↓	T145	10	35	ns
*MWR/*IOWR low form PCCLK ↓	T144	10	35	ns

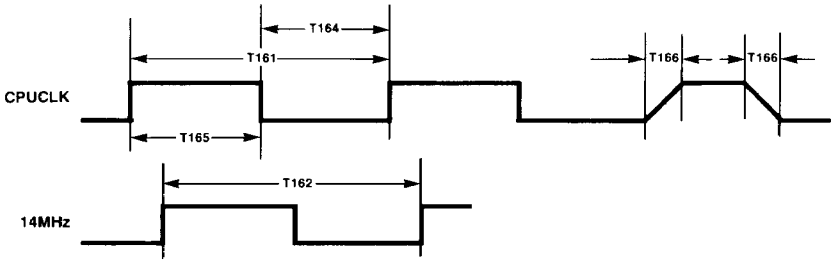
VG-501 TIMING CHARACTERISTICS (continued)

Parameter	Symbol	Limits Min	Limits Max	Unit
*MWR/*IOWR high from PCCLK ↓	T145	10	35	ns
PCCLK high from CPUCLK ↓	T148		40	ns
PCCLK low from CPUCLK ↓	T149		40	ns
DGATE/501RDY high from CPUCLK ↓	T152		25	ns
DGATE/501RDY low from CPUCLK ↓	T153		25	ns
NMI high from CPUCLK ↑	T154		25	ns
NMI low from CPUCLK ↑	T155		25	ns
NMI high from IOCHK ↓	T156		50	ns
NMI high from PARERR ↑	T157		50	ns
CPUCLK clock period	T161	62.5		ns
14 MHz clock period (see note 1)	T162	70		ns
TC valid from PCCLK ↑	T163		35	ns
CPUCLK Low	T164	26.5		ns
CPUCLK high	T165	26.5		ns
CPUCLK rise, fall time	T166		5	ns
DRQ2 setup to CPUCLK ↓	T167	15		ns
IORDY hold from PCCLK	T168	10		ns
SD/*AD hold from CPUCLK ↓	T169	10		ns
IORDY setup to PCCLK	T170	25		ns
SD/*AD setup to CPUCLK ↓	T171	25		ns

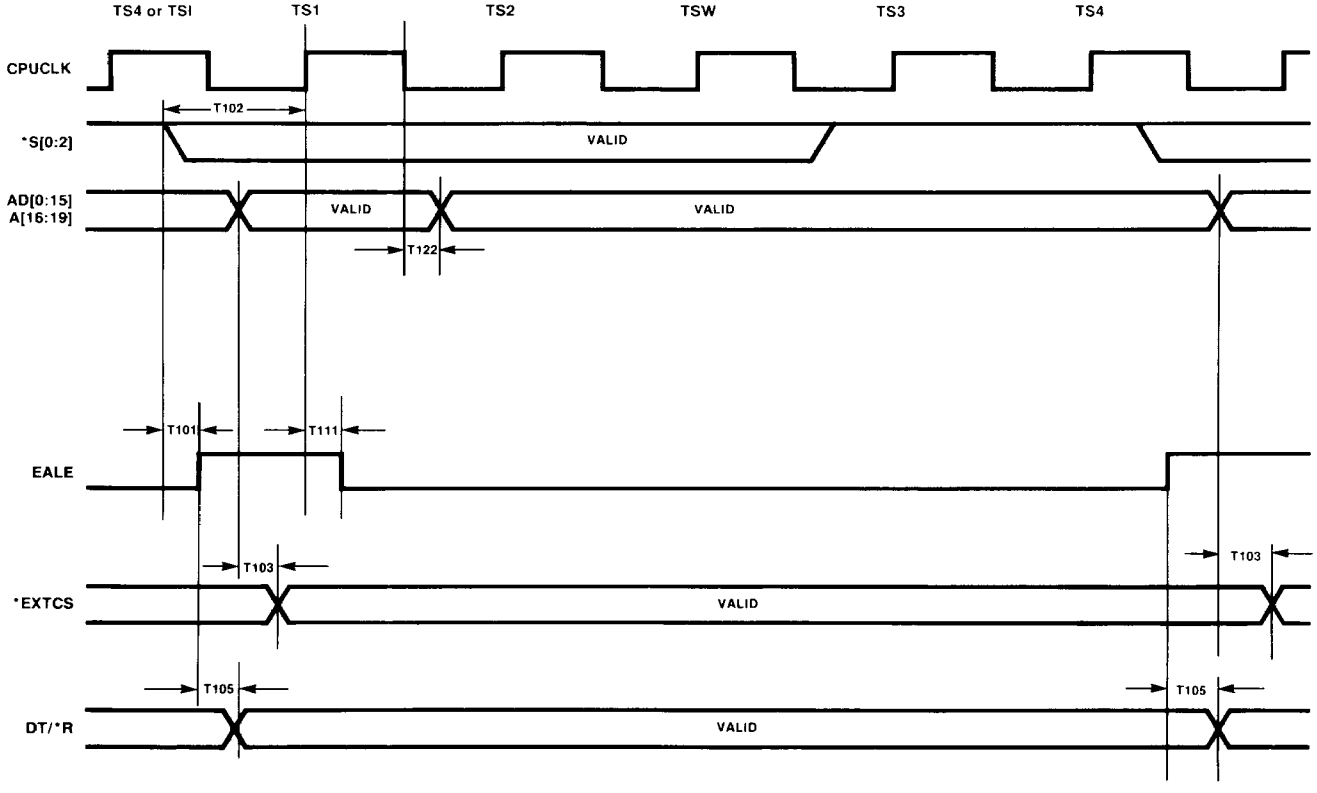
Note 1: 14.31818MHz clock period 69–84ns typ•100 ppm.

VG-501 TIMING WAVEFORMS

Clock Specifications

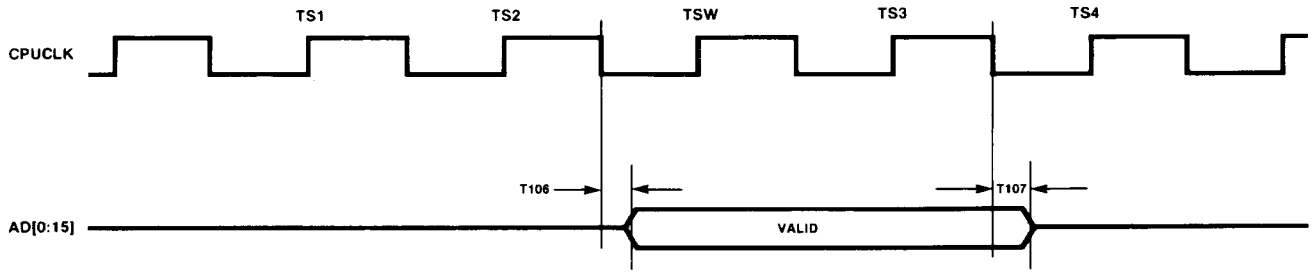


Basic CPU Cycle

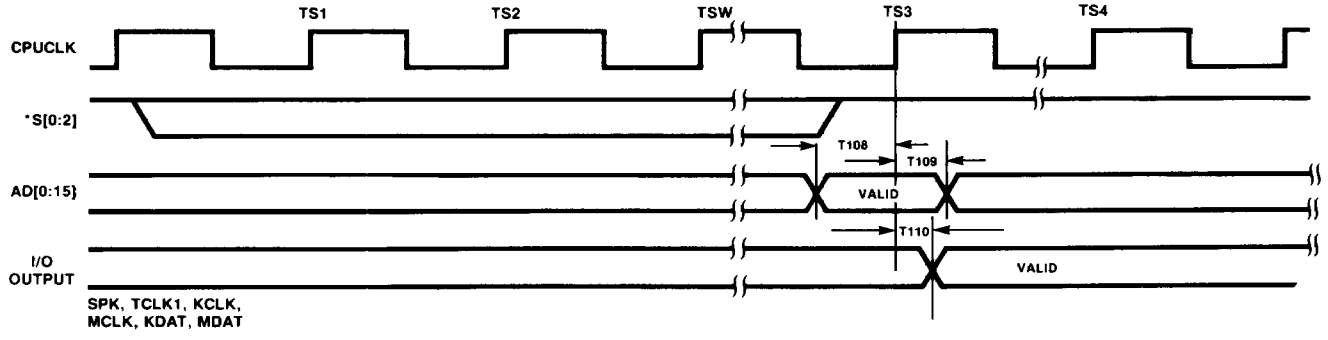


VG-501 TIMING WAVEFORMS (continued)

CPU I/O Read from VG-501 Registers

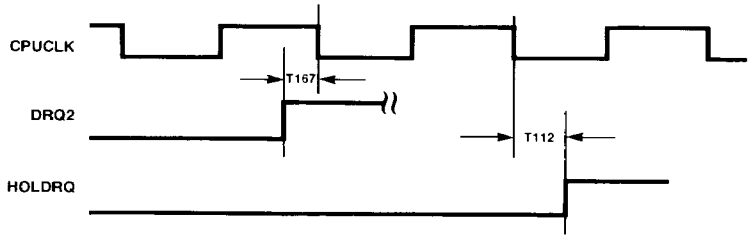


CPU I/O Write to VG-501 Registers

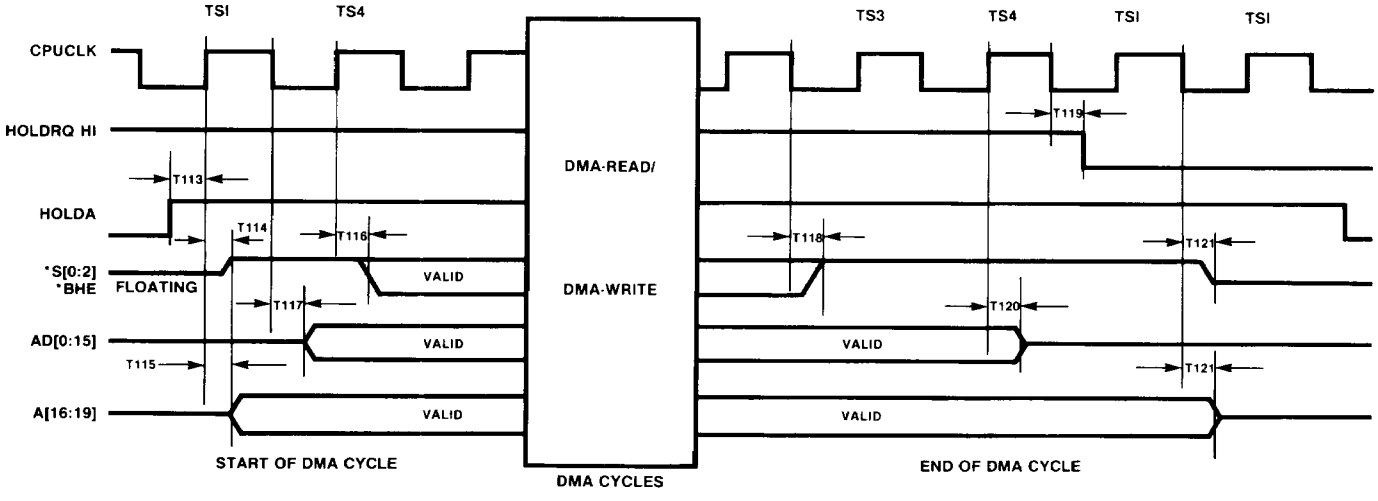


VG-501 TIMING WAVEFORMS (continued)

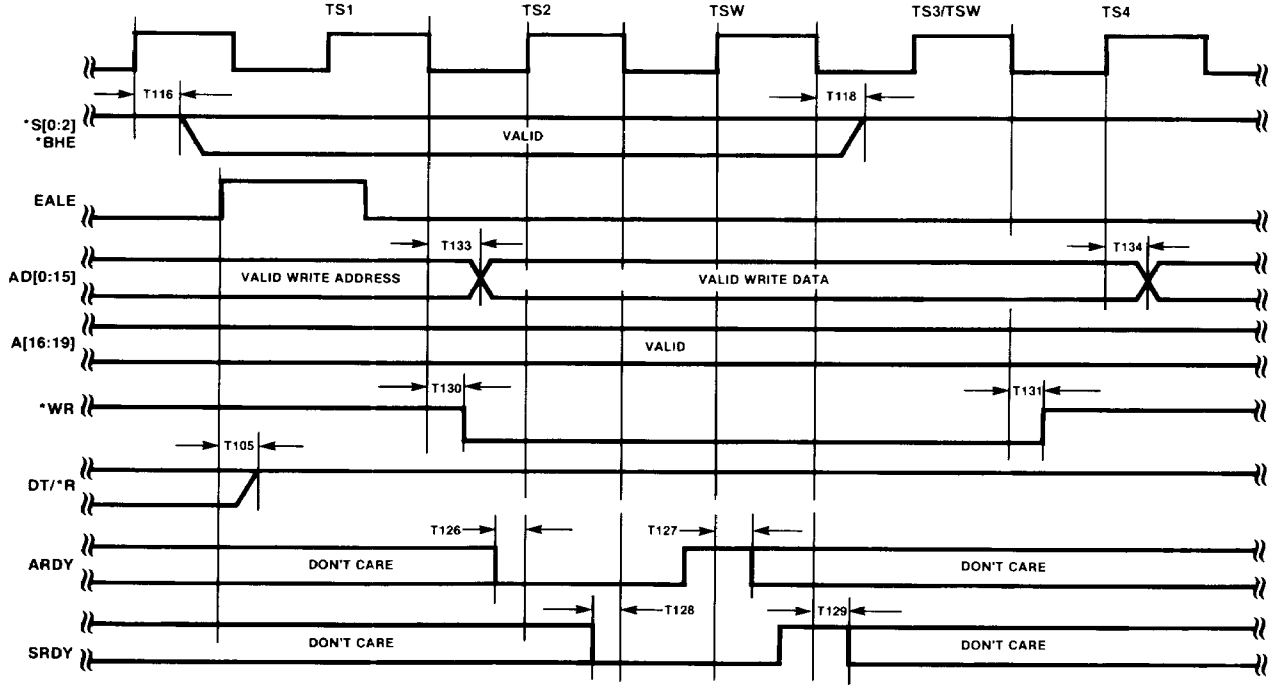
DMA Cycles



NOTE: A REFRESH CYCLE HAS THE SAME TIMING AS A DMA MEMORY READ CYCLE WITHOUT THE I/O PORTION.

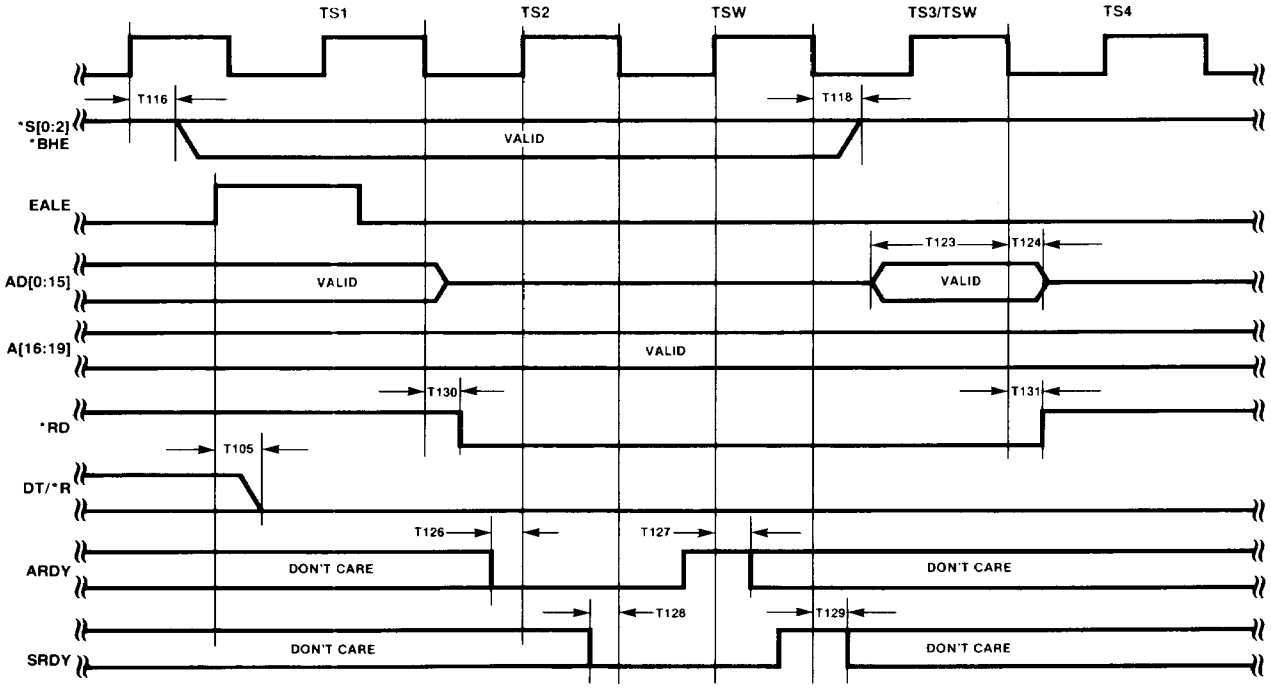


DMA-Write Cycle
1 W.S.

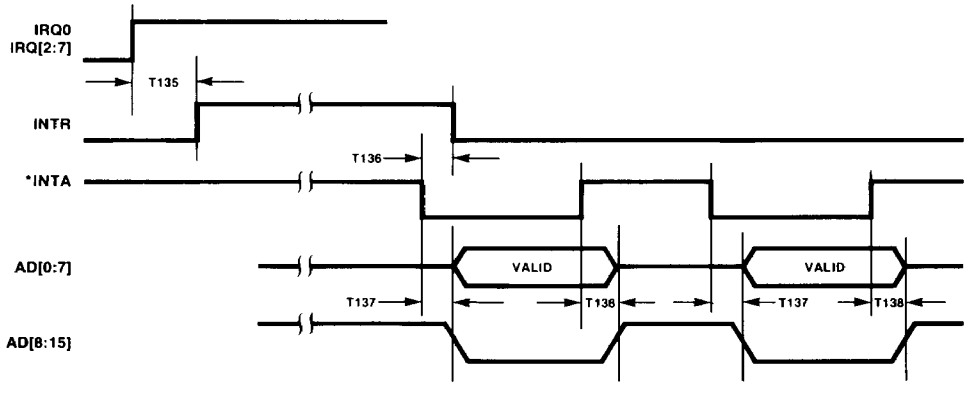


VG-501 TIMING WAVEFORMS (continued)

DMA-Read Cycle
1 W.S.

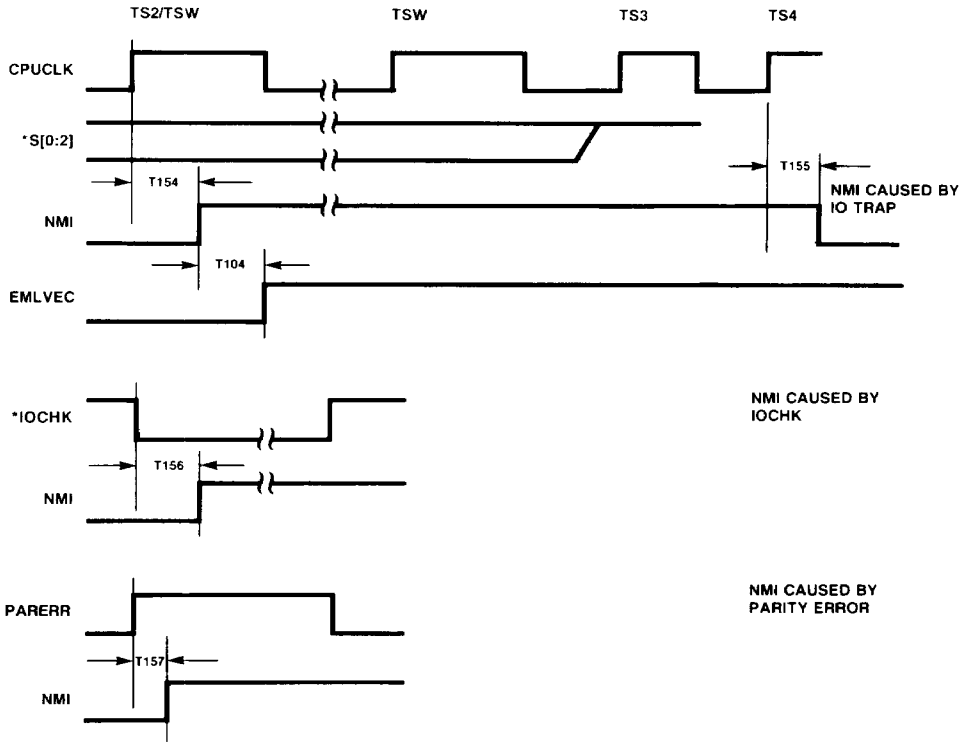


Interrupt Request and Acknowledge Cycles

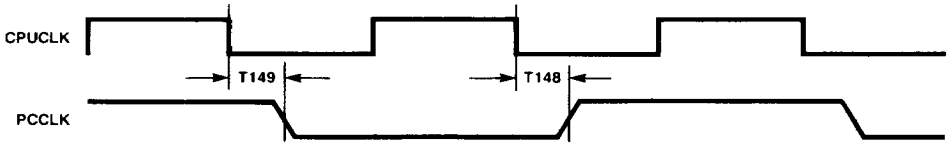


VG-501 TIMING WAVEFORMS (continued)

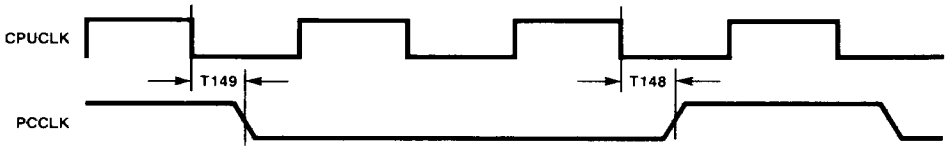
NMI Cycles



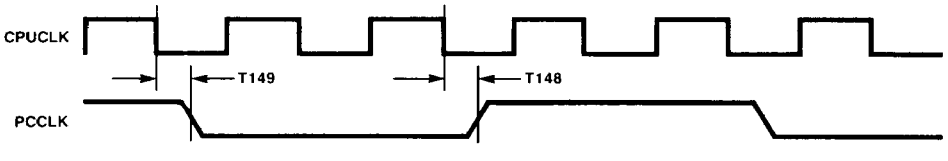
PCCLK — 1/2 CPUCLK Frequency



PCCLK — 1/3 CPUCLK Frequency

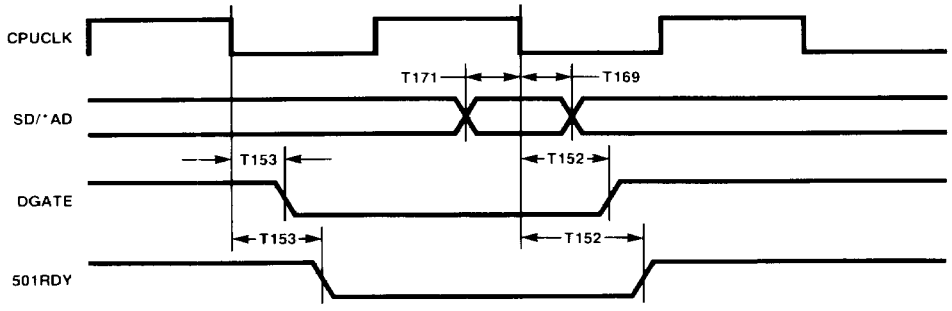


PCCLK — 1/4 CPUCLK Frequency

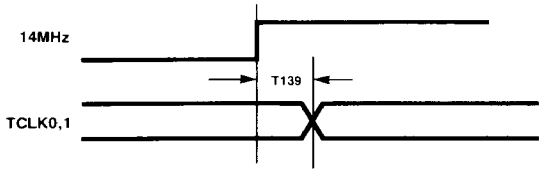


VG-501 TIMING WAVEFORMS (continued)

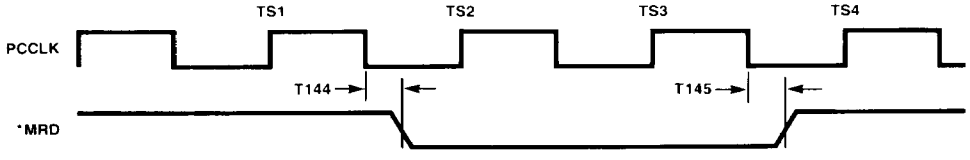
SD/*AD, DGATE and 501RDY Timing



Expansion Bus Cycle

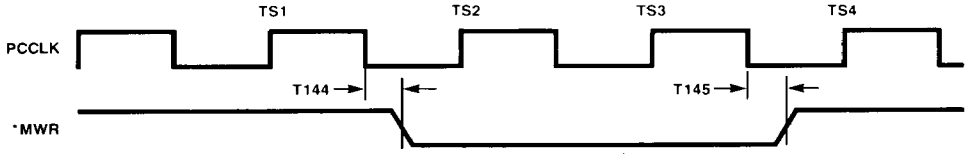


IO Channel Non-DMA Memory Read Cycle



*MRD = *IORD = *IOWR = *DACK[0:3] = 1 AEN = TC = 0

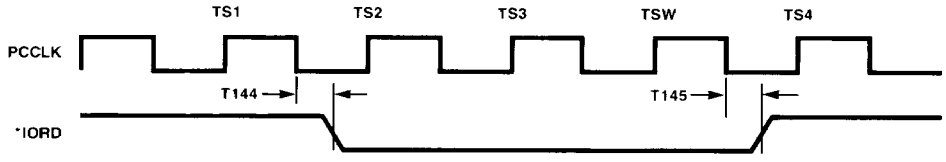
IO Channel Non-DMA Memory Write Cycle



*MWR = *IORD = *IOWR = *DACK[0:3] = 1 AEN = TC = 0

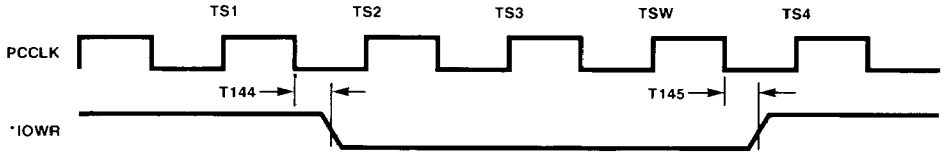
VG-501 TIMING WAVEFORMS (continued)

IO Channel Non-DMA IO Read Cycle



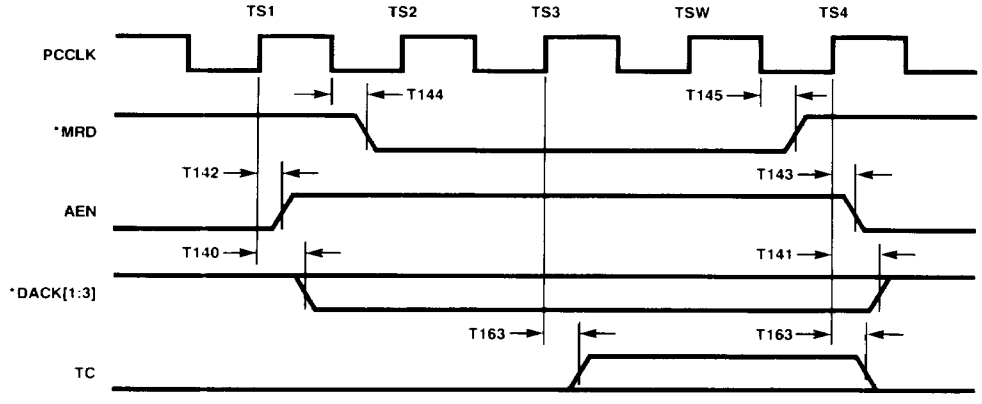
*MRD = *MWR = *IOWR = *DACK[0:3] = 1 AEN = TC = 0

IO Channel Non-DMA IO Write Cycle



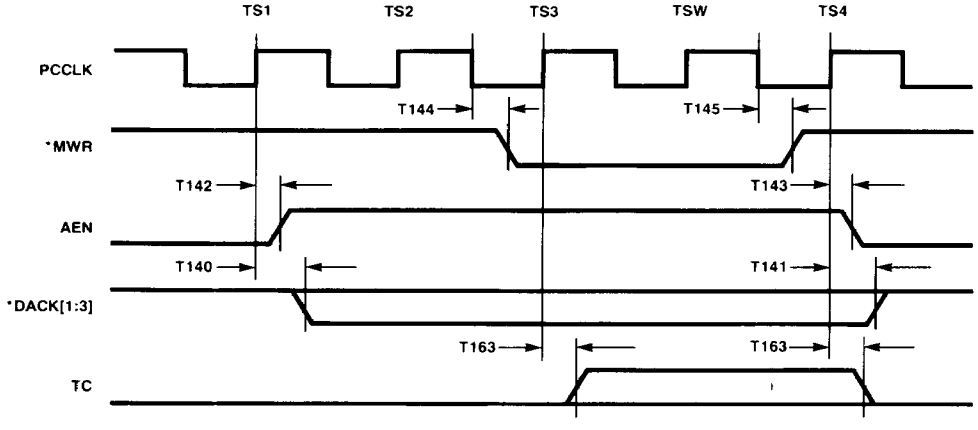
*MRD = *MWR = *IORD = *DACK[0:3] = 1 AEN = TC = 0

IO Channel DMA Memory Read Cycle



*MWR = *IORD = *IOWR = *DACK0 = 1

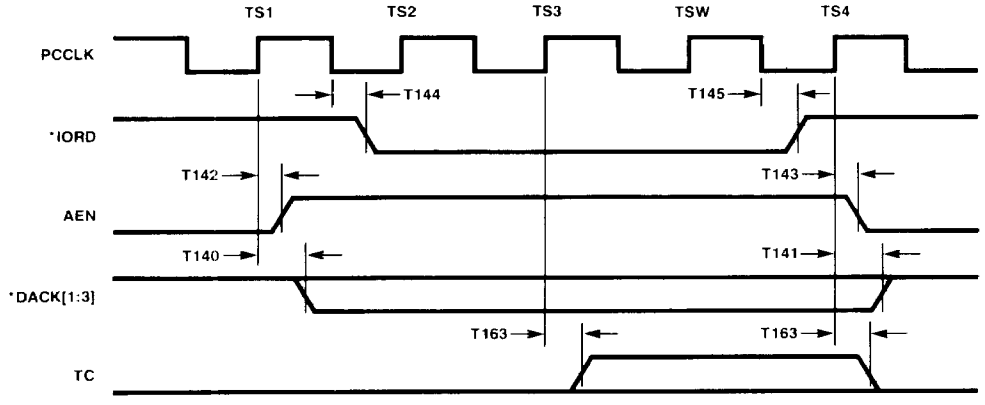
IO Channel DMA Memory Write Cycle



*MRD = *IORD = *IOWR = *DACK0 = 1

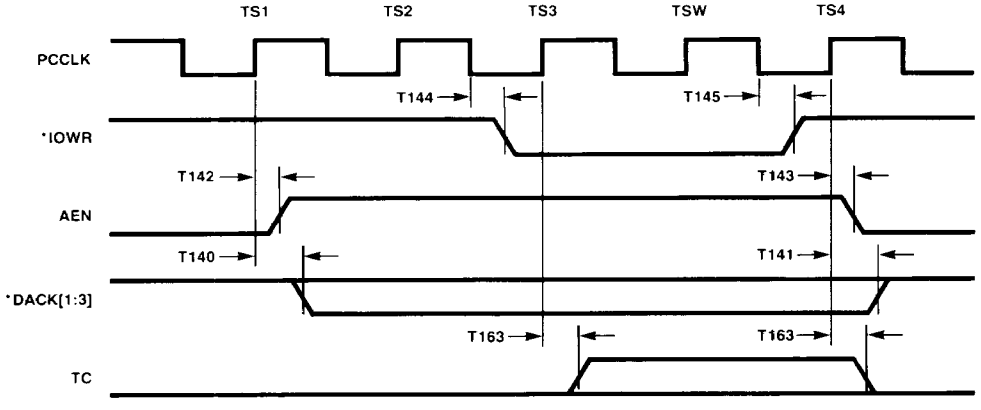
VG-501 TIMING WAVEFORMS (continued)

IO Channel DMA IO Read Cycle

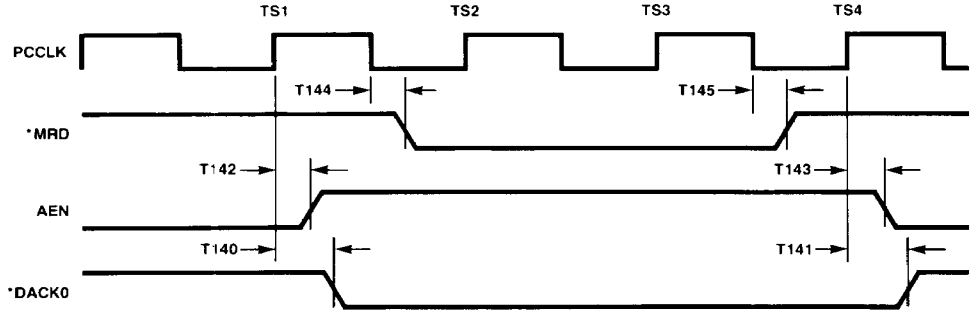


*MRD = *MWR = *IOWR = *DACK0 = 1

IO Channel DMA IO Write Cycle

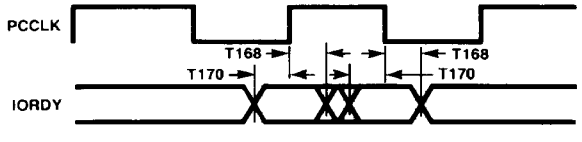


IO Channel Refresh Cycle



*MWR = *IORD = *IOWR = *DACK[1:3] = 1 TC = 0

IORDY Timing



VG-502 TIMING CHARACTERISTICS

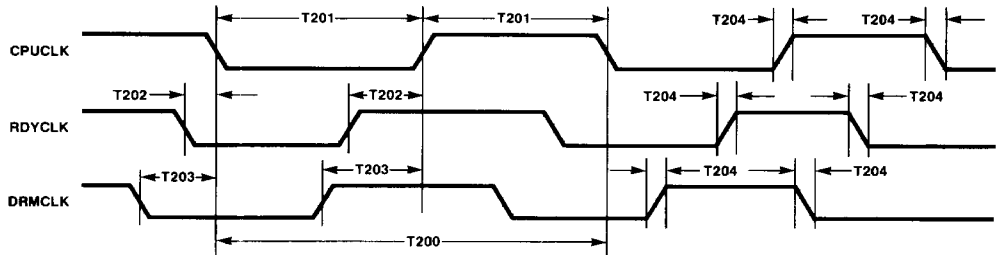
Parameter	No.	Limits Min	Limits Max	Unit
CPUCLK period	T200	62.5		ns
CPUCLK phase	T201	26		ns
RDYCLK to CPUCLK	T202	0	20	ns
DRMCLK to CPUCLK	T203	0	20	ns
CPUCLK, RDYCLK, DRMCLK risetime, falltime	T204		8	ns
*S[2:0] ↓ to CPUCLK ↑	T205	31		ns
*S[2:0] ↑ to CPUCLK ↓	T206	32		ns
CPUCLK ↑ to *BHE invalid	T207	5		ns
CPUCLK ↓ to A[19:16] invalid	T208	0		ns
AD[15:0] address valid to CPUCLK ↑	T209	0		ns
Write data valid to CPUCLK ↓	T210	50		ns
CPUCLK ↓ to write data invalid	T211	25		ns
CPUCLK ↓ to *RD valid	T212	5	31	ns
DRAM read data valid to CPUCLK ↓	T213	10		ns
PAR0:1 valid to CPUCLK	T214	2		ns
*RD ↑ to DRAM read data invalid	T215	0		ns
CPUCLK ↓ to DRAM write data valid	T216		50	ns
EXT[M,IO] valid to CPUCLK ↓	T217	30		ns
SD/*AD valid to CPUCLK ↓	T218	20		ns
DGATE valid to CPUCLK ↓	T219	22		ns
SD valid to CPUCLK ↓	T220	20		ns
CPUCLK ↓ to SD invalid	T221	15		ns
501RDY valid to RDYCLK ↓	T222	10		ns
CPUCLK ↓ to DGATE invalid	T223	5		ns
RDYCLK ↓ to 501RDY invalid	T224	2		ns
CPUCLK ↓ to read data valid	T230		53	ns
*RD ↑ to read data Hi-Z	T231	0	22	ns
Address valid to *ROM valid	T232		55	ns
CPUCLK ↓ to *ROM invalid	T233	0		ns
DRMCLK ↓ to MA column, MA refresh row valid	T234		36	ns
DRMCLK ↓ to *RAS ↓ (refresh)	T235		29	ns
DRMCLK ↓ to *RAS ↑	T236		26	ns
DRMCLK ↑ to MA address invalid	T237	0		ns
MA row valid to *RAS ↓ (refresh)	T238	T201-25		ns
Address valid to MA row valid	T239		31	ns

VG-502 TIMING CHARACTERISTICS (continued)

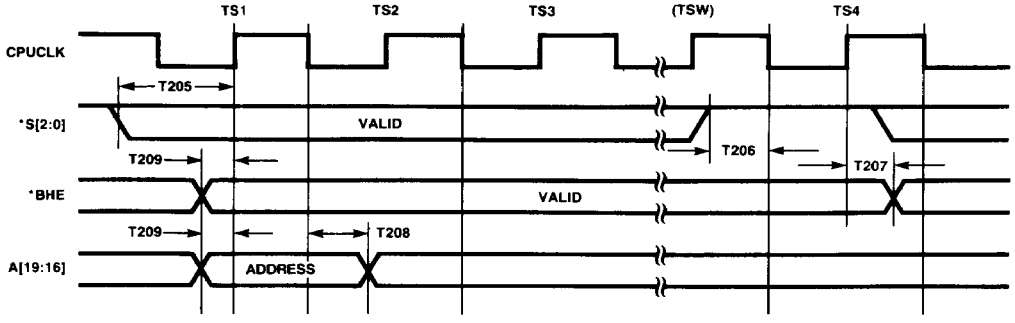
Parameter	No.	Limits Min	Limits Max	Unit
MA row valid to *RAS ↓	T240	T201-25		ns
RAS ↓ to MA row invalid	T241	T201-10		ns
DRMCLK ↓ to *RAS ↓	T242		24	ns
DRMCLK ↓ to *CAS ↓ (read)	T243		26	ns
DRMCLK ↓ to *CAS ↓ (read) (with COUT=20 pF)	T243		22	ns
*RD ↑ to *CAS ↑ (read)	T244	0	23	ns
MA column valid to *CAS ↓ (read)	T245	T201-25		ns
DRMCLK ↓ to *BUFAD ↑ (read)	T246		34	ns
*RD ↑ to *BUFAD ↑ (read)	T247	0	25	ns
CPUCLK ↓ to PARERR valid	T248		31	ns
DRMCLK ↓ to *DWR ↓	T249		29	ns
DRMCLK ↓ to *DWR ↑	T250		31	ns
MA column valid to *CAS ↓ (write)	T251	T201-25		ns
*CAS ↓ to *RAS ↑ (write)	T252	T200-T203-10		ns
Address valid to *BUFAD ↓ (write)	T253		45	ns
DRMCLK ↓ to *BUFAD ↓ (write)	T254		37	ns
CPUCLK ↓ to *BUFAD ↑ (write)	T255	0	40	ns
CPUCLK ↓ to *CAS ↑ (write)	T256		35	ns
CPUCLK ↓ to *CAS ↑ (write)	T257		35	ns
Write data valid to PAR valid	T258		40	ns
CPUCLK ↓ to PAR Hi-Z	T259	0	26	ns
CPUCLK ↓ to PAR driven	T260	0		ns
PAR valid to *CAS ↓	T261	0		ns
Address valid to SA valid	T262		40	ns
CPUCLK ↓ to SA invalid	T263	0		ns
SD valid to AD data valid	T265		37	ns
SD/*AD ↑ to AD data valid	T266		60	ns
CPUCLK ↓ to SD valid (write)	T267		37	ns
CPUCLK ↓ to SD Hi-Z (write)	T268	0		ns
CPUCLK ↓ to *BUFSD valid	T269		37	ns
EXT[M, IO] valid to *BUFSD valid	T270		37	ns
SD/*AD ↑ to *BUFSD valid	T271		55	ns
Address valid to SD/*AD valid	T272		42	ns
CPUCLK ↓ to SD/*AD invalid	T273	0		ns
CPUCLK ↓ to SA[0] ↑	T274		34	ns
Address valid to SRDY ↓	T275		75	ns
CPUCLK ↓ to SRDY valid	T276		45	ns
RDYCLK ↓ to ARDY valid	T277		21	ns

VG-502 TIMING WAVEFORMS

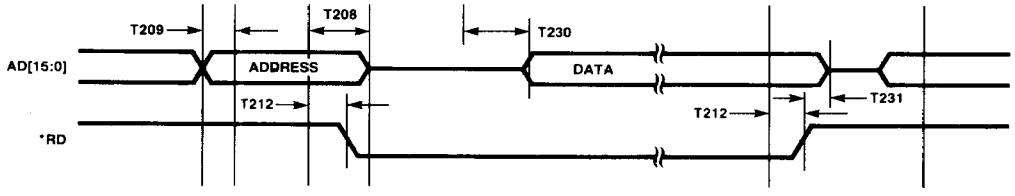
Clock Specifications



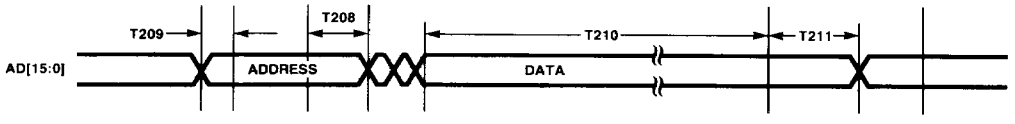
Basic Cycle



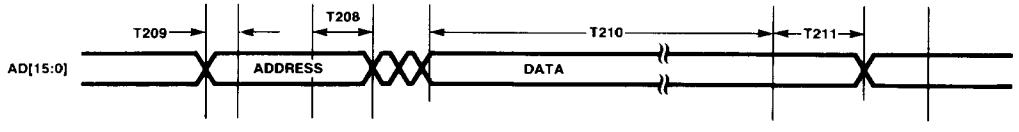
VG-502 IO Read Cycle



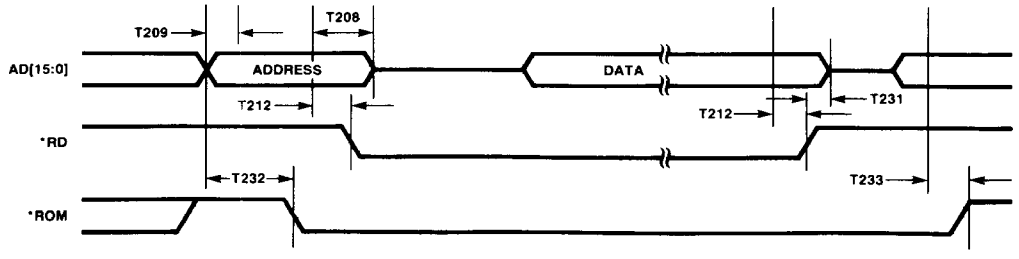
VG-502 IO Write Cycle



VG-501 IO Write Cycle

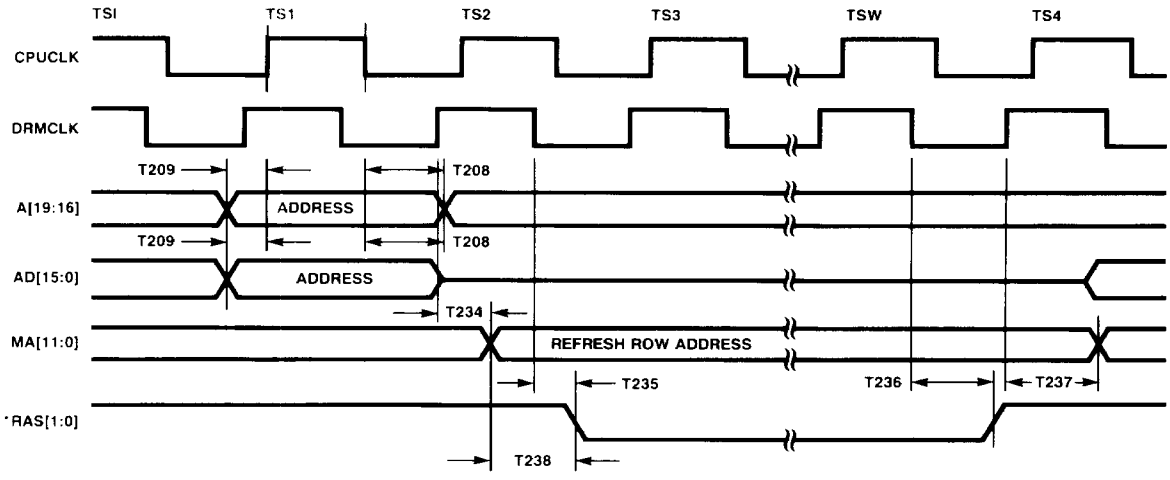


ROM Read Cycle

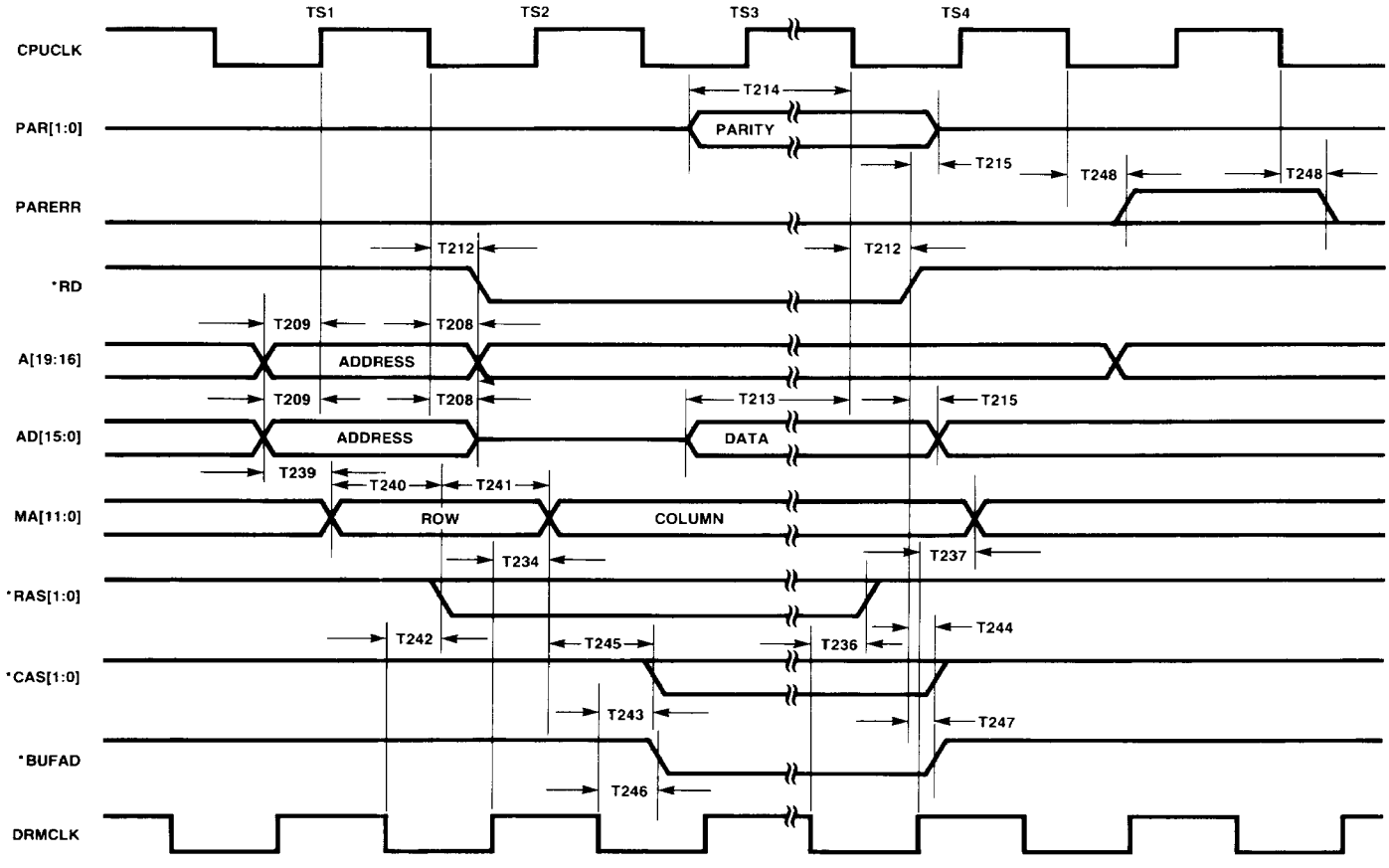


VG-502 TIMING WAVEFORMS (continued)

DRAM Refresh Cycle

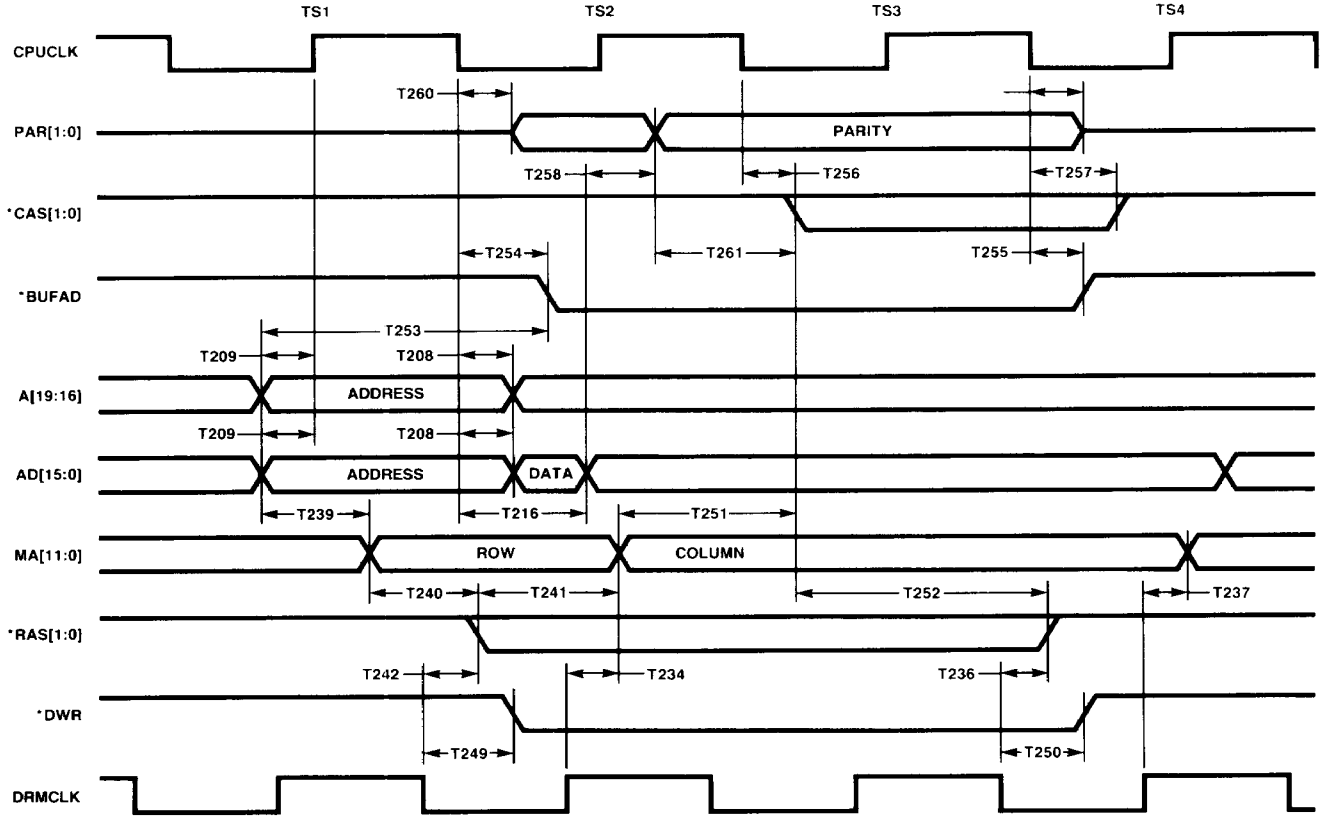


DRAM Read Cycle



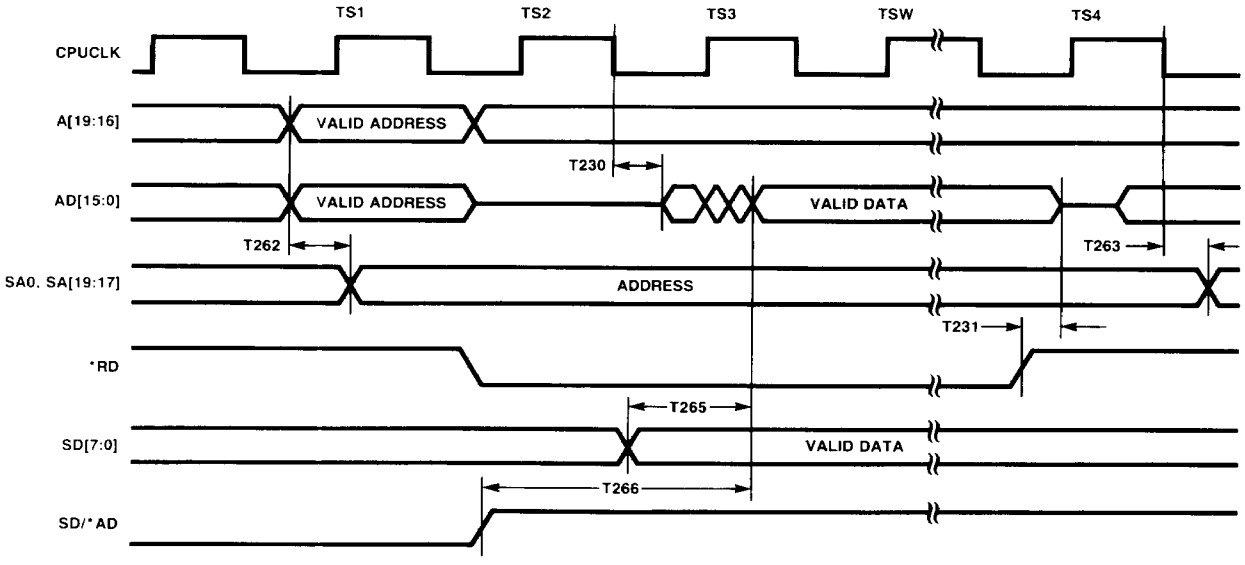
VG-502 TIMING WAVEFORMS (continued)

DRAM Write Cycle

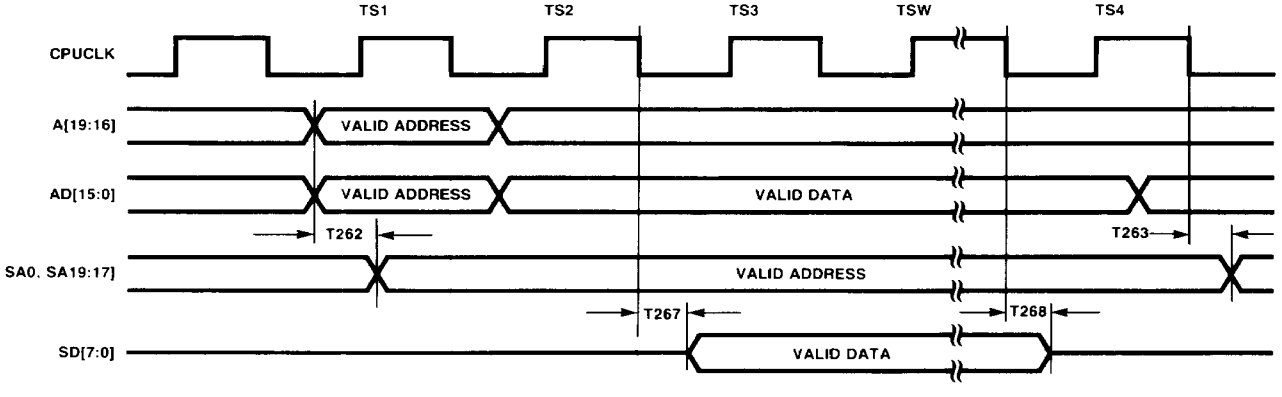


VG-502 TIMING WAVEFORMS (continued)

SD Bus Device Read Cycle

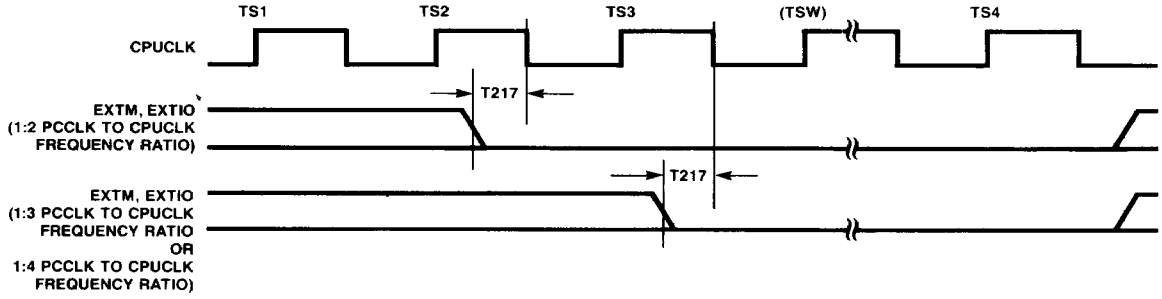


SD Bus Device Write Cycle

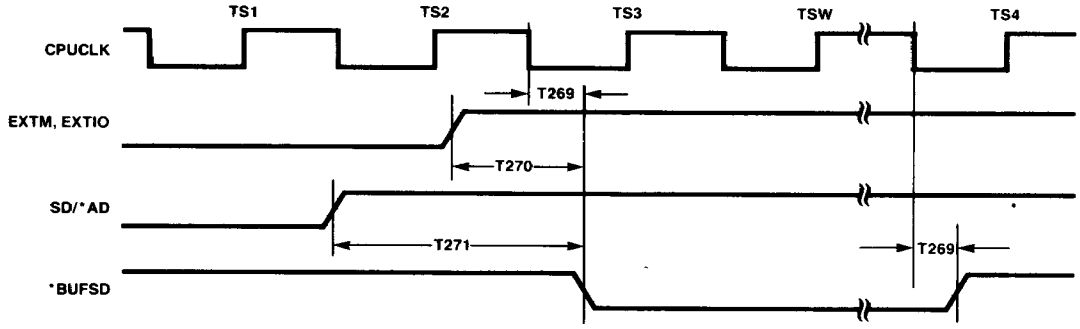


VG-502 TIMING WAVEFORMS (continued)

Internal SD Bus Device Cycle

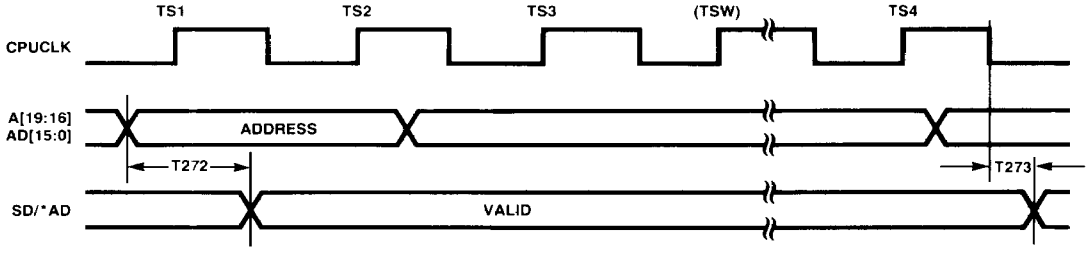


External SD Bus Device Cycle

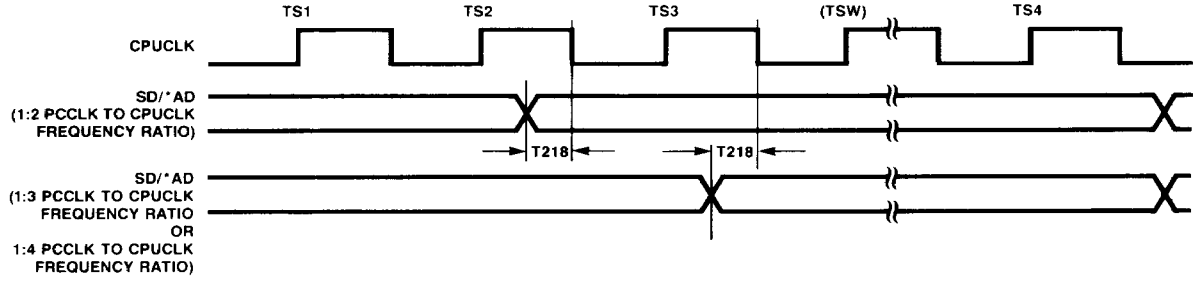


VG-502 TIMING WAVEFORMS (continued)

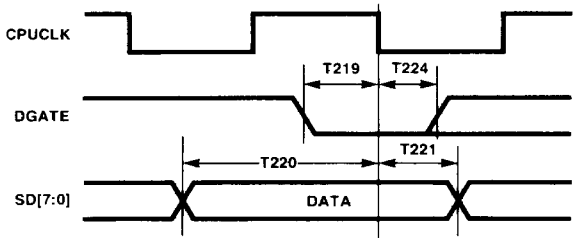
SD/*AD Output



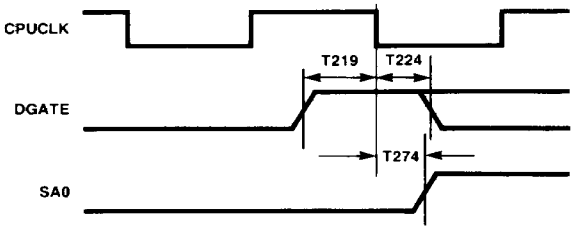
SD/*AD Input



SD Bus Data Latching (Read Cycle)

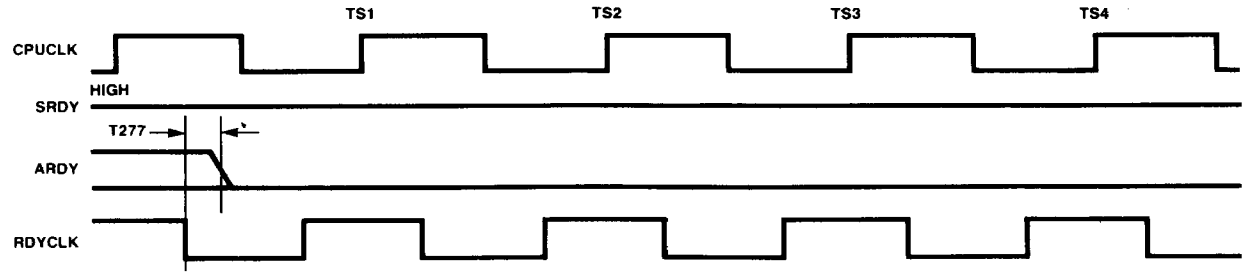


SA0 Double Cycle Control

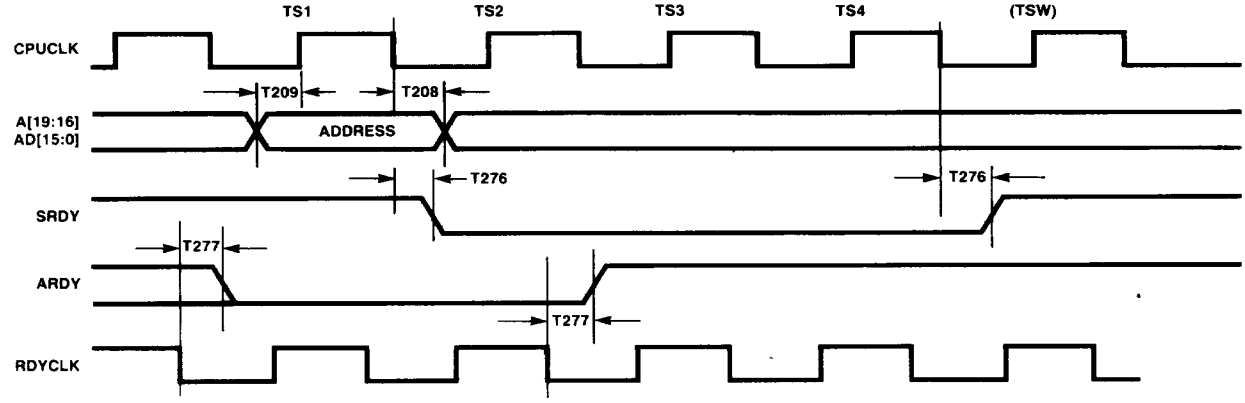


VG-502 TIMING WAVEFORMS (continued)

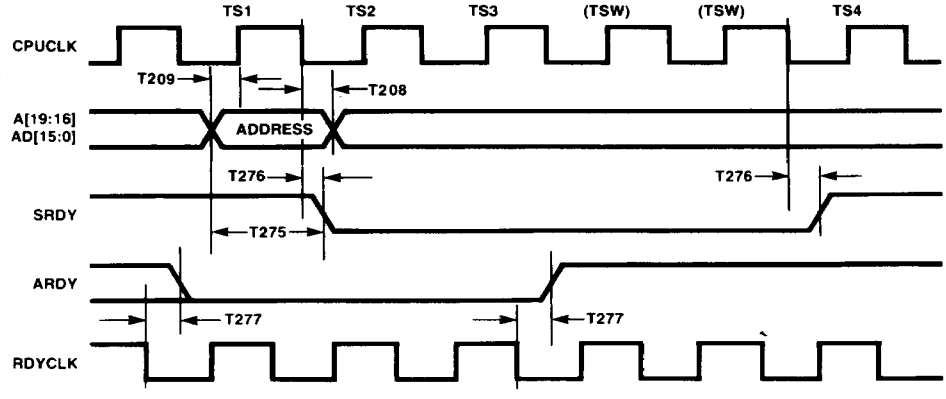
Zero Wait State Cycle



One Wait State Cycle

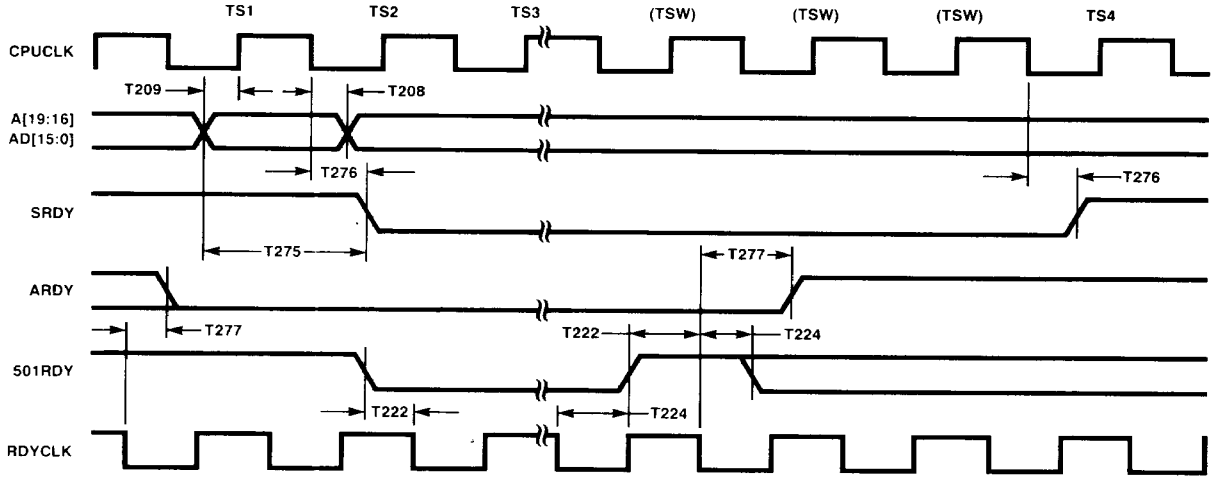


Two Wait State Cycle

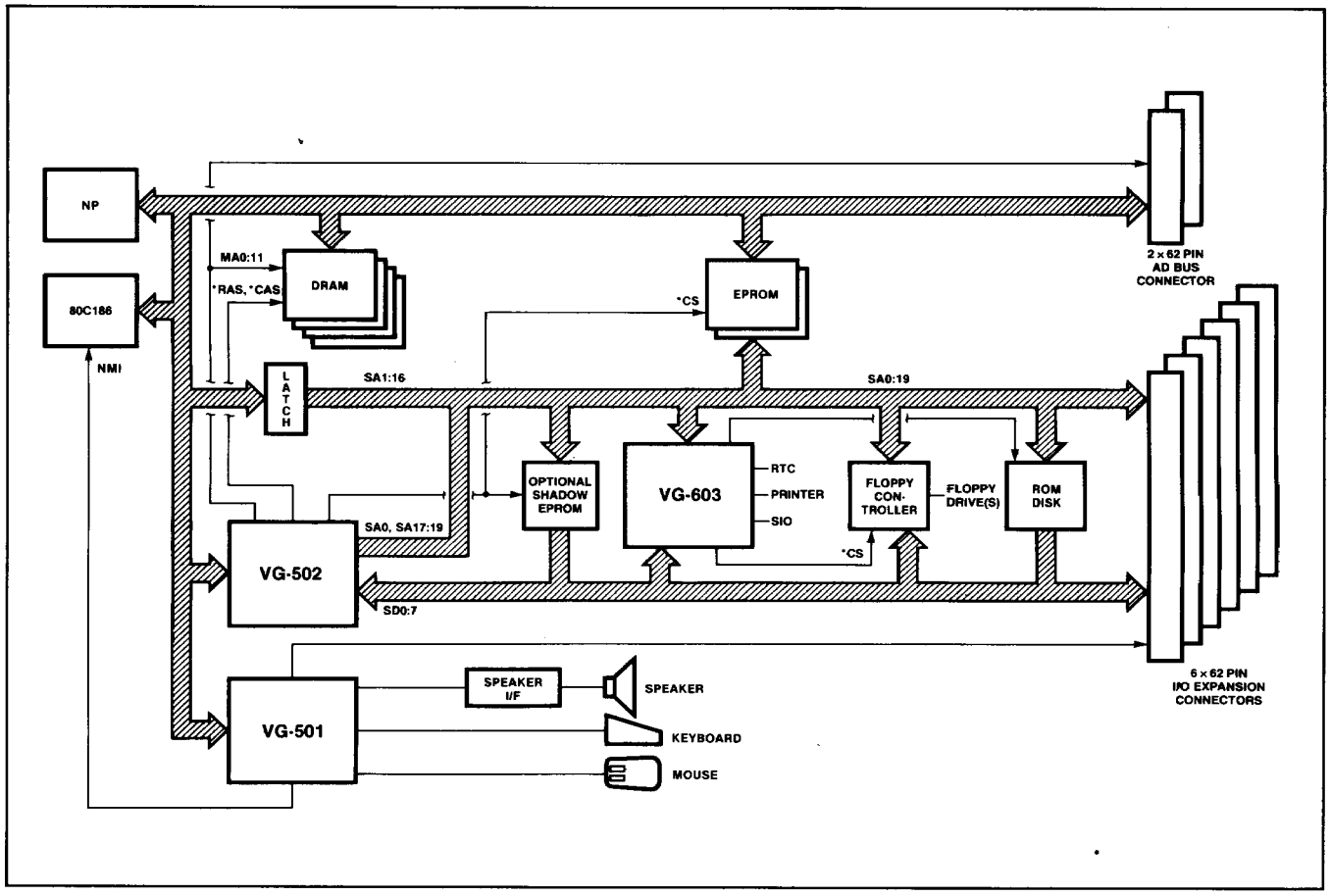


VG-502 TIMING WAVEFORMS (continued)

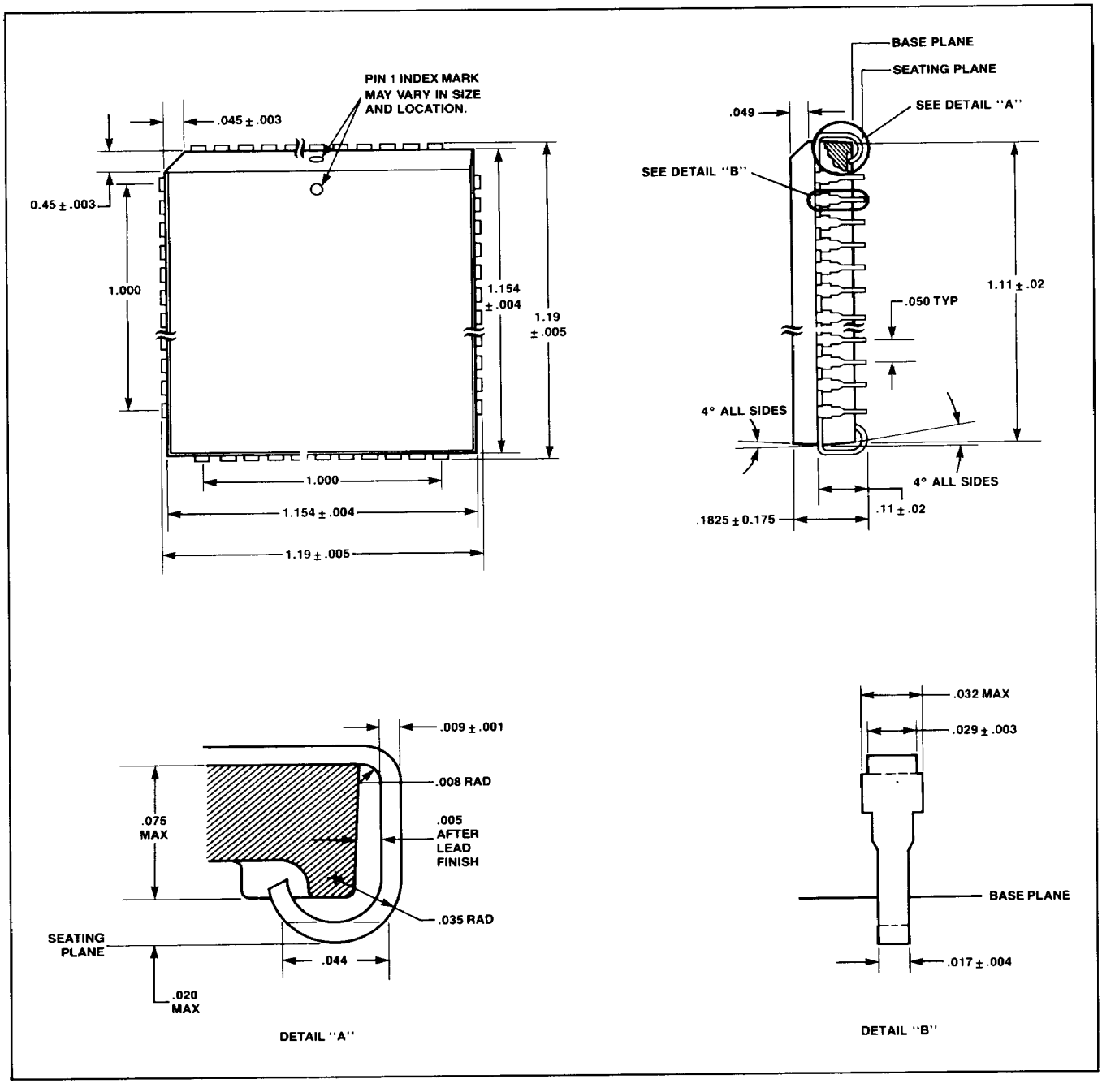
501RDY Controlled Wait State Cycle



SAMPLE APPLICATION



VG-501/502 PHYSICAL DIMENSIONS



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