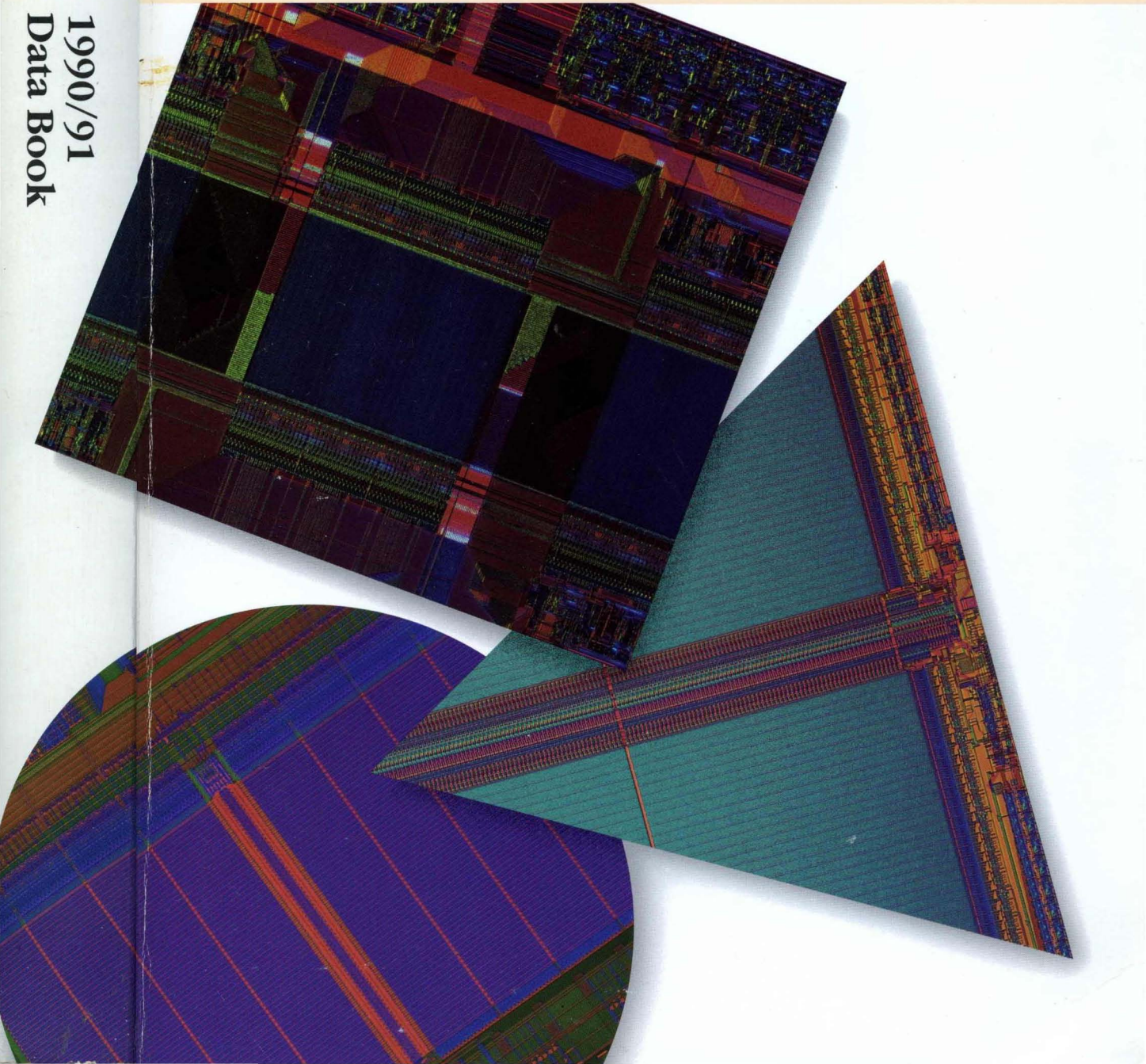
1990/91 Data Book

1990/91
Data Book



Atmel Corporation
Integrated Circuit Data Book

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Atmel Corporation designs, manufactures and markets high quality and high performance CMOS memory, logic and analog integrated circuits. Founded in 1984, the Company serves the manufacturers of computation, communications and instrumentation equipment in military and commercial environments.

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We thank you for considering Atmel semiconductors.

Section 1

Section 2

CMOS E^2PROMS

Section 3

CMOS PEROMs (Flash)

Section 4

CMOS EPROMs

TABLE OF CONTENTS

Section 10

Application Notes

Section 11

Quality and Reliability

Section 12

Military

Section 13

Die Products

Section 14

Package Outlines

CONTENTS

Section 1

Alpha-Numeric Product Selection Guide and Index

CMOS E^2PROMs

Part Number	Organization	Description	Page No.
AT28C010	128K x 8	1MBit E^2PROM with 128 Byte Page	2-125
AT28C04	512 x 8	4K E^2PROM	2-41
AT28C1024	64K x 16	1MBit E^2PROM	2-115
AT28C16	2K x 8	16K E^2PROM	2-51
AT28C16E	2K x 8	16K E^2PROM with Extended Endurance	2-51
AT28C16F	2K x 8	16K E^2PROM with Fast Write	2-51
AT28C17	2K x 8	16K E^2PROM	2-61
AT28C256	32K x 8	256K E^2PROM	2-93
AT28C256F	32K x 8	256K E^2PROM with Fast Write	2-93
AT28C64	8K x 8	64K E^2PROM	2-71
AT28C64E	8K x 8	64K E^2PROM with Extended Endurance	2-71
AT28C64F	8K x 8	64K E^2PROM with Fast Write	2-71
AT28C64X	8K x 8	64K E^2PROM without Ready-$\overline{\text{Busy}}$	2-71
AT28HC16	2K x 8	High Speed, 16K CMOS E^2PROM	2-3
AT28HC16L	2K x 8	High Speed, Low Power, 16K E^2PROM	2-3
AT28HC256	32K x 8	High Speed, 256K Paged E^2PROM	2-27
AT28HC256F	32K x 8	High Speed, 256K E^2PROM with Fast Write	2-27
AT28HC256L	32K x 8	High Speed, Low Power, 256K E^2PROM	2-27
AT28HC64	8K x 8	High Speed, 64K Paged E^2PROM	2-15
AT28HC64L	8K x 8	High Speed, Low Power, 64K E^2PROM	2-15
AT28MC010	128K x 8	1MBit Module E^2PROM	2-105
AT28PC64	8K x 8	64K E^2PROM with Page Mode Write	2-83

CMOS PEROMs

Part Number	Organization	Description	Page No.
AT29C010	128K x 8	1MBit 5-Volt Reprogrammable ROM	3-23
AT29C256	32K x 8	256K 5-Volt Reprogrammable ROM	3-3
AT29C257	32K x 8	256K 5-Volt Reprogrammable ROM	3-13

CMOS EPROMs

Part Number	Organization	Description	Page No.
AT27C010	128K x 8	1MBit EPROM	4-81
AT27C010L	128K x 8	Low Power, 1MBit EPROM	4-81
AT27C011	8 x 16K x 8	Paged, 1MBit EPROM	4-91
AT27C040	512K x 8	4MBit EPROM	4-111
AT27C1024	64K x 16	1MBit EPROM	4-101
AT27C1024L	64K x 16	Low Power, 1MBit EPROM	4-101
AT27C128	16K x 8	128K EPROM	4-33
AT27C256	32K x 8	256K EPROM	4-39
AT27C256R	32K x 8	256K EPROM	4-47
AT27C512	64K x 8	512K EPROM	4-55
AT27C512R	64K x 8	512K EPROM	4-63

Alpha-Numeric Product Selection Guide and Index *(continued)*

CMOS EPROMs *(continued)*

Part Number	Organization	Description	Page No.
AT27C513R	4x16Kx8	Paged, 512K EPROM	4-71
AT27HC1024	64Kx8	High Speed, 1MBit EPROM	4-29
AT27HC256	32Kx8	High Speed, 256K EPROM	4-15
AT27HC256L	32Kx8	High Speed, Low Power, 256K EPROM	4-15
AT27HC256R	32Kx8	High Speed, 256K EPROM	4-25
AT27HC256RL	32Kx8	High Speed, Low Power, 256K EPROM	4-25
AT27HC64	8Kx8	High Speed, 64K EPROM	4-3
AT27HC64L	8Kx8	High Speed, Low Power, 64K PROM	4-3
AT27HC64R	8Kx8	High Speed, 64K EPROM	4-11
AT27HC64RL	8Kx8	High Speed, Low Power, 64K EPROM	4-11

High-Speed CMOS PROMs

Part Number	Organization	Description	Page No.
AT28HC191	2Kx8	High Speed, 16K Reprogrammable [E^2] PROM	5-3
AT28HC191L	2Kx8	Low Power, 16K Reprogrammable [E^2] PROM	5-3
AT28HC291	2Kx8	High Speed, 16 Reprogrammable [E^2] PROM	5-11
AT28HC291L	2Kx8	Low Power, 16K Reprogrammable [E^2] PROM	5-11
AT27HC641	8Kx8	High Speed, 64K Reprogrammable [UV] PROM	5-19
AT27HC641R	8Kx8	High Speed, 64K Reprogrammable [UV] PROM	5-27
AT27HC642	8Kx8	High Speed, 64K Reprogrammable [UV] PROM	5-19
AT27HC642R	8Kx8	High Speed, 64K Reprogrammable [UV] PROM	5-27

CMOS SRAMs

Part Number	Organization	Description	Page No.
AT38256	32Kx8	256K High Speed SRAM	6-19
AT3864L	8Kx8	64K SRAM	6-3
AT3864L-15DMB	8Kx8	64K SRAM, Full Military Temperature	6-11

CMOS EPLDs

Part Number	Gates	Description	Page No.
AT22V10	500 Gates	EPLD	7-3
AT22V10L	500 Gates	Low Power EPLD	7-3
ATV2500	2500 Gates	EPLD	7-39
ATV2500H	2500 Gates	High Speed EPLD	7-39
ATV5000	5000 Gates	EPLD	7-57
ATV750	750 Gates	EPLD	7-19
ATV750L	750 Gates	Low Power EPLD	7-19

Alpha-Numeric Product Selection Guide and Index *(continued)*

CMOS Gate Arrays

Part Number	Gates	Description	Page No.
ATL4	4K	1-Micron CMOS Gate Array	8-3
ATL10	10K	1-Micron CMOS Gate Array	8-3
ATL20	22K	1-Micron CMOS Gate Array	8-3
ATL60	57K	1-Micron CMOS Gate Array	8-3
ATL130	131K	1-Micron CMOS Gate Array	8-3
ATL260	257K	1-Micron CMOS Gate Array	8-3

CMOS Analog

Part Number	Frequency	Description	Page No.
AT76C10	4KHz	Programmable, Phone Line Equalizer	9-3
AT76C10E	4KHz	Programmable, Phone Line Equalizer with on board E^2PROM	9-11
AT76C120	100KHz	Dual Channel 16/18-Bit A/D Converters	9-19
AT76C171	50MHz	Triple, 6-Bit Color Palette DAC	9-27
AT76C176	65MHz	Triple, 6-Bit Color Palette DAC	9-39
AT76C176A	50-100MHz	Triple, 6-Bit Color Palette DAC with Power-Down	9-51

Product Summary and Index

CMOS E^2PROMs

Part No.	Organization	Speeds	Description	Page No.
AT28C04	512x8	150-450ns	4K E^2PROM	2-41
AT28C16	2Kx8	150-450ns	16K E^2PROM	2-51
AT28C16E	2Kx8	150-450ns	16K E^2PROM with Extended Endurance	2-51
AT28C16F	2Kx8	150-450ns	16K E^2PROM with Fast Write	2-51
AT28C17	2Kx8	150-450ns	16K E^2PROM	2-61
AT28C64	8Kx8	150-450ns	64K E^2PROM	2-71
AT28C64E	8Kx8	150-450ns	64K E^2PROM with Extended Endurance	2-71
AT28C64F	8Kx8	150-450ns	64K E^2PROM with Fast Write	2-71
AT28C64X	8Kx8	150-450ns	64K E^2PROM without Ready-$\overline{\text{Busy}}$	2-71
AT28PC64	8Kx8	150-350ns	64K E^2PROM with Page Mode Write	2-83
AT28C256	32Kx8	150-350ns	256K E^2PROM	2-93
AT28C256F	32Kx8	150-350ns	256K E^2PROM with Fast Write	2-93

High-Speed CMOS E^2PROMs

Part No.	Organization	Speeds	Description	Page No.
AT28HC16	2Kx8	45-90ns	16K E^2PROM	2-3
AT28HC16L	2Kx8	55-90ns	Low Power, 16K E^2PROM	2-3
AT28HC64	8Kx8	55-120ns	64K Paged E^2PROM	2-15
AT28HC64L	8Kx8	70-120ns	Low Power, 64K E^2PROM	2-15
AT28HC256	32Kx8	70-120ns	256K Paged E^2PROM	2-27
AT28HC256F	32Kx8	70-120ns	256K E^2PROM with Fast Write	2-27
AT28HC256L	32Kx8	90-120ns	Low Power, 256K E^2PROM	2-27
AT28C1024	64Kx16	150-250ns	1MBit E^2PROM	2-115
AT28MC010	128Kx8	120-250ns	1MBit Module E^2PROM	2-105
AT28C010	128Kx8	120-250ns	1MBit E^2PROM	2-125

CMOS PEROMs (5-Volt Only)

Part No.	Organization	Speeds	Description	Page No.
AT29C256	32Kx8	150-250ns	256K 5-Volt Reprogrammable ROM	3-3
AT29C257	32Kx8	150-250ns	256K 5-Volt Reprogrammable ROM	3-13
AT29C010	128Kx8	150-250ns	1MBit 5-Volt Reprogrammable ROM	3-23

CMOS EPROMs

Part No.	Organization	Speeds	Description	Page No.
AT27C040	512Kx8	120-250ns	4 MBit EPROM	4-111
AT27C128	16Kx8	120-250ns	128K EPROM	4-33
AT27C256	32Kx8	120-350ns	256K EPROM	4-39
AT27C256R	32Kx8	90-250ns	256K EPROM	4-47
AT27C512	64Kx8	120-250ns	512K EPROM	4-55
AT27C512R	64Kx8	100-250ns	512K EPROM	4-63
AT27C513R	4x16Kx8	150-250ns	512K Paged EPROM	4-71
AT27C010	128Kx8	120-250ns	1MBit EPROM	4-81
AT27C010L	128Kx8	120-250ns	Low Power, 1MBit EPROM	4-81
AT27C011	8x16Kx8	150-250ns	1MBit Paged EPROM	4-91
AT27C1024	64Kx16	120-250ns	1MBit EPROM	4-101
AT27C1024L	64Kx16	120-250ns	Low Power, 1MBit EPROM	4-101

High-Speed CMOS EPROMs

Part No.	Organization	Speeds	Description	Page No.
AT27HC64	8Kx8	45-90ns	64K EPROM	4-3
AT27HC64L	8Kx8	55-90ns	Low Power, 64K EPROM	4-3
AT27HC64R	8Kx8	45-90ns	Low Power, 64K EPROM	4-11
AT27HC64RL	8Kx8	55-90ns	Low Power, 64K EPROM	4-11
AT27HC256	32Kx8	55-120ns	256K EPROM	4-15
AT27HC256L	32Kx8	70-120ns	Low Power, 256K EPROM	4-15
AT27HC256R	32Kx8	55-120ns	256 EPROM	4-25
AT27HC256RL	32Kx8	70-120ns	256 EPROM	4-25
AT27HC1024	64Kx8	55-120ns	1MBit EPROM	4-29

High-Speed CMOS PROMs

Part No.	Organization	Speeds	Description	Page No.
AT28HC191	2Kx8	35-55ns	16K [E^2] PROM	5-3
AT28HC191L	2Kx8	45-55ns	16K [E^2] PROM	5-3
AT28HC291	2Kx8	35-55ns	16K [E^2] PROM	5-11
AT28HC291L	2Kx8	45-55ns	16K [E^2] PROM	5-11
AT27HC641	8Kx8	35-90ns	64K [UV] PROM	5-19
AT27HC641R	8Kx8	35-90ns	High Speed, 64K Reprogrammable [UV] PROM	5-27
AT27HC642	8Kx8	35-90ns	64K [UV] PROM	5-19
AT27HC642R	8Kx8	35-90ns	High Speed, 64K Reprogrammable [UV] PROM	5-27

CMOS SRAMs

Part No.	Organization	Speeds	Description	Page No.
AT38256	32K x 8	20-35ns	256K High Speed SRAM	6-19
AT3864L	8K x 8	100-150ns	64K SRAM	6-3
AT3864L-15DMB	8K x 8	150ns	64K SRAM, Full Military Temperature	6-11

CMOS EPLDs

Part No.	Speeds	Description	Page No.
AT22V10	15-35ns	500 Gate EPLD	7-3
AT22V10L	15-35ns	500 Gate, Low Power EPLD	7-3
ATV750	20-40ns	750 Gate EPLD	7-19
ATV750L	20-30ns	750 Gate, Low Power EPLD	7-19
ATV2500	30-45ns	2500 Gate EPLD	7-39
ATV2500H	25-35ns	2500 Gate EPLD	7-39
ATV5000	25-35ns	5000 Gate EPLD	7-57

CMOS Gate Arrays

Part No.	Gates	Description	Page No.
ATL4	4K	1-Micron CMOS Gate Array	8-3
ATL10	10K	1-Micron CMOS Gate Array	8-3
ATL20	22K	1-Micron CMOS Gate Array	8-3
ATL60	57K	1-Micron CMOS Gate Array	8-3
ATL130	131K	1-Micron CMOS Gate Array	8-3
ATL260	257K	1-Micron CMOS Gate Array	8-3

CMOS Analog

Part No.	Frequency	Description	Page No.
AT76C10	4KHz	Programmable, Phone Line Equalizer	9-3
AT76C10E	4KHz	Programmable, Phone Line Equalizer w/ On-Board E^2PROM	9-11
AT76C171	50MHz	Triple, 6-Bit Color Palette DAC	9-27
AT76C176	66MHz	Triple, 6-Bit Color Palette DAC	9-39
AT76C176A	50-110MHz	Triple, 6-Bit Color Palette DAC, with Power-Down	9-51
AT76C120	100KHz	Dual Channel 16/18-Bit A/D Converts	9-19

CMOS E²PROM Product Selection Guide

AT28HC16 Part Number	Organization	Speed (ns)	Package D3	D6	P3	P6	W	Temp. Range	I_{CC} (mA) Active	Standby	No. of Pins DIP	Page Number
AT28HC16	2Kx8	45	•	•	•	•		C	80	60	24	2-3
	2Kx8	45	•	•	•	•		I	80	60	24	2-3
	2Kx8	55	•	•	•	•		C	80	60	24	2-3
	2Kx8	55	•	•	•	•		I	80	60	24	2-3
	2Kx8	55	•	•				M	80	60	24	2-3
	2Kx8	55	•	•				M/883	80	60	24	2-3
	2Kx8	70	•	•	•	•		C	80	60	24	2-3
	2Kx8	70	•	•	•	•		I	80	60	24	2-3
	2Kx8	70	•	•				M	80	60	24	2-3
	2Kx8	70	•	•				M/883	80	60	24	2-3
	2Kx8	90	•	•	•	•	•	C	80	60	24	2-3
	2Kx8	90	•	•	•	•		I	80	60	24	2-3
	2Kx8	90	•	•				M	80	60	24	2-3
	2Kx8	90	•	•				M/883	80	60	24	2-3

Package Type	
D3	24D3, 24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
D6	24D6, 24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P3	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
P6	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS E²PROM Product Selection Guide

AT28HC16L Part Number	Organization	Speed (ns)	Package D3	D6	P3	P6	W	Temperature Range	Icc (mA) Active	Standby	No. of Pins DIP	Page Number
AT28HC16L	2Kx8	55	•	•	•	•		C	80	0.5	24	2-3
	2Kx8	55	•	•	•	•		I	80	0.5	24	2-3
	2Kx8	55	•	•				M	80	0.5	24	2-3
	2Kx8	55	•	•				M/883	80	0.5	24	2-3
	2Kx8	70	•	•	•	•	•	C	80	0.5	24	2-3
	2Kx8	70	•	•	•	•		I	80	0.5	24	2-3
	2Kx8	70	•	•				M	80	0.5	24	2-3
	2Kx8	70	•	•				M/883	80	0.5	24	2-3
	2Kx8	90	•	•	•	•	•	C	80	0.5	24	2-3
	2Kx8	90	•	•	•	•		I	80	0.5	24	2-3
	2Kx8	90	•	•				M	80	0.5	24	2-3
	2Kx8	90	•	•				M/883	80	0.5	24	2-3

Package Type	
D3	24D3, 24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
D6	24D6, 24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P3	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
P6	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS E²PROM Product Selection Guide

AT28HC64 Part Number	Organization	Speed (ns)	Package D	J	L	P	Temp. Range	Option	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT28HC64	8Kx8	55	•		•	•	C	E	80	60	28	32	2-15
	8Kx8	55	•		•	•	I	E	80	60	28	32	2-15
	8Kx8	70	•	•	•	•	C	E	80	60	28	32	2-15
	8Kx8	70	•	•	•	•	I	E	80	60	28	32	2-15
	8Kx8	70	•		•		M	E	80	60	28	32	2-15
	8Kx8	70	•		•		M/883	E	80	60	28	32	2-15
	8Kx8	90	•	•	•	•	C	E	80	60	28	32	2-15
	8Kx8	90	•	•	•	•	I	E	80	60	28	32	2-15
	8Kx8	90	•		•		M	E	80	60	28	32	2-15
	8Kx8	90	•		•		M/883	E	80	60	28	32	2-15
	8Kx8	120	•	•	•	•	C	E	80	60	28	32	2-15
	8Kx8	120	•	•	•	•	I	E	80	60	28	32	2-15
	8Kx8	120	•		•		M	E	80	60	28	32	2-15
	8Kx8	120	•		•		M/883	E	80	60	28	32	2-15

	Package Type
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
	Options
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS E²PROM Product Selection Guide

AT28HC64L	Organi-	Speed	Package						Temp.	Option	Icc (mA)		No. of Pins		Page
Part Number	zation	(ns)	D	J	K	L	P	W	Range		Active	Standby	DIP	LCC	Number
AT28HC64L	8Kx8	70	•			•	•		C	E	80	0.1	28	32	2-15
	8Kx8	70	•			•	•		I	E	80	0.1	28	32	2-15
	8Kx8	90	•	•		•	•		C	E	80	0.1	28	32	2-15
	8Kx8	90	•	•		•	•		I	E	80	0.1	28	32	2-15
	8Kx8	90	•			•			M	E	80	0.2	28	32	2-15
	8Kx8	90	•			•			M/883	E	80	0.2	28	32	2-15
	8Kx8	120	•	•		•	•	•	C	E	80	0.1	28	32	2-15
	8Kx8	120	•	•		•	•		I	E	80	0.1	28	32	2-15
	8Kx8	120	•			•			M	E	80	0.2	28	32	2-15
	8Kx8	120	•			•			M/883	E	80	0.2	28	32	2-15
SMD Number															
5962-8751412	8Kx8	70	•		•	•			M/883		80	0.2	28	32	2-15
5962-8751411	8Kx8	90	•		•	•			M/883		80	0.2	28	32	2-15
5962-8751410	8Kx8	120	•		•	•			M/883		80	0.2	28	32	2-15

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
K	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS E²PROM Product Selection Guide

AT28HC256 Part Number	Organization	Speed (ns)	Package D	F	J	L	P	U	Temp. Range	Option	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT28HC256	32Kx8	70	•			•	•		C	E,F	80	60	28	32	2-27
	32Kx8	70	•			•	•		I	E,F	80	60	28	32	2-27
	32Kx8	90	•	•	•	•	•	•	C	E,F	80	60	28	32	2-27
	32Kx8	90	•	•	•	•	•	•	I	E,F	80	60	28	32	2-27
	32Kx8	90	•	•		•		•	M	E,F	80	60	28	32	2-27
	32Kx8	90	•	•		•		•	M/883	E,F	80	60	28	32	2-27
	32Kx8	120	•	•	•	•	•	•	C	E,F	80	60	28	32	2-27
	32Kx8	120	•	•	•	•	•	•	I	E,F	80	60	28	32	2-27
	32Kx8	120	•	•		•		•	M	E,F	80	60	28	32	2-27
	32Kx8	120	•	•		•		•	M/883	E,F	80	60	28	32	2-27
SMD Number															
5962-8863403	32Kx8	90	•	•		•		•	M/883		80	60	28	32	2-27
5962-8863404	32Kx8	90	•	•		•		•	M/883	F	80	60	28	32	2-27

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3ms

CMOS E²PROM Product Selection Guide

AT28HC256L	Organization	Speed (ns)	Package						Temp. Range	Option	Icc (mA)		No. of Pins		Page Number
Part Number			D	F	J	L	P	U			Active	Standby	DIP	LCC	
AT28HC256L	32Kx8	90	•	•	•	•	•	•	C	E, F	80	0.3	28	32	2-27
	32Kx8	90	•	•	•	•	•	•	I	E, F	80	0.3	28	32	2-27
	32Kx8	120	•	•	•	•	•	•	C	E, F	80	0.3	28	32	2-27
	32Kx8	120	•	•	•	•	•	•	I	E, F	80	0.3	28	32	2-27
	32Kx8	120	•	•		•		•	M	E, F	80	0.3	28	32	2-27
	32Kx8	120	•	•		•		•	M/883	E, F	80	0.3	28	32	2-27
SMD Number															
5962-8863401	32Kx8	120	•	•		•		•	M/883		80	0.3	28	32	2-27
5962-8863402	32Kx8	120	•	•		•		•	M/883	F	80	0.3	28	32	2-27

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3ms

CMOS E²PROM Product Selection Guide

AT28C04 Part Number	Organization	Speed (ns)	Package D	Package L	Package P	Package W	Temp. Range	Option	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT28C04	512x8	150	•	•	•		C	E,F	30	0.1	24	32	2-41
	512x8	150	•	•	•		I	E,F	45	0.1	24	32	2-41
	512x8	150	•	•			M	E,F	45	0.1	24	32	2-41
	512x8	150	•	•			M/883	E,F	45	0.1	24	32	2-41
	512x8	200	•	•	•	•	C	E,F	30	0.1	24	32	2-41
	512x8	200	•	•	•		I	E,F	45	0.1	24	32	2-41
	512x8	200	•	•			M	E,F	45	0.1	24	32	2-41
	512x8	200	•	•			M/883	E,F	45	0.1	24	32	2-41
	512x8	250	•	•	•	•	C	E,F	30	0.1	24	32	2-41
	512x8	250	•	•	•		I	E,F	45	0.1	24	32	2-41
	512x8	250	•	•			M	E,F	45	0.1	24	32	2-41
	512x8	250	•	•			M/883	E,F	45	0.1	24	32	2-41
	512x8	300	•	•			M/883	E,F	45	0.1	24	32	2-41
	512x8	350	•	•			M/883	E,F	45	0.1	24	32	2-41
	512x8	450	•	•			M/883	E,F	45	0.1	24	32	2-41

	Package Type
D	24D6, 24 Lead 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
	Options
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200µs
F	Fast Write Option: Write Time = 200µs

CMOS E²PROM Product Selection Guide

AT28C16 Part Number	Organization	Speed (ns)	Package D	J	L	P	S	W	Temp. Range	Option	I_{CC} (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT28C16	2Kx8	150	•	•	•	•	•		C	E, F	30	0.1	24	32	2-51
	2Kx8	150	•	•	•	•	•		I	E, F	45	0.1	24	32	2-51
	2Kx8	150	•		•				M	E, F	45	0.1	24	32	2-51
	2Kx8	150	•		•				M/883	E, F	45	0.1	24	32	2-51
	2Kx8	200	•	•	•	•	•	•	C	E, F	30	0.1	24	32	2-51
	2Kx8	200	•	•	•	•	•		I	E, F	45	0.1	24	32	2-51
	2Kx8	200	•		•				M	E, F	45	0.1	24	32	2-51
	2Kx8	200	•		•				M/883	E, F	45	0.1	24	32	2-51
	2Kx8	250	•	•	•	•	•	•	C	E, F	30	0.1	24	32	2-51
	2Kx8	250	•	•	•	•	•		I	E, F	45	0.1	24	32	2-51
	2Kx8	250	•		•				M	E, F	45	0.1	24	32	2-51
	2Kx8	250	•		•				M/883	E, F	45	0.1	24	32	2-51
	2Kx8	300	•		•				M/883	E, F	45	0.1	24	32	2-51
	2Kx8	350	•		•				M/883	E, F	45	0.1	24	32	2-51
	2Kx8	450	•		•				M/883	E, F	45	0.1	24	32	2-51

	Package Type
D	24D6, 24 Lead 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
	Options
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200µs
F	Fast Write Option: Write Time = 200µs

CMOS E²PROM Product Selection Guide

AT28C17 Part Number	Organization	Speed (ns)	Package D	J	L	P	S	W	Temp. Range	Option	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT28C17	2Kx8	150	•	•	•	•	•		C	E,F	30	0.1	28	32	2-61
	2Kx8	150	•	•	•	•	•		I	E,F	45	0.1	28	32	2-61
	2Kx8	150	•		•				M	E,F	45	0.1	28	32	2-61
	2Kx8	150	•		•				M/883	E,F	45	0.1	28	32	2-61
	2Kx8	200	•	•	•	•	•	•	C	E,F	30	0.1	28	32	2-61
	2Kx8	200	•	•	•	•	•		I	E,F	45	0.1	28	32	2-61
	2Kx8	200	•		•				M	E,F	45	0.1	28	32	2-61
	2Kx8	200	•		•				M/883	E,F	45	0.1	28	32	2-61
	2Kx8	250	•	•	•	•	•	•	C	E,F	30	0.1	28	32	2-61
	2Kx8	250	•	•	•	•	•		I	E,F	45	0.1	28	32	2-61
	2Kx8	250	•		•				M	E,F	45	0.1	28	32	2-61
	2Kx8	250	•		•				M/883	E,F	45	0.1	28	32	2-61
	2Kx8	300	•		•				M/883	E,F	45	0.1	28	32	2-61
	2Kx8	350	•		•				M/883	E,F	45	0.1	28	32	2-61
	2Kx8	450	•		•				M/883	E,F	45	0.1	28	32	2-61

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	28S, 28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200µs
F	Fast Write Option: Write Time = 200µs

CMOS E²PROM Product Selection Guide

AT28C64 Part Number	Organization	Speed (ns)	Package D	F	J	K	L	P	S	W	Temp. Range	Option	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT28C64	8Kx8	150	•	•	•		•	•	•		C	E,F	30	0.1	28	32	2-71
	8Kx8	150	•	•	•		•	•	•		I	E,F	45	0.1	28	32	2-71
	8Kx8	150	•	•			•				M	E,F	45	0.1	28	32	2-71
	8Kx8	150	•	•			•				M/883	E,F	45	0.1	28	32	2-71
	8Kx8	200	•	•	•		•	•	•	•	C	E,F	30	0.1	28	32	2-71
	8Kx8	200	•	•	•		•	•	•		I	E,F	45	0.1	28	32	2-71
	8Kx8	200	•	•			•				M	E,F	45	0.1	28	32	2-71
	8Kx8	200	•	•			•				M/883	E,F	45	0.1	28	32	2-71
	8Kx8	250	•	•	•		•	•	•	•	C	E,F	30	0.1	28	32	2-71
	8Kx8	250	•	•	•		•	•	•		I	E,F	45	0.1	28	32	2-71
	8Kx8	250	•	•			•				M	E,F	45	0.1	28	32	2-71
	8Kx8	250	•	•			•				M/883	E,F	45	0.1	28	32	2-71
	8Kx8	300	•	•			•				M/883	E,F	45	0.1	28	32	2-71
	8Kx8	350	•	•			•				M/883	E,F	45	0.1	28	32	2-71
	8Kx8	450	•	•			•				M/883	E,F	45	0.1	28	32	2-71
SMD Number																	
5962-8751417	8Kx8	150	•			•	•				M/883		45	0.1	28	32	2-71
5962-8751416	8Kx8	200	•			•	•				M/883		45	0.1	28	32	2-71
5962-8751415	8Kx8	250	•	•		•	•				M/883		45	0.1	28	32	2-71
5962-8751414	8Kx8	300	•			•	•				M/883		45	0.1	28	32	2-71
5962-8751413	8Kx8	350	•			•	•				M/883		45	0.1	28	32	2-71

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
K	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide Plastic Dual Inline Package (PDIP)
S	28S, 28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200μs
F	Fast Write Option: Write Time = 200μs

CMOS E²PROM Product Selection Guide

AT28C64X	Organi-	Speed	Package							Temp.	Icc (mA)		No. of Pins		Page
Part Number	zation	(ns)	D	F	J	K	L	P	S	Range	Active	Standby	DIP	LCC	Number
AT28C64X	8Kx8	150	•	•	•		•	•	•	C	30	0.1	28	32	2-71
	8Kx8	150	•	•	•		•	•	•	I	45	0.1	28	32	2-71
	8Kx8	150	•	•			•			M	45	0.1	28	32	2-71
	8Kx8	150	•	•			•			M/883	45	0.1	28	32	2-71
	8Kx8	200	•	•	•		•	•	•	C	30	0.1	28	32	2-71
	8Kx8	200	•	•	•		•	•	•	I	45	0.1	28	32	2-71
	8Kx8	200	•	•			•			M	45	0.1	28	32	2-71
	8Kx8	200	•	•			•			M/883	45	0.1	28	32	2-71
	8Kx8	250	•	•	•		•	•	•	C	30	0.1	28	32	2-71
	8Kx8	250	•	•	•		•	•	•	I	45	0.1	28	32	2-71
	8Kx8	250	•	•			•			M	45	0.1	28	32	2-71
	8Kx8	250	•	•			•			M/883	45	0.1	28	32	2-71
	8Kx8	300	•	•			•			M/883	45	0.1	28	32	2-71
	8Kx8	350	•	•			•			M/883	45	0.1	28	32	2-71
	8Kx8	450	•	•			•			M/883	45	0.1	28	32	2-71
SMD Number															
5962-8751422	8Kx8	150	•			•	•			M/883	45	0.1	28	32	2-71
5962-8751421	8Kx8	200	•			•	•			M/883	45	0.1	28	32	2-71
5962-8751420	8Kx8	250	•	•		•	•			M/883	45	0.1	28	32	2-71
5962-8751419	8Kx8	300	•			•	•			M/883	45	0.1	28	32	2-71
5962-8751418	8Kx8	350	•			•	•			M/883	45	0.1	28	32	2-71

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
K	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide Plastic Dual Inline Package (PDIP)
S	28S, 28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS E²PROM Product Selection Guide

AT28PC64 Part Number	Organization	Speed (ns)	Package D	J	K	L	P	W	Temp. Range	Option	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT28PC64	8Kx8	150	•	•		•	•	•	C	E	80	0.1	28	32	2-83
	8Kx8	150	•	•		•	•		I	E	80	0.1	28	32	2-83
	8Kx8	150	•			•			M	E	80	0.2	28	32	2-83
	8Kx8	150	•			•			M/883	E	80	0.2	28	32	2-83
	8Kx8	200	•	•		•	•	•	C	E	80	0.1	28	32	2-83
	8Kx8	200	•	•		•	•		I	E	80	0.1	28	32	2-83
	8Kx8	200		•		•			M	E	80	0.2	28	32	2-83
	8Kx8	200	•			•			M/883	E	80	0.2	28	32	2-83
	8Kx8	250	•	•		•	•	•	C	E	80	0.1	28	32	2-83
	8Kx8	250	•	•		•	•		I	E	80	0.1	28	32	2-83
	8Kx8	250	•			•			M	E	80	0.2	28	32	2-83
	8Kx8	250	•			•			M/883	E	80	0.2	28	32	2-83
	8Kx8	300	•			•			M/883	E	80	0.2	28	32	2-83
	8Kx8	350	•			•			M/883	E	80	0.2	28	32	2-83
SMD Number															
5962-8751409	8Kx8	200	•		•	•			M/883		80	0.2	28	32	2-83
5962-8751408	8Kx8	250	•		•	•			M/883		80	0.2	28	32	2-83
5962-8751407	8Kx8	300	•		•	•			M/883		80	0.2	28	32	2-83
5962-8751406	8Kx8	350	•		•	•			M/883		80	0.2	28	32	2-83

	Package Type
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
K	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
	Options
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS E²PROM Product Selection Guide

AT28C256 Part Number	Organization	Speed (ns)	Package D	F	J	L	P	U	W	Temp. Range	Option	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT28C256	32Kx8	150	•	•	•	•	•	•	•	C	E,F	80	0.2	28	32	2-93
	32Kx8	150	•	•	•	•	•	•		I	E,F	80	0.2	28	32	2-93
	32Kx8	150	•	•		•		•		M	E,F	80	0.3	28	32	2-93
	32Kx8	150	•	•		•		•		M/883	E,F	80	0.3	28	32	2-93
	32Kx8	200	•	•	•	•	•	•	•	C	E,F	80	0.2	28	32	2-93
	32Kx8	200	•	•	•	•	•	•		I	E,F	80	0.2	28	32	2-93
	32Kx8	200	•	•		•		•		M	E,F	80	0.3	28	32	2-93
	32Kx8	200	•	•		•		•		M/883	E,F	80	0.3	28	32	2-93
	32Kx8	250	•	•	•	•	•	•	•	C	E,F	80	0.2	28	32	2-93
	32Kx8	250	•	•	•	•	•	•		I	E,F	80	0.2	28	32	2-93
	32Kx8	250	•	•		•		•		M	E,F	80	0.3	28	32	2-93
	32Kx8	250	•	•		•		•		M/883	E,F	80	0.3	28	32	2-93
	32Kx8	300	•	•		•		•		M/883	E,F	80	0.3	28	32	2-93
	32Kx8	350	•	•		•		•		M/883	E,F	80	0.3	28	32	2-93
SMD Number																
5962-8852506	32Kx8	150	•	•		•				M/883		80	0.35	28	32	2-93
5962-8852507	32Kx8	150	•	•		•				M/883	F	80	0.35	28	32	2-93
5962-8852504	32Kx8	200	•	•		•		•		M/883		80	0.35	28	32	2-93
5962-8852503	32Kx8	250	•	•		•		•		M/883		80	0.35	28	32	2-93
5962-8852505	32Kx8	250	•	•		•				M/883	E	80	0.35	28	32	2-93
5962-8852502	32Kx8	300	•	•		•		•		M/883		80	0.35	28	32	2-93
5962-8852501	32Kx8	350	•	•		•		•		M/883		80	0.35	28	32	2-93

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3ms

CMOS E^{2}PROM Product Selection Guide

AT28MC010 Part Number	Organization	Speed (ns)	Package M	Temperature Range	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	Page Number
AT28MC010	128Kx8	120	•	C	100	0.5	32	2-105
	128Kx8	120	•	I	100	0.5	32	2-105
	128Kx8	120	•	M	100	0.5	32	2-105
	128Kx8	120	•	MB	100	0.5	32	2-105
	128Kx8	150	•	C	100	0.5	32	2-105
	128Kx8	150	•	I	100	0.5	32	2-105
	128Kx8	150	•	M	100	0.5	32	2-105
	128Kx8	150	•	MB	100	0.5	32	2-105
	128Kx8	200	•	C	100	0.5	32	2-105
	128Kx8	200	•	I	100	0.5	32	2-105
	128Kx8	200	•	M	100	0.5	32	2-105
	128Kx8	200	•	MB	100	0.5	32	2-105
	128Kx8	250	•	C	100	0.5	32	2-105
	128Kx8	250	•	I	100	0.5	32	2-105
	128Kx8	250	•	M	100	0.5	32	2-105
	128Kx8	250	•	MB	100	0.5	32	2-105

Package Type	
M	32M, 32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Module (Module)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
MB	MIL-STD-883C Class B Components (-55°C to 125°C)

CMOS E²PROM Product Selection Guide

AT28C1024 Part Number	Organization	Speed (ns)	Package B	Package L	Temperature Range	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT28C1024	64Kx16	150	•	•	C	100	0.5	40	44	2-115
	64Kx16	150	•	•	I	100	0.5	40	44	2-115
	64Kx16	150	•	•	M	100	0.5	40	44	2-115
	64Kx16	150	•	•	M/883	100	0.5	40	44	2-115
	64Kx16	200	•	•	C	100	0.5	40	44	2-115
	64Kx16	200	•	•	I	100	0.5	40	44	2-115
	64Kx16	200	•	•	M	100	0.5	40	44	2-115
	64Kx16	200	•	•	M/883	100	0.5	40	44	2-115
	64Kx16	250	•	•	C	100	0.5	40	44	2-115
	64Kx16	250	•	•	I	100	0.5	40	44	2-115
	64Kx16	250	•	•	M	100	0.5	40	44	2-115
	64Kx16	250	•	•	M/883	100	0.5	40	44	2-115

Package Type	
B	40B, 40 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
L	44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS E²PROM Product Selection Guide

AT28C010 Part Number	Organization	Speed (ns)	Package B	Package L	Temperature Range	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT28C010	128Kx8	150	•	•	C	80	0.3	32	44	2-125
	128Kx8	150	•	•	I	80	0.3	32	44	2-125
	128Kx8	150	•	•	M	80	0.3	32	44	2-125
	128Kx8	150	•	•	M/883	80	0.3	32	44	2-125
	128Kx8	200	•	•	C	80	0.3	32	44	2-125
	128Kx8	200	•	•	I	80	0.3	32	44	2-125
	128Kx8	200	•	•	M	80	0.3	32	44	2-125
	128Kx8	200	•	•	M/883	80	0.3	32	44	2-125
	128Kx8	250	•	•	C	80	0.3	32	44	2-125
	128Kx8	250	•	•	I	80	0.3	32	44	2-125
	128Kx8	250	•	•	M	80	0.3	32	44	2-125
	128Kx8	250	•	•	M/883	80	0.3	32	44	2-125

Package Type	
B	32B, 32 Lead, 0.600" Wide Ceramic Side Braze Dual Inline (Side Braze)
L	44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS PEROM Product Selection Guide

AT29C256 Part Number	Organization	Speed (ns)	Package D	J	L	P	Temp. Range	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT29C256	32Kx8	150	•	•	•	•	C	80	0.3	28	32	3-3
	32Kx8	150	•	•	•	•	I	80	0.3	28	32	3-3
	32Kx8	150	•		•		M	80	0.3	28	32	3-3
	32Kx8	150	•		•		M/883	80	0.3	28	32	3-3
	32Kx8	200	•	•	•	•	C	80	0.3	28	32	3-3
	32Kx8	200	•	•	•	•	I	80	0.3	28	32	3-3
	32Kx8	200	•		•		M	80	0.3	28	32	3-3
	32Kx8	200	•		•		M/883	80	0.3	28	32	3-3
	32Kx8	250	•	•	•	•	C	80	0.3	28	32	3-3
	32Kx8	250	•	•	•	•	I	80	0.3	28	32	3-3
	32Kx8	250	•		•		M	80	0.3	28	32	3-3
	32Kx8	250	•		•		M/883	80	0.3	28	32	3-3

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS PEROM Product Selection Guide

AT29C257 Part Number	Organization	Speed (ns)	Package D	Package P	Temperature Range	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	Page Number
AT29C257	32Kx8	150	•	•	C	80	0.3	32	3-13
	32Kx8	150	•	•	I	80	0.3	32	3-13
	32Kx8	150	•		M	80	0.3	32	3-13
	32Kx8	150	•		M/883	80	0.3	32	3-13
	32Kx8	200	•	•	C	80	0.3	32	3-13
	32Kx8	200	•	•	I	80	0.3	32	3-13
	32Kx8	200	•		M	80	0.3	32	3-13
	32Kx8	200	•		M/883	80	0.3	32	3-13
	32Kx8	250	•	•	C	80	0.3	32	3-13
	32Kx8	250	•	•	I	80	0.3	32	3-13
	32Kx8	250	•		M	80	0.3	32	3-13
	32Kx8	250	•		M/883	80	0.3	32	3-13

Package Type	
D	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS PEROM Product Selection Guide

AT29C010 Part Number	Organization	Speed (ns)	Package D	J	L	P	Temp. Range	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT29C010	128Kx8	150	•	•	•	•	C	80	0.3	32	32	3-23
	128Kx8	150	•	•	•	•	I	80	0.3	32	32	3-23
	128Kx8	150	•		•		M	80	0.3	32	32	3-23
	128Kx8	150	•		•		M/883	80	0.3	32	32	3-23
	128Kx8	200	•	•	•	•	C	80	0.3	32	32	3-23
	128Kx8	200	•	•	•	•	I	80	0.3	32	32	3-23
	128Kx8	200	•		•		M	80	0.3	32	32	3-23
	128Kx8	200	•		•		M/883	80	0.3	32	32	3-23
	128Kx8	250	•	•	•	•	C	80	0.3	32	32	3-23
	128Kx8	250	•	•	•	•	I	80	0.3	32	32	3-23
	128Kx8	250	•		•		M	80	0.3	32	32	3-23
	128Kx8	250	•		•		M/883	80	0.3	32	32	3-23

Package Type	
D	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27HC64 Part Number	Organization	Speed (ns)	Package D	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT27HC64	8Kx8	45	•	•		C	10%	75	35	28	32	4-3
	8Kx8	45	•	•		I	10%	90	40	28	32	4-3
	8Kx8	55	•	•	•	C	10%	75	35	28	32	4-3
	8Kx8	55	•	•	•	I	10%	90	40	28	32	4-3
	8Kx8	55	•	•		M	10%	90	40	28	32	4-3
	8Kx8	55	•	•		M/883	10%	90	40	28	32	4-3
	8Kx8	70	•	•	•	C	10%	75	35	28	32	4-3
	8Kx8	70	•	•	•	I	10%	90	40	28	32	4-3
	8Kx8	70	•	•		M	10%	90	40	28	32	4-3
	8Kx8	70	•	•		M/883	10%	90	40	28	32	4-3
	8Kx8	90	•	•	•	C	10%	75	35	28	32	4-3
	8Kx8	90	•	•	•	I	10%	90	40	28	32	4-3
	8Kx8	90	•	•		M	10%	90	40	28	32	4-3
	8Kx8	90	•	•		M/883	10%	90	40	28	32	4-3

AT27HC64L Part Number	Organization	Speed (ns)	Package D	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT27HC64L	8Kx8	55	•	•		C	10%	75	0.1	28	32	4-3
	8Kx8	55	•	•		I	10%	90	0.2	28	32	4-3
	8Kx8	70	•	•	•	C	10%	75	0.1	28	32	4-3
	8Kx8	70	•	•	•	I	10%	90	0.2	28	32	4-3
	8Kx8	70	•	•		M	10%	90	0.2	28	32	4-3
	8Kx8	70	•	•		M/883	10%	90	0.2	28	32	4-3
	8Kx8	90	•	•	•	C	10%	75	0.1	28	32	4-3
	8Kx8	90	•	•	•	I	10%	90	0.2	28	32	4-3
	8Kx8	90	•	•		M	10%	90	0.2	28	32	4-3
	8Kx8	90	•	•		M/883	10%	90	0.2	28	32	4-3
SMD Number												
5962-85102 04	8Kx8	90	•	•		M/883	10%	90	0.2	28	32	4-3

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27HC64R Part Number	Organization	Speed (ns)	Package D	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT27HC64R	8Kx8	45	•	•		C	10%	35	20	28	32	4-11
	8Kx8	45	•	•		I	10%	45	30	28	32	4-11
	8Kx8	55	•	•	•	C	10%	35	20	28	32	4-11
	8Kx8	55	•	•	•	I	10%	45	30	28	32	4-11
	8Kx8	55	•	•		M	10%	45	30	28	32	4-11
	8Kx8	55	•	•		M/883	10%	45	30	28	32	4-11
	8Kx8	70	•	•	•	C	10%	35	20	28	32	4-11
	8Kx8	70	•	•	•	I	10%	45	30	28	32	4-11
	8Kx8	70	•	•		M	10%	45	30	28	32	4-11
	8Kx8	70	•	•		M/883	10%	45	30	28	32	4-11
	8Kx8	90	•	•	•	C	10%	35	20	28	32	4-11
	8Kx8	90	•	•	•	I	10%	45	30	28	32	4-11
	8Kx8	90	•	•		M	10%	45	30	28	32	4-11
	8Kx8	90	•	•		M/883	10%	45	30	28	32	4-11

AT27HC64RL Part Number	Organization	Speed (ns)	Package D	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT27HC64RL	8Kx8	55	•	•		C	10%	35	0.1	28	32	4-11
	8Kx8	55	•	•		I	10%	45	0.2	28	32	4-11
	8Kx8	70	•	•	•	C	10%	35	0.1	28	32	4-11
	8Kx8	70	•	•	•	I	10%	45	0.2	28	32	4-11
	8Kx8	70	•	•		M	10%	45	0.2	28	32	4-11
	8Kx8	70	•	•		M/883	10%	45	0.2	28	32	4-11
	8Kx8	90	•	•	•	C	10%	35	0.1	28	32	4-11
	8Kx8	90	•	•	•	I	10%	45	0.2	28	32	4-11
	8Kx8	90	•	•		M	10%	45	0.2	28	32	4-11
	8Kx8	90	•	•		M/883	10%	45	0.2	28	32	4-11

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27HC256 Part Number	Organization	Speed (ns)	Package D	J	K	L	P	Temp. Range	Power Supply	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT27HC256	32Kx8	55	•		•	•		C	10%	75	40	28	32	4-15
	32Kx8	55	•		•	•		I	10%	90	45	28	32	4-15
	32Kx8	70	•	•	•	•	•	C	10%	75	40	28	32	4-15
	32Kx8	70	•	•	•	•	•	I	10%	90	45	28	32	4-15
	32Kx8	70	•		•	•		M	10%	90	45	28	32	4-15
	32Kx8	70	•		•	•		M/883	10%	90	45	28	32	4-15
	32Kx8	90	•	•	•	•	•	C	10%	75	40	28	32	4-15
	32Kx8	90	•	•	•	•	•	I	10%	90	45	28	32	4-15
	32Kx8	90	•		•	•		M	10%	90	45	28	32	4-15
	32Kx8	90	•		•	•		M/883	10%	90	45	28	32	4-15
	32Kx8	120	•	•	•	•	•	C	10%	75	40	28	32	4-15
	32Kx8	120	•	•	•	•	•	I	10%	90	45	28	32	4-15
	32Kx8	120	•		•	•		M	10%	90	45	28	32	4-15
	32Kx8	120	•		•	•		M/883	10%	90	45	28	32	4-15
SMD Number														
5962-86063 08	32Kx8	70	•			•		M/883	10%	90	45	28	32	4-15

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27HC256L Part Number	Organization	Speed (ns)	Package D	J	K	L	P	Temp. Range	Power Supply	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT27HC256L	32Kx8	70	•		•	•		C	10%	75	0.1	28	32	4-15
	32Kx8	70	•		•	•		I	10%	90	0.2	28	32	4-15
	32Kx8	90	•	•	•	•	•	C	10%	75	0.1	28	32	4-15
	32Kx8	90	•	•	•	•	•	I	10%	90	0.2	28	32	4-15
	32Kx8	90	•		•	•		M	10%	90	0.2	28	32	4-15
	32Kx8	90	•		•	•		M/883	10%	90	0.2	28	32	4-15
	32Kx8	120	•	•	•	•	•	C	10%	75	0.1	28	32	4-15
	32Kx8	120	•	•	•	•	•	I	10%	90	0.2	28	32	4-15
	32Kx8	120	•		•	•		M	10%	90	0.2	28	32	4-15
	32Kx8	120	•		•	•		M/883	10%	90	0.2	28	32	4-15
SMD Number														
5962-86063 07	32Kx8	90	•			•		M/883	10%	90	0.2	28	32	4-15
5962-86063 06	32Kx8	120	•			•		M/883	10%	90	0.2	28	32	4-15

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27HC256R Part Number	Organization	Speed (ns)	Package D	J	K	L	P	Temp. Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT27HC256R	32Kx8	55	•		•	•		C	10%	35	20	28	32	4-25
	32Kx8	55	•		•	•		I	10%	45	30	28	32	4-25
	32Kx8	70	•	•	•	•	•	C	10%	35	20	28	32	4-25
	32Kx8	70	•	•	•	•	•	I	10%	45	30	28	32	4-25
	32Kx8	70	•		•	•		M	10%	45	30	28	32	4-25
	32Kx8	70	•		•	•		M/883	10%	45	30	28	32	4-25
	32Kx8	90	•	•	•	•	•	C	10%	35	20	28	32	4-25
	32Kx8	90	•	•	•	•	•	I	10%	45	30	28	32	4-25
	32Kx8	90	•		•	•		M	10%	45	30	28	32	4-25
	32Kx8	90	•		•	•		M/883	10%	45	30	28	32	4-25
	32Kx8	120	•	•	•	•	•	C	10%	35	20	28	32	4-25
	32Kx8	120	•	•	•	•	•	I	10%	45	30	28	32	4-25
	32Kx8	120	•		•	•		M	10%	45	30	28	32	4-25
	32Kx8	120	•		•	•		M/883	10%	45	30	28	32	4-25

AT27HC256RL Part Number	Organization	Speed (ns)	Package D	J	K	L	P	Temp. Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT27HC256RL	32Kx8	70	•		•	•		C	10%	35	0.1	28	32	4-25
	32Kx8	70	•		•	•		I	10%	45	0.2	28	32	4-25
	32Kx8	90	•	•	•	•	•	C	10%	35	0.1	28	32	4-25
	32Kx8	90	•	•	•	•	•	I	10%	45	0.2	28	32	4-25
	32Kx8	90	•		•	•		M	10%	45	0.2	28	32	4-25
	32Kx8	90	•		•	•		M/883	10%	45	0.2	28	32	4-25
	32Kx8	120	•	•	•	•	•	C	10%	35	0.1	28	32	4-25
	32Kx8	120	•	•	•	•	•	I	10%	45	0.2	28	32	4-25
	32Kx8	120	•		•	•		M	10%	45	0.2	28	32	4-25
	32Kx8	120	•		•	•		M/883	10%	45	0.2	28	32	4-25

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27HC1024 Part Number	Organization	Speed (ns)	Package D	J	L	P	Temp. Range	Power Supply	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT27HC1024	64Kx16	55	•		•		C	10%	60	0.5	40	44	4-29
	64Kx16	70	•	•	•	•	C	10%	60	0.5	40	44	4-29
	64Kx16	70	•	•	•	•	I	10%	75	1.0	40	44	4-29
	64Kx16	70	•		•		M	10%	75	1.0	40	44	4-29
	64Kx16	70	•		•		M/883	10%	75	1.0	40	44	4-29
	64Kx16	90	•	•	•	•	C	10%	60	0.5	40	44	4-29
	64Kx16	90	•	•	•	•	I	10%	75	1.0	40	44	4-29
	64Kx16	90	•		•		M	10%	75	1.0	40	44	4-29
	64Kx16	90	•		•		M/883	10%	75	1.0	40	44	4-29
	64Kx16	120	•	•	•	•	C	10%	60	0.5	40	44	4-29
	64Kx16	120	•	•	•	•	I	10%	75	1.0	40	44	4-29
	64Kx16	120	•		•		M	10%	75	1.0	40	44	4-29
	64Kx16	120	•		•		M/883	10%	75	1.0	40	44	4-29

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier, OTP (PLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C128 Part Number	Organization	Speed (ns)	Package D	Package J	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins PLCC	Page Number
AT27C128	16Kx8	120	•			C	10%	30	0.1	28	32	4-33
	16Kx8	120	•			I	10%	40	0.2	28	32	4-33
	16Kx8	150	•	•	•	C	10%	30	0.1	28	32	4-33
	16Kx8	150	•	•	•	I	10%	40	0.2	28	32	4-33
	16Kx8	200	•	•	•	C	10%	30	0.1	28	32	4-33
	16Kx8	200	•	•	•	I	10%	40	0.2	28	32	4-33
	16Kx8	250	•	•	•	C	10%	30	0.1	28	32	4-33
	16Kx8	250	•	•	•	I	10%	40	0.2	28	32	4-33

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
P	28P6, 28 Lead, 0.600" Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS EPROM Product Selection Guide

AT27C256 –Not recommended for new designs. Use AT27C256R.

AT27C256R	Organi-	Speed	Package						Temp.	Power	Icc (mA)		No. of Pins		Page
Part Number	zation	(ns)	D	J	K	L	P	R	Range	Supply	Active	Standby	DIP	LCC	Number
AT27C256R	32Kx8	90	•		•	•			C	10%	20	0.1	28	32	4-47
	32Kx8	90	•		•	•			I	10%	25	0.2	28	32	4-47
	32Kx8	120	•	•	•	•	•	•	C	10%	20	0.1	28	32	4-47
	32Kx8	120	•	•	•	•	•	•	I	10%	25	0.2	28	32	4-47
	32Kx8	120	•		•	•			M	10%	25	0.2	28	32	4-47
	32Kx8	120	•		•	•			M/883	10%	25	0.2	28	32	4-47
	32Kx8	150	•	•	•	•	•	•	C	10%	20	0.1	28	32	4-47
	32Kx8	150	•	•	•	•	•	•	I	10%	25	0.2	28	32	4-47
	32Kx8	150	•		•	•			M	10%	25	0.2	28	32	4-47
	32Kx8	150	•		•	•			M/883	10%	25	0.2	28	32	4-47
	32Kx8	170	•	•	•	•	•	•	C	10%	20	0.1	28	32	4-47
	32Kx8	170	•	•	•	•	•	•	I	10%	25	0.2	28	32	4-47
	32Kx8	170	•		•	•			M	10%	25	0.2	28	32	4-47
	32Kx8	170	•		•	•			M/883	10%	25	0.2	28	32	4-47
	32Kx8	200	•	•	•	•	•	•	C	10%	20	0.1	28	32	4-47
	32Kx8	200	•	•	•	•	•	•	I	10%	25	0.2	28	32	4-47
	32Kx8	200	•		•	•			M	10%	25	0.2	28	32	4-47
	32Kx8	200	•		•	•			M/883	10%	25	0.2	28	32	4-47
	32Kx8	250	•	•	•	•	•	•	C	10%	20	0.1	28	32	4-47
	32Kx8	250	•	•	•	•	•	•	I	10%	25	0.2	28	32	4-47
	32Kx8	250	•		•	•			M	10%	25	0.2	28	32	4-47
	32Kx8	250	•		•	•			M/883	10%	25	0.2	28	32	4-47
SMD Number															
5962-86063 05	32Kx8	150	•			•			M/883	10%	25	0.2	28	32	4-47
5962-86063 04	32Kx8	170	•			•			M/883	10%	25	0.2	28	32	4-47
5962-86063 01	32Kx8	200	•			•			M/883	10%	25	0.2	28	32	4-47
5962-86063 02	32Kx8	250	•			•			M/883	10%	25	0.2	28	32	4-47
5962-86063 03	32Kx8	300	•			•			M/883	10%	25	0.2	28	32	4-47

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C512 –Not recommended for new designs. Use AT27C512R.

AT27C512R Part Number	Organization	Speed (ns)	Package D	J	K	L	P	R	Temp. Range	Power Supply	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT27C512R	64Kx8	100	•		•	•			C	5%	20	0.1	28	32	4-63
	64Kx8	120	•		•	•			C	10%	20	0.1	28	32	4-63
	64Kx8	120	•		•	•			I	10%	25	0.2	28	32	4-63
	64Kx8	120	•		•	•			M	10%	25	0.2	28	32	4-63
	64Kx8	120	•		•	•			M/883	10%	25	0.2	28	32	4-63
	64Kx8	150	•	•	•	•	•	•	C	10%	20	0.1	28	32	4-63
	64Kx8	150	•	•	•	•	•	•	I	10%	25	0.2	28	32	4-63
	64Kx8	150	•		•	•			M	10%	25	0.2	28	32	4-63
	64Kx8	150	•		•	•			M/883	10%	25	0.2	28	32	4-63
	64Kx8	200	•	•	•	•	•	•	C	10%	20	0.1	28	32	4-63
	64Kx8	200	•	•	•	•	•	•	I	10%	25	0.2	28	32	4-63
	64Kx8	200	•		•	•			M	10%	25	0.2	28	32	4-63
	64Kx8	200	•		•	•			M/883	10%	25	0.2	28	32	4-63
	64Kx8	250	•	•	•	•	•	•	C	10%	20	0.1	28	32	4-63
	64Kx8	250	•	•	•	•	•	•	I	10%	25	0.2	28	32	4-63
	64Kx8	250	•		•	•			M	10%	25	0.2	28	32	4-63
	64Kx8	250	•		•	•			M/883	10%	25	0.2	28	32	4-63
SMD Number															
5962-8764804	64Kx8	120	•			•			M/883	10%	25	0.2	28	32	4-63
5962-8764801	64Kx8	150	•			•			M/883	10%	25	0.2	28	32	4-63
5962-8764802	64Kx8	200	•			•			M/883	10%	25	0.2	28	32	4-63
5962-8764803	64Kx8	250	•			•			M/883	10%	25	0.2	28	32	4-63

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C513R	Organization	Speed	Package					Temp.	Power	Icc (mA)		No. of Pins		Page
Part Number		(ns)	D	J	L	P	R	Range	Supply	Active	Standby	DIP	LCC	Number
AT27C513R	4x16Kx8	120	•		•			C	10%	20	0.1	28	32	4-71
	4x16Kx8	120	•		•			I	10%	25	0.2	28	32	4-71
	4x16Kx8	150	•	•	•	•	•	C	10%	20	0.1	28	32	4-71
	4x16Kx8	150	•	•	•	•	•	I	10%	25	0.2	28	32	4-71
	4x16Kx8	150	•		•			M	10%	25	0.2	28	32	4-71
	4x16Kx8	150	•		•			M/883	10%	25	0.2	28	32	4-71
	4x16Kx8	200	•	•	•	•	•	C	10%	20	0.1	28	32	4-71
	4x16Kx8	200	•	•	•	•	•	I	10%	25	0.2	28	32	4-71
	4x16Kx8	200	•		•			M	10%	25	0.2	28	32	4-71
	4x16Kx8	200	•		•			M/883	10%	25	0.2	28	32	4-71
	4x16Kx8	250	•	•	•	•	•	C	10%	20	0.1	28	32	4-71
	4x16Kx8	250	•	•	•	•	•	I	10%	25	0.2	28	32	4-71
	4x16Kx8	250	•		•			M	10%	25	0.2	28	32	4-71
	4x16Kx8	250	•		•			M/883	10%	25	0.2	28	32	4-71

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C010 Part Number	Organization	Speed (ns)	Package D	J	K	L	P	Temp. Range	Power Supply	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT27C010	128Kx8	120	•		•	•		C	10%	40	0.1	32	32	4-81
	128Kx8	120	•		•	•		I	10%	50	0.1	32	32	4-81
	128Kx8	120	•		•	•		M	10%	50	0.1	32	32	4-81
	128Kx8	120	•		•	•		M/883	10%	50	0.1	32	32	4-81
	128Kx8	150	•	•	•	•	•	C	10%	40	0.1	32	32	4-81
	128Kx8	150	•	•	•	•	•	I	10%	50	0.1	32	32	4-81
	128Kx8	150	•		•	•		M	10%	50	0.1	32	32	4-81
	128Kx8	150	•		•	•		M/883	10%	50	0.1	32	32	4-81
	128Kx8	170	•	•	•	•	•	C	10%	40	0.1	32	32	4-81
	128Kx8	170	•	•	•	•	•	I	10%	50	0.1	32	32	4-81
	128Kx8	170	•		•	•		M	10%	50	0.1	32	32	4-81
	128Kx8	170	•		•	•		M/883	10%	50	0.1	32	32	4-81
	128Kx8	200	•	•	•	•	•	C	10%	40	0.1	32	32	4-81
	128Kx8	200	•	•	•	•	•	I	10%	50	0.1	32	32	4-81
	128Kx8	200	•		•	•		M	10%	50	0.1	32	32	4-81
	128Kx8	200	•		•	•		M/883	10%	50	0.1	32	32	4-81
	128Kx8	250	•	•	•	•	•	C	10%	40	0.1	32	32	4-81
	128Kx8	250	•	•	•	•	•	I	10%	50	0.1	32	32	4-81
	128Kx8	250	•		•	•		M	10%	50	0.1	32	32	4-81
	128Kx8	250	•		•	•		M/883	10%	50	0.1	32	32	4-81

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C010L Part Number	Organization	Speed (ns)	Package D	J	K	L	P	Temp. Range	Power Supply	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT27C010L	128Kx8	120	•		•	•		C	10%	25	0.1	32	32	4-81
	128Kx8	120	•		•	•		I	10%	30	0.1	32	32	4-81
	128Kx8	120	•		•	•		M	10%	30	0.1	32	32	4-81
	128Kx8	120	•		•	•		M/883	10%	30	0.1	32	32	4-81
	128Kx8	150	•	•	•	•	•	C	10%	25	0.1	32	32	4-81
	128Kx8	150	•	•	•	•	•	I	10%	30	0.1	32	32	4-81
	128Kx8	150	•		•	•		M	10%	30	0.1	32	32	4-81
	128Kx8	150	•		•	•		M/883	10%	30	0.1	32	32	4-81
	128Kx8	170	•	•	•	•	•	C	10%	25	0.1	32	32	4-81
	128Kx8	170	•	•	•	•	•	I	10%	30	0.1	32	32	4-81
	128Kx8	170	•		•	•		M	10%	30	0.1	32	32	4-81
	128Kx8	170	•		•	•		M/883	10%	30	0.1	32	32	4-81
	128Kx8	200	•	•	•	•	•	C	10%	25	0.1	32	32	4-81
	128Kx8	200	•	•	•	•	•	I	10%	30	0.1	32	32	4-81
	128Kx8	200	•		•	•		M	10%	30	0.1	32	32	4-81
	128Kx8	200	•		•	•		M/883	10%	30	0.1	32	32	4-81
	128Kx8	250	•	•	•	•	•	C	10%	25	0.1	32	32	4-81
	128Kx8	250	•	•	•	•	•	I	10%	30	0.1	32	32	4-81
	128Kx8	250	•		•	•		M	10%	30	0.1	32	32	4-81
	128Kx8	250	•		•	•		M/883	10%	30	0.1	32	32	4-81

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C011 Part Number	Organization	Speed (ns)	Package D	L	P	J	Temp. Range	Power Supply	I_{CC} (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT27C011	8x16Kx8	150	•	•			C	5%	25	0.1	28	32	4-91
	8x16Kx8	170	•	•	•	•	C	10%	25	0.1	28	32	4-91
	8x16Kx8	170	•	•	•	•	I	10%	30	0.1	28	32	4-91
	8x16Kx8	170	•	•			M	10%	30	0.1	28	32	4-91
	8x16Kx8	170	•	•			M/883	10%	30	0.1	28	32	4-91
	8x16Kx8	200	•	•	•	•	C	10%	25	0.1	28	32	4-91
	8x16Kx8	200	•	•	•	•	I	10%	30	0.1	28	32	4-91
	8x16Kx8	200	•	•			M	10%	30	0.1	28	32	4-91
	8x16Kx8	200	•	•			M/883	10%	30	0.1	28	32	4-91
	8x16Kx8	250	•	•	•	•	C	10%	25	0.1	28	32	4-91
	8x16Kx8	250	•	•	•	•	I	10%	30	0.1	28	32	4-91
	8x16Kx8	250	•	•			M	10%	30	0.1	28	32	4-91
	8x16Kx8	250	•	•			M/883	10%	30	0.1	28	32	4-91

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C1024 Part Number	Organization	Speed (ns)	Package D	L	P	J	Temp. Range	Power Supply	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT27C1024	64Kx16	120	•	•			C	5%	50	0.1	40	44	4-101
	64Kx16	150	•	•	•	•	C	10%	50	0.1	40	44	4-101
	64Kx16	150	•	•	•	•	I	10%	60	0.1	40	44	4-101
	64Kx16	150	•	•			M	10%	60	0.1	40	44	4-101
	64Kx16	150	•	•			M/883	10%	60	0.1	40	44	4-101
	64Kx16	170	•	•	•	•	C	10%	50	0.1	40	44	4-101
	64Kx16	170	•	•	•	•	I	10%	60	0.1	40	44	4-101
	64Kx16	170	•	•			M	10%	60	0.1	40	44	4-101
	64Kx16	170	•	•			M/883	10%	60	0.1	40	44	4-101
	64Kx16	200	•	•	•	•	C	10%	50	0.1	40	44	4-101
	64Kx16	200	•	•	•	•	I	10%	60	0.1	40	44	4-101
	64Kx16	200	•	•			M	10%	60	0.1	40	44	4-101
	64Kx16	200	•	•			M/883	10%	60	0.1	40	44	4-101
	64Kx16	250	•	•	•	•	C	10%	50	0.1	40	44	4-101
	64Kx16	250	•	•	•	•	I	10%	60	0.1	40	44	4-101
	64Kx16	250	•	•			M	10%	60	0.1	40	44	4-101
	64Kx16	250	•	•			M/883	10%	60	0.1	40	44	4-101

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C1024L Part Number	Organization	Speed (ns)	Package D	Package L	Package P	Package J	Temp. Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT27C1024L	64Kx16	120	•	•			C	5%	30	0.1	40	44	4-101
	64Kx16	150	•	•	•	•	C	10%	30	0.1	40	44	4-101
	64Kx16	150	•	•	•	•	I	10%	40	0.1	40	44	4-101
	64Kx16	150	•	•			M	10%	40	0.1	40	44	4-101
	64Kx16	150	•	•			M/883	10%	40	0.1	40	44	4-101
	64Kx16	170	•	•	•	•	C	10%	30	0.1	40	44	4-101
	64Kx16	170	•	•	•	•	I	10%	40	0.1	40	44	4-101
	64Kx16	170	•	•			M	10%	40	0.1	40	44	4-101
	64Kx16	170	•	•			M/883	10%	40	0.1	40	44	4-101
	64Kx16	200	•	•	•	•	C	10%	30	0.1	40	44	4-101
	64Kx16	200	•	•	•	•	I	10%	40	0.1	40	44	4-101
	64Kx16	200	•	•			M	10%	40	0.1	40	44	4-101
	64Kx16	200	•	•			M/883	10%	40	0.1	40	44	4-101
	64Kx16	250	•	•	•	•	C	10%	30	0.1	40	44	4-101
	64Kx16	250	•	•	•	•	I	10%	40	0.1	40	44	4-101
	64Kx16	250	•	•			M	10%	40	0.1	40	44	4-101
	64Kx16	250	•	•			M/883	10%	40	0.1	40	44	4-101

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C040 Part Number	Organization	Speed (ns)	Package D	Temp. Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT27C040	128Kx8	120	•	C	10%	25	0.1	32	32	4-111
	128Kx8	150	•	C	10%	25	0.1	32	32	4-111
	128Kx8	150	•	I	10%	30	0.1	32	32	4-111
	128Kx8	150	•	M	10%	30	0.1	32	32	4-111
	128Kx8	150	•	M/883	10%	30	0.1	32	32	4-111
	128Kx8	200	•	C	10%	25	0.1	32	32	4-111
	128Kx8	200	•	I	10%	30	0.1	32	32	4-111
	128Kx8	200	•	M	10%	30	0.1	32	32	4-111
	128Kx8	200	•	M/883	10%	30	0.1	32	32	4-111
	128Kx8	250	•	C	10%	25	0.1	32	32	4-111
	128Kx8	250	•	I	10%	30	0.1	32	32	4-111
	128Kx8	250	•	M	10%	30	0.1	32	32	4-111
	128Kx8	250	•	M/883	10%	30	0.1	32	32	4-111

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

High-Speed CMOS PROM Product Selection Guide

AT28HC191 Part Number	Organization	Speed (ns)	Package D	Package P	Temp. Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	Page Number
AT28HC191	2Kx8	35	•	•	C	10%	80	60	24	5-3
	2Kx8	45	•	•	C	10%	80	60	24	5-3
	2Kx8	45	•	•	I	10%	80	60	24	5-3
	2Kx8	45	•		M	10%	80	60	24	5-3
	2Kx8	45	•		M/883	10%	80	60	24	5-3
	2Kx8	55	•	•	C	10%	80	60	24	5-3
	2Kx8	55	•	•	I	10%	80	60	24	5-3
	2Kx8	55	•		M	10%	80	60	24	5-3
	2Kx8	55	•		M/883	10%	80	60	24	5-3

AT28HC191L Part Number	Organization	Speed (ns)	Package D	Package P	Temp. Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	Page Number
AT28HC191L	2Kx8	45	•	•	C	10%	80	3	24	5-3
	2Kx8	45	•	•	I	10%	80	3	24	5-3
	2Kx8	45	•		M	10%	80	3	24	5-3
	2Kx8	45	•		M/883	10%	80	3	24	5-3
	2Kx8	55	•	•	C	10%	80	3	24	5-3
	2Kx8	55	•	•	I	10%	80	3	24	5-3
	2Kx8	55	•		M	10%	80	3	24	5-3
	2Kx8	55	•		M/883	10%	80	3	24	5-3

Package Type	
D	24D6, 24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

High-Speed CMOS PROM Product Selection Guide

AT28HC291 Part Number	Organization	Speed (ns)	Package D	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT28HC291	2Kx8	35	•		•	C	10%	80	60	24	28	5-11
	2Kx8	45	•	•	•	C	10%	80	60	24	28	5-11
	2Kx8	45	•	•	•	I	10%	80	60	24	28	5-11
	2Kx8	45	•	•		M	10%	80	60	24	28	5-11
	2Kx8	45	•	•		M/883	10%	80	60	24	28	5-11
	2Kx8	55	•	•	•	C	10%	80	60	24	28	5-11
	2Kx8	55	•	•	•	I	10%	80	60	24	28	5-11
	2Kx8	55	•	•		M	10%	80	60	24	28	5-11
	2Kx8	55	•	•		M/883	10%	80	60	24	28	5-11

AT28HC291L Part Number	Organization	Speed (ns)	Package D	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT28HC291L	2Kx8	45	•		•	C	10%	80	3	24	28	5-11
	2Kx8	45	•		•	I	10%	80	3	24	28	5-11
	2Kx8	45	•			M	10%	80	3	24	28	5-11
	2Kx8	45	•			M/883	10%	80	3	24	28	5-11
	2Kx8	55	•	•	•	C	10%	80	3	24	28	5-11
	2Kx8	55	•	•	•	I	10%	80	3	24	28	5-11
	2Kx8	55	•	•		M	10%	80	3	24	28	5-11
	2Kx8	55	•	•		M/883	10%	80	3	24	28	5-11

Package Type	
D	24D3, 24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
L	28L, 28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

High-Speed CMOS PROM Product Selection Guide

AT27HC641 Part Number	Organization	Speed (ns)	Package D	F	L	P	Temp. Range	Power Supply	Icc (mA) Active	Standby	No. of Pins DIP	LCC	Page Number
AT27HC641	8Kx8	35	•		•		C	5%	75	35	24	28	5-19
	8Kx8	45	•		•		C	10%	75	35	24	28	5-19
	8Kx8	45	•		•		I	10%	90	40	24	28	5-19
	8Kx8	45	•		•		M	10%	90	40	24	28	5-19
	8Kx8	45	•		•		M/883	10%	90	40	24	28	5-19
	8Kx8	55	•		•	•	C	10%	75	35	24	28	5-19
	8Kx8	55	•		•	•	I	10%	90	40	24	28	5-19
	8Kx8	55	•		•		M	10%	90	40	24	28	5-19
	8Kx8	55	•		•		M/883	10%	90	40	24	28	5-19
	8Kx8	70	•		•	•	C	10%	75	35	24	28	5-19
	8Kx8	70	•		•	•	I	10%	90	40	24	28	5-19
	8Kx8	70	•		•		M	10%	90	40	24	28	5-19
	8Kx8	70	•		•		M/883	10%	90	40	24	28	5-19
	8Kx8	90	•		•	•	C	10%	75	35	24	28	5-19
	8Kx8	90	•		•	•	I	10%	90	40	24	28	5-19
	8Kx8	90	•		•		M	10%	90	40	24	28	5-19
	8Kx8	90	•		•		M/883	10%	90	40	24	28	5-19
SMD Number													
5962-87515 01	8Kx8	45	•	•	•		M/883	10%	90	40	24	28	5-19
5962-87515 02	8Kx8	55	•	•	•		M/883	10%	90	40	24	28	5-19
5962-87515 03	8Kx8	70	•	•	•		M/883	10%	90	40	24	28	5-19
5962-87515 04	8Kx8	90	•	•	•		M/883	10%	90	40	24	28	5-19

Package Type	
D	24DW6, 24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
F	24FW, 24 Lead, Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

High-Speed CMOS PROM Product Selection Guide

AT27HC642 Part Number	Organization	Speed (ns)	Package D	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	Page Number
AT27HC642	8Kx8	35	•		C	5%	75	35	24	5-19
	8Kx8	45	•		C	10%	75	35	24	5-19
	8Kx8	45	•		I	10%	90	40	24	5-19
	8Kx8	45	•		M	10%	90	40	24	5-19
	8Kx8	45	•		M/883	10%	90	40	24	5-19
	8Kx8	55	•	•	C	10%	75	35	24	5-19
	8Kx8	55	•	•	I	10%	90	40	24	5-19
	8Kx8	55	•		M	10%	90	40	24	5-19
	8Kx8	55	•		M/883	10%	90	40	24	5-19
	8Kx8	70	•	•	C	10%	75	35	24	5-19
	8Kx8	70	•	•	I	10%	90	40	24	5-19
	8Kx8	70	•		M	10%	90	40	24	5-19
	8Kx8	70	•		M/883	10%	90	40	24	5-19
	8Kx8	90	•	•	C	10%	75	35	24	5-19
	8Kx8	90	•	•	I	10%	90	40	24	5-19
	8Kx8	90	•		M	10%	90	40	24	5-19
	8Kx8	90	•		M/883	10%	90	40	24	5-19
SMD Number										
5962-87515 01	8Kx8	45	•		M/883	10%	90	40	24	5-19
5962-87515 02	8Kx8	55	•		M/883	10%	90	40	24	5-19
5962-87515 03	8Kx8	70	•		M/883	10%	90	40	24	5-19
5962-87515 04	8Kx8	90	•		M/883	10%	90	40	24	5-19

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

High-Speed CMOS PROM Product Selection Guide

AT27HC641R Part Number	Organization	Speed (ns)	Package D	Package L	Package P	Temp. Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins LCC	Page Number
AT27HC641R	8Kx8	35	•	•		C	10%	35	20	24	28	5-27
	8Kx8	45	•	•		C	10%	35	20	24	28	5-27
	8Kx8	45	•	•		I	10%	45	30	24	28	5-27
	8Kx8	45	•	•		M	10%	45	30	24	28	5-27
	8Kx8	45	•	•		M/883	10%	45	30	24	28	5-27
	8Kx8	55	•	•	•	C	10%	35	20	24	28	5-27
	8Kx8	55	•	•	•	I	10%	45	30	24	28	5-27
	8Kx8	55	•	•		M	10%	45	30	24	28	5-27
	8Kx8	55	•	•		M/883	10%	45	30	24	28	5-27
	8Kx8	70	•	•	•	C	10%	35	20	24	28	5-27
	8Kx8	70	•	•	•	I	10%	45	30	24	28	5-27
	8Kx8	70	•	•		M	10%	45	30	24	28	5-27
	8Kx8	70	•	•		M/883	10%	45	30	24	28	5-27
	8Kx8	90	•	•	•	C	10%	35	20	24	28	5-27
	8Kx8	90	•	•	•	I	10%	45	30	24	28	5-27
	8Kx8	90	•	•		M	10%	45	30	24	28	5-27
	8Kx8	90	•	•		M/883	10%	45	30	24	28	5-27

Package Type	
D	24DW6, 24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

High-Speed CMOS PROM Product Selection Guide

AT27HC642R Part Number	Organization	Speed (ns)	Package D	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	Page Number
AT27HC642R	8Kx8	35	•		C	10%	35	20	24	5-27
	8Kx8	45	•		C	10%	35	20	24	5-27
	8Kx8	45	•		I	10%	45	30	24	5-27
	8Kx8	45	•		M	10%	45	30	24	5-27
	8Kx8	45	•		M/883	10%	45	30	24	5-27
	8Kx8	55	•	•	C	10%	35	20	24	5-27
	8Kx8	55	•	•	I	10%	45	30	24	5-27
	8Kx8	55	•		M	10%	45	30	24	5-27
	8Kx8	55	•		M/883	10%	45	30	24	5-27
	8Kx8	70	•	•	C	10%	35	20	24	5-27
	8Kx8	70	•	•	I	10%	45	30	24	5-27
	8Kx8	70	•		M	10%	45	30	24	5-27
	8Kx8	70	•		M/883	10%	45	30	24	5-27
	8Kx8	90	•	•	C	10%	35	20	24	5-27
	8Kx8	90	•	•	I	10%	45	30	24	5-27
	8Kx8	90	•		M	10%	45	30	24	5-27
	8Kx8	90	•		M/883	10%	45	30	24	5-27

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS SRAM Product Selection Guide

AT3864L Part Number	Organization	Speed (ns)	Package P	Package R	Temperature Range	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	No. of Pins SOIC	Page Number
AT3864L	8Kx8	100	•	•	C	35	0.1	28	28	6-3
	8Kx8	100	•	•	I	35	0.1	28	28	6-3
	8Kx8	120	•	•	C	35	0.1	28	28	6-3
	8Kx8	120	•	•	I	35	0.1	28	28	6-3
	8Kx8	150	•	•	C	35	0.1	28	28	6-3
	8Kx8	150	•	•	I	35	0.1	28	28	6-3

Package Type	
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS SRAM Product Selection Guide

AT3864L-15DMB Part Number	Organization	Speed (ns)	Package D	Temperature Range	Icc (mA) Active	Icc (mA) Standby	No. of Pins DIP	Page Number
AT3864L-15DMB	8Kx8	150	•	M	40	1.0	28	6-11

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Temperature Range	
M	Military (-55°C to 125°C)

CMOS SRAM Product Selection Guide

AT38256 Part Number	Organization	Speed (ns)	Package B	D	N	P	X	Temperature Range	Icc (mA) Active	Standby	No. of Pins DIP	Page Number
AT38256	32Kx8	20			•		•	C	120	1.0	28	6-19
	32Kx8	20			•		•	I	120	1.0	28	6-19
	32Kx8	25			•	•	•	C	120	1.0	28	6-19
	32Kx8	25			•	•	•	I	120	1.0	28	6-19
	32Kx8	25	•	•				M	120	1.0	28	6-19
	32Kx8	35			•	•	•	C	120	1.0	28	6-19
	32Kx8	35			•	•	•	I	120	1.0	28	6-19
	32Kx8	35	•	•				M	120	1.0	28	6-19

Package Type	
B	28B, 28 Lead, 0.300" Wide, Ceramic Side Braze Dual Inline (Side Braze)
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
N	28P3, 28 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
X	28X, 28 Lead, 0.300" Wide, Plastic J-Leaded Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

CMOS EPLD Product Selection Guide

AT22V10 Part Number	Approx. Gates	Speed (ns)	Package D	F	G	J	K	L	N	P	Y	Temp. Range	Power Supply	Icc (mA)	No. of Pins DIP	LCC	Page Number
AT22V10	500	15	•	•	•	•	•	•	•	•	•	C	10%	90	24	28	7-3
		15	•	•	•	•	•	•	•	•	•	I	10%	90	24	28	7-3
		20	•	•	•	•	•	•	•	•	•	C	10%	55	24	28	7-3
		20	•	•	•	•	•	•	•	•	•	I	10%	55	24	28	7-3
		20	•	•	•		•	•	•		•	M	10%	55	24	28	7-3
		20	•	•	•		•	•	•		•	M/883	10%	55	24	28	7-3
		25	•	•	•	•	•	•	•	•	•	C	10%	55	24	28	7-3
		25	•	•	•	•	•	•	•	•	•	I	10%	55	24	28	7-3
		25	•	•	•		•	•	•		•	M	10%	55	24	28	7-3
		25	•	•	•		•	•	•		•	M/883	10%	55	24	28	7-3
		30	•	•	•		•	•	•		•	M	10%	55	24	28	7-3
		30	•	•	•		•	•	•		•	M/883	10%	55	24	28	7-3
		35	•	•	•	•	•	•	•	•	•	C	10%	55	24	28	7-3
		35	•	•	•	•	•	•	•	•	•	I	10%	55	24	28	7-3
SMD Number																	
5962-8753904	500	20	•					•				M/883	10%	55	24	28	7-3
5962-8753901	500	25	•					•			•	M/883	10%	55	24	28	7-3
5962-8753902	500	30	•					•			•	M/883	10%	55	24	28	7-3
5962-8753903	500	40	•					•			•	M/883	10%	55	24	28	7-3
5962-8867004	500	20		•	•				•			M/883	10%	55	24	28	7-3
5962-8867001	500	25		•	•				•			M/883	10%	55	24	28	7-3
5962-8867002	500	30		•	•				•			M/883	10%	55	24	28	7-3
5962-8867003	500	40		•	•				•			M/883	10%	55	24	28	7-3

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

AT22V10L Part Number	Approx. Gates	Speed (ns)	Package D	F	G	J	K	L	N	P	Y	Temp. Range	Power Supply	Icc (mA)	No. of Pins DIP	LCC	Page Number
AT22V10L	500	15	•	•	•	•	•	•	•	•	•	C	10%	12	24	28	7-3
		15	•	•	•	•	•	•	•	•	•	I	10%	15	24	28	7-3
		20	•	•	•	•	•	•	•	•	•	C	10%	12	24	28	7-3
		20	•	•	•	•	•	•	•	•	•	I	10%	15	24	28	7-3
		20	•	•	•		•	•	•		•	M	10%	15	24	28	7-3
		20	•	•	•		•	•	•		•	M/883	10%	15	24	28	7-3
		25	•	•	•	•	•	•	•	•	•	C	10%	12	24	28	7-3
		25	•	•	•	•	•	•	•	•	•	I	10%	15	24	28	7-3
		25	•	•	•		•	•	•		•	M	10%	15	24	28	7-3
		25	•	•	•		•	•	•		•	M/883	10%	15	24	28	7-3
		30	•	•	•		•	•	•		•	M	10%	15	24	28	7-3
		30	•	•	•		•	•	•		•	M/883	10%	15	24	28	7-3
		35	•	•	•	•	•	•	•	•	•	C	10%	12	24	28	7-3
		35	•	•	•	•	•	•	•	•	•	I	10%	15	24	28	7-3
SMD Number																	
5962-8872401	500	25		•	•				•			M/883	10%	15	24	28	7-3
5962-8872402	500	30		•	•				•			M/883	10%	15	24	28	7-3
5962-8872403	500	40		•	•				•			M/883	10%	15	24	28	7-3
5962-8975504	500	20		•	•				•			M/883	10%	15	24	28	7-3
5962-8975501	500	25		•	•				•			M/883	10%	15	24	28	7-3
5962-8975502	500	30		•	•				•			M/883	10%	15	24	28	7-3
5962-8975503	500	40		•	•				•			M/883	10%	15	24	28	7-3

	Package Type
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, (-55°C to 125°C) Class B, Fully Compliant

CMOS EPLD Product Selection Guide

ATV750 Part Number	Approx. Gates	Speed (ns)	Package D	F	G	J	K	L	N	P	Y	Temp. Range	Power Supply	Icc (mA)	No. of Pins DIP	LCC	Page Number
ATV750	750	20	•	•	•	•	•	•	•	•	•	C	10%	120	24	28	7-19
		20	•	•	•	•	•	•	•	•	•	I	10%	140	24	28	7-19
		20	•	•	•		•	•	•		•	M	10%	140	24	28	7-19
		20	•	•	•		•	•	•		•	M/883	10%	140	24	28	7-19
		25	•	•	•	•	•	•	•	•	•	C	10%	120	24	28	7-19
		25	•	•	•	•	•	•	•	•	•	I	10%	140	24	28	7-19
		25	•	•	•		•	•	•		•	M	10%	140	24	28	7-19
		25	•	•	•		•	•	•		•	M/883	10%	140	24	28	7-19
		30	•	•	•	•	•	•	•	•	•	C	10%	120	24	28	7-19
		30	•	•	•	•	•	•	•	•	•	I	10%	140	24	28	7-19
		30	•	•	•		•	•	•		•	M	10%	140	24	28	7-19
		30	•	•	•		•	•	•		•	M/883	10%	140	24	28	7-19
		35	•	•	•	•	•	•	•	•	•	C	10%	120	24	28	7-19
		35	•	•	•	•	•	•	•	•	•	I	10%	140	24	28	7-19
		35	•	•	•		•	•	•		•	M	10%	140	24	28	7-19
		35	•	•	•		•	•	•		•	M/883	10%	140	24	28	7-19
		40	•	•	•	•	•	•	•	•	•	I	10%	140	24	28	7-19
		40	•	•	•		•	•	•		•	M	10%	140	24	28	7-19
		40	•	•	•		•	•	•		•	M/883	10%	140	24	28	7-19
SMD Number																	
5962-8872602	750	35	•					•				M/883	10%	140	24	28	7-19
5962-8872601	750	40	•					•				M/883	10%	140	24	28	7-19

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, (-55°C to 125°C) Class B, Fully Compliant

CMOS EPLD Product Selection Guide

ATV750L Part Number	Approx. Gates	Speed (ns)	Package D	F	G	J	K	L	N	P	Y	Temp. Range	Power Supply	Icc (mA)	No. of Pins DIP	LCC	Page Number
ATV750L	750	20	•	•	•	•	•	•	•	•	•	C	10%	120	24	28	7-19
		20	•	•	•	•	•	•	•	•	•	I	10%	140	24	28	7-19
		25	•	•	•	•	•	•	•	•	•	C	10%	120	24	28	7-19
		25	•	•	•	•	•	•	•	•	•	I	10%	140	24	28	7-19
		25	•	•	•		•	•	•		•	M	10%	140	24	28	7-19
		25	•	•	•		•	•	•		•	M/883	10%	140	24	28	7-19
		30	•	•	•	•	•	•	•	•	•	I	10%	140	24	28	7-19
		30	•	•	•		•	•	•		•	M	10%	140	24	28	7-19
		30	•	•	•		•	•	•		•	M/883	10%	140	24	28	7-19

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, (-55°C to 125°C) Class B, Fully Compliant

CMOS EPLD Product Selection Guide

ATV2500 Part Number	Approx. Gates	Speed (ns)	Package D	J	K	L	P	Temp. Range	Power Supply	Icc (mA)	No. of Pins DIP	LCC	Page Number
ATV2500	2500	30	•	•	•	•	•	C	10%	5	40	44	7-39
		35	•	•	•	•	•	C	10%	5	40	44	7-39
		35	•	•	•	•	•	I	10%	10	40	44	7-39
		35	•		•	•		M	10%	10	40	44	7-39
		35	•		•	•		M/883	10%	10	40	44	7-39
		40	•	•	•	•	•	C	10%	5	40	44	7-39
		40	•	•	•	•	•	I	10%	10	40	44	7-39
		40	•		•	•		M	10%	10	40	44	7-39
		40	•		•	•		M/883	10%	10	40	44	7-39
		45	•	•	•	•	•	I	10%	10	40	44	7-39
		45	•		•	•		M	10%	10	40	44	7-39
		45	•		•	•		M/883	10%	10	40	44	7-39

ATV2500H Part Number	Approx. Gates	Speed (ns)	Package D	J	K	L	P	Temp. Range	Power Supply	Icc (mA)	No. of Pins DIP	LCC	Page Number
ATV2500H	2500	25	•	•	•	•	•	C	10%	120	40	44	7-39
		25	•	•	•	•	•	I	10%	140	40	44	7-39
		25	•		•	•		M	10%	140	40	44	7-39
		25	•		•	•		M/883	10%	140	40	44	7-39
		30	•	•	•	•	•	C	10%	120	40	44	7-39
		30	•	•	•	•	•	I	10%	140	40	44	7-39
		30	•		•	•		M	10%	140	40	44	7-39
		30	•		•	•		M/883	10%	140	40	44	7-39
		35	•	•	•	•	•	C	10%	120	40	44	7-39
		35	•	•	•	•	•	I	10%	140	40	44	7-39
		35	•		•	•		M	10%	140	40	44	7-39
		35	•		•	•		M/883	10%	140	40	44	7-39

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, (-55°C to 125°C) Class B, Fully Compliant

CMOS EPLD Product Selection Guide

ATV5000 Part Number	Approx. Gates	Speed (ns)	Package J	Package K	Temperature Range	Power Supply	Icc (mA)	No. of Pins LCC	Page Number
ATV5000	5000	25	•	•	C	10%	40	68	7-57
	5000	30	•	•	C	10%	40	68	7-57
	5000	30	•	•	I	10%	50	68	7-57
	5000	30		•	M	10%	50	68	7-57
	5000	30		•	M/883	10%	50	68	7-57
	5000	35	•	•	I	10%	50	68	7-57
	5000	35		•	M	10%	50	68	7-57
	5000	35		•	M/883	10%	50	68	7-57

Package Type	
J	68J, 68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	68KW, 68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS Analog Product Selection Guide

AT76C10 Part Number	Delay (ms)	Gain (dB)	Bandwidth (KHz)	Package D	Package P	Package S	Temp. Range	Power Supply	No. of Pins DIP	No. of Pins SOIC	Page Number
AT76C10	1.8	31.5	4		•	•	C	10%	16	16	9-3
	1.8	31.5	4		•	•	I	10%	16	16	9-3
	1.8	31.5	4	•			M	5%	16	16	9-3

AT76C10E Part Number	Delay (ms)	Gain (dB)	Bandwidth (KHz)	Package D	Package P	Package S	Temp. Range	Power Supply	No. of Pins DIP	No. of Pins SOIC	Page Number
AT76C10E	1.8	31.5	4		•	•	C	10%	16	16	9-11
	1.8	31.5	4		•	•	I	10%	16	16	9-11
	1.8	31.5	4	•			M	5%	16	16	9-11

	Package Type
D	16D3, 16 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
P	16P3, 16 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
S	16S, 16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

CMOS Analog Product Selection Guide

AT76C120 Part Number	Organization	Speed (kHz)	Signal-to-Noise (dB)	Accuracy (bits)	Package D	Package P	Temp. Range	Power Supply	No. of Pins DIP	Page Number
AT76C120-1	Dual 16/18-bit A/D	96	90	15		•	C	10%	24	9-19
	Dual 16/18-bit A/D	96	90	15		•	I	10%	24	9-19
	Dual 16/18-bit A/D	96	90	15	•		M	5%	24	9-19
AT76C120-2	Dual 16/18-bit A/D	96	84	13		•	C	10%	24	9-19
	Dual 16/18-bit A/D	96	84	13		•	I	10%	24	9-19
	Dual 16/18-bit A/D	96	84	13	•		M	5%	24	9-19

	Package Type
D	24D6, 24 Lead, 0.600" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

CMOS Analog Product Selection Guide

AT76C171 Part Number	Organization D/A	Organization RAM	Speed (MHz)	Package D	Package J	Package P	Temp. Range	Power Supply	No. of Pins DIP	No. of Pins LCC	Page Number
AT76C171	Triple 6-bit	256x18	35		•	•	C	10%	28	32	9-27
	Triple 6-bit	256x18	35		•	•	I	10%	28	32	9-27
	Triple 6-bit	256x18	35	•			M	5%	28	32	9-27
	Triple 6-bit	256x18	50		•	•	C	10%	28	32	9-27
	Triple 6-bit	256x18	50		•	•	I	10%	28	32	9-27

AT76C176 Part Number	Organization D/A	Organization RAM	Speed (MHz)	Package D	Package J	Package P	Temp. Range	Power Supply	No. of Pins DIP	No. of Pins LCC	Page Number
AT76C176	Triple 6-bit	256x18	40		•	•	C	10%	28	32	9-39
	Triple 6-bit	256x18	40		•	•	I	10%	28	32	9-39
	Triple 6-bit	256x18	40	•			M	5%	28	32	9-39
	Triple 6-bit	256x18	50		•	•	C	10%	28	32	9-39
	Triple 6-bit	256x18	50		•	•	I	10%	28	32	9-39
	Triple 6-bit	256x18	66		•	•	C	5%	28	32	9-39

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

CMOS Analog Product Selection Guide

AT76C176A	Organization		Speed	Package				Temp.	Power	No. of Pins		Page
Part Number	D/A	RAM	(MHz)	D	J1	J2	P	Range	Supply	DIP	LCC	Number
AT76C176A	Triple 6-bit	256x18	50		•	•	•	C	10%	28	32, 44	9-51
	Triple 6-bit	256x18	50		•	•	•	I	10%	28	32, 44	9-51
	Triple 6-bit	256x18	50	•				M	5%	28	32, 44	9-51
	Triple 6-bit	256x18	66		•	•	•	C	10%	28	32, 44	9-51
	Triple 6-bit	256x18	66		•	•	•	I	10%	28	32, 44	9-51
	Triple 6-bit	256x18	66	•				M	5%	28	32, 44	9-51
	Triple 6-bit	256x18	80		•	•	•	C	10%	28	32, 44	9-51
	Triple 6-bit	256x18	80		•	•	•	I	10%	28	32, 44	9-51
	Triple 6-bit	256x18	110		•	•	•	C	5%	28	32, 44	9-51

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J1	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
J2	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

Explanation of Atmel's Part Number Code

All Atmel part numbers begin with the prefix "AT." The next four to nine digits are the part number. In addition, Atmel parts can be ordered in particular speeds, in specific packages, for particular temperature ranges and with the option of 883C level B military compliance. The available options for each part are listed at the back of its data sheet in its "Ordering Information" table. These options are designated by the following suffixes placed at the end of the Atmel part number, in the order given:

Prefix	Device	Suffix
AT	XXXXX	X X X X

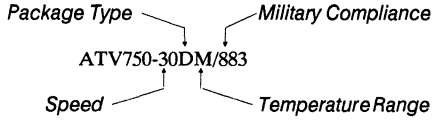
Processing
- Blank = Standard
- /883 = MIL-STD-883, Class B Fully Compliant

Temperature Range
- C = Com Temp (0°C to 70°C)
- I = Ind Temp (-40°C to 85°C)
- M = Mil Temp (-55°C to 125°C)

Package
- B = Ceramic Side Braze Dual Inline
- C = Cerpack
- D = Cerdip
- F = Flatpack
- G = Cerdip, One Time Programmable
- J = PLCC J-Lead Chip Carrier
- K = J-Lead Cequad
- L = Leadless Chip Carrier
- M = Ceramic Module
- N = Leadless Chip Carrier, One Time Programmable
- P = Plastic DIP
- R = SOIC
- S = SOIC
- T = SOIC
- U = PGA
- X = Plastic J-leaded SOIC
- Y = Cerpack

Speed

Here is an example of how to designate a part number:



CONTENTS

Section 2

CMOS E^2PROMS

16K (2K x 8) High Speed CMOS E^2PROM

Features

- Fast Read Access Time - 45ns
- Fast Byte Write - 1ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - DATA POLLING
- Low Power
  - 80mA Active Current
  - 500µA CMOS Standby Current (28HC16L)
- High Reliability CMOS Technology
  - Endurance: 10^4 cycles
  - Data Retention: 10 years
- 5 V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

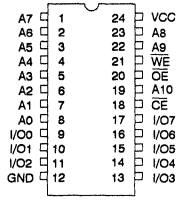
The AT28HC16/16L is a high-speed, low-power Electrically Erasable and Programmable Read Only Memory. The device is optimized for high speed applications, featuring access times to 45ns. Its 16k of memory is organized as 2,048 words by 8 bits. The AT28HC16/16L comes in a space saving 24 pin DIP.

The AT28HC16/16L is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device being written will go to a busy state and automatically clear and write the latched data using an internal control timer. Data polling of I/O7 may be used to detect the end of the write cycle. Once a write cycle has been completed, a new access for a read or a write may begin immediately.

Atmel's high-speed CMOS technology is used to achieve access times of 45ns for the AT28HC16 with under 440mW of power dissipation. The AT28HC16L offers ultra low standby power consumption of under 2.75mW at access time to 55ns.

The AT28HC16/16L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and for improved data retention characteristics. An extra 16 bytes of E^2PROM are available for device identification or tracking.

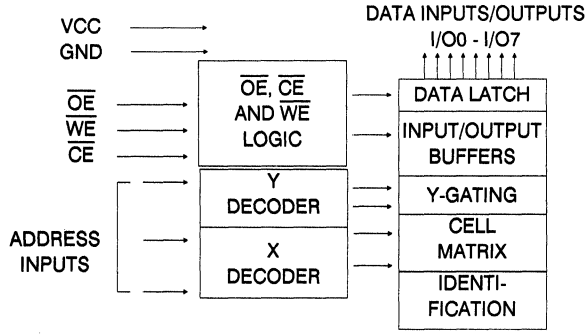
Pin Configurations



PIN NAMES

A0 - A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Block Diagram



Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. V_H = 12.0 ± 0.5V.

Device Operation

READ: The AT28HC16/16L is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28HC16/16L is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

$\overline{DATA}$ POLLING: The AT28HC16/16L provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) Vcc sense – if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay – once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles. (d) Noise Protection – a $\overline{WE}$ or $\overline{CE}$ pulse of less than 10ns (typical) will not initiate a write cycle.

CHIP CLEAR: The contents of the entire memory of the AT28HC16/16L may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: In the AT28HC16/16L there are an extra 16 bytes of E^2PROM memory available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7F0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

D.C. and A.C. Operating Range

		AT28HC16-45	AT28HC16L-55	AT28HC16-55	AT28HC16-70 AT28HC16L-70	AT28HC16-90 AT28HC16L-90
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.			-55°C - 125°	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3V to V_{CC} + 1.0V (AT28HC16L)			500	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V	AT28HC16L		3	mA
		to V_{CC} + 1.0V	AT28HC16		60	mA
I_{CC}	V_{CC} Active Current A.C	f = 10MHz; I_{out} = 0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 12mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0mA		2.4		V

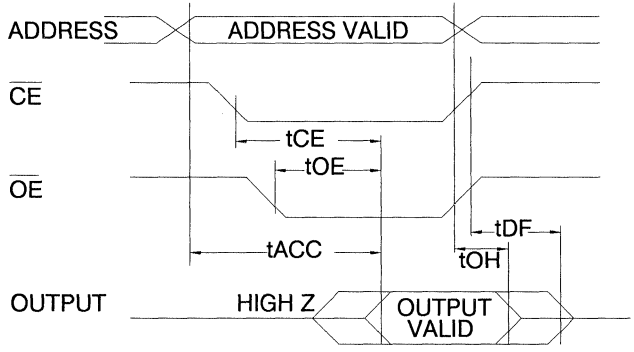
Pin Capacitance (f = 1MHz T = 25°C) [5]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics [1]

Symbol		28HC16-45 Min	28HC16-45 Max	28HC16-55 Min	28HC16-55 Max	28HC16L-55 Min	28HC16L-55 Max	28HC16-70 Min	28HC16-70 Max	28HC16L-70 Min	28HC16L-70 Max	28HC16L-90 Min	28HC16L-90 Max	Units
t_{ACC}	Address to Output Delay		45		55		55		70		70		90	ns
t_{CE}[2]	$\overline{CE}$ to Output Delay		30		40		55		50		70		90	ns
t_{OE}[3]	$\overline{OE}$ to Output Delay	0	30	0	40	0	40	0	50	0	50	0	50	ns
t_{DF}[4,5]	$\overline{OE}$ to Output Float	0	30	0	40	0	40	0	50	0	50	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$ or Address, whichever occurred first	0		0		0		0		0		0		ns

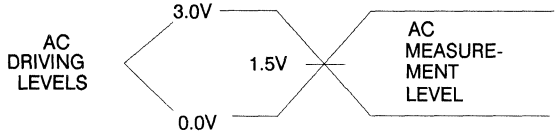
A.C. Read Waveforms



Notes:

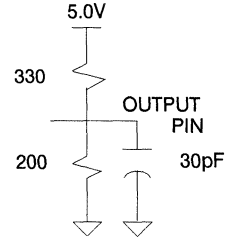
1. C_L = 30pF.
2. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
5. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

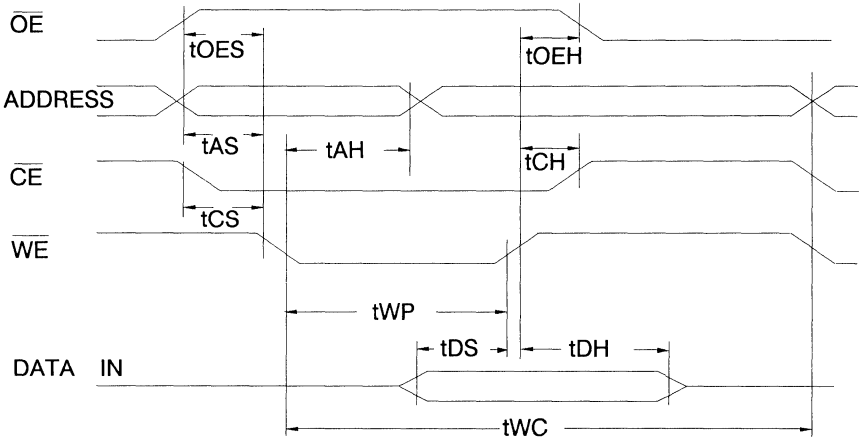
Output Test Load



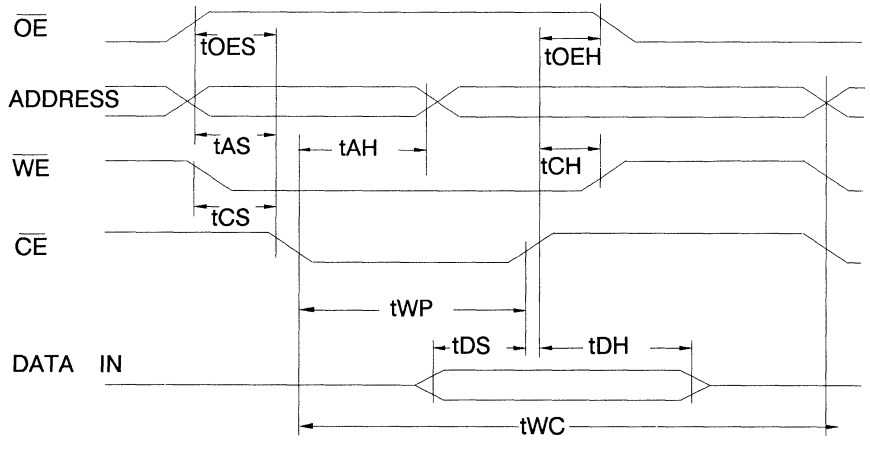
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{WC}	Write Cycle Time		0.5	1.0	ms

A.C. Write Waveforms - $\overline{WE}$ Controlled



A.C. Write Waveforms - $\overline{CE}$ Controlled

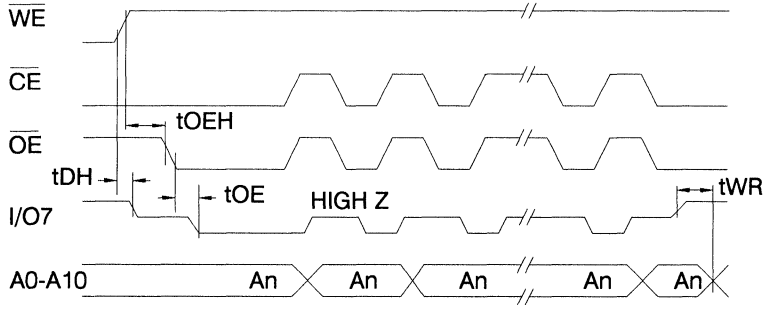


$\overline{\text{Data}}$ Polling Characteristics [1]

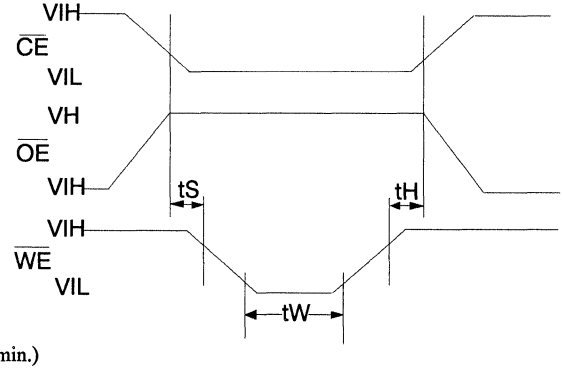
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms



Chip Erase Waveforms

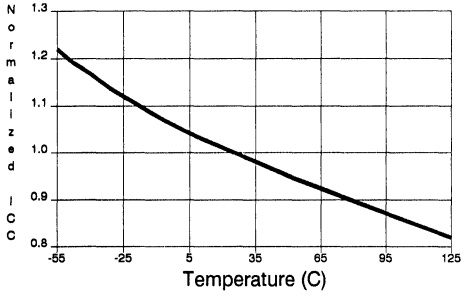


$t_S = t_H = 1\mu sec$ (min.)

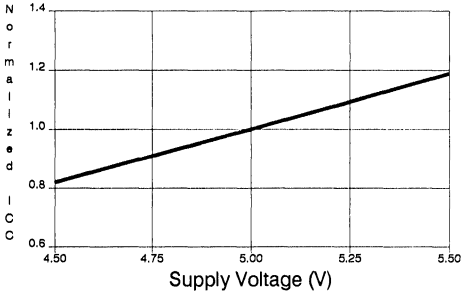
$t_W = 10msec$ (min.)

$V_H = 12 \pm 0.5V$

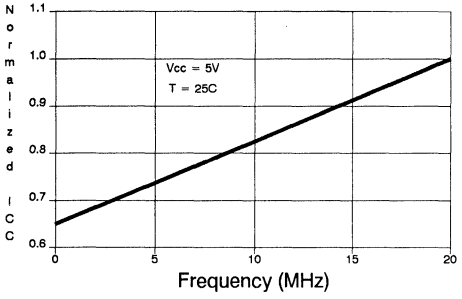
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	80	60	AT28HC16N-45DC AT28HC16-45DC AT28HC16N-45PC AT28HC16-45PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16N-45DI AT28HC16-45DI AT28HC16N-45PI AT28HC16-45PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
55	80	60	AT28HC16N-55DC AT28HC16-55DC AT28HC16N-55PC AT28HC16-55PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16N-55DI AT28HC16-55DI AT28HC16N-55PI AT28HC16-55PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16N-55DM AT28HC16-55DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16N-55DM/883 AT28HC16-55DM/883	24D3 24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	80	60	AT28HC16N-70DC AT28HC16-70DC AT28HC16N-70PC AT28HC16-70PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16N-70DI AT28HC16-70DI AT28HC16N-70PI AT28HC16-70PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16N-70DM AT28HC16-70DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16N-70DM/883 AT28HC16-70DM/883	24D3 24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	60	AT28HC16N-90DC AT28HC16-90DC AT28HC16N-90PC AT28HC16-90PC AT28HC16-90W	24D3 24D6 24P3 24P6 DIE	Commercial (0°C to 70°C)
			AT28HC16N-90DI AT28HC16-90DI AT28HC16N-90PI AT28HC16-90PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	60	AT28HC16N-90DM AT28HC16-90DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16N-90DM/883 AT28HC16-90DM/883	24D3 24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)

	Package Type
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	80	0.5	AT28HC16LN-55DC AT28HC16L-55DC AT28HC16LN-55PC AT28HC16L-55PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16LN-55DI AT28HC16L-55DI AT28HC16LN-55PI AT28HC16L-55PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16LN-55DM AT28HC16L-55DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16LN-55DM/883 AT28HC16L-55DM/883	24D3 24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	80	0.5	AT28HC16LN-70DC AT28HC16L-70DC AT28HC16LN-70PC AT28HC16L-70PC AT28HC16L-70W	24D3 24D6 24P3 24P6 DIE	Commercial (0°C to 70°C)
			AT28HC16LN-70DI AT28HC16L-70DI AT28HC16LN-70PI AT28HC16L-70PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16LN-70DM AT28HC16L-70DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16LN-70DM/883 AT28HC16L-70DM/883	24D3 24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	0.5	AT28HC16LN-90DC AT28HC16L-90DC AT28HC16LN-90PC AT28HC16L-90PC AT28HC16L-90W	24D3 24D6 24P3 24P6 DIE	Commercial (0°C to 70°C)
			AT28HC16LN-90DI AT28HC16L-90DI AT28HC16LN-90PI AT28HC16L-90PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16LN-90DM AT28HC16L-90DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16LN-90DM/883 AT28HC16L-90DM/883	24D3 24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

	Package Type
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die

64K (8K x 8) High Speed CMOS E^2PROM

Features

- **Fast Read Access Time - 55ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 32 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Maximum Page Write Cycle Time: 2ms**
  - **1 to 32 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80mA Active Current**
  - **100µA CMOS Standby Current**
- **Direct Microprocessor Control**
  - **$\overline{\text{DATA}}$ Polling**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

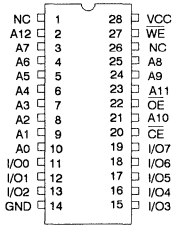
Description

The AT28HC64/L is a high-speed, low-power Electrically Erasable and Programmable Read Only Memory. Its 64k of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 55ns with power dissipation of just 440mW. When the device is deselected the standby current is less than 100µA.

The AT28HC64/L is accessed like a Static RAM for the read or write cycles without the need for external components. The device contains a 32-byte page register to allow writing of up to 32 bytes simultaneously. During a write cycle, the addresses and 1 to 32 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

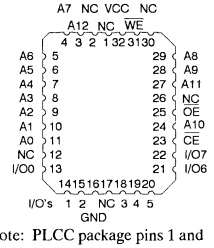
Atmel's 28HC64/L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. The AT28HC64/L also includes an extra 32 bytes of E^2PROM for device identification or tracking.

Pin Configurations



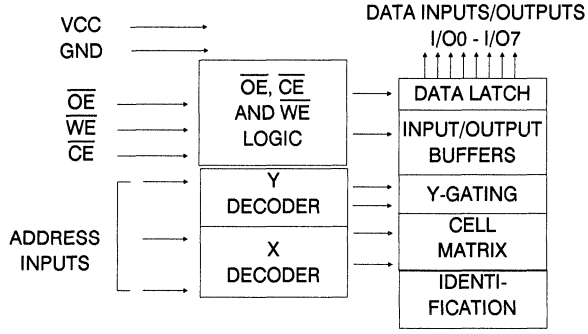
PIN NAMES

A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. V_H = 12.0 ± 0.5V.

Device Operation

READ: The AT28HC64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28HC64 allows one to 32 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded, successive bytes may be loaded in the same manner. Each byte to be written must be loaded into the AT28HC64 within 150µs of the first byte. A5 to A12 determine the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A4 are used to specify which bytes within the page are to be written. All bytes to be written must share the same page address. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28HC64 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28HC64 in the following ways: (a) Vcc sense – if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay – once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter – pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

CHIP CLEAR: The contents of the entire memory of the AT28HC64 may be set to the high state by the use of the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10ms low pulse is applied to the $\overline{WE}$ pin.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 +/-0.5V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28HC64-55	AT28HC64L-70	AT28HC64-70	AT28HC64-90 AT28HC64L-90	AT28HC64-12 AT28HC64L-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.			-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ±10%	5V ±10%	5V ±10%	5V ±10%	5V ±10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-.3V to V_{CC} + 1V	Com.,Ind.		100	µA
		AT28HC64L	Mil.		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V	AT28HC64L		3	mA
		to V_{CC} + 1V	AT28HC64		60	mA
I_{CC}	V_{CC} Active Current	f = 10MHz; I_{OUT} = 0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 4mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0mA		2.4		V

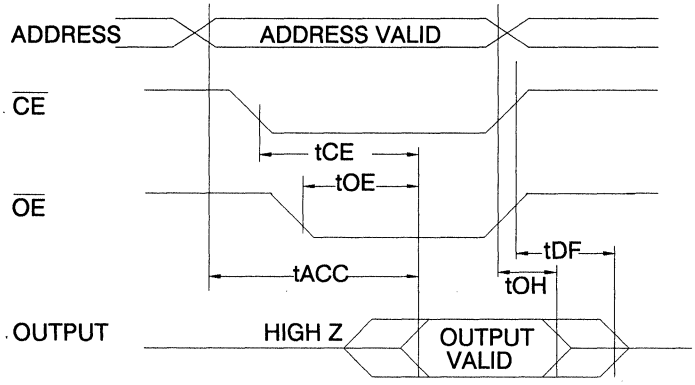
Pin Capacitance (f = 1MHz T = 25°C) [5]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics [1]

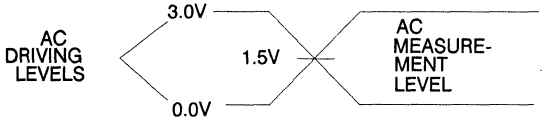
Symbol	Parameter	28HC64-55 Min	28HC64-55 Max	28HC64-70 Min	28HC64-70 Max	28HC64L-70 Min	28HC64L-70 Max	28HC64-90 Min	28HC64-90 Max	28HC64L-90 Min	28HC64L-90 Max	28HC64L-12 Min	28HC64L-12 Max	Units
t_{ACC}	Address to Output Delay		55		70		70		90		90		120	ns
t_{CE}[2]	$\overline{CE}$ to Output Delay		55		70		70		90		90		120	ns
t_{OE}[3]	$\overline{OE}$ to Output Delay	0	30	0	35	0	35	0	40	0	40	0	50	ns
t_{DF}[4,5]	$\overline{OE}$ to Output Float	0	30	0	35	0	35	0	40	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		0		0		ns

A.C. Read Waveforms



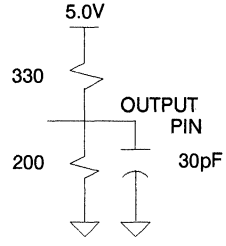
Notes:
1. C_L = 30pF.
2. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
5. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

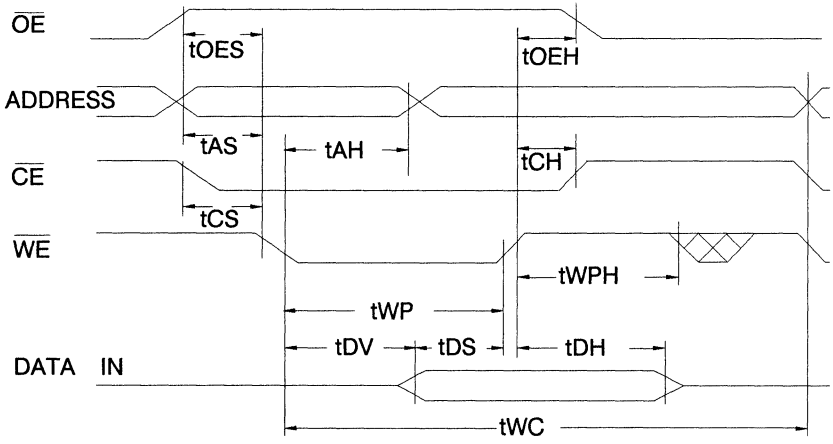
Output Test Load



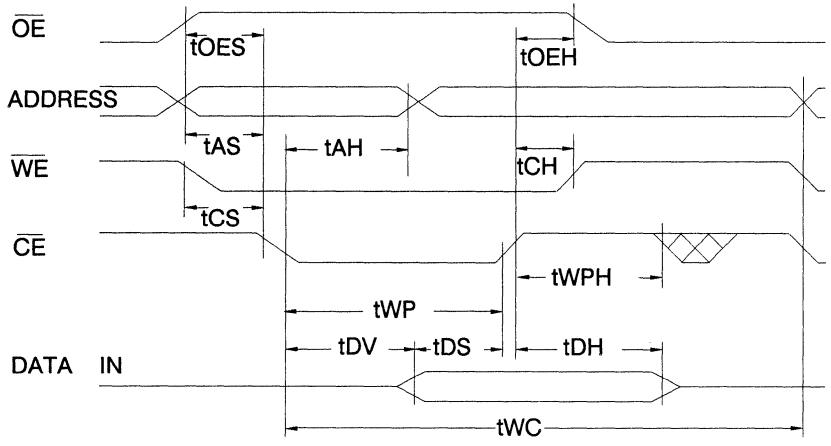
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{DV}	Time to Data Valid			1	µs
t_{WC}	Write Cycle Time		1.0	2.0	ms

A.C. Write Waveforms - $\overline{WE}$ Controlled



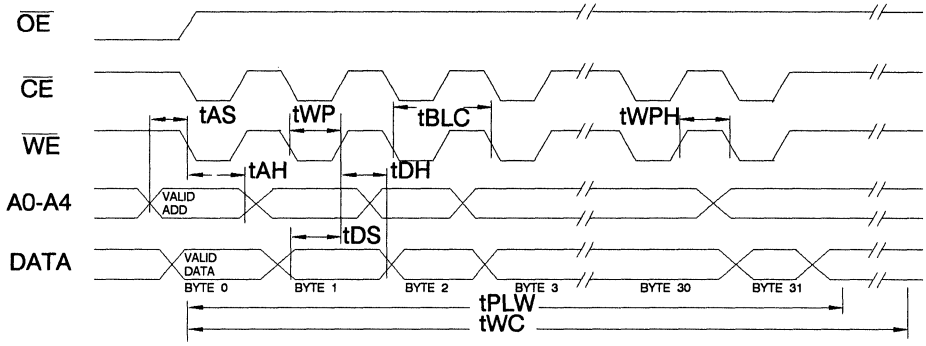
A.C. Write Waveforms - $\overline{CE}$ Controlled



Page Mode Write Characteristics

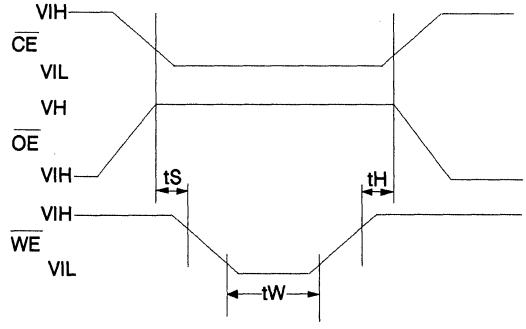
Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		1	2.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100		1000	ns
t_{BLC}	Byte Load Cycle Time	150			ns
t_{PLW}	Page Load Width			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms



Note: A5 through A12 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms



$t_S = t_H = 1\mu sec$ (min.)

$t_W = 10msec$ (min.)

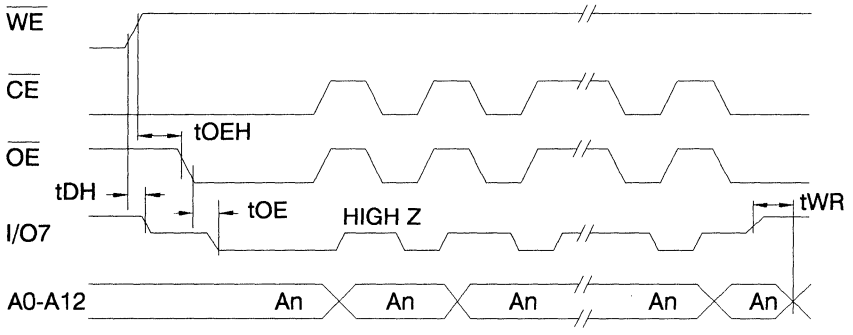
$V_H = 12 \pm 0.05$

$\overline{\text{Data}}$ Polling Characteristics [1]

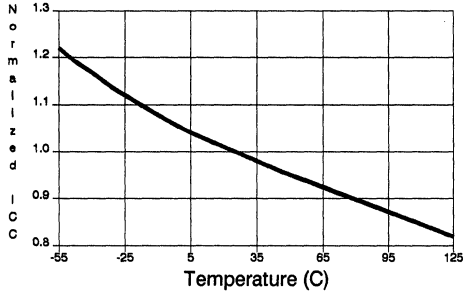
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			50	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

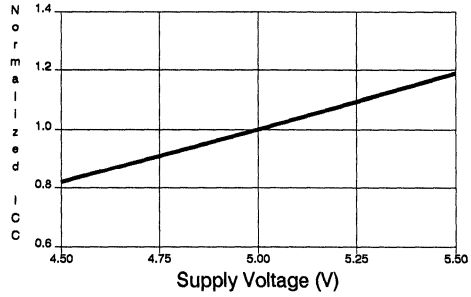
$\overline{\text{DATA}}$ Polling Waveforms



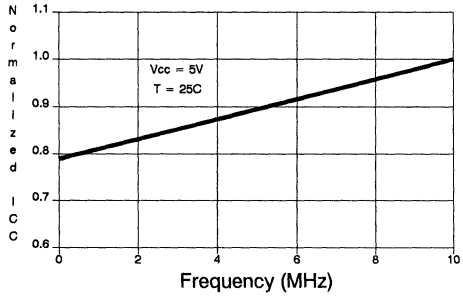
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	80	60	AT28HC64(E)-55DC AT28HC64(E)-55LC AT28HC64(E)-55PC	28D6 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-55DI AT28HC64(E)-55LI AT28HC64(E)-55PI	28D6 32L 28P6	Industrial (-40°C to 85°C)
70	80	60	AT28HC64(E)-70DC AT28HC64(E)-70JC AT28HC64(E)-70LC AT28HC64(E)-70PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-70DI AT28HC64(E)-70JI AT28HC64(E)-70LI AT28HC64(E)-70PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
			AT28HC64(E)-70DM AT28HC64(E)-70LM	28D6 32L	Military (-55°C to 125°C)
			AT28HC64(E)-70DM/883 AT28HC64(E)-70LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	60	AT28HC64(E)-90DC AT28HC64(E)-90JC AT28HC64(E)-90LC AT28HC64(E)-90PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-90DI AT28HC64(E)-90JI AT28HC64(E)-90LI AT28HC64(E)-90PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
			AT28HC64(E)-90DM AT28HC64(E)-90LM	28D6 32L	Military (-55°C to 125°C)
			AT28HC64(E)-90DM/883 AT28HC64(E)-90LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	60	AT28HC64(E)-12DC AT28HC64(E)-12JC AT28HC64(E)-12LC AT28HC64(E)-12PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-12DI AT28HC64(E)-12JI AT28HC64(E)-12LI AT28HC64(E)-12PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
			AT28HC64(E)-12DM AT28HC64(E)-12LM	28D6 32L	Military (-55°C to 125°C)
			AT28HC64(E)-12DM/883 AT28HC64(E)-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2ms
E	High Endurance Option: Endurance = 100K Write Cycles

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	0.1	AT28HC64L(E)-70DC AT28HC64L(E)-70LC AT28HC64L(E)-70PC	28D6 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64L(E)-70DI AT28HC64L(E)-70LI AT28HC64L(E)-70PI	28D6 32L 28P6	Industrial (-40°C to 85°C)
90	80	0.1	AT28HC64L(E)-90DC AT28HC64L(E)-90JC AT28HC64L(E)-90LC AT28HC64L(E)-90PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64L(E)-90DI AT28HC64L(E)-90JI AT28HC64L(E)-90LI AT28HC64L(E)-90PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
90	80	0.2	AT28HC64L(E)-90DM AT28HC64L(E)-90LM	28D6 32L	Military (-55°C to 125°C)
			AT28HC64L(E)-90DM/883 AT28HC64L(E)-90LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.1	AT28HC64L(E)-12DC AT28HC64L(E)-12JC AT28HC64L(E)-12LC AT28HC64L(E)-12PC AT28HC64L-12W	28D6 32J 32L 28P6 DIE	Commercial (0°C to 70°C)
			AT28HC64L(E)-12DI AT28HC64L(E)-12JI AT28HC64L(E)-12LI AT28HC64L(E)-12PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
120	80	0.2	AT28HC64L(E)-12DM AT28HC64L(E)-12LM	28D6 32L	Military (-55°C to 125°C)
			AT28HC64L(E)-12DM/883 AT28HC64L(E)-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	80	0.2	5962-87514 12 UX 5962-87514 12 XX 5962-87514 12 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	0.2	5962-87514 11 UX 5962-87514 11 XX 5962-87514 11 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.2	5962-87514 10 UX 5962-87514 10 XX 5962-87514 10 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

	Package Type
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32K	32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
	Options
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2ms
E	High Endurance Option: Endurance = 100K Write Cycles

256K (32K x 8) High Speed CMOS E^2PROM

Features

- **Fast Read Access Time - 70ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 64 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Page Write Cycle Time: 10ms or 3ms maximum**
  - **1 to 64 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80mA Active Current**
  - **3mA Standby Current (AT28HC256L)**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

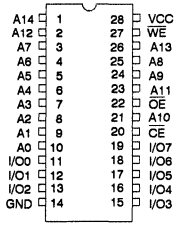
Description

The AT28HC256/L is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256k of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the AT28HC256 offers access times to 70ns with power dissipation of just 440mW. When the AT28HC256L is deselected, the standby current is less than 5mA.

The AT28HC256/L is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the addresses and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

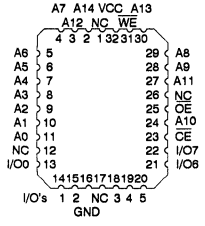
Atmel's 28HC256/L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of E^2PROM for device identification or tracking.

Pin Configurations



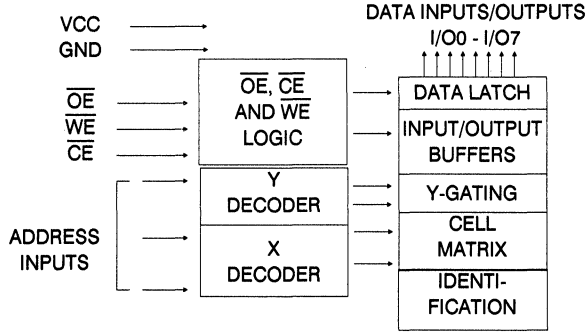
PIN NAMES

A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Device Operation

READ: The AT28HC256/L is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28HC256/L allows one to 64 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end, and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28HC256/L features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28HC256/L provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling, and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28HC256/L in the following ways: (a) Vcc sense– if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay– once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit– holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter– pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28HC256/L. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

DEVICE IDENTIFICATION: An extra 64 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to $12 \pm 0.5V$ and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28HC256-70	AT28HC256L-90	AT28HC256-90	AT28HC256-12 AT28HC256L-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.			-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. V_H = 12.0 ± 0.5V.

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V	AT28HC256L		3	mA
			AT28HC256		60	mA
I_{SB2}	V_{CC} Standby Current CMOS	$\overline{CE}$ = -0.3V to V_{CC} + 1V	AT28HC256L		300	µA
I_{CC}	V_{CC} Active Current	f = 5MHz; I_{OUT} = 0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 6.0mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -4mA		2.4		V

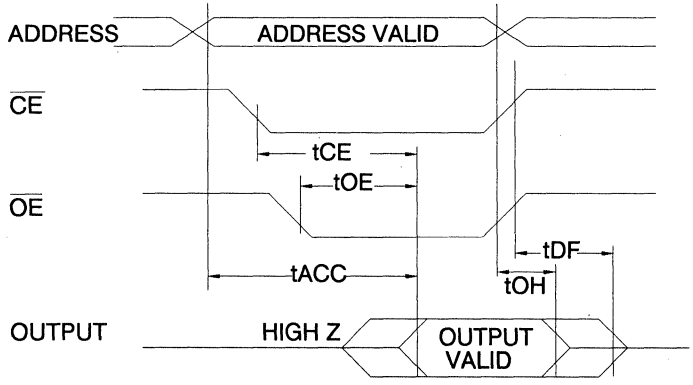
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

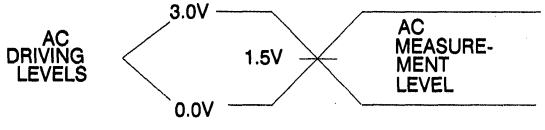
		AT28HC256-70		AT28HC256-90 AT28HC256L-90		AT28HC256-12 AT28HC256L-12		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
t_{ACC}	Address to Output Delay		70		90		120	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		70		90		120	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	ns
t_{DF}[3,4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	35	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



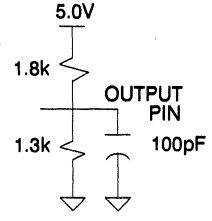
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load

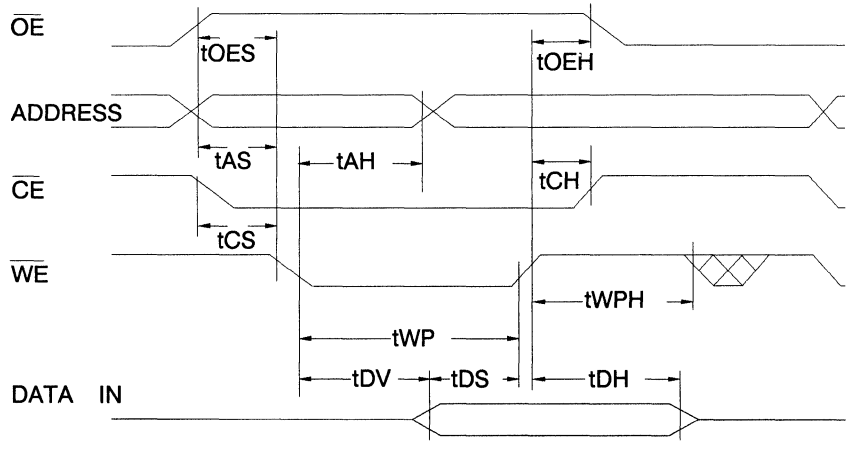


A.C. Write Characteristics

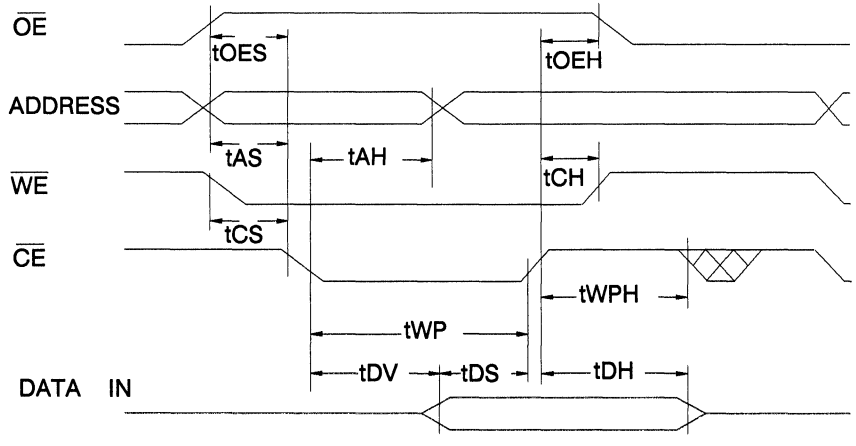
		Symbol	Parameter	Min
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR(1)		
t_{WC}	Write Cycle Time AT28HC256		10	ms
	AT28HC256F		3.0	ms

Note: 1. NR = No Restriction

A.C. Write Waveforms - $\overline{WE}$ Controlled



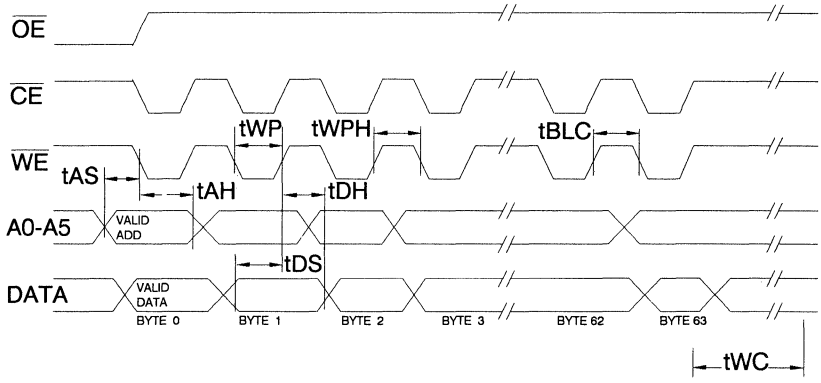
A.C. Write Waveforms - $\overline{CE}$ Controlled



Page Mode Write Characteristics

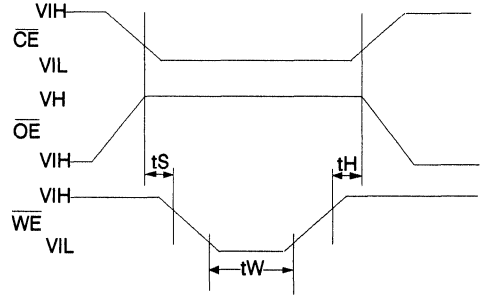
Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time AT28HC256		5	10	ms
	AT28HC256F		2	3.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100			ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms



Note: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

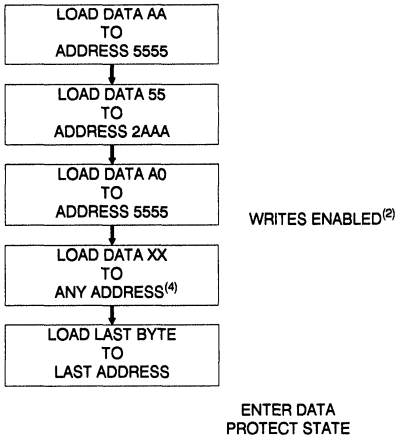


$t_S = t_H = 5\mu sec$ (min.)

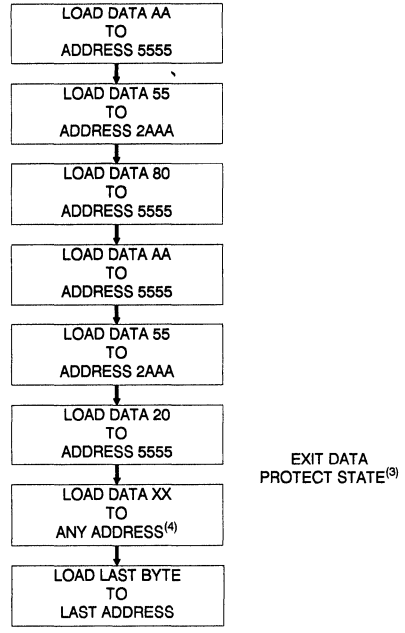
$t_W = 10msec$ (min.)

$V_H = 12 \pm 0.5V$

Software Data Protection Enable Algorithm [1]

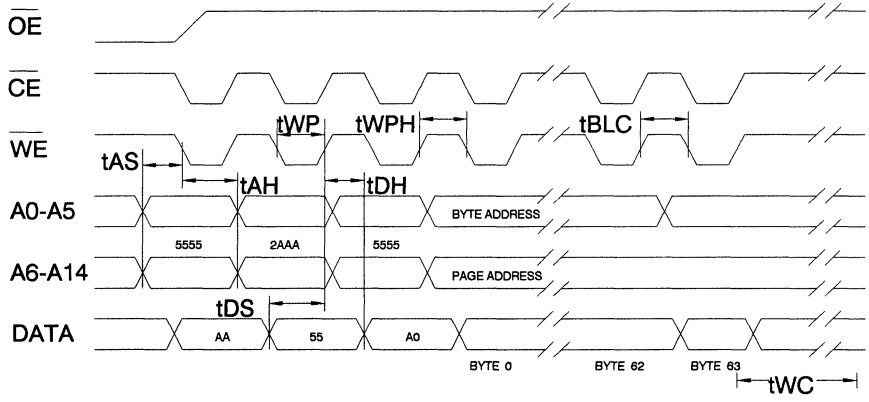


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data may be loaded.

Software Protected Write Cycle Waveforms



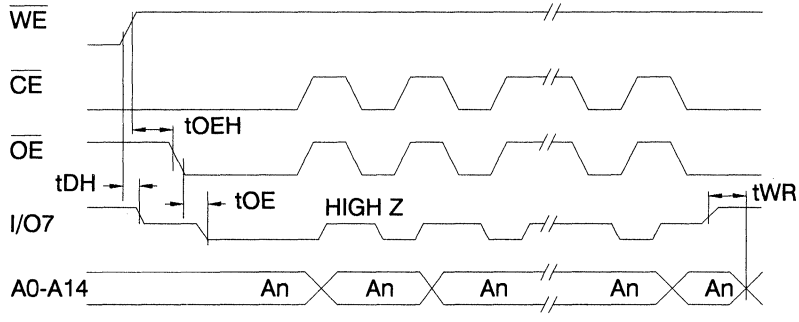
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{DATA}}$ Polling Waveforms

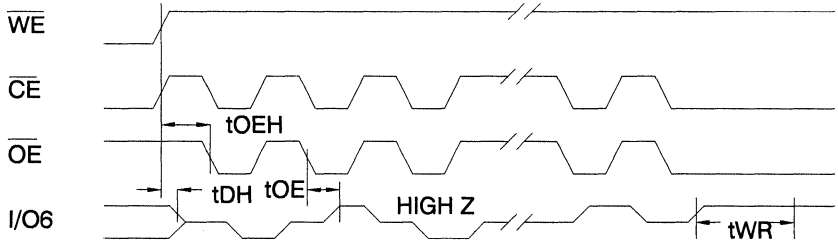


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

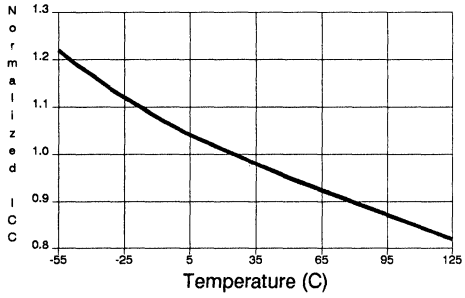
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

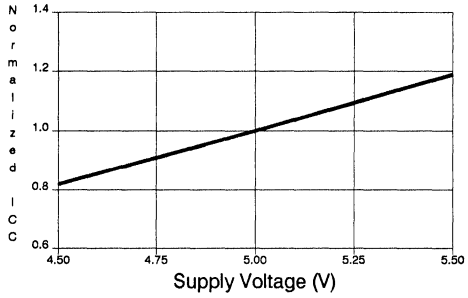


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

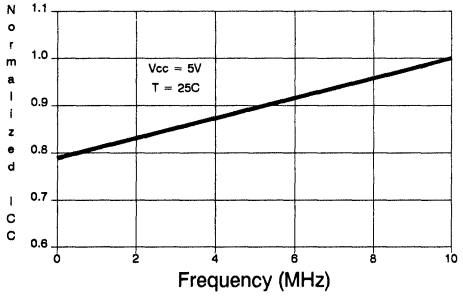
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	60	AT28HC256(E,F)-70DC AT28HC256(E,F)-70LC AT28HC256(E,F)-70PC	28D6 32L 28P6	Commercial (0°C to 70°C)
			AT28HC256(E,F)-70DI AT28HC256(E,F)-70LI AT28HC256(E,F)-70PI	28D6 32L 28P6	Industrial (-40°C to 85°C)
90	80	60	AT28HC256(E,F)-90DC AT28HC256(E,F)-90FC AT28HC256(E,F)-90JC AT28HC256(E,F)-90LC AT28HC256(E,F)-90PC AT28HC256(E,F)-90UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256(E,F)-90DI AT28HC256(E,F)-90FI AT28HC256(E,F)-90JI AT28HC256(E,F)-90LI AT28HC256(E,F)-90PI AT28HC256(E,F)-90UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256(E,F)-90DM AT28HC256(E,F)-90FM AT28HC256(E,F)-90LM AT28HC256(E,F)-90UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28HC256(E,F)-90DM/883 AT28HC256(E,F)-90FM/883 AT28HC256(E,F)-90LM/883 AT28HC256(E,F)-90UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	60	AT28HC256(E,F)-12DC AT28HC256(E,F)-12FC AT28HC256(E,F)-12JC AT28HC256(E,F)-12LC AT28HC256(E,F)-12PC AT28HC256(E,F)-12UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256(E,F)-12DI AT28HC256(E,F)-12FI AT28HC256(E,F)-12JI AT28HC256(E,F)-12LI AT28HC256(E,F)-12PI AT28HC256(E,F)-12UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	60	AT28HC256(E,F)-12DM AT28HC256(E,F)-12FM AT28HC256(E,F)-12LM AT28HC256(E,F)-12UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28HC256(E,F)-12DM/883 AT28HC256(E,F)-12FM/883 AT28HC256(E,F)-12LM/883 AT28HC256(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	60	5962-88634 03 UX 5962-88634 03 XX 5962-88634 03 YX 5962-88634 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88634 04 UX 5962-88634 04 XX 5962-88634 04 YX 5962-88634 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3ms

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT28HC256L(E,F)-90DC AT28HC256L(E,F)-90FC AT28HC256L(E,F)-90JC AT28HC256L(E,F)-90LC AT28HC256L(E,F)-90PC AT28HC256L(E,F)-90UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256L(E,F)-90DI AT28HC256L(E,F)-90FI AT28HC256L(E,F)-90JI AT28HC256L(E,F)-90LI AT28HC256L(E,F)-90PI AT28HC256L(E,F)-90UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
120	80	0.3	AT28HC256L(E,F)-12DC AT28HC256L(E,F)-12FC AT28HC256L(E,F)-12JC AT28HC256L(E,F)-12LC AT28HC256L(E,F)-12PC AT28HC256L(E,F)-12UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256L(E,F)-12DI AT28HC256L(E,F)-12FI AT28HC256L(E,F)-12JI AT28HC256L(E,F)-12LI AT28HC256L(E,F)-12PI AT28HC256L(E,F)-12UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256L(E,F)-12DM AT28HC256L(E,F)-12FM AT28HC256L(E,F)-12LM AT28HC256L(E,F)-12UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28HC256L(E,F)-12DM/883 AT28HC256L(E,F)-12FM/883 AT28HC256L(E,F)-12LM/883 AT28HC256L(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-88634 01 UX 5962-88634 01 XX 5962-88634 01 YX 5962-88634 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88634 02 UX 5962-88634 02 XX 5962-88634 02 YX 5962-88634 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3ms

4K (512 x 8) CMOS E²PROM

Features

- **Fast Read Access Time - 150ns**
- **Fast Byte Write - 200μs or 1 ms**
- **Self-Timed Byte Write Cycle**
  - **Internal Address and Data Latches**
  - **Internal Control Timer**
  - **Automatic Clear Before Write**
- **Direct Microprocessor Control**
  - **$\overline{\text{DATA}}$ POLLING**
- **Low Power**
  - **30mA Active Current**
  - **100μa CMOS Standby Current**
- **High Reliability**
  - **Endurance: 10^4 or 10^5 cycles**
  - **Data Retention: 10 years**
- **5V ± 10% Supply**
- **CMOS & TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

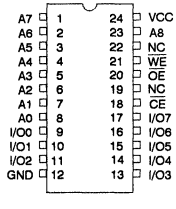
Description

The AT28C04 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C04 is a 4k memory organized as 512 words x 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

The AT28C04 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by $\overline{\text{DATA}}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150ns at low power dissipation. When the chip is deselected the standby current is less than 100μA. Atmel's 28C04 has additional features to ensure high quality and manufacturability, including internal error correction for extended endurance and for improved data retention characteristics.

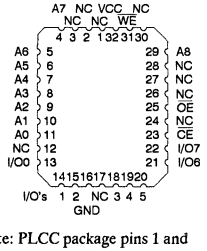
Pin Configurations



PIN NAMES

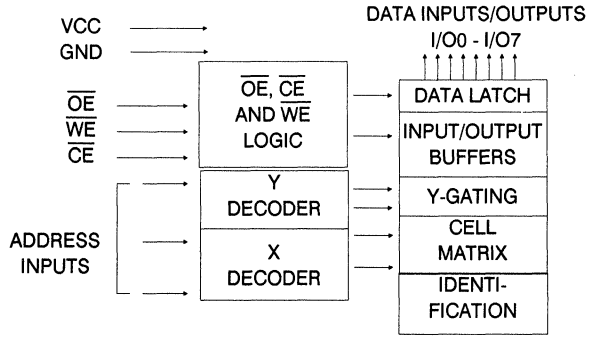
A0 - A10	Address
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Top Views



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. $V_H = 12.0 \pm 0.5V$.

Device Operation

READ: The AT28C04 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C04 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C04F offers a byte write time of 200μs maximum. This feature allows the entire device to be rewritten in 0.1 seconds.

$\overline{DATA}$ POLLING: The AT28C04 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense – if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay – once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C04 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

Absolute Maximum Ratings*

Temperature Under Bias..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground.....-0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

D.C. and A.C. Operating Range

		AT28C04-15	AT28C04-20	AT28C04-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ±10%	5V ±10%	5V ±10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V	Com.		2	mA
		to V_{CC} + 1.0V	Ind., Mil.		3	mA
I_{CC}	V_{CC} Active Current A.C.	f = 5MHz; I_{out} = 0mA	Com.		30	mA
		$\overline{CE}$ = V_{IL}	Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA		2.4		V

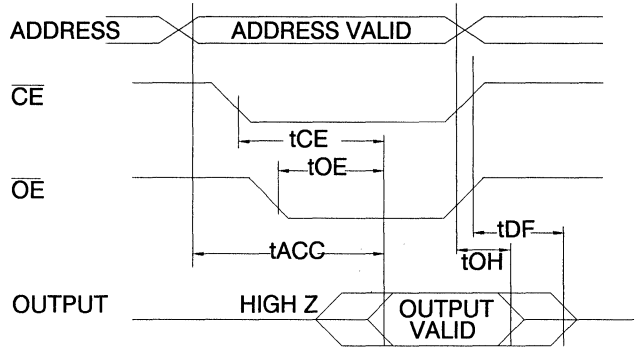
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

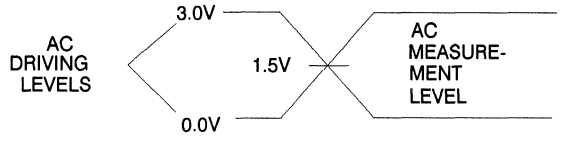
Symbol	Parameter	AT28C04-15 Min	AT28C04-15 Max	AT28C04-20 Min	AT28C04-20 Max	AT28C04-25 Min	AT28C04-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF}[3,4]	$\overline{OE}$ or $\overline{CE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



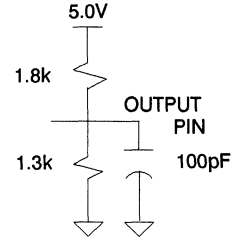
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20ns

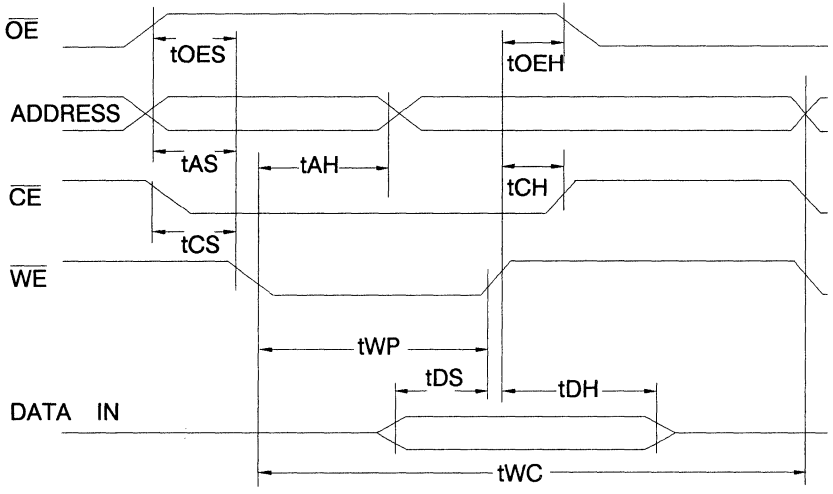
Output Test Load



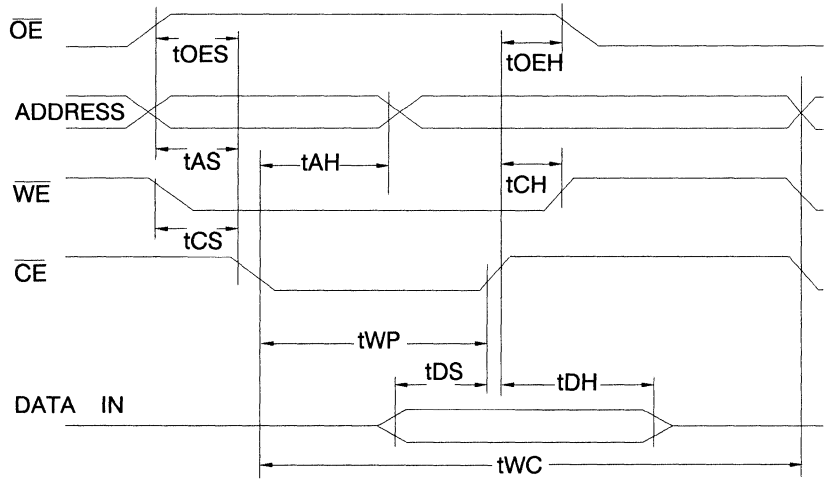
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	10			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10			ns
t_{WC}	Write Cycle Time 28C04		0.5	1.0	ms
	28C04E/F		100	200	µs

A.C. Write Waveforms - $\overline{WE}$ Controlled



A.C. Write Waveforms - $\overline{CE}$ Controlled

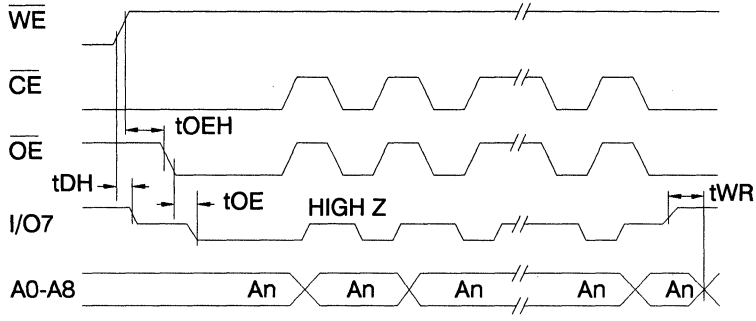


$\overline{\text{Data}}$ Polling Characteristics [1]

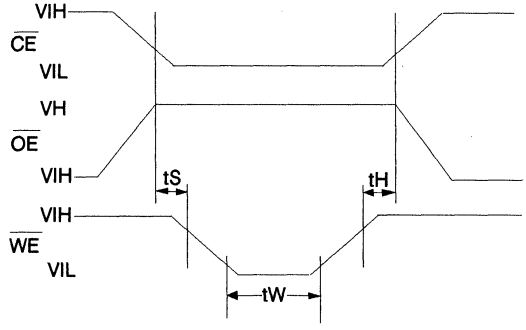
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms



Chip Erase Waveforms

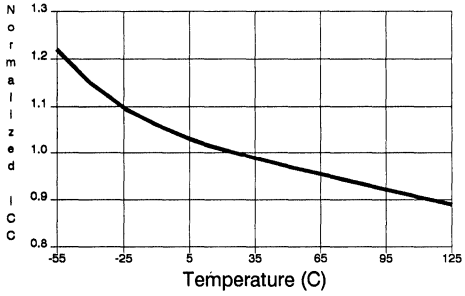


$t_S = t_H = 1\mu sec$ (min.)

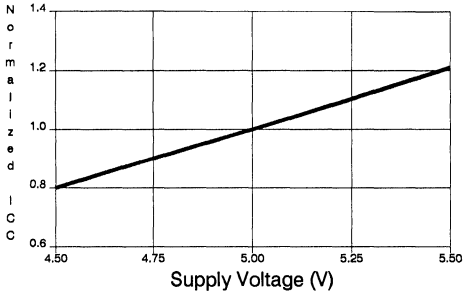
$t_W = 10msec$ (min.)

$V_H = 12 \pm 0.5V$

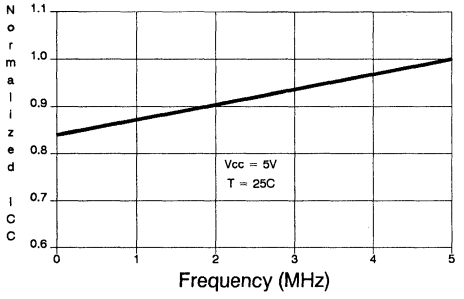
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



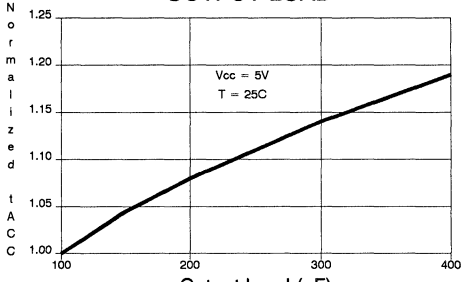
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



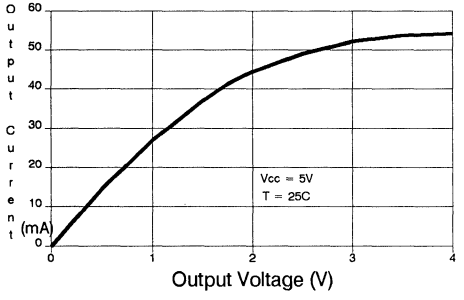
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



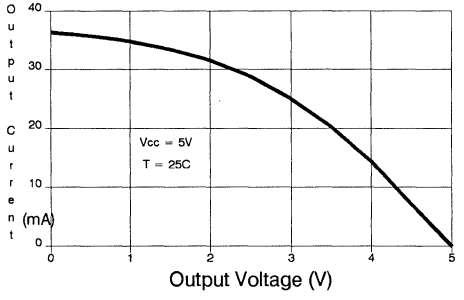
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C04(E,F)-15DC AT28C04(E,F)-15LC AT28C04(E,F)-15PC	24D6 32L 24P6	Commercial (0°C to 70°C)
150	45	0.1	AT28C04(E,F)-15DI AT28C04(E,F)-15LI AT28C04(E,F)-15PI	24D6 32L 24P6	Industrial (-40°C to 85°C)
			AT28C04(E,F)-15DM AT28C04(E,F)-15LM	24D6 32L	Military (-55°C to 125°C)
			AT28C04(E,F)-15DM/883 AT28C04(E,F)-15LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C04(E,F)-20DC AT28C04(E,F)-20LC AT28C04(E,F)-20PC AT28C04-20W	24D6 32L 24P6 DIE	Commercial (0°C to 70°C)
200	45	0.1	AT28C04(E,F)-20DI AT28C04(E,F)-20LI AT28C04(E,F)-20PI	24D6 32L 24P6	Industrial (-40°C to 85°C)
			AT28C04(E,F)-20DM AT28C04(E,F)-20LM	24D6 32L	Military (-55°C to 125°C)
			AT28C04(E,F)-20DM/883 AT28C04(E,F)-20LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C04(E,F)-25DC AT28C04(E,F)-25LC AT28C04(E,F)-25PC AT28C04-25W	24D6 32L 24P6 DIE	Commercial (0°C to 70°C)
250	45	0.1	AT28C04(E,F)-25DI AT28C04(E,F)-25LI AT28C04(E,F)-25PI	24D6 32L 24P6	Industrial (-40°C to 85°C)
			AT28C04(E,F)-25DM AT28C04(E,F)-25LM	24D6 32L	Military (-55°C to 125°C)
			AT28C04(E,F)-25DM/883 AT28C04(E,F)-25LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	AT28C04(E,F)-30DM/883 AT28C04(E,F)-30LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C04(E,F)-35DM/883 AT28C04(E,F)-35LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C04(E,F)-45DM/883 AT28C04(E,F)-45LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200μs
F	Fast Write Option: Write Time = 200μs

16K (2K x 8) CMOS E^2PROM

Features

- **Fast Read Access Time - 150ns**
- **Fast Byte Write - 200µs or 1 ms**
- **Self-Timed Byte Write Cycle**
  - **Internal Address and Data Latches**
  - **Internal Control Timer**
  - **Automatic Clear Before Write**
- **Direct Microprocessor Control**
  - **$\overline{\text{DATA}}$ POLLING**
- **Low Power**
  - **30mA Active Current**
  - **100µA CMOS Standby Current**
- **High Reliability**
  - **Endurance: 10^4 or 10^5 cycles**
  - **Data Retention: 10 years**
- **5V ± 10% Supply**
- **CMOS & TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

Description

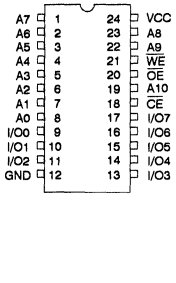
The AT28C16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C16 is a 16k memory organized as 2,048 words x 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

The AT28C16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by $\overline{\text{DATA}}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150ns at low power dissipation. When the chip is deselected the standby current is less than 100µA.

Atmel's 28C16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

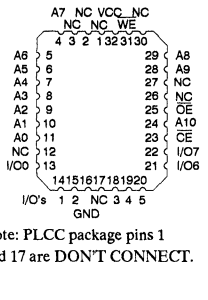
Pin Configurations



PIN NAMES

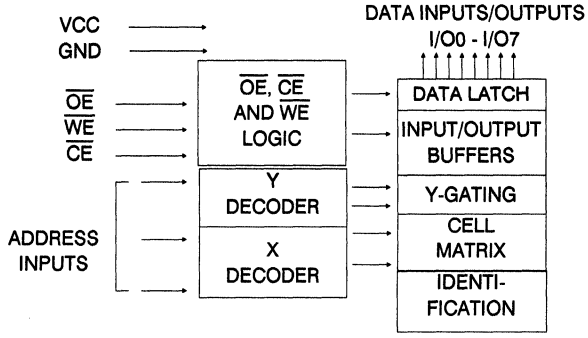
A0 - A10	Address
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

TOP VIEWS



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. $V_H = 12.0 \pm 0.5V$.

Device Operation

READ: The AT28C16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C16F offers a byte write time of 200µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

$\overline{DATA}$ POLLING: The AT28C16 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense– if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay– once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit– holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28C16-15	AT28C16-20	AT28C16-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ±10%	5V ± 10%	5V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1.0V	Com.		2	mA
			Ind., Mil.		3	mA
I_{CC}	V_{CC} Active Current A.C.	f = 5MHz; I_{out} = 0mA	Com.		30	mA
		$\overline{CE}$ = V_{IL}	Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA		2.4		V

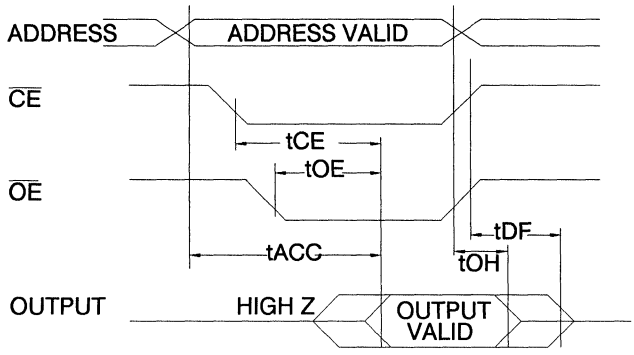
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

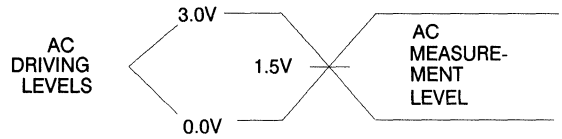
Symbol	Parameter	AT28C16-15 Min	AT28C16-15 Max	AT28C16-20 Min	AT28C16-20 Max	AT28C16-25 Min	AT28C16-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF}[3,4]	$\overline{OE}$ or $\overline{CE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



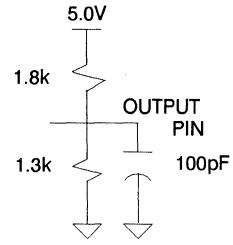
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20ns

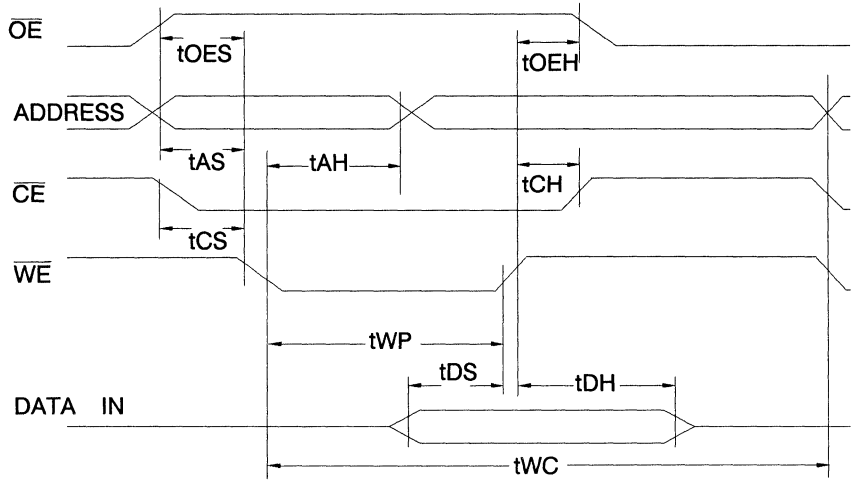
Output Test Load



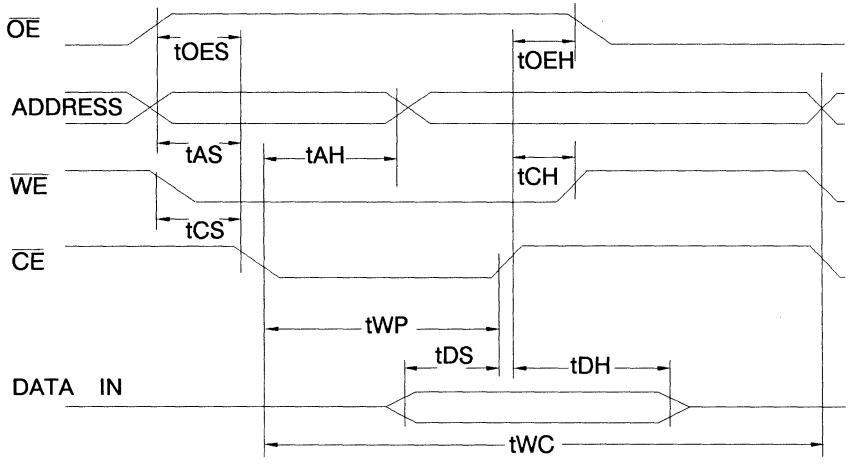
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	10			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10			ns
t_{WC}	Write Cycle Time 28C16		0.5	1.0	ms
	28C16E/F		100	200	µs

A.C. Write Waveforms - $\overline{WE}$ Controlled



A.C. Write Waveforms - $\overline{CE}$ Controlled

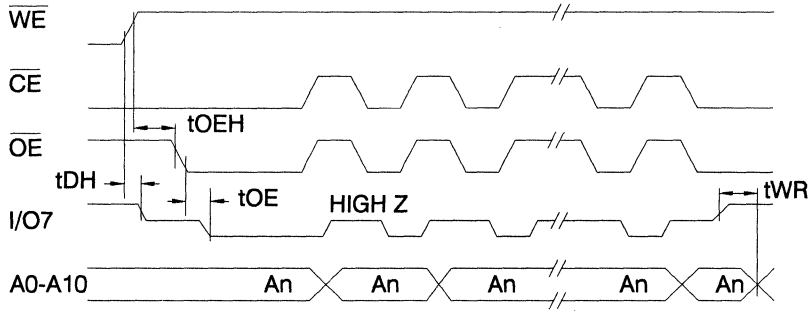


$\overline{\text{Data}}$ Polling Characteristics [1]

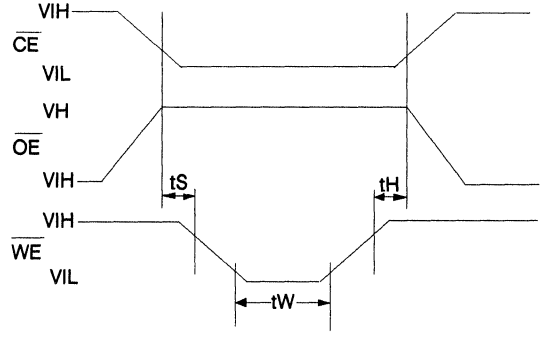
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms



Chip Erase Waveforms

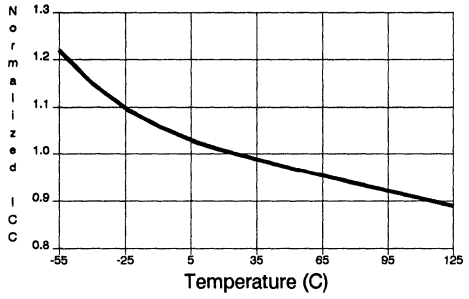


$t_S = t_H = 1\mu sec$ (min.)

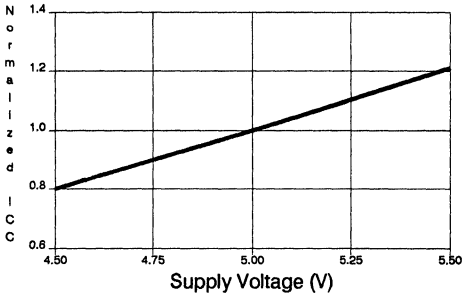
$t_W = 10msec$ (min.)

$V_H = 12 \pm 0.5V$

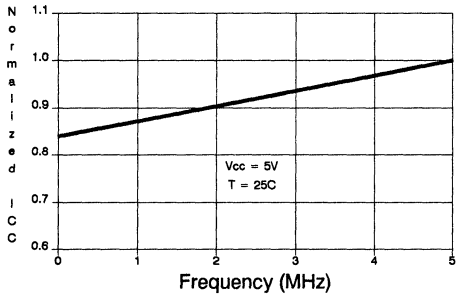
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



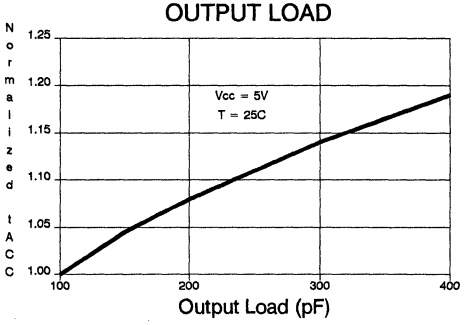
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



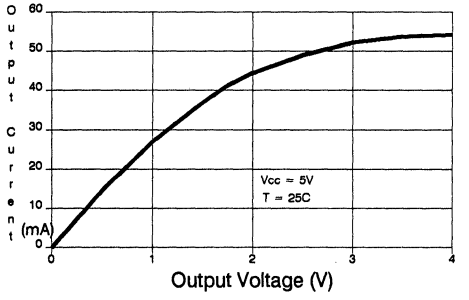
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



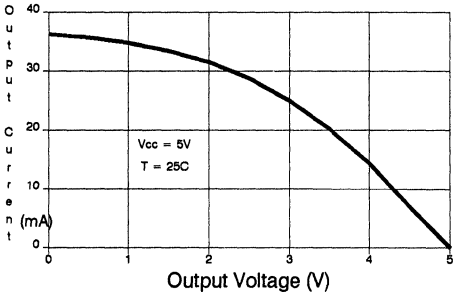
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16(E,F)-15DC AT28C16(E,F)-15JC AT28C16(E,F)-15LC AT28C16(E,F)-15PC AT28C16(E,F)-15SC	24D6 32J 32L 24P6 24S	Commercial (0°C to 70°C)
150	45	0.1	AT28C16(E,F)-15DI AT28C16(E,F)-15JI AT28C16(E,F)-15LI AT28C16(E,F)-15PI AT28C16(E,F)-15SI	24D6 32J 32L 24P6 24S	Industrial (-40°C to 85°C)
			AT28C16(E,F)-15DM AT28C16(E,F)-15LM	24D6 32L	Military (-55°C to 125°C)
			AT28C16(E,F)-15DM/883 AT28C16(E,F)-15LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C16(E,F)-20DC AT28C16(E,F)-20JC AT28C16(E,F)-20LC AT28C16(E,F)-20PC AT28C16(E,F)-20SC AT28C16-20W	24D6 32J 32L 24P6 24S DIE	Commercial (0°C to 70°C)
200	45	0.1	AT28C16(E,F)-20DI AT28C16(E,F)-20JI AT28C16(E,F)-20LI AT28C16(E,F)-20PI AT28C16(E,F)-20SI	24D6 32J 32L 24P6 24S	Industrial (-40°C to 85°C)
			AT28C16(E,F)-20DM AT28C16(E,F)-20LM	24D6 32L	Military (-55°C to 125°C)
			AT28C16(E,F)-20DM/883 AT28C16(E,F)-20LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C16(E,F)-25DC AT28C16(E,F)-25JC AT28C16(E,F)-25LC AT28C16(E,F)-25PC AT28C16(E,F)-25SC AT28C16-25W	24D6 32J 32L 24P6 24S DIE	Commercial (0°C to 70°C)
250	45	0.1	AT28C16(E,F)-25DI AT28C16(E,F)-25JI AT28C16(E,F)-25LI AT28C16(E,F)-25PI AT28C16(E,F)-25SI	24D6 32J 32L 24P6 24S	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	45	0.1	AT28C16(E,F)-25DM AT28C16(E,F)-25LM	24D6 32L	Military (-55°C to 125°C)
			AT28C16(E,F)-25DM/883 AT28C16(E,F)-25LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	AT28C16(E,F)-30DM/883 AT28C16(E,F)-30LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C16(E,F)-35DM/883 AT28C16(E,F)-35LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C16(E,F)-45DM/883 AT28C16(E,F)-45LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200µs
F	Fast Write Option: Write Time = 200µs

16K (2K x 8) CMOS E^2PROM

Features

- **Fast Read Access Time - 150ns**
- **Fast Byte Write - 200μs or 1 ms**
- **Self-Timed Byte Write Cycle**
  - **Internal Address and Data Latches**
  - **Internal Control Timer**
  - **Automatic Clear Before Write**
- **Direct Microprocessor Control**
  - **$\overline{\text{DATA}}$ POLLING**
  - **READY/$\overline{\text{BUSY}}$ Open Drain Output**
- **Low Power**
  - **30mA Active Current**
  - **100μa CMOS Standby Current**
- **High Reliability**
  - **Endurance: 10^4 or 10^5 cycles**
  - **Data Retention: 10 years**
- **5 V ± 10% Supply**
- **CMOS & TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

Description

The AT28C17 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C17 is a 16k memory organized as 2,048 words x 8 bits. The device is manufactured with Atmel's reliable non-volatile CMOS technology.

The AT28C17 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{\text{BUSY}}$ and $\overline{\text{DATA}}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150ns at low power dissipation. When the chip is deselected the standby current is less than 100μA.

Atmel's 28C17 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

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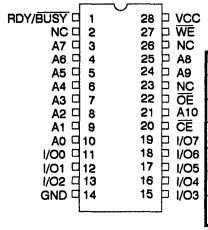
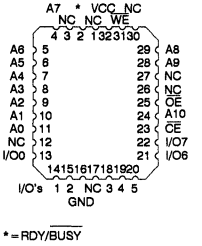


PIN NAMES

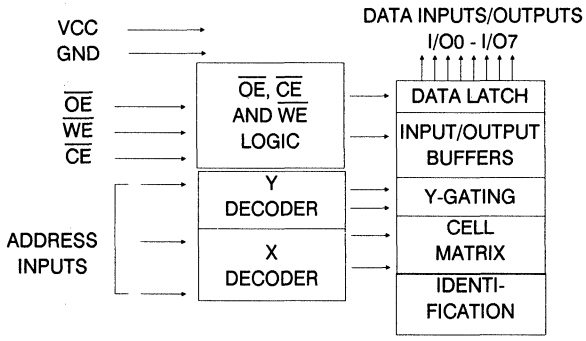
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{Busy}}$ Output
NC	No Connect



* = RDY/$\overline{\text{BUSY}}$

Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. $V_H = 12.0 \pm 0.5V$.

Device Operation

READ: The AT28C17 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C17 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C17F offers a byte write time of 200µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line.

$\overline{DATA}$ POLLING: The AT28C17 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense – if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay – once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C17 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28C17-15	AT28C17-20	AT28C17-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ±10%	5V ± 10%	5V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V	Com.		2	mA
		to V_{CC} + 1.0V	Ind., Mil.		3	mA
I_{CC}	V_{CC} Active Current A.C.	f = 5MHz; I_{out} = 0mA	Com.		30	mA
		$\overline{CE}$ = V_{IL}	Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA = 4.0mA for RDY/$\overline{BUSY}$			.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA		2.4		V

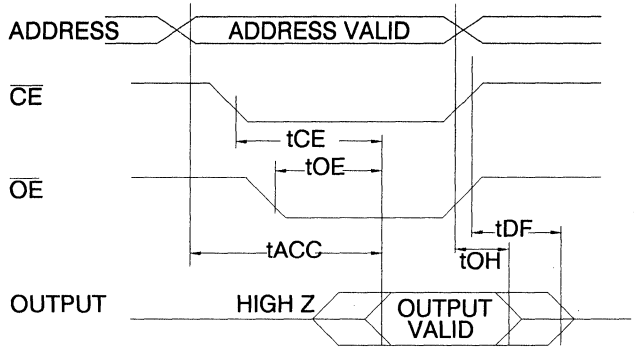
Pin Capacitance (f = 1MHz T = 25°C)[4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

Symbol	Parameter	AT28C17-15 Min	AT28C17-15 Max	AT28C17-20 Min	AT28C17-20 Max	AT28C17-25 Min	AT28C17-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF}[3,4]	$\overline{OE}$ or $\overline{CE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

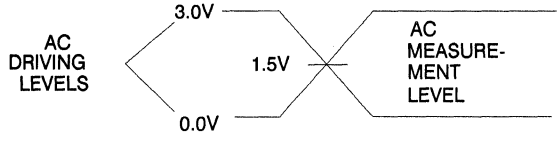
A.C. Read Waveforms



Notes:

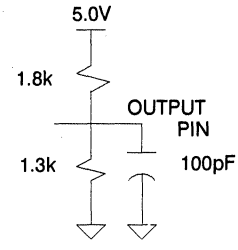
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20ns

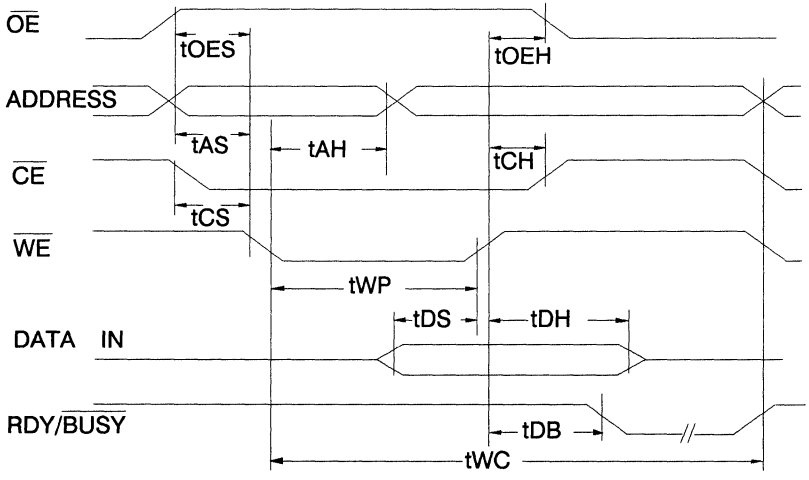
Output Test Load



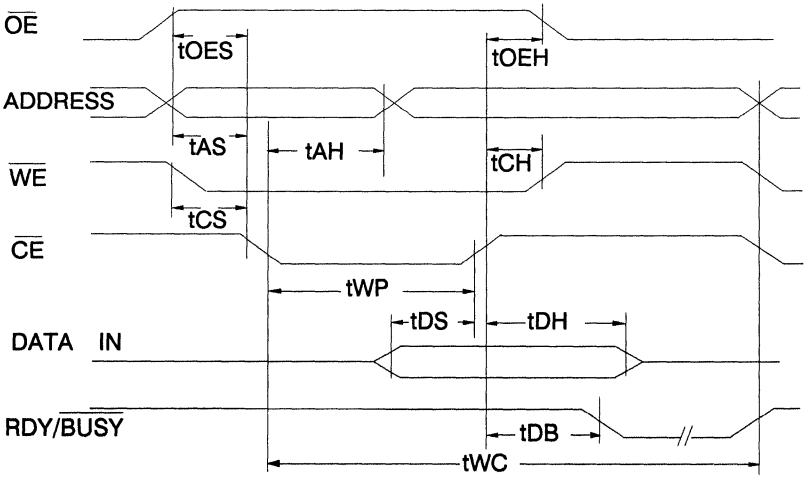
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	10			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10			ns
t_{DB}	Time to Device Busy			50	ns
t_{WC}	Write Cycle Time 28C17		0.5	1.0	ms
	28C17E/F		100	200	µs

A.C. Write Waveforms - $\overline{WE}$ Controlled



A.C. Waveforms - $\overline{CE}$ Controlled

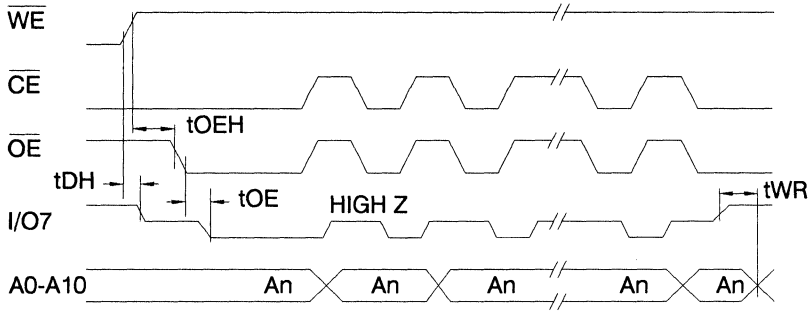


Data Polling Characteristics [1]

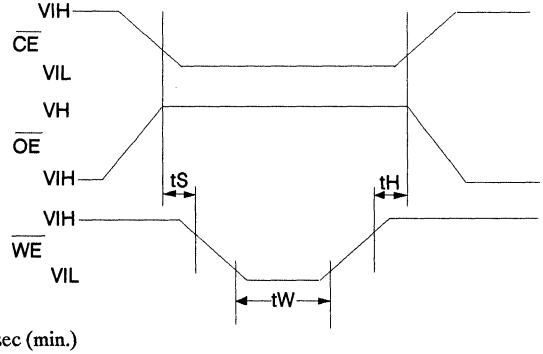
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Data Polling Waveforms



Chip Erase Waveforms

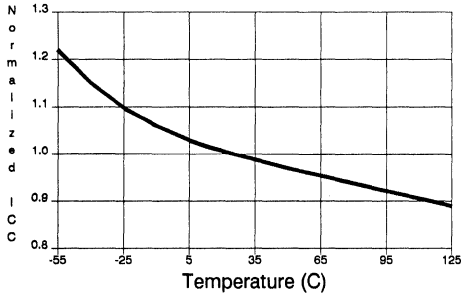


$t_S = t_H = 1\mu sec$ (min.)

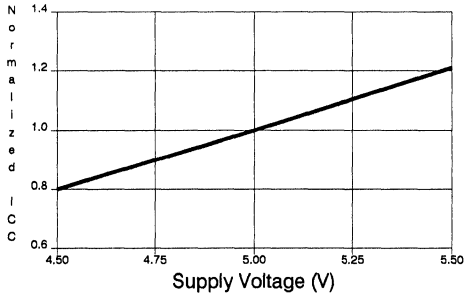
$t_W = 10msec$ (min.)

$V_H = 12 \pm 0.5V$

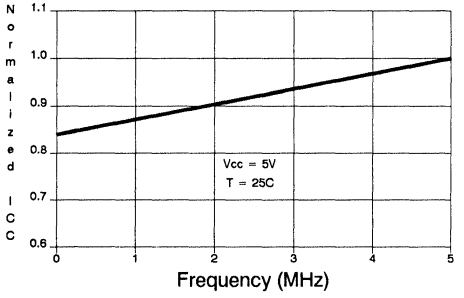
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



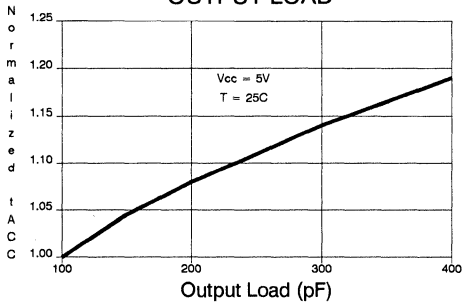
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



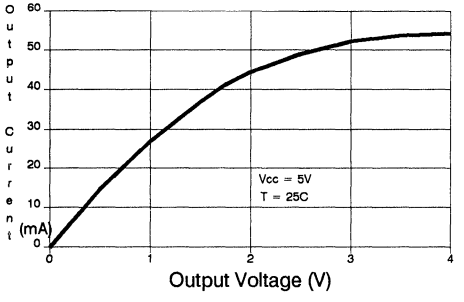
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



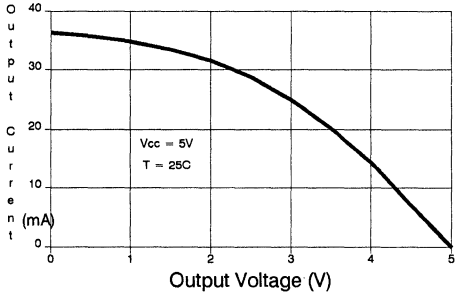
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C17(E,F)-15DC AT28C17(E,F)-15JC AT28C17(E,F)-15LC AT28C17(E,F)-15PC AT28C17(E,F)-15SC	28D6 32J 32L 28P6 28S	Commercial (0°C to 70°C)
150	45	0.1	AT28C17(E,F)-15DI AT28C17(E,F)-15JI AT28C17(E,F)-15LI AT28C17(E,F)-15PI AT28C17(E,F)-15SI	28D6 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C17(E,F)-15DM AT28C17(E,F)-15LM	28D6 32L	Military (-55°C to 125°C)
			AT28C17(E,F)-15DM/883 AT28C17(E,F)-15LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C17(E,F)-20DC AT28C17(E,F)-20JC AT28C17(E,F)-20LC AT28C17(E,F)-20PC AT28C17(E,F)-20SC AT28C17-20W	28D6 32J 32L 28P6 28S DIE	Commercial (0°C to 70°C)
200	45	0.1	AT28C17(E,F)-20DI AT28C17(E,F)-20JI AT28C17(E,F)-20LI AT28C17(E,F)-20PI AT28C17(E,F)-20SI	28D6 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C17(E,F)-20DM AT28C17(E,F)-20LM	28D6 32L	Military (-55°C to 125°C)
			AT28C17(E,F)-20DM/883 AT28C17(E,F)-20LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C17(E,F)-25DC AT28C17(E,F)-25JC AT28C17(E,F)-25LC AT28C17(E,F)-25PC AT28C17(E,F)-25SC AT28C17-25W	28D6 32J 32L 28P6 28S DIE	Commercial (0°C to 70°C)
250	45	0.1	AT28C17(E,F)-25DI AT28C17(E,F)-25JI AT28C17(E,F)-25LI AT28C17(E,F)-25PI AT28C17(E,F)-25SI	28D6 32J 32L 28P6 28S	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	45	0.1	AT28C17(E,F)-25DM AT28C17(E,F)-25LM	28D6 32L	Military (-55°C to 125°C)
			AT28C17(E,F)-25DM/883 AT28C17(E,F)-25LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	AT28C17(E,F)-30DM/883 AT28C17(E,F)-30LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C17(E,F)-35DM/883 AT28C17(E,F)-35LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C17(E,F)-45DM/883 AT28C17(E,F)-45LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200µs
F	Fast Write Option: Write Time = 200µs

64K (8K x 8) CMOS E^2PROM

Features

- Fast Read Access Time - 150ns
- Fast Byte Write - 200μs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - READY/$\overline{\text{BUSY}}$ Open Drain Output
  - $\overline{\text{DATA}}$ Polling
- Low Power
  - 30mA Active Current
  - 100μA CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

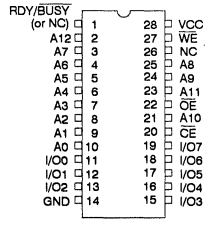
The AT28C64 is a low-power, high-performance 8,192 words x 8 bit non-volatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features. The device is manufactured with Atmel's reliable non-volatile technology.

The AT28C64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{\text{BUSY}}$ (unless pin 1 is N.C.) and $\overline{\text{DATA}}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The CMOS technology offers fast access times of 150ns at low power dissipation. When the chip is deselected the standby current is less than 100μA.

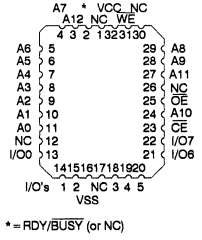
Atmel's 28C64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

Pin Configurations



PIN NAMES

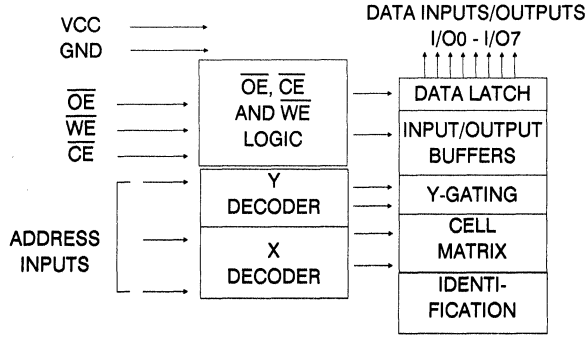
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/Busy Output
NC	No Connect



* = RDY/$\overline{\text{BUSY}}$ (or NC)

Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. $V_H = 12.0 \pm 0.5V$.

Device Operation

READ: The AT28C64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C64 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C64F offers a byte write time of 200µs maximum. This feature allows the entire device to be rewritten in 1.6 seconds.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line. Pin 1 is not connected for the AT28C64X.

$\overline{DATA}$ POLLING: The AT28C64 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense – if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay – once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C64 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to $12 \pm 0.5V$ and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28C64-15	AT28C64-20	AT28C64-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V +/-10%	5V +/-10%	5V +/-10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V	Com..		2	mA
		to V_{CC} + 1.0V	Ind., Mil.		3	mA
I_{CC}	V_{CC} Active Current A.C	f = 5MHz; I_{out} = 0mA	Com.		30	mA
		$\overline{CE}$ = V_{IL}	Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA = 4.0mA for RDY/$\overline{BUSY}$			.45	V
V_{OH}	Output High Voltage	I_{OH} = -400µA		2.4		V

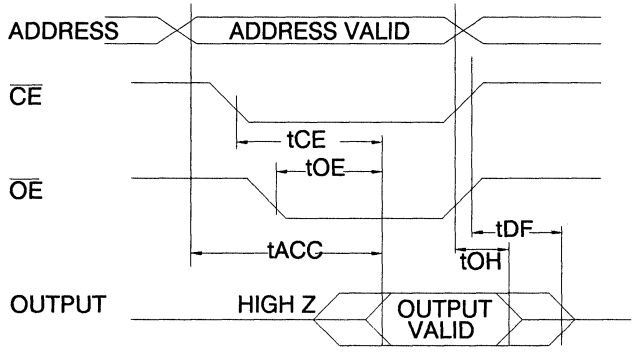
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

Symbol	Parameter	AT28C64-15 Min	AT28C64-15 Max	AT28C64-20 Min	AT28C64-20 Max	AT28C64-25 Min	AT28C64-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF}[3,4]	$\overline{OE}$ or $\overline{CE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

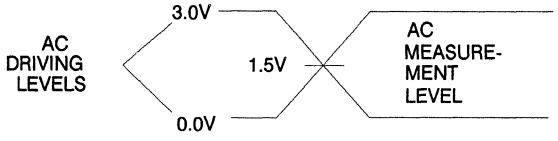
A.C. Read Waveforms



Notes:

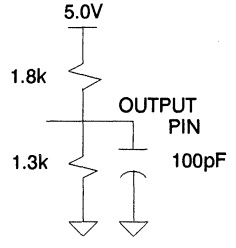
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20ns

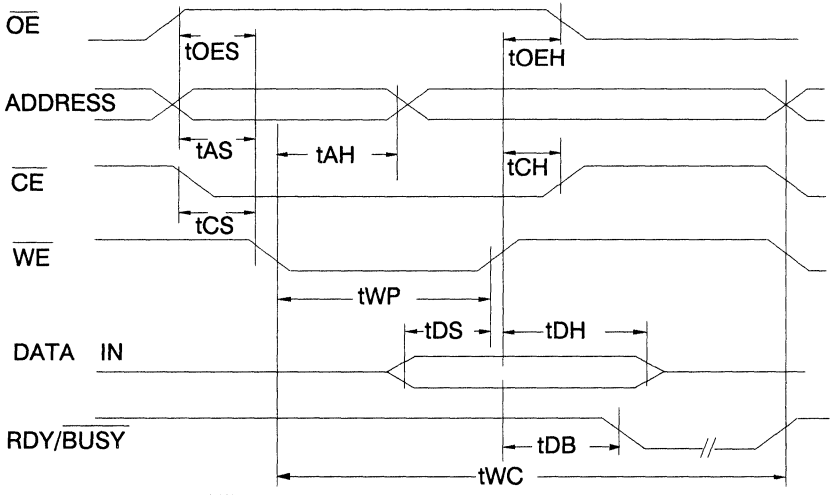
Output Test Load



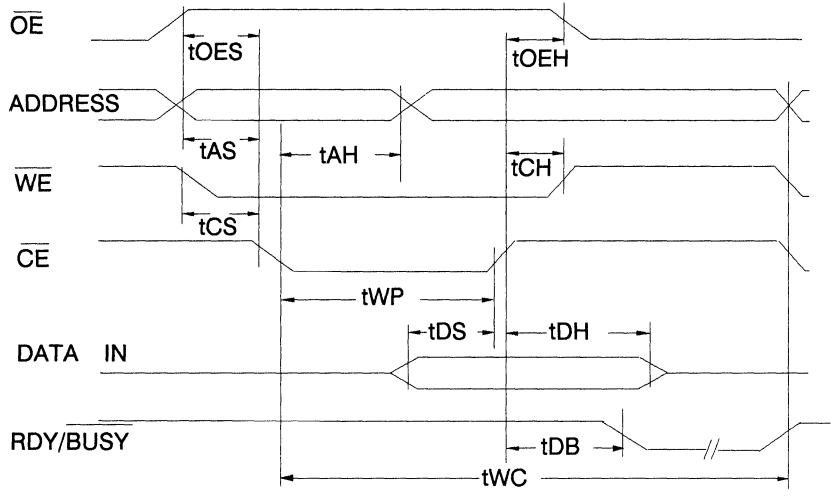
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	10			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10			ns
t_{DB}	Time to Device Busy			50	ns
t_{WC}	Write Cycle Time AT28C64		0.5	1.0	ms
	AT28C64E/F		100	200	µs

A.C. Write Waveforms - $\overline{WE}$ Controlled



A.C. Write Waveforms - $\overline{CE}$ Controlled

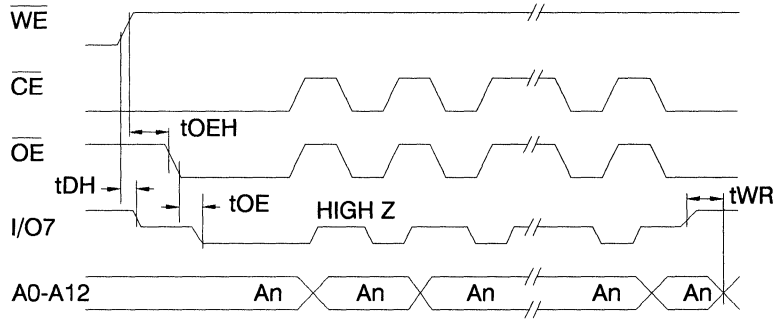


$\overline{\text{Data}}$ Polling Characteristics [1]

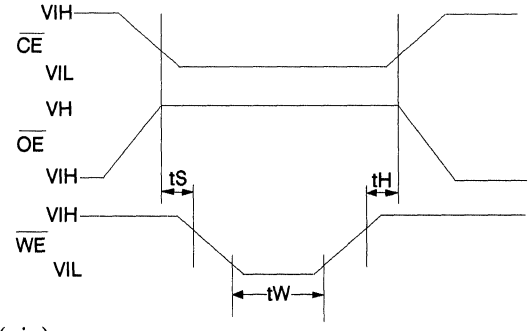
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms



Chip Erase Waveforms

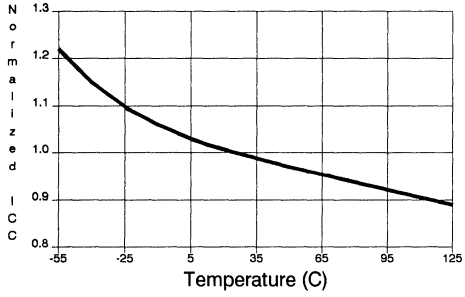


$t_S = t_H = 1\mu sec$ (min.)

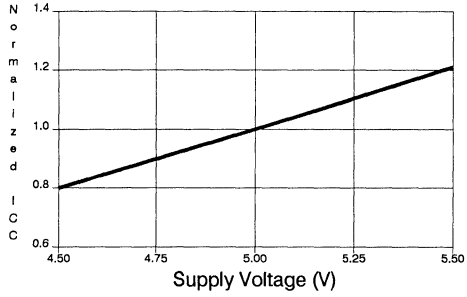
$t_W = 10msec$ (min.)

$V_H = 12 \pm 0.5V$

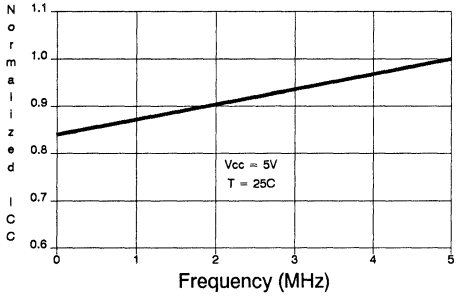
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



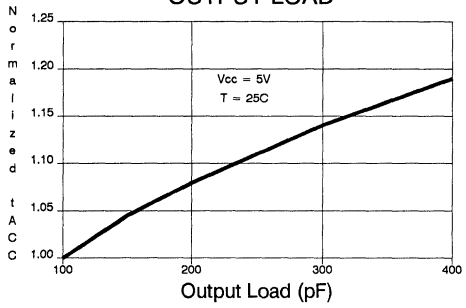
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



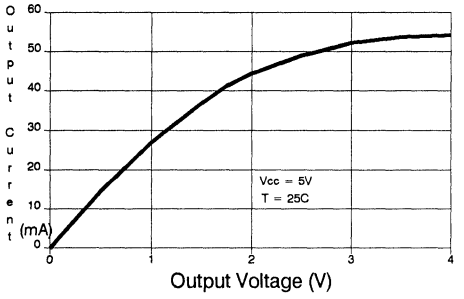
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



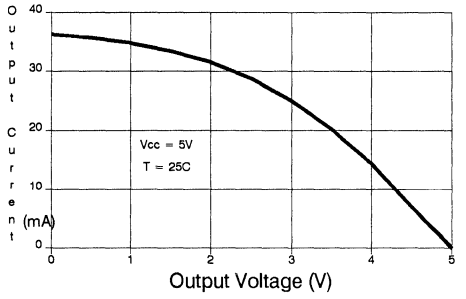
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C64(E,F)-15DC AT28C64(E,F)-15FC AT28C64(E,F)-15JC AT28C64(E,F)-15LC AT28C64(E,F)-15PC AT28C64(E,F)-15SC	28D6 28F 32J 32L 28P6 28S	Commercial (0°C to 70°C)
150	45	0.1	AT28C64(E,F)-15DI AT28C64(E,F)-15FI AT28C64(E,F)-15JI AT28C64(E,F)-15LI AT28C64(E,F)-15PI AT28C64(E,F)-15SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64(E,F)-15DM AT28C64(E,F)-15FM AT28C64(E,F)-15LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64(E,F)-15DM/883 AT28C64(E,F)-15FM/883 AT28C64(E,F)-15LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C64(E,F)-20DC AT28C64(E,F)-20FC AT28C64(E,F)-20JC AT28C64(E,F)-20LC AT28C64(E,F)-20PC AT28C64(E,F)-20SC AT28C64-20W	28D6 28F 32J 32L 28P6 28S DIE	Commercial (0°C to 70°C)
200	45	0.1	AT28C64(E,F)-20DI AT28C64(E,F)-20FI AT28C64(E,F)-20JI AT28C64(E,F)-20LI AT28C64(E,F)-20PI AT28C64(E,F)-20SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64(E,F)-20DM AT28C64(E,F)-20FM AT28C64(E,F)-20LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64(E,F)-20DM/883 AT28C64(E,F)-20FM/883 AT28C64(E,F)-20LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C64(E,F)-25DC AT28C64(E,F)-25FC AT28C64(E,F)-25JC AT28C64(E,F)-25LC AT28C64(E,F)-25PC AT28C64(E,F)-25SC AT28C64-25W	28D6 28F 32J 32L 28P6 28S DIE	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
250	45	0.1	AT28C64(E,F)-25DI AT28C64(E,F)-25FI AT28C64(E,F)-25JI AT28C64(E,F)-25LI AT28C64(E,F)-25PI AT28C64(E,F)-25SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64(E,F)-25DM AT28C64(E,F)-25FM AT28C64(E,F)-25LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64(E,F)-25DM/883 AT28C64(E,F)-25FM/883 AT28C64(E,F)-25LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	AT28C64(E,F)-30DM/883 AT28C64(E,F)-30FM/883 AT28C64(E,F)-30LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C64(E,F)-35DM/883 AT28C64(E,F)-35FM/883 AT28C64(E,F)-35LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C64(E,F)-45DM/883 AT28C64(E,F)-45FM/883 AT28C64(E,F)-45LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	45	0.1	5962-87514 17 UX 5962-87514 17 XX 5962-87514 17 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	45	0.1	5962-87514 16 UX 5962-87514 16 XX 5962-87514 16 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	45	0.1	5962-87514 15 UX 5962-87514 15 XX 5962-87514 15 YX 5962-87514 15 ZX	32K 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	5962-87514 14 UX 5962-87514 14 XX 5962-87514 14 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	5962-87514 13 UX 5962-87514 13 XX 5962-87514 13 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32K	32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200μs
F	Fast Write Option: Write Time = 200μs

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C64X-15DC AT28C64X-15FC AT28C64X-15JC AT28C64X-15LC AT28C64X-15PC AT28C64X-15SC	28D6 28F 32J 32L 28P6 28S	Commercial (0°C to 70°C)
150	45	0.1	AT28C64X-15DI AT28C64X-15FI AT28C64X-15JI AT28C64X-15LI AT28C64X-15PI AT28C64X-15SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64X-15DM AT28C64X-15FM AT28C64X-15LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64X-15DM/883 AT28C64X-15FM/883 AT28C64X-15LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C64X-20DC AT28C64X-20FC AT28C64X-20JC AT28C64X-20LC AT28C64X-20PC AT28C64X-20SC	28D6 28F 32J 32L 28P6 28S	Commercial (0°C to 70°C)
200	45	0.1	AT28C64X-20DI AT28C64X-20FI AT28C64X-20JI AT28C64X-20LI AT28C64X-20PI AT28C64X-20SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64X-20DM AT28C64X-20FM AT28C64X-20LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64X-20DM/883 AT28C64X-20FM/883 AT28C64X-20LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C64X-25DC AT28C64X-25FC AT28C64X-25JC AT28C64X-25LC AT28C64X-25PC AT28C64X-25SC	28D6 28F 32J 32L 28P6 28S	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	45	0.1	AT28C64X-25DI AT28C64X-25FI AT28C64X-25JI AT28C64X-25LI AT28C64X-25PI AT28C64X-25SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64X-25DM AT28C64X-25FM AT28C64X-25LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64X-25DM/883 AT28C64X-25FM/883 AT28C64X-25LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	AT28C64X-30DM/883 AT28C64X-30FM/883 AT28C64X-30LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C64X-35DM/883 AT28C64X-35FM/883 AT28C64X-35LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C64X-45DM/883 AT28C64X-45FM/883 AT28C64X-45LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	45	0.1	5962-87514 22 UX 5962-87514 22 XX 5962-87514 22 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	45	0.1	5962-87514 21 UX 5962-87514 21 XX 5962-87514 21 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	45	0.1	5962-87514 20 UX 5962-87514 20 XX 5962-87514 20 YX 5962-87514 20 ZX	32K 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	5962-87514 19 UX 5962-87514 19 XX 5962-87514 19 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	5962-87514 18 UX 5962-87514 18 XX 5962-87514 18 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32K	32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

64K (8K x 8) Paged CMOS E^2PROM

Features

- **Fast Read Access Time - 150ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 32 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Maximum Page Write Cycle Time: 2ms**
  - **1 to 32 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80mA Active Current**
  - **100μA CMOS Standby Current**
- **Direct Microprocessor Control**
  - **$\overline{\text{DATA}}$ Polling**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

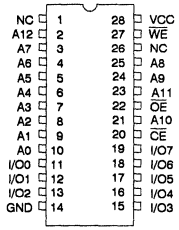
Description

The AT28PC64 is a high-speed, low-power Electrically Erasable and Programmable Read Only Memory. Its 64k of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150ns with power dissipation of just 440mW. When the device is deselected the standby current is less than 100μA.

The AT28PC64 is accessed like a Static RAM for the read or write cycles without the need for external components. The device contains a 32-byte page register to allow writing of up to 32 bytes simultaneously. During a write cycle, the addresses and 1 to 32 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

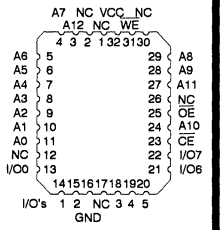
Atmel's 28PC64 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. The AT28PC64 also includes an extra 32 bytes of E^2PROM for device identification or tracking.

Pin Configurations



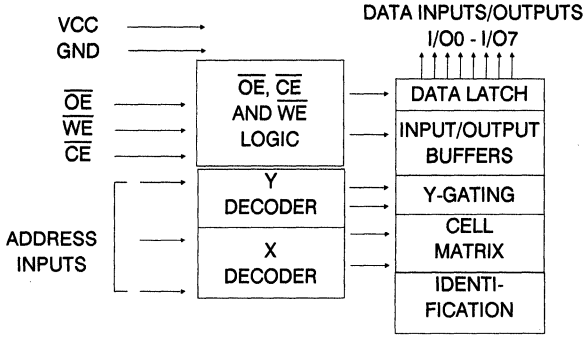
PIN NAMES

A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. V_H = 12.0 ± 0.5V.

Device Operation

READ: The AT28PC64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28PC64 allows one to 32 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded, successive bytes may be loaded in the same manner. Each byte to be written must be loaded into the AT28PC64 within 150μs of the first byte. A5 to A12 determine the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A4 are used to specify which bytes within the page are to be written. All bytes to be written must share the same page address. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28PC64 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28PC64 in the following ways: (a) Vcc sense – if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay – once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter – pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

CHIP CLEAR: The contents of the entire memory of the AT28PC64 may be set to the high state by the use of the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10ms low pulse is applied to the $\overline{WE}$ pin.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

D.C. and A.C. Operating Range

		AT28PC64-15	AT28PC64-20	AT28PC64-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-.3V	Com., Ind.		100	µA
		to V_{CC} + 1V	Mil.		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V			3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz; I_{OUT} = 0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA		2.4		V

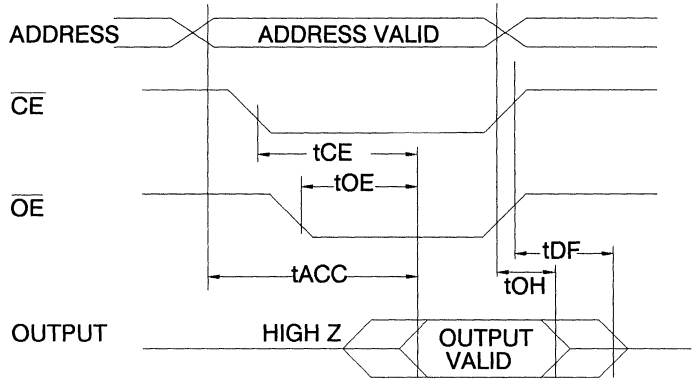
Pin Capacitance (f = 1MHz T = 25°C) [5]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Characteristics [1]

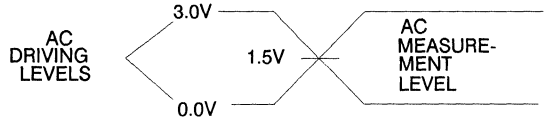
Symbol	Parameter	AT28PC64-15 Min	AT28PC64-15 Max	AT28PC64-20 Min	AT28PC64-20 Max	AT28PC64-25 Min	AT28PC64-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}[2]	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE}[3]	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF}[4,5]	$\overline{OE}$ or $\overline{CE}$ to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



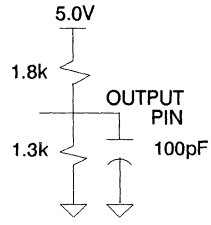
Notes:
1. C_L = 100pF.
2. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
5. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

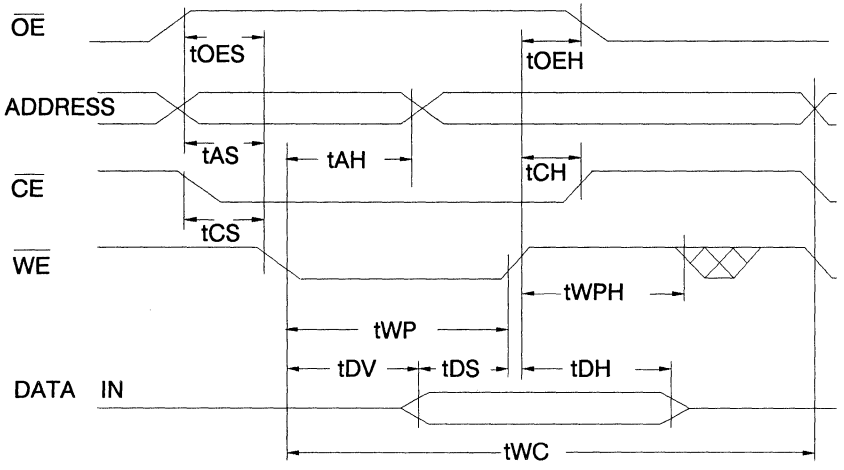
Output Test Load



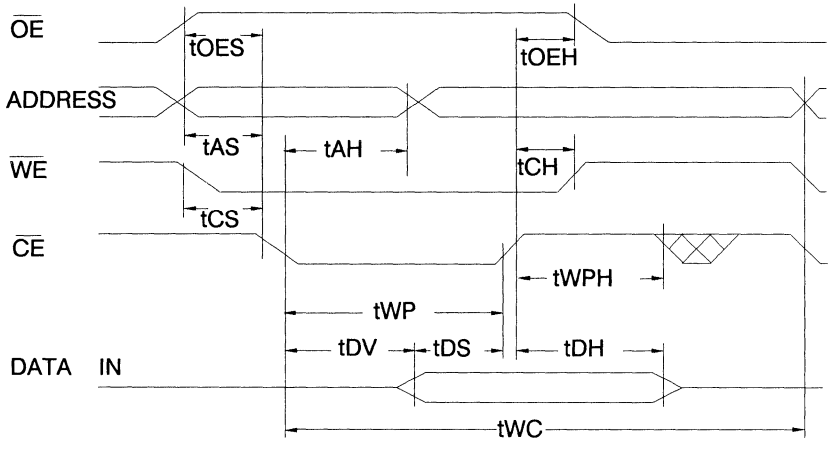
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{DV}	Time to Data Valid			1	µs
t_{WC}	Write Cycle Time		1.0	2.0	ms

A.C. Write Waveforms - $\overline{WE}$ Controlled



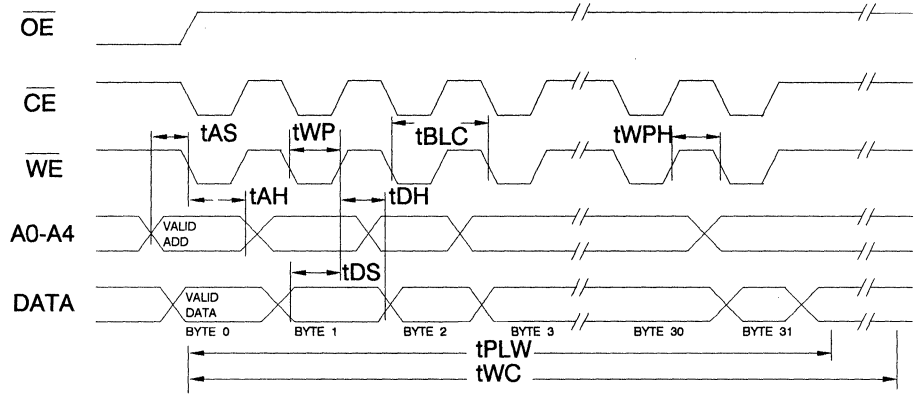
A.C. Write Waveforms - $\overline{CE}$ Controlled



Page Mode Write Characteristics

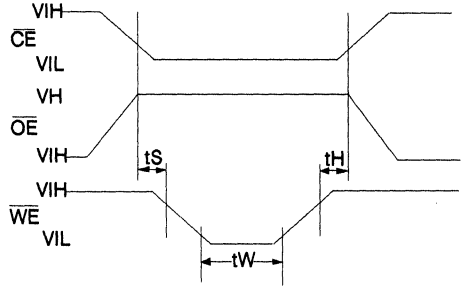
Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		1	2.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100		1000	ns
t_{BLC}	Byte Load Cycle Time	150			ns
t_{PLW}	Page Load Width			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms



Note: A5 through A12 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms



$t_S = t_H = 1\mu sec$ (min.)

$t_W = 10msec$ (min.)

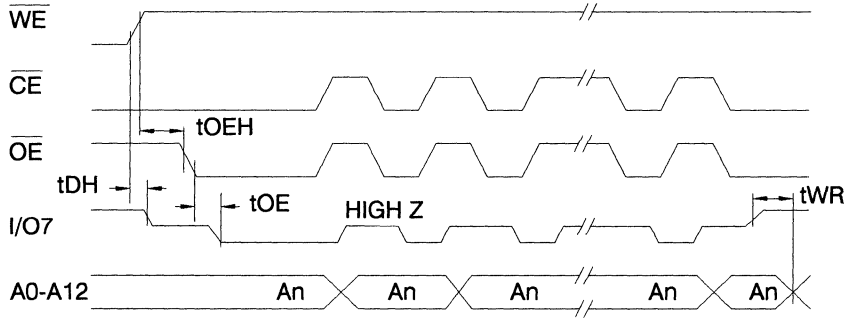
$V_H = 12 \pm 0.5V$

Data Polling Characteristics [1]

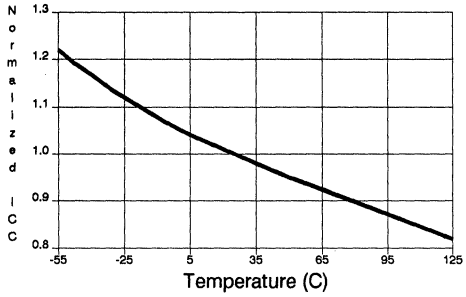
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			50	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

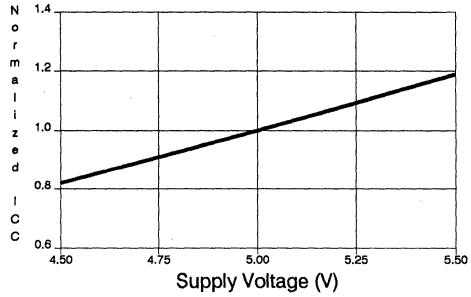
DATA Polling Waveforms



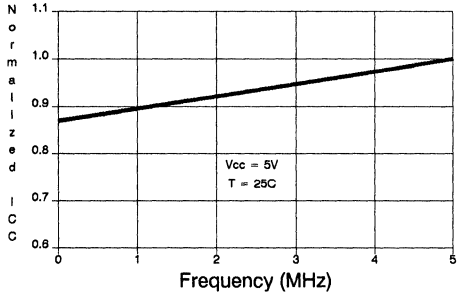
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.1	AT28PC64(E)-15DC AT28PC64(E)-15JC AT28PC64(E)-15LC AT28PC64(E)-15PC AT28PC64-15W	28D6 32J 32L 28P6 DIE	Commercial (0°C to 70°C)
			AT28PC64(E)-15DI AT28PC64(E)-15JI AT28PC64(E)-15LI AT28PC64(E)-15PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
150	80	0.2	AT28PC64(E)-15DM AT28PC64(E)-15LM	28D6 32L	Military (-55°C to 125°C)
			AT28PC64(E)-15DM/883 AT28PC64(E)-15LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.1	AT28PC64(E)-20DC AT28PC64(E)-20JC AT28PC64(E)-20LC AT28PC64(E)-20PC AT28PC64-20W	28D6 32J 32L 28P6 DIE	Commercial (0°C to 70°C)
			AT28PC64(E)-20DI AT28PC64(E)-20JI AT28PC64(E)-20LI AT28PC64(E)-20PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
200	80	0.2	AT28PC64(E)-20DM AT28PC64(E)-20LM	28D6 32L	Military (-55°C to 125°C)
			AT28PC64(E)-20DM/883 AT28PC64(E)-20LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.1	AT28PC64(E)-25DC AT28PC64(E)-25JC AT28PC64(E)-25LC AT28PC64(E)-25PC AT28PC64-25W	28D6 32J 32L 28P6 DIE	Commercial (0°C to 70°C)
			AT28PC64(E)-25DI AT28PC64(E)-25JI AT28PC64(E)-25LI AT28PC64(E)-25PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
250	80	0.2	AT28PC64(E)-25DM AT28PC64(E)-25LM	28D6 32L	Military (-55°C to 125°C)
			AT28PC64(E)-25DM/883 AT28PC64(E)-25LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
300	80	0.2	AT28PC64(E)-30DM/883 AT28PC64(E)-30LM/883	28D6 32L	Military/883 Class B, Fully Compliant (-55°C to 125°C)
350	80	0.2	AT28PC64(E)-35DM/883 AT28PC64(E)-35LM/883	28D6 32L	Military/883 Class B, Fully Compliant (-55°C to 125°C)
200	80	0.2	5962-87514 09 UX 5962-87514 09 XX 5962-87514 09 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.2	5962-87514 08 UX 5962-87514 08 XX 5962-87514 08 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	80	0.2	5962-87514 07 UX 5962-87514 07 XX 5962-87514 07 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	80	0.2	5962-87514 06 UX 5962-87514 06 XX 5962-87514 06 YX	32K 28D6 32L	Military/883 Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32K	32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2ms
E	High Endurance Option: Endurance = 100K Write Cycles

256K (32K x 8) Paged CMOS E^2PROM

Features

- **Fast Read Access Time - 150ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 64 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Page Write Cycle Time: 3.0ms or 10ms maximum**
  - **1 to 64 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80mA Active Current**
  - **200µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

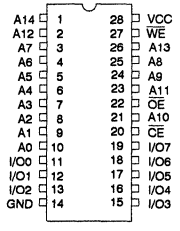
Description

The AT28C256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256k of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 200µA.

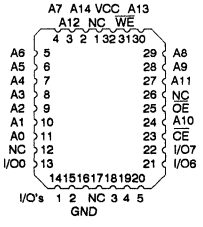
The AT28C256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of E^2PROM for device identification or tracking.

Pin Configurations

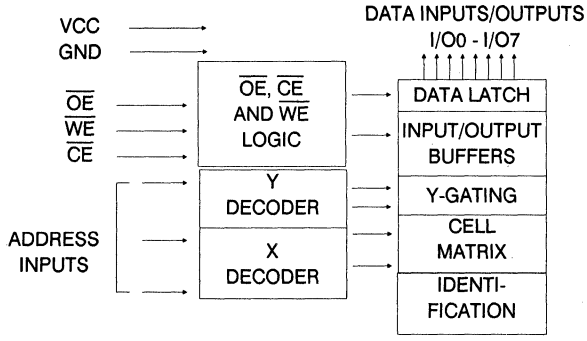


PIN NAMES	
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Device Operation

READ: The AT28C256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28C256 allows one to 64 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C256 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28C256 in the following ways: (a) Vcc sense – if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay – once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter – pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28C256. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

DEVICE IDENTIFICATION: An extra 64 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ..... -0.6V to +13.5V

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28C256-15	AT28C256-20	AT28C256-25	AT28C256-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. V_H = 12.0 ± 0.5V.

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-.3V to V_{CC} + 1V	Com.,Ind.		200	µA
			Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V			3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz; I_{OUT} = 0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -400µA		2.4		V

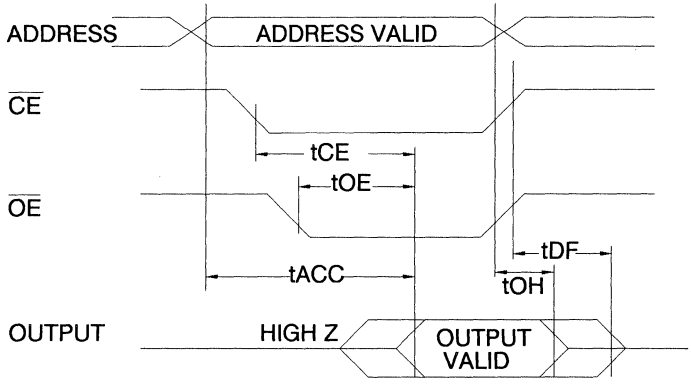
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

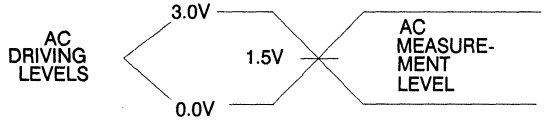
Symbol	Parameter	AT28C256-15 Min	AT28C256-15 Max	AT28C256-20 Min	AT28C256-20 Max	AT28C256-25 Min	AT28C256-25 Max	AT28C256-35 Min	AT28C256-35 Max	Units
t_{ACC}	Address to Output Delay		150		200		250		350	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150		200		250		350	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	0	100	ns
t_{DF}[3,4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



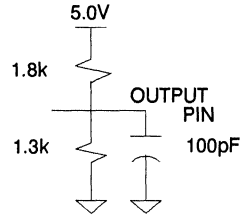
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load

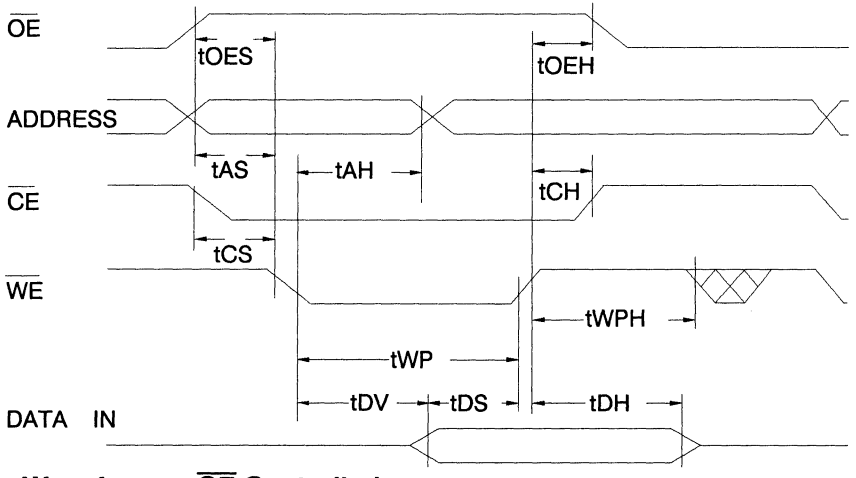


A.C. Write Characteristics

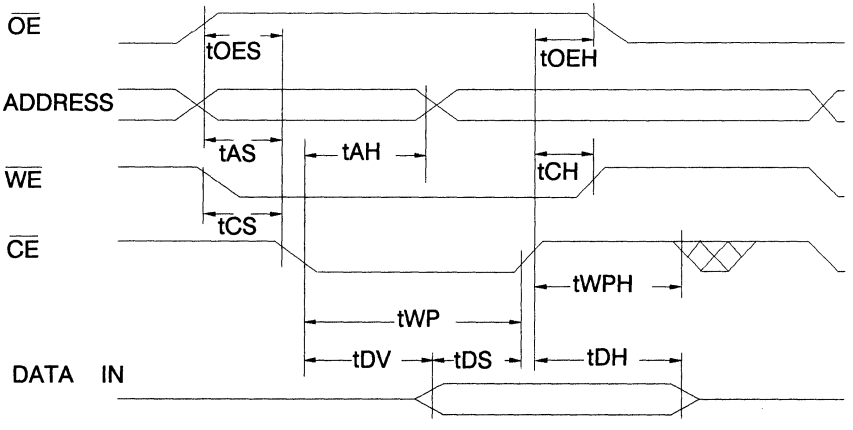
Symbol	Parameter		Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time		0			ns
t_{AH}	Address Hold Time		50			ns
t_{CS}	Chip Select Set-up Time		0			ns
t_{CH}	Chip Select Hold Time		0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100			ns
t_{DS}	Data Set-up Time		50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		0			ns
t_{DV}	Time to Data Valid		NR[1]			
t_{WC}	Write Cycle Time	AT28C256			10	ms
		AT28C256F			3.0	ms

Note: 1. NR = No Restriction

A.C. Write Waveforms - $\overline{WE}$ Controlled



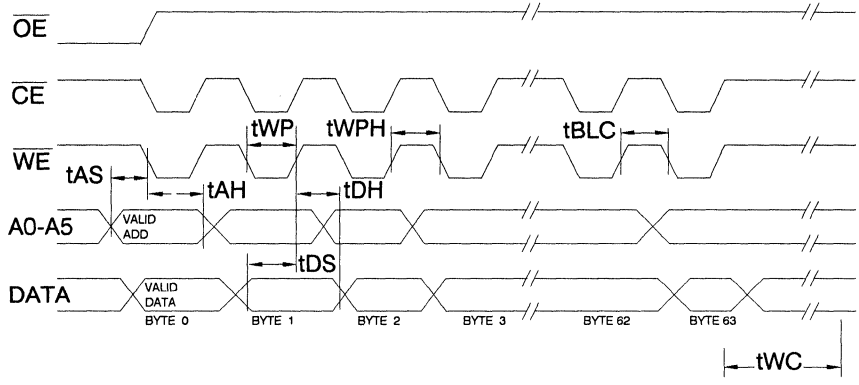
A.C. Write Waveforms - $\overline{CE}$ Controlled



Page Mode Write Characteristics

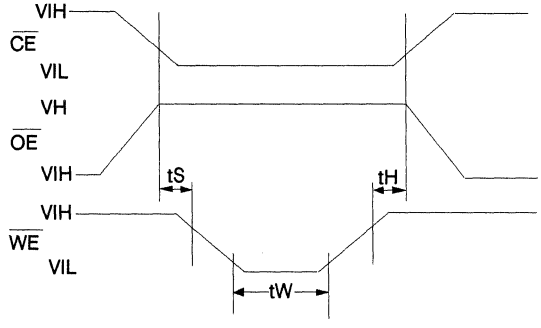
Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time AT28C256			10	ms
	AT28C256F			3.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100			ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms



Note: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

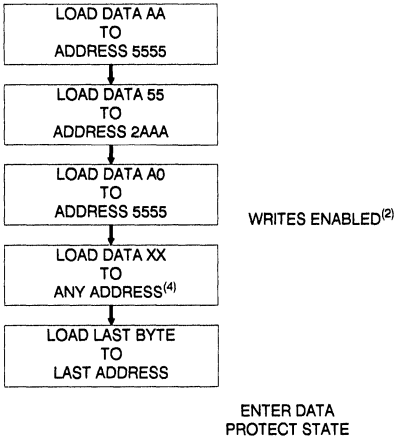


$t_S = t_H = 5\mu sec$ (min.)

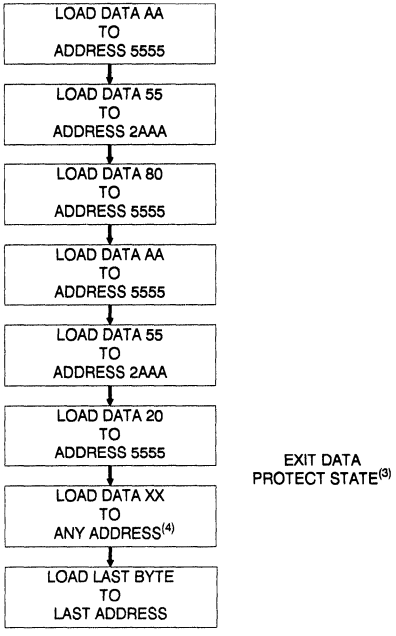
$t_W = 10msec$ (min.)

$V_H = 12 \pm 0.5V$

Software Data Protection Enable Algorithm [1]

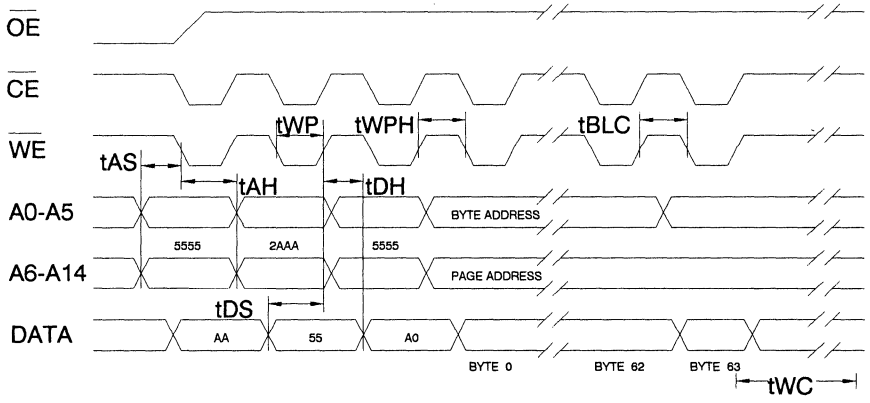


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data may be loaded.

Software Protected Write Cycle Waveforms



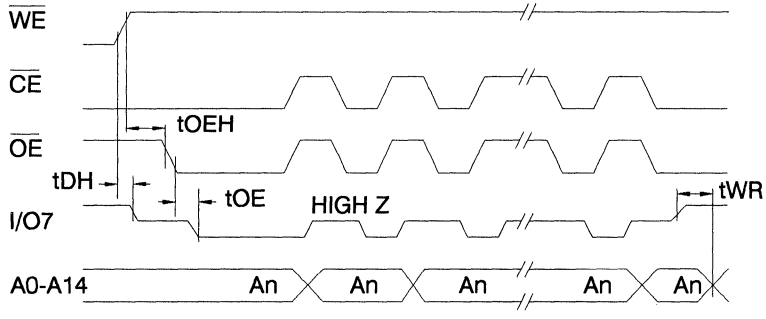
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{DATA}}$ Polling Waveforms

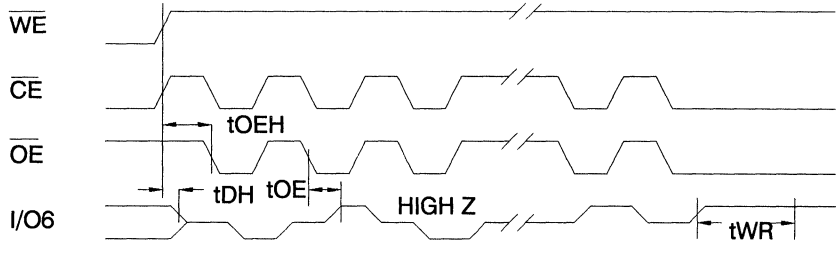


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

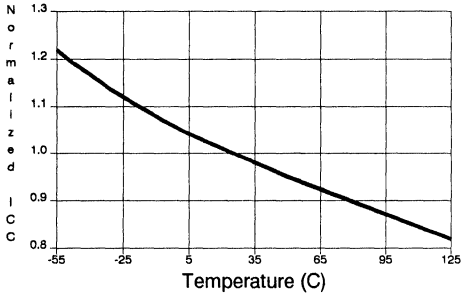
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

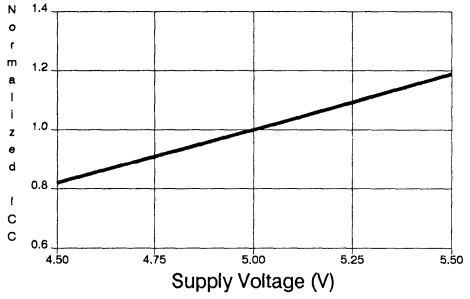


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

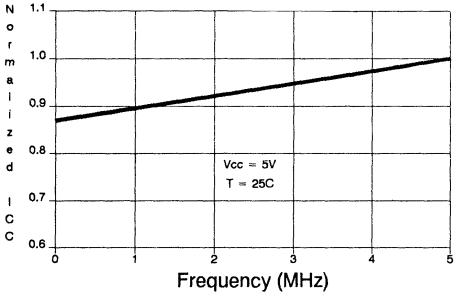
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.2	AT28C256(E,F)-15DC AT28C256(E,F)-15FC AT28C256(E,F)-15JC AT28C256(E,F)-15LC AT28C256(E,F)-15PC AT28C256(E,F)-15UC AT28C256-15W	28D6 28F 32J 32L 28P6 28U DIE	Commercial (0°C to 70°C)
			AT28C256(E,F)-15DI AT28C256(E,F)-15FI AT28C256(E,F)-15JI AT28C256(E,F)-15LI AT28C256(E,F)-15PI AT28C256(E,F)-15UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
150	80	0.3	AT28C256(E,F)-15DM AT28C256(E,F)-15FM AT28C256(E,F)-15LM AT28C256(E,F)-15UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28C256(E,F)-15DM/883 AT28C256(E,F)-15FM/883 AT28C256(E,F)-15LM/883 AT28C256(E,F)-15UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.2	AT28C256(E,F)-20DC AT28C256(E,F)-20FC AT28C256(E,F)-20JC AT28C256(E,F)-20LC AT28C256(E,F)-20PC AT28C256(E,F)-20UC AT28C256-20W	28D6 28F 32J 32L 28P6 28U DIE	Commercial (0°C to 70°C)
			AT28C256(E,F)-20DI AT28C256(E,F)-20FI AT28C256(E,F)-20JI AT28C256(E,F)-20LI AT28C256(E,F)-20PI AT28C256(E,F)-20UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
200	80	0.3	AT28C256(E,F)-20DM AT28C256(E,F)-20FM AT28C256(E,F)-20LM AT28C256(E,F)-20UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28C256(E,F)-20DM/883 AT28C256(E,F)-20FM/883 AT28C256(E,F)-20LM/883 AT28C256(E,F)-20UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	80	0.2	AT28C256(E,F)-25DC AT28C256(E,F)-25FC AT28C256(E,F)-25JC AT28C256(E,F)-25LC AT28C256(E,F)-25PC AT28C256(E,F)-25UC AT28C256-25W	28D6 28F 32J 32L 28P6 28U DIE	Commercial (0°C to 70°C)
			AT28C256(E,F)-25DI AT28C256(E,F)-25FI AT28C256(E,F)-25JI AT28C256(E,F)-25LI AT28C256(E,F)-25PI AT28C256(E,F)-25UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
250	80	0.3	AT28C256(E,F)-25DM AT28C256(E,F)-25FM AT28C256(E,F)-25LM AT28C256(E,F)-25UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28C256(E,F)-25DM/883 AT28C256(E,F)-25FM/883 AT28C256(E,F)-25LM/883 AT28C256(E,F)-25UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	80	0.3	AT28C256(E,F)-30DM/883 AT28C256(E,F)-30FM/883 AT28C256(E,F)-30LM/883 AT28C256(E,F)-30UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	80	0.3	AT28C256(E,F)-35DM/883 AT28C256(E,F)-35FM/883 AT28C256(E,F)-35LM/883 AT28C256(E,F)-35UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.35	5962-88525 07 XX 5962-88525 07 YX 5962-88525 07 ZX	28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 06 XX 5962-88525 06 YX 5962-88525 06 ZX	28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.35	5962-88525 04 UX 5962-88525 04 XX 5962-88525 04 YX 5962-88525 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.35	5962-88525 03 UX 5962-88525 03 XX 5962-88525 03 YX 5962-88525 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 05 XX 5962-88525 05 YX 5962-88525 05 ZX	28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
300	80	0.35	5962-88525 02 UX 5962-88525 02 XX 5962-88525 02 YX 5962-88525 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	80	0.35	5962-88525 01 UX 5962-88525 01 XX 5962-88525 01 YX 5962-88525 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3ms

1 Megabit (128K x 8) Paged CMOS E^2PROM Module

Features

- **Fast Read Access Time - 120ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 64 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Page Write Cycle Time: 10ms maximum**
  - **1 to 64 Byte Page Write Operation**
- **Low Power Dissipation**
  - **100mA Active Current**
  - **5mA Standby Current**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10,000 cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

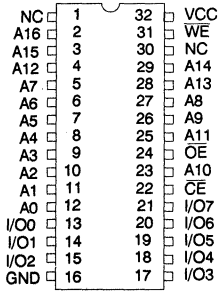
Description

The AT28MC010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 1 MBit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 120ns with power dissipation of just 550mW. When the device is deselected, the CMOS standby current is typically less than 100µA.

The AT28MC010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28MC010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes.

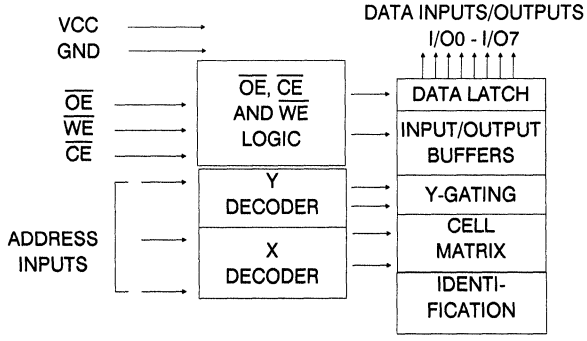
Pin Configurations



PIN NAMES

A0 - A16	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Block Diagram



Device Operation

READ: The AT28MC010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28MC010 allows one to 64 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end, and the internal programming period will start. A6 to A16 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28MC010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28MC010 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero (A15 and A16 must address the page being written). Once the write has completed, I/O6 will stop toggling, and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28MC010 in the following ways: (a) Vcc sense – if Vcc is below 3.8V (typical) the write function is inhibited (b) Vcc power on delay – once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write (c) Write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles (d) Noise filter – pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28MC010. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28MC010-12	AT28MC010-15	AT28MC010-20	AT28MC010-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms.

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		20	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		20	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-.3V to V_{CC} + 1V		5	mA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		8	mA
I_{CC}	V_{CC} Active Current	f = 5MHz; I_{OUT} = 0mA $\overline{CE}$ = 0V, $\overline{OE}$ = $\overline{WE}$ = V_{CC}		100	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		.45	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V

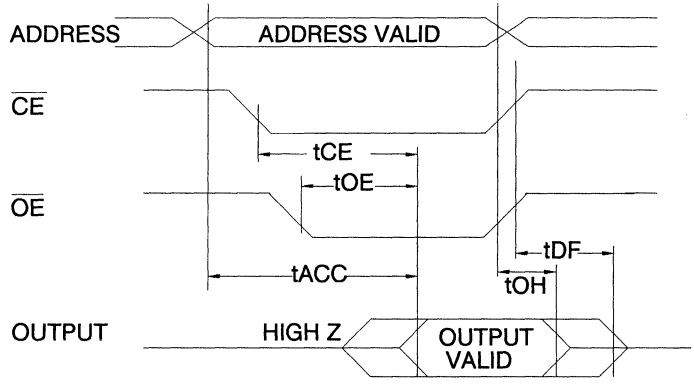
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	20	40	pF	V_{IN} = 0V
C_{OUT}	20	40	pF	V_{OUT} = 0V

A.C. Read Characteristics

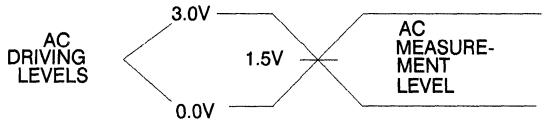
Symbol	Parameter	AT28MC010-12 Min	AT28MC010-12 Max	AT28MC010-15 Min	AT28MC010-15 Max	AT28MC010-20 Min	AT28MC010-20 Max	AT28MC010-25 Min	AT28MC010-25 Max	Units
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	60	0	70	0	80	0	100	ns
t_{DF}[3,4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



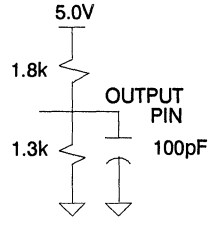
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load

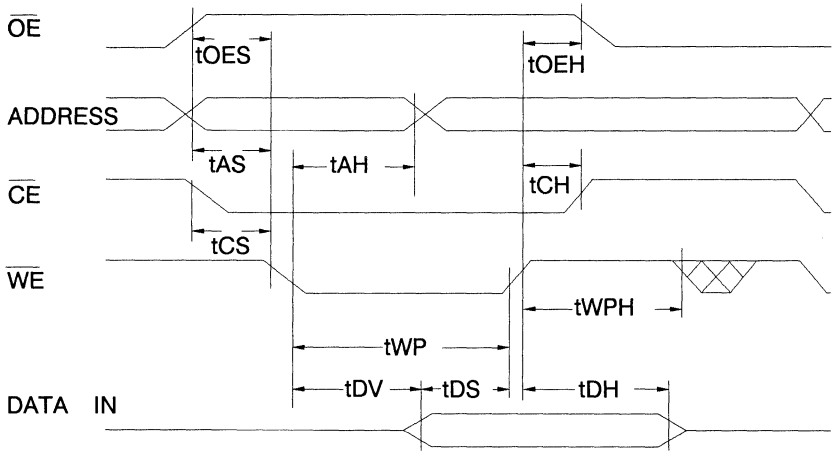


A.C. Write Characteristics

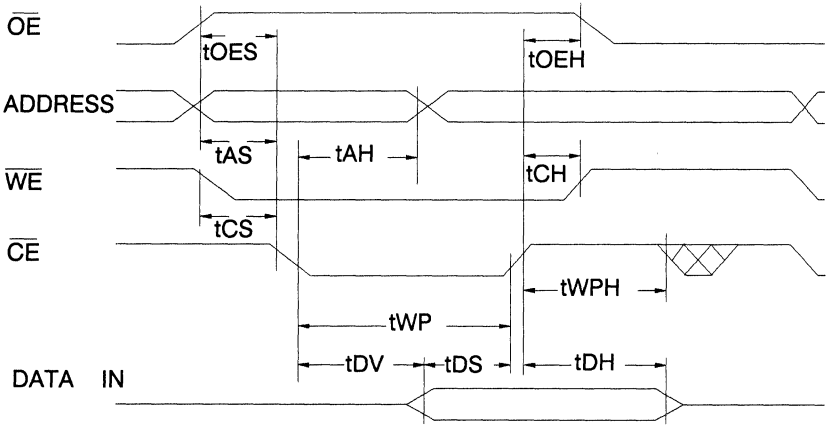
Symbol	Parameter	Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	10			ns
t_{AH}[1]	Address Hold Time	100			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150			ns
t_{DS}	Data Set-up Time	100			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10			ns
t_{DV}	Time to Data Valid	NR[2]			
t_{WC}	Write Cycle Time		5.0	10	ms

Note: 1. A15 and A16 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.
2. NR = No Restriction

A.C. Write Waveforms - $\overline{WE}$ Controlled



A.C. Write Waveforms - $\overline{CE}$ Controlled

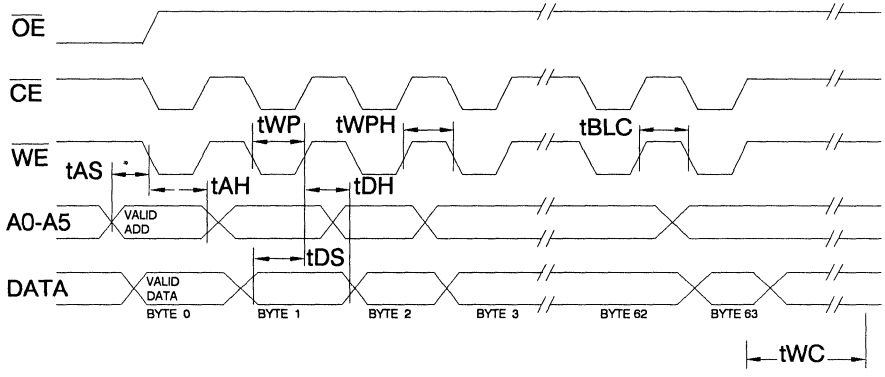


Page Mode Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		5	10	ms
t_{AS}	Address Set-up Time	10			ns
t_{AH}[1]	Address Hold Time	100			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	10			ns
t_{WP}	Write Pulse Width	150			ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High	100			ns
t_{DW}	Delay to Next Write	0			ns

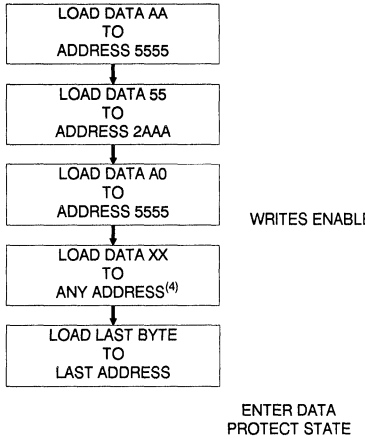
Note: 1. A15 and A16 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

Page Mode Write Waveforms

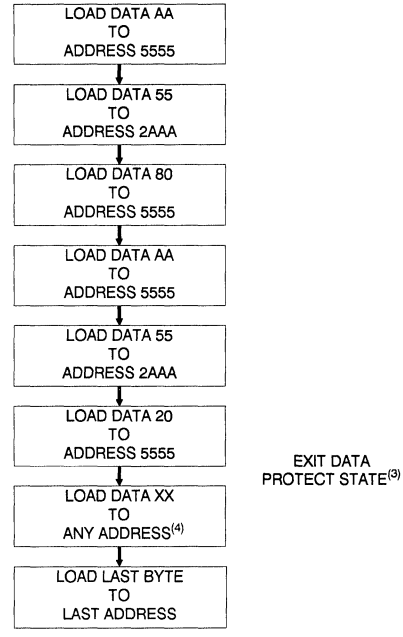


Note: A6 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm [1,5,6]

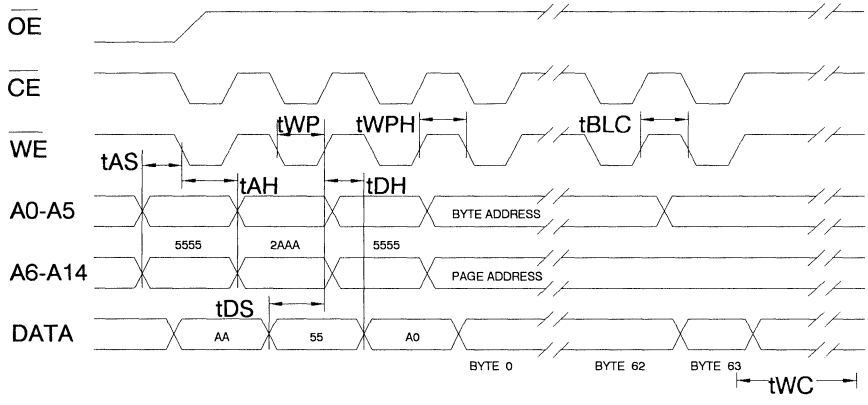


Software Data Protection Disable Algorithm [1,5,6]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data may be loaded.
5. A15 and A16 must address page to be written.
6. Quadrants determined by A15 and A16 act independently.

Software Protected Write Cycle Waveforms



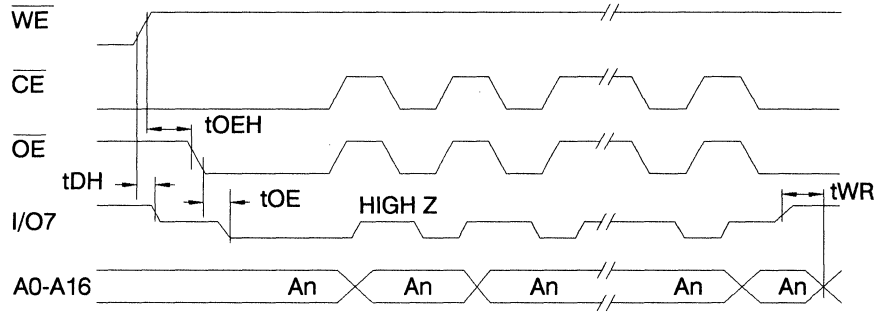
Notes: A6 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{DATA}}$ Polling Waveforms

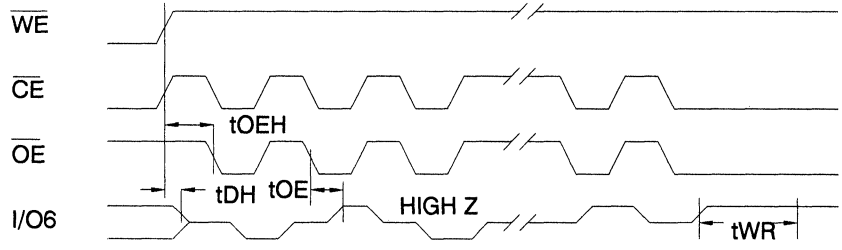


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location within quadrant determined by A15 and A16 may be used but the address should not vary.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	100	0.5	AT28MC010-12MC	32M	Commercial (0° to 70°C)
			AT28MC010-12MI	32M	Industrial (-40° to 85°C)
			AT28MC010-12MM	32M	Military (-55°C to 125°C)
			AT28MC010-12MMB	32M	Military/883C Class B Components (-55°C to 125°C)
150	100	0.5	AT28MC010-15MC	32M	Commercial (0° to 70°C)
			AT28MC010-15MI	32M	Industrial (-40° to 85°C)
			AT28MC010-15MM	32M	Military (-55°C to 125°C)
			AT28MC010-15MMB	32M	Military/883C Class B Components (-55°C to 125°C)
200	100	0.5	AT28MC010-20MC	32M	Commercial (0° to 70°C)
			AT28MC010-20MI	32M	Industrial (-40° to 85°C)
			AT28MC010-20MM	32M	Military (-55°C to 125°C)
			AT28MC010-20MMB	32M	Military/883C Class B Components (-55°C to 125°C)
250	100	0.5	AT28MC010-25MC	32M	Commercial (0° to 70°C)
			AT28MC010-25MI	32M	Industrial (-40° to 85°C)
			AT28MC010-25MM	32M	Military (-55°C to 125°C)
			AT28MC010-25MMB	32M	Military/883C Class B Components (-55°C to 125°C)

Package Type	
32M	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Module (Module)

1 Megabit (64K x 16) Paged CMOS E^2PROM

Preliminary

Features

- Fast Read Access Time - 120ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Words
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10ms maximum
  - 1 to 64 Word Page Write Operation
- Low Power Dissipation
  - 100mA Active Current
  - 400μA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

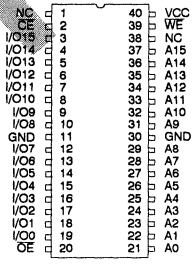
Description

The AT28C1024 is a high performance Electrically Erasable and Programmable Read Only Memory. Its 1 MBit of memory is organized as 65,536 words by 16 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times down to 120ns with power dissipation of just 550mW. When the device is deselected, the CMOS standby current is less than 400μA.

The AT28C1024 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-word page register to allow writing of up to 64 words simultaneously. During a write cycle, the addresses and 1 to 64 words of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7 or I/O15. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C1024 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 words of E^2PROM for device identification or tracking.

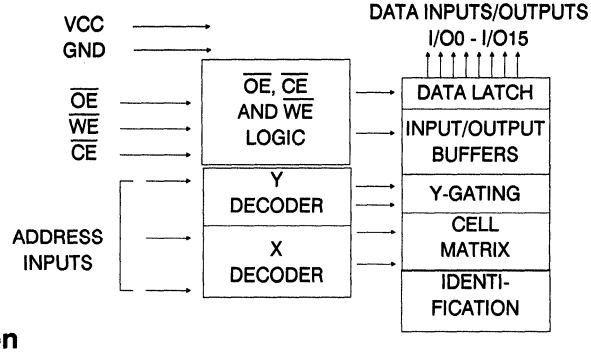
Pin Configurations



PIN NAMES

A0 - A15	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

Block Diagram



Device Operation

READ: The AT28C1024 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28C1024 allows 1 to 64 words of data to be loaded into the device and then simultaneously written during the internal programming period. After the first word has been loaded into the device successive words may be loaded in the same manner. Each new word to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding word. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end, and the internal programming period will start. A6 to A15 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 are used to specify which words within the page are to be written. The words may be loaded in any order and may be changed within the same load period. Only words which are specified for writing will be written; unnecessary cycling of other words within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C1024 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a write cycle an attempted read of the last word written will result in the complement of the written data on I/07 and I/O15. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28C1024 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O14 toggling between one and zero. Once the write has completed, I/O14 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28C1024 in the following ways: (a) Vcc sense – if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay – once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter – pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28C1024. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

DEVICE IDENTIFICATION: An extra 64 words of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations FFC0H to FFFFH the additional words may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Rating*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28C1024-12	AT28C1024-15	AT28C1024-20	AT28C1024-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. V_H = 12.0 ± 0.5V.

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-.3V to V_{CC} + 1V		500	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		5	mA
I_{CC}	V_{CC} Active Current	f = 5MHz; I_{OUT} = 0mA		100	mA
V_{IL}	Input Low Voltage		-0.1	0.8	V
V_{IH}	Input High Voltage		2.0	VCC + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		.45	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V

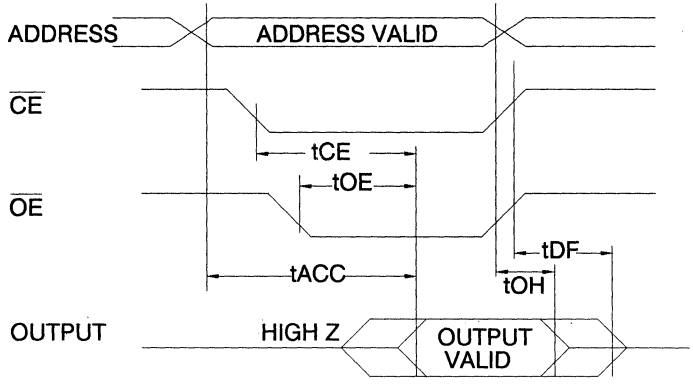
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

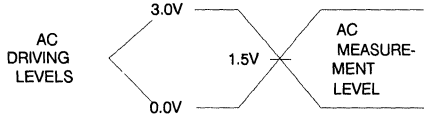
Symbol	Parameter	AT28C1024-12 Min	AT28C1024-12 Max	AT28C1024-15 Min	AT28C1024-15 Max	AT28C1024-20 Min	AT28C1024-20 Max	AT28C1024-25 Min	AT28C1024-25 Max	Units
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	60	0	70	0	80	0	100	ns
t_{DF}[3,4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



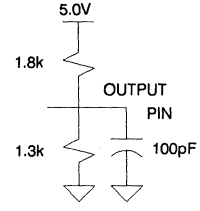
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

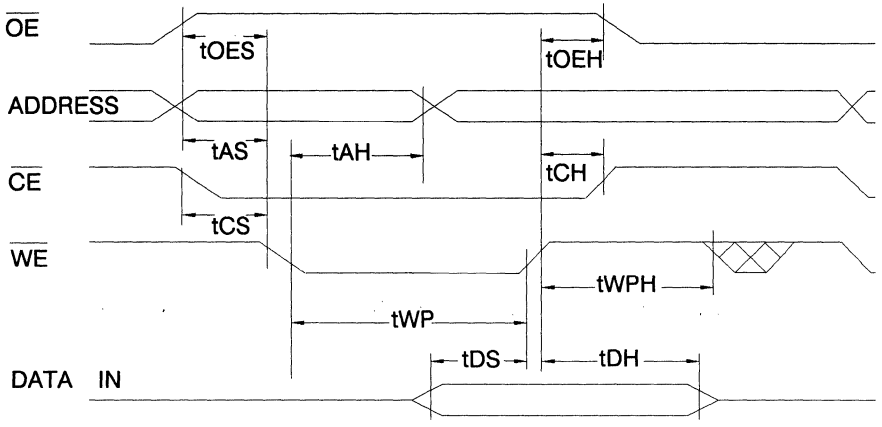
Output Test Load



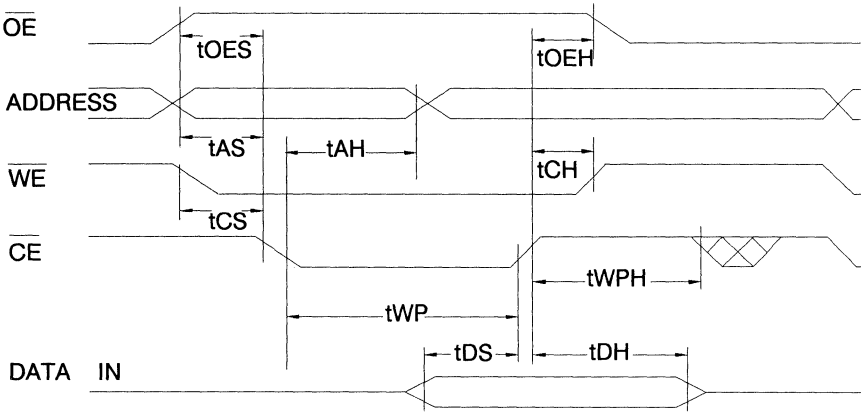
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{WC}	Write Cycle Time		5.0		ms

A.C. Write Waveforms - $\overline{WE}$ Controlled



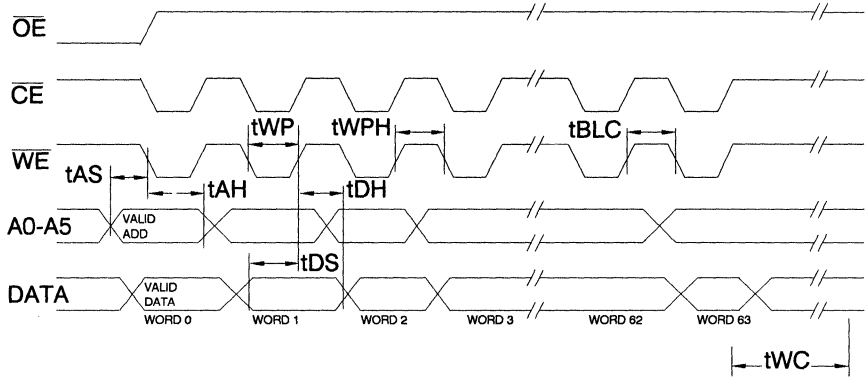
A.C. Write Waveforms - $\overline{CE}$ Controlled



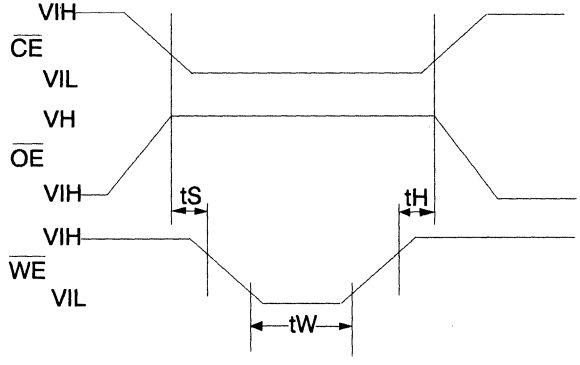
Page Mode Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		5		ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100			ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms



Chip Erase Waveforms

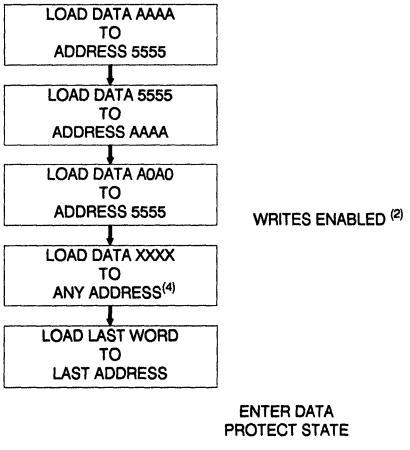


$t_S = t_H = 5\mu sec$ (min.)

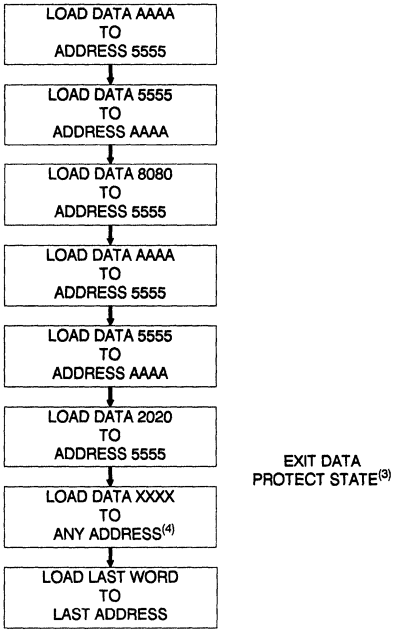
$t_W = 10msec$ (min.)

$V_H = 12 \pm 0.5V$

Software Data Protection Enable Algorithm [1]

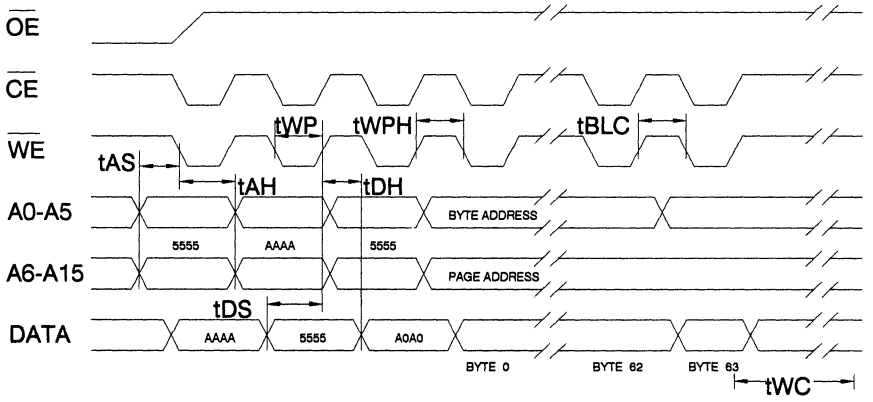


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O15 - I/O0 (Hex);
   Address Format: A15 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 words of data may be loaded.

Software Protected Write Cycle Waveforms



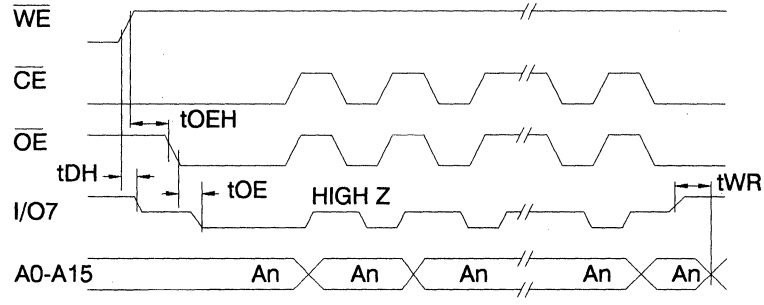
Notes: A6 through A15 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{DATA}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{DATA}}$ Polling Waveforms

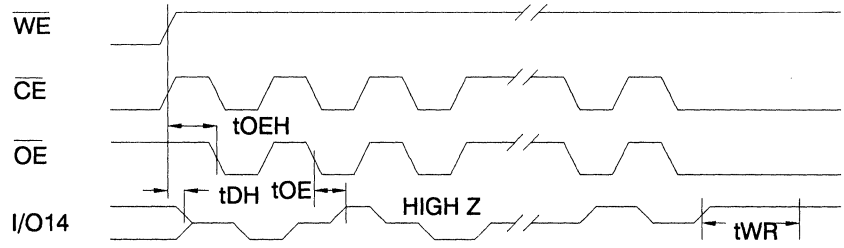


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O14 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	100	0.5	AT28C1024-15BC AT28C1024-15LC	40B 44L	Commercial (0° to 70°C)
			AT28C1024-15BI AT28C1024-15LI	40B 44L	Industrial (-40° to 85°C)
			AT28C1024-15BM AT28C1024-15LM	40B 44L	Military (-55°C to 125°C)
			AT28C1024-15BM/883 AT28C1024-15LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	100	0.5	AT28C1024-20BC AT28C1024-20LC	40B 44L	Commercial (0° to 70°C)
			AT28C1024-20BI AT28C1024-20LI	40B 44L	Industrial (-40° to 85°C)
			AT28C1024-20BM AT28C1024-20LM	40B 44L	Military (-55°C to 125°C)
			AT28C1024-20BM/883 AT28C1024-20LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	100	0.5	AT28C1024-25BC AT28C1024-25LC	40B 44L	Commercial (0° to 70°C)
			AT28C1024-25BI AT28C1024-25LI	40B 44L	Industrial (-40° to 85°C)
			AT28C1024-25BM AT28C1024-25LM	40B 44L	Military (-55°C to 125°C)
			AT28C1024-25BM/883 AT28C1024-25LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
40B	40 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

1 MEGABIT (128K x 8) Paged CMOS E^2PROM

Preliminary

Features

- **Fast Read Access Time - 120ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 128 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Time**
  - **Page Write Cycle Time - 10ms maximum**
  - **1 to 128 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80mA Active Current**
  - **300µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial and Industrial Temperature Ranges**

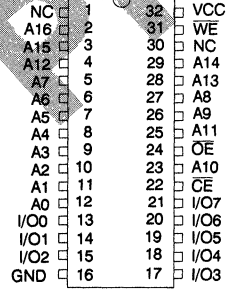
Description

The AT28C010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its one megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 120ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 300µA.

The AT28C010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128 bytes of E^2PROM for device identification or tracking.

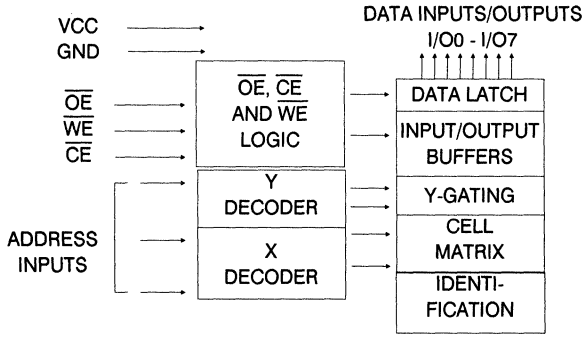
Pin Configurations



PIN NAMES

A0 - A16	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Block Diagram



Device Operation

READ: The AT28C010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28C010 allows one to 128 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C010 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28C010 in the following ways: (a) Vcc sense – if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay – once Vcc has reached 3.8V (typical) the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter – pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28C010. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

DEVICE IDENTIFICATION: An extra 128 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 1FF80H to 1FFFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

D.C. and A.C. Operating Range

		AT28C010-12	AT28C010-15	AT28C010-20	AT28C010-25
Operating Temperature	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. V_H = 12.0 ± 0.5V.

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} -.3V to V_{CC} + 1		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz; I_{OUT} = 0mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100µA; V_{CC} = 4.5V	4.2		V

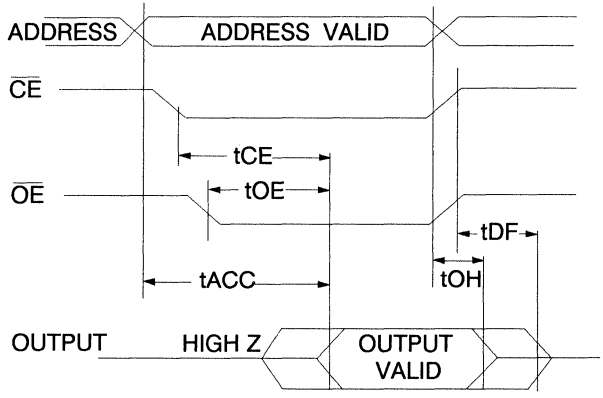
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

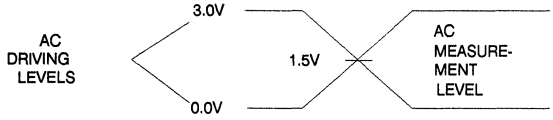
Symbol	Parameter	AT28C010-12 Min	AT28C010-12 Max	AT28C010-15 Min	AT28C010-15 Max	AT28C010-20 Min	AT28C010-20 Max	AT28C010-25 Min	AT28C010-25 Max	Units
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	60	0	70	0	80	0	100	ns
t_{DF}[3,4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



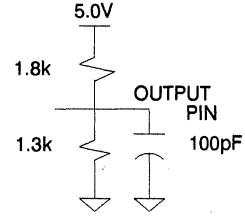
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



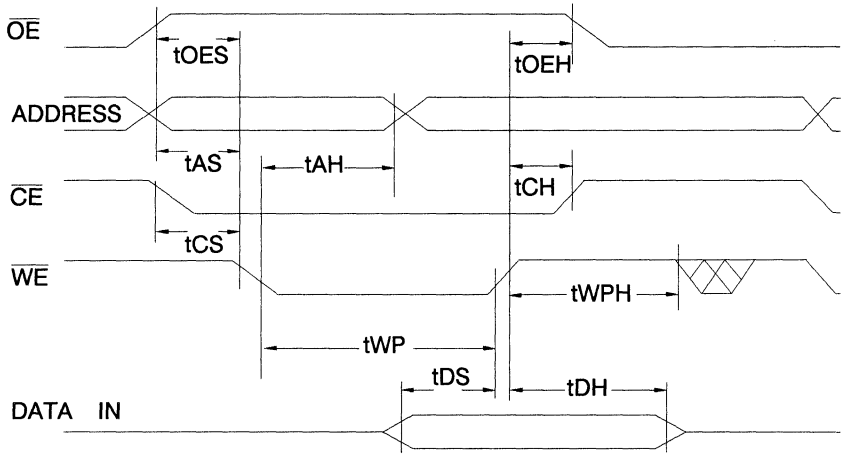
t_R, t_F < 5ns

Output Test Load

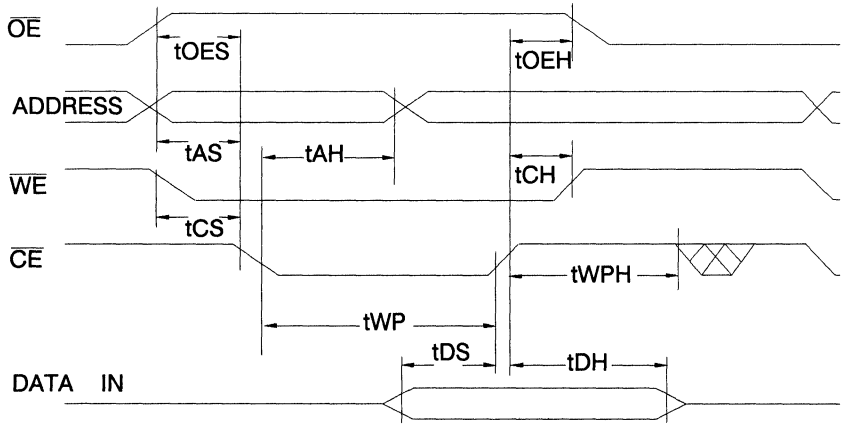


Symbol	Parameter	Min	Typ	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{WC}	Write Cycle Time			10	ms

A.C. Write Waveforms - $\overline{WE}$ Controlled



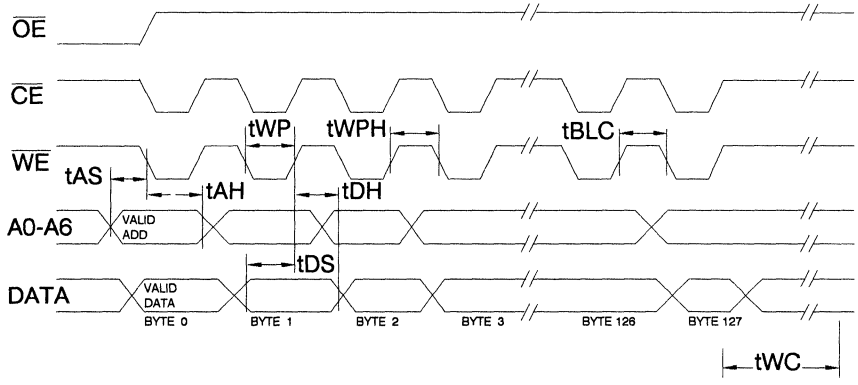
A.C. Write Waveforms - $\overline{CE}$ Controlled



Page Mode Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time			10	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100			ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms



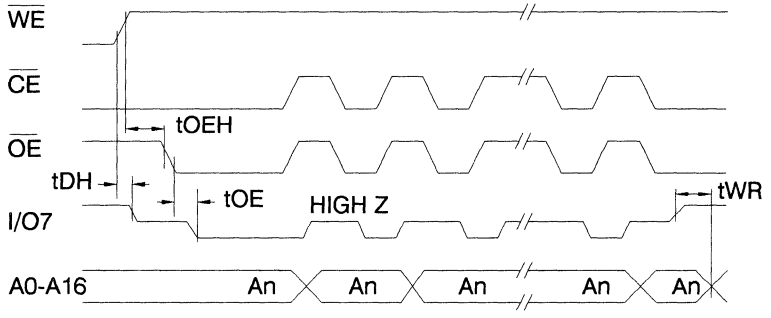
Note: A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics [1]

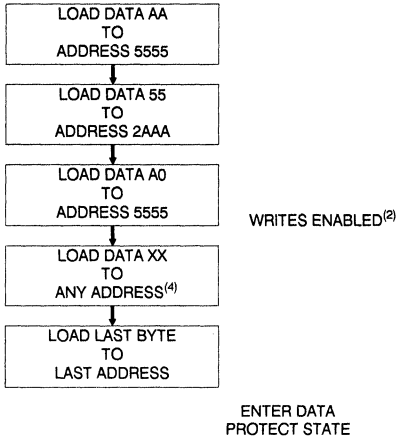
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

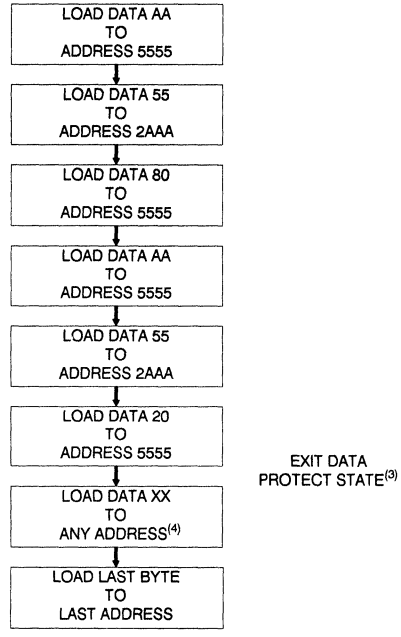
$\overline{\text{DATA}}$ Polling Waveforms



Software Data Protection Enable Algorithm [1]



Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.3	AT28C010-15BC AT28C010-15LC	32B 44L	Commercial (0° to 70°C)
			AT28C010-15BI AT28C010-15LI	32B 44L	Industrial (-40° to 85°C)
			AT28C010-15BM AT28C010-15LM	32B 44L	Military (-55°C to 125°C)
			AT28C010-15BM/883 AT28C010-15LM/883	32B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT28C010-20BC AT28C010-20LC	32B 44L	Commercial (0° to 70°C)
			AT28C010-20BI AT28C010-20LI	32B 44L	Industrial (-40° to 85°C)
			AT28C010-20BM AT28C010-20LM	32B 44L	Military (-55°C to 125°C)
			AT28C010-20BM/883 AT28C010-20LM/883	32B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT28C010-25BC AT28C010-25LC	32B 44L	Commercial (0° to 70°C)
			AT28C010-25BI AT28C010-25LI	32B 44L	Industrial (-40° to 85°C)
			AT28C010-25BM AT28C010-25LM	32B 44L	Military (-55°C to 125°C)
			AT28C010-25BM/883 AT28C010-25LM/883	32B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
32B	32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

ATMEL

CONTENTS

Section 3

Features

- **Fast Read Access Time - 150ns**
- **Five Volt Only Reprogramming**
- **Page Program Operation**
  - **Single Cycle Reprogram (Erase and Program)**
  - **Internal Address and Data Latches for 64 Bytes**
- **Fast Program Cycle Times**
  - **Page (64 Byte) Program Time - 10ms**
  - **Chip Erase Time - 10ms**
- **Internal Program Control Timer**
- **Low Power Dissipation**
  - **80mA Active Current**
  - **300μA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Program Detection**
- **High Reliability CMOS Technology**
  - **1000 Erase/Program Cycles**
  - **10 Year Data Retention**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Full Military, Commercial, and Industrial Temperature Ranges**

256K (32K x 8) 5 Volt Only CMOS PEROM

Preliminary

3

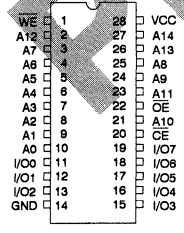
Description

The AT29C256 is a 5 volt only in system Programmable and Erasable Read Only Memory (PEROM). Its 256k of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 300μA.

To allow for simple in-system reprogrammability, the AT29C256 does not require high input voltages for programming. Five volt only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C256 is performed on a page basis; 64 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six byte software code (although erasure before programming is not needed).

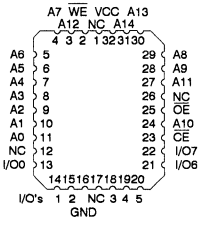
During a reprogram cycle, the address locations and 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Pin Configurations



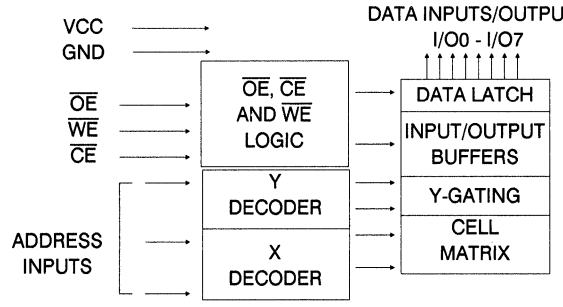
PIN NAMES

A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Device Operation

READ: The AT29C256 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Byte loads are used to enter the 64 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be erased to read FFh. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

$\overline{DATA}$ POLLING: The AT29C256 features $\overline{DATA}$ Polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT29C256 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C256 in the following ways: (a) Vcc sense – if Vcc is below 3.8V (typical), the program function is inhibited. (b) Vcc power on delay – once Vcc has reached the Vcc sense level, the device will automatically time out 5ms (typical) before programming. (c) Program inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter – pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C256. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

5 VOLT CHIP ERASE: The entire device may be erased at one time by using a six byte software code. The erase code consists of six byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFh). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required.

HIGH VOLTAGE CHIP ERASE: The contents of the entire device may be set to the high state by using an externally timed high voltage operation. $\overline{OE}$ is first raised to 12 volts with $\overline{CE}$ low and $\overline{WE}$ high; when $\overline{WE}$ is pulsed low for a minimum of 10ms, the contents of the entire device is erased.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

D.C. and A.C. Operating Range

		AT29C256-15	AT29C256-20	AT29C256-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
High Voltage Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. V_H = 12.0 ± 0.5V.

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz; I_{OUT} = 0mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100µA; V_{CC} = 4.5V	4.2		V

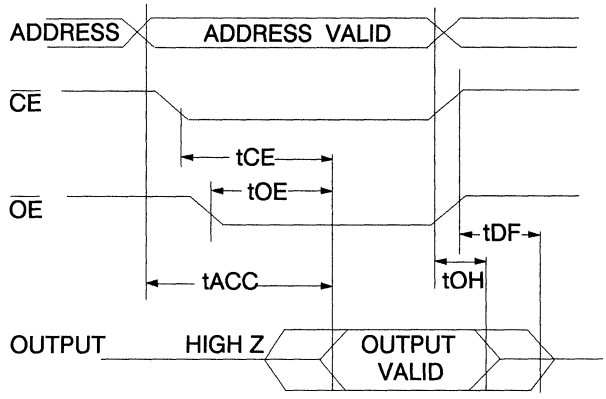
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

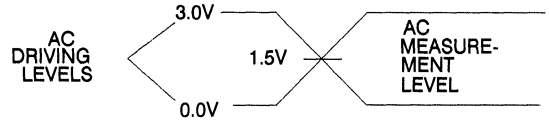
Symbol	Parameter	AT29C256-15 Min	AT29C256-15 Max	AT29C256-20 Min	AT29C256-20 Max	AT29C256-25 Min	AT29C256-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF}[3,4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



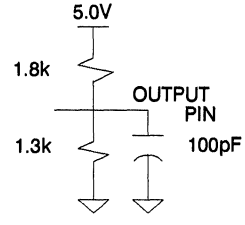
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load

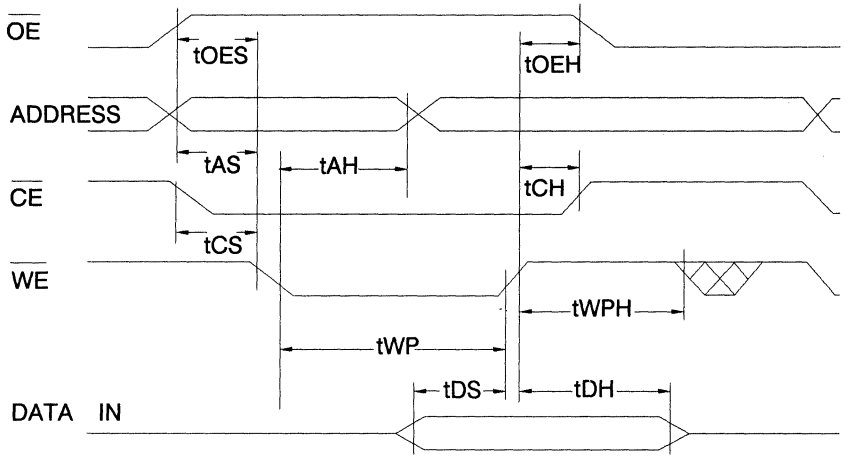


A.C. Byte Load Characteristics

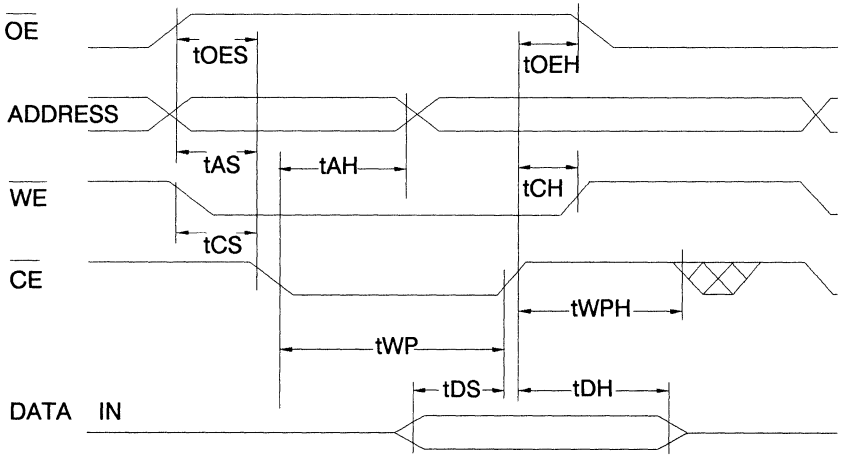
Symbol	Parameter	Min	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		10	ms

3

A.C. Byte Load Waveforms - $\overline{WE}$ Controlled



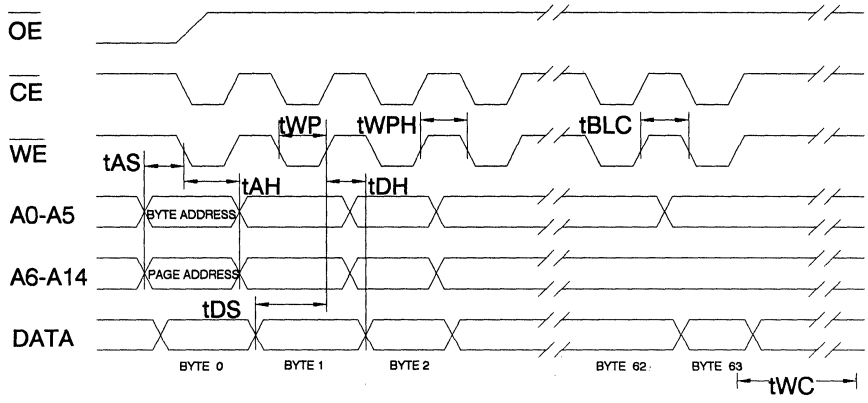
A.C. Byte Load Waveforms - $\overline{CE}$ Controlled



Program Cycle Characteristics

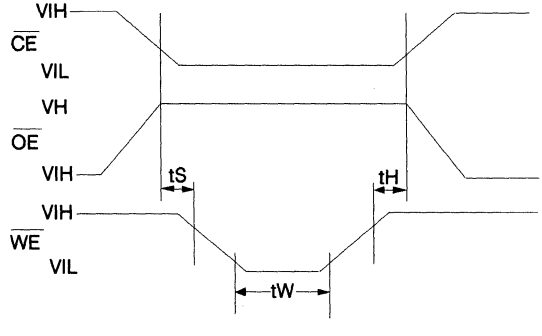
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms



Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

High Voltage Chip Erase Waveforms

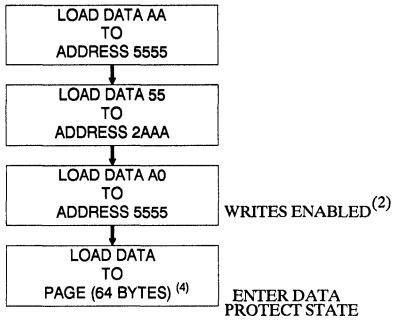


$t_S = t_H = 5\mu sec$ (min.)

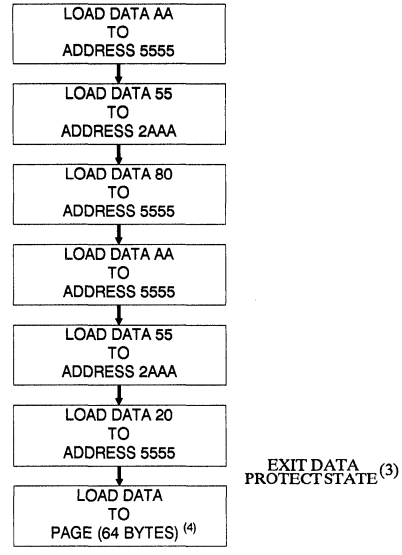
$t_W = 10msec$ (min.)

$V_H = 12.0V$

Software Data Protection Enable Algorithm [1]

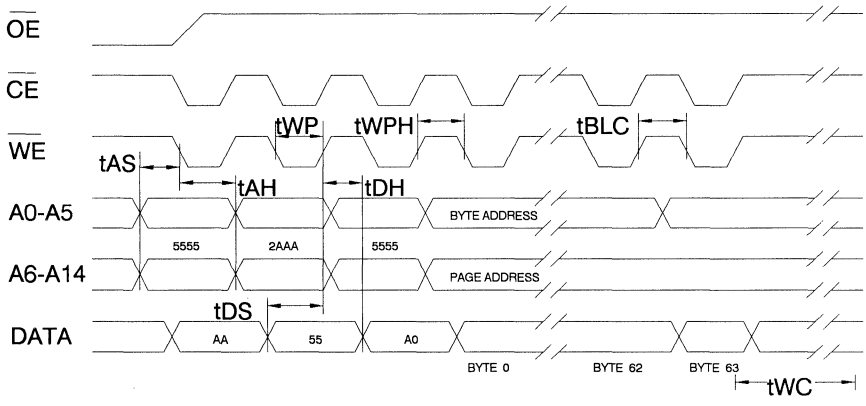


Software Data Protection Disable Algotithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64 bytes of data are loaded.

Software Protected Program Cycle Waveform

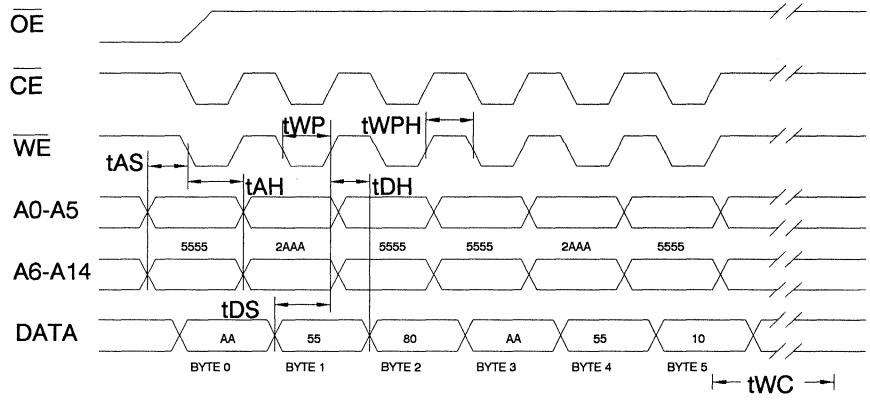


Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

Chip Erase Cycle Characteristics

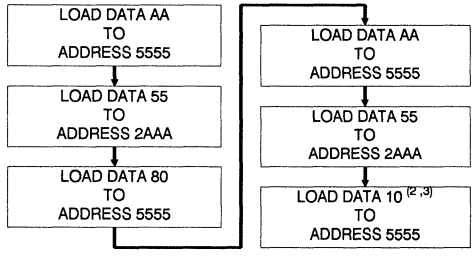
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Chip Erase Cycle Waveforms



Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Software Algorithm [1]



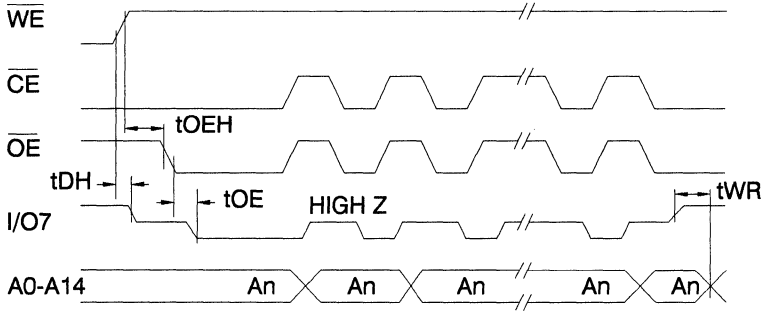
Notes for software erase code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. $\overline{DATA}$ polling may be used to determine the end of the erase cycle by checking any address for data equal to FF.
3. After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within t_{WC}.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{DATA}}$ Polling Waveforms

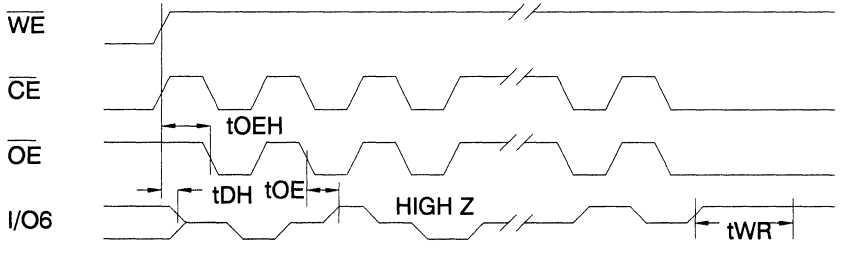


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms



Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.3	AT29C256-15DC AT29C256-15JC AT29C256-15LC AT29C256-15PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-15DI AT29C256-15JI AT29C256-15LI AT29C256-15PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-15DM AT29C256-15LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-15DM/883 AT29C256-15LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT29C256-20DC AT29C256-20JC AT29C256-20LC AT29C256-20PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-20DI AT29C256-20JI AT29C256-20LI AT29C256-20PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-20DM AT29C256-20LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-20DM/883 AT29C256-20LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT29C256-25DC AT29C256-25JC AT29C256-25LC AT29C256-25PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-25DI AT29C256-25JI AT29C256-25LI AT29C256-25PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-25DM AT29C256-25LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-25DM/883 AT29C256-25LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Features

- Fast Read Access Time - 150ns
- Five Volt Only Reprogramming
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - Internal Address and Data Latches for 64 Bytes
- Fast Program Cycle Times
  - Page (64 Byte) Program Time - 10ms
  - Chip Erase Time - 10ms
- Internal Program Control Timer
- Low Power Dissipation
  - 80mA Active Current
  - 300μA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Program Detection
- High Reliability CMOS Technology
  - 1000 Erase/Program Cycles
  - 10 Year Data Retention
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Full Military, Commercial, and Industrial Temperature Ranges

256K (32K x 8) 5 Volt Only CMOS PEROM

3

Preliminary

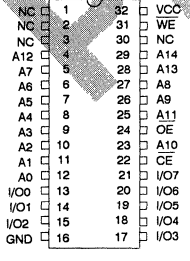
Description

The AT29C257 is a 5 volt only in system Programmable and Erasable Read Only Memory (PEROM). Its 256k of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 300μA.

To allow for simple in-system reprogrammability, the AT29C257 does not require high input voltages for programming. Five volt only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C257 is performed on a page basis; 64 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six byte software code (although erasure before programming is not needed).

During a reprogram cycle, the address locations and 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

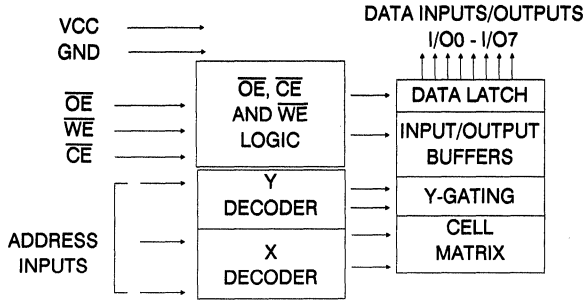
Pin Configurations



PIN NAMES

A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Block Diagram



Device Operation

READ: The AT29C257 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Byte loads are used to enter the 64 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be erased to read FFh. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

$\overline{DATA}$ POLLING: The AT29C257 features $\overline{DATA}$ Polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT29C257 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C257 in the following ways: (a) Vcc sense – if Vcc is below 3.8V (typical), the program function is inhibited. (b) Vcc power on delay – once Vcc has reached the Vcc sense level, the device will automatically time out 5ms (typical) before programming. (c) Program inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter – pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C257. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

5 VOLT CHIP ERASE: The entire device may be erased at one time by using a six byte software code. The erase code consists of six byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFH). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required.

HIGH VOLTAGE CHIP ERASE: The contents of the entire device may be set to the high state by using an externally timed high voltage operation. $\overline{OE}$ is first raised to 12 volts with $\overline{CE}$ low and $\overline{WE}$ high; when $\overline{WE}$ is pulsed low for a minimum of 10ms, the contents of the entire device is erased.

Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground ..... -0.6V to +6.25V

All Output Voltages
with Respect to Ground ..... -0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$
with Respect to Ground ..... -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

D.C. and A.C. Operating Range

		AT29C257-15	AT29C257-20	AT29C257-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
High Voltage Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}. 2. Refer to A.C. Programming Waveforms. 3. V_H = 12.0 ± 0.5V.

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz; I_{OUT} = 0mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100µA; V_{CC} = 4.5V	4.2		V

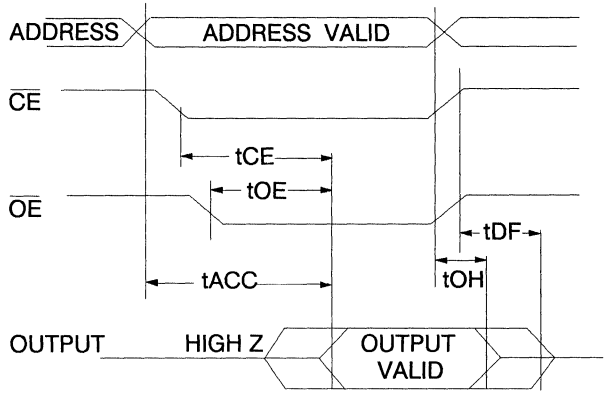
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

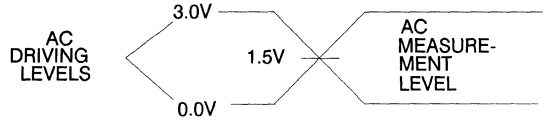
Symbol	Parameter	AT29C257-15 Min	AT29C257-15 Max	AT29C257-20 Min	AT29C257-20 Max	AT29C257-25 Min	AT29C257-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF}[3,4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



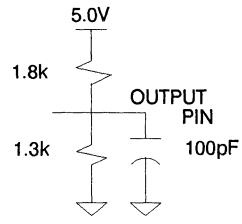
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



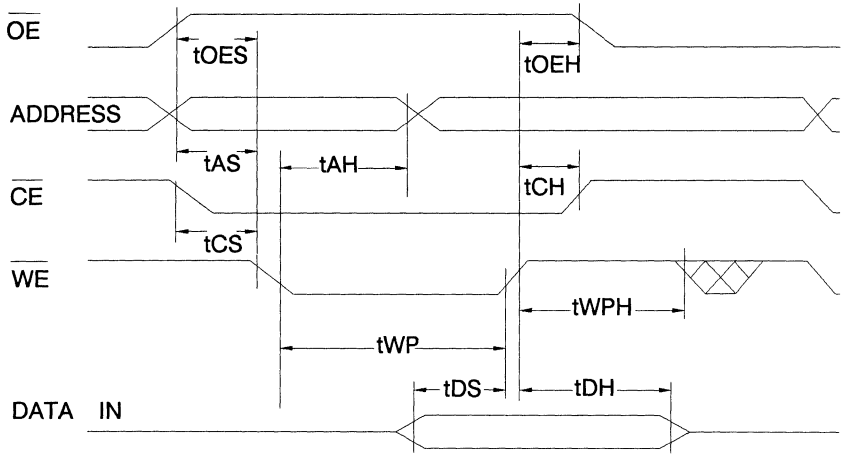
t_R, t_F < 5ns

Output Test Load

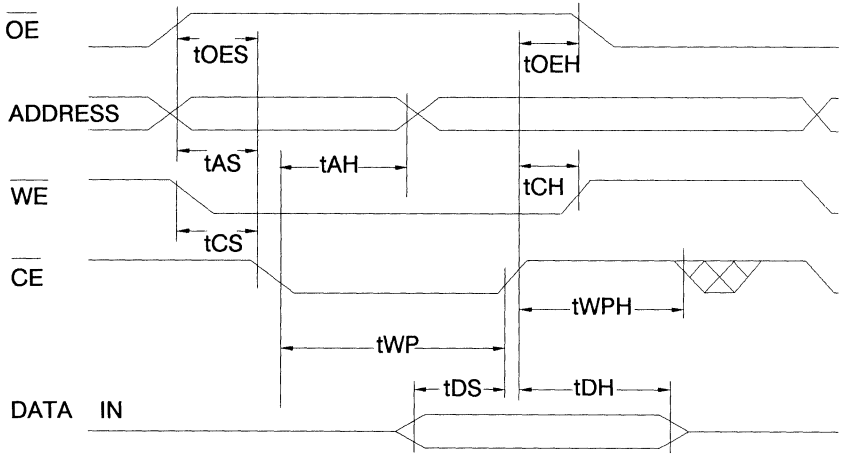


Symbol	Parameter	Min	Max	Units
t_{AS},t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Byte Load Waveforms - $\overline{WE}$ Controlled



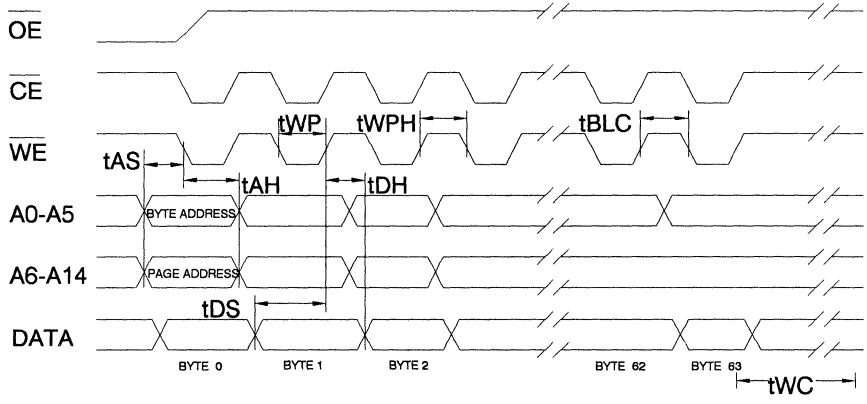
A.C. Byte Load Waveforms - $\overline{CE}$ Controlled



Program Cycle Characteristics

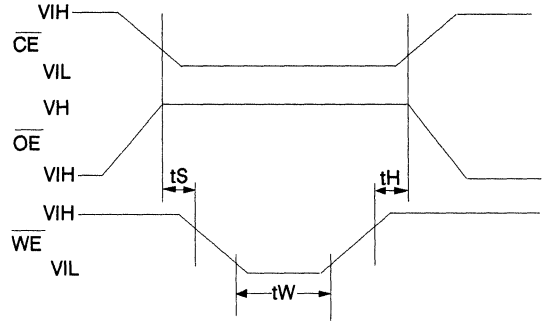
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms



Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

High Voltage Chip Erase Waveforms

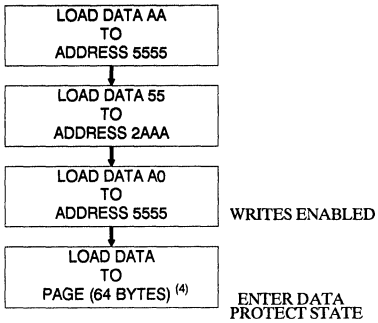


$t_S = t_H = 5\mu sec$ (min.)

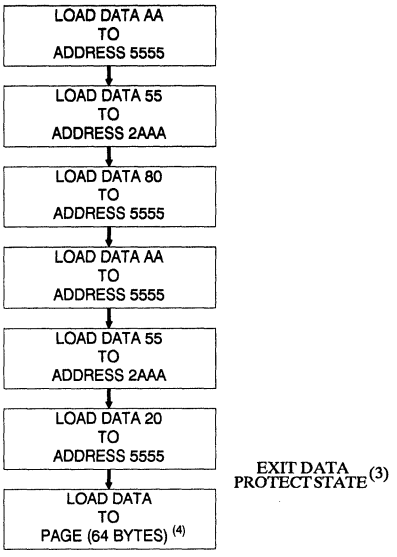
$t_W = 10msec$ (min.)

$V_H = 12.0V \pm 0.5$

Software Data Protection Enable Algorithm [1]

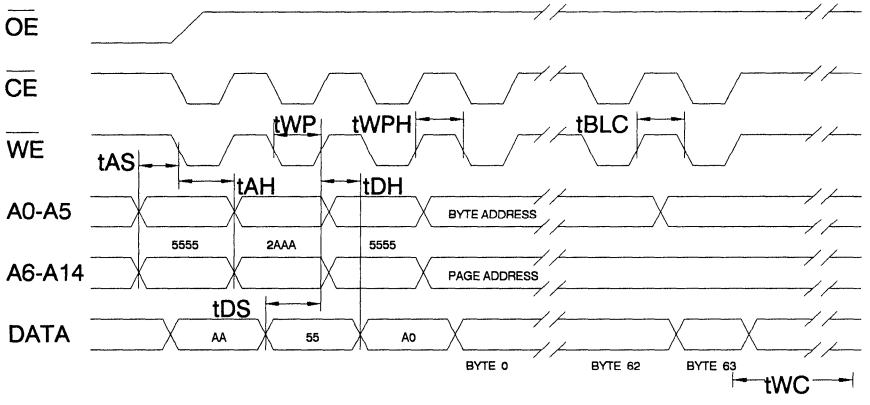


Software Data Protection Disable Algotithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64 bytes of data are loaded.

Software Protected Program Cycle Waveform

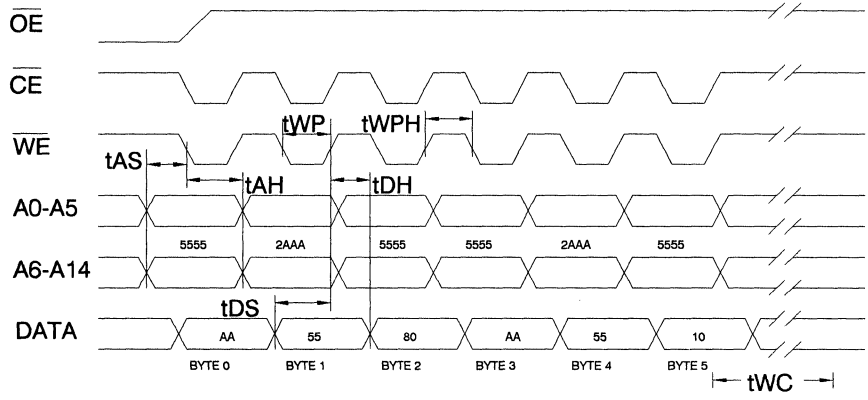


Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

Chip Erase Cycle Characteristics

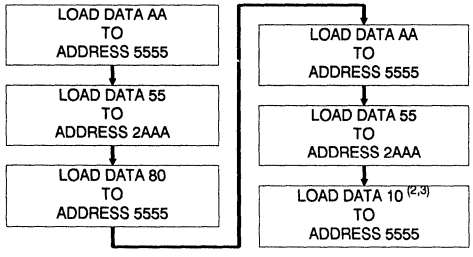
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Chip Erase Cycle Waveforms



Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Software Algorithm [1]



Notes for software erase code:

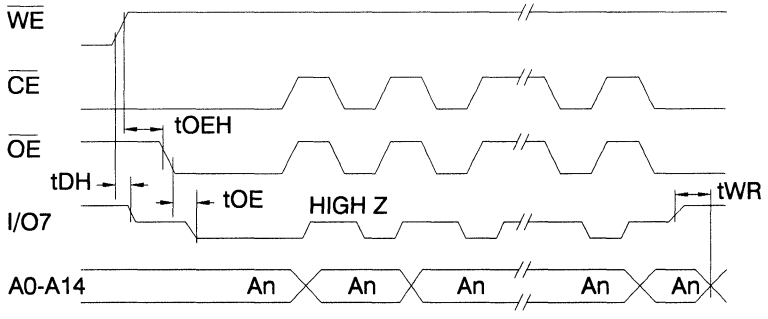
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. $\overline{DATA}$ polling may be used to determine the end of the erase cycle by checking any address for data equal to FF.
3. After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within t_{WC}.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{DATA}}$ Polling Waveforms

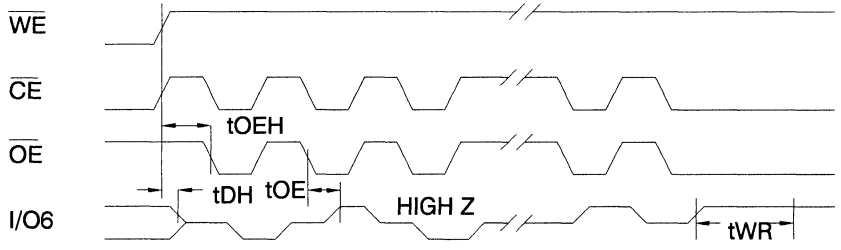


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	OE Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.3	AT29C257-15DC AT29C257-15PC	32D6 32P6	Commercial (0° to 70°C)
			AT29C257-15DI AT29C257-15PI	32D6 32P6	Industrial (-40° to 85°C)
			AT29C257-15DM	32D6	Military (-55°C to 125°C)
			AT29C257-15DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT29C257-20DC AT29C257-20PC	32D6 32P6	Commercial (0° to 70°C)
			AT29C257-20DI AT29C257-20PI	32D6 32P6	Industrial (-40° to 85°C)
			AT29C257-20DM	32D6	Military (-55°C to 125°C)
			AT29C257-20DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT29C257-25DC AT29C257-25PC	32D6 32P6	Commercial (0° to 70°C)
			AT29C257-25DI AT29C257-25PI	32D6 32P6	Industrial (-40° to 85°C)
			AT29C257-25DM	32D6	Military (-55°C to 125°C)
			AT29C257-25DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Features

- Fast Read Access Time - 150ns
- Five Volt Only Reprogramming
- Page Program Operation
  - Internal Address and Data Latches
- Fast Program Cycle Times
  - Page Program Time - 10ms
  - Chip Erase Time - 10ms
- Internal Program Control Timer
- Low Power Dissipation
  - 80mA Active Current
  - 200μA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Program Detection
- High Reliability CMOS Technology
  - 100 Erase/Program Cycles
  - 10 Year Data Retention
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Full Military, Commercial, and Industrial Temperature Ranges

1 Megabit (128K x 8) 5 Volt Only CMOS PEROM

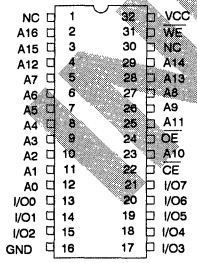
Advance Information

Description

The AT29C010 is a 5 volt only in system Programmable and Erasable Read Only Memory (PEROM). Its one megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 200μA.

To allow for simple in-system reprogrammability, the AT29C010 does not require high input voltages for programming. Five volt only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C010 is performed on a page basis. The contents of the entire device may be erased by using a six byte software code (although erasure before programming is not needed). The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Pin Configurations



PIN NAMES

A0 - A16	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.3	AT29C010-15DC AT29C010-15JC AT29C010-15LC AT29C010-15PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C010-15DI AT29C010-15JI AT29C010-15LI AT29C010-15PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C010-15DM AT29C010-15LM	32D6 32L	Military (-55°C to 125°C)
			AT29C010-15DM/883 AT29C010-15LM/883	32D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT29C010-20DC AT29C010-20JC AT29C010-20LC AT29C010-20PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C010-20DI AT29C010-20JI AT29C010-20LI AT29C010-20PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C010-20DM AT29C010-20LM	32D6 32L	Military (-55°C to 125°C)
			AT29C010-20DM/883 AT29C010-20LM/883	32D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT29C010-25DC AT29C010-25JC AT29C010-25LC AT29C010-25PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C010-25DI AT29C010-25JI AT29C010-25LI AT29C010-25PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C010-25DM AT29C010-25LM	32D6 32L	Military (-55°C to 125°C)
			AT29C010-25DM/883 AT29C010-25LM/883	32D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

CONTENTS

Section 4

CMOS EPROMs

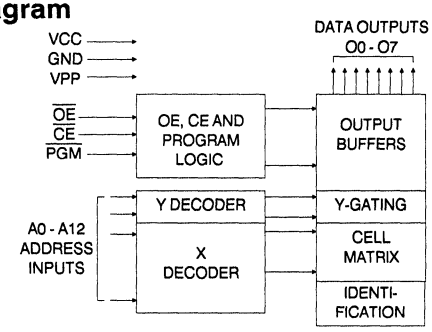
Features

- **Bipolar Speed in JEDEC Standard EPROM Pinout**
  - **Read Access Time - 45ns**
  - **600 mil DIP or LCC packages**
- **Low Power CMOS Operation**
  - **100 μA max. Standby**
  - **75 mA max. Active at 10 MHz**
- **High Output Drive Capability**
- **High Reliability Latch-Up Resistant CMOS Technology**
- **Fast Programming - 4ms/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Commercial and Industrial Temperature Ranges**

64K (8K x 8) High Speed UV Erasable CMOS EPROM

4

Block Diagram



Description

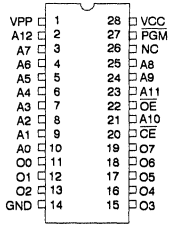
The AT27HC64/64L chip family is a high-speed, low-power 65,536 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM), organized 8K x 8. The AT27HC64 is suited for very high speed applications, while the AT27HC64L features low Vcc Standby Current. Both require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45ns on the AT27HC64, making this part compatible with high performance systems. Power consumption is typically only 40mA in Active Mode on both parts and less than 20μA in Standby on the AT27HC64L.

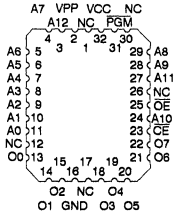
Atmel's 1.5 micron, high speed CMOS technology provides optimum speed, low-power and high noise immunity. The high speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

The AT27HC64/64L come in an industry standard JEDEC-approved 28-lead 64K EPROM pinout. The devices feature a two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention. Both parts are available in either 28-pin 600 mil DIP or 32-pad LCC packages.

Pin Configurations

Pin Name	Function
A0-A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect
O0-O7	Outputs





Description (Continued)

With a storage capacity of 8K bytes, Atmel's 27HC64/64L allow firmware to be stored reliably and to be accessed at bipolar PROM speeds. The AT27HC64/64L have exceptional output drive capability - source 4mA and sink 16mA per output.

The AT27HC64/64L have additional features to ensure high quality and efficient production use. The fast programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27HC64/64L is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15 W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 $W \cdot sec/cm^2$

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	V_{IH}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A12 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC64	AT27HC64 / AT27HC64L		
		-55	-70	-90	-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C(1)	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Notes: 1. AT27HC64 only.

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{PP} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC} + 0.3V			20	µA
I_{SB1}/I_{SB2}	V_{CC} (1) Standby Current	I_{SB1} (CMOS)	AT27HC64L			
		$\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V	Com.		0.1/2	mA
			Ind.,Mil.		0.2/3	mA
		I_{SB2} (TTL)	AT27HC64			
		$\overline{CE}$ = 2.0 to V_{CC} + 1.0V	Com.		35/35	mA
			Ind.,Mil.		40/40	mA
I_{CC}	V_{CC} Active Current	f = 10MHz, I_{OUT} = 0mA,	Com.		75	mA
		$\overline{CE}$ = V_{IL}	Ind.,Mil.		90	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 16mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -4.0mA		2.4		V
V_{PP}	V_{PP} Read Voltage	V_{CC} = 5 ± 0.5V		3.8	5.5	V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

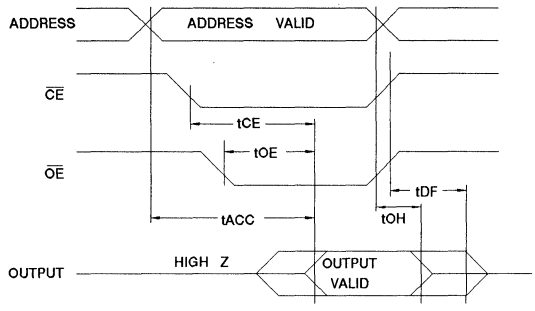
A.C. Characteristics for Read Operation

				AT27HC64	AT27HC64 / AT27HC64L					
				-45	-55		-70		-90	
Symbol	Parameter	Condition		Min Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.,Ind.	45		55		70		90	ns
			Mil.			55(1)		70		90	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		45		55		70		90	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		25		30		35		40	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}		25		30		35		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		0		0	ns

Notes: 1. AT27HC64 only.

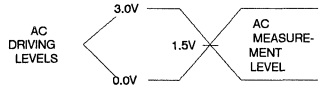
2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



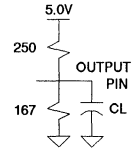
Notes:
1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.
   C_L = 30pF, add 10ns for C_L = 100pF.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. t_{DF} is measured at V_{OH}-0.5V or V_{OL}+0.5V with C_L=5pF.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns (10% to 90%)

Output Test Load



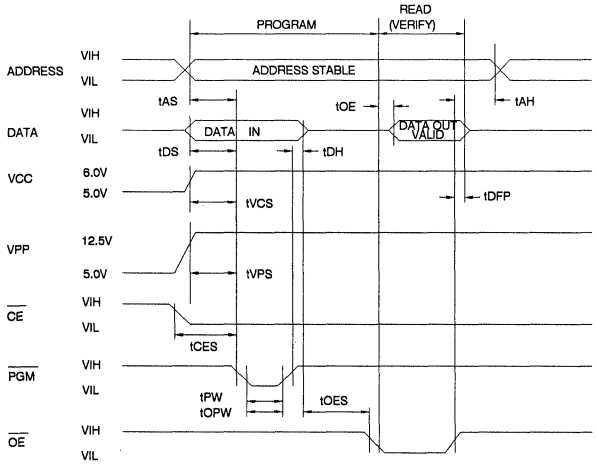
Note: C_L=30pF including jig capacitance.

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.0V for V_{IL} and 3.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27HC64/64L a 0.1μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, V_{PP}=12.5±0.5V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	I_{OL} = 16mA		.4	V
V_{OH}	Output High Volt.	I_{OH} = -4.0mA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			80	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, V_{PP}=12.5±0.5V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(Note 3)	0.95	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(Note 4)	2.85	78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			70	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 5ns
Input Pulse Levels ..... 0.0V to 3.0V
Input Timing Reference Level 1.5V
Output Timing Reference Level 1.5V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Initial Program Pulse width tolerance is 1msec±5%.
4. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

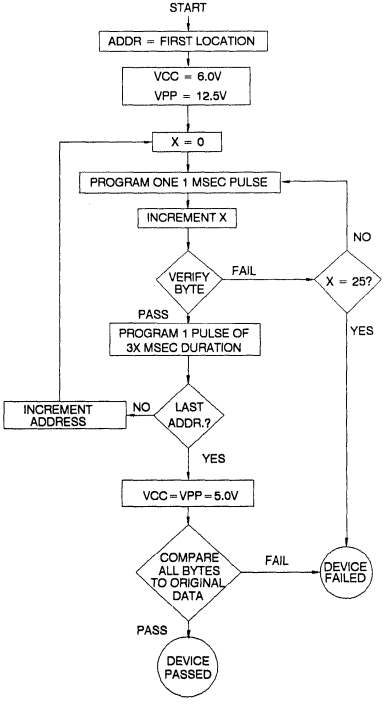
Atmel's 27HC64/L Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	1	1F
Device Type	1	1	0	0	1	0	0	0	1	91

Fast Programming Algorithm

Two $\overline{PGM}$ pulse widths are used to program; initial and overprogram. Ai are set to address the desired byte. V_{CC} is raised to 6.0V. The first $\overline{PGM}$ pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{PGM}$ pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then V_{CC} is lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	75	35	AT27HC64-45DC AT27HC64-45LC	28DW6 32LW	Commercial (0°C to 70°C)
45	90	40	AT27HC64-45DI AT27HC64-45LI	28DW6 32LW	Industrial (-40°C to 85°C)
55	75	35	AT27HC64-55DC AT27HC64-55LC AT27HC64-55PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
55	90	40	AT27HC64-55DI AT27HC64-55LI AT27HC64-55PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64-55DM AT27HC64-55LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64-55DM/883 AT27HC64-55LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	75	35	AT27HC64-70DC AT27HC64-70LC AT27HC64-70PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
70	90	40	AT27HC64-70DI AT27HC64-70LI AT27HC64-70PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64-70DM AT27HC64-70LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64-70DM/883 AT27HC64-70LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	75	35	AT27HC64-90DC AT27HC64-90LC AT27HC64-90PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
90	90	40	AT27HC64-90DI AT27HC64-90LI AT27HC64-90PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64-90DM AT27HC64-90LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64-90DM/883 AT27HC64-90LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	75	0.1	AT27HC64L-55DC AT27HC64L-55LC	28DW6 32LW	Commercial (0°C to 70°C)
55	90	0.2	AT27HC64L-55DI AT27HC64L-55LI	28DW6 32LW	Industrial (-40°C to 85°C)
70	75	0.1	AT27HC64L-70DC AT27HC64L-70LC AT27HC64L-70PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
70	90	0.2	AT27HC64L-70DI AT27HC64L-70LI AT27HC64L-70PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64L-70DM AT27HC64L-70LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64L-70DM/883 AT27HC64L-70LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	75	0.1	AT27HC64L-90DC AT27HC64L-90LC AT27HC64L-90PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
90	90	0.2	AT27HC64L-90DI AT27HC64L-90LI AT27HC64L-90PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64L-90DM AT27HC64L-90LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64L-90DM/883 AT27HC64L-90LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	90	0.2	5962-85102 04 YX 5962-85102 04 ZX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

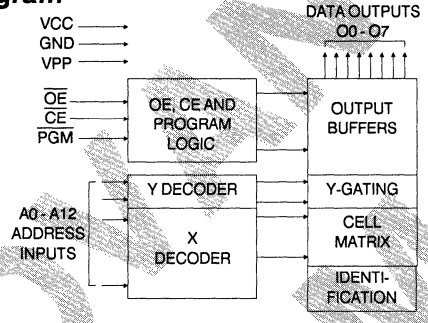
- **Bipolar Speed in JEDEC Standard EPROM Pinout**
  - **Read Access Time - 45ns**
  - **600 mil DIP, and LCC packages**
- **Low Power CMOS Operation**
  - **100 μA max. Standby**
  - **35 mA max. Active at 10 MHz**
- **High Output Drive Capability**
- **High Reliability Latch-Up Resistant CMOS Technology**
- **Rapid Programming - 100μs/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Industrial and Commercial Temperature Ranges**
- **Fully Compatible with AT27HC64/L**

64K (8K x 8) High Speed UV Erasable CMOS EPROM

4

Advance Information

Block Diagram



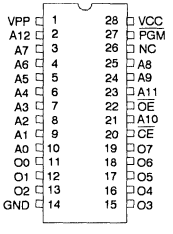
Description

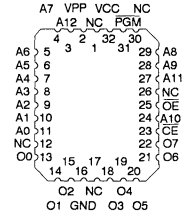
The AT27HC64R/RL chip family is a high-speed, low-power 65,536 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM), organized as 8K x 8 bits. The AT27HC64R is suited for very high-speed applications, while the AT27HC64RL features low Vcc Standby Current. Both require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45ns on the AT27HC64R, making this part ideal for high-performance systems. Power consumption is typically only 25mA in Active Mode on both parts, and less than 10μA in Standby on the AT27HC64RL.

Atmel's 1.2 micron, high-speed CMOS technology provides optimum speed, lower power and high noise immunity. The high-speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

Pin Configurations

Pin Name	Function
A0-A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect
O0-O7	Outputs





Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	35	20	AT27HC64R-45DC AT27HC64R-45LC	28DW6 32LW	Commercial (0°C to 70°C)
45	45	30	AT27HC64R-45DI AT27HC64R-45LI	28DW6 32LW	Industrial (-40°C to 85°C)
55	35	20	AT27HC64R-55DC AT27HC64R-55LC AT27HC64R-55PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
55	45	30	AT27HC64R-55DI AT27HC64R-55LI AT27HC64R-55PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64R-55DM AT27HC64R-55LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64R-55DM/883 AT27HC64R-55LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	35	20	AT27HC64R-70DC AT27HC64R-70LC AT27HC64R-70PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
70	45	30	AT27HC64R-70DI AT27HC64R-70LI AT27HC64R-70PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64R-70DM AT27HC64R-70LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64R-70DM/883 AT27HC64R-70LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	35	20	AT27HC64R-90DC AT27HC64R-90LC AT27HC64R-90PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
90	45	30	AT27HC64R-90DI AT27HC64R-90LI AT27HC64R-90PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64R-90DM AT27HC64R-90LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64R-90DM/883 AT27HC64R-90LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DW6	24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	35	0.1	AT27HC64RL-55DC AT27HC64RL-55LC	28DW6 32LW	Commercial (0°C to 70°C)
55	45	0.2	AT27HC64RL-55DI AT27HC64RL-55LI	28DW6 32LW	Industrial (-40°C to 85°C)
70	35	0.1	AT27HC64RL-70DC AT27HC64RL-70LC AT27HC64RL-70PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
70	45	0.2	AT27HC64RL-70DI AT27HC64RL-70LI AT27HC64RL-70PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64RL-70DM AT27HC64RL-70LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64RL-70DM/883 AT27HC64RL-70LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	35	0.1	AT27HC64RL-90DC AT27HC64RL-90LC AT27HC64RL-90PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
90	45	0.2	AT27HC64RL-90DI AT27HC64RL-90LI AT27HC64RL-90PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64RL-90DM AT27HC64RL-90LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64RL-90DM/883 AT27HC64RL-90LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DW6	24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

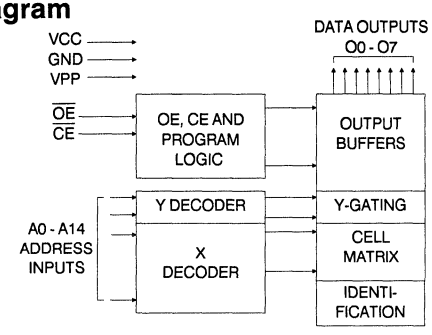
Features

- **Bipolar Speed in JEDEC Standard EPROM Pinout**
  - **Read Access Time - 55ns**
  - **28-Lead 600 mil CERDIP and OTP Plastic DIP**
  - **32-Pad LCC**
  - **32-Lead JLCC and OTP PLCC**
- **Low Power CMOS Operation**
  - **100 μA max. Standby**
  - **75 mA max. Active at 10 MHz**
- **High Output Drive Capability**
- **High Reliablity Latch-Up Resistant CMOS Technology**
- **Fast Programming - 4ms/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Commercial and Industrial Temperature Ranges**

256K (32K x 8) High Speed UV Erasable CMOS EPROM

4

Block Diagram



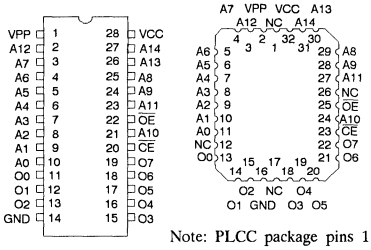
Description

The AT27HC256/256L chip family is a high speed, low-power 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 32K x 8. The AT27HC256 is suited for very high speed applications, while the AT27HC256L features low Vcc Standby Current. Both require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 55ns on the AT27HC256, making this part compatible with high performance systems. Power consumption is typically only 50mA in Active Mode on both parts and less than 10μA in Standby on the AT27HC256L.

Atmel's 1.5-micron, high speed CMOS technology provides optimum speed, low-power and high noise immunity. The high speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect
O0-O7	Outputs



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27HC256/256L come in a choice of industry standard JEDEC-approved packages including: 28-pin DIP ceramic or one time programmable (OTP) plastic, 32-pad ceramic leadless chip carrier (LCC), and 32-lead ceramic (JLCC), or OTP plastic (PLCC) J-leaded chip carrier. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With a storage capacity of 32K bytes, Atmel's 27HC256 / 256L allow firmware to be stored reliably and to be accessed at very high speeds. The AT27HC256/256L have exceptional output drive capability - source 4mA and sink 16mA per output.

The AT27HC256/256L have additional features to ensure high quality and efficient production use. The fast programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27HC256/256L is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15 W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 $w \cdot sec/cm^2$

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A14 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC256	AT27HC256 / AT27HC256L		
		-55	-70	-90	-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C(1)	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Notes: 1. AT27HC256 only.

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{PP} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC} + 0.3V			20	µA
I_{SB1}/I_{SB2}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V	AT27HC256L Com.		0.1/2	mA
			Ind.,Mil.		0.2/3	mA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V	AT27HC256 Com.		40/40	mA
			Ind.,Mil.		45/45	mA
I_{CC}	V_{CC} Active Current	f = 10MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		75	mA
			Ind.,Mil.		90	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 16mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -4.0mA		2.4		V
V_{PP}	V_{PP} Read Voltage	V_{CC} = 5 ± 0.5V		3.8	V_{CC} + 0.3	V

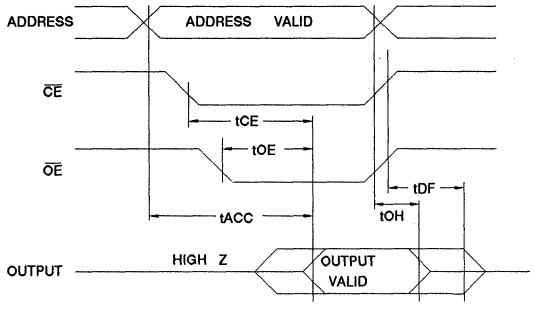
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27HC256		AT27HC256 / AT27HC256L						
				-55		-70		-90		-12		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.,Ind.		55		70		90		120	ns
			Mil.				70(1)		90		120	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			55		70		90		120	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			25		30		30		35	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}			25		30		30		35	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			0		0		0		0	ns

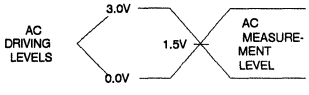
Notes: 1. AT27HC256 only.
2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



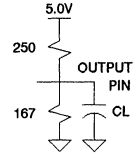
Notes:
1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.
   C_L = 30pF, add 10ns for C_L = 100pF.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. t_{DF} is measured at V_{OH}-0.5V or V_{OL}+0.5V with C_L=5pF.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns (10% to 90%)

Output Test Load



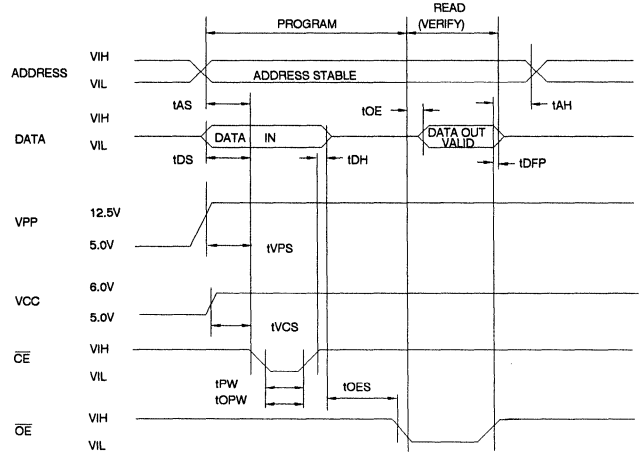
Note: C_L=30pF including jig capacitance.

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.0V for V_{IL} and 3.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27HC256/256L a 0.1μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, V_{PP}=12.5±0.5V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=16mA$		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-4.0mA$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			80	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, V_{PP}=12.5±0.5V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	(Note 3)	0.95	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(Note 4)	2.85	78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 5ns
Input Pulse Levels ..... 0.0V to 3.0V
Input Timing Reference Level 1.5V
Output Timing Reference Level 1.5V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Initial Program Pulse width tolerance is 1msec±5%.
4. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

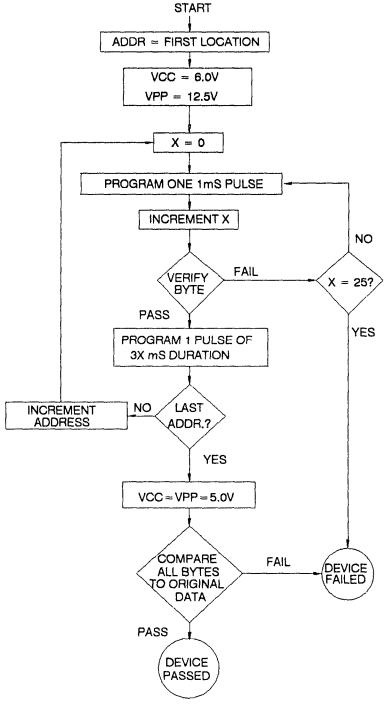
Atmel's 27HC256/L Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	1	1F
Device Type	1	1	0	0	1	0	1	0	0	94

Fast Programming Algorithm

Two $\overline{CE}$ pulse widths are used to program; initial and overprogram. Ai are set to address the desired byte. V_{CC} is raised to 6.0V. The first $\overline{CE}$ pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{CE}$ pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then V_{CC} is lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	75	40	AT27HC256-55DC AT27HC256-55KC AT27HC256-55LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
55	90	45	AT27HC256-55DI AT27HC256-55KI AT27HC256-55LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
70	75	40	AT27HC256-70DC AT27HC256-70JC AT27HC256-70KC AT27HC256-70LC AT27HC256-70PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
70	90	45	AT27HC256-70DI AT27HC256-70JI AT27HC256-70KI AT27HC256-70LI AT27HC256-70PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256-70DM AT27HC256-70KM AT27HC256-70LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256-70DM/883 AT27HC256-70KM/883 AT27HC256-70LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	75	40	AT27HC256-90DC AT27HC256-90JC AT27HC256-90KC AT27HC256-90LC AT27HC256-90PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
90	90	45	AT27HC256-90DI AT27HC256-90JI AT27HC256-90KI AT27HC256-90LI AT27HC256-90PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256-90DM AT27HC256-90KM AT27HC256-90LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256-90DM/883 AT27HC256-90KM/883 AT27HC256-90LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	75	40	AT27HC256-12DC AT27HC256-12JC AT27HC256-12KC AT27HC256-12LC AT27HC256-12PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	90	45	AT27HC256-12DI AT27HC256-12JI AT27HC256-12KI AT27HC256-12LI AT27HC256-12PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256-12DM AT27HC256-12KM AT27HC256-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256-12DM/883 AT27HC256-12KM/883 AT27HC256-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	90	45	5962-86063 08 XX 5962-86063 08 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	75	0.1	AT27HC256L-70DC AT27HC256L-70KC AT27HC256L-70LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
70	90	0.2	AT27HC256L-70DI AT27HC256L-70KI AT27HC256L-70LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
90	75	0.1	AT27HC256L-90DC AT27HC256L-90JC AT27HC256L-90KC AT27HC256L-90LC AT27HC256L-90PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
90	90	0.2	AT27HC256L-90DI AT27HC256L-90JI AT27HC256L-90KI AT27HC256L-90LI AT27HC256L-90PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256L-90DM AT27HC256L-90KM AT27HC256L-90LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256L-90DM/883 AT27HC256L-90KM/883 AT27HC256L-90LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	75	0.1	AT27HC256L-12DC AT27HC256L-12JC AT27HC256L-12KC AT27HC256L-12LC AT27HC256L-12PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
120	90	0.2	AT27HC256L-12DI AT27HC256L-12JI AT27HC256L-12KI AT27HC256L-12LI AT27HC256L-12PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256L-12DM AT27HC256L-12KM AT27HC256L-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256L-12DM/883 AT27HC256L-12KM/883 AT27HC256L-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	90	0.2	5962-86063 07 XX 5962-86063 07 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	90	0.2	5962-86063 06 XX 5962-86063 06 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

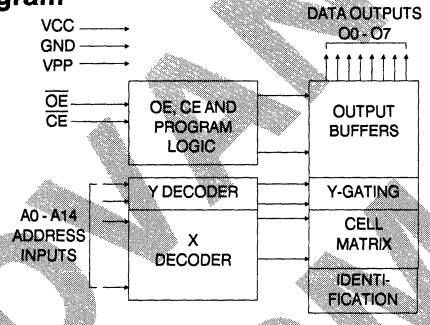
Ordering Information

	Package Type
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

- **Bipolar Speed in JEDEC Standard EPROM Pinout**
  - **Read Access Time - 55ns**
  - **28-Lead 600 mil CERDIP and OTP Plastic DIP**
  - **32-Pad LCC, JLCC and OTP PLCC**
- **Low Power CMOS Operation**
  - **100 μA max. Standby**
  - **35 mA max. Active at 10 MHz**
- **High Output Drive Capability**
- **High Reliablity Latch-Up Resistant CMOS Technology**
- **Rapid Programming - 100μs/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Industrial and Commercial Temperature Ranges**
- **Fully Compatible with AT27HC256/L**

Block Diagram



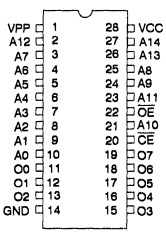
Description

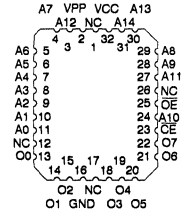
The AT27HC256R/RL chip family is a high-speed, low-power 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 32K x 8 bits. The AT27HC256R is suited for very high-speed applications, while the AT27HC256RL features low Vcc Standby Current. Both require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 55ns on the AT27HC256, making this part ideal for high-performance systems. Power consumption is typically only 25mA in Active Mode on both parts, and less than 10μA in Standby Mode on the AT27HC256RL.

Atmel's 1.2-micron, high-speed CMOS technology provides optimum speed, lower power and high noise immunity. The high-speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect
O0-O7	Outputs





Note: PLCC package pins 1 and 17 are DON'T CONNECT.

256K (32K x 8) High Speed UV Erasable CMOS EPROM

Advance Information

4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	35	20	AT27HC256R-55DC AT27HC256R-55KC AT27HC256R-55LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
55	45	30	AT27HC256R-55DI AT27HC256R-55KI AT27HC256R-55LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
70	35	20	AT27HC256R-70DC AT27HC256R-70JC AT27HC256R-70KC AT27HC256R-70LC AT27HC256R-70PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
70	45	30	AT27HC256R-70DI AT27HC256R-70JI AT27HC256R-70KI AT27HC256R-70LI AT27HC256R-70PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256R-70DM AT27HC256R-70KM AT27HC256R-70LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256R-70DM/883 AT27HC256R-70KM/883 AT27HC256R-70LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	35	20	AT27HC256R-90DC AT27HC256R-90JC AT27HC256R-90KC AT27HC256R-90LC AT27HC256R-90PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
90	45	30	AT27HC256R-90DI AT27HC256R-90JI AT27HC256R-90KI AT27HC256R-90LI AT27HC256R-90PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256R-90DM AT27HC256R-90KM AT27HC256R-90LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256R-90DM/883 AT27HC256R-90KM/883 AT27HC256R-90LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	35	20	AT27HC256R-12DC AT27HC256R-12JC AT27HC256R-12KC AT27HC256R-12LC AT27HC256R-12PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	45	30	AT27HC256R-12DI AT27HC256R-12JI AT27HC256R-12KI AT27HC256R-12LI AT27HC256R-12PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256R-12DM AT27HC256R-12KM AT27HC256R-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256R-12DM/883 AT27HC256R-12KM/883 AT27HC256R-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Ordering Information

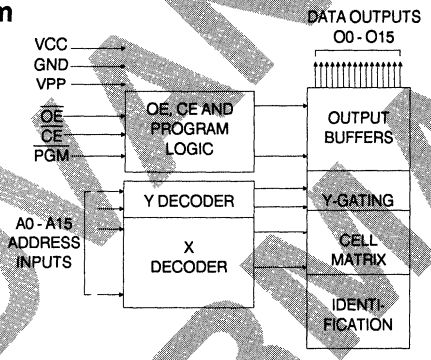
t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	35	0.1	AT27HC256RL-70DC AT27HC256RL-70KC AT27HC256RL-70LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
70	45	0.2	AT27HC256RL-70DI AT27HC256RL-70KI AT27HC256RL-70LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
90	35	0.1	AT27HC256RL-90DC AT27HC256RL-90JC AT27HC256RL-90KC AT27HC256RL-90LC AT27HC256RL-90PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
90	45	0.2	AT27HC256RL-90DI AT27HC256RL-90JI AT27HC256RL-90KI AT27HC256RL-90LI AT27HC256RL-90PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256RL-90DM AT27HC256RL-90KM AT27HC256RL-90LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256RL-90DM/883 AT27HC256RL-90KM/883 AT27HC256RL-90LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	35	0.1	AT27HC256RL-12DC AT27HC256RL-12JC AT27HC256RL-12KC AT27HC256RL-12LC AT27HC256RL-12PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
120	45	0.2	AT27HC256RL-12DI AT27HC256RL-12JI AT27HC256RL-12KI AT27HC256RL-12LI AT27HC256RL-12PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256RL-12DM AT27HC256RL-12KM AT27HC256RL-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256RL-12DM/883 AT27HC256RL-12KM/883 AT27HC256RL-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

- **Very Fast Read Access Time - 55ns**
- **Low Power CMOS Operation**
  - **500 μA max. Standby**
  - **60 mA max. Active at 10 MHz**
- **Wide Selection of JEDEC Standard Packages Including OTP**
  - **40-Lead 600 mil Cerdip and OTP Plastic**
  - **44-Pad LCC and OTP PLCC**
- **High Output Drive Capability**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200mA Latchup Immunity**
- **Rapid Programming - 100μs/word (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Industrial and Commercial Temperature Ranges**

Block Diagram



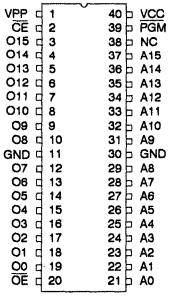
The AT27HC1024 chip is a high-speed, low-power 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 64K x 16 bits. It requires only one 5V power supply in normal read mode operation. Any word can be accessed in less than 55ns, eliminating the need for speed reducing WAIT states. The by-16 organization makes these parts ideal for high-performance 16 and 32 bit microprocessor and digital signal processor systems.

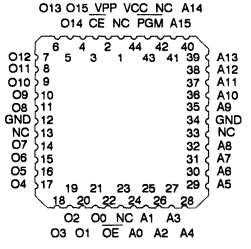
In read mode, the AT27HC1024 typically consumes 40mA while in standby mode supply current is typically less than 100μA.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.





Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

1 MEGABIT (64K x 16) High Speed UV Erasable CMOS EPROM

Advance Information

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	60	0.5	AT27HC1024-55DC AT27HC1024-55LC	40DW6 44LW	Commercial (0°C to 70°C)
70	60	0.5	AT27HC1024-70DC AT27HC1024-70LC AT27HC1024-70PC AT27HC1024-70JC	40DW6 44LW 40P6 44J	Commercial (0°C to 70°C)
70	75	1.0	AT27HC1024-70DI AT27HC1024-70LI AT27HC1024-70PI AT27HC1024-70JI	40DW6 44LW 40P6 44J	Industrial (-40°C to 85°C)
			AT27HC1024-70DM AT27HC1024-70LM	40DW6 44LW	Military (-55°C to 125°C)
			AT27HC1024-70DM/883 AT27HC1024-70LM/883	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	60	0.5	AT27HC1024-90DC AT27HC1024-90LC AT27HC1024-90PC AT27HC1024-90JC	40DW6 44LW 40P6 44J	Commercial (0°C to 70°C)
90	75	1.0	AT27HC1024-90DI AT27HC1024-90LI AT27HC1024-90PI AT27HC1024-90JI	40DW6 44LW 40P6 44J	Industrial (-40°C to 85°C)
			AT27HC1024-90DM AT27HC1024-90LM	40DW6 44LW	Military (-55°C to 125°C)
			AT27HC1024-90DM/883 AT27HC1024-90LM/883	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	60	0.5	AT27HC1024-12DC AT27HC1024-12LC AT27HC1024-12PC AT27HC1024-12JC	40DW6 44LW 40P6 44J	Commercial (0°C to 70°C)
120	75	1.0	AT27HC1024-12DI AT27HC1024-12LI AT27HC1024-12PI AT27HC1024-12JI	40DW6 44LW 40P6 44J	Industrial (-40°C to 85°C)
			AT27HC1024-12DM AT27HC1024-12LM	40DW6 44LW	Military (-55°C to 125°C)
			AT27HC1024-12DM/883 AT27HC1024-12LM/883	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

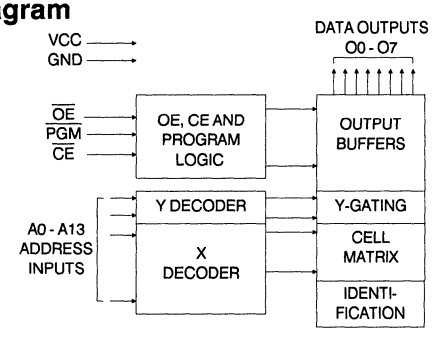
	Package Type
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

128K (16K x 8) UV Erasable CMOS EPROM

Features

- Low Power CMOS Operation
  - 100 μA max. Standby
  - 30 mA max. Active at 5 MHz
- Fast Read Access Time - 120ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP
  - 32-Pad OTP PLCC
- 5V± 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
- Fast Programming - 4ms/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Block Diagram



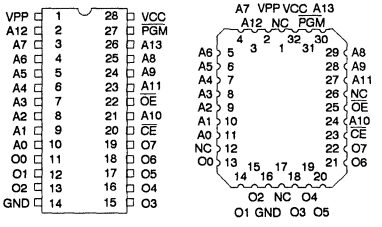
Description

The AT27C128 chip is a low-power, high performance 131,072 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 16K x 8. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

Atmel's 1.5 micron CMOS technology provides optimum speed, low power and high noise immunity. Power consumption is typically only 10mA in Active Mode and less than 10μA in Standby. In addition to the speed, power and reliability advantages of the CMOS process, the CMOS technology is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

Pin Configurations

Pin Name	Function
A0-A13	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect



Note: PLCC package Pins 1 and 17 are DON'T CONNECT

Description (Continued)

The AT27C128 comes in a choice of industry standard JEDEC-approved packages including; 32-pin DIP in ceramic or one time programmable (OTP) plastic, and 32-pin OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 16K byte storage capability, the AT27C128 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C128 has additional features to ensure high quality and efficient production use. The Fast Programming Algorithm reduces the time required to program the part and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C128 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15W \bullet sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 $w \bullet sec/cm^2$

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	Ai	X(1)	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A13 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming Characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code Byte.
5. Standby V_{CC} current (I_{SB}) is specified with $V_{PP}=V_{CC}$. $V_{CC} > V_{PP}$ will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C128			
		-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC} + 0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind.,Mil.		40	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -400µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

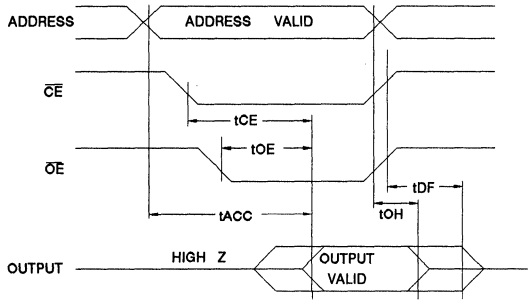
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C128								
				-12		-15		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		120		150		200		250	ns
			Ind.		120		150		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			120		150		200		250	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			60		70		75		100	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}			50		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			0		0		0		0	ns

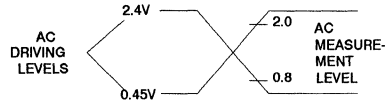
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



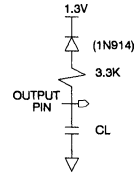
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



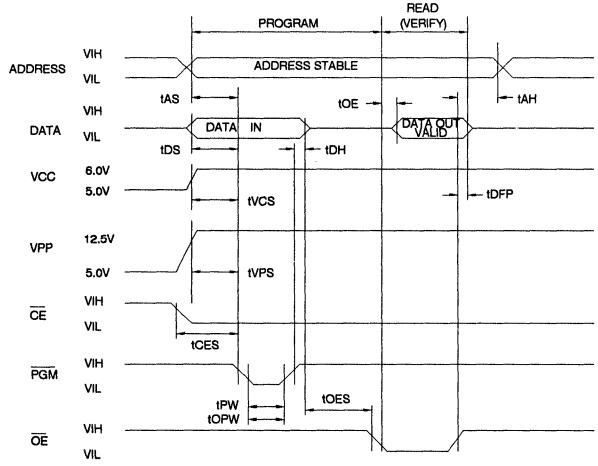
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C128 a 0.1μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, V_{PP}=12.5±0.5V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1mA$		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400\mu A$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			30	mA
I_{PP2}	V_{PP} Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, V_{PP}=12.5±0.5V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(Note 3)	0.95	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(Note 4)	2.85	78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Initial Program Pulse width tolerance is 1msec±5%.
4. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

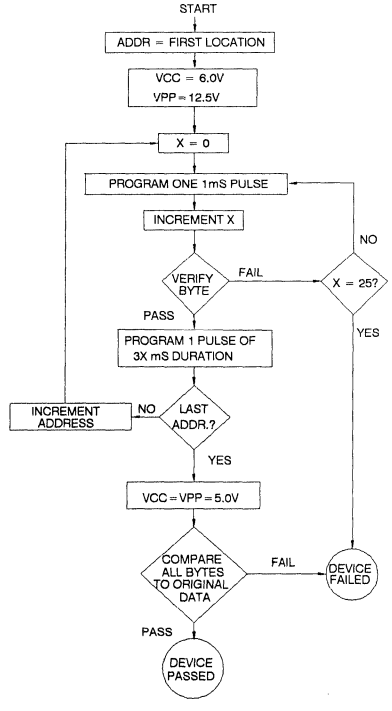
Atmel's 27C128 Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	1	1F
Device Type	1	1	0	0	0	0	0	1	1	83

Fast Programming Algorithm

Two $\overline{PGM}$ pulse widths are used to program; initial and overprogram. Ai are set to address the desired byte. V_{CC} is raised to 6.0V. The first $\overline{PGM}$ pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{PGM}$ pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then V_{CC} is lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	30	0.1	AT27C128-12DC	28DW6	Commercial (0°C to 70°C)
120	40	0.2	AT27C128-12DI	28DW6	Industrial (-40°C to 85°C)
150	30	0.1	AT27C128-15DC AT27C128-15PC AT27C128-15JC	28DW6 28P6 32J	Commercial (0°C to 70°C)
150	40	0.2	AT27C128-15DI AT27C128-15PI AT27C128-15JI	28DW6 28P6 32J	Industrial (-40°C to 85°C)
200	30	0.1	AT27C128-20DC AT27C128-20PC AT27C128-20JC	28DW6 28P6 32J	Commercial (0°C to 70°C)
200	40	0.2	AT27C128-20DI AT27C128-20PI AT27C128-20JI	28DW6 28P6 32J	Industrial (-40°C to 85°C)
250	30	0.1	AT27C128-25DC AT27C128-25PC AT27C128-25JC	28DW6 28P6 32J	Commercial (0°C to 70°C)
250	40	0.2	AT27C128-25DI AT27C128-25PI AT27C128-25JI	28DW6 28P6 32J	Industrial (-40°C to 85°C)

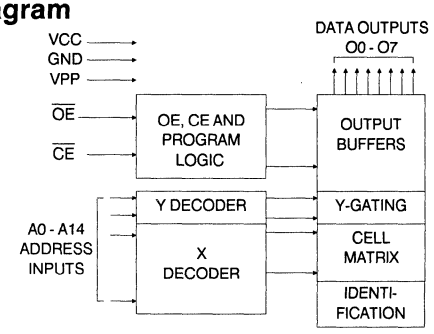
Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

256K (32K x 8) UV Erasable CMOS EPROM

Features

- **Low Power CMOS Operation**
  - **100 μA max. Standby**
  - **30 mA max. Active at 5 MHz**
- **Fast Read Access Time - 120ns**
- **Wide Selection of JEDEC Standard Packages Including OTP**
  - **28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC**
  - **32-Pad LCC and OTP PLCC**
- **5V± 10% Supply**
- **High Reliability Latch-Up Resistant CMOS Technology**
  - **2000V ESD Protection**
- **Fast Programming - 4ms/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Commercial and Industrial Temperature Ranges**

Block Diagram



Description

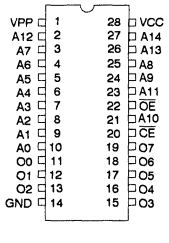
The AT27C256 is a low-power, high performance 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 32K x 8. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, making this part compatible with high performance microprocessor systems by eliminating the need for speed-reducing WAIT states.

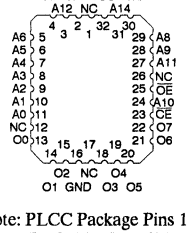
Atmel's 1.5-micron CMOS technology provides optimum speed, low-power and high noise immunity. Power consumption is typically only 10mA in Active Mode and less than 1μA in Standby. Atmel's CMOS EPROM process uses industry-proven floating poly EPROM technology to provide high quality and manufacturability.

The AT27C256 comes in a choice of industry standard JEDEC-approved packages including; 28-pin DIP in ceramic or one time programmable (OTP) plastic, 28-pin OTP plastic small outline (SOIC), and 32-pad ceramic leadless chip carrier (LCC) or OTP plastic J-leaded chip carrier (PLCC). The device features two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect
O0-O7	Outputs





Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

With a high density 32K byte storage capability, Atmel's 27C256 allows firmware to be stored reliably and to be quickly accessed by the system without the delays of mass storage media.

The AT27C256 has additional features to ensure high quality and efficient production use. The fast programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C256 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15 W \bullet sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 $w \bullet sec/cm^2$

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A14 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C256				
		-12	-15	-17	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC} + 0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind.,Mil.		40	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -400µA		2.4		V
V_{PP}	V_{PP} Read Voltage	V_{CC} = 5 ± 0.5V		3.8	V_{CC} + .3	V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

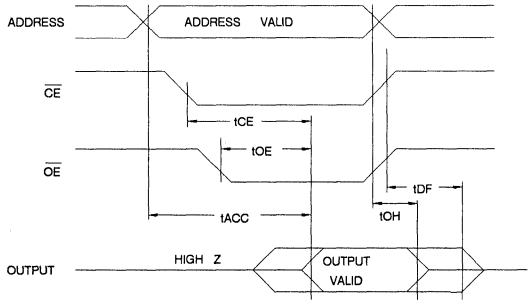
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C256										
				-12		-15		-17		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.,Ind.		120		150		170		200		250	ns
			Mil.				150		170		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			120		150		170		200		250	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			60		70		70		75		100	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}			45		50		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			0		0		0		0		0	ns

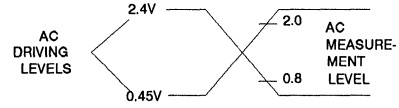
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



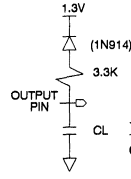
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



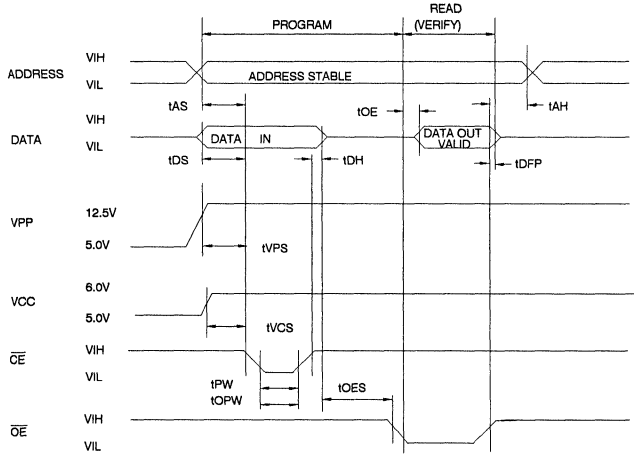
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C256 a 0.1μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, V_{PP}=12.5±0.5V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	VCC Supply Current (Program and Verify)			30	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, V_{PP}=12.5±0.5V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	(Note 3)	0.95	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(Note 4)	2.85	78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Initial Program Pulse width tolerance is 1msec±5%.
4. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

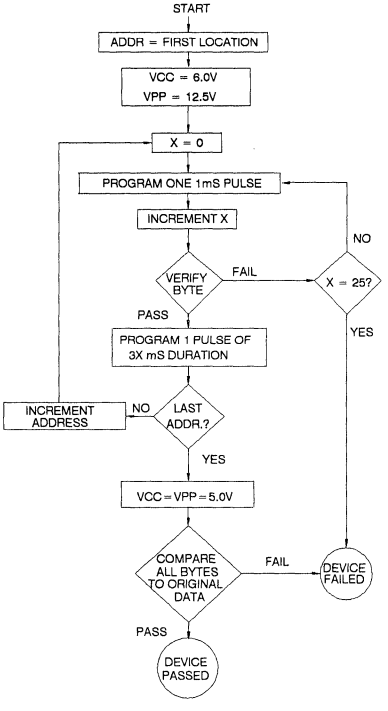
Atmel's 27C256 Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	1	0	1	0	0	1	29
Device Type	1	1	0	0	0	1	1	0	0	8C

Fast Programming Algorithm

Two $\overline{CE}$ pulse widths are used to program; initial and overprogram. Ai are set to address the desired byte. V_{CC} is raised to 6.0V. The first $\overline{CE}$ pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{CE}$ pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then V_{CC} is lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	30	0.1	AT27C256-12DC AT27C256-12LC	28DW6 32LW	Commercial (0°C to 70°C)
120	40	0.2	AT27C256-12DI AT27C256-12LI	28DW6 32LW	Industrial (-40°C to 85°C)
150	30	0.1	AT27C256-15DC AT27C256-15LC AT27C256-15PC AT27C256-15JC AT27C256-15RC	28DW6 32LW 28P6 32J 28R	Commercial (0°C to 70°C)
150	40	0.2	AT27C256-15DI AT27C256-15LI AT27C256-15PI AT27C256-15JI AT27C256-15RI	28DW6 32LW 28P6 32J 28R	Industrial (-40°C to 85°C)
			AT27C256-15DM AT27C256-15LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C256-15DM/883 AT27C256-15LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	30	0.1	AT27C256-17DC AT27C256-17LC AT27C256-17PC AT27C256-17JC AT27C256-17RC	28DW6 32LW 28P6 32J 28R	Commercial (0°C to 70°C)
170	40	0.2	AT27C256-17DI AT27C256-17LI AT27C256-17PI AT27C256-17JI AT27C256-17RI	28DW6 32LW 28P6 32J 28R	Industrial (-40°C to 85°C)
			AT27C256-17DM AT27C256-17LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C256-17DM/883 AT27C256-17LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT27C256-20DC AT27C256-20LC AT27C256-20PC AT27C256-20JC AT27C256-20RC	28DW6 32LW 28P6 32J 28R	Commercial (0°C to 70°C)
200	40	0.2	AT27C256-20DI AT27C256-20LI AT27C256-20PI AT27C256-20JI AT27C256-20RI	28DW6 32LW 28P6 32J 28R	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	40	0.2	AT27C256-20DM AT27C256-20LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C256-20DM/883 AT27C256-20LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT27C256-25DC AT27C256-25LC AT27C256-25PC AT27C256-25JC AT27C256-25RC	28DW6 32LW 28P6 32J 28R	Commercial (0°C to 70°C)
250	40	0.2	AT27C256-25DI AT27C256-25LI AT27C256-25PI AT27C256-25JI AT27C256-25RI	28DW6 32LW 28P6 32J 28R	Industrial (-40°C to 85°C)
			AT27C256-25DM AT27C256-25LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C256-25DM/883 AT27C256-25LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	40	0.2	AT27C256-30DM/883 AT27C256-30LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	40	0.2	AT27C256-35DM/883 AT27C256-35LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

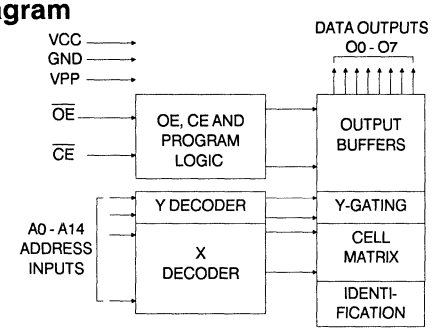
Features

- Low Power CMOS Operation
  - 100 μA max. Standby
  - 20 mA max. Active at 5 MHz
- Fast Read Access Time - 90ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC
  - 32-Lead JLCC and OTP PLCC
- 5V± 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100μs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges
- Fully Compatible with AT27C256

256K (32K x 8) UV Erasable CMOS EPROM

4

Block Diagram



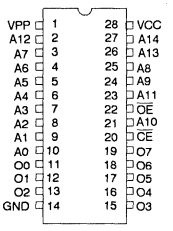
Description

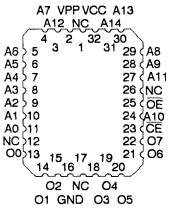
The AT27C256R chip is a low-power, high performance 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 32K x 8. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 90ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

The AT27C256R meets or exceeds all specifications for the AT27C256. Atmel's 1.2 micron scaled CMOS technology additionally provides lower active power consumption, and significantly faster programming. Power consumption is typically only 8mA in Active Mode and less than 10μA in Standby.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect





Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27C256R comes in a choice of industry standard JEDEC-approved packages including; 28-pin DIP ceramic or one time programmable (OTP) plastic, 28-pin OTP plastic small outline (SOIC), 32-pad ceramic leadless chip carrier (LCC), and 32 lead ceramic (JLCC),or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 32K byte storage capability, the AT27C256R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C256R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100μs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C256R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000μW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 w•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A14 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C256R				
		-90	-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC} + 0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		20	mA
			Ind.,Mil.		25	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -400µA		2.4		V
V_{PP}	V_{PP} Read Voltage	V_{CC} = 5 ± 0.25V		3.8	V_{CC} + .3	V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

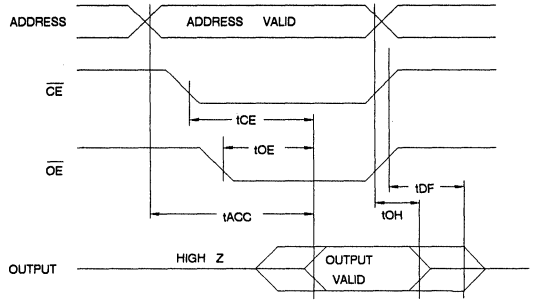
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C256R										
				-90		-12		-15		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		90		120		150		200		250	ns
			Ind.,Mil.		90		120		150		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			90		120		150		200		250	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			40		50		60		75		100	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}			30		30		45		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			0		0		0		0		0	ns

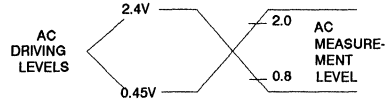
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



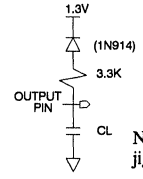
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



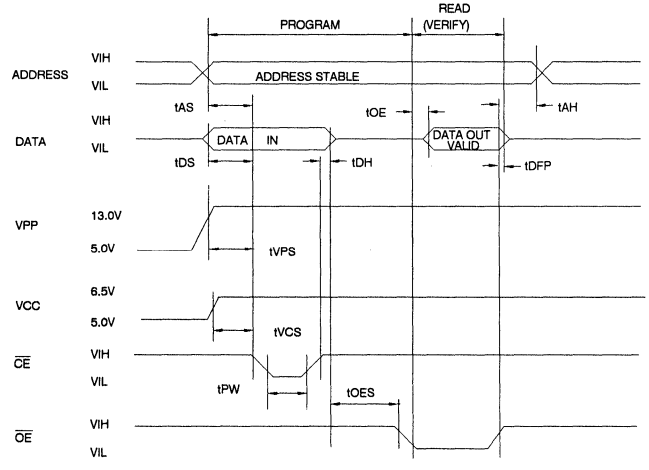
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C256R a 0.1μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1mA$		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400\mu A$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	(Note 2)		150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V

Notes:

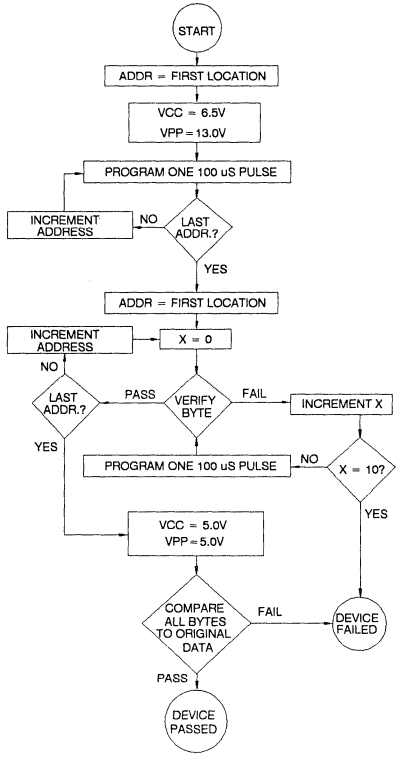
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27C256R Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Rapid Programming Algorithm

A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	20	0.1	AT27C256R-90DC AT27C256R-90KC AT27C256R-90LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
90	25	0.2	AT27C256R-90DI AT27C256R-90KI AT27C256R-90LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
120	20	0.1	AT27C256R-12DC AT27C256R-12JC AT27C256R-12KC AT27C256R-12LC AT27C256R-12PC AT27C256R-12RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
120	25	0.2	AT27C256R-12DI AT27C256R-12JI AT27C256R-12KI AT27C256R-12LI AT27C256R-12PI AT27C256R-12RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-12DM AT27C256R-12KM AT27C256R-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-12DM/883 AT27C256R-12KM/883 AT27C256R-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	20	0.1	AT27C256R-15DC AT27C256R-15JC AT27C256R-15KC AT27C256R-15LC AT27C256R-15PC AT27C256R-15RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
150	25	0.2	AT27C256R-15DI AT27C256R-15JI AT27C256R-15KI AT27C256R-15LI AT27C256R-15PI AT27C256R-15RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-15DM AT27C256R-15KM AT27C256R-15LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-15DM/883 AT27C256R-15KM/883 AT27C256R-15LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
170	20	0.1	AT27C256R-17DC AT27C256R-17JC AT27C256R-17KC AT27C256R-17LC AT27C256R-17PC AT27C256R-17RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
170	25	0.2	AT27C256R-17DI AT27C256R-17JI AT27C256R-17KI AT27C256R-17LI AT27C256R-17PI AT27C256R-17RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-17DM AT27C256R-17KM AT27C256R-17LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-17DM/883 AT27C256R-17KM/883 AT27C256R-17LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	20	0.1	AT27C256R-20DC AT27C256R-20JC AT27C256R-20KC AT27C256R-20LC AT27C256R-20PC AT27C256R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
200	25	0.2	AT27C256R-20DI AT27C256R-20JI AT27C256R-20KI AT27C256R-20LI AT27C256R-20PI AT27C256R-20RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-20DM AT27C256R-20KM AT27C256R-20LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-20DM/883 AT27C256R-20KM/883 AT27C256R-20LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	20	0.1	AT27C256R-25DC AT27C256R-25JC AT27C256R-25KC AT27C256R-25LC AT27C256R-25PC AT27C256R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	25	0.2	AT27C256R-25DI AT27C256R-25JI AT27C256R-25KI AT27C256R-25LI AT27C256R-25PI AT27C256R-25RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-25DM AT27C256R-25KM AT27C256R-25LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
250	25	0.2	AT27C256R-25DM/883 AT27C256R-25KM/883 AT27C256R-25LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	25	0.2	5962-86063 05 XX 5962-86063 05 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	25	0.2	5962-86063 04 XX 5962-86063 04 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	25	0.2	5962-86063 01 XX 5962-86063 01 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.2	5962-86063 02 XX 5962-86063 02 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	25	0.2	5962-86063 03 XX 5962-86063 03 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

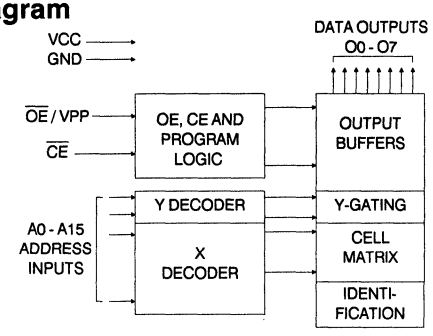
Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP, (SOIC)

512K (64K x 8) UV Erasable CMOS EPROM

Features

- **Low Power CMOS Operation**
  - **100 μA max. Standby**
  - **40 mA max. Active at 5 MHz**
- **Fast Read Access Time - 120ns**
- **Wide Selection of JEDEC Standard Packages Including OTP**
  - **28 -Lead 600 mil Cerdip and OTP Plastic DIP**
  - **32-Pad LCC and OTP PLCC**
- **5V± 10% Supply**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200mA Latchup Immunity**
- **Fast Programming - 4ms/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Commercial and Industrial Temperature Ranges**

Block Diagram



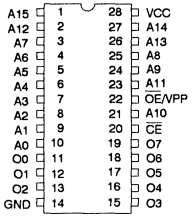
Description

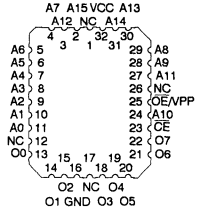
The AT27C512 chip is a low-power, high performance 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 8. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

Atmel's 1.5 micron CMOS technology provides optimum speed, low power and high noise immunity. Power consumption is typically only 15mA in Active Mode and less than 10μA in Standby. In addition to the speed, power and reliability advantages of the CMOS process, the CMOS technology is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$ /V_{PP}	Output Enable
NC	No Connect





Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27C512 comes in a choice of industry standard JEDEC-approved packages including; 28-pin DIP in ceramic or one time programmable (OTP) plastic, and 32-pad ceramic leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K byte storage capability, the AT27C512 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C512 has additional features to ensure high quality and efficient production use. The Fast Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 4ms/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C512 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15 W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 w•sec/cm²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{PP}	Ai	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A15 = V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C512			
		-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		40	mA
			Ind.,Mil.		50	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -400µA		2.4		V

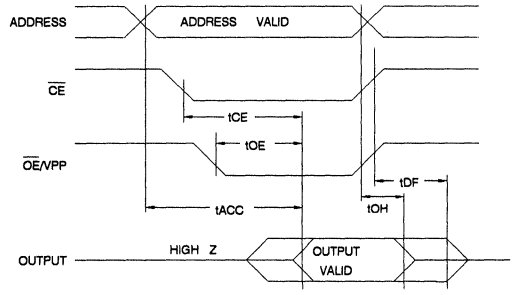
Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

A.C. Characteristics for Read Operation

				AT27C512								
				-12		-15		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = VIL	Com.		120		150		200		250	ns
			Ind., Mil.				150		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$ = V_{IL}			120		150		200		250	ns
t_{OE} (3,4)	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$ = V_{IL}			65		70		75		100	ns
t_{DF} (2,5)	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}			50		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}			0		0		0		0	ns

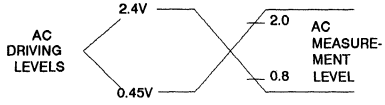
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



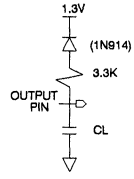
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ /V_{PP} or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$/V_{PP} may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ /V_{PP} may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



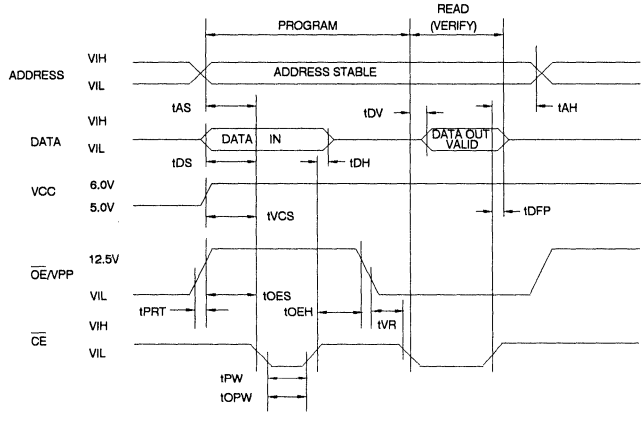
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, $\overline{OE}/V_{PP}$=12.5±0.5V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1$mA		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400$µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, $\overline{OE}/V_{PP}$=12.5±0.5V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	(Note 3)	0.95	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(Note 4)	2.85	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	(Note 2)		1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V

Notes:

1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Initial Program Pulse width tolerance is 1msec±5%.
4. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

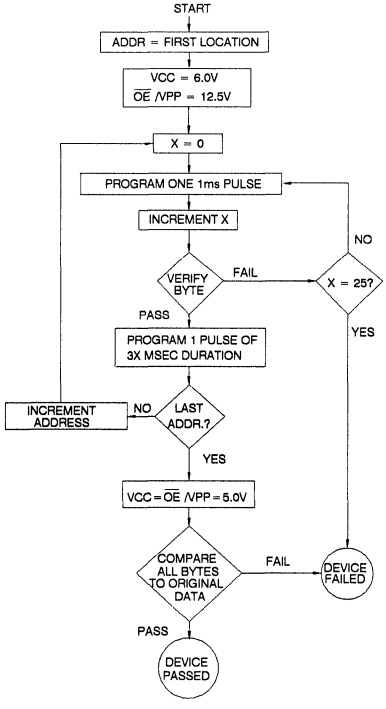
Atmel's 27C512 Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	1	1F
Device Type	1	0	0	0	0	1	1	0	1	0D

Fast Programming Algorithm

Two $\overline{CE}$ pulse widths are used to program; initial and overprogram. Ai are set to address the desired byte. V_{CC} is raised to 6.0V. The first $\overline{CE}$ pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{CE}$ pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then V_{CC} is lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	40	0.1	AT27C512-12DC AT27C512-12LC	28DW6 32LW	Commercial (0°C to 70°C)
150	40	0.1	AT27C512-15DC AT27C512-15LC AT27C512-15PC AT27C512-15JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
150	50	0.2	AT27C512-15DI AT27C512-15LI AT27C512-15PI AT27C512-15JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C512-15DM AT27C512-15LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C512-15DM/883 AT27C512-15LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	50	0.2	AT27C512-17DM/883 AT27C512-17LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	40	0.1	AT27C512-20DC AT27C512-20LC AT27C512-20PC AT27C512-20JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
200	50	0.2	AT27C512-20DI AT27C512-20LI AT27C512-20PI AT27C512-20JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C512-20DM AT27C512-20LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C512-20DM/883 AT27C512-20LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	40	0.1	AT27C512-25DC AT27C512-25LC AT27C512-25PC AT27C512-25JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
250	50	0.2	AT27C512-25DI AT27C512-25LI AT27C512-25PI AT27C512-25JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C512-25DM AT27C512-25LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C512-25DM/883 AT27C512-25LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

	Package Type
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

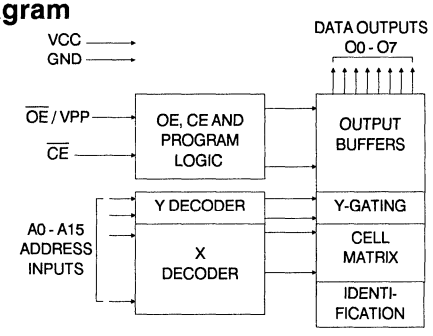
Features

- Low Power CMOS Operation
  - 100 μA max. Standby
  - 20 mA max. Active at 5 MHz
- Fast Read Access Time - 100ns
- Wide Selection of JEDEC Standard Packages including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC
  - 32-Lead JLCC and OTP PLCC
- 5V$\pm$ 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100μs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges
- Fully Compatible with AT27C512

512K (64K x 8) UV Erasable CMOS EPROM

4

Block Diagram



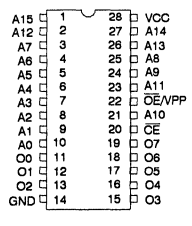
Description

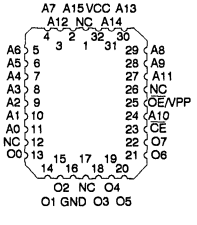
The AT27C512R chip is a low-power, high performance 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 8. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 100ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

The AT27C512R meets or exceeds all specifications for the AT27C512. Atmel's 1.2 micron scaled CMOS technology additionally provides lower active power consumption, and significantly faster programming. Power consumption is typically only 8mA in Active Mode and less than 10μA in Standby.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$ /V_{PP}	Output Enable
NC	No Connect





Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27C512R comes in a choice of industry standard JEDEC-approved packages including; 28-pin DIP ceramic or one time programmable (OTP) plastic, 28-pin OTP plastic small outline (SOIC), 32-pad ceramic leadless chip carrier (LCC), and 32-lead ceramic (JLCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K byte storage capability, the AT27C512R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C512R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100μs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C512R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000μW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{PP}	Ai	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A15 = V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C512R				
		-10	-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		20	mA
			Ind.,Mil.		25	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -400µA		2.4		V

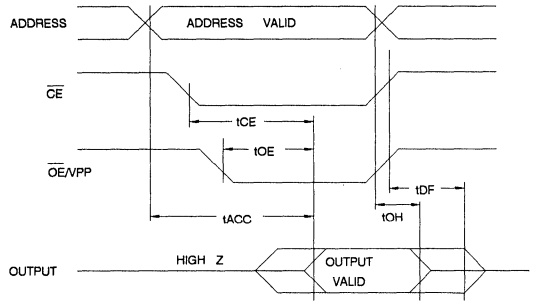
Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

A.C. Characteristics for Read Operation

				AT27C512R										
				-10		-12		-15		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$=$\overline{OE}/V_{PP}$ =VIL	Com.		100		120		150		200		250	ns
			Ind., Mil.				120		150		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$=V_{IL}			100		120		150		200		250	ns
t_{OE} (3,4)	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$=V_{IL}			40		50		60		75		100	ns
t_{DF} (2,5)	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$=V_{IL}			30		45		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first	$\overline{CE}$=$\overline{OE}/V_{PP}$ =V_{IL}			0		0		0		0		0	ns

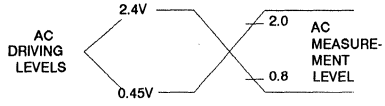
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



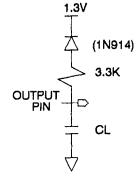
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ /V_{PP} or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$/V_{PP} may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ /V_{PP} may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



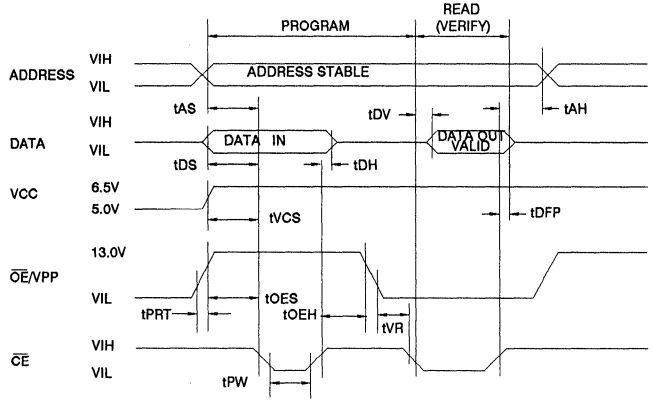
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{OE}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1mA$		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400\mu A$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{OE}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{DV}	Data Valid from $\overline{CE}$	(Note 2)		1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V

Notes:

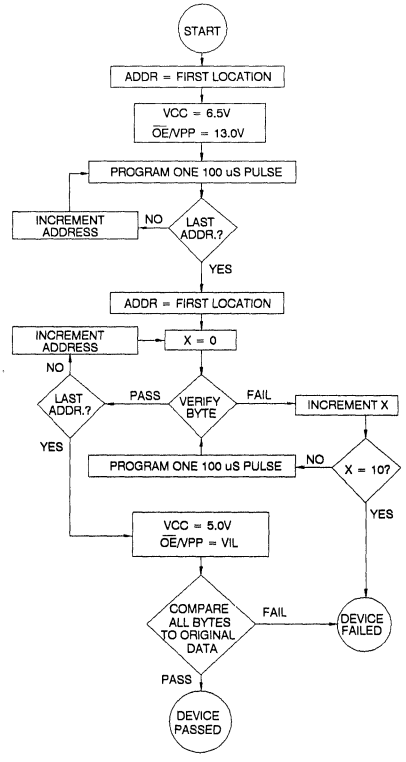
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27C512R Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

Rapid Programming Algorithm

A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	20	0.1	AT27C512R-10DC AT27C512R-10KC AT27C512R-10LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
120	20	0.1	AT27C512R-12DC AT27C512R-12KC AT27C512R-12LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
120	25	0.2	AT27C512R-12DI AT27C512R-12KI AT27C512R-12LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
			AT27C512R-12DM AT27C512R-12KM AT27C512R-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C512R-12DM/883 AT27C512R-12KM/883 AT27C512R-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	20	0.1	AT27C512R-15DC AT27C512R-15JC AT27C512R-15KC AT27C512R-15LC AT27C512R-15PC AT27C512R-15RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
150	25	0.2	AT27C512R-15DI AT27C512R-15JI AT27C512R-15KI AT27C512R-15LI AT27C512R-15PI AT27C512R-15RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C512R-15DM AT27C512R-15KM AT27C512R-15LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C512R-15DM/883 AT27C512R-15KM/883 AT27C512R-15LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	20	0.1	AT27C512R-20DC AT27C512R-20JC AT27C512R-20KC AT27C512R-20LC AT27C512R-20PC AT27C512R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	25	0.2	AT27C512R-20DI AT27C512R-20JI AT27C512R-20KI AT27C512R-20LI AT27C512R-20PI AT27C512R-20RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C512R-20DM AT27C512R-20KM AT27C512R-20LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C512R-20DM/883 AT27C512R-20KM/883 AT27C512R-20LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	20	0.1	AT27C512R-25DC AT27C512R-25JC AT27C512R-25KC AT27C512R-25LC AT27C512R-25PC AT27C512R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
250	25	0.2	AT27C512R-25DI AT27C512R-25JI AT27C512R-25KI AT27C512R-25LI AT27C512R-25PI AT27C512R-25RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C512R-25DM AT27C512R-25KM AT27C512R-25LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C512R-25DM/883 AT27C512R-25KM/883 AT27C512R-25LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	25	0.2	5962-87648 04 XX 5962-87648 04 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	25	0.2	5962-87648 01 XX 5962-87648 01 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	25	0.2	5962-87648 02 XX 5962-87648 02 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.2	5962-87648 03 XX 5962-87648 03 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

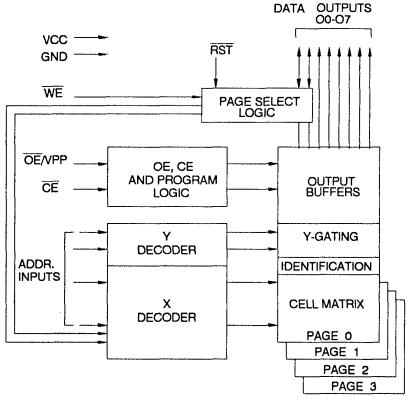
	Package Type
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic, J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

512K (4x16Kx8) UV Erasable Paged CMOS EPROM

Features

- Paged Configurations with Page Reset on Power-Up or $\overline{RST}$ Signal
- 4 Pages, 16K x 8
- Low Power CMOS Operation
  - 100 μA max. Standby
  - 20 mA max. Active at 5 MHz
- Fast Read Access Time - 120ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC and OTP PLCC
- 5V $\pm$ 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100μs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges
- Fully Compatible with 27128, 27513, 27011

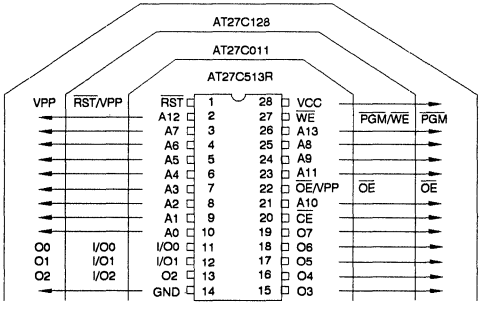
Block Diagram



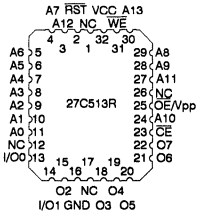
Address Pins	Number of Pages	Bits per Page
A0-A13	4	131,072

Pin Name	Function
A0-A13	Addresses
O2-O7	Outputs
I/O0-I/O1	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$/V_{PP}	Output Enable
$\overline{WE}$	Page Write Enable
$\overline{RST}$	Page Reset
NC	No Connect

Pin Configurations



Note: JEDEC standard pinouts for AT27C011 and AT27C128 are shown for comparison only.



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description

The AT27C513R is a low-power, high performance 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM). This device requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, making this part compatible with high performance microprocessor systems by eliminating the need for speed-reducing WAIT states.

The AT27C513R features page mode addressing. Atmel's 27C513R has 4 pages, each organized 16K x 8, and provides a compatible upgrade for existing 128K EPROM based designs. Increased memory capacity and improved system performance can now be easily retrofitted without using costly additional board space.

The AT27C513R has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latches are automatically reset to page 0 upon power-up (resets typically for $V_{CC} \leq 3.8V$) or when $\overline{RST}$ is brought low (V_{IL}).

The AT27C513R meets or exceeds all specifications for the AT27C513. Atmel's 1.2 micron scaled CMOS technology additionally provides lower active power consumption, and significantly faster programming. Power consumption is typically only 8mA in Active Mode and less than 10uA in Standby.

The AT27C513R is available in a choice of industry standard JEDEC-approved packages including; 28-pin DIP in ceramic or one time programmable (OTP) plastic, and 32-pad ceramic leadless chip carrier (LCC) or OTP plastic J-leaded chip carrier (PLCC). All devices feature a two line control ($\overline{CE}$,$\overline{OE}$) to give designers the flexibility to prevent bus contention.

With a high density 64K byte storage capability, the Atmel 512K EPROMs allow firmware to be stored reliably and to be quickly accessed by the system without the delays of mass storage media.

The AT27C513R has additional features to ensure high quality and efficient production use. The rapid programming algorithm reduces the time required to program the chip and guarantees reliable programming. Programming time is typically 100μs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Page Selection Data [1]

	Page D_{IN}	
Page Selection	**I/O1**	**I/O0**
Select Page 0	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IH}
Select Page 2	V_{IH}	V_{IL}
Select Page 3	V_{IH}	V_{IH}

Note: 1. The AT27C513R automatically resets to page 0 whenever $V_{CC} \leq 3.8V$ (typical conditions).

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	$\overline{WE}$	$\overline{RST}$	Ai	V_{CC} [3]	Outputs	I/Oi
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	V_{CC}	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X[1]	V_{CC}	High Z	High Z
Standby	V_{IH}	X	X	V_{IH}	X	V_{CC}	High Z	High Z
Rapid Program[2]	V_{IL}	V_{PP}	V_{IH}	V_{IH}	Ai	V_{CC}	D_{IN}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	V_{CC}	D_{OUT}	D_{OUT}
PGM Inhibit	V_{IH}	V_{PP}	V_{IH}	V_{IH}	X	V_{CC}	High Z	High Z
Page Select	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	V_{CC} [3]	High Z	Page D_{IN}
Page Reset	X	X	X	V_{IL}	X	V_{CC} [3]	High Z	High Z
Product Identification[5]	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A9=V_H [4] A0=V_{IH} or V_{IL} A1-A13=V_{IL}	V_{CC}	Identification Code	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. Page 0 is automatically selected at power up ($V_{CC} < 3.8V$).
4. $V_H = 12.0 \pm 0.5V$.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 w•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

4

D.C. and A.C. Operating Conditions for Read and Page Select Operations

		AT27C513R			
		-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read and Page Select Operations

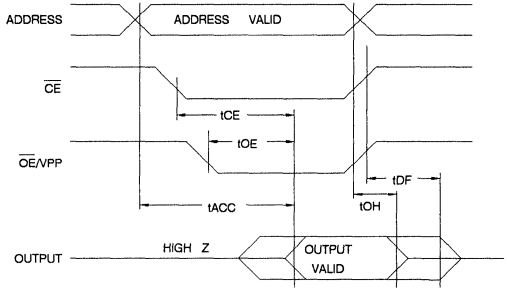
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		20	mA
			Ind.,Mil.		25	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -400µA		2.4		V
V_{CLR}	Page Latch Clear V_{CC} Supply Voltage				4.0	V

Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

A.C. Characteristics for Read Operation

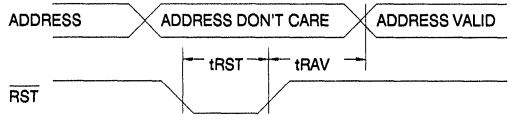
Symbol	Parameter	Condition		AT27C513R -12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}=\overline{OE}/V_{PP}=V_{IL}$	Com., Ind.		120		150		200		250	ns
			Mil.				150		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}=V_{IL}$			120		150		200		250	ns
t_{OE} (3,4)	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}=V_{IL}$			60		60		75		100	ns
t_{DF} (2,5)	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float	$\overline{CE}=V_{IL}$			50		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first	$\overline{CE}=\overline{OE}/V_{PP}=V_{IL}$			0		0		0		0	ns

A.C. Waveforms for Read Operation (1)



Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

A.C. Waveforms for Page Reset Operation



Pin Capacitance (f = 1MHz T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

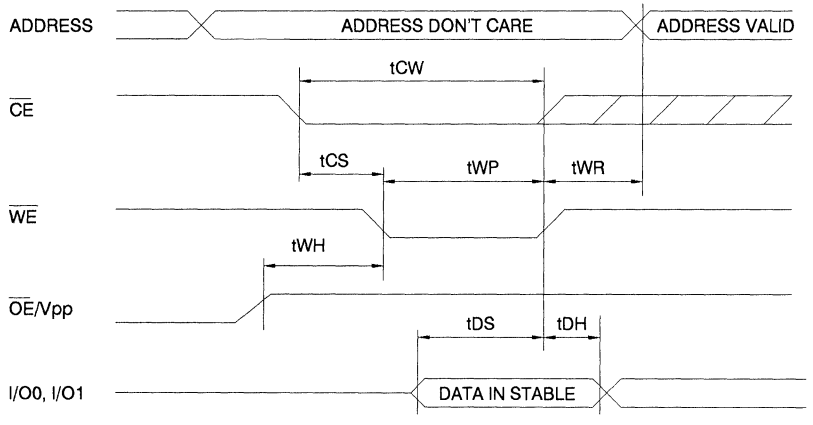
Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

A.C. Characteristics for Page Select and Page Reset Operations

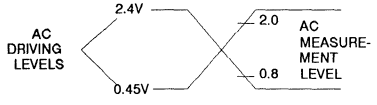
Symbol	Parameter	Condition	AT27C513R -12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{CW} (1)	$\overline{CE}$ to End of Write	$\overline{OE}/V_{PP} = V_{IH}$	110		110		145		180		ns
t_{WP} (1)	Write Pulse Width	$\overline{OE}/V_{PP} = V_{IH}$	60		60		80		100		ns
t_{WR} (3)	Write Recovery Time		20		20		20		20		ns
t_{DS}	Data Setup Time	$\overline{OE}/V_{PP} = V_{IH}$	35		35		45		50		ns
t_{DH}	Data Hold Time	$\overline{OE}/V_{PP} = V_{IH}$	20		20		20		20		ns
t_{CS}	$\overline{CE}$ to Write Setup Time	$\overline{OE}/V_{PP} = V_{IH}$	0		0		0		0		ns
t_{WH} (2,3)	$\overline{WE}$ Low from $\overline{OE}/V_{PP}$ High Delay Time		50		50		50		55		ns
t_{RST}	Reset Low Time		120		150		200		250		ns
t_{RAV}	Reset to Address Valid		120		150		200		250		ns

Notes: 1. Writing can be terminated by either $\overline{CE}$ or $\overline{WE}$ going high after the minimum t_{CW} or t_{WP} reguirements have been met.
2. $\overline{OE}/V_{PP}$ must be at V_{IH} during a Page Select.
3. This parameter is only sampled and is not 100% tested.

A.C. Waveforms for Page Select Operation

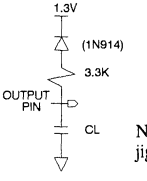


Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



Note: C_L=100pF including jig capacitance.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{OE}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1mA$		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400\mu A$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

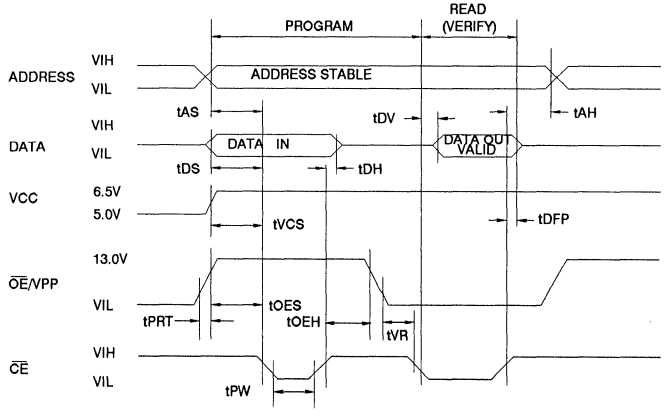
A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{OE}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{DV}	Data Valid from $\overline{CE}$	(Note 2)		1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Programming Waveforms [1]

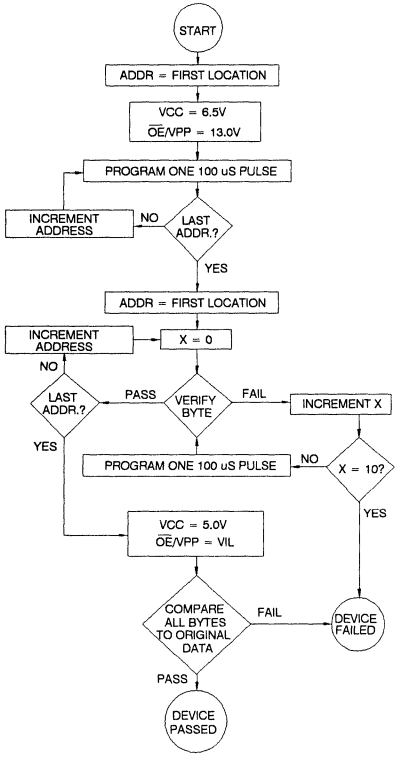


Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{DV} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page select operation prior to programming the AT27C513R.

Rapid Programming Algorithm [1]

A 100μs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100μs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100μs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

Note: 1. The proper page to be programmed must be selected by a page select operation prior to programming the AT27C513R.



Erasure Characteristics

The entire memory array of the AT27C513R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000μW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

4

Identification Code:

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	1	0	0E

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	20	0.1	AT27C513R-12DC AT27C513R-12LC	28DW6 32LW	Commercial (0°C to 70°C)
120	25	0.2	AT27C513R-12DI AT27C513R-12LI	28DW6 32LW	Industrial (-40°C to 85°C)
150	20	0.1	AT27C513R-15DC AT27C513R-15LC AT27C513R-15PC AT27C513R-15JC AT27C513R-15RC	28DW6 32LW 28P6 32J 28R	Commercial (0°C to 70°C)
150	25	0.2	AT27C513R-15DI AT27C513R-15LI AT27C513R-15PI AT27C513R-15JI AT27C513R-15RI	28DW6 32LW 28P6 32J 28R	Industrial (-40°C to 85°C)
			AT27C513R-15DM AT27C513R-15LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C513R-15DM/883 AT27C513R-15LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	20	0.1	AT27C513R-20DC AT27C513R-20LC AT27C513R-20PC AT27C513R-20JC AT27C513R-20RC	28DW6 32LW 28P6 32J 28R	Commercial (0°C to 70°C)
200	25	0.2	AT27C513R-20DI AT27C513R-20LI AT27C513R-20PI AT27C513R-20JI AT27C513R-20RI	28DW6 32LW 28P6 32J 28R	Industrial (-40°C to 85°C)
			AT27C513R-20DM AT27C513R-20LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C513R-20DM/883 AT27C513R-20LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	20	0.1	AT27C513R-25DC AT27C513R-25LC AT27C513R-25PC AT27C513R-25JC AT27C513R-25RC	28DW6 32LW 28P6 32J 28R	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	25	0.2	AT27C513R-25DI AT27C513R-25LI AT27C513R-25PI AT27C513R-25JI AT27C513R-25RI	28DW6 32LW 28P6 32J 28R	Industrial (-40°C to 85°C)
			AT27C513R-25DM AT27C513R-25LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C513R-25DM/883 AT27C513R-25LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

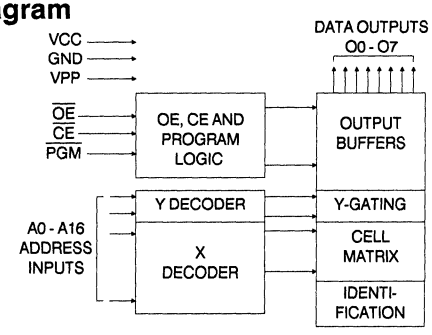
Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

1 MEGABIT (128K x 8) UV Erasable CMOS EPROM

Features

- **Low Power CMOS Operation**
  - **100 μA max. Standby**
  - **25 mA max. Active at 5 MHz (AT27C010L)**
  - **40 mA max. Active at 5 MHz (AT27C010)**
- **Fast Read Access Time - 120ns**
- **Wide Selection of JEDEC Standard Packages Including OTP**
  - **32-Lead 600 mil Cerdip and OTP Plastic DIP**
  - **32-Pad LCC**
  - **32-Lead JLCC and OTP PLCC**
- **5V± 10% Supply**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200mA Latchup Immunity**
- **Rapid Programming - 100μs/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Commercial and Industrial Temperature Ranges**

Block Diagram



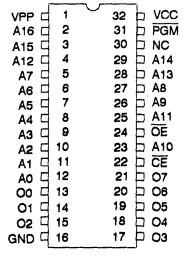
Description

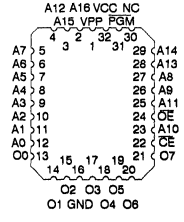
The AT27C010/L chip family is a low-power, high performance 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 128K x 8 bits. They require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

Two power versions are offered. In read mode, the AT27C010 typically consumes 25mA while the AT27C010L takes only 8mA. Standby mode supply current for both parts is typically less than 20μA.

Pin Configurations

Pin Name	Function
A0-A16	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect





Description (Continued)

The AT27C010/L come in a choice of industry standard JEDEC-approved packages including; 32-pin DIP in ceramic or one time programmable (OTP) plastic, 32-pad ceramic leadless chip carrier (LCC), and 32-lead ceramic (JLCC) or OTP plastic (PLCC) J-leaded chip carrier. All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 128K byte storage capability, the AT27C010/L allow firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C010/L have additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100μs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C010/L is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000μW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 w•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A16 = V_{IL}	X	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C010 / AT27C010L				
		-12	-15	-17	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V				5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V				10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC} + 0.3V				10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V				100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 1.0V				1	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	AT27C010L	Com.		25	mA
				Ind.,Mil.		30	mA
			AT27C010	Com.		40	mA
				Ind.,Mil.		50	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA				.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA			V_{CC}-0.3		V
		I_{OH} = -2.5mA			3.5		V
		I_{OH} = -400µA			2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

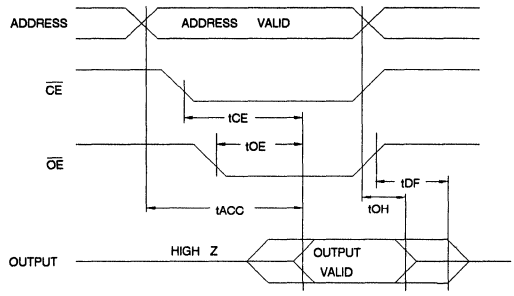
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C010 / AT27C010L										
				-12		-15		-17		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$ =V_{IL}	Com.		120		150		170		200		250	ns
			Ind.,Mil.		120		150		170		200		250	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			120		150		170		200		250	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			35		40		65		75		100	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}			30		40		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$ =V_{IL}			0		0		0		0		0	ns

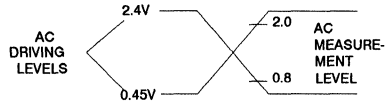
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



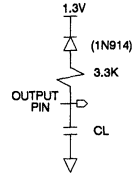
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



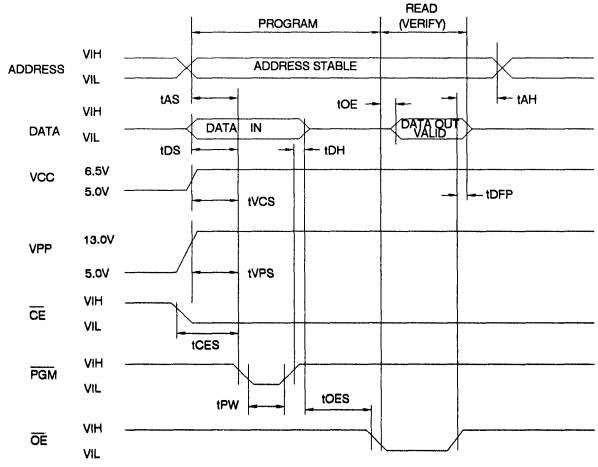
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C010/L a 0.1μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V

Notes:

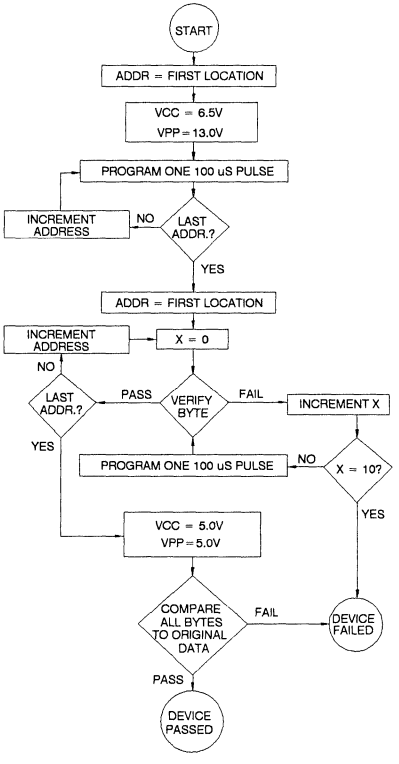
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27C010/L Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	05

Rapid Programming Algorithm

A 100µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{PGM}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	40	0.1	AT27C010-12DC AT27C010-12KC AT27C010-12LC	32DW6 32KW 32LW	Commercial (0°C to 70°C)
120	50	0.1	AT27C010-12DI AT27C010-12KI AT27C010-12LI	32DW6 32KW 32LW	Industrial (-40°C to 85°C)
			AT27C010-12DM AT27C010-12KM AT27C010-12LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-12DM/883 AT27C010-12KM/883 AT27C010-12LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	40	0.1	AT27C010-15DC AT27C010-15JC AT27C010-15KC AT27C010-15LC AT27C010-15PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
150	50	0.1	AT27C010-15DI AT27C010-15JI AT27C010-15KI AT27C010-15LI AT27C010-15PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010-15DM AT27C010-15KM AT27C010-15LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-15DM/883 AT27C010-15KM/883 AT27C010-15LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	40	0.1	AT27C010-17DC AT27C010-17JC AT27C010-17KC AT27C010-17LC AT27C010-15PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
170	50	0.1	AT27C010-17DI AT27C010-17JI AT27C010-17KI AT27C010-17LI AT27C010-17PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010-17DM AT27C010-17KM AT27C010-17LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-17DM/883 AT27C010-17KM/883 AT27C010-17LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	40	0.1	AT27C010-20DC AT27C010-20JC AT27C010-20KC AT27C010-20LC AT27C010-20PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
200	50	0.1	AT27C010-20DI AT27C010-20JI AT27C010-20KI AT27C010-20LI AT27C010-20PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010-20DM AT27C010-20KM AT27C010-20LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-20DM/883 AT27C010-20KM/883 AT27C010-20LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	40	0.1	AT27C010-25DC AT27C010-25JC AT27C010-25KC AT27C010-25LC AT27C010-25PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
250	50	0.1	AT27C010-25DI AT27C010-25JI AT27C010-25KI AT27C010-25LI AT27C010-25PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010-25DM AT27C010-25KM AT27C010-25LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-25DM/883 AT27C010-25KM/883 AT27C010-25LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	25	0.1	AT27C010L-12DC AT27C010L-12KC AT27C010L-12LC	32DW6 32KW 32LW	Commercial (0°C to 70°C)
120	30	0.1	AT27C010L-12DI AT27C010L-12KI AT27C010L-12LI	32DW6 32KW 32LW	Industrial (-40°C to 85°C)
			AT27C010L-12DM AT27C010L-12KM AT27C010L-12LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-12DM/883 AT27C010L-12KM/883 AT27C010L-12LM/883	32DW6 32KW 32LW	Military Class B, Fully Compliant (-55°C to 125°C)
150	25	0.1	AT27C010L-15DC AT27C010L-15JC AT27C010L-15LC AT27C010L-15KC AT27C010L-15PC	32DW6 32J 32LW 32KW 32P6	Commercial (0°C to 70°C)
150	30	0.1	AT27C010L-15DI AT27C010L-15JI AT27C010L-15KI AT27C010L-15LI AT27C010L-15PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010L-15DM AT27C010L-15KM AT27C010L-15LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-15DM/883 AT27C010L-15KM/883 AT27C010L-15LM/883	32DW6 32KW 32LW	Military Class B, Fully Compliant (-55°C to 125)
170	25	0.1	AT27C010L-17DC AT27C010L-17JC AT27C010L-17KC AT27C010L-17LC AT27C010L-17PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
170	30	0.1	AT27C010L-17DI AT27C010L-17JI AT27C010L-17KI AT27C010L-17LI AT27C010L-17PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010L-17DM AT27C010L-17KM AT27C010L-17LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-17DM/883 AT27C010L-17KM/883 AT27C010L-17LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	25	0.1	AT27C010L-20DC AT27C010L-20JC AT27C010L-20KC AT27C010L-20LC AT27C010L-20PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
200	30	0.1	AT27C010L-20DI AT27C010L-20JI AT27C010L-20KI AT27C010L-20LI AT27C010L-20PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010L-20DM AT27C010L-20KM AT27C010L-20LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-20DM/883 AT27C010L-20KM/883 AT27C010L-20LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.1	AT27C010L-25DC AT27C010L-25JC AT27C010L-25KC AT27C010L-25LC AT27C010L-25PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
250	30	0.1	AT27C010L-25DI AT27C010L-25JI AT27C010L-25KI AT27C010L-25LI AT27C010L-25PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010L-25DM AT27C010L-25KM AT27C010L-25LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-25DM/883 AT27C010L-25KM/883 AT27C010L-25LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

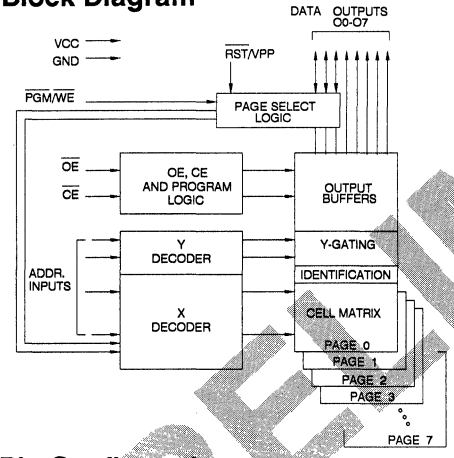
1 MEGABIT (8 x 16K x 8) UV Erasable Paged CMOS EPROM

Preliminary

Features

- Paged Configurations with Page Reset on Power-Up or $\overline{RST}$ Signal
  - 8 Pages, 16K x 8
- Low Power CMOS Operation
  - 100 μA max. Standby
  - 25 mA max. Active at 5 MHz
- Fast Read Access Time - 150ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP
  - 32-Pad LCC and OTP PLCC
- 5V± 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100μs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges
- Fully Compatible with 27128, 27513, 27011

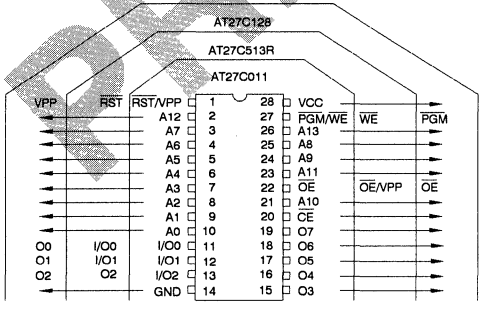
Block Diagram



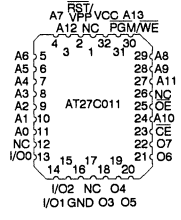
Address Pins	Number of Pages	Bits per Page
A0-A13	8	131,072

Pin Name	Function
A0-A13	Addresses
O2-O7	Outputs
I/O0-I/O1	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}/\overline{WE}$	Page Write Enable
$\overline{RST}/V_{PP}$	Page Reset
NC	No Connect

Pin Configurations



Note: JEDEC standard pinouts for AT27C513R and AT27C128 are shown for comparison only.



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description

The AT27C011 is a low-power, high performance 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM). This device requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 150ns, making this part compatible with high performance microprocessor systems by eliminating the need for speed-reducing WAIT states.

The AT27C011 features page mode addressing. Atmel's 27C011 has 8 pages, each organized 16K x 8, and provides a compatible upgrade for existing 128K EPROM based designs. Increased memory capacity and improved system performance can now be easily retrofitted without using costly additional board space.

The AT27C011 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latches are automatically reset to page 0 upon power-up (resets typically for $V_{CC} \leq 3.8V$) or when $\overline{RST}$/Vpp is brought low (V_{IL}).

Atmel's 1.2 micron scaled CMOS technology provides significantly lower active power consumption than similar NMOS designs. Power consumption is typically only 8mA in Active Mode and less than 20μA in Standby.

The AT27C011 is available in a choice of industry standard JEDEC-approved packages including; 28-pin DIP in ceramic or one time programmable (OTP) plastic, and 32-pad ceramic leadless chip carrier (LCC) or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$,$\overline{OE}$) to give designers the flexibility to prevent bus contention.

With a high density 128K byte storage capability, the AT27C011 allows firmware to be stored reliably and to be quickly accessed by the system without the delays of mass storage media.

The AT27C011 has additional features to ensure high quality and efficient production use. The rapid programming algorithm reduces the time required to program the chip and guarantees reliable programming. Programming time is typically 100μs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Page Selection Data [1]

	Page D_{IN}				Page D_{IN}		
Page Selection	**I/O2**	**I/O1**	**I/O0**	**Page Selection**	**I/O2**	**I/O1**	**I/O0**
Select Page 0	V_{IL}	V_{IL}	V_{IL}	Select Page 4	V_{IH}	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IL}	V_{IH}	Select Page 5	V_{IH}	V_{IL}	V_{IH}
Select Page 2	V_{IL}	V_{IH}	V_{IL}	Select Page 6	V_{IH}	V_{IH}	V_{IL}
Select Page 3	V_{IL}	V_{IH}	V_{IH}	Select Page 7	V_{IH}	V_{IH}	V_{IH}

Note: 1. The AT27C011 automatically resets to page 0 whenever $V_{CC} \leq 3.8V$ (typical conditions).

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}/\overline{WE}$	$\overline{RST}/V_{PP}$	Ai	V_{CC} [3]	**Outputs**	**I/Oi**
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	V_{CC}	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X[1]	V_{CC}	High Z	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	High Z	High Z
Rapid Program[2]	V_{IL}	V_{IH}	V_{IL}	V_{PP}	Ai	V_{CC}	D_{IN}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	Ai	V_{CC}	D_{OUT}	D_{OUT}
PGM Inhibit	V_{IH}	X	V_{IH}	V_{PP}	X	V_{CC}	High Z	High Z
Page Select	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	V_{CC} [3]	High Z	Page D_{IN}
Page Reset	X	X	X	V_{IL}	X	V_{CC} [3]	High Z	High Z
Product Identification[5]	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A9=V_H [4] A0=V_{IH} or V_{IL} A1-A13=V_{IL}	V_{CC}	Identification Code	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. Page 0 is automatically selected at power up (V_{CC} < 3.8V).
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 w•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

4

D.C. and A.C. Operating Conditions for Read and Page Select Operations

		AT27C011			
		-15	-17	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read and Page Select Operations

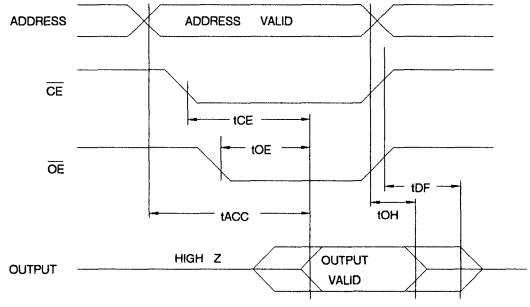
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{PP1}	$\overline{RST}/V_{PP}$ (1) Read/Standby Current	$\overline{RST}/V_{PP}$ = 3.8 to V_{CC} + 0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V			100	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V			1	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		25	mA
			Ind., Mil.		30	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -400µA		2.4		V
V_{CLR}	Page Latch Clear V_{CC} Supply Voltage				4.0	V

Notes: 1. V_{CC} must be applied simultaneously or before $\overline{RST}/V_{PP}$, and removed simultaneously or after $\overline{RST}/V_{PP}$.

A.C. Characteristics for Read Operation

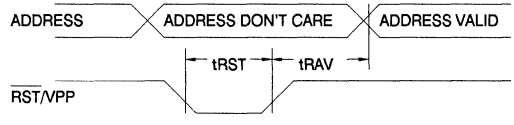
Symbol	Parameter	Condition		AT27C011 -15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}=\overline{OE}=V_{IL}$	Com.		150		170		200		250	ns
			Ind., Mil.				170		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay, $\overline{OE}=V_{IL}$				150		170		200		250	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}=V_{IL}$			65		70		75		100	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}=V_{IL}$			50		55		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}=\overline{OE}=V_{IL}$			0		0		0		0	ns

A.C. Waveforms for Read Operation (1)



Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

A.C. Waveforms for Page Reset Operation



Pin Capacitance (f = 1MHz T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

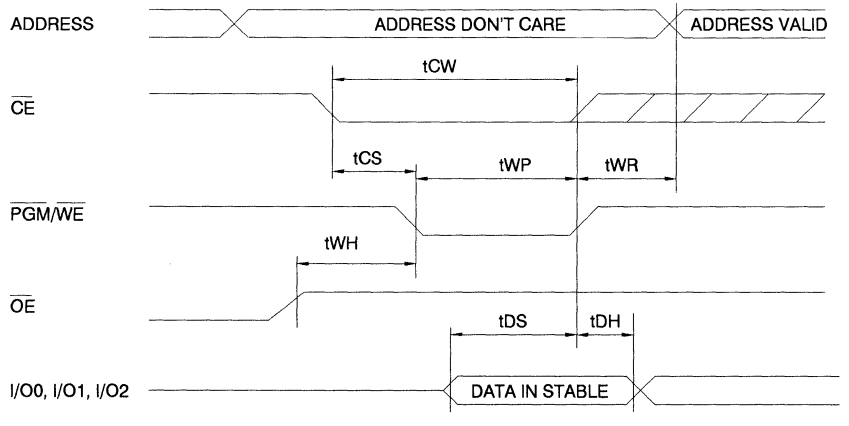
Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

A.C. Characteristics for Page Select and Page Reset Operations

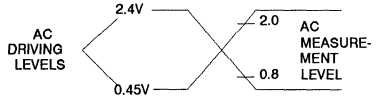
Symbol	Parameter	Condition	AT27C011 -15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{CW} (1)	$\overline{CE}$ to End of Write	$\overline{OE}=V_{IH}$	110		125		145		180		ns
t_{WP} (1)	Write Pulse Width	$\overline{OE}=V_{IH}$	60		70		80		100		ns
t_{WR} (3)	Write Recovery Time		20		20		20		20		ns
t_{DS}	Data Setup Time	$\overline{OE}=V_{IH}$	35		40		45		50		ns
t_{DH}	Data Hold Time	$\overline{OE}=V_{IH}$	20		20		20		20		ns
t_{CS}	$\overline{CE}$ to Write Setup Time	$\overline{OE}=V_{IH}$	0		0		0		0		ns
t_{WH} (2,3)	$\overline{PGM}/\overline{WE}$ Low from $\overline{OE}$ High Delay Time		50		50		50		55		ns
t_{RST}	Reset Low Time		150		170		200		250		ns
t_{RAV}	Reset to Address Valid		150		170		200		250		ns

Notes: 1. Writing can be terminated by either $\overline{CE}$ or $\overline{PGM}/\overline{WE}$ going high after the minimum t_{CW} or t_{WP} requirements have been met.
2. $\overline{OE}$ must be at V_{IH} during a Page Select.
3. This parameter is only sampled and is not 100% tested.

A.C. Waveforms for Page Select Operation

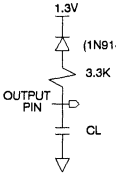


Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



Note: C_L=100pF including jig capacitance.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{RST}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1mA$		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400\mu A$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{RST}/V_{PP}$ Current	$\overline{CE}=\overline{PGM/WE}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{RST}/V_{PP}$=13.0±0.25V

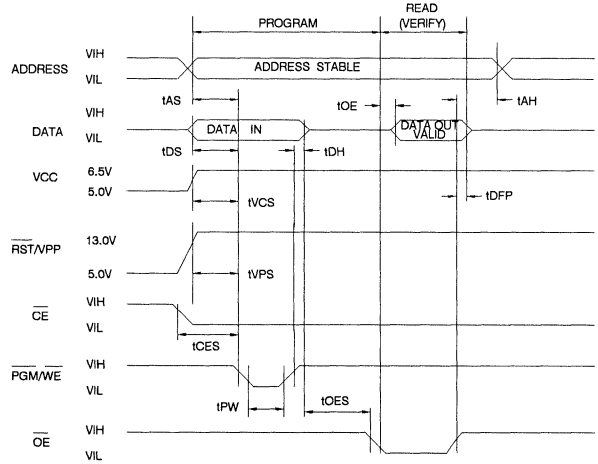
Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	$\overline{RST}/V_{PP}$ Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM/WE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{RST}/V_{PP}$ and removed simultaneously or after $\overline{RST}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Programming Waveforms (1)

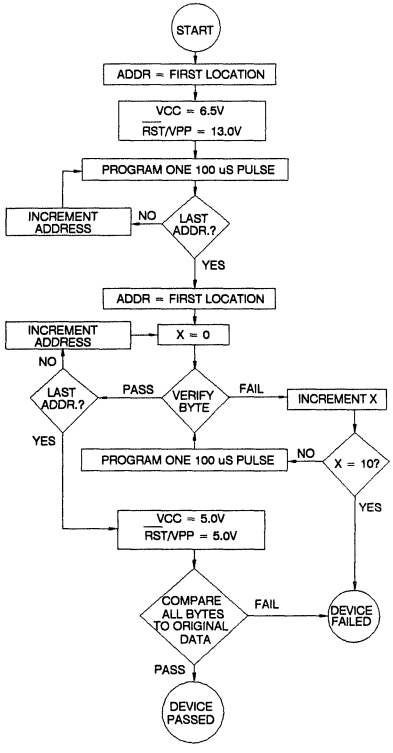


Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{DV} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page select operation prior to programming the AT27C011.

Rapid Programming Algorithm [1]

A 100μs $\overline{PGM}/\overline{WE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{RST}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100μs $\overline{PGM}/\overline{WE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100μs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{RST}/V_{PP}$ is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

Note: 1. The proper page to be programmed must be selected by a page select operation prior to programming the AT27C011.



Erasure Characteristics

The entire memory array of the AT27C011 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15W \bullet sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

4

Identification Code:

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	0	1	0	1	85

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	25	0.1	AT27C011-15DC AT27C011-15LC	28DW6 32LW	Commercial (0°C to 70°C)
170	25	0.1	AT27C011-17DC AT27C011-17LC AT27C011-17PC AT27C011-17JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
170	30	0.1	AT27C011-17DI AT27C011-17LI AT27C011-17PI AT27C011-17JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C011-17DM AT27C011-17LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C011-17DM/883 AT27C011-17LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	25	0.1	AT27C011-20DC AT27C011-20LC AT27C011-20PC AT27C011-20JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
200	30	0.1	AT27C011-20DI AT27C011-20LI AT27C011-20PI AT27C011-20JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C011-20DM AT27C011-20LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C011-20DM/883 AT27C011-20LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.1	AT27C011-25DC AT27C011-25LC AT27C011-25PC AT27C011-25JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
250	30	0.1	AT27C011-25DI AT27C011-25LI AT27C011-25PI AT27C011-25JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C011-25DM AT27C011-25LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C011-25DM/883 AT27C011-25LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

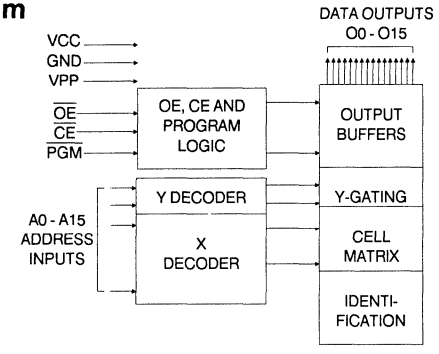
Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

1 MEGABIT (64K x 16) UV Erasable CMOS EPROM

Features

- Low Power CMOS Operation
  - 100 μA max. Standby
  - 30 mA max. Active at 5 MHz (AT27C1024L)
  - 50 mA max. Active at 5 MHz (AT27C1024)
- Fast Read Access Time - 120ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 40-Lead 600 mil Cerdip and OTP Plastic DIP
  - 44-Pad LCC and OTP PLCC
- 5V$\pm$ 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100μs/word (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Commercial and Industrial Temperature Ranges

Block Diagram



Description

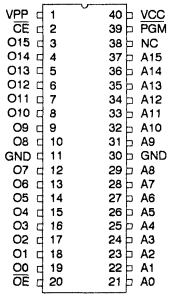
The AT27C1024/L chip family is a low-power, high performance 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 16. They require only one 5V power supply in normal read mode operation. Any word can be accessed in less than 120ns, eliminating the need for speed reducing WAIT states. The by-16 organization makes these parts ideal for high-performance 16 and 32 bit microprocessor systems.

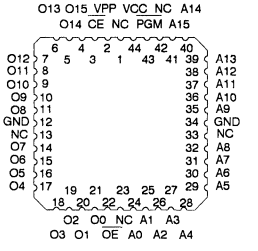
Two power versions are offered. In read mode, the AT27C1024 typically consumes 30mA while the AT27C1024L takes only 15mA. Standby mode supply current for both parts is typically less than 20μA.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.





Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

Description (Continued)

The AT27C1024/L come in a choice of industry standard JEDEC-approved packages including; 40-pin DIP in ceramic or one time programmable (OTP) plastic, and 44-pad ceramic leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K word storage capability, the AT27C1024/L allow firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C1024/L have additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100μs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C1024/L is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15W \bullet sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 $w \bullet sec/cm^2$

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A15 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} current (I_{SB}) is specified with $V_{PP}=V_{CC}$. $V_{CC} > V_{PP}$ will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C1024 / AT27C1024L				
		-12	-15	-17	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V				5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V				10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC} + 0.3V				10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V				100	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V				1	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	AT27C1024L	Com.		30	mA
				Ind.,Mil.		40	mA
			AT27C1024	Com.		50	mA
				Ind.,Mil.		60	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA				.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA			V_{CC}-0.3		V
		I_{OH} = -2.5mA			3.5		V
		I_{OH} = -400µA			2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

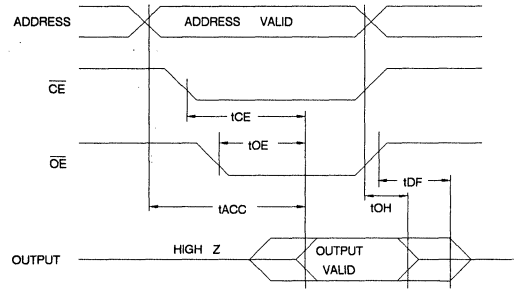
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C1024 / AT27C1024L										
				-12		-15		-17		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$ =V_{IL}	Com.		120		150		170		200		250	ns
			Ind.,Mil.						170		200		250	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			120		150		170		200		250	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			60		65		65		75		100	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}			30		40		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$ =V_{IL}			0		0		0		0		0	ns

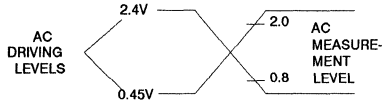
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



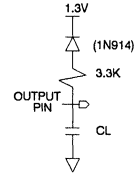
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



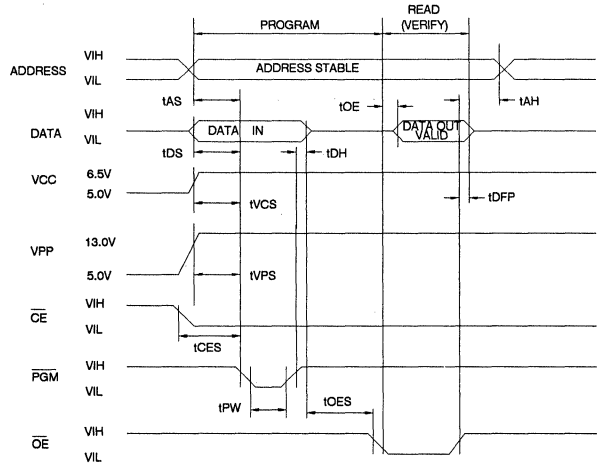
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C1024/L a 0.1μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V

Notes:

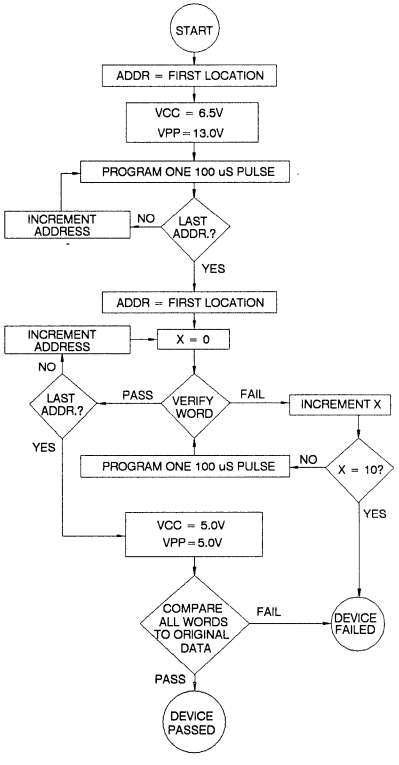
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27C1024/L Integrated Product Identification Code:

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	0	1	00F1

Rapid Programming Algorithm

A 100µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{PGM}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	50	0.1	AT27C1024-12DC AT27C1024-12LC	40DW6 44LW	Commercial (0°C to 70°C)
150	50	0.1	AT27C1024-15DC AT27C1024-15LC AT27C1024-15PC AT27C1024-15JC	40DW6 44LW 40P6 44J	Commercial (0°C to 70°C)
150	60	0.1	AT27C1024-15DI AT27C1024-15LI AT27C1024-15PI AT27C1024-15JI	40DW6 44LW 40P6 44J	Industrial (-40°C to 85°C)
			AT27C1024-15DM AT27C1024-15LM	40DW6 44LW	Military (-55°C to 125°C)
			AT27C1024-15DM/883 AT27C1024-15LM/883	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	50	0.1	AT27C1024-17DC AT27C1024-17LC AT27C1024-17PC AT27C1024-17JC	40DW6 44LW 40P6 44J	Commercial (0°C to 70°C)
170	60	0.1	AT27C1024-17DI AT27C1024-17LI AT27C1024-17PI AT27C1024-17JI	40DW6 44LW 40P6 44J	Industrial (-40°C to 85°C)
			AT27C1024-17DM AT27C1024-17LM	40DW6 44LW	Military (-55°C to 125°C)
			AT27C1024-17DM/883 AT27C1024-17LM/883	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	50	0.1	AT27C1024-20DC AT27C1024-20LC AT27C1024-20PC AT27C1024-20JC	40DW6 44LW 40P6 44J	Commercial (0°C to 70°C)
200	60	0.1	AT27C1024-20DI AT27C1024-20LI AT27C1024-20PI AT27C1024-20JI	40DW6 44LW 40P6 44J	Industrial (-40°C to 85°C)
			AT27C1024-20DM AT27C1024-20LM	40DW6 44LW	Military (-55°C to 125°C)
			AT27C1024-20DM/883 AT27C1024-20LM/883	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	50	0.1	AT27C1024-25DC AT27C1024-25LC AT27C1024-25PC AT27C1024-25JC	40DW6 44LW 40P6 44J	Commercial (0°C to 70°C)
250	60	0.1	AT27C1024-25DI AT27C1024-25LI AT27C1024-25PI AT27C1024-25JI	40DW6 44LW 40P6 44J	Industrial (-40°C to 85°C)
			AT27C1024-25DM AT27C1024-25LM	40DW6 44LW	Military (-55°C to 125°C)
			AT27C1024-25DM/883 AT27C1024-25LM/883	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	50	0.1	AT27C1024L-12DC AT27C1024L-12LC	40DW6 44LW	Commercial (0°C to 70°C)
150	30	0.1	AT27C1024L-15DC AT27C1024L-15LC	40DW6 44LW	Commercial (0°C to 70°C)
150	50	0.1	AT27C1024L-15PC AT27C1024L-15JC	40P6 44J	Commercial (0°C to 70°C)
150	60	0.1	AT27C1024L-15PI AT27C1024L-15JI	40P6 44J	Industrial (-40°C to 85°C)
170	30	0.1	AT27C1024L-17DC AT27C1024L-17LC AT27C1024L-17PC AT27C1024L-17JC	40DW6 44LW 40P6 44J	Commercial (0°C to 70°C)
170	40	0.1	AT27C1024L-17DI AT27C1024L-17LI AT27C1024L-17PI AT27C1024L-17JI	40DW6 44LW 40P6 44J	Industrial (-40°C to 85°C)
			AT27C1024L-17DM AT27C1024L-17LM	40DW6 44LW	Military (-55°C to 125°C)
			AT27C1024L-17DM/883 AT27C1024L-17LM/883	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT27C1024L-20DC AT27C1024L-20LC AT27C1024L-20PC AT27C1024L-20JC	40DW6 44LW 40P6 44J	Commercial (0°C to 70°C)
200	40	0.1	AT27C1024L-20DI AT27C1024L-20LI AT27C1024L-20PI AT27C1024L-20JI	40DW6 44LW 40P6 44J	Industrial (-40°C to 85°C)
			AT27C1024L-20DM AT27C1024L-20LM	40DW6 44LW	Military (-55°C to 125°C)
			AT27C1024L-20DM/883 AT27C1024L-20LM/883	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT27C1024L-25DC AT27C1024L-25LC AT27C1024L-25PC AT27C1024L-25JC	40DW6 44LW 40P6 44J	Commercial (0°C to 70°C)
250	40	0.1	AT27C1024L-25DI AT27C1024L-25LI AT27C1024L-25PI AT27C1024L-25JI	40DW6 44LW 40P6 44J	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	40	0.1	AT27C1024L-25DM AT27C1024L-25LM	40DW6 44LW	Military (-55°C to 125°C)
			AT27C1024L-25DM/883 AT27C1024L-25LM/883	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

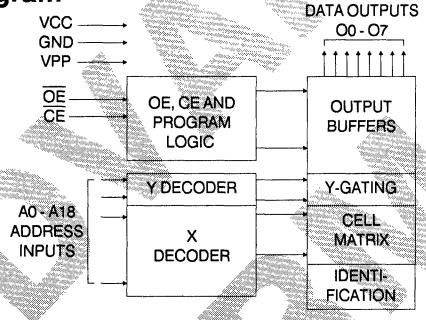
- Low Power CMOS Operation
  - 100 μA max. Standby
  - 25 mA max. Active at 5 MHz
- Fast Read Access Time - 120ns
- JEDEC Standard Package
  - 32-Lead 600 mil Cerdip
- 5V± 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100μs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Industrial and Commercial Temperature Ranges

4 MEGABIT (512K x 8) UV Erasable CMOS EPROM

4

Advance Information

Block Diagram



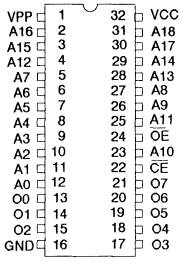
Description

The AT27C040 chip family is a low-power, high-performance 4,194,304 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 512K x 8 bits. The AT27C040 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

Atmel's 1.2 micron scaled CMOS technology provides for significantly lower active power consumption than similar NMOS designs. Power consumption is typically 20mA in active mode and less than 20μA in standby mode.

Pin Configurations

Pin Name	Function
A0-A18	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	25	0.1	AT27C040-12DC	32DW6	Commercial (0°C to 70°C)
150	25	0.1	AT27C040-15DC	32DW6	Commercial (0°C to 70°C)
150	30	0.1	AT27C040-15DI	32DW6	Industrial (-40°C to 85°C)
			AT27C040-15DM	32DW6	Military (-55°C to 125°C)
			AT27C040-15DM/883	32DW6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	25	0.1	AT27C040-20DC	32DW6	Commercial (0°C to 70°C)
200	30	0.1	AT27C040-20DI	32DW6	Industrial (-40°C to 85°C)
			AT27C040-20DM	32DW6	Military (-55°C to 125°C)
			AT27C040-20DM/883	32DW6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.1	AT27C040-25DC	32DW6	Commercial (0°C to 70°C)
250	30	0.1	AT27C040-25DI	32DW6	Industrial (-40°C to 85°C)
			AT27C040-25DM	32DW6	Military (-55°C to 125°C)
			AT27C040-25DM/883	32DW6	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)

CONTENTS

Section 5

High-Speed CMOS PROMs

5

Features

- **Fast Access Time - 35ns**
- **Low Power Dissipation**
  - **100 μA Standby Current (AT28HC191L)**
  - **80 mA Active Current**
- **E^{2}PROM Technology - 100% Reprogrammable**
- **Direct Replacement for Bipolar PROMs**
- **Reprogrammable 1000 times**
- **Chip Clear**
- **JEDEC Approved Byte-Wide Pinout**
  - **Industry Standard 600 mil Wide Package**
- **CMOS and TTL Compatible Inputs and Outputs**
- **High Reliability High Speed CMOS Technology**
- **Full Military, Commercial, and Industrial Temperature Ranges**

16K (2K x 8) High Speed Electrically Erasable CMOS PROM

5

Description

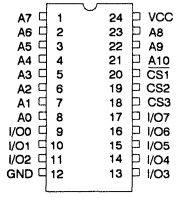
The AT28HC191/191L are a pair of high-speed, low-power 2,048 words by 8 bit CMOS PROMs. The high speed AT28HC191 offers access times to 35ns while the AT28HC191L provides low standby current consumption of just 100μA. Both devices are packaged in 24 pin dual inline packages using the JEDEC approved pinout for byte-wide PROMs. The AT28HC191 and AT28HC191L are packaged in the industry standard 600 mil wide package.

These devices are plug-in replacements for 16k bipolar PROMs, while offering distinct advantages in power consumption, performance and programming. Atmel's low power CMOS devices provide a direct power saving upgrade to systems originally using bipolar PROMs. The ultra-low standby power of the 28HC191L brings bipolar speeds to battery powered systems.

The electrically erasable and programmable memory cell allows for 100% testing of each memory location. The E^{2}PROM cell's low programming current permits devices to be programmed one byte at a time. On chip circuitry automatically erases each byte and rewrites it with the new data, permitting in socket reprogramming. The entire memory array can also be erased simultaneously, if desired, by using the device's "chip- clear" mode.

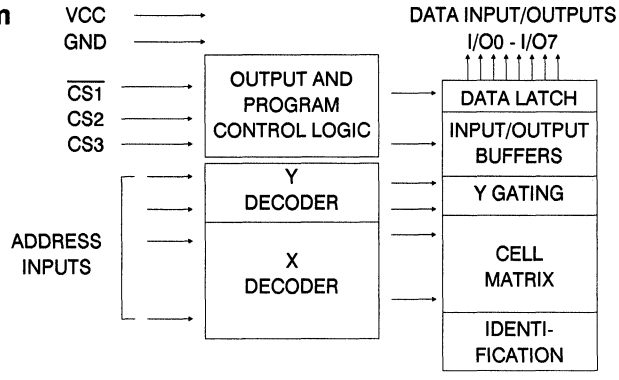
The fast access time of the devices makes them suitable for high-performance applications such as micro-control storage. In such an application the device allows for fast execution speeds, without penalizing storage density or power consumption. With a memory capacity of 2K bytes, these devices provide economical, reliable and high-performance means of storing program instructions. System reliability is enhanced by the low power and inherent reliability of Atmel's 1.5 micron floating poly technology.

Pin Configurations



Pin Name	Function
A0-A10	Addresses
$\overline{CS1}$	Chip Select (Power Down Option)
CS2	Chip Select
CS3	Chip Select
I/O0-I/O7	Data

Block Diagram



Operating Modes

Mode	CS3	CS2	$\overline{CS1}$	I/O
Read	V_{IH}	V_{IH}	V_{IL}	D_{OUT}
Standby	X(1)	X	V_{IH}	High Z
Output Disable	V_{IL}	X	X	High Z
Output Disable	X	V_{IL}	X	High Z
Write(2)	V_{IL}	V_{IL}	V_H (3)	D_{IN}
Verify	V_{IH}	V_{IH}	V_H	D_{OUT}
Chip Erase	V_{IL}	V_H	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0 \pm 0.5V$.

Device Operation

READ: When $\overline{CS1}$ is low and CS2 and CS3 are high, the data stored at the memory location determined by the address inputs is asserted on the outputs of the device. The outputs are put in a high impedance state whenever CS2 or CS3 is low or whenever $\overline{CS1}$ is high. The availability of three control lines gives the designer flexibility in preventing bus contention.

STANDBY: The AT28HC191L consumes less than 550μW when deselected by raising $\overline{CS1}$ to V_{CC}-0.3V. This part retains the fast chip select times from CS2 and CS3 that are common to the AT28HC191.

PROGRAMMING: A 12 volt input is required on the $\overline{CS1}$ pin in order to program the devices. This input voltage is not needed to supply the programming current required by the memory cells as all high voltages used inside the chip are self-generated. After $\overline{CS1}$ is raised to 12 volts with CS2 low and CS3 high, CS3 is pulsed low to begin the internally timed write cycle. The address location presented to the device on the falling edge of the CS3 signal is written with the data that is presented to the device on the rising edge of CS3. An entire eight bit byte is programmed during each programming cycle. Any byte can be programmed to any data pattern regardless of the current data in that byte. An internal timer uses 1 ms to program a byte. No additional time is required nor are any additional programming pulses.

VERIFY: A verify of programmed data may be performed with $\overline{CS1}$ at 12 volts by taking CS2 and CS3 to V_{IH}. The verify works exactly as a device read except that $\overline{CS1}$ is at 12 volts rather than V_{IL}.

MEMORY CELL: The AT28HC191 family of parts uses fully reprogrammable E^2PROM cells to store data. Unlike the one time programmable fuse link cells commonly found in bipolar PROMs, E^2PROM cells allow each bit to be fully tested before shipment by Atmel. The electrical reprogrammability of E^2PROM cells allows for multiple patterns to be written into each device during testing to ensure proper programming, functioning, and timing. All cells may be reprogrammed up to 1000 times by the user.

CHIP CLEAR: The entire contents of these memory devices may be set to the high state by the chip clear function. By setting $\overline{CS1}$ low and CS2 to 12 volts, the chip is cleared when a 10 msec low pulse is applied to CS3.

PRODUCT IDENTIFICATION CODE: The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages for the device.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{CS1}$, CS2 and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5

D.C. and A.C. Operating Range

		AT28HC191-35	AT28HC191-45 AT28HC191L-45	AT28HC191-55 AT28HC191L-55
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	μA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	μA
I_{CC1}	V_{CC} Standby Current	$\overline{CS1}$ = V_{IH} ADDR = 0/V_{CC}	AT28HC191L		3	mA
			AT28HC191		60	mA
I_{CC}	V_{CC} Active Current	f = 10MHz; I_{OUT} = 0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 12mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0mA		2.4		V

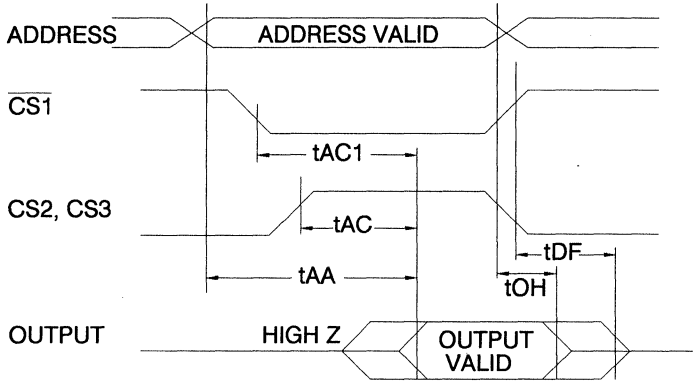
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Characteristics for Read Operation [1]

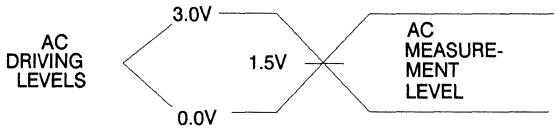
Symbol	Parameter	AT28HC191 -35 Min	AT28HC191 -35 Max	AT28HC191 -45 Min	AT28HC191 -45 Max	AT28HC191 -55 Min	AT28HC191 -55 Max	AT28HC191L -45 Min	AT28HC191L -45 Max	AT28HC191L -55 Min	AT28HC191L -55 Max	Units
t_{AA} [2]	Address to Output Delay		35		45		55		45		55	ns
t_{AC} [2]	CS2, CS3 to Output Delay		25		30		40		30		40	ns
t_{AC1} [2]	$\overline{CS1}$ to Output Delay		30		35		40		45		55	ns
t_{DF} [3,4]	$\overline{CS1}$, CS2, CS3 to Output Float	0	25	0	30	0	40	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{CS1}$,CS2, CS3, or Address, whichever occurred first	0		0		0		0		0		ns

A.C. Read Waveforms



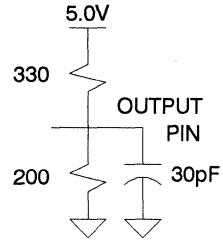
Notes:
1. CL=30pF
2. $\overline{CS}$, CS2 or CS3 may be delayed up to t_{AA}-t_{AC} after the address transition without impact on t_{AA}.
3. t_{DF} is specified from $\overline{CS1}$, CS2, or CS3, whichever occurs first.
4. This parameter is only characterized and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns

Output Test Load

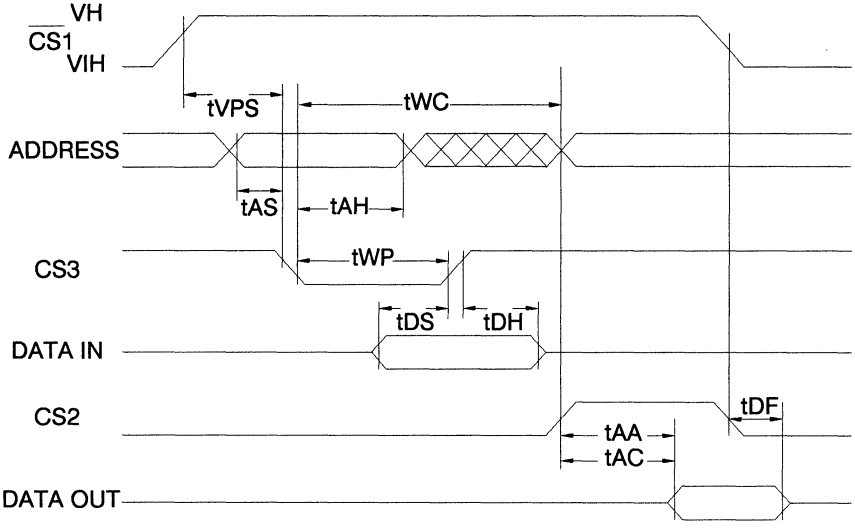


A.C. Write Characteristics

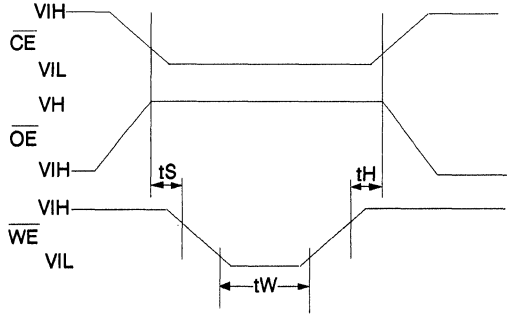
Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width	50		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WC}	Write Cycle Time	1			ms
t_{VPS}	Programming Set-up Time	2			μs
t_{AA}	Address to Output Delay			100	ns
t_{AC}	CSn to Output Delay			100	ns
t_{DF}	CSn to Output Float			60	ns

5

A.C. Write Waveforms



Chip Erase Waveforms



$t_S = t_H = 1\mu$sec (min.)
t_W = 10msec (min.)
$V_H = 12 \pm 0.5V$

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	80	60	28HC191-35DC AT28HC191-35PC	24D6 24P6	Commercial (0° to 70°C)
45	80	60	AT28HC191-45DC AT28HC191-45PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191-45DI AT28HC191-45PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191-45DM	24D6	Military (-55° to 125°C)
			AT28HC191-45DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	60	AT28HC191-55DC AT28HC191-55PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191-55DI AT28HC191-55PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191-55DM	24D6	Military (-55° to 125°C)
			AT28HC191-55DM/883	24D6	Military Class B, Fully Compliant (-55° to 125°C)

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	80	3	AT28HC191L-45DC AT28HC191L-45PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191L-45DI AT28HC191L-45PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191L-45DM	24D6	Military (-55° to 125°C)
			AT28HC191L-45DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	3	AT28HC191L-55DC AT28HC191L-55PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191L-55DI AT28HC191L-55PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191L-55DM	24D6	Military (-55° to 125°C)
			AT28HC191L-55DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)

5

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Features

- **Fast Access Time - 35ns**
- **Low Power Dissipation**
  - **100 μA Standby Current (AT28HC291L)**
  - **80 mA Active Current**
- **E^{2}PROM Technology - 100% Reprogrammable**
- **Direct Replacement for Bipolar PROMs**
- **Reprogrammable 1000 times**
- **Chip Clear**
- **JEDEC Approved Byte-Wide Pinout**
  - **Space-Saving 300 mil Wide Package**
- **CMOS and TTL Compatible Inputs and Outputs**
- **High Reliability High Speed CMOS Technology**
- **Full Military, Commercial, and Industrial Temperature Ranges**

16K (2K x 8) High Speed Electrically Erasable CMOS PROM

5

Description

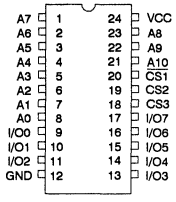
The AT28HC291/291L are a pair of high-speed, low-power 2,048 words by 8 bit CMOS PROMs. The high speed AT28HC291 offers access times to 35ns while the AT28HC291L provides low standby current consumption of just 100μA. Both devices are packaged in 24 pin dual inline packages using the JEDEC approved pinout for byte-wide PROMs. The AT28HC291 and AT28HC291L are supplied in space-saving 300 mil wide packages and also in 28 pad leadless chip carriers.

These devices are plug-in replacements for 16k bipolar PROMs, while offering distinct advantages in power consumption, performance and programming. Atmel's low power CMOS devices provide a direct power saving upgrade to systems originally using bipolar PROMs. The ultra-low standby power of the 28HC291L brings bipolar speeds to battery powered systems.

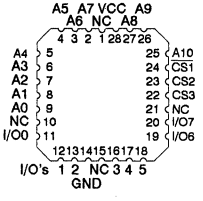
The electrically erasable and programmable memory cell allows for 100% testing of each memory location. The E^{2}PROM cell's low programming current permits devices to be programmed one byte at a time. On chip circuitry automatically erases each byte and rewrites it with the new data, permitting in socket reprogramming. The entire memory array can also be erased simultaneously, if desired, by using the device's "chip- clear" mode.

The fast access time of the devices makes them suitable for high-performance applications such as micro-control storage. In such an application the device allows for fast execution speeds, without penalizing storage density or power consumption. With a memory capacity of 2K bytes, these devices provide economical, reliable, and high-performance means of storing program instructions. System reliability is enhanced by the low power and inherent reliability of Atmel's 1.5 micron floating poly technology.

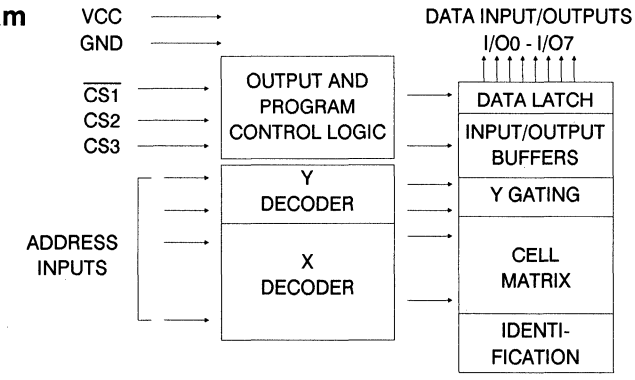
Pin Configurations



Pin Name	Function
A0-A10	Addresses
$\overline{CS1}$	Chip Select (Power Down Option)
CS2	Chip Select
CS3	Chip Select
I/O0-I/O7	Data
NC	No Connect



Block Diagram



Operating Modes

Mode	CS3	CS2	$\overline{CS1}$	I/O
Read	V_{IH}	V_{IH}	V_{IL}	D_{OUT}
Standby	X(1)	X	V_{IH}	High Z
Output Disable	V_{IL}	X	X	High Z
Output Disable	X	V_{IL}	X	High Z
Write(2)	V_{IL}	V_{IL}	V_H (3)	D_{IN}
Verify	V_{IH}	V_{IH}	V_H	D_{OUT}
Chip Erase	V_{IL}	V_H	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0 \pm 0.5V$.

Device Operation

READ: When $\overline{CS1}$ is low and CS2 and CS3 are high, the data stored at the memory location determined by the address inputs is asserted on the outputs of the device. The outputs are put in a high impedance state whenever CS2 or CS3 is low or whenever $\overline{CS1}$ is high. The availability of three control lines gives the designer flexibility in preventing bus contention.

STANDBY: The AT28HC291L consumes less than 550μW when deselected by raising $\overline{CS1}$ to V_{CC}-0.3V. This part retains the fast chip select times from CS2 and CS3 that are common to the AT28HC291.

PROGRAMMING: A 12 volt input is required on the $\overline{CS1}$ pin in order to program the devices. This input voltage is not needed to supply the programming current required by the memory cells as all high voltages used inside the chip are self-generated. After $\overline{CS1}$ is raised to 12 volts with CS2 low and CS3 high, CS3 is pulsed low to begin the internally timed write cycle. The address location presented to the device on the falling edge of the CS3 signal is written with the data that is presented to the device on the rising edge of CS3. An entire eight bit byte is programmed during each programming cycle. Any byte can be programmed to any data pattern regardless of the current data in that byte. An internal timer uses 1 ms to program a byte. No additional time is required nor are any additional programming pulses.

VERIFY: A verify of programmed data may be performed with $\overline{CS1}$ at 12 volts by taking CS2 and CS3 to VIH. The verify works exactly as a device read except that CS1 is at 12 volts rather than VIL.

MEMORY CELL: AT28HC291 family of parts uses fully reprogrammable E^2PROM cells to store data. Unlike the one time programmable fuse link cells commonly found in bipolar PROMs, E^2PROM cells allow each bit to be fully tested before shipment by Atmel. The electrical reprogrammability of E^2PROM cells allows for multiple patterns to be written into each device during testing to ensure proper programming, functioning and timing. All cells may be reprogrammed up to 1000 times by the user.

CHIP CLEAR: The entire contents of these memory devices may be set to the high state by the chip clear function. By setting $\overline{CS1}$ low and CS2 to 12 volts, the chip is cleared when a 10 msec low pulse is applied to CS3.

PRODUCT IDENTIFICATION CODE: The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages for the device.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{CS1}$, CS2 and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28HC291-35	AT28HC291-45 AT28HC291L-45	AT28HC291-55 AT28HC291L-55
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{CC1}	V_{CC} Standby Current	$\overline{CS1}$ = V_{IH} ADDR = 0/V_{CC}	AT28HC291L		3	mA
			AT28HC291		60	mA
I_{CC}	V_{CC} Active Current	f = 10MHz; I_{OUT} = 0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 12mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0mA		2.4		V

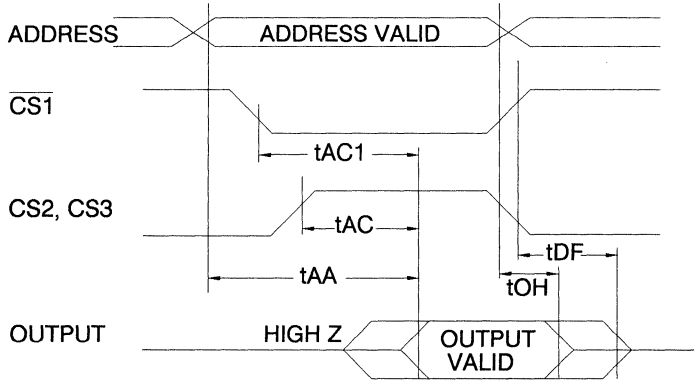
Pin Capacitance (f = 1MHz T = 25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Characteristics for Read Operation [1]

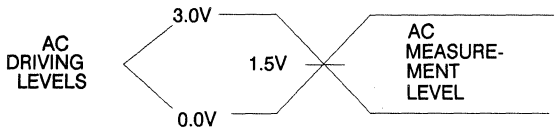
Symbol	Parameter	AT28HC291 -35 Min	AT28HC291 -35 Max	AT28HC291 -45 Min	AT28HC291 -45 Max	AT28HC291 -55 Min	AT28HC291 -55 Max	AT28HC291L -45 Min	AT28HC291L -45 Max	AT28HC291L -55 Min	AT28HC291L -55 Max	Units
t_{AA} [2]	Address to Output Delay		35		45		55		45		55	ns
t_{AC} [2]	CS2, CS3 to Output Delay		25		30		40		30		40	ns
t_{AC1} [2]	$\overline{CS1}$ to Output Delay		30		35		40		45		55	ns
t_{DF} [3,4]	$\overline{CS1}$, CS2, CS3 to Output Float	0	25	0	30	0	40	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{CS1}$,CS2, CS3, or Address, whichever occurred first	0		0		0		0		0		ns

A.C. Read Waveforms



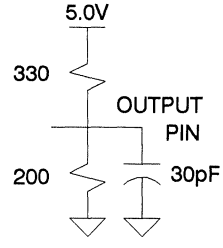
Notes:
1. CL=30pF
2. $\overline{CS}$, CS2 or CS3 may be delayed up to t_{AA}-t_{AC} after the address transition without impact on t_{AA}.
3. t_{DF} is specified from $\overline{CS1}$, CS2, or CS3, whichever occurs first.
4. This parameter is only characterized and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns

Output Test Load



A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width	50		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WC}	Write Cycle Time	1			ms
t_{VPS}	Programming Set-up Time	2			μs
t_{AA}	Address to Output Delay			100	ns
t_{AC}	CSn to Output Delay			100	ns
t_{DF}	CSn to Output Float			60	ns

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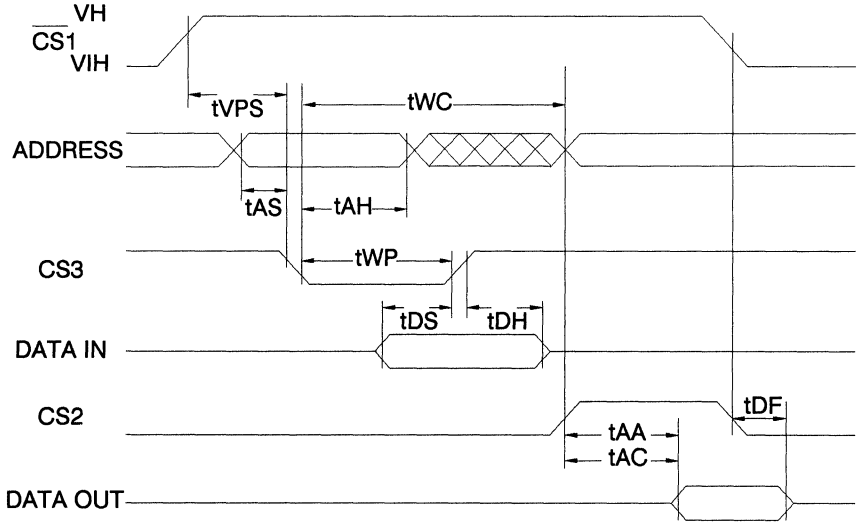
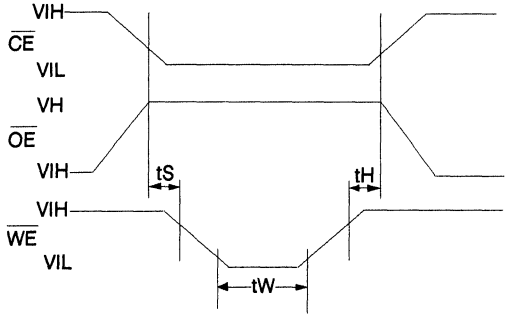
A.C. Write Waveforms



Chip Erase Waveforms



$t_S = t_H = 1\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12 \pm 0.5V$

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	80	60	AT28HC291-35DC AT28HC291-35PC	24D3 24P3	Commercial (0° to 70°C)
45	80	60	AT28HC291-45DC AT28HC291-45LC AT28HC291-45PC	24D3 28L 24P3	Commercial (0° to 70°C)
			AT28HC291-45DI AT28HC291-45LI AT28HC291-45PI	24D3 28L 28P3	Industrial (-40° to 85°C)
			AT28HC291-45DM AT28HC291-45LM	24D3 28L	Military (-55° to 125°C)
			AT28HC291-45DM/883 AT28HC291-45LM/883	24D3 28L	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	60	AT28HC291-55DC AT28HC291-55LC AT28HC291-55PC	24D3 28L 24P3	Commercial (0° to 70°C)
			AT28HC291-55DI AT28HC291-55LI AT28HC291-55PI	24D3 28L 24P3	Industrial (-40° to 85°C)
			AT28HC291-55DM AT28HC291-55LM	24D3 28L	Military (-55° to 125°C)
			AT28HC291-55DM/883 AT28HC291-55LM/883	24D3 28L	Military/883 Class B, Fully Compliant (-55° to 125°C)

Package Type	
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	80	3	AT28HC291L-45DC AT28HC291L-45PC	24D3 24P3	Commercial (0° to 70°C)
			AT28HC291L-45DI AT28HC291L-45PI	24D3 28P3	Industrial (-40° to 85°C)
			AT28HC291L-45DM	24P3	Military (-55° to 125°C)
			AT28HC291L-45DM/883	24D3	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	3	AT28HC291L-55DC AT28HC291L-55LC AT28HC291L-55PC	24D3 28L 24P3	Commercial (0° to 70°C)
			AT28HC291L-55DI AT28HC291L-55LI AT28HC291L-55PI	24D3 28L 24P3	Industrial (-40° to 85°C)
			AT28HC291L-55DM AT28HC291L-55LM	24D3 28L	Military (-55° to 125°C)
			AT28HC291L-55DM/883 AT28HC291L-55LM/883	24D3 28L	Military/883 Class B, Fully Compliant (-55° to 125°C)

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Package Type	
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

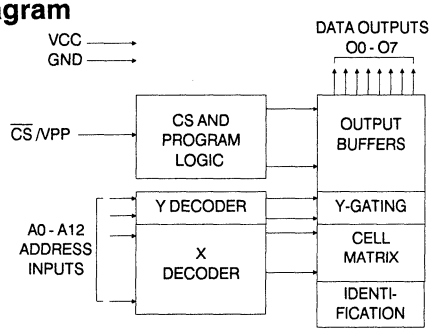
Features

- **Bipolar Speed**
  - **Read Access Time - 35ns**
- **Low Power CMOS Operation**
  - **35 mA max. Standby**
  - **75 mA Active at 10 MHz**
- **Direct Bipolar PROM Replacement**
- **High Output Drive Capability**
- **Reprogrammable - 4ms/byte (typical)**
  - **Tested 100% for Programmability**
- **JEDEC Approved Byte-Wide Pinout**
  - **300 mil, 600 mil, DIP, or LCC packages**
- **CMOS and TTL Compatible Inputs and Outputs**
- **High Reliability Latch-Up Resistant CMOS Technology**
- **Integrated Product Identification Code**
- **Full Military, Commercial and Industrial Temperature Ranges**

64K (8K x 8) UV Erasable CMOS PROM

5

Block Diagram



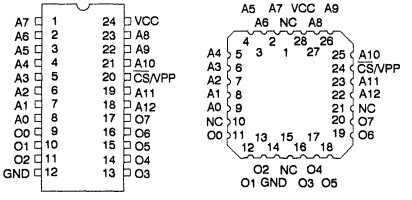
Description

The AT27HC641/642 chip family is a high-speed, low-power 65,536 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 8K x 8. All require only one 5V power supply in normal read mode operation. All bytes on the 641 and 642 parts can be accessed in less than 35ns, making these parts compatible with high performance systems, without penalizing bit density or power consumption.

The 640 series chips come in a choice of JEDEC-approved 24-pin DIPs or 28-pad LCC packages, providing a direct power saving CMOS upgrade for systems originally using Bipolar PROMs. The AT27HC641 is available in standard 600 mil cerdip or plastic (OTP) and LCC packages, while the AT27HC642 provides a space-saving 300 mil cerdip or plastic (OTP) package.

Pin Configurations

Pin Name	Function
A0-A12	Addresses
$\overline{CS}$/V_{PP}	Chip Select/V_{PP}
O0-O7	Outputs



Description (Continued)

Atmel's 1.5 micron, high speed CMOS technology provides optimum speed, low-power and high noise immunity. Power consumption on the AT27HC641 and AT27HC642 is typically only 50 mA in Active Mode and less than 20mA in Standby. The high speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology. EPROM reprogrammability, which is fully tested before shipment, provides inherently better programmability and reliability than one-time fusable PROMs.

With a storage capacity of 8K bytes, Atmel's 640 series parts allow firmware to be stored reliably and to be accessed at bipolar PROM speeds. All the 640 series parts have exceptional output drive capability - source 4 mA and sink 16 mA per output.

Atmel's 640 series chips also have additional features to ensure high quality and efficient production use. The fast programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of an Atmel 640 series chip is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
$\overline{CS}/V_{PP}$ Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 $W \cdot sec/cm^2$

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CS}/V_{PP}$	Ai	V_{CC}	Outputs
Read	V_{IL}	Ai	V_{CC}	D_{OUT}
Standby	V_{IH}	X(1)	V_{CC}	High Z
Fast Program(2)	V_{PP}	Ai	V_{CC}	D_{IN}
PGM Verify	V_{IL}	Ai	V_{CC}	D_{OUT}
Product Identification(4)	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A12 = V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC641 / AT27HC642				
		-35	-45	-55	-70	-90
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{PP1}	$\overline{CS}/V_{PP}$ (1) Read/Standby Current	$\overline{CS}/V_{PP}$ = -0.1V to V_{CC} + 1V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CS}/V_{PP}$ = V_{CC}-0.3 to V_{CC} + 1.0V	Com.		35	mA
			Ind.,Mil.		40	mA
		I_{SB2} (TTL) $\overline{CS}/V_{PP}$ = 2.0 to V_{CC} + 1.0V	Com.		35	mA
			Ind.,Mil.		40	mA
I_{CC}	V_{CC} Active Current	f = 10MHz, I_{OUT} = 0mA, $\overline{CS}/V_{PP}$ = V_{IL}	Com.		75	mA
			Ind.,Mil.		90	mA
I_{OS} (2)	Output Short Circuit Current	V_{OUT} = 0V			-100	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 16mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -4.0mA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before $\overline{CS}/V_{PP}$, and removed simultaneously or after $\overline{CS}/V_{PP}$.

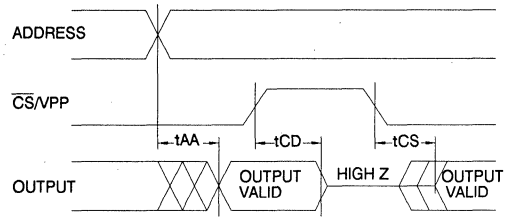
2. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec. This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

A.C. Characteristics for Read Operation

			AT27HC641 / AT27HC642										
			-35		-45		-55		-70		-90		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{AA} (4)	Address to Output Delay	Com.		35		45		55		70		90	ns
		Ind.,Mil				45		55		70		90	ns
t_{CS} (2,4)	$\overline{CS}/V_{PP}$ to Output Delay			25		30		35		45		55	ns
t_{CD} (3,4,5)	$\overline{CS}/V_{PP}$ to Output Float		0	25	0	30	0	35	0	40	0	45	ns

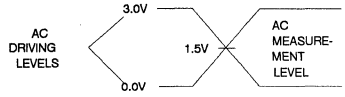
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



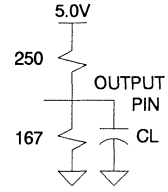
Notes:
1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.
2. Asserting $\overline{CS}/V_{PP}$ may be delayed up to $t_{AA} - t_{CS}$ after the address transition without impact on access time.
3. This parameter is only sampled and is not 100% tested.
4. C_L = 30pF, add 10ns for C_L = 100pF.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns (10% to 90%)

Output Test Load



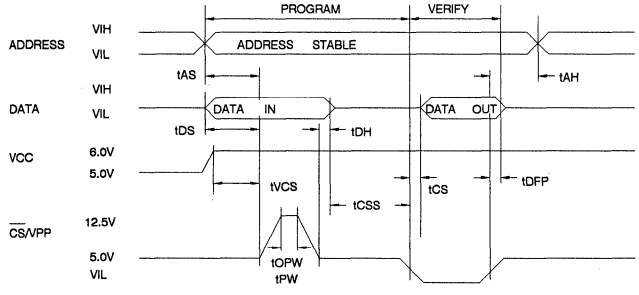
Note: C_L=30pF including jig capacitance.

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing References are 0.0V for V_{IL} and 3.0V for V_{IH}.
2. t_{CS} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, $\overline{CS}/V_{PP}$=12.5±0.5V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	I_{OL} = 16mA		.4	V
V_{OH}	Output High Volt.	I_{OH} = -4.0mA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			80	mA
I_{PP2}	$\overline{CS}/V_{PP}$ Supply Current	$\overline{CS}/V_{PP}=V_{PP}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, $\overline{CS}/V_{PP}$=12.5±0.5V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CSS}	$\overline{CS}/V_{PP}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CS}/V_{PP}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CS}/V_{PP}$ Initial Program Pulse Width	(Note 3)	0.95	1.05	ms
t_{OPW}	$\overline{CS}/V_{PP}$ Overprogram Pulse Width	(Note 4)	2.85	78.75	ms
t_{CS}	Data Valid from $\overline{CS}/V_{PP}$			70	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 5ns
Input Pulse Levels ..... 0.0V to 3.0V
Input Timing Reference Level 1.5V
Output Timing Reference Level 1.5V

Notes:

1. V_{CC} must be applied simultaneously or before $\overline{CS}/V_{PP}$ and removed simultaneously or after $\overline{CS}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Initial Program Pulse width tolerance is 1msec±5%.
4. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

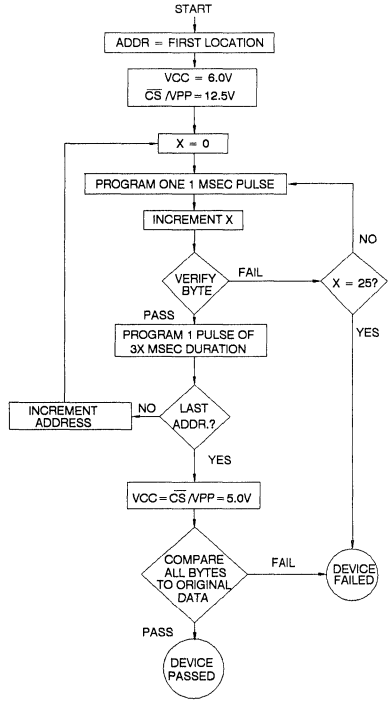
Atmel's 27HC641/2 Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	1	1F
Device Type	1	0	0	0	1	0	0	0	0	10

Fast Programming Algorithm

Two 12.5V $\overline{CS}/V_{PP}$ pulse widths are used to program; initial and overprogram. Ai are set to address the desired byte. V_{CC} is raised to 6.0V. The first $\overline{CS}/V_{PP}$ pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{CS}/V_{PP}$ pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then V_{CC} is lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	75	35	AT27HC641-35DC AT27HC642-35DC AT27HC641-35LC	24DW6 24DW3 28LW	Commercial (0°C to 70°C)
45	75	35	AT27HC641-45DC AT27HC642-45DC AT27HC641-45LC	24DW6 24DW3 28LW	Commercial (0°C to 70°C)
45	90	40	AT27HC641-45DI AT27HC642-45DI AT27HC641-45LI	24DW6 24DW3 28LW	Industrial (-40°C to 85°C)
			AT27HC641-45DM AT27HC642-45DM AT27HC641-45LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641-45DM/883 AT27HC642-45DM/883 AT27HC641-45LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
55	75	35	AT27HC641-55DC AT27HC642-55DC AT27HC641-55LC AT27HC641-55PC AT27HC642-55PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
55	90	40	AT27HC641-55DI AT27HC642-55DI AT27HC641-55LI AT27HC641-55PI AT27HC642-55PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641-55DM AT27HC642-55DM AT27HC641-55LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641-55DM/883 AT27HC642-55DM/883 AT27HC641-55LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	75	35	AT27HC641-70DC AT27HC642-70DC AT27HC641-70LC AT27HC641-70PC AT27HC642-70PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
70	90	40	AT27HC641-70DI AT27HC642-70DI AT27HC641-70LI AT27HC641-70PI AT27HC642-70PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641-70DM AT27HC642-70DM AT27HC641-70LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	90	40	AT27HC641-70DM/883 AT27HC642-70DM/883 AT27HC641-70LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	75	35	AT27HC641-90DC AT27HC642-90DC AT27HC641-90LC AT27HC641-90PC AT27HC642-90PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
90	90	40	AT27HC641-90DI AT27HC642-90DI AT27HC641-90LI AT27HC641-90PI AT27HC642-90PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641-90DM AT27HC642-90DM AT27HC641-90LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641-90DM/883 AT27HC642-90DM/883 AT27HC641-90LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
45	90	40	5962-87515 01 JX 5962-87515 01 KX 5962-87515 01 LX 5962-87515 01 3X	24DW6 24FW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
55	90	40	5962-87515 02 JX 5962-87515 02 KX 5962-87515 02 LX 5962-87515 02 3X	24DW6 24FW 24DW3 24LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	90	40	5962-87515 03 JX 5962-87515 03 KX 5962-87515 03 LX 5962-87515 03 3X	24DW6 24FW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	90	40	5962-87515 04 JX 5962-87515 04 KX 5962-87515 04 LX 5962-87515 04 3X	24DW6 24FW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24DW6	24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24FW	24 Lead, Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

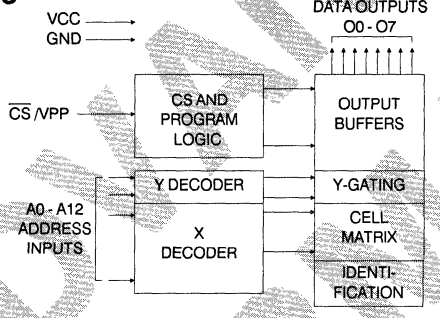
- **Bipolar Speed**
  - **Read Access Time - 35ns**
- **Low Power CMOS Operation**
  - **20 mA max. Standby**
  - **35 mA max. Active at 10 MHz**
- **Direct Bipolar PROM Replacement**
- **High Output Drive Capability**
- **Reprogrammable - 100μs/byte (typical)**
  - **Tested 100% for Programmability**
- **JEDEC Approved Byte-Wide Pinout**
  - **300 mil DIP, 600 mil DIP and LCC packages**
- **CMOS and TTL Compatible Inputs and Outputs**
- **High Reliability Latch-Up Resistant CMOS Technology**
- **Integrated Product Identification Code**
- **Full Military, Industrial and Commercial Temperature Ranges**
- **Fully Compatible with AT27HC641/2**

64K (8K x 8) UV Erasable CMOS PROM

5

Advance Information

Block Diagram



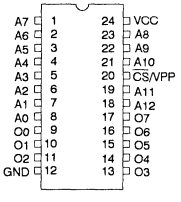
Description

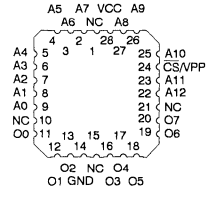
The AT27HC641R/642R chip family is a high-speed, low-power 65,536 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 8K x 8 bits. All devices require only one 5V power supply in normal read mode operation. All bytes on the 641R and 642R parts can be accessed in less than 35ns, making these parts ideal for high-performance systems without penalizing bit density or power consumption.

The 640R series of devices come in a choice of JEDEC-approved 24-pin DIP or 28 pad LCC packages, providing a direct power saving CMOS upgrade for systems originally using Bipolar PROMs. The AT27HC641R is available in a standard 600 mil cerdip or one-time programmable plastic "blank" (OTP) package, and LCC package, while the AT27HC642R is available in a space-saving 300 mil cerdip or plastic "blank" (OTP) package.

Pin Configurations

Pin Name	Function
A0-A12	Addresses
$\overline{CS}$/V_{PP}	Chip Select/V_{PP}
O0-O7	Outputs





Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	35	20	AT27HC641R-35DC AT27HC642R-35DC AT27HC641R-35LC	24DW6 24DW3 28LW	Commercial (0°C to 70°C)
45	35	20	AT27HC641R-45DC AT27HC642R-45DC AT27HC641R-45LC	24DW6 24DW3 28LW	Commercial (0°C to 70°C)
45	45	30	AT27HC641R-45DI AT27HC642R-45DI AT27HC641R-45LI	24DW6 24DW3 28LW	Industrial (-40°C to 85°C)
			AT27HC641R-45DM AT27HC642R-45DM AT27HC641R-45LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-45DM/883 AT27HC642R-45DM/883 AT27HC641R-45LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
55	35	20	AT27HC641R-55DC AT27HC642R-55DC AT27HC641R-55LC AT27HC641R-55PC AT27HC642R-55PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
55	45	30	AT27HC641R-55DI AT27HC642R-55DI AT27HC641R-55LI AT27HC641R-55PI AT27HC642R-55PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-55DM AT27HC642R-55DM AT27HC641R-55LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-55DM/883 AT27HC642R-55DM/883 AT27HC641R-55LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	35	20	AT27HC641R-70DC AT27HC642R-70DC AT27HC641R-70LC AT27HC641R-70PC AT27HC642R-70PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
70	45	30	AT27HC641R-70DI AT27HC642R-70DI AT27HC641R-70LI AT27HC641R-70PI AT27HC642R-70PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-70DM AT27HC642R-70DM AT27HC641R-70LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	45	30	AT27HC641R-70DM/883 AT27HC642R-70DM/883 AT27HC641R-70LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	35	20	AT27HC641R-90DC AT27HC642R-90DC AT27HC641R-90LC AT27HC641R-90PC AT27HC642R-90PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
90	45	30	AT27HC641R-90DI AT27HC642R-90DI AT27HC641R-90LI AT27HC641R-90PI AT27HC642R-90PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-90DM AT27HC642R-90DM AT27HC641R-90LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-90DM/883 AT27HC642R-90DM/883 AT27HC641R-90LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

5

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24DW6	24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24FW	24 Lead, Windowed, Ceramic Bottom-Brazed Flat Package (FlatPack)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

ATMEL

CONTENTS

Section 6

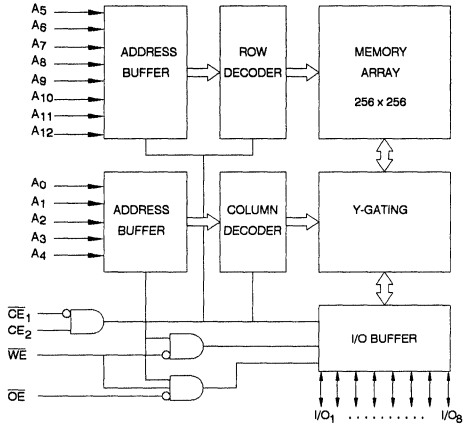
CMOS SRAMs

Features

- **Fast Read Access Time - 100ns**
- **Low Power**
  - **35mA Maximum (Active)**
  - **100μA Maximum (Standby)**
- **2V Data Retention**
- **Fully Static: No Clock Required**
- **Three Control Inputs ($\overline{CE}_1$, CE_2, and $\overline{OE}$)**
- **TTL Compatible Inputs and Outputs**
- **5V ± 10% Supply**
- **28 Lead Dual In-line and Surface Mount Packages**
- **JEDEC Pinout**
- **Commercial and Industrial Temperature Ranges**

64K (8K x 8) CMOS SRAM

Block Diagram



Description

The AT3864L is a high performance CMOS static Random Access Memory. Its 64K of memory is organized as 8192 words by 8 bits. Manufactured with an advanced CMOS technology, the AT3864L offers access times down to 100ns with power dissipation of under 200mW. When the AT3864L is deselected, the standby current is just 100μA. In addition, the AT3864L offers a data retention capability of only 100μW power dissipation when operated on a 2V power supply.

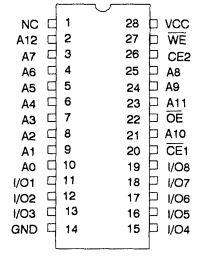
The AT3864L powers down to the standby mode when deselected ($\overline{CE}_1$ is HIGH or CE_2 is LOW). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE}_1$ is LOW and CE_2 is HIGH), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT3864L is completely TTL compatible and requires a single 5V power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

PIN NAMES

A_0-A_{12}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE}_1$, CE_2	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground
NC	No Connect



Device Operation

READ: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the 8 bits of data stored at the memory location determined by the address input (pins A_0 through A_{12}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW, the 8 bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{12}).

DATA RETENTION: When the chip is in standby mode, V_{CC} can be reduced to as low as 2 volts without impacting data integrity. Power dissipation will be reduced to 100 µW maximum.

Operating Modes

MODE\PIN	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	H	L	H	D_{OUT}
Write	L	H	X[1]	L	D_{IN}
$Standby_1$	H	X	X	X	High Z
$Standby_2$	X	L	X	X	High Z
Output Disable	X	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

Absolute Maximum Ratings*

Temperature Under Bias ..... -40° C to 85° C

Storage Temperature ..... -55° C to 125° C

All Input Voltages
(including NC Pins)
with Respect to Ground ..... -0.3 V to V_{CC} + 0.3V

All Output Voltages
with Respect to Ground ..... -0.3V to V_{CC} + 0.3V

Maximum Supply Voltage ..... + 7.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Conditions

		AT3864L-10	AT3864L-12	AT3864L-15
Operating Temperature (Case)	Commercial	0°C to 70°C	0°C to 70°C	0°C to 70°C
	Industrial	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics

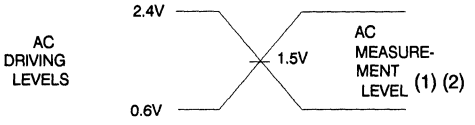
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = 0 to V_{CC}	-1.0		1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE_1}$ = 2.2V to V_{CC} + 0.3V or CE_2 = -0.3V to 0.8V or $\overline{OE}$ = 2.2V to V_{CC} + 0.3V or $\overline{WE}$ = -0.3V to 0.8V $V_{I/O}$ = 0 to V_{CC}	-1.0		1.0	µA
I_{SB1}	Standby Current (CMOS)	$CE_2 \le 0.2V$ or $\overline{CE_1} \ge V_{CC}$ - 0.2V, $CE_2 \ge V_{CC}$ - 0.2V or $CE_2 \le 0.2V$ V_{IN} = 0 to V_{CC}		2	100	µA
I_{SB2}	Standby Current (TTL)	CE_2 = -0.3V to 0.8V or $\overline{CE_1}$ = 2.2V to V_{CC} + 0.3V, V_{IN} = 0 to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE_1}$ = -0.3V to 0.8V, CE_2 = 2.2V to V_{CC} + 0.3V, I_{OUT} = 0mA, min cycle		20	35	mA
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.2V		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4			V

Pin Capacitance (f = 1MHz T = 25°C) [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V		6	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		6	10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



Notes: 1. Input rise and fall time 5ns.
2. Output load: 1TTL gate + 100pF.

6

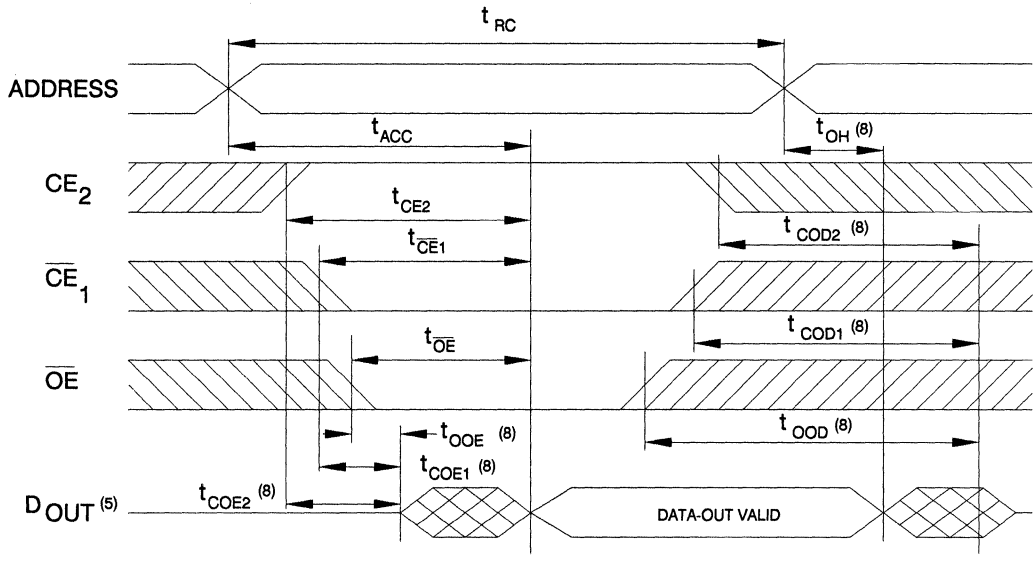
A.C. Characteristics for Read

		AT3864L-10		AT3864L-12		AT3864L-15		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
t_{RC}	Read Cycle Time	100		120		150		ns
t_{ACC}	Address Access Time		100		120		150	ns
$t_{\overline{CE}1}$, t_{CE2}	$\overline{CE}_1$, CE_2 Access Time		100		120		150	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		50		60		70	ns
t_{OH}	Output Hold Time	15		15		15		ns
$t_{COE1,2}$	$\overline{CE}_1$, CE_2 Output Enable Time	10		10		10		ns
t_{OOE}	$\overline{OE}$ Output Enable Time	5		5		5		ns
$t_{COD1,2}$	$\overline{CE}_1$, CE_2 Output Disable Time		45		45		60	ns
t_{OOD}	$\overline{OE}$ Output Disable Time		40		40		50	ns

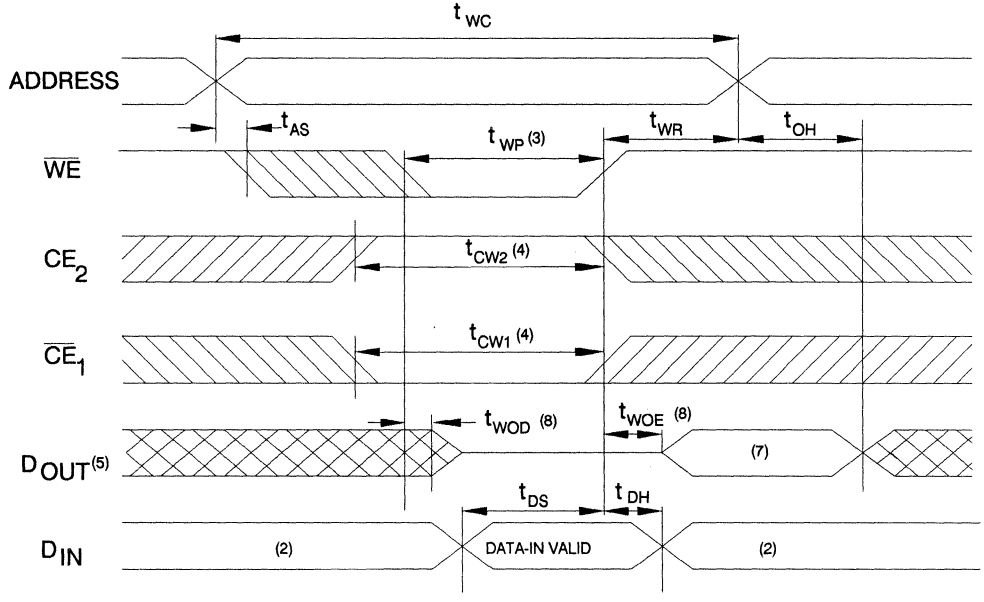
A.C. Characteristics for Write

		AT3864L-10		AT3864L-12		AT3864L-15		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
t_{WC}	Write Cycle Time	100		120		150		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	60		70		90		ns
$t_{CW1,2}$	$\overline{CE}_1$, CE_2 Setup Time	80		80		90		ns
t_{WR}	Write Recovery Time	0		0		0		ns
$t_{WR1,2}$	$\overline{CE}_1$, CE_2 Write Recovery Time	0		0		0		ns
t_{DS}	Data Setup Time	40		50		60		ns
t_{DH}	Data Hold Time	0		0		0		ns
$t_{DH1,2}$	$\overline{CE}_1$, CE_2 Data Hold Time	0		0		0		ns
t_{WOE}	$\overline{WE}$ Output Enable Time	5		5		5		ns
t_{WOD}	$\overline{WE}$ Output Disable Time		40		40		50	ns

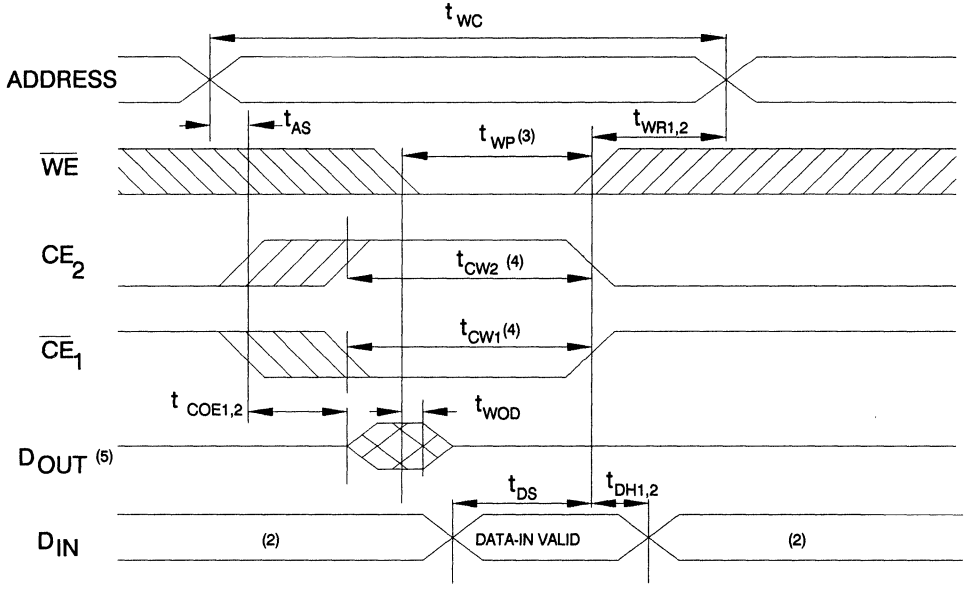
A.C. Waveforms for Read Cycle[1]



A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write)[6]



A.C. Waveforms for Write Cycle 2 ($\overline{CE}$ Write)[6]



Notes:

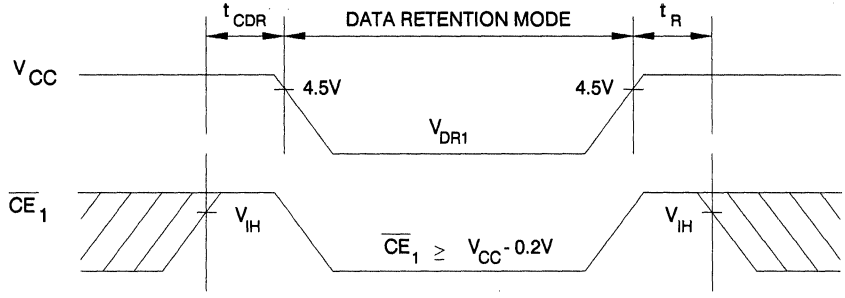
1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE}_1$, CE_2 and $\overline{WE}$ are all active at the same time.
   A Write begins at the latest transition among $\overline{CE}_1$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE}_1$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE}_1$ going LOW or CE_2 going HIGH to the end of Write.
5. If $\overline{OE}$ or $\overline{CE}_1$ is HIGH, or CE_2 or $\overline{WE}$ is LOW, D_{OUT} goes to a HIGH impedance state.
6. During a write cycle, $\overline{OE} = V_{IH}$ or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.
8. Parameter is sampled and not 100% tested.

Data Retention Characteristics

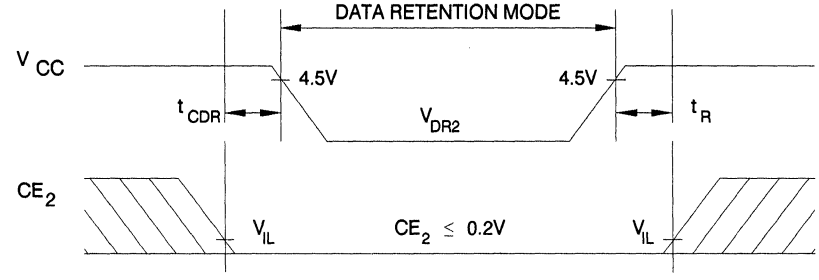
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Power Supply Voltage	VDR1	$\overline{CE_1} \geq V_{CC} - 0.2V$ $CE_2 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$	2.0		5.5	V
	V_{DR2}	$CE_2 \leq 0.2V$	2.0		5.5	
Data Retention Current	I_{CCDR1}	$V_{CC} = 3.0V$ $\overline{CE_1} \geq V_{CC} - 0.2V$ $CE_2 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$		1	50	µA
	I_{CCDR2}	$V_{CC} = 3.0V$, $CE_2 \leq 0.2V$		1	50	µA
Chip Enable Setup Time	t_{CDR}		0			ns
Chip Enable Hold Time	t_R		t_{RC}(1)			ns

Note: 1. t_{RC} = Read Cycle Time

Data Retention Waveform 1 ($\overline{CE}_1$ Control)



Data Retention Waveform 2 (CE_2 Control)



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	35	0.1	AT3864L-10PC AT3864L-10RC	28P6 28R	Commercial (0° to 70°C)
			AT3864L-10PI AT3864L-10RI	28P6 28R	Industrial (-40° to 85°C)
120	35	0.1	AT3864L-12PC AT3864L-12RC	28P6 28R	Commercial (0° to 70°C)
			AT3864L-12PI AT3864L-12RI	28P6 28R	Industrial (-40° to 85°C)
150	35	0.1	AT3864L-15PC AT3864L-15RC	28P6 28R	Commercial (0° to 70°C)
			AT3864L-15PI AT3864L-15RI	28P6 28R	Industrial (-40° to 85°C)

Package Type	
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28R	28 Lead, 0.330" Wide Plastic Gull Wing Small Outline (SOIC)

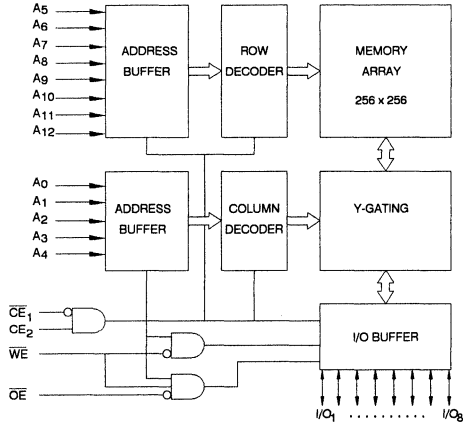
Features

- **Fast Read Access Time - 150ns**
- **Low Power**
  - **40mA Maximum (Active)**
  - **1mA Maximum (Standby)**
- **2V Data Retention**
- **Fully Static: No Clock Required**
- **Three Control Inputs ($\overline{CE}_1$, CE_2, and $\overline{OE}$)**
- **TTL Compatible Inputs and Outputs**
- **5V ± 10% Supply**
- **28 Lead Dual In-line**
- **JEDEC Pinout**
- **Full Military Temperature Range**

64K (8K x 8) CMOS SRAM

6

Block Diagram



Description

The AT3864L-15DMB is a high performance CMOS static Random Access Memory. Its 64K of memory is organized as 8192 words by 8 bits. Manufactured with an advanced CMOS technology, the AT3864L-15DMB offers access times down to 150ns with power dissipation of 220mW maximum. When the AT3864L-15DMB is deselected, the standby current is just 1mA. In addition, the AT3864L-15DMB offers a data retention capability of only 800μW power dissipation when operated on a 2V power supply.

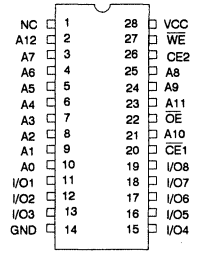
The AT3864L-15DMB powers down to the standby mode when deselected ($\overline{CE}_1$ is HIGH or CE_2 is LOW). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE}_1$ is LOW and CE_2 is HIGH), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT3864L-15DMB is completely TTL compatible and requires a single 5V power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

PIN NAMES

A_0-A_{12}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE}_1$, CE_2	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground
NC	No Connect



Device Operation

READ: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the 8 bits of data stored at the memory location determined by the address input (pins A_0 through A_{12}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW, the 8 bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{12}).

DATA RETENTION: When the chip is in standby mode, V_{CC} can be reduced to as low as 2 volts without impacting data integrity. Power dissipation will be reduced to 800 µW maximum.

Operating Modes

MODE\PIN	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	H	L	H	D_{OUT}
Write	L	H	X[1]	L	D_{IN}
$Standby_1$	H	X	X	X	High Z
$Standby_2$	X	L	X	X	High Z
Output Disable	X	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

Absolute Maximum Ratings*

Temperature Under Bias ..... -55° C to 150° C

Storage Temperature ..... -65° C to 150° C

All Input Voltages
(including NC Pins)
with Respect to Ground ..... -0.3 V to V_{CC} + 0.3V

All Output Voltages
with Respect to Ground ..... -0.3V to V_{CC} + 0.3V

Maximum Supply Voltage ..... + 7.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Conditions

		AT3864L-15
Operating Temperature (Case)	Military	-55°C to 125°C
VCC Power Supply		5V ± 10%

D.C. and Operating Characteristics

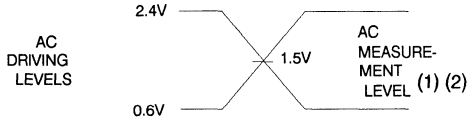
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = 0 to V_{CC}	-1.0		1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE_1}$ = 2.2V to V_{CC} + 0.3V or CE_2 = -0.3V to 0.8V or $\overline{OE}$ = 2.2V to V_{CC} + 0.3V or $\overline{WE}$ = -0.3V to 0.8V $V_{I/O}$ = 0 to V_{CC}	-1.0		1.0	µA
I_{SB1}	Standby Current (CMOS)	$CE_2 \le 0.2V$ or $\overline{CE_1} \ge V_{CC}$ - 0.2V, $CE_2 \ge V_{CC}$ - 0.2V or $CE_2 \le 0.2V$ V_{IN} = 0 to V_{CC}			1	mA
I_{SB2}	Standby Current (TTL)	CE_2 = -0.3V to 0.8V or $\overline{CE_1}$ = 2.2V to V_{CC} + 0.3V, V_{IN} = 0 to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE_1}$ = -0.3V to 0.8V, CE_2 = 2.2V to V_{CC} + 0.3V, I_{OUT} = 0mA, min cycle		20	40	mA
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.2V		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4			V

Pin Capacitance (f = 1MHz T = 25°C) [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V		6	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		6	10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



Notes: 1. Input rise and fall time 5ns.
2. Output load: 1TTL gate + 100pF.

6

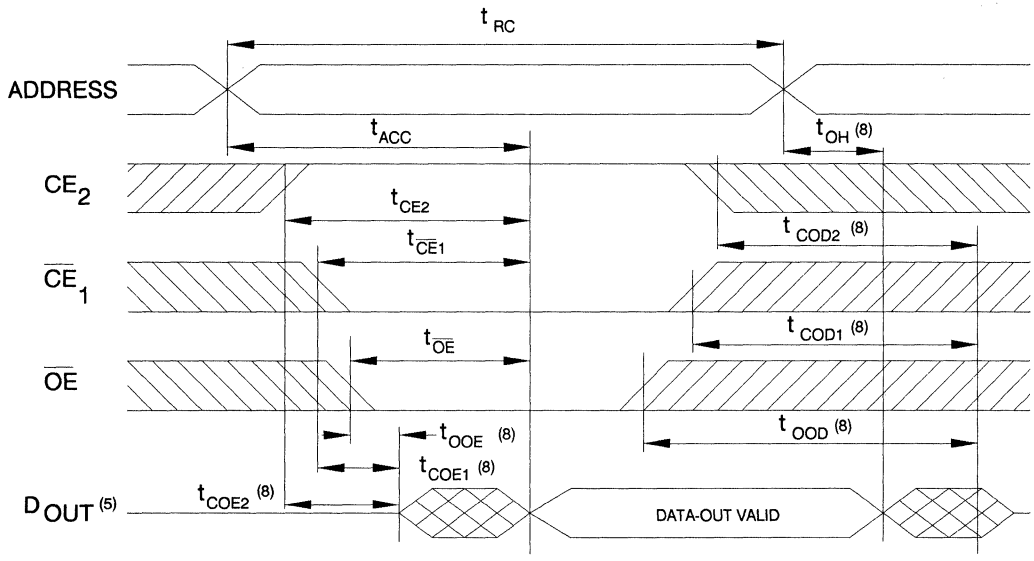
A.C. Characteristics for Read

		AT3864L-15		
Symbol	Parameter	Min	Max	Unit
t_{RC}	Read Cycle Time	150		ns
t_{ACC}	Address Access Time		150	ns
$t_{\overline{CE}1}$, t_{CE2}	$\overline{CE}_1$, CE_2 Access Time		150	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		70	ns
t_{OH}	Output Hold Time	15		ns
$t_{COE1,2}$	$\overline{CE}_1$, CE_2 Output Enable Time	10		ns
t_{OOE}	$\overline{OE}$ Output Enable Time	5		ns
$t_{COD1,2}$	$\overline{CE}_1$, CE_2 Output Disable Time		60	ns
t_{OOD}	$\overline{OE}$ Output Disable Time		50	ns

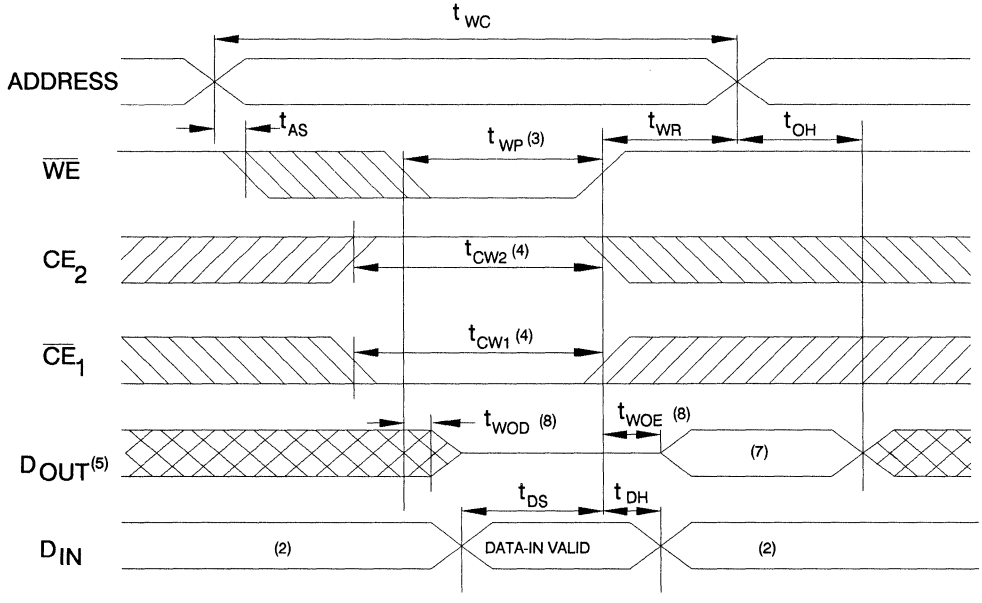
A.C. Characteristics for Write

		AT3864L-15		
Symbol	Parameter	Min	Max	Unit
t_{WC}	Write Cycle Time	150		ns
t_{AS}	Address Setup Time	0		ns
t_{WP}	Write Pulse Width	90		ns
$t_{CW1,2}$	$\overline{CE}_1$, CE_2 Setup Time	90		ns
t_{WR}	Write Recovery Time	0		ns
$t_{WR1,2}$	$\overline{CE}_1$, CE_2 Write Recovery Time	0		ns
t_{DS}	Data Setup Time	60		ns
t_{DH}	Data Hold Time	0		ns
$t_{DH1,2}$	$\overline{CE}_1$, CE_2 Data Hold Time	0		ns
t_{WOE}	$\overline{WE}$ Output Enable Time	5		ns
t_{WOD}	$\overline{WE}$ Output Disable Time		50	ns

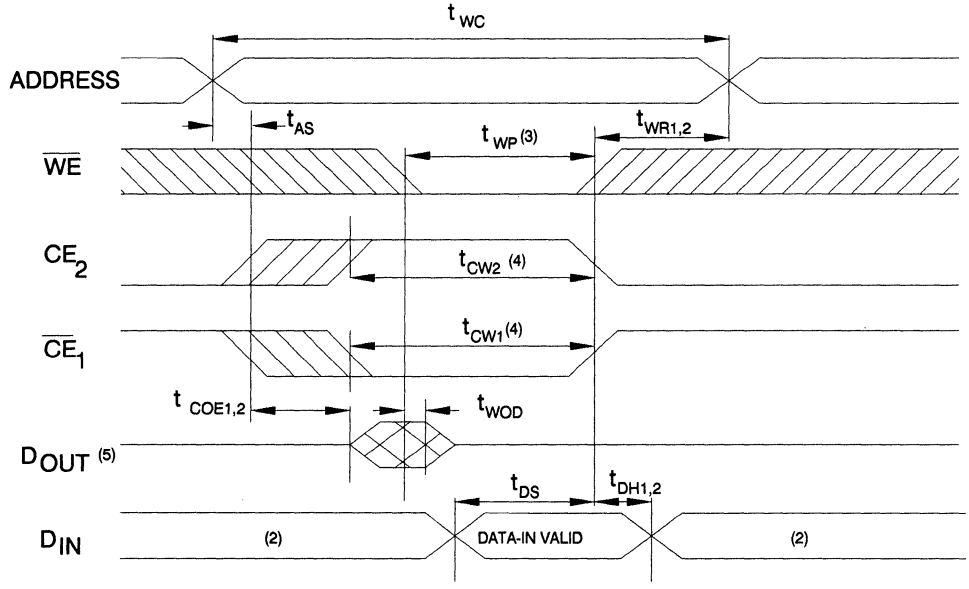
A.C. Waveforms for Read Cycle[1]



A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write)[6]



A.C. Waveforms for Write Cycle 2 ($\overline{CE}$ Write)[6]



Notes:

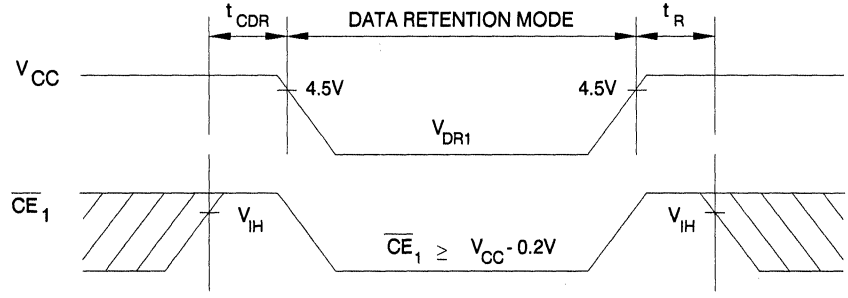
1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW.
   A Write begins at the latest transition among $\overline{CE_1}$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE_1}$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE_1}$ going LOW or CE_2 going HIGH to the end of Write.
5. If $\overline{OE}$ or $\overline{CE_1}$ is HIGH, or CE_2 or $\overline{WE}$ is LOW, D_{OUT} goes to a HIGH impedance state.
6. During a write cycle, $\overline{OE}$ is V_{IH} or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.
8. Parameter is sampled and not 100% tested.

Data Retention Characteristics

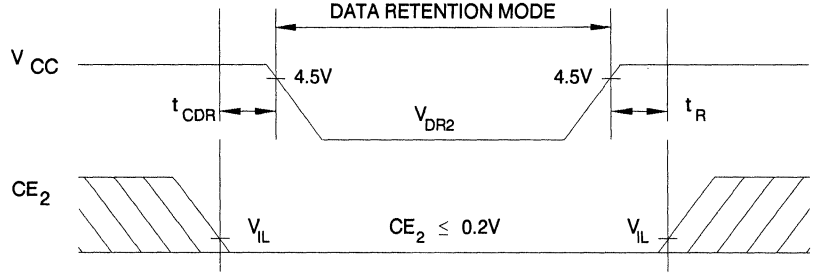
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Power Supply Voltage	V_{DR1}	$\overline{CE_1} \geq V_{CC}$ - 0.2V $CE_2 \geq V_{CC}$ - 0.2V or $CE_2 \leq 0.2V$	2.0		5.5	V
	V_{DR2}	$CE_2 \leq 0.2V$	2.0		5.5	
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V $\overline{CE_1} \geq V_{CC}$ - 0.2V $CE_2 \geq V_{CC}$-0.2V or $CE_2 \leq 0.2V$		1	400	µA
	I_{CCDR2}	V_{CC} = 3.0V, $CE_2 \leq 0.2V$		1	400	µA
Chip Enable Setup Time	t_{CDR}		0			ns
Chip Enable Hold Time	t_R		t_{RC}(1)			ns

Note: 1. t_{RC} = Read Cycle Time

Data Retention Waveform 1 ($\overline{CE}_1$ Control)



Data Retention Waveform 2 (CE_2 Control)



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	1.0	AT3864L-15DMB	28D6	Military (-55° to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)

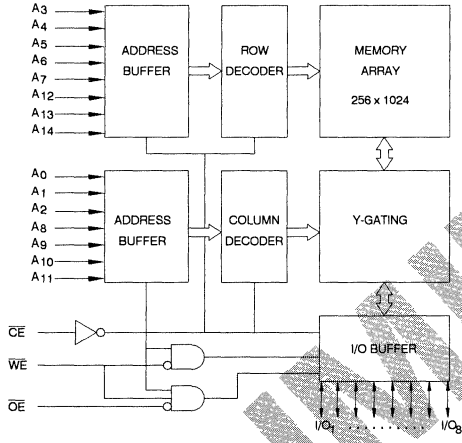
Features

- Fast Read Access Time - 20ns
- Low Power
  - 120mA Maximum (Active)
  - 1mA Maximum (Standby)
  - 500µA Maximum (2V Data Retention)
- Fully Static: No Clock Required
- Two Control Inputs ($\overline{CE}$ and $\overline{OE}$)
- TTL Compatible Inputs and Outputs
- 5V ± 10% Supply
- 28 Lead Dual In-line and Surface Mount Packages
- JEDEC Pinout
- Commercial, Industrial and Military Temperature Ranges

256K (32K x 8) CMOS SRAM

Preliminary

Block Diagram



Description

The AT38256 is a high performance CMOS static Random Access Memory. Its 256K of memory is organized as 32768 words by 8 bits. Manufactured with an advanced CMOS technology, the AT38256 offers access times down to 20ns with power dissipation of 660mW. When the AT38256 is deselected, the standby current is just 1mA. In addition, the AT38256 offers a data retention capability of only 1mW power dissipation when operated on a 2V power supply.

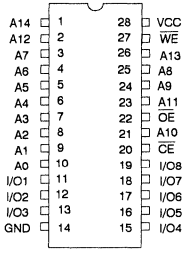
The AT38256 powers down to the standby mode when deselected ($\overline{CE}$ is HIGH). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE}$ is LOW), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT38256 is completely TTL compatible and requires a single 5V power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

For .300 DIP/.600 DIP/.300 SOJ

Pin Name	Function
A_0-A_{14}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground



Device Operation

READ: When $\overline{CE}$ is LOW, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the 8 bits of data stored at the memory location determined by the address input (pins A_0 through A_{14}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE}$ is LOW and $\overline{WE}$ is LOW, the 8 bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{14}).

DATA RETENTION: When the chip is in standby mode, V_{CC} can be reduced to as low as 2 volts without impacting data integrity. Power dissipation will be reduced to 1mW maximum.

Operating Modes

MODE\PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	D_{OUT}
Write	L	X(1)	L	D_{IN}
Standby (not selected)	H	X	X	High Z
Output Disable	L	H	H	High Z

Note: 1. X can be L (Low) or H (High)

Absolute Maximum Ratings*

Temperature Under Bias ..... -55° C to 125° C

Storage Temperature ..... -65° C to 150° C

All Input Voltages
with Respect to Ground ..... -0.3 V(1) to V_{CC} + 0.3V

All Output Voltages
with Respect to Ground ..... -0.3V(1) to V_{CC} + 0.3V

Maximum Supply Voltage ..... + 7.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum input voltages are -3.5V for pulse width less than 20 ns.

D.C. and A.C. Operating Conditions

		AT38256
Operating Temperature (Ambient)	Commercial	0°C to 70°C
	Industrial	-40°C to 85°C
	Military	-55°C to 125°C
V_{CC} Power Supply		5V ± 10%

D.C. and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = 0 to V_{CC}	-1.0		1.0	µA
I_{LO}	Output Leakage	$\overline{CE}$ = 2.2V to VCC + 0.3V or $\overline{OE}$ = 2.2V to V_{CC} + 0.3V or $\overline{WE}$ = -0.3V to 0.8V $V_{I/O}$ = 0 to V_{CC}	-1.0		1.0	µA
I_{SB1}	Standby Current (CMOS)	$\overline{CE}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ (V_{CC}-0.2V) or ≤ 0.2V			1	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = 2.2V to V_{CC} + 0.3V, V_{IN} = V_{IL} or V_{IH}			25	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE}$ = -0.3V to 0.8V, I_{OUT} = 0mA, min cycle			120	mA
V_{IL} (1)	Input Low Voltage		-0.3 (2)		0.8	V
V_{IH} (1)	Input High Voltage		2.2V		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0mA	2.4			V

Note: 1. These are voltages with respect to device GND.
2. V_{IL} = -3.0V for pulse width less than 20ns.

Pin Capacitance (f = 1MHz TA = 25°C) [1]

Symbol	Parameter	Conditions	Min	Max	Unit
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V		8	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		8	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Output Test Load

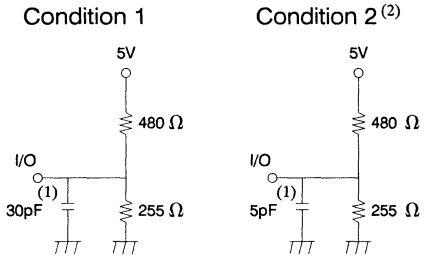


Figure 1

Item	Condition
Input pulse "High" level	V_{IH} = 3.0V
Input pulse "Low" level	V_{IL} = 0V
Input rise time	t_R = 5ns
Input fall time	t_F = 5ns
Input and output reference level	1.5V
Output load	See Figure 1

Notes: 1. Capacitance Load includes scope and jig capacitances
2. For t_{COE}, t_{OOE}, t_{COD}, t_{OOD}, t_{WOE}, t_{WOD}

6

A.C. Characteristics for Read

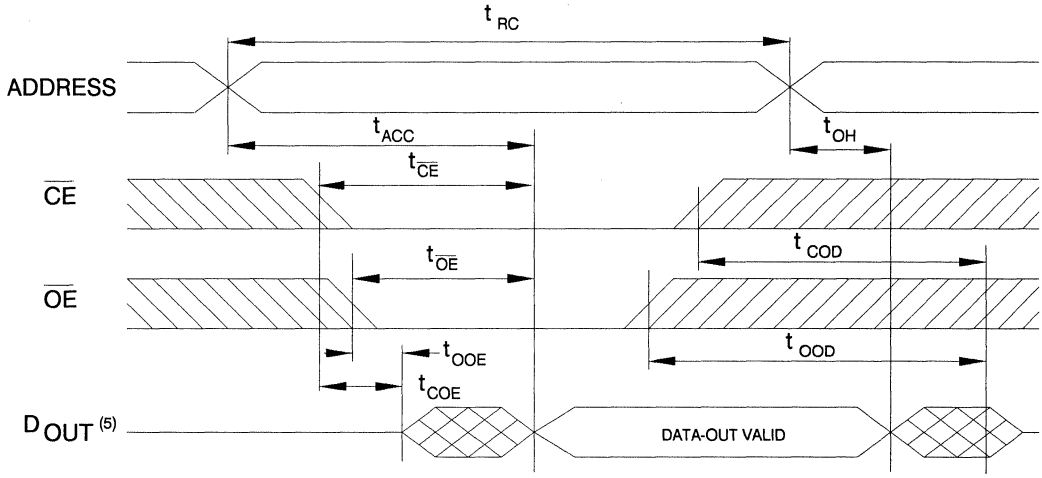
		AT38256-20		AT38256-25		AT38256-35		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
t_{RC}	Read Cycle Time	20		25		35		ns
t_{ACC}	Address Access Time		20		25		35	ns
$t_{\overline{CE}}$	$\overline{CE}$ Access Time		20		25		35	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		12		12		20	ns
t_{OH}	Output Hold Time	5		5		5		ns
t_{COE} (1)	$\overline{CE}$ Output Enable Time	5		5		5		ns
t_{OOE} (1)	$\overline{OE}$ Output Enable Time	0		0		0		ns
t_{COD} (1)	$\overline{CE}$ Output Disable Time		15		15		15	ns
t_{OOD} (1)	$\overline{OE}$ Output Disable Time		13		13		15	ns

A.C. Characteristics for Write

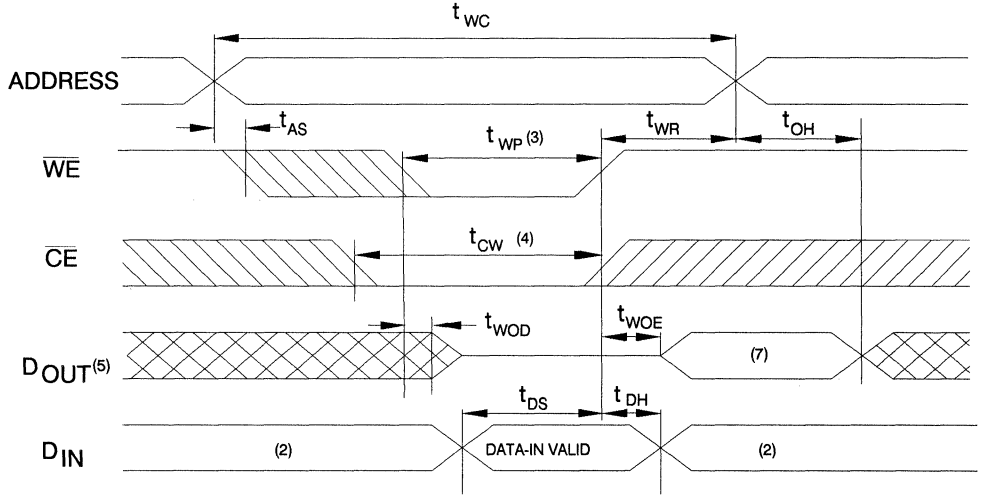
		AT38256-20		AT38256-25		AT38256-35		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
t_{WC}	Write Cycle Time	20		25		35		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	15		20		30		ns
t_{CW}	$\overline{CE}$ Setup Time	15		20		30		ns
t_{WR}	Write Recovery Time	2		2		2		ns
t_{DS}	Data Setup Time	12		12		15		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WOE} (1)	$\overline{WE}$ Output Enable Time	0		0		0		ns
t_{WOD} (1)	$\overline{WE}$ Output Disable Time		13		13		15	ns

Note: 1. Tansition is measured by ±500 mV from the normal state with the output test load circuit, condition 2. This parameter is sampled and is not 100% tested.

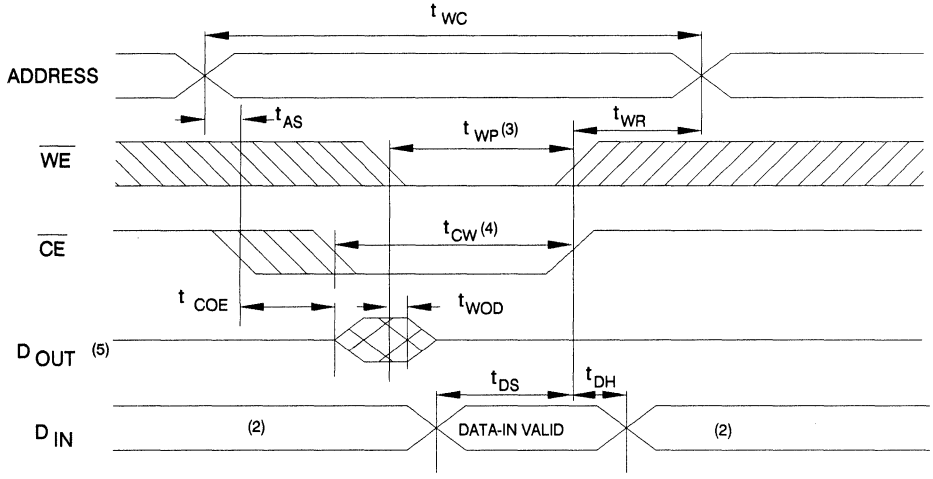
A.C. Waveforms for Read Cycle [1]



A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write) [6]



A.C. Waveforms for Write Cycle 2 ($\overline{CE}$ Write) [6]



Notes:

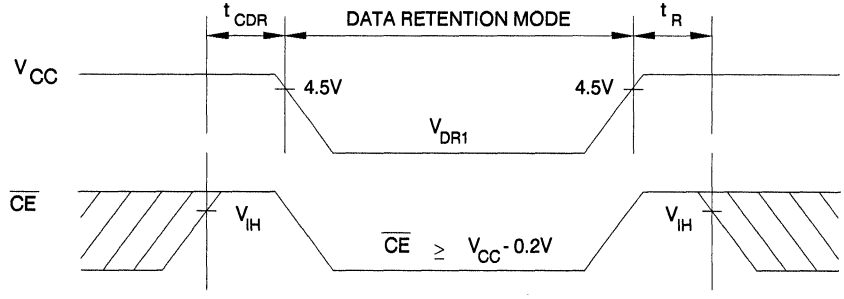
1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE}$ and $\overline{WE}$ are LOW at the same time.
   A Write begins at the latest transition among $\overline{CE}$ going LOW, and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE}$ going HIGH, and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE}$ going LOW or going HIGH to the end of Write.
5. If $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW, D_{OUT} goes to a high impedance state.
6. During a write cycle, $\overline{OE} = V_{IH}$ or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.

Data Retention Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Power Supply Voltage	VDR1	$\overline{CE} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{CCDR1}	$V_{CC} = 2.0V$ $\overline{CE} \geq V_{CC} - 0.2V$ and $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$			500	µA
	I_{CCDR2}	$V_{CC} = 3.0V$ and $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$			750	µA
Chip Enable Setup Time	t_{CDR}		0			ns
Chip Enable Hold Time	t_R		t_{RC} (1)			ns

Note: 1. t_{RC} = Read Cycle Time

Data Retention Waveform ($\overline{CE}$ Control)



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
20	120	1.0	AT38256-20NC AT38256-20XC	28P3 28X	Commercial (0° to 70°C)
			AT38256-20NI AT38256-20XI	28P3 28X	Industrial (-40° to 85°C)
25	120	1.0	AT38256-25PC AT38256-25NC AT38256-25XC	28P6 28P3 28X	Commercial (0° to 70°C)
			AT38256-25PI AT38256-25NI AT38256-25XI	28P6 28P3 28X	Industrial (-40° to 85°C)
			AT38256-25BM AT38256-25DM	28B 28D6	Military (-55° to 125°C)
35	120	1.0	AT38256-35PC AT38256-35NC AT38256-35XC	28P6 28P3 28X	Commercial (0° to 70°C)
			AT38256-35PI AT38256-35NI AT38256-35XI	28P6 28P3 28X	Industrial (-40° to 85°C)
			AT38256-35BM AT38256-35DM	28B 28D6	Military (-55° to 125°C)

6

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28B	28 Lead, 0.300" Wide, Ceramic Side Braze Dual Inline (Side Braze)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28P3	28 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
28X	28 Lead, 0.300" Wide, Plastic J-Leaded Small Outline (SOIC)

ATMEL

CONTENTS

Section 7

CMOS EPLDs

7

Features

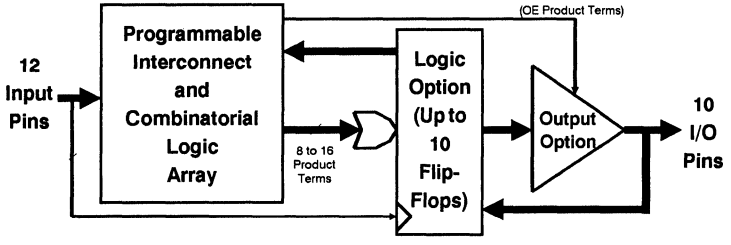
- **High Speed Programmable Logic Device**
  - **15 ns Max Propagation Delay**
  - **5V ± 10% Operation**
- **Low Power CMOS Operation**

Speed	"L"	-15	All
Temp	C/M	All	Others
Icc(mA)	12/15	90	55

- **CMOS and TTL Compatible Inputs and Outputs**
  - **10 μA Leakage Maximum**
- **Reprogrammable - Tested 100% for Programmability**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200mA Latchup Immunity**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Dual-In-Line and Surface Mount Packages**

High Speed UV Erasable Programmable Logic Device

Logic Diagram



Description

The AT22V10 and AT22V10L are CMOS high performance Erasable Programmable Logic Devices (EPLDs). Speeds down to 15 ns and power dissipation as low as 12 mA are offered. All speed ranges are specified over the full 5V ± 10% range. All pins offer a low ± 10 μA leakage.

The AT22V10L provides the optimum low power CMOS EPLD solution, with low DC power (8mA typical) and full CMOS output levels. The AT22V10L significantly reduces total system power and enhances system reliability.

Full CMOS output levels help reduce power in many other system components.

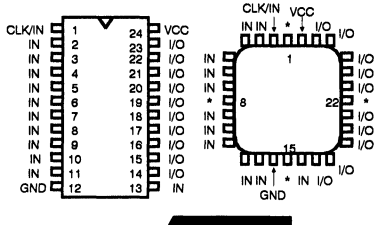
The AT22V10 and AT22V10L incorporate a variable product term architecture. Each output is allocated from 8 to 16 product terms, which allows highly complex logic functions to be realized.

Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all 10 registers. All registers are automatically cleared upon power up.

Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5V Supply



7

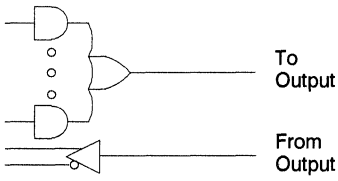
Absolute Maximum Ratings*

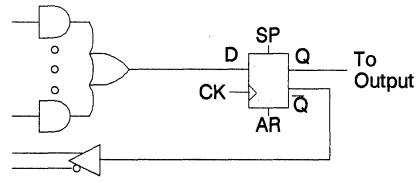
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 w•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

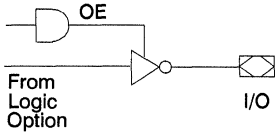
Note:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

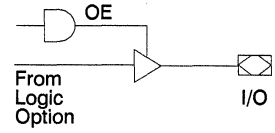
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial AT22V10/L -15, -20, -25, -35	Industrial AT22V10/L -15, -20, -25, -35	Military AT22V10/L -15(1), -20, -25, -30
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5V± 10%	5V± 10%	5V± 10%

Note: 1. Preliminary.

Operating Modes

Mode	24 DIP Pin / 28 JLCC Pin	1 / 2	5 / 6	8 / 10	13 / 16	I/O's	V_{CC}(24) / V_{CC}(28)
"EPLD"		X (1)	X	X	X	I/O	5V
Program		V_{PP}	X/V_H (2)	X	V_{PP}	D_{IN}	6V
PGM Verify		V_{PP}	X/V_H	X	V_{IL}	D_{OUT}	6V
PGM Inhibit		V_{PP}	X/V_H	X	V_{IH}	High Z	6V
Preload		X	X	V_H	X	D_{IN}	5V

Notes: 1. X can be V_{IL} or V_{IH}. 2. V_H = 11.0V to 14.0V

D.C. Characteristics

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V				10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND, Outputs Open	AT22V10-15			90	mA
			AT22V10-20,-25,-35[2]			55	mA
			22V10L[2]	Com.		12	mA
				Ind., Mil.		15	mA
I_{CC2}	Clocked Power Supply Current	f = 1MHz, V_{CC} = MAX, Outputs Open	22V10L[2]	Com.		15	mA
				Ind., Mil.		20	mA
I_{OS} [1]	Output Short Circuit Current	V_{OUT} = 0.5V				-90	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 16mA	Com.,Ind.		0.5	V
			I_{OL} = 12mA	Mil.		0.5	V
			I_{OL} = 24mA	Com.		0.8	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OH} = -100µA		V_{CC}-0.3		V
			I_{OH} = -4.0mA		2.4		V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec. This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

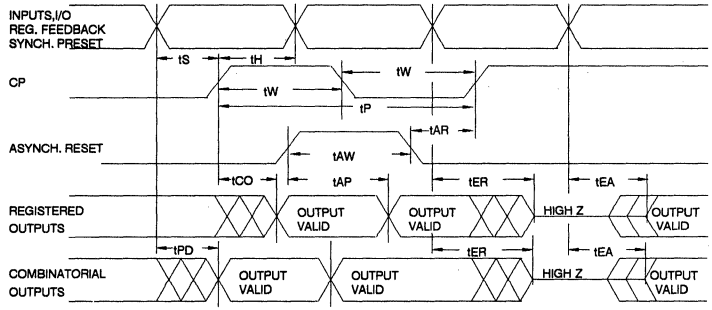
2. See I_{CC} vs. Frequency curves in the back of this data sheet.

7

A.C. Characteristics, Commercial and Industrial

		22V10/L-15			22V10/L-20			22V10/L-25			22V10/L-35			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		10	15		12	20		15	25		20	35	ns
t_{EA}	Input to Output Enable		10	15			20		15	25		20	35	ns
t_{ER}	Input to Output Disable		10	15			20		15	25		20	35	ns
t_{CF}	Clock to Feedback	0	1	2.5	0	4	8	0	5	10	0	10	15	ns
t_{CO}	Clock to Output	0	7	10	0	8	12	0	10	15	0	12	20	ns
t_S	Input or Feedback Setup Time	10	8		12	8		15	12		20	15		ns
t_H	Hold Time	0			0			0			0			ns
t_P	Clock Period	12			20			24			30			ns
t_W	Clock Width	6			10			12			15			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			50.0			41.6			33.3			25.0	MHz
	Internal Feedback $1/(t_S + t_{CF})$			80.0			50.0			40.0			28.5	MHz
	No Feedback $1/(t_P)$			83.3			50.0			41.6			33.3	MHz
t_{AW}	Asynchronous Reset Width	15	8		20	9		25	10		30	15		ns
t_{AR}	Asynchronous Reset Recovery Time	15	8		20	12		25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		12	20		15	22		18	25		20	30	ns

A.C. Waveforms [1]



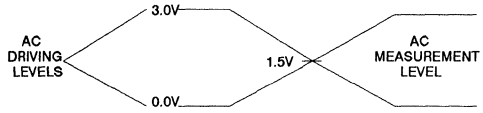
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

A.C. Characteristics, Military

Symbol	Parameter	AT22V10/L-15[1]			AT22V10/L-20			AT22V10/L-25			AT22V10/L-30			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		10	15		12	20		15	25		20	30	ns
t_{EA}	Input to Output Enable		10	15			20		15	25		20	30	ns
t_{ER}	Input to Output Disable		10	15			20		15	25		20	30	ns
t_{CF}	Clock to Feedback	0	1	2.5	0	4	8	0	5	10	0	10	15	ns
t_{CO}	Clock to Output	0	7	10	0	8	15	0	10	15	0	12	20	ns
t_{SF}	Feedback Setup Time	10	8		12	10		15	12		18	15		ns
t_S	Input Setup Time	10	8		17	14		18	15		20	15		ns
t_H	Hold Time	0			0			0			0			ns
t_P	Clock Period	12			20			24			30			ns
t_W	Clock Width	6			10			12			15			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			50.0			31.2			30.3			25.0	MHz
	Internal Feedback $1/(t_S + t_{CF})$			80.0			50.0			40.0			30.0	MHz
	No Feedback $1/(t_P)$			83.3			50.0			41.6			33.3	MHz
t_{AW}	Asynchronous Reset Width	15	8		20	9		25	10		30	15		ns
t_{AR}	Asynchronous Reset Recovery Time	15	8		20	12		25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		12	20		15	22		18	25		20	20	ns

Note: 1. Preliminary

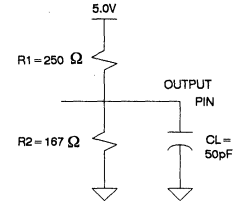
Input Test Waveforms and Measurement Levels



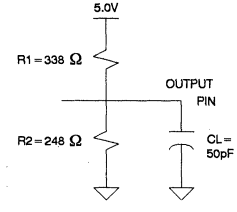
tR, tF < 5ns (10% to 90%)

Output Test Loads:

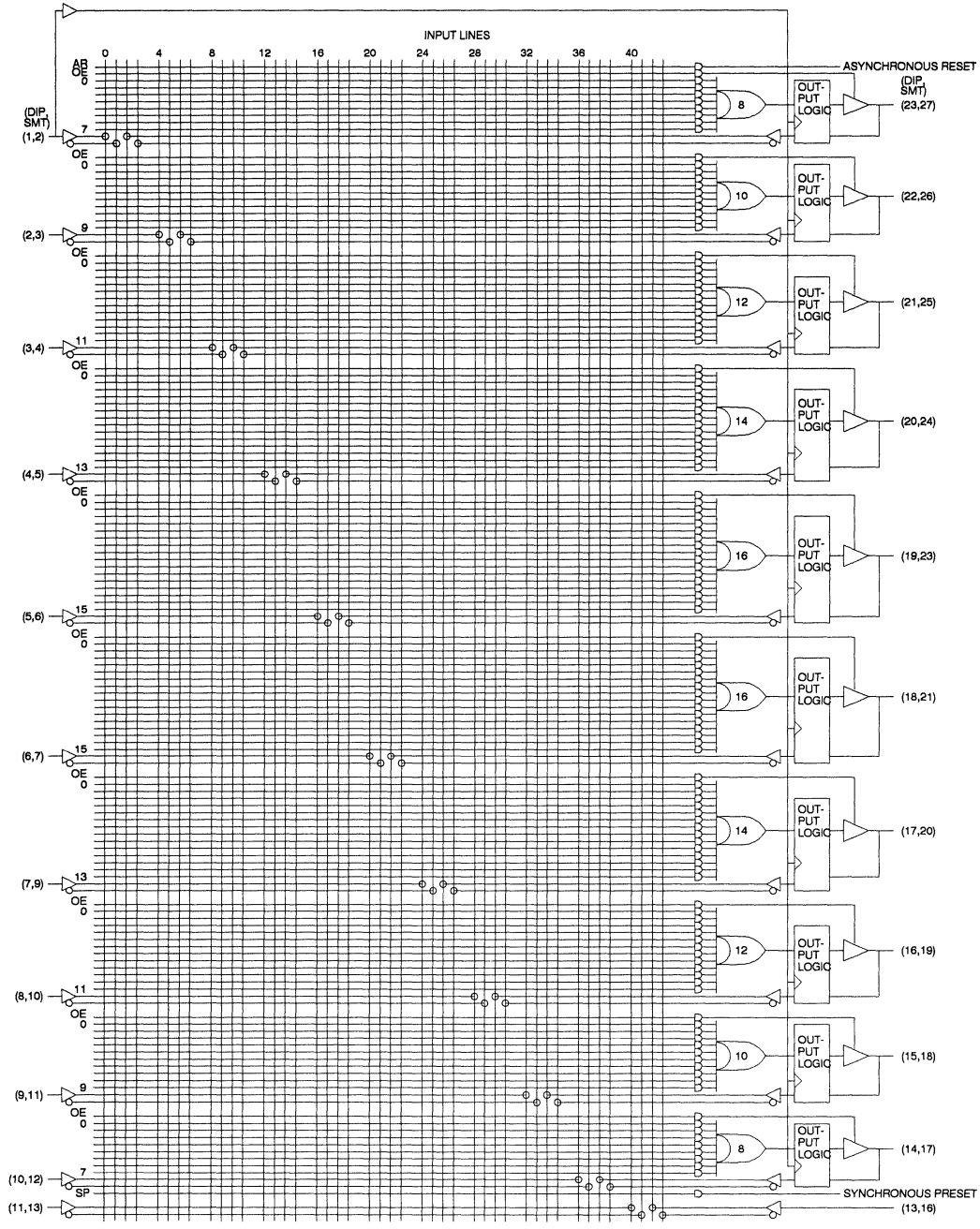
Commercial



Military



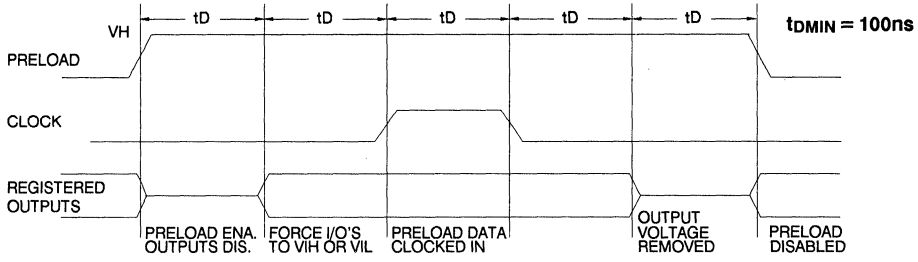
Functional Logic Diagram AT22V10/L



Preload of Registered Outputs

The registers in the AT22V10 and AT22V10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The PRELOAD state is entered by placing an 11V to 14V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the 10 registers.

Level forced on registered output pin during PRELOAD cycle.	Register state After Cycle
V_{IH}	High
V_{IL}	Low



Power Up Reset

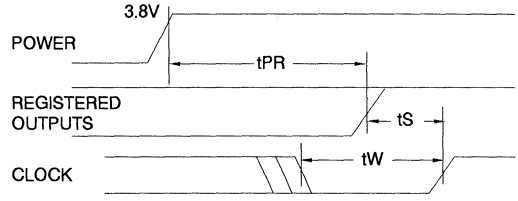
The registers in the AT22V10 and AT22V10L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

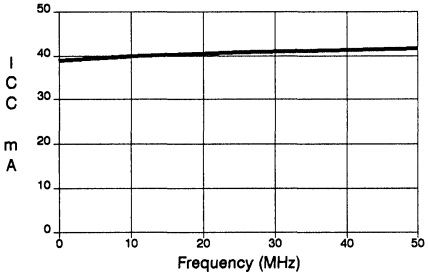
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22V10 or AT22V10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15W \bullet sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

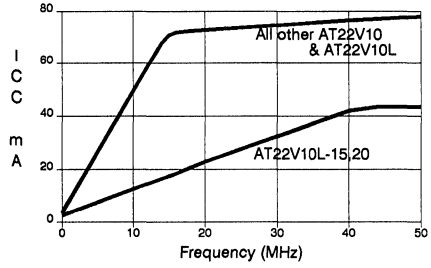
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10-15 (TA = 25C, VCC = 5V)

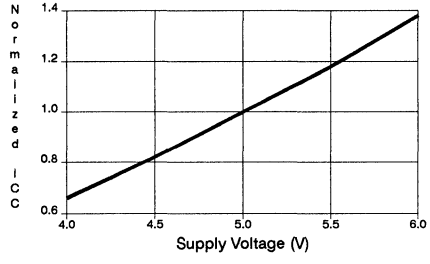


SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10L & AT22V10 (except AT22V10-15)

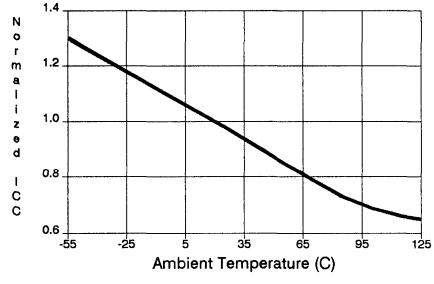


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

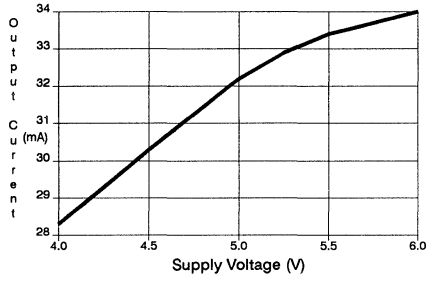


NORMALIZED ICC vs. AMBIENT TEMP.

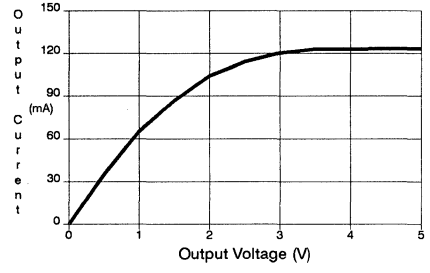
f = 30 MHz



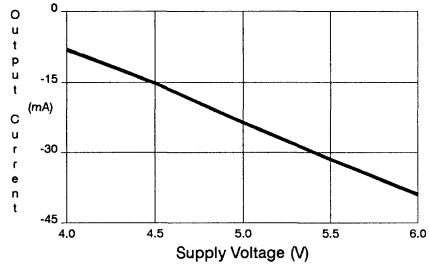
OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE (VOL = 0.5V)



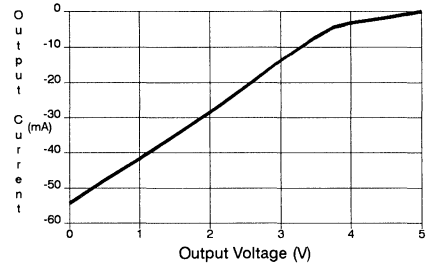
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE (VOH = 2.4V)



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



7

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	10	10	AT22V10-15DC AT22V10-15FC AT22V10-15GC AT22V10-15JC AT22V10-15KC AT22V10-15LC AT22V10-15NC AT22V10-15PC AT22V10-15YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10-15DI AT22V10-15FI AT22V10-15GI AT22V10-15JI AT22V10-15KI AT22V10-15LI AT22V10-15NI AT22V10-15PI AT22V10-15YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
20	12	15	AT22V10-20DC AT22V10-20FC AT22V10-20GC AT22V10-20JC AT22V10-20KC AT22V10-20LC AT22V10-20NC AT22V10-20PC AT22V10-20YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10-20DI AT22V10-20FI AT22V10-20GI AT22V10-20JI AT22V10-20KI AT22V10-20LI AT22V10-20NI AT22V10-20PI AT22V10-20YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
20	17	15	AT22V10-20DM AT22V10-20FM AT22V10-20GM AT22V10-20KM AT22V10-20LM AT22V10-20NM AT22V10-20YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	17	15	AT22V10-20DM/883 AT22V10-20FM/883 AT22V10-20GM/883 AT22V10-20KM/883 AT22V10-20LM/883 AT22V10-20NM/883 AT22V10-20YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	AT22V10-25DC AT22V10-25FC AT22V10-25GC AT22V10-25JC AT22V10-25KC AT22V10-25LC AT22V10-25NC AT22V10-25PC AT22V10-25YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10-25DI AT22V10-25FI AT22V10-25GI AT22V10-25JI AT22V10-25KI AT22V10-25LI AT22V10-25NI AT22V10-25PI AT22V10-25YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
25	18	15	AT22V10-25DM AT22V10-25FM AT22V10-25GM AT22V10-25KM AT22V10-25LM AT22V10-25NM AT22V10-25YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			AT22V10-25DM/883 AT22V10-25FM/883 AT22V10-25GM/883 AT22V10-25KM/883 AT22V10-25LM/883 AT22V10-25NM/883 AT22V10-25YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	AT22V10-30DM AT22V10-30FM AT22V10-30GM AT22V10-30KM AT22V10-30LM AT22V10-30NM AT22V10-30YM	24DW3 24C 28D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)

7

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
30	20	20	AT22V10-30DM/883 AT22V10-30FM/883 AT22V10-30GM/883 AT22V10-30KM/883 AT22V10-30LM/883 AT22V10-30NM/883 AT22V10-30YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	25	25	AT22V10-35DC AT22V10-35FC AT22V10-35GC AT22V10-35JC AT22V10-35KC AT22V10-35LC AT22V10-35NC AT22V10-35PC AT22V10-35YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10-35DI AT22V10-35FI AT22V10-35GI AT22V10-35JI AT22V10-35KI AT22V10-35LI AT22V10-35NI AT22V10-35PI AT22V10-35YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
20	17	15	5962-87539 04 LX 5962-87539 04 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-87539 01 KX 5962-87539 01 LX 5962-87539 01 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-87539 02 KX 5962-87539 02 LX 5962-87539 02 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-87539 03 KX 5962-87539 03 LX 5962-87539 03 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	17	15	5962-88670 04 KX 5962-88670 04 LX 5962-88670 04 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-88670 01 KX 5962-88670 01 LX 5962-88670 01 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-88670 02 KX 5962-88670 02 LX 5962-88670 02 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
40	30	25	5962-88670 03 KX 5962-88670 03 LX 5962-88670 03 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	10	10	AT22V10L-15DC AT22V10L-15FC AT22V10L-15GC AT22V10L-15JC AT22V10L-15KC AT22V10L-15LC AT22V10L-15NC AT22V10L-15PC AT22V10L-15YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10L-15DI AT22V10L-15FI AT22V10L-15GI AT22V10L-15JI AT22V10L-15KI AT22V10L-15LI AT22V10L-15NI AT22V10L-15PI AT22V10L-15YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
20	12	15	AT22V10L-20DC AT22V10L-20FC AT22V10L-20GC AT22V10L-20JC AT22V10L-20KC AT22V10L-20LC AT22V10L-20NC AT22V10L-20PC AT22V10L-20YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10L-20DI AT22V10L-20FI AT22V10L-20GI AT22V10L-20JI AT22V10L-20KI AT22V10L-20LI AT22V10L-20NI AT22V10L-20PI AT22V10L-20YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
20	17	15	AT22V10L-20DM AT22V10L-20FM AT22V10L-20GM AT22V10L-20KM AT22V10L-20LM AT22V10L-20NM AT22V10L-20YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	17	15	AT22V10L-20DM/883 AT22V10L-20FM/883 AT22V10L-20GM/883 AT22V10L-20KM/883 AT22V10L-20LM/883 AT22V10L-20NM/883 AT22V10L-20YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	AT22V10L-25DC AT22V10L-25FC AT22V10L-25GC AT22V10L-25JC AT22V10L-25KC AT22V10L-25LC AT22V10L-25NC AT22V10L-25PC AT22V10L-25YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10L-25DI AT22V10L-25FI AT22V10L-25GI AT22V10L-25JI AT22V10L-25KI AT22V10L-25LI AT22V10L-25NI AT22V10L-25PI AT22V10L-25YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
25	18	15	AT22V10L-25DM AT22V10L-25FM AT22V10L-25GM AT22V10L-25KM AT22V10L-25LM AT22V10L-25NM AT22V10L-25YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			AT22V10L-25DM/883 AT22V10L-25FM/883 AT22V10L-25GM/883 AT22V10L-25KM/883 AT22V10L-25LM/883 AT22V10L-25NM/883 AT22V10L-25YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	AT22V10L-30DM AT22V10L-30FM AT22V10L-30GM AT22V10L-30KM AT22V10L-30LM AT22V10L-30NM AT22V10L-30YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)

7

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
30	20	20	AT22V10L-30DM/883 AT22V10L-30FM/883 AT22V10L-30GM/883 AT22V10L-30KM/883 AT22V10L-30LM/883 AT22V10L-30NM/883 AT22V10L-35YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	25	25	AT22V10L-35DC AT22V10L-35FC AT22V10L-35GC AT22V10L-35JC AT22V10L-35KC AT22V10L-35LC AT22V10L-35NC AT22V10L-35PC AT22V10L-35YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
35	25	15	AT22V10L-35DI AT22V10L-35FI AT22V10L-35GI AT22V10L-35JI AT22V10L-35KI AT22V10L-35LI AT22V10L-35NI AT22V10L-35PI AT22V10L-35YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
20	17	15	5962-88724 04 KX 5962-88724 04 LX 5962-88724 04 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-88724 01 KX 5962-88724 01 LX 5962-88724 01 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-88724 02 KX 5962-88724 02 LX 5962-88724 02 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-88724 03 KX 5962-88724 03 LX 5962-88724 03 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-89755 01 KX 5962-89755 01 LX 5962-89755 01 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-89755 02 KX 5962-89755 02 LX 5962-89755 02 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
40	30	25	5962-89755 03 KX 5962-89755 03 LX 5962-89755 03 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

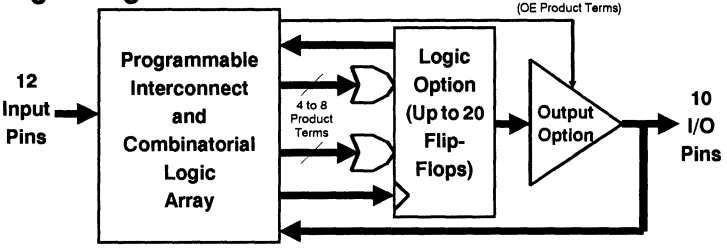
Features

- Third Generation Programmable Logic Structure
  - High Density Replacement for Discrete Logic
- High Speed - Plus a New Low Power Version
- Increased Logic Flexibility
  - 42 Inputs and 20 SUM terms
- Flexible Output Logic
  - 20 Flip-Flops - 10 Extra
  - All Can Be Individually Buried or 10 Output Directly
  - Each has Individual Asynchronous Reset or Clock Terms
- Multiple Feedback Paths Provide for Buried State Machines and I/O Bus Compatibility
- Pin Compatible with the AT22V10
  - Upgrade With The V750's 2X Usable Gates
- Proven and Reliable High Speed CMOS EPROM Process
  - 2000V ESD Protection
  - 200 mA Latchup Immunity
- Reprogrammable - Tested 100% for Programmability
- 24 pin, 300 mil Dual-In-line and 28 Lead Surface Mount Packages

High Density UV Erasable Programmable Logic Device

7

Logic Diagram



Description

The ATV750/L is 100% more powerful than most other programmable logic devices in 24 pin packages. Increased Product terms, SUM Terms, and Flip-Flops translate into more usable gates.

Each of the ATV750's 22 logic pins can be used as an input. Ten of these can be used as input, output, or bi-directional I/O pins. All 20 Flip-Flops can be fed back into the array independently. This flexibility allows burying all of the SUM terms and Flip-Flops.

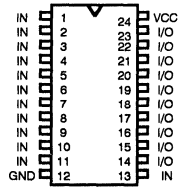
There are 171 Product Terms available. A variable format is used to assign between 4 and 8 Product Terms per Sum Term. There are 2 Sum Terms per output, providing added flexibility. Much more logic can be replaced by this one 24 pin device.

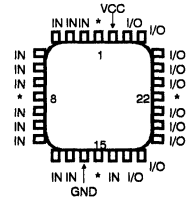
The ATV750/L has more flip-flops available than other EPLDs in this density range. Complex state machines are easily implemented.

Product terms are available providing Asynchronous Resets, Flip-Flop clocks, and Output Enables. One reset and one clock term are provided per Flip-Flop, with one Enable term per output. One product term provides a global synchronous Preset. Register Preload simplifies testing. The device has an internal power up clear function.

Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5V Supply





Absolute Maximum Ratings*

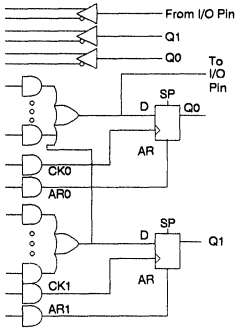
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 w•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

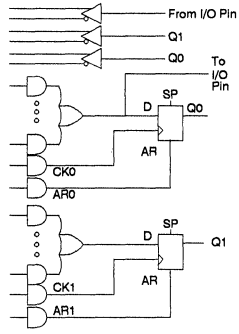
Note:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Logic Options

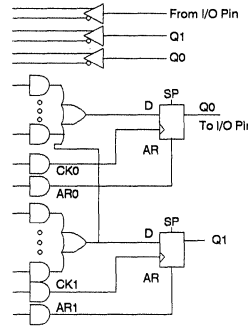
Combined Terms



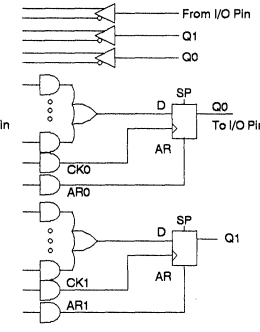
Separate Terms



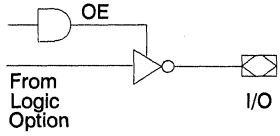
Combined Terms

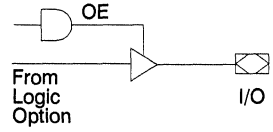


Separate Terms



Output Options





D.C. and A.C. Operating Conditions

		ATV750/L-20(1)	ATV750-25/L(1)	ATV750/L-30	ATV750/L-35	ATV750/L-40
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C(1)	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C(1)	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Note: 1. All ATV750L Characteristics are preliminary. ATV750 Characteristics for -20 and -25 are preliminary, and ATV750-30 Industrial and Military are preliminary.

D.C. Characteristics

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V				10	µA
I_{CC}	Power Supply Current	VCC = MAX, V_{IN} = GND, Outputs Open	ATV750	Com.		120	mA
				Ind.,Mil.		140	mA
			ATV750L(2)	Com.		12	mA
				Ind.,Mil.		15	mA
I_{CC2} (3)	Clocked Power Supply Current	f = 1MHz, VCC = MAX, Outputs Open	ATV750L(2)	Com.		15	mA
				Ind.,Mil.		20	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5V				-90	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 12mA Com.,Ind.			0.5	V
			I_{OL} = 8mA Mil.			0.5	V
			I_{OL} = 24mA, Com.			1.0	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OH} = -100µA		V_{CC}-0.3		V
			I_{OH} = -4.0mA		2.4		V

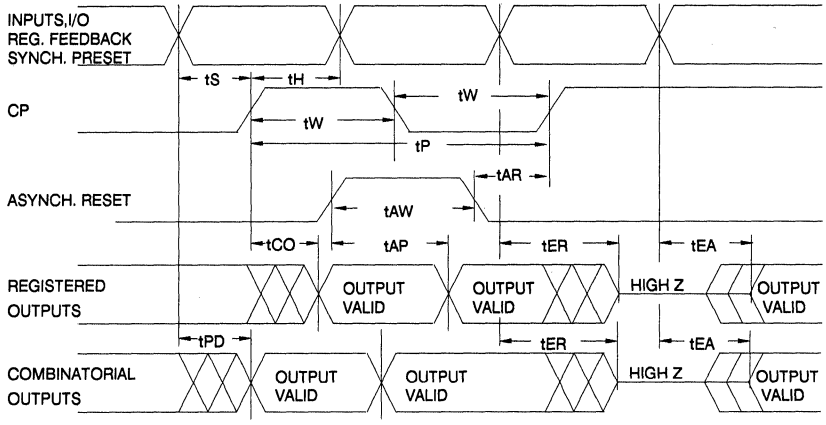
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.
2. Preliminary Data
3. Outputs not loaded.

Operating Modes

	24 DIP Pin	1	5	8	11	13	I/O's	Vcc(24)
Mode	28 JLCC Pin	2	6	10	13	16	I/O's	Vcc(28)
"EPLD"		X (1)	X	X	X	X	I/O	5V
Program		V_{PP}	X/V_H (2)	X	X/V_H	V_{PP}	D_{IN}	6V
PGM Verify		V_{PP}	X/V_H	X	X/V_H	V_{IL}	D_{OUT}	5V
PGM Inhibit		V_{PP}	X/V_H	X	X/V_H	V_{IH}	High Z	5-6V
Preload #1		X	X	V_H	X	V_{IL}	D_{IN}	5V
Preload #2		X	X	V_H	X	V_{IH}	D_{IN}	5V

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0V to 14.0V

A.C. Waveforms [1]



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

A.C. Characteristics

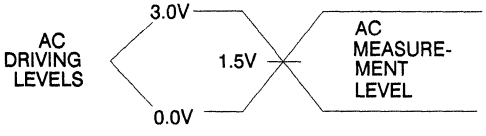
Symbol	Parameter	ATV750-30 Min	ATV750-30 Max	ATV750-35 Min	ATV750-35 Max	ATV750-40 Min	ATV750-40 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		30		35		40	ns
t_{EA}	Input to Output Enable		30		35		40	ns
t_{ER}	Input to Output Disable		30		35		40	ns
t_{CO}	Clock to Output	5	25	10	30	10	35	ns
t_{CF}	Clock to Feedback	5	10	10	12	10	15	ns
t_S	Input Setup Time	15		18		20		ns
t_H	Hold Time	5		10		15		ns
t_P	Clock Period	25		30		35		ns
t_W	Clock Width	12		15		17		ns
F_{MAX}	Maximum Frequency		40		33		28	MHz
t_{AW}	Asynchronous Reset Width	30		35		40		ns
t_{AR}	Asynchronous Reset Recovery Time	30		35		40		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		30		35		40	ns
t_{SP}	Setup Time, Synchronous Preset	15		18		20		ns

A.C. Characteristics, Preliminary

Symbol	Parameter	ATV750/L-20		ATV750/L-25		ATV750L-30		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		20		25		30	ns
t_{EA}	Input to Output Enable		20		25		30	ns
t_{ER}	Input to Output Disable		20		25		30	ns
t_{CO}	Clock to Output		18		22	5	25	ns
t_{CF}	Clock to Feedback	5	10	5	10	5	10	ns
t_S	Input Setup Time	10		12		15		ns
t_{SF}	Feedback Setup Time	5		7		15		ns
t_H	Hold Time	5		5		5		ns
t_P	Clock Period	18		22		25		ns
t_W	Clock Width	8		10		12		ns
F_{MAX}	Maximum Frequency		55		45		40	MHz
t_{AW}	Asynchronous Reset Width	15		20		30		ns
t_{AR}	Asynchronous Reset Recovery Time	15		20		30		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		20		25		30	ns
t_{SP}	Setup Time, Synchronous Preset	12		15		15		ns

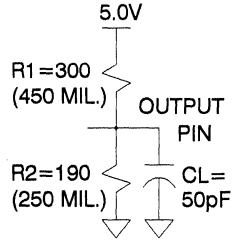
7

Input Test Waveforms and Measurement Levels

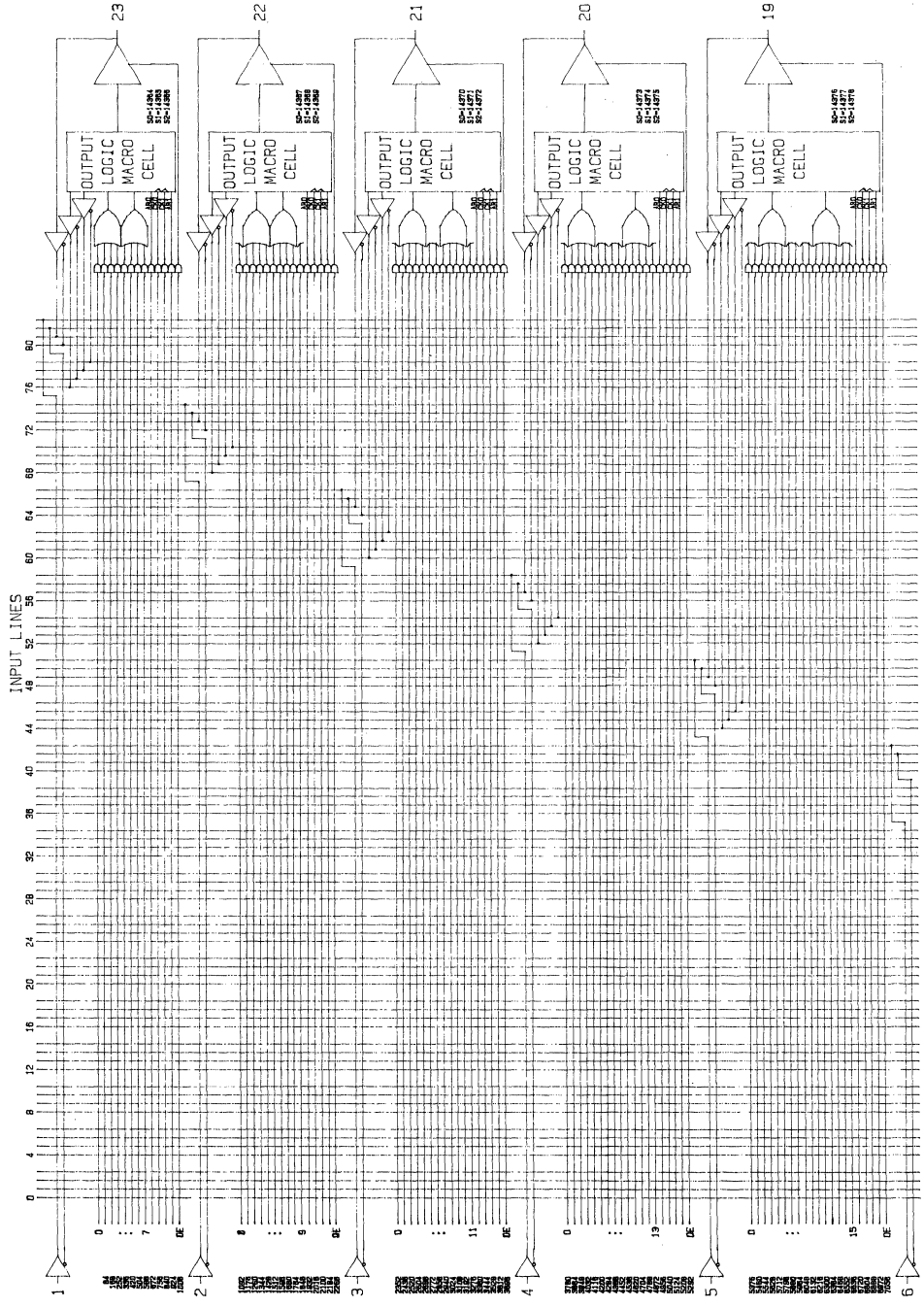


tR, tF < 5ns (10% to 90%)

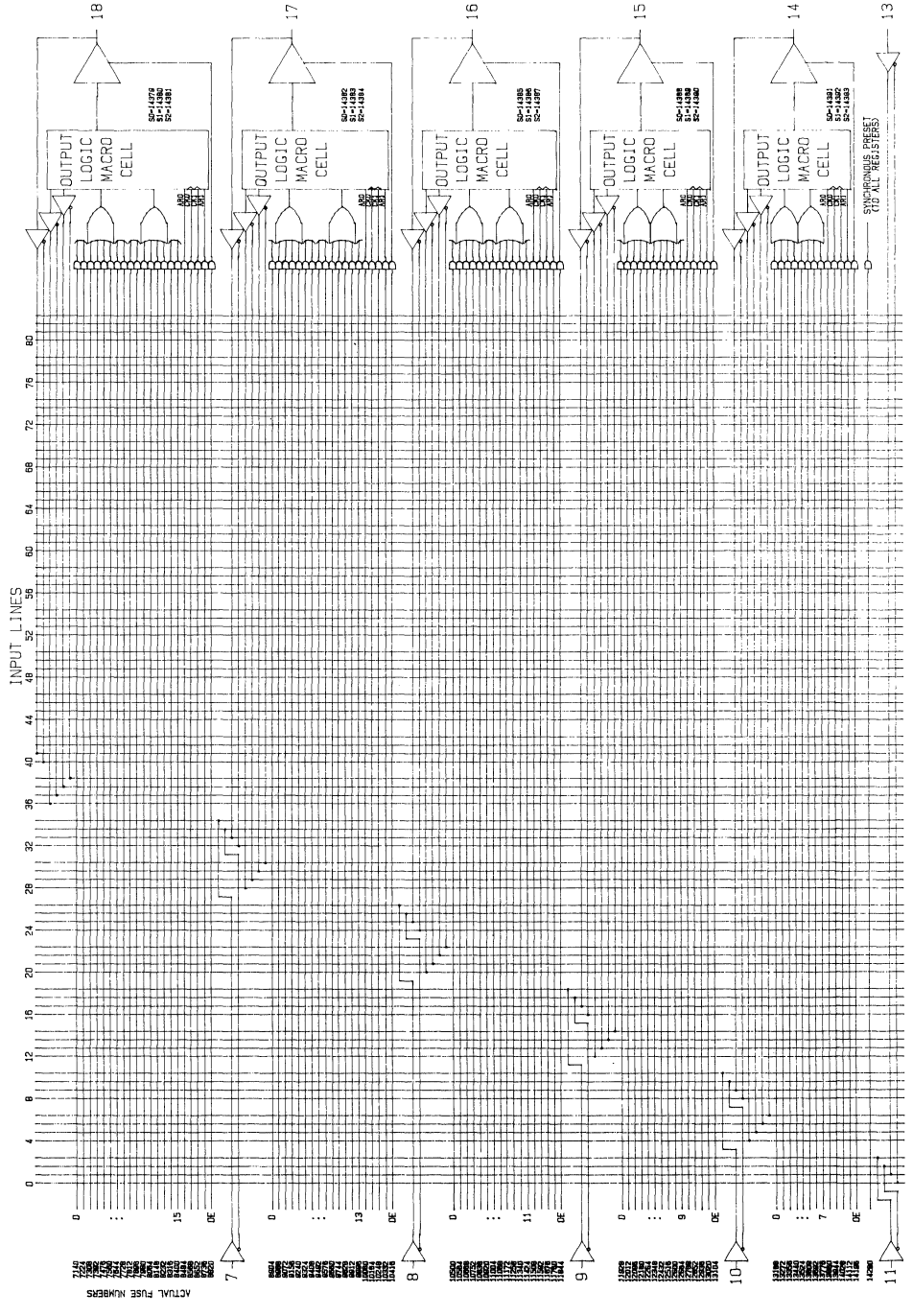
Output Test Load



Functional Logic Diagram ATV750, Upper Half

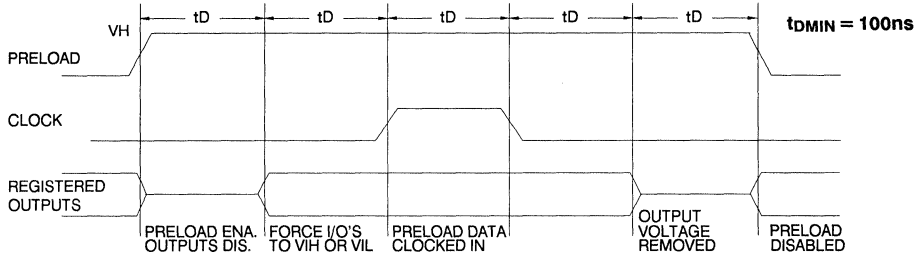


Functional Logic Diagram ATV750, Lower Half



Preload of Registered Outputs

The ATV750's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (S0) setting. The PRELOAD state is entered by placing an 11V to 14V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock term is pulsed high, the data on the I/O pin is placed into the register chosen by the Select Pin.



Level forced on registered output pin during PRELOAD cycle	Select Pin State	Register #1 state after cycle	Register #2 State after cycle
V_{IH}	Low	High	X
V_{IL}	Low	Low	X
V_{IH}	High	X	High
V_{IL}	High	X	Low

Power Up Reset

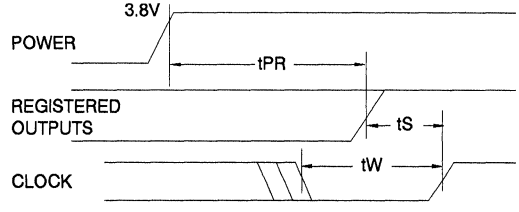
The registers in the ATV750/L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Using The ATV750's Many Advanced Features

The ATV750's flexibility puts more usable gates in 24 pins than other EPLDs. The ATV750/L starts with an architecture similar to the popular AT22V10, and adds several enhancements:

- Asynchronous Clocks -
  Each of the Flip-Flops in the ATV750/L has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV750/L clock period matches that of similar synchronous devices.
- A Full Bank of 10 More Registers -
  The ATV750/L provides two Flip-Flops for each Output Macrocell - a total of 20. Each register has its own clock and reset product terms, as well as its own SUM term.
- Independent I/O Pin and Feedback Paths -
  Each I/O pin on the ATV750/L has a dedicated input path. Each of the 20 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's Output Enable, facilitates designs using bi-directional I/O buses.
- Combinable Sum Terms -
  Each Output Macrocell's 2 SUM terms can be combined in an OR gate before the Output or the Register. This provides up to 16 product terms per Output or Flip-Flop. This architecture increases the number of usable gates available.

Programming Software Support

Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV750/L is available from the following sources:

Data I/O / Futurenet Corp.	- ABEL 2.1, 3.0, and above
Logical Devices	- CUPL 2.15B, and above

Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATV750/L. The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 Flip-Flops. Both Master and Slave halves of the Flip-Flops are reset when the input signals received combine so as to force the internal resets high.

7

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV750/L fuse patterns. Once programmed, the output buffers will remain in a high impedance state during verify.

The security fuse should be programmed last, as its effect is immediate.

Erasure Characteristics

The entire memory array of an ATV750/L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

Atmel CMOS EPLDs

Atmel's Erasable Programmable Logic Devices utilize an advanced 1.5 micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for EPLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing EPLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64k to 1 megabit devices.

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	18	55	ATV750-20DC ATV750-20FC ATV750-20GC ATV750-20JC ATV750-20KC ATV750-20LC ATV750-20NC ATV750-20PC ATV750-20YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			ATV750-20DI ATV750-20FI ATV750-20GI ATV750-20JI ATV750-20KI ATV750-20LI ATV750-20NI ATV750-20PI ATV750-20YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750-20DM ATV750-20FM ATV750-20GM ATV750-20KM ATV750-20LM ATV750-20NM ATV750-20YM	24DW3 24C 28D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750-20DM/883 ATV750-20FM/883 ATV750-20GM/883 ATV750-20KM/883 ATV750-20LM/883 ATV750-20NM/883 ATV750-20YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	22	45	ATV750-25DC ATV750-25FC ATV750-25GC ATV750-25KC ATV750-25LC ATV750-25NC ATV750-25YC	24DW3 24C 24D3 28KW 28LW 28L 24CW	Commercial (0°C to 70°C)
			ATV750-25DI ATV750-25FI ATV750-25GI ATV750-25JI ATV750-25KI ATV750-25LI ATV750-25NI ATV750-25PI ATV750-25YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	22	45	ATV750-25DM ATV750-25FM ATV750-25GM ATV750-25KM ATV750-25LM ATV750-25NM ATV750-25YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750-25DM/883 ATV750-25FM/883 ATV750-25GM/883 ATV750-25KM/883 ATV750-25LM/883 ATV750-25NM/883 ATV750-25YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	25	40	ATV750-30DC ATV750-30FC ATV750-30GC ATV750-30JC ATV750-30KC ATV750-30LC ATV750-30NC ATV750-30PC ATV750-30YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			ATV750-30DI ATV750-30FI ATV750-30GI ATV750-30JI ATV750-30KI ATV750-30LI ATV750-30NI ATV750-30PI ATV750-30YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750-30DM ATV750-30FM ATV750-30GM ATV750-30KM ATV750-30LM ATV750-30NM ATV750-30YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750-30DM/883 ATV750-30FM/883 ATV750-30GM/883 ATV750-30KM/883 ATV750-30LM/883 ATV750-30NM/883 ATV750-30YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
35	30	33	ATV750-35DC ATV750-35FC ATV750-35GC ATV750-35JC ATV750-35KC ATV750-35LC ATV750-35NC ATV750-35PC ATV750-35YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			ATV750-35DI ATV750-35FI ATV750-35GI ATV750-35JI ATV750-35KI ATV750-35LI ATV750-35NI ATV750-35PI ATV750-35YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750-35DM ATV750-35FM ATV750-35GM ATV750-35KM ATV750-35LM ATV750-35NM ATV750-35YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750-35DM/883 ATV750-35FM/883 ATV750-35GM/883 ATV750-35KM/883 ATV750-35LM/883 ATV750-35NM/883 ATV750-35YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	35	28	ATV750-40DI ATV750-40FI ATV750-40GI ATV750-40JI ATV750-40KI ATV750-40LI ATV750-40NI ATV750-40PI ATV750-40YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750-40DM ATV750-40FM ATV750-40GM ATV750-40KM ATV750-40LM ATV750-40NM ATV750-40YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
40	35	28	ATV750-35DM/883 ATV750-35FM/883 ATV750-35GM/883 ATV750-35KM/883 ATV750-35LM/883 ATV750-35NM/883 ATV750-35YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	30	33	5962-88726 02 LX 5962-88726 02 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	35	28	5962-88726 01 LX 5962-88726 01 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

7

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide Plastic Dual Inline Package OTP (PDIP)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	18	55	ATV750L-20DC ATV750L-20FC ATV750L-20GC ATV750L-20JC ATV750L-20KC ATV750L-20LC ATV750L-20NC ATV750L-20PC ATV750L-20YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			ATV750L-20DI ATV750L-20FI ATV750L-20GI ATV750L-20JI ATV750L-20KI ATV750L-20LI ATV750L-20NI ATV750L-20PI ATV750L-20YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
25	22	45	ATV750L-25DC ATV750L-25FC ATV750L-25GC ATV750L-25JC ATV750L-25KC ATV750L-25LC ATV750L-25NC ATV750L-25PC ATV750L-25YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24P3	Commercial (0°C to 70°C)
			ATV750L-25DI ATV750L-25FI ATV750L-25GI ATV750L-25JI ATV750L-25KI ATV750L-25LI ATV750L-25NI ATV750L-25PI ATV750L-25YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750L-25DM ATV750L-25FM ATV750L-25GM ATV750L-25KM ATV750L-25LM ATV750L-25NM ATV750L-25YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750L-25DM/883 ATV750L-25FM/883 ATV750L-25GM/883 ATV750L-25KM/883 ATV750L-25LM/883 ATV750L-25NM/883 ATV750L-25YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	25	40	ATV750L-30DI ATV750L-30FI ATV750L-30GI ATV750L-30JI ATV750L-30KI ATV750L-30LI ATV750L-30NI ATV750L-30PI ATV750L-30YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750L-30DM ATV750L-30FM ATV750L-30GM ATV750L-30KM ATV750L-30LM ATV750L-30NM ATV750L-30YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750L-30DM/883 ATV750L-30FM/883 ATV750L-30GM/883 ATV750L-30KM/883 ATV750L-30LM/883 ATV750L-30NM/883 ATV750L-30YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide Plastic Dual Inline Package OTP (PDIP)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

Using the ATV750 with ABEL™ and CUPL™

High Density UV Erasable Programmable Logic Device

Application Brief

Typical applications for first and second generation PLDs include address decoding and counting. Here is an example using the ATV750, a third generation PLD, to implement a more complex counter. The following pages show example input listings for ABEL™ and CUPL™.

The first listing is for ABEL™ 3.0. The second listing is for CUPL™ 2.15b.

This design uses all twenty flip-flops of the ATV750 to build a 20-bit synchronous / asynchronous counter. With COUNT high and COUNT10, PRESET, RESET, Q1SEL, and OE low, a 1 MHz signal on the CLK pin will produce roughly a 1 Hz signal on pin 23.

The unique architecture of the macrocell gives the ATV750 its versatility and also increases gate utilization. Each of the twenty registers has its Q and $\overline{Q}$ feeding back to the array.

The Output Registers (Q0's) can be addressed directly (by the pin names in ABEL™; in CUPL™ define PINNODES 35 through 44). However, to access the Buried Registers (Q1's), the corresponding nodes have to be named (nodes 26 through 35 in ABEL™, PINNODEs 25 through 34 in CUPL™). They are called B14, B15,....B24 to show the correspondence with their Q0 counterparts. Any valid identifier can be used as a node name.

The ATV750 provides a global synchronous Preset which is accessible through the node definition or by extension. Each of the twenty flip-flops has its own clock, reset and sum term (not like a second generation PLD that allows only one clock and one reset for all registers). Use the '.CK' extension in conjunction with the named registers to define the equations for the clock inputs for all the registers. Use the '.RE' command following the named registers to define the reset terms.

The ATV750 gives the user a total of eight choices to configure each output. The operators ':=' and '=' inform ABEL™ the output is registered or combinatorial, respectively. In CUPL™, use of the .Q extension defines a registered output. Use the '!' operator to define an active low output; active high output is assumed by default. Another convenient method is to use the 'ISTYPE' statement (ABEL™ only) to define the outputs as high/low and registered / combinatorial. (Note: the ATV22V10 is defined the same way.)

The ATV750 has an advanced feature that lets the user combine or separate the sum terms in each macrocell. By default, the terms are combined. In CUPL™and ABEL™, using the buried register automatically splits the sum terms.

'Sets' (ABEL™) or 'fields' (CUPL™) are often defined for ease of referencing a group of signals or constants. In this particular example, 'OUTS' is a collection of outputs used in the OE definition. "Out" is a reserved word in CUPL, and "Ouch" was used instead.

When PRESET and COUNT are asserted and the Clk pin goes high, all registers, even the asynchronously clocked ones, will go to the 'one' state. This is because as each flip-flop goes high, it forces the clock of the next flip-flop high, rippling the preset condition throughout the entire bank. To reset the output registers and the buried registers, simply have RESET high and vary !Q1SEL accordingly.

The O registers pair with the corresponding B registers to form ten 2-bit synchronous counters. These are clocked by the preceding pair's output, thus forming a 20-bit counter. The last product term for the 'O' logic changes this device into a 10-bit counter with the output register mimicking the B registers. This provides observability, and a handy test mode. Test vectors take full advantage of ABEL™'s

and CUPL™'s ability to simulate the device before programming. This feature can save hours of testing and enable the user to make the necessary changes in seconds without ever leaving his or her PC. Therefore, it is highly recommended to take the time to write a comprehensive set of test vectors; this will reduce the time spent on the test bench.

ABEL™ is a trademark of DATA I/O Corporation
CUPL™ is a trademark of Logical Devices, Inc.

ABEL™ Example

```
module EX3
title '20 Bit Counter for Atmel's ATV750
EX375  device   'P750';
Clk                              pin     1;
COUNT,COUNT10,PRESET             pin     2, 3, 4;
RESET, Q1SEL , OE                pin     5, 11, 13;
O14,O15,O16,O17,O18              pin     14,15,16,17,18;
O19,O20,O21,O22,O23              pin     19,20,21,22,23;
B14,B15,B16,B17,B18              node    26,27,28,29,30;
B19,B20,B21,B22,B23              node    31,32,33,34,35;
"       Nodes           Description
"       26..35          Q1 for pins 14 to 23
"Sets
OUTS = [O23,O22,O21,O20,O19,O18,O17,O16,O15,O14];
H,L,Z,C,X = 1,0,.Z.,.C.,.X.;
Equations
O14.RE          =       O14.Q & RESET & !Q1SEL;
B14.RE          =       B14 & RESET & Q1SEL;
O15.RE          =       O15.Q & RESET & !Q1SEL;
B15.RE          =       B15 & RESET & Q1SEL;
O16.RE          =       O16.Q & RESET & !Q1SEL;
B16.RE          =       B16 & RESET & Q1SEL;
O17.RE          =       O17.Q & RESET & !Q1SEL;
B17.RE          =       B17 & RESET & Q1SEL;
O18.RE          =       O18.Q & RESET & !Q1SEL;
B18.RE          =       B18 & RESET & Q1SEL;
O19.RE          =       O19.Q & RESET & !Q1SEL;
B19.RE          =       B19 & RESET & Q1SEL;
O20.RE          =       O20.Q & RESET & !Q1SEL;
B20.RE          =       B20 & RESET & Q1SEL;
O21.RE          =       O21.Q & RESET & !Q1SEL;
B21.RE          =       B21 & RESET & Q1SEL;
O22.RE          =       O22.Q & RESET & !Q1SEL;
B22.RE          =       B22 & RESET & Q1SEL;
O23.RE          =       O23.Q & RESET & !Q1SEL;
B23.RE          =       B23 & RESET & Q1SEL;
O14.C           =       Clk & COUNT;
B14.CK          =       Clk & COUNT; "Synchronous
O15.CK          =       O14.Q & COUNT;
B15.CK          =       O14.Q & COUNT; "Asynchronous
O16.CK          =       O15.Q & COUNT;
B16.CK          =       O15.Q & COUNT;
O17.CK          =       O16.Q & COUNT;
B17.CK          =       O16.Q & COUNT;
O18.CK          =       O17.Q & COUNT;
B18.CK          =       O17.Q & COUNT;
O19.CK          =       O18.Q & COUNT;
B19.CK          =       O18.Q & COUNT;
O20.CK          =       O19.Q & COUNT;
B20.CK          =       O19.Q & COUNT;
O21.CK          =       O20.Q & COUNT;
B21.CK          =       O20.Q & COUNT;
O22.CK          =       O21.Q & COUNT;
B22.CK          =       O21.Q & COUNT;
O23.CK          =       O22.Q & COUNT;
B23.CK          =       O22.Q & COUNT;
B14             :=      !B14;
!O14            :=      !O14.Q &  B14 & !COUNT10
                #       O14.Q & !B14 & !COUNT10
                #       !B14 & COUNT10;
B15             :=      !B15;
!O15            :=      !O15.Q & B15 & !COUNT10
                #       O15.Q & !B15 & !COUNT10
                #       !B15 & COUNT10;
B16             :=      !B16;
!O16            :=      !O16.Q & B16 & !COUNT10
                #       O16.Q & !B16 & !COUNT10
                #       !B16 & COUNT10;
B17             :=      !B17;
!O17            :=      !O17.Q & B17 & !COUNT10
                #       O17.Q & !B17 & !COUNT10
                #       !B17 & COUNT10;
B18             :=      !B18;
!O18            :=      !O18.Q & B18 & !COUNT10
                #       O18.Q & !B18 & !COUNT10
                #       !B18 & COUNT10;
B19             :=      !B19;
!O19            :=      !O19.Q &  B19 & !COUNT10
                #       O19.Q & !B19 & !COUNT10
                #       !B19 & COUNT10;
B20             :=      !B20;
!O20            :=      !O20.Q & B20 & !COUNT10
                #       O20.Q & !B20 & !COUNT10
                #       !B20 & COUNT10;
B21             :=      !B21;
!O21            :=      !O21.Q & B21 & !COUNT10
                #       O21.Q & !B21 & !COUNT10
                #       !B21 & COUNT10;
B22             :=      !B22;
!O22            :=      !O22.Q & B22 & !COUNT10
                #       O22.Q & !B22 & !COUNT10
                #       !B22 & COUNT10;
B23             :=      !B23;
!O23            :=      !O23.Q & B23 & !COUNT10
                 #      O23.Q & !B23 & !COUNT10
                #       !B23 & COUNT10;
O23.PR          =       PRESET;
ENABLE OUTS     =       !OE;
End
```

CUPL™ Example

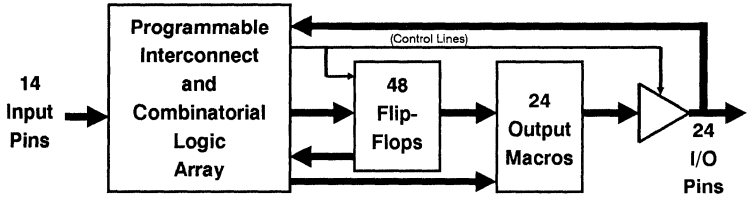
```
Name            EX75;
Company         Atmel;
Device          V750;
/*****************************************/
/** Allowable Target Device Types : V750        */
/*****************************************/
/**Inputs**/
PIN [1..4]      =       [Clk,COUNT,COUNT10,PRESET];
PIN [5,11,13]   =       RESET,Q1SEL,OE;
/**Outputs**/
PIN [14..23]    =       [O14..O23];     /* Pin Outputs*/
/*The easiest way to access the buried nodes in CUPL*/
/*Refer to the I/O pins by their pin names, and the */
/* Q0 and Q1 outputs by their pinnode names */
PINNODE [25..34]        =       [B14..B23]; /* Q1 nodes*/
PINNODE [35..44]        =       [Q14..Q23]; /* Q0 nodes*/
field BEES      =       [B23..B14];     /*Q1 field*/
field Ohi       =       [O23..O19];     /*output hi field*/
field Olo       =       [O18..O14];     /*output low field*/
field Ouch      =       [O23..O14];     /*outputfield*/
/** Logic Equations **/
/* The Asynch. Reset terms use the .AR extension*/
Q14.AR          =       Q14 & RESET & !Q1SEL;
B14.AR          =       B14 & RESET & Q1SEL;
Q15.AR          =       Q15 & RESET & !Q1SEL;
B15.AR          =       B15 & RESET & Q1SEL;
Q16.AR          =       Q16 & RESET & !Q1SEL;
B16.AR          =       B16 & RESET & Q1SEL;
Q17.AR          =       Q17 & RESET & !Q1SEL;
B17.AR          =       B17 & RESET & Q1SEL;
Q18.AR          =       Q18 & RESET & !Q1SEL;
B18.AR          =       B18 & RESET & Q1SEL;
Q19.AR          =       Q19 & RESET & !Q1SEL;
B19.AR          =       B19 & RESET & Q1SEL;
Q20.AR          =       Q20 & RESET & !Q1SEL;
B20.AR          =       B20 & RESET & Q1SEL;
Q21.AR          =       Q21 & RESET & !Q1SEL;
B21.AR          =       B21 & RESET & Q1SEL;
Q22.AR          =       Q22 & RESET & !Q1SEL;
B22.AR          =       B22 & RESET & Q1SEL;
Q23.AR          =       Q23 & RESET & !Q1SEL;
B23.AR          =       B23 & RESET & Q1SEL;
/* The Clock lines are accessed with the .CK extension*/
Q14.CK          =       Clk & COUNT;
B14.CK          =       Clk & COUNT; /* Synchronous */
Q15.CK          =       Q14 & COUNT;
B15.CK          =       Q14 & COUNT; /* Asynchronous*/
Q16.CK          =       Q15 & COUNT;
B16.CK          =       Q15 & COUNT;
Q17.CK          =       Q16 & COUNT;
B17.CK          =       Q16 & COUNT;
Q18.CK          =       Q17 & COUNT;
B18.CK          =       Q17 & COUNT;
Q19.CK          =       Q18 & COUNT;
B19.CK          =       Q18 & COUNT;
Q20.CK          =       Q19 & COUNT;
B20.CK          =       Q19 & COUNT;
Q21.CK          =       Q20 & COUNT;
B21.CK          =       Q20 & COUNT;
Q22.CK          =       Q21 & COUNT;
B22.CK          =       Q21 & COUNT;
Q23.CK          =       Q22 & COUNT;
B23.CK          =       Q22 & COUNT;
B14.D           =       !B14;
Q14.D           =       !Q14 &  B14 & !COUNT10
                #       Q14 & !B14 & !COUNT10
                #       !B14 & COUNT10;
/* Equations for both the B and the Q automatically  */
/*tells CUPL to set the 'split' SUM term's architecture bit.*/
B15.D           =       !B15;
Q15.D           =       !Q15 & B15 & !COUNT10
                #       Q15 & !B15 & !COUNT10
                #       !B15 & COUNT10;
B16.D           =       !B16;
Q16.D           =       !Q16 & B16 & !COUNT10
                #       Q16 & !B16 & !COUNT10
                #       !B16 & COUNT10;
B17.D           =       !B17;
Q17.D           =       !Q17 & B17 & !COUNT10
                #       Q17 & !B17 & !COUNT10
                #       !B17 & COUNT10;
B18.D           =       !B18;
Q18.D           =       !Q18 & B18 & !COUNT10
                #       Q18 & !B18 & !COUNT10
                #       !B18 & COUNT10;
B19.D           =       !B19;
Q19.D           =       !Q19 & B19 & !COUNT10
                #       Q19 & !B19 & !COUNT10
                #       !B19 & COUNT10;
B20.D           =       !B20;
Q20.D           =       !Q20 & B20 & !COUNT10
                #       Q20 & !B20 & !COUNT10
                #       !B20 & COUNT10;
B21.D           =       !B21;
Q21.D           =       !Q21 & B21 & !COUNT10
                #       Q21 & !B21 & !COUNT10
                #       !B21 & COUNT10;
B22.D           =       !B22;
Q22.D           =       !Q22 &  B22 & !COUNT10
                #       Q22 & !B22 & !COUNT10
                #       !B22 & COUNT10;
B23.D           =       !B23;
Q23.D           =       !Q23 & B23 & !COUNT10
                #       Q23 & !B23 & !COUNT10
                #       !B23 & COUNT10;
/*Only one synch preset equation is required  */
O23.SP  =       PRESET;
/*Use the .OE extension for the OE product term*/
O14.oe          =       !OE ;   O19.oe  =       !OE ;
O15.oe          =       !OE ;   O20.oe  =       !OE ;
O16.oe          =       !OE ;   O21.oe  =       !OE ;
O17.oe          =       !OE ;   O22.oe  =       !OE ;
O18.oe          =       !OE ;   O23.oe  =       !OE ;
```

Features

- Third Generation Programmable Logic Structure
  - Easily Achieves Gate Utilization Factors of 80%
- Increased Logic Flexibility
  - 86 Inputs and 72 Sum Terms
- Flexible Output Macrocell
  - 48 Flip-Flops - 2 per Macrocell
  - 3 Sum Terms - Can Be OR'ed and Shared
- High Speed
- Low Power - Less than 0.5mA Typical (ATV2500)
- Multiple Feedback Paths Provide For Buried State Machines and I/O Bus Compatibility
- Asynchronous Clocks and Resets
  - Multiple Synchronous Presets - 1 per 4 or 8 Flip-Flops
- Proven and Reliable High Speed CMOS EPROM Process
  - 2000V ESD Protection
  - 200 mA Latchup Immunity
- Reprogrammable - Tested 100% for Programmability
- 40 pin Dual-In-line and 44 Lead Surface Mount Packages

High Density UV Erasable Programmable Logic Device

Block Diagram



Description

The ATV2500/H is the most powerful programmable logic device available in a 40 pin package. Increased Product terms, Sum Terms, and Flip-Flops translate into many more usable gates. High gate utilization is easily obtainable.

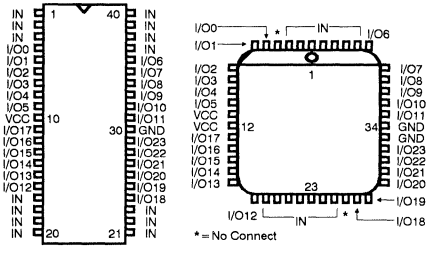
The ATV2500/H is organized around a global bus. All pin and feedback terms are always available to every Logic Cell. Each of the 38 logic pins and their complements are array inputs, as well as the true and false outputs of each of the 48 Flip-Flops.

There are 416 Product Terms available. Four Product Terms are input to each Sum Term. The 3 Sum terms per Logic Cell can be combined to provide up to 12 Product Terms, Combinatorial and Registered. Independent of output configuration, the 2 Flip-Flops are always usable, and always have at least 4 Product Term inputs.

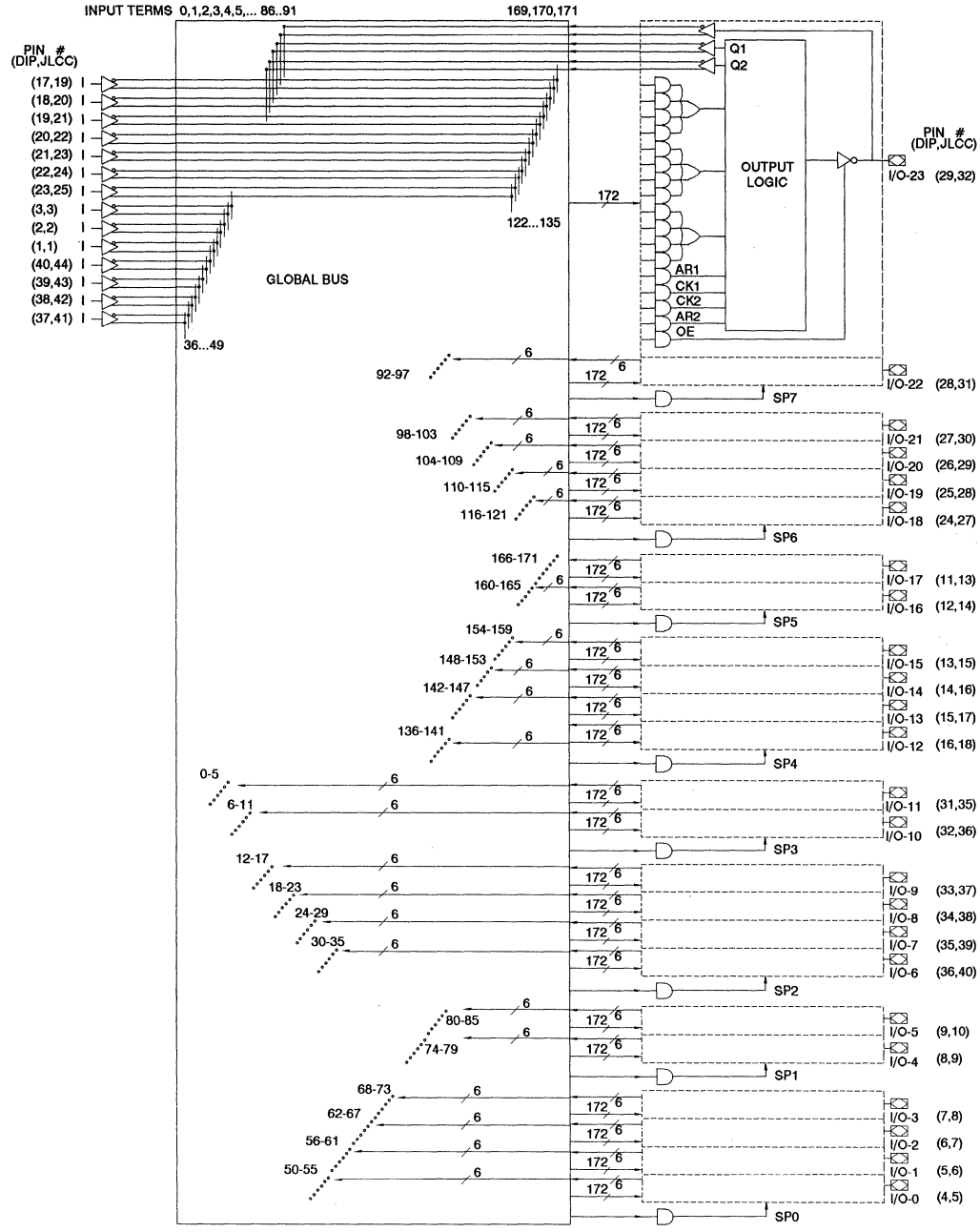
Product terms are available providing Asynchronous Resets, Flip-Flop clocks, and Output Enables. One reset and one clock term are provided per Flip-Flop, with one Enable term per output. Eight product terms provide local Synchronous Presets, divided up into banks of 4 and 8 Flip-Flops. Register Preload and buried register observability simplify testing. The device has an internal power up clear function.

Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
I/O,0,2,4..	"Even" I/O Buffers
I/O,1,3,5..	"Odd" I/O Buffers
*	No Internal Connection
VCC	+5V Supply



Functional Logic Diagram ATV2500/H



Functional Logic Diagram Description

The ATV2500/H Functional Logic Diagram describes the interconnections between the input, feedback pins and Logic Cells. All interconnections are routed through the Global Bus.

The ATV2500/H is a straightforward and uniform EPLD. The 24 Macrocells are numbered 0 through 23. Each Macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per Flip-Flop, and an Output Enable. The top 12 product terms are grouped into 3 sum terms, which are used as shown in the Macrocell diagrams.

Eight Synchronous Preset terms are distributed in a 2/4 pattern. The first four Macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two Macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each Macrocell provides 6 inputs to the global bus: (left to right) Flip-Flop Q2 true and false, Flip-Flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the Global Bus are the six numbers in the bus diagram next to each Macrocell.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

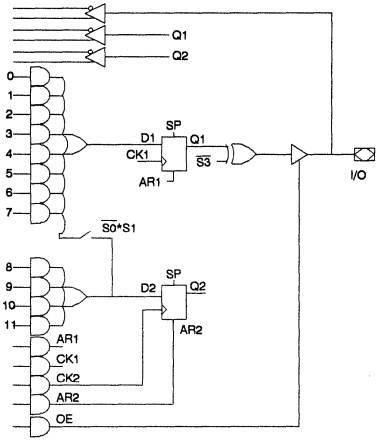
7

Operating Modes

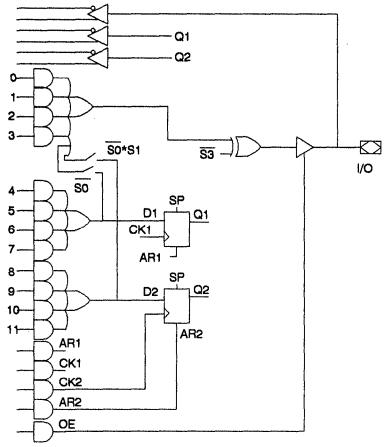
	40 DIP PIN	21	2	38	23	20	V_{CC}(10)	Odd	Even
Mode	44 JLCC PIN	23	2	42	25	22	V_{CC}(11,12)	I/O's	I/O's
"EPLD"		X[1]	X	X	X	X	5V	I/O	I/O
Program		V_{PP}	X	X	X	V_H (2)	6V	D_{IN}	N.C.
PGM Verify		V_{PP}	X	X	X	V_{IL}	6V	D_{OUT}	V_{OH}
PGM Inhibit		V_{PP}	X	X	X	V_{IH}	6V	High Z	High Z
Preload Q1		⎍	X	V_H	V_{IL}/V_{IH}	V_{IL}	5V	D_{IN}(Even/Odd)	V_{IH}
Preload Q2		⎍	X	V_H	V_{IL}/V_{IH}	V_{IH}	5V	D_{IN}(Even/Odd)	V_{IH}
Observe Q2		X	V_H	X	X	X	5V	D_{OUT}	D_{OUT}

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0V to 14.0V

Output Logic, Registered (1)



Output Logic, Combinatorial (1)



Note: 1. These diagrams shows equivalent logic functions, not necessarily the actual circuit implementation.

			Terms In		
S2	S1	S0	D1	D2	Output Configuration
0	0	0	8	4	Registered (Q1)
0	1	0	12	4(1)	Registered (Q1)

Note: 1. These 4 terms are shared with D1.

			Terms In		
S2	S1	S0	D1	D2	Output Configuration
1	0	0	4(1)	4	Combinatorial (8 Terms)
1	0	1	4	4	Combinatorial (4 Terms)
1	1	0	4(1)	4(1)	Combinatorial (12 Terms)

Note: 1. These 4 terms are shared with D1.

S3	Output Configuration
0	Active Low
1	Active High

S3	Output Configuration
0	Active Low
1	Active High

D.C. and A.C. Operating Conditions

		ATV2500H-25(1)	ATV2500/H-30(1)	ATV2500/H-35	ATV2500-40	ATV2500-45
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C(2)	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C(2)	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Notes: 1. Preliminary data for all ATV2500H-25's and all ATV2500-30's.
2. Preliminary data for both Industrial and Military ATV2500-35 .

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	ATV2500	Com.		0.5	5	mA
				Ind.,Mil.		0.5	10	mA
			ATV2500H	Com.		65	120	mA
				Ind.,Mil.		65	140	mA
I_{CC2}	Clocked Power Supply Current (ATV2500)	f = 1MHz, V_{CC} = MAX Outputs Open		Com.		10	15	mA
				Ind.,Mil.		10	20	mA
I_{OS} [1]	Output Short Circuit Current	V_{OUT} = 0.5V					-90	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8mACom,Ind;6mA Mil.					0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100µA			V_{CC}-0.3			V
		I_{OH} = -4.0mA			2.4			V

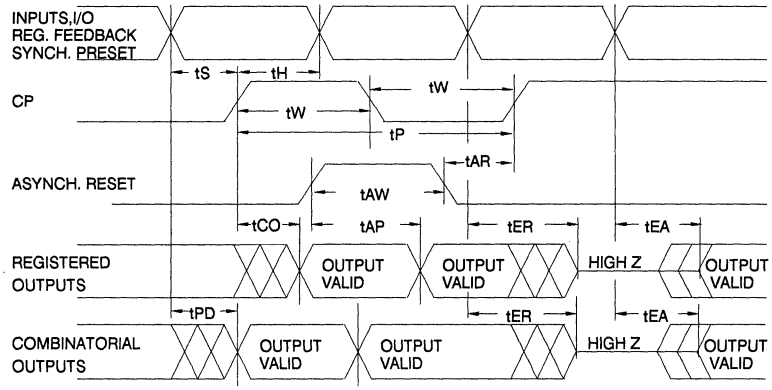
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

A.C. Waveforms [1]



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

A.C. Characteristics for the ATV2500

		ATV2500-30[1]		ATV2500-35		ATV2500-40		ATV2500-45		
Symbol	**Parameter**	Min	Max	Min	Max	Min	Max	Min	Max	**Units**
t_{PD}	Input or Feedback to Non-Registered Output		30		35		40		45	ns
t_{EA}	Input to Output Enable		30		35		40		45	ns
t_{ER}	Input to Output Disable		30		35		40		45	ns
t_{CO}	Clock to Output	5	30	5	35	5	40	5	45	ns
t_{CF}	Clock to Feedback	10	20	15	20	15	22	15	25	ns
t_{SI1}	Input Setup Time, Output Register	20		22		25		30		ns
t_{SI2}	Input Setup Time, Buried Register[2]	5		5		5		5		ns
t_{SF}	Feedback Setup Time	10		15		18		20		ns
t_{H1}	Hold Time, Output Register	10		15		15		15		ns
t_{H2}	Hold Time, Buried Register[2]	5		5		5		5		ns
t_W	Clock Width	12		15		17		20		ns
t_P	Clock Period	30		35		40		45		ns
F_{MAX}	Maximum Frequency (1/t_P)		33		28		25		22	MHz
t_{AW}	Asynchronous Reset Width	18		20		22		25		ns
t_{AR}	Asynchronous Reset Recovery Time	18		20		22		25		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		30		35		40		45	ns

Note: 1. Preliminary data.
2. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

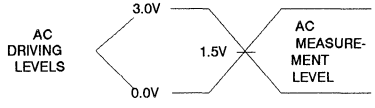
A.C. Characteristics for the ATV2500H

Symbol	Parameter	ATV2500H-25[1]		ATV2500H-30		ATV2500H-35		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		25		30		35	ns
t_{EA}	Input to Output Enable		25		30		35	ns
t_{ER}	Input to Output Disable		25		30		35	ns
t_{CO}	Clock to Output	10	25	12	30	15	35	ns
t_{CF}	Clock to Feedback	10	18	12	20	15	20	ns
t_{SI1}	Input Setup Time, Output Register	10		12		15		ns
t_{SI2}	Input Setup Time, Buried Register[2]	5		5		5		ns
t_{SF}	Feedback Setup Time	7		10		15		ns
t_{H1}	Hold Time	5		5		5		ns
t_W	Clock Width	10		12		15		ns
t_P	Clock Period	25		30		35		ns
F_{MAX}	Maximum Frequency (1/t_P)		40		33		28	MHz
t_{AW}	Asynchronous Reset Width	15		18		20		ns
t_{AR}	Asynchronous Reset Recovery Time	15		18		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		25		30		35	ns

Note: 1. Preliminary Data.
2. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

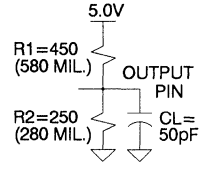
7

Input Test Waveforms and Measurement Levels



tR, tF < 5ns (10% to 90%)

Output Test Load

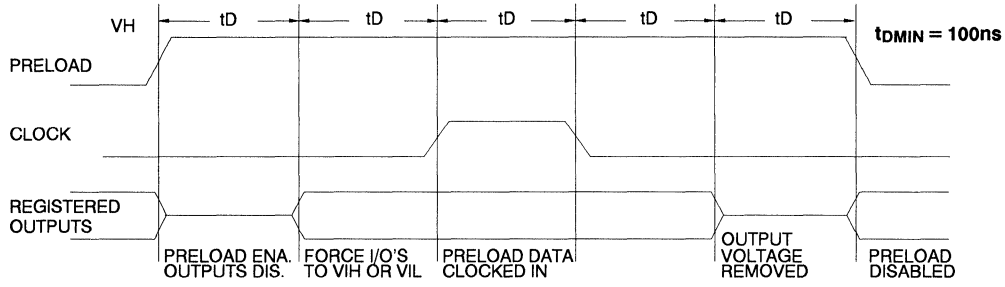


Preload and Observability of Registered Outputs

The ATV2500/H's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the Odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD state is entered by placing an 11V to 14V signal on pin 38 on the DIP and pin 42 on the SMP. When the clock term is pulsed high, (pin 21 on the DIP, pin 23 on the SMP) the data on the I/O pins is placed into the 12 registers chosen by the Q Select and Even/Odd Select Pins.

Register 2 Observability Mode is entered by placing an 11V to 14V signal on pin 2 (DIP or SMP). In this mode, the contents of the Buried Register bank will appear on the associated outputs when the OE control signals are active.



Level forced on Odd I/O pin during PRELOAD cycle.	Q Select Pin State	Even/ Odd Select	Even Q1 state after cycle	Even Q2 state after cycle	Odd Q1 state after cycle	Odd Q2 state after cycle
V_{IH}	Low	Low	High	X	X	X
V_{IL}	Low	Low	Low	X	X	X
V_{IH}	High	Low	X	High	X	X
V_{IL}	High	Low	X	Low	X	X
V_{IH}	Low	High	X	X	High	X
V_{IL}	Low	High	X	X	Low	X
V_{IH}	High	High	X	X	X	High
V_{IL}	High	High	X	X	X	Low

Power Up Reset

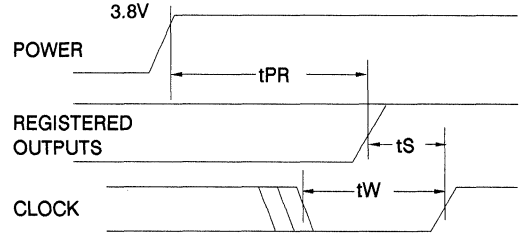
The registers in the ATV2500/H are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV2500/H fuse patterns. Once programmed, the outputs will read programmed during verify. The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits Preload and Q2 observability.

Atmel CMOS EPLDs

Atmel's Erasable Programmable Logic Devices utilize an advanced 1.25 micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for EPLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing EPLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64k to 1024k bit devices.

Using The ATV2500's Many Advanced Features

The ATV2500's flexibility puts more usable gates in 40 pins than other EPLDs. Some of the ATV2500's key features are:

- Asynchronous Clocks -

Each of the Flip-Flops in the ATV2500/H has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV2500/H clock period matches that of similar synchronous devices.

- A Total of 48 Registers -

The ATV2500/H provides two Flip-Flops for each Output Macrocell - a total of 48. Each register has its own clock and reset product terms, as well as its own SUM term.

- Independent I/O Pin and Feedback Paths -

Each I/O pin on the ATV2500/H has a dedicated input path. Each of the 48 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's Output Enable, facilitates designs using bi-directional I/O buses.

- 3 Sum Terms per Macrocell -

The ATV2500/H Macrocell can be configured with one Sum term feeding the output, and still have 2 Sum terms feeding the Flip-Flops. This is the simplest method for interfacing with an I/O bus, and no Flip-Flops need be sacrificed.

- Combinable Sum Terms -

Each Output Macrocell's 3 SUM terms can be combined in an OR gate before the Output or the Register. This provides up to 12 product terms per Output or Flip-Flop. When the Registered Output configuration is chosen, 8 terms are automatically available to D1. The 4 terms feeding D2 can also be shared with D1, giving it a total of 12. In the combinatorial mode, 4, 8, or 12 terms can feed the output, with the middle 4 still driving D1 and the bottom 4 still driving D2.

7

Programming Software Support

Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV2500/H is available from the following sources:

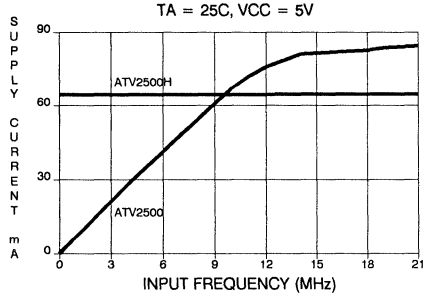
Data I/O / Futurenet Corp.	- ABEL 3.0, 3.1, and above
Logical Devices	- CUPL 3.0 and above
Atmel Corp.	-Atmel-ABEL™ 1.01

Erasure Characteristics

The entire memory array of an ATV2500/H is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

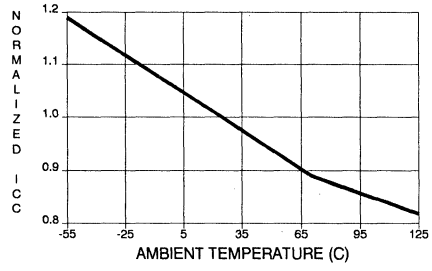
SUPPLY CURRENT vs. INPUT FREQUENCY

TA = 25C, VCC = 5V



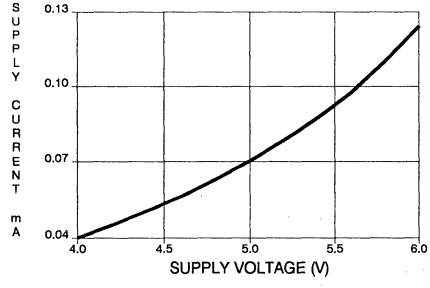
NORMALIZED ICC vs. AMBIENT TEMP.

f = 20 MHz, VCC = 5V



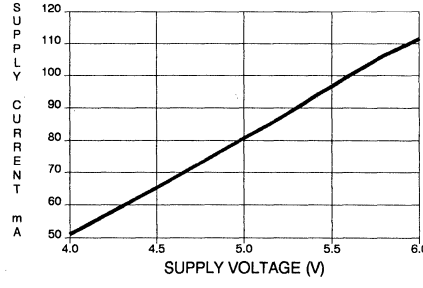
SUPPLY CURRENT vs. SUPPLY VOLTAGE

f = 0 HZ, TA = 25C



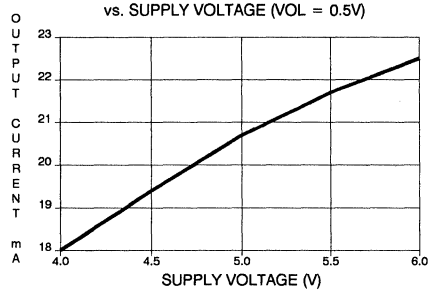
SUPPLY CURRENT vs. SUPPLY VOLTAGE

f = 20 MHz , TA = 25C



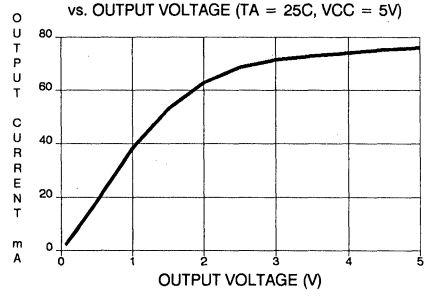
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (VOL = 0.5V)



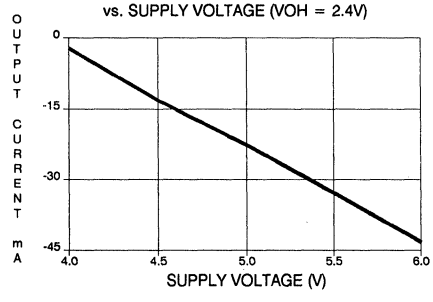
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



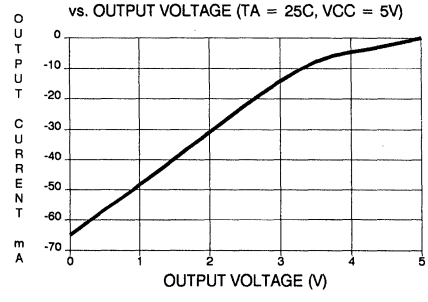
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V)

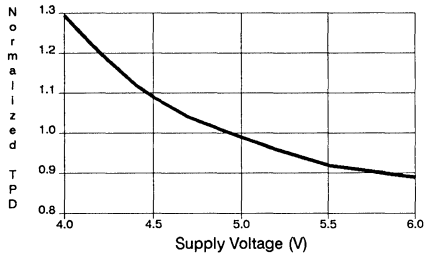


OUTPUT SOURCE CURRENT

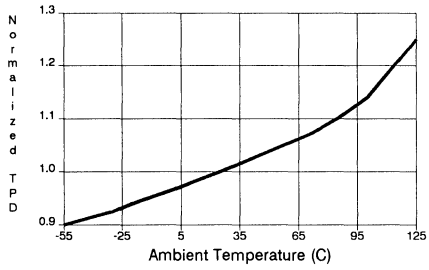
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



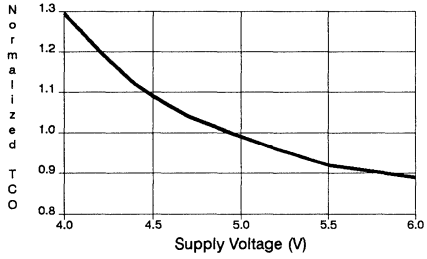
NORMALIZED TPD
vs. SUPPLY VOLTAGE



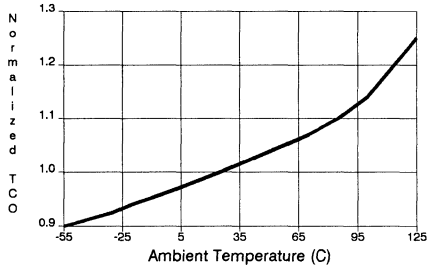
NORMALIZED TPD
vs. TEMPERATURE



NORMALIZED TCO
vs. SUPPLY VOLTAGE

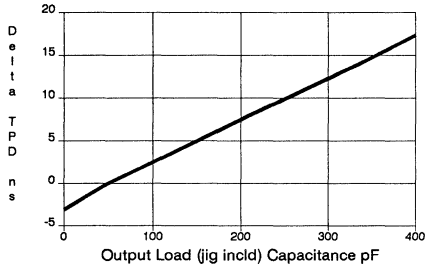


NORMALIZED TCO
vs. TEMPERATURE



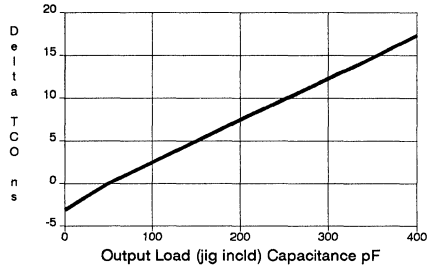
DELTA TPD vs. OUTPUT LOADING

TA = 25C, VCC = 5V



DELTA TCO vs. OUTPUT LOADING

TA = 25C, VCC = 5V



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Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	30	33	ATV2500-30DC ATV2500-30JC ATV2500-30KC ATV2500-30LC ATV2500-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
35	35	28	ATV2500-35DC ATV2500-35JC ATV2500-35KC ATV2500-35LC ATV2500-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500-35DI ATV2500-35JI ATV2500-35KI ATV2500-35LI ATV2500-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500-35DM ATV2500-35KM ATV2500-35LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500-35DM/883 ATV2500-35KM/883 ATV2500-35LM/883	40DW6 44KW 44LW	Military (-55°C to 125°C) Class B, Fully Compliant
40	40	25	ATV2500-40DC ATV2500-40JC ATV2500-40KC ATV2500-40LC ATV2500-40PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500-40DI ATV2500-40JI ATV2500-40KI ATV2500-40LI ATV2500-40PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500-40DM ATV2500-40KM ATV2500-40LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500-40DM/883 ATV2500-40KM/883 ATV2500-40LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
45	45	22	ATV2500-45DI ATV2500-45JI ATV2500-45KI ATV2500-45LI ATV2500-45PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
45	45	22	ATV2500-45DM ATV2500-45KM ATV2500-45LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500-45DM/883 ATV2500-45KM/883 ATV2500-45LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	25	40	ATV2500H-25DC ATV2500H-25JC ATV2500H-25KC ATV2500H-25LC ATV2500H-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-25DI ATV2500H-25JI ATV2500H-25KI ATV2500H-25LI ATV2500H-25PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-25DM ATV2500H-25KM ATV2500H-25LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-25DM/883 ATV2500H-25KM/883 ATV2500H-25LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	30	33	ATV2500H-30DC ATV2500H-30JC ATV2500H-30KC ATV2500H-30LC ATV2500H-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-30DI ATV2500H-30JI ATV2500H-30KI ATV2500H-30LI ATV2500H-30PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-30DM ATV2500H-30KM ATV2500H-30LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-30DM/883 ATV2500H-30KM/883 ATV2500H-30LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	35	28	ATV2500H-35DC ATV2500H-35JC ATV2500H-35KC ATV2500H-35LC ATV2500H-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-35DI ATV2500H-35JI ATV2500H-35KI ATV2500H-35LI ATV2500H-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-35DM ATV2500H-35KM ATV2500H-35LM	40DW6 44KW 44LW	Military (-55°C to 125°C)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
35	35	28	ATV2500H-35DM/883 ATV2500H-35KM/883 ATV2500H-35LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)

Using the ATV2500 with ABEL™ and CUPL™

The following two examples show example headers to use when designing the ATV2500 with ABEL™ or CUPL™.

For ABEL™, the node numbers shown may be assigned any legal ABEL™ label. The fuse numbers for combining the product terms are included.

For CUPL™, the pinnodes shown may be assigned any legal CUPL™ label. Combining the product terms is handled automatically.

ABEL™ Example

```
module _NODE2500
title 'Addressing 48 Registers in V2500
NODE2500 device 'P2500';
        @message 'Use P2500PC device file.';
        @message 'for ABEL on a PC/Clone';
"Inputs
I1,I2,I3                        pin     1,2,3;
I17,I18,I19,I20,I21,I22,I23     pin     17,18,19,20,21,22,23;
I37,I38,I39,I40                 pin     37,38,39,40;
"I/Os
O4,O5,O6,O7,O8,O9               pin     4,5,6,7,8,9;
O11,O12,O13,O14,O15,O16         pin     11,12,13,14,15,16;
O24,O25,O26,O27,O28,O29         pin     24,25,26,27,28,29;
O31,O32,O33,O34,O35,O36         pin     31,32,33,34,35,36;

"Q2 Registers
"Node Name          Node    Number          Pin Associated With:
B4,B5,B6            node    41,42,43;       " pin 4 to pin 6
B7,B8,B9            node    44,45,46;       " pin 7 to pin 9
B11,B12,B13         node    47,48,49;       " pin 11 to pin 13
B14,B15,B16         node    50,51,52;       " pin 14 to pin 16
B24,B25,B26         node    53,54,55;       " pin 24 to pin 26
B27,B28,B29         node    56,57,58;       " pin 27 to pin 29
B31,B32,B33         node    59,60,61;       " pin 31 to pin 33
B34,B35,B36         node    62,63,64;       " pin 34 to pin 36
"Q1 Registers
"Node Name          Node    Number          Pin Associated With:
Q4,Q5,Q6            node    217,218,219;    " pin 4 to pin 6
Q7,Q8,Q9            node    220,221,222;    " pin 7 to pin 9
Q11,Q12,Q13         node    223,224,225;    " pin 11 to pin 13
Q14,Q15,Q16         node    226,227,228;    " pin 14 to pin 16
Q24,Q25,Q26         node    229,230,231;    " pin 24 to pin 26
Q27,Q28,Q29         node    232,233,234;    " pin 27 to pin 29
Q31,Q32,Q33         node    235,236,237;    " pin 31 to pin 33
Q34,Q35,Q36         node    238,239,240;    " pin 34 to pin 36
```

High Density UV Erasable Programmable Logic Device

Application Brief

7

CUPL™ Example

```
Name        NODE2500
Partno      00;
Date        11/21/88;
Revision    00;
Designer    J. Yu
Company     Atmel;
Assembly    None;
Location    None;
Device      V2500;
/*****************************************/
/** Allowable Target Device Types : V2500      **/
/*****************************************/
/** Inputs **/
/* This is a handy way to name a set of pins */
PIN [1..3]      =       [I1..I3];
PIN [17..23]    =       [I17..I23];
PIN [37..40]    =       [I37..I40];
/**  I/Os      **/
PIN [4..9]      =       [O4..O9];
PIN [11..16]    =       [O11..O16];
PIN [24..29]    =       [O24..O29];
PIN [31..36]    =       [O31..O36];
/** Declarations and Intermediate Variable Definitions */
/* Q2 nodes                                Pin assoc. with:*/
PINNODE [41..46]   = [B4..B9];      /*PIN 4 to 9*/
PINNODE [47..52]   = [B11..B16];    /*PIN 11 to 16*/
PINNODE [53..58]   = [B24..B29];    /*PIN 24 to 29*/
PINNODE [59..64]   = [B31..B36];    /*PIN 31 to 36*/
/* Q1 nodes                                Pin assoc. with:*/
PINNODE [65..70]   = [Q4..Q9];      /*PIN 4 to 9*/
PINNODE [71..76]   = [Q11..Q16];    /*PIN 11 to 16*/
PINNODE [77..82]   = [Q24..Q29];    /*PIN 24 to 29*/
PINNODE [83..88]   = [Q31..Q36];    /*PIN 31 to 36*/
etc.
```

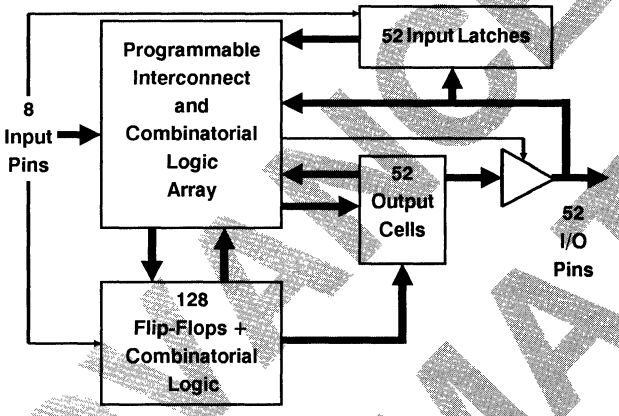
Features

- Advanced Programmable Logic Device - High Gate Utilization
- Flexible Interconnect Architecture - Universal Routing
- Flexible Logic Cells - 128 Flip-Flops and 52 Latches
- Synchronous or Asynchronous Registers
- High Speed - 50 MHz Operation
- Complete Third Party Software Support
  No Placement, Routing or Layout Software Required
- Proven and Reliable High Speed CMOS EPROM Process

Programmable Logic Device

Advance Information

Block Diagram



Description

The ATV5000 is an easy to use, high density programmable logic device. Its simple, regular architecture and very flexible resource configuration translate into increased utilization and high performance.

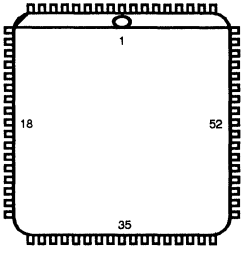
The ATV5000 is organized around one programmable interconnect and combinatorial logic array (see block diagram above). This guarantees easy interconnection of and uniform performance from all nodes. Logic is grouped into "sum terms", which are easy to use groupings of AND-OR gates. Sum terms can be wire-or'd together to integrate larger logic blocks. Buried sum terms can be fed back into the logic array to expand the levels of logic. The 52 I/O pins can each be driven by a register or a sum term. Each I/O pin has an indivually enabled input latch.

All 128 registers are configurable without using extra logic gates. Individual sum terms, asynchronous presets, resets and clocks give each flip-flop added flexibility. An input pin clock option guarantees synchronization and fast clock to output performance.

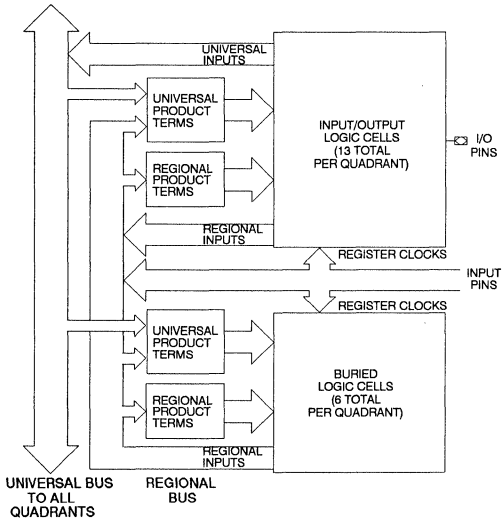
The ATV5000 will be supported by standard, off-the-shelf third party software tools and programmers, minimizing start-up investment and improving product support.

Chip Carrier Pin Configuration

Pin Name	Qty.	Function
I	8	Logic and Clock Inputs
I/O	52	Bidirectional Buffer
VCC	4	+5V Supply
GND	4	



Functional Logic Diagram ATV5000



Logic Diagram Description

The ATV5000's logic resources are grouped into 52 identical Input/Ouput logic cells and 24 identical buried logic cells. Each I/O cell has 2 flip-flops, up to 3 sum terms, individual clock, reset, and preset terms per flip-flop, and one output enable term. Independent of output configuration, all flip-flops are always usable, and have at least 4 Product Term inputs each.

Each I/O pin (52 total) can be used directly or latched, with one latch clock per quadrant.

The ATV5000 has 4 identical quadrants. The Universal Bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ regionally. The 8 input-only pins are available in all 4 regional buses.

Each logic cell has a number of "regional" and "universal" product terms. The I/O Logic Cells contain 3 sum terms, 2 flip-flops, and an I/O buffer.

The Buried Logic Cells each contain 1 flip-flop. In addition, each buried logic cell sum term can be fed back into the regional bus. This allows for logic expansion.

Register preload and observability are incorporated serially to simplify testing. All registers automatically clear at power up.

D.C. Characteristics (Preliminary)

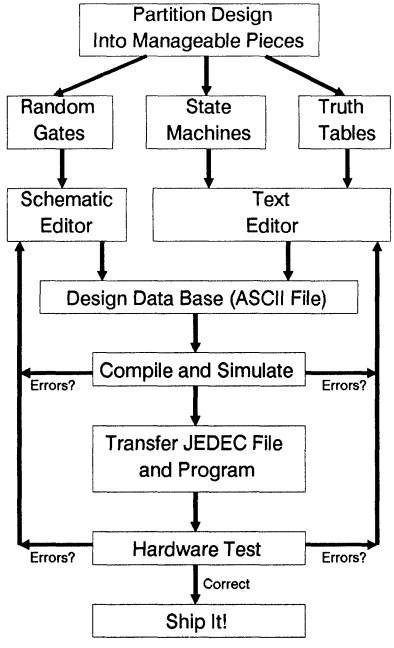
Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V				10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		20	40	mA
			Ind.,Mil.		20	50	mA
I_{CC2}	Clocked Power Supply Current	f = 1MHz, V_{CC} = MAX Outputs Open	Com.		30	50	mA
			Ind.,Mil.		30	60	mA
V_{IL}	Input Low Voltage			-0.6		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8mACom,Ind;6mA Mil.				0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100µA (CMOS Load)		V_{CC}-0.3			V
		I_{OH} = -4.0mA (TTL Load)		2.4			V

A.C. Characteristics (Preliminary)

Symbol	Parameter	ATV5000-25		ATV5000-30		Units
		Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-Registered Output		25		30	ns
t_{EA1}	Input to Output Enable		25		30	ns
t_{COS}	Clock to Output (Synchronous)		15		20	ns
t_{CO}	Clock to Output (Asynchronous)		25		30	ns
t_{SI}	Input Latch Setup Time	15		18		ns
t_H	Input Latch Hold Time	0		0		ns
t_{SIS}	Input Setup Time (Synchronous)	15		20		ns
t_{HS}	Input Hold Time (Synchronous)	0		0		ns
t_{SIA}	Input Setup Time (Asynchronous)	10		12		ns
t_{HA}	Input Hold Time (Asynchronous)	7		10		ns
t_W	Clock Width	7		10		ns
t_P	Clock Period	20		25		ns
F_{MAX}	Maximum Frequency (1/t_P)		50		40	MHz

7

Design Flow Diagram



Using The ATV5000

The ATV5000's simple, regular architecture means that only simple logic compilers are required to configure the device. No layout or route and place are required. These software tools are readily available from companies such as Data I/O Corporation (ABEL™), Logical Devices (CUPL™), and ISDATA (LOGiC™).

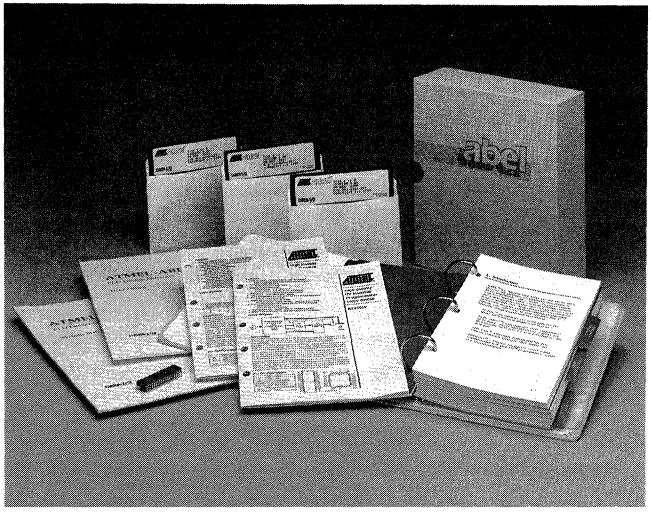
The first step in designing a device as complex as the ATV5000 is to partition your design into manageable blocks. These blocks are then allocated proportionally to each of the four quadrants of the ATV5000. Random gates can be described either with boolean equations (a behavioral description) or with a schematic editor. Truth table logic and state machines are best described behaviorially and entered with a text editor. The design is then combined into one ASCII file, which is then submitted to the logic compiler. Compilation, logic reduction, simulation, JEDEC file creation and documentation are then completed by all of the popular compilers.

After correcting any syntax and logic errors discovered by the compiler, the JEDEC file is ready to download to an EPLD programmer. These are available from a number of manufacturers. Programmed devices are usually first tested in the programmer with your supplied test vectors. The next step is check out your "custom chip" in the target system. When this hardware debug step is complete, your system is ready to go - all in a matter of hours.

ABEL™ is a trademark of Data I/O Corporation.
CUPL™ is a trademark of Logical Devices.
LOGiC™ is a trademark of ISDATA.

Features

- **Atmel-ABEL Uses the Industry-Standard Natural Design Language**
- **Multiple Input Methods :**
  Boolean Equations, Truth Tables and State Diagrams
- **Automatic - Logic Reduction, Simulation, Error Checking,**
  and Generation of Design Documentation
- **Automatically Takes Advantage of Atmel's EPLD Architecture,**
  Joining Sum Terms When Extra Product Terms are Needed
- **Runs on MS-DOS™ Compatible Personal Computers**
- **This Inexpensive Package Includes:**
  Atmel-ABEL Software which Supports the ATV750 and ATV2500
  Design Examples
  Complete ABEL Manual
  Sample ATV2500-35DC
- **Special Offers and Coupons**



High-Level Design Tool for Atmel Programmable Logic Devices: ATV750 ATV2500

7

Description

Atmel Programmable Logic Devices (PLD's) offer powerful solutions for logic design. Atmel-ABEL, developed by Data I/O Corporation, is a software package specifically designed to support developement with Atmel Programmable Logic Devices.

Atmel-ABEL automatically takes advantage of Atmel's innovative multiple sum term PLD architecture. When your reduced equations require more product terms than anticipated, the software automatically allocates the next available block of product terms to your equation.

Atmel-ABEL automatically reduces your logic equations to near minimal form. Depending on your requirements, you can choose among several reduction algorithms. The result is a more efficient, cost-effective design.

Behavioral simulation is an integral part of the Atmel-ABEL design package. Simulation is automatic and software-based so that you can verify your design and test vectors before you program your first device.

Once your design is ready, Atmel-ABEL generates standard JEDEC files which can be downloaded to your programmer with the terminal emulation software included with the package.

ABEL™ is a trademark of Data I/O Corporation.
MS-DOS™ is a trademark of Microsoft Corporation.

Programming Software Companies

Data I/O Corporation (ABEL™)
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

Logical Devices (CUPL™)
1321 N.W. 65 Place
Ft. Lauderdale, FL 33309
(305) 974-0967
(800) 331-7766

ISDATA Gmbh (LOG/iC)
Haid-und-Neu- Str. 7
D-7500 Karlsruhe 1
West Germany
0721 / 69309

C/O Adams MacDonald Enterprises
800 Airport Rd.
Monterey, CA 93940
(408) 373-3607
(800) 777-1202

PistoHl Electronic Tool Co.
22560 Alcalde Rd.
Cupertino, CA 95014
(408) 255-2422
(800) 2PISTOHL

ACCEL Technologies, Inc.
6825 Flanders Drive
San Diego, CA 92121
(800) 433-7801

Programming Hardware Companies

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118

PistoHl Electronic Tool Co.
22560 Alcalde Rd.
Cupertino, CA 95014
(408) 255-2422

Logical Devices
1321 N.W. 65 Place
Ft. Lauderdale, FL 33309
(305) 974-0967
(800) 331-7766

SMS
C/O Adams MacDonald Enterprises
800 Airport Rd.
Monterey, CA 93940
(408) 373-3607

BP Microsystems
10681 Haddington #190
Houston, TX 77043
(713) 461-9430

Advin Systems, Inc.
1050-L East Duane Ave.
Sunnyvale, CA 94086
(408) 984-8600

System General
510 South Park Victoria Drive
Milipitas, CA 95035
(408) 263-6667

Inlab
2150 I W 6th Ave
Broomfiled, CO 80020
(800) 237-6759

CMOS EPLD Programming Hardware and Software Support

7

ATMEL

CONTENTS

Section 8

CMOS Gate Arrays

Features

- 0.8µm effective gate lengths (1.0µm drawn) combined with close metal spacing provides outstanding speed/power performance
- Modified channeless architecture provides higher utilization ranging from 2,600 to 130,000 usable gates
- I/O counts from 60 to 320 reduce the number of off-chip transactions for increased system performance
- Design translation from other libraries provides for easy alternate sourcing
- Cell library contains...
  - Over 50 logic functions and memory cells
  - "Soft" macrocells
  - Serial Scan and Boundary Scan macrocells
- Scan Path/Built-In Self Test provide shorter test times
- User-friendly design tools support...
  - Design Statistics
  - Network Synthesis
  - Logic Optimization
  - Fault Grading
  - Worst-case Path Delay Estimates
  - Functional and Timing Simulation
  - Test Program Generation
- Wafer fabrication, packaging and screening in a U.S. facility

Description

The high-performance ATL Series CMOS gate arrays offer superior system performance, flexibility, testability and board utilization. The ATL gate arrays employ 1.0µm-drawn (0.8µm-effective), double-level metal, Si-gate, CMOS technology processed in a U.S.-based, advanced manufacturing facility.

The arrays utilize a modified channeless architecture in which routing channels with four routing lanes provide greater than 50 percent usable gates. This efficient routing scheme combined with close spacing for both metal layers allows the highest usable gate densities.

Clock and power distribution schemes are designed to minimize skew and voltage drop. Scan-compatible flip-flops and shadow registers in the I/O cells provide for improved testability.

ATL Array Organization

Device	ATL4	ATL10	ATL20	ATL60	ATL130	ATL260
Total Gates	4K	10K	22K	57K	131K	257K
Usable Gates	2.6K	6.5K	12K	30K	67K	130K
Total Pins	68	124	144	224	256	360
I/O	60	116	136	208	236	320

1-MICRON CMOS GATE ARRAYS

ATL4
ATL10
ATL20
ATL60
ATL130
ATL260
Preliminary

8

ASIC Design Flow

Netlist Translation

Design netlists existing in a customer's format can be automatically translated into Atmel's gate array cell library.

Library

Atmel provides the cell library, with schematic symbols, functional models, and timing models, on the customer's workstation. Simulators supported include Quicksim, AIDA, HILO and ZYCAD. Customer training in the library can be provided.

Logic Design

Schematic capture, simulation and test vector generation is typically a customer responsibility. Netlists and test vectors provide an unambiguous interface between the customer and Atmel.

Netlist Validation

Upon receipt of a customer's design, Atmel performs netlist checks for common CMOS design problems. Any issues are then resolved with the customer. Next, the netlist is simulated using customer provided vectors to insure a valid starting point for physical design.

Placement and Routing

Automatic placement and routing are performed using a number of physical design tools. Both placement and routing can be influenced by high priority nets in the netlist. Placement tools support force-directed placement, pair wise swapping for optimized wire length, and congestion smoothing. Routing systems include global assignment, channel routing, maze routing and rip up/retry routers. Manual intervention in placement and routing is supported for critical portions of the circuit.

Verification

Post-route verifcation includes design rule checks, layout versus schematic checks, and interconnect capacitance extraction for back annotation.

Post-Route Simulation

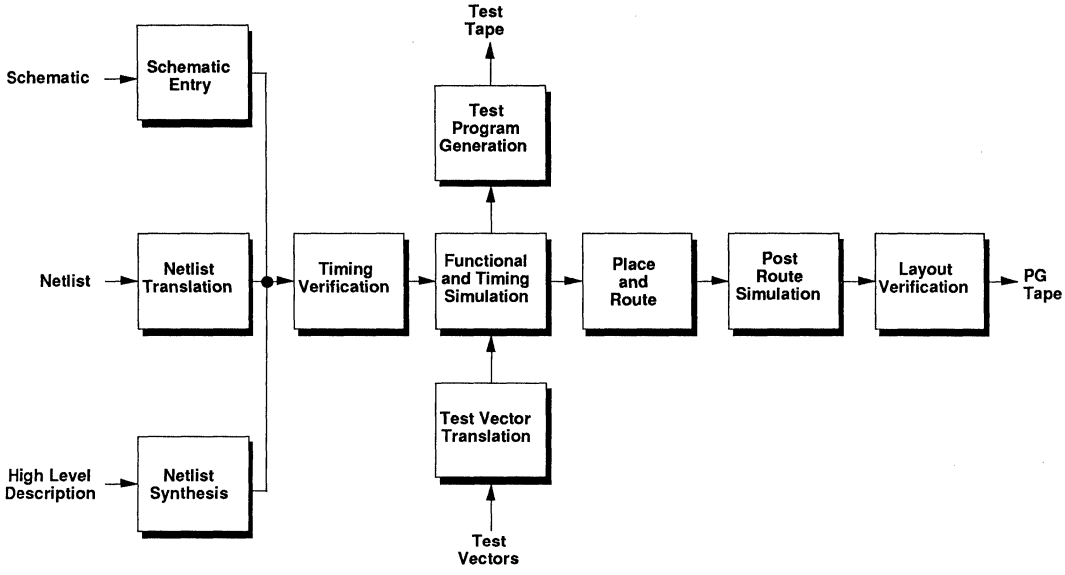
Using the interconnect capacitance extracted above, the as-routed timing performance is verified. This can be done by Atmel, the customer, or both.

Test Vector Translation

Atmel provides translation of the simulation results to its foundry's tester format. Sentry™ and Ando™ testers are supported. Additional test support, in the form of fault grading and automatic test vector generation can be provided.

Final Design Review

Prior to fabrication, the layout, simulation and verification are reviewed and approved by the customer.



Performance Optimized Cell Library

Atmel's ATL series gate arrays use cells from an accurately modeled and highly flexible library. The cell library contains over 50 hard-wired data path elements, ranging from inverters to flip-flops, adders, and multiplexers. Each cell has been characterized via extensive SPICE modeling at the transistor level and verification of the simulation results through measurements made on processed arrays. Characterization has been done over the military temperature and voltage ranges, and worst-case process limits to ensure an accurate estimate of worst-case delays. SCAN flip-flops with Reset control are also available.

Cell Guide

BUFFERS AND INVERTERS

1X Inverter	4X Inverter
Dual 1X Inverter	1X Buffer
Quad 1X Inverter	2X Buffer
2X Inverter	3X Buffer
Dual 2X Inverter	4X Buffer
3X Inverter	QUAD Tri-State Inverter

AND, NAND, OR, NOR GATES

2-input NAND	2-input AND
Dual 2-input NAND	3-input AND
3-input NAND	2-input NOR
4-input NAND	Dual 2-input NOR
5-input NAND	3-input NOR
6-input NAND	4-input NOR
8-input NAND	2-input OR

MULTIPLEXERS

2:1 MUX
2:1 MUX w/Enable
QUAD 2:1 MUX
QUAD 2:1 MUX w/Enable
4:1 MUX
8:1 MUX
8:1 MUX w/Enable

EXCLUSIVE OR/NOR GATES

2-input Exclusive OR
2-input Exclusive NOR
1-bit Adder

AND/OR, OR/AND Gates

3-input AND/OR/INVERT
4-input AND/OR/INVERT
7-input AND/OR/INVERT
3-input OR/AND/INVERT
4-input OR/AND/INVERT

DECODERS

2:4 Decoder
2:4 Decoder w/Enable
3:8 Decoder

FLIP-FLOPS/ LATCHES

D Flip-flop
D Flip-flop w/asynchronous CLR
D Flip-flop w/asynchronous RESET
D Flip-flop w/asynchronous SET
D Flip-flop w/asynchronous SET/RESET
JK Flip-flop
JK Flip-flop w/asynchronous CLR
QUAD Inverting Latch
Latch
Latch w/RESET
Latch w/SET
Latch w/SET/RESET
Perimeter D Flip-flop

SCAN CELLS

Set-Scan Register
QUAD Set-Scan Register w/Enable
QUAD Set-Scan Register w/Controls

I/O CELLS

All I/O's are designated as PAD cells followed by up to six fields defining capability. For example, a TTL input with 4K pull up would be PADIOOT4K.

P911 [F1] [F2] [F3] [F4] [F5] [F6]

Field 1:	B	- Bidirectional
	I	- Input
	O	- Output
	T	- Tristate Output
Field 2:	0-12	- N-Drive Value
Field 3:	0-12	- P-Drive Value
Field 4:	C	- CMOS
	T	- TTL
Field 5:	4K or 40K	- Pull-up Value
Field 6:	S	- SCHMITT

8

I/O Buffers

The ATL series input/output ring contains the I/O buffer circuitry, capable of sourcing and sinking currents up to 16mA, responding to either CMOS or TTL logic levels, and having ESD protection networks capable of withstanding a 2000V discharge. All outputs can be switched to a high impedance state. I/O locations on this ring can accomodate bidirectional cells.

- Programmable output drive (2 to 24mA I_{OL}, -4 to -48mA I_{OH})
- CMOS or TTL I/O configurable interface
- ESD input protection greater than 2000 volts
- Built-in configurable test logic
- High drive internal buffers
- High impedance state

CMOS/TTL Input Interface Characteristics

Interface	Logic High	Logic Low	Switchpoint
CMOS	3.5V Minimum	1.5V Maximum	Vdd/2 Typical
TTL	2.0V Minimum	0.8V Maximum	1.3V Typical

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V[1]

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

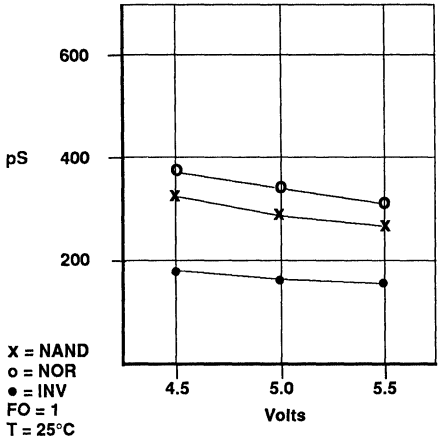
DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{CC} = 4.5V to 5.5V (unless otherwise noted)

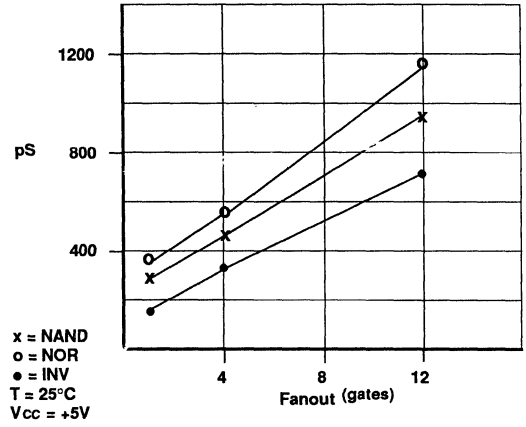
Symbol	Parameter	Test Condition	Min	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{CC} = 5.5V$		10	µA
I_{IL}	Input Leakage Low	$V_{IN} = 0, V_{CC} = 5.5V$			
	4K Pullup			1.35	mA
	40K Pullup			0.19	mA
I_{OL}	Output Leakage	$V_{OUT} = 0$ or V_{CC}, $V_{CC} = 5.5V$		10	µA
V_{IL}	TTL Input Low Voltage	$V_{CC} = 5.5V$		0.8	V
V_{IL}	CMOS Input Low Voltage	$V_{CC} = 5.0V$		1.5	V
V_{IH}	TTL Input High Voltage	$V_{CC} = 4.5V$	2.0		V
V_{IH}	CMOS Input High Voltage	$V_{CC} = 5.0V$	3.5		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 2mA I_{OL} per stage.	$V_{CC} = 4.5V$		0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -4mA I_{OH} per stage.	$V_{CC} = 4.5V$	3.5		V

AC Characteristics

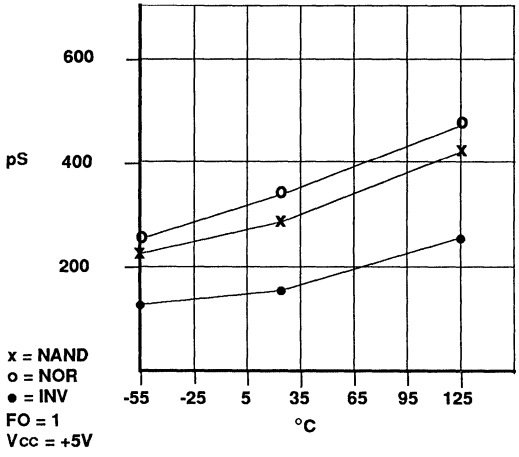
Delay vs V_{CC}



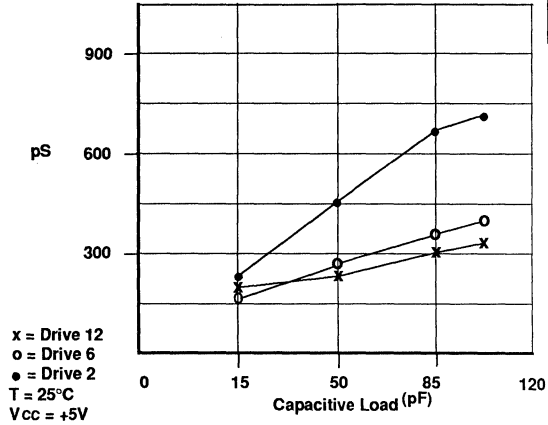
Delay vs Fanout



Delay vs Temperature



Output Buffer vs Load



Power Dissipation

Power dissipation is typically 5µW/MHz per active gate switching during a clock period.

Design for Testability

Today's designs often carry demanding component and system-level functional test and maintenance requirements. Atmel's arrays support a full range of Design-for-Test (DFT) testability improvement techniques, which reduces design debug time, component test time, board and system test times and improves system diagnostics.

Designs that permit easy application of stimuli and examination of responses are necessary to make circuits thoroughly functionally testable. Serial Scan techniques, using specially designed registers, improve this controllability and observability by allowing the establishment of scan paths deep inside the circuit logic. Serial patterns can be loaded into these registers and signature analysis techniques used to provide an easy means of determining circuit functionality. This testability improvement method is supported on each of the ATL arrays.

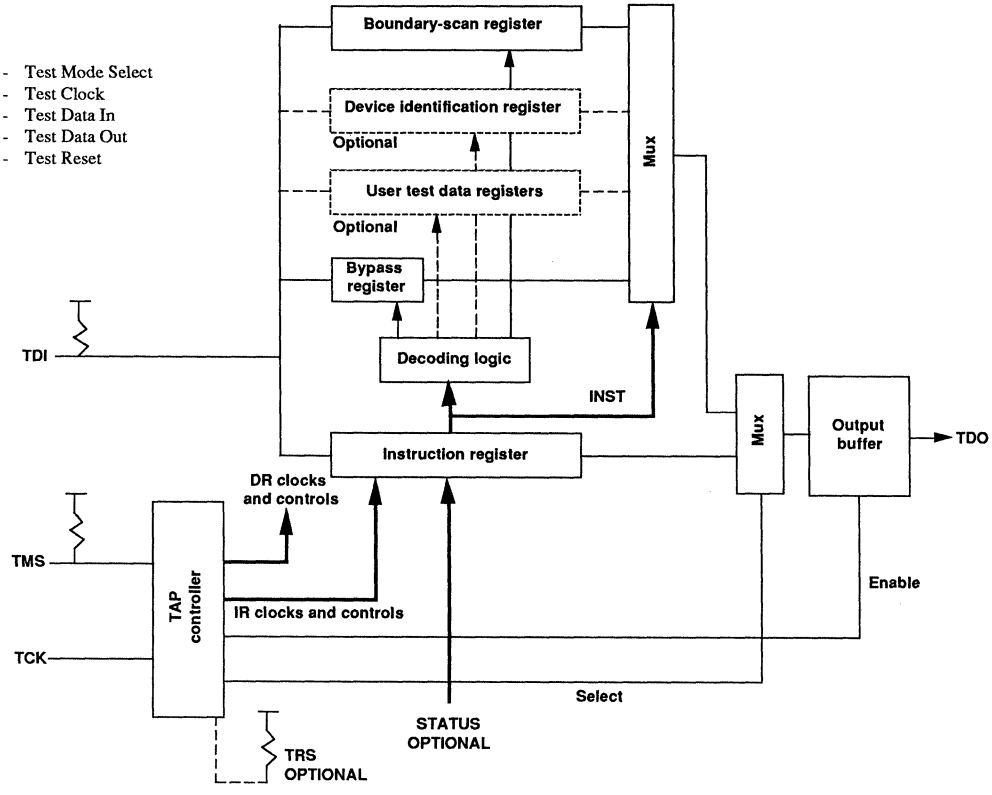
Shadow registers, included in the I/O buffer cells for the arrays, facilitate the use of Boundary Scan techniques. This testability improvement method, coupled with Serial Scan techniques, provides excellent fault isolation within the array as well as simplifying the testing of interconnects on the board. Scan registers in the periphery can be configured to generate pseudo-random test patterns and signature analysis registers, thus acting as on-chip test pattern generators.

The Joint Testability Action Group (JTAG) macros also feature Built-In Self Test circuitry. This permits testability access to IEEE proposed standards through only four package pins. This extra circuitry, contained in a soft macro, further relieves the designer of the task of developing detailed testability controller designs.

Atmel uses TDS™ software from Test Systems Strategies Inc. (TSSI™) as its primary test program generator for high-performance ASICs. Functional test programs are generated from the simulation files and formatted to be compatible with high speed, high pin-count ANDO & Sentry testers. This software tool can save the designer weeks of tedious test vector generation and debugging.

JTAG Architecture

TMS - Test Mode Select
TCK - Test Clock
TDI - Test Data In
TDO - Test Data Out
TRS - Test Reset



Advanced Packaging

Atmel offers its ATL series in packages designed to maintain the performance edge obtained in the silicon. Leaded and leadless chip carriers, pin grid arrays, flatpacks, dual-in-line packages and tape automated bonded (TAB) packages are available.

When a standard package can't meet a customer's specific needs, Atmel can design a package to precisely fit the application.

Atmel's close working relationship with both domestic and foreign package suppliers ensures a first-pass design success. The Company has proven success in the design and volume delivery of dozens of custom packages. Atmel's new packaging facility includes the capability for screening to commercial, industrial, Class B, and Class S levels.

Packaging Options

	Maximum Pins	DIP	LCC	LDCC	Flatpack	PGA	TAB/Custom
ATL4	68	X	X	X	X	X	
ATL10	124			X	X	X	
ATL20	144			X	X	X	X
ATL60	224			X	X	X	X
ATL130	256				X	X	X
ATL260	360					X	X

8

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CONTENTS

Section 9

CMOS Analog

Features

- High Accuracy Programmable Gain Amplifiers
  - ± 0.02 dB Accuracy (Typical)
  - 31.5 dB Range in 0.5 dB Steps
- Software Programmable Group Delay Equalizer For Leased and Dial-Up Lines
- High Dynamic Range - over 90 dB
- On-Chip Anti-Aliasing Filters
- Microcomputer Interface with Serial Data Port
- Three Convenient Clock Options
  - 11.0592 MHz
  - 3.6864 MHz
  - 2.4576 MHz (or 2.56 MHz)
- Operates from +/- 5 V Supplies
- Low Power Standby Mode - 100 μA (Typical)
- TTL and CMOS Compatible Digital Interface
- Economical 16-Lead Package
- Full Military, Commercial and Industrial Temperature Ranges

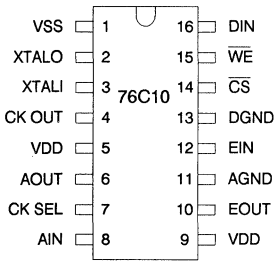
CMOS Programmable Amplifier

Delay Equalizer

Description

The AT76C10 integrates two Programmable Gain Amplifiers and a Programmable Telephone Line Group Delay Equalizer on a monolithic substrate. It is fabricated in a state-of-the-art, low power CMOS process. The Gain and Group Delay steps are controlled by a 7-bit configuration code which can be programmed in real time. The AT76C10 is implemented in an advanced switched-capacitor technology and is designed to provide precise Gain and Group Delay compensation for low bit-error-rate data transmission over dial-up and leased lines. Anti-alias and clock filters are included on-chip as the AT76C10 employs sampled-data techniques, and external filters are not required for most applications.

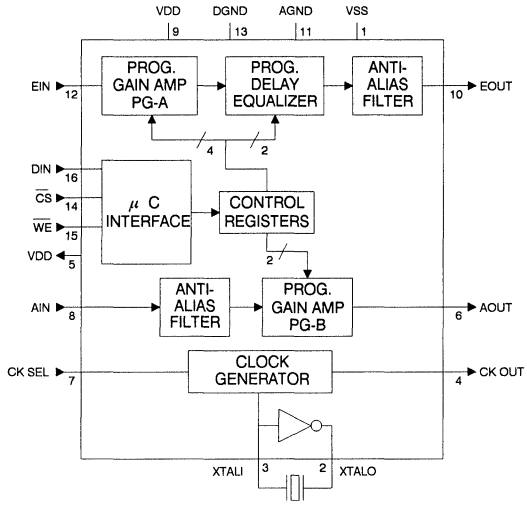
Pin Configuration



Pin Definitions

No.	Pin Name	Function
1	VSS	Negative Power Supply. Nominal -5 Volts.
2	XTALO	Crystal Oscillator Output.
3	XTALI	Crystal Oscillator Input.
4	CK OUT	Sampling Clock Output. (Open Drain)
5	VDD	Connect to VDD.
6	AOUT	PG-B Analog Signal Output.
7	CK SEL	Clock Select. Selects one of the 3 recommended Clock frequencies.
8	AIN	PG-B Analog Signal Input.
9	VDD	Positive Power Supply. Nominal +5 Volts.
10	EOUT	Delay Equalizer Analog Signal Output.
11	AGND	Analog Ground.
12	EIN	Delay Equalizer Analog Signal Input.
13	DGND	Digital Ground.
14	$\overline{CS}$	Chip Select Control Input.
15	$\overline{WE}$	Write Enable Control Input.
16	DIN	Serial Data Input.

Block Diagram



Device Operation

The AT76C10 is designed for use in the signal paths of a modem or voice/data phone to minimize the bit-error-rate over dial-up and leased lines. Gain and Group Delay response of the AT76C10 are controlled by a serial 7-bit configuration code. D1 and D0 of the configuration code are the address bits which select one of the three control registers. Bits D2 to D5 set the gain and delay equalizer steps. D6 is an option bit which controls the power down mode. All the functions associated with the configuration code are summarized in Tables 1 to 4.

Configuration Code Format

D6	D5	D4	D3	D2	D1	D0
OPTION SELECT	CONTROL CODE				ADDRESS	

This chip can be used as part of an adaptive equalizer for medium to high speed modems (1200 bps to greater than 19.2K bps). The configuration code is loaded into the chip at a serial data input port and updated in real time. The amplitude response of the equalizer is nominally at 0 dB with negligible ripple. The AT76C10 can also be used as a fixed compromise delay equalizer.

PROGRAMMABLE GAIN AMPLIFIER: The AT76C10 provides two high dynamic range amplifiers for maximizing signal-to-noise ratio. Amplifier PG-A offers 16 programmable gain steps from 0 dB to 7.5 dB in 0.5 dB steps. Amplifier PG-B provides -8 to 16 dB of gain in 8 dB steps. The two amplifiers can be cascaded to provide 31.5 dB range of programmable gain in 0.5 dB steps. The Programmable Amplifiers can be used as an Automatic Gain Control Circuit or as a fixed gain adjustment.

PROGRAMMABLE GROUP DELAY EQUALIZER: The Group Delay Equalizer is designed to provide programmable compromise group delay compensation to achieve low bit-error-rate data transmission. Four group delay responses are provided to accommodate the majority of conditioned as well as unconditioned lines. The first three responses are recommended for line types C2 and C1, while the fourth response can be used for 3002-type lines. Two or more AT76C10s can be cascaded to obtain additional group delay compensation.

CONTROL REGISTERS: Four control registers are used to store the configuration codes for the gain steps of PG-A and PG-B, the delay steps of the Delay Equalizer, and the control bit for the power-down mode.

MICROCOMPUTER INTERFACE: Control inputs $\overline{CS}$ and $\overline{WE}$ and serial data input DIN allow the AT76C10 to be easily interfaced with most popular microcontrollers. All digital I/Os are TTL as well as CMOS compatible.

WRITE OPERATION: To program a configuration code into a particular control register, the voltage at $\overline{CS}$ has to be brought low while the data bits appearing at DIN are strobed in at the rising edge of $\overline{WE}$. At the rising edge of $\overline{CS}$, the last 7 input data bits are latched into the control registers.

POWER-DOWN MODE: To minimize power consumption for battery powered applications and in certain linecard applications, the AT76C10 provides a low power standby mode of operation. In the power-down mode, the analog outputs go into a high impedance state. The power-down mode is initiated by writing a "0" into the power-down register. Once in the power-down mode, the AT76C10 can be reactivated by writing a "1" into the power-down register. It should be noted that upon powering up the AT76C10 for the first time, it automatically goes into the normal active mode of operation.

CRYSTAL OSCILLATOR: Internal timing of the chip is generated either by connecting a crystal across pins XTALI and XTALO of the on-chip oscillator, or by applying an external clock at pin XTALI. In the latter case, pin XTALO should be left unconnected. To accommodate different applications, three clock options: 2.4576 MHz, 3.6864 MHz and 11.0592 MHz, can be selected via control pin CK SEL. For applications in a linecard environment, a 2.56 MHz clock can be used instead of the 2.4576 MHz clock. The 153.6 KHz (160 KHz with 2.56 MHz clock) sampling clock is available as an open drain output at CK OUT for synchronization or driving other circuits, e.g. the transmit or receive filters, or A/D and D/A converters.

CK SEL	Recommended XTAL Frequency	CK OUT
VDD	11.0592 MHz	153.6 KHz
DGND	3.6864 MHz	153.6 KHz
VSS	2.4576 MHz	153.6 KHz
VSS	2.56 MHz	160.0 KHz

Group Delay Characteristics (Microseconds)

Fs = 153.6 KHz

Frequency (Hz)	Step #1	Step #2	Step #3	Step #4
300	158	278	416	284
600	188	336	502	386
900	237	463	681	680
1200	325	671	985	1360
1500	431	890	1330	1791
1700	462	938	1382	1838
1900	435	897	1305	1810
2100	372	777	1144	1510
2400	266	542	808	683
2700	181	361	534	342
3000	136	250	368	213
3300	102	182	267	148

Table 1. Option Selection

Address D1	Address D0	Option Bit D6	Function
0	0	1	
0	1	1	Updates Control Registers
1	0	1	
1	1	0	Power Down Mode
1	1	1	Active Mode

Table 2. Equalizer Selection

Address D1	Address D0	Control Code D5	D4	D3	D2	Equalizer Step No.	Recommened Line Condition
0	0	X	X	0	0	1	C2
0	0	X	X	0	1	2	C1
0	0	X	X	1	0	3	C1
0	0	X	X	1	1	4	3002

Table 3. Programmable Gain Amplifier, PG-A

Address D1	Address D0	Control Code D5	D4	D3	D2	PG-A Step No.	PG-A Gain (dB)
0	1	0	0	0	0	1	0.0
0	1	0	0	0	1	2	0.5
0	1	0	0	1	0	3	1.0
0	1	0	0	1	1	4	1.5
0	1	0	1	0	0	5	2.0
0	1	0	1	0	1	6	2.5
0	1	0	1	1	0	7	3.0
0	1	0	1	1	1	8	3.5
0	1	1	0	0	0	9	4.0
0	1	1	0	0	1	10	4.5
0	1	1	0	1	0	11	5.0
0	1	1	0	1	1	12	5.5
0	1	1	1	0	0	13	6.0
0	1	1	1	0	1	14	6.5
0	1	1	1	1	0	15	7.0
0	1	1	1	1	1	16	7.5

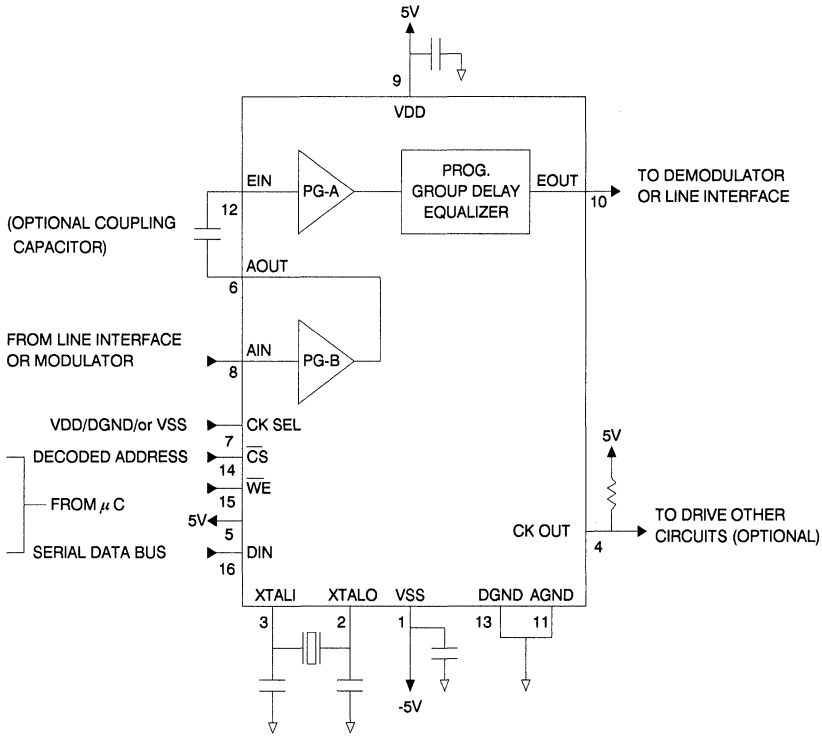
Table 4. Programmable Gain Amplifier, PG-B

Address D1	Address D0	Control Code D5	D4	D3	D2	PG-B Step No.	PG-B Gain (dB)
1	0	X	X	0	0	1	0.0
1	0	X	X	0	1	2	8.0
1	0	X	X	1	0	3	16.0
1	0	X	X	1	1	4	-8.0

X = Don't Care

9

Sample Connection for Typical Application



Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 125° C
Storage Temperature	-65° C to 150° C
Voltage on Pins AGND and DGND with Respect to VSS	-0.6 V to 6.25 V
All Voltages with Respect to VSS	-0.6V to VDD + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

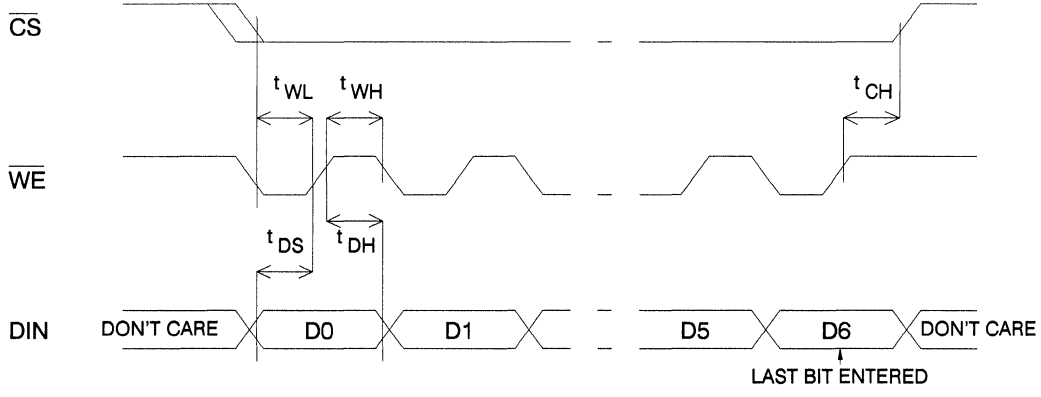
D.C. and A.C. Operating Range

	Operating Temperature (Case)	VDD / VSS Power Supplies
Commercial	0° C - 70° C	5V / -5V ± 10%
Industrial	-40° C - 85° C	5V / -5V ± 10%
Military	-55° C - 125° C	5V / -5V ± 5%

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DDO}	VDD Quiescent Current (active mode)			3	6	mA
I_{SSO}	VSS Quiescent Current (active mode)			3	6	mA
I_{DDP}	VDD Quiescent Current (power-down mode)			100	500	μA
I_{SSP}	VSS Quiescent Current (power-down mode)			100	500	μA
R_{IA}	Input Resistance at AIN		100			Kohm
R_{IE}	Input Resistance at EOUT	F_S = 153.6 KHz	1			Mohm
C_I	Input Capacitance				20	pF
ROA	Ouput Resistance at AOUT				1	Kohm
ROE	Ouput Resistance at EOUT				200	ohm
F_O	Center Frequency			1700		Hz
DT	Group Delay Tolerance		-1.5		+1.5	%
GT	Gain Tolerance		-0.05		0.05	dB
G_O	Insertion Loss		-0.15		0.15	dB
V_O	Output Voltage	RL = 20 Kohm	VSS		VDD	Volts
V_N	Output Noise	BW = F_S/2			200	μVrms
THD	Total Harmonic Distortion	RL = 20 Kohm V_O = 8Vpp		0.1	0.5	%
F_S	Sampling Frequency			153.6		KHz
V_{FT}	Clock Feedthrough				5	mVpp

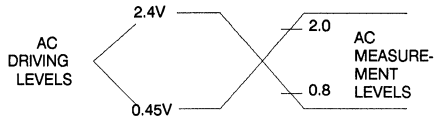
Configuration Code Write Waveform



Digital Timing Parameters

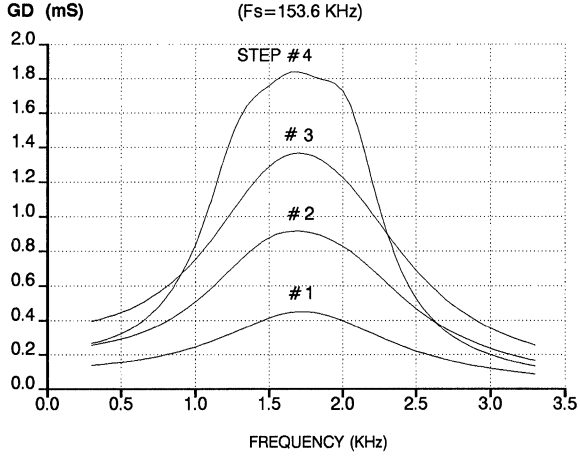
Symbol	Parameter	Min	Max	Units
t_{WL}	Write Enable Low	50		ns
t_{WH}	Write Enable High	50		ns
t_{CH}	$\overline{CS}$ Hold Time	100		ns
t_{DS}	Data Setup Time	40		ns
t_{DH}	Data Hold Time	40		ns

Input Test Waveform

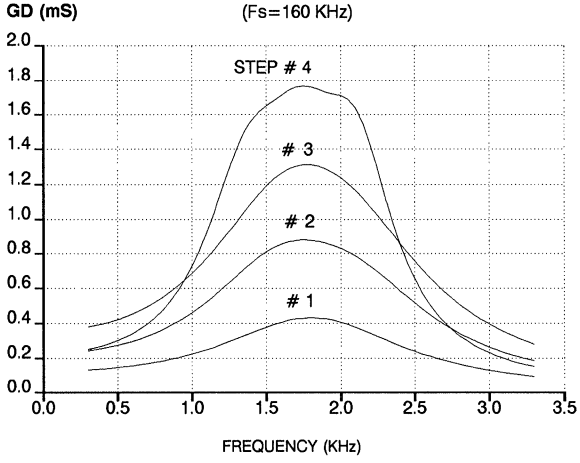


t_R, t_F < 20ns (10% to 90%)

Typical Group Delay Response



Typical Group Delay Response



Ordering Information

Delay (ms)	Gain (dB)	Power Supply	Bandwidth (KHz)	Ordering Code	Package	Operation Range
1.8	31.5	±10%	4	AT76C10-PC AT76C10-SC	16P3 16S	Commercial (0°C to 70°C)
				AT76C10-PI AT76C10-SI	16P3 16S	Industrial (-40°C to 85°C)
1.8	31.5	±5%	4	AT76C10-DM	16D3	Military (-55°C to 125°C)

Package Type	
16D3	16 Lead, 0.300" Wide Non-Windowed, Ceramic Dual Inline Package (Cerdip)
16P3	16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
16S	16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

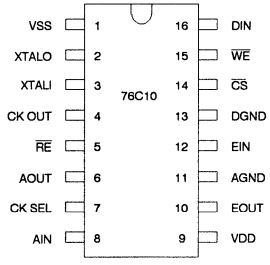
Features

- High Accuracy Programmable Gain Amplifiers
  - ± 0.02 dB Accuracy (Typical)
  - 31.5 dB Range in 0.5 dB Steps
- Software Programmable Group Delay Equalizer For Leased and Dial-Up Lines
- High Dynamic Range - over 90 dB
- On-Chip Anti-Aliasing Filters
- On-Chip E^2PROM Configuration Code Memory
- Microcomputer Interface with Serial Data Port
- Three Convenient Clock Options
  - 11.0592 MHz
  - 3.6864 MHz
  - 2.4576 MHz (or 2.56 MHz)
- Operates from +/- 5 V Supplies
- Low Power Standby Mode - 100 μA (Typical)
- TTL and CMOS Compatible Digital Interface
- Economical 16-Lead Package
- Full Military, Commercial and Industrial Temperature Ranges

Description

The AT76C10E integrates two Programmable Gain Amplifiers and a Programmable Telephone Line Group Delay Equalizer on a monolithic substrate. It is fabricated in a state-of-the-art, low power CMOS process. The Gain and Group Delay steps are controlled by a 7-bit configuration code which can be programmed in real time and can also be stored permanently in on-chip E^2PROMS. The AT76C10E is implemented in an advanced switched-capacitor technology and is designed to provide precise Gain and Group Delay compensation for low bit-error-rate data transmission over dial-up and leased lines. Anti-alias and clock filters are included on-chip as the AT76C10E employs sampled-data techniques, and external filters are not required for most applications.

Pin Configuration



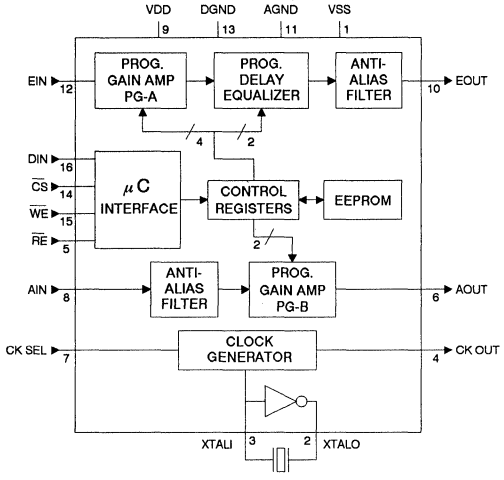
Pin Definitions

No.	Pin Name	Function
1	VSS	Negative Power Supply. Nominal -5 Volts.
2	XTALO	Crystal Oscillator Output.
3	XTALI	Crystal Oscillator Input.
4	CK OUT	Sampling Clock Output. (Open Drain)
5	$\overline{RE}$	Recall Enable Input. Loads Configuration into Control Registers from On-Chip E^2PROM.
6	AOUT	PG-B Analog Signal Output.
7	CK SEL	Clock Select. Selects one of the 3 recommended Clock frequencies.
8	AIN	PG-B Analog Signal Input.
9	VDD	Positive Power Supply. Nominal +5 Volts.
10	EOUT	Delay Equalizer Analog Signal Output.
11	AGND	Analog Ground.
12	EIN	Delay Equalizer Analog Signal Input.
13	DGND	Digital Ground.
14	$\overline{CS}$	Chip Select Control Input.
15	$\overline{WE}$	Write Enable Control Input.
16	DIN	Serial Data Input.

CMOS E^2PROM Programmable Amplifier Delay Equalizer

9

Block Diagram



Device Operation

The AT76C10E is designed for use in the signal paths of a modem or voice/data phone to minimize the bit-error-rate over dial-up and leased lines. Gain and Group Delay response of the AT76C10E are controlled by a serial 7-bit configuration code. D1 and D0 of the configuration code are the address bits which select one of the three control registers. Bits D2 to D5 set the gain and delay equalizer steps. D6 is an option bit which determines whether the configuration code will update one of the control registers only, or also be stored in on-chip non-volatile memory (E^2PROM) of the AT76C10E. All the functions associated with the configuration code are summarized in Tables 1 to 4.

Configuration Code Format

D6	D5	D4	D3	D2	D1	D0
OPTION SELECT	CONTROL CODE				ADDRESS	

This chip can be used as part of an adaptive equalizer for medium to high speed modems (1200 bps to greater than 19.2K bps). The configuration code is loaded into the chip at a serial data input port and updated in real time. It can also be stored permanently in on-chip E^2PROMS and updated periodically. The high performance Atmel E^2PROM process together with redundancy circuits allows over 10E6 write cycles. The amplitude response of the equalizer is nominally at 0 dB with negligible ripple. The AT76C10E can also be used as a fixed compromise delay equalizer.

PROGRAMMABLE GAIN AMPLIFIER: The AT76C10E provides two high dynamic range amplifiers for maximizing signal-to-noise ratio. Amplifier PG-A offers 16 programmable gain steps from 0 dB to 7.5 dB in 0.5 dB steps. Amplifier PG-B provides -8 to 16 dB of gain in 8 dB steps. The two amplifiers can be cascaded to provide 31.5 dB range of programmable gain in 0.5 dB steps. The Programmable Amplifiers can be used as an Automatic Gain Control Circuit or as a fixed gain adjustment.

PROGRAMMABLE GROUP DELAY EQUALIZER: The Group Delay Equalizer is designed to provide programmable compromise group delay compensation to achieve low bit-error-rate data transmission. Four group delay responses are provided to accommodate the majority of conditioned as well as unconditioned lines. The first three responses are recommended for line types C2 and C1, while the fourth response can be used for 3002-type lines. Two or more AT76C10Es can be cascaded to obtain additional group delay compensation.

CONTROL REGISTERS: Four control registers are used to store the configuration codes for the gain steps of PG-A and PG-B, the delay steps of the Delay Equalizer, and the control bit for the power-down mode. All the control bits, except the power down-bit, can also be programmed into on-chip non-volatile memories of the AT76C10E.

MICROCOMPUTER INTERFACE: Control inputs $\overline{CS}$, $\overline{WE}$, $\overline{RE}$ and serial data input DIN allow the AT76C10E to be easily interfaced with most popular microcontrollers. All digital I/Os are TTL as well as CMOS compatible. For stand alone operation, $\overline{CS}$ should be tied to VDD while $\overline{WE}$, $\overline{RE}$ and DIN should be tied to ground.

WRITE OPERATION: To program a configuration code into a particular control register, the voltage at $\overline{CS}$ has to be brought low while the data bits appearing at DIN are strobed in at the rising edge of $\overline{WE}$. At the rising edge of $\overline{CS}$, the last 7 input data bits are latched into the control registers. Therefore, if the first bit of an update byte is a "start bit," it will be ignored. If a "0" was inserted at D6 of the input code, the configuration code will also be immediately written into on-chip E^2PROM of the AT76C10E. As all timing signals and programming voltages are generated internally, writing the E^2PROM is transparent to the user. However, while the E^2PROM is being programmed, which takes 1.5 mS, any further attempt to initiate programming will be ignored until the first operation is completed.

RECALL OPERATION: A RECALL operation can be initiated any time during operation by bringing both $\overline{CS}$ and $\overline{RE}$ low simultaneously. The configuration codes which have been pre-programmed in the E^2PROM of the AT76C10E are loaded into the control registers.

POWER-DOWN MODE: To minimize power consumption for battery powered applications and in certain linecard applications, the AT76C10E provides a low power standby mode of operation. In the power-down mode, the analog outputs go into a high impedance state. The power-down mode is initiated by writing a "0" into the power-down register. Once in the power-down mode, the AT76C10E can be reactivated by writing a "1" into the power-down register or performing a RECALL operation. It should be noted that upon powering up the AT76C10E for the first time, it automatically goes into the normal active mode of operation.

CRYSTAL OSCILLATOR: Internal timing of the chip is generated either by connecting a crystal across pins XTALI and XTALO of the on-chip oscillator, or by applying an external clock at pin XTALI. In the latter case, pin XTALO should be left unconnected. To accommodate different applications, three clock options: 2.4576 MHz, 3.6864 MHz and 11.0592 MHz, can be selected via control pin CK SEL. For applications in a linecard environment, a 2.56 MHz clock can be used instead of the 2.4576 MHz clock. The 153.6 KHz (160 KHz with 2.56 MHz clock) sampling clock is available as an open drain output at CK OUT for synchronization or driving other circuits, e.g. the transmit or receive filters, or A/D and D/A converters.

CK SEL	Recommended XTAL Frequency	CK OUT
VDD	11.0592 MHz	153.6 KHz
DGND	3.6864 MHz	153.6 KHz
VSS	2.4576 MHz	153.6 KHz
VSS	2.56 MHz	160.0 KHz

Group Delay Characteristics (Microseconds)

Fs = 153.6 KHz

Frequency (Hz)	Step #1	Step #2	Step #3	Step #4
300	158	278	416	284
600	188	336	502	386
900	237	463	681	680
1200	325	671	985	1360
1500	431	890	1330	1791
1700	462	938	1382	1838
1900	435	897	1305	1810
2100	372	777	1144	1510
2400	266	542	808	683
2700	181	361	534	342
3000	136	250	368	213
3300	102	182	267	148

Table 1. Option Selection

Address D1	Address D0	Option Bit D6	Function
0	0	0	Writes Control Code into E^2PROM and updates Control Registers
0	1	0	
1	0	0	
0	0	1	Updates Control Registers Only
0	1	1	
1	0	1	
1	1	0	Power Down Mode
1	1	1	Active Mode

Table 2. Equalizer Selection

Address D1	Address D0	Control Code D5	D4	D3	D2	Equalizer Step No.	Recommened Line Condition
0	0	X	X	0	0	1	C2
0	0	X	X	0	1	2	C1
0	0	X	X	1	0	3	C1
0	0	X	X	1	1	4	3002

Table 3. Programmable Gain Amplifier, PG-A

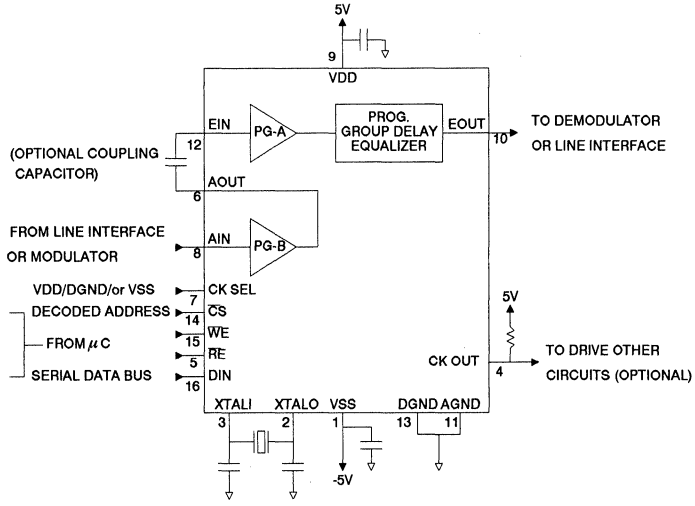
Address D1	Address D0	Control Code D5	D4	D3	D2	PG-A Step No.	PG-A Gain (dB)
0	1	0	0	0	0	1	0.0
0	1	0	0	0	1	2	0.5
0	1	0	0	1	0	3	1.0
0	1	0	0	1	1	4	1.5
0	1	0	1	0	0	5	2.0
0	1	0	1	0	1	6	2.5
0	1	0	1	1	0	7	3.0
0	1	0	1	1	1	8	3.5
0	1	1	0	0	0	9	4.0
0	1	1	0	0	1	10	4.5
0	1	1	0	1	0	11	5.0
0	1	1	0	1	1	12	5.5
0	1	1	1	0	0	13	6.0
0	1	1	1	0	1	14	6.5
0	1	1	1	1	0	15	7.0
0	1	1	1	1	1	16	7.5

Table 4. Programmable Gain Amplifier, PG-B

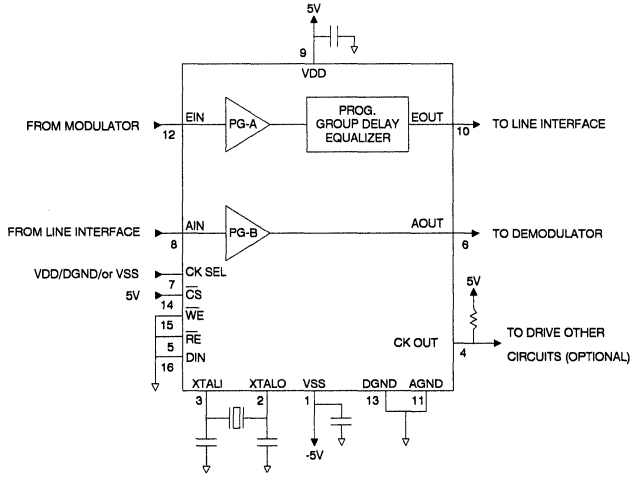
Address D1	Address D0	Control Code D5	D4	D3	D2	PG-B Step No.	PG-B Gain (dB)
1	0	X	X	0	0	1	0.0
1	0	X	X	0	1	2	8.0
1	0	X	X	1	0	3	16.0
1	0	X	X	1	1	4	-8.0

X = Don't Care

Sample Connection for Typical Application



Stand Alone Operation Example



Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 125° C
Storage Temperature	-65° C to 150° C
Voltage on Pins AGND and DGND with Respect to VSS	-0.6 V to 6.25 V
All Voltages with Respect to VSS	-0.6V to VDD + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

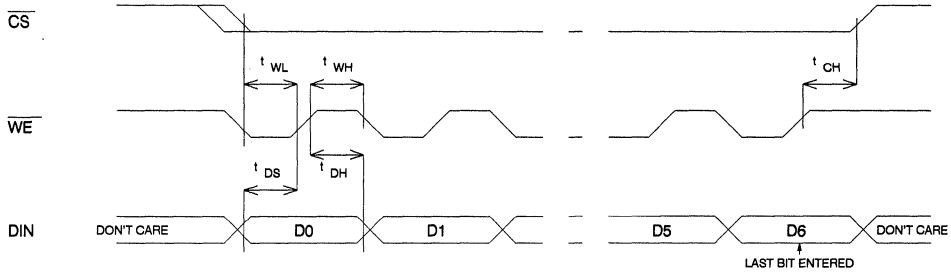
	Operating Temperature (Case)	VDD / VSS Power Supplies
Commercial	0° C - 70° C	5V / -5V ± 10%
Industrial	-40° C - 85° C	5V / -5V ± 10%
Military	-55° C - 125° C	5V / -5V ± 5%

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DDO}	VDD Quiescent Current (active mode)			3	6	mA
I_{SSO}	VSS Quiescent Current (active mode)			3	6	mA
I_{DDP}	VDD Quiescent Current (power-down mode)			100	500	μA
I_{SSP}	VSS Quiescent Current (power-down mode)			100	500	μA
R_{IA}	Input Resistance at AIN		100			Kohm
R_{IE}	Input Resistance at EOUT	F_S = 153.6 KHz	1			Mohm
C_I	Input Capacitance				20	pF
ROA	Ouput Resistance at AOUT				1	Kohm
ROE	Ouput Resistance at EOUT				200	ohm
F_O	Center Frequency			1700		Hz
DT	Group Delay Tolerance		-1.5		+1.5	%
GT	Gain Tolerance		-0.05		0.05	dB
G_O	Insertion Loss		-0.15		0.15	dB
V_O	Output Voltage	RL = 20 Kohm	VSS		VDD	Volts
V_N	Output Noise	BW = F_S/2			200	μVrms
THD	Total Harmonic Distortion	RL = 20 Kohm V_O = 8Vpp		0.1	0.5	%
F_S	Sampling Frequency			153.6		KHz
V_{FT}	Clock Feedthrough				5	mVpp

9

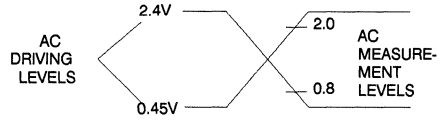
Configuration Code Write Waveform



Digital Timing Parameters

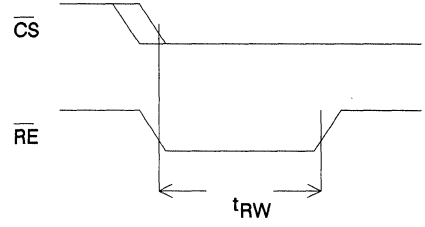
Symbol	Parameter	Min	Max	Units
t_{WL}	Write Enable Low	50		ns
t_{WH}	Write Enable High	50		ns
t_{CH}	$\overline{CS}$ Hold Time	100		ns
t_{DS}	Data Setup Time	40		ns
t_{DH}	Data Hold Time	40		ns

Input Test Waveform

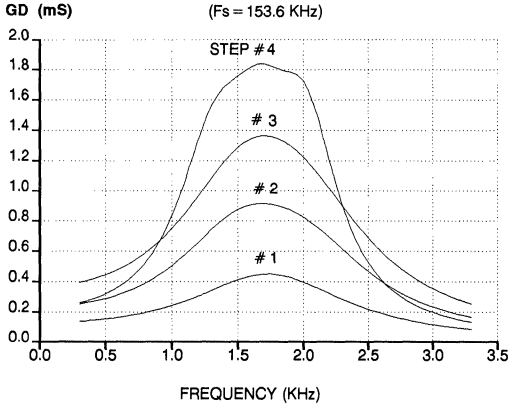


t_R, t_F < 20ns (10% to 90%)

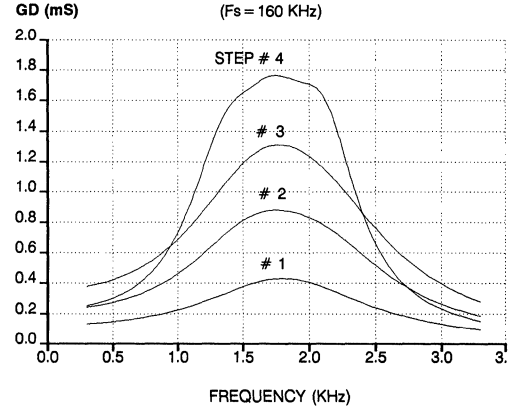
Configuration Code Recall Waveform



Typical Group Delay Response



Typical Group Delay Response



Ordering Information

Delay (ms)	Gain (dB)	Power Supply	Bandwidth (KHz)	Ordering Code	Package	Operation Range
1.8	31.5	±10%	4	AT76C10E-PC AT76C10E-SC	16P3 16S	Commercial (0°C to 70°C)
				AT76C10E-PI AT76C10E-SI	16P3 16S	Industrial (-40°C to 85°C)
1.8	31.5	±5%	4	AT76C10E-DM	16D3	Military (-55°C to 125°C)

9

Package Type	
16D3	16 Lead, 0.300" Wide Non-Windowed, Ceramic Dual Inline Package (Cerdip)
16P3	16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
16S	16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Features

- **Monolithic Dual-Channel 16/18-Bit A/D Converters**
  - **On-Chip Sample/Hold**
  - **Automatic Linearity Error Correction**
- **High Conversion Rates to 96K Samples Per Second at 18 Bits for Each Channel**
- **Operates from a Single 5V +/- 10% Supply**
- **High Signal-to-Noise Ratio: 90 dB**
- **Single Multiplexed Serial Data Output**
- **High Reliability CMOS Technology**
- **Full Military, Commercial and Industrial Temperature Ranges**

CMOS Dual-Channel 16/18-Bit A/D Converters

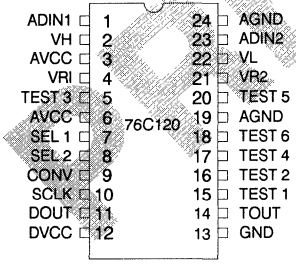
Preliminary

Description

The AT76C120 provides two complete Analog-to-Digital (A/D) Converters integrated on a monolithic substrate. It is designed for Digital Audio and Signal Processing applications as well as Industrial Control and Datacommunication. The Sample/Hold function is incorporated in both A/D channels. Each channel can independently perform 96K 18-Bit conversions per second. The AT76C120 needs a minimum of external components and provides a simple and cost effective solution for applications requiring high resolution A/D conversion.

The AT76C120 is fabricated in a state-of-the-art, low power CMOS process and operates from a single 5V supply. A modified successive approximation algorithm is used to optimize conversion speed. Linearity errors caused by tap weight variations are automatically compensated by adding a correction factor to each A/D conversion result. The optimum correction factors are factory programmed into each individual chip. The digital output code is presented serially, in 2's complement format.

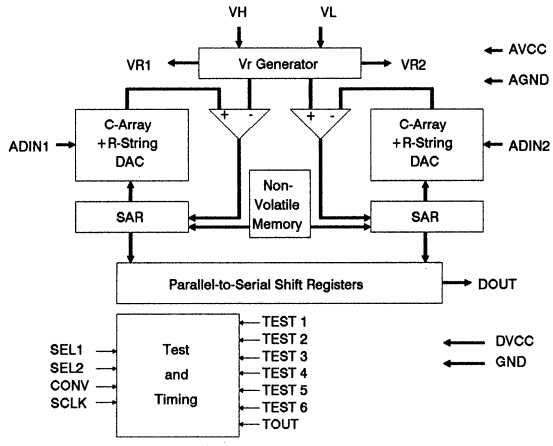
Pin Configuration



Pin Name	Function
AGND, GND	Analog Ground, Ground
ADIN1	Analog Input for Channel-1
ADIN2	Analog Input for Channel-2
AVCC	+5V Analog Supply Input
DOUT	Digital Data Output
DVCC	+5V Digital Supply Input
CONV	Convert Clock Input
SCLK	System Clock Input
SEL1	DOUT Mode Select Input
SEL2	16/18-Bit Mode Select Input
TEST 1,2,3,4,5,6	Test Inputs
TOUT	Test I/O
V_H,V_L	Reference Voltage Inputs
VR1,VR2	Channel-1,-2 Reference Voltage Outputs

9

Block Diagram



Device Operation

Each analog input to the AT76C120 is sampled and held simultaneously once every CONV clock period. As shown in the Block Diagram, the AT76C120 uses a combination of binary ratioed double-polysilicon Capacitor Arrays and Resistor String networks to generate the analog decision levels (or tap weights). The Capacitor Arrays also provide the internal Sample-and-Hold function. A high-gain auto-zeroed Comparator is used to compare an analog input with the decision levels. The Vr Generator supplies internal reference voltages equal to (VH - VL)/2 used by the comparators.

A/D conversion is accomplished through 18-bit Successive Approximation Registers (SAR's). An improved successive approximation scheme is used to optimize conversion speed. The A/D output codes are stored in Parallel-to-Serial Shift Registers and are available at a single multiplexed serial data output port.

System Clock input, SCLK, provides the internal timing reference and the Convert Clock, CONV, input initiates an A/D conversion. The Test and Timing circuits shown in the Block Diagram generate all the timing control signals from SCLK and CONV for sample-and-hold, A/D conversion and tap weight error correction during normal operation as well as tap weight error calibration at the factory.

A minimum of 64 SCLK clock cycles are required for one A/D conversion. The maximum SCLK clock frequency is 6.144 MHz. The minimum 18-bit conversion time for each channel is 10.4 μs, which corresponds to a maximum conversion rate of 96 KHz making 2X sampling in Digital Audio applications possible.

To minimize overall system cost while achieving high resolution, the AT76C120 compensates for linearity errors caused by tap weight variations by adding a correction factor to each A/D conversion result. This operation is done automatically without the intervention of the host processsor. The optimum correction factors are factory programmed into on-chip nonvolatile storage.

The AT76C120 requires only a single 5V supply for operation.

System Implementation Considerations

POWER SUPPLY DECOUPLING AND GROUNDING: To obtain the highest performance possible with the AT76C120, critical signal paths, power supply lines and ground planes on the circuit board should be laid out carefully to minimize noise coupling or aliasing into sensitive analog paths. As illustrated in the diagram showing a Sample Connection for Typical Application, a separate AVCC line decoupled to AGND with an electrolytic capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C120. Similarly, a separate analog ground return, AGND, which is connected to the most quiet point in the system ground plane, should be used.

For best results, four layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath pins 1 to 6 and pins 19 to 24.

High frequency noise on the power and ground lines can be aliased into the passband by the sampling action of the AT76C120. If a switching power supply has to be used, both AVCC and AGND need to be isolated from the system supplies with inductors of appropriate values.

ANALOG INTERFACE: Due to the high sampling rate of the AT76C120, little if any anti-alias filtering is required for most industrial applications. For high performance Digital Audio applications, external Anti-Alias Lowpass or Bandpass Filters, shown as AAFs' in the Sample Connection diagram, should be used to eliminate signals outside the desired passband. Low noise op amps with low output impedances should also be used to supply the analog inputs.

The A/D full-scale range is determined by the voltage applied across pins VH and VL, i.e. (VH - VL). VL is normally connected to the analog ground, AGND, while VH should be supplied by a stable voltage reference.

The internal reference voltage appearing at output pins VR1 and VR2 is nominally (VH - VL)/2. For low noise applications, VR1 and VR2 should be decoupled to AGND with high quality capacitors.

If the voltage of the input signal can swing below ground, it is necessary to apply an offset to the input to make the AC ground correspond to the mid point of the full scale range, (VH - VL)/2. Outputs VR1 and VR2 provide the AC ground reference as shown in the diagram for Sample Connection.

SYSTEM TIMING: Internal and output data timing of the AT76C120 are synchronized with the system clock, SCLK. To avoid possible synchronization and aliasing problems, deriving the convert clock, CONV, by dividing SCLK by 64 is recommended.

The AT76C120 samples both analog inputs, ADIN1 and ADIN2, once every CONV period. Both inputs are sampled simultaneously, i.e. in-phase. The AT76C120 then performs an A/D conversin on both samples and returns the two resulting 18-bit codes at the serial data output pin, DOUT, during the following CONV clock period.

The convert clock, CONV, is used inside the AT76C120 to initiate sample-and-hold and can also be used by the host processor to latch in the serial 16-bit or 18-bit wide output data.

DIGITAL INTERFACE: The AT76C120 uses a single multiplexed serial data output pin, DOUT. CH-1 and CH-2 data bits are synchronized with SCLK and are available during either the "High" or the "Low" period of convert clock, CONV. A logic "1" at DOUT Mode Select, SEL1, results in the AT76C120 returning the A/D output of CH-1 during the CONV "Low" period, and CH-2 output during the CONV "High" period. A logic "0" at SEL1 results in CH-1 output during the CONV "High" period and CH-2 output during the CONV "Low" period.

The convert clock, CONV, if equal to SCLK divided by 64, makes a transition from "High" to "Low" or vice versa after the LSB is shifted out of DOUT. This allows the serial data to be easily latched into most popular D/A converters or digital signal processors by using CONV rising or falling edges. To further enhance digital interface compatibility, DOUT Mode Select Input, SEL1, allows the user to choose either CONV transitions for both channels.

The AT76C120 allows the user to choose either 16-bit wide or 18- bit wide A/D outputs in 2's complement format. A logic "1" at 16/18 Mode Select Input, SEL2, returns two 18-bit codes at DOUT, while a logic "0" results in 16-bit output codes at CONV rising or falling edges as shown in Input/Output Timing diagram.

In Digital Audio and many signal processing applications, the A/D outputs are further processed by a digital filter. The 18-bit output mode provides better dynamic range and resolution than 16- bit outputs. However, for applications with a 8-bit or 16-bit host microprocessor, 16-bit wide data are more convenient to manage.

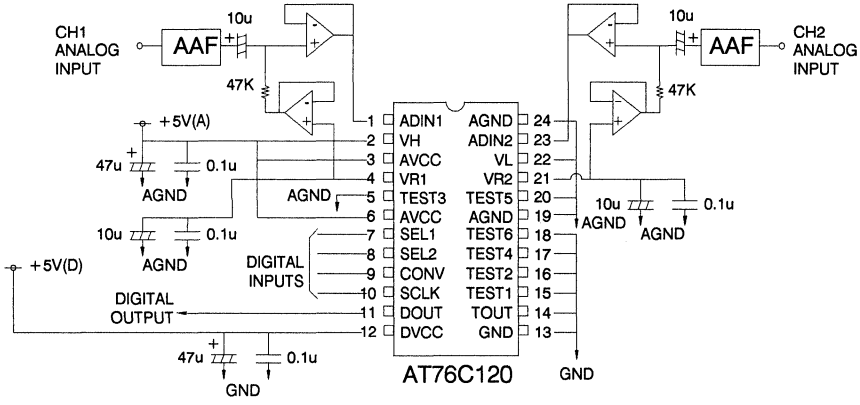
Pin Definitions

	Symbol	Functional Descriptions
Analog Interface	ADIN1 ADIN2	Analog Inputs for Channel-1 (CH-1) and Channel-2 (CH-2). The Sample/Hold function is provided on-chip for both channels. The analog inputs at ADIN1 and ADIN2 are sampled in-phase. Each A/D conversion takes at least 64 SCLK periods.
	V_L V_H	Reference Voltage Inputs. V_L and V_H are normally tied to Analog Ground and the desired full-scale voltage respectively. The full scale range is given by (V_H-V_L). The maximum full-scale voltage can be as high as AVCC.
	VR1 VR2	Reference Voltage Outputs for CH-1 and CH-2. The nominal value at these pins is (V_H-V_L)/2. For low noise applications, VR1 and VR2 should be bypassed to AGND with capacitors.
Digital Interface	CONV	Convert Clock Input. CONV is normally obtained by dividing the system clock SCLK by 64. The internal Sample/Hold pulse and A/D data output are synchronized with CONV.
	DOUT	Serial Digital Output. DOUT returns two 18-bit serial outputs for CH-1 and CH-2 in 2's complement format. The output data bits are synchronized with SCLK. Please refer to DOUT Timing Diagram for detailed timing relationship with CONV and SCLK.
	SCLK	System Clock Input. The maximum frequency for 18-bit operation is 6.144 MHz. This corresponds to a minimum conversion time of 10.4 μs.
	SEL1	DOUT Mode Select Input. i) SEL1 = "1", CH-1 data output during CONV "Low" CH-2 data output during CONV "High" ii) SEL1 = "0", CH-1 data output during CONV "High" CH-2 data output during CONV "Low"
	SEL2	16/18-Bit Mode Select. i) SEL2 = "1" selects 18-bit A/D mode, ii) SEL2 = "0" selects 16-bit A/D mode.

Pin Definitions (cont'd)

	Symbol	Functional Descriptions
Test Interface	TEST1 TEST2 TEST3 TEST4 TEST5 TEST6	Test Inputs. Normally tied to Ground for TEST 1, 2, 4, 6 and to AGND for TEST 3, 5. These inputs are used for testing and calibration at the factory and are not required for normal A/D operations.
	T_{OUT}	Test I/O. Normally tied to Ground. Like the Test Input pins, this pin is not used for normal A/D operations.
Power Supply	AVCC	Analog Power Input. Nominal 5 Volts. AVCC should be connected to a filtered system supply and kept separate from the Digital Supply.
	DVCC	Digital Power Input. Nominal 5 Volts.
	AGND	Analog Ground. AGND should be kept separate from the digital Ground.
	GND	Digital Ground.

Sample Connection for Typical Application



Notes: AVCC, AGND, +5V (A)— analog supply
DVCC, GND, +5V (D)— digital supply

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to AGND and GND	-2.0V to 7.0V(1)
Power Dissipation	1W
Reference Current	10mA
Analog Input Current	10mA
DC Digital Output Current	25mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is AVCC/DVCC+0.75V DC which may overshoot to 7.0V for pulses of less than 20ns.

D.C. and A.C. Operating Range

		AT76C120-1	AT76C120-2	AVCC/DVCC Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C	0° C - 70° C	5V +/- 10%
	Ind.	-40° C - 85° C	-40° C - 85° C	5V +/- 10%
	Mil.	-55° C -125° C	-55° C -125° C	5V +/- 5%

D.C. Characteristics

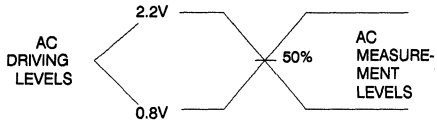
Symbol	Parameter	Conditions	Min	Max	Units
I_{LI}	Digital Input Load Current	V_{IN} = -0.1V to DVCC + 0.1V		10	μA
I_{LO}	Digital Output Leakage Current	V_{OUT} = -0.1V to DVCC + 0.1V		10	μA
I_{CCD}	Digital Supply Current			40	mA
I_{CCA}	Analog Supply Current			10	mA
I_{REF}	Reference Input Current			5	mA
V_{IL}	Digital Input Low Voltage		-0.5	0.8	V
V_{IH}	Digital Input High Voltage		2.2	DVCC + 0.5	V
V_{OL}	Digital Output Low Voltage	IO = 5mA		0.4	V
V_{OH}	Digital Output High Voltage	IO = -5mA	2.4		V
V_{AIN}	Analog Input Voltage		V_L	V_H	V
V_H	Analog Input Voltage at V_H Pin		AVCC-0.5	AVCC	V
V_L	Analog Input Voltage at V_L Pin		0.0	0.5	V

9

Analog Characteristics (AVCC = DVCC = 5V, Ta = 25° C)

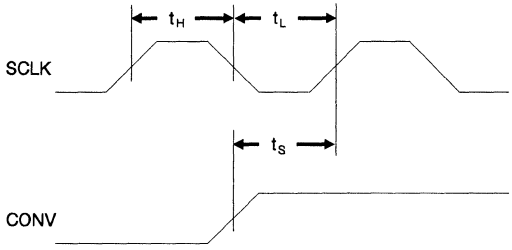
			AT76C120-1			AT76C120-2			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Units
RES	A/D Resolution		18			18			Bits
DLE	Differential Linearity Error	@ 18 Bits			± 1			± 1	LSB
ILE	Integral Linearity Error	@ 15 Bits			± 1				LSB
		@ 13 Bits						± 1	LSB
Fs	A/D Sampling Frequency	18-Bit Mode			96			96	KHz
FSE	Full Scale Error			± 1.5			± 1.5		% FSR
THD + N	Total Harmonic Distortion Plus Noise	0dB, 1KHz Input		0.01			0.03		%
		-20dB, 1KHz Input		0.02			0.06		%
		-60dB, 1KHz Input		2			5		%
S/N	Signal-to-Noise Ratio			90			84		dB

Input Test Waveforms

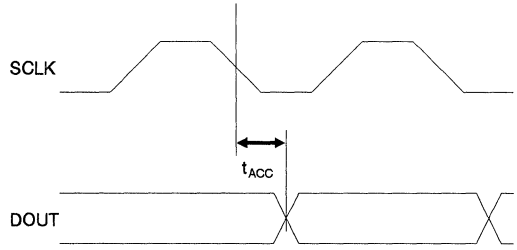


Notes: 1. tR, tF < 30 ns (10% to 90%)
2. Input timing reference is at 1.5V

Digital Input Waveforms



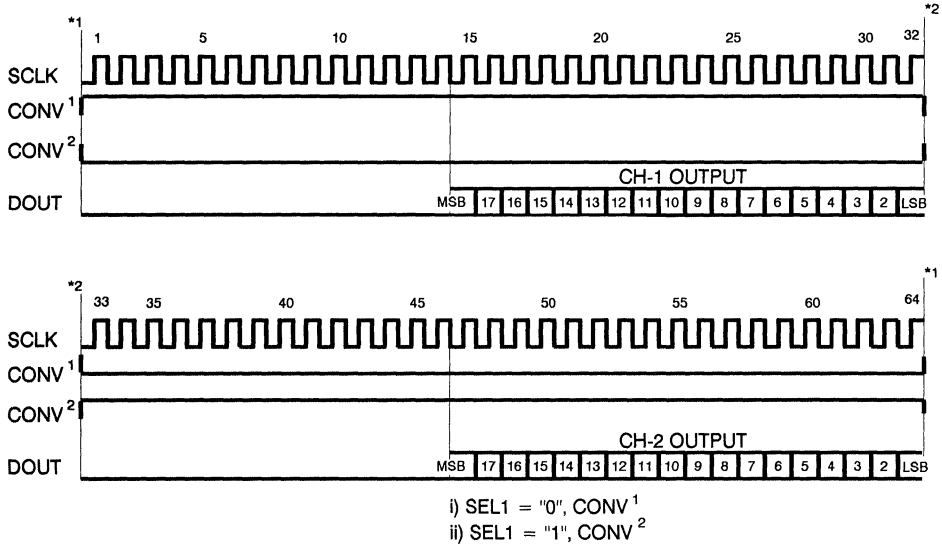
Digital Output Timing Waveforms



Digital Timing Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
t_R	Input Rise Time			30	ns
t_F	Input Fall Time			30	ns
t_H	SCLK High Width		50		ns
t_L	SCLK Low Width		50		ns
t_S	CONV Setup Time		40		ns
t_{ACC}	DOUT Access Time	C_{LOAD} = 30pF		50	ns
T_{CONV}	CONV Period		10.4		μs
T_{SCLK}	SCLK Period		162		ns

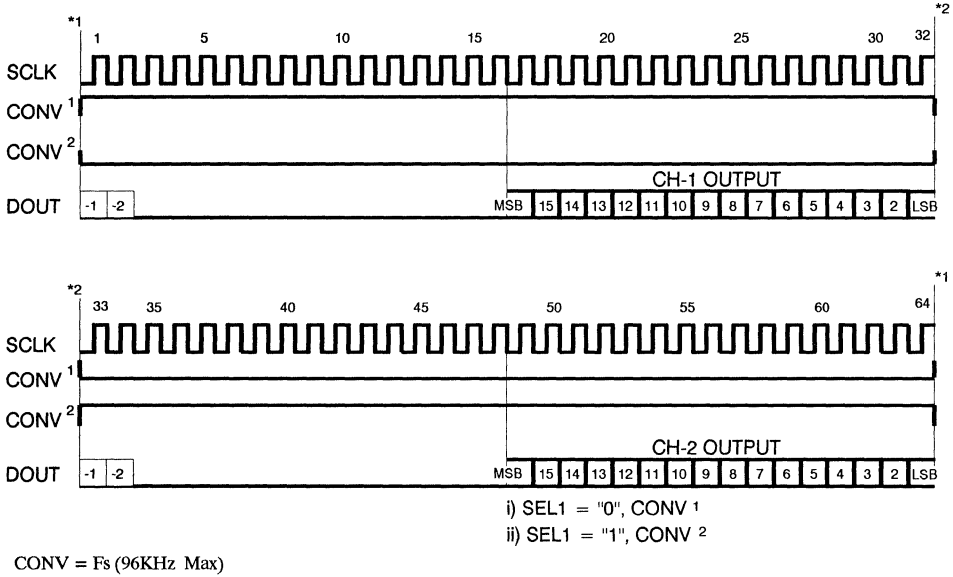
Input/Output Timing for 18-Bit Mode (SEL2 = "1")



i) SEL1 = "0", CONV 1
ii) SEL1 = "1", CONV 2

Notes: CONV = Fs (96KHz Max)
SCLK = CONV x 64

Input/Output Timing for 16-Bit Mode (SEL2 = "0")



i) SEL1 = "0", CONV 1
ii) SEL1 = "1", CONV 2

Notes: CONV = Fs (96KHz Max)
SCLK = CONV x 64

9

Ordering Information

Speed (KHz)	Signal-to-Noise (dB)	Power Supply	Ordering Code	Package	Operation Range
96	90	±10%	AT76C120-1PC	24P6	Commercial (0°C to 70°C)
			AT76C120-1PI	24P6	Industrial (-40°C to 85°C)
96	90	±5%	AT76C120-1DM	24D6	Military (-55°C to 125°C)
96	84	±10%	AT76C120-2PC	24P6	Commercial (0°C to 70°C)
			AT76C120-2PI	24P6	Industrial (-40°C to 85°C)
96	84	±5%	AT76C120-2DM	24D6	Military (-55°C to 125°C)

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

- **Personal System/2* and VGA* Compatible**
- **Pixel Rates to 50 MHz**
- **Triple 6-Bit DACs Display 256K Possible Colors**
- **Pixel Word Mask and Composite Blank on All Three Channels**
- **18-Bit Wide Color Palette Stores 256 Colors**
- **RGB Video Outputs Drive 37.5 Ohm Loads Directly**
- **Low Power, Low Glitch Operation**
- **Single +5 V Supply**
- **Available in Standard 28 Pin DIP and 32 Pin Plastic LCC**
- **Full Military, Commercial and Industrial Temperature Ranges**

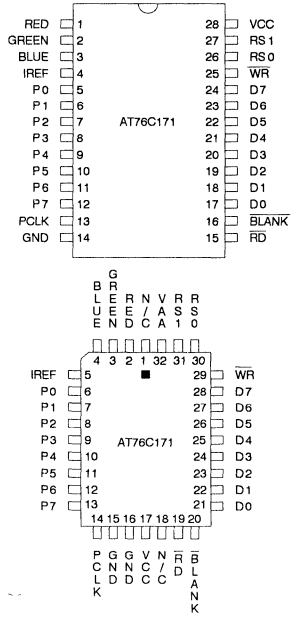
CMOS Triple Video DAC Color Palette

Description

The AT76C171 is a second generation color palette DAC (Digital-to-Analog Converter) which provides direct drives for RGB color displays. The AT76C171 integrates three high performance 6-bit video DACs, an advanced 256 x 18 Color Palette (Color Look-up Table) and a versatile microprocessor interface on a monolithic substrate.

The AT76C171 supports the RS170 video standard and graphics controllers compatible with the VGA standard. This device allows 256 colors to be displayed out of a total of 262,144 colors. The AT76C171 provides composite blank outputs on all three channels. Additional advanced features include on-chip pixel mask logic which allows displayed colors to be modified in a single write cycle rather than by altering the contents of the color palette.

Pin Configurations

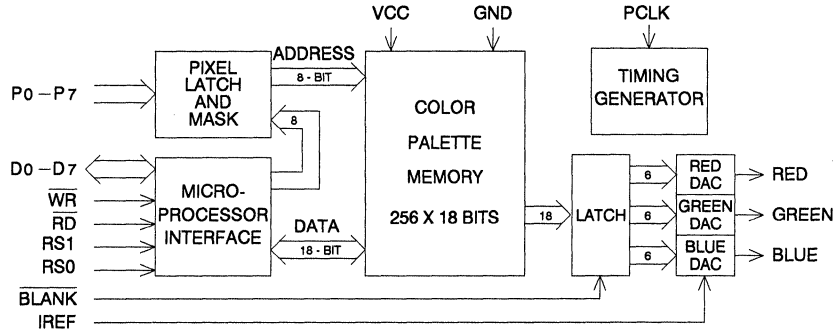


Pin Name	Function
RED GREEN BLUE	Analog Video Outputs for R,G,B Guns
IREF	Reference Current Input
P0-P7	Pixel Address Inputs
PCLK	Pixel Clock Input
GND	Ground
$\overline{RD}$	Read Enable Input
$\overline{BLANK}$	Video Blanking Input
D0-D7	Program Data I/O
$\overline{WR}$	Write Enable Input
RS0,RS1	Register Select Inputs
VCC	+5 Volts Supply Input
VAA	+5 Volts Analog Supply Input
N/C	No Connect

* Personal System/2 and VGA are registered trademarks of IBM Corporation.

9

Block Diagram



Pin Definitions

	Symbol	Functional Descriptions
Video Interface	RED GREEN BLUE	Analog Video Outputs. These are the outputs of the triple video DACs. The 18-bit wide color palette output and the $\overline{\text{BLANK}}$ input drive the DAC inputs.
	IREF	Reference Current Input. The Reference Current sets the full scale current sourced by each DAC.
	P0-P7	Pixel Address Inputs. The 8-bit Pixel Address is logically AND'ed with the Pixel Mask value before it is used to select a stored 18-bit color value from the palette.
	PCLK	Pixel (or Dot) Clock Input. The rising edge of PCLK samples the Pixel Address and $\overline{\text{BLANK}}$ inputs. PCLK is the system clock for the palette DAC pipeline.
	$\overline{\text{BLANK}}$	Blanking Input. A logic "0" at $\overline{\text{BLANK}}$ input overrides the current color value and forces the Analog Video Outputs to the zero (or Blank) level. The Color Palette can be updated while Blanking is active.
Power Supply	GND	Ground. GND should be connected to a solid ground plane in the system.
	VCC	Digital Supply. Nominal 5 Volts. VCC should be bypassed to GND with a high-frequency capacitor.
	VAA	Analog Supply. Nominal 5 Volts. VAA should be connected to a filtered system supply.
Microprocessor Interface	$\overline{\text{RD}}$	Read Enable Input. $\overline{\text{RD}}$ controls the timing of microprocesssor Read operations.
	$\overline{\text{WR}}$	Write Enable Input. $\overline{\text{WR}}$ controls the timing of microprocessor Write operations. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should not be active (low) at the same time.
	D0-D7	Program Data I/O Ports (Bidirectional). The rising edge of $\overline{\text{WR}}$ latches Program Data at D7-D0 into the selected internal register. The falling edge of $\overline{\text{RD}}$ enables D7-D0 as outputs and the rising edge of $\overline{\text{RD}}$ returns D7-D0 to a high impedance state.
	RS0, RS1	Register Select Inputs. Control the selection of internal registers. (See description on Internal Registers.) The falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ latches in the value at RS1, RSO.

Internal Registers

RS1	RS0	Bits	Register Name	Functional Description
0	0	8	Pixel Address (Write Mode)	The Pixel Address Register is accessed via Register Address (0,0) or (1,1). Reading the Pixel Address value from (0,0) is the same as reading from (1,1). A pixel address value is normally written to Pixel Address Register at (0,0) before one or more color values are written to the Color Palette. A pixel address value is normally written to Pixel Address Register at (1,1) before one or more color values are read from the Color Palette.
1	1	8	Pixel Address (Read Mode)	
0	1	18	Color Value	The Color Value Register acts as a buffer between the 18-bit wide Color Palette and the 8-bit microprocessor interface. Each READ and WRITE at (0,1) consists of three byte transfers in the order of RED first, Green second and BLUE last. Only the LSBs D5-D0 of each byte are used, the two MSBs are set to "0" when a color value is read. The Pixel Address Register automatically increments after each 18-bit color value Read or Write operation. Each color value READ or WRITE operation overrides the pixel stream for one PCLK period.
1	0	8	Pixel Mask	The Pixel Mask value is bitwise AND'ed with the Pixel Address value at P7-P0. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Address supplied via the microprocessor interface is not affected by the Pixel Mask.

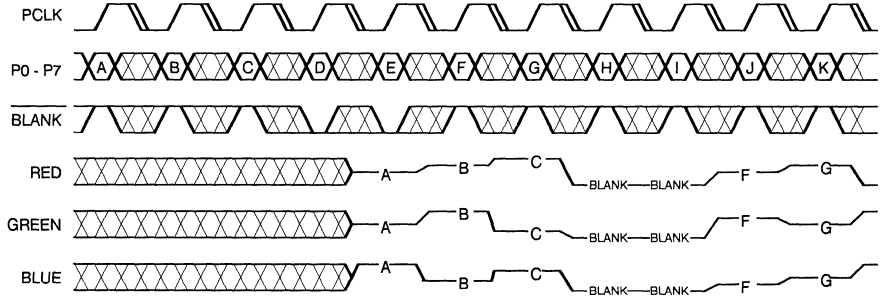
Device Operation

COLOR PALETTE: The AT76C171 provides an 18-bit wide by 256 word deep color palette static RAM array for storing the desired color intensity values. Each word is divided into three fields for the RED, GREEN and BLUE video DACs respectively. The 8-bit wide Pixel Address is decoded and used to select a particular location in the RAM array. The color value retrieved from that location is then used as inputs to the three video DACs which convert the digital color code into analog color intensity values.

The AT76C171 achieves low power, high speed operation by using an advanced pipelined palette DAC architecture. Delay from Pixel Address to color intensity value out is 3 PCLK periods.

9

Video Pipeline Timing Diagram



MPU INTERFACE: The AT76C171 provides a standard microprocessor interface which allows the host display controller to access the Color Palette RAM and all internal registers of the AT76C171. MPU READ and WRITE operations are internally synchronized with the video pipeline and therefore can take place asynchronously from the normal pixel mapping operation. An on-chip address counter allows the MPU to READ or WRITE the Color Palette in a Block Mode.

COLOR PALETTE READ AND WRITE: Four MPU operations are required to write (i.e. store a Color Value) to a specific location in the Color Palette RAM. The desired RAM address is first written into the internal Pixel Address register by executing a WRITE operation at register address (0,0). A new Color Value is next written into the internal Color Value register at register address (0,1) by three consecutive WRITE operations, with the RED color first, GREEN second and BLUE last. Only LSBs D5-D0 of each byte transferred are used. The new Color Value is then automatically written into the designated address in the Color Palette RAM.

Similarly, four MPU operations are required to read a Color Value from a specific location in the Color Palette RAM. The RAM address is written into the internal Pixel Address register by executing a WRITE operation at register address (1,1). The Color Value stored in that particular RAM location is automatically transferred to the internal Color Value Register. Three consecutive READ operations are then required to read the retrieved Color Value in three bytes, with the RED color first, GREEN second and BLUE last. Only the last 6 LSBs D5-D0 contain valid data, the two MSBs are set to "0".

BLOCK READ AND WRITE MODE: The on-chip Pixel Address Register automatically increments by one after each complete Color Value READ or WRITE operation. This useful feature allows an entire block of the Color Palette RAM to be accessed by simply writing the starting address into the Pixel Address register at the appropriate register address. Subsequent READ or WRITE operations require only 3-byte transfers at D7-D0.

TRIPLE VIDEO DAC: Each of the three video DACs on the AT76C171 consists of an array of current sources tied to a common output. The current sources use an advanced current steering scheme to minimize glitch energy. The number of current sources in each DAC steered to the output during any PCLK period equals the value represented by the Color Value selected from the Color Palette. The rest of the current sources are steered to ground.

The input Reference Current (IREF) determines the current in each current source. Each DAC is designed to produce a 0.7 Volt peak white level when driving a doubly terminated 75 ohm load with IREF = -8.88 mA. The relationship between the peak white level and IREF is given by the equation:

$$V_{Peak\ White} = 2.1 \times IREF \times R_{Load}$$

BLANKING: The AT76C171 supports composite blanking at all three RED, GREEN and BLUE video outputs. The $\overline{BLANK}$ input is latched on the rising edge of PCLK and affects the analog video outputs after 3 PCLK periods. An internal pipelined delay circuit is used to synchronize the $\overline{BLANK}$ input with the normal pixel pipeline. A logic "0" at $\overline{BLANK}$ input overrides the current color value and forces the analog video outputs to the zero (or Blank) level. The $\overline{BLANK}$ circuit has no effect on the MPU interface and the Color Palette remains accessible via READ and WRITE.

PIXEL MASK: The AT76C171 features an advanced on-chip Pixel Mask which is very useful for cursor control, flashing objects, and animation. The Pixel Mask value stored in internal register (1,0) is bitwise AND'ed with the input Pixel Address value at P7-P0 to form the actual RAM address for the Color Palette. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Addresses supplied via the MPU interface are not affected by the Pixel Mask. Note that when loading the Pixel Mask, $\overline{WR}$ must be synchronized with PCLK as shown in "AC Waveforms for Pixel Mask Synchronization."

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-2.0V to 7.0V(1)
Power Dissipation	1W
Reference Current	-15mA
Analog Output Current	45mA
DC Digital Output Current	25mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is VCC+0.75V DC which may overshoot to 7.0V for pulses of less than 20ns.

D.C. and A.C. Operating Range

		AT76C171-50	AT76C171-35	VCC/VAA Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C	0° C - 70° C	5V +/- 10%
	Ind.	-40° C - 85° C	-40° C - 85° C	5V +/- 10%
	Mil.		-55° C -125° C	5V +/- 5%

D.C. Characteristics

Symbol	Parameter	Conditions	All Min	35MHz Max	50MHz Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 0.1V		10	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V		10	10	μuA
I_{CC}	Power Supply Current	IO = 21mA Digital Outputs Open		140	150	mA
I_{REF}	Reference Current		-7	-10	-10	mA
V_{IL}	Input Low Voltage		-0.5	0.8	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	IO = 5mA		0.4	0.4	V
V_{OH}	Output High Voltage	IO = -5mA	2.4			V
V_{REF}	Voltage at IREF Input		V_{CC}-3	V_{CC}	V_{CC}	V

Video DAC Characteristics

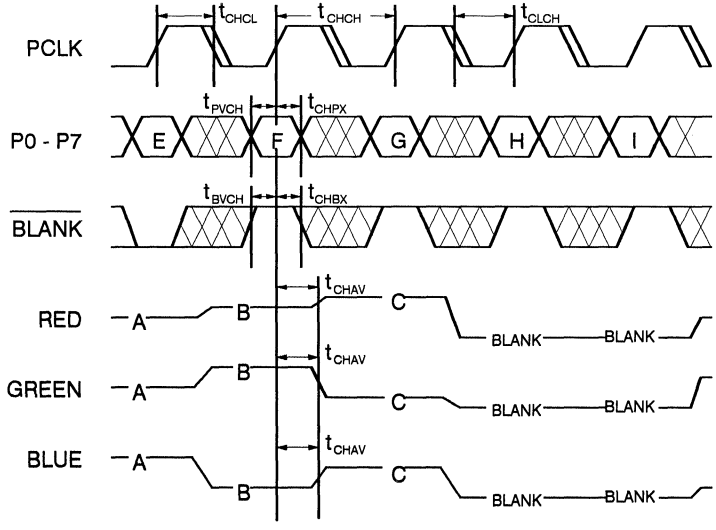
Symbol	Parameter	Conditions	All Min	All Typ	35MHz Max	50MHz Max	Units
RES	Resolution			6			Bits
ILE	Integral Linearity Error	Note A			±0.5	±0.5	LSB
COR	DAC to DAC Correlation	Note B			±2	±2	%
FSE	Full Scale Error	Note C			±5	±5	%
DVT	Glitch Energy	Notes D, E		75			pVsec
IO	Output Current	VO < 1V		18.6	21	21	mA
VO	Output Voltage	IO < 21mA		0.7	1.5	1.5	V
t_{DR}	Rise Time (10% to 90%)	Notes D, E			8	8	ns
t_{DF}	Full Scale Settling Time	Notes D, E, F			28	20	ns

9

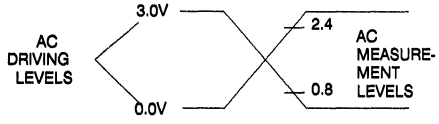
Video Timing Characteristics

Symbol	Parameter	Conditions	All Max	35MHz Min	50MHz Min	Units
t_{CHCH}	PCLK Period (τ)		10000	28	20	ns
Δt_{CHCH}	PCLK Jitter	$t_{CHCH} = \tau$	±2.5			%
t_{CLCH}	PCLK Low Width		10000	9	6	ns
t_{CHCL}	PCLK High Width		10000	9	6	ns
t_{PVCH}	Pixel Word Setup Time			5	4	ns
t_{CHPX}	Pixel Word Hold Time			5	4	ns
t_{BVCH}	$\overline{\text{BLANK}}$ Setup Time			5	4	ns
t_{CHBX}	$\overline{\text{BLANK}}$ Hold Time			5	4	ns
t_{CHAV}	PCLK to DAC Output Valid	Note G	30	5	5	ns
Δt_{CHAV}	Differential Output Delay	Note H	2			ns
t_{CC}	Pixel Clock Transition Time		50			ns

Video Timing Waveforms Diagram

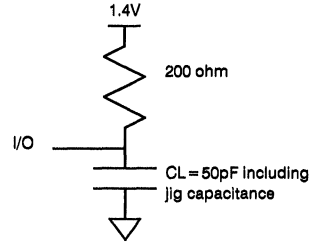


Input Test Waveforms



Notes: 1. t_R, t_F <3 ns (10% to 90%).
2. Input timing reference is at 1.5V.

Digital Input/Output Load



MPU Interface Timing Characteristics

Symbol	Parameter	Conditions	All Max	35MHz Min	50MHz Min	Units
t_{WLWH}	$\overline{WR}$ Pulse Width Low			50	50	ns
t_{RLRH}	$\overline{RD}$ Pulse Width Low			50	50	ns
t_{SVWL}	Register Select Setup Time	WRITE Operations		15	10	ns
t_{SVRL}	Register Select Setup Time	READ Operations		15	10	ns
t_{WLSX}	Register Select Hold Time	WRITE Operations		15	10	ns
t_{RLSX}	Register Select Hold Time	READ Operations		15	10	ns
t_{DVWH}	Write Data Setup Time			15	10	ns
t_{WHDX}	Write Data Hold Time			15	10	ns
t_{RLQX}	Output Turn-on Delay			5	5	ns
t_{RLQV}	Read Enable Access Time		40			ns
t_{RHQX}	Output Hold Time			5	5	ns
t_{RHQZ}	Output Turn-off Delay	Note I	20			ns
t_{WHWL1}	Successive Write Interval	τ = PCLK Period		3τ	3τ	ns
t_{WHRL1}	Write Followed by Read Interval	τ = PCLK Period		3τ	3τ	ns
t_{RHRL1}	Successive Read Interval	τ = PCLK Period		3τ	3τ	ns
t_{RHWL1}	Read Followed by Write Interval	τ = PCLK Period		3τ	3τ	ns
t_{WHWL2}	Write After Color Write	τ = PCLK Period		3τ	3τ	ns
t_{WHRL2}	Read After Color Write	τ = PCLK Period		3τ	3τ	ns
t_{RHRL2}	Read After Color Read	τ = PCLK Period		6τ	6τ	ns
t_{RHWL2}	Write After Color Read	τ = PCLK Period		6τ	6τ	ns
t_{WHRL3}	Read After Read Address Write	τ = PCLK Period		6τ	6τ	ns
t_{WREN}	Read/Write Enable Transition Time		50			ns

Pixel Mask Synchronization Timing

Symbol	Parameter	Conditions	All Max	35MHz Min	50MHz Min	Units
t_{WLCH}	$\overline{WR}$ Illegal Transition Window	Notes J, K	12	1	1	ns
t_{DVWL}	Data Setup Time	Note K		15	15	ns

Notes

Note A: Measured from best fit line through DAC transfer curve.

Note B: Measured from the mid point of the distribution of the three DAC transfer curves.

Note C: $FSE = \left[\frac{VO - 2.1 \times IREF \times R_{Load}}{2.1 \times IREF \times R_{Load}}\right] \times 100\%$

Note D: Z_{Load}=37.5 ohm + 30pF, IREF=-8.88mA

Note E: This parameter is sampled and not 100% tested.

Note F: Measured from a 2% change in the DAC output voltage to within 2% of the final value.

Note G: Measured between the 50% point of the rising edge of PCLK and at the analog output half way between successive output values.

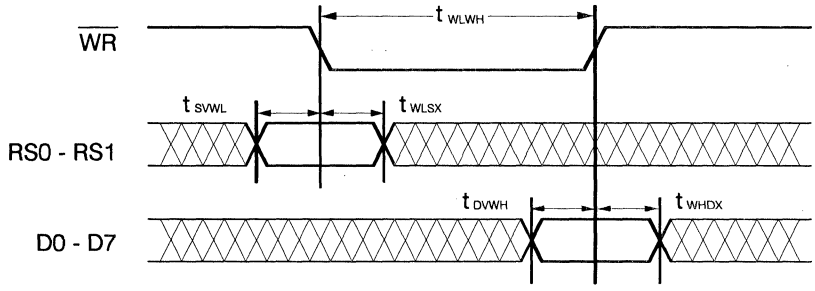
Note H: Measured between different analog outputs on the same device.

Note I: Measured at ±200mV from steady state output values.

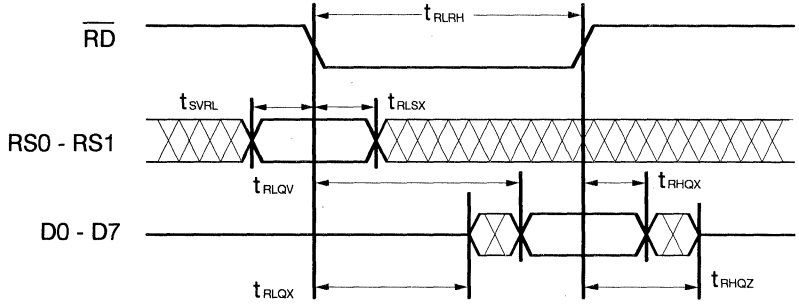
Note J: $\overline{WR}$ should be active (i.e. low) within this timing window.

Note K: This parameter is required to synchronize the Pixel Mask Register to the pixel stream.

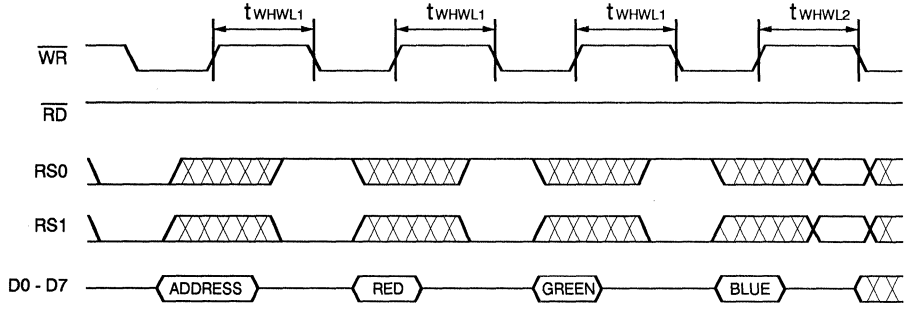
Write Operations Waveforms



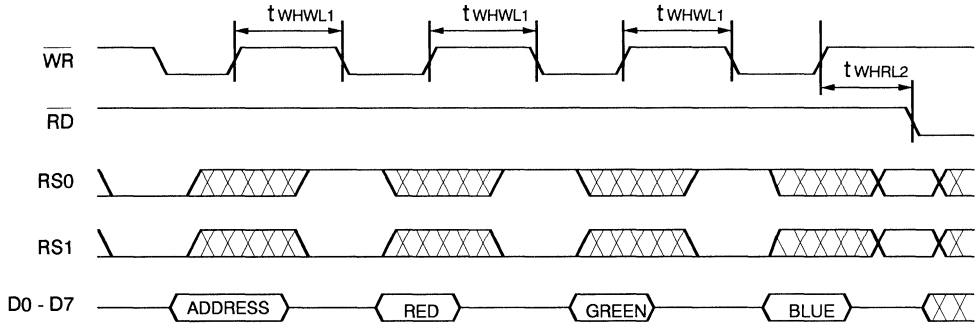
Read Operations Waveforms



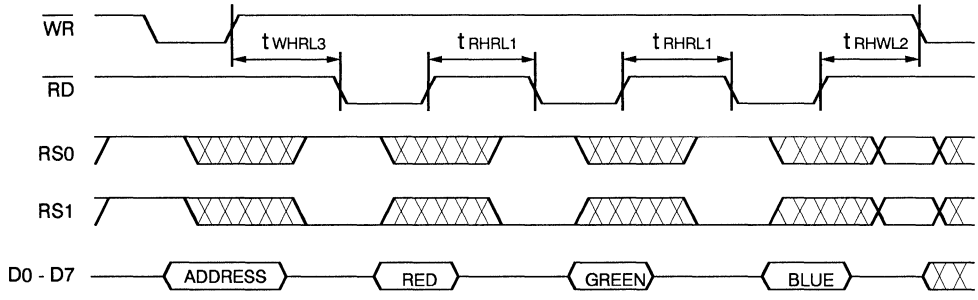
A.C. Waveforms for Color Value Write Followed by Any Write



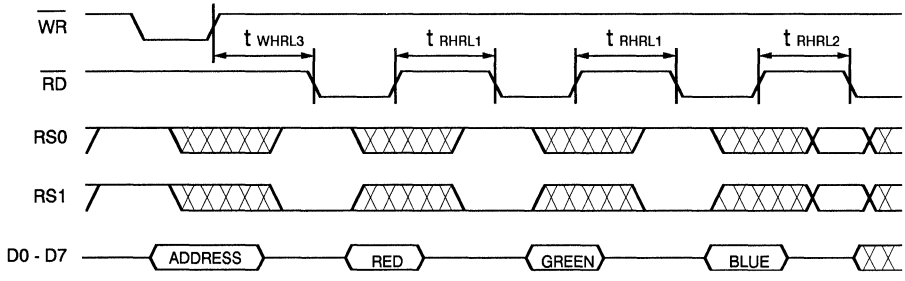
A.C. Waveforms for Color Value Write Followed by Any Read



A.C. Waveforms for Color Value Read Followed by Any Write

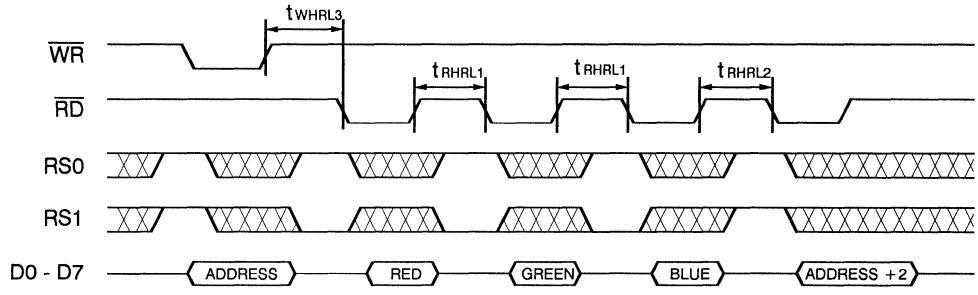


A.C. Waveforms for Color Value Read Followed by Any Read

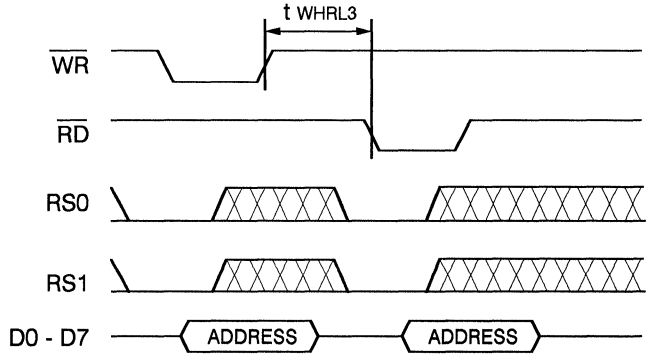


A.C. Waveforms for Color Value Read

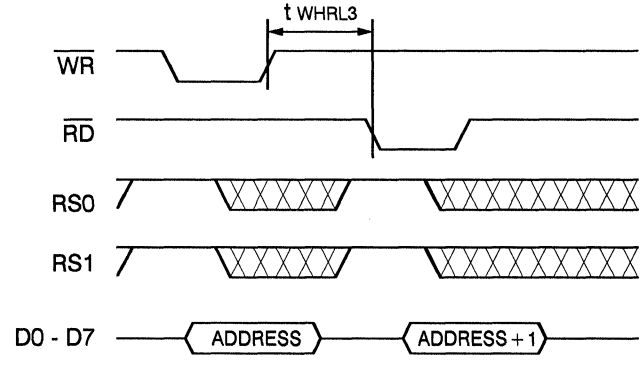
Followed by Pixel Address (Read Mode) Read



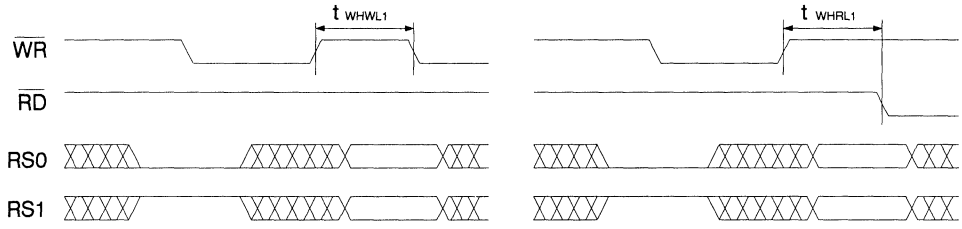
A.C. Waveforms for Pixel Address (Write Mode) Write and Read Back



A.C. Waveforms for Pixel Address (Read Mode) Write and Read Back

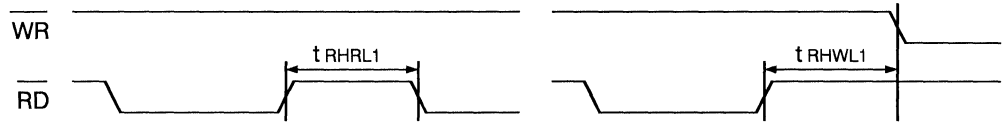


A.C Waveforms for Pixel Mask Write Followed by Any Write or Read



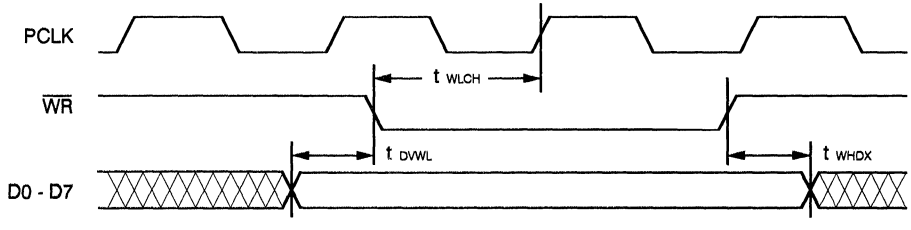
A.C. Waveforms for Pixel Mask or Pixel Address Read

Followed by Any Read or Write



9

A.C. Waveforms for Pixel Mask Synchronization



Ordering Information

Speed (MH_z)	Power Supply	Ordering Code	Package	Operation Range
35	±10%	AT76C171-35PC AT76C171-35JC	28P6 32J	Commercial (0°C to 70°C)
		AT76C171-35PI AT76C171-35JI	28P6 32J	Industrial (-40°C to 85°C)
35	±5%	AT76C171-35DM	28D6	Military (-55°C to 125°C)
50	±10%	AT76C171-50PC AT76C171-50JC	28P6 32J	Commercial (0°C to 70°C)
		AT76C171-50PI AT76C171-50JI	28P6 32J	Industrial (-40°C to 85°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier, OTP (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package, OTP (PDIP)

Features

- **Personal System/2* and VGA* Compatible**
- **Pixel Rates to 66 MHz**
- **Triple 6-Bit DACs Display 256K Possible Colors**
- **Pixel Word Mask and Composite Blank on All Three Channels**
- **18-Bit Wide Color Palette Stores 256 Colors**
- **RGB Video Outputs Drive 37.5 Ohm Loads Directly**
- **Low Power, Low Glitch Operation**
- **Asynchronous MPU Read/Write to All Internal Registers**
- **Single +5 V Supply**
- **Available in Standard 28 Pin DIP and 32 Pin Plastic LCC**
- **Full Military, Commercial and Industrial Temperature Ranges**

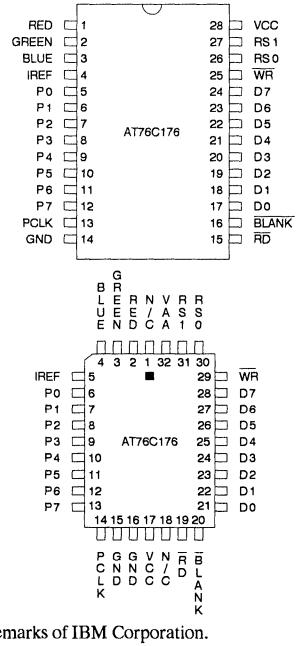
CMOS Triple Video DAC Color Palette

Description

The AT76C176 is a second generation color palette DAC which provides direct drives for RGB color displays. The AT76C176 integrates three high performance 6-bit video DACs (Digital-to-Analog Converters), an advanced 256 x 18 Color Palette (Color Look-up Table) and a versatile microprocessor interface on a monolithic substrate.

The AT76C176 supports the RS170 video standard and graphics controllers compatible with the VGA standard. This device allows 256 colors to be displayed out of a total of 262,144 colors. The AT76C176 provides composite blank outputs on all three channels. Additional advanced features include on-chip pixel mask logic which allows displayed colors to be modified in a single write cycle rather than by altering the contents of the color palette.

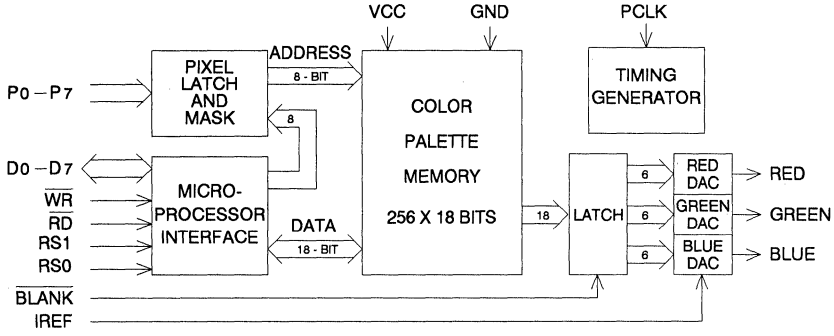
Pin Configurations



Pin Name	Function
RED GREEN BLUE	Analog Video Outputs for R,G,B Guns
IREF	Reference Current Input
P0-P7	Pixel Address Inputs
PCLK	Pixel Clock Input
GND	Ground
$\overline{RD}$	Read Enable Input
$\overline{BLANK}$	Video Blanking Input
D0-D7	Program Data I/O
$\overline{WR}$	Write Enable Input
RS0,RS1	Register Select Inputs
VCC	+5 Volts Supply Input
VAA	+5 Volts Analog Supply Input
N/C	No Connect

* Personal System/2 and VGA are registered trademarks of IBM Corporation.

Block Diagram



Pin Definitions

	Symbol	Functional Descriptions
Video Interface	RED GREEN BLUE	Analog Video Outputs. These are the outputs of the triple video DACs. The 18-bit wide color palette output and the $\overline{\text{BLANK}}$ input drive the DAC inputs.
	IREF	Reference Current Input. The Reference Current sets the full scale current sourced by each DAC.
	P0-P7	Pixel Address Inputs. The 8-bit Pixel Address is logically AND'ed with the Pixel Mask value before it is used to select a stored 18-bit color value from the palette.
	PCLK	Pixel (or Dot) Clock Input. The rising edge of PCLK samples the Pixel Address and $\overline{\text{BLANK}}$ inputs. PCLK is the system clock for the palette DAC pipeline.
	$\overline{\text{BLANK}}$	Blanking Input. A logic "0" at $\overline{\text{BLANK}}$ input overrides the current color value and forces the Analog Video Outputs to the zero (or Blank) level. The Color Palette can be updated while Blanking is active.
Power Supply	GND	Ground. GND should be connected to a solid ground plane in the system.
	VCC	Digital Supply. Nominal 5 Volts. VCC should be bypassed to GND with a high-frequency capacitor.
	VAA	Analog Supply. Nominal 5 Volts. VAA should be connected to a filtered system supply.
Microprocessor Interface	$\overline{\text{RD}}$	Read Enable Input. $\overline{\text{RD}}$ controls the timing of microprocesssor Read operations.
	$\overline{\text{WR}}$	Write Enable Input. $\overline{\text{WR}}$ controls the timing of microprocessor Write operations. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should not be active (low) at the same time.
	D0-D7	Program Data I/O Ports (Bidirectional). The rising edge of $\overline{\text{WR}}$ latches Program Data at D7-D0 into the selected internal register. The falling edge of $\overline{\text{RD}}$ enables D7-D0 as outputs and the rising edge of $\overline{\text{RD}}$ returns D7-D0 to a high impedance state.
	RS0, RS1	Register Select Inputs. Control the selection of internal registers. (See description on Internal Registers.) The falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ latches in the value at RS1, RSO.

Internal Registers

RS1	RS0	Bits	Register Name	Functional Description
0	0	8	Pixel Address (Write Mode)	The Pixel Address Register is accessed via Register Address (0,0) or (1,1). Reading the Pixel Address value from (0,0) is the same as reading from (1,1). A pixel address value is normally written to Pixel Address Register at (0,0) before one or more color values are written to the Color Palette. A pixel address value is normally written to Pixel Address Register at (1,1) before one or more color values are read from the Color Palette.
1	1	8	Pixel Address (Read Mode)	
0	1	18	Color Value	The Color Value Register acts as a buffer between the 18-bit wide Color Palette and the 8-bit microprocessor interface. Each READ and WRITE at (0,1) consists of three byte transfers in the order of RED first, Green second and BLUE last. Only the LSBs D5-D0 of each byte are used, the two MSBs are set to "0" when a color value is read. The Pixel Address Register automatically increments after each 18-bit color value Read or Write operation. Each color value READ or WRITE operation overrides the pixel stream for one PCLK period.
1	0	8	Pixel Mask	The Pixel Mask value is bitwise AND'ed with the Pixel Address value at P7-P0. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Address supplied via the microprocessor interface is not affected by the Pixel Mask.

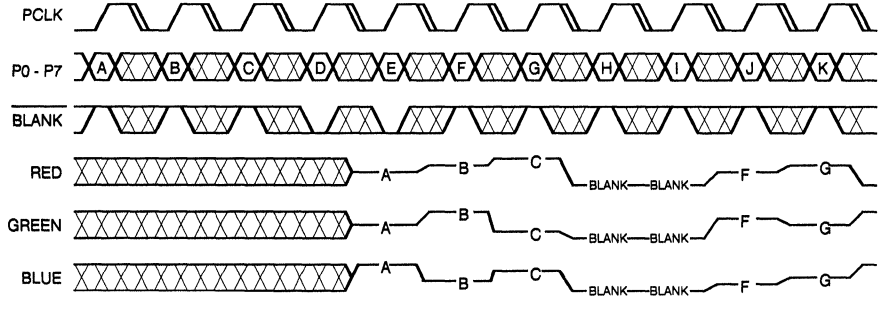
Device Operation

COLOR PALETTE: The AT76C176 provides an 18-bit wide by 256 word deep color palette static RAM array for storing the desired color intensity values. Each word is divided into three fields for the RED, GREEN and BLUE video DACs respectively. The 8-bit wide Pixel Address is decoded and used to select a particular location in the RAM array. The color value retrieved from that location is then used as inputs to the three video DACs which convert the digital color code into analog color intensity values.

The AT76C176 achieves low power, high speed operation by using an advanced pipelined palette DAC architecture. Delay from Pixel Address to color intensity value out is 3 PCLK periods.

9

Video Pipeline Timing Diagram



MPU INTERFACE: The AT76C176 provides a standard microprocessor interface which allows the host display controller to access the Color Palette RAM and all internal registers of the AT76C176. MPU READ and WRITE operations are internally synchronized with the video pipeline and therefore can take place asynchronously from the normal pixel mapping operation. An on-chip address counter allows the MPU to READ or WRITE the Color Palette in a Block Mode.

COLOR PALETTE READ AND WRITE: Four MPU operations are required to write (i.e. store a Color Value) to a specific location in the Color Palette RAM. The desired RAM address is first written into the internal Pixel Address register by executing a WRITE operation at register address (0,0). A new Color Value is next written into the internal Color Value register at register address (0,1) by three consecutive WRITE operations, with the RED color first, GREEN second and BLUE last. Only LSBs D5-D0 of each byte transferred are used. The new Color Value is then automatically written into the designated address in the Color Palette RAM.

Similarly, four MPU operations are required to read a Color Value from a specific location in the Color Palette RAM. The RAM address is written into the internal Pixel Address register by executing a WRITE operation at register address (1,1). The Color Value stored in that particular RAM location is automatically transferred to the internal Color Value Register. Three consecutive READ operations are then required to read the retrieved Color Value in three bytes, with the RED color first, GREEN second and BLUE last. Only the last 6 LSBs D5-D0 contain valid data, the two MSBs are set to "0".

BLOCK READ AND WRITE MODE: The on-chip Pixel Address Register automatically increments by one after each complete Color Value READ or WRITE operation. This useful feature allows an entire block of the Color Palette RAM to be accessed by simply writing the starting address into the Pixel Address register at the appropriate register address. Subsequent READ or WRITE operations require only 3-byte transfers at D7-D0.

TRIPLE VIDEO DAC: Each of the three video DACs on the AT76C176 consists of an array of current sources tied to a common output. The current sources use an advanced current steering scheme to minimize glitch energy. The number of current sources in each DAC steered to the output during any PCLK period equals the value represented by the Color Value selected from the Color Palette. The rest of the current sources are steered to ground.

The input Reference Current (IREF) determines the current in each current source. Each DAC is designed to produce a 0.7 Volt peak white level when driving a doubly terminated 75 ohm load with IREF = -8.88 mA. The relationship between the peak white level and IREF is given by the equation:

$$V_{Peak\ White} = 2.1 \times IREF \times R_{Load}$$

BLANKING: The AT76C176 supports composite blanking at all three RED, GREEN and BLUE video outputs. The $\overline{BLANK}$ input is latched on the rising edge of PCLK and affects the analog video outputs after 3 PCLK periods. An internal pipelined delay circuit is used to synchronize the $\overline{BLANK}$ input with the normal pixel pipeline. A logic "0" at $\overline{BLANK}$ input overrides the current color value and forces the analog video outputs to the zero (or Blank) level. The $\overline{BLANK}$ circuit has no effect on the MPU interface and the Color Palette remains accessible via READ and WRITE.

PIXEL MASK: The AT76C176 features an advanced on-chip Pixel Mask which is very useful for cursor control, flashing objects, and animation. The Pixel Mask value stored in internal register (1,0) is bitwise AND'ed with the input Pixel Address value at P7-P0 to form the actual RAM address for the Color Palette. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Addresses supplied via the MPU interface are not affected by the Pixel Mask.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-2.0V to 7.0V(1)
Power Dissipation	1.5W
Reference Current	-15mA
Analog Output Current	45mA
DC Digital Output Current	25mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is VCC+0.75V DC which may overshoot to 7.0V for pulses of less than 20ns.

D.C. and A.C. Operating Range

		AT76C176-66	AT76C176-50	AT76C176-40	VCC/VAA Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C			5V +/- 5%
			0° C - 70° C	0° C - 70° C	5V +/- 10%
	Ind.		-40° C - 85° C	-40° C - 85° C	5V +/- 10%
	Mil.			-55° C -125° C	5V +/- 5%

D.C. Characteristics

Symbol	Parameter	Conditions	All Min	40MHz Max	50MHz Max	66MHz Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 0.1V		10	10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V		10	10	10	µA
I_{CC}	Power Supply Current	IO = 21mA Digital Outputs Open		140	150	170	mA
I_{REF}	Reference Current		-7	-10	-10	-10	mA
V_{IL}	Input Low Voltage		-0.5	0.8	0.8	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V_{CC} + 0.5	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	IO = 5mA		0.4	0.4	0.4	V
V_{OH}	Output High Voltage	IO = -5mA	2.4				V
V_{REF}	Voltage at IREF Input		V_{CC}-3	V_{CC}	V_{CC}	V_{CC}	V

9

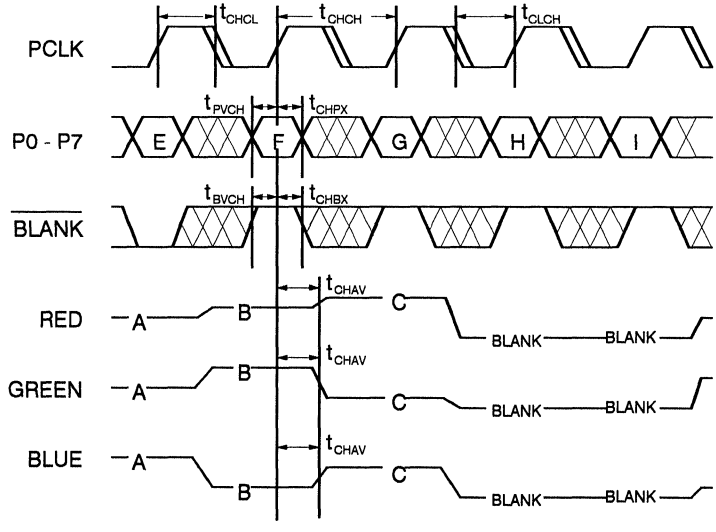
Video DAC Characteristics

Symbol	Parameter	Conditions	All Min	All Typ	40MHz Max	50MHz Max	66MHz Max	Units
RES	Resolution		6					Bits
ILE	Integral Linearity Error	Note A			±0.5	±0.5	±0.5	LSB
COR	DAC to DAC Correlation	Note B			±2	±2	±2	%
FSE	Full Scale Error	Note C			±5	±5	±5	%
DVT	Glitch Energy	Notes D, E		75				pVsec
IO	Output Current	VO < 1V		18.6	21	21	21	mA
VO	Output Voltage	IO < 21mA		0.7	1.5	1.5	1.5	V
t_{DR}	Rise Time (10% to 90%)	Notes D, E			8	8	6	ns
t_{DF}	Full Scale Settling Time	Notes D, E, F			25	20	15	ns

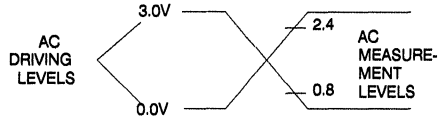
Video Timing Characteristics

Symbol	Parameter	Conditions	All Max	40MHz Min	50MHz Min	66MHz Min	Units
t_{CHCH}	PCLK Period (τ)		10000	28	20	15	ns
Δt_{CHCH}	PCLK Jitter	$t_{CHCH} = \tau$	±2.5				%
t_{CLCH}	PCLK Low Width		10000	9	6	5	ns
t_{CHCL}	PCLK High Width		10000	7	6	5	ns
t_{PVCH}	Pixel Word Setup Time			5	4	3	ns
t_{CHPX}	Pixel Word Hold Time			5	4	3	ns
t_{BVCH}	$\overline{\text{BLANK}}$ Setup Time			5	4	3	ns
t_{CHBX}	$\overline{\text{BLANK}}$ Hold Time			5	4	3	ns
t_{CHAV}	PCLK to DAC Output Valid	Note G	30	5	5	5	ns
Δt_{CHAV}	Differential Output Delay	Note H	2				ns
t_{CC}	Pixel Clock Transition Time		50				ns

Video Timing Waveforms Diagram

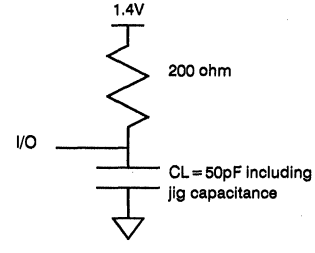


Input Test Waveforms



Notes: 1. t_R, t_F <3 ns (10% to 90%).
2. Input timing reference is at 1.5V.

Digital Input/Output Load



MPU Interface Timing Characteristics

Symbol	Parameter	Conditions	All Max	40MHz Min	50MHz Min	66MHz Min	Units
t_{WLWH}	$\overline{WR}$ Pulse Width Low			50	50	50	ns
t_{RLRH}	$\overline{RD}$ Pulse Width Low			50	50	50	ns
t_{SVWL}	Register Select Setup Time	WRITE Operations		15	10	10	ns
t_{SVRL}	Register Select Setup Time	READ Operations		15	10	10	ns
t_{WLSX}	Register Select Hold Time	WRITE Operations		15	10	10	ns
t_{RLSX}	Register Select Hold Time	READ Operations		15	10	10	ns
t_{DVWH}	Write Data Setup Time			15	10	10	ns
t_{WHDX}	Write Data Hold Time			15	10	10	ns
t_{RLQX}	Output Turn-on Delay			5	5	5	ns
t_{RLQV}	Read Enable Access Time		40				ns
t_{RHQX}	Output Hold Time			5	5	5	ns
t_{RHQZ}	Output Turn-off Delay	Note I	20				ns
t_{WHWL1}	Successive Write Interval	τ = PCLK Period		4τ	4τ	4τ	ns
t_{WHRL1}	Write Followed by Read Interval	τ = PCLK Period		4τ	4τ	4τ	ns
t_{RHRL1}	Successive Read Interval	τ = PCLK Period		4τ	4τ	4τ	ns
t_{RHWL1}	Read Followed by Write Interval	τ = PCLK Period		4τ	4τ	4τ	ns
t_{WHWL2}	Write After Color Write	τ = PCLK Period		4τ	4τ	4τ	ns
t_{WHRL2}	Read After Color Write	τ = PCLK Period		4τ	4τ	4τ	ns
t_{RHRL2}	Read After Color Read	τ = PCLK Period		7τ	7τ	7τ	ns
t_{RHWL2}	Write After Color Read	τ = PCLK Period		7τ	7τ	7τ	ns
t_{WHRL3}	Read After Read Address Write	τ = PCLK Period		7τ	7τ	7τ	ns
t_{WREN}	Read/Write Enable Transition Time		50				ns

Notes

Note A: Measured from best fit line through DAC transfer curve.

Note B: Measured from the mid point of the distribution of the three DAC transfer curves.

Note C: $FSE = \left[\frac{VO - 2.1 \times IREF \times R_{Load}}{2.1 \times IREF \times R_{Load}}\right] \times 100\%$

Note D: Z_{Load}=37.5 ohm + 30pF, IREF=-8.88mA

Note E: This parameter is sampled and not 100% tested.

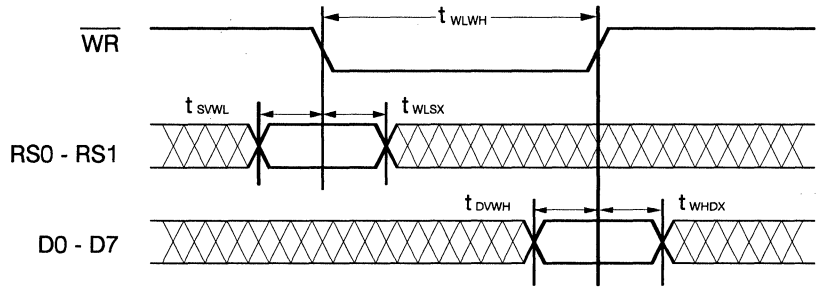
Note F: Measured from a 2% change in the DAC output voltage to within 2% of the final value.

Note G: Measured between the 50% point of the rising edge of PCLK and at the analog output half way between successive output values.

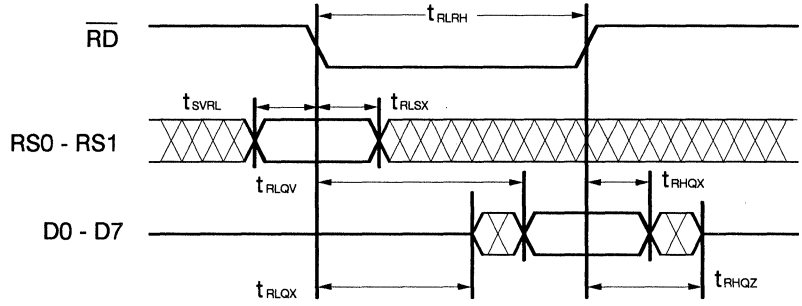
Note H: Measured between different analog outputs on the same device.

Note I: Measured at ±200mV from steady state output values.

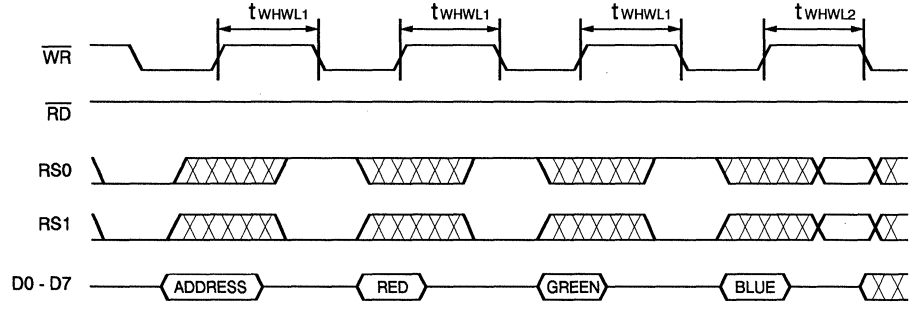
Write Operations Waveforms



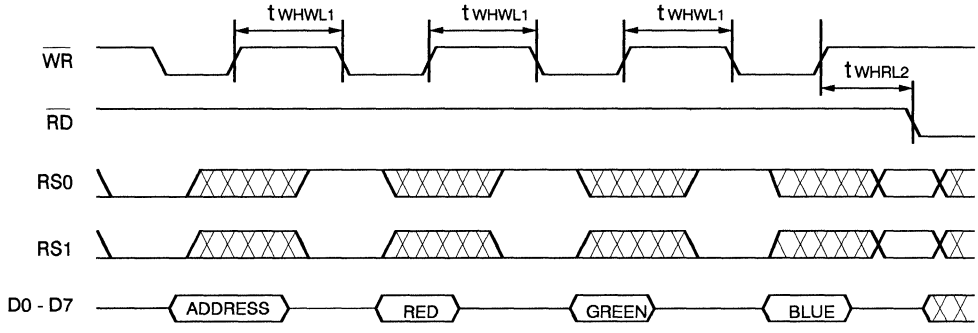
Read Operations Waveforms



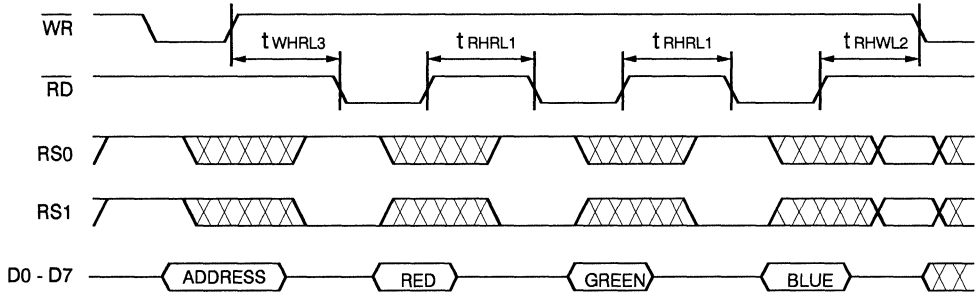
A.C. Waveforms for Color Value Write Followed by Any Write



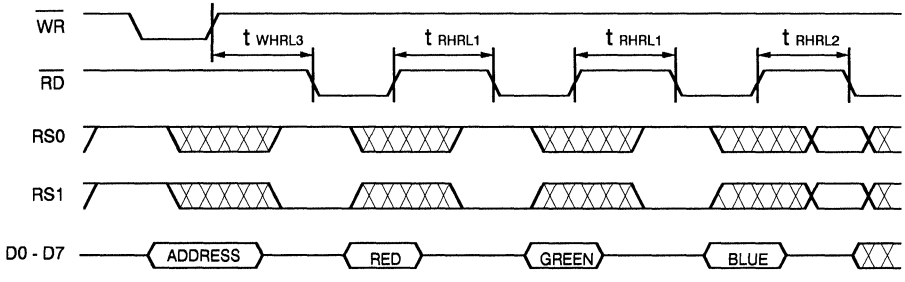
A.C. Waveforms for Color Value Write Followed by Any Read



A.C. Waveforms for Color Value Read Followed by Any Write

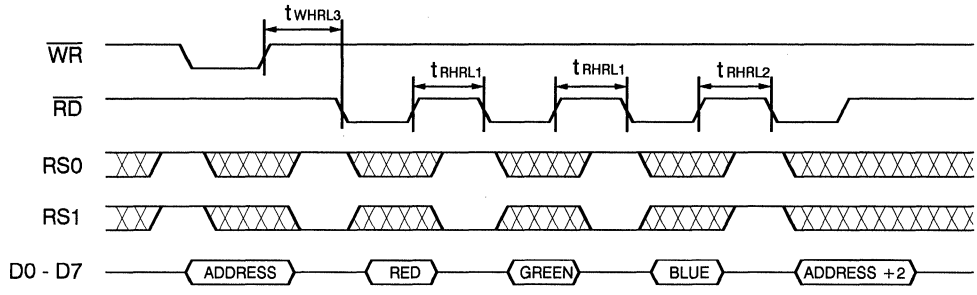


A.C. Waveforms for Color Value Read Followed by Any Read

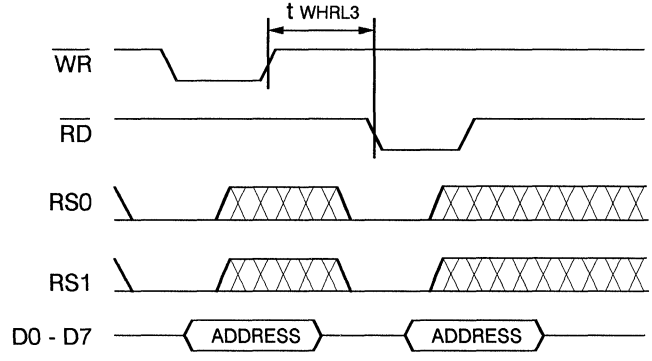


A.C. Waveforms for Color Value Read

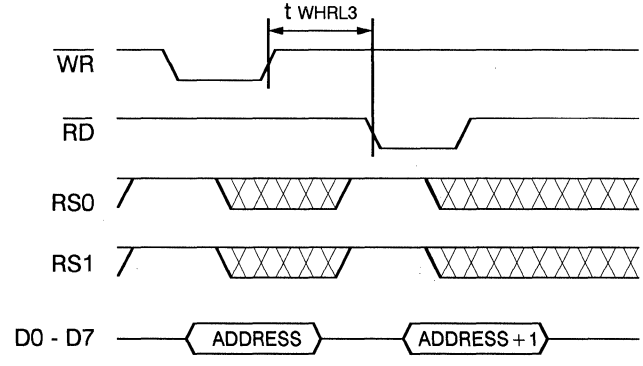
Followed by Pixel Address (Read Mode) Read



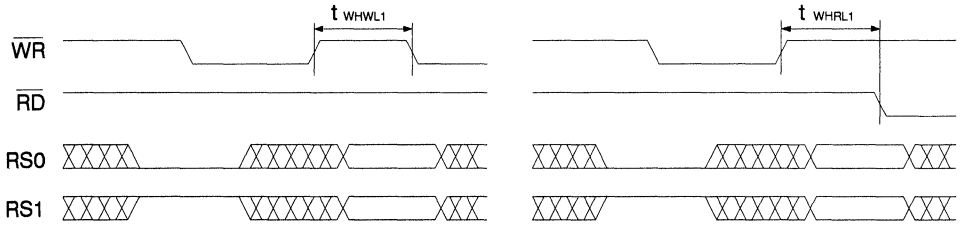
A.C. Waveforms for Pixel Address (Write Mode) Write and Read Back



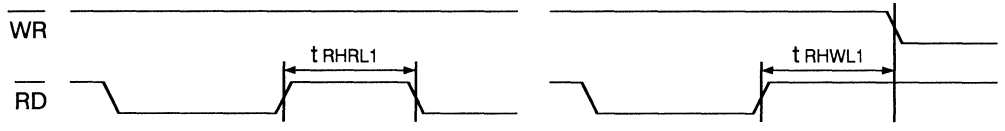
A.C. Waveforms for Pixel Address (Read Mode) Write and Read Back



A.C Waveforms for Pixel Mask Write Followed by Any Write or Read



A.C. Waveforms for Pixel Mask or Pixel Address Read Followed by Any Read or Write



9

Ordering Information

Speed (MH_z)	Power Supply	Ordering Code	Package	Operation Range
40	±10%	AT76C176-40PC AT76C176-40JC	28P6 32J	Commercial (0°C to 70°C)
		AT76C176-40PI AT76C176-40JI	28P6 32J	Industrial (-40°C to 85°C)
40	±5%	AT76C176-40DM	28D6	Military (-55°C to 125°C)
50	±10%	AT76C176-50PC AT76C176-50JC	28P6 32J	Commercial (0°C to 70°C)
		AT76C176-50PI AT76C176-50JI	28P6 32J	Industrial (-40°C to 85°C)
66	±5%	AT76C176-66PC AT76C176-66JC	28P6 32J	Commercial (0°C to 70°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

FEATURES

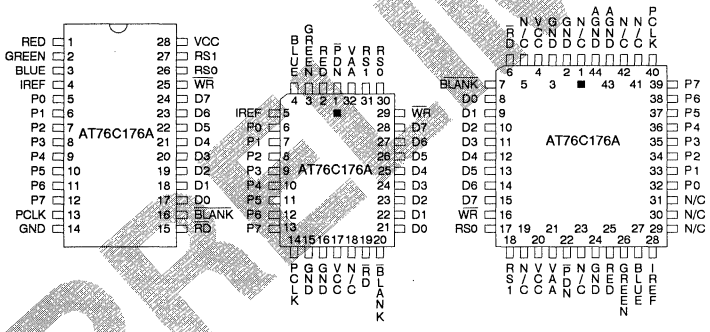
- **Personal System/2*, 8514A, and VGA* Compatible**
- **High Pixel Rates to 110 MHz**
- **Supports High Resolution 1280 x 1280 Pixels Color Graphics Displays**
- **Low Standby Current Less than 100μA (PLCC Packages Only)**
- **Triple 6-Bit DACs Display 256K Possible Colors**
- **Pixel Word Mask and Composite Blank on All Three Channels**
- **18-Bit Wide Color Palette Stores 256 Colors**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200mA Latchup Immunity**
- **Single +5 V Supply**
- **Available in Standard 28 Pin DIP, and 32 and 44 Pin Plastic LCC**
- **Full Military, Commercial and Industrial Temperature Ranges**

Description

The AT76C176A is a second generation color palette DAC which provides direct drives for high resolution RGB color displays with resolutions up to 1280 x 1280 pixels. The AT76C176A integrates three high performance 6-bit video DACs (Digital-to-Analog Converters), an advanced 256 x 18 Color Palette (Color Look-up Table) and a versatile microprocessor interface on a monolithic substrate.

The AT76C176A supports the RS170 video standard and graphics controllers compatible with the VGA and extended VGA standards. This device allows 256 colors to be displayed out of a total of 262,144 colors. The AT76C176A provides composite blank outputs on all three channels. Additional advanced features include on-chip pixel mask logic which allows displayed colors to be modified in a single write cycle rather than by altering the contents of the color palette. For lap-top computers and other battery powered applications, the AT76C176A provides a low power standby mode of operation.

Pin Configurations



Pin Name	Function
RED GREEN BLUE	Analog Video Outputs for R,G,B Guns
IREF	Reference Current Input
P0-P7	Pixel Address Inputs
PCLK	Pixel Clock Input
AGND	Analog Ground
GND	Ground
$\overline{RD}$	Read Enable Input

$\overline{BLANK}$	Video Blanking Input
D0-D7	Program Data I/O
$\overline{WR}$	Write Enable Input
RS0,RS1	Register Select Inputs
$\overline{PDN}$	Power-Down Input
VCC	+5 Volts Supply Input
VAA	+5 Volts Analog Supply Input
N/C	No Connect

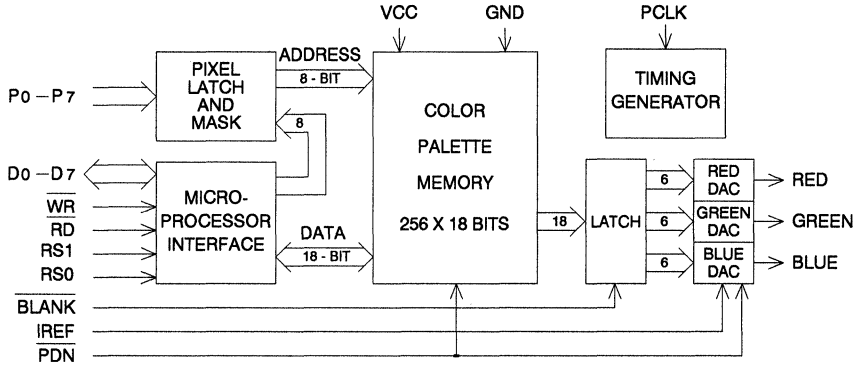
* Personal System/2 and VGA are registered trademarks of IBM Corporation.

110 MHz Monolithic CMOS Hi-Res Video Color Palette

Preliminary

9

Block Diagram



Pin Definitions

	Symbol	Functional Descriptions
Video Interface	RED GREEN BLUE	Analog Video Outputs. These are the outputs of the triple video DACs. The 18-bit wide color palette output and the $\overline{\text{BLANK}}$ input drive the DAC inputs.
	IREF	Reference Current Input. The Reference Current sets the full scale current sourced by each DAC.
	P0-P7	Pixel Address Inputs. The 8-bit Pixel Address is logically AND'ed with the Pixel Mask value before it is used to select a stored 18-bit color value from the palette.
	PCLK	Pixel (or Dot) Clock Input. The rising edge of PCLK samples the Pixel Address and $\overline{\text{BLANK}}$ inputs. PCLK is the system clock for the palette DAC pipeline.
	$\overline{\text{BLANK}}$	Blanking Input. A logic "0" at $\overline{\text{BLANK}}$ input overrides the current color value and forces the Analog Video Outputs to the zero (or Blank) level. The Color Palette can be updated while Blanking is active.
Power Supply	AGND GND	Ground. Both AGND and GND should be connected to a solid ground plane in the system.
	VCC	Digital Supply. Nominal 5 Volts. VCC should be bypassed to GND with a high-frequency capacitor.
	VAA	Analog Supply. Nominal 5 Volts. VAA should be connected to a filtered system supply.
Microprocessor Interface	$\overline{\text{RD}}$	Read Enable Input. $\overline{\text{RD}}$ controls the timing of microprocessor Read operations.
	$\overline{\text{WR}}$	Write Enable Input. $\overline{\text{WR}}$ controls the timing of microprocessor Write operations. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should not be active (low) at the same time.
	D0-D7	Program Data I/O Ports (Bidirectional). The rising edge of $\overline{\text{WR}}$ latches Program Data at D7-D0 into the selected internal register. The falling edge of $\overline{\text{RD}}$ enables D7-D0 as outputs and the rising edge of $\overline{\text{RD}}$ returns D7-D0 to a high impedance state.
	RS0, RS1	Register Select Inputs. Control the selection of internal registers. (See description on Internal Registers.) The falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ latches in the value at RS1, RSO.
	$\overline{\text{PDN}}$	Power-Down Input. A logic "0" at $\overline{\text{PDN}}$ input powers down the video DAC and Color Palette circuits for low power standby mode operation. The Color Palette can still be read or updated if PCLK is active. $\overline{\text{PDN}}$ should be held at logic "1" for normal operation.

Internal Registers

RS1	RS0	Bits	Register Name	Functional Description
0	0	8	Pixel Address (Write Mode)	The Pixel Address Register is accessed via Register Address (0,0) or (1,1). Reading the Pixel Address value from (0,0) is the same as reading from (1,1). A pixel address value is normally written to Pixel Address Register at (0,0) before one or more color values are written to the Color Palette. A pixel address value is normally written to Pixel Address Register at (1,1) before one or more color values are read from the Color Palette.
1	1	8	Pixel Address (Read Mode)	
0	1	18	Color Value	The Color Value Register acts as a buffer between the 18-bit wide Color Palette and the 8-bit microprocessor interface. Each READ and WRITE at (0,1) consists of three byte transfers in the order of RED first, Green second and BLUE last. Only the LSBs D5-D0 of each byte are used, the two MSBs are set to "0" when a color value is read. The Pixel Address Register automatically increments after each 18-bit color value Read or Write operation. Each color value READ or WRITE operation overrides the pixel stream for one PCLK period.
1	0	8	Pixel Mask	The Pixel Mask value is bitwise AND'ed with the Pixel Address value at P7-P0. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Address supplied via the microprocessor interface is not affected by the Pixel Mask.

Device Operation

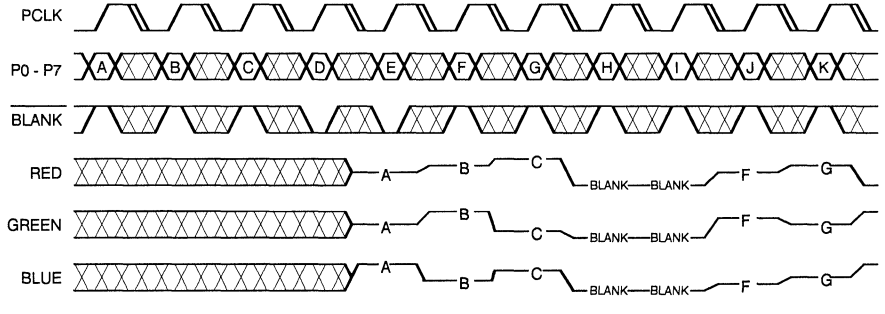
COLOR PALETTE: The AT76C176A provides an 18-bit wide by 256 word deep color palette static RAM array for storing the desired color intensity values. Each word is divided into three fields for the RED, GREEN and BLUE video DACs respectively. The 8-bit wide Pixel Address is decoded and used to select a particular location in the RAM array. The color value retrieved from that location is then used as inputs to the three video DACs which convert the digital color code into analog color intensity values.

The AT76C176A achieves low power, high speed operation by using an advanced pipelined palette DAC architecture. Delay from Pixel Address to color intensity value out is 3 PCLK periods.

MPU INTERFACE: The AT76C176A provides a standard microprocessor interface which allows the host display controller to access the Color Palette RAM and all internal registers of the AT76C176A. MPU READ and WRITE operations are internally synchronized with the video pipeline and therefore can take place asynchronously from the normal pixel mapping operation. An on-chip address counter allows the MPU to READ or WRITE the Color Palette in a Block Mode.

9

Video Pipeline Timing Diagram



COLOR PALETTE READ AND WRITE: Four MPU operations are required to write (i.e. store a Color Value) to a specific location in the Color Palette RAM. The desired RAM address is first written into the internal Pixel Address register by executing a WRITE operation at register address (0,0). A new Color Value is next written into the internal Color Value register at register address (0,1) by three consecutive WRITE operations, with the RED color first, GREEN second and BLUE last. Only LSBs D5-D0 of each byte transferred are used. The new Color Value is then automatically written into the designated address in the Color Palette RAM.

Similarly, four MPU operations are required to read a Color Value from a specific location in the Color Palette RAM. The RAM address is written into the internal Pixel Address register by executing a WRITE operation at register address (1,1). The Color Value stored in that particular RAM location is automatically transferred to the internal Color Value Register. Three consecutive READ operations are then required to read the retrieved Color Value in three bytes, with the RED color first, GREEN second and BLUE last. Only the last 6 LSBs D5-D0 contain valid data, the two MSBs are set to "0".

BLOCK READ AND WRITE MODE: The on-chip Pixel Address Register automatically increments by one after each complete Color Value READ or WRITE operation. This useful feature allows an entire block of the Color Palette RAM to be accessed by simply writing the starting address into the Pixel Address register at the appropriate register address. Subsequent READ or WRITE operations require only 3-byte transfers at D7-D0.

TRIPLE VIDEO DAC: Each of the three video DACs on the AT76C176A consists of an array of current sources tied to a common output. The current sources use an advanced current steering scheme to minimize glitch energy. The number of current sources in each DAC steered to the output during any PCLK period equals the value represented by the Color Value selected from the Color Palette. The rest of the current sources are steered to ground.

The input Reference Current (IREF) determines the current in each current source. Each DAC is designed to produce a 0.7 Volt peak white level when driving a doubly terminated 75 ohm load with IREF = -8.88 mA. The relationship between the peak white level and IREF is given by the equation:

$$V_{Peak\ White} = 2.1 \times IREF \times R_{Load}$$

BLANKING: The AT76C176A supports composite blanking at all three RED, GREEN and BLUE video outputs. The $\overline{BLANK}$ input is latched on the rising edge of PCLK and affects the analog video outputs after 3 PCLK periods. An internal pipelined delay circuit is used to synchronize the $\overline{BLANK}$ input with the normal pixel pipeline. A logic "0" at $\overline{BLANK}$ input overrides the current color value and forces the analog video outputs to the zero (or Blank) level. The $\overline{BLANK}$ circuit has no effect on the MPU interface and the Color Palette remains accessible via READ and WRITE.

PIXEL MASK: The AT76C176A features an advanced on-chip Pixel Mask which is very useful for cursor control, flashing objects, and animation. The Pixel Mask value stored in internal register (1,0) is bitwise AND'ed with the input Pixel Address value at P7-P0 to form the actual RAM address for the Color Palette. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Addresses supplied via the MPU interface are not affected by the Pixel Mask.

POWER-DOWN MODE: In PLCC packages, the AT76C176A provides an on-chip power-down feature for use in lap-top computers and other battery powered applications. During normal operation, pin $\overline{PDN}$ should be held as logic "1." A logic "0" at $\overline{PDN}$ powers down the video DAC and Color Palette circuits. With a reduced PCLK frequency, the Color Palette can be read or updated in the power-down mode.

Further power reduction can be obtained by reducing the frequency of PCLK to the minimum or stopping it altogether.

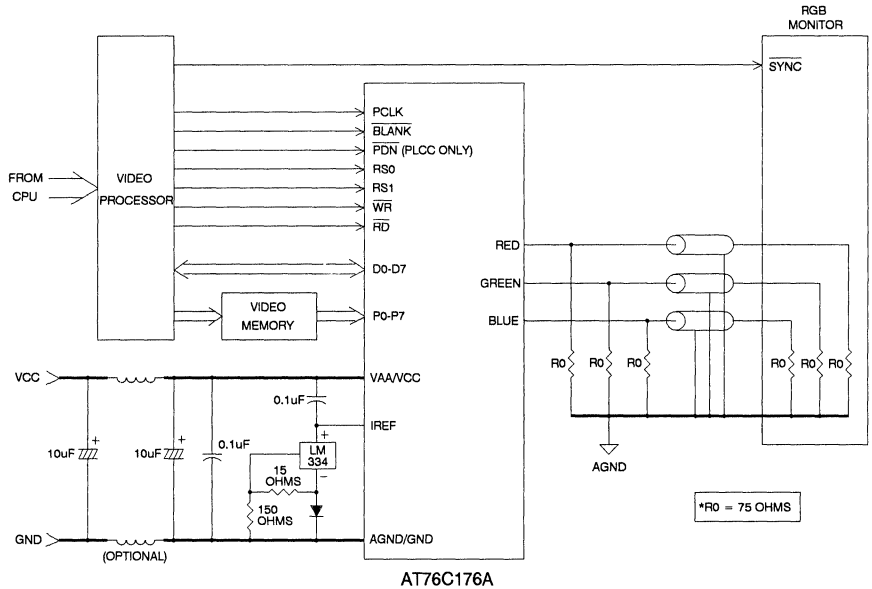
Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-2.0V to 7.0V(1)
Power Dissipation	1.5W
Reference Current	-15mA
Analog Output Current	45mA
DC Digital Output Current	25mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is VCC+0.75V DC which may overshoot to 7.0V for pulses of less than 20ns.

Sample Connection for Typical Application



System Implementation Considerations

POWER SUPPLY DECOUPLING AND GROUNDING: To obtain the cleanest possible analog outputs from the AT76C176A, digital noise coupling into the analog signal paths needs to be minimized. The video data paths, power supply lines and ground planes on the circuit board should be laid out carefully to reduce noise coupling. As illustrated in the diagram showing a Sample Connection for Typical Application, a separate VAA line decoupled to AGND with an electrolytic capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C176A. Similarly, a separate analog ground return, AGND, which is connected to the lowest impedance point in the system ground plane, should be used.

For best results, four layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath the AT76C176A. All video frequency signal traces should be kept as short as possible to minimize radiation and all decoupling capacitors should be placed as close to the AT76C176A as the layout rules permit.

Noise and transients on the power and ground lines can be coupled or aliased into the video circuits by the switching action of the AT76C176A. For applications at 66 MHz and above, it may be necessary to isolate both VAA and AGND from the system supplies with inductors of appropriate values.

CURRENT REFERENCE: The maximum full scale output of the video DACs is determined by the reference current supplied externally at pin IREF. An adjustable current source such as the LM334 is recommended to set the reference current at 8.88 mA for a full scale output of 0.7 Volt when driving a 37.5 ohm load. The video DACs employ current sources which are referenced to the positive supply voltage. A high quality 0.1 μF chip capacitor may be required to decouple IREF to VAA or VCC.

VIDEO INTERFACE: The Red, Green and Blue video outputs are designed to drive doubly terminated 75 ohm lines. To minimize ringing due to impedance mismatch, 75 ohm +/- 1% thin film resistors should be placed close to the AT76C176A on the PC board.

To comply with FCC RF emission regulations, ferrite beads can be inserted at the video outputs to limit the amount of high frequency emission. The AT76C176A is designed to produce very little high frequency digital feedthrough.

SYSTEM TIMING: The pixel clock, PCLK, controls the timing of the Color Palette and the Video DACs. To obtain the highest quality display possible with the AT76C176A, Setup and Hold time requirements with respect to PCLK should be strictly adhered to. The duty cycle limits of PCLK should also be met over the entire display.

DIGITAL INTERFACE: When the high impedance digital inputs of the CMOS AT76C176A are driven by low impedance sources, considerable ringing can occur, which may degrade high video rate operation. Impedance matching resistors of the order of 50 ohms can be inserted in series at the inputs to the Pixel Address and Blanking inputs to reduce ringing. This also minimizes the amount of high frequency emission due to excessively high slew rates at the video data inputs.

D.C. and A.C. Operating Range

		AT76C176A-110	AT76C176A-80	AT76C176A-66 AT76C176A-50	VCC/VAA Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C			5V +/- 5%
			0° C - 70° C	0° C - 70° C	5V +/- 10%
	Ind.		-40° C - 85° C	-40° C - 85° C	5V +/- 10%
	Mil.			-55° C -125° C	5V +/- 5%

D.C. Characteristics

Symbol	Parameter	Conditions	All Min	50MHz Max	66MHz Max	80MHz Max	110MHz Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+0.1V		10	10	10	10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC} + 0.1V		10	10	10	10	µA
I_{CC}	Power Supply Current	IO=21mA, $\overline{PDN}$ = V_{IH} Digital Outputs Open		150	170	190	220	mA
I_{SB}	Standby Supply Current	$\overline{PDN}$=V_{IL} PCLK=0Hz			100	100	100	µA
I_{ILP}	Current Sourced by Pin $\overline{PDN}$	$\overline{PDN}$=V_{IL}			20	20	20	µA
I_{REF}	Reference Current		-7	-10	-10	-10	-10	mA
V_{IL}	Input Low Voltage		-0.5	0.8	0.8	0.8	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	IO=5mA		0.4	0.4	0.4	0.4	V
V_{OH}	Output High Voltage	IO=-5mA	2.4					V
V_{REF}	Voltage at IREF Input		V_{CC}-3	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V

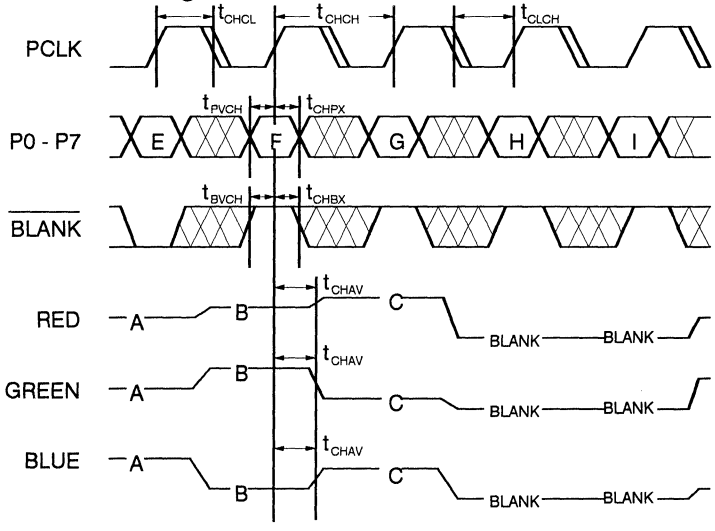
Video DAC Characteristics

Symbol	Parameter	Conditions	All Min	All Typ	50MHz Max	66MHz Max	80MHz Max	110MHz Max	Units
RES	Resolution		6						Bits
ILE	Integral Linearity Error	Note A			±0.5	±0.5	±0.5	±0.5	LSB
COR	DAC to DAC Correlation	Note B			±2	±2	±2	±2	%
FSE	Full Scale Error	Note C			±5	±5	±5	±5	%
DVT	Glitch Energy	Notes D, E		75					pVsec
IO	Output Current	VO<1V		18.6	21	21	21	21	mA
VO	Output Voltage	IO<21mA		0.7	1.5	1.5	1.5	1.5	V
t_{DR}	Rise Time (10% to 90%)	Notes D, E			8	6	6	5	ns
t_{DF}	Full Scale Settling Time	Notes D, E, F			20	15	12.5	9	ns

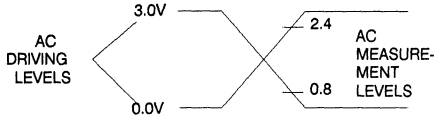
Video Timing Characteristics

Symbol	Parameter	Conditions	All Max	50MHz Min	66MHz Min	80MHz Min	110MHz Min	Units
t_{CHCH}	PCLK Period (τ)	Normal	10000	20	15	12.5	9	ns
		Standby		35	25	20	20	ns
Δt_{CHCH}	PCLK Jitter	$t_{CHCH} = \tau$	±2.5					%
t_{CLCH}	PCLK Low Width	Normal	10000	6	5	5	4	ns
		Satndby		12	9	7	7	ns
t_{CHCL}	PCLK High Width	Normal	10000	6	5	5	4	ns
		Standby		12	9	7	7	ns
t_{PVCH}	Pixel Word Setup Time			4	3	3	3	ns
t_{CHPX}	Pixel Word Hold Time			4	3	3	2	ns
t_{BVCH}	$\overline{BLANK}$ Setup Time			4	3	3	3	ns
t_{CHBX}	$\overline{BLANK}$ Hold Time			4	3	3	2	ns
t_{CHAV}	PCLK to DAC Output Valid	Note G	30	5	5	5	5	ns
Δt_{CHAV}	Differential Output Delay	Note H	2					ns
t_{CC}	Pixel Clock Transition Time		50					ns

Video Timing Waveforms Diagram

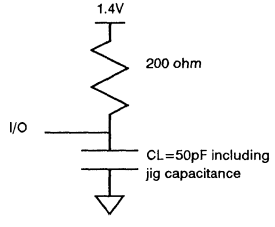


Input Test Waveforms



Notes: 1. t_R, t_F <3 ns (10% to 90%).
2. Input timing reference is at 1.5V.

Digital Input/Output Load



MPU Interface Timing Characteristics

Symbol	Parameter	Conditions	All Max	66/50MHz Min	80MHz Min	110MHz Min	Units
t_{WLWH}	$\overline{WR}$ Pulse Width Low			50	50	50	ns
t_{RLRH}	$\overline{RD}$ Pulse Width Low			50	50	50	ns
t_{SVWL}	Register Select Setup Time	WRITE Operations		10	10	10	ns
t_{SVRL}	Register Select Setup Time	READ Operations		10	10	10	ns
t_{WLSX}	Register Select Hold Time	WRITE Operations		10	10	10	ns
t_{RLSX}	Register Select Hold Time	READ Operations		10	10	10	ns
t_{DVWH}	Write Data Setup Time			10	10	10	ns
t_{WHDX}	Write Data Hold Time			10	10	10	ns
t_{RLQX}	Output Turn-on Delay			5	5	5	ns
t_{RLQV}	Read Enable Access Time		40				ns
t_{RHQX}	Output Hold Time			5	5	5	ns
t_{RHQZ}	Output Turn-off Delay	Note I	20				ns
t_{WHWL1}	Successive Write Interval	τ = PCLK Period		4τ	4τ	4τ	ns
t_{WHRL1}	Write Followed by Read Interval	τ = PCLK Period		4τ	4τ	4τ	ns
t_{RHRL1}	Successive Read Interval	τ = PCLK Period		4τ	4τ	4τ	ns
t_{RHWL1}	Read Followed by Write Interval	τ = PCLK Period		4τ	4τ	4τ	ns
t_{WHWL2}	Write After Color Write	τ = PCLK Period		4τ	4τ	4τ	ns
t_{WHRL2}	Read After Color Write	τ = PCLK Period		4τ	4τ	4τ	ns
t_{RHRL2}	Read After Color Read	τ = PCLK Period		7τ	7τ	7τ	ns
t_{RHWL2}	Write After Color Read	τ = PCLK Period		7τ	7τ	7τ	ns
t_{WHRL3}	Read After Read Address Write	τ = PCLK Period		7τ	7τ	7τ	ns
t_{WREN}	Read/Write Enable Transition Time		50				ns

Notes

Note A: Measured from best fit line through DAC transfer curve.

Note B: Measured from the mid point of the distribution of the three DAC transfer curves.

Note C: $FSE=\left[\frac{VO-2.1\times IREF\times R_{Load}}{2.1\times IREF\times R_{Load}}\right]\times 100\%$

Note D: Z_{Load}=37.5 ohm + 30pF, IREF=-8.88mA

Note E: This parameter is sampled and not 100% tested.

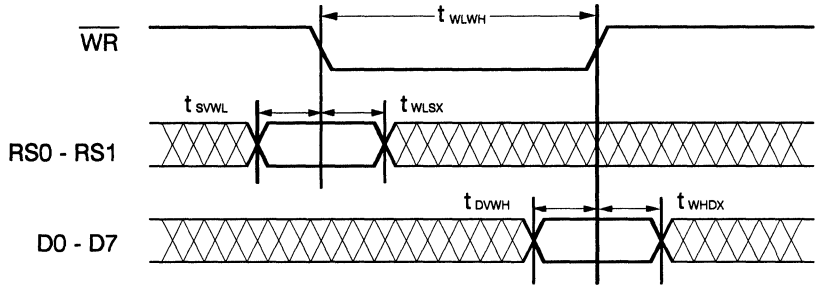
Note F: Measured from a 2% change in the DAC output voltage to within 2% of the final value.

Note G: Measured between the 50% point of the rising edge of PCLK and at the analog output half way between successive output values.

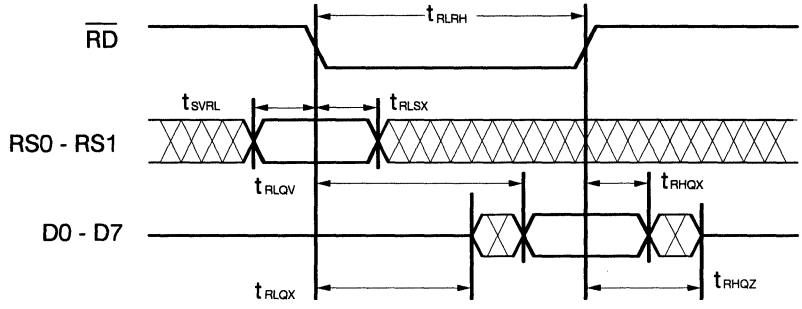
Note H: Measured between different analog outputs on the same device.

Note I: Measured at ±200mV from steady state output values.

Write Operations Waveforms

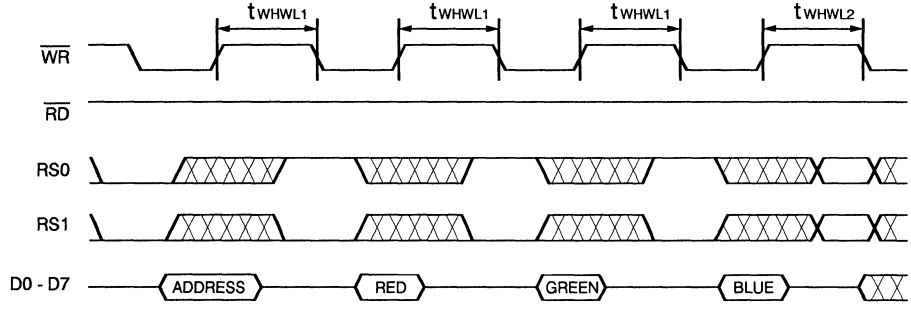


Read Operations Waveforms

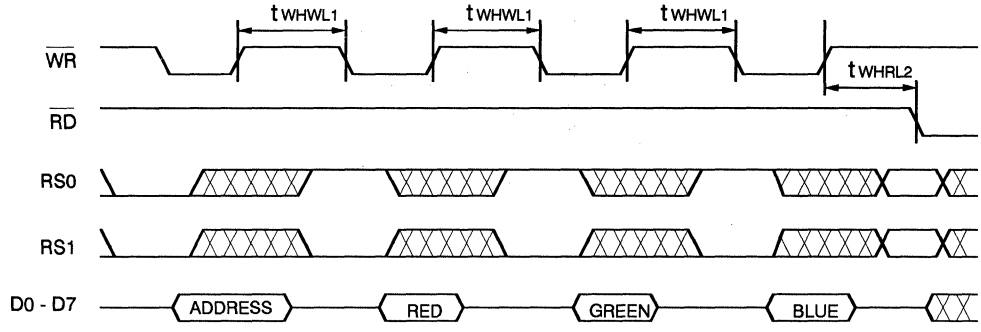


9

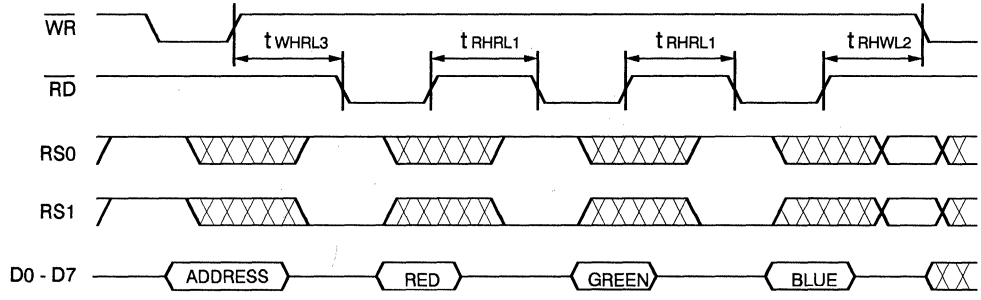
A.C. Waveforms for Color Value Write Followed by Any Write



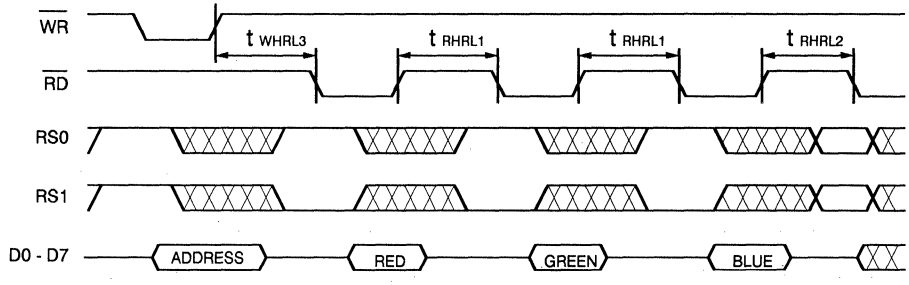
A.C. Waveforms for Color Value Write Followed by Any Read



A.C. Waveforms for Color Value Read Followed by Any Write

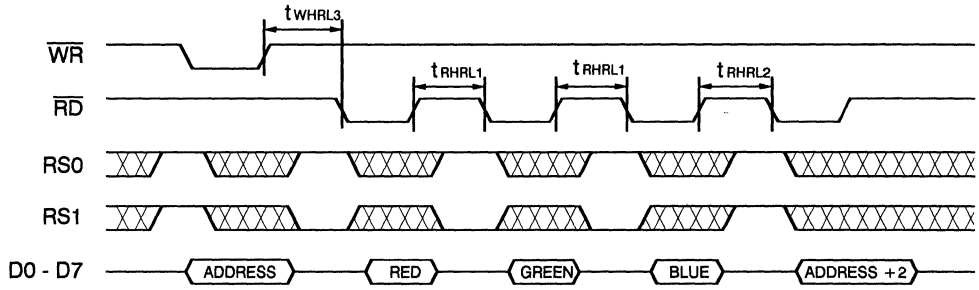


A.C. Waveforms for Color Value Read Followed by Any Read

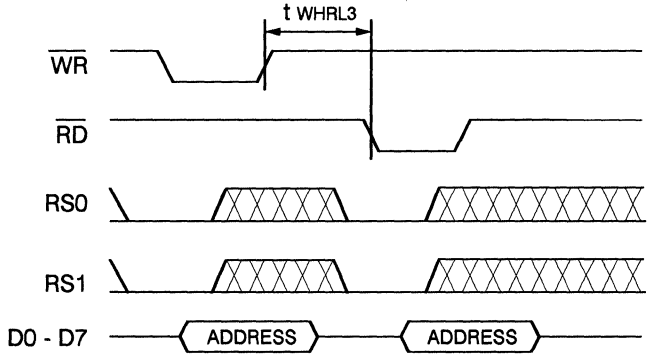


A.C. Waveforms for Color Value Read

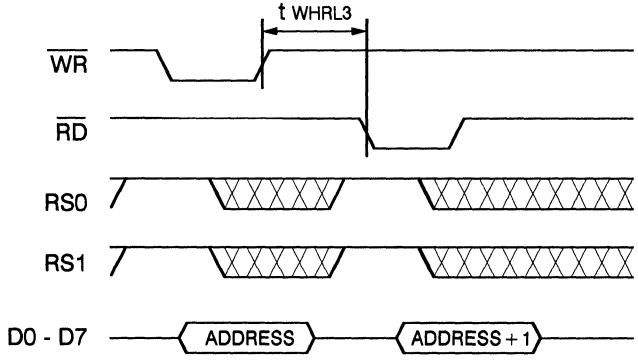
Followed by Pixel Address (Read Mode) Read



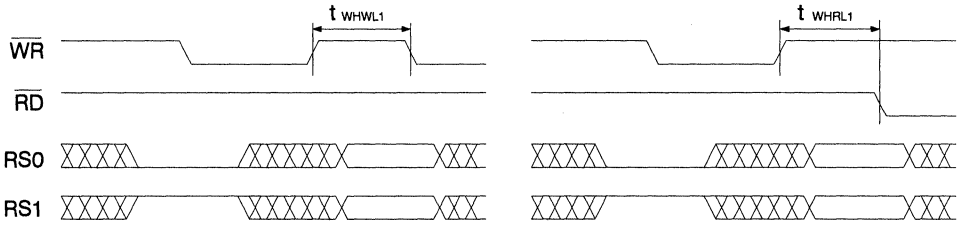
A.C. Waveforms for Pixel Address (Write Mode) Write and Read Back



A.C. Waveforms for Pixel Address (Read Mode) Write and Read Back

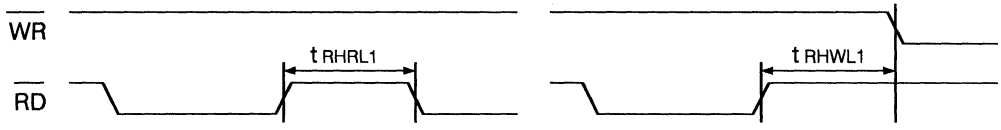


A.C Waveforms for Pixel Mask Write Followed by Any Write or Read



A.C. Waveforms for Pixel Mask or Pixel Address Read

Followed by Any Read or Write



Ordering Information

Speed (MH_z)	Power Supply	Ordering Code	Package	Operation Range
50	±10%	AT76C176A-50PC AT76C176A1-50JC AT76C176A2-50JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-50PI AT76C176A1-50JI AT76C176A2-50JI	28P6 32J 44J	Industrial (-40°C to 85°C)
50	±5%	AT76C176A-50DM	28D6	Military (-55°C to 125°C)
66	±10%	AT76C176A-66PC AT76C176A1-66JC AT76C176A2-66JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-66PI AT76C176A1-66JI AT76C176A2-66JI	28P6 32J 44J	Industrial (-40°C to 85°C)
66	±5%	AT76C176A-66DM	28D6	Military (-55°C to 125°C)
80	±10%	AT76C176A-80PC AT76C176A1-80JC AT76C176A2-80JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-80PI AT76C176A1-80JI AT76C176A2-80JI	28P6 32J 44J	Industrial (-40°C to 85°C)
110	±5%	AT76C176A-110PC AT76C176A1-110JC AT76C176A2-110JC	28P6 32J 44J	Commercial (0°C to 70°C)

9

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Section 10

Application Notes

Using Atmel's CMOS E²PROMs

E²PROMs offer many features desired for present day memory systems. They are non-volatile, preserving data for years whether or not power is applied. They provide high density memory storage, with 1 megabit devices now available. They offer high speed reads and can be re-written on a byte or page basis.

Five volt only signals are used to operate the devices. When writing new data only the data bytes that are desired to be changed need be rewritten. No erasure steps are required before rewriting any memory location. Since all of Atmel's products are made with CMOS technology, the supply current required to operate Atmel E²PROMs is low. Other features such as $\overline{\text{DATA}}$ polling, internal error correction and software data protection, make Atmel E²PROMs the correct solution for many memory systems.

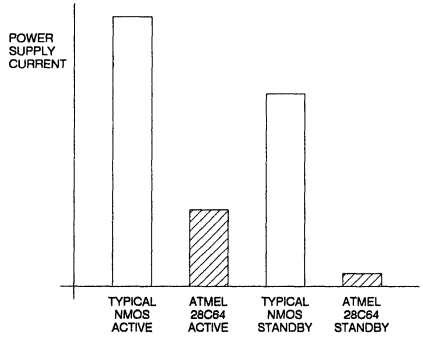
CMOS Versus NMOS E²PROMS

CMOS is quickly becoming the dominant MOS technology. Many systems however, have been designed without the use of CMOS products, and therefore do not have the benefits of this advanced process technology. The most obvious advantage of CMOS is in the power savings. Figure 1 shows a comparison of a typical 64K NMOS E²PROM current specification versus that of Atmel's AT28C64. The power advantage of CMOS is quite clear. The power savings actually does more than just reduce the drain on the power supply. The low power consumption helps to keep system temperatures lower, reducing the need for cooling and allowing for greater packing density on boards. With less internally generated heat, CMOS products can be more reliable than their NMOS counterparts.

The TTL and CMOS compatible inputs and outputs of Atmel's CMOS E²PROMs offer additional advantages. The input stages consume no active power when the input voltage is at ground or the positive supply level. Figure 2 shows the typical power consumption curve for an Atmel input stage versus input voltage. By using full CMOS input levels to the device, the active power consumption can be reduced below the specified levels.

The outputs of Atmel E²PROMs drive to the full limits of the supply voltage. When driving other CMOS input stages, this full

Figure 1. Comparison of typical NMOS 64K E²PROM current consumption to that of Atmel's AT28C64.



swing drive capability can actually reduce the power consumed by other devices within the system! Also, by driving to the high power supply limit, Atmel devices improve the noise margin of the high input level of the device they are driving as compared to typical NMOS devices which do not drive to the high supply level (see Figure 3).

Upgrading from NMOS to CMOS

It is generally quite easy to upgrade a system using NMOS devices to use CMOS parts. In most cases, NMOS E^2PROM devices organized from 512 by 8 to 32k by 8 may be directly replaced by an Atmel CMOS device of the same density and pinout. No hardware nor software changes need necessarily be made when upgrading the system.

In some cases, power switching transistors have been used to power down NMOS E^2PROMs while the rest of the system remains active. In such a state, the DATA lines of the NMOS E^2PROM do not load the DATA bus of the system. A CMOS device in such a configuration may show substantial input current through the DATA pins if the DATA bus is higher than the E^2PROM's power supply input. To permit CMOS devices to work properly in such a system, it is recommended that the switching transistor be removed from the power supply of the E^2PROM. With the low power standby mode of Atmel'S E^2PROMs, the power switching is not necessary. The low power consumption of the CMOS device will not adversely affect the system power consumption and there will be negligible input leakage at the E^2PROM DATA pins. Additionally, the power consumption of the E^2PROM will be much lower when selected and, with the removal of the switching transistor, the number of devices in the system will be reduced.

Figure 2. Typical power consumption curve for Atmel input stage versus input level.

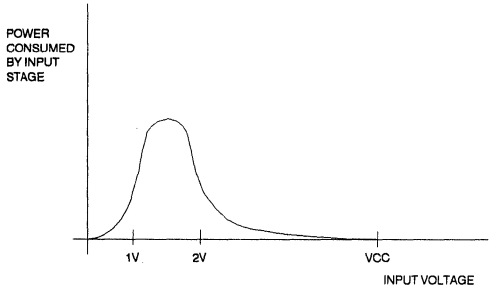
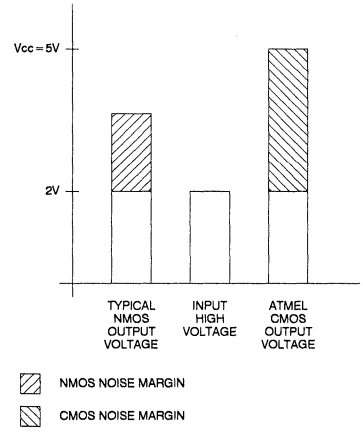


Figure 3. High input voltage noise margin comparison of typical NMOS output to Atmel CMOS output.



Read Cycle

The E^2PROM read cycle is controlled by the $\overline{CE}$ and $\overline{OE}$ signals. When $\overline{CE}$ and $\overline{OE}$ are both low, data is read from the device. The address inputs specify the memory location being read. The address and data lines are not latched during a read cycle; changing the address while $\overline{CE}$ and $\overline{OE}$ are low will result in the output of the device changing. If $\overline{CE}$ or $\overline{OE}$ is high, the outputs are put in a high impedance state. This dual line control allows for flexibility in avoiding buss line contention. There is no need for periodic refresh of the memory; E^2PROMs retain their data whether or not power is applied. Addresses may be randomly selected; there are no restrictions on address lines.

When $\overline{CE}$ is high, the internal power consumption of the device is greatly reduced; the device is said to be in the standby mode. The power reduction is achieved by turning off the internal circuits of the device. When $\overline{CE}$ is returned low, the internal circuits are again powered on and a new read is performed.

Atmel E^2PROMs are designed to provide the fastest access times available among like devices. They therefore may have large transient current requirements. It is recommended that each device be carefully decoupled. A decoupling capacitor across the power and ground line as close to the device as possible should be used. As with any high performance device, the integrity of the power and input signals can affect its operation in the system. Maintaining clean power and input signals will ensure the best performance of the device.

Byte Write Cycle

Writing to Atmel E²PROMs has been designed to minimize the time that the system must spend in issuing commands to the memory device. The write cycle is controlled by $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$. Initiating a write cycle is done with a short pulse on either the $\overline{WE}$ or $\overline{CE}$ input. With $\overline{OE}$ high and $\overline{CE}$ (or $\overline{WE}$) low, the address to be written is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$, whichever occurred last). The data to be written is latched on the rising edge of $\overline{WE}$ (or $\overline{CE}$, whichever occurred first). The latching of the address and data inputs allows the address and data busses to be used to access other devices while the write is in progress. During its write cycle, data may not be read from the E²PROM (the device may however be polled to see if the write is completed).

Internal to the E²PROM device, the write cycle can be divided into two steps. The first is to load the data into a temporary buffer; this operation can be done very quickly (measured in nanoseconds). The second step is to perform the non-volatile storage. It takes considerably longer for this step (up to several milliseconds). After the non-volatile storage is completed, a new read or write cycle may begin immediately.

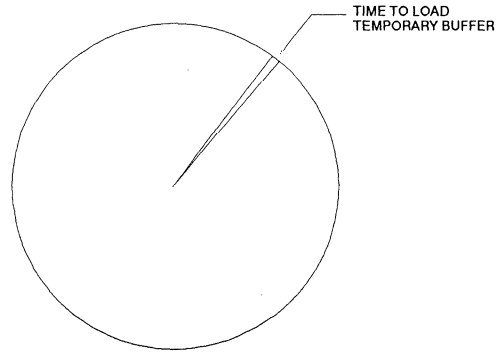
Page Write Cycle

To improve the effective write time when large sections of the memory are being rewritten, some Atmel E²PROMs provide a page write operation. The page write allows a group of bytes to be quickly loaded into the device's temporary buffer and then simultaneously written to the non-volatile storage elements. Figure 4 is a pie chart showing the time needed for completely loading the temporary 64 byte page buffer of the AT28C256 as a portion of the write cycle time. Clearly, by utilizing the page write with minimum write load times, the write time can effectively be reduced by a factor approximately equal to the page width.

Similar to the writing of a single byte, address location and data to be written are latched on the falling and rising edges of $\overline{WE}$ or $\overline{CE}$. All bytes being written must have the same page address. The page address is determined by the higher order addresses and is specified in the data sheet of each particular device. The page address must be valid during each high to low transition of $\overline{WE}$ or $\overline{CE}$. The $\overline{OE}$ input must be high whenever $\overline{CE}$ and $\overline{WE}$ are low.

During write cycles, only the bytes that are specified to be written are altered; other bytes within the device are not rewritten or otherwise affected. A write cycle will only occur when requested; however, there may be conditions present during such times as power-up or power-down when a system might inadvertently initiate a write cycle. Atmel devices include many features to help prevent inadvertent write cycles. Users of E²PROMs should become familiar with these features.

Figure 4. Time to load 64 bytes to temporary buffer in AT28C256 as a portion of the write cycle time.



Additional Features

Atmel E²PROMs include other features to help ensure reliability and to improve overall system performance. The internal error correction incorporated into Atmel's E²PROMs protects against single bit data errors from appearing in the devices. The user does nothing to utilize the feature; whenever a write or read cycle is performed, parity generation or checking occurs internally to the E²PROM device to help ensure the integrity of the data.

The inputs and outputs of Atmel devices contain circuitry to protect the device from electrostatic damage. Even though the devices do have this protection circuitry, it is strongly recommended that safe handling procedures be used with these devices. All equipment and personnel that may come in contact with the devices should be well grounded. Other features such as $\overline{DATA}$ polling, READY/$\overline{BUSY}$ outputs or toggle bit are available and may be employed by users as required by their particular application.

E²PROM Data Protection

Advantages of E²PROMs

E²PROMs provide the memory solution wherever reprogrammable, non-volatile memory is required. They are easy to use, requiring little or no support hardware such as refresh clocks or batteries. Each memory location can be selectively changed without impact on any other location; blanket erasure and rewriting of the entire device or a large section of it is not required.

E²PROMs made at Atmel were designed to provide the best features available. Atmel E²PROMs provide high speed read access times so that many applications can use them without inserting costly wait states. The page mode write operation of Atmel E²PROMs allows for the fastest effective write time available in E²PROM memories. Since all of Atmel's devices are made in CMOS, they offer the benefits of low operating and standby power.

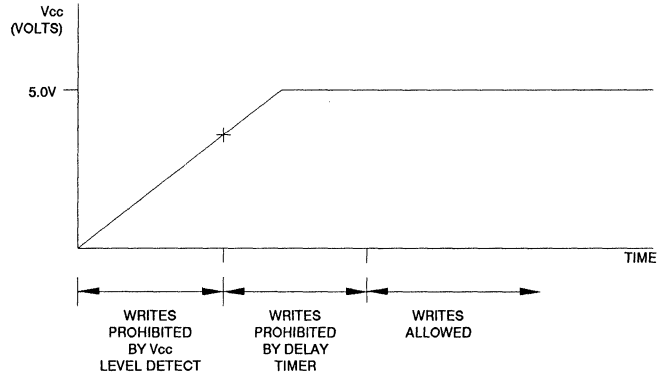
In order to take advantage of all of the benefits of Atmel E²PROMs, care must be taken to maintain the integrity of the data. While an E²PROM will retain its data for many years with or without power applied, improper operation of the device could result in data being inadvertently rewritten.

When is Data Susceptible to Corruption

In the use of any memory device, it is expected that the data stored in it is available as it is written. This is especially true of E²PROMs since their code often controls the operation of the system in which they are contained. Unlike most other memory types that are rewritten in systems, E²PROMs are often expected to retain their data for a period of many years, with or without power applied and during power transitions. For these reasons, added attention is given to avoid corrupting data in E²PROMs.

There are a number of situations in which data is particularly prone to corruption. These situations include powering on and off of the devices, noise spikes on the control lines and system glitches. Atmel E²PROMs include features to help protect against each of these potential

Figure 1.



CMOS E²PROM

Application Note

10

sources of inadvertent writes. Atmel data protection features are broken down into two different types: hardware data protection features and software data protection features.

Atmel Hardware Data Protection Features

Atmel E^2PROMs include four different types of hardware data protection. These features provide protection against most inadvertent writes that might occur in a system. Atmel hardware data protection features include: three line write control, power level sense detector, power on delay timer and noise filters on $\overline{CE}$ and $\overline{WE}$.

Three Line Write Control: In order to write a device the $\overline{OE}$ signal must be high with the $\overline{CE}$ and $\overline{WE}$ signals low. Holding any of the three lines in the opposite state will prohibit a write cycle. For example, whenever the $\overline{OE}$ signal is low, a write to the device cannot be started.

Power Level Sense Detector: An active circuit in Atmel E^2PROMs monitors the level of the supply voltage to the device. If the supply is below 3.8 volts, typical, write cycles to the devices can not be activated.

Power On Delay Timer: As power is applied to Atmel E^2PROMs, the power level sense detector will issue an internal signal that indicates that the supply is above the sense level. At this time an internal timer is initiated that times out in typically 5ms. During this time period, writes to the device cannot be performed. This delay period serves two purposes. First, it allows the supply level additional time to rise to within the standard operating region before writes are permitted. Secondly, it lets the system stabilize and present the correct levels to the control pins of the E^2PROM so that the E^2PROM doesn't react to its inputs before they are actually valid. Figure 1 shows the combined action of the power supply level detector and the delay timer upon writes to the device.

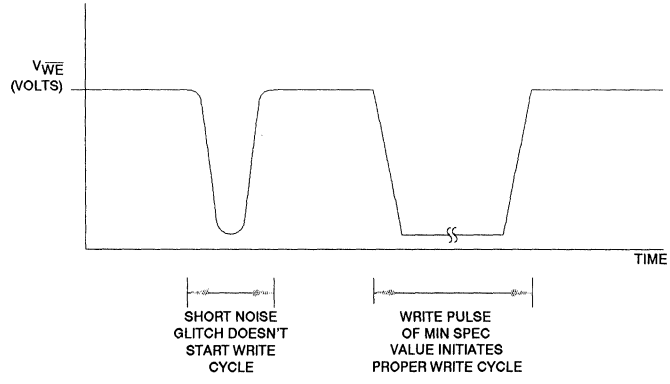
Noise Filters on $\overline{WE}$ and $\overline{CE}$: If brief noise pulses below V_{IH} occur on the $\overline{WE}$ or $\overline{CE}$ inputs to the device, a write cycle will not be initiated. Internal to the E^2PROM, a noise filter does not allow the short pulses to activate a write cycle. As shown in Figure 2, write pulses of sufficient length will still initiate writes but short noise spikes on the $\overline{WE}$ or $\overline{CE}$ control lines will not.

Atmel Software Data Protection Feature

Available on some Atmel E^2PROMs is a user selectable feature that requires a software sequence at the beginning of each write cycle in order for a write to be performed. To enable the software data protection feature, a series of three write commands to specific addresses with specific data must be performed. Once set, the same three byte code must begin each write request. (A separate write cycle to enable the software feature is not necessary; after any write that is preceded with the three byte code, the software data protection function will be enabled, see Figure 3.) The feature may be disabled by issuing a six byte code to the device as shown in Figure 4. After being set, the software data protection feature remains active until its disable command is issued. Power transitions will not reset the software data protection feature, but the feature will prevent against inadvertent writes during power transitions.

The software data protection feature protects data against various causes of inadvertent writes. Since it is active during power transitions it protects data when powering on or off the device. Noise spikes that occur on the control lines will be ignored since they will not show the correct address and data

Figure 2.



needed to start a write cycle. Even for system malfunctions, such as when write pulses of adequate length are given to the device, the software feature can prevent the corruption of the data in the E²PROM. The address locations used for the software code are not sacrificed from the usable memory array. The device recognizes the software code and does not alter the data stored at the address locations of the code. Byte locations of code are still usable, and don't have to be rewritten.

System Design Considerations

Designing systems with data integrity in mind can greatly reduce the chance of lost data. The amount of attention needed depends upon the nature of the design. Following are a few areas that might need special attention in certain designs.

External Power On Protection

Many systems will have a PON (power on) signal to control the operation of the system. Such a signal can be gated with the logic creating the $\overline{OE}$ signal to the E²PROM, holding $\overline{OE}$ low when the PON signal is false. Similarly, a PON type signal could be gated with the $\overline{WE}$ or $\overline{CE}$ logic, forcing $\overline{WE}$ or $\overline{CE}$ high when writes should not be allowed.

If the system does not include a PON type signal, one can be created from various programmable voltage reference devices. With such a device, the user can select the voltage supply level below which the device cannot be written. It should be noted that in many systems, using Atmel's E²PROMS with their internal power level detection and power delay timer, no additional power on circuitry is required for the device.

Multiple Power Supplies

In systems that utilize more than one power supply, extra care must be taken during power transitions to both the E²PROM and the devices controlling the inputs to the E²PROM. Power on rates of the different supplies are likely to vary. Using programmable voltage reference devices to detect the power level of both supplies and forcing the $\overline{OE}$ pin low when either line is below the desired level may be used in such situations to avoid inadvertent writes.

Memory Cards

Since memory cards are often pushed into and pulled out of systems that are already powered on, they have additional chances of inadvertent writes. If the edge connector is arranged such that power and control lines are not asserted in a prescribed manner, false writes to the device may occasionally occur depending upon how the card is inserted. To provide proper power on sequencing, a card could be designed with its control pins recessed from the edge of the card. Resisters would be placed on the card to connect $\overline{CE}$ and $\overline{WE}$ to V_{CC} and $\overline{OE}$ to ground. This arrangement insures that power is first applied to the device and that the control pins are not in the write state until each pin is being controlled by the host system. Variations of this technique may be used effectively in different systems; the basic idea is to guarantee systematic application of the power and control pins such that a write state is not entered upon insertion or removal of the card from the host.

Figure 3.

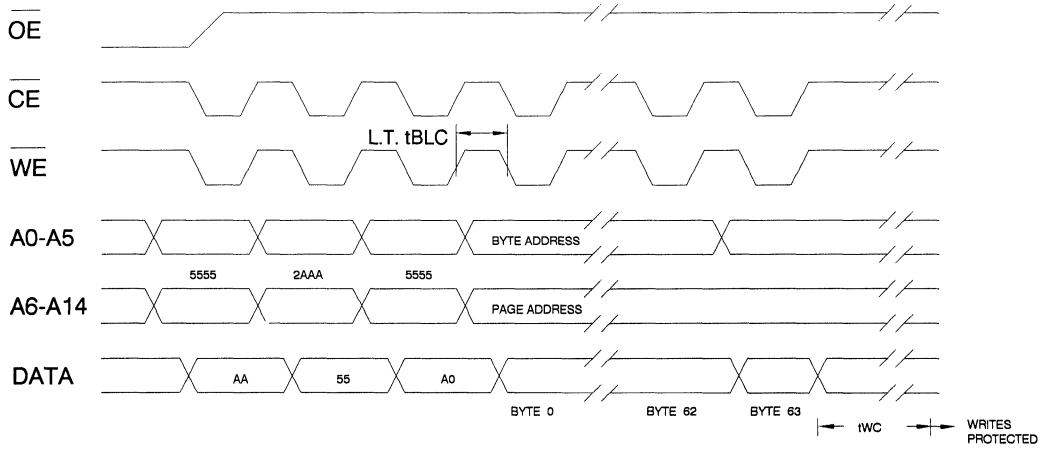
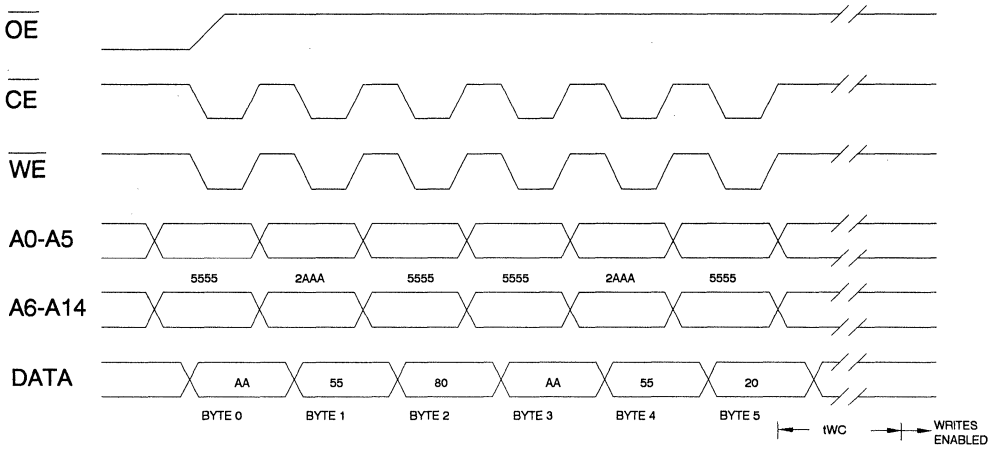


Figure 4.


OE
CE
WE
A0-A5
5555
2AAA
5555
5555
2AAA
5555
A6-A14
DATA
AA
55
80
AA
55
20
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
tWC
WRITES ENABLED

Programming Socket Adapter

As the market for non-volatile memory parts in surface mount packages increases, so does the interest in simple, low cost programming socket adapters. These adapters allow users of standard programming equipment to program any package type including LCC (leadless), SOIC (Gull-wing), PLCC (J-Lead), and flat-pack. The adapter plugs into the programmer in place of a 600mil or 300mil DIP package of the same part. The surface mount part to be programmed then plugs into the socket on the adapter.

The two major disadvantages of building a socket adapter are:

- Little or no support from programmer manufacturers.
- Prolonged use of socket adapters using wire-wrap pins is not recommended due to spring tension loss damage of the programmer's zero insertion force sockets. That may degrade the reliability of the programmer when the adapter is not used.

Table 1. Piece-Part Descriptions (see Figure 1)

Item No.	Qty.	Description
(1)	1	Zero insertion force socket.
(2)	2	Wire wrap strips with 100mils pin centers and about 500 mils long on the end which will plug into the programmer's socket and 200 mils long on the opposite end to attach to (5) below.
(3)	2	Wire wrap strips similar to (2) above except only 100 mils and 200 mils long to connect (4) and (5) below.
(4)	1	PC board to accept the socket (1) and run traces to the edge of the card connecting to (3).
(5)	1	PC board to run traces from the card edge (3) to the two strips (2) (usually seperated by 600 mils).
(6)	20"	#16-18 insulated stranded copper wire.
(7)	1-2	0.1μF ceramic high-frequency decoupling capacitors.
(8)	1	(Recommended) Pin socket board to fit between (1) and (4) to allow easy replacement of the socket (1). (8) is soldered to (4) and (1) plugs into (8). Zero insertion force sockets wear out quickly so replaceability is a good feature to have.

The advantages are more obvious. Some manufacturers charge up to $500 for an adapter which slides or plugs into the programmer compared to about $100 for the hardware described here.

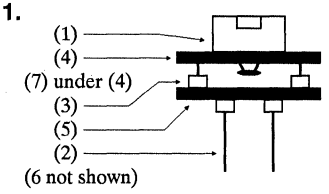
Assembly of a custom programming adapter is very simple. Table 1 describes the typical piece parts needed. Table 2 lists sockets and piece-part sources for different package configurations. The finished adapter is about 2 inches square and 1.5 inches high.

As listed in Table 2, Emulation Technology, Inc., (408) 982-0660, can supply the adapter sockets preassembled, but we recommend you order the parts as an UNSOLDERED KIT to facilitate attaching the decoupling capacitors. The additional wire shunts (not required if a -LN kit is ordered from ET) and capacitors are essential to reduce inductive noise effects during programming and to maintain adequate programming yield. It is necessary to "beef-up" all the power (V_{CC}, V_{PP}) and ground (Gnd) connections by adding short jumpers of wire (6) running from the socket (1), around the edge of the module and finally to the pins of item (2) on the bottom of the module. Bypass capacitors (7) must be soldered between Gnd and V_{CC} or V_{PP} (if applicable). The leads on the capacitors must be trimmed as short as possible and soldered as close to the socket (1) as possible (on the wide traces on the -LN board (4)). The other end of each capacitator will be connected to short stranded wires (6) running from the top, around the edge of the adapter, and finally soldered to the ground pin of item (2).

Assembly proceeds as follows (see Figure 1 and note that jumper wires (6) are not required if a -LN kit is used):

1) Trim the leads on the jumper wires (6) to about 3.0 inches. Solder capacitors (7) with shrink-wrap insulation on the cap leads, and jumper wires (6) under the socket (1) (or under (8) if socket replaceability is needed) in such a way that they do not interfere with attaching the socket (or (8)) to the board (4). (If a -LN kit is used, just solder the capacitators on the wide traces provided on board (4).)
2) Solder the socket (or item (8)) to the PC board (4) and trim the pins on the socket flush to the board (4).
3) Solder the shorter pin strips (3) to the outside of board (4) with the spacers on the side away from the socket (1).
4) Solder the longer pin strips (2) into the other PC board (5) such that the spacers stick out of the bottom of the adapter. These longer pins will be used to plug directly into the programmer socket. Trim the shorter leads of (2) flush with the board (5) after soldering.
5) Solder the PC board (5) to the short pins protruding below PC board (4).
6) (Omit this step if a -LN kit is used.) Connect all the V_{CC}, V_{PP} (if applicable) and Gnd wires which were connected in step (1) to their appropriate pins on item (2) on the underside of the assembly close to the protruding spacer in such a way that they will not interfere with plugging the completed module into the programmer DIP socket. Trim these shunt wires as short as possible to minimize inductance effects.

Figure 1.



This application note has described how to build a simple and cheap programming adapter socket to support a wide variety of non-volatile memory product packages available from Atmel.

Table 2. Vendors / Part Numbers By Package Type

Package Type	Pin Count	Emulation Technology[1]	Socket Manufacturer	Part No.
LCC	28	AS-28-28-01-L6-LN	Textool[2,3]	228-4960
	32	AS-32-28-01-P6-LN	Yamaichi	IC51-0324-453
	32 (27C010)	AG-32-32-01-L6-LOW	Textool	232-5427
	44	AS-44-40-08-L6-LN	Textool	244-5292
	32 (27C010)	AG-32-32-01-P6-LOW	Textool	232-6917
PLCC	32	AS-32-28-01P-P6-LN	Yamaichi	IC51-0324-453
	44	AS-44-40-08-P6-LN	Textool	244-5292
SOIC	28	Call ET	Yamaichi[4]	IC51-0282-334-1

Notes: 1. ET can also supply finished adapter sockets built per this application note or other customer requirements.
2. Made by 3M. Check with your local distributor.
3. Windowed LCC packages (ie, EPROM's) require removal of the circular bumper in the Textool socket lid which snaps apart. Non-windowed packages (ie, E^2PROM's, OTP's) do not require any socket adjustment.
4. See Atmel SOIC Package and Programming Socket Modification Application Note before building the SOIC adapter.

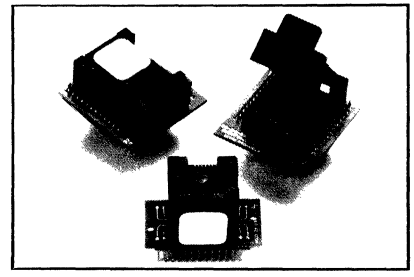
Figure 2.

LCC / PLCC / SOIC to DIP Adapter

ADAPT-A-SOCKET®

LCC / PLCC / SOIC to DIP

Prices from $67.00 to $148.00



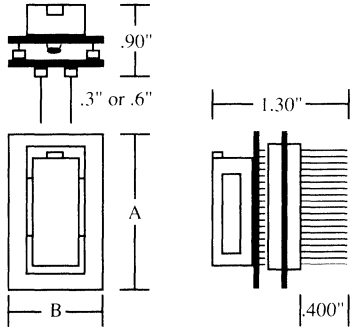
- For programming PROMS, PLDS, EPROMS, EEPROMS, PALS†
- Production ATE testing
- Test points provided for each signal
- Decoupling capacitors can be added.
- Available for LCC, PLCC and SOIC.
- Natural for prototype processing.
- Sturdy base contact pins.
- Saves development $$$.

† PAL is a registered trademark of Monolithic Memories, Inc.

When Your Equipment is Designed for DIPs

ADAPT-A-SOCKET converts your Dual-In-Line (DIP) sockets to ceramic Leadless Chip Carrier (LCC), Plastic Leaded Chip Carrier (PLCC) and Small Outline Integrated Circuits (SOIC) sockets in just seconds. Without having to purchase expensive equipment. Just plug ADAPT-A-SOCKET into your programmer socket, burn-in board or test head and you're ready to go.

Call Factory for *Cross Reference Guide*



Number of Top Pins	A	B
16	1.60 Max	1.45
20	"	"
24	"	"
28	"	"
32	1.65	1.60
32 AG*	1.70	.90
52	2.70	1.80

* AG-32-28-01P-6 is available for gang programmers

Specifications

- **SOCKET** (LCC, PLCC, SOIC, FLAT PACK)
  Body Material ..... Ryton
  Contact Material ..... BeCu
  Contact Plating ..... 30 Microinches of ..... Gold over Nickel
- **PHYSICAL**
  Lids and latches are replaceable.
- **BASE** (DIP, PGA, LCC, PLCC)
  Body Material FR4
  Contact Material ..... BeCU
  Contact Plating ..... 30 Microinches of Gold over Nickel
- **ELECTRICAL**
  Contact Resistance ..... 25 MilliOHMs per Contact MAX.
  Insulation Resistance ..... 20 MegOHMs MIN. @50 VDC
  Capacitance ..... 2.0 Pico-Farads between ..... any pair of isolated contacts
- **TEMPERATURE RATING** ..... -55°C to +125°C

Test Point Specifications

Insulator Material ..... Glass-filled nylon black, UL94V-0
Contact Material ..... Phosphor Bronze
Current Rating ..... 1 Amp
Voltage Rating ..... 300 VRMS
Dielectric Withstanding Voltage ..... 500 VRMS
Insulation Resistance ..... >1,000 MegOHMs
Temperature Rating ..... -55°C to 125°C

® ADAPT-A-SOCKET is registered trademark of Emulation Technology, inc.

Emulation Technology, Inc. • 2368B Walsh Avenue, Bldg. D • Santa Clara, CA 95051 • (408) 982-0660
FAX (408) 982-0664 TLX 981 866

10

Atmel SOIC Package and Programming Socket Modification

Atmel's new "T Style" SOIC package design brings together Japanese SOIC reliability while still maintaining compatibility with American (JEDEC Standard) sockets. This is achieved via a simple machining of the SOIC socket lid described below.

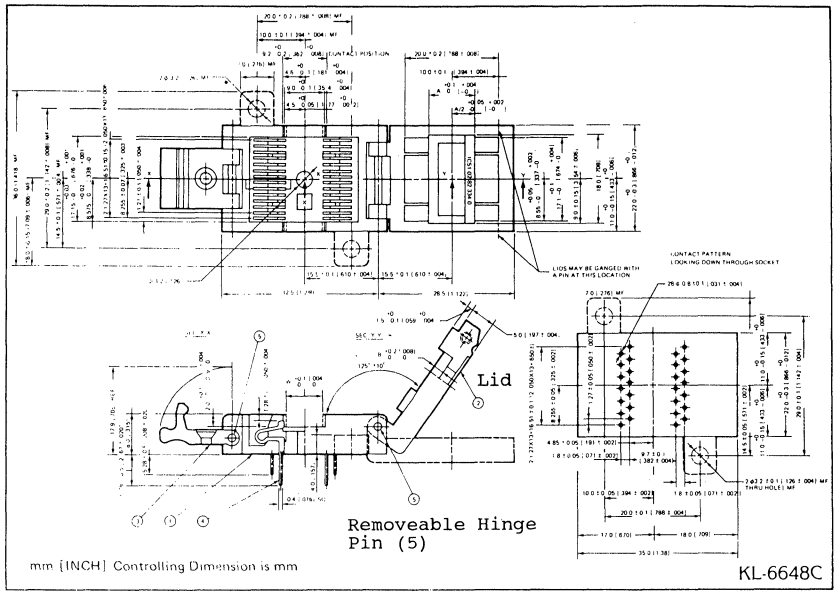
The body width and end-to-end lead length of the Japanese SOIC packages are larger than the American standard. Thus, a Japanese SOIC package will not fit a common American programming socket. However, the American SOIC package design suffers from a smaller lead pad (footprint) which is more susceptible to soldering problems and programming yield loss due to poor electrical contact in a socket.

The Atmel SOIC design uses the Japanese style frame which provides the more desirable wider lead footprint while maintaining the American width package body mold. This combination allows the use of a widely available, high quality programming socket built for American style packages (Yamaichi No. IC51-0282-334-1; see Figure 1). That socket can be simply and inexpensively modified to fit the Atmel SOIC package at any local machine shop.

The procedure to modify the Yamaichi - 334-1 socket lid is as follows: If the socket is already mounted on a board or in a programmer, the lid should be detached from the socket body. This is accomplished by using a No.55 (0.052inch) drill bit as a tool to punch out the hinge pin joining the lid to the body (see Figure1). The lid can then be sent out for machining or used interchangeably with unmodified lids on the same socket body, allowing the user to switch between Atmel and American style SOIC packages using the same programmer. The lid machining instructions are shown in Figure 2 and simply require cutting 0.03 inches from the two inner edges of the two upstanding members on the lid. Those members press the package leads against the pins in the socket body when the fully assembled socket is closed about a package. The lid machining can be easily checked by placing an Atmel SOIC upside-down on the lid as shown in Figure 3. There should be a small amount of play in the package fit to the lid but the package should not be able to slip down into the lid recess. After machining, the lid and socket body are rejoined using the same hinge pin which was removed earlier.

Figure 1. Unmodified Yamaichi SOIC Socket

YAMAICHI IC51-0282-334-1



Body Material: (1)
Polyethersulphone G.F.

Contact Material: (4)
Beryllium Copper

Cover Material: (2)
Polyethersulphone G.F.

Latch Material: (3)
Polyethersulphone G.F.

Shaft Material: (5)
Brass

Contact Plating:
Gold over Nickel

Characteristics:

Insulation Resistance: 1000 M ohms MIN at 500 VDC
Breakdown Voltage: 700 VAC MIN for one minute
Contact Resistance: 30 m ohms MAX at 10mA/20mV
Operating Temperature Range: −55°C ~ +170°C MAX
Typical Life: 10,000 insertions

Ordering Procedure:

IC51 – 028 2 – 334-1 – MF

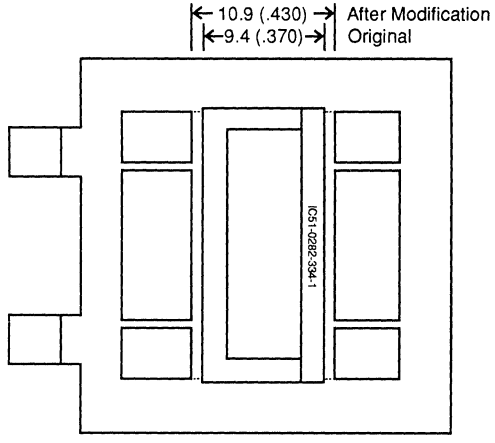
- 028: Socket Series
- 2: No. of Pins
- 334-1: Design No.
- MF: Mounting Flange (Optional)

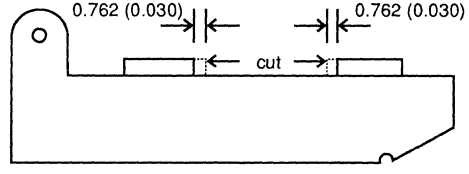
PART NUMBER	W	A	B
IC51-0282-334-1	7.55 [.297]	9.4 [.370]	2.0 [.079]

Figure 1. Unmodified Yamaichi SOIC socket.

NOTE: • Product sample may bear a black anodized aluminum label 3 mil thick. Adhesive is Scotch 467 or 468.

Figure 2.

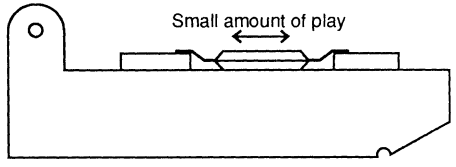




Dimensions in mm (inch)

10

Figure 3.



EPROM Programming with V_{CC}=5V

Present day EPROMs use V_{CC} = 6-6.25V during programming. This non-5V supply level occasionally presents a system design problem with applications where a commercially available programmer cannot be used. This application note will briefly address the issues associated with using a 5V V_{CC} supply during programming.

Modern EPROM programming algorithms can be divided into two sections namely, programming and verify (or read). The programming algorithm usually proceeds by selecting the desired voltage levels and address. A programming pulse is applied followed by a verify at the elevated V_{CC} used for programming.

During programming, the MOS threshold voltage (Vt) of a previously erased N-channel floating gate EPROM cell (Vt = 1.0-2.0V) is raised to 6.5-9.0V via the accumulation of electrons on the floating gate by hot electron injection. In normal read mode operation the address decoding circuitry in the chip selects the desired cell by pulling the gate voltage of the cell to V_{CC}. Since V_{CC} is typically 4.5-5.5V an erased cell with Vt = 1.5V would be turned on while a programmed cell with Vt = 7.5V would remain in an off state. If, V_{CC} were raised above the threshold voltage for the programmed cell (i.e. V_{CC} > 7.5V), the cell would begin to conduct and the programmed data would no longer be valid until V_{CC} was again lowered.

The V_{CC} voltage that causes data loss on a programmed EPROM is called the programming margin. During the programming algorithm the V_{CC} level is held at 6-6.25V to make sure that each cell is guaranteed to have a programming margin at least to that level. This is verified by reading each byte twice, once during the initial programming section and again during a final read where all addresses are compared to the desired data.

The 0.5V difference between the guaranteed programming margin and the 5.5V V_{CC} maximum supply rating provides a reliability guardband for long term data charge retention and, more importantly, for system noise immunity. Poor programming margin can lead to EPROM memory chip instability which can cause apparently slower operation due to oscillations and false reading. This in turn makes the problem directly related to the specific system noise environment and will vary from application to application.

By lowering the V_{CC} voltage to 5.0V during the programming algorithm two effects may occur. First, the part may not be able to program (i.e. programmed cell threshold = 5.0V). Second, the part may not have enough programming margin to reliably work over worst case conditions over the lifetime of the part.

The first problem is rare since most manufacturers design their EPROM technology to provide a large programming margin guardband to account for statistical variations in the manufacturing process.

The second problem is also considerably reduced by the same margin guardband, but unlike the first problem which is easily detectable at the time of programming, the second problem may only occur later when the parts are in the field. The resulting field failure rate may still be acceptably small depending on the application.

The second problem may also result in a failure mode even when the nominal V_{CC} programming voltage is used. In that case standard accelerated reliability tests and statistical sampling techniques can be used to determine failure rates. But such test results only apply to parts with the same programming technique. Since those tests require great expenditure of labor, time, and units, significant reliability data for V_{CC} = 5V programming is not readily available. Another way to get around the possible reliability problem is testing the parts in such a way so as to screen out any

low margin parts. This specially tested group will then have the same programming margin as parts programmed at the nominal V_{CC} even when they are programmed using $V_{CC} = 5V$.

We have discussed general EPROM operation for most currently available EPROM chips on the market today including Atmel's EPROM line. Atmel's chips specifically do not have any programming problem "of the first kind" with $V_{CC} = 5V$. This is due to the proprietary programming circuits used in Atmel EPROMs. That same programming circuitry also makes an Atmel EPROM quite insensitive (compared to other EPROM suppliers) to the level of V_{PP} voltage used during programming. However, just as with other EPROM suppliers, Atmel can guarantee the same product reliability for $V_{CC} = 5V$ programming as with nominal V_{CC} programming only if parts are specially tested.

Using Programmable Logic Devices

Introduction

This Application Note covers three areas:

- Where and *why* do I use programmable Logic Devices (*PLDs*)?
- *How* do I use PLDs?
- Software and Hardware *support* for Atmel PLDs.

Where Do I Use PLDs?

Any digital logic design can be done using PLDs. If you normally begin your design by:

- Using AND and OR functions
- Thinking of 7400 series components
- Using truth tables, or
- State diagrams

you are already on the path to using PLDs.

Designing a microprocessor based system, with memory and I/O? How about all that "glue" logic you use to interface with the bus, provide chip selects, and any unusual signals required by special chips? Most of these functions are currently done with 7400 series TTL. *How about using a PLD instead?*

Designing a stand-alone PC board which uses a state machine to control multiple output signals? Using latches to synchronize signals? Using counters to divide down master clock frequencies? Converting parallel to serial and back again? All of these functions fit easily in modern PLD's. *Most anything found in your TTL Databook can be replaced with your own, PERSONALIZED, programmable logic device.*

PLD Applications

- **Glue Logic**
- **State Machines**
- **Synchronization**
- **Decoders**
- **Counters**
- **Bus Interfaces**
- **Parallel to Serial**
- **Serial to Parallel**
- **Subsystems**
- **and Many Others**

Why PLDs?

Maybe you have already heard all the wonderful reasons for using PLDs. Well, they're true! First, let's review some of the more important ones:

- **Increased Integration.** You can reduce the package count of your designs while simultaneously increasing the features offered by your product.
- **Lower Power.** CMOS and fewer packages combine to reduce power consumption.
- **Improved Reliability.** Lower Power plus fewer interconnections and packages translate into greatly improved system reliability.
- **Lower Cost.** PLDs reduce inventory costs, too.
- **Easier To Use!** Yes, believe it or not, once you get past the initial learning period, PLDs are easier to use than discrete logic functions.
- **Easier to Change.** Oops! Need to make a change? You won't need "blue wire" when you use a PLD - all changes are internal, and can be done quickly. ECNs are a snap - and system reliability is maintained!

UV Erasable Programmable Logic Device

Application Note

Let's Get Started!

Figure 1 describes the PLD design process. After having read the first part of this application note, you now have the perfect application for a PLD, right? So here you go!

How do you translate your idea into a working prototype? *First, you need a computer with an editor of some kind.* If you have a workstation with a schematic editor, you may input your design using familiar logic blocks. Otherwise, a line or full screen text editor, used in the non-document mode will do. An example of an ABEL™ text file is on the next page.

Next, turn the **logic compiler** loose on your design. First it will *check for typographical errors* and any inconsistencies in your specification. Most compilers then attempt to *reduce your logic* using standard logic reduction theory. Then, a **simulator** will check the test vectors you input, comparing your logic description against the predicted responses. This is an excellent way to verify your design. Check with the appropriate software manuals for more information.

At the end of the compilation process, a "**JEDEC**" file is output. This file is a standard format accepted by most programming hardware. Next *download this file* to your chosen programmer.

At this point you are ready to "build" your **prototype**. Make sure the programmer has the correct information to program the device you have chosen (an Atmel PLD, of course), plug in your device, and go! Most programmers will even functionally test your prototype for you if you include test vectors in your JEDEC file.

Take your configured PLD, and *plug it into your system.* If you find any errors, just use your editor to make the necessary changes, and repeat the process. It's easy!

Example Design

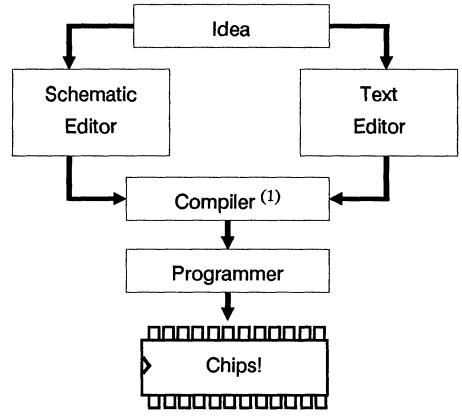
The following design is a simple example using ABEL™ to process the logic description file and an AT22V10 as the target device. The equations are on the next page, and are a direct reproduction of the actual ABEL input file.

Each of the three allowable input formats are shown. A truth table is used to describe a simple 2 to 4 decoder, as is often used to decode chip selects in a microprocessor system. Next, the state machine format is used to describe a divide by 4 counter. And finally, boolean equations are used to describe some random logic.

Note the test vectors used to test the device. The "c" nomenclature means that this pin has a low to high to low series of transitions for this vector. Each time this happens, the counter should increment. Also note that the counter starts in the reset condition, which is both outputs "1" for an active low output.

Now you're ready to go - Have fun!

Figure 1. PLD Design Process



Note: 1. Examples of compilers are ABEL™, CUPL™, and LOG/iC. Each of these products contains modules which allow simulation of your design. They also minimize your logic equations, which gives you flexibility in describing your design.

Software Support Versions

Atmel EPLD	Data I/O ABEL™	Logical Devices CUPL™	ISDATA LOG/iC	Atmel-ABEL™	PistoHI Pet100
AT22V10	1.3,2.0,3.0	2.0	2.3		1.XX
ATV750	3.0	2.15b	3.0	1.01	1.XX
ATV2500	3.2	3.2a		1.01	1.XX

Example Abel™ Description File

```
module X3  flag'-r3';
title 'Example using 22V10 - KHG 1/6/88';
X310 device 'P22V10';
"
Clk,A12,A13              pin     1,2,3;
CE0,CE1,CE2,CE3          pin     20,21,22,23;
Q1,Q2,CarOut             pin     17,18,14;
CarEn,A,B,C,D            pin     6,7,8,9,10;
Out1,Out2                pin     15,16;
"
X,Z,c       =       .X.,.Z.,.C.;
"
"Counter States
State1   =  ^b00;   State2   =  ^b01;
State3   =  ^b10;   State4   =  ^b11;
"
"The following truth table defines the 2 to 4 decoder, which decodes
"  A13 and A12 into CE0, CE1, CE2, and CE3.
truth_table ([A13,A12] -> [CE0,CE1,CE2,CE3])
[0,0] -> [0,1,1,1];
[0,1] -> [1,0,1,1];
[1,0] -> [1,1,0,1];
[1,1] -> [1,1,1,0];
"The following state description defines the divide by 4 counter
state_diagram  [Q2,Q1]
State State1:   GOTO   State2;
State State2:   GOTO   State3;
State State3:   GOTO   State4;
State State4:   GOTO   State1;
"The following equations are general in nature to illustrate boolean input
"  format.  The CarOut equation uses state 4 above to produce a carry.
Equations
CarOut  =   Q2 & Q1 & CarEn;   "& = AND
Out1    =   A & B + C & D;  "+ = OR, AND takes precedence
Out2    =   A & C + B & D;
"The following are the appropriate test vectors
test_vectors
"
([Clk, CarEn, A13,A12, A, B, C, D]  - > [CE0,CE1,CE2,CE3,Q2,Q1,CarOut,Out1,Out2]);
[0, 0, 0, 0, 0, 0, 0, 0] - > [0, 1, 1, 1, 1, 1, 0, 0, 0];
[c, 0, 0, 1, 1, 1, 0, 0] - > [1, 0, 1, 1, 0, 0, 0, 1, 0];
[c, 0, 1, 0, 1, 0, 1, 0] - > [1, 1, 0, 1, 0, 1, 0, 0, 1];
[c, 0, 1, 1, 0, 0, 1, 1] - > [1, 1, 1, 0, 1, 0, 0, 1, 0];
[c, 0, 0, 0, 0, 1, 0, 1] - > [0, 1, 1, 1, 1, 1, 0, 0, 1];
[0, 1, 0, 1, 1, 1, 1, 1] - > [1, 0, 1, 1, 1, 1, 1, 1, 1];

end X3;
```

New Programmer Support Information

Company	Model	AT22V10 Version	Fam/Pin Code	ATV750 Version	Fam/Pin Code	ATV2500 Version
Data I/O	Model 29B LogicPak 303A-011A	V04	6528	V05	650F	
	Model 60A	V11	6528			
	Unisite	V1.7	Menu	V2.2	Menu	2.45
Stag	Model ZL30,ZL30A	30A27	47070	30A30	47165	
	Model PPZ Zm2200					
PistoHI	PET100	PP61	Menu	PP61	Menu	PP62
Logical Devices	AllPro	V1.49C	Menu	V1.48C	Menu	V1.49C
SMS	Sprint Plus	3.2H	Menu	3.2H	Menu	
	Sprint Expert			3.2J3	Menu	3.2J3
BP Microsystems	PLD-1100	1.11	Menu	1.12	Menu	
Advin Systems	Sailor-PAL	9.72		9.71		
System General	SGUP-85	2.1		3.1		
Inlab	28A	10.03g		10.03g		

Programming Software Companies

Data I/O Corporation (ABEL™)
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

Logical Devices (CUPL™)
1321 N.W. 65 Place
Ft. Lauderdale, FL 33309
(305) 974-0967
(800) 331-7766

ISDATA Gmbh (LOG/iC)
Haid-und-Neu- Str. 7
D-7500 Karlsruhe 1
West Germany
0721 / 69309

C/O Adams MacDonald Enterprises
800 Airport Rd.
Monterey, CA 93940
(408) 373-3607
(800) 777-1202

PistoHI Electronic Tool Co.
22560 Alcalde Rd.
Cupertino, CA 95014
(408) 255-2422
(800) 2PISTOHL

ACCEL Technologies, Inc.
6825 Flanders Drive
San Diego, CA 92121
(800) 433-7801

Programming Hardware Companies

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118

PistoHI Electronic Tool Co.
22560 Alcalde Rd.
Cupertino, CA 95014
(408) 255-2422

Logical Devices
1321 N.W. 65 Place
Ft. Lauderdale, FL 33309
(305) 974-0967
(800) 331-7766

SMS
C/O Adams MacDonald Enterprises
800 Airport Rd.
Monterey, CA 93940
(408) 373-3607

BP Microsystems
10681 Haddington #190
Houston, TX 77043
(713) 461-9430

Advin Systems, Inc.
1050-L East Duane Ave.
Sunnyvale, CA 94086
(408) 984-8600

System General
510 South Park Victoria Drive
Milipitas, CA 95035
(408) 263-6667

Inlab
2150 I W 6th Ave
Broomfiled, CO 80020
(800) 237-6759

Selecting Decoupling Capacitors For Atmel's EPLDs

UV Erasable Programmable Logic Device

Application Note

Introduction

This application note provides a summary of information needed when selecting decoupling capacitors for Atmel Programmable Logic Devices. A .22μF, multi-layer ceramic or plastic dielectric capacitor is recommended for such use. Either surface-mount (SMD) or radial-leaded devices should be used. Because of their high parasitic resistance and/or inductance, tantalum, aluminum electrolytic, and axially leaded capacitors are not recommended.

When Is a Capacitor Not a Capacitor

Unfortunately, capacitors are not the perfect charge storage devices we would like them to be. Their lead wires and internal construction create parasitic resistance and inductance in series with the capacitance. These parasitics are usually referred to as ESR (equivalent series resistance) and ESL (equivalent series inductance), respectively. As will be shown, these parasitics can seriously reduce the ability of many types of capacitors to decouple supply noise in high-speed systems. Table 1 gives typical ESR and ESL values for various types of capacitors.

As shown, ESR values range from 0.01 Ohm to as high as 9 Ohms. ESL varies from 2nH for typical surface mount devices to 20nH for electrolytic capacitors. These numbers are typical values, taken from data from several manufacturers. As expected, there is some variation between manufacturers. Also, worst case specification values will be significantly higher, especially for ESR values.

How ESR And ESL Can Affect High Speed Operation

The effects of these parasitics may be best illustrated by a simple example. Consider the case of a 22V10L. In the stand-by mode, Icc current is typically only 5mA. When an input switches, Icc may temporarily go as high as 100mA. This increase in current draws charge from the local decoupling capacitor. This capacitor current will create voltage drops across the ESR and ESL parasitic elements. To see how these voltage drops can cause problems in a system, look at a typical decoupling application.

In this example the design goal of the capacitor is to keep local supply noise below .2 Volts, a reasonable expectation. This immediately sets an upper limit on ESR of 2 Ohms.

$ESR_{max} = V_{noise} / I_{max}$

Imax= Highest Expected Capacitor Current

The upper limit on ESL is determined by how quickly the capacitor's current must change, as well as how much supply noise will be tolerated during that change. For high-speed logic devices, Icc must be able to switch from stand-by to active levels within 2 to 3 nanoseconds.

$ESL_{max} = V_{noise} \bullet I_{max} / \Delta_t$

Δt = Time allowed for capacitor current to switch

In this example, an upper limit on ESL of 4 to 6nH is set.

Consider what can happen if these limits are exceeded. If an axially leaded multilayer ceramic capacitor with ESR of .15 Ohm is used, the resistance drop in our

10

application will not be significant (100 mA X .15 Ohm = 15 mV). However, the inductance will not allow the current to reach 100mA in 6nsec. This can slow the logic device switching by several nanoseconds.

What Types To Use: Multi-layered Ceramic and Plastic Dielectrics

From this example, it is apparent that the parasitic elements on capacitors can easily limit their decoupling ability. Therefore, users of high-speed logic need to pick their capacitors with care. The data in Table 1 shows that the best bets are surface-mount, multi-layered ceramic (MLC) or plastic dielectrics. Of the leaded devices, only radial types are recommended.

Within the MLCs, there are different classes of dielectric. Class I has the best characteristics, but its small dielectric constant makes it impractical for decoupling values. Class II is highly recommended, as it has good temperature stability (% variation -55C to 125C) and aging characteristics (10% in 10 years). Class III, on the other hand, drops to less than 50% of its rated capacitance at 85C, and to only 25% at -55C. Class III dielectric also loses 20% of its rated value in 10 years. Therefore, Class III MLCs are only recommended for applications where temperature excursions are minimal.

Plastic dielectric capacitors in general offer performance as good as Class II MLCs. Among the dielectrics available today are polypropylene, polyester, polycarbonate, polystyrene and teflon. Capacitance variation with temperature depends on the particular material, but is generally less than +/-20% from -55C to 125C. Aging is minimal, usually less than 2% in 10 years. Unfortunately, not many manufacturers make surface mount plastic dielectric capacitors. That should change soon, as surface mount technology advances and becomes more common.

When using radial leaded cases, be sure to minimize lead lengths, as ESL increases quickly with longer leads. For example, if a capacitor has 6nH of inductance with 2 mm leads, extending leads to 5mm will increase ESL to 10nH.

What Types Not To Use: Aluminum Electrolytic, Tantalum, And Anything Axial

The design example above together with the numbers given in Table 1 show that some types are not suitable at all for decoupling high-speed devices. Specifically, the high inductance of axially leaded capacitors puts them on the "don't use" list. Also, tantalum and aluminum electrolytic devices are generally not recommended, as they have high ESR and/or ESL, even in radial and surface mount configurations.

In Any Case, know Your ESL and ESR

ESR data is often found in catalogs. However, this will normally be only low-frequency data, and ESR is frequency dependent (dropping at higher f). ESL data is not usually given in catalogs. The best thing to do is get Z versus frequency data from the manufacturer. From such a graph (with frequency up to at least 10MHz), you can extract high frequency ESR and ESL.

How Much Capacitance Do I Need

For decoupling Atmel's EPLDs a .22μF capacitor is recommended. In many cases, this will be overkill. However, determining how much less you could get by with for a particular application is dependent upon several factors. The number of PC board supply planes, the board's dielectric thickness and dielectric constant, the value (AND ESR AND ESL!) of power entry decoupling capacitors, among other things, will determine just how much is really needed. The best bet is to use a good .22μF and be safe. Besides, the more decoupling is taken care of by local capacitors, the lower the board's HF emissions will be.

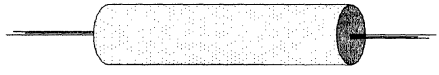
Summary

Choosing the right decoupling capacitor is an important part of high-speed circuit design. Choosing the wrong one can introduce supply noise that can slow down signal switching or even end up giving incorrect data. For decoupling Atmel EPLDs, .22uF capacitors are recommended. These should be of either multi-layer ceramic or plastic dielectric type. Surface mount devices are best, with radial leaded cases also being acceptable.

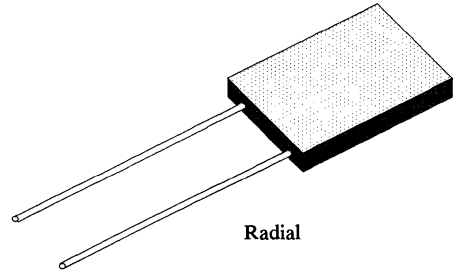
Table 1. Capacitor Types and Recommendation Ratings

Dielectric	Body	L (nH,typ)	R (ohm,typ)	Rating	Comments
Ceramic II	SMD	2	.02	E	Highly recommended
	Radial	6	.07	G	Keep leads short
	Axial	12	.07	S	Axial always = Higher L
Ceramic III	SMD	2	.04	G	C loss hot/cold/old
	Radial	6	.15+	S	
	Axial	12	.15+	X	
Plastics	SMD	2	.03	E	Hard to find
	Radial	5+	.01+	G	Get R and L data
	Axial	12+	.01+	X	
Aluminum Electrolytic	SMD	13	9.0	X	Forget it
	Radial	15+	1.5+	X	
	Axial	20	1.5	X	
Tantalum	SMD	?	3.0	X	
	Radial	10+	1.0	X	
	Axial	15+	1.0	X	

Ratings code:
E Excellent; highly recommended
G Good; will perform well in most applications
S Satisfactory; be aware of specific vendor's device performance
X Not recommended



Axial



Radial

S.M.D.

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Using A Programmable Logic Device As A System Controller In an I/O Bus Based System [1]

Summary

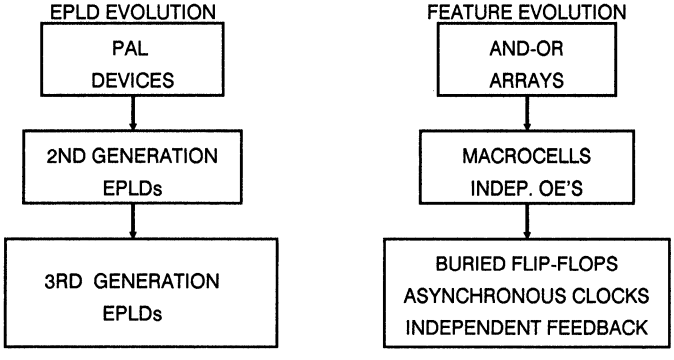
As PLDs (Programmable Logic Devices) become more complex, the amount of logic that can be placed in one device is rapidly increasing. Complete controllers and subsystems now fit into one or two PLDs. As a result, the PLD may now be connected directly to the system bus as an independent peripheral. First generation PAL® devices are difficult to use in these applications. However, recent innovations in PLD architecture enable them to be easily designed into bus-based systems.

PLD Evolution

The driving force behind PLD usage has been to integrate as much of the SSI (Small Scale Integration) logic on a packed PC board as possible. The first level of integration was made possible by the invention of the PAL device. First generation products were usually in 20-pin packages with a typical device having nine dedicated inputs and eight dedicated outputs. One input pin was a dedicated output enable, and one pin a dedicated, common clock for up to eight flip-flops. Making one of these devices work on an I/O bus was difficult and typically was used as little more than a simple latch.

In the mid eighties, second generation devices appeared. These PLDs are generally in 24 or more pins, have independent output enable controls and "Output Macrocells." The macrocells allow the designer to configure each output independently as registered or combinatorial. However, there are still too few registers in these devices to allow the design of complex state machines. Also, these circuits lack independent feedback paths, which further reduce the usable number of registers. This also complicates the use of the output pins as true I/O structures.

Note: 1. This article originally appeared in Northcon '86
®PAL is the registered trademark of Monolithic Memories



Recently several third generation devices (such as the Atmel ATV750) have appeared. These devices are differentiated by the following features:

- **Extra Registers**

Up to twice the usual number. The ATV750 has 20 flip-flops.

- **Independent Feedbacks**

Feedback paths for the registers are independent of the output configuration. In addition, there are separate input paths from the I/O pads.

- **Asynchronous Clocks**

Product terms for each flip-flop's clock allows the designer to break up the registers into different functional blocks.

Control function outputs that have no other use than to manage the other resources inside the PLD need not be brought outside the device, allowing implementation of complex state machines internally.

As PLDs have evolved, so have the applications for them. Initially, PLDs could only integrate a few SSI functions. A typical application was a special-purpose decoder or encoder. With the introduction of more flip-flops, MSI (Medium Scale Integration) functions such as state machines could be designed. Third generation devices are the first true LSI (Large Scale Integration) devices, and are capable of integrating several of the previous generation devices into one package. Now state machines can be combined with an output decoder to control peripheral functions, and still have adequate resources to interface directly to the microprocessor.

System Application

The following example is an application of the Atmel ATV750 as a peripheral resource controller. The design required a state machine, a bus interface unit and a peripheral control interface. All 10 outputs of the ATV750 are used, most in the combinatorial mode. However, the 17 required flip-flops were still available to latch the address and data buses, provide a status register, and a two-bit counter. This design would require three second generation, 24-pin PLDs, or five first generation 20-pin devices and at least two other discrete devices. In all, more than 80 per cent of the ATV750 is utilitized. The number of gates alone integrated into the ATV750 in this application is more than other 24-pin PLD's have to offer.

- **The System**

The system described is a peripheral controller/bus interface for connecting a special-purpose, custom encryption / exponentiation chip to an 80186 microprocessor (Figure 1). The custom chip has a serial interface, and only one bi-directional pin to indicate its "busy" status. All chip functions are controlled with a set of single-purpose input pins. While simple, this interface is not directly compatible with a modern microprocessor, such as the 80186. The PLD system described not only combines the required glue logic, but also offloads the parallel-to-serial conversion from the processor. This application note will only touch on the salient features of the design, and why a third generation device is so useful.

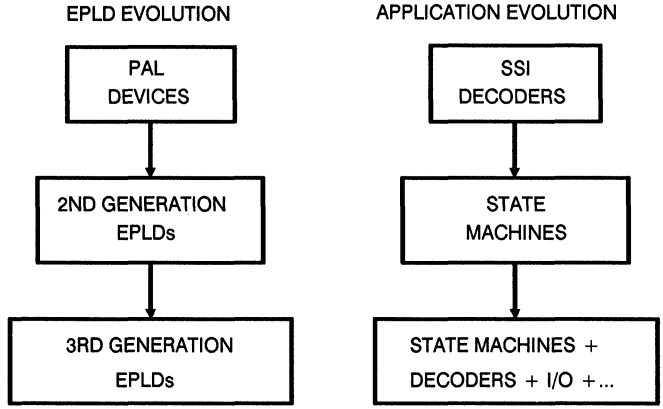
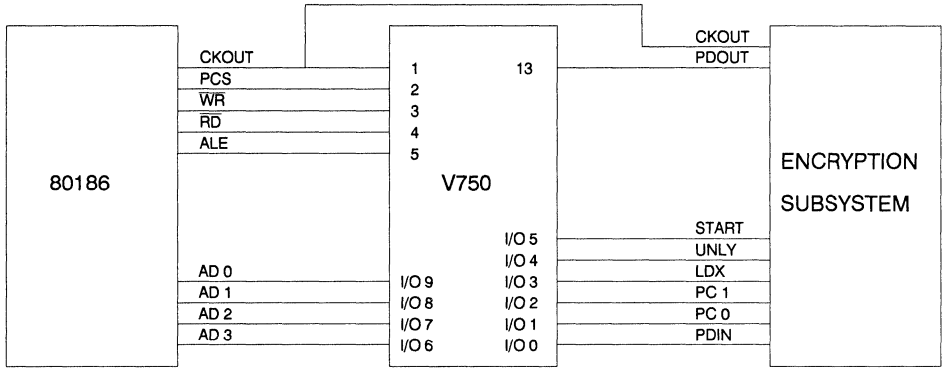


Figure 1. System Diagram



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• The Microprocessor Bus

The 80186 uses a multiplexed address and data bus. Several control signals, such as ALE, $\overline{RD}$ and $\overline{WR}$ tell the system when to get what type of data from the bus. The 80186 also has some internally decoded chip selects, and one is used here for convenience. The system clock is an 8Mhz signal, which is appropriate for the encryption chip and well within this PLDs timing specification. The lower four bits of the address are latched into the PLD to define the upcoming operation, which then allows the PLD to output the requested data in one read cycle of the microprocessor. These address bits are decoded to define the instruction to be executed by the PLD subsystem.

• Tackling the I/O Bus

Using first and second generation PLDs, the equations for the I/O bus interface are shown in Figure 2. These equations consume 12 sum terms, 8 flip-flops, and 12 output pins. Since this requires two PLDs, another 10 input pins are required as well. When rewritten for the ATV750, only four macrocells are required, and eight sum terms and flip-flops. No extra inputs are required, as the ATV750s I/Os are true input/output pins.

The equations for the ATV750 are in Figure 3. This compaction is possible for three reasons:

1. The individual product terms for OE permit the pin to be used as both an input and output.

2. The three feedback paths allow both registers to be used while the pin status is still available to the array.

3. The product term for the flip-flop clock means that the sum term for one of the flip-flops can be shared between the D input and the output pin. A single ATV750 macrocell can incorporate logic which would require up to three output pins and one input pin in other PLDs.

Figure 2

```
ad0     =     adp0 & !pcs & !rd & ai0 & !ai2          "output data
        #     !pc0 & !pcs & !rd & !ai0 & !ai2         "status "
        #     yst & !pcs & !rd & !ai0 & !ai2;         "status unly

ad1     =     adp1 & !pcs & !rd & ai0 & !ai2          "output data
        #     !pc1 & !pcs & !rd & !ai0 & !ai2;        " status "

ad2     =     adp2 & !pcs & !rd & ai0 & !ai2          " output data
        #     xst & !pcs & !rd & !ai0 & !ai2          " status "
        #     !pc0 & !pcs & !rd & !ai0 & !ai2         " status "
        #     !pc1 & !pcs & !rd & !ai0 & !ai2;        " status "

ad3     =     adp3  & !pcs & !rd & ai0 & !ai2         " output data
        #     startqb & !pcs & !rd & !ai0 & !ai2;     " status "

adp0    :=    ad0 & !pcs & !wr                        " load data
        #     pdout & !ystb                           " circulate y"
        #     pdout & !xstb                           " circulate x"
        #     pdout & !pcs0                           " circulate load"
        #     pdout & !pcs1                           " circulate load"
        #     adp0 & ystb & xstb & pcs0 & pcs1 & pcs  " hold data"
        #     adp0 & ystb & xstb & pcs0 & pcs1 & wr;  " hold data"

adp1    :=    ad1 & !pcs & !wr                        " load data
        #     adp0 & !ystb                            " circulate y"
        #     adp0 & !xstb                            " circulate x"
        #     adp0 & !pcs0                            " circulate load"
        #     adp0 & !pcs1                            " circulate load"
        #     adp1 & ystb & xstb & pcs0 & pcs1 & pcs  " hold data"
        #     adp1 & ystb & xstb & pcs0 & pcs1 & wr;  " hold data"

adp2    :=    ad2 & !pcs & !wr                        " load data
        #     adp1 & !ystb                            " circulate y"
        #     adp1 & !xstb                            " circulate x"
        #     adp1 & !pcs0                            " circulate load"
        #     adp1 & !pcs1                            " circulate load"
        #     adp2 & ystb & xstb & pcs0 & pcs1 & pcs  " hold data"
        #     adp2 & ystb & xstb & pcs0 & pcs1 & wr;  " hold data"

adp3    :=    ad3 & !pcs & !wr                        " load data
        #     adp2 & !ystb                            " circulate y"
        #     adp2 & !xstb                            " circulate x"
        #     adp2 & !pcs0                            " circulate load"
        #     adp2 & !pcs1                            " circulate load"
        #     adp3 & ystb & xstb & pcs0 & pcs1 & pcs  " hold data"
        #     adp3 & ystb & xstb & pcs0 & pcs1 & wr;  " hold data"

ai0     :=    ad0 & pcs                               " idle state "
        #     ad0 & ale                               " idle state "
        #     ai0 & !pcs & !ale;                      " hold instruction"

ai1     :=    ad1 & pcs                               " idle state "
        #     ad1 & ale                               " idle state "
        #     ai1 & !pcs & !ale;                      " hold instruction"

ai2     :=    ad2 & pcs                               " idle state "
        #     ad2 & ale                               " idle state "
        #     ai2 & !pcs & !ale;                      " hold instruction"

ai3     :=    ad3 & pcs                               " idle state "
```

Figure 3

```
ai0.ck      =     clk2 & !ale; ai2.ck  =   clk2 & !ale;    ".....clock instruction
ai1.ck      =     clk2 & !ale; ai3.ck  =   clk2 & !ale;    ".....clock instruction

ai0         =     ad0 & !pcs & ale                         ".....load instruction"
            #     adp0 & !pcs & !rd & ai0 & !ai2           ".....output data
            #     !pc0 & !pcs & !rd & !ai0 & !ai2          ".....status "
            #     yst & !pcs & !rd & !ai0 & !ai2           ".....status unly

ai1         =     ad1 & !pcs & ale                         ".....load instruction"
            #     adp1 & !pcs & !rd & ai0 & !ai2           ".....output data
            #     !pc1 & !pcs & !rd & !ai0 & !ai2;         ".....status "

ai2         =     ad2 & !pcs & ale                         ".....load instruction"
            #     adp2 & !pcs & !rd & ai0 & !ai2           ".....output data
            #     xst & !pcs & !rd & !ai0 & !ai2           ".....status "
            #     !pc0 & !pcs & !rd & !ai0 & !ai2          ".....status "
            #     !pc1 & !pcs & !rd & !ai0 & !ai2;         ".....status "

ai3         =     ad3 & !pcs & ale                         ".....load instruction"
            #     adp3  & !pcs & !rd & ai0 & !ai2          ".....output data
            #     startqb & !pcs & !rd & !ai0 & !ai2;      ".....status "

enable ad0  =     !pcs & !rd;  enable ad2  =   !pcs & !rd;
enable ad1  =     !pcs & !rd;  enable ad3  =   !pcs & !rd;
(adp equations remain the same as before, but are now buried in the macrocell)
```

Figure 4

```
!pc0        =     !clk22 & !pcs0;          state diagram [count,cn1,cn0]
                                           state s0 : case (ai3 & start):ss1;
!pc1        =     !clk22 & !pcs1;          (ai2)          : s1;
                                           (ai0 & !ai2)   : s1;
!pcs0       :=    ai2 & ai0 & start        endcase;
            #     !cn0 & count & !pcs0     state s1:                GOTO  s2;
            #     !cn1 & count & !pcs0     state s2:                GOTO  s3;
                                           state s3:                GOTO  s0;
!pcs1       :=    ai1 & ai2 & start        state ss1:               GOTO  ss2;
            #     !cn0 & count & !pcs1     state ss2:               GOTO  ss3;
            #     !cn1 & count & !pcs1;    state ss3:               GOTO  s0;
```

• The Chip Interface

The encryption chip is loaded and unloaded serially, four bits at a time in this design. The equations for the interface logic are in Figure 4. Also in this figure is a simple state diagram for the two bit counter required for this design. This state machine is buried, and its decoded outputs are used to control the serial transfers.

• Starting the Peripheral Chip

To begin execution in the peripheral chip, a bi-directional signal named "start" is asserted. This is an active low signal. The controller must assert this signal low for four clock cycles. Then the exponentiation chip will hold this line low until it has completed its operations. An external pull up resistor is required. The internal flip-flop, whose output is named "stint", contains the state of the peripheral. This is used to signal the microprocessor that the subsystem is busy when the processor reads the ATV750's status.

• Multiplexing Flip-Flop Inputs and I/O Pins

One I/O pin / flip-flop combination can be used to store the state of the encryption chip and to output this to the peripheral. This is accomplished by multiplexing the sum term output between the flip-flop's D input and the output buffer. The sum term and the OE product term are active to begin the encryption chip's exponentiation cycle. After the state machine counter finishes counting, the output is put into the high impedance state. If the external chip has begun its operation correctly, it will then hold the pin low. Now the state of the I/O pin is used as the D input to the flip-flop, but not output because the OE term is off. The multiplexed macrocell is in Figure 7. The following simple equations are all that is required to implement this logic:

enable start = !count;

stint: = !count

#!start & count;

start.c = clk2;

Conclusion

The application of a third generation EPLD in an I/O bus based system demonstrates the usefulness of the following features:

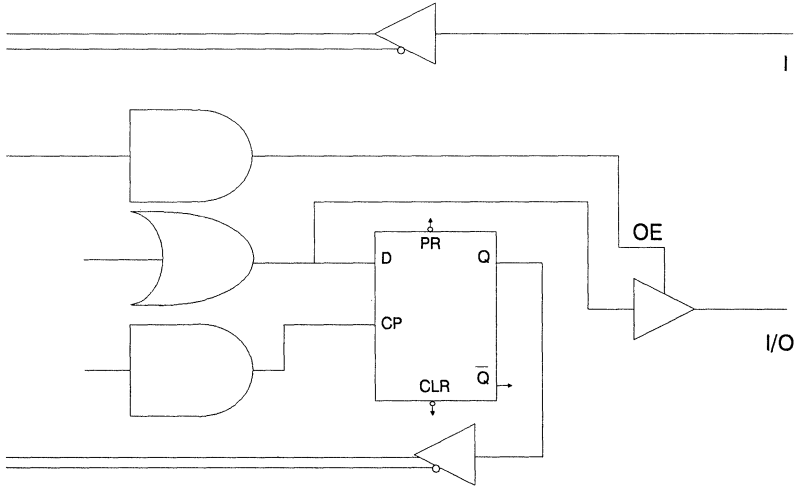
Buried Registers

Independent Feedback Paths

Asynchronous Register Clocks.

This design consists of roughly 600 gates, which fit into a ATV750 gate complexity EPLD with an 80 per cent utilization factor. Due to the usefulness of the new features and their implementation in the macrocell of the ATV750, this design, which would have required 3 second generation devices, could easily fit into one ATV750.

Mulitplexed "D" Input

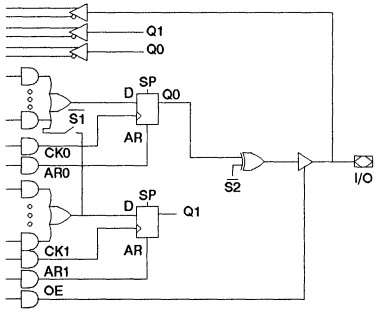


Using the Buried Nodes and Feedbacks

Introduction

Conventional EPLD I/O pin logic forces you to choose either a dedicated output pin or a dedicated input pin. This renders the output register unusable. Multiple feedback paths and individual product term controlled output enables (OEs) make the ATV750 I/O pins truly bi-directional. An ATV750 I/O pin can be configured as a dedicated input, a dedicated output, or an input and output bus interface pin. No registers are sacrificed in the process. All registers can be buried.

Registered Output



Buried Registers

To use the buried register outputs, they must have a unique name. The compilers need to know which register to associate with each signal name. Each compiler uses a different method for assigning node numbers to signal names. Table 1 shows how to assign these names for each compiler. Table 2 lists node names for each compiler. Note: Q1 need not be defined if Q0 is sharing Q1's product terms.

ABEL, Atmel-ABEL, CUPL, and TangoPLD: If the output is combinatorial or if Q0 shares the product terms of Q1 in a registered output, the Q1 node does not need a name. Name Q1 nodes with the proper node numbers and refer to Feedback Options on how to access Q0s and Q1s.

LOGiC: LOGiC requires you to name the Q0 nodes if you are using the pin as an input and still using Q0, or if you are using OE to make the pin an input and an output.

PistoHl: No node numbers are necessary.
Q0 nodes are named by declaring
: nodename0 Q0! pinname;
Q1 nodes are named by declaring
: nodename1 Q1! pinname;

Table 1. ATV750 Node Declaration

Product	Example	Node	Declaration	Comments
ABEL	anyname	node	26;	
Atmel-ABEL	anyname	node	26;	
CUPL	pinnode	25 =	anyname;	
LOGiC	anyname	=	1;	Following key word *NODE
PistoHl	anyname	Q0!	pinname;	Use Q1! for Q1 declaration
TangoPLD	anyname			In PUTPART place "anyname" as the 25th signal

Table 2. ATV750 Node Numbers

ATV750 Pin Numbers	ABEL Q1	Atmel-ABEL Q1	CUPL Q1	LOGiC Q0	LOGiC Q1	TangoPLD Q1
14	26	26	25	2	1	25
15	27	27	26	4	3	26
16	28	28	27	6	5	27
17	29	29	28	8	7	28
18	30	30	29	10	9	29
19	31	31	30	12	11	30
20	32	32	31	14	13	31
21	33	33	32	16	15	32
22	34	34	33	18	17	33
23	35	35	34	20	19	34

ATV750 Feedbacks

Each third party product uses a slightly different syntax for accessing the feedback paths (refer to Table 3). Whenever the Q0 register is used and the OE term is disabled or conditionally disabled, care must be taken to ensure the correct feedback path is referred to in your equations. Version 1.11 of Tango-PLD does not support the Q0 feedback. This syntax may change with each new software revision. Please check with the specific software manufacturer or Atmel EPLD Applications if you are experiencing unexpected results.

Feedback Options: Registered Output

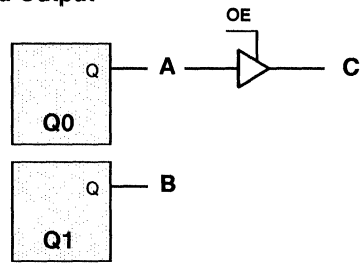


Table 3. ATV750 Feedback Paths

	A	B	C
ABEL	pinname.Q	nodename	pinname
Atmel-ABEL	pinname.Q	nodename	pinname
CUPL	pinname	nodename	pinname.IO
LOGiC	nodename0	nodename1	pinname
PistoHI	nodename0	nodename1	pinname
TangoPLD	no support	nodename	pinname

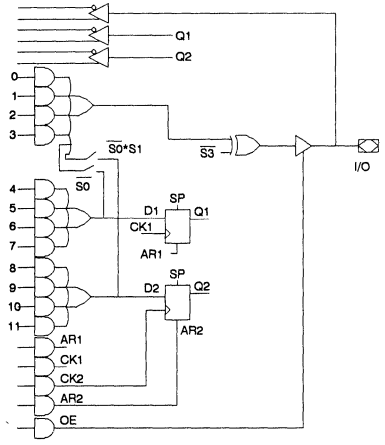
ATV2500 Node Numbering

With an additional OR, the ATV2500 logic cell becomes even more versatile than the ATV750 logic cell. Under certain situations, an additional set of buried registers must be defined. The same syntax used for ATV750 (Table 3) can be used to name the ATV2500 buried registers. The node numbers are listed in Table 4.

ABEL, Atmel-ABEL, CUPL, and TangoPLD: Q1 need not be named when the output logic cell is configured as 8 or 12 term combinatorial output. Q2 need not be named when output logic cell is configured as 12 product term combinatorial or registered output. Name Q1 and Q2 nodes with the proper node numbers and refer to Feedback Options for selecting the correct feedback paths.

PistoHl: No node numbers are necessary.
Q1 nodes are named by declaring
: nodename1 Q1! pinname;
Q2 nodes are named by declaring
: nodename2 Q2! pinname;

Combinatorial Output



Registered Output

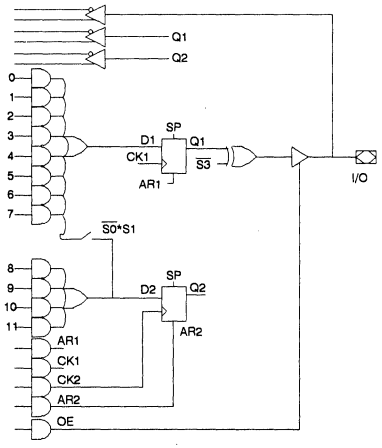


Table 4. ATV2500 Node Numbers

ATV2500 Pin Numbers	ABEL		Atmel-ABEL		CUPL		TangoPLD	
	Q1	Q2	Q1	Q2	Q1	Q2	Q1	Q2
4(1)	217	41	217	41	65	41	41	65
5(1)	218	42	218	42	66	42	42	66
6(2,3)	219	43	219	43	67	43	43	67
7(3)	220	44	220	44	68	44	44	68
8	221	45	221	45	69	45	45	69
9	222	46	222	46	70	46	46	70
11	223	47	223	47	71	47	47	71
12	224	48	224	48	72	48	48	72
13	225	49	225	49	73	49	49	73
14	226	50	226	50	74	50	50	74
15	227	51	227	51	75	51	51	75
16	228	52	228	52	76	52	52	76
24	229	53	229	53	77	53	53	77
25	230	54	230	54	78	54	54	78
26	231	55	231	55	79	55	55	79
27	232	56	232	56	80	56	56	80
28	233	57	233	57	81	57	57	81
29	234	58	234	58	82	58	58	82
31	235	59	235	59	83	59	59	83
32	236	60	236	60	84	60	60	84
33	237	61	237	61	85	61	61	85
34	238	62	238	62	86	62	62	86
35	239	63	239	63	87	63	63	87
36	240	64	240	64	88	64	64	88

Notes: 1. Due to the memory limitations of PC/MS DOS, ABEL PC versions 3.0 to 3.2 and Atmel-ABEL 1.01 do not support the macrocells associated with pin 4 and 5. These pins can only be used as inputs.
2. These same versions of ABEL and Atmel-ABEL (see above) do not support the AR terms of Q2 associated with pin 6.
3. These same versions of ABEL and Atmel-ABEL (see above) do not support the Synchronous Preset of pin 6 and 7.

ATV2500 Feedbacks

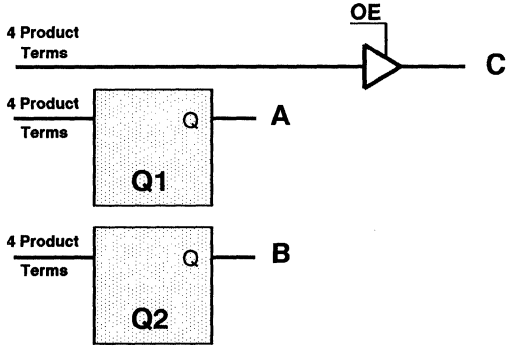
Each third party product uses a slightly different syntax for accessing the feedback paths (refer to Table 5). Whenever the Q1 register is used while the OE term is disabled or conditionally disabled (e.g. during read cycles), care must be taken to ensure the correct feedback path is used. For example, a counter can lose its count if you use the pin feedbacks rather than the Q1 register feedbacks and decide to disable the OE for the read cycle.

The current version of Tango_PLD cannot support the Q1 feedback when the I/O pin is configured as an input (OE disabled) or when OE is conditionally disabled.

This syntax may change with each new software revision. Please check with the specific software manufacturer or Atmel EPLD Applications if you experience unexpected results.

Feedback Options:

Combinatorial Output



Registered Output

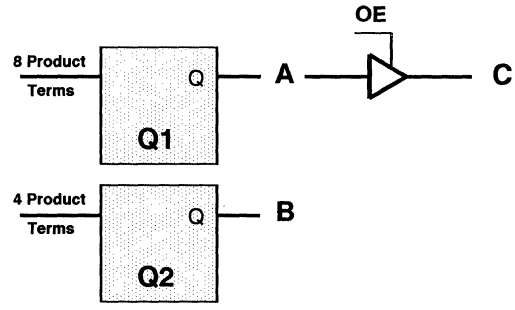


Table 5. ATV2500 Feedback Paths

		A	B	C
ABEL	Registered	pinname.Q	nodename2	pinname
	Combinatorial	nodename1	nodename2	pinname,
CUPL	Registered	pinname	nodename2	pinname.IO
	Combinatorial	nodename1	nodename2	pinname
Tango-PLD	Registered	no support	nodename2	pinname
	Combinatorial	nodename1	nodename2	pinname

Interfacing the AT76C10/E to a Microcontroller

CMOS Programmable Amplifier

Delay Equalizer

Application Note

Introduction

The AT76C10/E is a programmable gain amplifier integrated with a programmable telephone line group delay equalizer on a single chip. Its serial interface enables it to be packaged in an economical and space-saving 16-pin DIP. The AT76C10/E is especially suited for modems and data communications equipment where it can compensate for line gain variations and group delay distortions. In the E^2PROM version of the chip, the AT76C10E, a particular gain or delay configuration can be stored in the device's non-volatile memory and recalled later by the user.

The programmable gain and group delay responses are controlled and configured by a serial 7-bit configuration code. The purpose of this application note is to illustrate how this serial configuration can be accomplished in a microcomputer environment, more specifically, utilizing a microcontroller (the Intel 8031AH) to interface to the AT76C10/E. Such an interface enables the gain and delay responses to be changed or updated in real-time (for the AT76C10) as well as saved into the E^2PROM (for the AT76C10E).

As shown in Figure 1, the Intel 8031AH, an 8-bit latch, a transmission line receiver, and external memory form a complete and versatile system to generate control and data bits for the AT76C10/E. An RS-232C cable can connect this system to the serial port of a microcomputer (e.g. IBM PC) or TTY terminal. The serial port transmits data to the microcontroller, which, under software control, outputs them as serial bits to the AT76C10/E for controlling the gain and delay outputs as desired by the user. As will be explained below, an evaluation board implementing the system just described has been developed by Atmel Corporation following the guidelines in this application note.

The Hardware

The 8031AH has four 8-bit I/O ports: P0, P1, P2, and P3. Ports P0 and P2, however, are used for external memory addressing when external memory is present (as is the case here) and are thus unavailable as general-purpose I/O ports. This leaves all of the 8 bits of port P1 and five bits of port P3 available for I/O. P1.0, P1.1, and P1.2, are used to produce respectively, via software instructions, the signals $\overline{CS}$, $\overline{WE}$, and DIN necessary to program the AT76C10/E.

The 8-bit latch acts as the low-order address latch/data buffer for the signals between the P0 I/O port of the microcontroller and the external memory. The line receiver enables the microcontroller to receive data signals from the microcomputer or TTY terminal via the RS-232C link.

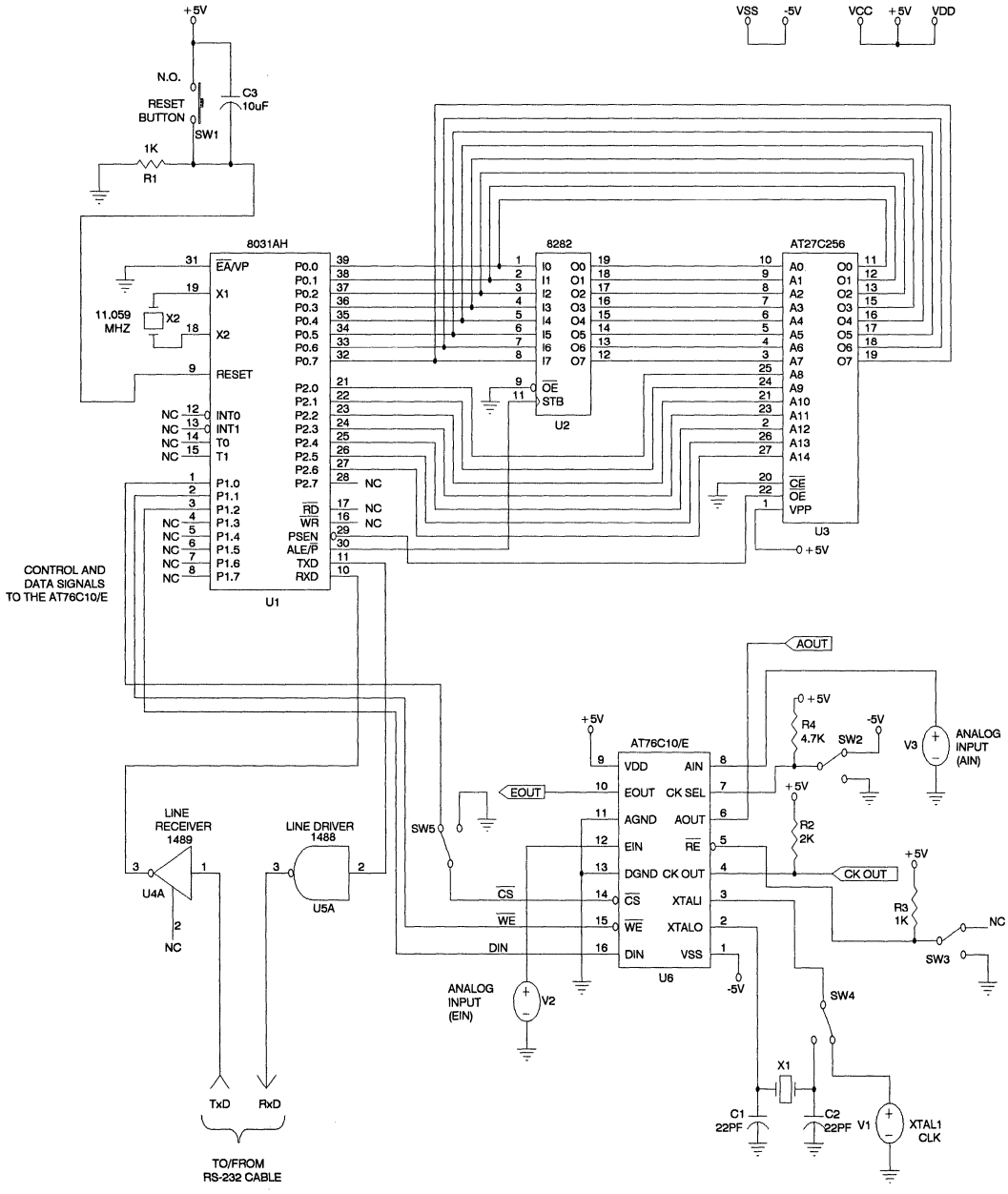
External memory consists of the AT27C256 EPROM, which houses the system software. This firmware directs the microcontroller to send out the necessary timing and data signals to configure the AT76C10/E. If additions or changes need to be made to the firmware code the AT27C256 can be easily erased via ultraviolet (UV) light and reprogrammed.

The Software

The software programs the 8031AH to generate the correct timing waveforms and to strobe desired data bit patterns into the AT76C10/E. This is achieved as illustrated by the programming flowchart in Figure 2.

First the serial port data register and timer 1 need to be initialized with proper values depending on desired transmission parameters and baud rate. A 9600-baud data transmission rate has been used in this application. As soon as the accumulator receives a character from the

Figure 1. Microcontroller Interface to the AT76C10/E



The Software (Continued)

keyboard the data is sent out bit by bit (LSB first) as data bits through the carry flag to the serial data input pin of the AT76C10/E. Appropriate delays and specific bit-manipulating instructions then control and synchronize the transitions of $\overline{CS}$ and $\overline{WE}$ with the data bits so that the writing waveforms conform to timing specifications defined in the device data sheet. Seven rising edges of $\overline{WE}$ strobe in a complete data word in a single write cycle.

The complete programming code is given in Figure 3. It directly implements the flowchart in Figure 2.

Using The AT76C10/E Evaluation Board

As previously mentioned, an evaluation board integrating the hardware and software subsystems covered in this application note is available from Atmel Corporation. This board includes a 5.25" disk (IBM-PC format) with gain/delay programming menus and is designed to enable the user to quickly and easily evaluate the functionality and performance of the AT76C10/E through a standard serial interface to an IBM PC or compatible computer. Through the board one can cycle through all the individual gain/delay steps in each of the two amplifiers and the group delay equalizer.

Figure 2. 8031 Programming Algorithm

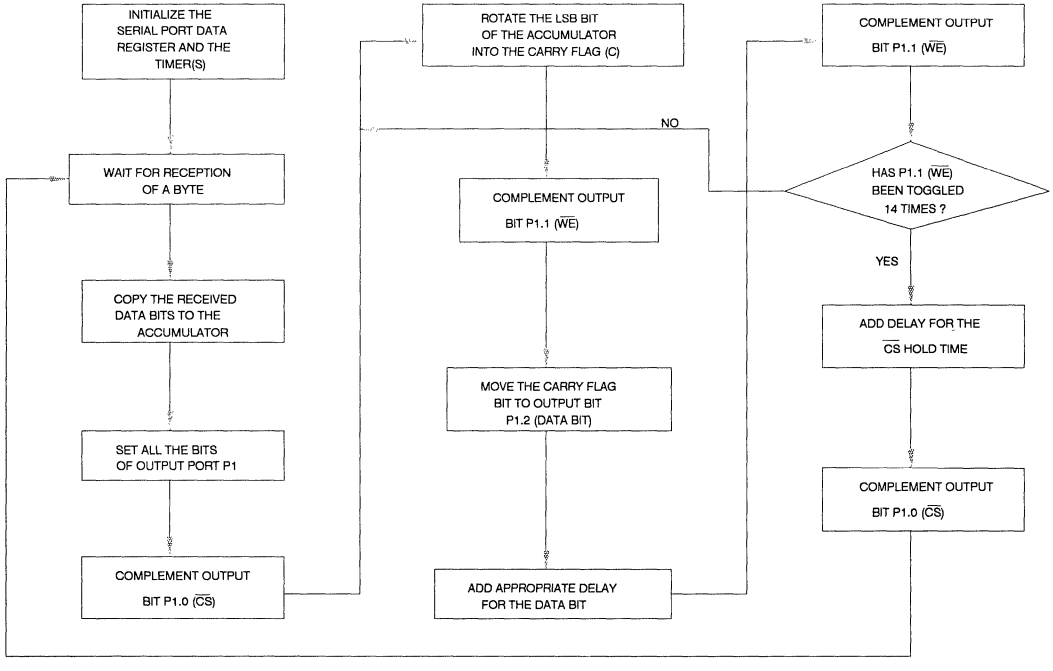


Figure 3. Program Code for AT76C10/E

```
;*****************************************************************
;*                  8031 program for the AT76C10/E               *
;*                       Evaluation Board                        *
;*                                                               *
;*                    Written by: Ta Wei (David) Lee             *
;*                    (C) 1988  ATMEL Corporation                *
;*****************************************************************
; 8031 control program for programming the AT76C10/E

; Constant Definitions:
ST          EQU     0FFH
RST         EQU     00H
DONE        EQU     14          ; 14 edges (falling and rising) for WEB
UARTMODE    EQU     01010000B   ; Set UART for: start, 8 data bits, stop
TMODLOAD    EQU     00100001B   ; Initialization word for the TMOD register
PCON        EQU     87H         ; Power Control Register
RELOAD      EQU     -3          ; Reload rate for 9600 baud
DATADLY     EQU     3H          ; Delay for a valid data bit
CSBHDLY     EQU     4H          ; Delay for CSB hold time
CSBIDLE     EQU     2           ; Delay before starting another CSB cycle
WEBIDLE     EQU     1           ; Delay before starting another WEB cycle

; Start of the program:
START:      ORG     00H
            LJMP    BEGIN

; Initialize the serial port data register for 8-bit UART mode:
BEGIN:      ORG     100H        ; Start of the code
            MOV     P3,#ST      ; Set the entire P3 I/O register
            MOV     PCON,#RST   ; No double baud rate wanted !
            MOV     SCON,#UARTMODE  ; Initialize the register

; Initialize timer 1 for an auto-reload rate of 32x9600 Hz.
; (T0 is used as a cascaded 16-bit counter.)
            MOV     TMOD,#TMODLOAD  ; Initialize the TMOD register
            MOV     TH1,#RELOAD ; Load the reload rate
            SETB    TR1         ; Turn Timer 1 ON

; Receive a character (byte) from the serial port:
RECEIVE:    JNB     RI,$        ; Wait for a character
            CLR     RI
            MOV     A,SBUF      ; Copy the byte to the accumulator

; Start the programming sequence:
; First cycle:
            MOV     R1,#RST     ; Reset the WEB counter
            MOV     P1,#ST      ; Set all bits of output port 1
            CPL     P1.0        ; Toggle CSB low
            AJMP    CONTINUE
MORE:       MOV     R2,#WEBIDLE ; Delay to generate the proper WEB high time
AGAIN1:     NOP
            DJNZ    R2,AGAIN1
CONTINUE:   RRC     A           ; Rotate the LSB bit of the accumulator
                                ; into the carry flag
            MOV     P1.2,C      ; Output one data bit
            CPL     P1.1        ; Toggle WEB
            INC     R1          ; Increment the WEB counter

; Add delay for a data bit to stabilize:
            MOV     R0,#DATADLY ; Load the delay into the counter
            DJNZ    R0,$        ; If not done yet, wait some more...

; Continue the data bit strobe cycle:
            CPL     P1.1        ; Toggle WEB
            INC     R1          ; Increment the WEB counter
            CJNE    R1,#DONE,MORE   ; Have 7 data bits been strobed in ?

; Add delay for the CSB hold time:
            MOV     R0,#CSBHDLY ; Load the delay for TCH
            DJNZ    R0,$        ; Delay finished ?

; End of one programming cycle:
            CPL     P1.0        ; Toggle CSB high
            MOV     R2,#CSBIDLE ; Waiting time for another cycle start...
AGAIN2:     NOP
            DJNZ    R2,AGAIN2
            AJMP    RECEIVE     ; Wait for another byte reception
            END     START       ; End of the program
```

CONTENTS

Section 11

Quality and Reliability

Continuous Improvement System

Introduction

When one of the recipients of the 1989 Malcolm Baldridge National Quality Award accepted his award, he stated: "We realize that we are in a race without a finish line." The goal is "to improve constantly and forever the system of production and service, to improve quality and productivity, and thus constantly decrease costs."

The journey of continuous improvement involves the use of various techniques such as statistical process control (SPC), statistical design of experiments (DOE), quality functional deployment (QFD), just in time (JIT), and many others.

The mind-set to use these techniques and to support the requirements of a continuous improvement system is just as important as the tools themselves. This is the key responsibility of the executives and managers and employees of Atmel Corporation.

Our use of these techniques *throughout* the Corporation and not just in manufacturing is proof of Atmel's commitment to continuous improvement. For example, it is just as important to properly enter a customer's order as it is to manufacture it. Errors in either process result in a dissatisfied customer.

Statistical Process Control (SPC)

SPC can be divided into either statistical or non-statistical techniques. Several statistical techniques involve the mathematical portrayal of data in graphical form to display whether a process is *in control* or *out of control* (see Figure 1). Although this sounds complicated, the procedures are very easy for operators to follow.

Other statistical techniques involve determining whether a process is capable of statistically meeting the specification limits or not. Usually called the capability indices of the process, these *figures of merit* for processes are becoming widely accepted.

The non-statistical techniques are steps in problem solving. These begin with methods to collect and portray data to achieve an understanding of the process.

Figure 1. Examples of process control charts

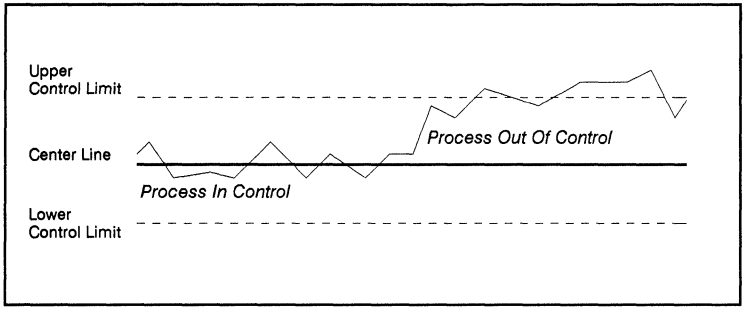
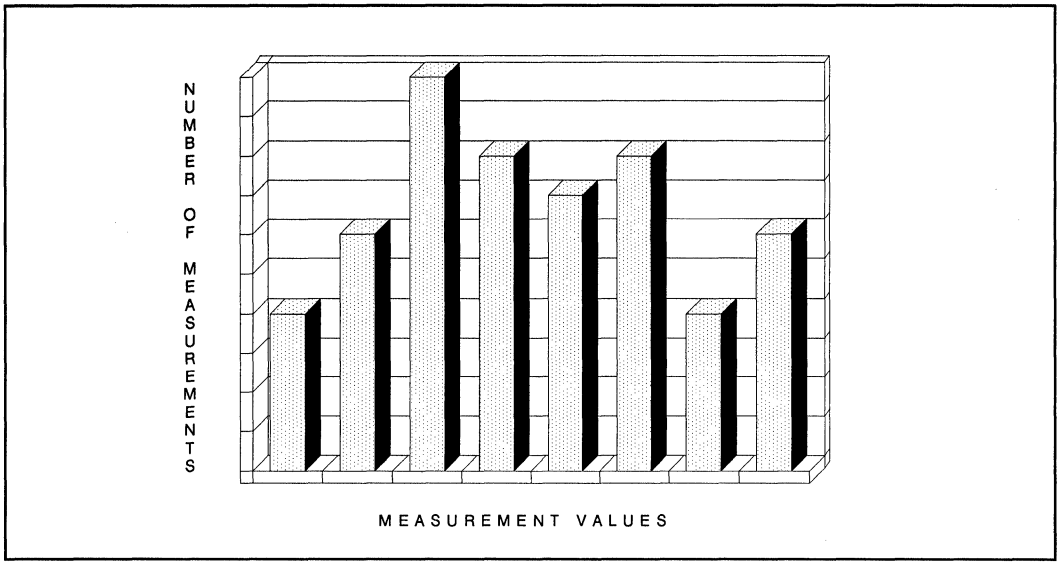


Figure 2. Example of a process histogram



Checklists, trend charts, and histograms are good examples of these techniques (see Figure 2).

The non-statistical problem solving techniques include the Pareto chart. The Pareto chart reduces the number of problems down to the *significant few* that contribute the majority of the problems.

Once those significant few are identified, the use of the Cause and Effect diagram identifies the probable causes of the problem and becomes the outline for solving it.

Statistical Design Of Experiments (DOE)

The DOE technique has been used for many years by the agricultural and chemical industries. Only recently has it made its presence felt in the *high-tech* industries.

It is perfectly suited to this industry because it has the capability to handle large numbers of variables simultaneously and to determine statistically significant variables, interactions between variables, and the amount of variation they can cause in a process or product.

When DOE is coupled with computer-aided design and process models, it can predict these relationships and outcomes without running actual experiments. This in turn reduces the time and cost of designing new products and processes or improving existing ones.

Quality Functional Deployment (QFD)

The best controlled and capable process is only as good as the product that is designed to go through it. If the design does not meet the customer's needs to begin with, there is nothing the process can do to improve it. And that is where QFD steps in.

QFD is a procedure which involves the customer in the definition and design of a product. The customer is a key member of the company team which includes marketing, design & development, manufacturing and quality departments.

The key to this technique is looking at the inter-relationships between critical variables controlled by each member of the QFD team early in the design process. Identifying and taking action on these variables enhances the design and insures that "glitches" are eliminated.

Just-In-Time (JIT)

Continuous improvement can achieve reduced production cycle times and and inventory levels. However, without a *system* to plan and oversee these reductions, the existing system may not adjust to the improvements. A JIT system insures that excess production time and inventory levels are reduced.

Consortium for Continuous Improvement

Atmel is a participating member of a consortium of major semiconductor companies. Its purpose is to create guidelines and workshops for implementing a continuous improvement system.

The consortium will publish a continuous improvement document as well as accompanying workshop materials.

Malcolm Baldridge National Quality Award

One of the best guides for company commitments towards continuous improvement lies within the criteria for the Baldridge Award. The Baldridge criteria are not a set of tools or methodologies for improvement, but rather an assessment of a company's continuous improvement system.

The major criteria evaluated by the Baldridge committee are:

- Customer Satisfaction
- Corporate Leadership
- Strategic Quality Planning
- Quality Assurance of Products and Services
- Quality Results
- Human Resource Utilization
- Information Analysis

Atmel's management team is integrating the Baldridge criteria into its continuous improvement system and the Company has announced that it will apply for the Baldridge Award.

Conclusion

Atmel is committed to the process of continuous improvement. This is most clearly displayed by its corporate-wide implementation of continuous improvement, its dedication to win the Baldridge Award, and its participation in the continuous improvement consortium.

An Executive Decision

Atmel's corporate goal is to meet or exceed our customers' requirements 100% of the time.

Atmel guarantees and tests product quality at all levels and all critical paths in the manufacturing process. Quality assurance and control are the responsibility of the executive staff reporting directly to the chief executive officer. The concern with quality begins with the initial product inception, and never ends. Atmel quality is critical for the entire life of any system that our products become a part of.

Design For Quality And Reliability

The Atmel design staff emphasizes quality and reliability throughout the design cycle. Design rules are established by experiment to insure manufacturability and reliable performance over time. All devices are designed with proprietary anti-latchup structures to eliminate the necessity of using epitaxial starting materials with their inherent higher defect densities. Special electro-static discharge circuits are incorporated to protect package pins during handling and insertion.

Each product family has specific quality and reliability issues that require special design consideration. Non-volatile memories that depend on charge storage must allow for the testing of charge retention to insure long term data retention. E^2PROM devices are electrically alterable, and additional circuits are incorporated to maintain data integrity during times of external signal instability (such as system power-up or failure). High performance CMOS analog designs depend on stable threshold voltage and transistor gains and must be designed to minimize manufacturing variations. Since operation frequency is a critical parameter in an EPLD device, Atmel incorporated two levels of metal interconnect into its process to allow the use of conservative transistor technology.

Eliminating inadvertent writes might be considered a system design issue, but Atmel designed write protect features into its E^2PROM family. Active on board circuits sense VCC and prevent writes for 5ms after VCC has increased above 3.8 volts. Three line write control (CHIP ENABLE, WRITE ENABLE, AND OUTPUT ENABLE must all be held in their active states to initiate a write) and noise pulse filters (pulses less than 15ns in duration are ignored) on the control lines are incorporated to prevent false write commands. A software key (user activated) can require that a specific sequence of addresses and data be issued to the chip before a write is activated.

The " Bathtub " Failure Curve

It is well known that integrated circuits exhibit a classical "bathtub" failure curve (Figure 11.1). Early relatively high failure rates (Phase 1) are due to process anomalies and are found during Atmel's outgoing production test. Devices which are shipped to customers then exhibit a long period of stable very low failure rates (Phase 2) which are random in time and occurrence. Finally, other failure modes will become predominant (such as metal electromigration, voltage threshold shifts, or moisture related corrosion) and the failure rate will again increase as the chip "wears out" (Phase 3).

Atmel production test flows have been developed to insure that Phase 1 failures are found before shipment. Special test structures are incorporated on chip which correlate to these failures. Specific temperature, voltage, and time dependant tests are performed to guarantee the quality of the outgoing products.

Quality and Reliability Assurance

Atmel guarantees non-volatile data retention for greater than 10 years. A high temperature bake has been shown to be a good stress test for data retention[1], and 100% of Atmel's products are tested in this way. In addition, periodic 1000 hour monitor tests routinely show retention life times in excess of 50 years.

Since E^2PROM memory circuits have high transistor densities, Phase 2 failures are often dominated by write cycle induced oxide integrity faults. Atmel has incorporated internal error correction into its E^2PROM product line to minimize this type of failure. Each byte (8 bits) of data is internally stored as a 12 bit word generated using a modified Hamming code, and any single bit failure is automatically corrected during the read cycle. Failure rates for chips incorporating internal error correction are improved dramatically. For example, at the point where the cumulative failure rate for a 64K bit uncorrected E^2PROM has reached 0.1 (10% of the chips have exhibited failures), an AT28C64 corrected circuit would exhibit a failure rate of only 2 parts per million.

Phase 3 failure modes are dependant on the system application of the specific circuit. Long term reliability studies and failure analyses are used to identify potential failure modes and control them through processing, layout rules, packaging, and design. To illustrate, all E^2PROM's exhibit a finite number of write cycles (defined as endurance) due to electrons slowly becoming trapped in the tunneling oxide. The number of write cycles that occur before this failure mode predominates is dependant on such things as the cleanliness of the process and the thickness and integrity of the oxide film. The Atmel process is based on a "thin" (less than 100 Angstroms) tunnel oxide to minimize the effects of trapping and thus increase the number of cycles.

Manufacturing For Quality and Reliability

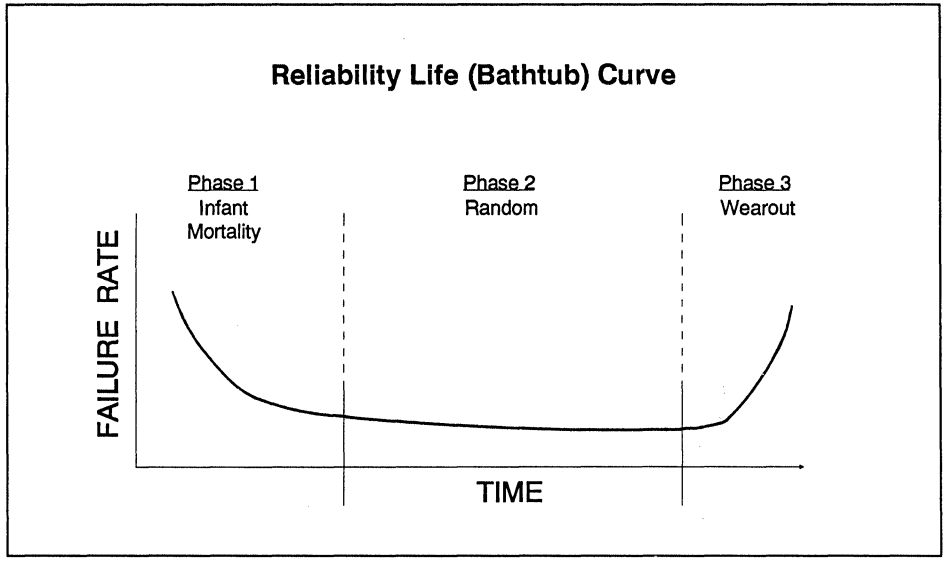
All Atmel products are manufactured to the standards of Military Standard 883C, Class B through wafer fabrication and assembly as shown in Figure 11.2. The products then follow different test flows that correspond to the different classes of products that Atmel offers.

(1) Commercial Grade. This product follows Test Flow (1), Figure 11.3 and is guaranteed over the temperature range of 0°C to +70°C.

(2) Industrial Grade. This product follows Test Flow (2), Figure 11.4 and is guaranteed over the temperature range of -40°C to +85°C.

(3) Military Grade. Three classes of military products are offered by Atmel (MIL-STD-883C, Class B standard product, Standard Military Drawing (SMD) product, and Source Control Drawing (SCD) product). The Military Section discusses test procedures for these products in detail.

Figure 11.1



Note: 1. R. E. Shiner, J. M. Caywood, B. L. Euzent, "Data Retention in EPROMs", Proceedings International Reliability Physics Symposium 18, (1980), P. 238.

The Payoff

The focus of Atmel's quality and reliability efforts is the customer and his system. The common goals of highest field reliability and lowest system life cycle cost are achieved through close working relationships using programs such as "ship to stock", "just in time", and "failure trend analysis". Under these programs incoming Atmel circuits go straight to the customers' workfloors – they do not go through an incoming inspection cycle. This, of course, lowers manufacturing costs and is a testimony of the trust that has been established. In addition, long term field failures are analyzed so that corrective action plans can be implemented. Atmel has developed programs such as these with many major customers.

Figure 11.2

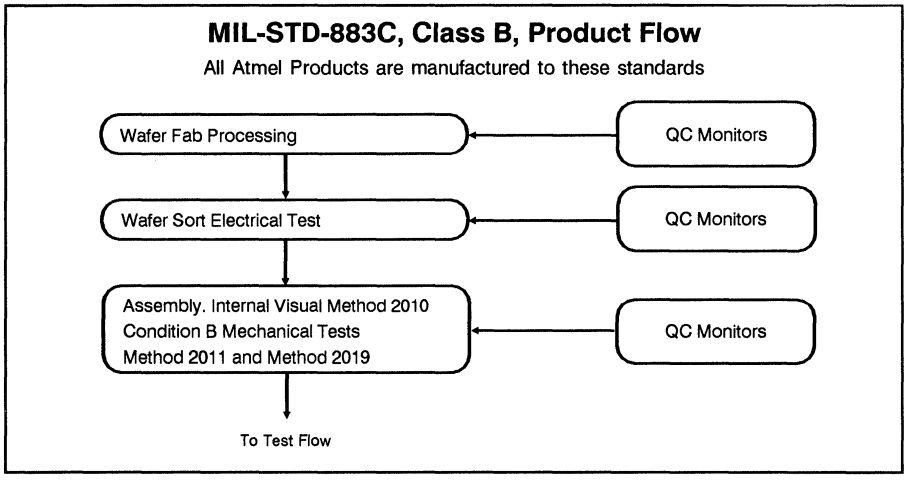


Figure 11.3

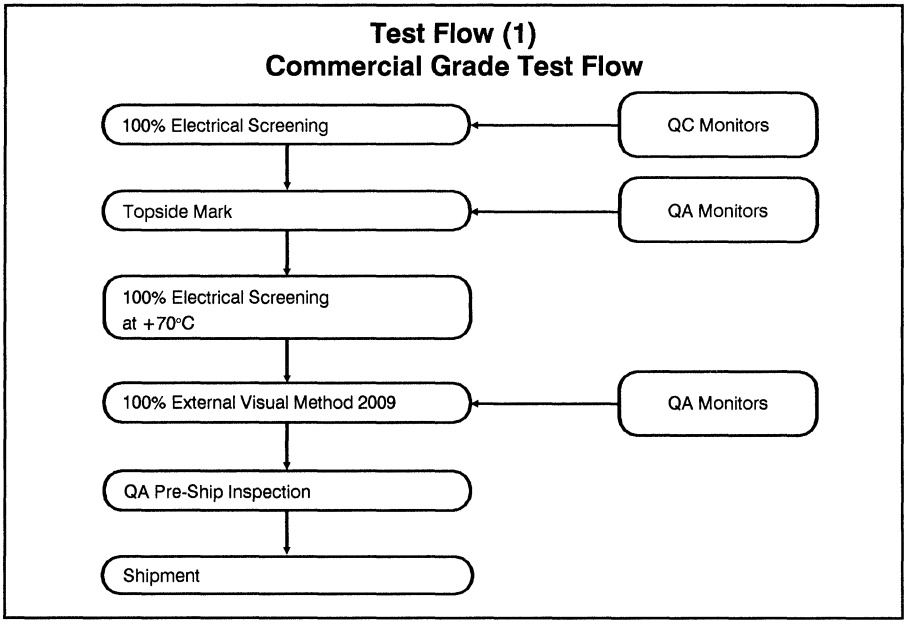
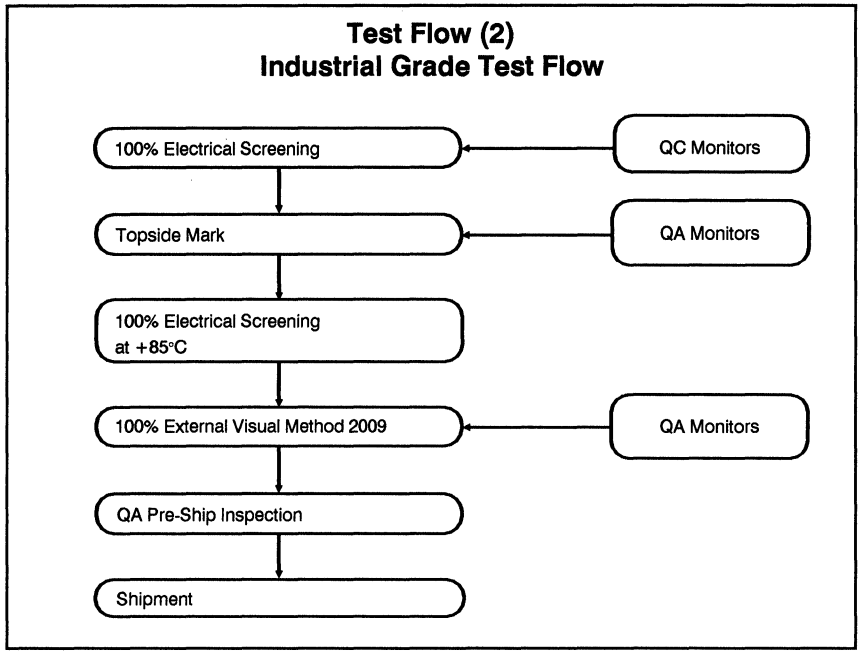


Figure 11.4


Test Flow (2)
Industrial Grade Test Flow
100% Electrical Screening
QC Monitors
Topside Mark
QA Monitors
100% Electrical Screening
at +85°C
100% External Visual Method 2009
QA Monitors
QA Pre-Ship Inspection
Shipment

CONTENTS

12

Program Overview

All Atmel products are manufactured to the standards of Military Standard 883C, Class B through wafer fabrication and assembly, as shown in Figure 12.1. Military products then follow the test flow shown in Figure 12.2.

Quality Conformance Inspection Data

As shown in Table 12.1, Atmel performs Groups A, B, C, and D tests in compliance with Military Standard 883C, Class B. Groups A and B are performed on each inspection lot for MIL-STD-883C, Class B products. Groups C and D are periodic inspections as defined in MIL-M-38510. Pre-conditioning data, Group A, Group B, Group C, and Group D generic data are available for customer procurement.

Military Product Classes

Atmel offers three classes of military products:

(1) MIL-STD-883C, Class B products are fully compliant to MIL-STD-883C Paragraph 1.2.1, with no exceptions. A Certificate of Compliance (C of C) is enclosed with each shipment of MIL-STD-883C, Class B product.

(2) Standard Military Drawing (SMD) products are fully compliant to MIL-STD-883C Paragraph 1.2.1 with optional additional tests as specified in the applicable Standard Military Drawing as approved by DESC. Table 12.2 lists currently approved Atmel SMD parts, organized by Atmel part type. Table 12.3 lists currently approved Atmel SMD parts, organized by SMD number.

(3) Source Control Drawing (SCD) products are fully compliant to MIL-STD-883C Paragraph 1.2.1 with optional additional tests as specified by the specific customer specification. Atmel must review and accept a customer Source Control Drawing prior to order acceptance to assure compliance.

Figure 12.1

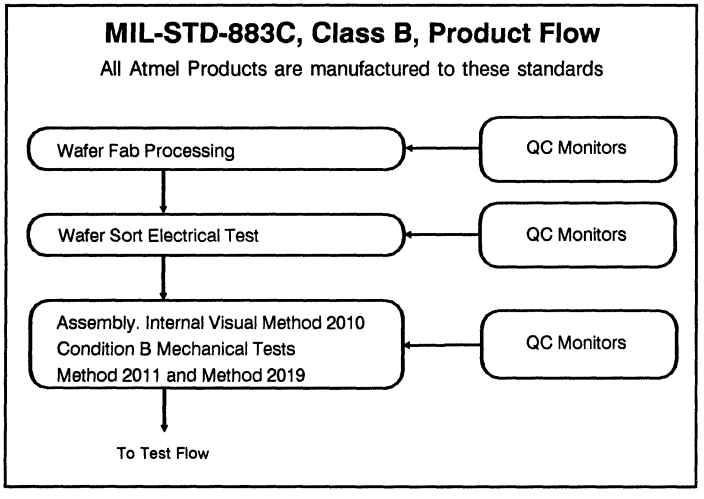


Figure 12.2

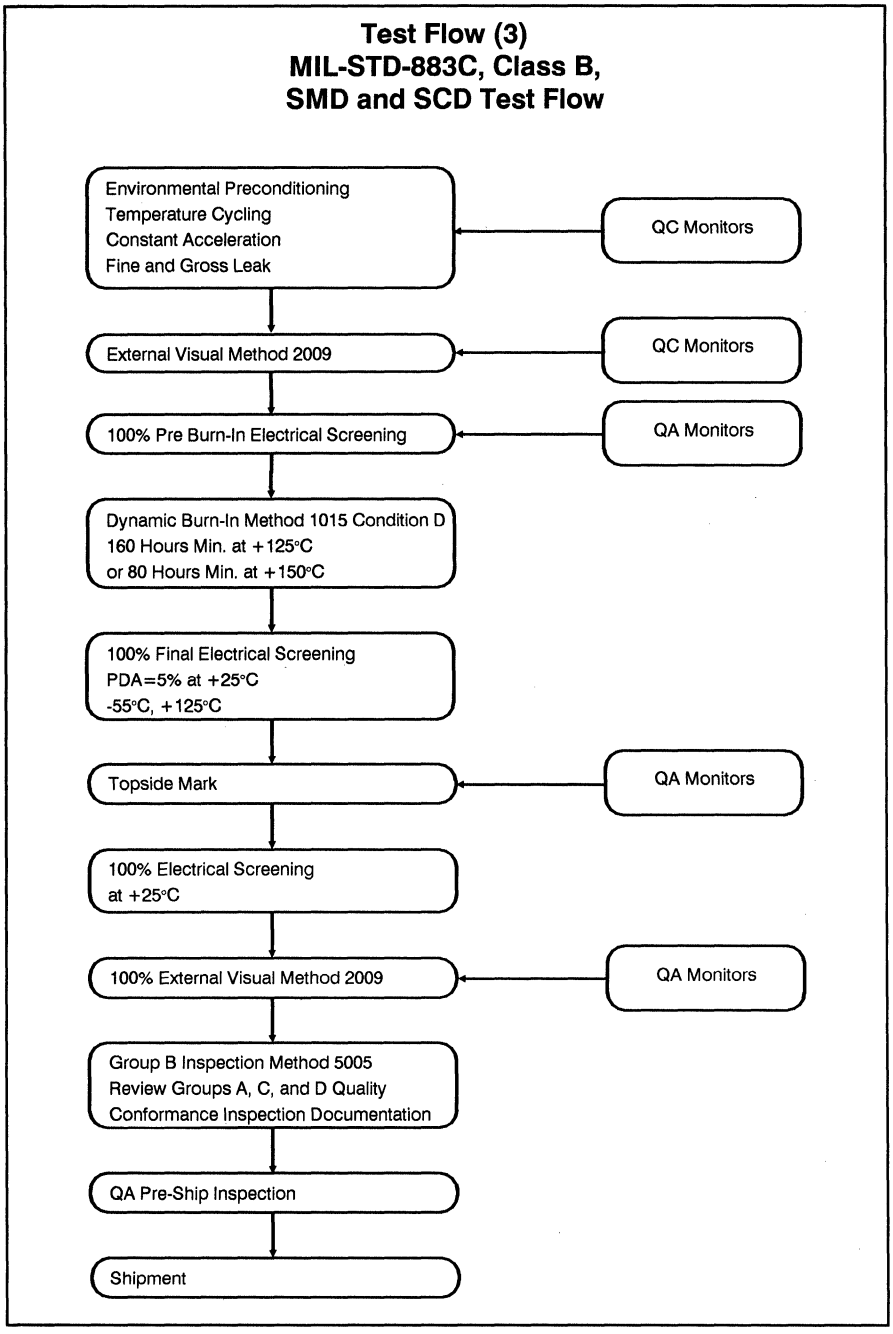

Test Flow (3)
MIL-STD-883C, Class B,
SMD and SCD Test Flow
Environmental Preconditioning
Temperature Cycling
Constant Acceleration
Fine and Gross Leak
QC Monitors
External Visual Method 2009
QC Monitors
100% Pre Burn-In Electrical Screening
QA Monitors
Dynamic Burn-In Method 1015 Condition D
160 Hours Min. at +125°C
or 80 Hours Min. at +150°C
100% Final Electrical Screening
PDA=5% at +25°C
-55°C, +125°C
Topside Mark
QA Monitors
100% Electrical Screening
at +25°C
100% External Visual Method 2009
QA Monitors
Group B Inspection Method 5005
Review Groups A, C, and D Quality
Conformance Inspection Documentation
QA Pre-Ship Inspection
Shipment

Table 12.1 Military Standard 883C, Class B Tests

Group A: Electrical Tests

Performed On Each Lot

Screen	MIL-STD-883C Method 5005 Table 1 Subgroups	LPTD
Static Tests at +25°C	1	2
Static Tests at +125°C	2	2
Static Tests at -55°C	3	2
Dynamic Tests at +25°C	4	2
Function Tests at +25°C	7	2
Function Tests at +125°C	8A	2
Function Tests at -55°C	8B	2
Switching Tests at +25°C	9	2
Switching Tests at +125°C	10	2
Switching Tests at -55°C	11	2

Group B: Assembly Integrity Tests

Performed On Each Lot

Screen	MIL-STD-883C Test Method	Conditions	Quantity (Accept No. or LTPD)
SUBGROUP 2 Resistance to Solvents	2015	Top and Bottom Marks	4(0)
SUBGROUP 3 Solderability	2003	+245°C +/-5°C	10
SUBGROUP 5 Bond Strength	2011	Condition D	15

Group C: Die Related Tests

Performed Per MIL-STD-883C Paragraph 1.2.1

Screen	MIL-STD-883C Test Method	Conditions	LTPD
SUBGROUP 1			
Steady State Life Test	1005	Condition D	5
End Point Electricals	5005	Subgroups 1, 2, 3, 7-11	15

Table 12.1 Military Standard 883C, Class B Tests *(continued)*

Group D: Package Related Tests

Performed Per MIL-STD-883C Paragraph 1.2.1
By Package Type, Assembly Location, and Exterior Lead Finish

Screen	MIL-STD-883C Test Method	Conditions	Quantity (Accept No. or LTPD)
SUBGROUP 1			
Physical Dimensions	2016	MIL-M-38510, Appendix C	15
SUBGROUP 2			15
Lead Integrity	2004	Condition B2 (Condition D for LCC)	
Seal: Fine	1014	Conditon A or B	
Seal:Gross	1014	Condition C	
SUBGROUP 3			15
Thermal Shock	1011	Condition B, 15 Cycles	
Temperature Cycling	1010	Condition C, 100 Cycles	
Moisture Resistance	1004	10 Cycles	
End Point Electricals	5005	Subgroups 1, 7, 9 (within 42 hrs)	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination		Per Visual of Method 1004 and 1010	
SUBGROUP 4			15
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E, 30 KG., Y1	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination	1010		
End Point Electricals	5005	Subgroups 1, 7, 9	
SUBGROUP 5			15
Salt Atmosphere	1009	Condition A	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination		Per Visual of Method 1009	
SUBGROUP 6			3 (0) or 5 (1)
Internal Water Vapor Content	1018	5,000 PPM Maximum Water Content at 100°C	
SUBGROUP 7			15
Adhesion of Lead Finish	2025	Glass Frit Seal Only (LTPD for Number of Leads)	
SUBGROUP 8			5 (0)
Lid Torque	2024	Glass Frit Seal Only	

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT22V10

Generic Number	Standard Military Drawing Number				Description	
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
C22V10	5962-87539	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-87539	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-87539	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-87539	04	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-87539 **01 KX**		AT22V10-25YM/883
	5962-87539 **01 LX**		AT22V10-25DM/883
	5962-87539 **01 3X**		AT22V10-25LM/883
	5962-87539 **02 KX**		AT22V10-30YM/883
	5962-87539 **02 LX**		AT22V10-30DM/883
	5962-87539 **02 3X**		AT22V10-30LM/883
	5962-87539 **03 KX**		AT22V10-40YM/883
	5962-87539 **03 LX**		AT22V10-40DM/883
	5962-87539 **03 3X**		AT22V10-40LM/883
	5962-87539 **04 LX**		AT22V10-20DM/883
	5962-87539 **04 3X**		AT22V10-20LM/883

Case Outline	
K	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerdip)
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT22V10L

Generic Number	Standard Military Drawing Number				Description	
C22V10L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88724	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88724	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-88724	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-88724	04	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-88724 **01 KX**		AT22V10L-25YM/883
	5962-88724 **01 LX**		AT22V10L-25DM/883
	5962-88724 **01 3X**		AT22V10L-25LM/883
	5962-88724 **02 KX**		AT22V10L-30YM/883
	5962-88724 **02 LX**		AT22V10L-30DM/883
	5962-88724 **02 3X**		AT22V10L-30LM/883
	5962-88724 **03 KX**		AT22V10L-40YM/883
	5962-88724 **03 LX**		AT22V10L-40DM/883
	5962-88724 **03 3X**		AT22V10L-40LM/883
	5962-88724 **04 KX**		AT22V10L-20YM/883
	5962-88724 **04 LX**		AT22V10L-20DM/883
	5962-88724 **04 3X**		AT22V10L-20LM/883

Case Outline	
K	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT22V10 OTP

Generic Number	Standard Military Drawing Number				Description	
C22V10 OTP	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88670	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88670	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-88670	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-88670	04	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-88670 **01 KX**		AT22V10-25FM/883
	5962-88670 **01 LX**		AT22V10-25GM/883
	5962-88670 **01 3X**		AT22V10-25NM/883
	5962-88670 **02 KX**		AT22V10-30FM/883
	5962-88670 **02 LX**		AT22V10-30GM/883
	5962-88670 **02 3X**		AT22V10-30NM/883
	5962-88670 **03 KX**		AT22V10-40FM/883
	5962-88670 **03 LX**		AT22V10-40GM/883
	5962-88670 **03 3X**		AT22V10-40NM/883
	5962-88670 **04 KX**		AT22V10-20FM/883
	5962-88670 **04 LX**		AT22V10-20GM/883
	5962-88670 **04 3X**		AT22V10-20NM/883

Case Outline	
K	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
L	24D3, 24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
3	28L, 28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT22V10L OTP

Generic Number	Standard Military Drawing Number				Description	
C22V10L OTP	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-89755	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-89755	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-89755	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-89755 **01 KX**		AT22V10L-25FM/883
	5962-89755 **01 LX**		AT22V10L-25GM/883
	5962-89755 **01 3X**		AT22V10L-25NM/883
	5962-89755 **02 KX**		AT22V10L-30FM/883
	5962-89755 **02 LX**		AT22V10L-30GM/883
	5962-89755 **02 3X**		AT22V10L-30NM/883
	5962-89755 **03 KX**		AT22V10L-40FM/883
	5962-89755 **03 LX**		AT22V10L-40GM/883
	5962-89755 **03 3X**		AT22V10L-40NM/883

Case Outline	
K	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
L	24D3, 24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
3	28L, 28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

ATV750						
Generic Number	Standard Military Drawing Number				Description	
V750	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88726	01	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-88726	02	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	35
	Example:	Atmel Order Number		Atmel Cage No. 1FN41	Atmel Similar Part Number	
		5962-88726 **01 LX**			ATV750-40DM/883	
		5962-88726 **01 3X**			ATV750-40LM/883	
		5962-88726 **02 LX**			ATV750-35DM/883	
		5962-88726 **02 3X**			ATV750-35LM/883	

Case Outline	
L	24DW3, 24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT27HC64L

Generic Number	Standard Military Drawing Number				Description	
27HC64L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-85102	04	Y, Z	X, A, C	8Kx8 EPROM	90
	Example:	Atmel Order Number		Atmel Cage No. 1FN41	Atmel Similar Part Number	
		5962-85102 **04 YX**			AT27HC64L-90DM/883	
		5962-85102 **04 ZX**			AT27HC64L-90LM/883	

Case Outline	
Y	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Z	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT27C256R

Generic Number	Standard Military Drawing Number				Description	
27C256R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-86063	01	X, Y	X, A, C	32Kx8 EPROM	200
	5962-86063	02	X, Y	X, A, C	32Kx8 EPROM	250
	5962-86063	03	X, Y	X, A, C	32Kx8 EPROM	300
	5962-86063	04	X, Y	X, A, C	32Kx8 EPROM	170
	5962-86063	05	X, Y	X, A, C	32Kx8 EPROM	150

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-86063 **01 XX**		AT27C256R-20DM/883
	5962-86063 **01 YX**		AT27C256R-20LM/883
	5962-86063 **02 XX**		AT27C256R-25DM/883
	5962-86063 **02 YX**		AT27C256R-25LM/883
	5962-86063 **03 XX**		AT27C256R-30DM/883
	5962-86063 **03 YX**		AT27C256R-30LM/883
	5962-86063 **04 XX**		AT27C256R-17DM/883
	5962-86063 **04 YX**		AT27C256R-17LM/883
	5962-86063 **05 XX**		AT27C256R-15DM883
	5962-86063 **05 YX**		AT27C256R-15LM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT27HC256

Generic Number	Standard Military Drawing Number				Description	
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
27HC256	5962-86063	08	X, Y	X, A, C	32K x 8 EPROM	70

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-86063 **08 XX**		AT27HC256-70DM/883
	5962-86063 **08 YX**		AT27HC256-70LM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

AT27HC256L

Generic Number	Standard Military Drawing Number				Description	
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
27HC256L	5962-86063	06	X, Y	X, A, C	32K x 8 EPROM	120
	5962-86063	07	X, Y	X, A, C	32K x 8 EPROM	90

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-86063 **06 XX**		AT27HC256L-12DM/883
	5962-86063 **06 YX**		AT27HC256L-12LM/883
	5962-86063 **07 XX**		AT27HC256L-90DM/883
	5962-86063 **07 YX**		AT27HC256L-90LM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT27C512R

Generic Number	Standard Military Drawing Number				Description	
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
27C512R	5962-87648	01	X, Y	X, A, C	64Kx8 EPROM	150
	5962-87648	02	X, Y	X, A, C	64Kx8 EPROM	200
	5962-87648	03	X, Y	X, A, C	64Kx8 EPROM	250
	5962-87648	04	X, Y	X	64Kx8 EPROM	120

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-87648 **01 XX**		AT27C512R-15DM/883
	5962-87648 **01 YX**		AT27C512R-15LM/883
	5962-87648 **02 XX**		AT27C512R-20DM/883
	5962-87648 **02 YX**		AT27C512R-20LM/883
	5962-87648 **03 XX**		AT27C512R-25DM/883
	5962-87648 **03 YX**		AT27C512R-25LM/883
	5962-87648 **04 XX**		AT27C512R-12DM/883
	5962-87648 **04 YX**		AT27C512R-12LM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT27HC641

Generic Number	Standard Military Drawing Number				Description	
27HC641	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-87515	01	J, K, 3	X, A, C	8Kx8 [UV] PROM	45
	5962-87515	02	J, K, 3	X, A, C	8Kx8 [UV] PROM	55
	5962-87515	03	J, K, 3	X, A, C	8Kx8 [UV] PROM	70
	5962-87515	04	J, K, 3	X, A, C	8Kx8 [UV] PROM	90

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-87515 **01 JX**		AT27HC641-45DM/883
	5962-87515 **01 KX**		AT27HC641-45FM/883
	5962-87515 **01 3X**		AT27HC641-45LM/883
	5962-87515 **02 JX**		AT27HC641-55DM/883
	5962-87515 **02 KX**		AT27HC641-55FM/883
	5962-87515 **02 3X**		AT27HC641-55LM/883
	5962-87515 **03 JX**		AT27HC641-70DM/883
	5962-87515 **03 KX**		AT27HC641-70FM/883
	5962-87515 **03 3X**		AT27HC641-70LM/883
	5962-87515 **04 JX**		AT27HC641-90DM/883
	5962-87515 **04 KX**		AT27HC641-90FM/883
	5962-87515 **04 3X**		AT27HC641-90LM/883

Case Outline	
J	24DW6, 24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
K	24FW, 24 Lead, Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT27HC642

Generic Number	Standard Military Drawing Number				Description	
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
27HC642	5962-87515	01	L	X, A, C	8Kx8 [UV] PROM	45
	5962-87515	02	L	X, A, C	8Kx8 [UV] PROM	55
	5962-87515	03	L	X, A, C	8Kx8 [UV] PROM	70
	5962-87515	04	L	X, A, C	8Kx8 [UV] PROM	90

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-87515 **01 LX**		AT27HC642-45DM/883
	5962-87515 **02 LX**		AT27HC642-55DM/883
	5962-87515 **03 LX**		AT27HC642-70DM/883
	5962-87515 **04 LX**		AT27HC642-90DM/883

Case Outline	
L	24DW3, 24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT28C64

Generic Number	Standard Military Drawing Number				Description				
28C64	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-87514	13	U, X, Y	X, A, C	8Kx8 E^2PROM Rdy/$\overline{Busy}$	Byte	350	1	10K
	5962-87514	14	U, X, Y	X, A, C	8Kx8 E^2PROM Rdy/$\overline{Busy}$	Byte	300	1	10K
	5962-87514	15	U, X, Y, Z	X, A, C	8Kx8 E^2PROM Rdy/$\overline{Busy}$	Byte	250	1	10K
	5962-87514	16	U, X, Y	X, A, C	8Kx8 E^2PROM Rdy/$\overline{Busy}$	Byte	200	1	10K
	5962-87514	17	U, X, Y	X, A, C	8Kx8 E^2PROM Rdy/$\overline{Busy}$	Byte	150	1	10K

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-87514 **13 UX**		AT28C64-35KM/883
	5962-87514 **13 XX**		AT28C64-35DM/883
	5962-87514 **13 YX**		AT28C64-35LM/883
	5962-87514 **14 UX**		AT28C64-30KM/883
	5962-87514 **14 XX**		AT28C64-30DM/883
	5962-87514 **14 YX**		AT28C64-30LM/883
	5962-87514 **15 UX**		AT28C64-25KM/883
	5962-87514 **15 XX**		AT28C64-25DM/883
	5962-87514 **15 YX**		AT28C64-25LM/883
	5962-87514 **15 ZX**		AT28C64-25FM/883
	5962-87514 **16 UX**		AT28C64-20KM/883
	5962-87514 **16 XX**		AT28C64-20DM/883
	5962-87514 **16 YX**		AT28C64-20LM/883
	5962-87514 **17 UX**		AT28C64-15KM/883
	5962-87514 **17 XX**		AT28C64-15DM/883
	5962-87514 **17 YX**		AT28C64-15LM/883

Case Outline	
U	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT28C64X

Generic Number	Standard Military Drawing Number				Description				
28C64X	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-87514	18	U, X, Y	X, A, C	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	350	1	10K
	5962-87514	19	U, X, Y	X, A, C	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
	5962-87514	20	U, X, Y, Z	X, A, C	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
	5962-87514	21	U, X, Y	X, A, C	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
	5962-87514	22	U, X, Y	X, A, C	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-87514 **18 UX**		AT28C64X-35KM/883
	5962-87514 **18 XX**		AT28C64X-35DM/883
	5962-87514 **18 YX**		AT28C64X-35LM/883
	5962-87514 **19 UX**		AT28C64X-30KM/883
	5962-87514 **19 XX**		AT28C64X-30DM/883
	5962-87514 **19 YX**		AT28C64X-30LM/883
	5962-87514 **20 UX**		AT28C64X-25KM/883
	5962-87514 **20 XX**		AT28C64X-25DM/883
	5962-87514 **20 YX**		AT28C64X-25LM/883
	5962-87514 **20 ZX**		AT28C64X-25FM/883
	5962-87514 **21 UX**		AT28C64X-20KM/883
	5962-87514 **21 XX**		AT28C64X-20DM/883
	5962-87514 **21 YX**		AT28C64X-20LM/883
	5962-87514 **22 UX**		AT28C64X-15KM/883
	5962-87514 **22 XX**		AT28C64X-15DM/883
	5962-87514 **22 YX**		AT28C64X-15LM/883

Case Outline

U	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish

X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT28PC64

Generic Number	Standard Military Drawing Number				Description				
28PC64	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-87514	06	U, X, Y	X, A, C	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	2	10K
	5962-87514	07	U, X, Y	X, A, C	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	2	10K
	5962-87514	08	U, X, Y	X, A, C	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	2	10K
	5962-87514	09	U, X, Y	X, A, C	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	2	10K

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-87514 **06 UX**		AT28PC64-35KM/883
	5962-87514 **06 XX**		AT28PC64-35DM/883
	5962-87514 **06 YX**		AT28PC64-35LM/883
	5962-87514 **07 UX**		AT28PC64-30KM/883
	5962-87514 **07 XX**		AT28PC64-30DM/883
	5962-87514 **07 YX**		AT28PC64-30LM/883
	5962-87514 **08 UX**		AT28PC64-25KM/883
	5962-87514 **08 XX**		AT28PC64-25DM/883
	5962-87514 **08 YX**		AT28PC64-25LM/883
	5962-87514 **09 UX**		AT28PC64-20KM/883
	5962-87514 **09 XX**		AT28PC64-20DM/883
	5962-87514 **09 YX**		AT28PC64-20LM/883

Case Outline	
U	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT28HC64L

Generic Number	Standard Military Drawing Number				Description				
28HC64L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-87514	10	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	2	10K
	5962-87514	11	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	2	10K
	5962-87514	12	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	70	2	10K

Example:	Atmel Order Number	Atmel Cage No. 1 FN41	Atmel Similar Part Number
	5962-87514 **10 UX**		AT28HC64L-12KM/883
	5962-87514 **10 XX**		AT28HC64L-12DM/883
	5962-87514 **10 YX**		AT28HC64L-12LM/883
	5962-87514 **11 UX**		AT28HC64L-90KM/883
	5962-87514 **11 XX**		AT28HC64L-90DM/883
	5962-87514 **11 YX**		AT28HC64L-90LM/883
	5962-87514 **12 UX**		AT28HC64L-70KM/883
	5962-87514 **12 XX**		AT28HC64L-70DM/883
	5962-87514 **12 YX**		AT28HC64L-70LM/883

Case Outline	
U	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT28C256

Generic Number	Standard Military Drawing Number				Description				
28C256	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-88525	01	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
	5962-88525	02	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
	5962-88525	03	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
	5962-88525	04	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
	5962-88525	06	X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-88525 **01 UX**		AT28C256-35UM/883
	5962-88525 **01 XX**		AT28C256-35DM/883
	5962-88525 **01 YX**		AT28C256-35LM/883
	5962-88525 **01 ZX**		AT28C256-35FM/883
	5962-88525 **02 UX**		AT28C256-30UM/883
	5962-88525 **02 XX**		AT28C256-30DM/883
	5962-88525 **02 YX**		AT28C256-30LM/883
	5962-88525 **02 ZX**		AT28C256-30FM/883
	5962-88525 **03 UX**		AT28C256-25UM/883
	5962-88525 **03 XX**		AT28C256-25DM/883
	5962-88525 **03 YX**		AT28C256-25LM/883
	5962-88525 **03 ZX**		AT28C256-25FM/883
	5962-88525 **04 UX**		AT28C256-20UM/883
	5962-88525 **04 XX**		AT28C256-20DM/883
	5962-88525 **04 YX**		AT28C256-20LM/883
	5962-88525 **04 ZX**		AT28C256-20FM/883
	5962-88525 **06 XX**		AT28C256-15DM/883
	5962-88525 **06 YX**		AT28C256-15LM/883
	5962-88525 **06 ZX**		AT28C256-15FM/883

Case Outline

U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish

X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT28C256E

Generic Number	Standard Military Drawing Number				Description				
28C256E	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-88525	05	X, Y, Z	X, A, C	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
	Example:	Atmel Order Number		Atmel Cage No. 1FN41		Atmel Similar Part Number			
		5962-88525 **05 XX**				AT28C256E-25DM/883			
		5962-88525 **05 YX**				AT28C256E-25LM/883			
		5962-88525 **05 ZX**				AT28C256E-25FM/883			

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT28C256F

Generic Number	Standard Military Drawing Number				Description				
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Function End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
28C256F	5962-88525	07	X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-88525 **07 XX**		AT28C256F-15DM/883
	5962-88525 **07 YX**		AT28C256F-15LM/883
	5962-88525 **07 ZX**		AT28C256F-15FM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

AT28HC256

Generic Number	Standard Military Drawing Number				Description				
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
28HC256	5962-88634	03	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	10	10K

Example:	Atmel Order Number	Atmel Cage No. 1FN41	Atmel Similar Part Number
	5962-88634 **03 UX**		AT28HC256-90UM/883
	5962-88634 **03 XX**		AT28HC256-90DM/883
	5962-88634 **03 YX**		AT28HC256-90LM/883
	5962-88634 **03 ZX**		AT28HC256-90FM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT28HC256F

Generic Number	Standard Military Drawing Number				Description				
28HC256F	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-88634	04	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	3	10K
	Example:	Atmel Order Number		Atmel Cage No. 1FN41		Atmel Similar Part Number			
		5962-88634 **04 UX**				AT28HC256F-90UM/883			
		5962-88634 **04 XX**				AT28HC256F-90DM/883			
		5962-88634 **04 YX**				AT28HC256F-90LM/883			
		5962-88634 **04 ZX**				AT28HC256F-90FM/883			

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT28HC256L

Generic Number	Standard Military Drawing Number				Description				
28HC256L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-88634	01	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	10	10K
	Example:	Atmel Order Number		Atmel Cage No. 1FN41		Atmel Similar Part Number			
		5962-88634 **01 UX**				AT28HC256L-12UM/883			
		5962-88634 **01 XX**				AT28HC256L-12DM/883			
		5962-88634 **01 YX**				AT28HC256L-12LM/883			
		5962-88634 **01 ZX**				AT28HC256L-12FM/883			

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.2 - ATMEL SMD Part Types, Listed by ATMEL Part Number

AT28HC256LF

Generic Number	Standard Military Drawing Number				Description				
28HC256LF	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
	5962-88634	02	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	3	10K
	Example:	Atmel Order Number		Atmel Cage No. 1FN41		Atmel Similar Part Number			
		5962-88634 **02 UX**				AT28HC256LF-12UM/883			
		5962-88634 **02 XX**				AT28HC256LF-12DM/883			
		5962-88634 **02 YX**				AT28HC256LF-12LM/883			
		5962-88634 **02 ZX**				AT28HC256LF-12FM/883			

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 12.3 - ATMEL SMD Part Types, Listed by SMD Number

5962-85102

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time(ns)
5962-85102 04 YX	AT27HC64L-90DM/883	8Kx8 EPROM	90
5962-85102 04 ZX	AT27HC64L-90LM/883	8Kx8 EPROM	90

5962-86063

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time(ns)
5962-86063 01 XX	AT27C256-20DM/883	32Kx8 EPROM	200
5962-86063 01 YX	AT27C256-20LM/883	32Kx8 EPROM	200
5962-86063 02 XX	AT27C256-25DM/883	32Kx8 EPROM	250
5962-86063 02 YX	AT27C256-25LM/883	32Kx8 EPROM	250
5962-86063 03 XX	AT27C256-30DM/883	32Kx8 EPROM	300
5962-86063 03 YX	AT27C256-30LM/883	32Kx8 EPROM	300
5962-86063 04 XX	AT27C256-17DM/883	32Kx8 EPROM	170
5962-86063 04 YX	AT27C256-17LM/883	32Kx8 EPROM	170
5962-86063 05 XX	AT27C256-15DM/883	32Kx8 EPROM	150
5962-86063 05 YX	AT27C256-15LM/883	32Kx8 EPROM	150
5962-86063 06 XX	AT27HC256L-12DM/883	32Kx8 EPROM	120
5962-86063 06 YX	AT27HC256L-12LM/883	32Kx8 EPROM	120
5962-86063 07 XX	AT27HC256L-90DM/883	32Kx8 EPROM	90
5962-86063 07 YX	AT27HC256L-90LM/883	32Kx8 EPROM	90
5962-86063 08 XX	AT27HC256-70DM/883	32Kx8 EPROM	70
5962-86063 08 YX	AT27HC256-70LM/883	32Kx8 EPROM	70

5962-87514

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
5962-87514 06 UX	AT28PC64-35KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	2	10K
5962-87514 06 XX	AT28PC64-35DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	2	10K
5962-87514 06 YX	AT28PC64-35LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	2	10K
5962-87514 07 UX	AT28PC64-30KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	2	10K
5962-87514 07 XX	AT28PC64-30DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	2	10K
5962-87514 07 YX	AT28PC64-30LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	2	10K

Table 12.3 - ATMEL SMD Part Types, Listed by SMD Number

5962-87514	*(continued)*					
Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
5962-87514 08 UX	AT28PC64-25KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	2	10K
5962-87514 08 XX	AT28PC64-25DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	2	10K
5962-87514 08 YX	AT28PC64-25LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	2	10K
5962-87514 09 UX	AT28PC64-20KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	2	10K
5962-87514 09 XX	AT28PC64-20DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	2	10K
5962-87514 09 YX	AT28PC64-20LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	2	10K
5962-87514 10 UX	AT28HC64L-12KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	2	10K
5962-87514 10 XX	AT28HC64L-12DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	2	10K
5962-87514 10 YX	AT28HC64L-12LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	2	10K
5962-87514 11 UX	AT28HC64L-90KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	2	10K
5962-87514 11 XX	AT28HC64L-90DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	2	10K
5962-87514 11 YX	AT28HC64L-90LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	2	10K
5962-87514 12 UX	AT28HC64L-70KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	70	2	10K
5962-87514 12 XX	AT28HC64L-70DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	70	2	10K
5962-87514 12 YX	AT28HC64L-70LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	70	2	10K
5962-87514 13 UX	AT28C64-35KM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
5962-87514 13 XX	AT28C64-35DM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
5962-87514 13 YX	AT28C64-35LM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
5962-87514 14 UX	AT28C64-30KM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	300	1	10K
5962-87514 14 XX	AT28C64-30DM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	300	1	10K
5962-87514 14 YX	AT28C64-30LM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	300	1	10K

Table 12.3 - ATMEL SMD Part Types, Listed by SMD Number

5962-87514	*(continued)*					
Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
5962-87514 15 UX	AT28C64-25KM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
5962-87514 15 XX	AT28C64-25DM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
5962-87514 15 YX	AT28C64-25LM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
5962-87514 15 ZX	AT28C64-25FM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
5962-87514 16 UX	AT28C64-20KM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	200	1	10K
5962-87514 16 XX	AT28C64-20DM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	200	1	10K
5962-87514 16 YX	AT28C64-20LM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	200	1	10K
5962-87514 17 UX	AT28C64-15KM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	150	1	10K
5962-87514 17 XX	AT28C64-15DM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	150	1	10K
5962-87514 17 YX	AT28C64-15LM/883	8Kx8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	150	1	10K
5962-87514 18 UX	AT28C64X-35KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	350	1	10K
5962-87514 18 XX	AT28C64X-35DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	350	1	10K
5962-87514 18 YX	AT28C64X-35LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	350	1	10K
5962-87514 19 UX	AT28C64X-30KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
5962-87514 19 XX	AT28C64X-30DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
5962-87514 19 YX	AT28C64X-30LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
5962-87514 20 UX	AT28C64X-25KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 20 XX	AT28C64X-25DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 20 YX	AT28C64X-25LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 20 ZX	AT28C64X-25FM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K

Table 12.3 - ATMEL SMD Part Types, Listed by SMD Number

5962-87514 *(continued)*

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
5962-87514 21 UX	AT28C64X-20KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
5962-87514 21 XX	AT28C64X-20DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
5962-87514 21 YX	AT28C64X-20LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
5962-87514 22 UX	AT28C64X-15KM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K
5962-87514 22 XX	AT28C64X-15DM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K
5962-87514 22 YX	AT28C64X-15LM/883	8Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K

5962-87515

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-87515 01 JX	AT27HC641-45DM/883	8Kx8 [UV] PROM	45
5962-87515 01 KX	AT27HC641-45FM/883	8Kx8 [UV] PROM	45
5962-87515 01 LX	AT27HC642-45DM/883	8Kx8 [UV] PROM	45
5962-87515 01 3X	AT27HC641-45LM/883	8Kx8 [UV] PROM	45
5962-87515 02 JX	AT27HC641-55DM/883	8Kx8 [UV] PROM	55
5962-87515 02 KX	AT27HC641-55FM/883	8Kx8 [UV] PROM	55
5962-87515 02 LX	AT27HC642-55DM/883	8Kx8 [UV] PROM	55
5962-87515 02 3X	AT27HC641-55LM/883	8Kx8 [UV] PROM	55
5962-87515 03 JX	AT27HC641-70DM/883	8Kx8 [UV] PROM	70
5962-87515 03 KX	AT27HC641-70FM/883	8Kx8 [UV] PROM	70
5962-87515 03 LX	AT27HC642-70DM/883	8Kx8 [UV] PROM	70
5962-87515 03 3X	AT27HC641-70LM/883	8Kx8 [UV] PROM	70
5962-87515 04 JX	AT27HC641-90DM/883	8Kx8 [UV] PROM	90
5962-87515 04 KX	AT27HC641-90FM/883	8Kx8 [UV] PROM	90
5962-87515 04 LX	AT27HC642-90DM/883	8Kx8 [UV] PROM	90
5962-87515 04 3X	AT27HC641-90LM/883	8Kx8 [UV] PROM	90

Table 12.3 - ATMEL SMD Part Types, Listed by SMD Number

5962-87539

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-87539 01 KX	AT22V10-25YM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 01 LX	AT22V10-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 01 3X	AT22V10-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 02 KX	AT22V10-30YM/883	22-Input, 10-Output and-or-Logic Array	30
5962-87539 02 LX	AT22V10-30DM/883	22-Input, 10-Output and-or-Logic Array	30
5962-87539 02 3X	AT22V10-30LM/883	22-Input, 10-Output and-or-Logic Array	30
5962-87539 03 KX	AT22V10-40YM/883	22-Input, 10-Output and-or-Logic Array	40
5962-87539 03 LX	AT22V10-40DM/883	22-Input, 10-Output and-or-Logic Array	40
5962-87539 03 3X	AT22V10-40LM/883	22-Input, 10-Output and-or-Logic Array	40
5962-87539 04 LX	AT22V10-20DM/883	22-Input, 10-Output and-or-Logic Array	20
5962-87539 04 3X	AT22V10-20LM/883	22-Input, 10-Output and-or-Logic Array	20

5962-87648

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-87648 01 XX	AT27C512R-15DM/883	64Kx8 EPROM	150
5962-87648 01 YX	AT27C512R-15LM/883	64Kx8 EPROM	150
5962-87648 02 XX	AT27C512R-20DM/883	64Kx8 EPROM	200
5962-87648 02 YX	AT27C512R-20LM/883	64Kx8 EPROM	200
5962-87648 03 XX	AT27C512R-25DM/883	64Kx8 EPROM	250
5962-87648 03 YX	AT27C512R-25LM/883	64Kx8 EPROM	250
5962-87648 04 XX	AT27C512R-12DM/883	64Kx8 EPROM	120
5962-87648 04 YX	AT27C512R-12LM/883	64Kx8 EPROM	120

5962-88525

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
5962-88525 01 UX	AT28C256-35UM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 01 XX	AT28C256-35DM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 01 YX	AT28C256-35LM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte Page	350	10	10K
5962-88525 01 ZX	AT28C256-35FM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K

Table 12.3 - ATMEL SMD Part Types, Listed by SMD Number

5962-88525	*(continued)*					
Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
5962-88525 02 UX	AT28C256-30UM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 XX	AT28C256-30DM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 YX	AT28C256-30LM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 ZX	AT28C256-30FM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 03 UX	AT28C256-25UM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 XX	AT28C256-25DM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 YX	AT28C256-25LM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 ZX	AT28C256-25FM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 04 UX	AT28C256-20UM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 XX	AT28C256-20DM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 YX	AT28C256-20LM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 ZX	AT28C256-20FM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 05 XX	AT28C256E-25DM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 YX	AT28C256E-25LM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 ZX	AT28C256E-25FM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 06 XX	AT28C256-15DM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 06 YX	AT28C256-15LM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 06 ZX	AT28C256-15FM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 07 XX	AT28C256F-15DM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 YX	AT28C256F-15LM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 ZX	AT28C256F-15FM/883	32Kx8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K

Table 12.3 - ATMEL SMD Part Types, Listed by SMD Number

5962-88634

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
5962-88634 01 UX	AT28HC256L-12UM/883	32K x 8 E^2PROM	Byte/Page	120	10	10K
5962-88634 01 XX	AT28HC256L-12DM/883	32K x 8 E^2PROM	Byte/Page	120	10	10K
5962-88634 01 YX	AT28HC256L-12LM/883	32K x 8 E^2PROM	Byte/Page	120	10	10K
5962-88634 01 ZX	AT28HC256L-12FM/883	32K x 8 E^2PROM	Byte/Page	120	10	10K
5962-88634 02 UX	AT28HC256LF-12UM/883	32K x 8 E^2PROM	Byte/Page	120	3	10K
5962-88634 02 XX	AT28HC256LF-12DM/883	32K x 8 E^2PROM	Byte/Page	120	3	10K
5962-88634 02 YX	AT28HC256LF-12LM/883	32K x 8 E^2PROM	Byte/Page	120	3	10K
5962-88634 02 ZX	AT28HC256LF-12FM/883	32K x 8 E^2PROM	Byte/Page	120	3	10K
5962-88634 03 UX	AT28HC256-90UM/883	32K x 8 E^2PROM	Byte/Page	90	10	10K
5962-88634 03 XX	AT28HC256-90DM/883	32K x 8 E^2PROM	Byte/Page	90	10	10K
5962-88634 03 YX	AT28HC256-90LM/883	32K x 8 E^2PROM	Byte/Page	90	10	10K
5962-88634 03 ZX	AT28HC256-90FM/883	32K x 8 E^2PROM	Byte/Page	90	10	10K
5962-88634 04 UX	AT28HC256F-90UM/883	32K x 8 E^2PROM	Byte/Page	90	3	10K
5962-88634 04 XX	AT28HC256F-90DM/883	32K x 8 E^2PROM	Byte/Page	90	3	10K
5962-88634 04 YX	AT28HC256F-90LM/883	32K x 8 E^2PROM	Byte/Page	90	3	10K
5962-88634 04 ZX	AT28HC256F-90FM/883	32K x 8 E^2PROM	Byte/Page	90	3	10K

5962-88670

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-88670 01 KX	AT22V10-25FM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 01 LX	AT22V10-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 01 3X	AT22V10-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 02 KX	AT22V10-30FM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88670 02 LX	AT22V10-30GM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88670 02 3X	AT22V10-30NM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88670 03 KX	AT22V10-40FM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88670 03 LX	AT22V10-40GM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88670 03 3X	AT22V10-40NM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88670 04 KX	AT22V10-20FM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88670 04 LX	AT22V10-20GM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88670 04 3X	AT22V10-20NM/883	22-Input, 10-Output and-or-Logic Array	20

Table 12.3 - ATMEL SMD Part Types, Listed by SMD Number

5962-88724

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-88724 01 KX	AT22V10L-25YM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 01 LX	AT22V10L-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 01 3X	AT22V10L-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 02 KX	AT22V10L-30YM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88724 02 LX	AT22V10L-30DM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88724 02 3X	AT22V10L-30LM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88724 03 KX	AT22V10L-40YM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88724 03 LX	AT22V10L-40DM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88724 03 3X	AT22V10L-40LM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88724 04 KX	AT22V10L-20YM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88724 04 LX	AT22V10L-20DM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88724 04 3X	AT22V10L-20LM/883	22-Input, 10-Output and-or-Logic Array	20

5962-88726

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-88726 01 LX	ATV750-40DM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88726 01 3X	ATV750-40LM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88726 02 LX	ATV750-35DM/883	22-Input, 10-Output and-or-Logic Array	35
5962-88726 02 3X	ATV750-35LM/883	22-Input, 10-Output and-or-Logic Array	35

5962-89755

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-89755 01 KX	AT22V10L-25FM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 01 LX	AT22V10L-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 01 3X	AT22V10L-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 02 KX	AT22V10L-30FM/883	22-Input, 10-Output and-or-Logic Array	30
5962-89755 02 LX	AT22V10L-30GM/883	22-Input, 10-Output and-or-Logic Array	30
5962-89755 02 3X	AT22V10L-30NM/883	22-Input, 10-Output and-or-Logic Array	30
5962-89755 03 KX	AT22V10L-40FM/883	22-Input, 10-Output and-or-Logic Array	40
5962-89755 03 LX	AT22V10L-40GM/883	22-Input, 10-Output and-or-Logic Array	40
5962-89755 03 3X	AT22V10L-40NM/883	22-Input, 10-Output and-or-Logic Array	40

ATMEL®

CONTENTS

Section 13

13

Features

- High Performance CMOS Technology
- Low Power Dissipation - Active and Standby
- Hardware Data Protection Features
- DATA Polling for End of Write Detection
- High Reliability
  - Endurance: 10^4 Cycles
  - Data Retention: 10 years
- Single 5V ± 10% Supply
- CMOS Compatible Inputs and Outputs
- 0°C to +70°C Operating Range
- Typical Die Thickness of 22 Mils

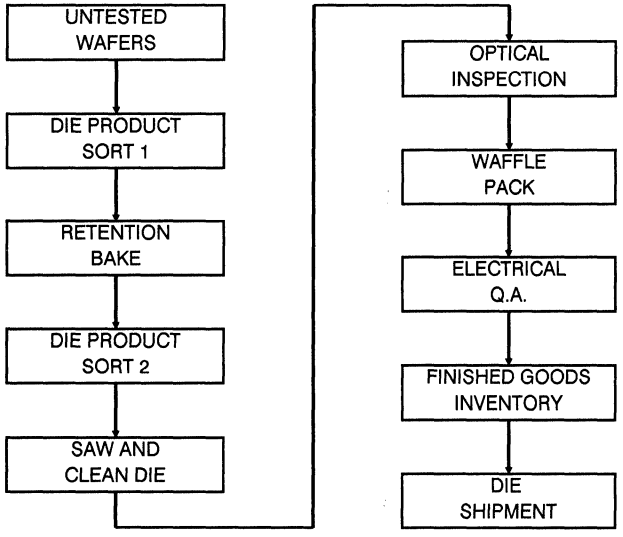
E²PROM Die Products

Description

To facilitate custom packaging, some Atmel E²PROMS are available in die form. All Atmel E²PROM die products are 100% electrically tested in wafer form and visually inspected after saw and clean. Atmel's E²PROM die products are processed with an advanced CMOS floating gate technology. As with all Atmel products, they are designed and tested to ensure high quality and manufacturability. The devices may include such features as internal error correction for extended endurance and improved data retention characteristics.

Test Flow

Atmel's die product sort testing incorporates comprehensive functional and parametric tests into wafer level tests. The typical Atmel E²PROM die test flow is outlined below.



Testing

Die product sort test 1 includes checks for basic D.C. parameters such as I_{CC} and input leakage as well as for A.C. switching parameters. Data pattern testing is included to guarantee the functionality of each bit and to guard against pattern sensitivity. Several oxide stress tests are included to reduce the likelihood of infant mortality failures.

The Data retention bake is included to ensure the integrity of the core cell oxides. A pattern is written to each die at the end of die sort test 1. The wafers are then subjected to a high temperature bake. After the bake, the pattern written in die sort test 1 is verified by die sort test 2. All die are optically inspected to the specifications of Military Standard 883C method 2010.

A final quality assurance test is performed on each assembly lot. A sample of the dice ready to ship is selected and electrically examined.

Die Product Offering

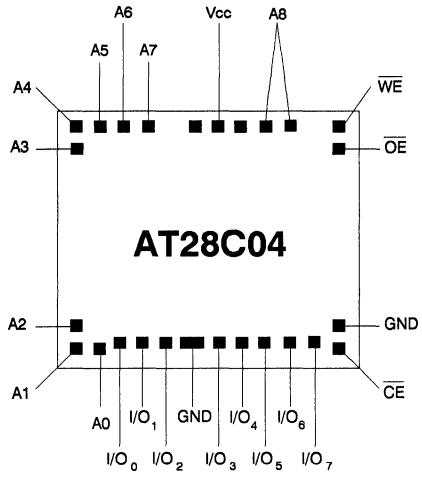
Die products are guaranteed across the commercial temperature operating range. The following E^2PROM die products are currently available from Atmel:

AT28C04	AT28C16
AT28C17	AT28C64
AT28PC64	AT28C256
AT28HC16L	AT28HC64L
AT28HC256L	AT28HC291L
AT28C010	

Handling and Die Information

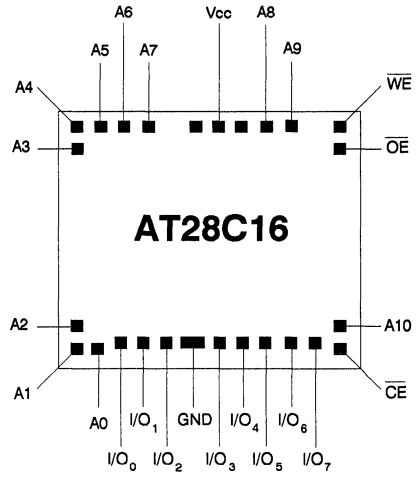
Handling instructions for E^2PROM die and other information needed for using E^2PROM die are available from Atmel.

AT28C04 DIE PINOUT



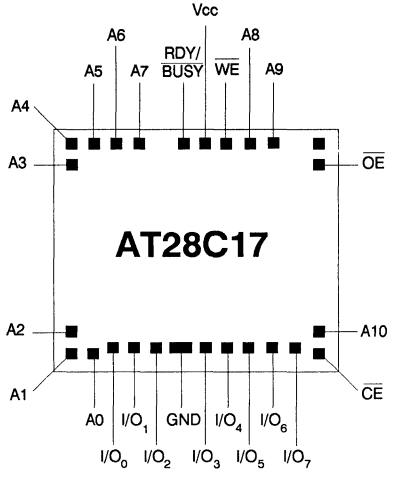
DIE SIZE: 137 X 117 mils
CONNECT SUBSTRATE TO GROUND

AT28C16 DIE PINOUT



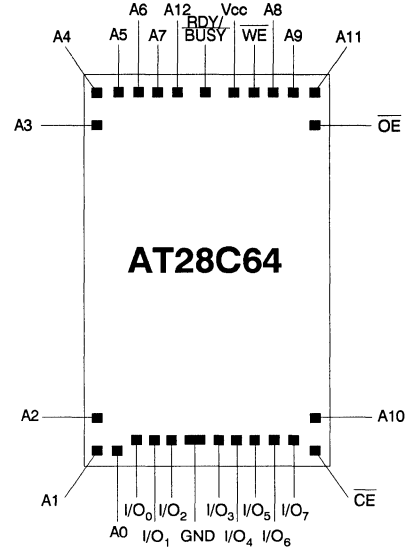
DIE SIZE: 137 X 117 mils
CONNECT SUBSTRATE TO GROUND

AT28C17 DIE PINOUT



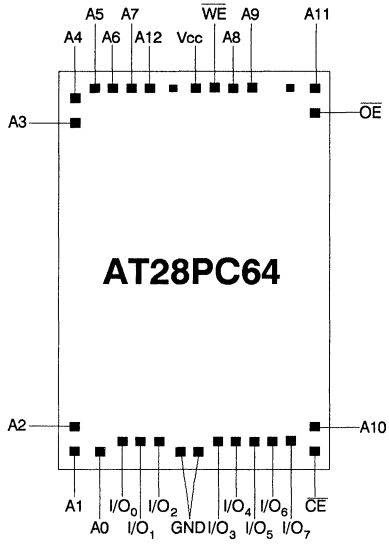
DIE SIZE: 137 X 117 mils
CONNECT SUBSTRATE TO GROUND

AT28C64 DIE PINOUT



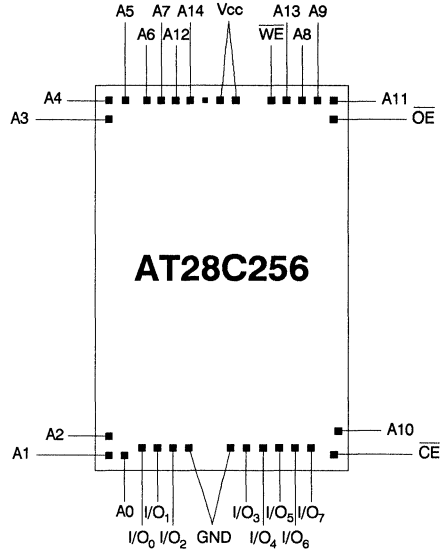
DIE SIZE: 133 X 207 mils
CONNECT SUBSTRATE TO GROUND

AT28PC64 DIE PINOUT



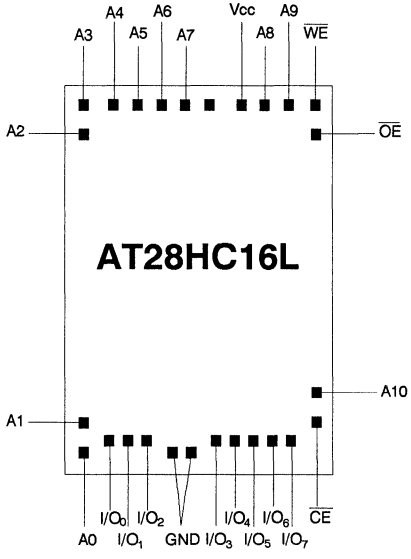
DIE SIZE: 146 X 217 mils
CONNECT SUBSTRATE TO GROUND

AT28C256 DIE PINOUT



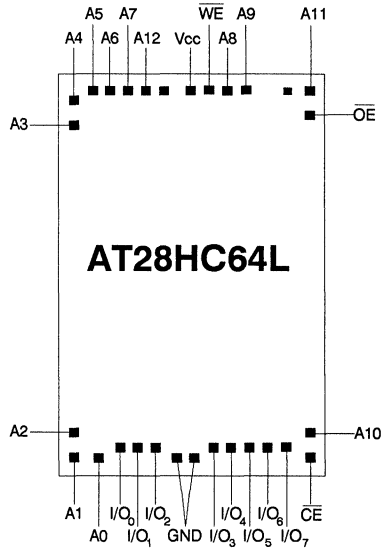
DIE SIZE: 224 X 323 mils
CONNECT SUBSTRATE TO GROUND

AT28HC16L DIE PINOUT



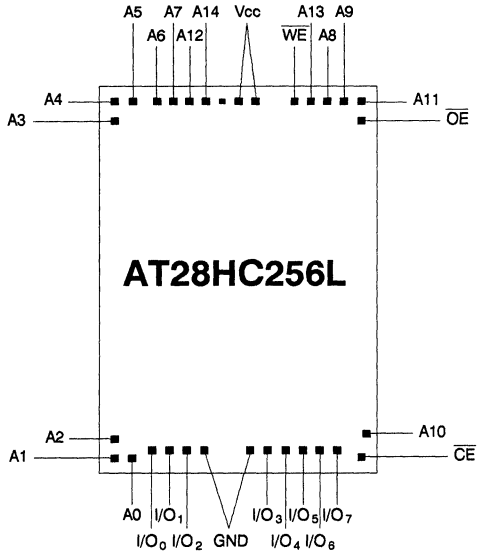
DIE SIZE: 118 X 144 mils
CONNECT SUBSTRATE TO GROUND

AT28HC64L DIE PINOUT



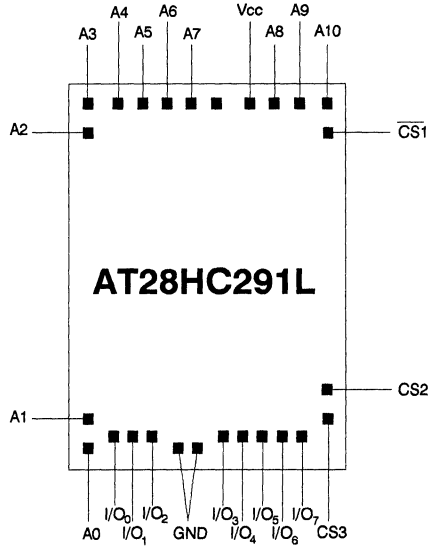
DIE SIZE: 146 X 217 mils
CONNECT SUBSTRATE TO GROUND

AT28HC256L DIE PINOUT



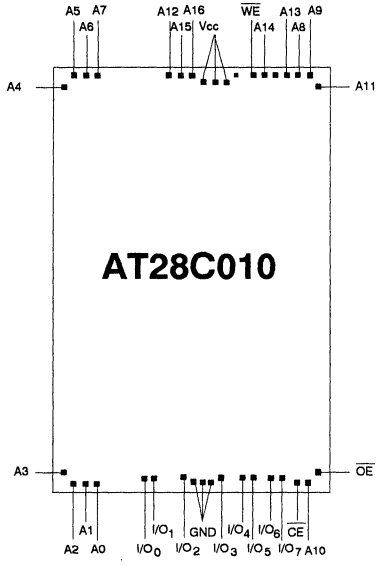
DIE SIZE: 224 X 323 mils
CONNECT SUBSTRATE TO GROUND

AT28HC291L DIE PINOUT



DIE SIZE: 118 X 144 mils
CONNECT SUBSTRATE TO GROUND

AT28C010 DIE PINOUT



DIE SIZE: 356 X 429 mils
CONNECT SUBSTRATE TO GROUND

ATMEL

CONTENTS

Section 14

Package Outlines

14

Each Atmel Data Sheet includes an Ordering Information Section which specifies the package types available. This section provides size specifications and outlines for all package types.

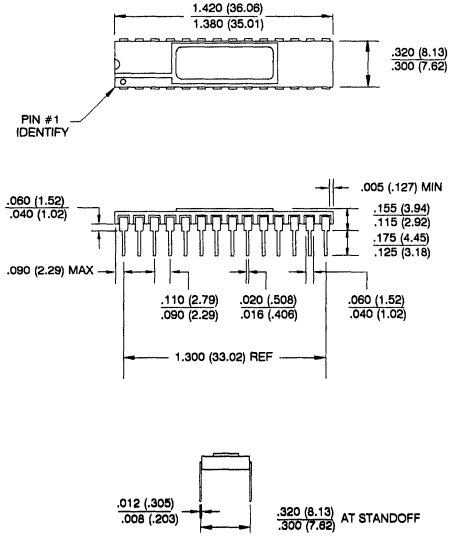
Package Outlines

Package *Description*

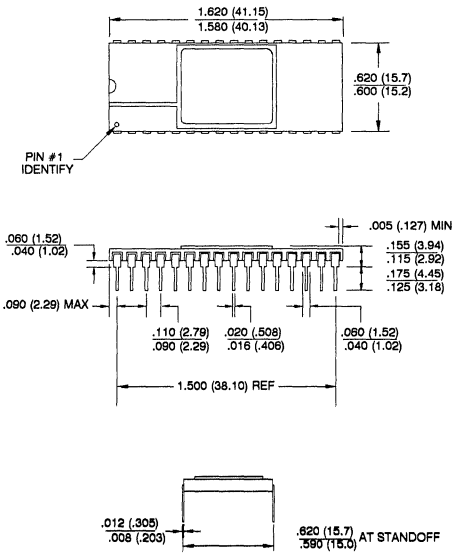
Continued on next page

Package *Description*

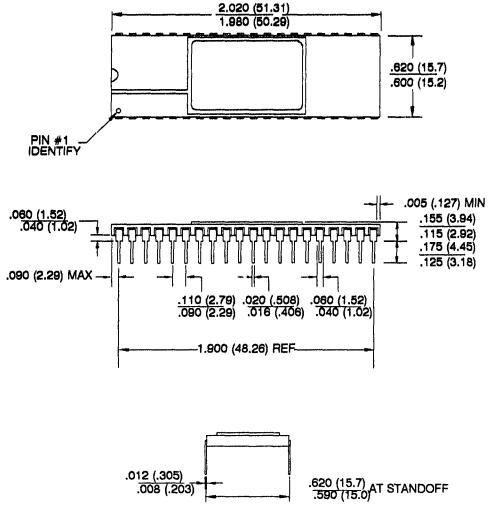
28B, 28-Lead, 0.300" Wide, Side Braze Ceramic Dual-In-Line
Dimensions in Inches and (Millimeters)



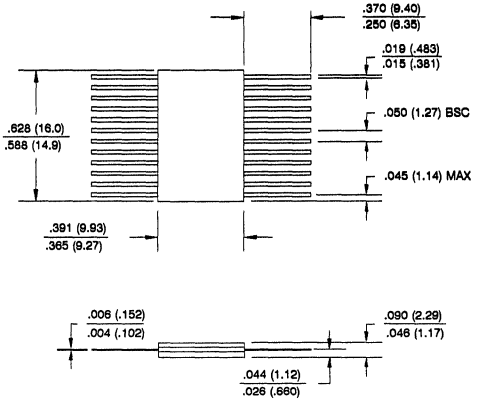
32B, 32-Lead, 0.600" Wide, Side Braze Ceramic Dual-In-Line
Dimensions in Inches and (Millimeters)
MIL-M-38510 CONFIG 3



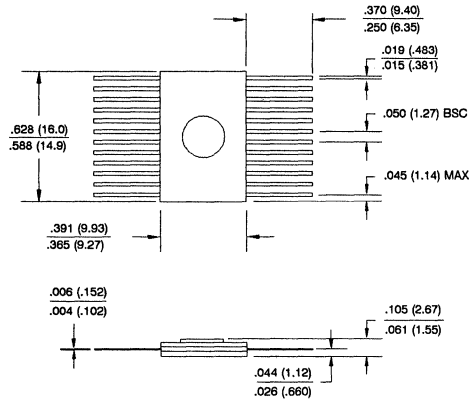
40B, 40-Lead, 0.600" Wide, Side Braze Ceramic Dual-In-Line
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-5 CONFIG 3



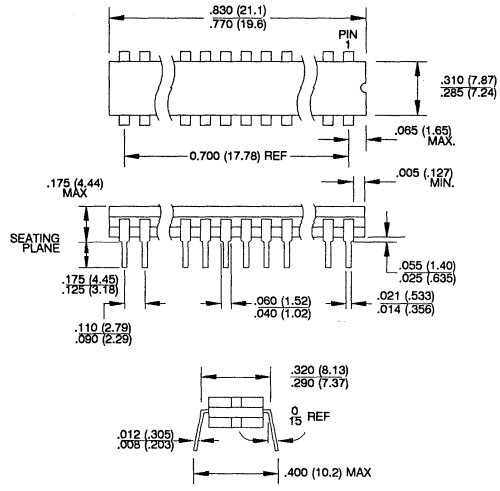
24C, 24-Lead, Non-Windowed, Cerpack
Dimensions in Inches and (Millimeters)
MIL-M-38510 F-6 CONFIG 1
JEDEC OUTLINE MO-019 AA



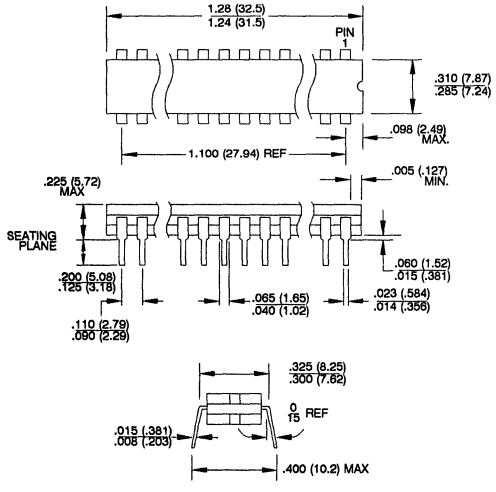
24CW, 24-Lead, Windowed, Cerpack
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE M0-019 AA



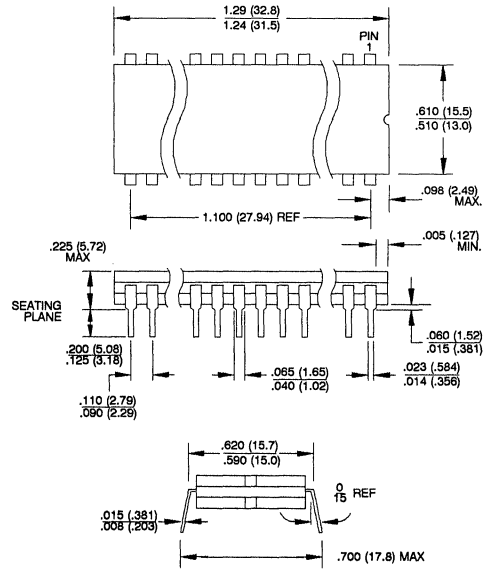
16D3, 16-Lead, 0.300" Wide, Non-Windowed, Cerdip
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-9 CONFIG 1



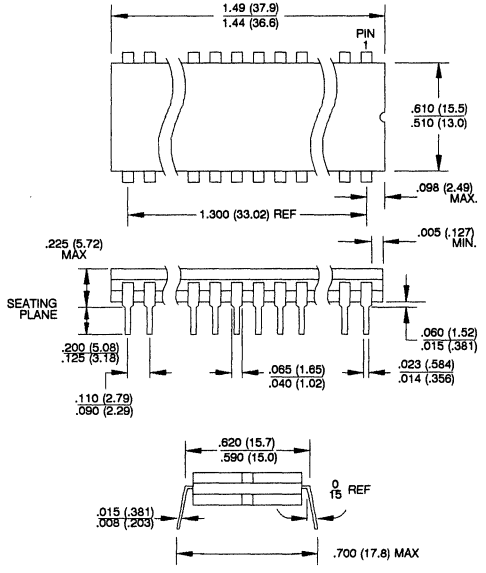
24D3, 24-Lead, 0.300" Wide, Non-Windowed Cerdip
Dual-In-Line
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-9 CONFIG 1



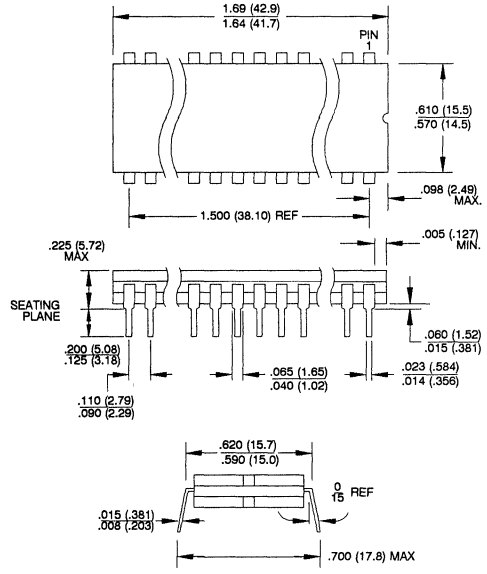
24D6, 24-Lead, 0.600" Wide, Non-Windowed, Cerdip
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-3 CONFIG 1



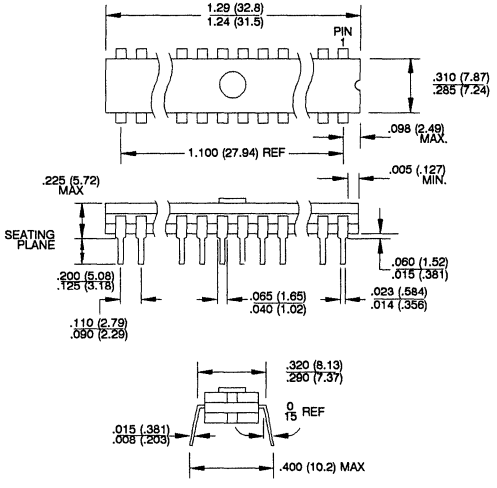
28D6, 28-Lead, 0.600" Wide, Non-Windowed, Cerdip
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-10 CONFIG 1



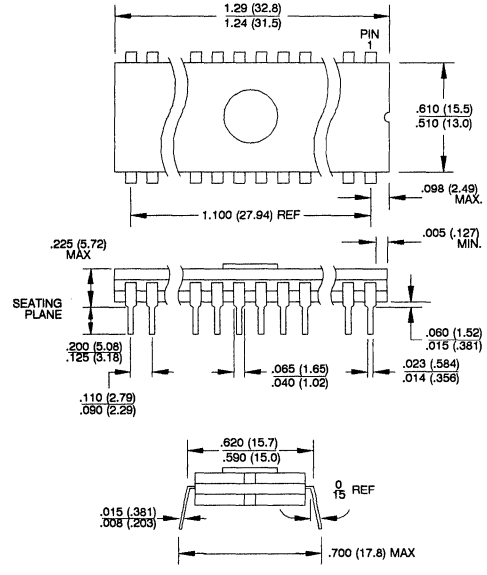
32D6, 32-Lead, 0.600" Wide, Non-Windowed, Cerdip
Dimensions in Inches and (Millimeters)



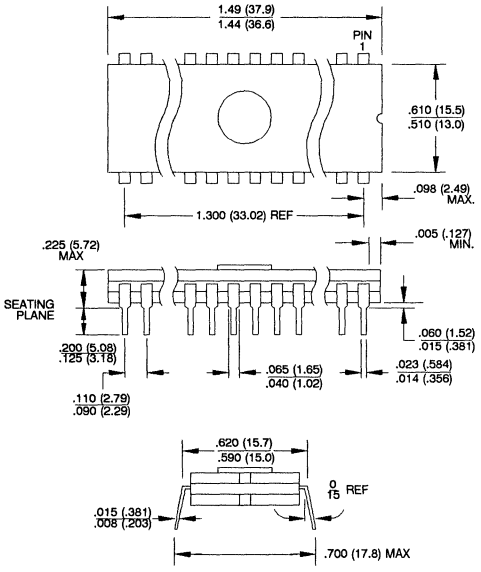
24DW3, 24-Lead, 0.300" Wide, Windowed, Cerdip
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-9 CONFIG 1



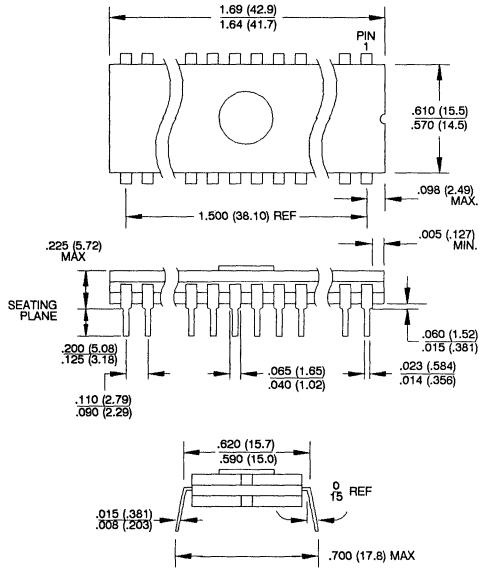
24DW6, 24-Lead, 0.600" Wide, Windowed, Cerdip
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-3 CONFIG 1



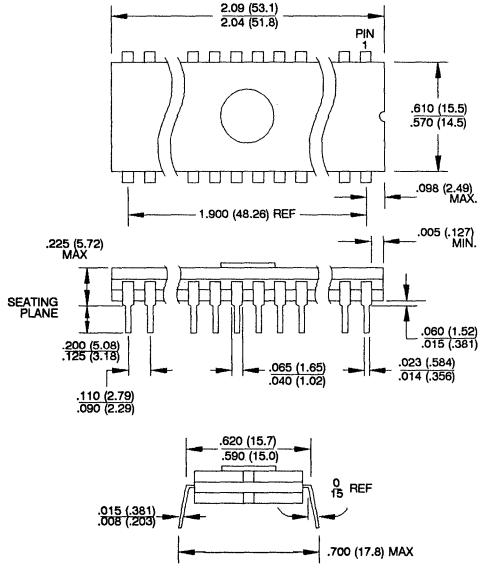
28DW6, 28-Lead, 0.600" Wide, Windowed, Cerdip
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-10 CONFIG 1



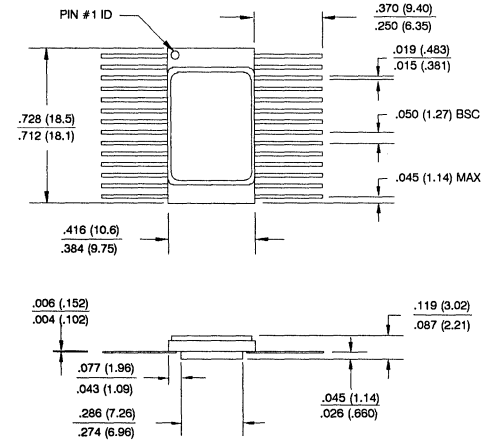
32DW6, 32-Lead, 0.600" Wide, Windowed, Cerdip
Dimensions in Inches and (Millimeters)



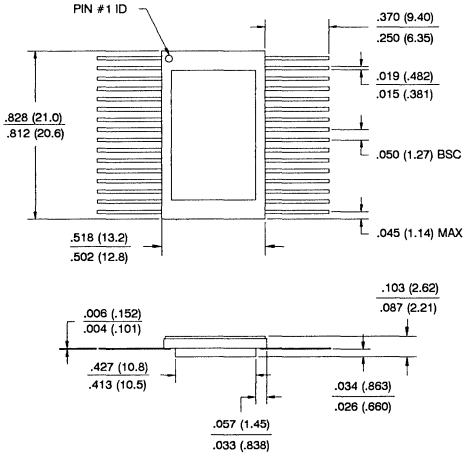
40DW6, 40-Lead, 0.600" Wide, Windowed, Cerdip
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-5 CONFIG 1



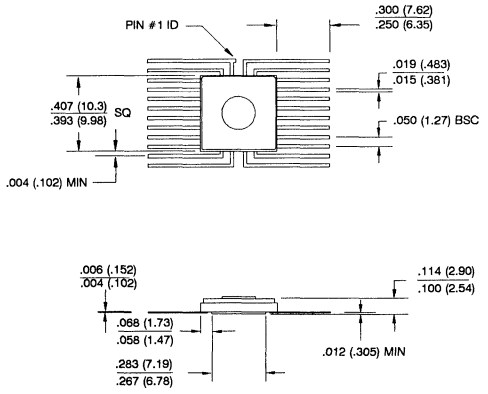
28F, 28-Lead, Non-Windowed, Brazed Flat Package
Dimensions in Inches and (Millimeters)
MIL-M-38510 F-12 CONFIG 2



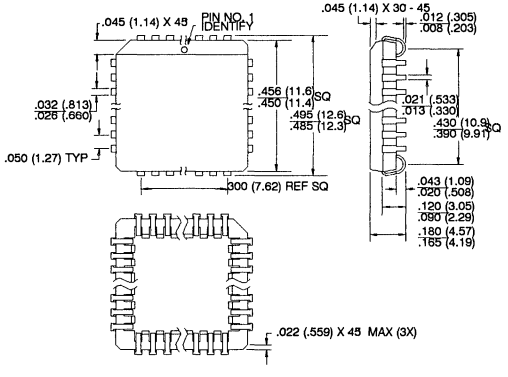
32F, 32-Lead, Non-Windowed, Brazed Flat Package
Dimensions in Inches and (Millimeters)



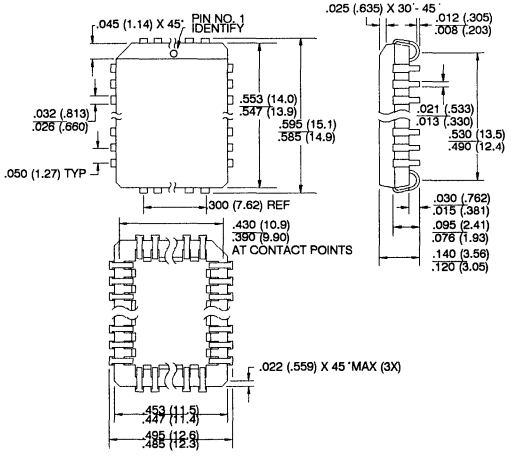
24FW, 24-Lead, Windowed, Brazed Flat Package
Dimensions in Inches and (Millimeters)



28J, 28-Lead Plastic J-Lead Chip Carrier
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE M0-047 AB

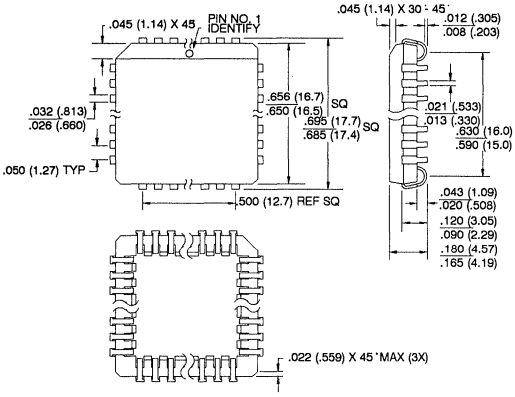


32J, 32-Lead Plastic J-Lead Chip Carrier
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-052 AE

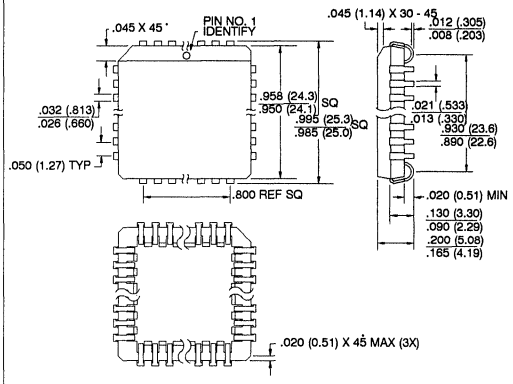


14

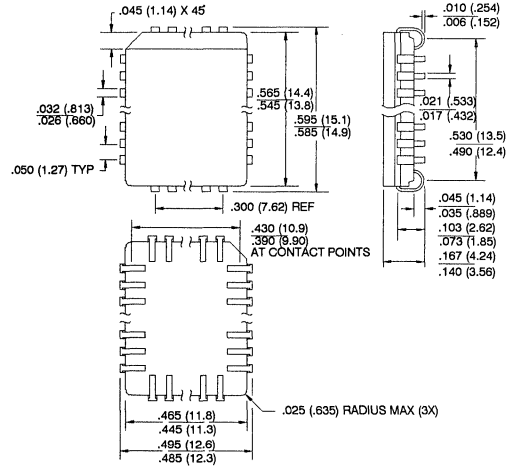
44J, 44-Lead, Plastic J-Lead Chip Carrier
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-047 AC



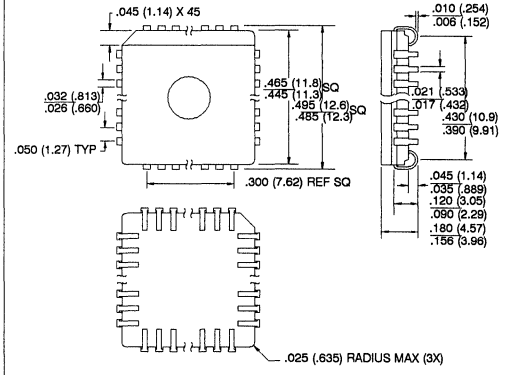
68J, 68-Lead Plastic J-Lead Chip Carrier
Dimensions in Inches and (Millimeters)



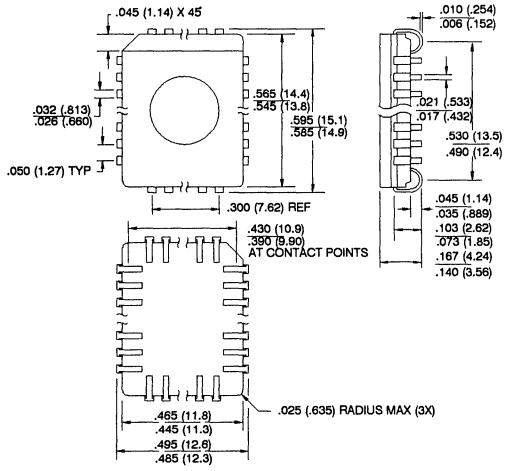
32K, 32-Lead, Non-Windowed, J-Leaded Chip Carrier
Dimensions in Inches and (Millimeters)



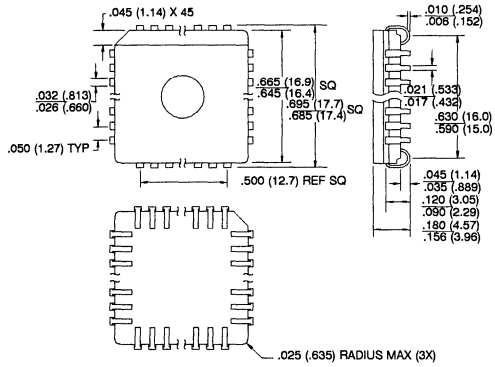
28KW, 28-Lead, Windowed, J-Leaded Chip Carrier
Dimensions in Inches and (Millimeters)



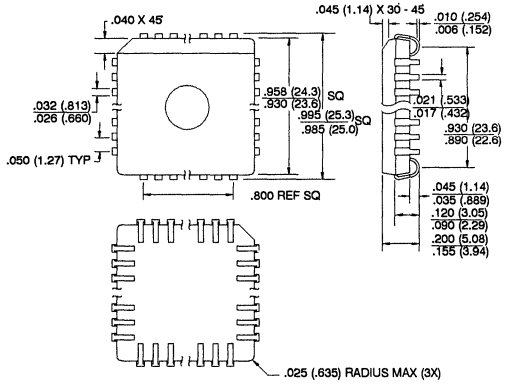
32KW, 32-Lead, Windowed, J-Leaded Chip Carrier
Dimensions in Inches and (Millimeters)



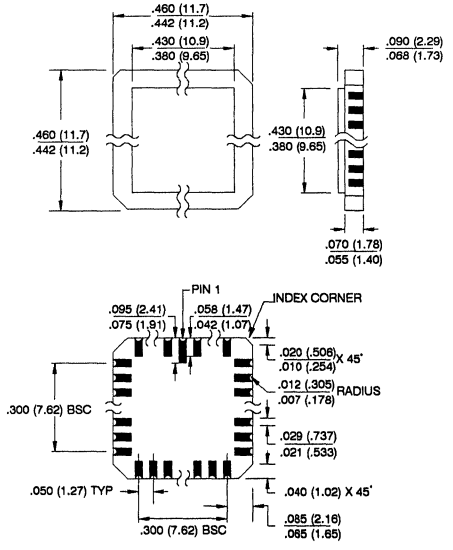
44KW, 44-Lead, Windowed, J-Leaded Chip Carrier
Dimensions in Inches and (Millimeters)



68KW, 68-Lead, Windowed, J-Leaded Chip Carrier
Dimensions in Inches and (Millimeters)

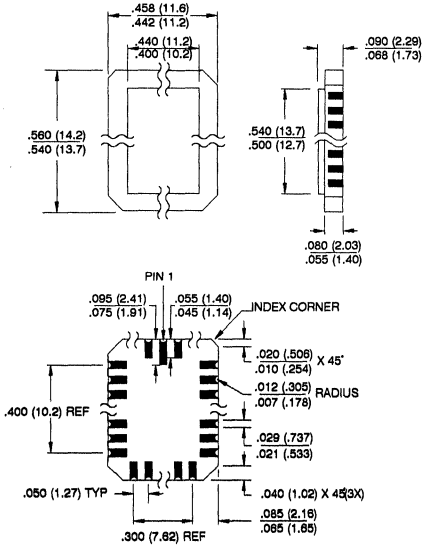


28L, 28-Pad, Non-Windowed, Ceramic Leadless Chip Carrier
Dimensions in Inches and (Millimeters)
MIL-M-38510 C-4

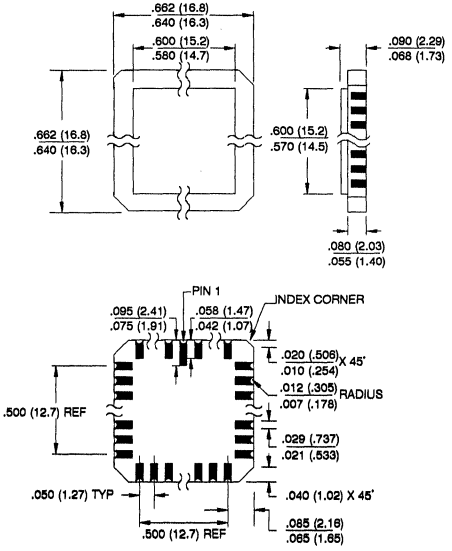


14

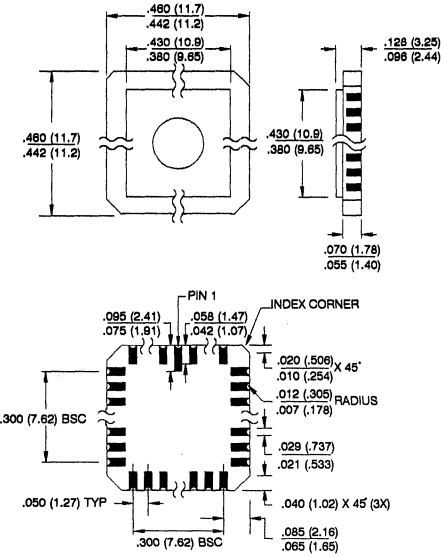
32L, 32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier
Dimensions in Inches and (Millimeters)
MIL-M-38510 C-12



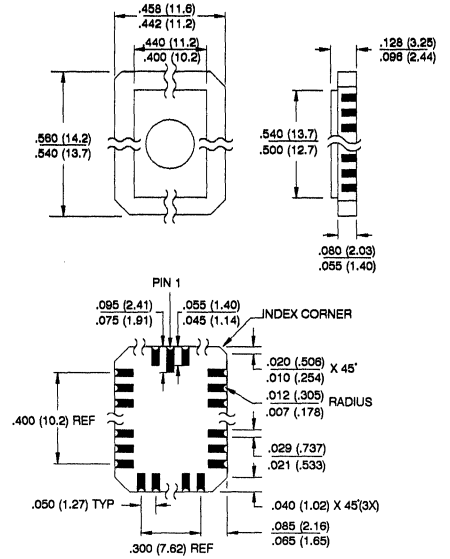
44L, 44-Pad, Non-Windowed, Ceramic Leadless Chip Carrier
Dimensions in Inches and (Millimeters)
MIL-M-38510 C-5



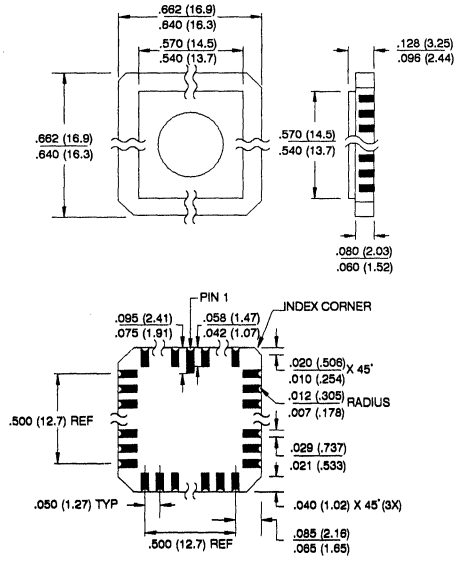
28LW, 28-Pad, Windowed, Ceramic Leadless Chip Carrier
Dimensions in Inches and (Millimeters)



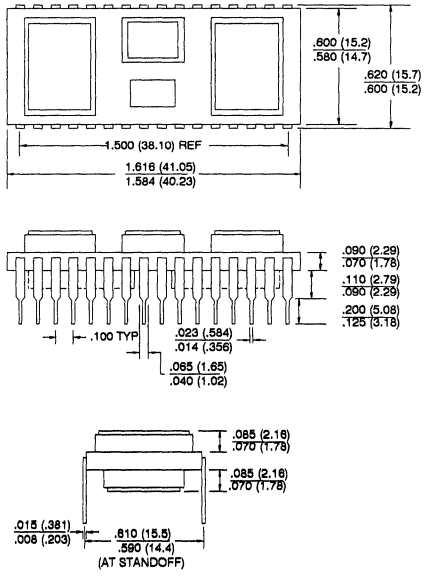
32LW, 32-Pad, Windowed, Ceramic Leadless Chip Carrier
Dimensions in Inches and (Millimeters)



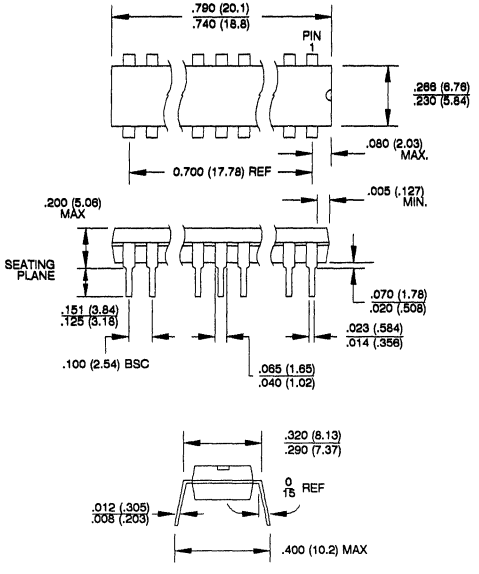
44LW, 44-Pad, Windowed, Ceramic Leadless Chip Carrier
Dimensions in Inches and (Millimeters)



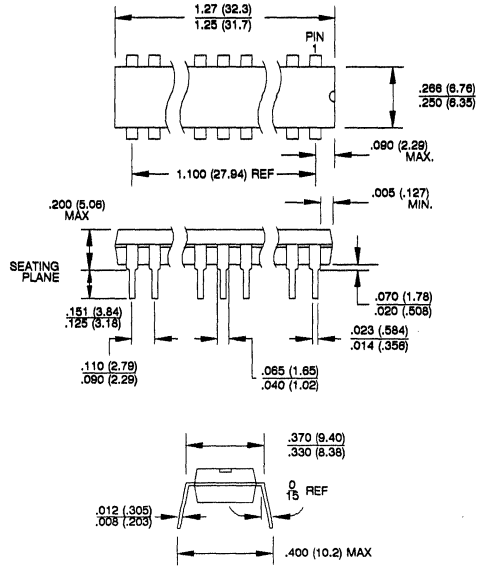
32M, 32-Lead, Non-Windowed, 32D6 Compatible, Ceramic Module
Dimensions in Inches and (Millimeters)



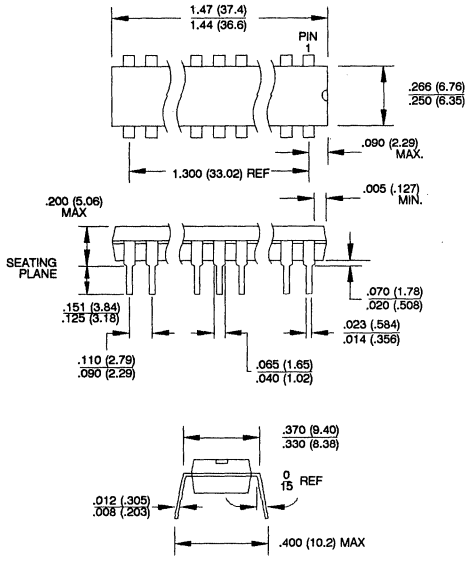
16P3, 16-Lead, 0.300" Wide, Plastic Dual-In-Line
Dimensions in Inches and (Millimeters)



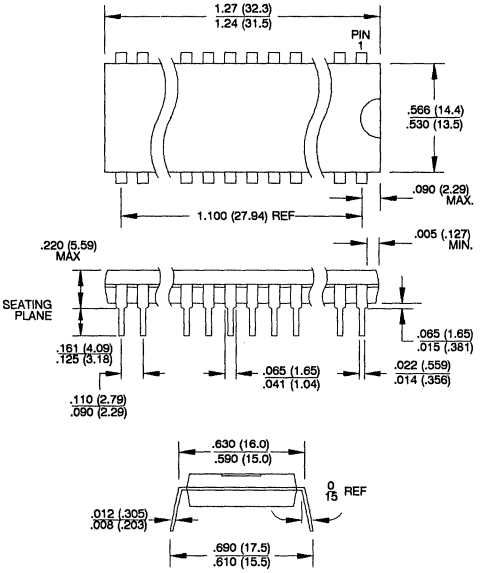
24P3, 24-Lead, 0.300" Wide, Plastic Dual-In-Line
Dimensions in Inches and (Millimeters)



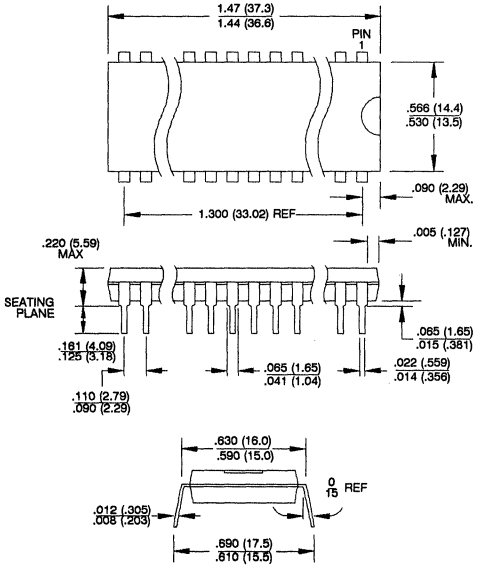
28P3, 28-Lead, 0.300" Wide, Plastic Dual-In-Line
Dimensions in Inches and (Millimeters)



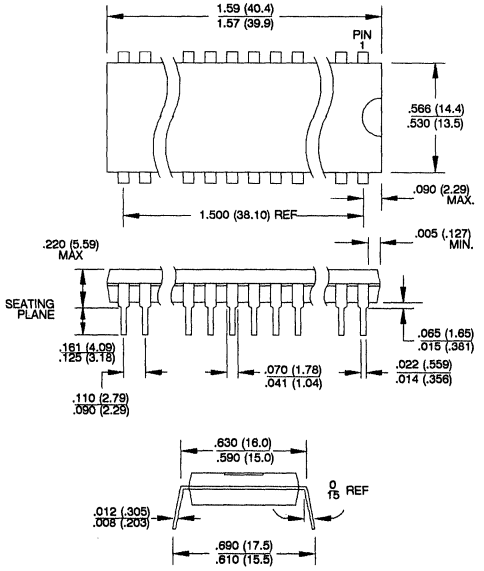
24P6, 24-Lead, 0.600" Wide, Plastic Dual-In-Line
Dimensions in Inches and (Millimeters)



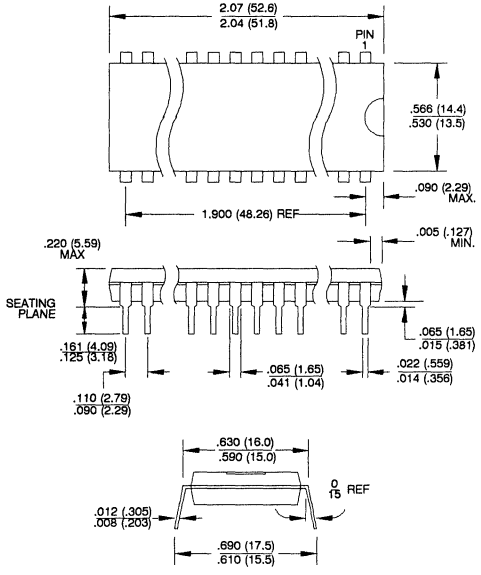
28P6, 28-Lead, 0.600" Wide, Plastic Dual-In-Line
Dimensions in Inches and (Millimeters)



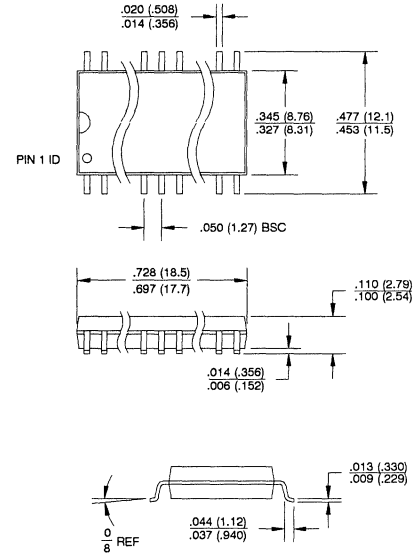
32P6, 32-Lead, 0.600" Wide, Plastic Dual-In-Line
Dimensions in Inches and (Millimeters)



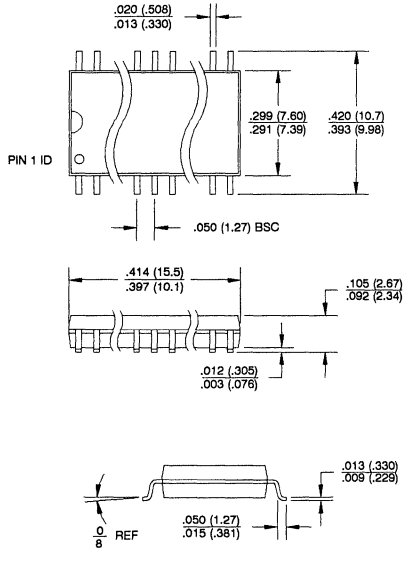
40P6, 40-Lead, 0.600" Wide, Plastic Dual-In-Line
Dimensions in Inches and (Millimeters)



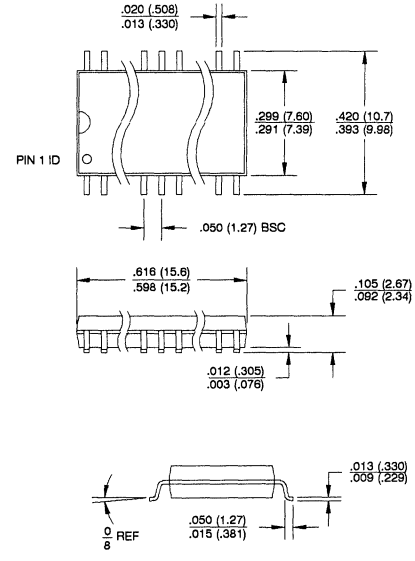
28R, 28-Lead, 0.330" Wide, Plastic Gull Wing SOIC
Dimensions in Inches and (Millimeters)



16S, 16-Lead, 0.300" Wide, Plastic Gull Wing SOIC
Dimensions in Inches and (Millimeters)

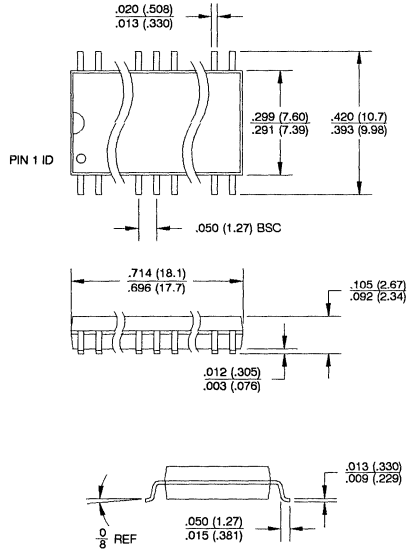


24S, 24-Lead, 0.300" Wide, Plastic Gull Wing SOIC
Dimensions in Inches and (Millimeters)

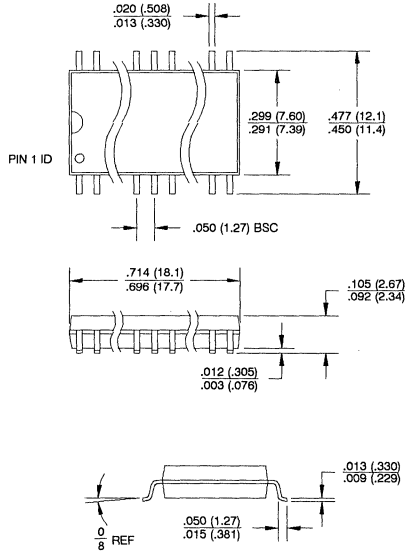


14

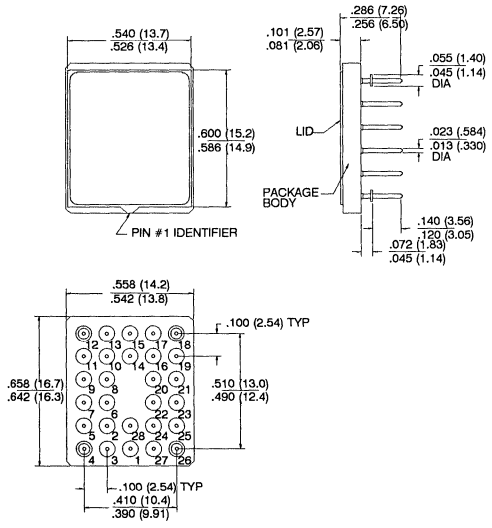
28S, 28-Lead, 0.300" Wide, Plastic Gull Wing SOIC
Dimensions in Inches and (Millimeters)



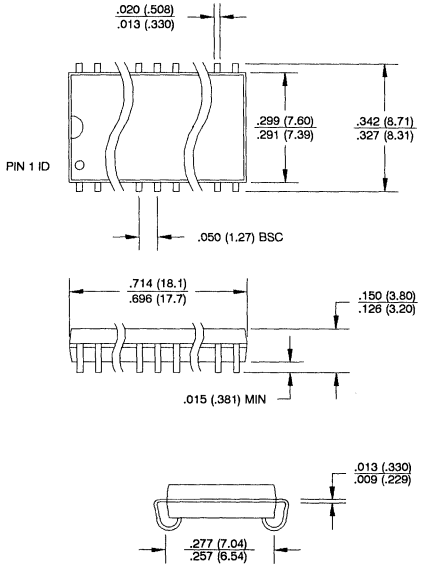
28T, 28-Lead, 0.300" Wide, Wide Footprint Plastic Gull-Wing SOIC
Dimensions in Inches and (Millimeters)



28U, 28-Pin, Ceramic Pin Grid Array
Dimensions in Inches and (Millimeters)



28X, 28-Lead, 28 Pin, 0.300" Wide, Plastic J-Lead SOIC
Dimensions in Inches and (Millimeters)



Thermal Characteristics of Atmel Packages

The thermal performance of the semiconductor package is a very important consideration for the board designer. The reliability and functional life of the device is directly related to its junction operating temperature. As the temperature of the device increases, the stability of its junctions decline, as does its reliable life. The thermal performance is also important to the board design, because it may limit the board density, or dictate the board location of high power-dissipating devices, or require expensive cooling methods for the system. As devices have become more complex and boards have become denser, the need to account for the thermal characteristics of packages have shifted from being a minor consideration to being a necessary consideration.

The thermal performance of a package is measured by its ability to dissipate the power required by the device into its surroundings. The electrical power drawn by the device generates heat on the top surface of the die. This heat is conducted through the package to the surface and then transferred to the surrounding air by convection. Each heat transfer step has a corresponding "resistance" to the heat flow, which is given the value θ, the thermal resistance coefficient. Subscripts are added to the coefficient to specify the two points that the heat is transferred between. Commonly used coefficients are θ_{JA} (junction to ambient air), θ_{JC} (junction to package case), and θ_{CA} (case to ambient air).

An electrical analogy can be made, as shown in the figure below, to illustrate the heat flow of a package. The heat transfer can be characterized mathematically by the following equation,

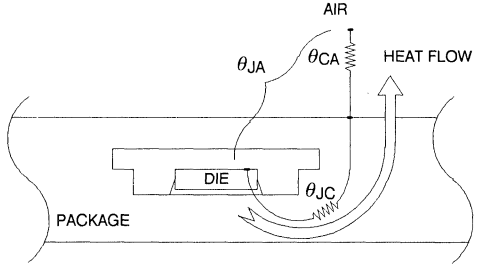
$$Tj - Ta = P \times \theta_{JA}$$

where,

P = Device operating power [watts]
Tj = Temperature of a junction on the device [°C]
Ta = Temperature of the surrounding ambient air [°C]

Two conclusions can be made after examining this analogy. First, the lower the value of θ_{JA}, the better the heat dissipation of the package. Secondly, the value of θ_{JA} is directly dependent upon both the conductive (θ_{JC}) and convective (θ_{CA}) properties of the package. θ_{JC} is a function of the package material, the adhesion between the package materials, and device size. θ_{CA} is a function of the package size and configuration, package mounting method, and air flow across the package. Lower θ_{JA} values can be achieved by specifying ceramic packages instead of plastic packages, choosing larger packages, or improving air flow across the package.

The thermal resistance values of Atmel standard packages are listed on the following page. The figures shown are maximum values for θ, typical values are lower dependent upon the device type.



Thermal Resistance Coefficients

		θ_{JC} [°C/W]	θ_{JA} [°C/W]		
			Airflow=0 ft/min	Airflow=100 ft/min	Airflow=500 ft/min
Ceramic DIP	24D3/DW3	9	65	50	35
	24D6/DW6	10-15	45	35	20
	28D6/DW6	10-15	45	35	30
	32D6/DW6	10	45	35	30
	40D6/DW6	7	40	30	25
Plastic DIP	24P3	22	82	72	60
	24P6	39	82	72	60
	28P6	36	77	68	56
	32P6	34	72	64	53
	40P6	30	68	60	49
Leadless Chip Carrier	28L/LW	12	68	56	48
	32L/LW	10	65	55	47
	44L/LW	4	60	49	40
Plastic Leaded Chip Carrier	28J	16	60	50	40
	32J	16	60	50	40
	44J	14	50	44	35
JLCC	28K/KW	16	72	64	53
	32K/KW	16	72	64	53
	44K/KW	16	68	60	49
Cerpack	24C/CW	15	81	72	63

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Fax. 011-3373180

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Elecktronik AB
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Prospect Technology
5, Lane 55, Long-Chiang Road
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Fax. (886)-27733756

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9F No 8
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Taipei
Taiwan R.O.C.
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Insight Electronics
1515 West University
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Tempe, AZ 85281
(602) 829-1800

Time Electronics
1301 West Geneva Drive
Tempe, AZ 85282
(602) 967-2000

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Added Value
1582 Parkway Loop
Unit G
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31194 La Baya Drive
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Bell Industries
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(213) 826-6778

306 East Alondra Boulevard
Gardena, CA 90248
(213) 515-1800

11095 Knott Ave.
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(714) 895-7801

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7827 Convey Court
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15120 Marquardt Ave.
Santa Fe Springs, CA 90670
(213) 921-3611

Bradas Microtech
2175 Martin Ave.
Santa Clara, CA 95050
(408) 980-2500

Insight Electronics
15635 Alton Pkwy
Suite 120
Irvine, CA 92718
(714) 727-2111

28038 Dorothy Drive
Suite 2
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(818) 707-2100

6885 Flanders Drive
Suite C
San Diego, CA 92121
(619) 587-9757

Jan Devices
6925 Canby Ave.
Bldg. 109
Reseda, CA 91335
(818) 708-1100

Merit Electronics
2070 Ringwood Ave.
San Jose, CA 95131
(408) 434-0800

Milgray/Los Angeles
912 Pancho Road
Camarillo, CA 93010-8508
(805) 484-4055

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Suite 102
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(818) 707-2890

9285 Dowdy Drive
San Diego, CA 92126
(619) 586-1331

9751 Independence Avenue
Chatsworth, CA 91311
(818) 998-7200

1339 Moffett Park Drive
Sunnyvale, CA 94089
(408) 734-9888

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Technologies, Inc.
12900 Saratoga Ave.
Saratoga, CA 95070
(408) 725-1660

6837 Nancy Ridge Drive
San Diego, CA 92121
(619) 453-8430

1637 North Brian St.
Orange, CA 92667
(714) 637-0200

28720 Roadside Dr.
Suite 175
Agoura, CA 91301
(818) 707-0377

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Added Value (AVED)
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(303) 422-1701

Bell Industries
12421 West 49th Avenue
Wheatridge, CO 80033
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Englewood,CO 80112
(303) 799-8851

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(203) 265-3134

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384 Pratt Street
Meriden, CT 06450
(203) 235-1422

Milgray/Connecticut
326 West Main St.
Milford, CT 06460
(203) 878-5538

Phase I Technology
36A Padanaram Road
Danbury, CT 06811
(203) 791-9042

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(203) 262-1319

Western Micro
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731 Main Street
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Lantridge, CA 06468
(203) 798-2366

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Sunrise, FL 33351
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Altamonte Springs, FL 32701
(407) 339-0078

Milgray/Florida
1850 Lee Road
Suite 104
Winter Park, FL 32789
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4203 Vineland-Suite K7
Orlando, FL 32811
(407) 841-6565

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Milgray/Atlanta
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Norcross, GA 30071
(404) 446-9777

Time Electronics
4045 Wetherburn Way
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Norcross, GA 3007
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200 Galleria Parkway
Suite 1740
Atlanta, GA 30339
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7110-16 North Lydon Street
Rosemont, IL 60018
(708) 297-6200

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870 Cambridge Drive
Elk Grove Village, IL 60007
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GBL Goold Electronics
101 Leland Court
Bensenville, IL 60106
(312) 860-7171

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3223 North Wilke
Suite 2312
Arlington Heights, IL 60004
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Time Electronics
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Schaumburg, IL 60195
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8446 Moller Road
Indianapolis, IN 46248
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Carmel, IN 46032
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Indianapolis, IN 46268
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Cedar Rapids, IA 52404
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Overland Park, KS 66202
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14636 Rothgeb Drive
Rockville, MD 20850
(301) 251-1205

Jaco Electronics, Inc.
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Columbia, MD 21046
(301) 995-6620

Milgray/Washington
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Baltimore, MD 21236
(301) 529-0500

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Beltsville, MD 20705
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Time Electronics
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(301) 964-3090

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2 Lowell Avenue
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100 Burtt Rd.
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Andover, MA 01810
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Cronin Electronics, Inc.
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Needham, MA 02194
(617) 449-5000

Jaco Electronics
1053 East Street
Tewksbury, MA 01876
(508) 640-0010

Milgray/New England
Ballardvale Park
187 Ballardvale Street
Wilmington, MA 01887
(508) 657-5900

Nu Horizons
107 Audubon Road #19
Wakefield, MA 01880
(617) 246-4442

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10A Centennial Drive
Peabody, MA 01960
(508) 532-9900

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20 Blanchard Rd.
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Farmington Hills, MI 48331
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Ann Arbor, MI 48104
(313) 971-9093

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3001 Greentree Executive
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(201) 882-8300

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Farmingdale, NY 11735
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145 Oser Avenue
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Milgray/Upstate New York
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(513) 435-8660

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Concord, Ontario L4K 2Z4
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Suite 506 Bell Mews
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Tele. (403) 436-9555
Fax. (403) 438-4983

#210, 3015-5th Ave. N.E.
Calgary, Alberta T2A 6T8
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760 Century Street
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Tele. (204) 786-8401
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June 1990

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