NONVOLATILE MEMORY

DATA BOOK

MAY 1996

ATMEL

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NONVOLATILE MEMORY

E^2PROM • EPROM • FLASH

DATA BOOK

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Atmel Corporation
Nonvolatile Memory Data Book
May 1996

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Nonvolatile Memory Overview

With the nonvolatile memories available from Atmel, you are given the ability to program devices late in a system's development cycle, or even after the system is complete. This feature gives you the flexibility for meeting changing market conditions. The principle products of nonvolatile memory are EPROMs (erasable programmable read-only memories), E^2PROMs (electronically erasable programmable read-only memories) and Flash devices.

EPROMs

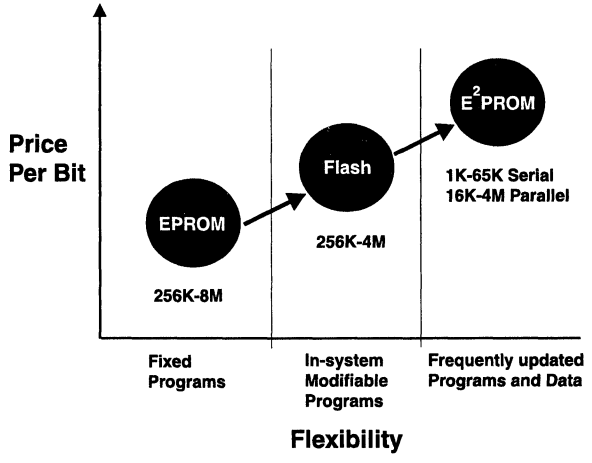
Atmel is a leading supplier of high-speed and low-voltage EPROMs and is recognized as one of the top three world suppliers in the market. EPROMs, the lowest cost user-programmable nonvolatile memory, can be programmed electrically in a programmer or its current system. These devices are used for program storage in computer and communications equipment, such as cellular phones, pagers, modems, and other computer peripherals. Atmel's EPROMs are manufactured in 5V and 2.7V versions with capacities up to 8M bits and access times as fast as 45 ns.

Flash Memory

Known as the major volume supplier of 2.7V read and write Flash memories, Atmel leads the industry as one of the top three Flash makers in the world. Flash memories combine the electrically erasable flexibility of E^2PROMs with the higher density and lower cost per bit of EPROMs—representing the fastest growing product sector in the semiconductor industry. What distinguishes Atmel's Flash products from its competitors is its use of a single low-voltage power source, for write and read functions. Atmel's Flash devices are used primarily to store operating programs in telecommunications, graphics, networking systems, and home video game systems. With Atmel's 2.7V low-voltage devices, you can extend battery life or reduce the number of batteries necessary for portable systems such as cellular telephones, pagers, laptop and palmtop devices.

Parallel E^2PROMs

Since 1991 Atmel has been the world's largest supplier of these in-system, reprogrammable nonvolatile memories. E^2PROMs are distinguished as Parallel- or Serial-interface through their connection to the system's microcontroller or microprocessor. Atmel offers the industry's most complex full-featured Parallel E^2PROM, the world's first single-chip 4M bit monolithic E^2PROM, which is used extensively in many military and commercial avionics applications. Atmel produces the industry's only complete line of standard-voltage and battery-voltage Parallel devices that serve the growing portable equipment market. Parallel E^2PROM leadership; first to market with battery-voltage devices and first to market with the largest density devices.



Serial E^2PROMs

Serial-interface E^2PROMs are used in a broad spectrum of consumer, telecommunication and automotive products, primarily for recording and holding personal preference data, such as programmable radio stations, seat comfort controls, auto-dial in telephones and program memory in camcorders. Key to Atmel's success in Serials is its 1.8V low-voltage family. Atmel is the only manufacturer to offer all Serial devices available in today's market.

Atmel Corporation designs, manufactures, and markets high quality and high performance CMOS memory, logic and analog integrated circuits. Founded in 1984, the Company serves the manufacturers of computation, communications and instrumentation equipment in commercial, industrial and military environments.

Atmel's broad line of products provide customers with a variety of solutions to their memory and logic applications. Atmel offers high-density, high-speed memory and logic standard products as well as custom gate arrays.

Atmel guarantees quality and reliability by fabricating all products— no matter what their intended application— to meet or exceed the specifications of Military Standard 883.

Whether you are new to programmable logic or an experienced user, Atmel is committed to your success. If you have any questions or would like to place an order, please contact your local Atmel sales office as listed in the back of this data book, or contact Atmel's corporate headquarters:

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EPROMs

Part Number	Organization	Speeds	Description
Battery-Voltage™ **(2.7V to 3.6V)**			
AT27BV256	32K x 8	70-150 ns	256K bit, 2.7-Volt to 3.6-Volt
AT27BV512	64K x 8	90-150 ns	512K bit, 2.7-Volt to 3.6-Volt
AT27BV010	128K x 8	90-150 ns	1M bit, 2.7-Volt to 3.6-Volt EPROM
AT27BV1024	64K x 16	120-150 ns	1M bit, 2.7-Volt to 3.6-Volt
AT27BV020	256K x 8	120-150 ns	2M bit, 2.7-Volt to 3.6-Volt EPROM
AT27BV4096	256K x 16	150 ns	4M bit, 2.7-Volt to 3.6-Volt
AT27BV040	512K x 8	150 ns	4M bit, 2.7-Volt to 3.6-Volt EPROM
Low Voltage (3.0 to 3.6V)			
AT27LV256A	32K x 8	70-150 ns	256K bit, 3-Volt EPROM
AT27LV512A	64K x 8	90-150 ns	512K bit, 3-Volt EPROM
AT27LV010A	128K x 8	90-150 ns	1M bit, 3-Volt EPROM
AT27LV020A	256K x 8	120-150 ns	2M bit, 3-Volt EPROM
AT27LV040A	512K x 8	150 ns	4M bit, 3-Volt EPROM
Standard Voltage (5V)			
AT27C256R	32K x 8	45-150 ns	256K, 5-Volt EPROM
AT27C512R	64K x 8	45-150 ns	512K, 5-Volt EPROM
AT27C516	32K x 16	45-150 ns	512K, 5-Volt EPROM
AT27C1024	64K x 16	45-150 ns	1M bit, 5-Volt EPROM
AT27C010,L	128K x 8	45-150 ns	1M bit, 5-Volt EPROM, Standard & Low Power
AT27C2048	128K x 16	70-150 ns	2M bit, 5-Volt EPROM
AT27C020	256K x 8	85-150 ns	2M bit, 5-Volt EPROM
AT27C4096	256K x 16	85-150 ns	4M bit, 5-Volt EPROM
AT27C040	512K x 8	80-150 ns	4M bit, 5-Volt EPROM
AT27C080	1024K x 8	100-150 ns	8M bit, 5-Volt EPROM
AT27C8192	512K x 16	100-150 ns	8M bit, 5-Volt EPROM

Flash Memory

Part Number	Organization	Speeds	Description
Battery-Voltage™ **(2.7V to 3.6V)**			
AT29BV010A	128K x 8	200-350 ns	1M bit, 2.7-Volt Read and 2.7-Volt Write Flash
AT29BV020	256K x 8	250-350 ns	2M bit, 2.7-Volt Read and 2.7-Volt Write Flash
AT29BV040A	512K x 8	250-350 ns	4M bit, 2.7-Volt Read and 2.7-Volt Write Flash
Low Voltage (3V to 3.6V)			
AT29LV256	32K x 8	150-250 ns	256K, 3-Volt Read and 3-Volt Write Flash
AT29LV512	64K x 8	150-250 ns	512K, 3-Volt Read and 3-Volt Write Flash
AT29LV010A	128K x 8	150-250 ns	1M bit, 3-Volt Read and 3-Volt Write Flash
AT29LV1024	64K x 16	150-250 ns	1M bit, 3-Volt Read and 3-Volt Write Flash
AT29LV020	256K x 8	200-250 ns	2M bit, 3-Volt Read and 3-Volt Write Flash
AT29LV040A	512K x 8	200-250 ns	4M bit, 3-Volt Read and 3-Volt Write Flash
Standard Voltage (5V)			
AT29C256	32K x 8	70-250 ns	256K, 5-Volt Read and 5-Volt Write Flash
AT29C257	32K x 8	70-250 ns	256K, 5-Volt Read and 5-Volt Write Flash
AT29C512	64K x 8	70-200 ns	512K, 5-Volt Read and 5-Volt Write Flash
AT29C1024	64K x 16	70-200 ns	1M bit, 5-Volt Read and 5-Volt Write Flash
AT29C010A	128K x 8	70-200 ns	1M bit, 5-Volt Read and 5-Volt Write Flash
AT29C020	256K x 8	90-200 ns	2M bit, 5-Volt Read and 5-Volt Write Flash
AT29C040A	512K x 8	120-250 ns	4M bit, 5-Volt Read and 5-Volt Write Flash
AT49F010	128K x 8	70-200 ns	1M bit, 5-Volt Read and 5-Volt Write Flash
AT49F020	256K x 8	90-200 ns	2M bit, 5-Volt Read and 5-Volt Write Flash
AT49F2048	128K x 16	90-200 ns	2M bit, 5-Volt Read and 5-Volt Write Flash
AT49F040	512K x 8	120-250 ns	4M bit, 5-Volt Read and 5-Volt Write Flash
AT49F4096	256K x 16	90-200 ns	4M bit, 5-Volt Read and 5-Volt Write Flash
AT49F008	1M x 8	120-200 ns	8M bit, 5-Volt Read and 5-Volt Write Flash
AT49F8192	512K x 16	120-200 ns	8M bit, 5-Volt Read and 5-Volt Write Flash

FPGA Serial Configuration E^2PROM

Part Number	Memory Size	Description
AT17C65	65,536 x 1	65K FPGA Configuration E^2PROM
AT17C128	131,072 x 1	128K FPGA Configuration E^2PROM
AT17C256	262,144 x 1	256K FPGA Configuration E^2PROM

Parallel E²PROMs

Part Number	Organization	Speeds	Description
High Speed			
AT28HC64B	8K x 8	55-120 ns	64K E²PROM with 64-Byte Page & Software Data Protection
AT28HC256	32K x 8	70-120 ns	256K E²PROM with 64-Byte Page & Software Data Protection
AT28HC256E	32K x 8	70-120 ns	256K E²PROM with Extended Endurance, Standard & Low Power
Battery-Voltage™ **(2.7V to 3.6V)**			
AT28BV16	2K x 8	250-300 ns	16K E²PROM, 2.7-Volt
AT28BV64	8K x 8	300 ns	64K E²PROM, 2.7-Volt
Low Voltage (3.0V to 3.6V)			
AT28LV64B	8K x 8	200-300 ns	64K E²PROM with 64-Byte Page & Software Data Protection, 3.0-Volt
AT28LV256	32K x 8	200-300 ns	256K E²PROM with 64-Byte Page & Software Data Protection, 3.0-Volt
AT28LV010	128K x 8	200-250 ns	1M bit E²PROM with 128-Byte Page & Software Data Protection, 3.0-Volt
Standard Voltage (5V)			
AT28C16	2K x 8	150-250 ns	16K E²PROM
AT28C16E	2K x 8	150-250 ns	16K E²PROM with Extended Endurance & Fast Write
AT28C17	2K x 8	150-250 ns	16K E²PROM with Ready/$\overline{\text{Busy}}$
AT28C17E	2K x 8	150-250 ns	16K E²PROM with Ready/$\overline{\text{Busy}}$ & Extended Endurance & Fast Write
AT28C64	8K x 8	120-350 ns	64K E²PROM
AT28C64E	8K x 8	120-350 ns	64K E²PROM with Extended Endurance & Fast Write
AT28C64X	8K x 8	150-450 ns	64K E²PROM without Ready-$\overline{\text{Busy}}$
AT28C64B	8K x 8	150-250 ns	64K E²PROM with 64-Byte Page & Software Data Protection
AT28C256	32K x 8	150-350 ns	256K E²PROM with 64-Byte Page & Software Data Protection
AT28C256E	32K x 8	150-350 ns	256K E²PROM with Extended Endurance
AT28C010	128K x 8	120-250 ns	1M bit E²PROM with 128-Byte Page & Software Data Protection
AT28C010E	128K x 8	120-250 ns	1M bit E²PROM with 128-Byte Page & Extended Endurance & Software Data Protection
AT28C040	512K x 8	150-250 ns	4M bit E²PROM with 256-Byte Page & Software Data Protection

Serial E²PROMs

Part Number	Organization	V_{CC}	Description
AT24C01	128 x 8	1.8, 2.5, 2.7, 5.0 V	1K, 2-Wire Bus Serial E²PROM, Non-Cascadable
AT24C21	128 x 8	2.5 V	1K, 2-Wire Bus Serial E²PROM, Dual Mode, Plug & Play Operation
AT24C01A	128 x 8	1.8, 2.5, 2.7, 5.0 V	1K, 2-Wire Bus Serial E²PROM
AT24C02	256 x 8	1.8, 2.5, 2.7, 5.0 V	2K, 2-Wire Bus Serial E²PROM
AT24C04	512 x 8	1.8, 2.5, 2.7, 5.0 V	4K, 2-Wire Bus Serial E²PROM
AT24C08	1024 x 8	1.8, 2.5, 2.7, 5.0 V	8K, 2-Wire Bus Serial E²PROM
AT24C16	2048 x 8	1.8, 2.5, 2.7, 5.0 V	16K, 2-Wire Bus Serial E²PROM
AT24C164	2048 x 8	1.8, 2.5, 2.7, 5.0 V	16K, 2-Wire Bus Serial E²PROM with Cascadable Feature
AT24C32	4096 x 8	1.8, 2.5, 2.7, 5.0 V	32K, 2-Wire Bus Serial E²PROM with Cascadable Feature
AT24C64	8192 x 8	1.8, 2.5, 2.7, 5.0 V	64K, 2-Wire Bus Serial E²PROM with Cascadable Feature
AT25010	128 x 8	1.8, 2.7, 5.0 V	1K, SPI Bus Serial E²PROM, Supports SPI Mode 0 and 3
AT25020	256 x 8	1.8, 2.7, 5.0 V	2K, SPI Bus Serial E²PROM, Supports SPI Mode 0 and 3
AT25040	512 x 8	1.8, 2.7, 5.0 V	4K, SPI Bus Serial E²PROM, Supports SPI Mode 0 and 3
AT25320	4096 x 8	1.8, 2.7, 5.0 V	32K, SPI Bus Serial E²PROM, Supports SPI Mode 0 and 3
AT25640	8192 x 8	1.8, 2.7, 5.0 V	64K, SPI Bus Serial E²PROM, Supports SPI Mode 0 and 3
AT93C46	64 x 16 / 128 x 8	1.8, 2.5, 2.7, 5.0 V	1K, 3-Wire Bus Serial E²PROM
AT93C46A	64 x 16	1.8, 2.5, 2.7, 5.0 V	1K, 3-Wire Bus Serial E²PROM
AT93C56	128 x 16 / 256 x 8	2.5, 2.7, 5.0 V	2K, 3-Wire Bus Serial E²PROM
AT93C57	128 x 16 / 256 x 8	2.5, 2.7, 5.0 V	2K, 3-Wire Bus Serial E²PROM with Special Address
AT93C66	256 x 16 / 512 x 8	2.5, 2.7, 5.0 V	4K, 3-Wire Bus Serial E²PROM
AT59C11	64 x 16 / 128 x 8	2.5, 2.7, 5.0 V	1K, 4-Wire Bus Serial E²PROM
AT59C22	128 x 16 / 256 x 8	2.5, 2.7, 5.0 V	2K, 4-Wire Bus Serial E²PROM
AT59C13	256 x 16 / 512 x 8	2.5, 2.7, 5.0 V	4K, 4-Wire Bus Serial E²PROM

Explanation of Atmel's Part Number Code

All Atmel part numbers begin with the prefix "AT." The next four to nine digits are the part number. In addition, Atmel parts can be ordered in particular speeds, in specific packages, for particular temperature ranges and with the option of 883C level B military compliance. The available options for each part are listed at the back of its data sheet in its "Ordering Information" table. These options are designated by the following suffixes placed at the end of the Atmel part number, in the order given:

Prefix	Device -	Suffix
AT	XXXXX	X X X X

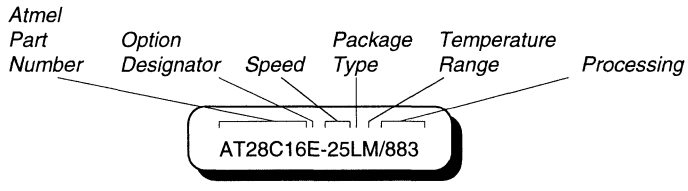
Processing
- Blank = Standard
- /883 = MIL-STD-883, Class B Fully Compliant
- B = MIL-STD-883, Class B Non-Compliant

Temperature Range
- C = Com Temp (0°C to 70°C)
- I = Ind Temp (-40°C to 85°C)
- M = Mil Temp (-55°C to 125°C)

Package
- B = Ceramic Side Braze Dual Inline
- C = Cerpack
- D = Cerdip
- F = Flatpack
- G = Cerdip, One Time Programmable
- J = Plastic J-Lead Chip Carrier
- K = Ceramic J-Lead Chip Carrier
- L = Leadless Chip Carrier
- M = Ceramic Module
- N = Leadless Chip Carrier, One Time Programmable
- P = Plastic DIP
- Q = Plastic Quad Flatpack
- R = SOIC
- S = SOIC
- T = TSOP
- U = PGA
- V = TAB
- W = Die
- Y = Cerpack
- Z = Ceramic Multi-Chip Module

Speed

Here is an example Atmel part number:



0538A

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ATMEL

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Parallel E^2PROMs

***Battery-Voltage*™ • 2.7V - 3.6V Operation**

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Low Voltage • 3.0V - 3.6V Operation

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2-Wire Serial CMOS E²PROM

1K (128 x 8)

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **2.5 (V_{CC} = 2.5V to 5.5V)**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **Internally Organized 128 x 8**
- **2-Wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility**
- **4-Byte Page Write Mode**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Cycles**
  - **Data Retention: 100 Years**
- **Automotive Grade and Extended Temperature Devices Available**
- **8-Pin PDIP and JEDEC SOIC Packages**

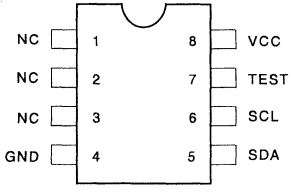
Description

The AT24C01 provides 1024 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01 is available in space saving 8-pin PDIP and 8-pin SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

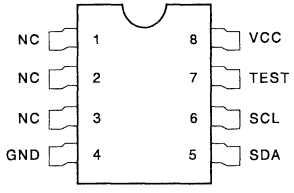
Pin Configurations

Pin Name	Function
NC	No Connect
SDA	Serial Data
SCL	Serial Clock Input
Test	Test Input (GND or V_{CC})

8-Pin PDIP



8-Pin SOIC



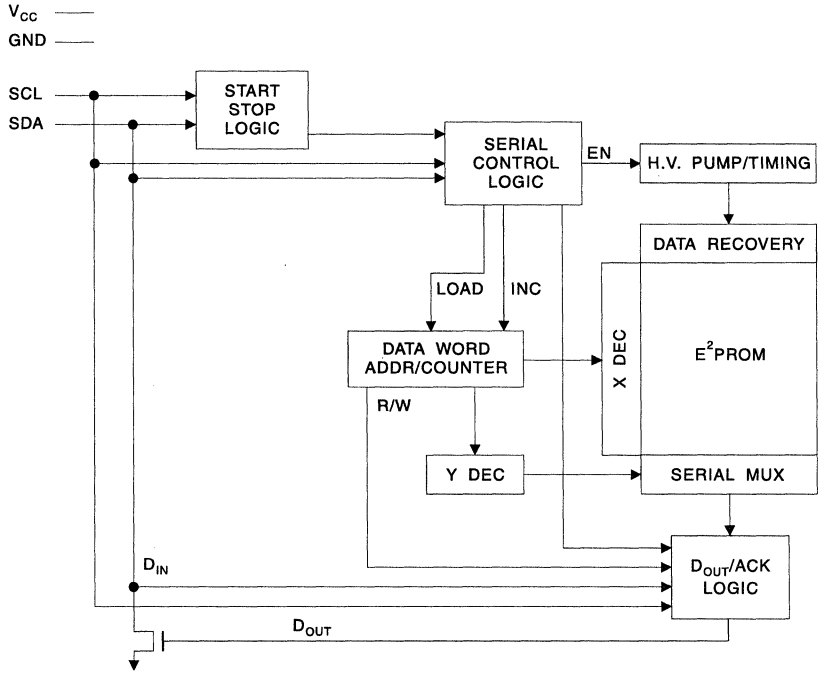
0134B

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each E^2PROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

Memory Organization

AT24C01, 1K SERIAL E^2PROM: Internally organized with 128 pages of 1-byte each. The 1K requires a 7 bit data word address for random word addressing.

Pin Capacitance

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level (1)		-1.0		V_{CC} x 0.3	V
V_{IH}	Input High Level (1)		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time (1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start (1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time (1)		1.0		0.3	µs
t_F	Inputs Fall Time (1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns

Note: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

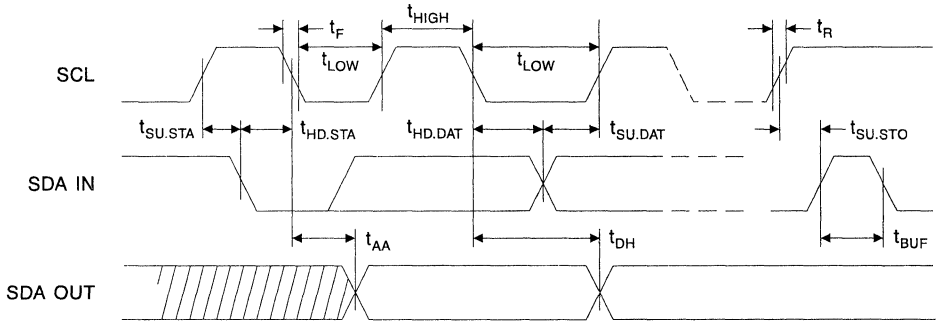
START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition which terminates all communications. After a read sequence, the stop command will place the E^2PROM in a standby power mode (refer to Start and Stop Definition timing diagram).

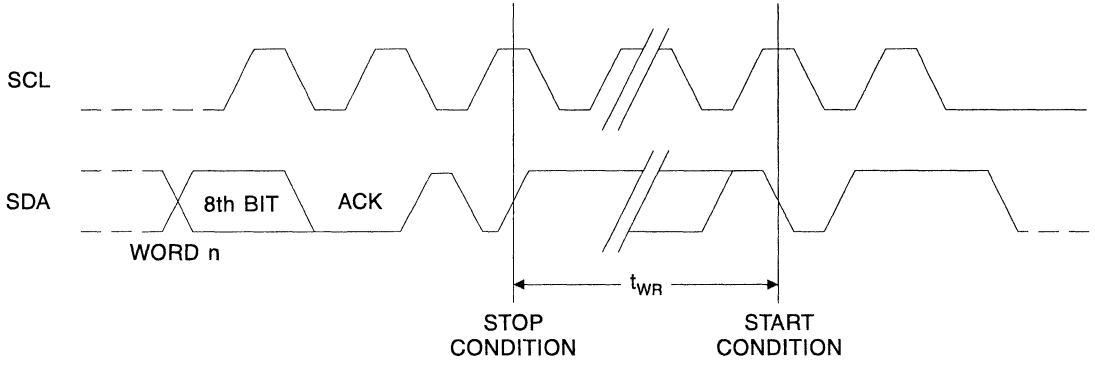
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E^2PROM in 8 bit words. Any device on the system bus receiving data (when communicating with the E^2PROM) must pull the SDA bus low to acknowledge that it has successfully received each word. This must happen during the ninth clock cycle after each word received and after all other system devices have freed the SDA bus. The E^2PROM will likewise acknowledge by pulling SDA low after receiving each address or data word (refer to Acknowledge Response from Receiver timing diagram).

STANDBY MODE: The AT24C01 features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

Bus Timing SCL: Serial Clock SDA: Serial Data I/O

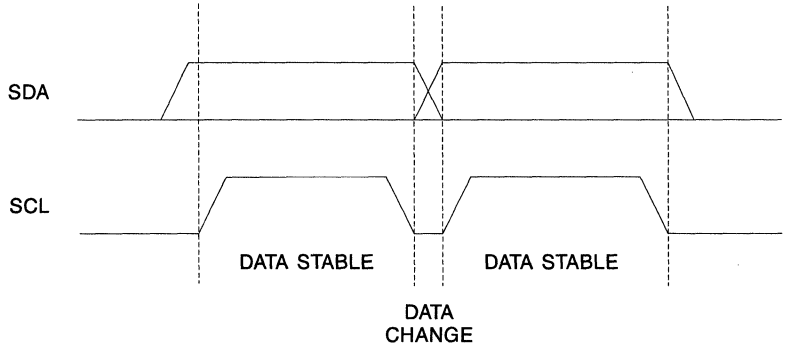


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O

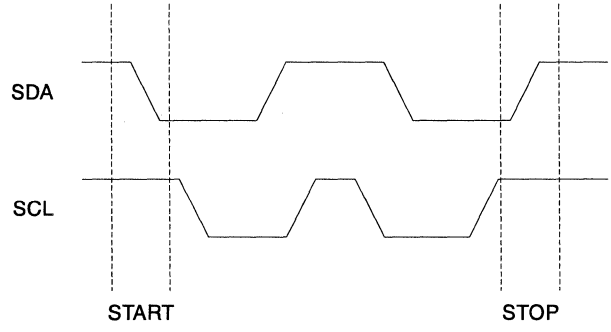


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

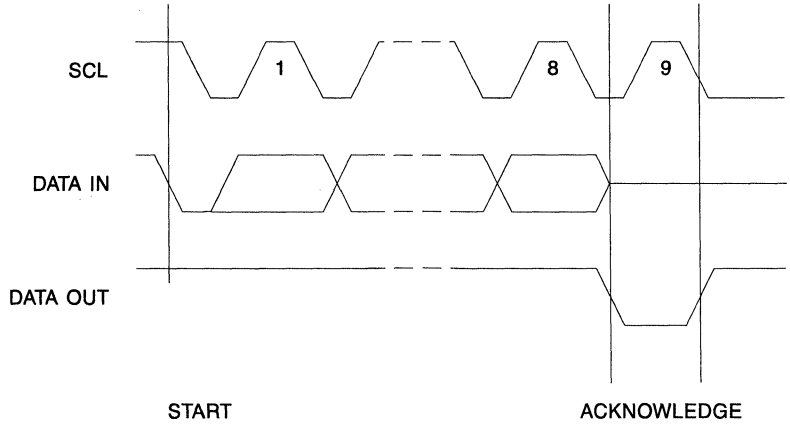
Data Validity



Start and Stop Definition



Output Acknowledge



Write Operations

BYTE WRITE: Following a start condition, a write operation requires a 7 bit data word address and a low write bit. Upon receipt of this address, the E^2PROM will again respond with a zero and then clock in the first 8 bit data word. Following receipt of the 8 bit data word, the E^2PROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the E^2PROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the E^2PROM will not respond until the write is complete (refer to Figure 1).

PAGE WRITE: The AT24C01 is capable of a 4-byte page write.

A page write is initiated the same as a byte write but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the E^2PROM acknowledges receipt of the first data word, the microcontroller can transmit up to three more data words. The E^2PROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 2).

The data word address lower 2 bits are internally incremented following the receipt of each data word. The higher five data word address bits are not incremented, retaining the memory page row location. If more than four data words are transmitted to the E^2PROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the E^2PROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the E^2PROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are two read operations: byte read and sequential read.

BYTE READ: A byte read is initiated with a start condition followed by a 7 bit data word address and a high read bit. The AT24C01 will respond with an acknowledge and then serially output 8 data bits. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 3).

SEQUENTIAL READ: Sequential reads are initiated the same as a byte read. After the microcontroller receives an 8 bit data word, it responds with an acknowledge. As long as the E^2PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

Figure 1. Byte Write

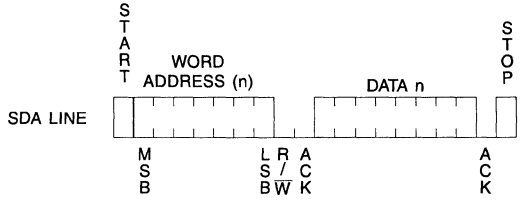


Figure 2. Page Write

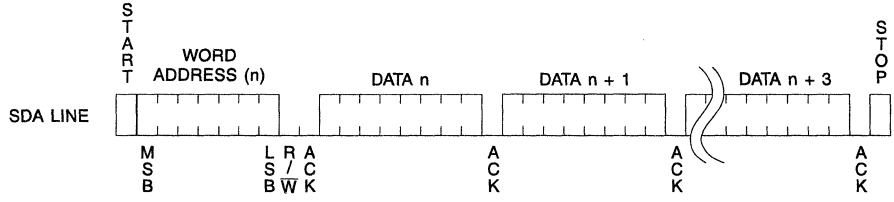


Figure 3. Byte Read

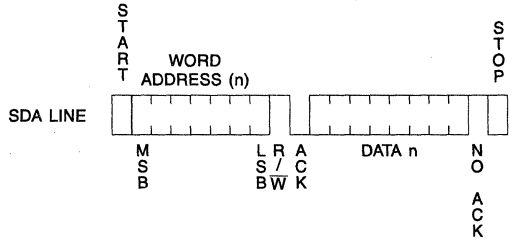
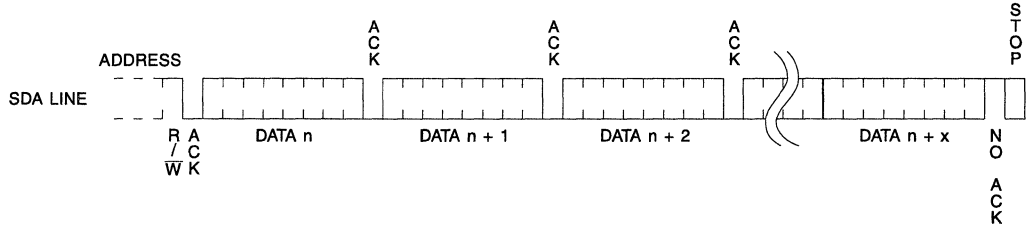


Figure 4. Sequential Read



Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C01-10PC AT24C01-10SC	8P3 8S1	Commercial (0°C to 70°C)
	3000	18	400	AT24C01-10PI AT24C01-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C01-10PC-2.7 AT24C01-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
	1500	4	100	AT24C01-10PI-2.7 AT24C01-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C01-10PC-2.5 AT24C01-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
	1000	4	100	AT24C01-10PI-2.5 AT24C01-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)
10	800	3	100	AT24C01-10PC-1.8 AT24C01-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
	800	3	100	AT24C01-10PI-1.8 AT24C01-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

2-Wire Serial CMOS E²PROM

1K (128 x 8)

Features

- 2-Wire Serial Interface
- DDC1™/ DDC2™ Interface Compliant for Monitor Identification
- Low Voltage and Standard Voltage Operation
  - 2.5 (V_{CC} = 2.5V to 5.5V)
- Internally Organized 128 x 8
- 100 kHz (2.5V) and 400 kHz (5V) Compatibility
- 8-Byte Page Write Mode
- Write Protection Available
- Self-timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Cycles
  - Data Retention: 100 Years
- 8-Pin PDIP and JEDEC SOIC Packages

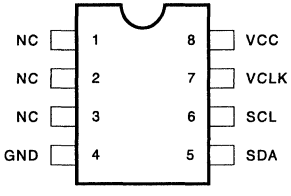
Description

The AT24C21 provides 1024 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128 words of 8 bits each. The device is optimized for use in applications requiring data storage and serial transmission of configuration and control information. The AT24C21 features two modes of operation: Transmit-Only Mode and Bi-Directional Mode. Upon power-up, the AT24C21 will be in the Transmit-Only Mode, sending a serial-bit stream of the entire memory contents, clocked via the VCLK pin. The Bi-Directional Mode is selected by a valid high-to-low transition on the SCL pin and offers byte selectable read/write capability of the entire memory array. The AT24C21 is available in space saving 8-pin PDIP and 8-pin SOIC packages.

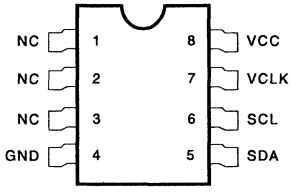
Pin Configurations

Pin Name	Function
NC	No Connect
SDA	Serial Data
SCL	Serial Clock Input (Bi-Directional Mode)
VCLK	Serial Clock Input (Transmit-Only Mode)

8-Pin PDIP



8-Pin SOIC



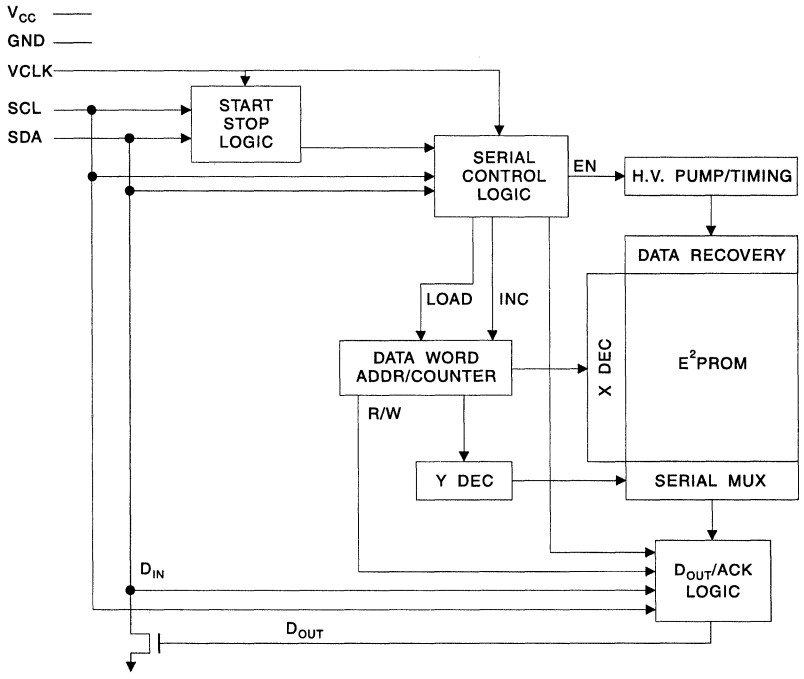
0405D

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each E^2PROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open drain or open collector devices.

SERIAL CLOCK (VCLK): Upon power-up, the device is in the Transmit-Only mode and will transmit the entire memory contents via the SDA pin with positive signals on the VCLK pin.

Memory Organization

AT24C21, 1K SERIAL E^2PROM: Internally organized with 128 pages of one byte each. The 1K requires a 7 bit data word address for random word addressing.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, T_{AC} = 0°C to +70°C, V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		2.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		3.0	4.0	µA
	V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		12.0	30.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	1.0	µA
V_{IL}	Input Low Level (1) SCL, SDA Pin				V_{CC} x 0.3	V
	Input Low Level VCLK Pin	$V_{CC} \geq 2.7V$			0.8	V
		$V_{CC} < 2.7V$			0.2 x V_{CC}	V
V_{IH}	Input High Level (1) SCL, SDA Pin		V_{CC} x 0.7		V_{CC} + 0.5	V
	Input High Level VCLK Pin		2.0			V
V_{OL}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.40	V

Note: 1. V_{IL} min and V_{IH} max are for reference only and not tested.

Pin Capacitance (1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL, VCLK)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Transmit-Only Mode

Symbol	Parameter	2.5-volt		5.0-volt		Units
		Min	Max	Min	Max	
T_{VAA}	Output valid from VCLK		500		500	ns
T_{VHIGH}	VCLK high-time	4.0		.6		µs
T_{VLOW}	VCLK low-time	4.7		1.3		µs
T_{VHZ}	Mode transition time		500		500	ns
T_{VPU}	Transmit-Only power-up time	0		0		ns

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +2.5V to +5.5V C_L = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.5-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL	0	100	0	400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.3		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time (1) (SDA and SCL pins)		NA		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	3.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		1.3		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	250		100		ns
t_R	Inputs Rise Time (1)		1.0		0.3	µs
t_F	Inputs Fall Time (1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.0		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms

Note: 1. This parameter is characterized and is not 100% tested.

Functional Description

The AT24C21 has two modes of operation: the Transmit-Only Mode and the Bi-Directional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input (SCL and VCLK) and both modes sharing a common bi-directional data line (SDA). The AT24C21 enters the Transmit-Only Mode upon powering up the device. In this mode, the device transmits data on the SDA pin upon a clock signal on the VCLK pin. The device will remain in the Transmit-Only Mode until a valid high-to-low transition takes place on the SCL pin. The device will switch into the Bi-Directional Mode when a valid transition on the SCL pin is recognized. Once the device has transitioned to the Bi-Directional Mode, there is no way to return to the Transmit-Only Mode, except to power down (reset) the device.

Transmit-Only Mode (DDC1)

The AT24C21 will power up in the Transmit-Only Mode. In this mode, the device will output one bit of data on the SDA pin on each rising edge on the VCLK pin. Data is transmitted in 8 bit words with the most significant bit first. Each word is followed by a 9th "don't care" bit which will be in high impedance state (refer to Figure 1). The AT24C21 will continuously cycle through the entire memory array in incremental sequence as long a VCLK is present and no falling edges on SCL are received. When the maximum address (7FH) is reached, the ouput will wrap around to the zero location (00H) and continue. The Bi-Directional mode clock (SCL) pin must be held high for the device to remain in the Transmit-Only mode.

Upon power-up, the AT24C21 will not output valid data until it has been initialized. During initialization, data will not be available until after the first nine clocks are sent to the device (refer to Figure 2). The starting address for the Transmit-Only mode can be determined during initialization. If the SDA pin is held high during the first eight clocks (refer to Figure 2), the starting address will be 7FH. If the SDA pin is low during the first eight clocks, the starting address will be 00H. During the ninth clock, SDA should be in high impedance.

Figure 1. Transmit-Only Mode

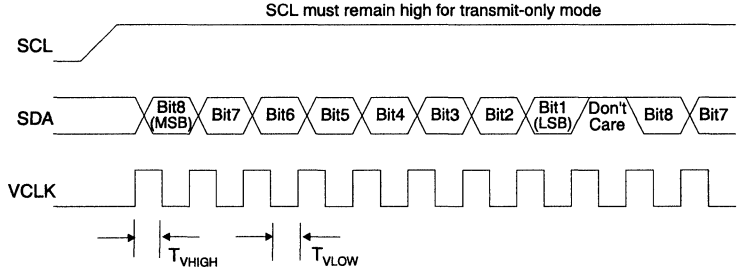
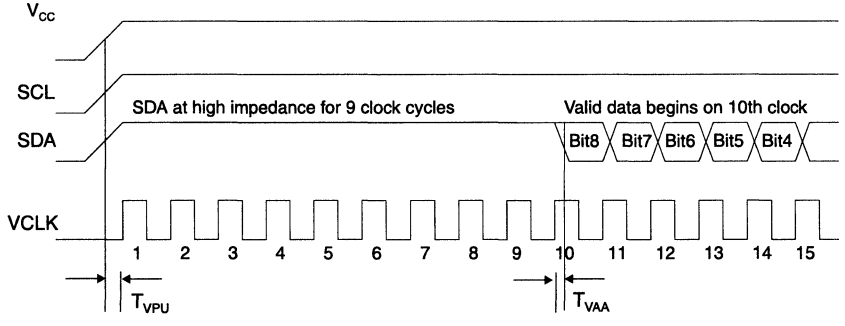


Figure 2. Device Initialization for Transmit-Only Mode



Bi-Directional Mode (DDC2)

This mode supports a 2-wire, bi-directional data transmission protocol. The AT24C21 can be switched into the Bi-Directional Mode by issuing a valid high to low transition on the SCL pin (refer to Figure 3). After the device is in the Bi-Directional Mode, all inputs to the VCLK pin are ignored, except when a logic high is required to enable write capability. All byte and page writes and byte and sequential reads are supported in this mode.

Bi-Directional Mode Operation:

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read or write sequence, the stop command will place the E^2PROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E^2PROM in 8 bit words. The E^2PROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Device Addressing

The AT24C21 requires an 8 bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 4).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the E^2PROM devices.

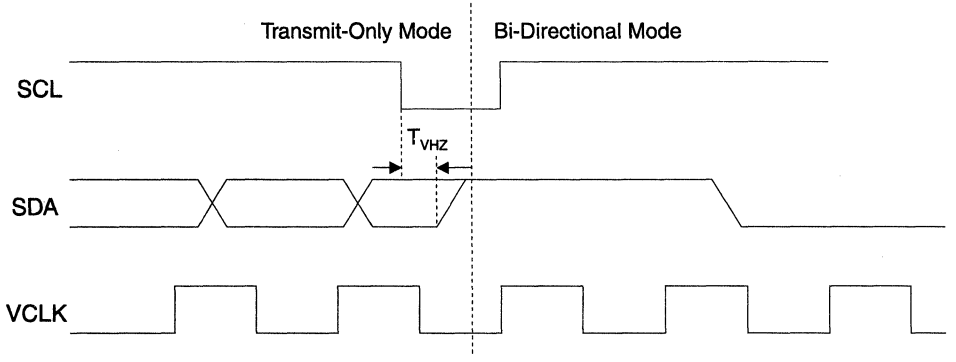
The next three bits are don't care for the AT24C21.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

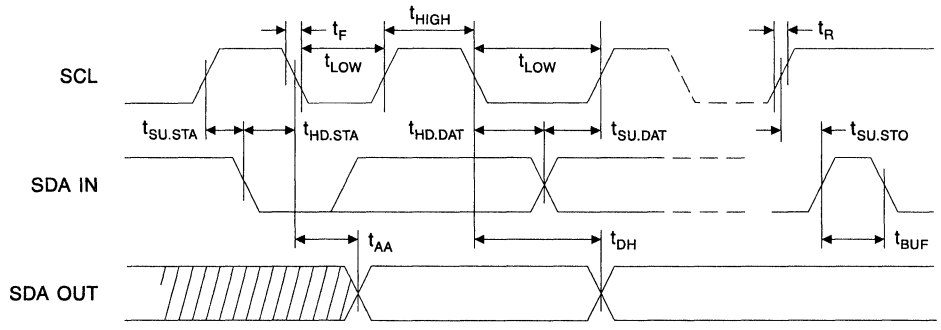
Upon a compare of the device address, the E^2PROM will output a zero. If a compare is not made, the chip will return to a standby state.

STANDBY MODE: The AT24C21 features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

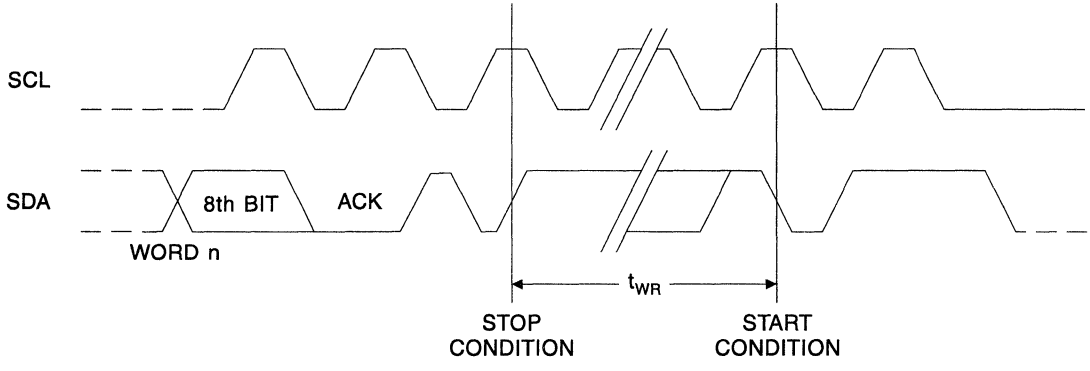
Figure 3. Mode Transition



Bus Timing SCL: Serial Clock SDA: Serial Data I/O

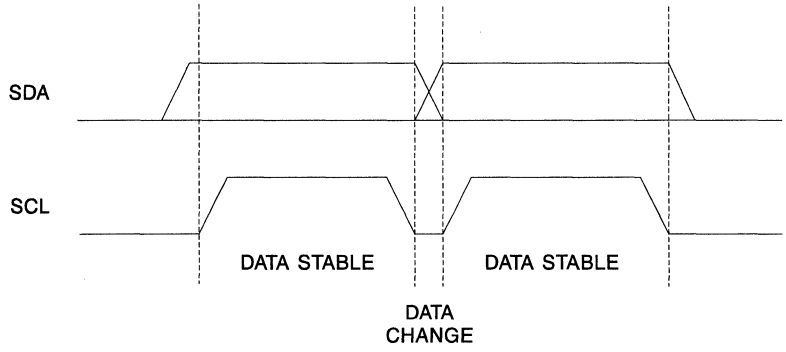


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O

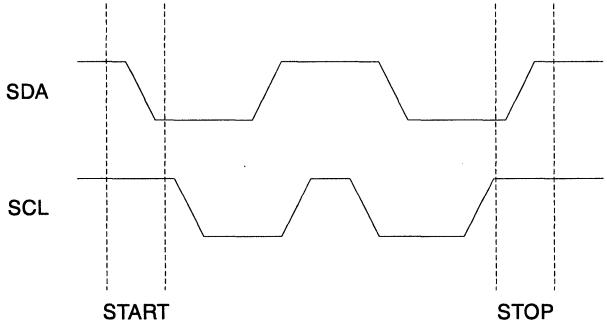


Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

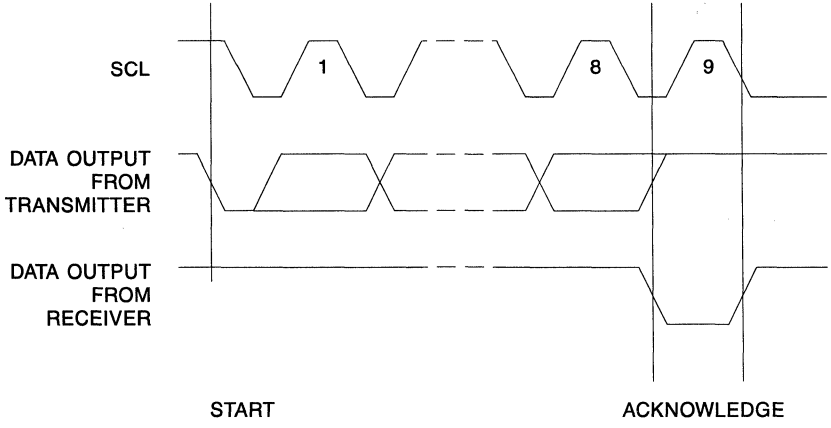
Data Validity



Start and Stop Definition



Output Acknowledge



Write Operations

BYTE WRITE: A write operation requires an 8 bit data word addresses following the device address word and acknowlegement. Upon receipt of this address, the E^2PROM will again respond with a zero and then clock in the first 8 bit data word. Following receipt of the 8 bit data word, the E^2PROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the E^2PROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the E^2PROM will not respond until the write is complete (refer to Figure 5).

It is required that VCLK be held at a high logic level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

PAGE WRITE: The AT24C21 is capable of an 8-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the E^2PROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven more data words. The E^2PROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 6).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. If more than eight data words are transmitted to the E^2PROM, the data word address will "roll over" and previous data will be overwritten. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

It is required that VCLK be held at a high logic level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the E^2PROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the E^2PROM respond with a zero allowing the read or write sequence to continue.

WRITE PROTECTION: When VCLK pin is connected to GND and in the Bi-Directional Mode, the entire memory is protected and becomes ROM only. This protects the device memory from any inadvertent write operations.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device. Furthermore, the AT24C21 employs a low V_{CC} detector circuit which disables the erase\write logic whenever V_{CC} falls below 1.5 volts.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the E^2PROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 7).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the E^2PROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The E^2PROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 8).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the E^2PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 9).

Figure 4. Device Address

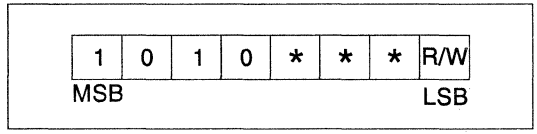


Figure 5. Byte Write

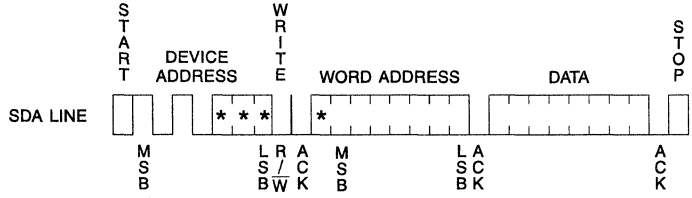
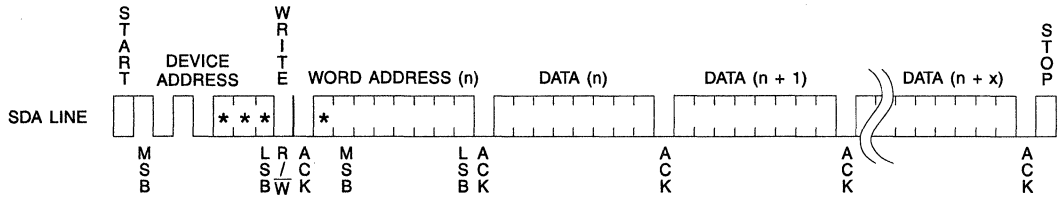


Figure 6. Page Write



(* = Don't care bits)

Figure 7. Current Address Read

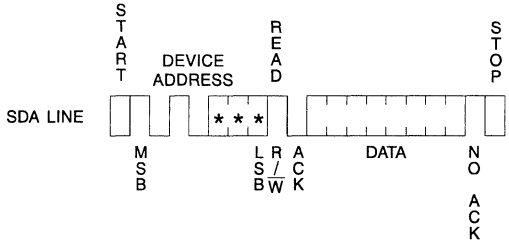


Figure 8. Random Read

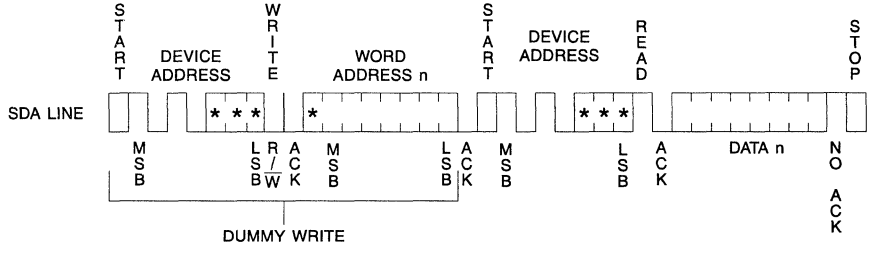
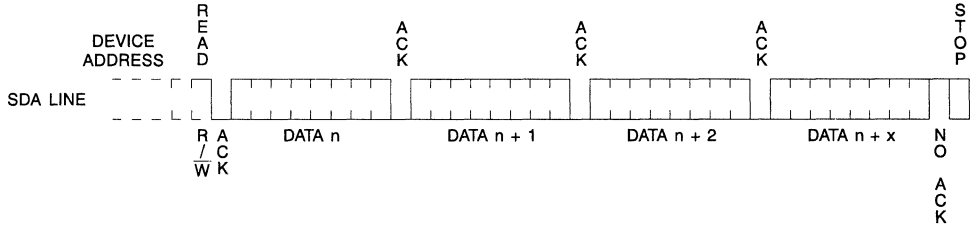


Figure 9. Sequential Read



(* = Don't care bits)

Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	4	400	AT24C21-10PC-2.5 AT24C21-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
	3000	4	400	AT24C21-10PI-2.5 AT24C21-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
-2.5	Low Voltage (2.5V to 5.5V)

2-Wire Serial CMOS E²PROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

Features

- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)
- 2-Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Cycles
  - Data Retention: 100 Years
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin and 14-Pin JEDEC SOIC and 8-Pin PDIP Packages

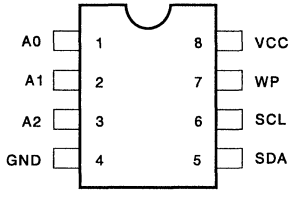
Description

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01A/02/04/08/16 is available in space saving 8-pin PDIP, 8-pin and 14-pin SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

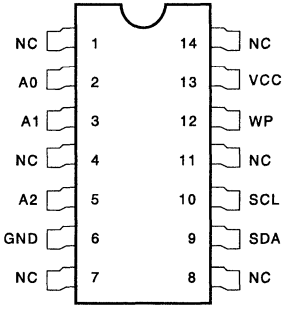
Pin Configurations

Pin Name	Function
A_0 to A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

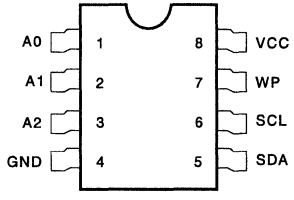
8-Pin PDIP



14-Pin SOIC



8-Pin SOIC



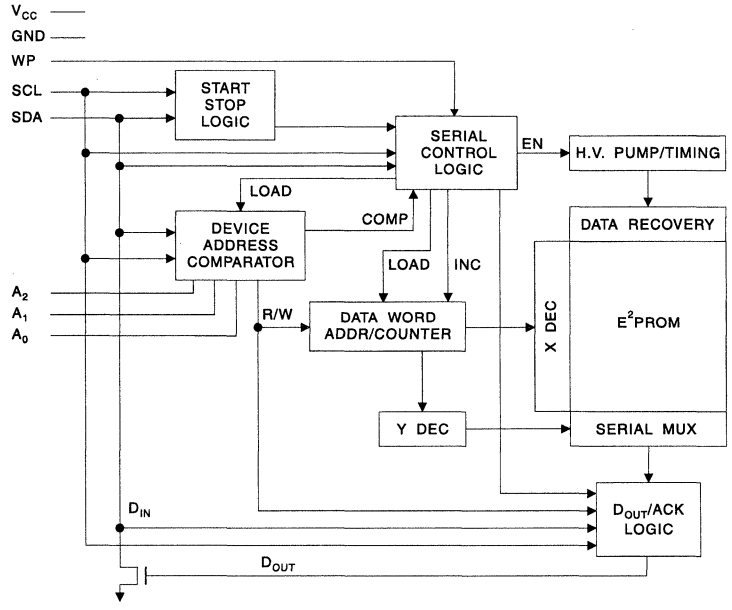
0180C

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each E^2PROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16 does not use the device address pins which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

(continued)

Pin Description (Continued)

WRITE PROTECT (WP): The AT24C01A/02/04/16 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

WP Pin Status	Part of the Array Protected				
	24C01A	24C02	24C04	24C08	24C16
At V_{CC}	Full (1K) Array	Full (2K) Array	Full (4K) Array	Normal Read/Write Operation	Upper Half (8K) Array
At GND	Normal Read/Write Operations				

Memory Organization

AT24C01A, 1K SERIAL E²PROM: Internally organized with 128 pages of 1-byte each, the 1K requires a 7 bit data word address for random word addressing.

AT24C02, 2K SERIAL E²PROM: Internally organized with 256 pages of 1-byte each, the 2K requires an 8 bit data word address for random word addressing.

AT24C04, 4K SERIAL E²PROM: The 4K is internally organized with 256 pages of 2-bytes each. Random word addressing requires a 9 bit data word address.

AT24C08, 8K SERIAL E²PROM: The 8K is internally organized with 4 blocks of 256 pages of 4-bytes each. Random word addressing requires a 10 bit data word address.

AT24C16, 16K SERIAL E²PROM: The 16K is internally organized with 8 blocks of 256 pages of 8-bytes each. Random word addressing requires an 11 bit data word address.

Pin Capacitance (1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level (1)		-1.0		V_{CC} x 0.3	V
V_{IH}	Input High Level (1)		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time (1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start (1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time (1)		1.0		0.3	µs
t_F	Inputs Fall Time (1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms

Note: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

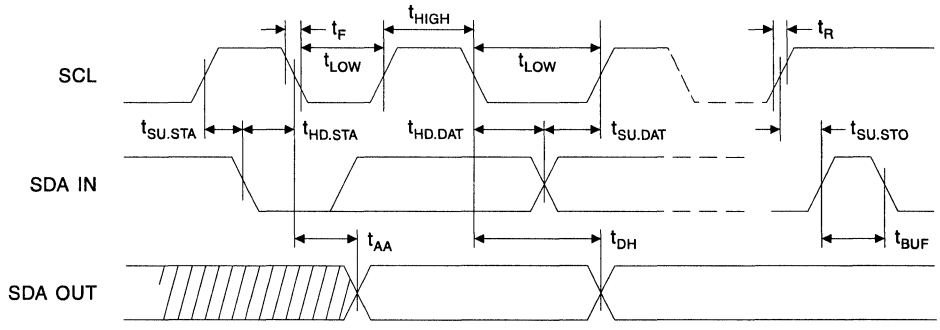
START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the E^2PROM in a standby power mode (refer to Start and Stop Definition timing diagram).

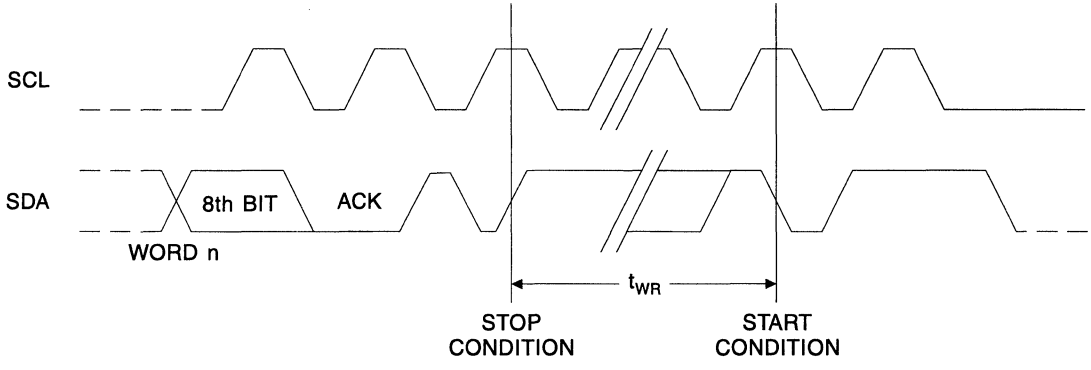
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E^2PROM in 8 bit words. The E^2PROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C01A/02/04/08/16 features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

Bus Timing SCL: Serial Clock SDA: Serial Data I/O

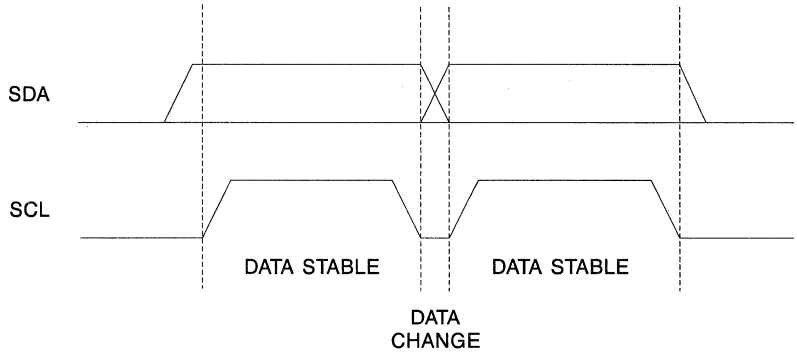


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O

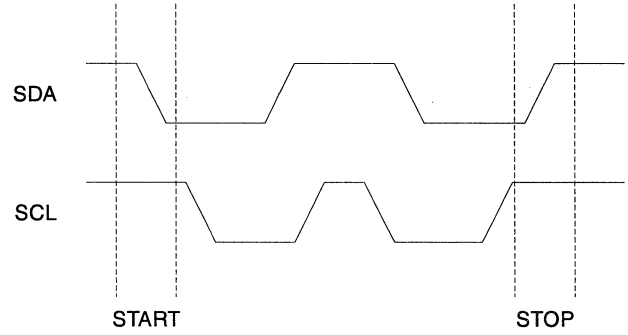


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

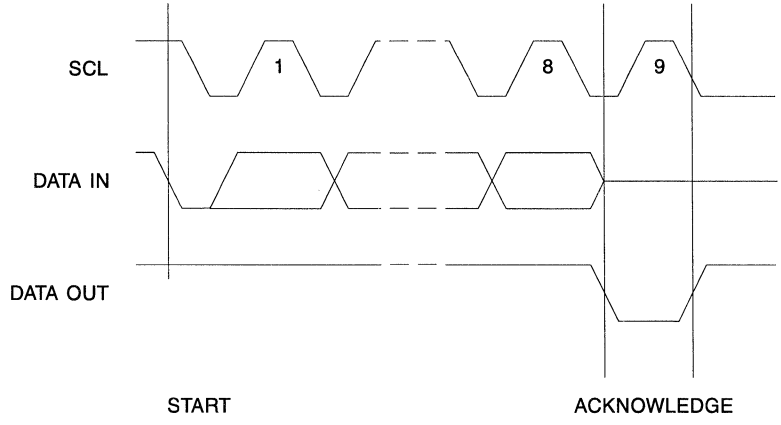
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The 1K, 2K, 4K, 8K and 16K E^2PROM devices all require an 8 bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the E^2PROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 1K/2K E^2PROM. These 3 bits must compare to their corresponding hard-wired input pins.

The 4K E^2PROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins. The A0 pin is no connect.

The 8K E^2PROM only uses the A2 device address bit with the next 2 bits being for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connect.

The 16K does not use any device address bits but instead the 3 bits are used for memory page addressing. These page addressing bits on the 4K, 8K, and 16K devices should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the E^2PROM will output a zero. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8 bit data word address following the device address word and acknowledgement. Upon receipt of this address, the E^2PROM will again respond with a zero and then clock in the first 8 bit data word. Following receipt of the 8 bit data word, the E^2PROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the E^2PROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the E^2PROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The 1K/2K E^2PROM is capable of an 8-byte page write, and the 4K, 8K and 16K devices are capable of 16-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the E^2PROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (1K/2K) or fifteen (4K, 8K, 16K) more data words. The E^2PROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower three (1K/2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. If more than eight (1K/2K) or sixteen (4K, 8K, 16K) data words are transmitted to the E^2PROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the E^2PROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the E^2PROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the E^2PROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the E^2PROM, the micro-

(continued)

Read Operations (Continued)

controller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The E²PROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the E²PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

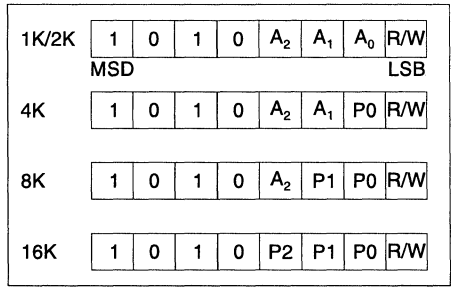


Figure 2. Byte Write

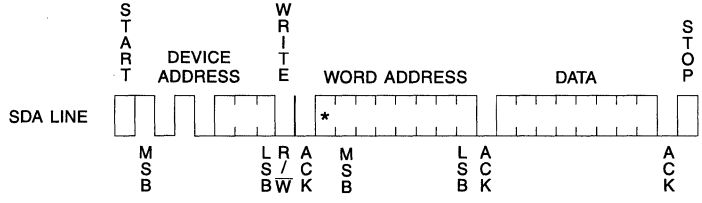
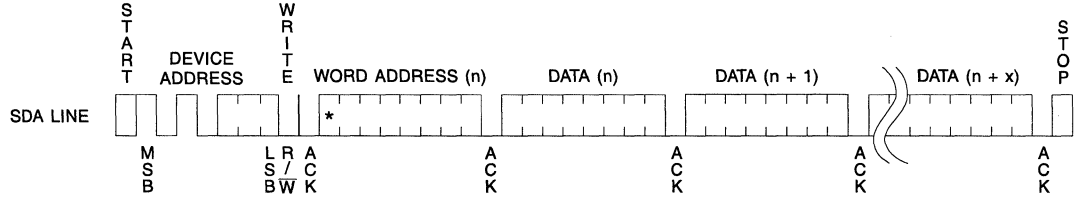


Figure 3. Page Write



(* = DON'T CARE bit for 1K)

Figure 4. Current Address Read

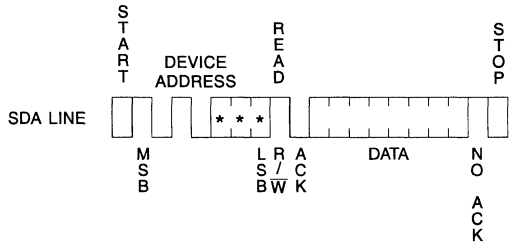
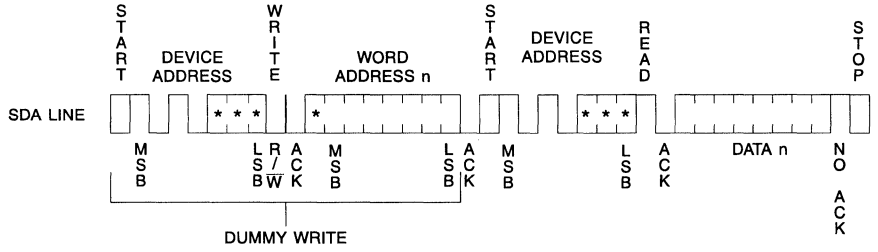
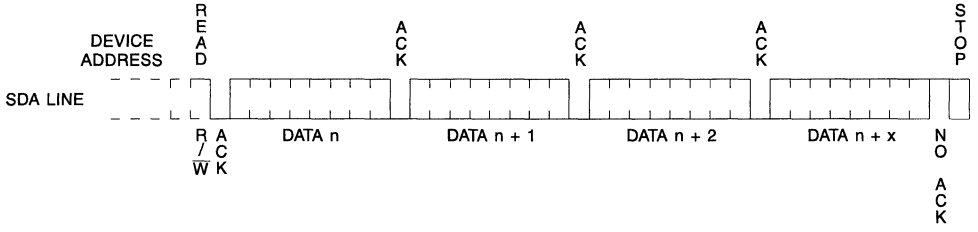


Figure 5. Random Read



(* = DON'T CARE bit for 1K)

Figure 6. Sequential Read



Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C01A-10PC AT24C01A-10SC	8P3 8S1	Commercial (0°C to 70°C)
	3000	18	400	AT24C01A-10PI AT24C01A-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C01A-10PC-2.7 AT24C01A-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
	1500	4	100	AT24C01A-10PI-2.7 AT24C01A-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C01A-10PC-2.5 AT24C01A-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
	1000	4	100	AT24C01A-10PI-2.5 AT24C01A-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)
10	800	3	100	AT24C01A-10PC-1.8 AT24C01A-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
	800	3	100	AT24C01A-10PI-1.8 AT24C01A-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C02-10PC AT24C02N-10SC AT24C02-10SC	8P3 8S1 14S	Commercial (0°C to 70°C)
	3000	18	400	AT24C02-10PI AT24C02N-10SI AT24C02-10SI	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C02-10PC-2.7 AT24C02N-10SC-2.7 AT24C02-10SC-2.7	8P3 8S1 14S	Commercial (0°C to 70°C)
	1500	4	100	AT24C02-10PI-2.7 AT24C02N-10SI-2.7 AT24C02-10SI-2.7	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C02-10PC-2.5 AT24C02N-10SC-2.5 AT24C02-10SC-2.5	8P3 8S1 14S	Commercial (0°C to 70°C)
	100	4	100	AT24C02-10PI-2.5 AT24C02N-10SI-2.5 AT24C02-10SI-2.5	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	800	3	100	AT24C02-10PC-1.8 AT24C02N-10SC-1.8 AT24C02-10SC-1.8	8P3 8S1 14S	Commercial (0°C to 70°C)
	800	3	100	AT24C02-10PI-1.8 AT24C02N-10SI-1.8 AT24C02-10SI-1.8	8P3 8S1 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C04-10PC AT24C04N-10SC AT24C04-10SC	8P3 8S1 14S	Commercial (0°C to 70°C)
	3000	18	400	AT24C04-10PI AT24C04N-10SI AT24C04-10SI	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C04-10PC-2.7 AT24C04N-10SC-2.7 AT24C04-10SC-2.7	8P3 8S1 14S	Commercial (0°C to 70°C)
	1500	4	100	AT24C04-10PI-2.7 AT24C04N-10SI-2.7 AT24C04-10SI-2.7	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C04-10PC-2.5 AT24C04N-10SC-2.5 AT24C04-10SC-2.5	8P3 8S1 14S	Commercial (0°C to 70°C)
	1000	4	100	AT24C04-10PI-2.5 AT24C04N-10SI-2.5 AT24C04-10SI-2.5	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	800	3	100	AT24C04-10PC-1.8 AT24C04N-10SC-1.8 AT24C04-10SC-1.8	8P3 8S1 14S	Commercial (0°C to 70°C)
	800	3	100	AT24C04-10PI-1.8 AT24C04N-10SI-1.8 AT24C04-10SI-1.8	8P3 8S1 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C08-10PC AT24C08N-10SC AT24C08-10SC	8P3 8S1 14S	Commercial (0°C to 70°C)
	3000	18	400	AT24C08-10PI AT24C08N-10SI AT24C08-10SI	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C08-10PC-2.7 AT24C08N-10SC-2.7 AT24C08-10SC-2.7	8P3 8S1 14S	Commercial (0°C to 70°C)
	1500	4	100	AT24C08-10PI-2.7 AT24C08N-10SI-2.7 AT24C08-10SI-2.7	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C08-10PC-2.5 AT24C08N-10SC-2.5 AT24C08-10SC-2.5	8P3 8S1 14S	Commercial (0°C to 70°C)
	1000	4	100	AT24C08-10PI-2.5 AT24C08N-10SI-2.5 AT24C08-10SI-2.5	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	800	3	100	AT24C08-10PC-1.8 AT24C08N-10SC-1.8 AT24C08-10SC-1.8	8P3 8S1 14S	Commercial (0°C to 70°C)
	800	3	100	AT24C08-10PI-1.8 AT24C08N-10SI-1.8 AT24C08-10SI-1.8	8P3 8S1 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C16-10PC AT24C16N-10SC AT24C16-10SC	8P3 8S1 14S	Commercial (0°C to 70°C)
	3000	18	400	AT24C16-10PI AT24C16N-10SI AT24C16-10SI	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C16-10PC-2.7 AT24C16N-10SC-2.7 AT24C16-10SC-2.7	8P3 8S1 14S	Commercial (0°C to 70°C)
	1500	4	100	AT24C16-10PI-2.7 AT24C16N-10SI-2.7 AT24C16-10SI-2.7	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C16-10PC-2.5 AT24C16N-10SC-2.5 AT24C16-10SC-2.5	8P3 8S1 14S	Commercial (0°C to 70°C)
	1000	4	100	AT24C16-10PI-2.5 AT24C16N-10SI-2.5 AT24C16-10SI-2.5	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	800	3	100	AT24C16-10PC-1.8 AT24C16N-10SC-1.8 AT24C16-10SC-1.8	8P3 8S1 14S	Commercial (0°C to 70°C)
	800	3	100	AT24C16-10PI-1.8 AT24C16N-10SI-1.8 AT24C16-10SI-1.8	8P3 8S1 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

2-Wire Serial CMOS E²PROM

16K (2048 x 8)

Features

- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 2048 x 8 (16K)
- 2-Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- Cascadable Feature Allows for Extended Densities
- 16-Byte Page Write Mode
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Cycles
  - Data Retention: 100 Years
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin JEDEC SOIC and 8-Pin PDIP Packages

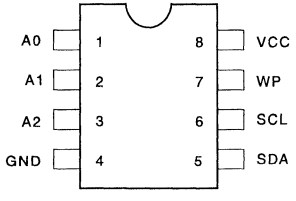
Description

The AT24C164 provides 16,384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 2048 words of 8 bits each. The device's cascadable feature allows up to eight devices (128K) to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C164 is available in space saving 8-pin PDIP and 8-pin SOIC packages and is accessed via a 2-wire serial interface. In addition, this device is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

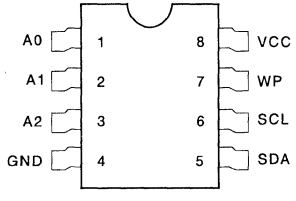
Pin Configurations

Pin Name	Function
A_0 to A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

8-Pin PDIP



8-Pin SOIC



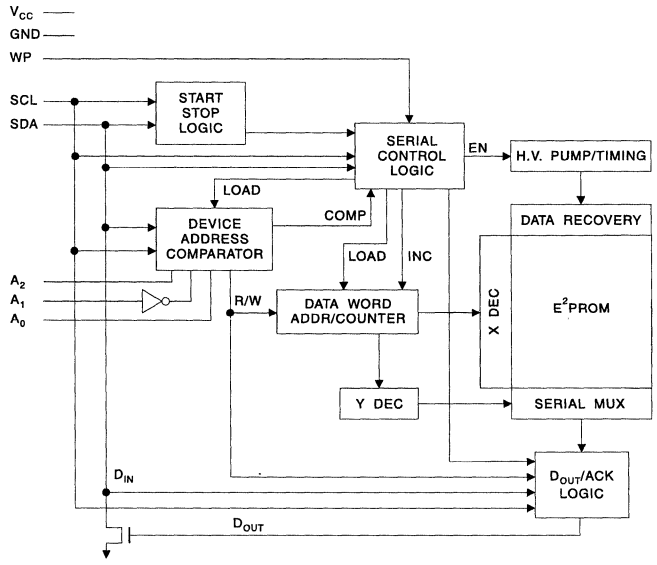
0105C

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each E^2PROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE SELECT (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that may be hardwired or actively driven to V_{DD} or V_{SS}. These inputs allow the selection for one of eight possible devices sharing a common bus. The AT24C164 can be made compatible with the AT24C16 by tying A2, A1 and A0 to V_{SS}. Device addressing is discussed in detail in the device addressing section.

WRITE PROTECT (WP): The write protect input, when tied low to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the memory are inhibited.

Memory Organization

The AT24C164 is internally organized with 256 pages of 8-bytes each. Random word addressing requires an 11 bit data word address.

Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Standby Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Standby Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level [1]		-1.0		V_{CC} x 0.3	V
V_{IH}	Input High Level [1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time (1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start (1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time (1)		1.0		0.3	µs
t_F	Inputs Fall Time (1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

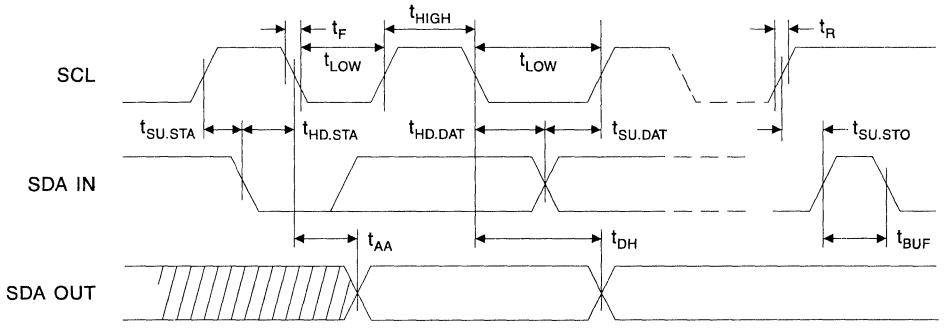
START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the E^2PROM in a standby power mode (refer to Start and Stop Definition timing diagram).

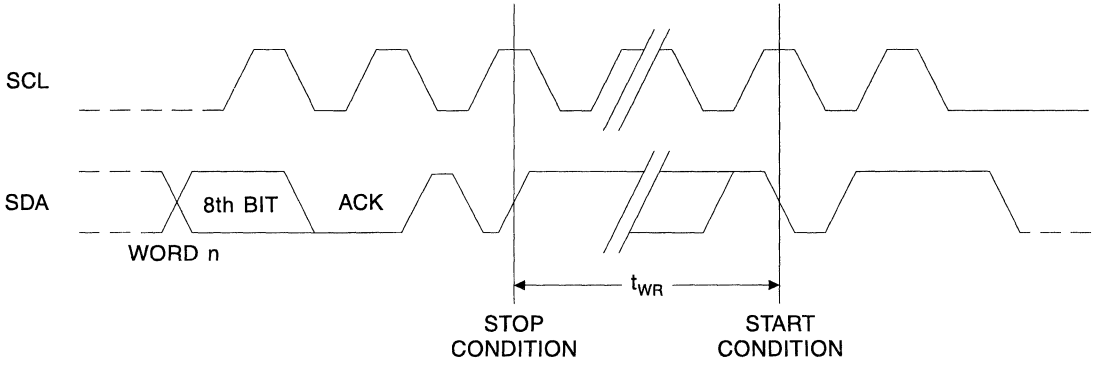
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E^2PROM in 8 bit words. The E^2PROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C164 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

Bus Timing SCL: Serial Clock SDA: Serial Data I/O

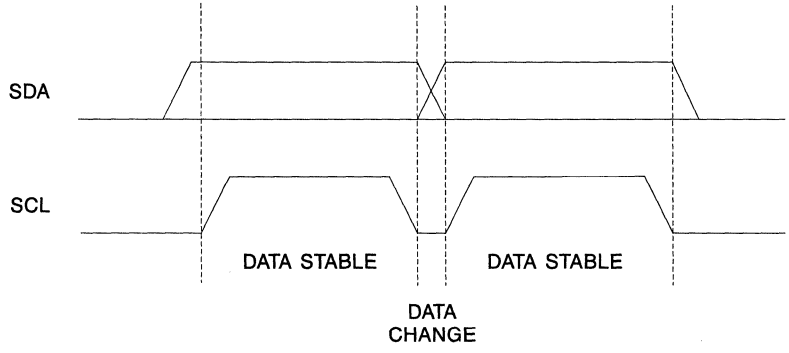


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O

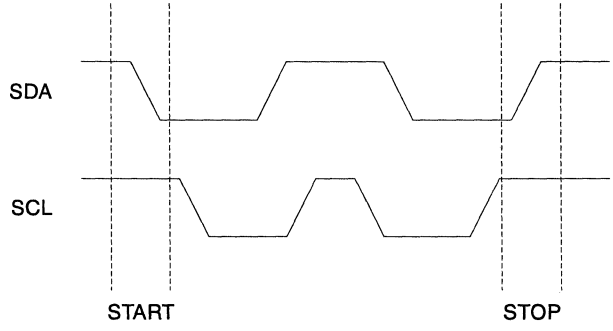


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

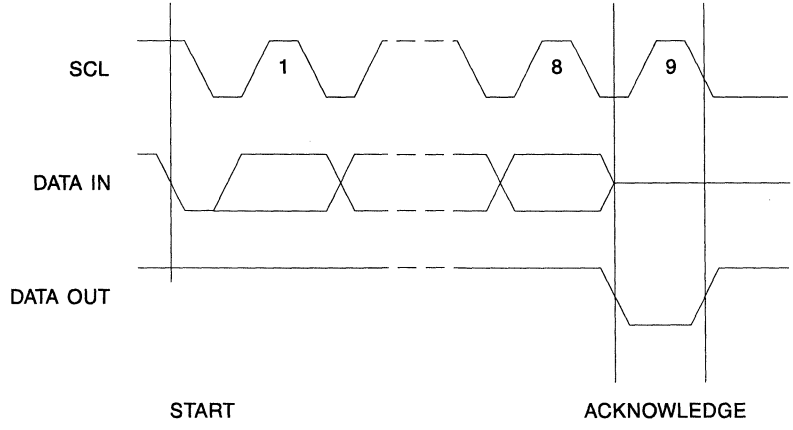
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The AT24C164 requires an 8 bit device address word following a start condition to enable the chip for read or write operations (refer to Figure 1). The most significant bit must be a one followed by the A2, A1 and A0 device select bits (the A1 bit must be the compliment of the A1 input pin signal). The next 3 bits are used for memory block addressing and select one of the eight 256 x 8 memory blocks. These bits should be considered the three most significant bits of the data word address. The eighth bit of the device address is the read/write select bit. A read operation is selected if this bit is high or a write operation is selected if this bit is low.

Upon a compare of the device address, the E^2PROM will output a zero. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8 bit data word address following the device address word and acknowledgement. Upon receipt of this address, the E^2PROM will again respond with a zero and then clock in the first 8 bit data word. Following receipt of the 8 bit data word, the E^2PROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the E^2PROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the E^2PROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The AT24C164 is capable of a 16-byte page write. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the E^2PROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The E^2PROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower 4 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented retaining the memory page row location. If more than sixteen data words are transmitted to the E^2PROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the E^2PROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the E^2PROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the E^2PROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the E^2PROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The E^2PROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the E^2PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

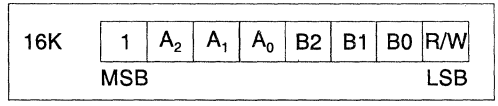


Figure 2. Byte Write

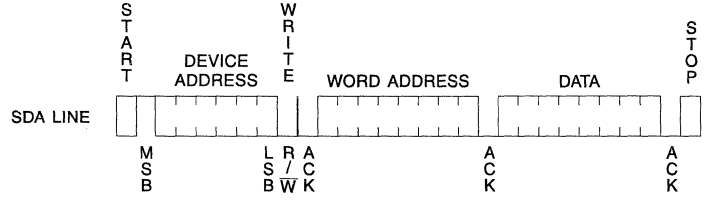


Figure 3. Page Write

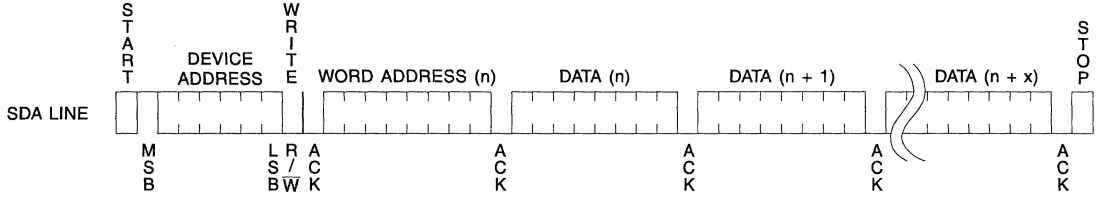


Figure 4. Current Address Read

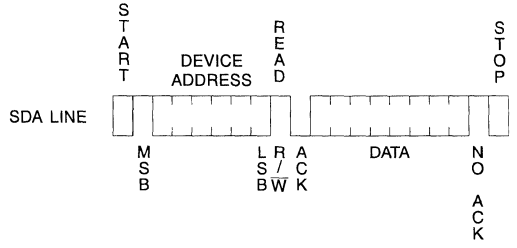


Figure 5. Random Read

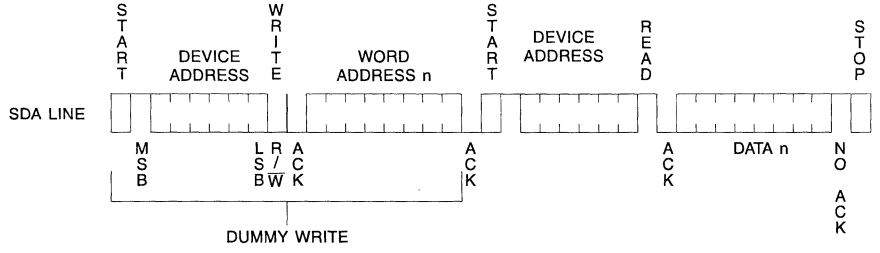
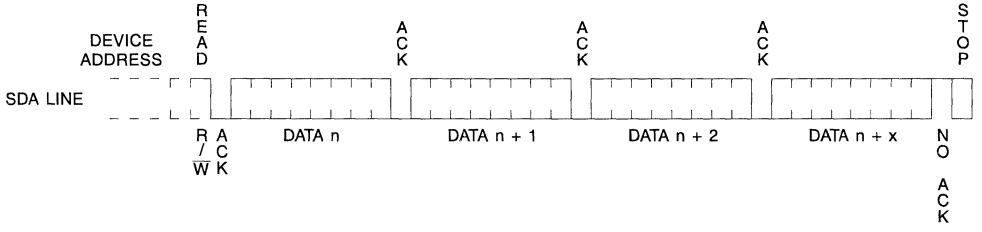


Figure 6. Sequential Read



Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C164-10PC AT24C164-10SC	8P3 8S1	Commercial (0°C to 70°C)
	3000	18	400	AT24C164-10PI AT24C164-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C164-10PC-2.7 AT24C164-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
	1500	4	100	AT24C164-10PI-2.7 AT24C164-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C164-10PC-2.5 AT24C164-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
	1000	4	100	AT24C164-10PI-2.5 AT24C164-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)
10	800	4	100	AT24C164-10PC-1.8 AT24C164-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
	800	4	100	AT24C164-10PI-1.8 AT24C164-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

2-Wire Serial CMOS E²PROM

32K (4096 x 8)

64K (8192 x 8)

Features

- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Low Power Devices (I_{SB} = 2 µA @ 5.5V) Available
- Internally Organized 4096 x 8, 8192 x 8
- 2-Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 32-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Cycles
  - Data Retention: 100 Years
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin JEDEC PDIP, 8-Pin and 14-Pin JEDEC SOIC and 8-Pin EIAJ Packages

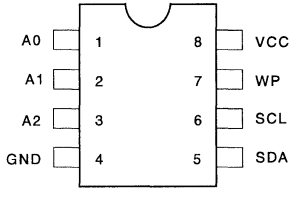
Description

The AT24C32/64 provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32/64 is available in space saving 8-pin JEDEC PDIP, 8-pin and 14-pin JEDEC SOIC and 8-pin EIAJ packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

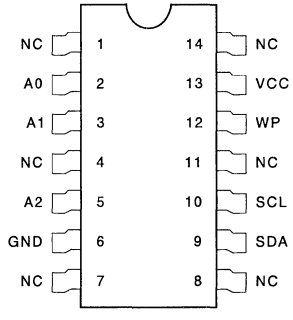
Pin Configurations

Pin Name	Function
A_0 to A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

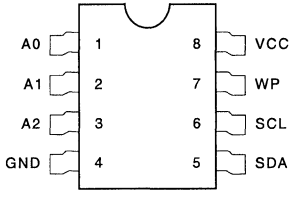
8-Pin PDIP



14-Pin SOIC



8-Pin SOIC



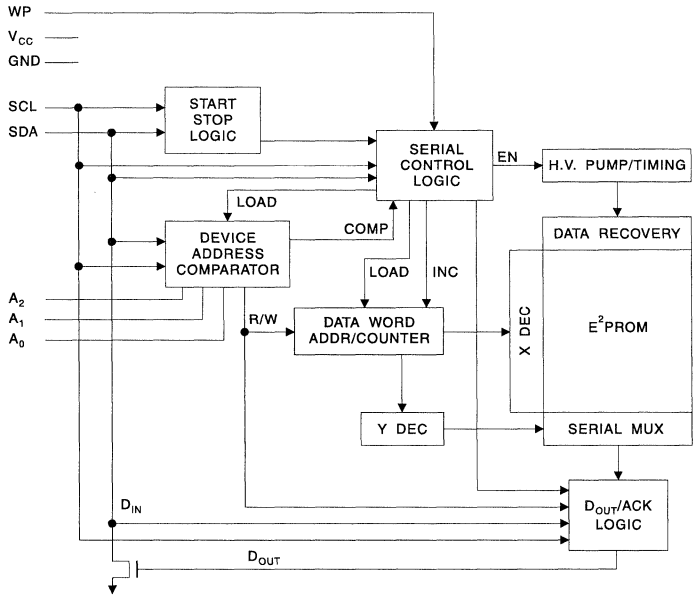
0336D

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each E^2PROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with AT24C16. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A_2, A_1, and A_0 are zero.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the upper quandrant (8/16K bits) of memory are inhibited. If left unconnected, WP is internally pulled down to GND.

Memory Organization

AT24C32/64, 32K/64K SERIAL E^2PROM: The 32K/64K is internally organized as 256 pages of 32-bytes each. Random word addressing requires a 12/13 bit data word address.

Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter		Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current V_{CC} = 5.0V		READ at 100 kHz		0.4	1.0	mA
I_{CC2}	Supply Current V_{CC} = 5.0V		WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}			0.1	µA
		V_{CC} = 5.5V				2.0	
I_{SB2}	Standby Current (2.5V option)	V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}			0.5	µA
		V_{CC} = 5.5V				2.0	
I_{SB3}	Standby Current (2.7V option)	V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}			0.5	µA
		V_{CC} = 5.5V				2.0	
I_{SB4} [1]	Standby Current (5V option)	V_{CC} = 4.5 - 5.5V	V_{IN} = V_{CC} or V_{SS}		20	35	µA
I_{LI}	Input Leakage Current		V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current		V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level [2]			-1.0		V_{CC} x 0.3	V
V_{IH}	Input High Level [2]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V		I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V		I_{OL} = 0.15 mA			0.2	V

Notes: 1. V_{CC} lockout = 3.8V.
2. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	1.8-volt		2.7-, 2.5-volt		5.0-volt		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		4.0		0.6		µs
t_I	Noise Suppression Time (1)		100		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start (1)	4.7		4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		200		100		ns
t_R	Inputs Rise Time (1)		1.0		1.0		0.3	µs
t_F	Inputs Fall Time (1)		300		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		100		50		ns
t_{WR}	Write Cycle Time		20		10		10	ms

Note: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

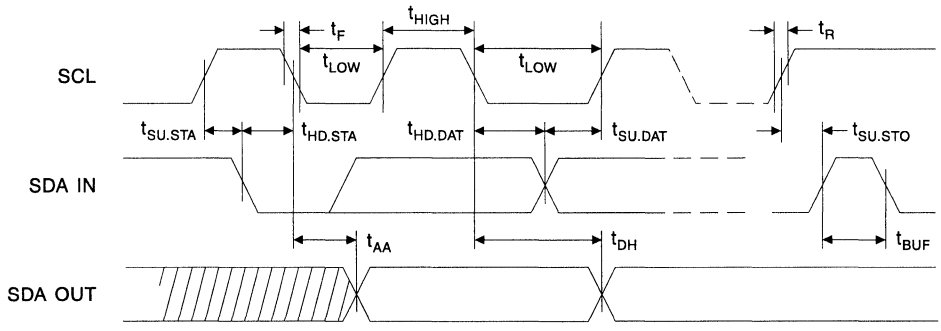
START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the E^2PROM in a standby power mode (refer to Start and Stop Definition timing diagram).

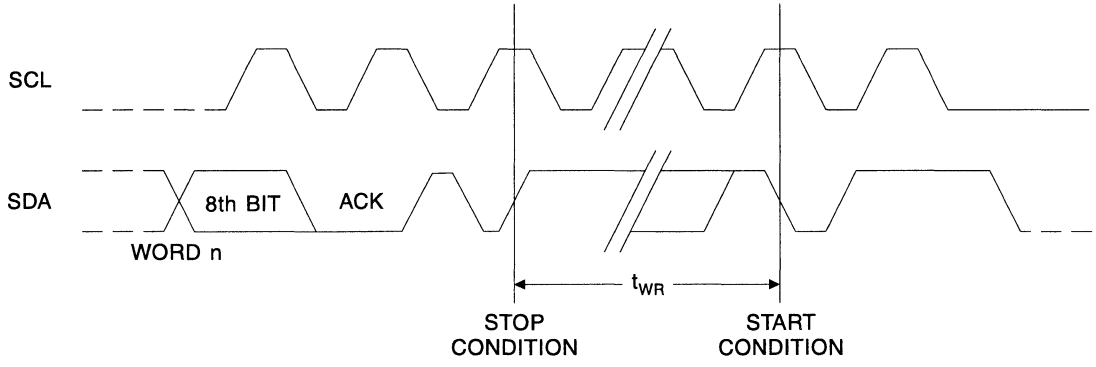
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E^2PROM in 8 bit words. The E^2PROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE: The AT24C32/64 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

Bus Timing SCL: Serial Clock SDA: Serial Data I/O

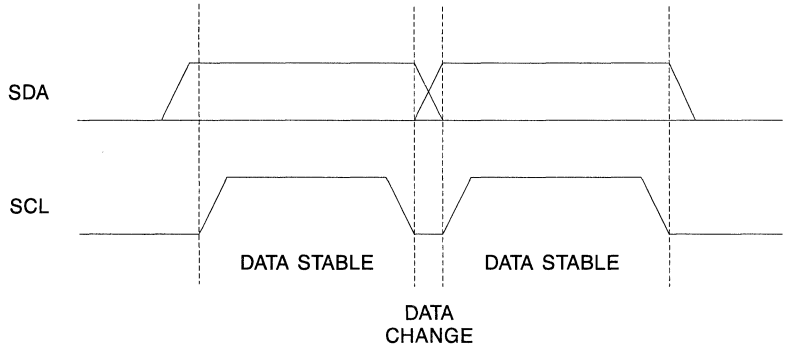


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O

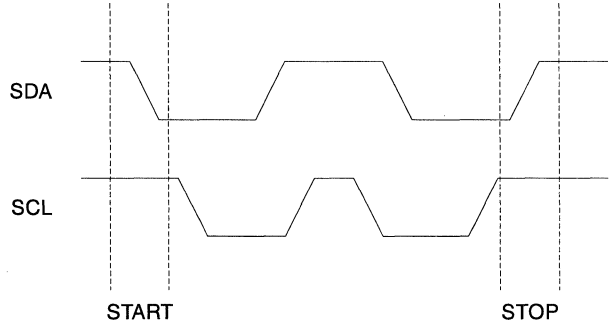


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

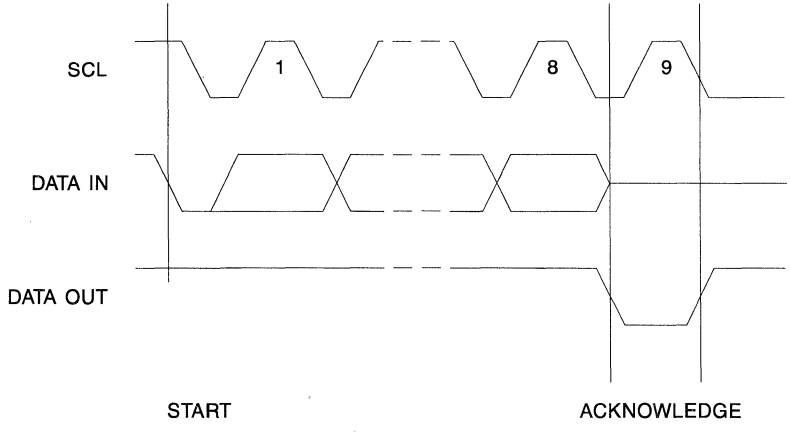
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The 32K/64K E^2PROM requires an 8 bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire E^2PROM devices.

The 32K/64K uses the three device address bits A_2, A_1, A_0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A_2, A_1, and A_0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the E^2PROM will output a zero. If a compare is not made, the device will return to standby state.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device. A low-V_{CC} detector (5-volt option) resets the device to prevent data corruption in a noisy environment.

DATA SECURITY: The AT24C32/64 has a hardware data protection scheme that allows the user to write protect the upper quadrant (8/16K bits) of memory when the WP pin is at V_{CC}.

Write Operations

BYTE WRITE: A write operation requires two 8 bit data word addresses following the device address word and acknowledgement. Upon receipt of this address, the E^2PROM will again respond with a zero and then clock in the first 8 bit data word. Following receipt of the 8 bit data word, the E^2PROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the E^2PROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the E^2PROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The 32K/64K E^2PROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the E^2PROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The E^2PROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower 5 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. If more than 32 data words are transmitted to the E^2PROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the E^2PROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the E^2PROM respond with a zero, allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page, to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the E^2PROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the E^2PROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The E^2PROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

(continued)

Read Operations (Continued)

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the E^2PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

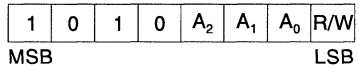


Figure 2. Byte Write

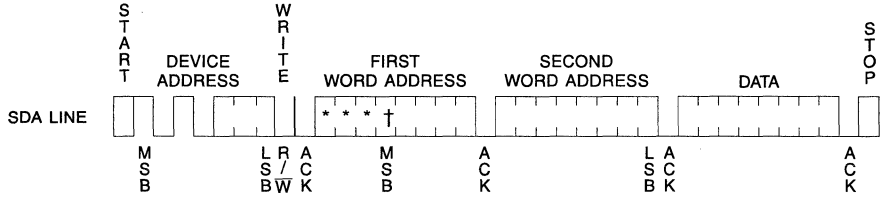
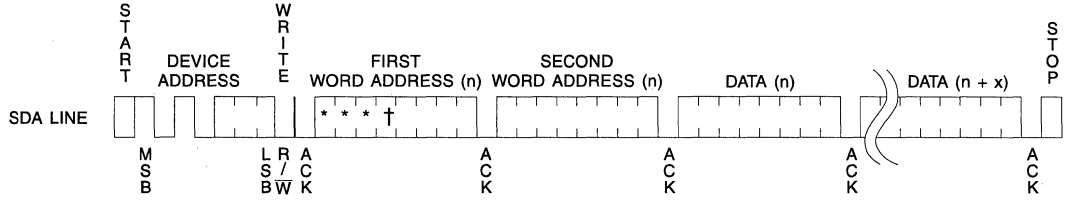


Figure 3. Page Write



(* = DON'T CARE bits)

(† = DON'T CARE bits for the 32K)

Figure 4. Current Address Read

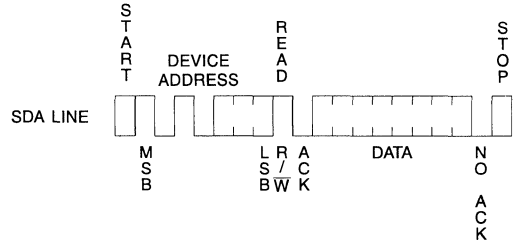
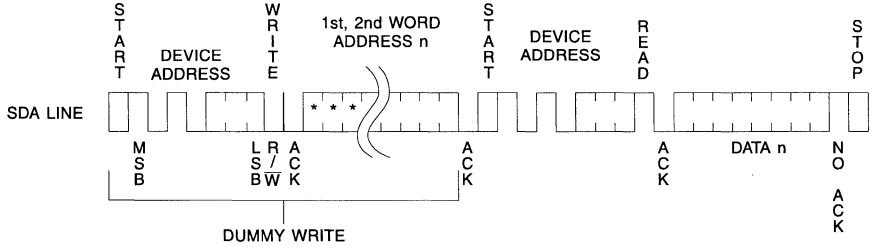
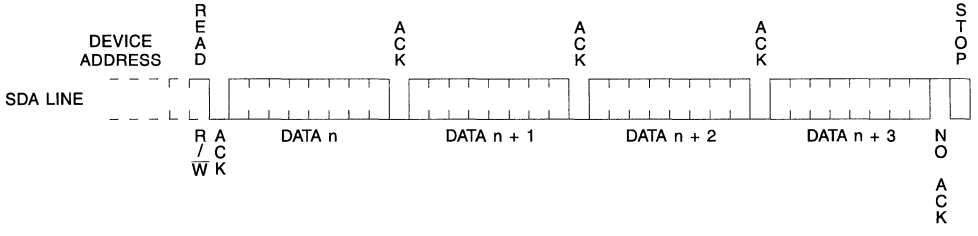


Figure 5. Random Read



(* = DON'T CARE bits)

Figure 6. Sequential Read



Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	35	400	AT24C32-10PC AT24C32N-10SC AT24C32W-10SC AT24C32-10SC	8P3 8S1 8S2 14S	Commercial (0°C to 70°C)
	3000	35	400	AT24C32-10PI AT24C32N-10SI AT24C32W-10SI AT24C32-10SI	8P3 8S1 8S2 14S	Industrial (-40°C to 85°C)
10	1500	0.5	100	AT24C32-10PC-2.7 AT24C32N-10SC-2.7 AT24C32W-10SC-2.7 AT24C32-10SC-2.7	8P3 8S1 8S2 14S	Commercial (0°C to 70°C)
	1500	0.5	100	AT24C32-10PI-2.7 AT24C32N-10SI-2.7 AT24C32W-10SI-2.7 AT24C32-10SI-2.7	8P3 8S1 8S2 14S	Industrial (-40°C to 85°C)
10	1000	0.5	100	AT24C32-10PC-2.5 AT24C32N-10SC-2.5 AT24C32W-10SC-2.5 AT24C32-10SC-2.5	8P3 8S1 8S2 14S	Commercial (0°C to 70°C)
	1000	0.5	100	AT24C32-10PI-2.5 AT24C32N-10SI-2.5 AT24C32W-10SI-2.5 AT24C32-10SI-2.5	8P3 8S1 8S2 14S	Industrial (-40°C to 85°C)
10	800	0.1	100	AT24C32-10PC-1.8 AT24C32N-10SC-1.8 AT24C32W-10SC-1.8 AT24C32-10SC-1.8	8P3 8S1 8S2 14S	Commercial (0°C to 70°C)
	800	0.1	100	AT24C32-10PI-1.8 AT24C32N-10SI-1.8 AT24C32W-10SI-1.8 AT24C32-10SI-1.8	8P3 8S1 8S2 14S	Industrial (-40°C to 85°C)

Ordering Information

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	35	400	AT24C64-10PC AT24C64N-10SC AT24C64W-10SC AT24C64-10SC	8P3 8S1 8S2 14S	Commercial (0°C to 70°C)
	3000	35	400	AT24C64-10PI AT24C64N-10SI AT24C64W-10SI AT24C64-10SI	8P3 8S1 8S2 14S	Industrial (-40°C to 85°C)
10	1500	0.5	100	AT24C64-10PC-2.7 AT24C64N-10SC-2.7 AT24C64W-10SC-2.7 AT24C64-10SC-2.7	8P3 8S1 8S2 14S	Commercial (0°C to 70°C)
	1500	0.5	100	AT24C64-10PI-2.7 AT24C64N-10SI-2.7 AT24C64W-10SI-2.7 AT24C64-10SI-2.7	8P3 8S1 8S2 14S	Industrial (-40°C to 85°C)
10	1000	0.5	100	AT24C64-10PC-2.5 AT24C64N-10SC-2.5 AT24C64W-10SC-2.5 AT24C64-10SC-2.5	8P3 8S1 8S2 14S	Commercial (0°C to 70°C)
	1000	0.5	100	AT24C64-10PI-2.5 AT24C64N-10SI-2.5 AT24C64W-10SI-2.5 AT24C64-10SI-2.5	8P3 8S1 8S2 14S	Industrial (-40°C to 85°C)
10	800	0.1	100	AT24C64-10PC-1.8 AT24C64N-10SC-1.8 AT24C64W-10SC-1.8 AT24C64-10SC-1.8	8P3 8S1 8S2 14S	Commercial (0°C to 70°C)
	800	0.1	100	AT24C64-10PI-1.8 AT24C64N-10SI-1.8 AT24C64W-10SI-1.8 AT24C64-10SI-1.8	8P3 8S1 8S2 14S	Industrial (-40°C to 85°C)

Ordering Information

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

3-Wire Serial CMOS E²PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **2.5 (V_{CC} = 2.5V to 5.5V)**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **User Selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
  - **2K: 256 x 8 or 128 x 16**
  - **4K: 512 x 8 or 256 x 16**
- **3-Wire Serial Interface**
- **2 MHz Clock Rate (5V) Compatibility**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Cycles**
  - **Data Retention: 100 Years**
- **Automotive Grade and Extended Temperature Devices Available**
- **8-Pin PDIP, JEDEC SOIC, and EIAJ SOIC Packages**

Description

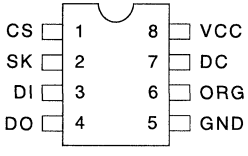
The AT93C46/56/57/66 provides 1024/2048/4096 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46/56/57/66 is available in space saving 8-pin PDIP and 8-pin JEDEC and EIAJ SOIC packages.

(continued)

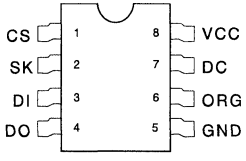
Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
DC	Don't Connect

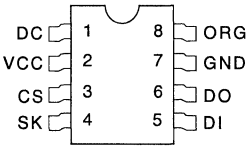
8-Pin PDIP



8-Pin SOIC



8-Pin SOIC



Rotated (R)
(1K JEDEC Only)

0172J

Description (Continued)

The AT93C46/56/57/66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

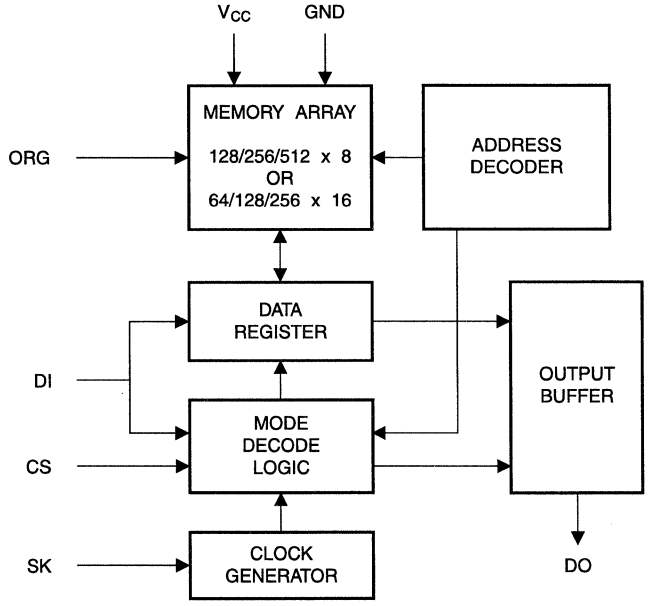
The AT93C46/56/57/66 is available in 4.5V to 5.5V, 2.7V to 5.5V, 2.5V to 5.5V, and 1.8V to 5.5V versions.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note: 1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device (of approximately 1 MΩ) will select the x 16 organization. This feature is not available on 1.8V devices.

Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V		0	0.1	µA
I_{SB2}	Standby Current	V_{CC} = 2.5V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB4}	Standby Current	V_{CC} = 5.0V	CS = 0V		17	30	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1} [1] V_{IH1} [1]	Input Low Voltage Input High Voltage	4.5V ≤ V_{CC} ≤ 5.5V		-0.1 2.0		0.8 V_{CC} + 1	V
V_{IL2} [1] V_{IH2} [1]	Input Low Voltage Input High Voltage	1.8V ≤ V_{CC} ≤ 2.7V		0.0 V_{CC} x 0 .7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA			0.4	V
			I_{OH} = -0.4 mA	2.4			V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA			0.2	V
			I_{OH} = -100 µA	V_{CC} - 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		0 0 0 0		2 1 0.5 0.25	MHz
t_{SKH}	SK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{SKL}	SK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	50 50 100 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{PD1}	Output Delay to '1'	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{PD0}	Output Delay to '0'	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{SV}	CS to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			100 100 200 400	ns
t_{WP}	Write Cycle Time			0.1		10	ms
			$4.5V \le V_{CC} \le 5.5V$		1		ms

Instruction Set for the AT93C46

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_6 - A_0	A_5 - A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes.
ERASE	1	11	A_6 - A_0	A_5 - A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXX	01XXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions.

Instruction Set for the AT93C57

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_7 - A_0	A_6 - A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXX	11XXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_7 - A_0	A_6 - A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_7 - A_0	A_6 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXX	10XXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXXX	01XXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXXXX	00XXXXX			Disables all programming instructions.

Instruction Set for the AT93C56 and AT93C66

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_8 - A_0	A_7 - A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_8 - A_0	A_7 - A_0			Erases memory location A_n - A_0.
WRITE	1	01	A_8 - A_0	A_7 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXXXX	01XXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid when V_{CC} = 5.0V ± 10% and Disable Register cleared.
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Functional Description

The AT93C46/56/57/66 is accessed via a simple and versatile 3-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic '0') precedes the 8 or 16 bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical '1' state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '1' at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A READY/BUSY status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP}.

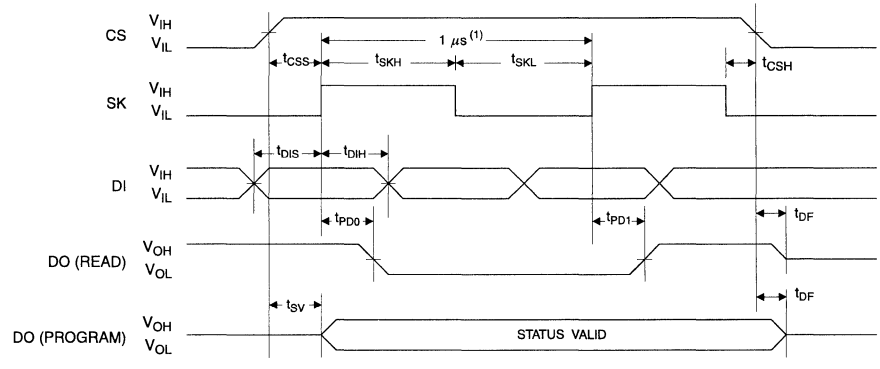
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing



Note: 1. This is the minimum SK period.

(continued)

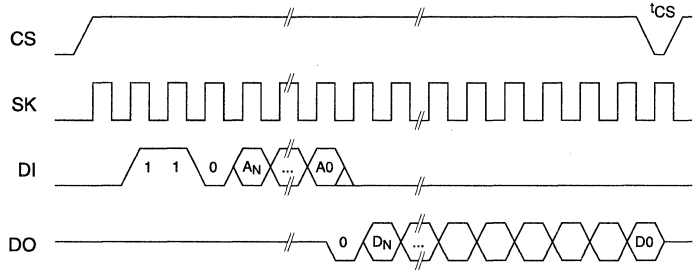
Organization Key for Timing Diagrams

	AT93C46 (1K)		AT93C56 (2K)		AT93C57 (2K)		AT93C66 (4K)	
I/O	x 8	x 16	x 8	x 16	x 8	x 16	x 8	x 16
A_N	A_6	A_5	A_8 (1)	A_7	A_7	A_6	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}	D_7	D_{15}	D_7	D_{15}

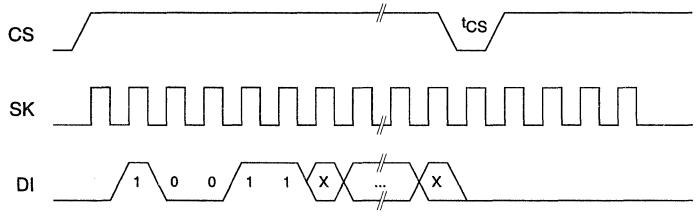
Note: 1. A_8 is a DON'T CARE value, but the extra clock is required.

Timing Diagrams (Continued)

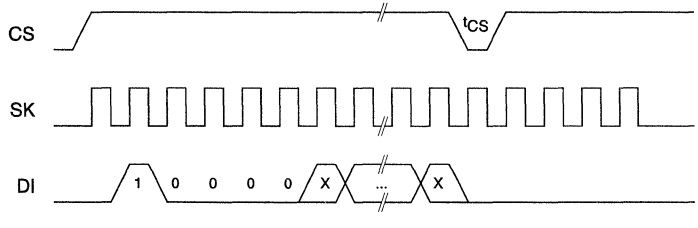
READ Timing



EWEN Timing



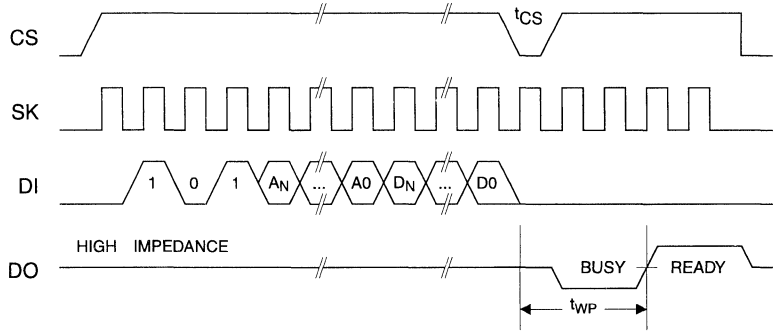
EWDS Timing



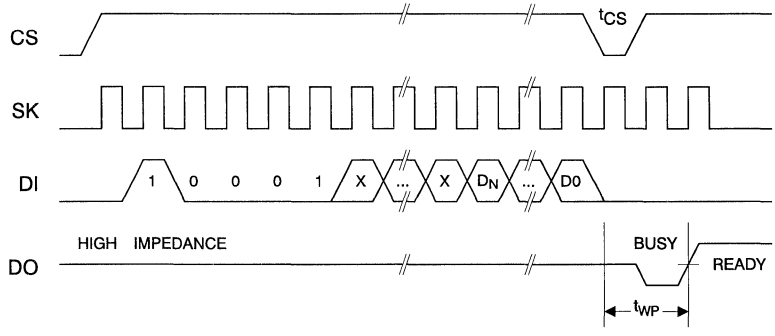
(continued)

Timing Diagrams (Continued)

WRITE Timing

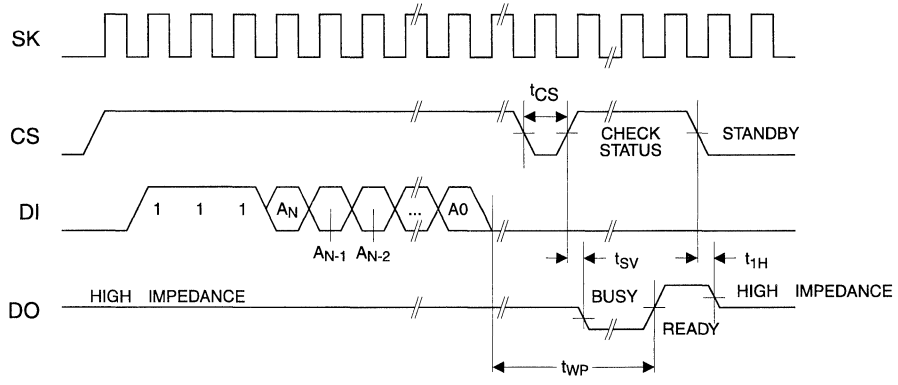


WRAL Timing (1)



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

ERASE Timing



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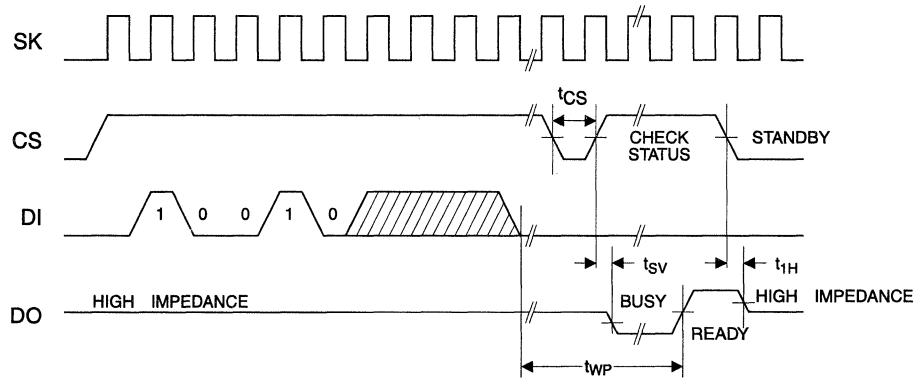
Timing Diagrams (Continued)

TERAL Timing (1)



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C46-10PC AT93C46-10SC AT93C46R-10SC AT93C46W-10SC	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT93C46-10PC-2.7 AT93C46-10SC-2.7 AT93C46R-10SC-2.7 AT93C46W-10SC-2.7	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT93C46-10PC-2.5 AT93C46-10SC-2.5 AT93C46R-10SC-2.5 AT93C46W-10SC-2.5	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT93C46-10PC-1.8 AT93C46-10SC-1.8 AT93C46R-10SC-1.8 AT93C46W-10SC-1.8	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	2000	30.0	2000	AT93C46-10PI AT93C46-10SI AT93C46R-10SI AT93C46W-10SI	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C46-10PI-2.7 AT93C46-10SI-2.7 AT93C46R-10SI-2.7 AT93C46W-10SI-2.7	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C46-10PI-2.5 AT93C46-10SI-2.5 AT93C46R-10SI-2.5 AT93C46W-10SI-2.5	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT93C46-10PI-1.8 AT93C46-10SI-1.8 AT93C46R-10SI-1.8 AT93C46W-10SI-1.8	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)

Ordering Information

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)
R	Rotated Pinout

Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C56-10PC AT93C56-10SC AT93C56W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT93C56-10PC-2.7 AT93C56-10SC-2.7 AT93C56W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT93C56-10PC-2.5 AT93C56-10SC-2.5 AT93C56W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT93C56-10PC-1.8 AT93C56-10SC-1.8 AT93C56W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	2000	30.0	2000	AT93C56-10PI AT93C56-10SI AT93C56W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C56-10PI-2.7 AT93C56-10SI-2.7 AT93C56W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C56-10PI-2.5 AT93C56-10SI-2.5 AT93C56W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT93C56-10PI-1.8 AT93C56-10SI-1.8 AT93C56W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
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8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C57-10PC AT93C57-10SC AT93C57W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT93C57-10PC-2.7 AT93C57-10SC-2.7 AT93C57W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT93C57-10PC-2.5 AT93C57-10SC-2.5 AT93C57W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT93C57-10PC-1.8 AT93C57-10SC-1.8 AT93C57W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	2000	30.0	2000	AT93C57-10PI AT93C57-10SI AT93C57W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C57-10PI-2.7 AT93C57-10SI-2.7 AT93C57W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C57-10PI-2.5 AT93C57-10SI-2.5 AT93C57W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT93C57-10PI-1.8 AT93C57-10SI-1.8 AT93C57W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
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Options	
Blank	Standard Device (4.5V to 5.5V)
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-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C66-10PC AT93C66-10SC AT93C66W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT93C66-10PC-2.7 AT93C66-10SC-2.7 AT93C66W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT93C66-10PC-2.5 AT93C66-10SC-2.5 AT93C66W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT93C66-10PC-1.8 AT93C66-10SC-1.8 AT93C66W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	2000	30.0	2000	AT93C66-10PI AT93C66-10SI AT93C66W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C66-10PI-2.7 AT93C66-10SI-2.7 AT93C66W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C66-10PI-2.5 AT93C66-10SI-2.5 AT93C66W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT93C66-10PI-1.8 AT93C66-10SI-1.8 AT93C66W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
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Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

3-Wire Serial CMOS E²PROMs

1K (64 x 16)

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **2.5 (V_{CC} = 2.5V to 5.5V)**
- **3-Wire Serial Interface**
- **2 MHz Clock Rate (5V) Compatibility**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Cycles**
  - **Data Retention: 100 Years**
- **Automotive Grade and Extended Temperature Devices Available**
- **8-Pin PDIP and JEDEC SOIC Packages**

Description

The AT93C46A provides 1024 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 64 words of 16 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46A is available in space saving 8-pin PDIP and 8-pin JEDEC packages.

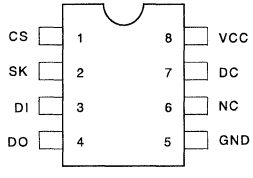
The AT93C46A is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

The AT93C46A is available in 4.5V to 5.5V, 2.7V to 5.5V, and 2.5V to 5.5V versions.

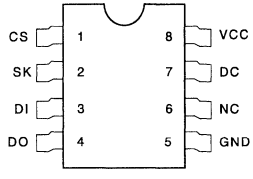
Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
NC	No Connect
DC	Don't Connect

8-Pin PDIP



8-Pin SOIC



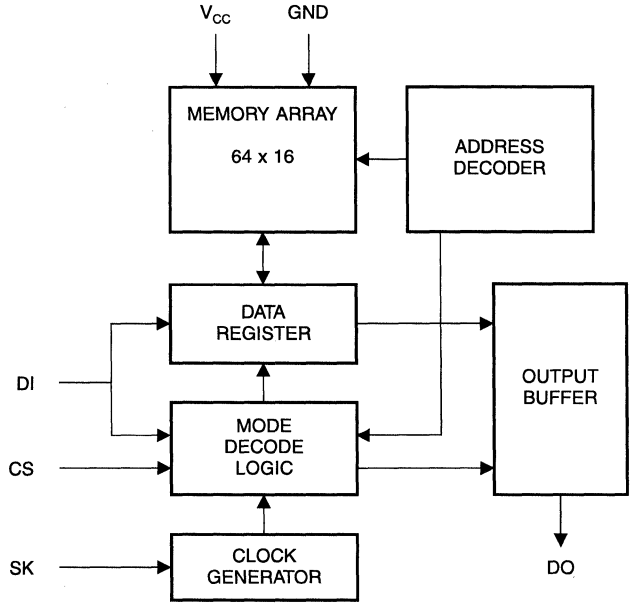
0539A

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.5V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 2.5V	CS = 0V		14.0	20.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		14.0	20.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		35.0	50.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1} [1] V_{IH1} [1]	Input Low Voltage Input High Voltage	4.5V ≤ V_{CC} ≤ 5.5V		-0.1 2.0		0.8 V_{CC} + 1	V
V_{IL2} [1] V_{IH2} [1]	Input Low Voltage Input High Voltage	1.8V ≤ V_{CC} ≤ 2.7V		0.0 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA			0.4	V
			I_{OH} = -0.4 mA	2.4			V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA			0.2	V
			I_{OH} = -100 µA	V_{CC} - 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = +2.5V to + 5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency		4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	0 0 0 0		2 1 0.5 0.25	MHz
t_{SKH}	SK High Time		4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	250 250 500 1000			ns
t_{SKL}	SK Low Time		4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	250 250 500 1000			ns
t_{CS}	Minimum CS Low Time		4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	250 250 500 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	50 50 100 200			ns
t_{DIS}	DI Setup Time	Relative to SK	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	100 100 200 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	100 100 200 400			ns
t_{PD1}	Output Delay to '1'	AC Test	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V			250 250 500 1000	ns
t_{PD0}	Output Delay to '0'	AC Test	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V			250 250 500 1000	ns
t_{SV}	CS to Status Valid	AC Test	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V			250 250 500 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V			100 100 200 400	ns
t_{WP}	Write Cycle Time			0.1		10	ms
			4.5V ≤ V_{CC} ≤ 5.5V		1		ms

Instruction Set for the AT93C46A

Instruction	SB	Op Code	Address x 16	Comments
READ	1	10	A_5 - A_0	Reads data stored in memory, at specified address.
EWEN	1	00	11XXXX	Write enable must precede all programming modes.
ERASE	1	11	A_5 - A_0	Erase memory location A_n - A_0.
WRITE	1	01	A_5 - A_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXX	Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXX	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXX	Disables all programming instructions.

Functional Description

The AT93C46A is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic '0') precedes the 16 bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical '1' state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY / BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '1' at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

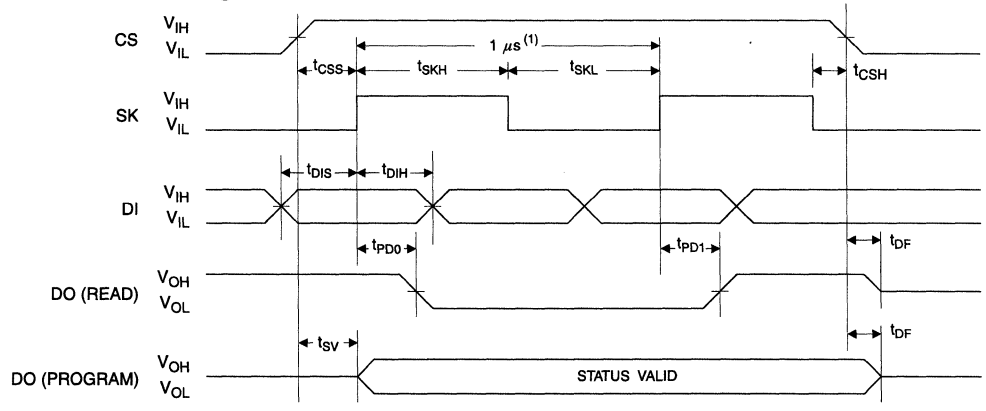
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing



Note: 1. This is the minimum SK period.

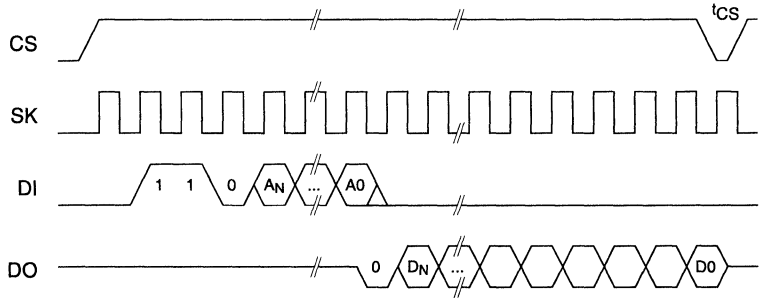
(continued)

Organization Key for Timing Diagrams

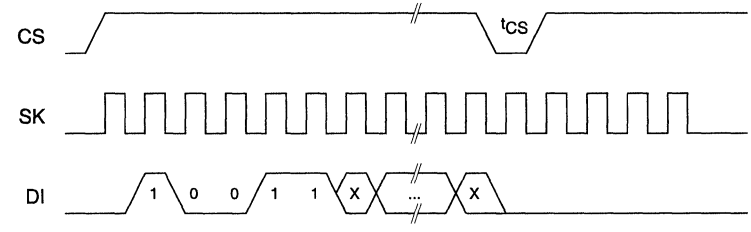
I/O	AT93C46A x 16
A_N	A_5
D_N	D_{15}

Timing Diagrams (Continued)

READ Timing

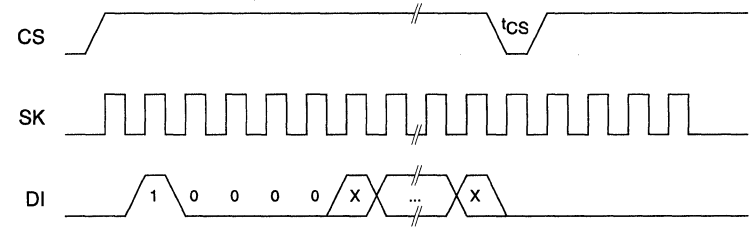


EWEN Timing (1)



Note: 1. Requires a minimum of nine clock cycles.

EWDS Timing (1)

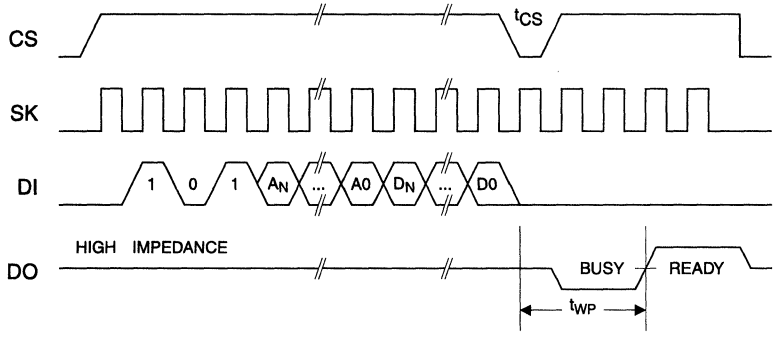


Note: 1. Requires a minimum of nine clock cycles.

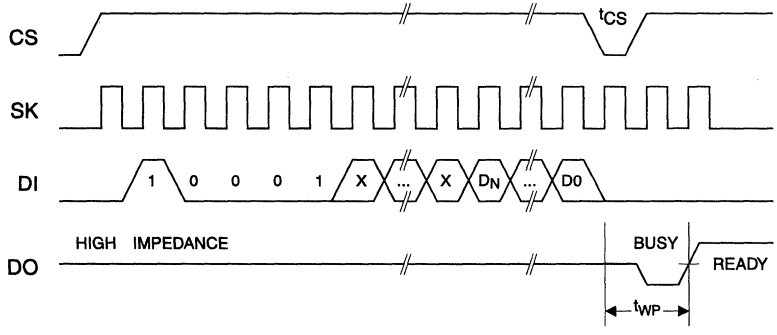
(continued)

Timing Diagrams (Continued)

WRITE Timing

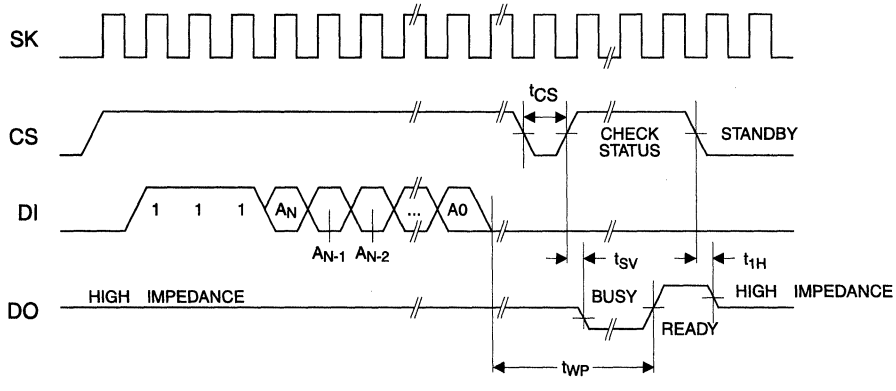


WRAL Timing (1, 2)



Notes: 1. Valid only at V_{CC} = 4.5V to 5.5V.
2. Requires a minimum of nine clock cycles.

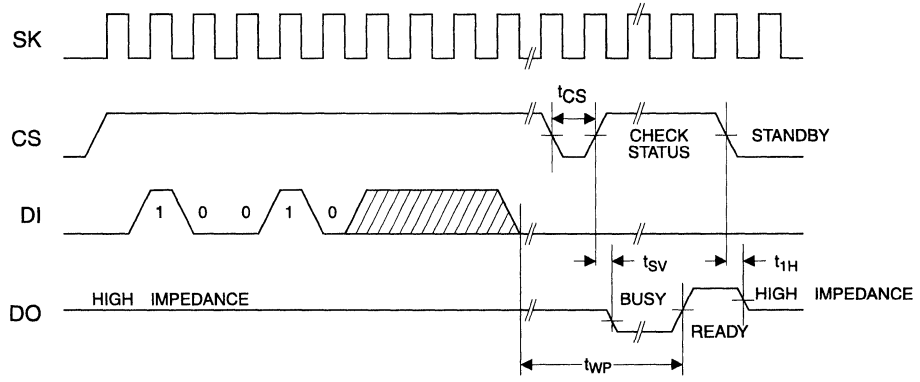
ERASE Timing



(continued)

Timing Diagrams (Continued)

TERAL Timing [1]



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	50.0	2000	AT93C46A-10PC AT93C46A-10SC	8P3 8S1	Commercial (0°C to 70°C)
10	800	20.0	1000	AT93C46A-10PC-2.7 AT93C46A-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
10	600	20.0	500	AT93C46A-10PC-2.5 AT93C46A-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
10	2000	50.0	2000	AT93C46A-10PI AT93C46A-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	800	20.0	1000	AT93C46A-10PI-2.7 AT93C46A-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	600	20.0	500	AT93C46A-10PI-2.5 AT93C46A-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

4-Wire Serial CMOS E²PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **2.5 (V_{CC} = 2.5V to 5.5V)**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **User Selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
  - **2K: 256 x 8 or 128 x 16**
  - **4K: 512 x 8 or 256 x 16**
- **4-Wire Serial Interface**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Cycles**
  - **Data Retention: 100 Years**
- **8-Pin PDIP and EIAJ SOIC Packages**

Description

The AT59C11/22/13 provides 1024/2048/4096 bits of serial EEPROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT59C11/22/13 is available in space saving 8-pin PDIP and 8-pin EIAJ SOIC packages.

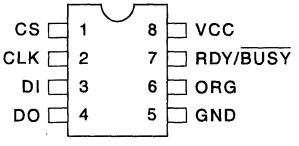
The AT59C11/22/13 is enabled through the Chip Select pin (CS), and accessed via a 4-wire serial interface consisting of Data Input (DI), Data Output (DO), and Clock (CLK). Upon receiving a READ instruction at DI, the address is decoded and the data

(continued)

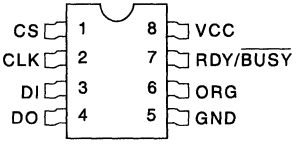
Pin Configurations

Pin Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
RDY/$\overline{BUSY}$	Status Output

8-Pin PDIP



8-Pin SOIC



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Description (Continued)

is clocked out serially on the data output pin DO, the WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. Ready/Busy status can be monitored upon completion of a programming operation by polling the Ready/Busy pin.

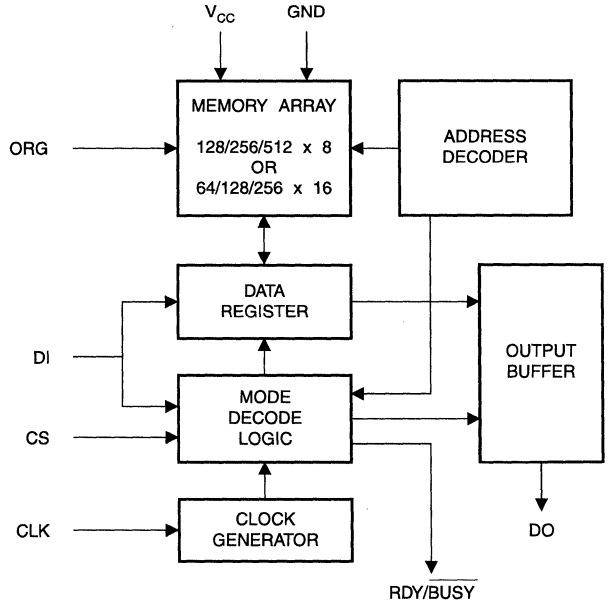
The AT59C11/22/13 is available in 5.0V ± 10%, 2.7V to 5.5V, 2.5V to 5.5V, and 1.8V to 5.5V versions.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note: 1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization. This feature is not available on 1.8V devices.

Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, CLK, DI, RDY/$\overline{BUSY}$)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V		0.0	0.1	µA
I_{SB2}	Standby Current	V_{CC} = 2.5V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB4}	Standby Current	V_{CC} = 5.0V	CS = 0V		21.0	30.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1} [1] V_{IH1} [1]	Input Low Voltage Input High Voltage	4.5V ≤ V_{CC} ≤ 5.5V		-0.1 2.0		0.8 V_{CC} + 1	V
V_{IL2} [1] V_{IH2} [1]	Input Low Voltage Input High Voltage	1.8V ≤ V_{CC} ≤ 2.7V		0.0 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA I_{OH} = 0.4 mA	 2.4		0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA I_{OH} = -0.1 mA	 V_{CC} - 0.2		0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{CLK}	CLK Clock Frequency		4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	0 0 0 0		1 1 0.5 0.25	MHz
t_{CKH}	CLK High Time		4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	250 250 500 1000			ns
t_{CKL}	CLK Low Time		4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	250 250 500 1000			ns
t_{CS}	Minimum CS Low Time		4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	250 250 500 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	50 50 100 200			ns
t_{DIS}	DI Setup Time	Relative to SK	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	100 100 200 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V	100 100 200 400			ns
t_{PD1}	Output Delay to '1'	AC Test	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V			250 250 500 1000	ns
t_{PD0}	Output Delay to '0'	AC Test	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V			250 250 500 1000	ns
t_{RBD}	CS to Status Valid	AC Test	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V			250 250 500 1000	ns
t_{CZ}	CS to DO in High Impedance	AC Test CS = V_{IL}	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} ≤ 5.5V			100 100 200 400	ns
t_{WC}	Write Cycle Time			0.1		10	ms

Instruction Set for the AT59C11

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10XX	A_6 - A_0	A_5 - A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXX	XXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXX	XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	0001	XXXXXXX	XXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	0000	XXXXXXX	XXXXXX			Disables all programming instructions.

Instruction Set for the AT59C22

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10XX	A_7 - A_0	A_6 - A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXXX	XXXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_7 - A_0	A_6 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXXX	XXXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	0001	XXXXXXXX	XXXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid when V_{CC} = 5.0V ± 10% and Disable Register cleared.
EWDS	1	0000	XXXXXXXX	XXXXXXX			Disables all programming instructions.

Instruction Set for the AT59C13

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10XX	A_8 - A_0	A_7 - A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXXXX	XXXXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_8 - A_0	A_7 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXXXX	XXXXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	0001	XXXXXXXXX	XXXXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid when V_{CC} = 5.0V ± 10% and Disable Register cleared.
EWDS	1	0000	XXXXXXXXX	XXXXXXXX			Disables all programming instructions.

Functional Description

The AT59C11/22/13 are accessed via a simple and versatile 4-wire serial communication interface. Device operation is controlled by six instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock CLK. It should be noted that a dummy bit (logic '0') precedes the 8 or 16 bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The Ready/Busy status of the AT59C11/22/13 can be determined by polling the RDY/BUSY pin. A logic '0' at RDY/BUSY indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

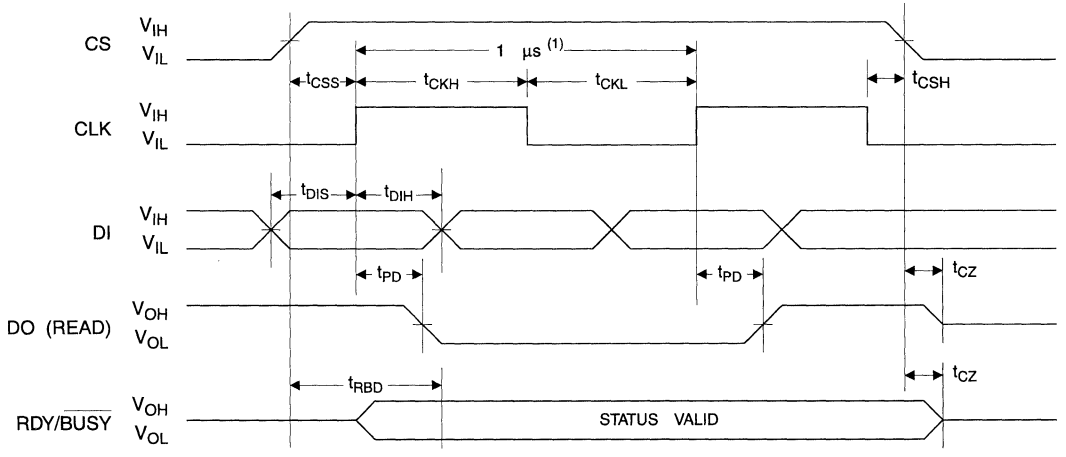
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The Ready/Busy status of the AT59C11/22/13 can be determined by polling the RDY/BUSY pin. The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The Ready/Busy status of the AT59C11/22/13 can be determined by polling the RDY/BUSY pin. The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing



Note: 1. This is the minimum CLK period.

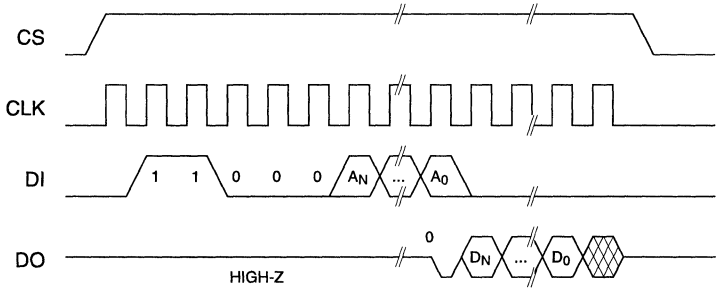
(continued)

Organization Key for Timing Diagrams

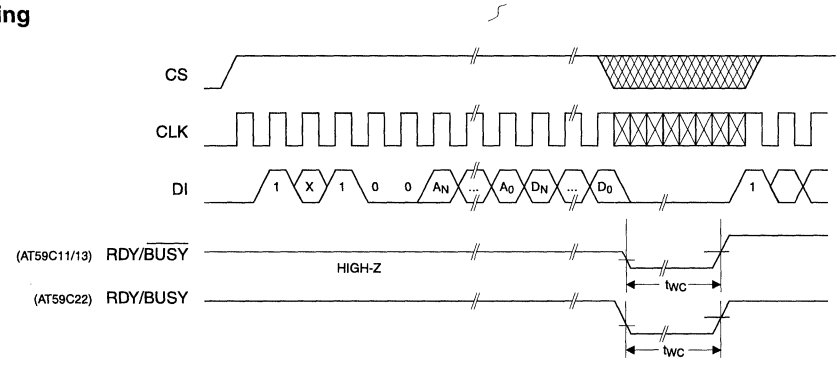
I/O	Density 1K		Density 2K		Density 4K	
	x 8	x 16	x 8	x 16	x 8	x 16
A_N	A_6	A_5	A_7	A6	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}	D_7	D_{15}

Timing Diagrams (Continued)

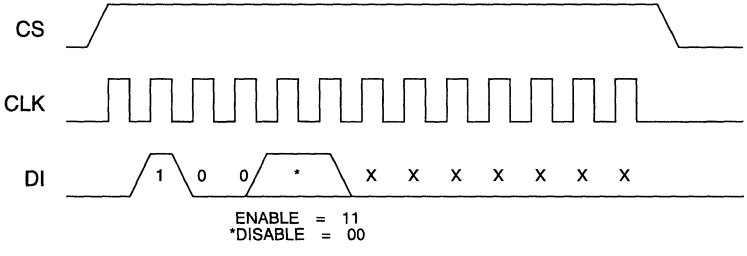
READ Timing



WRITE Timing



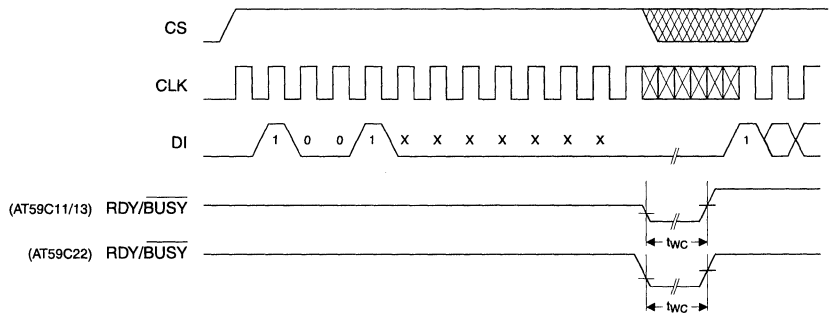
EWEN/EWDS Timing



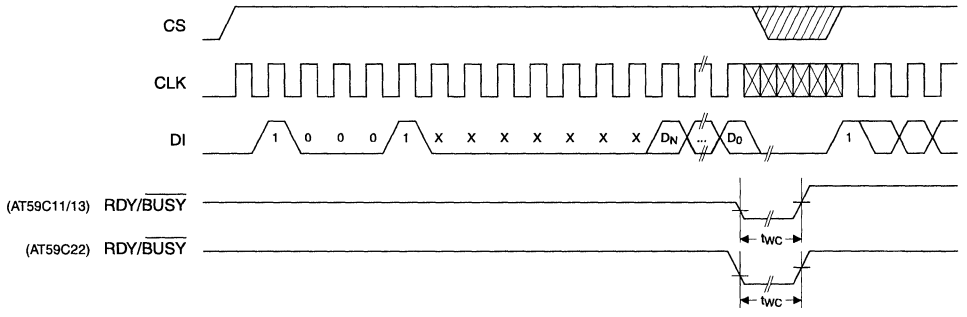
(continued)

Timing Diagrams (Continued)

ERAL Timing



WRAL Timing



Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	1000	AT59C11-10PC AT59C11W-10SC	8P3 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT59C11-10PC-2.7 AT59C11W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT59C11-10PC-2.5 AT59C11W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT59C11-10PC-1.8 AT59C11W-10SC-1.8	8P3 8S2	Commercial (0°C to 70°C)
10	2000	30.0	1000	AT59C11-10PI AT59C11W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT59C11-10PI-2.7 AT59C11W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT59C11-10PI-2.5 AT59C11W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT59C11-10PI-1.8 AT59C11W-10SI-1.8	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	1000	AT59C22-10PC AT59C22W-10SC	8P3 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT59C22-10PC-2.7 AT59C22W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT59C22-10PC-2.5 AT59C22W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT59C22-10PC-1.8 AT59C22W-10SC-1.8	8P3 8S2	Commercial (0°C to 70°C)
10	2000	30.0	1000	AT59C22-10PI AT59C22W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT59C22-10PI-2.7 AT59C22W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT59C22-10PI-2.5 AT59C22W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT59C22-10PI-1.8 AT59C22W-10SI-1.8	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	1000	AT59C13-10PC AT59C13W-10SC	8P3 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT59C13-10PC-2.7 AT59C13W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT59C13-10PC-2.5 AT59C13W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT59C13-10PC-1.8 AT59C13W-10SC-1.8	8P3 8S2	Commercial (0°C to 70°C)
10	2000	30.0	1000	AT59C13-10PI AT59C13W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT59C13-10PI-2.7 AT59C13W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT59C13-10PI-2.5 AT59C13W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT59C13-10PI-1.8 AT59C13W-10SI-1.8	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
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Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
-1.8	Low Voltage (1.8V to 5.5V)

SPI Serial CMOS E²PROMs

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

Preliminary

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 and 3
- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- 2 MHz Clock Rate (5V) Compatibility
- 8-Byte Page Mode
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-Timed Write Cycle (10 ms Max)
- High Reliability
  - Endurance: 1 Million Cycles
  - Data Retention: 100 Years
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP and JEDEC SOIC Packages

Description

The AT25010/020/040 provides 1024/2048/4096 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 128/256/512 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT25010/020/040 is available in space saving 8-pin PDIP and 8-pin JEDEC (SOIC) packages.

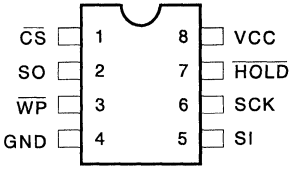
The AT25010/020/040 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 4-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate ERASE cycle is required before WRITE.

(continued)

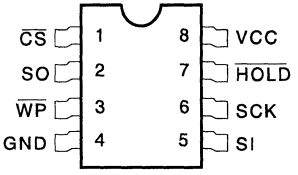
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

8-Pin PDIP



8-Pin SOIC



0606B

Description (Continued)

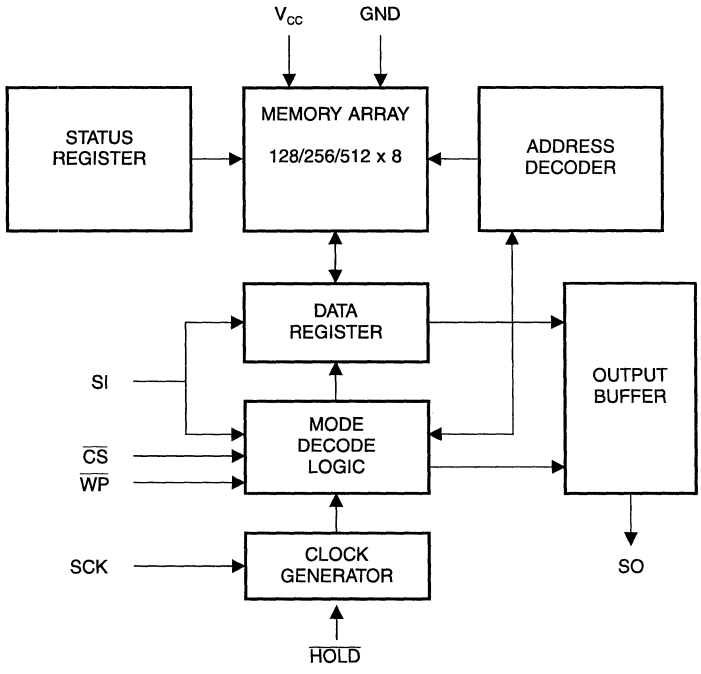
BLOCK WRITE protection is enabled by programming the status register with one of four blocks of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Max	Units
V_{CC1} [1]	Supply Voltage			1.8	5.5	V
V_{CC2}	Supply Voltage			2.7	5.5	V
V_{CC3}	Supply Voltage			4.5	5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 1 MHz, SO = Open			3.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 2 MHz, SO = Open			6.0	mA
I_{SB1} [1]	Standby Current	V_{CC} = 1.8V	$\overline{CS}$ = V_{CC}		100	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	$\overline{CS}$ = V_{CC}		100	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	$\overline{CS}$ = V_{CC}		100	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		-1.0	3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		-1.0	3.0	µA
V_{IL} [2]	Input Low Voltage			-1.0	V_{CC} x 0.3	V
V_{IH} [2]	Input High Voltage			V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.0 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -1.0 mA	V_{CC} - 0.8		V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2		V

Notes: 1. This parameter is preliminary and Atmel may change the specifications upon further characterization.
2. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	2 1 (1)	MHz
t_{RI}	Input Rise Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		2 2 2	µs
t_{FI}	Input Fall Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		2 2 2	µs
t_{WH}	SCK High Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 400 (1)		ns
t_{WL}	SCK Low Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	200 400 (1)		ns
t_{CS}	$\overline{CS}$ High Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 500 (1)		ns
t_{CSS}	$\overline{CS}$ Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 500 (1)		ns
t_{CSH}	$\overline{CS}$ Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	250 500 (1)		ns
t_{SU}	Data In Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	50 100 100		ns
t_H	Data In Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	50 100 100		ns
t_{HD}	$\overline{Hold}$ Setup Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	100 200 (1)		ns
t_{CD}	$\overline{Hold}$ Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	100 200 (1)		ns
t_V	Output Valid	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	200 400 (1)	ns
t_{HO}	Output Hold Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0		ns
t_{LZ}	$\overline{Hold}$ to Output Low Z	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6	0 0 0	100 100 100	ns

Note: 1. To be characterized.

(continued)

AC Characteristics (Continued)

Symbol	Parameter	Voltage	Min	Max	Units
t_{HZ}	$\overline{\text{Hold}}$ to Output High Z	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		100 100 100	ns
t_{DIS}	Output Disable Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		250 500 (1)	ns
t_{WC}	Write Cycle Time	4.5 - 5.5 2.7 - 5.5 1.8 - 3.6		10	ms

Note: 1. To be characterized.

Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the Serial Clock pin (SCK) is always an input, the AT25010/020/040 always operates as a slave.

TRANSMITTER/RECEIVER: The AT25010/020/040 has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed. The op-code also contains address bit A8 in both the READ and WRITE instructions.

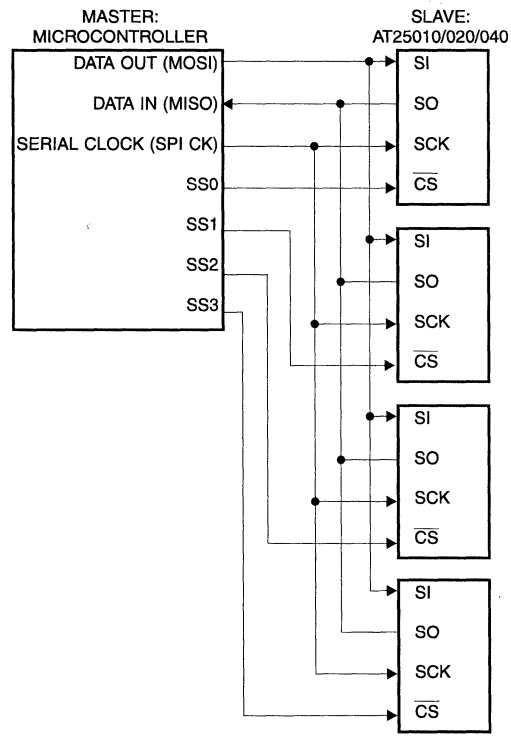
INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25010/020/040, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25010/020/040 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25010/020/040. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin ($\overline{WP}$) will allow normal read/write operations when held high. When the $\overline{WP}$ pin is brought low, all write operations are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the AT25010/020/040. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation.

SPI Serial Interface



Functional Description

The AT25010/020/040 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

The AT25010/020/040 utilizes an 8 bit instruction register. The list of instructions and their operation codes are contained in Table 1. All instructions, addresses, and data are transferred with the MSB first.

Table 1. Instruction Set for the AT25010/020/040

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 A011	Read Data from Memory Array
WRITE	0000 A010	Write Data to Memory Array
Note: "A" represents MSB address bit A8.		

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction. The $\overline{WP}$ pin must be held high during a WREN instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 2a. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Table 2b. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = 0 ($\overline{RDY}$) indicates the device is READY. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1= 0 indicates the device *is not* WRITE ENABLED. Bit 1 = 1 indicates the device is WRITE ENABLED.
Bit 2 (BP0)	See Table 3.
Bit 3 (BP1)	See Table 3.
Bits 4-7 are 0s when device is not in an internal write cycle.	
Bits 0-7 are 1s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25010/020/040 is divided into four array segments. One quarter (1/4), one half (1/2), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be READ only. The block write protection levels and corresponding status register control bits are shown in Table 3.

The two bits, BP1 and BP0 are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g. WREN, t_{WC}, RDSR).

Table 3. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected		
	BP1	BP0	AT25010	AT25020	AT25040
0	0	0	None	None	None
1 (1/4)	0	1	60-7F	C0-FF	180-1FF
2 (1/2)	1	0	40-7F	80-FF	100-1FF
3 (All)	1	1	00-7F	00-FF	000-1FF

READ SEQUENCE (READ): Reading the AT25010/020/040 via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the READ op-code (including A8) is transmitted via the SI line followed by the byte address to be read (A7-A0). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The READ sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ cycle.

(continued)

Functional Description (Continued)

WRITE SEQUENCE (WRITE): In order to program the AT25010/020/040, the Write Protect pin ($\overline{WP}$) must be held high and two separate instructions must be executed. First, the device **must be write enabled** via the Write Enable (WREN) Instruction. Then a Write (WRITE) Instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write Instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code (including A8) is transmitted via the SI line followed by the byte address (A7-A0) and the data (D7-D0) to be programmed. Programming will start after the $\overline{CS}$ pin is brought high. (The LOW to High transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

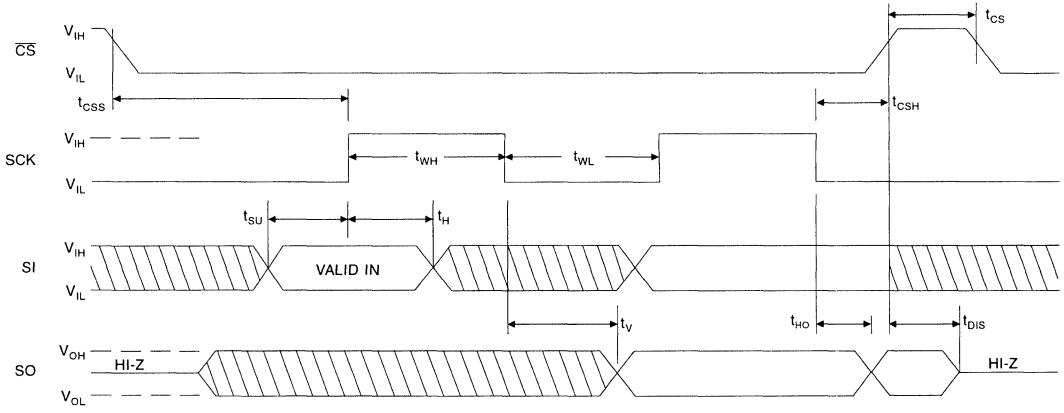
The READY/BUSY status of the device can be determined by initiating a READ STATUS REGISTER (RDSR) Instruction. If Bit 0 = 1, the WRITE cycle is still in progress. If Bit 0 = 0, the WRITE cycle has ended. Only the READ STATUS REGISTER instruction is enabled during the WRITE programming cycle.

The AT25010/020/040 is capable of an 8-byte PAGE WRITE operation. After each byte of data is received, the three low order address bits are internally incremented by one; the six high order bits of the address will remain constant. If more than 8-bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25010/020/040 is automatically returned to the write disable state at the completion of a WRITE cycle.

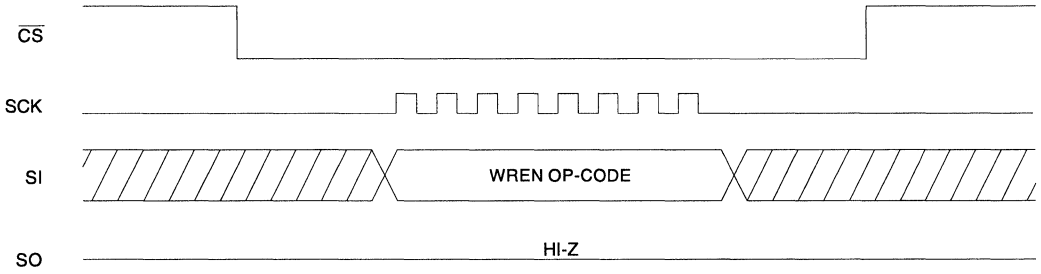
NOTE: If the $\overline{WP}$ pin is brought low or if the device is not Write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new CS falling edge is required to re-initiate the serial communication.

Timing Diagrams

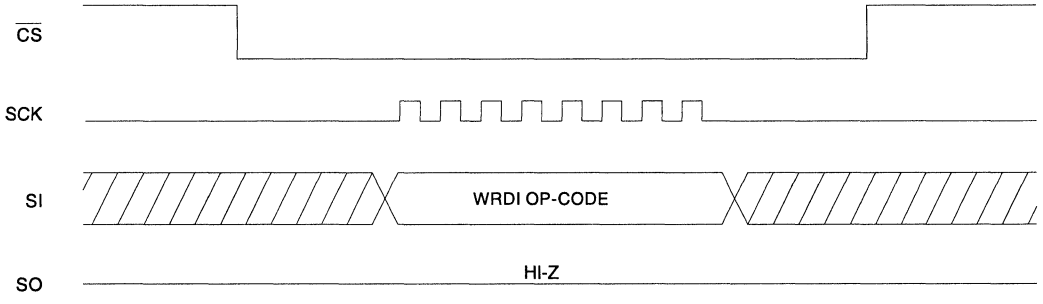
Synchronous Data Timing



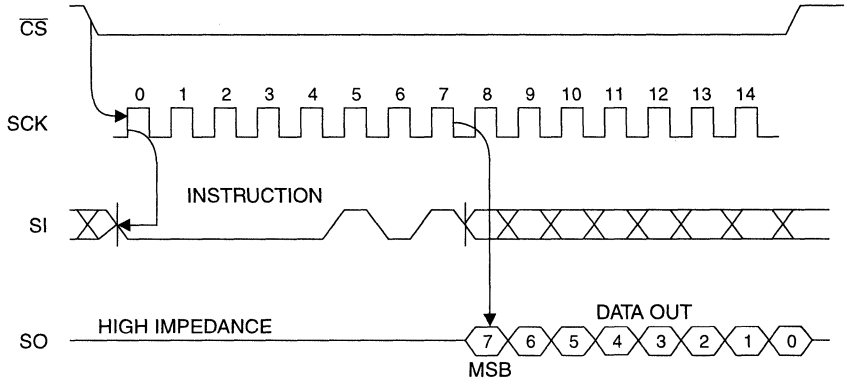
WREN Timing



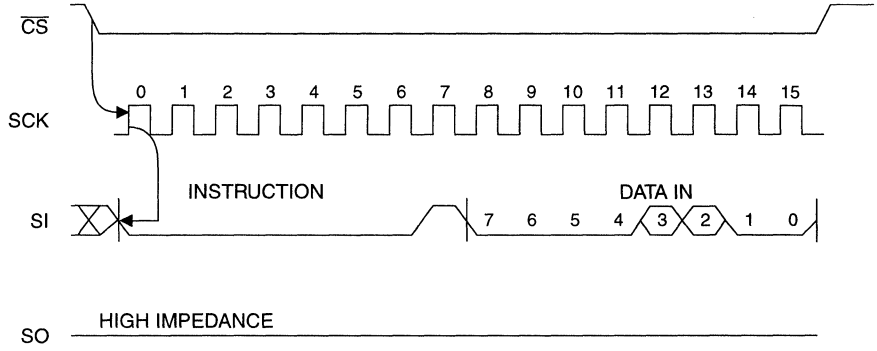
WRDI Timing



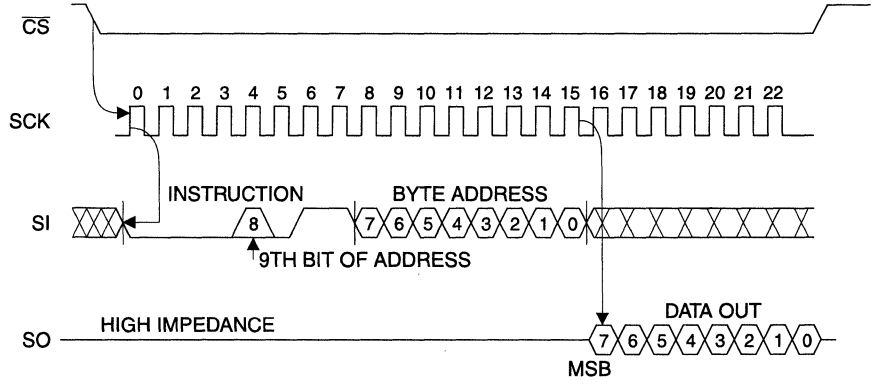
RDSR Timing



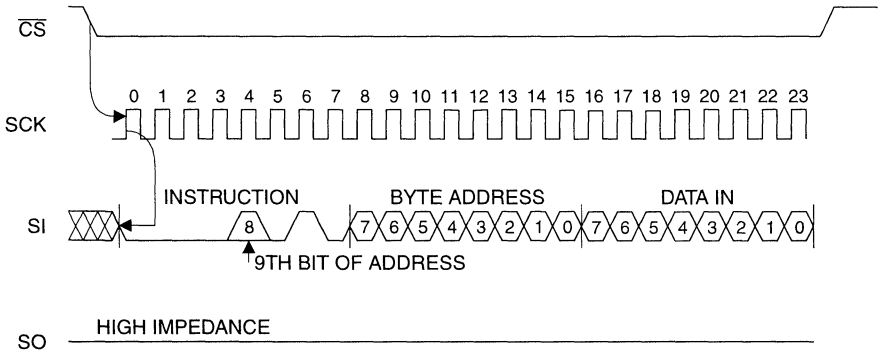
WRSR Timing



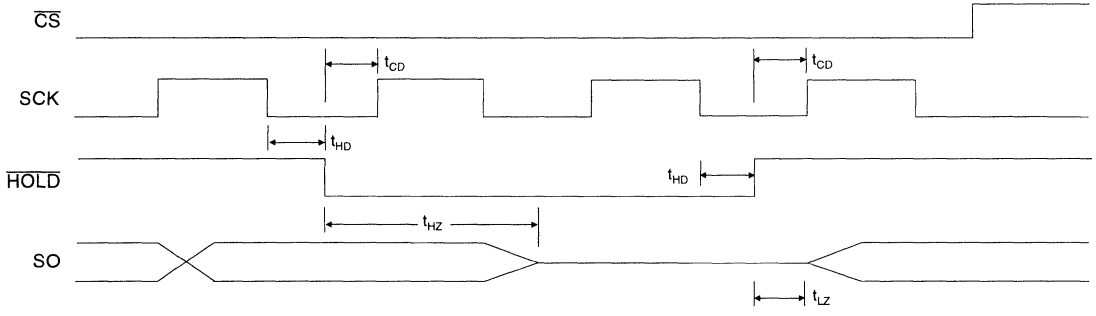
READ Timing



WRITE Timing



$\overline{\text{HOLD}}$ Timing



Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	6000	100	2000	AT25010-10PC AT25010-10SC	8P3 8S1	Commercial (0°C to 70°C)
10	3000	100	1000	AT25010-10PC-2.7 AT25010-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
10	3000	100	(1)	AT25010-10PC-1.8 AT25010-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
10	6000	100	2000	AT25010-10PI AT25010-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	1000	AT25010-10PI-2.7 AT25010-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	(1)	AT25010-10PI-1.8 AT25010-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Note: 1. To be characterized.

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	6000	100	2000	AT25020-10PC AT25020N-10SC	8P3 8S1	Commercial (0°C to 70°C)
10	3000	100	1000	AT25020-10PC-2.7 AT25020N-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
10	3000	100	(1)	AT25020-10PC-1.8 AT25020N-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
10	6000	100	2000	AT25020-10PI AT25020N-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	1000	AT25020-10PI-2.7 AT25020N-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	(1)	AT25020-10PI-1.8 AT25020N-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Note: 1. To be characterized.

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	6000	100	2000	AT25040-10PC AT25040N-10SC	8P3 8S1	Commercial (0°C to 70°C)
10	3000	100	1000	AT25040-10PC-2.7 AT25040N-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
10	3000	100	(1)	AT25040-10PC-1.8 AT25040N-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
10	6000	100	2000	AT25040-10PI AT25040N-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	1000	AT25040-10PI-2.7 AT25040N-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	3000	100	(1)	AT25040-10PI-1.8 AT25040N-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Note: 1. To be characterized.

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-1.8	Low Voltage (1.8V to 3.6V)

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 and 3
- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- 2 MHz Clock Rate
- 32-Byte Page Mode
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-Timed Write Cycle (10 ms Max)
- High Reliability
  - Endurance: 1 Million Cycles
  - Data Retention: 100 Years
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP and JEDEC SOIC Packages

Description

The AT25320/640 provides 32768/65536 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT25320/640 is available in space saving 8-pin PDIP and 8-pin JEDEC (SOIC) packages.

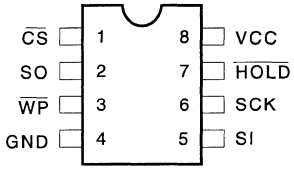
The AT25320/640 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 4-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate ERASE cycle is required before WRITE.

(continued)

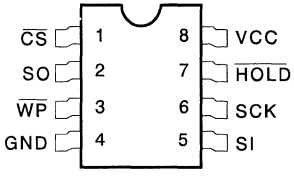
Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

8-Pin PDIP



8-Pin SOIC



SPI Serial CMOS E^2PROMs

32K (4096 x 8)

64K (8192 x 8)

Advance Information

0639A

Description (Continued)

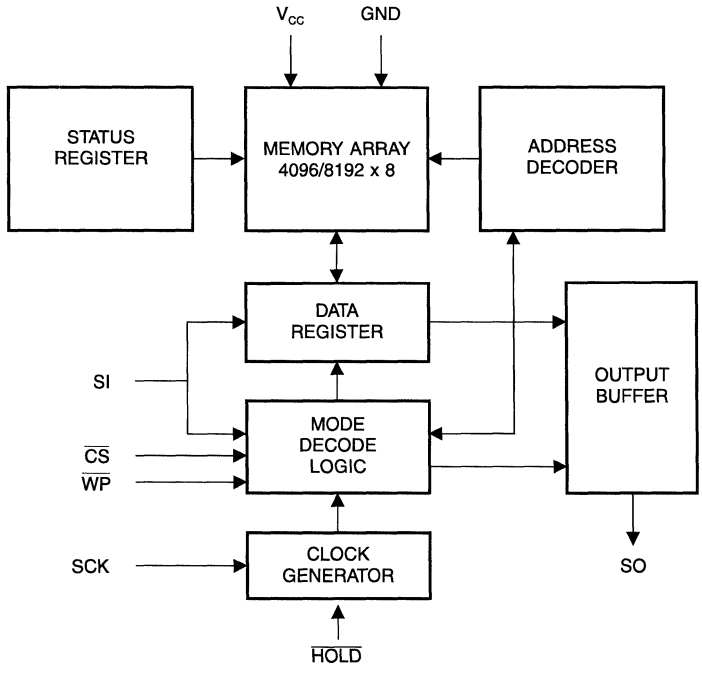
BLOCK WRITE protection is enabled by programming the status register with one of four blocks of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



FPGA Configuration E²PROM

65K, 128K, and 256K

Features

- E² Programmable 65,536 x 1, 131,072 x 1, and 262,144 x 1 bit Serial Memories Designed To Store Configuration Programs For Programmable Gate Arrays
- Simple Interface to SRAM FPGAs Requires Only One User I/O Pin
- Compatible With AT6000 FPGAs, ATT3000 FPGA, EPF8000 FPGAs, ORCA FPGAs, XC2000, XC3000, XC4000, XC5000 FPGAs
- Cascadable To Support Additional Configurations or Future Higher-density Arrays (17C128 and 17C256 only)
- Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- Available In the Space-efficient Plastic DIP or Surface-mount PLCC and SOIC Packages
- In-system Programmable Via 2-Wire Bus
- Emulation of 24CXX Serial E²PROMs

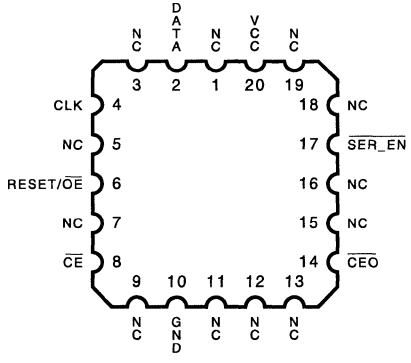
Description

The AT17C65/128/256 (AT17CXXX family) FPGA Configuration E²PROMS (Configurator) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. Both the AT17C65 and the AT17C128 are packaged in the 8-pin DIP and the popular 20-pin Plastic Leaded Chip Carrier, and SOIC. The AT17C256 is available in 14-pin SOIC or 20-pin PLCC or SOIC packages. The AT17CXXX family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17CXXX organization supplies enough memory to configure one or multiple smaller FPGAs. Using a special feature of the AT17CXXX, the user can select the polarity of the reset function by programming a special E²PROM bit.

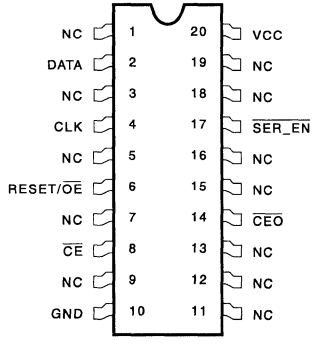
The AT17C65/128/256 can be programmed with the standard programmers from other manufacturers.

Pin Configurations

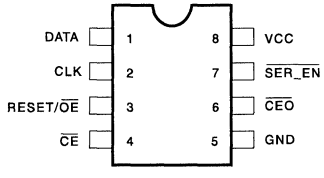
20-Pin PLCC



20-Pin SOIC



8-Pin DIP



- Please refer to Section 5, FPGA Configuration Memories, page 5-3 for complete AT17C65/128/256 data sheet.

0391D

Controlling The AT17C65/128/256 Serial E²PROMs

Most connections between the FPGA device and the Serial E²PROM are simple and self-explanatory:

- The DATA output of the AT17C65/128/256 drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17C65/128/256.
- The $\overline{CEO}$ output of any AT17C128/256 drives the $\overline{CE}$ input of the next AT17C128/256 in a cascade chain of PROMs.
- $\overline{SER\_EN}$ must be connected to V_{CC}.

There are, however, two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$, as shown in the AC Characteristics Waveform.

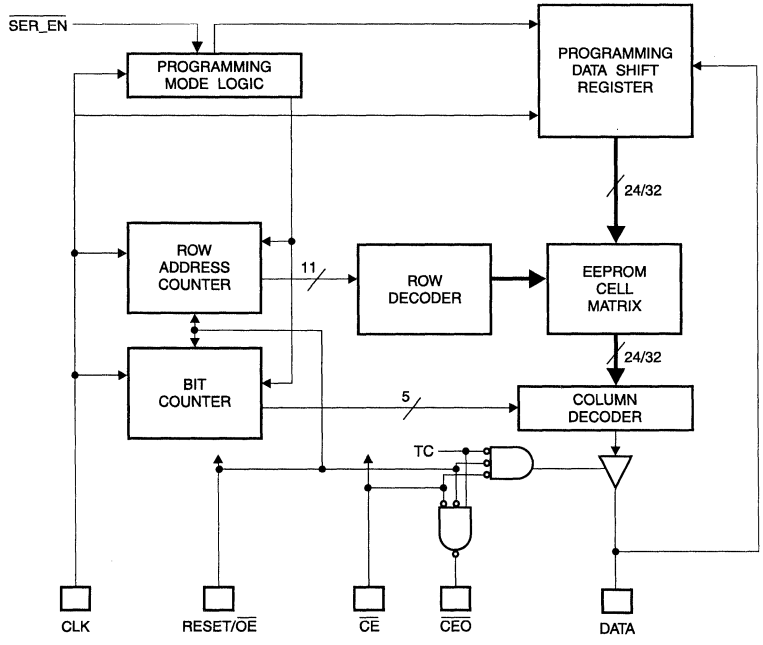
Condition 1

The simplest connection is to have the FPGA D/$\overline{P}$ output drive both $\overline{CE}$ and RESET/$\overline{OE}$ in parallel. Due to its simplicity, however, this method will fail if the FPGA receives an external reset condition during the configuration cycle. If a system reset is applied to the FPGA, it will abort the original configuration and then reset itself for a new configuration, as intended. Of course, the AT17C65/128/256 does not see the external reset signal and will not reset its internal address counters and, consequently, will remain out of sync with the FPGA for the remainder of the configuration cycle.

Condition 2

The FPGA D/$\overline{P}$ output drives only the CE input of the AT17C65/128/256, while its $\overline{OE}$ input is driven by the inversion of the FPGA $\overline{RESET}$ input. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. A high level on the RESET/$\overline{OE}$ input to the AT17CXXX during FPGA reset clears the PROM internal address pointer, so that the reconfiguration starts at the beginning. The AT17C65/128/256 does not require an inverter since the RESET polarity is programmable.

Block Diagram



16K (2K x 8) *Battery-Voltage*™ CMOS E^2PROM

Features

- 2.7 to 3.6V Supply
  - Full Read and Write Operation
- Low Power Dissipation
  - 8 mA Active Current
  - 50 µA CMOS Standby Current
- Read Access Time - 250 ns
- Byte Write - 3 ms
- Direct Microprocessor Control
  - DATA Polling
  - READ/BUSY Open Drain Output on TSOP
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Low Voltage CMOS Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

The AT28BV16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28BV16 is a 16K memory organized as 2,048 words by 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

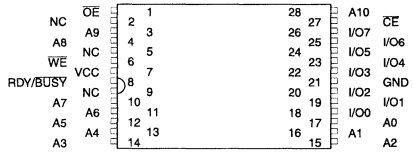
The AT28BV16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched

(continued)

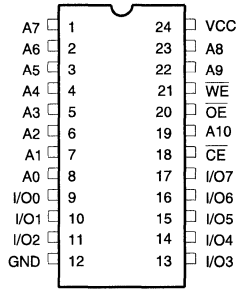
Pin Configurations

Pin Name	Function
A0 - A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

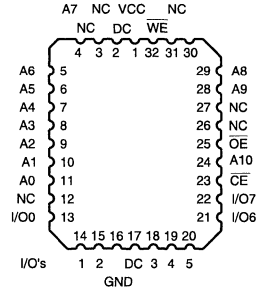
TSOP
Top View



PDIP, SOIC
Top View



PLCC
Top View



0308A

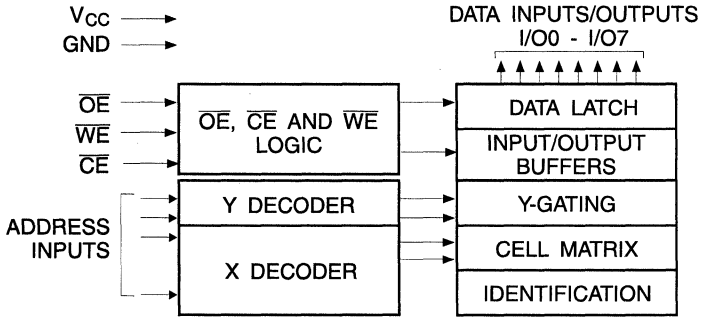
Description (Continued)

internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by DATA polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 250 ns at low power dissipation. When the chip is deselected the standby current is less than 50 µA.

Atmel's 28BV16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes of E^2PROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28BV16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28BV16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

$\overline{\text{DATA}}$ POLLING: The AT28BV16 provides $\overline{\text{DATA}}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

READY/$\overline{\text{BUSY}}$ (TSOP only): READY/$\overline{\text{BUSY}}$ is an open drain output; it is pulled low during the internal write cycle and released at the completion of the write cycle.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense— if Vcc is below 2.0V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 2.0V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

DEVICE IDENTIFICATION: An extra 32-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28BV16-25	AT28BV16-30
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

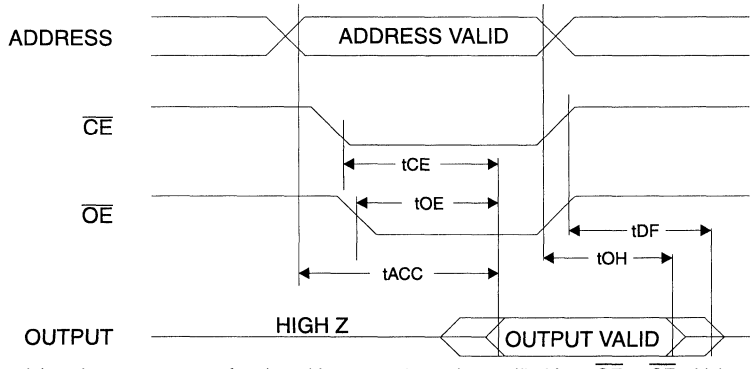
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1.0V		5	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		5	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V		50	µA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA; CE = V_{IL}		8	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.3	V
		I_{OL} = 2 mA for RDY/$\overline{BUSY}$		0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	2.0		V

AC Read Characteristics

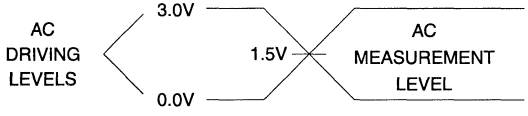
Symbol	Parameter	AT28BV16-25 Min	AT28BV16-25 Max	AT28BV16-30 Min	AT28BV16-30 Max	Units
t_{ACC}	Address to Output Delay		250		300	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		250		300	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay		100		100	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms (1, 2, 3, 4)



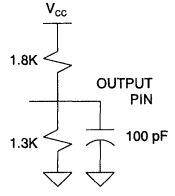
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

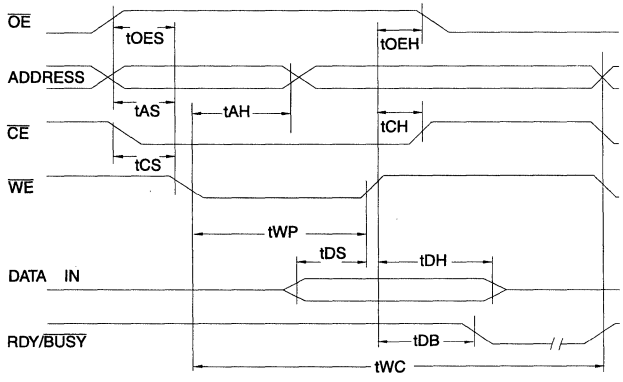
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

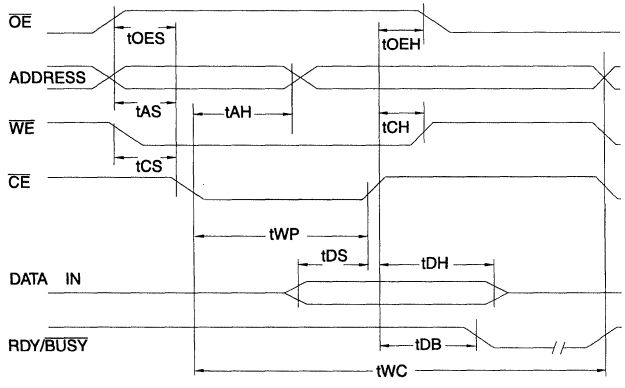
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150	1000	ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time	0		ns
t_{WC}	Write Cycle Time		3.0	ms
t_{DB}	Time to Device Busy		50	ns

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

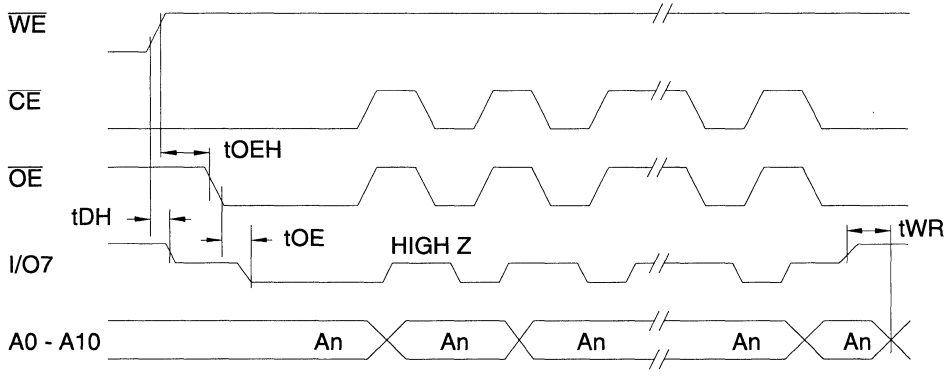


$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Characteristics.

$\overline{\text{Data}}$ Polling Waveforms



Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	8	0.05	AT28BV16-25TC AT28BV16-25JC AT28BV16-25PC AT28BV16-25SC	28T 32J 24P6 24S	Commercial (0°C to 70°C)
	8	0.05	AT28BV16-25TI AT28BV16-25JI AT28BV16-25PI AT28BV16-25SI	28T 32J 24P6 24S	Industrial (-40°C to 85°C)
300	8	0.05	AT28BV16-30TC AT28BV16-30JC AT28BV16-30PC AT28BV16-30SC	28T 32J 24P6 24S	Commercial (0°C to 70°C)
	8	0.05	AT28BV16-30TI AT28BV16-30JI AT28BV16-30PI AT28BV16-30SI	28T 32J 24P6 24S	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28BV16	25	JC, JI, PC, PI, SC, SI, TC, TI
AT28BV16	30	JC, JI, PC, PI, SC, SI, TC, TI

Package Type	
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

64K (8K x 8) *Battery-Voltage*™ CMOS E²PROM

Features

- 2.7V to 3.6V Supply
  - Full Read and Write Operation
- Low Power Dissipation
  - 8 mA Active Current
  - 50 µA CMOS Standby Current
- Read Access Time - 300 ns
- Byte Write - 3 ms
- Direct Microprocessor Control
  - $\overline{\text{DATA}}$ Polling
  - READY/$\overline{\text{BUSY}}$ Open Drain Output
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

The AT28BV64 is a low-voltage, low-power Electrically Erasable and Programmable Read Only Memory specifically designed for battery powered applications. Its 64K of memory is organized 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation less than 30 mW. When the device is deselected the standby current is less than 50 µA.

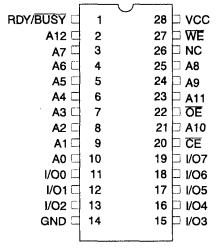
The AT28BV64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Fol-

(continued)

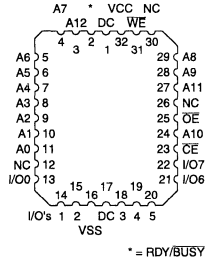
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{Busy}}$ Output
NC	No Connect
DC	Don't Connect

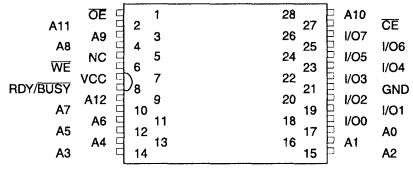
PDIP, SOIC Top View



PLCC Top View



TSOP Top View



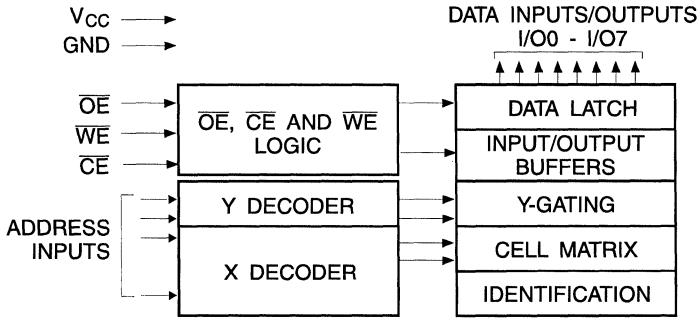
0493A

Description (Continued)

lowing the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/BUSY and DATA polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's 28BV64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes of E^2PROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on OE and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28BV64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28BV64 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line.

$\overline{DATA}$ POLLING: The AT28BV64 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) V_{CC} sense— if V_{CC} is below 1.8V (typical) the write function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached 2.0V the device will automatically time out 10 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

2

DC and AC Operating Range

		AT28BV64-30
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

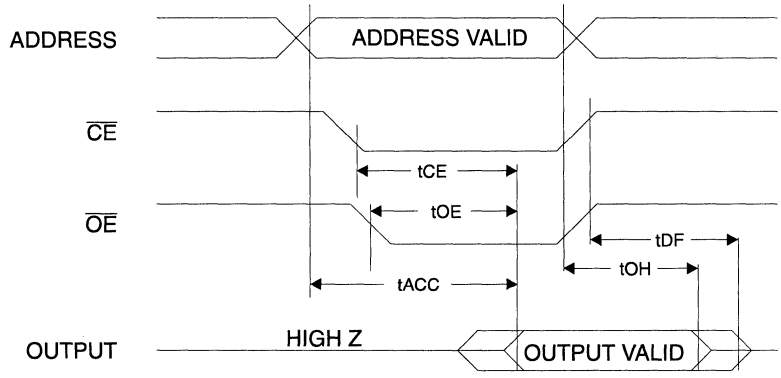
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1.0V		5	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		5	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V		50	µA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA; CE = V_{IL}		8	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.3	V
		I_{OL} = 2 mA for RDY/$\overline{BUSY}$		0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	2.0		V

AC Read Characteristics

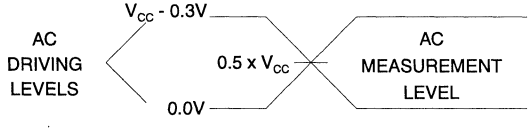
Symbol	Parameter	AT28BV64-30 Min	AT28BV64-30 Max	Units
t_{ACC}	Address to Output Delay		300	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		300	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	150	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

AC Read Waveforms (1, 2, 3, 4)



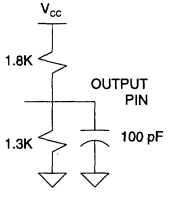
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

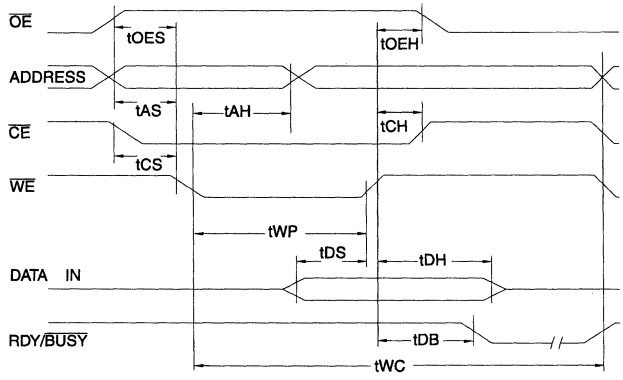
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

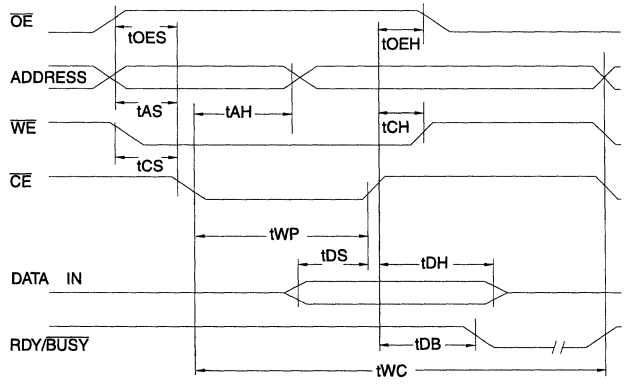
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150	1000	ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{DB}	Time to Device Busy		50	ns
t_{WC}	Write Cycle Time		3	ms

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

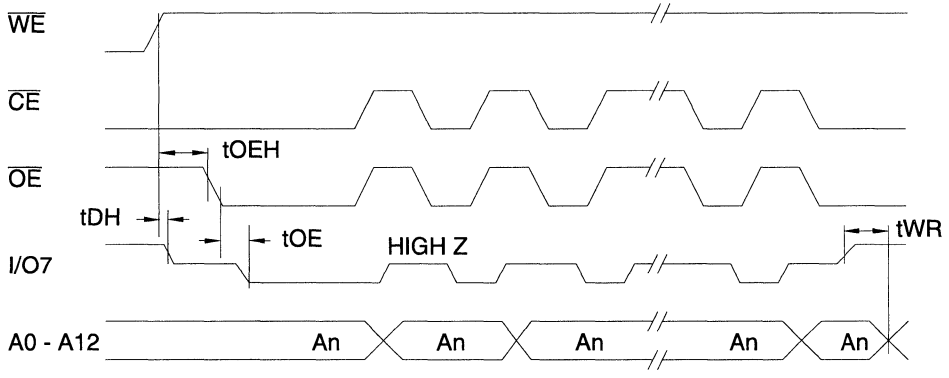


$\overline{\text{Data}}$ Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms



Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Operating Voltage	Ordering Code	Package	Operation Range
	Active	Standby				
300	8	0.05	2.7V to 3.6V	AT28BV64-30JC AT28BV64-30PC AT28BV64-30SC AT28BV64-30TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	8	0.05	2.7V to 3.6V	AT28BV64-30JI AT28BV64-30PI AT28BV64-30SI AT28BV64-30TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28BV64	30	JC, JI, PC, PI, SC, SI, TC, TI

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

64K (8K x 8) Low Voltage CMOS E^2PROM with Page Write and Software Data Protection

Features

- Single 3.3V ± 10% Supply
- 3-Volt-Only Read and Write Operation
- Software-Protected Programming
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Fast Read Access Time – 200 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64-Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10,000 Cycles
  - Data Retention: 10 Years
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

The AT28LV64B is a high-performance electrically erasable programmable read only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 20 µA.

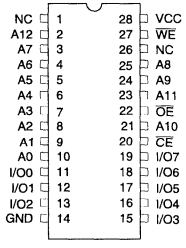
The AT28LV64B is accessed like a static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow

(continued)

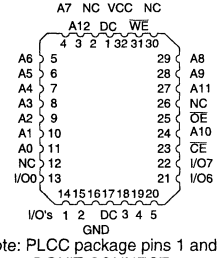
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PDIP, SOIC
Top View

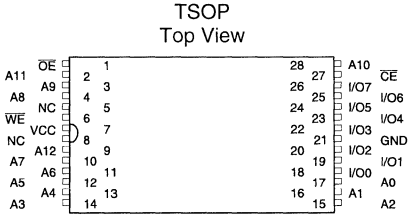


PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

TSOP
Top View



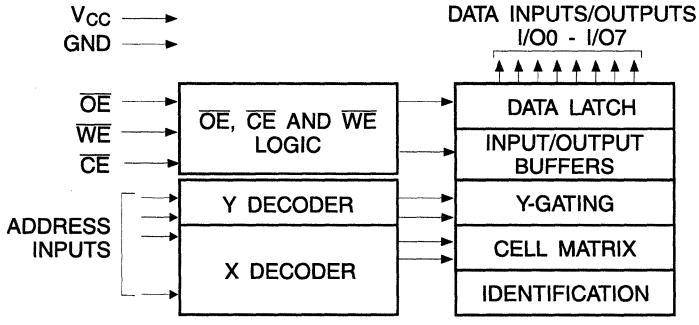
0299C

Description (Continued)

writing of up to 64-bytes simultaneously. During a write cycle, the addresses and 1 to 64-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28LV64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. A software data protection mechanism guards against inadvertent writes. The device also includes an extra 64-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28LV64B is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28LV64B allows 1 to 64-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 100 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28LV64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28LV64B features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28LV64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28LV64B in the following ways: (a) V_{CC} power-on delay– once V_{CC} has reached 1.8V (typical) the device will automatically time out 10 ms (typical) before allowing a write; (b) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (c) noise filter—pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software-controlled data protection feature has been implemented on the AT28LV64B. Software data protection (SDP) helps prevent inadvertent writes from corrupting the data in the device. SDP can prevent inadvertent writes during power-up and power-down as well as any other potential periods of system instability.

The AT28LV64B can only be written using the software data protection feature. A series of three write commands to specific addresses with specific data must be presented to the device before writing in the byte or page mode. The same three write commands must begin each write operation. All software write commands must obey the page mode write timing specifications. The data in the 3-byte command sequence is not written to the device; the addresses in the command sequence can be utilized just like any other location in the device.

Any attempt to write to the device without the 3-byte sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28LV64B-20	AT28LV64B-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 10%	3.3V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

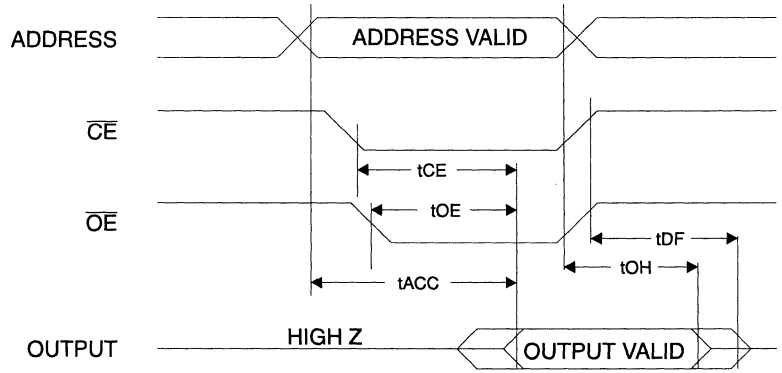
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V	Com.		20	µA
			Ind.		50	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		2.0		V

AC Read Characteristics

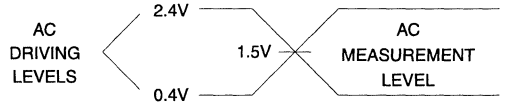
Symbol	Parameter	AT28LV64B-20 Min	AT28LV64B-20 Max	AT28LV64B-25 Min	AT28LV64B-25 Max	Units
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	80	0	100	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms (1, 2, 3, 4)



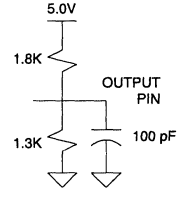
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

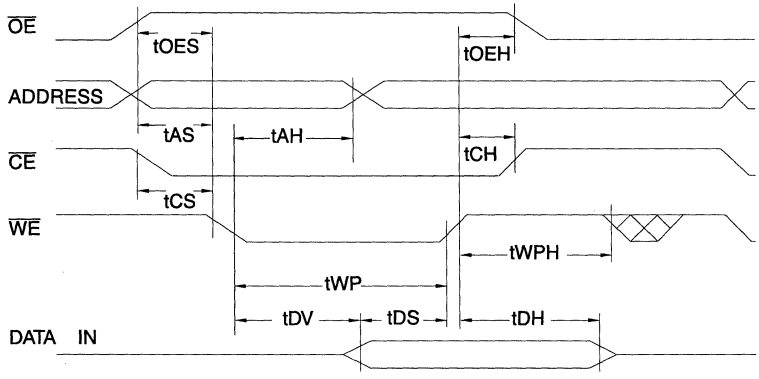
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR [1]		
t_{WPH}	Write Pulse Width High	100		ns

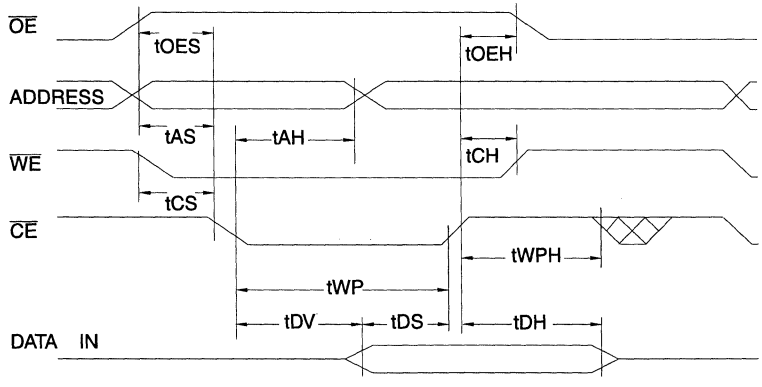
Notes: 1. NR = No Restriction.
2. All byte write operations must be preceded by the SDP command sequence.

AC Write Waveforms

$\overline{WE}$ Controlled



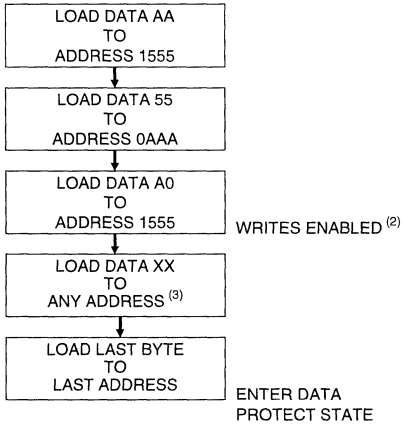
$\overline{CE}$ Controlled



Page Mode Characteristics

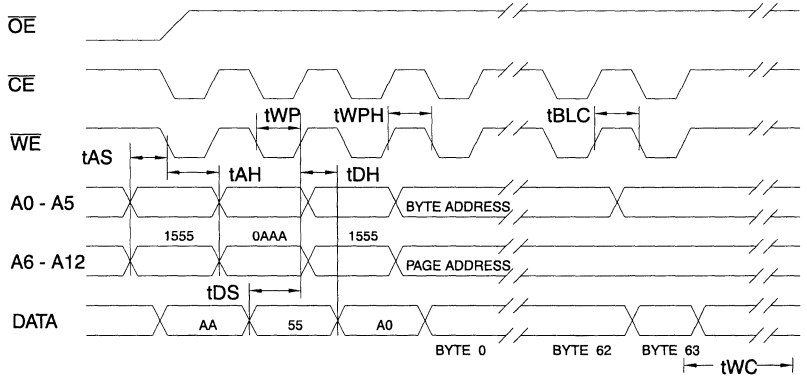
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		100	µs
t_{WPH}	Write Pulse Width High	100		ns

Write Algorithm (1)



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A12 - A0 (Hex).
2. Data protect state will be re-activated at the end of the write cycle.
3. 1 to 64-bytes of data are loaded.

Software Data Protection Write Cycle Waveforms (1, 2, 3)



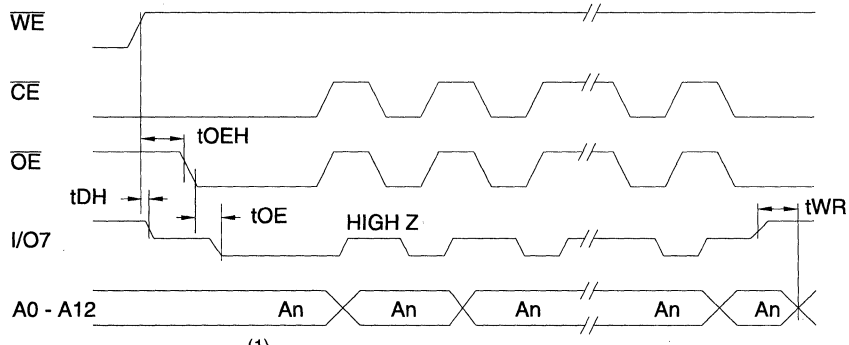
Notes: 1. A0 - A12 must conform to the addressing sequence for the first three bytes as shown above.
2. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

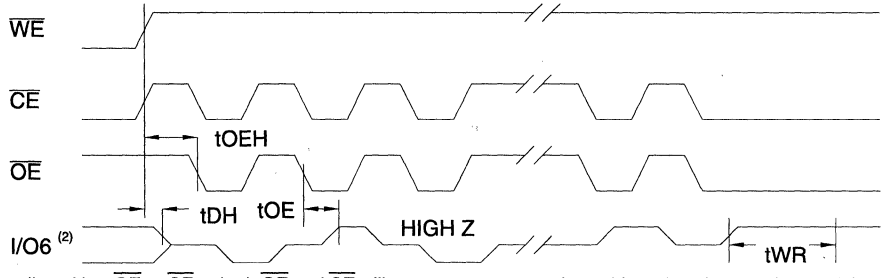


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used, but the address should not vary.

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.05	AT28LV64B-20JC AT28LV64B-20PC AT28LV64B-20SC AT28LV64B-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	15	0.05	AT28LV64B-20JI AT28LV64B-20PI AT28LV64B-20SI AT28LV64B-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	15	0.05	AT28LV64B-25JC AT28LV64B-25PC AT28LV64B-25SC AT28LV64B-25TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	15	0.05	AT28LV64B-25JI AT28LV64B-25PI AT28LV64B-25SI AT28LV64B-25TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28LV64B	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28LV64B	25	JC, JI, PC, PI, SC, SI, TC, TI

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

256K (32K x 8) Low Voltage CMOS E^2PROM

Features

- Fast Read Access Time - 200 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64-Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10,000 Cycles
  - Data Retention: 10 Years
- Single 3.3V ± 5% Supply
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

The AT28LV256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 200 µA.

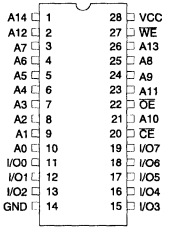
The AT28LV256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64-bytes simultaneously. During a write cycle, the addresses and 1 to

(continued)

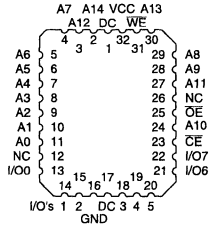
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

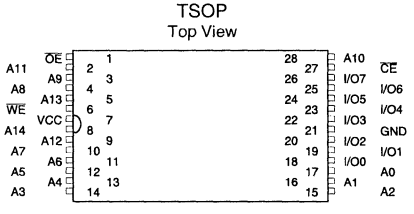
PDIP, SOIC
Top View



PLCC
Top View



TSOP
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

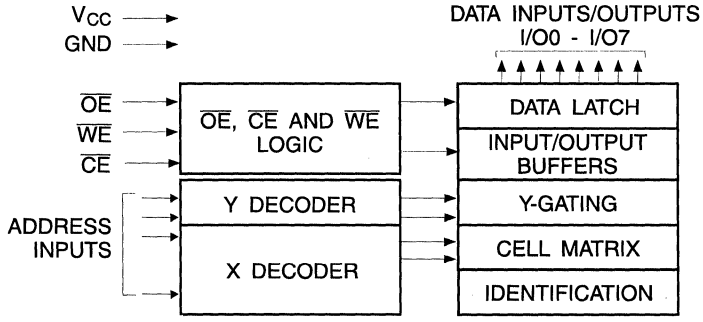
0273E

Description (Continued)

64-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28LV256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28LV256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28LV256 allows 1 to 64-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28LV256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28LV256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28LV256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28LV256 in the following ways: (a) V_{CC} power-on delay - once V_{CC} has reached 1.8V (typical) the device will automatically time out 10 ms (typical) before allowing a write: (b) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (c) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software-controlled data protection feature has been implemented on the AT28LV256. Software data protection (SDP) helps prevent inadvertent writes from corrupting the data in the device. SDP can prevent inadvertent writes during power-up and power-down as well as any other potential periods of system instability.

The AT28LV256 can only be written using the software data protection feature. A series of three write commands to specific addresses with specific data must be presented to the device before writing in the byte or page mode. The same three write commands must begin each write operation. All software write commands must obey the page mode write timing specifications. The data in the 3-byte command sequence is not written to the device; the address in the command sequence can be utilized just like any other location in the device.

Any attempt to write to the device without the 3-byte sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28LV256-20	AT28LV256-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 5%	3.3V ± 5%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.

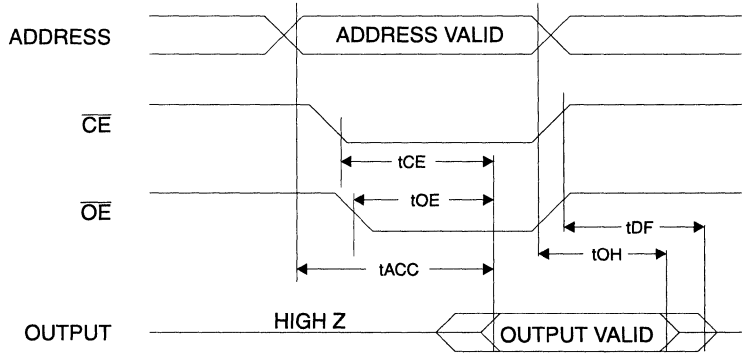
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V	Com.		20	µA
			Ind.		50	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		2.0		V

AC Read Characteristics

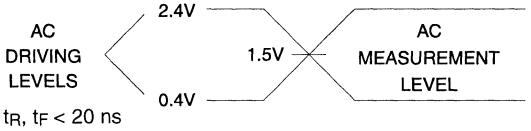
Symbol	Parameter	AT28LV256-20 Min	AT28LV256-20 Max	AT28LV256-25 Min	AT28LV256-25 Max	Units
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	80	0	100	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms (1, 2, 3, 4)



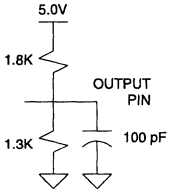
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

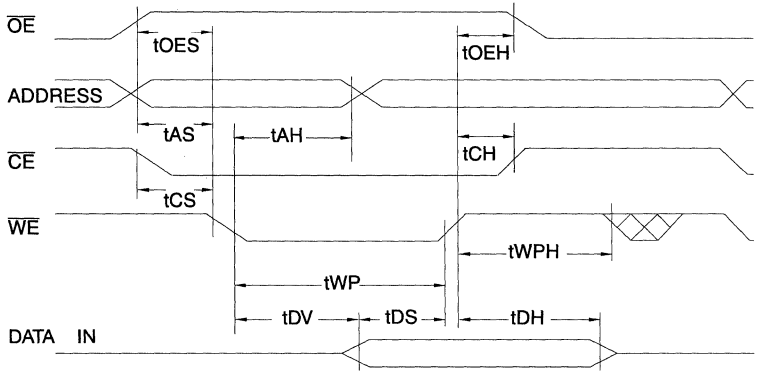
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR (1)		

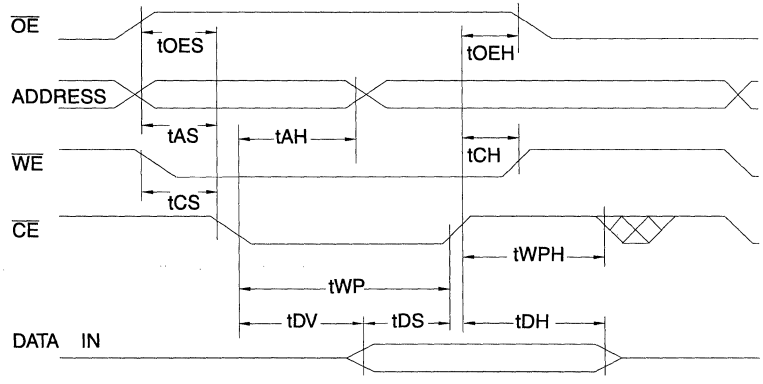
Note: 1. NR = No Restriction

AC Write Waveforms

$\overline{WE}$ Controlled



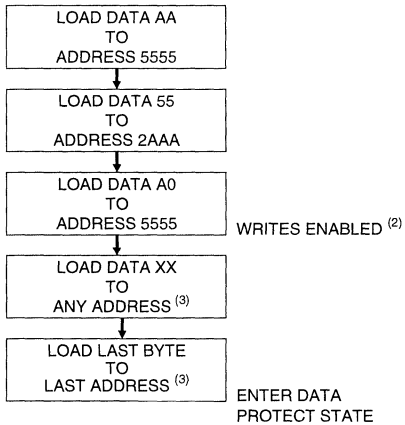
$\overline{CE}$ Controlled



Page Mode Characteristics

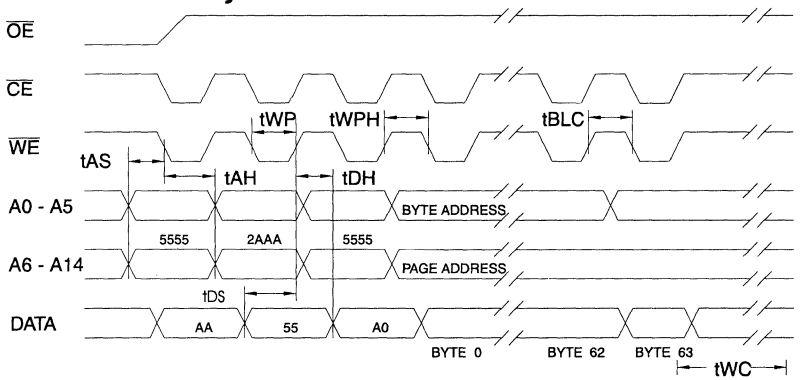
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Programming Algorithm



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data protect state will be re-activated at the end of program cycle.
3. 1 to 64-bytes of data are loaded.

Software Protected Write Cycle Waveforms (1, 2, 3)



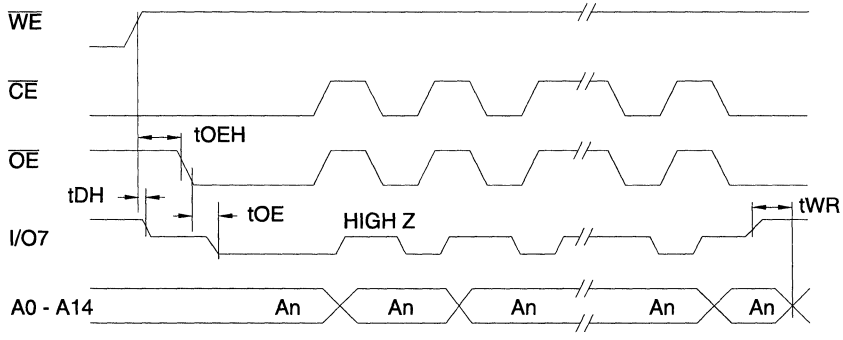
Notes: 1. A0 - A14 must conform to the addressing sequence for the first three bytes as shown above.
2. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

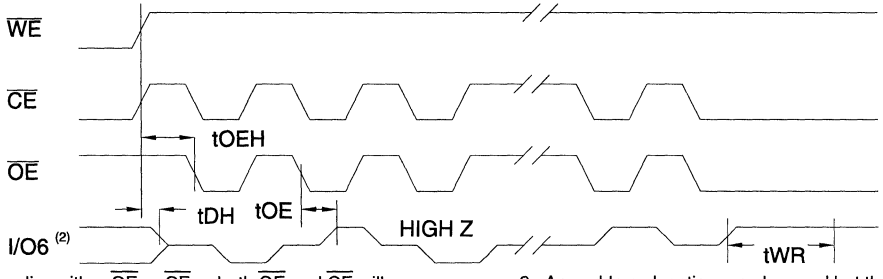


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

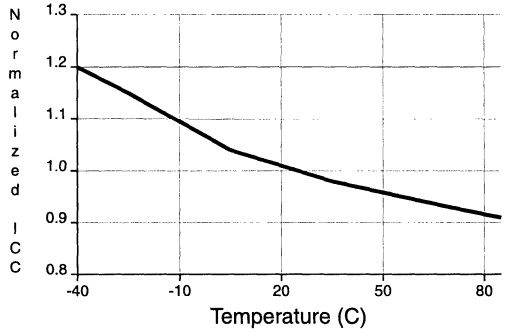
Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms

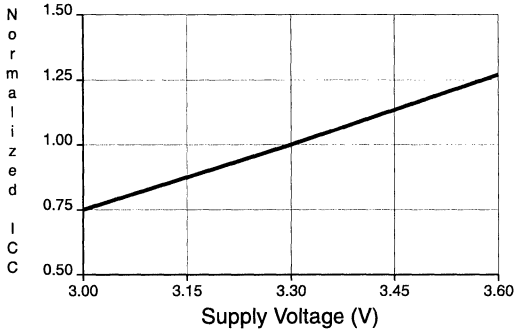


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

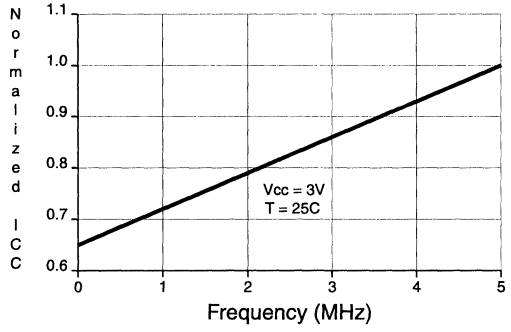
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	80	0.2	AT28LV256-20JC AT28LV256-20PC AT28LV256-20SC AT28LV256-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	80	0.2	AT28LV256-20JI AT28LV256-20PI AT28LV256-20SI AT28LV256-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	80	0.2	AT28LV256-25JC AT28LV256-25PC AT28LV256-25SC AT28LV256-25TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	80	0.2	AT28LV256-25JI AT28LV256-25PI AT28LV256-25SI AT28LV256-25TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28LV256	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28LV256	25	JC, JI, PC, PI, SC, SI, TC, TI

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

1 Megabit (128K x 8) Low Voltage Paged CMOS E^2PROM

Features

- Single 3.3V ± 10% Supply
- Fast Read Access Time - 200 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128-Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms Maximum
  - 1 to 128-Byte Page Write Operation
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000K Cycles
  - Data Retention: 10 Years
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

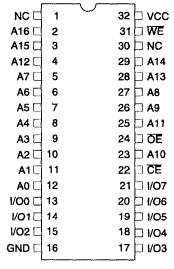
The AT28LV010 is a high-performance 3-volt only Electrically Erasable and Programmable Read Only Memory. Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 20 µA.

Pin Configurations

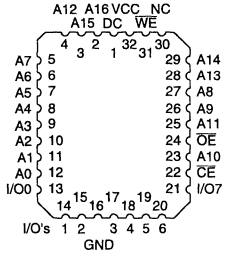
(continued)

Pin Name	Function
A0 - A16	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

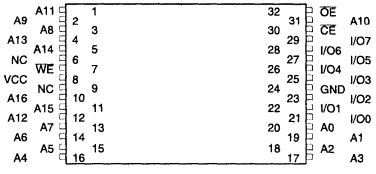
PDIP
Top View



PLCC
Top View



TSOP
Top View



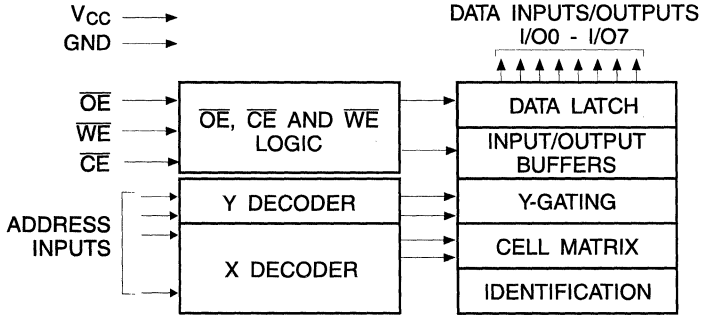
0395A

Description (Continued)

The AT28LV010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128-bytes simultaneously. During a write cycle, the address and 1 to 128-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28LV010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. Software data protection is implemented to guard against inadvertent writes. The device also includes an extra 128-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28LV010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

WRITE: The write operation of the AT28LV010 allows 1 to 128-bytes of data to be written into the device during a single internal programming period. Each write operation must be preceded by the software data protection (SDP) command sequence. This sequence is a series of three unique write command operations that enable the internal write circuitry. The command sequence and the data to be written must conform to the software protected write cycle timing. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last and data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28LV010 will cease accepting data and commence the interal programming operation. If more than one data byte is to be written during a single programming operation, they must reside on the same page as defined by the state of the A7 - A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28LV010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28LV010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28LV010 in the following ways: (a) V_{CC} power-on delay - once V_{CC} has reached 2.0V (typical) the device will automatically time out 5 ms (typical) before allowing a write: (b) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (c) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: The AT28LV010 incorporates the industry standard software data protection (SDP) function. Unlike standard 5-volt only E^2PROM's, the AT28LV010 has SDP enabled at all times. Therefore, all write operations must be preceded by the SDP command sequence.

The data in the 3-byte command sequence is not written to the device; the addresses in the command sequence can be utilized just like any other location in the device. Any attempt to write to the device without the 3-byte sequence will start the internal timers. No data will be written to the device. However, for the duration of t_{WC}, read operations will effectively be polling operations.

DC and AC Operating Range

		AT28LV010-20	AT28LV010-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 5%	3.3V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

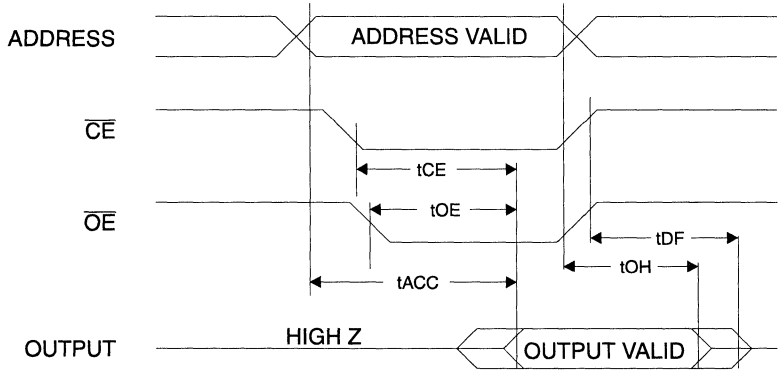
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V	Com.		20	µA
			Ind.		50	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

AC Read Characteristics

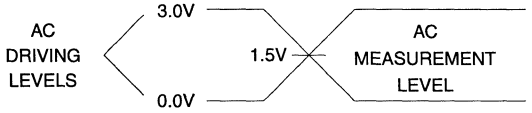
Symbol	Parameter	AT28LV010-20 Min	AT28LV010-20 Max	AT28LV010-25 Min	AT28LV010-25 Max	Units
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	80	0	100	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms (1, 2, 3, 4)



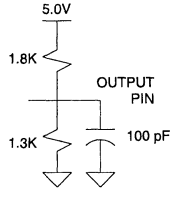
Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

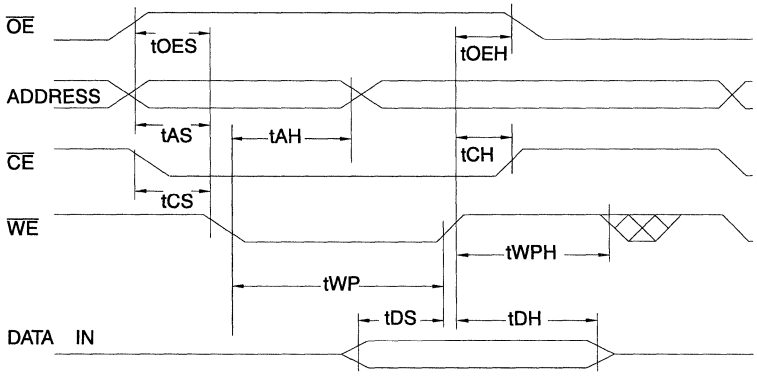
AC Write Characteristics (1)

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns

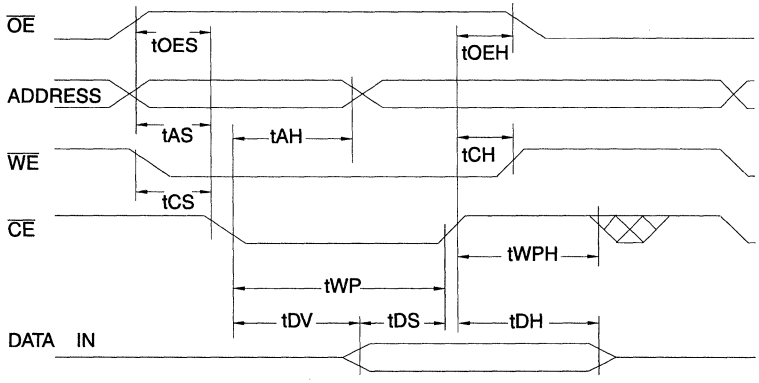
Note: 1. All write operations must be preceded by the SDP command sequence.

AC Write Waveforms

$\overline{WE}$ Controlled



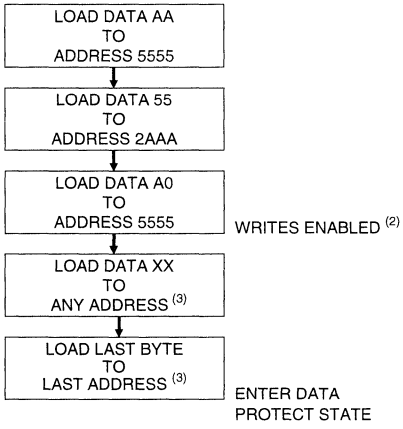
$\overline{CE}$ Controlled



Software Protected Write Characteristics

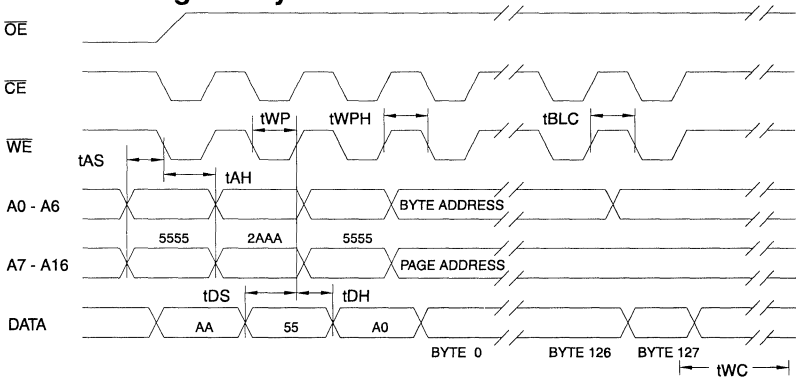
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Programming Algorithm



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data protect state will be re-activated at the end of program cycle.
3. 1 to 128-bytes of data are loaded.

Software Protected Program Cycle Waveforms (1, 2, 3)



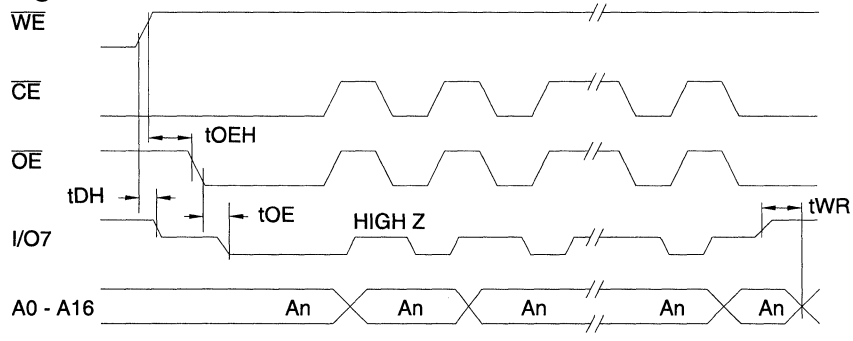
Notes: 1. A0 - A14 must conform to the addressing sequence for the first 3-bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7 - A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

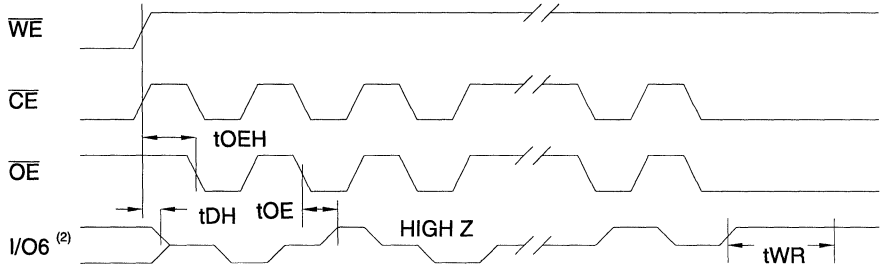


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.2	AT28LV010-20JC AT28LV010-20PC AT28LV010-20TC	32J 32P6 32T	Commercial (0° to 70°C)
	15	0.2	AT28LV010-20JI AT28LV010-20PI AT28LV010-20TI	32J 32P6 32T	Industrial (-40° to 85°C)
250	15	0.2	AT28LV010-25JC AT28LV010-25PC AT28LV010-25TC	32J 32P6 32T	Commercial (0° to 70°C)
	15	0.2	AT28LV010-25JI AT28LV010-25PI AT28LV010-25TI	32J 32P6 32T	Industrial (-40° to 85°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28LV010	20	JC, JI, PC, PI, TC, TI
AT28LV010	25	JC, JI, PC, PI, TC, TI

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

16K (2K x 8) CMOS E^2PROM

Features

- Fast Read Access Time - 150 ns
- Fast Byte Write - 200 µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - DATA POLLING
- Low Power
  - 30 mA Active Current
  - 100 µA CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- 5V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

The AT28C16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C16 is a 16K memory organized as 2,048 words by 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

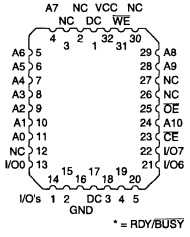
The AT28C16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched

(continued)

Pin Configurations

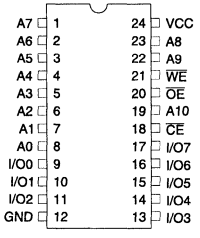
Pin Name	Function
A0 - A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

PDIP, SOIC
Top View



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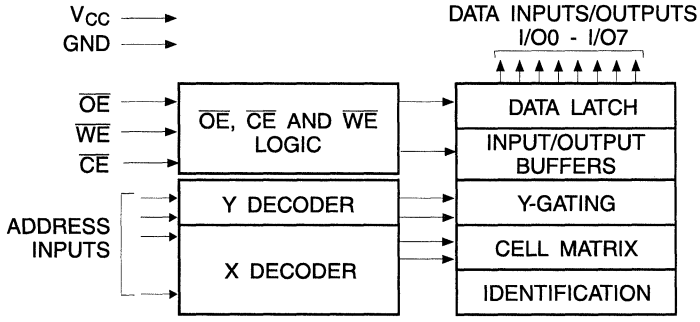
Description (Continued)

internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by DATA POLLING of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes of E^2PROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

FAST BYTE WRITE: The AT28C16E offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

$\overline{\text{DATA}}$ POLLING: The AT28C16 provides $\overline{\text{DATA}}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) V_{CC} sense— if V_{CC} is below 3.8V (typical) the write function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28C16-15
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

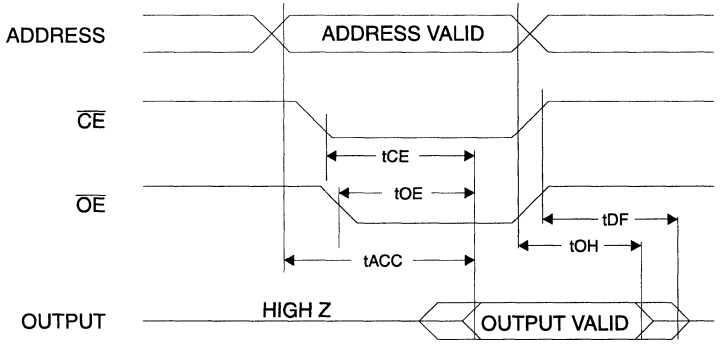
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1.0V	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

AC Read Characteristics

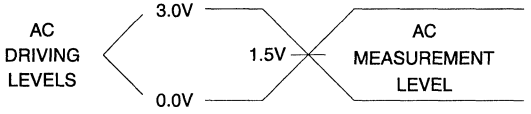
Symbol	Parameter	AT28C16-15 Min	AT28C16-15 Max	Units
t_{ACC}	Address to Output Delay		150	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

AC Read Waveforms (1, 2, 3, 4)



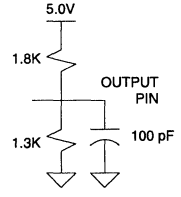
Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

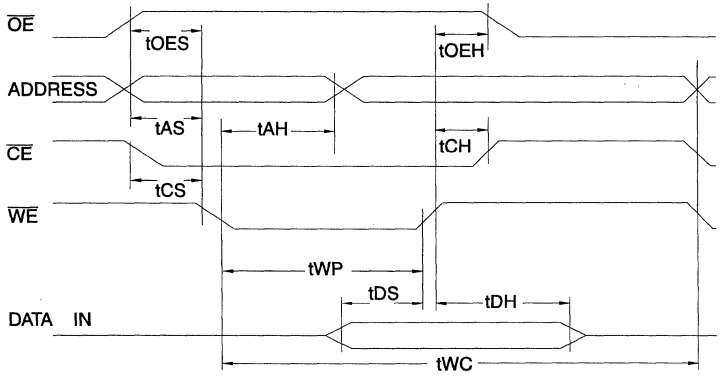
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

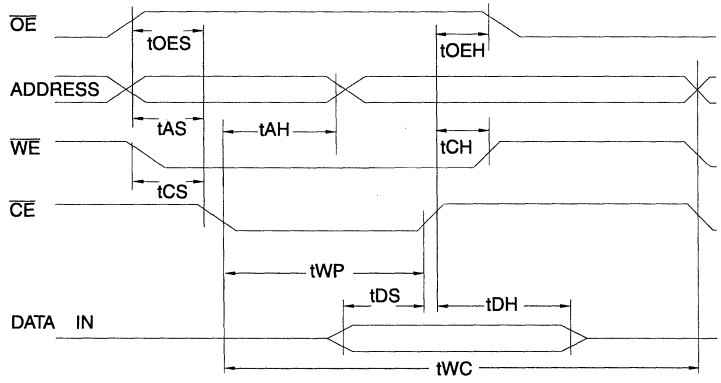
Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time		0			ns
t_{WC}	Write Cycle Time	AT28C16		0.5	1.0	ms
		AT28C16E		100	200	µs

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

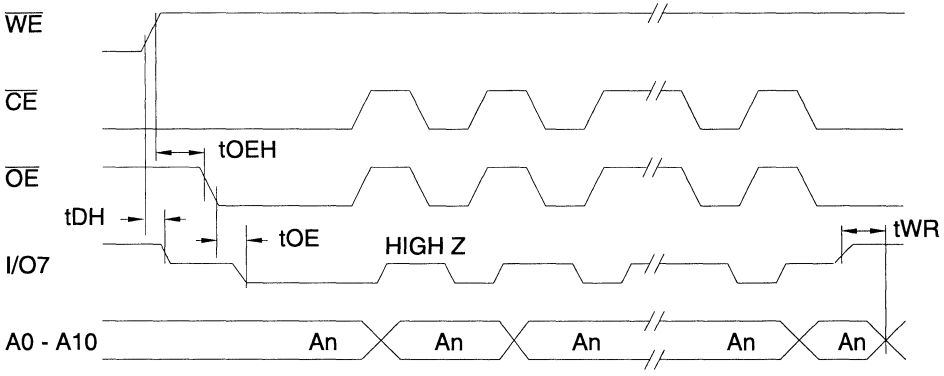


$\overline{\text{Data}}$ Polling Characteristics [1]

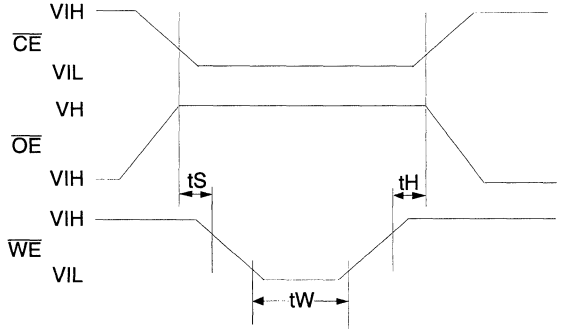
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

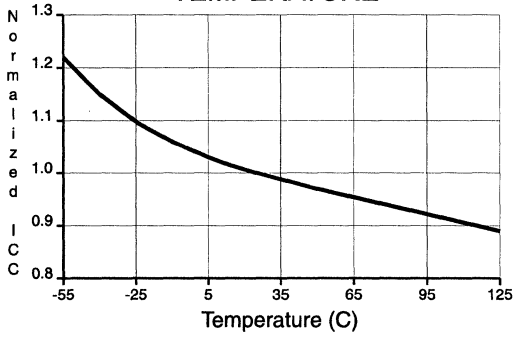


Chip Erase Waveforms

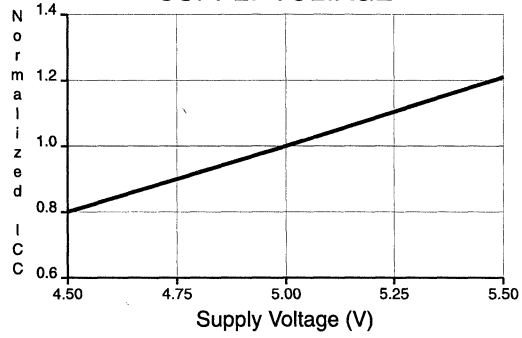


$t_S = t_H = 1\ \mu sec$ (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

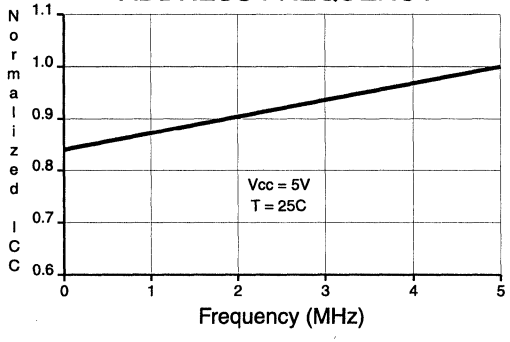
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



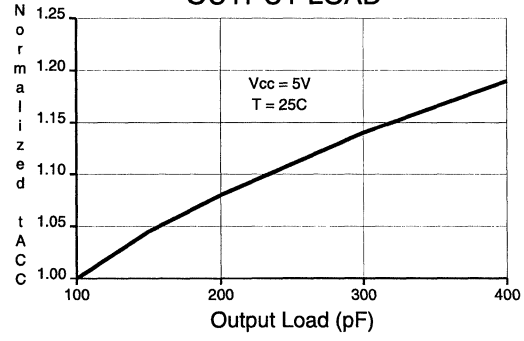
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



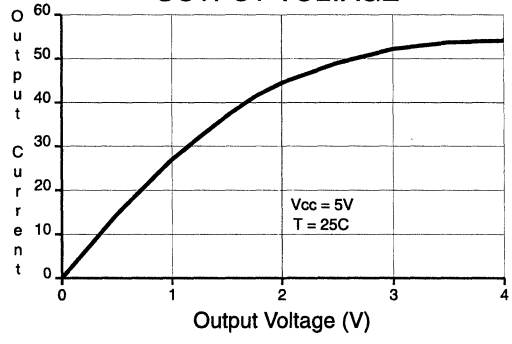
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



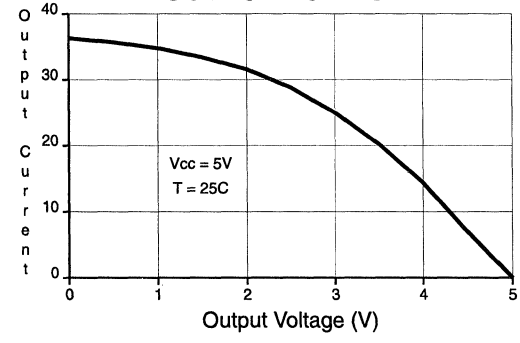
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16(E)-15JC AT28C16(E)-15PC AT28C16(E)-15SC	32J 24P6 24S	Commercial (0°C to 70°C)
	45	0.1	AT28C16(E)-15JI AT28C16(E)-15PI AT28C16(E)-15SI	32J 24P6 24S	Industrial (-40°C to 85°C)
250	30	0.1	AT28C16-W	DIE	Commercial (0°C to 70°C)

Notes: 1. See Valid Part Number table below.
2. The 28C16 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 150 ns T_{AA} offering.
3. The 28C16 ceramic package offerings have been removed. New designs should utilize the 28C256 ceramic offerings.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C16	15	JC, JI, PC, PI, SC, SI
AT28C16E	15	JC, JI, PC, PI, SC, SI
AT28C16	-	W

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs

16K (2K x 8) PCMCIA Nonvolatile Attribute Memory

Features

- Ideal Rewriteable Attribute Memory
- Simple Write Operation
  - Self-Timed Byte Writes
  - On-chip Address and Data Latch for SRAM-like Write Operation
  - Fast Write Cycle Time - 1 ms
  - 5-Volt-Only Nonvolatile Writes
- End of Write Detection
  - RDY/$\overline{\text{BUSY}}$ Output
  - $\overline{\text{DATA}}$ Polling
- High Reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: 10 Years Minimum
- Single 5-Volt Supply for Read and Write
- Very Low Power
  - 30 mA Active Current
  - 100 µA Standby Current

Description

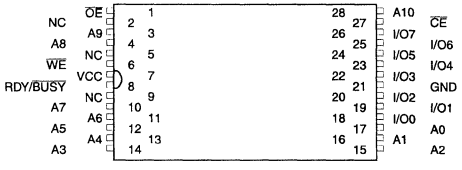
The AT28C16-T is the ideal nonvolatile attribute memory: it is a low power, 5-volt-only byte writeable nonvolatile memory (E^2PROM). Standby current is typically less than 100 µA. The AT28C16-T is written like a Static RAM, eliminating complex programming algorithms. The fast write cycle times of 1 ms, allow quick card reconfiguration in-system. Data retention is specified as 10 years minimum, precluding the necessity for batteries. Three access times have been specified to allow for varying layers of buffering between the memory and the PCMCIA interface.

The AT28C16-T is accessed like a Static RAM for read and write operations. During a byte write, the address and data are latched internally. Following the initiation of a write cycle, the device will go to a busy state and automatically write the latched data using an internal control timer. The device provides two methods for detecting the end of a write cycle; the RDY/$\overline{\text{BUSY}}$ output and $\overline{\text{DATA}}$ POLLING of I/O_7.

Pin Configurations

Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BSY}}$	Ready/Busy Output
NC	No Connect

TSOP
Top View



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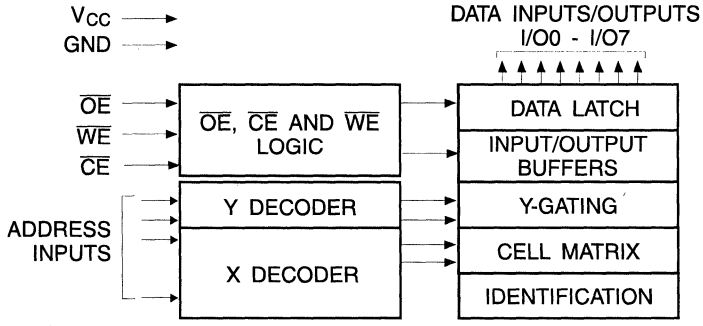
Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +125°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C16-T is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location detemined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16-T is similar to writing into a Static RAM. A low pulse on $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever occurs last) and the data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever occurs first). Once a byte write is started it will automatically time itself to completion. For the AT28C16-T the write cycle time is 1 ms maximum. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that indicates the current status of the self-timed internal write cycle. READY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain output allows OR-tying of several devices to a common interrupt input.

$\overline{DATA}$ POLLING: The AT28C16-T also provides $\overline{DATA}$ polling to signal the completion of a write cycle. During a write cycle, an attempted read of the the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all ouputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power on delay— once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16-T may be set to the high state by the Chip Clear operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12V, the chip is cleared when a 10ms low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32-bytes of E^2PROM memory are available to the user for device identifcation. By raising A_9 to 12V (± 0.5V) and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28C16-15T
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

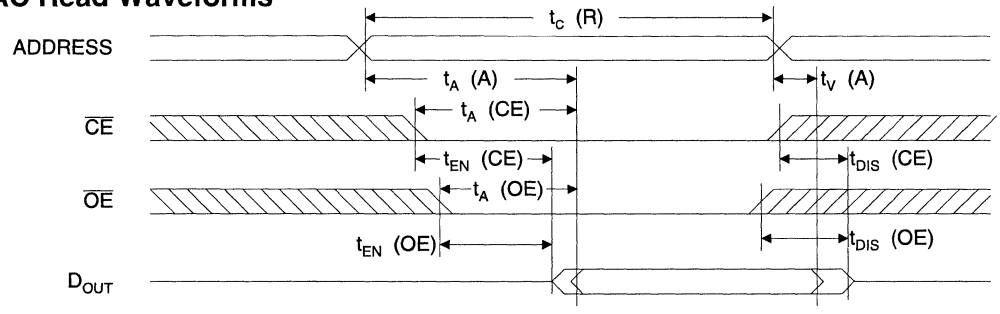
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1.0V	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

AC Read Characteristics

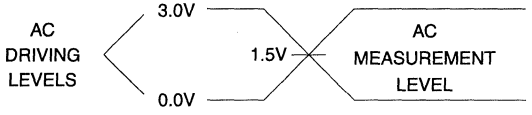
PCMCIA Symbol	Atmel Symbol	Parameter	AT28C16-15T		Units
			Min	Max	
t_C (R)	t_{RC}	Read Cycle Time	150		ns
t_A (A)	t_{ACC}	Address Access Time		150	ns
t_A (CE)	t_{CE} (1)	$\overline{CE}$ Access Time		150	ns
t_A (OE)	t_{OE} (2)	$\overline{OE}$ Access Time	0	75	ns
t_{EN} (CE)	t_{LZ} (4)	Output Enable Time From $\overline{CE}$	0		ns
t_{EN} (OE)	t_{OLZ} (4)	Output Enable Time From $\overline{OE}$	0		ns
t_V (A)	t_{OH}	Output Hold Time	0		ns
t_{DIS} (CE)	t_{DF} (3, 4)	Output Disable Time From $\overline{CE}$	0	50	ns
t_{DIS} (OE)	t_{DF} (3, 4)	Output Disable Time From $\overline{OE}$	0	50	ns

AC Read Waveforms (1, 2, 3, 4)



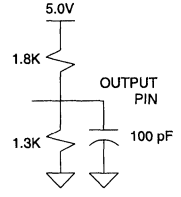
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

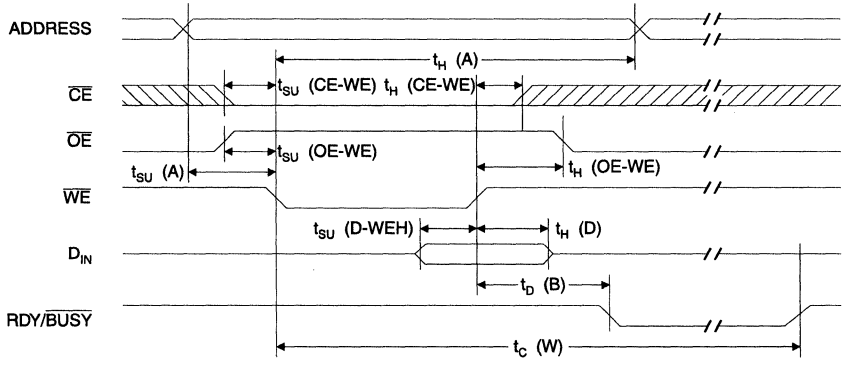
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

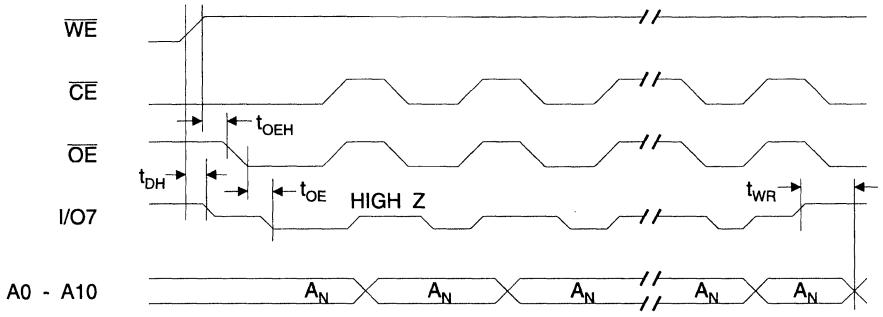
AC Write Characteristics

PCMCIA Symbol	Atmel Symbol	Parameter	Min	Max	Units
t_{SU} (A)	t_{AS}	Address Setup Time	10		ns
t_{SU} (OE-WE)	t_{OES}	Output Disable Time To $\overline{WE}$	10		ns
t_{SU} (CE-WE)	t_{CS}	Chip Enable Time To $\overline{WE}$	0		ns
t_W (WE)	t_{WP}	Write Enable Pulse Width	100	1000	ns
t_{SU} (D-WEH)	t_{DS}	Data Setup To $\overline{WE}$ High	50		ns
t_H (A)	t_{AH}	Address Hold Time From $\overline{WE}$	50		ns
t_H (D)	t_{DH}	Data Hold Time From $\overline{WE}$ High	10		ns
t_H (OE-WE)	t_{OEH}	Output Enable Hold Time From $\overline{WE}$ High	10		ns
t_H (CE-WE)	t_{CH}	Chip Enable Hold Time From $\overline{WE}$ High	0		ns
t_D (B)	t_{DB}	Delay From $\overline{WE}$ High To $\overline{BUSY}$ Asserted		50	ns
t_C (W)	t_{WC}	Write Cycle Time		1	ms

AC Write Waveforms

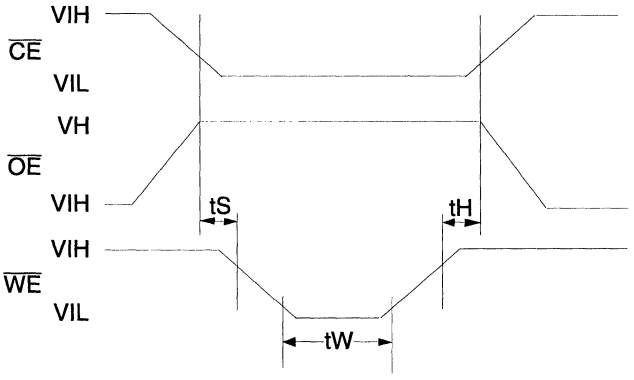


Data Polling Waveforms



Note: 1. Data Polling AC Timing Characteristics are the same as the AC Read Characteristics.

Chip Erase Waveforms



$t_S = t_H = 1\ \mu sec$ (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0 \pm 0.5V$

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16-15TC	28T	Commercial (0°C to 70°C)
	45	0.1	AT28C16-15TI	28T	Industrial (-40°C to 85°C)

Notes: 1. See Valid Part Number table below.
2. The 28C16 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 150 ns T_{AA} offering.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C16	15	TC, TI

Package Type	
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

16K (2K x 8) CMOS E^2PROM

Features

- Fast Read Access Time - 150 ns
- Fast Byte Write - 200 µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - $\overline{\text{DATA}}$ POLLING
  - READY/$\overline{\text{BUSY}}$ Open Drain Output
- Low Power
  - 30 mA Active Current
  - 100 µa CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- 5V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

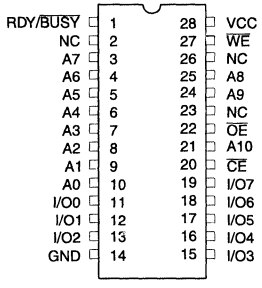
The AT28C17 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C17 is a 16K memory organized as 2,048 words by 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

(continued)

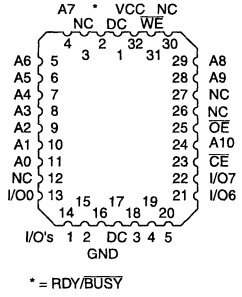
Pin Configurations

Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{Busy}}$ Output
NC	No Connect
DC	Don't Connect

PDIP, SOIC
Top View



PLCC
Top View



* = RDY/$\overline{\text{BUSY}}$

Note: PLCC package pins 1 and 17 are DON'T CONNECT.

0541A

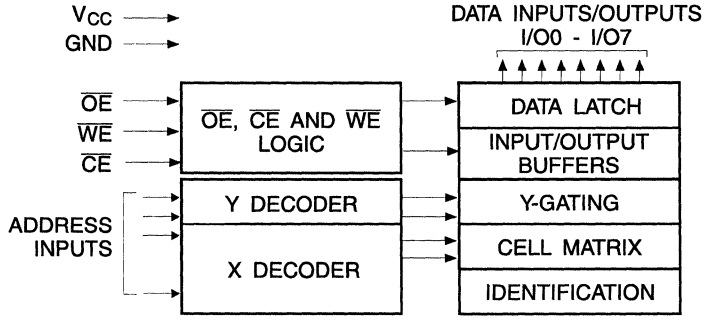
Description (Continued)

The AT28C17 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/BUSY and DATA POLLING of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C17 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes of E^2PROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on OE and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C17 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C17 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

FAST BYTE WRITE: The AT28C17E offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line.

$\overline{DATA}$ POLLING: The AT28C17 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) V_{CC} sense— if V_{CC} is below 3.8V (typical) the write function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C17 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28C17-15
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.

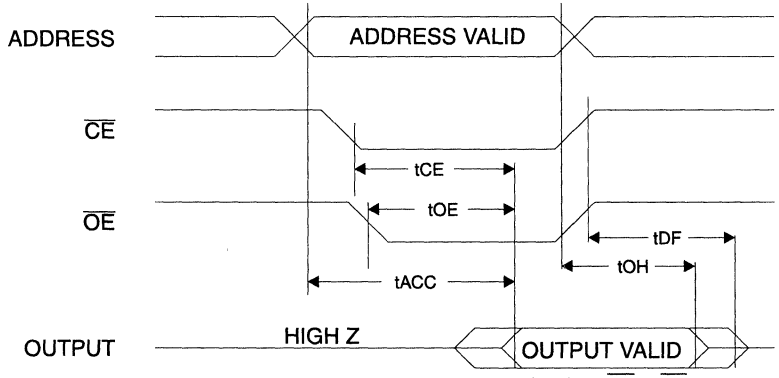
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1.0V	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA = 4.0 for RDY/$\overline{BUSY}$			.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

AC Read Characteristics

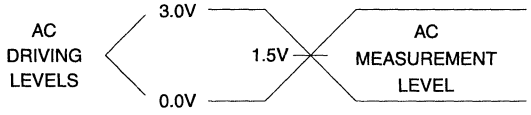
Symbol	Parameter	AT28C17-15 Min	AT28C17-15 Max	Units
t_{ACC}	Address to Output Delay		150	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

AC Read Waveforms (1, 2, 3, 4)



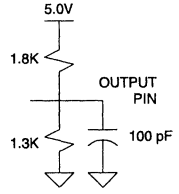
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

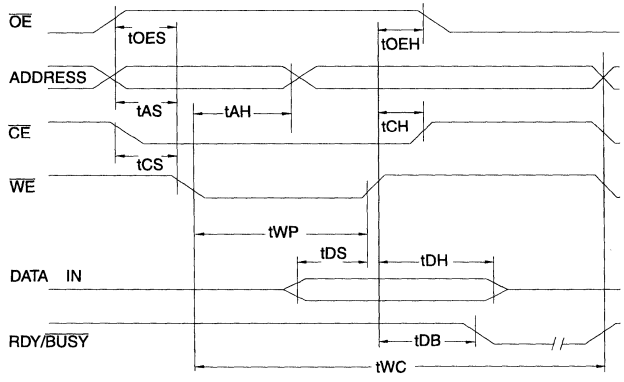
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

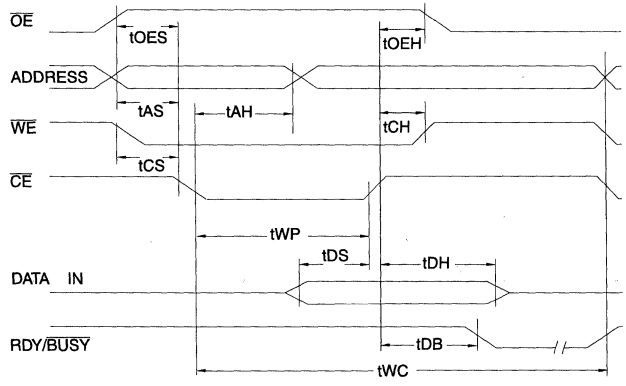
Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time		0			ns
t_{DB}	Time to Device Busy				50	ns
t_{WC}	Write Cycle Time	AT28C17		0.5	1.0	ms
		AT28C17E		100	200	µs

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

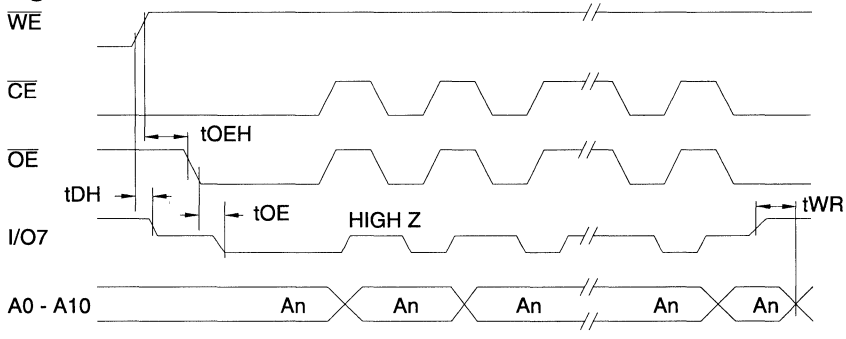


$\overline{\text{Data}}$ Polling Characteristics [1]

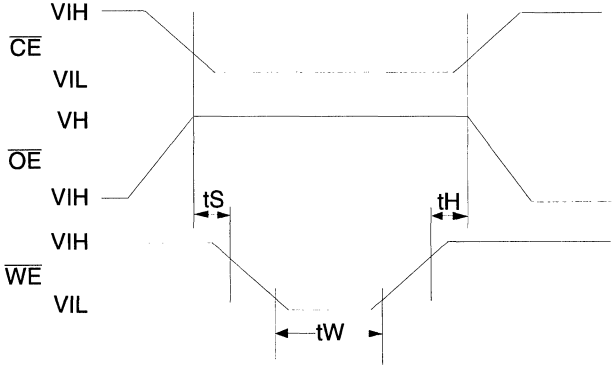
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

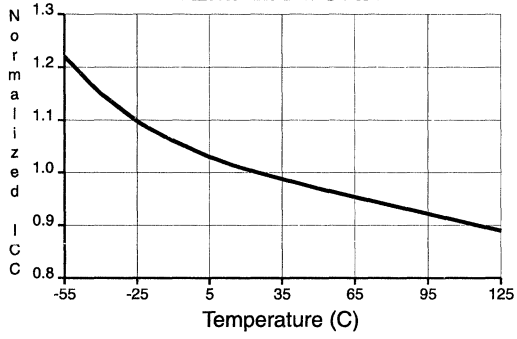


Chip Erase Waveforms

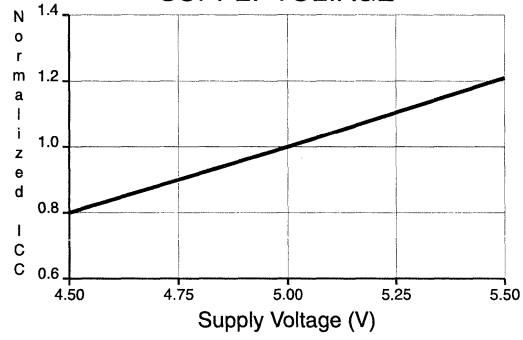


$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

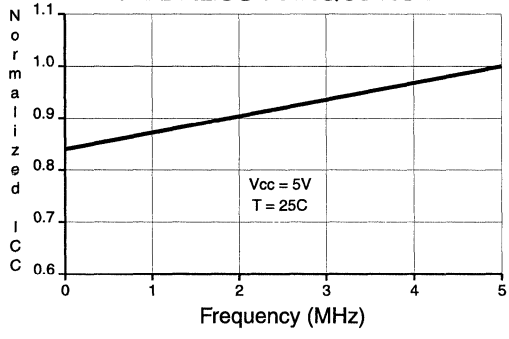
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



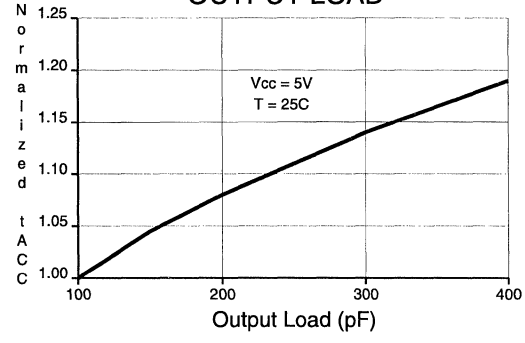
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



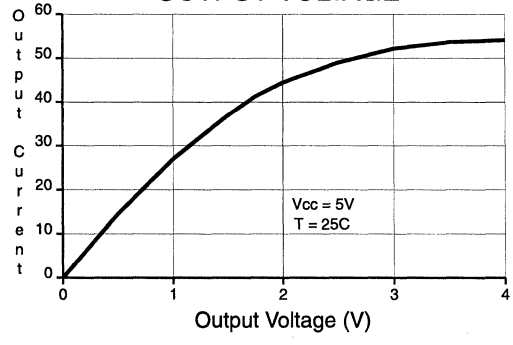
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



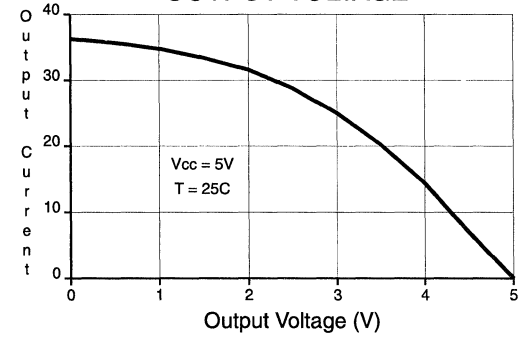
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C17(E)-15JC AT28C17(E)-15PC AT28C17(E)-15SC	32J 28P6 28S	Commercial (0°C to 70°C)
	45	0.1	AT28C17(E)-15JI AT28C17(E)-15PI AT28C17(E)-15SI	32J 28P6 28S	Industrial (-40°C to 85°C)
250	30	0.1	AT28C17-W	DIE	Commercial (0°C to 70°C)

Notes: 1. See Valid Part Number table below.
2. The 28C17 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 150 ns T_{AA} offering.
3. The 28C17 ceramic and LCC package offerings have been removed. New designs should utilize the 28C256 ceramic offerings.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C17	15	JC, JI, PC, PI, SC, SI
AT28C17E	15	JC, JI, PC, PI, SC, SI
AT28C17	-	W

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs

64K (8K x 8) CMOS E²PROM

Features

- Fast Read Access Time - 120 ns
- Fast Byte Write - 200 µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - READY/BUSY Open Drain Output
  - DATA Polling
- Low Power
  - 30 mA Active Current
  - 100 µA CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

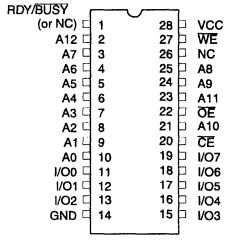
The AT28C64 is a low-power, high-performance 8,192 words by 8 bit nonvolatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features. The device is manufactured with Atmel's reliable nonvolatile technology.

(continued)

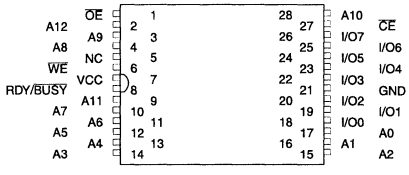
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{Busy}$ Output
NC	No Connect
DC	Don't Connect

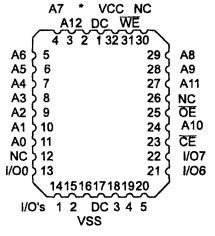
PDIP, SOIC
Top View



TSOP
Top View



LCC, PLCC
Top View



* = RDY/$\overline{BUSY}$ (or NC)

Note: PLCC package pins 1 and 17 are DON'T CONNECT.

0001F

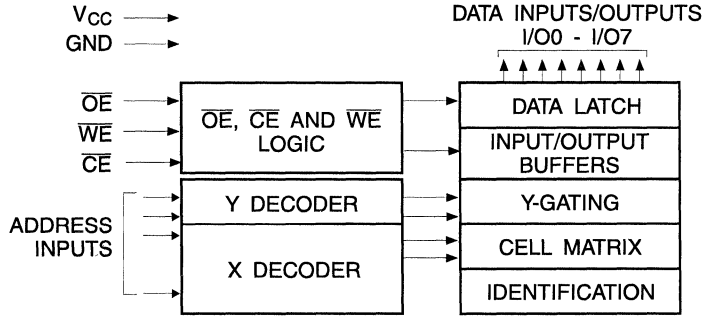
Description (Continued)

The AT28C64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{BUSY}$ (unless pin 1 is N.C.) and $\overline{DATA}$ POLLING of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The CMOS technology offers fast access times of 120 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes of E^2PROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C64 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

FAST BYTE WRITE: The AT28C64E offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 1.6 seconds.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line. Pin 1 is not connected for the AT28C64X.

$\overline{DATA}$ POLLING: The AT28C64 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) V_{CC} sense— if V_{CC} is below 3.8V (typical) the write function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C64 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28C64-12	AT28C64-15	AT28C64-20	AT28C64-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

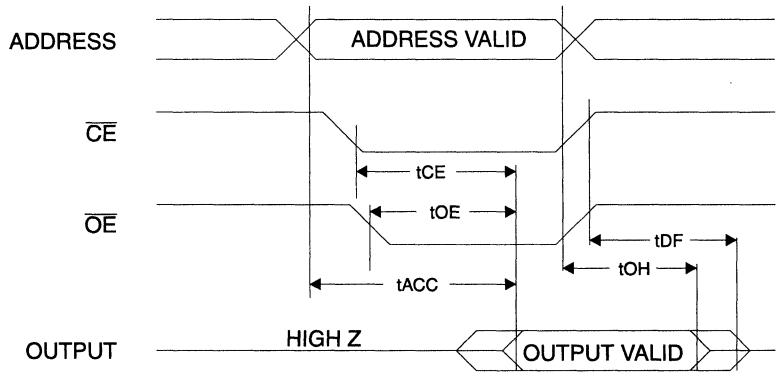
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1.0V	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA = 4.0 mA for RDY/$\overline{BUSY}$			.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

AC Read Characteristics

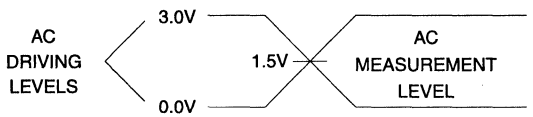
Symbol	Parameter	AT28C64-12		AT28C64-15		AT28C64-20		AT28C64-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	60	10	70	10	80	10	100	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	45	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



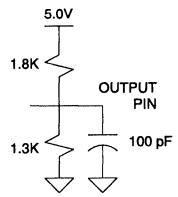
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

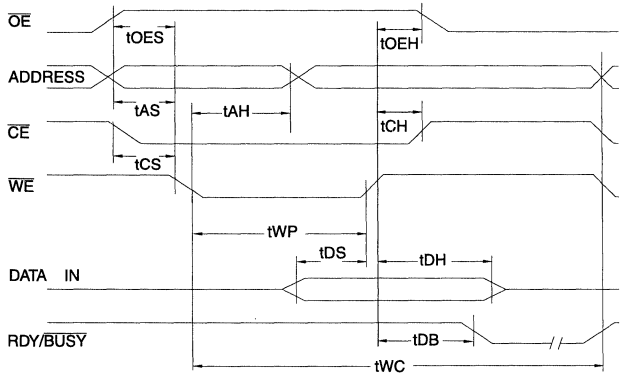
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

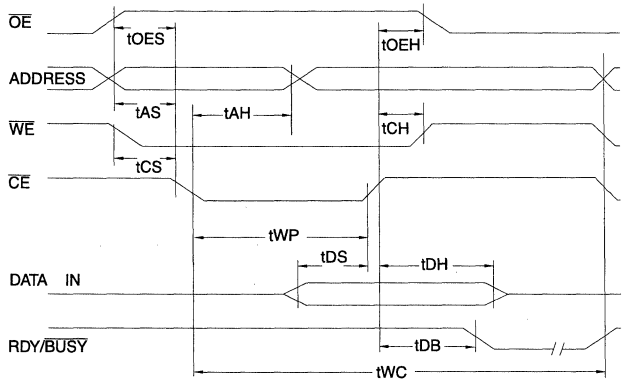
Symbol	Parameter		Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10		ns
t_{AH}	Address Hold Time		50		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100	1000	ns
t_{DS}	Data Set-up Time		50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time		10		ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time		0		ns
t_{DB}	Time to Device Busy			50	ns
t_{WC}	Write Cycle Time	AT28C64		1.0	ms
		AT28C64E		200	µs

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

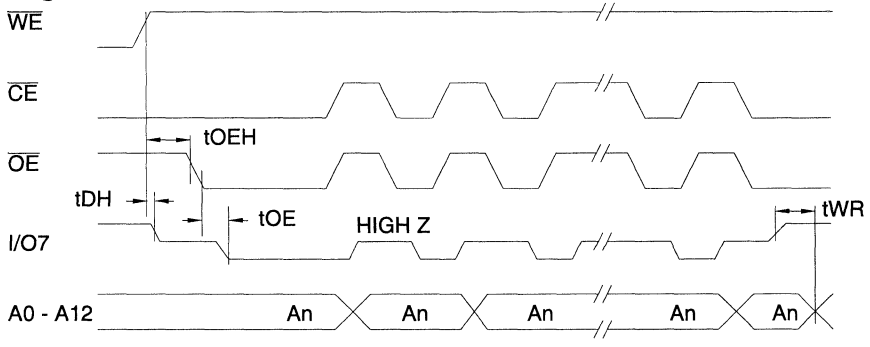


$\overline{\text{Data}}$ Polling Characteristics [1]

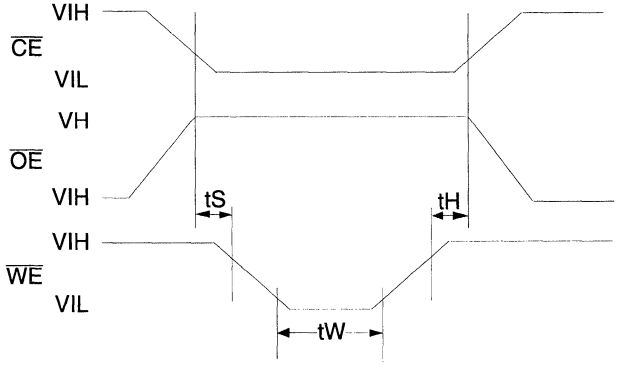
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

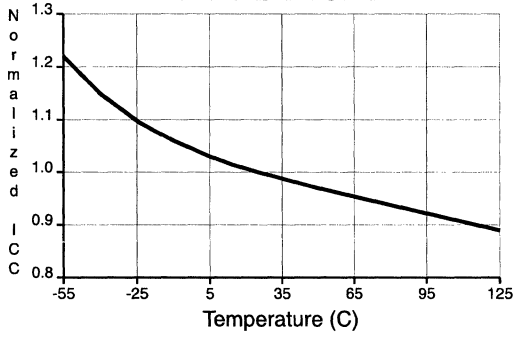


Chip Erase Waveforms

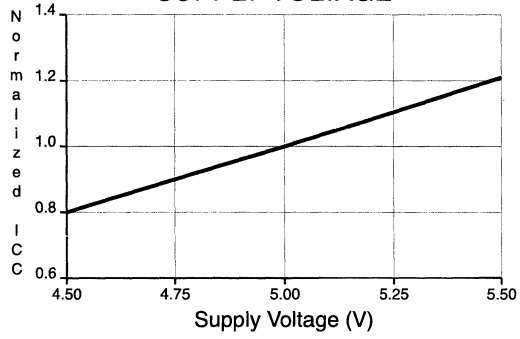


$t_S = t_H = 1\ \mu sec$ (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

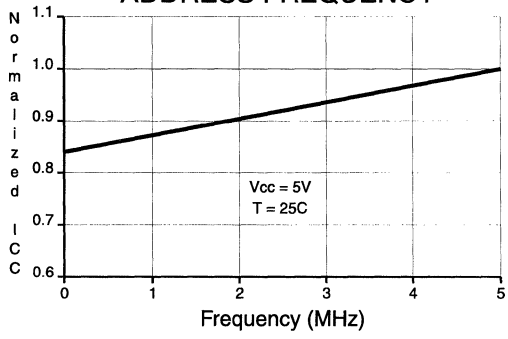
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



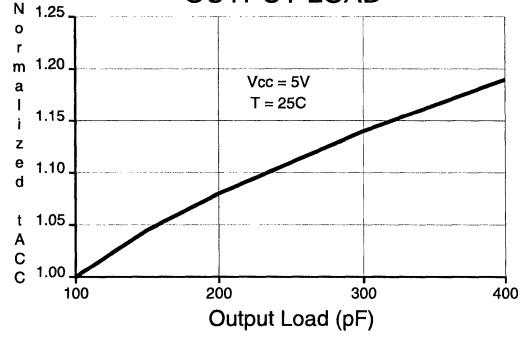
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



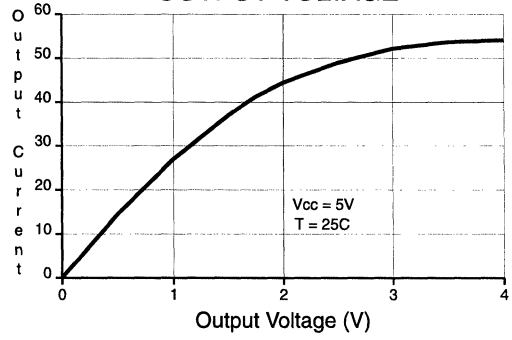
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



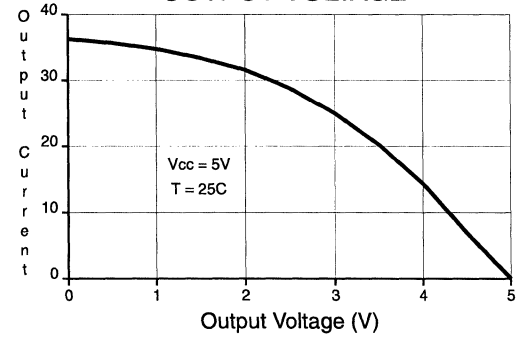
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	30	0.1	AT28C64(E)-12JC AT28C64(E)-12PC AT28C64(E)-12SC AT28C64(E)-12TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64(E)-12JI AT28C64(E)-12PI AT28C64(E)-12SI AT28C64(E)-12TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
150	30	0.1	AT28C64(E)-15JC AT28C64(E)-15PC AT28C64(E)-15SC AT28C64(E)-15TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64(E)-15JI AT28C64(E)-15PI AT28C64(E)-15SI AT28C64(E)-15TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	30	0.1	AT28C64(E)-20JC AT28C64(E)-20PC AT28C64(E)-20SC AT28C64(E)-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64(E)-20JI AT28C64(E)-20PI AT28C64(E)-20SI AT28C64(E)-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	30	0.1	AT28C64(E)-25JC AT28C64(E)-25PC AT28C64(E)-25SC AT28C64(E)-25TC AT28C64-W	32J 28P6 28S 28T DIE	Commercial (0°C to 70°C)
	45	0.1	AT28C64(E)-25JI AT28C64(E)-25PI AT28C64(E)-25SI AT28C64(E)-25TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C64X-15JC AT28C64X-15PC AT28C64X-15SC AT28C64X-15TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64X-15JI AT28C64X-15PI AT28C64X-15SI AT28C64X-15TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	30	0.1	AT28C64X-20JC AT28C64X-20PC AT28C64X-20SC AT28C64X-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64X-20JI AT28C64X-20PI AT28C64X-20SI AT28C64X-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	30	0.1	AT28C64X-25JC AT28C64X-25PC AT28C64X-25SC AT28C64X-25TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	45	0.1	AT28C64X-25JI AT28C64X-25PI AT28C64X-25SI AT28C64X-25TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C64 X	12	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64 X	15	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64 X	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64 X	25	JC, JI, PC, PI, SC, SI, TC, TI

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

64K (8K x 8) CMOS E²PROM with Page Write and Software Data Protection

Features

- Fast Read Access Time - 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64-Bytes
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 100 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

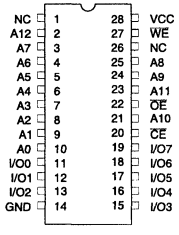
The AT28C64B is a high-performance electrically erasable and programmable read only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 µA.

(continued)

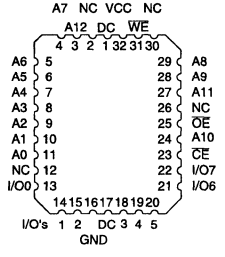
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PDIP, SOIC
Top View

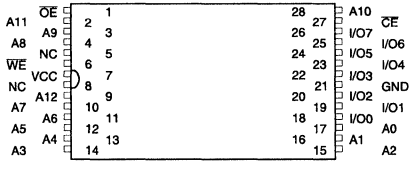


PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

TSOP
Top View



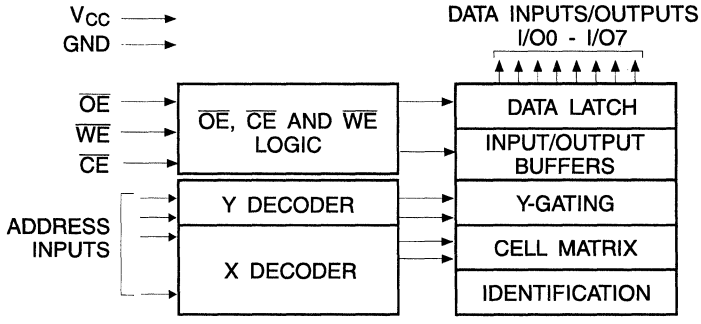
0270E

Description (Continued)

The AT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64-bytes simultaneously. During a write cycle, the addresses and 1 to 64-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28C64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C64B is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C64B allows 1 to 64-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C64B features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28C64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28C64B in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical), the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high, or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (refer to the *Software Data Protection Algorithm* diagram in this data sheet). After writing the 3-byte command sequence and waiting t_{WC}, the entire AT28C64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28C64B by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the AT28C64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device. However, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64-bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28C64B-15	AT28C64B-20	AT28C64B-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to the *AC Write Waveforms* diagrams in this data sheet.
3. $V_H = 12.0V \pm 0.5V$.

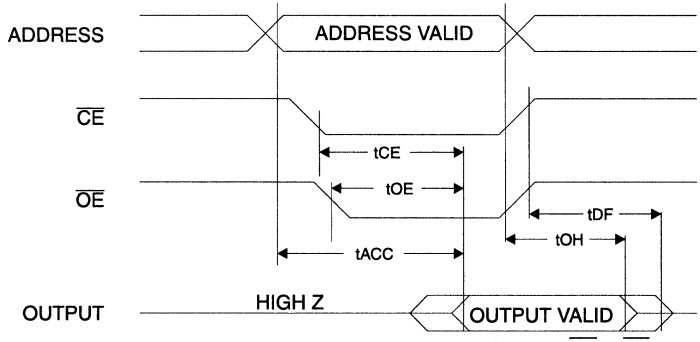
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V Com., Ind.		100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		2	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		40	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.40	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

AC Read Characteristics

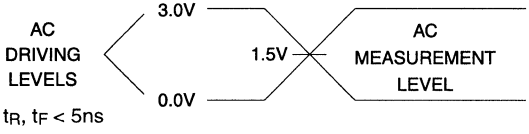
Symbol	Parameter	AT28C64B-15 Min	AT28C64B-15 Max	AT28C64B-20 Min	AT28C64B-20 Max	AT28C64B-25 Min	AT28C64B-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)

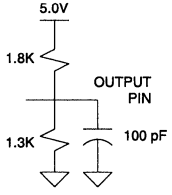


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

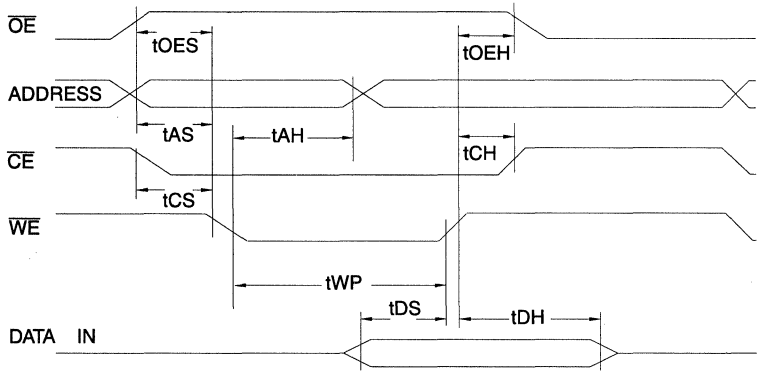
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

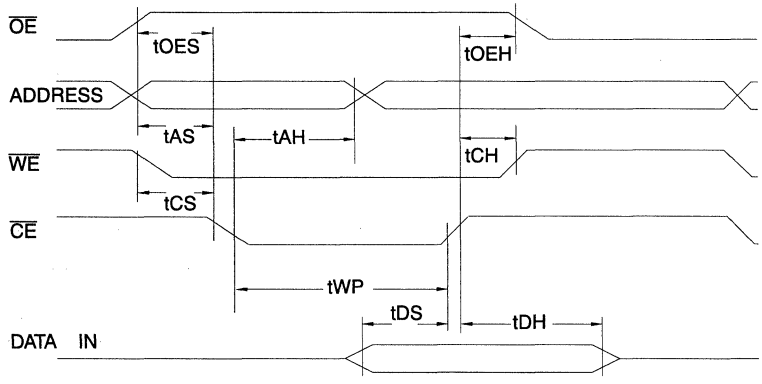
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



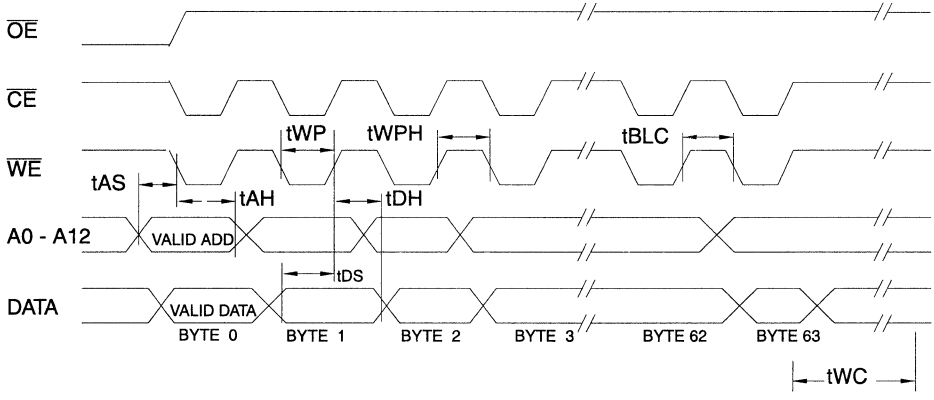
$\overline{CE}$ Controlled



Page Mode Characteristics

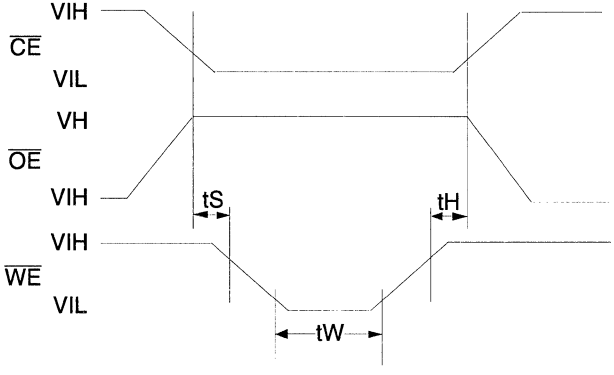
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms (1, 2)



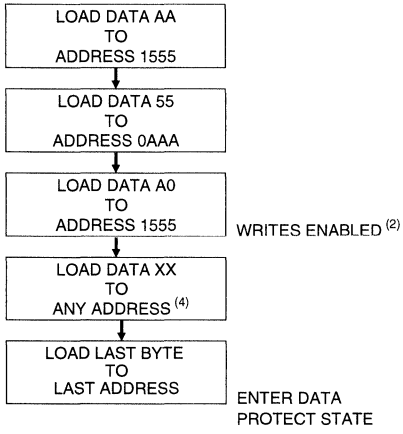
Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

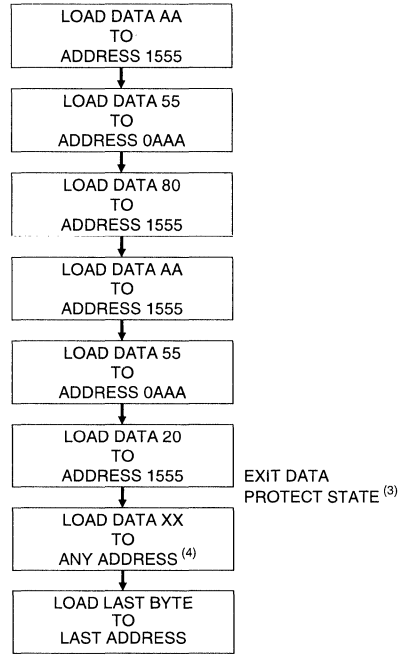


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm [1]

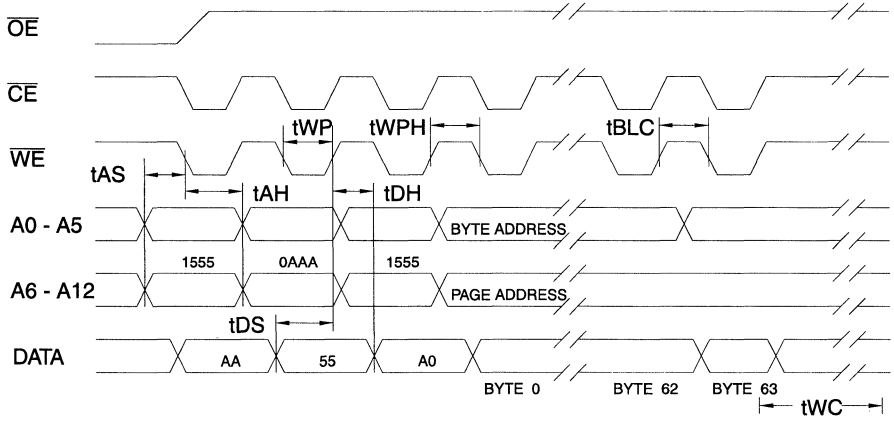


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A12 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64-bytes of data are loaded.

Software Protected Write Cycle Waveforms [1, 2]



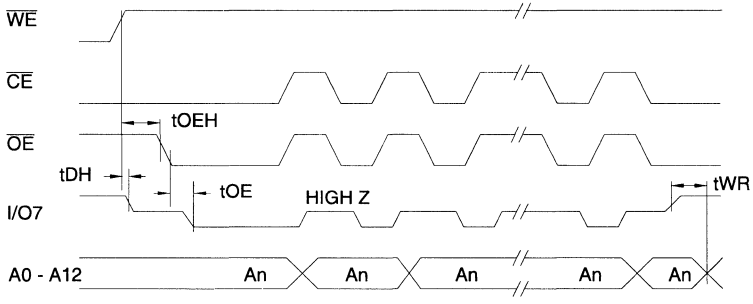
Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

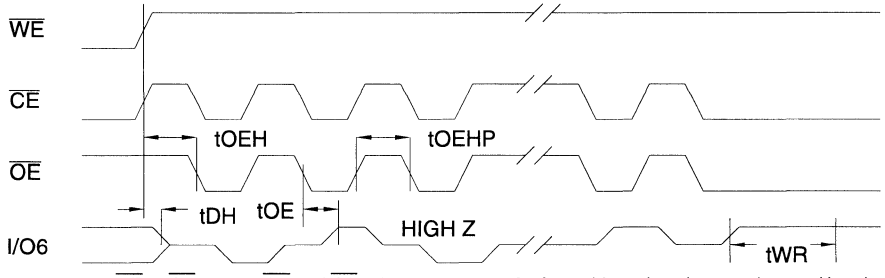


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

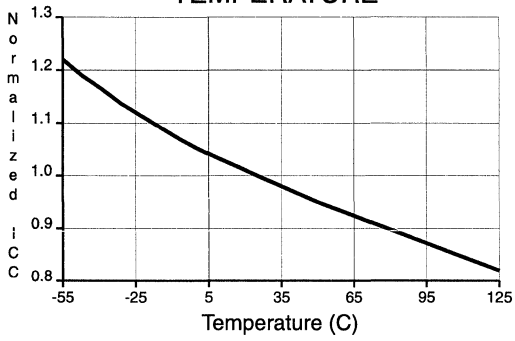
Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms (1, 2, 3)

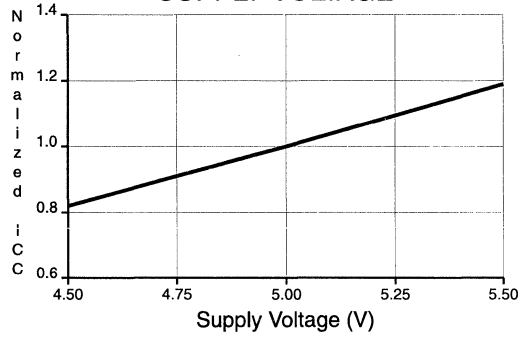


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

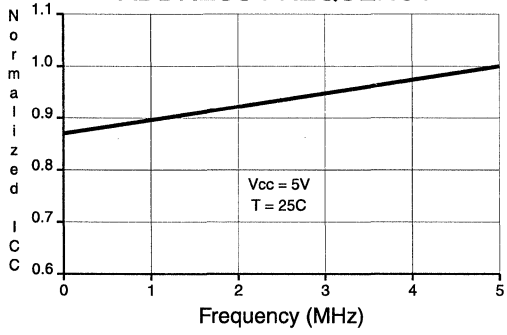
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	0.1	AT28C64B-15JC AT28C64B-15PC AT28C64B-15SC AT28C64B-15TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-15JI AT28C64B-15PI AT28C64B-15SI AT28C64B-15TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
200	40	0.1	AT28C64B-20JC AT28C64B-20PC AT28C64B-20SC AT28C64B-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-20JI AT28C64B-20PI AT28C64B-20SI AT28C64B-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
250	40	0.1	AT28C64B-25JC AT28C64B-25PC AT28C64B-25SC AT28C64B-25TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C64B-25JI AT28C64B-25PI AT28C64B-25SI AT28C64B-25TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
	40	0.1	AT28C64B-W	DIE	Commercial (0°C to 70°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C64B	15	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	25	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	-	W

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
W	DIE

256K (32K x 8) Paged CMOS E²PROM

Features

- Fast Read Access Time - 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64-Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 3 ms or 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 50 mA Active Current
  - 200 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

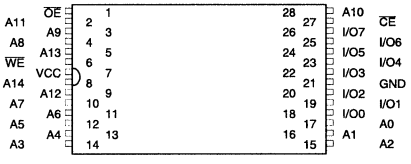
The AT28C256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 200 µA.

(continued)

Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

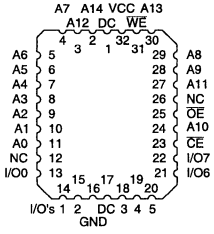
TSOP
Top View



PGA
Top View

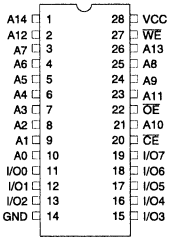
4 A6	3 A7	1 A14	27 $\overline{WE}$	26 A13
5 A5	2 A12	28 VCC	24 A9	25 A8
7 A3	6 A4		22 $\overline{OE}$	23 A11
9 A1	8 A2		20 $\overline{CE}$	21 A10
11 I/O0	10 A0	14 GND	16 I/O4	19 I/O7
12 I/O1	13 I/O2	15 I/O3	17 I/O5	18 I/O6

LCC, PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

CERDIP, PDIP, FLATPACK, SOIC
Top View



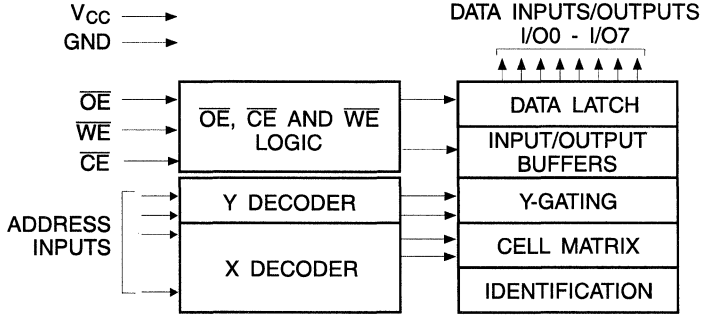
0006F

Description (Continued)

The AT28C256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64-bytes simultaneously. During a write cycle, the addresses and 1 to 64-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA POLLING of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C256 allows 1 to 64-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C256 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C256 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28C256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C256. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

(continued)

Device Operation (Continued)

DEVICE IDENTIFICATION: An extra 64-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28C256-15	AT28C256-20	AT28C256-25	AT28C256-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.

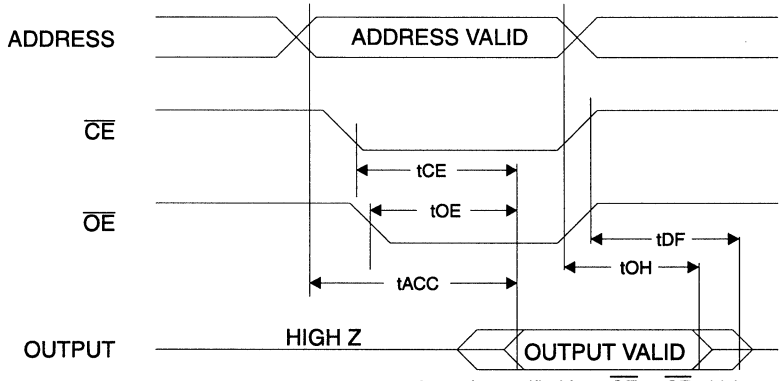
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V	Com., Ind.		200	µA
			Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

AC Read Characteristics

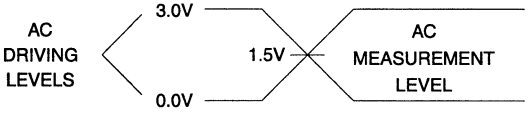
Symbol	Parameter	AT28C256-15		AT28C256-20		AT28C256-25		AT28C256-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250		350	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250		350	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	0	100	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



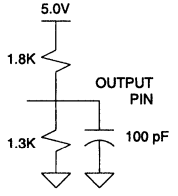
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

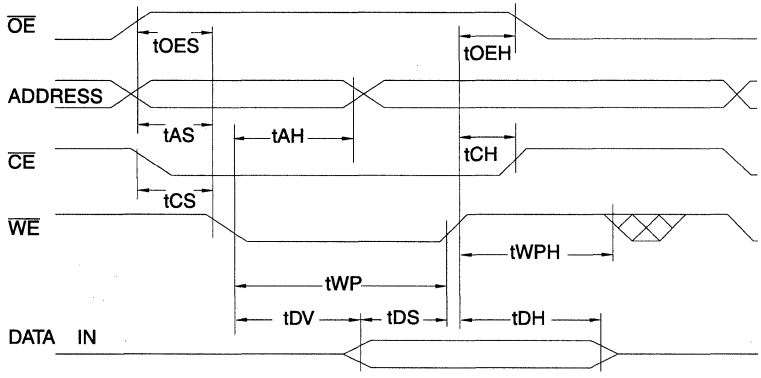
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR (1)		

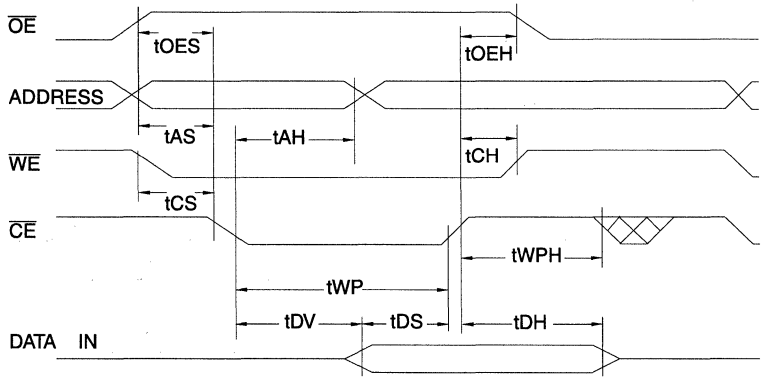
Note: 1. NR = No Restriction

AC Write Waveforms

$\overline{WE}$ Controlled



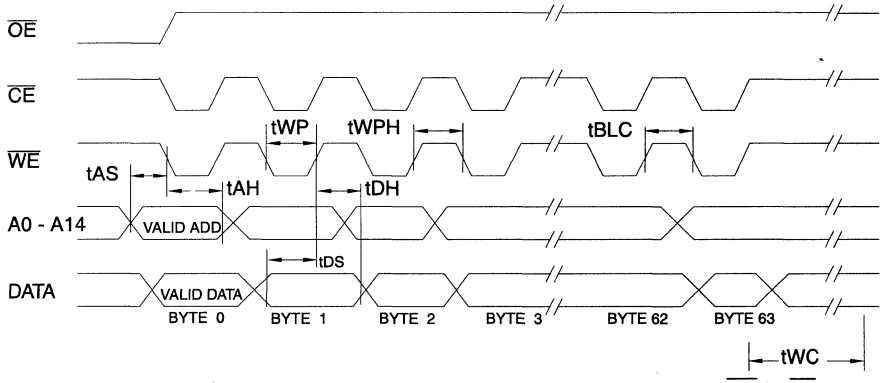
$\overline{CE}$ Controlled



Page Mode Characteristics

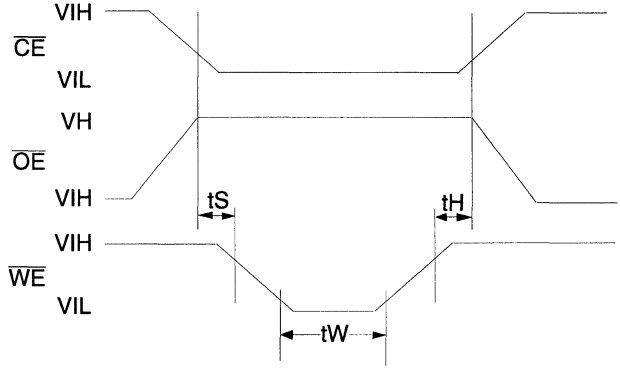
Symbol	Parameter		Min	Max	Units
t_{WC}	Write Cycle Time	AT28C256		10	ms
		AT28C256F		3.0	ms
t_{AS}	Address Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH}	Data Hold Time		0		ns
t_{WP}	Write Pulse Width		100		ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High		50		ns

Page Mode Write Waveforms (1, 2)



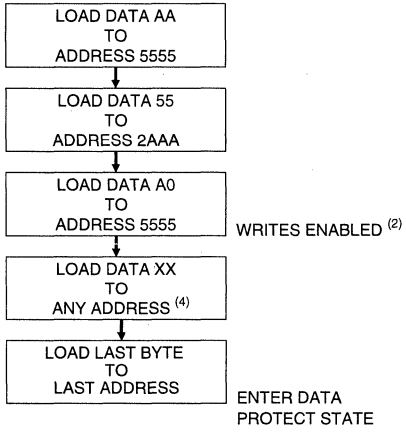
Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

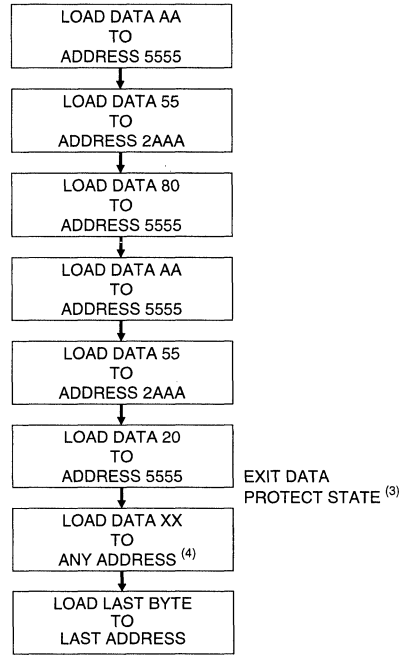


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm [1]

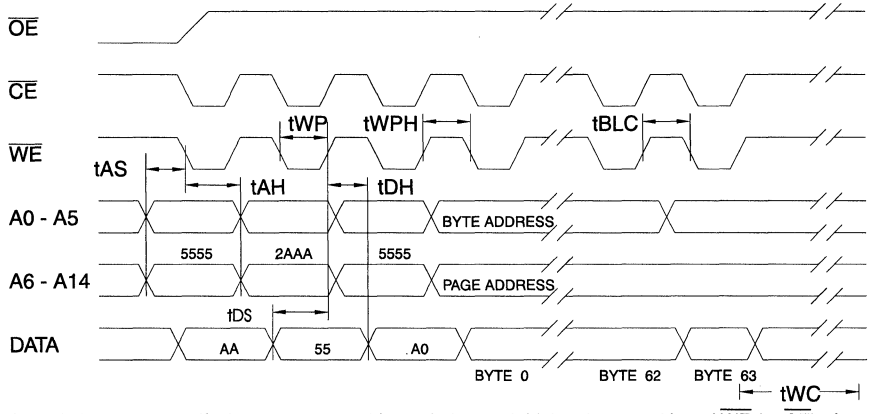


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64-bytes of data are loaded.

Software Protected Write Cycle Waveforms [1, 2]



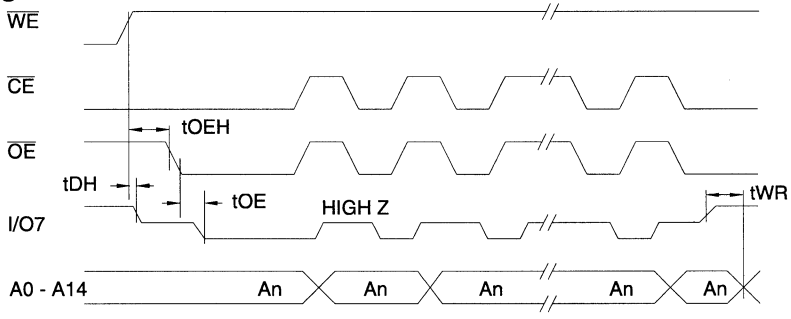
Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

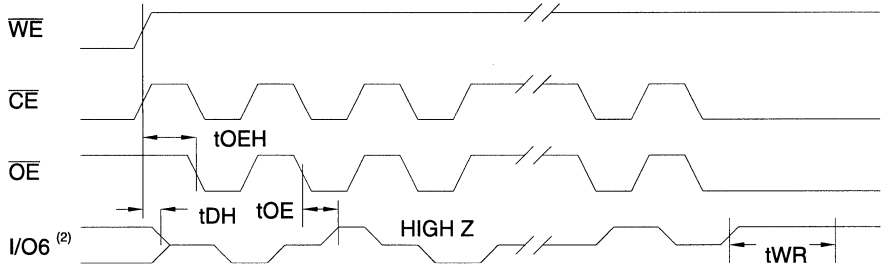


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

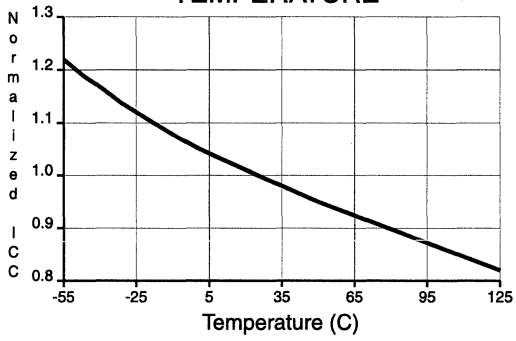
Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms (1, 2, 3)

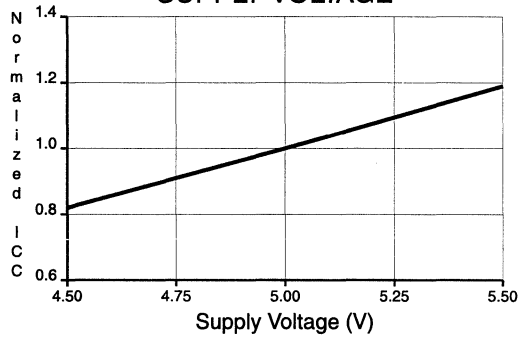


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

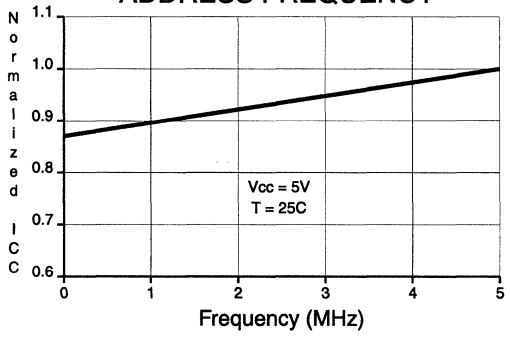
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information [2]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	50	0.2	AT28C256(E,F)-15JC AT28C256(E,F)-15PC AT28C256(E,F)-15SC AT28C256(E,F)-15TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C256(E,F)-15JI AT28C256(E,F)-15PI AT28C256(E,F)-15SI AT28C256(E,F)-15TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
	50	0.3	AT28C256(E,F)-15DM/883 AT28C256(E,F)-15FM/883 AT28C256(E,F)-15LM/883 AT28C256(E,F)-15UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	50	0.2	AT28C256(E,F)-20JC AT28C256(E,F)-20PC AT28C256(E,F)-20SC AT28C256(E,F)-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C256(E,F)-20JI AT28C256(E,F)-20PI AT28C256(E,F)-20SI AT28C256(E,F)-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
	50	0.3	AT28C256(E,F)-20DM/883 AT28C256(E,F)-20FM/883 AT28C256(E,F)-20LM/883 AT28C256(E,F)-20UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	50	0.2	AT28C256(E,F)-25JC AT28C256(E,F)-25PC AT28C256-W	32J 28P6 DIE	Commercial (0°C to 70°C)
			AT28C256(E,F)-25JI AT28C256(E,F)-25PI	32J 28P6	Industrial (-40°C to 85°C)
	50	0.3	AT28C256(E,F)-25DM/883 AT28C256(E,F)-25FM/883 AT28C256(E,F)-25LM/883 AT28C256(E,F)-25UM/883 AT28C256(E,F)-35UM/883	28D6 28F 32L 28U 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	50	0.2	AT28C256-W	DIE	Commercial (0°C to 70°C)

(continued)

Ordering Information (Continued)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150 (3)	50	0.35	5962-88525 16 UX 5962-88525 16 XX 5962-88525 16 YX 5962-88525 16 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 15 UX 5962-88525 15 XX 5962-88525 15 YX 5962-88525 15 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 14 UX 5962-88525 14 XX 5962-88525 14 YX 5962-88525 14 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	50	0.35	5962-88525 08 UX 5962-88525 08 XX 5962-88525 08 YX 5962-88525 08 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 07 UX 5962-88525 07 XX 5962-88525 07 YX 5962-88525 07 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 06 UX 5962-88525 06 XX 5962-88525 06 YX 5962-88525 06 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200 (3)	50	0.35	5962-88525 12 UX 5962-88525 12 XX 5962-88525 12 YX 5962-88525 12 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	50	0.35	5962-88525 04 UX 5962-88525 04 XX 5962-88525 04 YX 5962-88525 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250 (3)	50	0.35	5962-88525 13 UX 5962-88525 13 XX 5962-88525 13 YX 5962-88525 13 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 11 UX 5962-88525 11 XX 5962-88525 11 YX 5962-88525 11 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

(continued)

Ordering Information (Continued)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	50	0.35	5962-88525 05 UX 5962-88525 05 XX 5962-88525 05 YX 5962-88525 05 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 03 UX 5962-88525 03 XX 5962-88525 03 YX 5962-88525 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	50	0.35	5962-88525 10 UX 5962-88525 10 XX 5962-88525 10 YX 5962-88525 10 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	50	0.35	5962-88525 02 UX 5962-88525 02 XX 5962-88525 02 YX 5962-88525 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	50	0.35	5962-88525 09 UX 5962-88525 09 XX 5962-88525 09 YX 5962-88525 09 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	50	0.35	5962-88525 01 UX 5962-88525 01 XX 5962-88525 01 YX 5962-88525 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Notes: 1. Electrical specifications for these speeds are defined by Standard Microcircuit Drawing 5962-88525.
2. See Valid Part Number table below.
3. SMD specifies Software Data Protection feature for device type, although Atmel product supplied to *every* device type in the SMD is 100% tested for this feature.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C256	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	-	W

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

1 Megabit (128K x 8) Paged CMOS E²PROM

Commercial and Industrial

Features

- Fast Read Access Time - 120 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128-Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms Maximum
  - 1 to 128-Byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 200 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

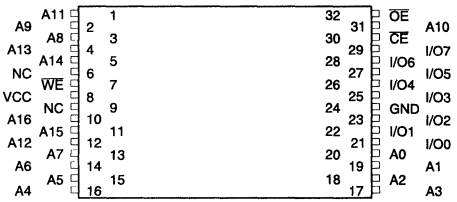
The AT28C010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 120 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 200 µA.

(continued)

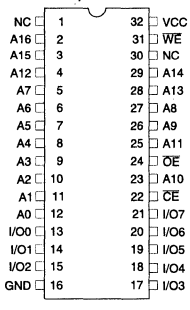
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

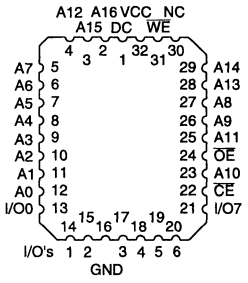
TSOP
Top View



PDIP
Top View



PLCC
Top View



Note: PLCC package pin 1 is a DON'T CONNECT.

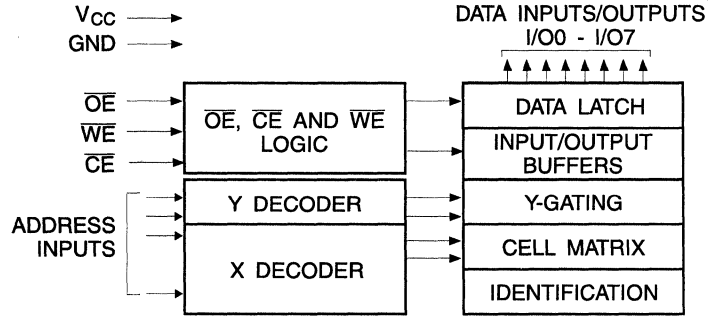
0353C

Description (Continued)

The AT28C010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128-bytes simultaneously. During a write cycle, the address and 1 to 128-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA POLLING of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C010 allows 1 to 128-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 127 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C010 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7 - A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C010 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C010. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C010 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28C010 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C010. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C010 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

(continued)

Device Operation (Continued)

DEVICE IDENTIFICATION: An extra 128-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28C010-12	AT28C010-15	AT28C010-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

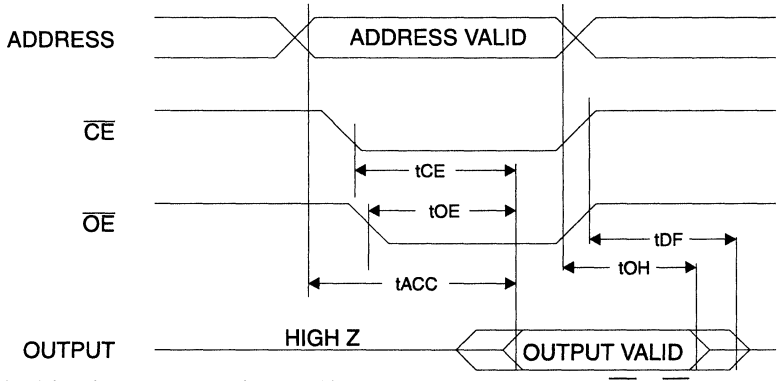
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		40	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

AC Read Characteristics

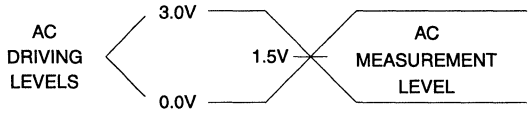
Symbol	Parameter	AT28C010-12 Min	AT28C010-12 Max	AT28C010-15 Min	AT28C010-15 Max	AT28C010-20 Min	AT28C010-20 Max	Units
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	55	0	55	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



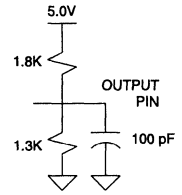
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

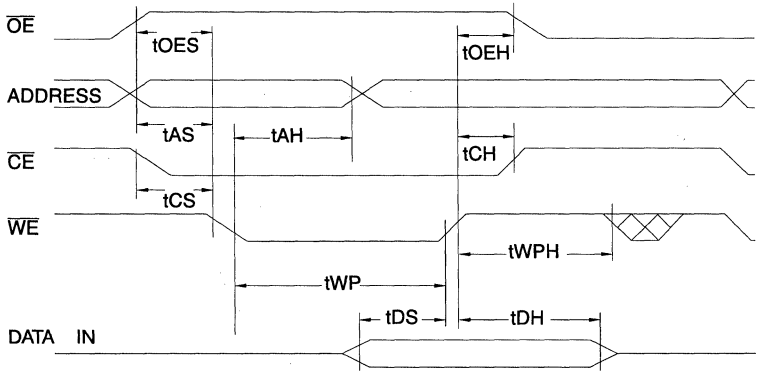
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

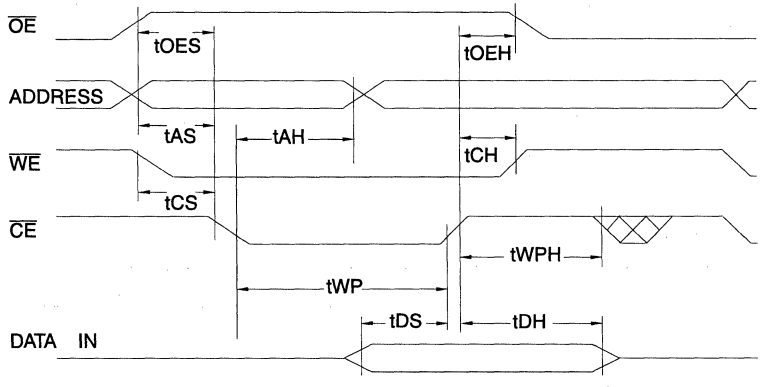
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



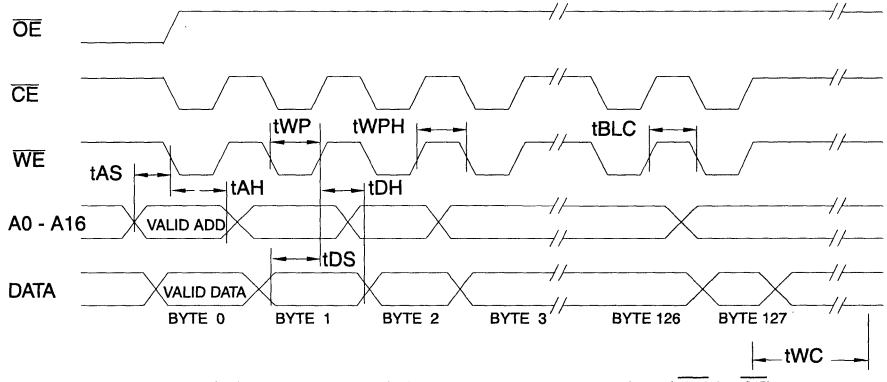
$\overline{CE}$ Controlled



Page Mode Characteristics

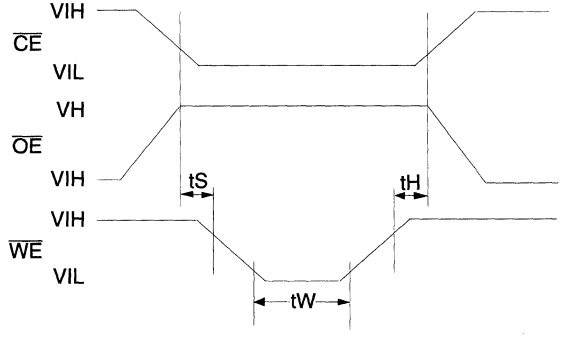
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms (1, 2)



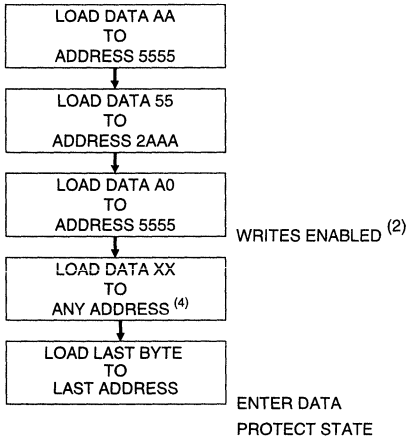
Notes: 1. A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

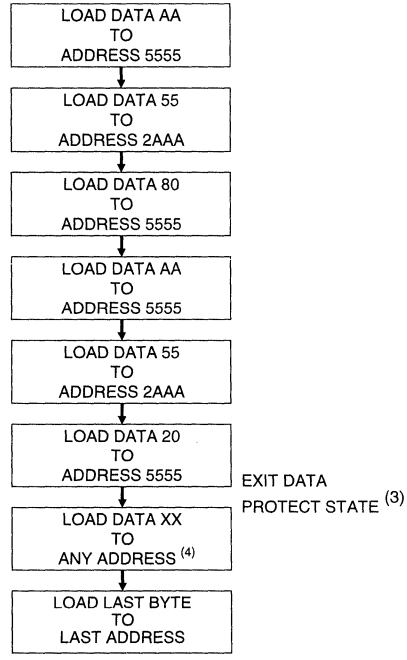


t_S = 5 µsec (min.)
t_W = t_H = 10 msec (min.)
V_H = 12.0V ± 0.5V

Software Data Protection Enable Algorithm [1]

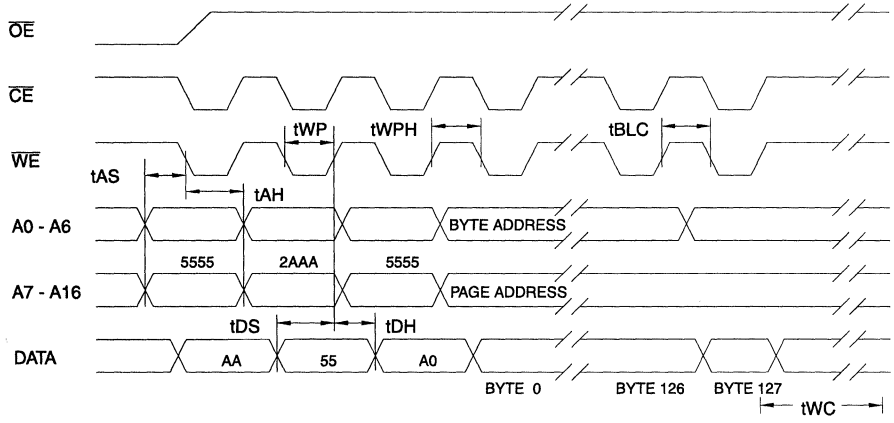


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128-bytes of data are loaded.

Software Protected Program Cycle Waveform [1, 2, 3]



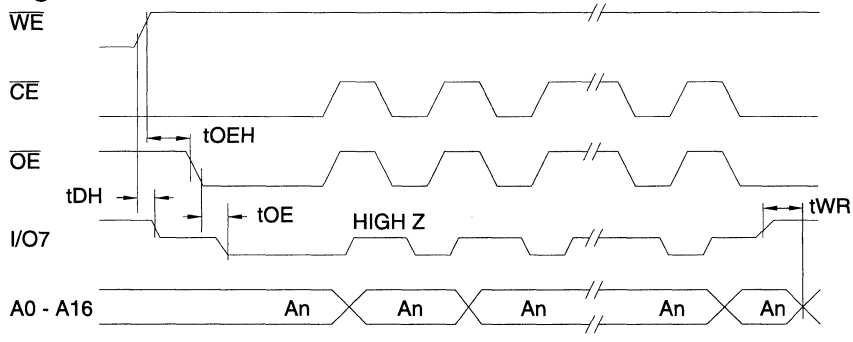
Notes: 1. A0 - A14 must conform to the addressing sequence for the first 3-bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7 - A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

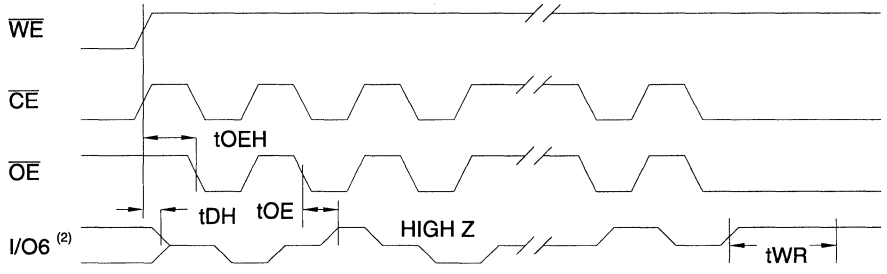


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	40	0.2	AT28C010(E)-12JC AT28C010(E)-12PC AT28C010(E)-12TC	32J 32P6 32T	Commercial (0° to 70°C)
	40	0.2	AT28C010(E)-12JI AT28C010(E)-12PI AT28C010(E)-12TI	32J 32P6 32T	Industrial (-40° to 85°C)
150	40	0.2	AT28C010(E)-15JC AT28C010(E)-15PC AT28C010(E)-15TC	32J 32P6 32T	Commercial (0° to 70°C)
	40	0.2	AT28C010(E)-15JI AT28C010(E)-15PI AT28C010(E)-15TI	32J 32P6 32T	Industrial (-40° to 85°C)
200	40	0.2	AT28C010(E)-20JC AT28C010(E)-20PC AT28C010(E)-20TC	32J 32P6 32T	Commercial (0° to 70°C)
	40	0.2	AT28C010(E)-20JI AT28C010(E)-20PI AT28C010(E)-20TI	32J 32P6 32T	Industrial (-40° to 85°C)
	40	0.2	AT28C010-W	DIE	Commercial (0° to 70°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C010	12	JC, JI, PC, PI, TC, TI
AT28C010E	12	JC, JI, PC, PI, TC, TI
AT28C010	15	JC, JI, PC, PI, TC, TI
AT28C010E	15	JC, JI, PC, PI, TC, TI
AT28C010	20	JC, JI, PC, PI, TC, TI
AT28C010E	20	JC, JI, PC, PI, TC, TI
AT28C010	-	W

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)
W	DIE
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles

1 Megabit (128K x 8) Paged CMOS E²PROM

Military

Features

- Fast Read Access Time - 120 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128-Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms Maximum
  - 1 to 128-Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 300 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout

Description

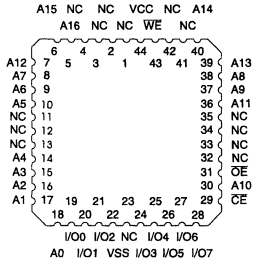
The AT28C010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its one megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers

(continued)

Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

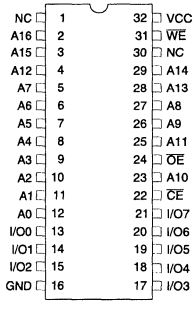
44 LCC
Top View



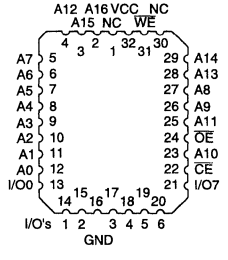
PGA
Top View

4 A6	3 A7	1 A14	27 $\overline{WE}$	26 A13
5 A5	2 A12	28 VCC	24 A9	25 A8
7 A3	6 A4	29 A15	22 $\overline{OE}$	23 A11
9 A1	8 A2	30 A16	20 $\overline{CE}$	21 A10
11 I/O0	10 A0	14 GND	16 I/O4	19 I/O7
12 I/O1	13 I/O2	15 I/O3	17 I/O5	18 I/O6

CERDIP, FLATPACK
Top View



32 LCC
Top View



0353C

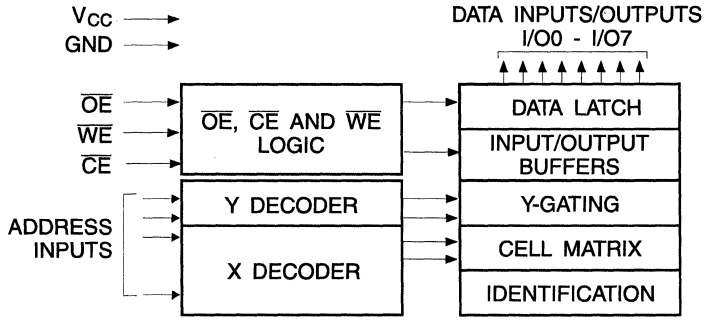
Description (Continued)

access times to 120 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 µA.

The AT28C010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128-bytes simultaneously. During a write cycle, the address and 1 to 128-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA POLLING of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C010 allows 1 to 128-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 127 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C010 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7 - A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C010 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C010. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C010 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28C010 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C010. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C010 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

(continued)

Device Operation (Continued)

DEVICE IDENTIFICATION: An extra 128-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

	AT28C010-12	AT28C010-15	AT28C010-20	AT28C010-25
Operating Temperature (Case) Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

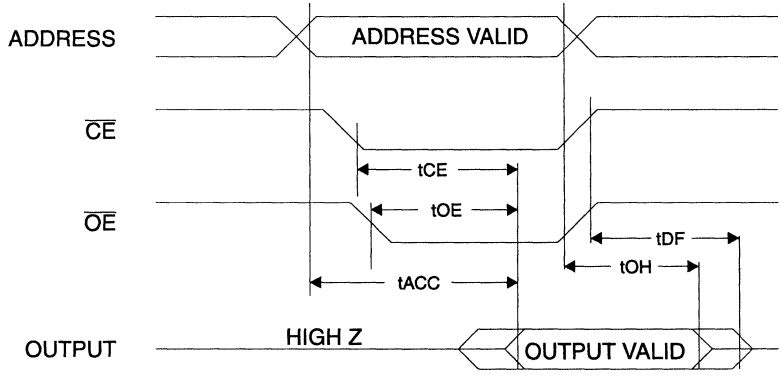
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

AC Read Characteristics

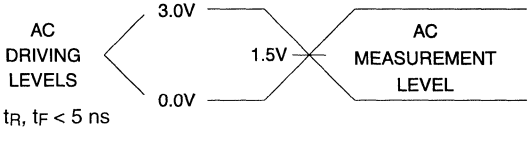
Symbol	Parameter	AT28C010-12		AT28C010-15		AT28C010-20		AT28C010-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	55	0	55	0	55	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)

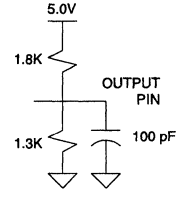


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

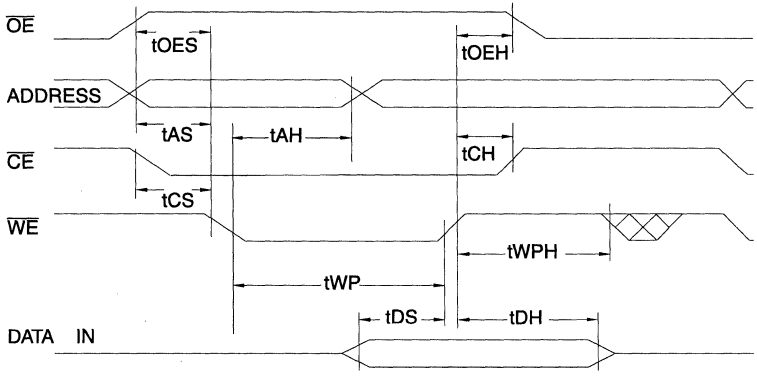
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

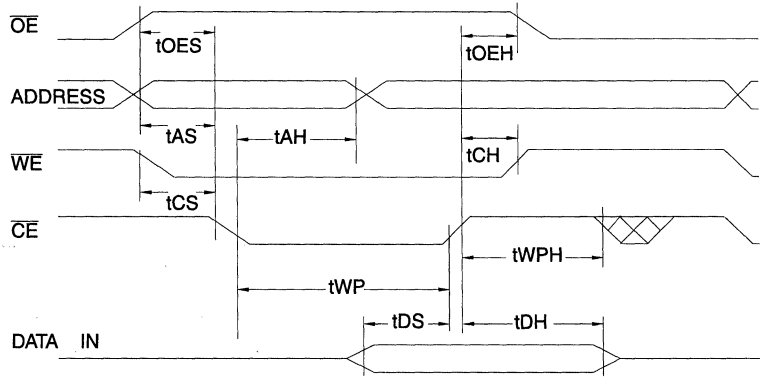
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



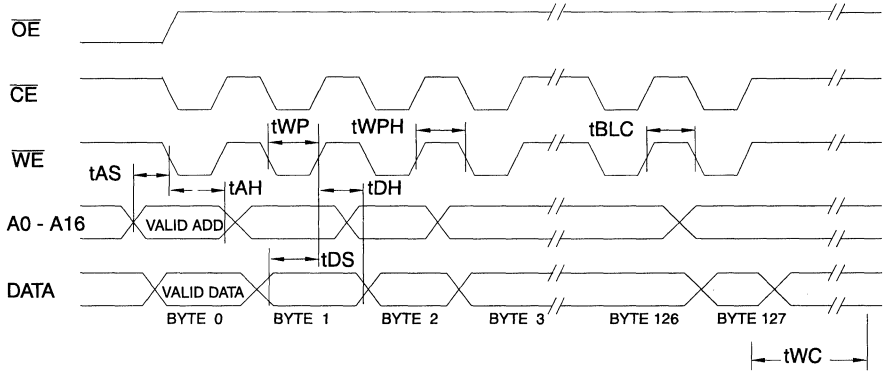
$\overline{CE}$ Controlled



Page Mode Characteristics

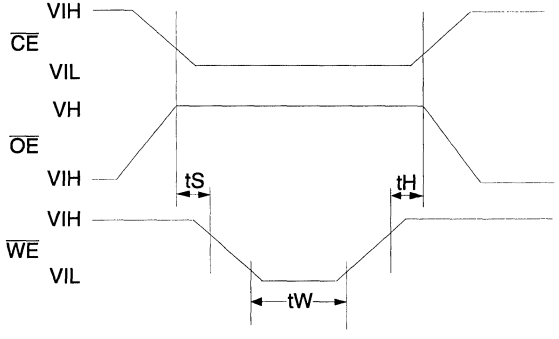
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms (1, 2)



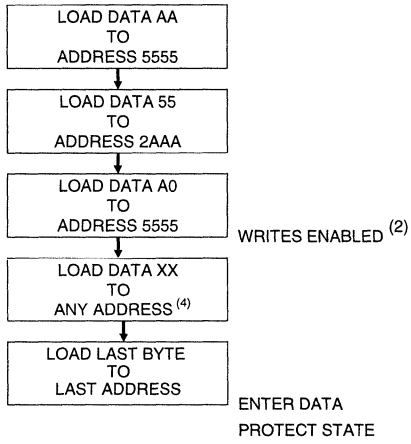
Notes: 1. A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

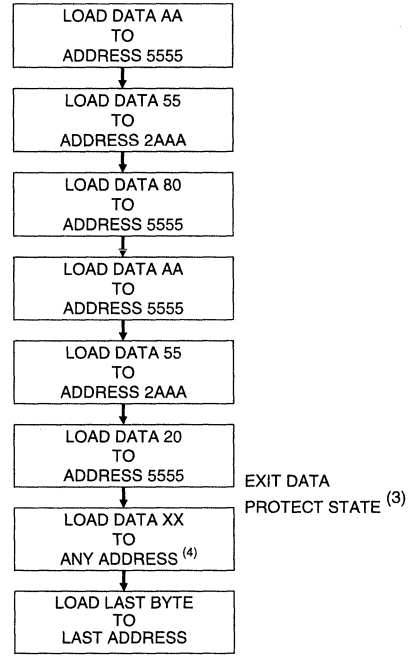


t_S = 5 µsec (min.)
t_W = t_H = 10 msec (min.)
V_H = 12.0V ± 0.5V

Software Data Protection Enable Algorithm [1]

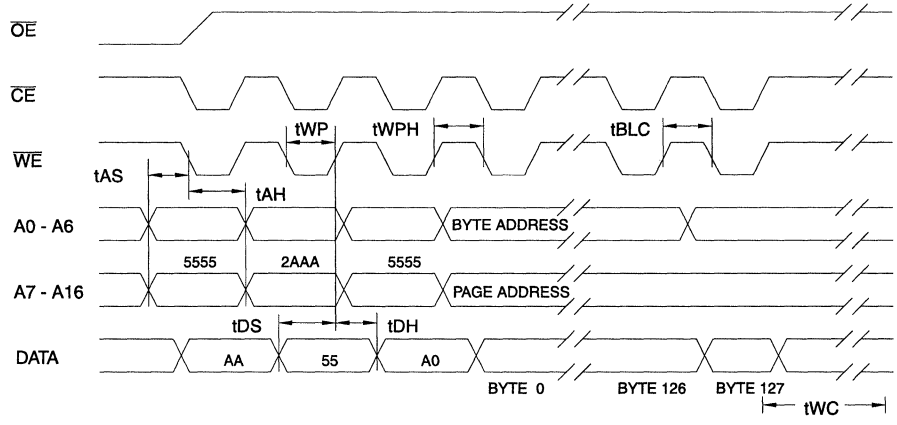


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128-bytes of data are loaded.

Software Protected Program Cycle Waveform [1, 2, 3]



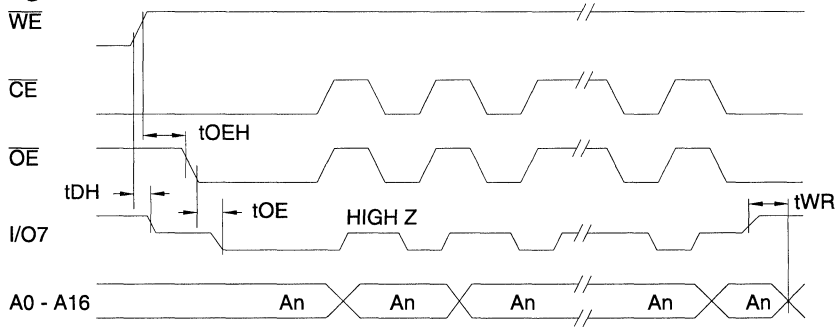
Notes: 1. A0 - A14 must conform to the addressing sequence for the first 3-bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7 - A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Data Polling Waveforms

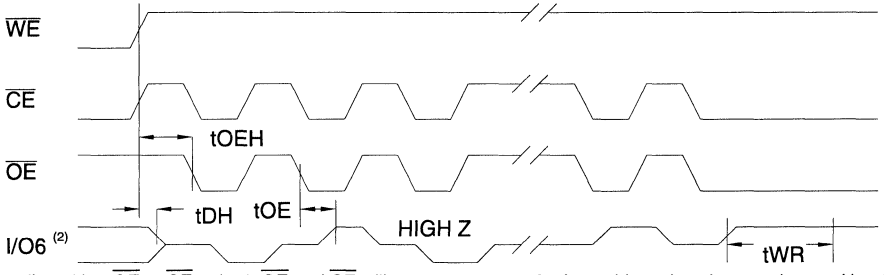


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms (1, 2, 3)



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	0.3	AT28C010(E)-12DM/883 AT28C010(E)-12EM/883 AT28C010-12FM/883 AT28C010(E)-12LM/883 AT28C010(E)-12UM/883	32D6 32L 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	AT28C010(E)-15DM/883 AT28C010(E)-15EM/883 AT28C010-15FM/883 AT28C010(E)-15LM/883 AT28C010(E)-15UM/883	32D6 32L 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT28C010(E)-20DM/883 AT28C010(E)-20EM/883 AT28C010-20FM/883 AT28C010(E)-20LM/883 AT28C010(E)-20UM/883	32D6 32L 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT28C010(E)-25DM/883 AT28C010(E)-25EM/883 AT28C010-25FM/883 AT28C010(E)-25LM/883 AT28C010(E)-25UM/883	32D6 32L 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-38267 07 MXX 5962-38267 07 MZX 5962-38267 07 MYX 5962-38267 07 MTX	32D6 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	5962-38267 05 MXX 5962-38267 05 MUX 5962-38267 05 MZX 5962-38267 05 MYX 5962-38267 05 MTX	32D6 32L 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	5962-38267 03 MXX 5962-38267 03 MUX 5962-38267 03 MZX 5962-38267 03 MYX 5962-38267 03 MTX	32D6 32L 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	5962-38267 01 MXX 5962-38267 01 MUX 5962-38267 01 MZX 5962-38267 01 MYX 5962-38267 01 MTX	32D6 32L 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	80	0.3	AT28C010-W	DIE	

Note: 1. See Valid Part Number table on next page.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C010	12	DM/883, EM/883, FM/883, LM/883, UM/883
AT28C010E	12	DM/883, EM/883, LM/883, UM/883
AT28C010	15	DM/883, EM/883, FM/883, LM/883, UM/883
AT28C010E	15	DM/883, EM/883, LM/883, UM/883
AT28C010	20	DM/883, EM/883, FM/883, LM/883, UM/883
AT28C010E	20	DM/883, EM/883, LM/883, UM/883
AT28C010	25	DM/883, EM/883, FM/883, LM/883, UM/883
AT28C010E	25	DM/883, EM/883, LM/883, UM/883

Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline (CERDIP)
32F	32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
30U	30 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles

Features

- Fast Read Access Time - 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 256-Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms Maximum
  - 1 to 256-Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 300 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10,000 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial and Industrial Temperature Ranges

Description

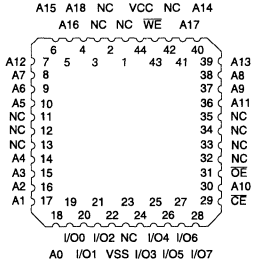
The AT28C040 is a high-performance electrically erasable and programmable read only memory (E^2PROM). Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 µA.

(continued)

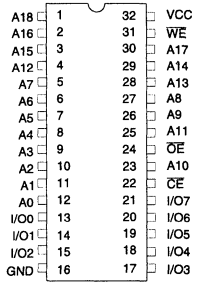
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

LCC
Top View



SIDE BRAZE,
FLATPACK
Top View



2

4 Megabit (512K x 8) Paged CMOS E^2PROM

Preliminary

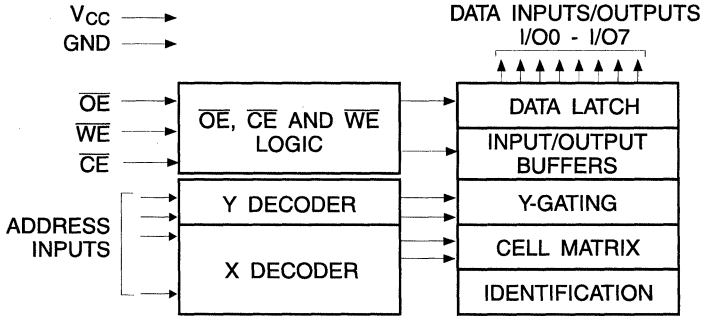
0542A

Description (Continued)

The AT28C040 is accessed like a static RAM for the read or write cycle without the need for external components. The device contains a 256-byte page register to allow writing of up to 256-bytes simultaneously. During a write cycle, the address and 1 to 256-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28C040 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 256-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C040 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C040 allows 1 to 256-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 255 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C040 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A8 - A18 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A8 - A18 must be the same.

The A0 to A7 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C040 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28C040 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C040 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C040. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C040 is shipped from Atmel with SDP disabled.

SDP is enabled when the host system issues a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC}, the entire AT28C040 will be protected against inadvertent write operations. It should be noted that once protected, the host can still perform a byte or page write to the AT28C040. To do so, the same 3-byte command sequence used to enable SDP must precede the data to be written.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP will protect the AT28C040 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device, and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

(continued)

Device Operation (Continued)

DEVICE IDENTIFICATION: An extra 256-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FF80H to 7FFFFH, the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software erase code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28C040-15	AT28C040-20	AT28C040-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

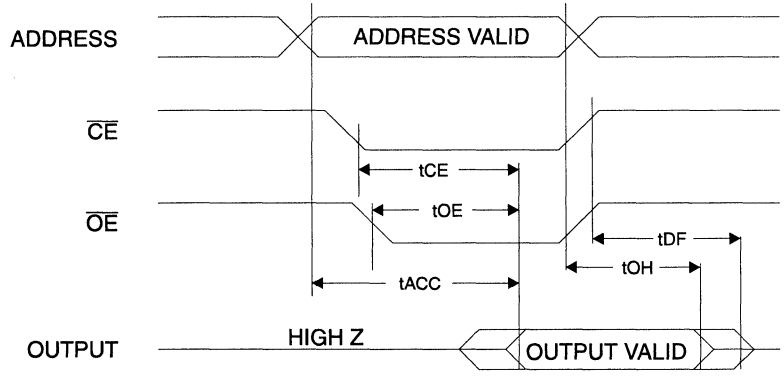
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

AC Read Characteristics

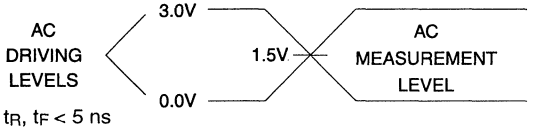
Symbol	Parameter	AT28C040-15 Min	AT28C040-15 Max	AT28C040-20 Min	AT28C040-20 Max	AT28C040-25 Min	AT28C040-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	55	0	55	0	55	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)

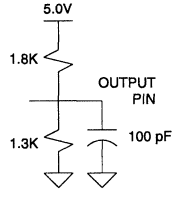


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

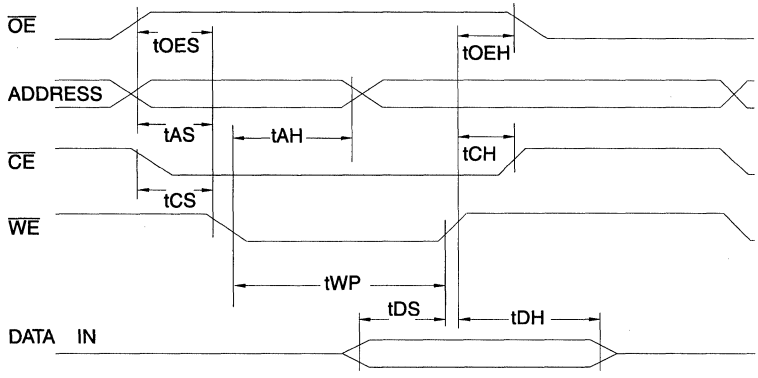
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

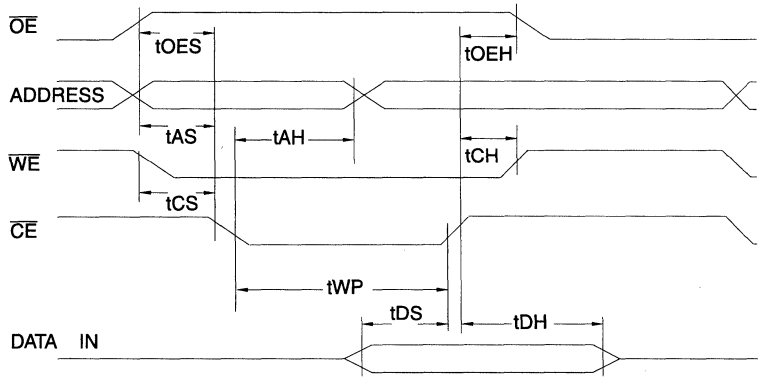
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



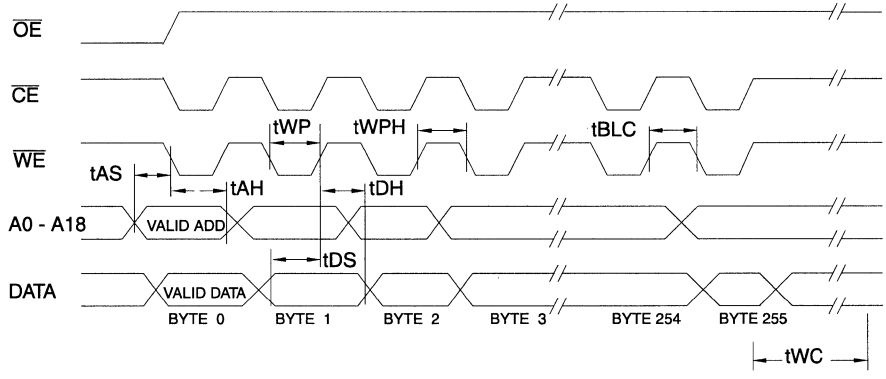
$\overline{CE}$ Controlled



Page Mode Characteristics

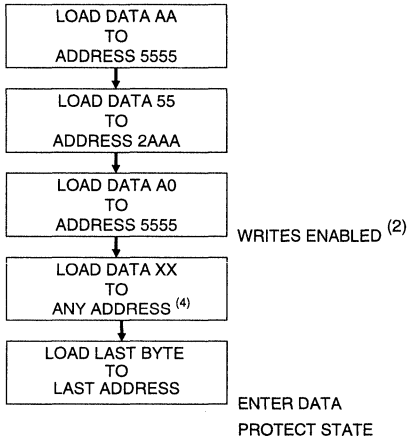
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms (1, 2)

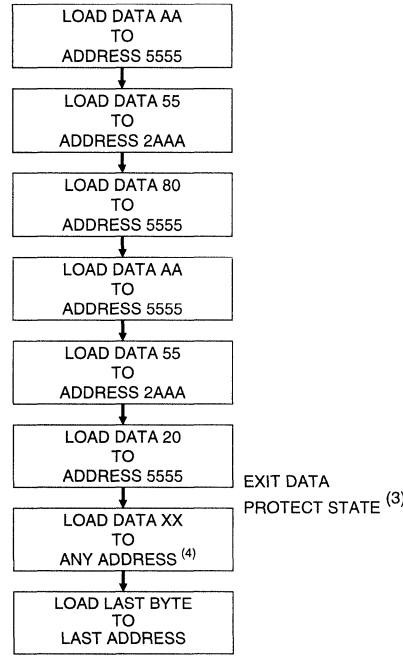


Notes: 1. A8 through A18 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm [1]

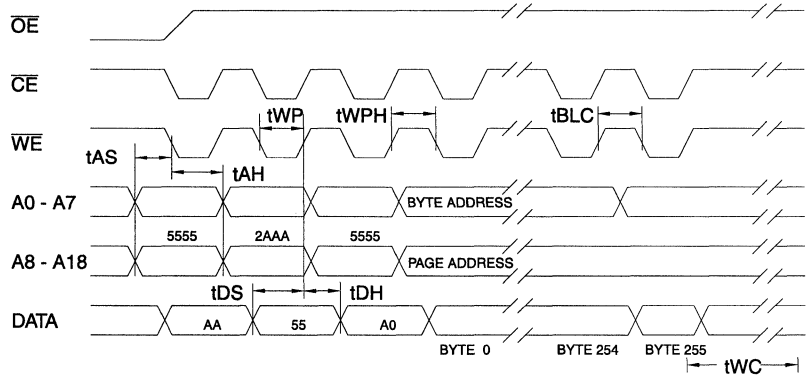


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 256-bytes of data are loaded.

Software Protected Program Cycle Waveform [1, 2, 3]



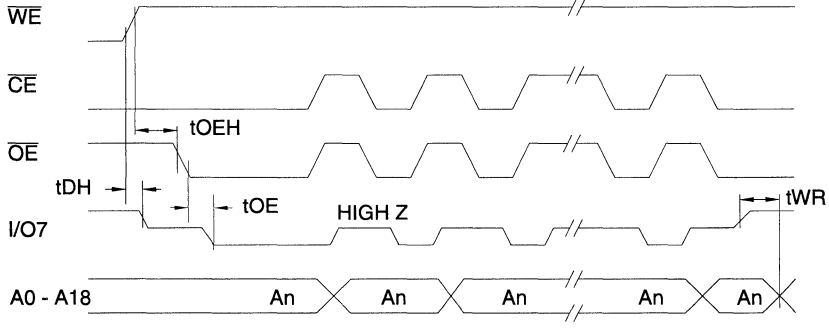
Notes: 1. A0 - A14 must conform to the addressing sequence for the first 3-bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A8 - A18) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Data Polling Waveforms

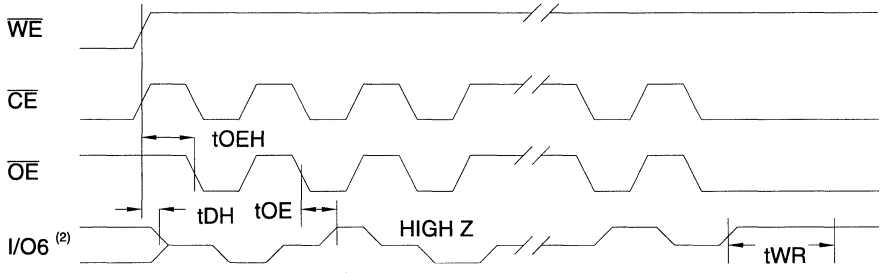


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms (1, 2, 3)



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.3	AT28C040-15BC AT28C040-15FC AT28C040-15LC	32B 32F 44L	Commercial (0° to 70°C)
	80	0.3	AT28C040-15BI AT28C040-15FI AT28C040-15LI	32B 32F 44L	Industrial (-40° to 85°C)
	80	0.3	AT28C040-15BM AT28C040-15FM AT28C040-15LM	32B 32F 44L	Military (-55°C to 125°C)
	80	0.3	AT28C040-15BM/883 AT28C040-15FM/883 AT28C040-15LM/883	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT28C040-20BC AT28C040-20FC AT28C040-20LC	32B 32F 44L	Commercial (0° to 70°C)
	80	0.3	AT28C040-20BI AT28C040-20FI AT28C040-20LI	32B 32F 44L	Industrial (-40° to 85°C)
	80	0.3	AT28C040-20BM AT28C040-20FM AT28C040-20LM	32B 32F 44L	Military (-55°C to 125°C)
	80	0.3	AT28C040-20BM/883 AT28C040-20FM/883 AT28C040-20LM/883	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT28C040-25BC AT28C040-25FC AT28C040-25LC	32B 32F 44L	Commercial (0° to 70°C)
	80	0.3	AT28C040-25BI AT28C040-25FI AT28C040-25LI	32B 32F 44L	Industrial (-40° to 85°C)
	80	0.3	AT28C040-25BM AT28C040-25FM AT28C040-25LM	32B 32F 44L	Military (-55°C to 125°C)
	80	0.3	AT28C040-25BM/883 AT28C040-25FM/883 AT28C040-25LM/883	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Note: 1. See Valid Part Numbers on next page.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C040	15	BC, BI, FC, FI, LC, LI, BM/883, FM/883, LM/883
AT28C040	20	BC, BI, FC, FI, LC, LI, BM/883, FM/883, LM/883
AT28C040	25	BC, BI, FC, FI, LC, LI, BM/883, FM/883, LM/883

Package Type	
32B	32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
32F	32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms

64K (8K x 8) High Speed CMOS E^2PROM with Page Write and Software Data Protection

Features

- Fast Read Access Time - 55 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64-Bytes
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 100 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

The AT28HC64B is a high-performance electrically erasable and programmable read only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 µA.

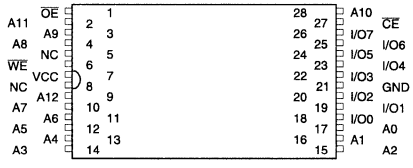
The AT28HC64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow

(continued)

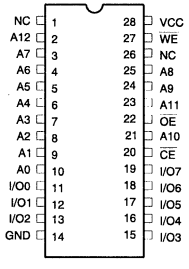
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

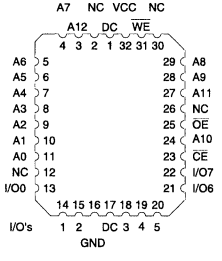
TSOP
Top View



PDIP, SOIC
Top View



PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

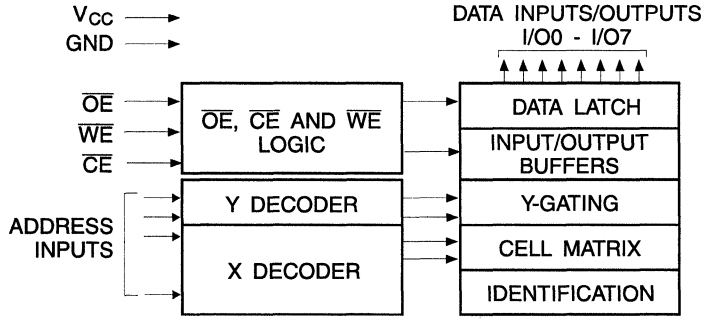
0274D

Description (Continued)

writing of up to 64-bytes simultaneously. During a write cycle, the addresses and 1 to 64-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA Polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28HC64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64-bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28HC64B is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28HC64B allows 1 to 64-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28HC64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28HC64B features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28HC64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28HC64B in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical), the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software-controlled data protection feature has been implemented on the AT28HC64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28HC64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (refer to the *Software Data Protection Algorithm* diagram in this data sheet). After writing the 3-byte command sequence and waiting t_{WC}, the entire AT28HC64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28HC64B. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the AT28HC64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device, however. For the duration of t_{WC}, read operations will effectively be polling operations.

(continued)

Device Operation (Continued)

DEVICE IDENTIFICATION: An extra 64-bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28HC64B-55	AT28HC64B-70	AT28HC64B-90	AT28HC64B-120
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to the *AC Write Waveforms* diagrams in this data sheet.
3. V_H = 12.0V ± 0.5V.

DC Characteristics

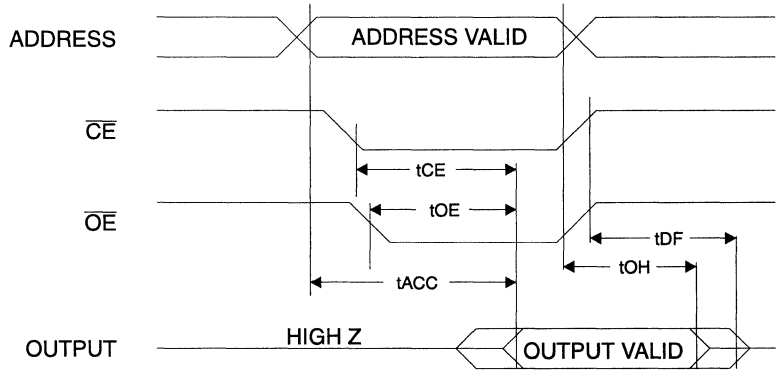
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V Com., Ind.		100 (1)	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		2 (1)	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		40	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.40	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Note: 1. I_{SB1} and I_{SB2} for the 55 ns part is 40 mA maximum.

AC Read Characteristics

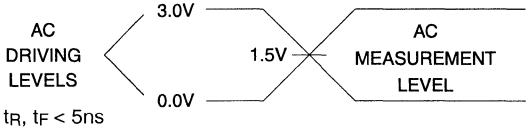
Symbol	Parameter	AT28HC64B-55		AT28HC64B-70		AT28HC64B-90		AT28HC64B-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		55		70		90		120	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		55		70		90		120	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	30	0	35	0	40	0	50	ns
t_{DF} (3, 4)	$\overline{OE}$ to Output Float	0	30	0	35	0	40	0	50	ns
t_{OH}	Output Hold	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)

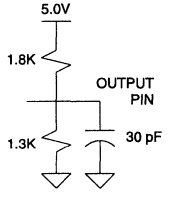


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

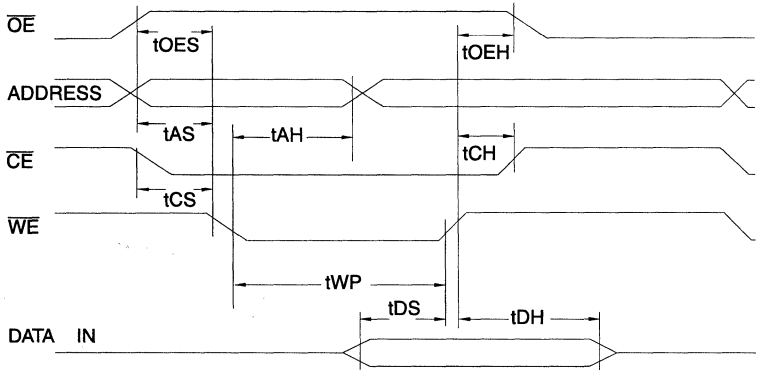
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

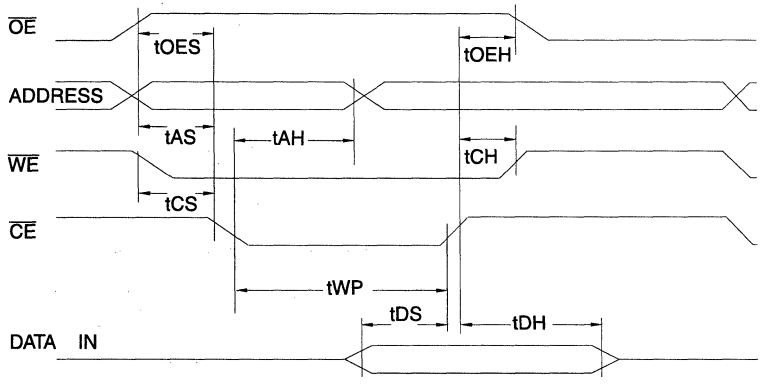
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



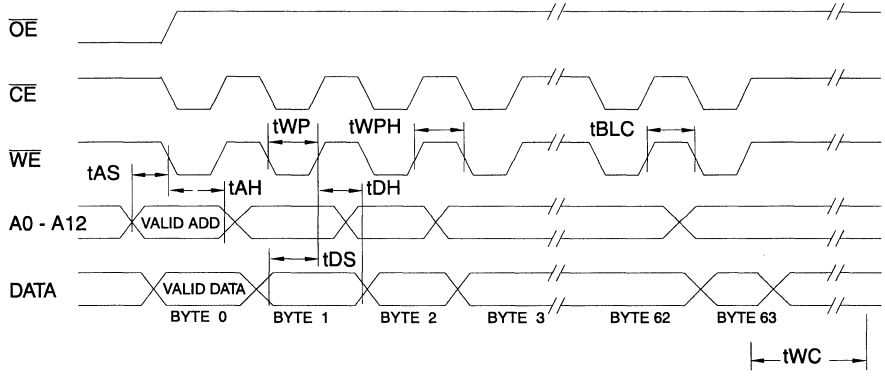
$\overline{CE}$ Controlled



Page Mode Characteristics

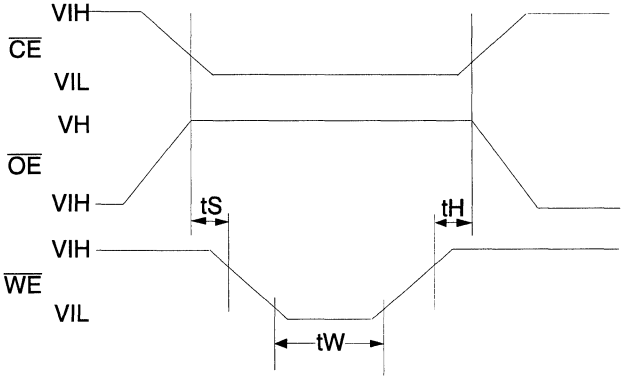
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms (1, 2)



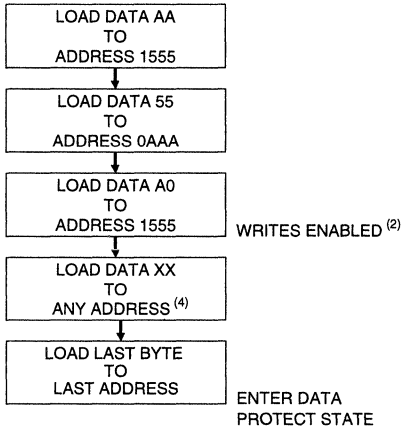
Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

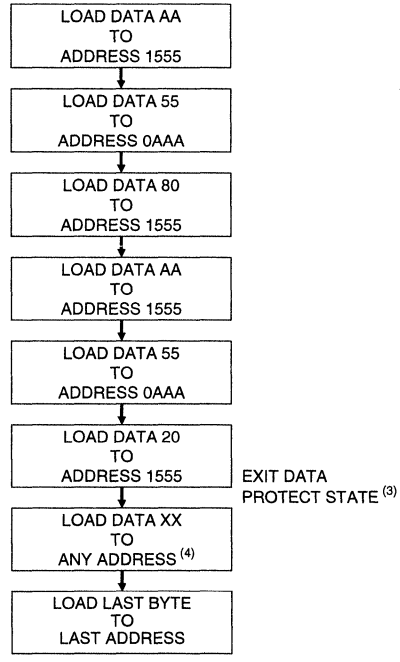


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm [1]

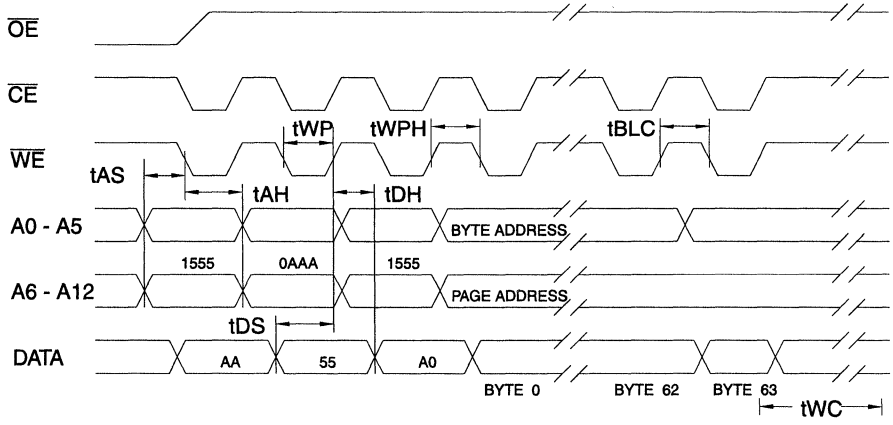


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A12 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64-bytes of data are loaded.

Software Protected Write Cycle Waveforms [1, 2]



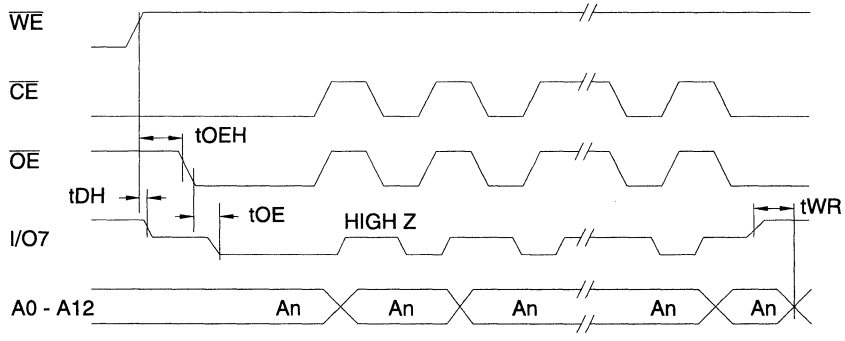
Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

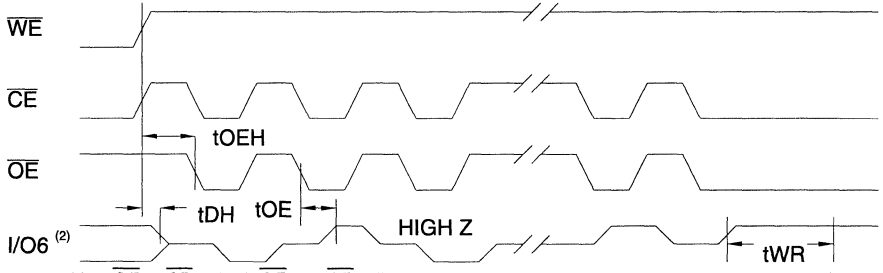


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

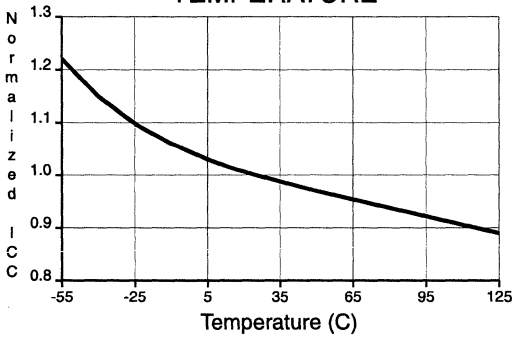
Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms (1, 2, 3)

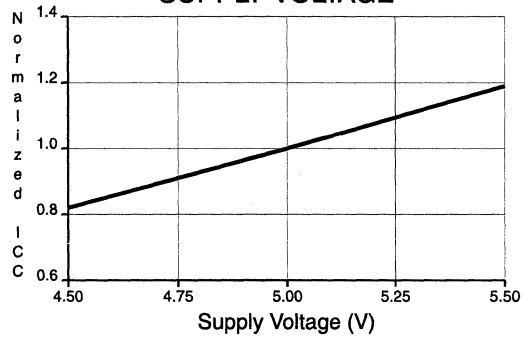


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used, but the address should not vary.

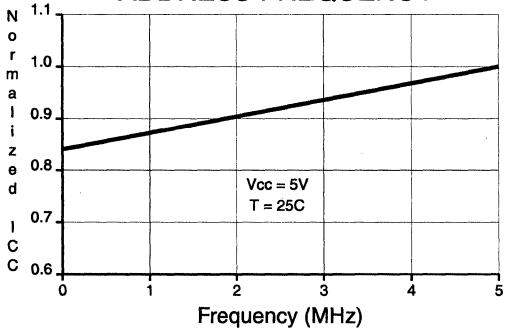
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	40	0.1	AT28HC64B-55JC AT28HC64B-55PC AT28HC64B-55SC	32J 28P6 28S	Commercial (0°C to 70°C)
70	40	0.1	AT28HC64B-70JC AT28HC64B-70PC AT28HC64B-70SC AT28HC64B-70TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	40	0.1	AT28HC64B-70JI AT28HC64B-70PI AT28HC64B-70SI AT28HC64B-70TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
90	40	0.1	AT28HC64B-90JC AT28HC64B-90PC AT28HC64B-90SC AT28HC64B-90TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	40	0.1	AT28HC64B-90JI AT28HC64B-90PI AT28HC64B-90SI AT28HC64B-90TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
120	40	0.1	AT28HC64B-12JC AT28HC64B-12PC AT28HC64B-12SC AT28HC64B-12TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	40	0.1	AT28HC64B-12JI AT28HC64B-12PI AT28HC64B-12SI AT28HC64B-12TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28HC64B	55	PC, SC
AT28HC64B	70	JI, PC, PI, SC, SI, TC, TI
AT28HC64B	90	JI, PC, PI, SC, SI, TC, TI
AT28HC64B	12	JI, PC, PI, SC, SI, TC, TI

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

256 (32K x 8) High Speed CMOS E^2PROM

Features

- Fast Read Access Time - 70 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64-Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 3 ms or 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 3 mA Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

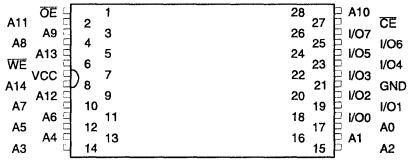
The AT28HC256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the AT28HC256 offers access times to 70 ns with power dissipation of just 440 mW. When the AT28HC256 is deselected, the standby current is less than 5 mA.

(continued)

Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

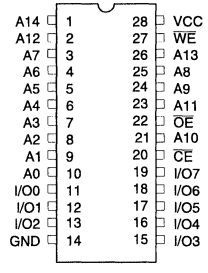
TSOP
Top View



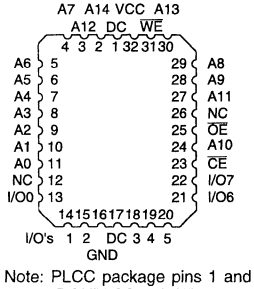
PGA
Top View

4 A6	3 A7	1 A14	27 $\overline{WE}$	26 A13
5 A5	2 A12	28 VCC	24 A9	25 A8
7 A3	6 A4		22 $\overline{OE}$	23 A11
9 A1	8 A2		20 $\overline{CE}$	21 A10
11 I/O0	10 A0	14 GND	16 I/O4	19 I/O7
12 I/O1	13 I/O2	15 I/O3	17 I/O5	18 I/O6

CERDIP, PDIP, FLATPACK
Top View



LCC, PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

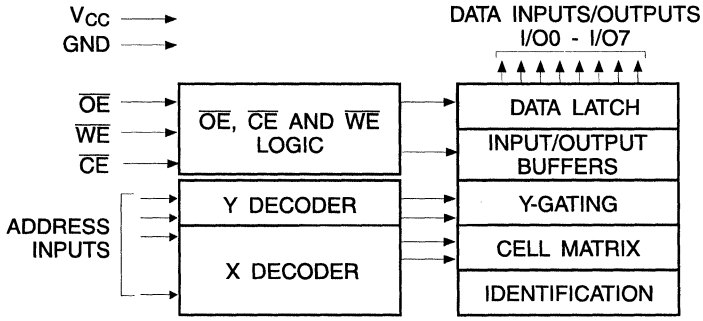
0007F

Description (Continued)

The AT28HC256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64-bytes simultaneously. During a write cycle, the address and 1 to 64-bytes of data are internally latched, freeing the addresses and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28HC256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28HC256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28HC256 allows 1 to 64-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. That is, for each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28HC256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28HC256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Testing the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes to any 5-volt-only nonvolatile memory may occur during transition of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28HC256 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28HC256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28HC256 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28HC256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28HC256. This is done by preceding the data to be written by the same 3-byte command sequence.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28HC256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. It should also be noted that the data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

(continued)

Device Operation (Continued)

DEVICE IDENTIFICATION: An extra 64-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28HC256-70	AT28HC256-90	AT28HC256-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.

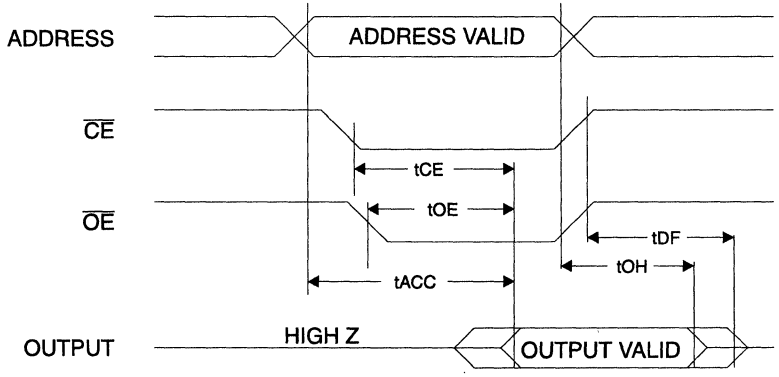
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V	AT28HC256-90, -12		3	mA
			AT28HC256-70		60	mA
I_{SB2}	V_{CC} Standby Current CMOS	$\overline{CE}$ = -3.0V to V_{CC} + 1V	AT28HC256-90, -12		300	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 6.0 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4		V

AC Read Characteristics

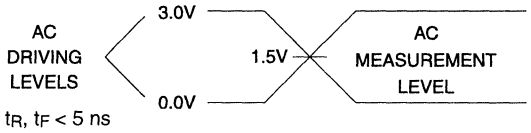
Symbol	Parameter	AT28HC256-70 Min	AT28HC256-70 Max	AT28C256-90 Min	AT28C256-90 Max	AT28HC256-12 Min	AT28HC256-12 Max	Units
t_{ACC}	Address to Output Delay		70		90		120	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		70		90		120	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	35	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



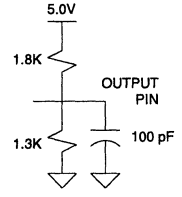
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

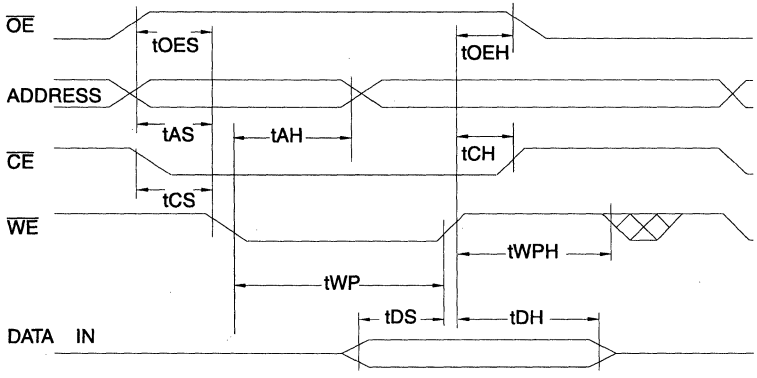
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR (1)		

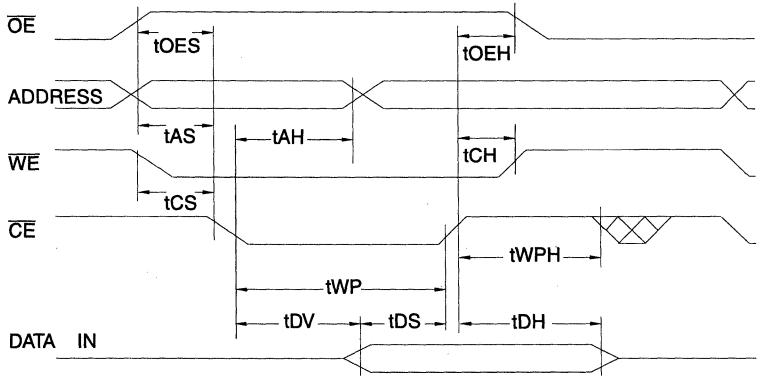
Note: 1. NR = No Restriction

AC Write Waveforms

$\overline{WE}$ Controlled



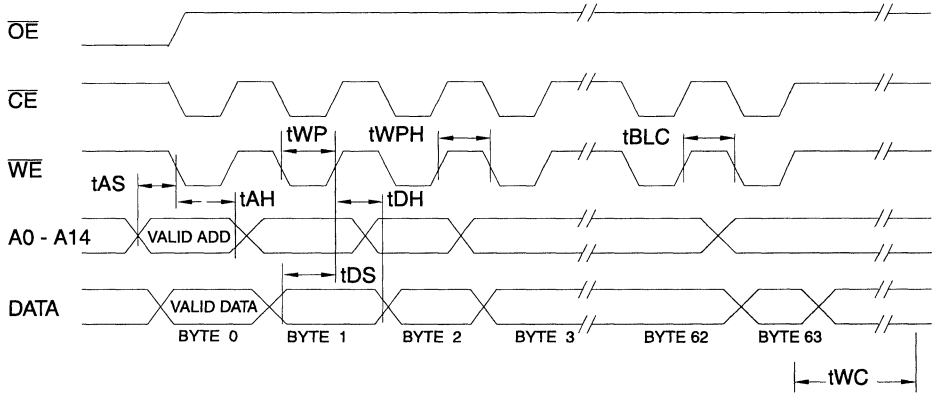
$\overline{CE}$ Controlled



Page Mode Write Characteristics

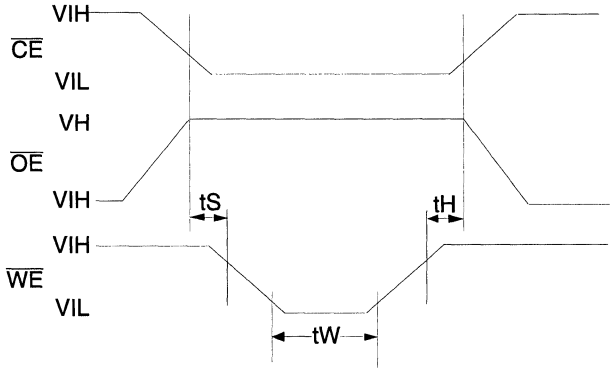
Symbol	Parameter		Min	Typ	Max	Units
t_{WC}	Write Cycle Time	AT28HC256		5	10	ms
		AT28HC256F		2	3.0	ms
t_{AS}	Address Set-up Time		0			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Set-up Time		50			ns
t_{DH}	Data Hold Time		0			ns
t_{WP}	Write Pulse Width		100			ns
t_{BLC}	Byte Load Cycle Time				150	µs
t_{WPH}	Write Pulse Width High		50			ns

Page Mode Write Waveforms (1, 2)



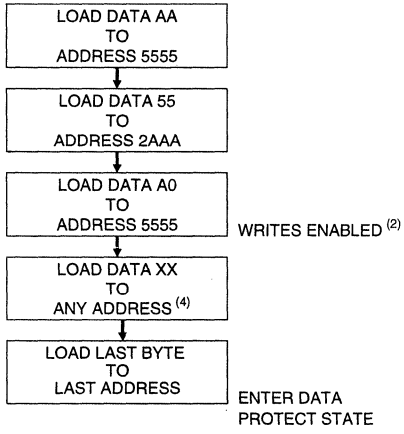
Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

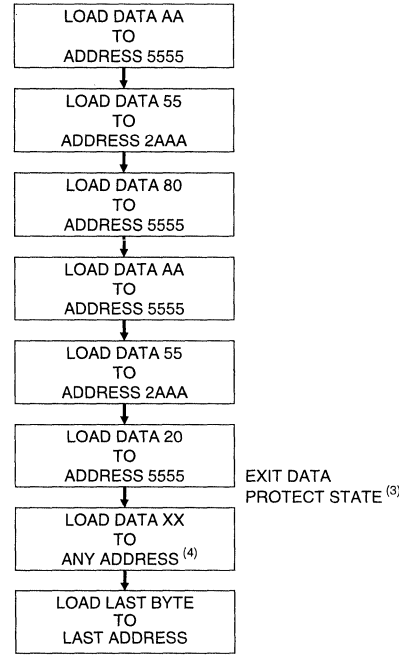


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm [1]

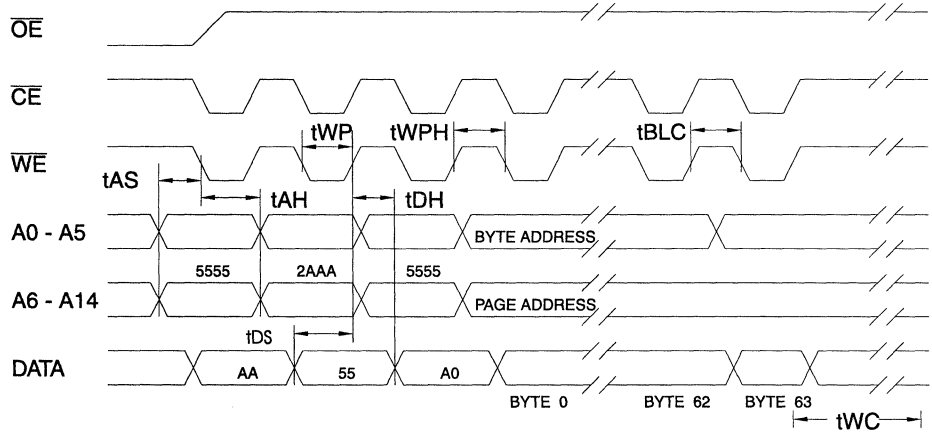


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64-bytes of data are loaded.

Software Protected Write Cycle Waveforms [1, 2]



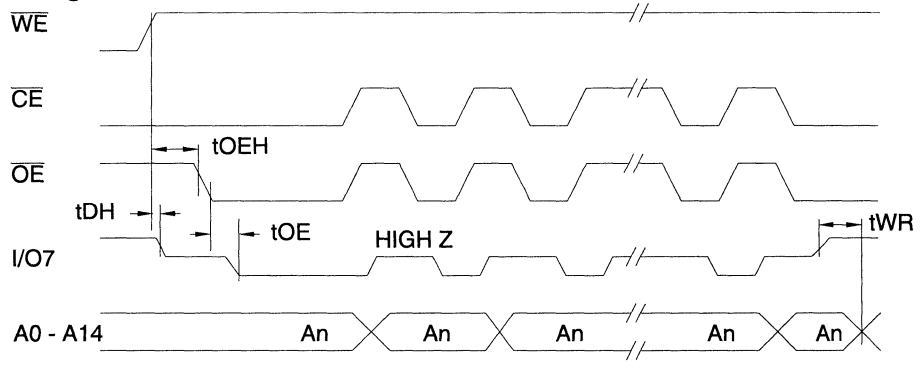
Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ ($\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Data Polling Waveforms

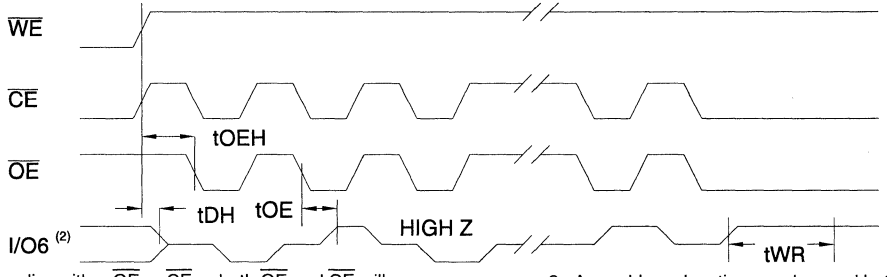


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

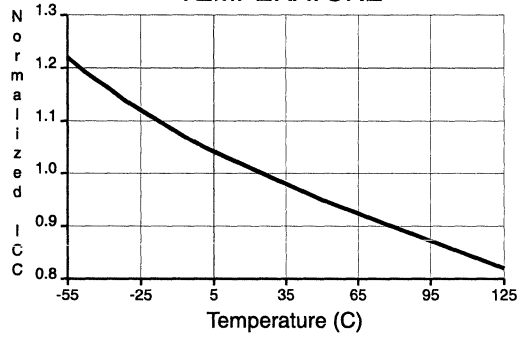
Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms

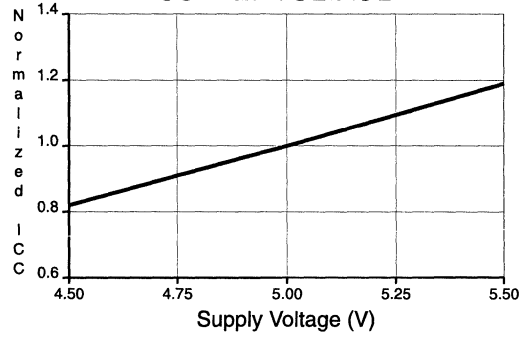


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary
3. Any address location may be used but the address should not vary.

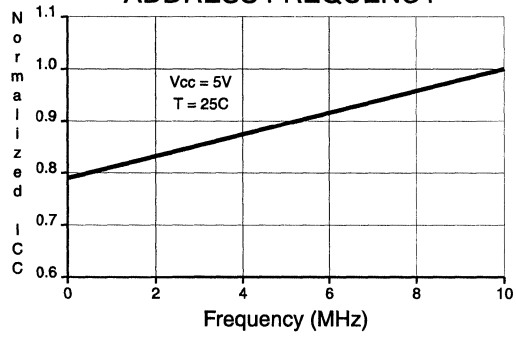
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	60	AT28HC256(E,F)-70JC AT28HC256(E,F)-70PC	32J 28P6	Commercial (0°C to 70°C)
	80	0.3	AT28HC256(E,F)-70JI AT28HC256(E,F)-70PI	32J 28P6	Industrial (-40°C to 85°C)
90	80	0.3	AT28HC256(E,F)-90JC AT28HC256(E,F)-90PC	32J 28P6	Commercial (0°C to 70°C)
	80	0.3	AT28HC256(E,F)-90JI AT28HC256(E,F)-90PI	32J 28P6	Industrial (-40°C to 85°C)
	80	0.3	AT28HC256(E,F)-90DM/883 AT28HC256(E,F)-90FM/883 AT28HC256(E,F)-90LM/883 AT28HC256(E,F)-90UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	AT28HC256(E,F)-12JC AT28HC256(E,F)-12PC AT28HC256(E,F)-12SC AT28HC256(E,F)-12TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	80	0.3	AT28HC256(E,F)-12JI AT28HC256(E,F)-12PI AT28HC256(E,F)-12SI AT28HC256(E,F)-12TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
	80	0.3	AT28HC256(E,F)-12DM/883 AT28HC256(E,F)-12FM/883 AT28HC256(E,F)-12LM/883 AT28HC256(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	0.3	5962-88634 03 UX 5962-88634 03 XX 5962-88634 03 YX 5962-88634 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	80	0.3	5962-88634 04 UX 5962-88634 04 XX 5962-88634 04 YX 5962-88634 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-88634 01 UX 5962-88634 01 XX 5962-88634 01 YX 5962-88634 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	80	0.3	5962-88634 02 UX 5962-88634 02 XX 5962-88634 02 YX 5962-88634 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Note: 1. See Valid Part Number table below.

Ordering Information Note

Previous data sheets included the low power suffixes L, LE and LF on the AT28HC256 for 120 ns and 90 ns speeds. The low power parameters are now *standard*; therefore, the L, LE and LF suffixes are no longer required.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28HC256	70	JC, JI, PC, PI
AT28HC256	90	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256E	90	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256F	90	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256	12	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256E	12	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256F	12	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

E²PROM Data Protection

Advantages of E²PROMs

E²PROMs provide the memory solution wherever reprogrammable, nonvolatile memory is required. They are easy to use, requiring little or no support hardware such as refresh clocks or batteries. Each memory location can be selectively changed without impact on any other location; blanket erasure and rewriting of the entire device or a large section of it is not required.

E²PROMs made at Atmel were designed to provide the best features available. Atmel E²PROMs provide high speed read access times so that many applications can use them without inserting costly wait states. The page mode write operation of Atmel E²PROMs allows for the fastest effective write time available in E²PROM memories. Since all of Atmel's devices are made in CMOS, they offer the benefits of low operating and standby power.

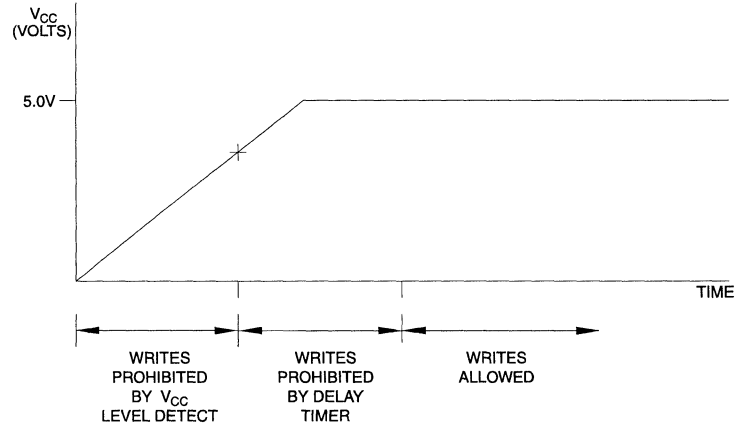
In order to take advantage of all of the benefits of Atmel E²PROMs, care must be taken to maintain the integrity of the data. While an E²PROM will retain its data for many years with or without power applied, improper operation of the device could result in data being inadvertently rewritten.

When is Data Susceptible to Corruption

In the use of any memory device, it is expected that the data stored in it is available as it is written. This is especially true of E²PROMs since their code often controls the operation of the system in which they are contained. Unlike most other memory types that are rewritten in systems, E²PROMs are often expected to retain their data for a period of many years, with or without power applied and during power transitions. For these reasons, added attention is given to avoid corrupting data in E²PROMs.

(continued)

Figure 1. Hardware Data Protection- Power Level Sense Detector and Power On Delay Timer



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When is Data Susceptible to Corruption (Continued)

There are a number of situations in which data is particularly prone to corruption. These situations include powering on and off of the devices, noise spikes on the control lines and system glitches. Atmel E^2PROMs include features to help protect against each of these potential sources of inadvertent writes. Atmel data protection features are broken down into two different types: hardware data protection features and software data protection features.

Atmel Hardware Data Protection Features

Atmel E^2PROMs include four different types of hardware data protection. These features provide protection against most inadvertent writes that might occur in a system. Atmel hardware data protection features include: three line write control, power level sense detector, power on delay timer and noise filters on $\overline{CE}$ and $\overline{WE}$.

THREE-LINE WRITE CONTROL: In order to write a device the $\overline{OE}$ signal must be high with the $\overline{CE}$ and $\overline{WE}$ signals low. Holding any of the three lines in the opposite state will prohibit a write cycle. For example, whenever the $\overline{OE}$ signal is low, a write to the device cannot be started.

POWER LEVEL SENSE DETECTOR: An active circuit in Atmel E^2PROMs monitors the level of the supply voltage to the device. If the supply is below 3.8 volts, typical, write cycles to the devices can not be activated.

POWER ON DELAY TIMER: As power is applied to Atmel E^2PROMs, the power level sense detector will issue an internal signal that indicates that the supply is above the sense level. At this time an internal timer is initiated that times out in typically 5 ms. During this time period, writes to the device cannot be performed. This delay period serves two purposes. First, it allows the supply level additional time to rise to within the standard operating region before writes are permitted. Secondly, it lets the system stabilize and present the correct levels to the control pins of the E^2PROM so that the E^2PROM doesn't react to its inputs before they are actually valid. Figure 1 shows the combined action of the power supply level detector and the delay timer upon writes to the device.

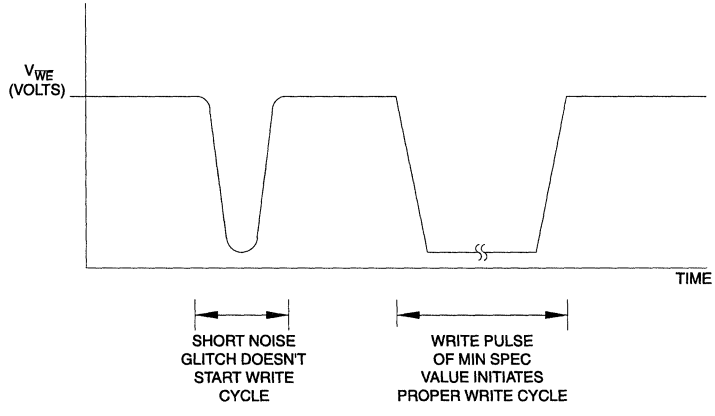
NOISE FILTERS ON $\overline{WE}$ AND $\overline{CE}$: If brief noise pulses below V_{IH} occur on the $\overline{WE}$ or $\overline{CE}$ inputs to the device, a write cycle will not be initiated. Internal to the E^2PROM, a noise filter does not allow the short pulses to activate a write cycle. As shown in Figure 2, write pulses of sufficient length will still initiate writes but short noise spikes on the $\overline{WE}$ or $\overline{CE}$ control lines will not.

Atmel Software Data Protection Feature

Available on some Atmel E^2PROMs is a user selectable feature that requires a software sequence at the beginning of each write cycle in order for a write to be performed. To enable the software data protection feature, a series of three-write commands to specific addresses with specific data must be performed. Once set, the same 3-byte code must begin each write request. (A separate write cycle to enable the software feature is not necessary; after any write that is preceded with the 3-byte code, the software data protection function will be enabled, see Figure 3.) The feature may be disabled by issuing a 6-byte code to the device as shown in Figure 4. After being set, the software data protection feature remains active until its disable command is issued. Power transitions will not reset the software data protection feature, but the feature will prevent against inadvertent writes during power transitions.

(continued)

Figure 2. Hardware Data Protection- Noise Filter



Atmel Software Data Protection Feature (Continued)

The software data protection feature protects data against various causes of inadvertent writes. Since it is active during power transitions it protects data when powering on or off the device. Noise spikes that occur on the control lines will be ignored since they will not show the correct address and data needed to start a write cycle. Even for system malfunctions, such as when write pulses of adequate length are given to the device, the software feature can prevent the corruption of the data in the E²PROM. The address locations used for the software code are not sacrificed from the usable memory array. The device recognizes the software code and does not alter the data stored at the address locations of the code. Byte locations of code are still usable, and don't have to be rewritten.

System Design Considerations

Designing systems with data integrity in mind can greatly reduce the chance of lost data. The amount of attention needed depends upon the nature of the design. Following are a few areas that might need special attention in certain designs.

External Power On Protection

Many systems will have a PON (power on) signal to control the operation of the system. Such a signal can be gated with the logic creating the $\overline{OE}$ signal to the E²PROM, holding $\overline{OE}$ low when the PON signal is false. Similarly, a PON-type signal could be gated with the $\overline{WE}$ or $\overline{CE}$ logic, forcing $\overline{WE}$ or $\overline{CE}$ high when writes should not be allowed.

If the system does not include a PON-type signal, one can be created from various programmable voltage reference devices. With such a device, the user can select the voltage supply level below which the device cannot be written. It should be noted that in many systems, using Atmel's E²PROMS with their internal power level detection and power delay timer, no additional power on circuitry is required for the device.

Multiple Power Supplies

In systems that utilize more than one power supply, extra care must be taken during power transitions to both the E²PROM and the devices controlling the inputs to the E²PROM. Power on rates of the different supplies are likely to vary. Using programmable voltage reference devices to detect the power level of both supplies and forcing the $\overline{OE}$ pin low when either line is below the desired level may be used in such situations to avoid inadvertent writes.

Memory Cards

Since memory cards are often pushed into and pulled out of systems that are already powered on, they have additional chances of inadvertent writes. If the edge connector is arranged such that power and control lines are not asserted in a prescribed manner, false writes to the device may occasionally occur depending upon how the card is inserted. To provide proper power on sequencing, a card could be designed with its control pins recessed from the edge of the card. Resistors would be placed on the card to connect $\overline{CE}$ and $\overline{WE}$ to V_{CC} and $\overline{OE}$ to ground. This arrangement insures that power is first applied to the device and that the control pins are not in the write state until each pin is being controlled by the host system. Variations of this technique may be used effectively in different systems; the basic idea is to guarantee systematic application of the power and control pins such that a write state is not entered upon insertion or removal of the card from the host.

Figure 3. Software Data Protection- Enable

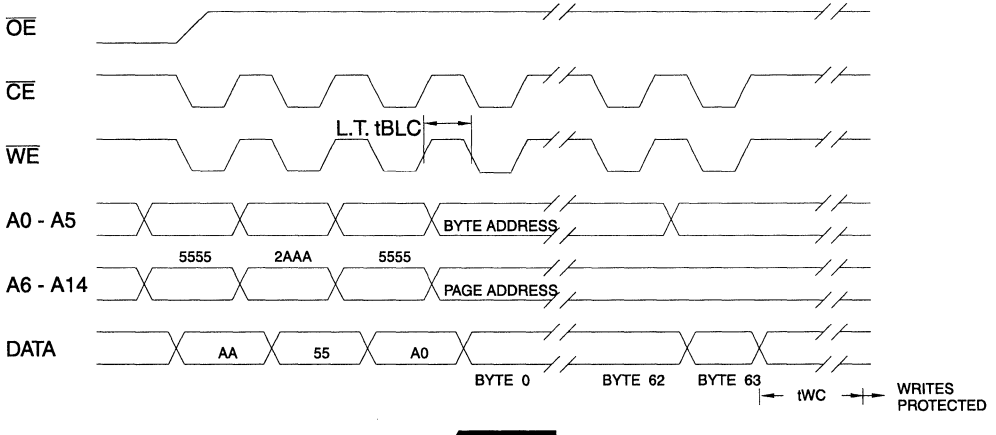
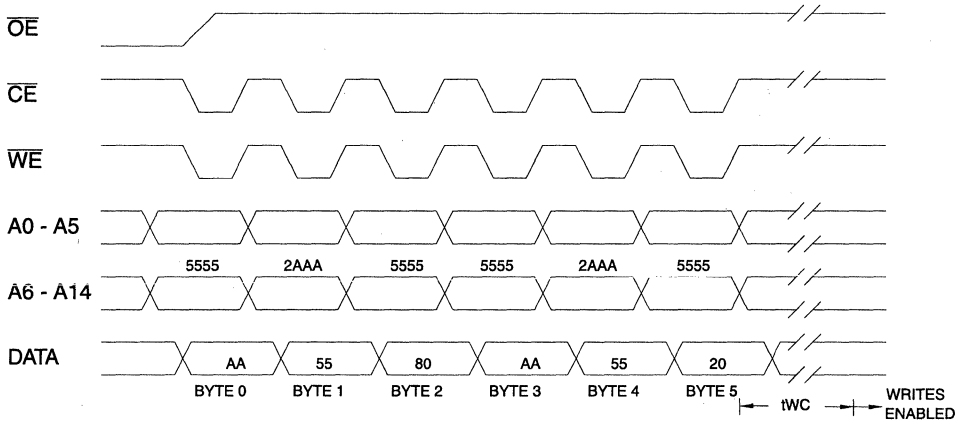


Figure 4. Software Data Protection- Disable



Software Chip Erase

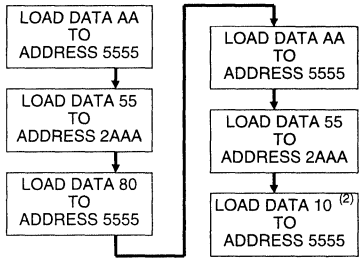
The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFh). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time required to erase the whole chip is t_{EC} (20 ms). The software data protection is still enabled even after the software chip erase is performed.

Chip Erase Cycle Characteristics

Symbol	Parameter	
t_{EC}	Chip Erase Cycle Time	20 ms Max

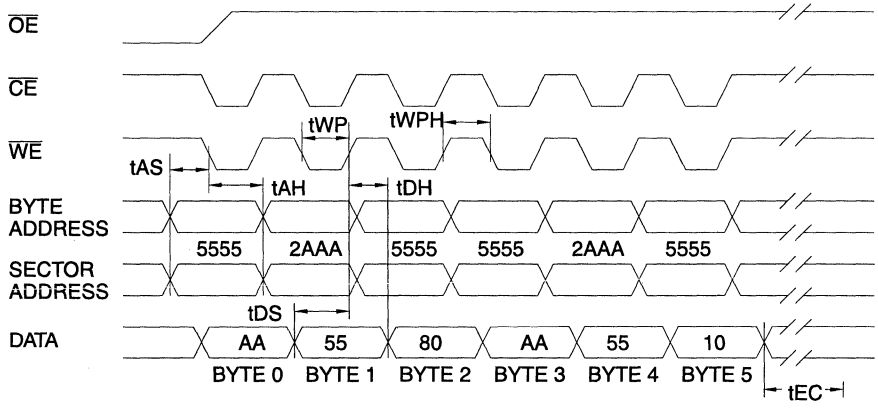
Note: 1. Please refer to individual data sheets for the minimum and maximum values of the t_{AS}, t_{AH}, t_{DS}, t_{DH}, t_{WP}, t_{BLC}, and t_{WPH} parameters.

Chip Erase Software Algorithm (1, 3)



Notes: 1. Data Format: (Hex); Address Format: (Hex).
2. After loading the 6-byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion in 20 ms (max).
3. The flow diagram shown is for a x8 part. For a x16 part, the data should be 16 bits long (e.g., the data to be loaded should be AAAA for step 1 in the algorithm).

Chip Erase Cycle Waveforms



Note: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Programmers That Support Atmel Memory Products

The following programmers support Atmel memory products. Please contact the companies individually to find out if specific products and packages are supported.

Advin Systems Inc.
1050-L East Duane Avenue
Sunnyvale, California 95086
(408) 243-7000

BP Microsystems
1000 North Post Oak Road, Suite #225
Houston, Texas 77055-7237
(713) 688-4600

Bytek Corporation
543 North West 77th Street
Bocaraton, Florida 33487-1323
(407) 994-3520

Data I/O Corporation
P.O. Box 97946
10525 Willows Road NE
Redmond, Washington 98073-9746
(800) 247-5700

Elan Systems, Inc.
365 Woodview Avenue, Suite #700
Morgan Hill, California 95037
(408) 778-7267

Logical Devices
692 South Military Trail
Deerfield Beach, Florida 33442
(305) 428-6868

Minato Electronics
3628 Madison Avenue, Suite #5
North Highlands, California 95660
(916) 348-6066

Needham's Electronics
4630 Beloit Drive, Suite #20
Sacramento, California 95841
(916) 924-8037

SMS
17411 N.E. Union Hill Road,
Suite #100
Redmond, Washington 98052
(206) 883-8447

System General
1603A South Main Street
Milpitas, California 95035
(408) 263-6667

Interfacing AT24CXX Serial E²PROMs with AT89CX051 Microcontrollers

Serial memory devices offer significant advantages over parallel devices in applications where lower data transfer rates are acceptable. In addition to requiring less board space, serial devices allow microcontroller I/O pins to be conserved. This is especially valuable when adding external memory to low pin count microcontrollers such as the Atmel AT89C1051 and AT89C2051.

This application note presents a suite of software routines which may be incorporated into a user's application to allow an AT89CX051 microcontroller to read and write AT24CXX serial E²PROMs. The software supports all members of the AT24CXX family, and may easily be modified for compatibility with any of the Atmel 8051-code compatible microcontrollers.

Hardware

A typical interconnection between an AT89CX051 microcontroller and an AT24CXX serial E²PROM is shown in Figure 1. As indicated in the figure, up to eight members of the AT24CXX family may share the bus, utilizing the same two microcontroller I/O pins. Each device on the bus must have its address inputs (A0, A1, A2) hard-wired to a unique address. In the figure, the first device recognizes address zero (A0, A1, A2 tied low), while the eighth recognizes address seven (A0, A1, A2 tied high). Not all members of the AT24CXX family recognize all three address inputs, limiting the number of some devices which may be present to less than eight. The exact number of devices of each type which may share the bus is shown in Table 1.

Bidirectional Data Transfer Protocol

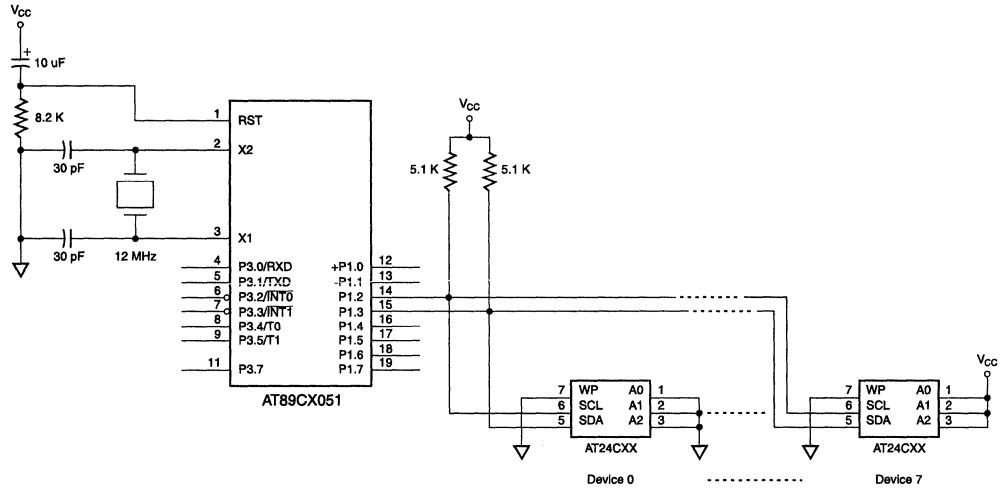
The Bidirectional Data Transfer Protocol utilized by the AT24CXX family allows a number of compatible devices to share a common 2-wire bus. The bus consists of a serial clock (SCL) line and a serial

(continued)

Table 1. Atmel's 2-Wire Serial E²PROM Family

Device	Size (Bytes)	Page Size (Bytes)	Max Per Bus	Addresses Used
AT24C01	1K	8	1	None
AT24C01A	1K	8	8	A0, A1, A2
AT24C02	2K	8	8	A0, A1, A2
AT24C04	4K	16	4	A1, A2
AT24C08	8K	16	2	A2
AT24C16	16K	16	1	None
AT24C164	16K	16	8	A0, A1, A2
AT24C32	32K	32	8	A0, A1, A2
AT24C64	64K	32	8	A0, A1, A2

Figure 1. Typical Circuit Configuration



Bidirectional Data Transfer Protocol (Continued)

data (SDA) line. The clock is generated by the bus master and data is transmitted serially on the data line, most significant bit first, synchronized to the clock. The protocol supports bidirectional data transfers in 8 bit bytes.

In this application, the microcontroller serves as the bus master, initiating all data transfers and generating the clock which regulates the flow of data. The serial devices present on the bus are considered slaves, accepting or sending data in response to orders from the master.

The bus master initiates a data transfer by generating a start condition on the bus. This is followed by transmission of a byte containing the device address of the intended recipient. The device address consists of a 4 bit fixed portion and a 3 bit programmable portion. The fixed portion must match the value hard-wired into the slave, while the programmable portion allows the master to select between a maximum of eight slaves of similar type on the bus.

AT24CXX serial E^2PROMs respond to device addresses with a fixed portion equal to '1010' and a programmable portion matching the address inputs (A0, A1, A2). Not all members of the AT24CXX family examine all three address inputs; Table 1 shows which of the three address inputs are valid for each member of the family.

The eighth bit in the device address byte specifies a write or read operation. After the eighth bit is transmitted, the master releases the data line and generates a ninth clock.

If a slave has recognized the transmitted device address, it will respond to the ninth clock by generating an acknowledge condition on the data line. A slave which is busy when addressed may not generate an acknowledge. This is true for the AT24CXX when a write operation is in progress.

Following receipt of the slave's address acknowledgment, the master continues with the data transfer. If a write operation has been ordered, the master transmits the remaining data, with the slave acknowledging receipt of each byte. If the master has ordered a read operation, it releases the data line and clocks in data sent by the slave. After each byte is received, the master generates an acknowledge condition on the bus. The acknowledge is omitted following receipt of the last byte. The master terminates all operations by generating a stop condition on the bus. The master may also abort a data transfer at any time by generating a stop condition.

Refer to the AT24CXX family data sheets for detailed information on AT24CXX device operation and Bidirectional Data Transfer Protocol bus timing.

The software for this application may be obtained by downloading from Atmel's Web Site or BBS: (408) 436-4309. Consult the comment block at the beginning of the source code file for detailed information on features and operation.

Web Site: http://www.atmel.com

BBS: 1-(408) 436-4309

Interfacing AT93CXX Serial E²PROMs with AT89CX051 Microcontrollers

Serial memory devices offer significant advantages over parallel devices in applications where lower data transfer rates are acceptable. In addition to requiring less board space, serial devices allow microcontroller I/O pins to be conserved. This is especially valuable when adding external memory to low pin count microcontrollers such as the Atmel AT89C1051 and AT89C2051.

This appplication note presents a suite of software routines which may be incorporated into a user's application to allow AT89CX051 microcontrollers to read and write AT93CXX serial E²PROMs. All seven AT93CXX device functions are supported: read, write, write all, erase, erase all, erase/write enable and erase/write disable. The routines are general purpose, supporting both eight-bit and sixteen-bit accesses to all members of the 93CXX family. In addition, both 3-wire and 4-wire configurations are supported.

The AT93CXX may be connected to the AT89CX051 microcontroller in either a 3-wire (Figure 1) or 4-wire (Figure 2) configuration. In the 3-wire configuration, the E²PROM serial data in (DI) and serial data out (DO) pins are both connected to the same microcontroller I/O pin, thereby saving a pin. This is possible because the microcontroller I/O pins can be dynamically reprogrammed as input or output.

Note the strapping of the AT93CXX ORG pins shown in Figure 1 and Figure 2. The ORG (internal organization) pin selects 8 bit data when grounded and 16 bit data when floating or tied to V_{CC}. The ORG pin connections shown in the figures are for illustration only; 8 bit or 16 bit data may be selected in either the 3-wire or 4-wire configuration.

The software for this application may be obtained by downloading from Atmel's Web Site or BBS. Consult the comment block at the beginning of the source code file for detailed information on features and operation.

Web Site: http://www.atmel.com
BBS: 1-(408) 436-4309

2

Interfacing 93CXX Serial E²PROMS

Application Note

0521B

Figure 1. 3-Wire Configuration

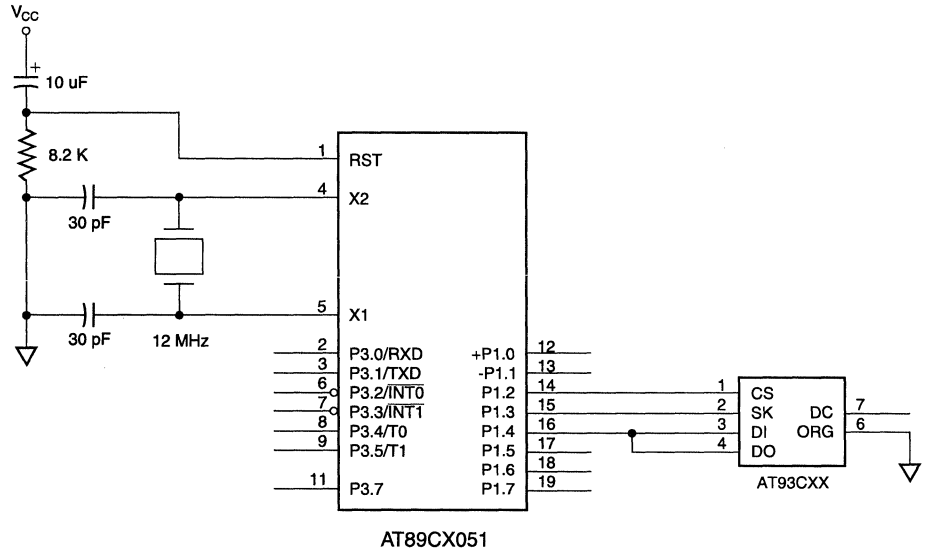
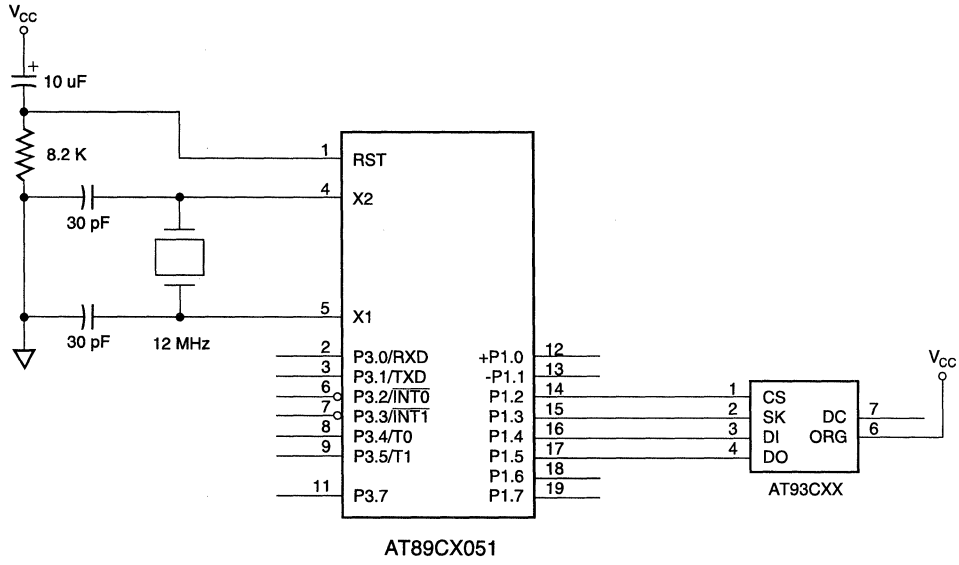


Figure 2. Typical Circuit Configuration



Interfacing AT25XXX Serial E²PROMs with AT89CXX Microcontrollers

SERIAL PERIPHERAL INTERFACE

Serial memory devices offer significant advantages over parallel devices in applications where lower data transfer rates are acceptable. In addition to requiring less board space, serial devices allow microcontroller I/O pins to be conserved. This is especially valuable when adding external memory to low pin count microcontrollers such as the Atmel AT89C1051 and AT89C2051.

This application note presents a suite of software routines which may be incorporated into a user's application to allow AT89CXX microcontrollers to read from and write to AT25XXX serial E²PROMs. All six AT25XXX device operations are supported: read memory, write memory, read status, write status, (set write protection levels), write enable and write disable. Routines are also provided to read from and write to memory utilizing the page mode of the AT25XXX. The software supports both 3-wire and 4-wire configurations and meets all AT25XXX family timing requirements when run on an AT89CXX microcontroller with a 24 MHz clock.

HARDWARE

The AT25XXX may be connected to the AT89CXX microcontroller in either a 3-wire (Figure 1) or 4-wire (Figure 2) configuration. In the 3-wire configuration, the E²PROM serial data in (SI) and serial data out (SO) pins are both connected to the same microcontroller I/O pin, thereby saving a pin. This is possible because the microcontroller I/O pins can be dynamically reprogrammed as input or output.

SOFTWARE

Software for this application note may be downloaded from Atmel's Web Site or BBS. Consult the comment block at the beginning of the source code file for detailed information on features and operation.

Web Site: http://www.atmel.com

BBS: 1-(408) 436-4309

Figure 1. 3-Wire Configuration

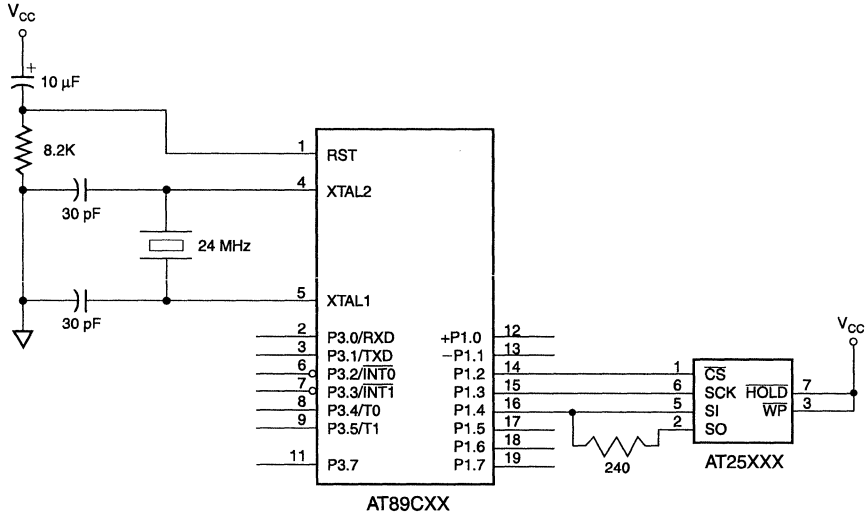
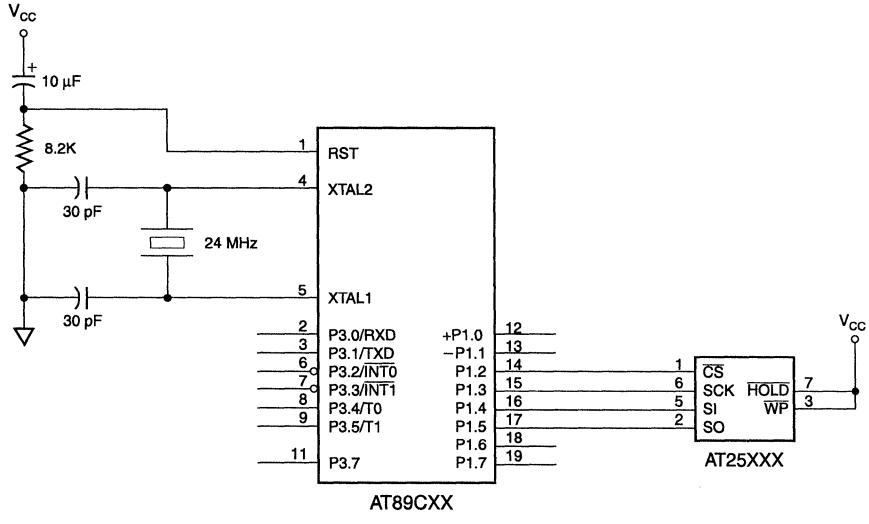


Figure 2. 4-Wire Configuration



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ATMEL

ATTENTION:

The following data sheets show the improper pinout, a 40-pin TSOP instead of a 32-pin TSOP:

AT27BV010

AT27LV010A

AT27CO10/L

For the corrected data sheets, access Atmel's Fax-on-Demand system, Web site or CD-ROM version of this data book.

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256K (32K x 8) Unregulated *Battery-Voltage*™ High Speed OTP CMOS EPROM

Features

- Fast Read Access Time - 70 ns
- Dual Voltage Range Operation
  - Unregulated Battery Power Supply Range, 2.7V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Pin Compatible with JEDEC Standard AT27C256
- Low Power CMOS Operation
  - 20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Surface Mount Packages
  - 32-Lead PLCC
  - 28-Lead 330-mil SOIC
  - 28-Lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL and LVBO
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27BV256 is a high performance, low power, low voltage 262,144 bit one-time programmable read only memory (OTP EPROM) organized as 32K by 8 bits. It requires only one supply in the range of 2.7V to 3.6V in normal read mode operation, making it ideal for fast, portable systems using either regulated or unregulated battery power.

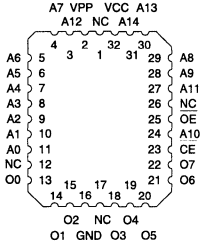
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 2.7V, any word can be accessed in less than 70 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3V, the AT27BV256 consumes less than one fifth the power of a standard 5V EPROM.

(continued)

Pin Configurations

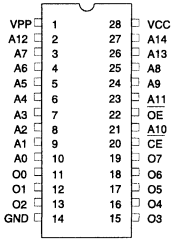
Pin Name	Function
A0 - A14	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

PLCC Top View



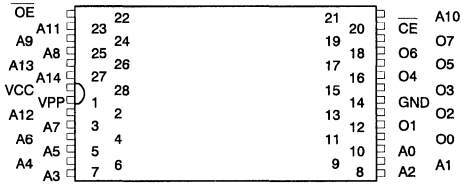
Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

SOIC Top View



TSOP Top View

Type 1



0601A

Description (Continued)

Standby mode supply current is typically less than 1 µA at 3V. The AT27BV256 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

The AT27BV256 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC, SOIC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

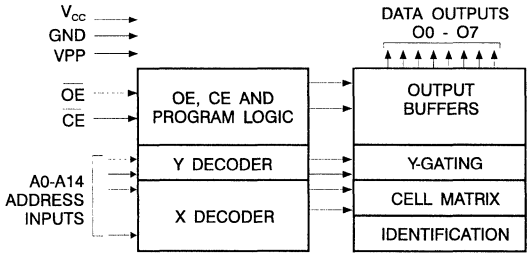
The AT27BV256 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. At V_{CC} = 2.7V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27BV256 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV256 programs exactly the same way as a standard 5V AT27C256R and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC} (2)	D_{OUT}
Output Disable (2)	V_{IL}	V_{IH}	X (1)	V_{CC}	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	V_{CC}	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (3)	D_{IN}
PGM Verify (3)	X	V_{IL}	Ai	V_{PP}	V_{CC} (3)	D_{OUT}
Optional PGM Verify (3)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A14 = V_{IL}	V_{CC}	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, $2.7V \le V_{CC} \le 3.6V$, or $4.5V \le V_{CC} \le 5.5V$.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. $V_H = 12.0 \pm 0.5V$.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27BV256			
		-70	-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 2.7V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.6V		8	mA
V_{IL}	Input Low Voltage	V_{CC} = 3.0 to 3.6V	-0.6	0.8	V
		V_{CC} = 2.7 to 3.6V	-0.6	0.2 x V_{CC}	V
V_{IH}	Input High Voltage	V_{CC} = 3.0 to 3.6V	2.0	V_{CC} + 0.5	V
		V_{CC} = 2.7 to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
		I_{OL} = 100 µA		0.2	V
		I_{OL} = 20 µA		0.1	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
		I_{OH} = -100 µA	V_{CC} - 0.2		V
		I_{OH} = -20 µA	V_{CC} - 0.1		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		20	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

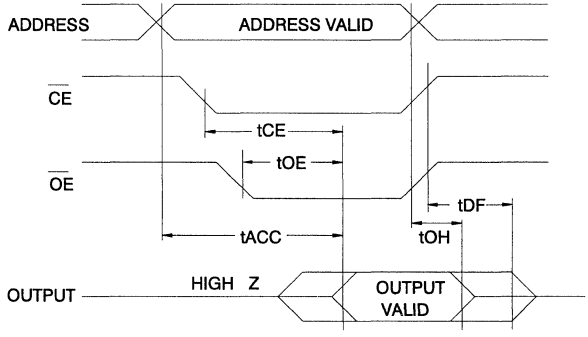
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation (V_{CC} = 2.7V to 3.6V and 4.5V to 5.5V)

			AT27BV256								
			-70		-90		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		50		50		50		60	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		40		40		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		0		0		ns

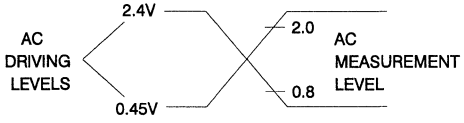
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

AC Waveforms for Read Operation (1)



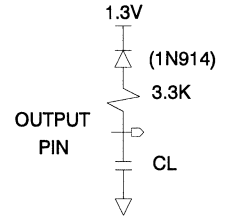
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.
6. When reading a 27BV256, a 0.1 µF capacitor is required across V_{CC} and ground to supress spurious voltage transients.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



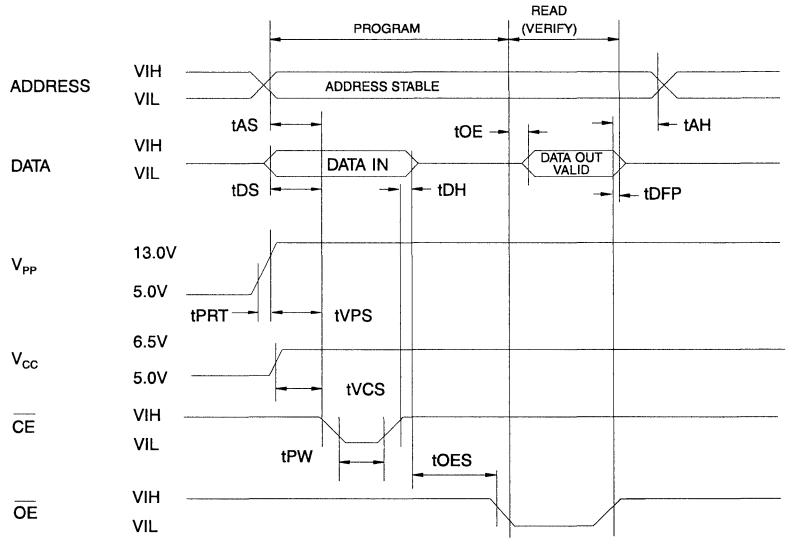
Note: CL = 100 pF
including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27BV256 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$ (2)			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

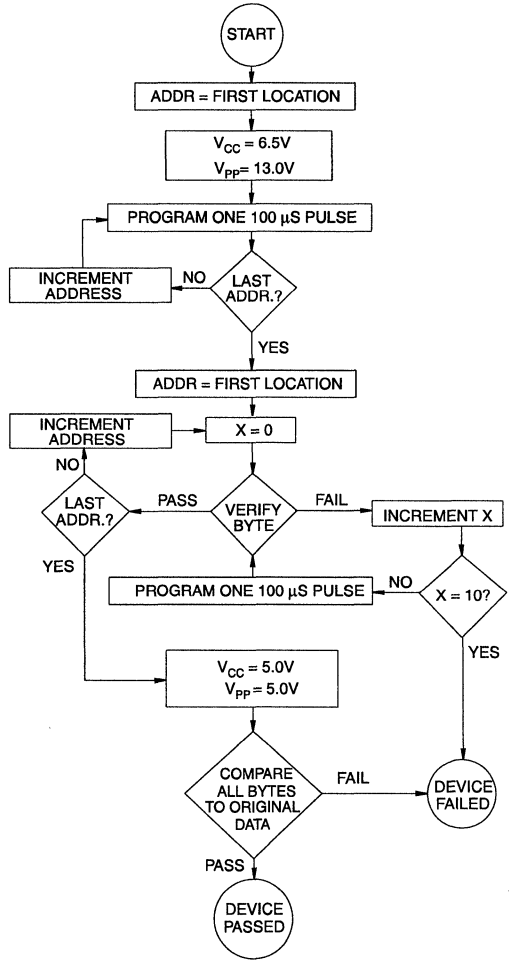
Atmel's 27BV256 Integrated Product Identification Code (1)

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Note: 1. The AT27BV256 has the same Product Identification Code as the AT27C256R. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	8	0.02	AT27BV256-70JC AT27BV256-70RC AT27BV256-70TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27BV256-70JI AT27BV256-70RI AT27BV256-70TI	32J 28R 28T	Industrial (-40°C to 85°C)
90	8	0.02	AT27BV256-90JC AT27BV256-90RC AT27BV256-90TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27BV256-90JI AT27BV256-90RI AT27BV256-90TI	32J 28R 28T	Industrial (-40°C to 85°C)
120	8	0.02	AT27BV256-12JC AT27BV256-12RC AT27BV256-12TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27BV256-12JI AT27BV256-12RI AT27BV256-12TI	32J 28R 28T	Industrial (-40°C to 85°C)
150	8	0.02	AT27BV256-15JC AT27BV256-15RC AT27BV256-15TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27BV256-15JI AT27BV256-15RI AT27BV256-15TI	32J 28R 28T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 90 ns
- Dual Voltage Range Operation
  - Unregulated Battery Power Supply Range, 2.7V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Pin Compatible with JEDEC Standard AT27C512
- Low Power CMOS Operation
  - 20 µA max. (less than 1µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Surface Mount Packages
  - 32-Lead PLCC
  - 28-Lead 330-mil SOIC
  - 28-Lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL and LVBO
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27BV512 is a high performance, low power, low voltage 524,288 bit one-time programmable read only memory (OTP EPROM) organized as 64K by 8 bits. It requires only one supply in the range of 2.7V to 3.6V in normal read mode operation, making it ideal for fast, portable systems using either regulated or unregulated battery power.

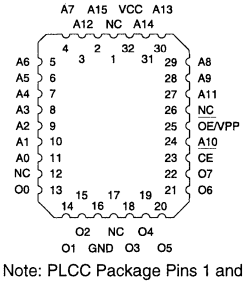
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 2.7V, any byte can be accessed in less than 90 ns. With a typical power consumption of only 18 mW at 5 MHz and V_{CC} = 3V, the AT27BV512 consumes less than one fifth the power of a standard 5V EPROM.

(continued)

Pin Configurations

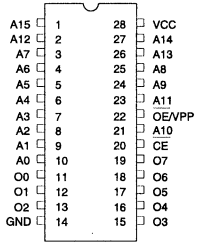
Pin Name	Function
A0 - A15	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable
NC	No Connect

PLCC Top View



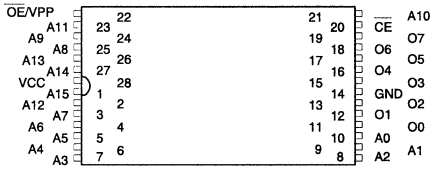
Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

SOIC Top View



TSOP Top View

Type 1



512K (64K x 8) Unregulated *Battery-Voltage*™ High Speed OTP CMOS EPROM

3

0602A

Description (Continued)

Standby mode supply current is typically less than 1 µA at 3V. The AT27BV512 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

The AT27BV512 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC, SOIC, and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

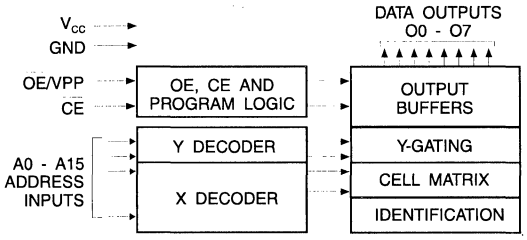
The AT27BV512 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. At V_{CC} = 2.7V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27BV512 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV512 programs exactly the same way as a standard 5V AT27C512R and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	Ai	V_{CC} (2)	D_{OUT}
Output Disable (2)	V_{IL}	V_{IH}	X (1)	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{PP}	Ai	V_{CC} (3)	D_{IN}
PGM Verify (3)	V_{IL}	V_{IL}	Ai	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	V_{PP}	X	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A15 = V_{IL}	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 2.7V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27BV512		
		-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 2.7V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.6V		8	mA
V_{IL}	Input Low Voltage	V_{CC} = 3.0 to 3.6V	-0.6	0.8	V
		V_{CC} = 2.7 to 3.6V	-0.6	0.2 x V_{CC}	V
V_{IH}	Input High Voltage	V_{CC} = 3.0 to 3.6V	2.0	V_{CC} + 0.5	V
		V_{CC} = 2.7 to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
		I_{OL} = 100 µA		0.2	V
		I_{OL} = 20 µA		0.1	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
		I_{OH} = -100 µA	V_{CC} - 0.2		V
		I_{OH} = -20 µA	V_{CC} - 0.1		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		20	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before $\overline{OE}/V_{PP}$, and removed simultaneously with or after $\overline{OE}/V_{PP}$.

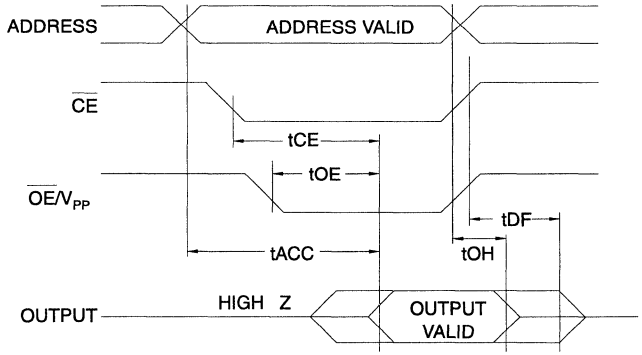
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation (V_{CC} = 2.7V to 3.6V and 4.5V to 5.5V)

Symbol	Parameter	Condition	AT27BV512 -90 Min	-90 Max	-12 Min	-12 Max	-15 Min	-15 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}		90		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$ = V_{IL}		90		120		150	ns
t_{OE} (2, 3)	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$ = V_{IL}		50		50		60	ns
t_{DF} (4, 5)	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		40		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first		0		0		0		ns

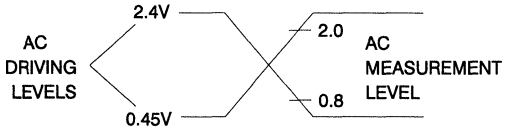
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

AC Waveforms for Read Operation (1)



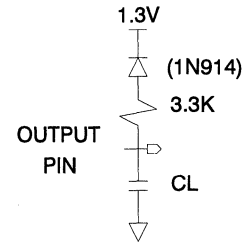
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.
6. When reading the 27BV512, a 0.1 µF capacitor is required across V_{CC} and grond to supress spurious voltage transients.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



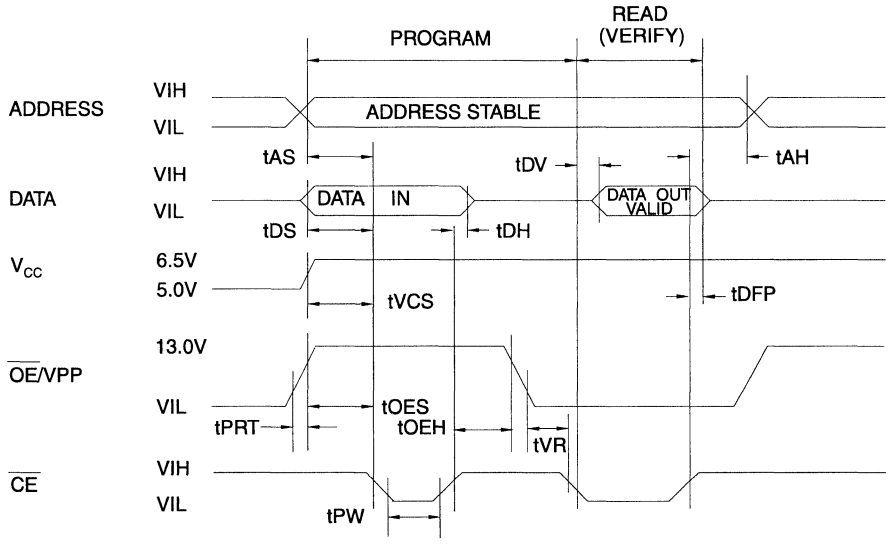
Note: CL = 100 pF
including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27BV512, a 0.1 µF capacitor is required across V_{PP} and ground to supress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, $\overline{OE}/V_{PP}$ = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, $\overline{OE}/V_{PP}$ = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay (2)		0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		95	105	µs
t_{DV}	Data Valid from $\overline{CE}$ (2)			1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

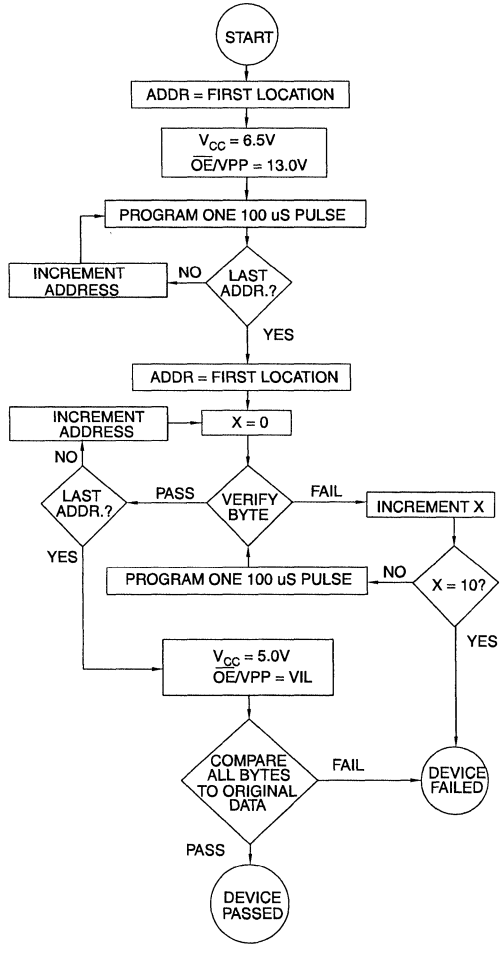
Atmel's 27BV512 Integrated Product Identification Code (1)

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

Note: 1. The AT27BV512 has the same Product Identification Code as the AT27C512R. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	8	0.02	AT27BV512-90JC AT27BV512-90RC AT27BV512-90TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27BV512-90JI AT27BV512-90RI AT27BV512-90TI	32J 28R 28T	Industrial (-40°C to 85°C)
120	8	0.02	AT27BV512-12JC AT27BV512-12RC AT27BV512-12TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27BV512-12JI AT27BV512-12RI AT27BV512-12TI	32J 28R 28T	Industrial (-40°C to 85°C)
150	8	0.02	AT27BV512-15JC AT27BV512-15RC AT27BV512-15TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27BV512-15JI AT27BV512-15RI AT27BV512-15TI	32J 28R 28T	Industrial (-40°C to 85°C)

3

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Thin Small Outline Package (TSOP)

1 Megabit (128K x 8) Unregulated *Battery-Voltage*™ OTP CMOS EPROM

Features

- **Fast Read Access Time - 70 ns**
- **Dual Voltage Range Operation**
  - **Unregulated Battery Power Supply Range, 2.7V to 3.6V**
  - **or Standard 5V ± 10% Supply Range**
- **Compatible with JEDEC Standard AT27C010**
- **Low Power CMOS Operation**
  - **20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V**
  - **29 mW max. Active at 5 MHz for V_{CC} = 3.6V**
- **JEDEC Standard Packages**
  - **32-Lead PLCC**
  - **32-Lead TSOP**
- **High Reliability CMOS Technology**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming Algorithm - 100 µs/byte (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **JEDEC Standard for LVTTL and LVBO**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

Description

The AT27BV010 is a high performance, low power, low voltage 1,048,576 bit one-time programmable read only memory (OTP EPROM) organized as 128K by 8 bits. It requires only one supply in the range of 2.7V to 3.6V in normal read mode operation, making it ideal for fast, portable systems using either regulated or unregulated battery power.

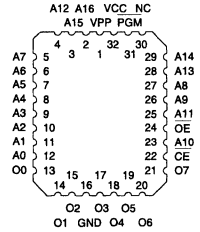
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 2.7V, any byte can be accessed in less than 70 ns. With a typical power draw of only 18 mW at 5 MHz and V_{CC} = 3V, the AT27BV010 consumes less than one fifth the power of a standard 5V

(continued)

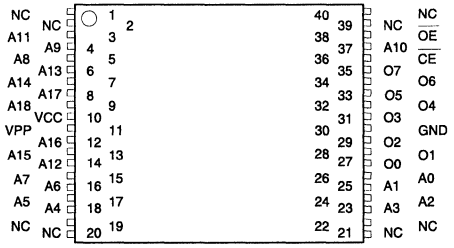
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

PLCC Top View



TSOP Top View
Type 1



0344D

Description (Continued)

EPROM. Standby mode supply current is typically less than 1 µA at 3V. The AT27BV010 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

The AT27BV010 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

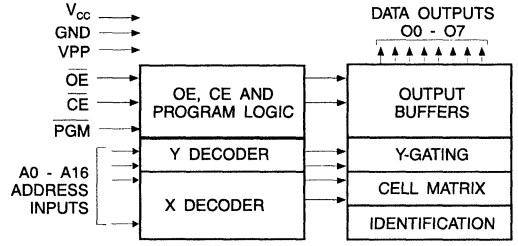
The AT27BV010 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. At V_{CC} = 2.7V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27BV010 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV010 programs exactly the same way as a standard 5V AT27C010 and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	X (1)	Ai	X	V_{CC} (2)	D_{OUT}
Output Disable (2)	X	V_{IH}	X	X	X	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	X	X	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC} (3)	D_{IN}
PGM Verify (3)	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	X	X	X	V_{PP}	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	X	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A16 = V_{IL}	X	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 2.7V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27BV010			
		-70	-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

= Preliminary Information

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 2.7V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.6V		8	mA
V_{IL}	Input Low Voltage	V_{CC} = 3.0 to 3.6V	-0.6	0.8	V
		V_{CC} = 2.7 to 3.6V	-0.6	0.2 x V_{CC}	V
V_{IH}	Input High Voltage	V_{CC} = 3.0 to 3.6V	2.0	V_{CC} + 0.5	V
		V_{CC} = 2.7 to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
		I_{OL} = 100 µA		0.2	V
		I_{OL} = 20 µA		0.1	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
		I_{OH} = -100 µA	V_{CC} - 0.2		V
		I_{OH} = -20 µA	V_{CC} - 0.1		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		25	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during pro gramming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation (V_{CC} = 2.7V to 3.6V and 4.5V to 5.5V)

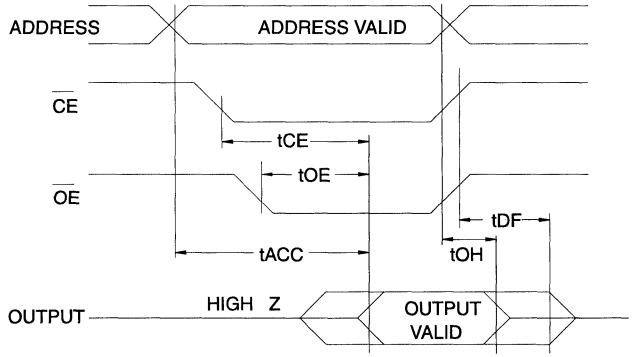
Symbol	Parameter	Condition	AT27BV010 -70 Min	-70 Max	-90 Min	-90 Max	-12 Min	-12 Max	-15 Min	-15 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		50		50		50		60	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		40		40		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

= Preliminary Information

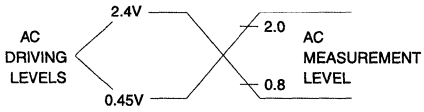
3

AC Waveforms for Read Operation (1)



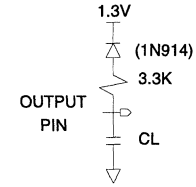
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



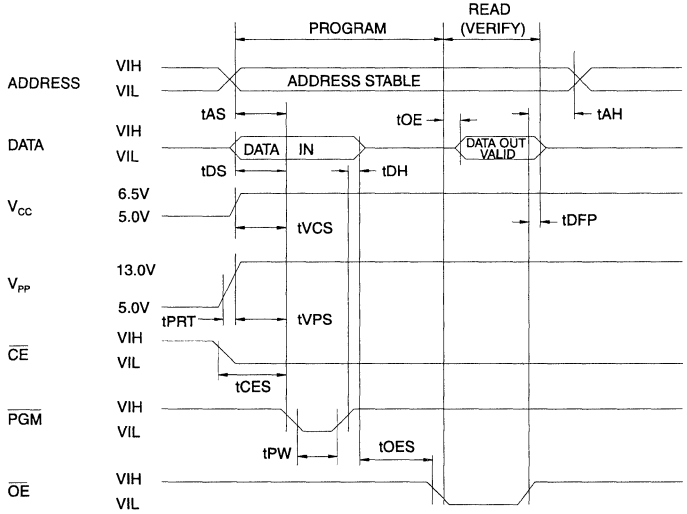
Note: CL = 100 pF
including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27BV010, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.2V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

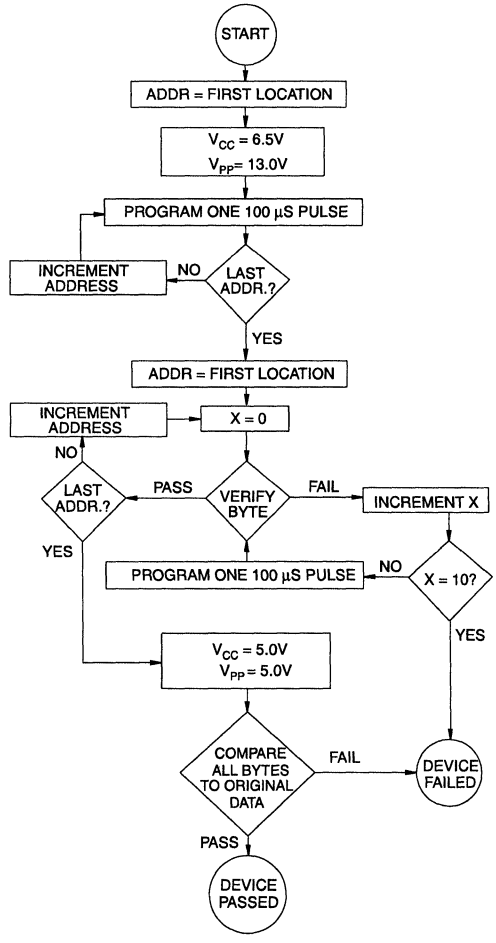
Atmel's 27BV010 Integrated Product Identification Code (1)

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	05

Note: 1. The AT27BV010 has the same Product Identification Code as the AT27C010. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.6V		Ordering Code	Package	Operation Range
	Active	Standby			
70	8	0.02	AT27BV010-70JC AT27BV010-70TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27BV010-70JI AT27BV010-70TI	32J 32T	Industrial (-40°C to 85°C)
90	8	0.02	AT27BV010-90JC AT27BV010-90TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27BV010-90JI AT27BV010-90TI	32J 32T	Industrial (-40°C to 85°C)
120	8	0.02	AT27BV010-12JC AT27BV010-12TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27BV010-12JI AT27BV010-12TI	32J 32T	Industrial (-40°C to 85°C)
150	8	0.02	AT27BV010-15JC AT27BV010-15TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27BV010-15JI AT27BV010-15TI	32J 32T	Industrial (-40°C to 85°C)

= Preliminary Information

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 90 ns
- Dual Voltage Range Operation
  - Unregulated Battery Power Supply Range, 2.7V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Pin Compatible with JEDEC Standard AT27C1024
- Low Power CMOS Operation
  - 20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Surface Mount Packages
  - 44-Lead PLCC
  - 40-Lead TSOP (10 x 14mm)
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/word (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL and LVBO
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27BV1024 is a high performance, low power, low voltage 1,048,576 bit one-time programmable read only memory (OTP EPROM) organized as 64K by 16 bits. It requires only one supply in the range of 2.7V to 3.6V in normal read mode operation. The by-16 organization makes this part ideal for portable and handheld 16 and 32 bit microprocessor based systems using either regulated or unregulated battery power.

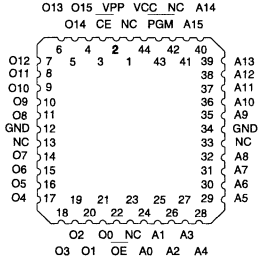
(continued)

Pin Configurations

Pin Name	Function
A0 - A15	Addresses
O0 - O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

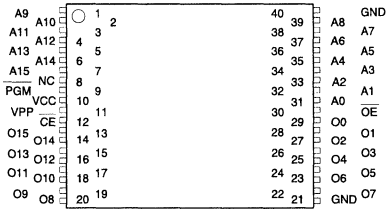
Note: Both GND pins must be connected.

PLCC Top View



Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

TSOP Top View
Type 1



1 Megabit (64K x 16) Unregulated *Battery-Voltage*™ High Speed OTP CMOS EPROM

3

0631A

Description (Continued)

Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 2.7V, any word can be accessed in less than 120 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3V, the AT27BV1024 consumes less than one fifth the power of a standard 5V EPROM.

Standby mode supply current is typically less than 1 µA at 3V. The AT27BV1024 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

The AT27BV1024 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

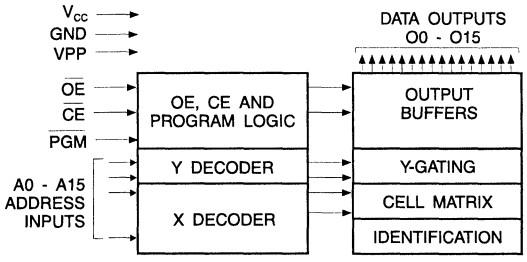
The AT27BV1024 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. At V_{CC} = 2.7V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27BV1024 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV1024 programs exactly the same way as a standard 5V AT27C1024 and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	X (1)	Ai	X	V_{CC} (2)	D_{OUT}
Output Disable (2)	X	V_{IH}	X	X	X	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	X	X (5)	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC} (3)	D_{IN}
PGM Verify (3)	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	X	X	X	V_{PP}	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	X	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A15 = V_{IL}	V_{CC}	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 2.7V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.

DC and AC Operating Conditions for Read Operation

		AT27BV1024		
		-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V - 3.6V	2.7V - 3.6V	2.7V - 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%

= Preliminary Information

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 2.7V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.6V		8	mA
V_{IL}	Input Low Voltage	V_{CC} = 3.0 to 3.6V	-0.6	0.8	V
		V_{CC} = 2.7 to 3.6V	-0.6	0.2 x V_{CC}	V
V_{IH}	Input High Voltage	V_{CC} = 3.0 to 3.6V	2.0	V_{CC} + 0.5	V
		V_{CC} = 2.7 to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
		I_{OL} = 100 µA		0.2	V
		I_{OL} = 20 µA		0.1	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
		I_{OH} = -100 µA	V_{CC} - 0.2		V
		I_{OH} = -20 µA	V_{CC} - 0.1		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation (V_{CC} = 2.7V to 3.6V and 4.5V to 5.5V)

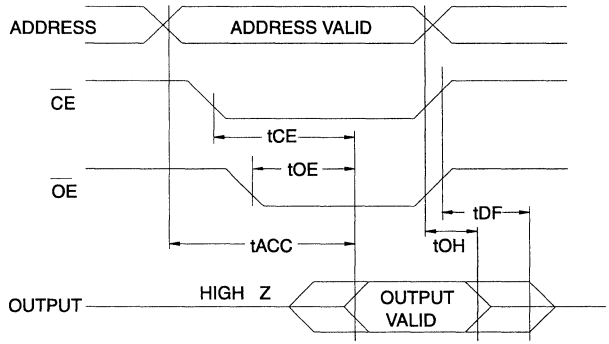
Symbol	Parameter	Condition	AT27BV1024 -90 Min	AT27BV1024 -90 Max	AT27BV1024 -12 Min	AT27BV1024 -12 Max	AT27BV1024 -15 Min	AT27BV1024 -15 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		90		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		90		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		30		35		50	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30		30		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

= Preliminary Information

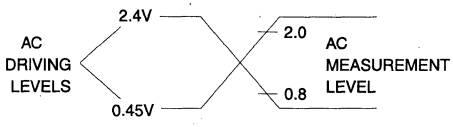
3

AC Waveforms for Read Operation (1)



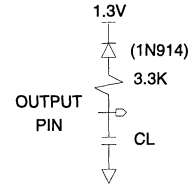
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.
6. When reading a 27BV1024, a 0.1 µF capacitor is required across V_{CC} and ground to supress spurious voltage transients.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



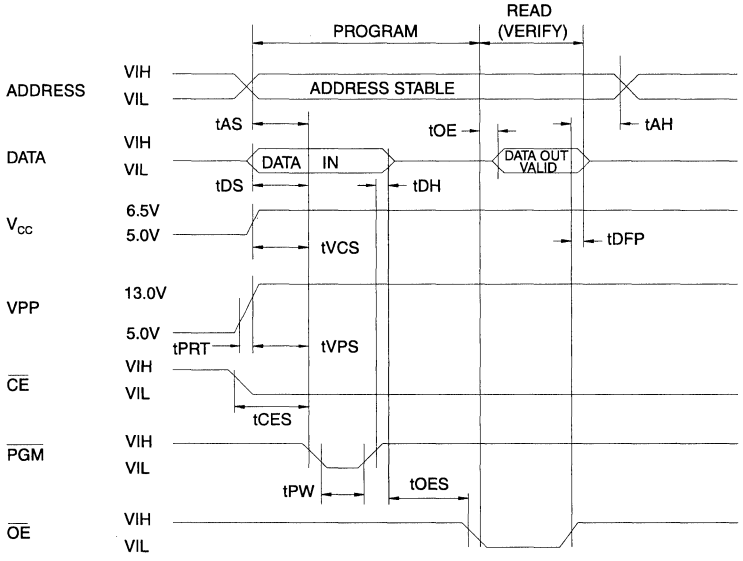
Note: CL = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27BV1024 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels..... 0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

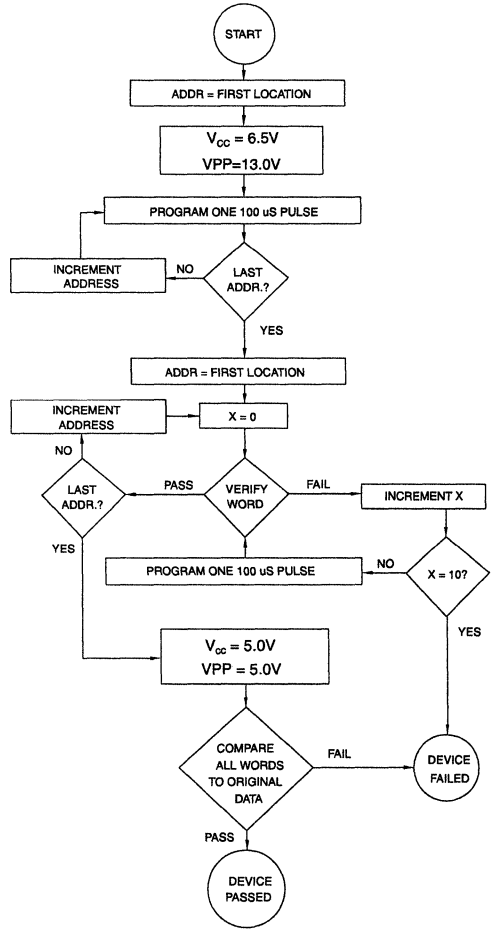
Atmel's 27BV1024 Integrated Product Identification Code (1)

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	0	1	00F1

Note: 1. The AT27BV1024 has the same Product Identification Code as the AT27C1024. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	8	0.02	AT27BV1024-90JC AT27BV1024-90VC	44J 40V	Commercial (0°C to 70°C)
	8	0.02	AT27BV1024-90JI AT27BV1024-90VI	44J 40V	Industrial (-40°C to 85°C)
120	8	0.02	AT27BV1024-12JC AT27BV1024-12VC	44J 40V	Commercial (0°C to 70°C)
	8	0.02	AT27BV1024-12JI AT27BV1024-12VI	44J 40V	Industrial (-40°C to 85°C)
150	8	0.02	AT27BV1024-15JC AT27BV1024-15VC	44J 40V	Commercial (0°C to 70°C)
	8	0.02	AT27BV1024-15JI AT27BV1024-15VI	44J 40V	Industrial (-40°C to 85°C)

= Preliminary Information

3

Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40V	40 Lead, Plastic Thin Small Outline Package (TSOP) 10 x 14 mm

Features

- Fast Read Access Time - 100 ns
- Dual Voltage Range Operation
  - Unregulated Battery Power Supply Range, 2.7V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Compatible with JEDEC Standard AT27C020
- Low Power CMOS Operation
  - 20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- Wide Selection of JEDEC Standard Packages
  - 32-Lead PLCC
  - 32-Lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL and LVBO
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27BV020 is a high performance, low power, low voltage 2,097,152 bit one-time programmable read only memory (OTP EPROM) organized as 256K by 8 bits. It requires only one supply in the range of 2.7 to 3.6V in normal read mode operation, making it ideal for fast, portable systems using either regulated or unregulated battery power.

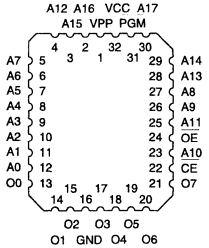
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 2.7V, any byte can be accessed in less than 100 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3V, the AT27BV020 consumes less than one fifth the power of a standard 5V EPROM. Standby mode supply current is typically less than 1 µA at 3V. The AT27BV020 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

(continued)

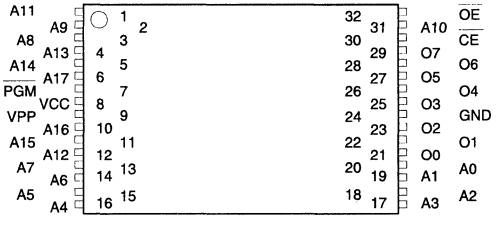
Pin Configurations

Pin Name	Function
A0 - A17	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe

PLCC, Top View



TSOP Top View
Type 1



2 Megabit (256K x 8) Unregulated *Battery-Voltage*™ High Speed OTP CMOS EPROM

3

0345C

Description (Continued)

The AT27BV020 is available in industry standard JEDEC approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

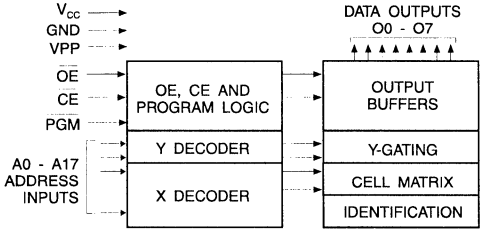
The AT27BV020 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. At V_{CC} = 2.7V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27BV020 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV020 programs exactly the same way as a standard 5V AT27C020 and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	X (1)	Ai	X	V_{CC} (2)	D_{OUT}
Output Disable (2)	X	V_{IH}	X	X	X	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	X	X	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC} (3)	D_{IN}
PGM Verify (3)	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	X	X	X	V_{PP}	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	X	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A17 = V_{IL}	X	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 2.7V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27BV020		
		-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%

= Preliminary Information

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 2.7V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.6V		8	mA
V_{IL}	Input Low Voltage	V_{CC} = 3.0 to 3.6V	-0.6	0.8	V
		V_{CC} = 2.7 to 3.6V	-0.6	0.2 x V_{CC}	V
V_{IH}	Input High Voltage	V_{CC} = 3.0 to 3.6V	2.0	V_{CC} + 0.5	V
		V_{CC} = 2.7 to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
		I_{OL} = 100 µA		0.2	V
		I_{OL} = 20 µA		0.1	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
		I_{OH} = -100 µA	V_{CC} - 0.2		V
		I_{OH} = -20 µA	V_{CC} - 0.1		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		25	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

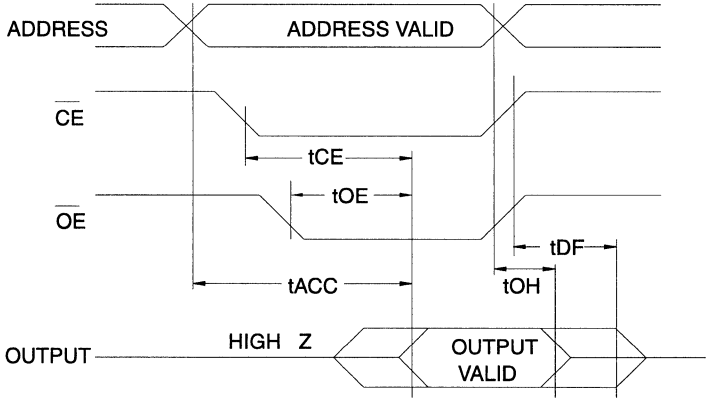
AC Characteristics for Read Operation (V_{CC} = 2.7V to 3.6V and 4.5V to 5.5V)

Symbol	Parameter	Condition	AT27BV020 -10 Min	AT27BV020 -10 Max	AT27BV020 -12 Min	AT27BV020 -12 Max	AT27BV020 -15 Min	AT27BV020 -15 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		100		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		100		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		50		50		60	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		40		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

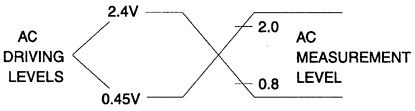
= Preliminary Information

AC Waveforms for Read Operation (1)



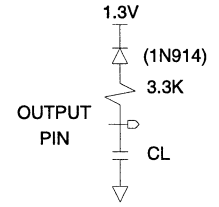
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



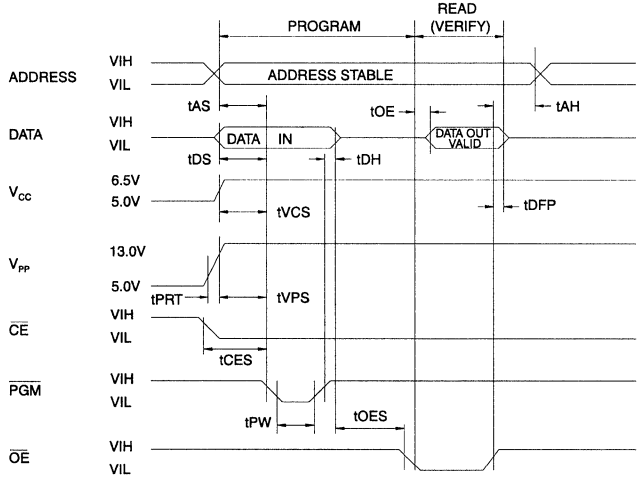
Note: CL = 100 pF
including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27BV020 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (3)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (2)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

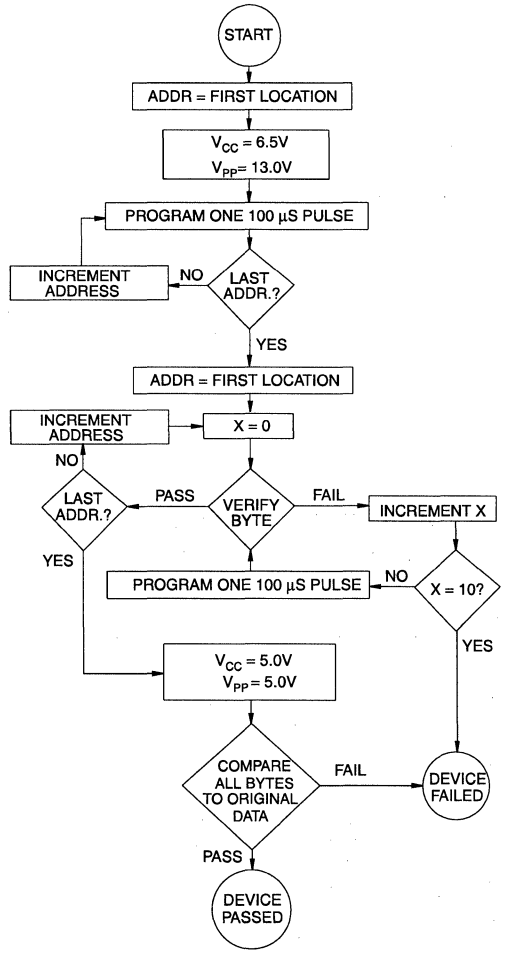
Atmel's 27BV020 Integrated Product Identification Code (1)

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	0	1	1	0	86

Note: 1. The AT27BV020 has the same Product Identification Code as the AT27C020. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.6V		Ordering Code	Package	Operation Range
	Active	Standby			
100	8	0.02	AT27BV020-10JC AT27BV020-10TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27BV020-10JI AT27BV020-10TI	32J 32T	Industrial (-40°C to 85°C)
120	8	0.02	AT27BV020-12JC AT27BV020-12TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27BV020-12JI AT27BV020-12TI	32J 32T	Industrial (-40°C to 85°C)
150	8	0.02	AT27BV020-15JC AT27BV020-15TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27BV020-15JI AT27BV020-15TI	32J 32T	Industrial (-40°C to 85°C)

□ = Preliminary Information

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Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 120 ns
- Dual Voltage Range Operation
  - Unregulated Battery Power Supply Range, 2.7V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Compatible with JEDEC Standard AT27C040
- Low Power CMOS Operation
  - 20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Packages
  - 32-Lead PLCC
  - 32-Lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL and LVBO
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27BV040 chip is a high performance, low power, low voltage, 4,194,304 bit one-time programmable read only memory (EPROM) organized as 512K by 8 bits. It requires only one supply in the range of 2.7 to 3.6V in normal read mode operation, making it ideal for fast, portable systems using either regulated or unregulated battery power.

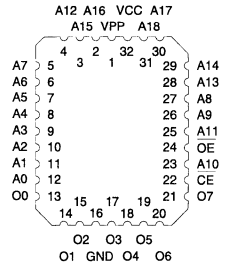
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 2.7V, any byte can be accessed in less than 100 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3V, the AT27BV040 consumes less than one fifth the power of a standard 5V EPROM. Standby mode supply current is typically less than 1 µA at 3V. The AT27BV040 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

(continued)

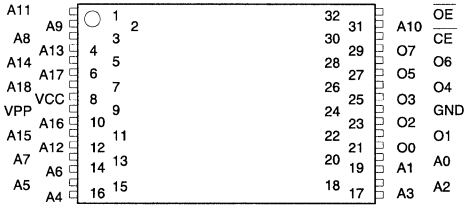
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

PLCC Top View



TSOP Top View
Type 1



4 Megabit (512K x 8) Unregulated *Battery-Voltage*™ High Speed OTP CMOS EPROM

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0346C

Description (Continued)

The AT27BV040 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

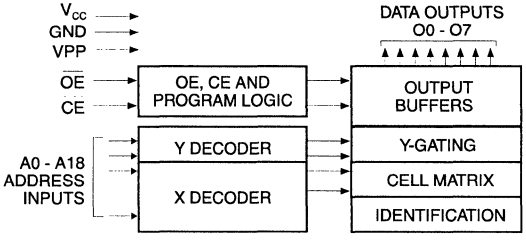
The AT27BV040 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. At V_{CC} = 2.7V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27BV040 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV040 programs exactly the same way as a standard 5V AT27C040 and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	Ai	X (1)	V_{CC} (2)	D_{OUT}
Output Disable (2)	X	V_{IH}	X	X	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	X	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (3)	D_{IN}
PGM Verify (3)	X	V_{IL}	Ai	V_{PP}	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A18 = V_{IL}	X	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 2.7V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27BV040	
		-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V
		5V ± 10%	5V ± 10%

= Preliminary Information

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 2.7V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.6V		8	mA
V_{IL}	Input Low Voltage	V_{CC} = 3.0 to 3.6V	-0.6	0.8	V
		V_{CC} = 2.7 to 3.6V	-0.6	0.2 x V_{CC}	V
V_{IH}	Input High Voltage	V_{CC} = 3.0 to 3.6V	2.0	V_{CC} + 0.5	V
		V_{CC} = 2.7 to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
		I_{OL} = 100 µA		0.2	V
		I_{OL} = 20 µA		0.1	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
		I_{OH} = -100 µA	V_{CC} - 0.2		V
		I_{OH} = -20 µA	V_{CC} - 0.1		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation (V_{CC} = 2.7V to 3.6V and 4.5V to 5.5V)

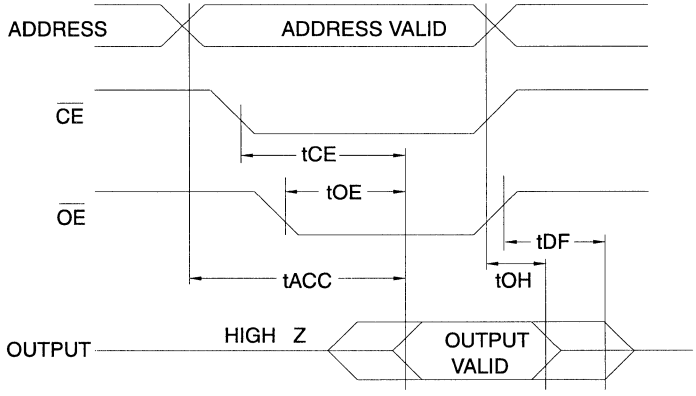
Symbol	Parameter	Condition	AT27BV040 -12 Min	AT27BV040 -12 Max	AT27BV040 -15 Min	AT27BV040 -15 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		50		60	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

= Preliminary Information

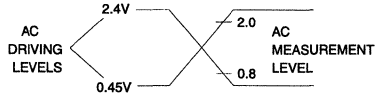
3

AC Waveforms for Read Operation (1)



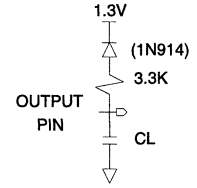
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



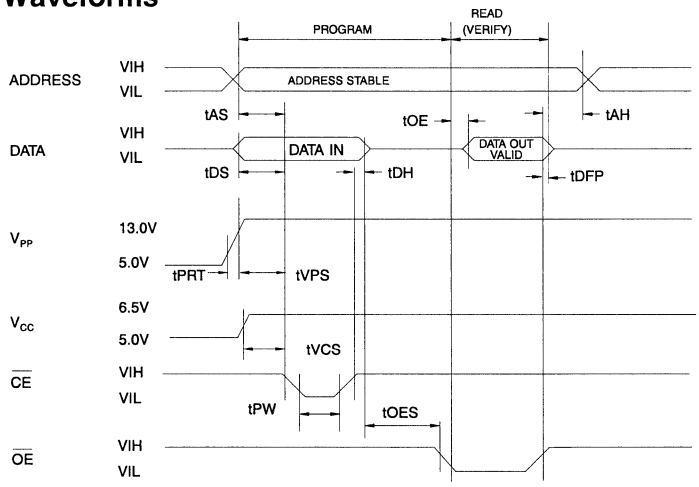
Note: CL = 100 pF
including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27BV040 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.7	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$ (2)			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

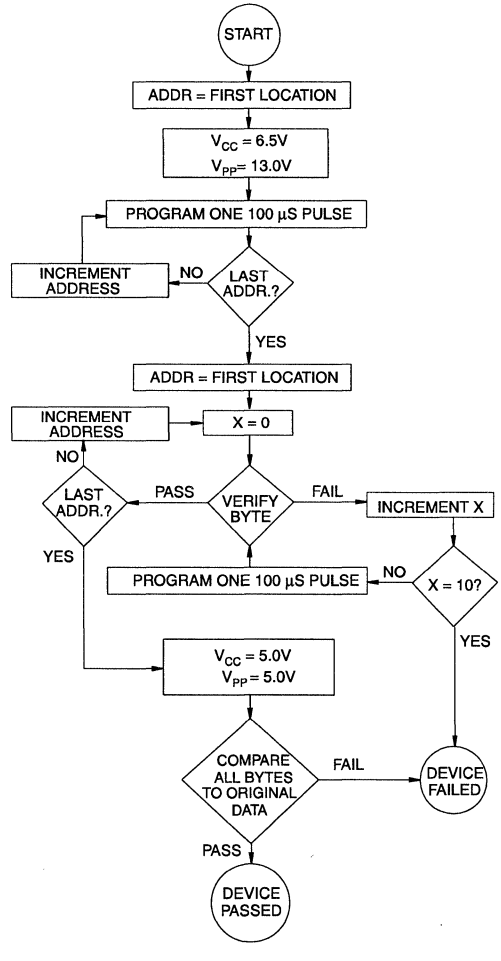
Atmel's 27BV040 Integrated Product Identification Code (1)

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

Note: 1. The AT27BV040 has the same Product Identification Code as the AT27C040. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.6V		Ordering Code	Package	Operation Range
	Active	Standby			
120	8	0.02	AT27BV040-12JC AT27BV040-12TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27BV040-12JI AT27BV040-12TI	32J 32T	Industrial (-40°C to 85°C)
150	8	0.02	AT27BV040-15JC AT27BV040-15TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27BV040-15JI AT27BV040-15TI	32J 32T	Industrial (-40°C to 85°C)

= Preliminary Information

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

4 Megabit (256K x 16) Unregulated *Battery-Voltage*™ High Speed OTP CMOS EPROM

Features

- Fast Read Access Time - 120 ns
- Dual Voltage Range Operation
  - Unregulated Battery Power Supply Range, 2.7V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Pin Compatible with JEDEC Standard AT27C4096
- Low Power CMOS Operation
  - 20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Surface Mount Packages
  - 44-Lead PLCC
  - 40-Lead TSOP (10 x 14mm)
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming algorithm - 100 µs/word (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL and LVBO
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27BV4096 is a high performance, low power, low voltage 4,194,304 bit one-time programmable read only memory (OTP EPROM) organized as 256K by 16 bits. It requires only one supply in the range of 2.7V to 3.6V in normal read mode operation. The by-16 organization makes this part ideal for portable and handheld 16 and 32 bit microprocessor based systems using either regulated or unregulated battery power.

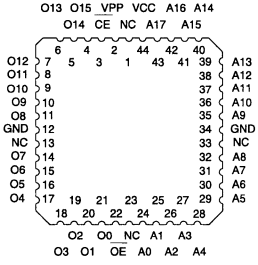
(continued)

Pin Configurations

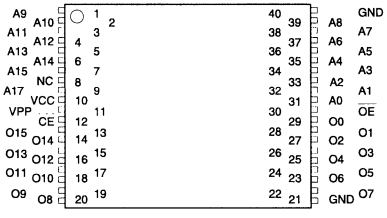
Pin Name	Function
A0 - A17	Addresses
O0 - O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

Note: Both GND pins must be connected.

PLCC Top View



TSOP Top View
Type 1



Note: 1. PLCC package pins 1 and 23 are DON'T CONNECT.

0640A

Description (Continued)

Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 2.7V, any word can be accessed in less than 120 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3V, the AT27BV4096 consumes less than one fifth the power of a standard 5V EPROM.

Standby mode supply current is typically less than 1 µA at 3V. The AT27BV4096 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

The AT27BV4096 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

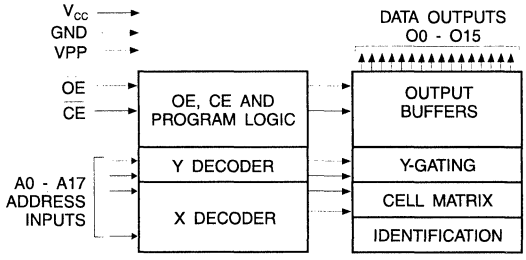
The AT27BV4096 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. At V_{CC} = 2.7V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27BV4096 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV4096 programs exactly the same way as a standard 5V AT27C4096 and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	Ai	X (1)	V_{CC} (2)	D_{OUT}
Output Disable (2)	X	V_{IH}	X	X	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	X (5)	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (3)	D_{IN}
PGM Verify (3)	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A17 = V_{IL}	V_{CC}	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 2.7V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.

DC and AC Operating Conditions for Read Operation

		AT27BV4096	
		-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V - 3.6V	2.7V - 3.6V
		5V ± 10%	5V ± 10%

= Preliminary Information

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 2.7V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.6V		8	mA
V_{IL}	Input Low Voltage	V_{CC} = 3.0 to 3.6V	-0.6	0.8	V
		V_{CC} = 2.7 to 3.6V	-0.6	0.2 x V_{CC}	V
V_{IH}	Input High Voltage	V_{CC} = 3.0 to 3.6V	2.0	V_{CC} + 0.5	V
		V_{CC} = 2.7 to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
		I_{OL} = 100 µA		0.2	V
		I_{OL} = 20 µA		0.1	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
		I_{OH} = -100 µA	V_{CC} - 0.2		V
		I_{OH} = -20 µA	V_{CC} - 0.1		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		40	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation (V_{CC} = 2.7V to 3.6V and 4.5V to 5.5V)

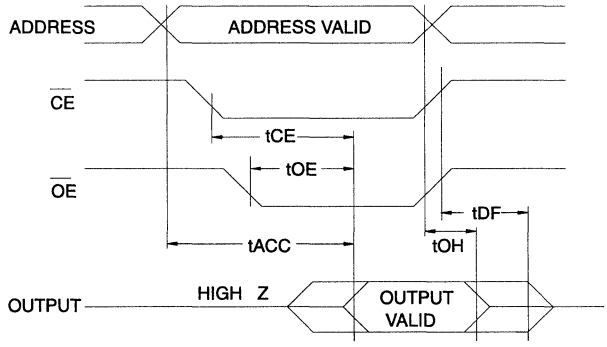
Symbol	Parameter	Condition	AT27BV4096 -12 Min	AT27BV4096 -12 Max	AT27BV4096 -15 Min	AT27BV4096 -15 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		35		50	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

= Preliminary Information

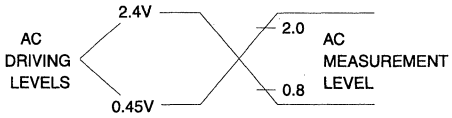
3

AC Waveforms for Read Operation (1)



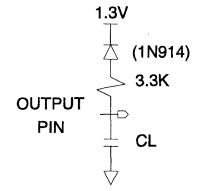
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.
6. When reading a 27BV4096, a 0.1 µF capacitor is required across V_{CC} and ground to supress spurious voltage transients.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



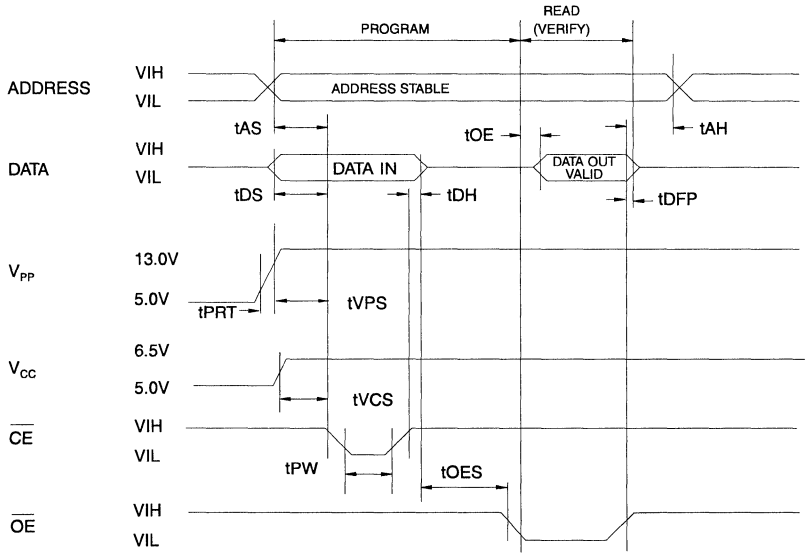
Note: CL = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27BV4096 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (3)		47.5	52.5	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels..... 0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 50 µsec ± 5%.

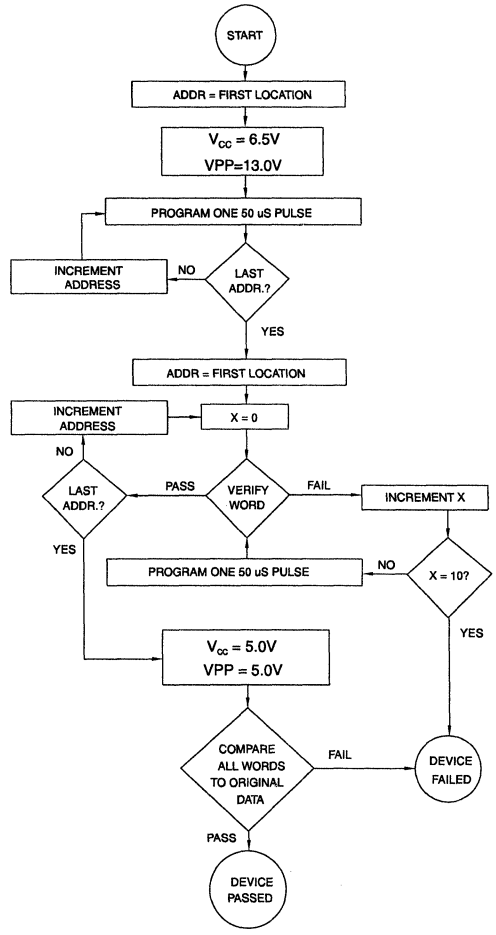
Atmel's 27BV4096 Integrated Product Identification Code (1)

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	1	0	0	00F4

Note: 1. The AT27BV4096 has the same Product Identification Code as the AT27C4096. Both are programming compatible.

Rapid Programming Algorithm

A 50 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{CE}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	8	0.02	AT27BV4096-12JC AT27BV4096-12VC	44J 40V	Commercial (0°C to 70°C)
	8	0.02	AT27BV4096-12JI AT27BV4096-12VI	44J 40V	Industrial (-40°C to 85°C)
150	8	0.02	AT27BV4096-15JC AT27BV4096-15VC	44J 40V	Commercial (0°C to 70°C)
	8	0.02	AT27BV4096-15JI AT27BV4096-15VI	44J 40V	Industrial (-40°C to 85°C)

= Preliminary Information

3

Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40V	40 Lead, Plastic Thin Small Outline Package (TSOP) 10 x 14 mm

The Atmel 3-Volt EPROM Family

Low Voltage OTP CMOS EPROM

- Why 3-volt operation?
- Does the whole system have to be operated at 3 volts?
- How do you program a 3-volt EPROM?
- What happens if you run a 3-volt device at 3.6 volts?

The Atmel AT27LVXXX series of EPROMs was designed to operate over a wide range of supply voltages from 3.0 to 3.6 volts. This offers the designer the opportunity to take advantage of the greatly reduced power consumption at 3 volts.

The 3-volt series of EPROMs is specified to draw a maximum of 8.0 mA at 5.0 MHz when operated at 3.6VDC. This is less than half of the specified maximum current of a standard EPROM operating at 5.0VDC. Because of the low supply voltage, the power savings calculations are even more dramatic: 29 mW for the LV series compared to 165 mW (5.5V @ 30 mA; i.e. 27C040) for standard five-volt devices. That means much longer battery life.

The LV series has CMOS inputs and outputs specified for TTL levels and 3-volt CMOS levels (Rail-to-Rail). In other words, an LV device with V_{CC} = 3.0VDC can drive standard 5-volt TTL logic devices on its data output lines making interface with 5-volt logic easy. The LV series of EPROMs can even be safely driven by 5-volt signals, even though their V_{CC} is at 3.0VDC (please refer to application note *Interfacing Atmel LV EPROMs on a Mixed Three-Volt/Five-Volt Data Bus*, this chapter). The next question that comes to mind is "Why run just one EPROM at 3 volts while the rest of the system uses 5 volts?" One reason is if your system is on a very tight power budget, such as battery operated equipment, daughter boards or phone line powered products, the **six times** power savings might make a significant difference. Of course your design might use more than one EPROM, for map memory, operating system, font storage or maybe smart cards. In this case the total power savings can be very large. Remember at 165 mW each, 8 EPROMs at 5 volts use 1.3 Watts instead of 235 mW for the 3-volt devices!

When the 3-volt devices are in a programmer they work just like their standard Atmel 5-volt counterparts. Absolutely no difference! Programming support is already in place and widely available on most programmers on the market today.

The AT27LVXXX series of EPROMs are specified to operate from 3.0 to 3.6 volts. So what happens when the device is operated above 3 volts? It speeds up and draws more power, but never more than a standard EPROM. This feature offers the most flexibility for system manufacturers.

0546A

256K (32K x 8) Low Voltage OTP CMOS EPROM

Features

- Fast Read Access Time - 70 ns
- Dual Voltage Range Operation
  - Low Voltage Power Supply Range, 3.0V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Pin Compatible with JEDEC Standard AT27C256
- Low Power CMOS Operation
  - 20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Packages
  - 32-Lead PLCC
  - 28-Lead 330-mil SOIC
  - 28-Lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27LV256A is a high performance, low power, low voltage 262,144 bit one-time programmable read only memory (OTP EPROM) organized as 32K by 8 bits. It requires only one supply in the range of 3.0V to 3.6V in normal read mode operation, making it ideal for fast, portable systems using battery power.

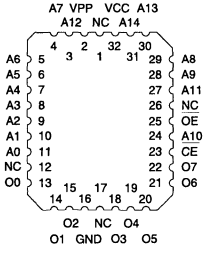
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3.3V supply. At V_{CC} = 3.0V, any byte can be accessed in less than 70 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3.3V, the AT27LV256A consumes less than one fifth the power of a standard 5V EPROM.

(continued)

Pin Configurations

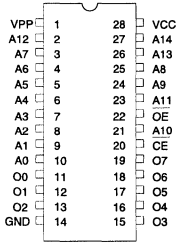
Pin Name	Function
A0 - A14	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

PLCC Top View



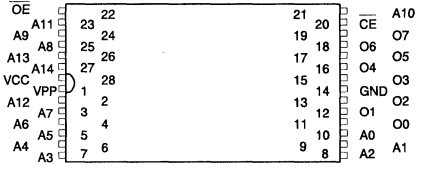
Note:PLCC Package Pins 1 and 17 are DON'T CONNECT.

SOIC Top View



TSOP Top View

Type 1



0547A

Description (Continued)

Standby mode supply current is typically less than 1 µA at 3.3V.

The AT27LV256A is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC, SOIC and TSOP packages . All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

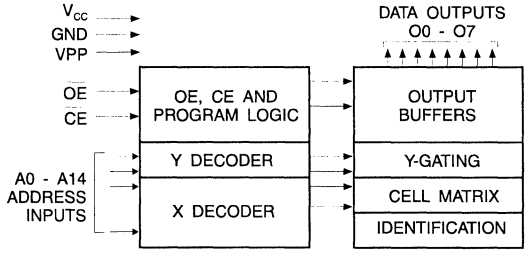
The AT27LV256A operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27LV256A has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV256A programs exactly the same way as a standard 5V AT27C256R and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 volts for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC} (2)	D_{OUT}
Output Disable (2)	V_{IL}	V_{IH}	X (1)	V_{CC}	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X (1)	X (1)	V_{CC}	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (3)	D_{IN}
PGM Verify (3)	X (1)	V_{IL}	Ai	V_{PP}	V_{CC} (3)	D_{OUT}
Optional PGM Verify (3)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	V_{IH}	X (1)	V_{PP}	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A14 = V_{IL}	V_{CC}	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 3.0V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27LV256A			
		-70	-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0V to 3.6V	3.0V to 3.6V	3.0V to 3.6V	3.0V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 3.0V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		8	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0 .5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		20	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

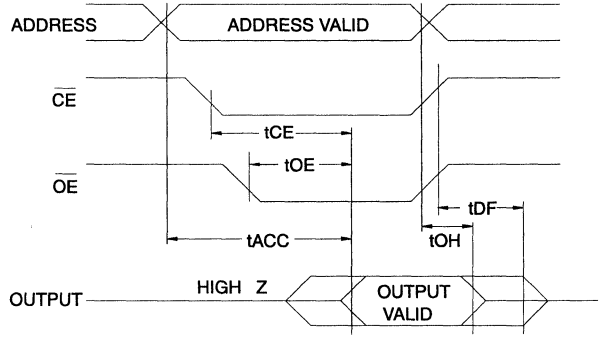
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation (V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V)

Symbol	Parameter	Condition	AT27LV256A -70 Min	-70 Max	-90 Min	-90 Max	-12 Min	-12 Max	-15 Min	-15 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		50		50		50		60	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		40		40		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		0		0		ns

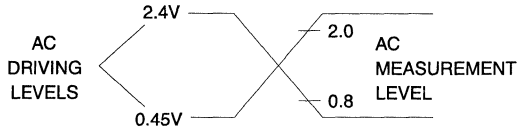
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

AC Waveforms for Read Operation (1)



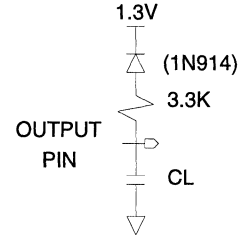
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



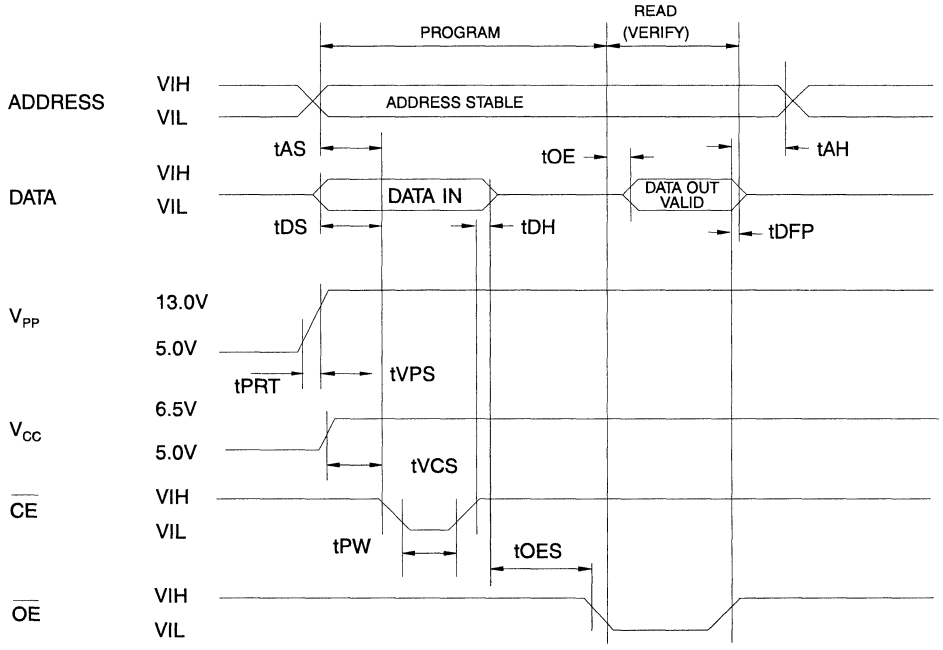
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV256A a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

TA = 25 ± 5°C, VCC = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$ (2)			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

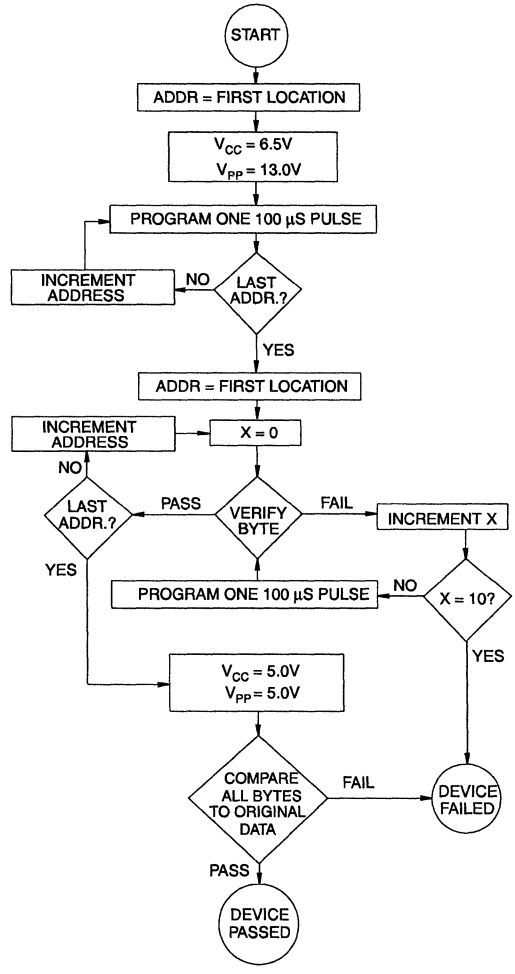
Atmel's 27LV256A Integrated Product Identification Code (1)

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Note: 1. The AT27LV256A has the same Product Identification Code as the AT27C256R. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	8	0.02	AT27LV256A-70JC AT27LV256A-70RC AT27LV256A-70TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27LV256A-70JI AT27LV256A-70RI AT27LV256A-70TI	32J 28R 28T	Industrial (-40°C to 85°C)
90	8	0.02	AT27LV256A-90JC AT27LV256A-90RC AT27LV256A-90TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27LV256A-90JI AT27LV256A-90RI AT27LV256A-90TI	32J 28R 28T	Industrial (-40°C to 85°C)
120	8	0.02	AT27LV256A-12JC AT27LV256A-12RC AT27LV256A-12TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27LV256A-12JI AT27LV256A-12RI AT27LV256A-12TI	32J 28R 28T	Industrial (-40°C to 85°C)
150	8	0.02	AT27LV256A-15JC AT27LV256A-15RC AT27LV256A-15TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27LV256A-15JI AT27LV256A-15RI AT27LV256A-15TI	32J 28R 28T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

512K (64K x 8) Low Voltage OTP CMOS EPROM

Features

- Fast Read Access Time - 90 ns
- Dual Voltage Range Operation
  - Low Voltage Power Supply Range, 3.0V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Compatible with JEDEC Standard AT27C512
- Low Power CMOS Operation
  - 20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Packages
  - 32-Lead PLCC
  - 28-Lead 330-mil SOIC
  - 28-Lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27LV512A is a high performance, low power, low voltage 524,288 bit one-time programmable read only memory (OTP EPROM) organized as 64K by 8 bits. It requires only one supply in the range of 3.0V to 3.6V in normal read mode operation, making it ideal for fast, portable systems using battery power.

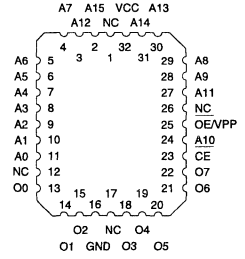
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3.3V supply. At V_{CC} = 3.0V, any byte can be accessed in less than 90 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3.3V, the AT27LV512A consumes less than one fifth the power of a standard 5V EPROM.

(continued)

Pin Configurations

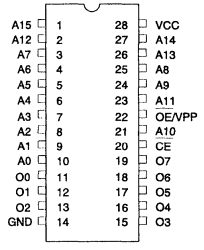
Pin Name	Function
A0 - A15	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable
NC	No Connect

PLCC Top View



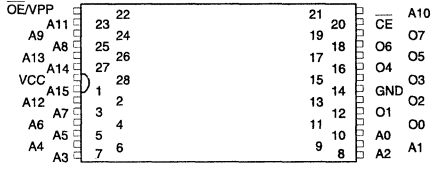
Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

SOIC Top View



TSOP Top View

Type 1



0607A

Description (Continued)

Standby mode supply current is typically less than 1 µA at 3.3V.

The AT27LV512A is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC, SOIC, and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

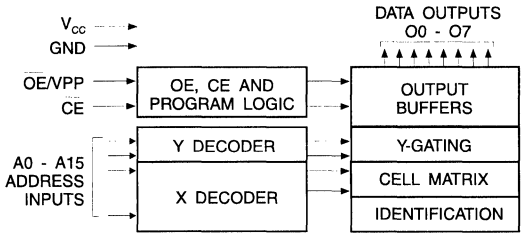
The AT27LV512A operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27LV512A has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV512A programs exactly the same way as a standard 5V AT27C512R and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 volts for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	Ai	V_{CC} (2)	D_{OUT}
Output Disable (2)	V_{IL}	V_{IH}	X (1)	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{PP}	Ai	V_{CC} (3)	D_{IN}
PGM Inhibit (3)	V_{IH}	V_{PP}	X	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A15 = V_{IL}	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 3.0V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27LV512A		
		-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0V to 3.6V	3.0V to 3.6V	3.0V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 3.0V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		8	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0 .5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		20	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

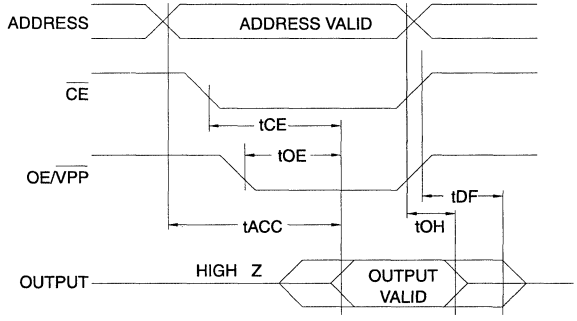
Note: 1. V_{CC} must be applied simultaneously with or before $\overline{OE}/V_{PP}$, and removed simultaneously with or after $\overline{OE}/V_{PP}$.

AC Characteristics for Read Operation (V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V)

Symbol	Parameter	Condition	-90 Min	-90 Max	-12 Min	-12 Max	-15 Min	-15 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}		90		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$ = V_{IL}		90		120		150	ns
t_{OE} (2, 3)	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$ = V_{IL}		50		50		60	ns
t_{DF} (4, 5)	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		40		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first		0		0		0		ns

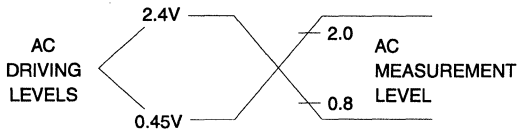
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

AC Waveforms for Read Operation (1)



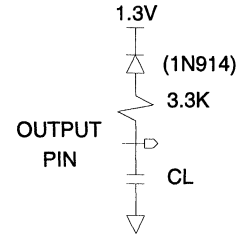
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



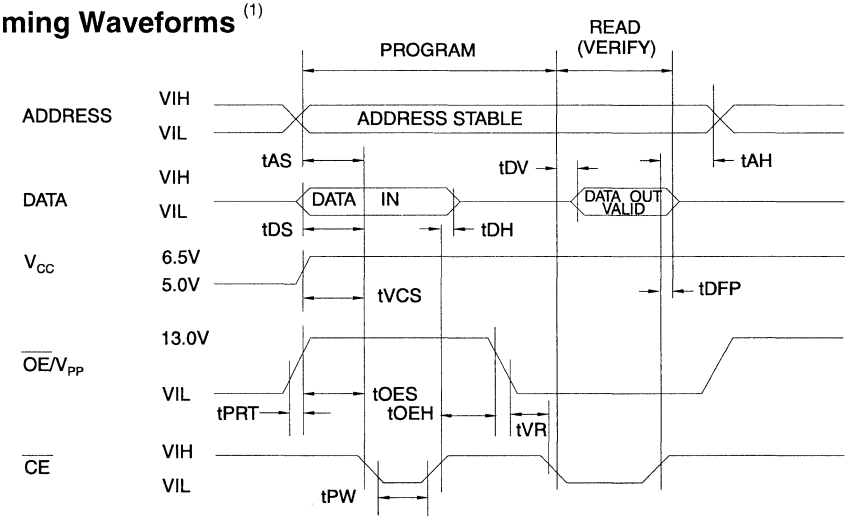
Note: CL = 100 pF
including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, $\overline{OE}/V_{PP}$ = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, $\overline{OE}/V_{PP}$ = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay (2)		0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		95	105	µs
t_{DV}	Data Valid from $\overline{CE}$ (2)			1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

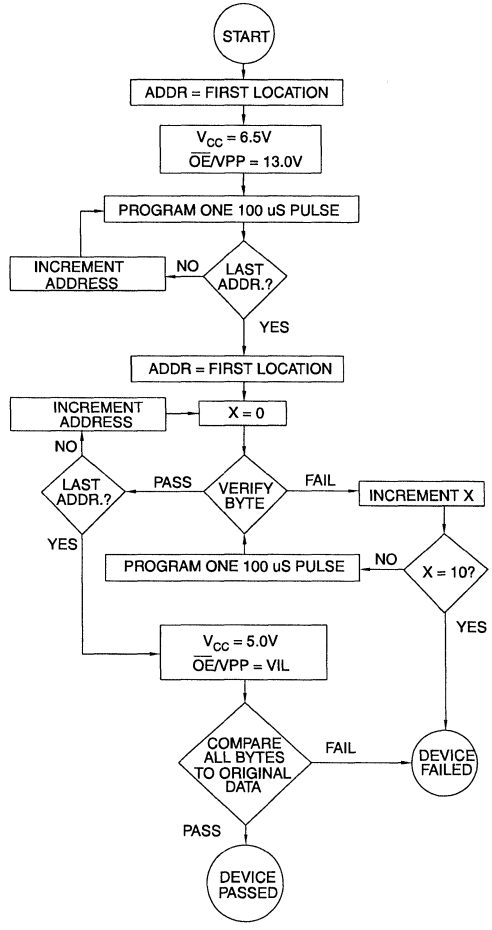
Atmel's 27LV512A Integrated Product Identification Code (1)

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	0D

Note: 1. The AT27LV512A has the same Product Identification Code as the AT27C512R. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	8	0.02	AT27LV512A-90JC AT27LV512A-90RC AT27LV512A-90TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27LV512A-90JI AT27LV512A-90RI AT27LV512A-90TI	32J 28R 28T	Industrial (-40°C to 85°C)
120	8	0.02	AT27LV512A-12JC AT27LV512A-12RC AT27LV512A-12TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27LV512A-12JI AT27LV512A-12RI AT27LV512A-12TI	32J 28R 28T	Industrial (-40°C to 85°C)
150	8	0.02	AT27LV512A-15JC AT27LV512A-15RC AT27LV512A-15TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27LV512A-15JI AT27LV512A-15RI AT27LV512A-15TI	32J 28R 28T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 90 ns
- Dual Voltage Range Operation
  - Low Voltage Power Supply Range, 3.0V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Compatible with JEDEC Standard AT27C010
- Low Power CMOS Operation
  - 20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Packages
  - 32-Lead PLCC
  - 32-Lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

1 Megabit (128K x 8) Low Voltage OTP CMOS EPROM

3

Description

The AT27LV010A is a high performance, low power, low voltage 1,048,576 bit one-time programmable read only memory (OTP EPROM) organized as 128K by 8 bits. It requires only one supply in the range of 3.0V to 3.6V in normal read mode operation, making it ideal for fast, portable systems using battery power.

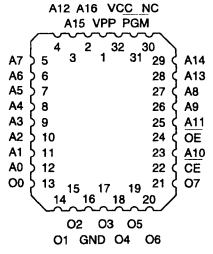
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3.3V supply. At V_{CC} = 3.0V, any byte can be accessed in less than 90 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3.3V, the AT27LV010A consumes less than one fifth the power of a standard 5V EPROM. Standby mode supply current is typically less than 1 µA at 3.3V.

(continued)

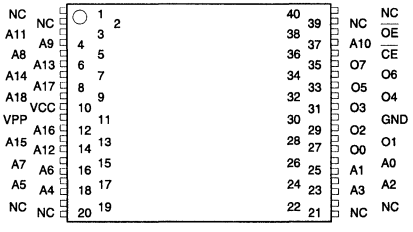
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

PLCC Top View



TSOP Top View
Type 1



0548A

Description (Continued)

The AT27LV010A is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

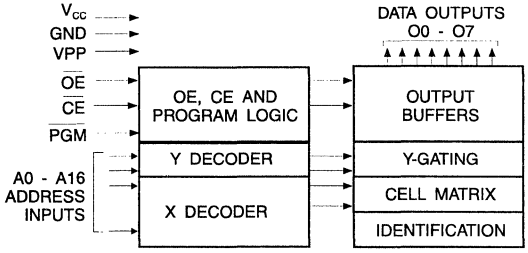
The AT27LV010A operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27LV010A has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV010A programs exactly the same way as a standard 5V AT27C010 and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 volts for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	X (1)	Ai	X	V_{CC} (2)	D_{OUT}
Output Disable (2)	X	V_{IH}	X	X	X	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	X	X	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC} (3)	D_{IN}
PGM Verify (3)	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	X	X	X	V_{PP}	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	X	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A16 = V_{IL}	X	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 3.0V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27LV010A		
		-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0V to 3.6V	3.0V to 3.6V	3.0V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 3.0V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		8	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0 .5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		25	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

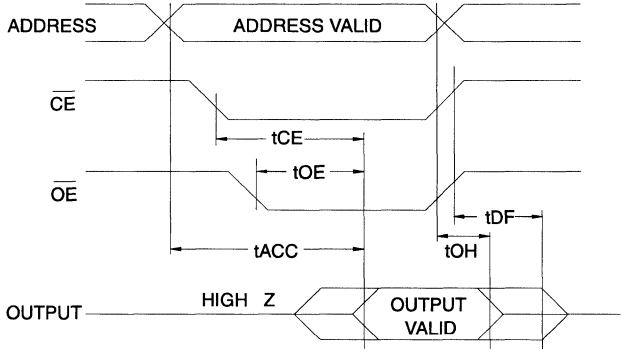
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation (V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V)

			AT27LV010A						
			-90		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		90		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		90		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		50		50		60	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		40		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		0		ns

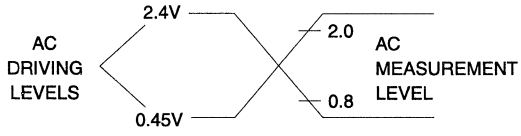
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

AC Waveforms for Read Operation (1)



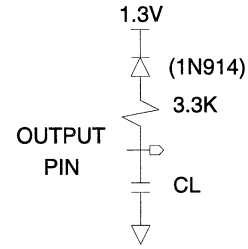
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



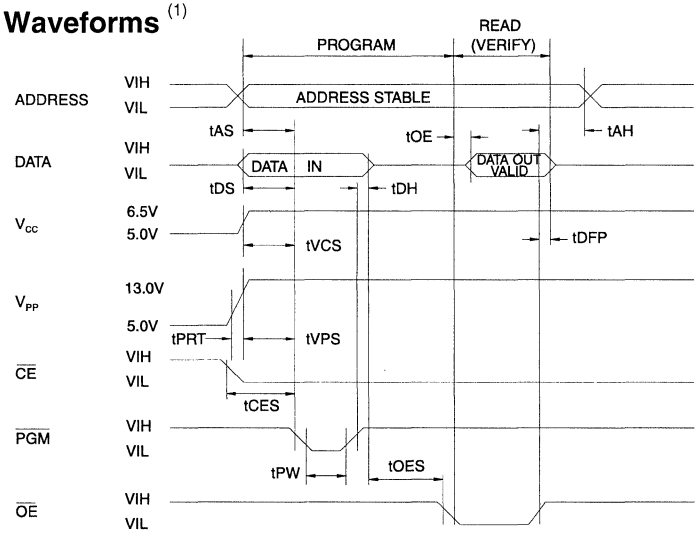
Note: CL = 100 pF
including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV010A a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.2V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

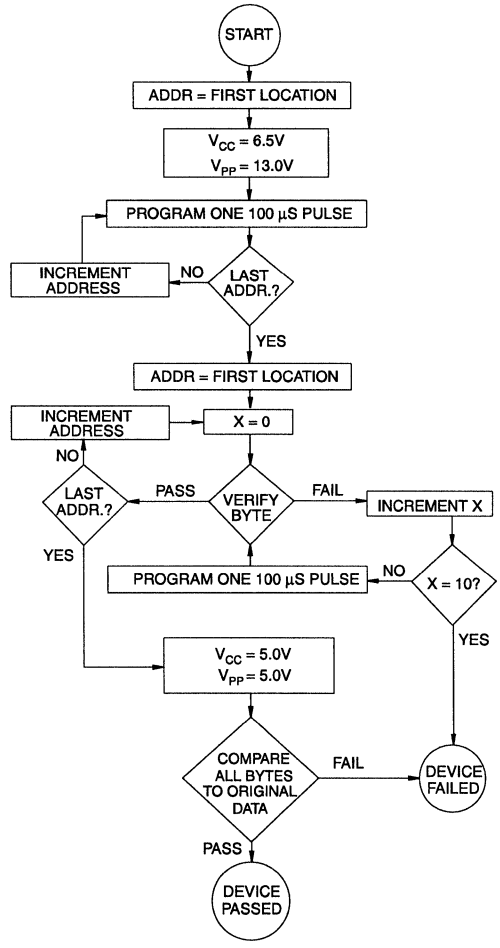
Atmel's 27LV010A Integrated Product Identification Code (1)

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	05

Note: 1. The AT27LV010A has the same Product Identification Code as the AT27C010. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.6V		Ordering Code	Package	Operation Range
	Active	Standby			
90	8	0.02	AT27LV010A-90JC AT27LV010A-90TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27LV010A-90JI AT27LV010A-90TI	32J 32T	Industrial (-40°C to 85°C)
120	8	0.02	AT27LV010A-12JC AT27LV010A-12TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27LV010A-12JI AT27LV010A-12TI	32J 32T	Industrial (-40°C to 85°C)
150	8	0.02	AT27LV010A-15JC AT27LV010A-15TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27LV010A-15JI AT27LV010A-15TI	32J 32T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 100 ns
- Dual Voltage Range Operation
  - Low Voltage Power Supply Range, 3.0V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Compatible with JEDEC Standard AT27C020
- Low Power CMOS Operation
  - 20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Packages
  - 32-Lead PLCC
  - 32-Lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- Two-Line Control
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

2 Megabit (256K x 8) Low Voltage OTP CMOS EPROM

3

Description

The AT27LV020A is a high performance, low power, low voltage 2,097,152 bit one-time programmable read only memory (OTP EPROM) organized as 256K by 8 bits. It requires only one supply in the range of 3.0 to 3.6V in normal read mode operation, making it ideal for fast, portable systems using battery power.

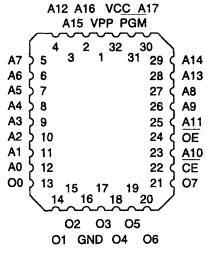
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 3.0V, any byte can be accessed in less than 100 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3.3V, the AT27LV020A consumes less than one fifth the power of a standard 5V EPROM. Standby mode supply current is typically less than 1 µA at 3.3V.

(continued)

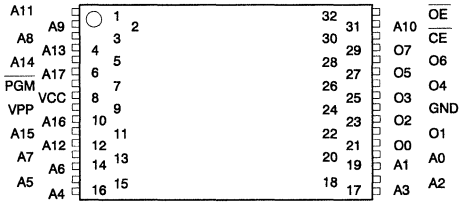
Pin Configurations

Pin Name	Function
A0 - A17	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe

PLCC, Top View



TSOP Top View
Type 1



0549A

Description (Continued)

The AT27LV020A is available in industry standard JEDEC approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

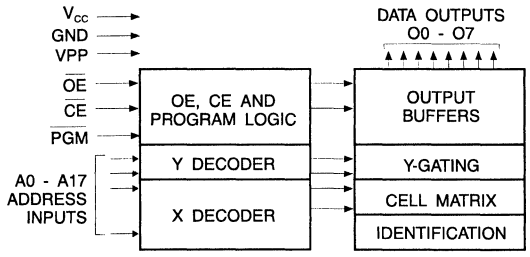
The AT27LV020A operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27LV020A has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV020A programs exactly the same way as a standard 5V AT27C020 and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 volts for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	X (1)	Ai	X	V_{CC} (2)	D_{OUT}
Output Disable (2)	X	V_{IH}	X	X	X	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	X	X	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC} (3)	D_{IN}
PGM Verify (3)	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	X	X	X	V_{PP}	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	X	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A17 = V_{IL}	X	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 3.0V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27LV020A		
		-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0V to 3.6V	3.0V to 3.6V	3.0V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%

= Preliminary Information

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 3.0V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		8	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0 .5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		25	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

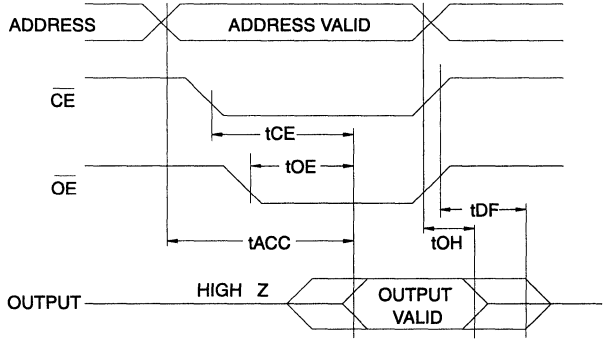
AC Characteristics for Read Operation (V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V)

Symbol	Parameter	Condition	AT27LV020A -10 Min	AT27LV020A -10 Max	AT27LV020A -12 Min	AT27LV020A -12 Max	AT27LV020A -15 Min	AT27LV020A -15 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		100		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		100		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		50		50		60	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		40		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

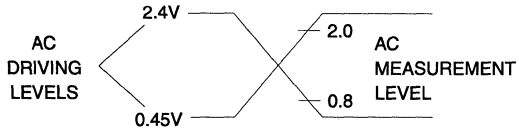
= Preliminary Information

AC Waveforms for Read Operation (1)



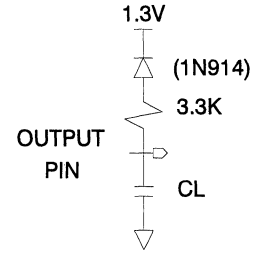
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. OE may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



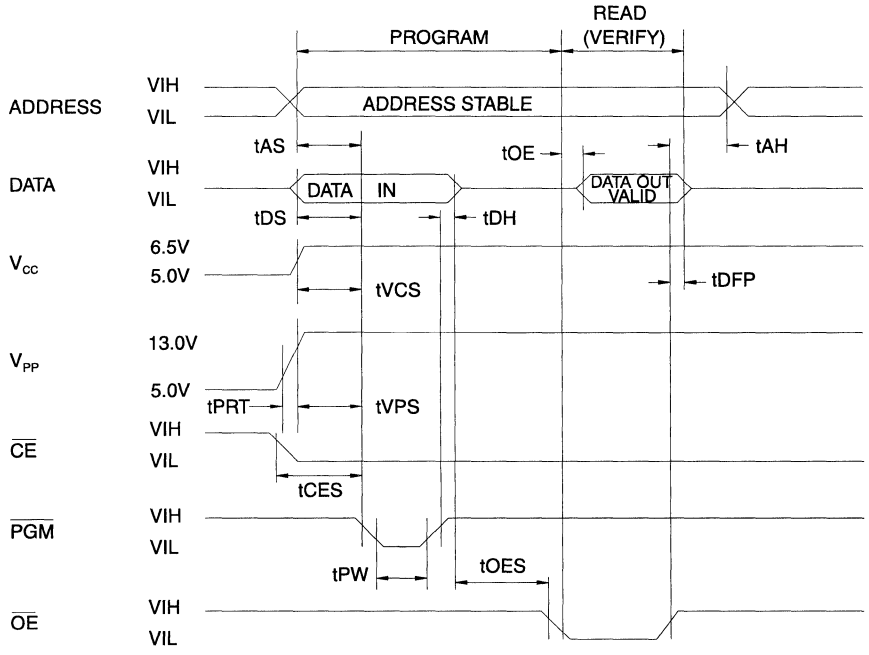
Note: CL = 100 pF
including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV020A a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Sym-bol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

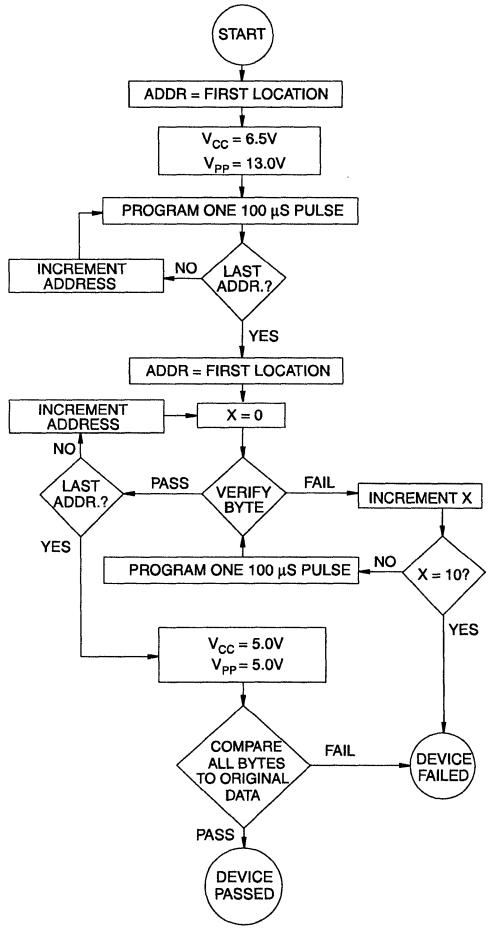
Atmel's 27LV020A Integrated Product Identification Code (1)

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	0	1	1	0	86

Note: 1. The AT27LV020A has the same Product Identification Code as the AT27C020. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	Icc (mA) Vcc = 3.6V		Ordering Code	Package	Operation Range
	Active	Standby			
100	8	0.02	AT27LV020A-10JC AT27LV020A-10TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27LV020A-10JI AT27LV020A-10TI	32J 32T	Industrial (-40°C to 85°C)
120	8	0.02	AT27LV020A-12JC AT27LV020A-12TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27LV020A-12JI AT27LV020A-12TI	32J 32T	Industrial (-40°C to 85°C)
150	8	0.02	AT27LV020A-15JC AT27LV020A-15TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27LV020A-15JI AT27LV020A-15TI	32J 32T	Industrial (-40°C to 85°C)

= Preliminary Information

3

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 120 ns
- Dual Voltage Range Operation
  - Low Voltage Power Supply Range, 3.0V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Compatible With JEDEC Standard AT27C040
- Low Power 3.3-volt CMOS Operation
  - 20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
  - 29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Packages
  - 32-Lead PLCC
  - 32-Lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

4 Megabit (512K x 8) Low Voltage OTP CMOS EPROM

3

Description

The AT27LV040A is a high performance, low power, low voltage, 4,194,304 bit one-time programmable read only memory (OTP EPROM) organized as 512K by 8 bits. It requires only one supply in the range of 3.0 to 3.6V in normal read mode operation, making it ideal for fast, portable systems using battery power.

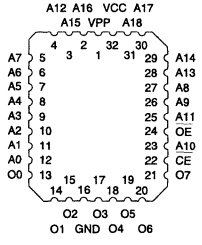
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 3.0V, any byte can be accessed in less than 120 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3.3V, the AT27LV040A consumes less than one half the power of a standard 5V EPROM. Standby mode supply current is typically less than 1 µA at 3.3V.

(continued)

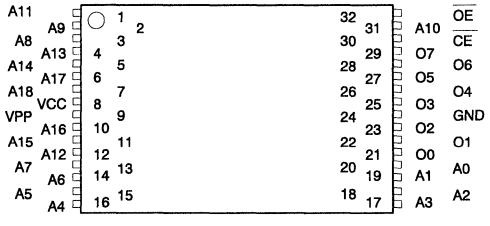
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

PLCC Top View



TSOP Top View
Type 1



0557A

Description (Continued)

The AT27LV040A is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

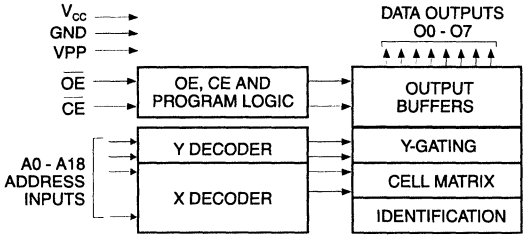
The AT27LV040A operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27LV040A has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV040A programs exactly the same way as a standard 5V AT27C040 and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 volts for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read (2)	V_{IL}	V_{IL}	Ai	X (1)	V_{CC} (2)	D_{OUT}
Output Disable (2)	X	V_{IH}	X	X	V_{CC} (2)	High Z
Standby (2)	V_{IH}	X	X	X	V_{CC} (2)	High Z
Rapid Program (3)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (3)	D_{IN}
PGM Verify (3)	X	V_{IL}	Ai	V_{PP}	V_{CC} (3)	D_{OUT}
PGM Inhibit (3)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC} (3)	High Z
Product Identification (3, 5)	V_{IL}	V_{IL}	A9 = V_H (4) A0 = V_{IH} or V_{IL} A1 - A18 = V_{IL}	X	V_{CC} (3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Read, output disable, and standby modes require, 3.0V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27LV040A	
		-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0V to 3.6V	3.0V to 3.6V
		5V ± 10%	5V ± 10%

= Preliminary Information

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 3.0V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		8	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0 .5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

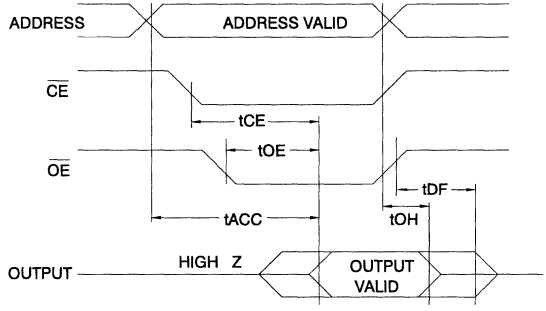
AC Characteristics for Read Operation (V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V)

Symbol	Parameter	Condition	AT27LV040A -12 Min	AT27LV040A -12 Max	AT27LV040A -15 Min	AT27LV040A -15 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		50		60	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

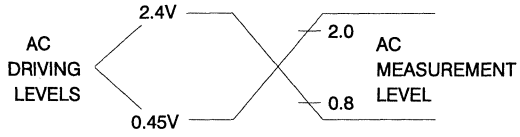
= Preliminary Information

AC Waveforms for Read Operation (1)



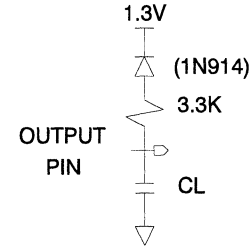
Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveform and Measurement Level



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



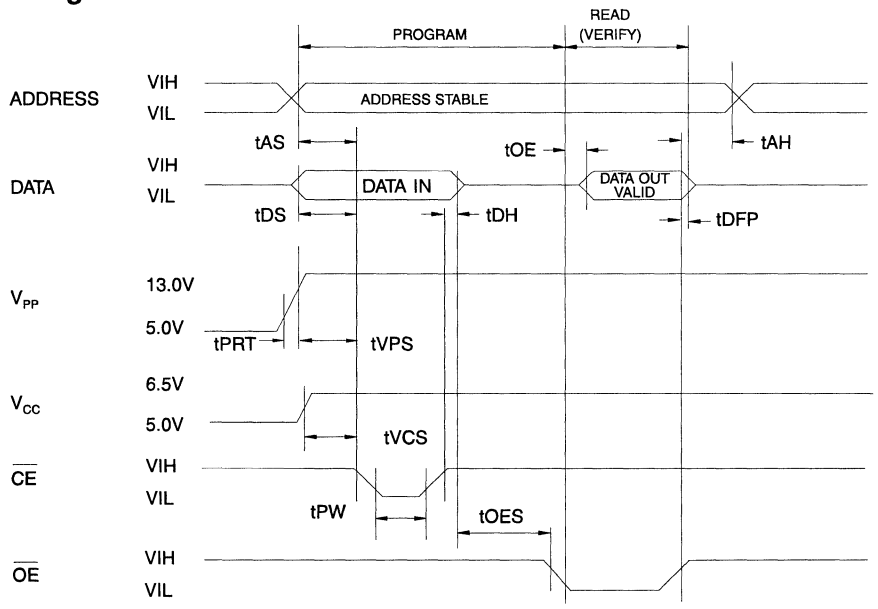
Note: CL = 100 pF
including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV040A a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}$ = V_{IL}		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$ (2)			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

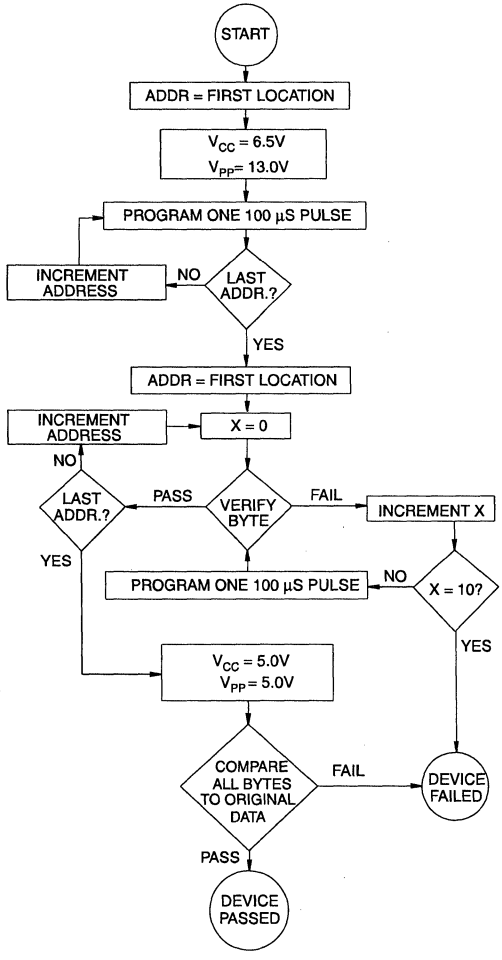
Atmel's 27LV040A Integrated Product Identification Code (1)

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

Note: 1. The AT27LV040A has the same Product Identification Code as the AT27C040. Both are programming compatible.

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.6V		Ordering Code	Package	Operation Range
	Active	Standby			
120	8	0.02	AT27LV040A-12JC AT27LV040A-12TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27LV040A-12JI AT27LV040A-12TI	32J 32T	Industrial (-40°C to 85°C)
150	8	0.02	AT27LV040A-15JC AT27LV040A-15TC	32J 32T	Commercial (0°C to 70°C)
	8	0.02	AT27LV040A-15JI AT27LV040A-15TI	32J 32T	Industrial (-40°C to 85°C)

= Preliminary Information

3

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

256K (32K x 8) OTP CMOS EPROM

Features

- Fast Read Access Time - 45 ns
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 20 mA max. Active at 5 MHz
- JEDEC Standard Packages
  - 28-Lead 600-mil PDIP
  - 32-Lead PLCC
  - 28-Lead TSOP and SOIC
- 5V ± 10% Supply
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27C256R is a low-power, high performance 262,144 bit one-time programmable read only memory (OTP EPROM) organized 32K by 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

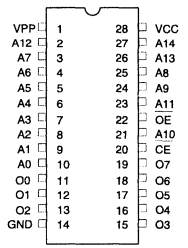
Atmel's scaled CMOS technology provides low active power consumption, and fast programming. Power consumption is typically only 8 mA in Active Mode and less than 10 µA in Standby.

(continued)

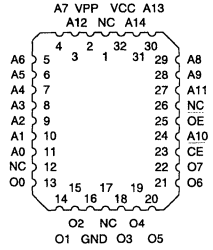
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

PDIP, SOIC Top View



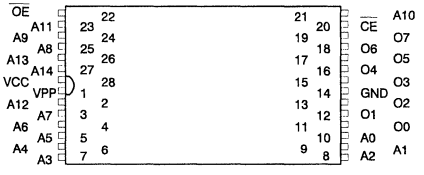
PLCC Top View



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

TSOP Top View

Type 1



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Description (Continued)

The AT27C256R is available in a choice of industry standard JEDEC-approved one time programmable (OTP) plastic DIP, PLCC, SOIC, and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

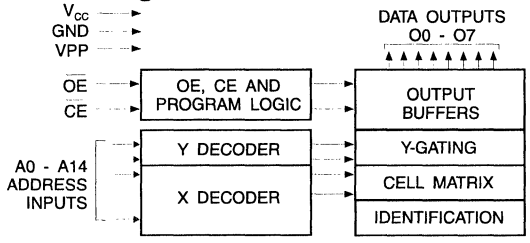
With 32K byte storage capability, the AT27C256R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C256R has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X (1)	V_{CC}	High Z
Standby	V_{IH}	X (1)	X (1)	V_{CC}	High Z
Rapid Program (2)	V_{IL}	V_{IH}	Ai	V_{PP}	D_{IN}
PGM Verify (2)	X (1)	V_{IL}	Ai	V_{PP}	D_{OUT}
Optional PGM Verify (2)	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
PGM Inhibit (2)	V_{IH}	V_{IH}	X (1)	V_{PP}	High Z
Product Identification (4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A14 = V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27C256R					
		-45	-55	-70	-90	-12	-15
Operating Temp. (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		20	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

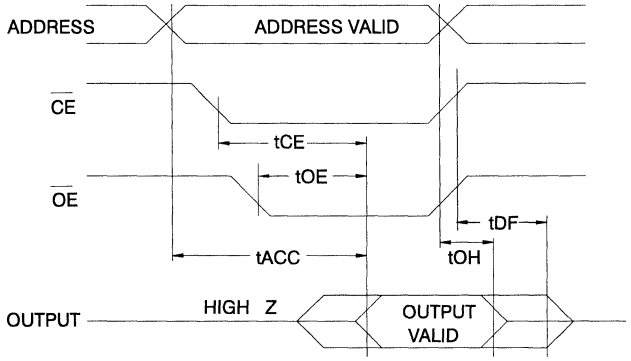
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C256R										
			-45		-55		-70		-90		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		45		55		70		90		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		45		55		70		90		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		25		30		30		35		40	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			20		20		25		25		30		35	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		7		7		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

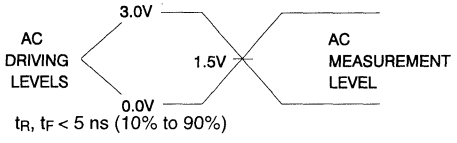
AC Waveforms for Read Operation [1]



Notes:
1. Timing measurement reference level is 1.5V for -45 and -55 devices. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

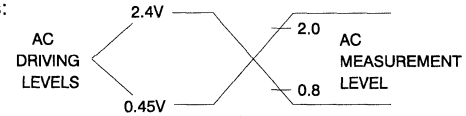
Input Test Waveforms and Measurement Levels

For -45 and -55 devices only:



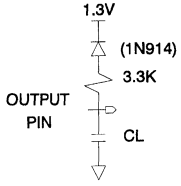
t_R, t_F < 5 ns (10% to 90%)

For -70, -90, -12, and -15 devices:



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



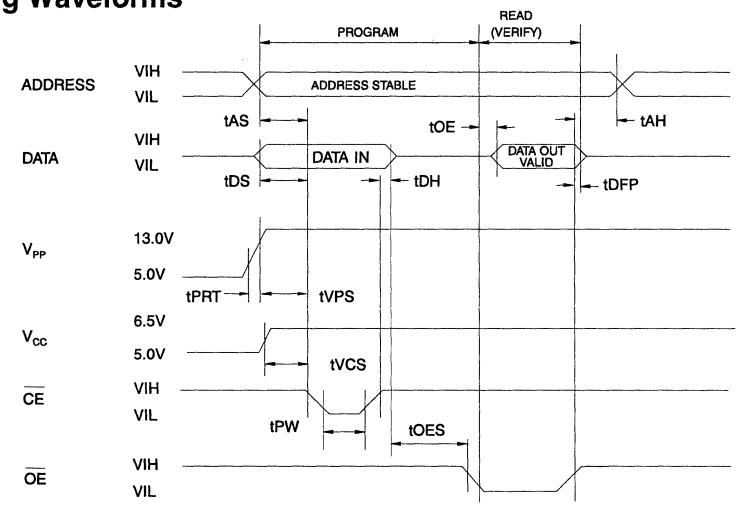
Note: C_L = 100 pF including jig capacitance, except for the -45 and -55 devices, where C_L = 30 pF.

Pin Capacitance (f = 1MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C256R a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Volt.	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Volt.	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions*(1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$ (2)			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

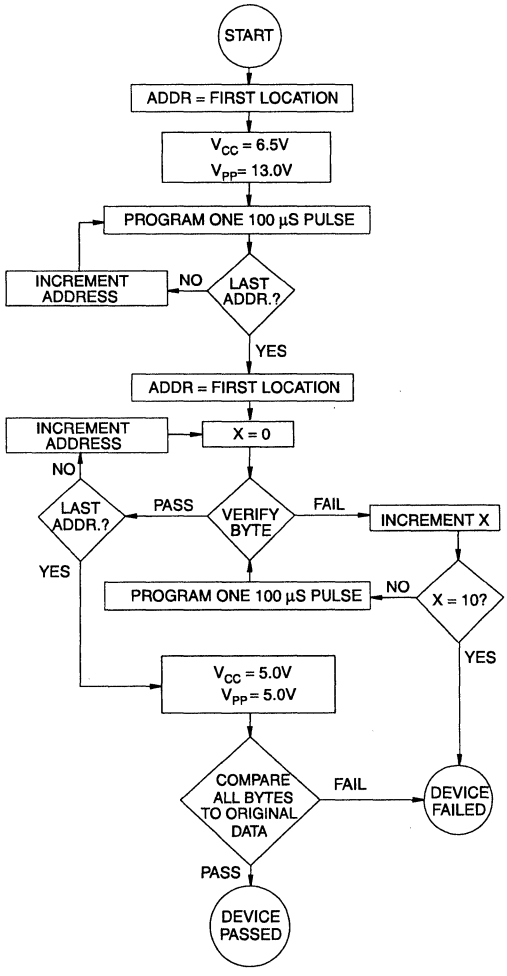
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C256R Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	20	0.1	AT27C256R-45JC AT27C256R-45PC AT27C256R-45RC AT27C256R-45TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C256R-45JI AT27C256R-45PI AT27C256R-45RI AT27C256R-45TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)
55	20	0.1	AT27C256R-55JC AT27C256R-55PC AT27C256R-55RC AT27C256R-55TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C256R-55JI AT27C256R-55PI AT27C256R-55RI AT27C256R-55TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)
70	20	0.1	AT27C256R-70JC AT27C256R-70PC AT27C256R-70RC AT27C256R-70TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C256R-70JI AT27C256R-70PI AT27C256R-70RI AT27C256R-70TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)
90	20	0.1	AT27C256R-90JC AT27C256R-90PC AT27C256R-90RC AT27C256R-90TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C256R-90JI AT27C256R-90PI AT27C256R-90RI AT27C256R-90TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)
120	20	0.1	AT27C256R-12JC AT27C256R-12PC AT27C256R-12RC AT27C256R-12TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C256R-12JI AT27C256R-12PI AT27C256R-12RI AT27C256R-12TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)

(continued)

Ordering Information (Continued)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	20	0.1	AT27C256R-15JC AT27C256R-15PC AT27C256R-15RC AT27C256R-15TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C256R-15JI AT27C256R-15PI AT27C256R-15RI AT27C256R-15TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 45 ns
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 20 mA max. Active at 5 MHz
- JEDEC Standard Packages
  - 28-Lead 600-mil PDIP
  - 32-Lead PLCC
  - 28-Lead TSOP and SOIC
- 5V ± 10% Supply
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

512K (64K x 8) OTP CMOS EPROM

3

Description

The AT27C512R is a low-power, high performance 524,288 bit one-time programmable read only memory (OTP EPROM) organized 64K by 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

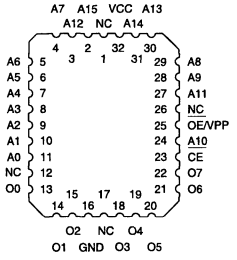
Atmel's scaled CMOS technology provides high speed, lower active power consumption, and significantly faster programming. Power consumption is typically only 8 mA in Active Mode and less than 10 µA in Standby.

(continued)

Pin Configurations

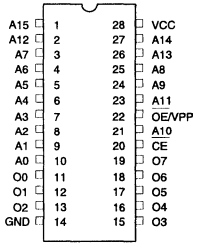
Pin Name	Function
A0 - A15	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$ /VPP	Output Enable/VPP
NC	No Connect

PLCC Top View



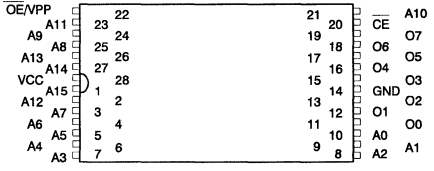
Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

PDIP, SOIC Top View



TSOP Top View

Type 1



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Description (Continued)

The AT27C512R is available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, SOIC, and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

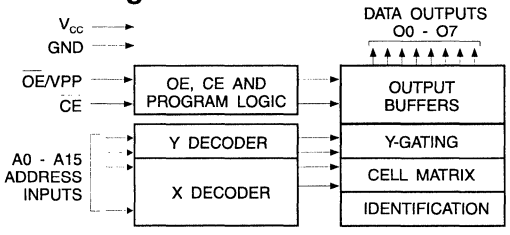
With 64K byte storage capability, the AT27C512R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C512R has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	Outputs
Read	V_{IL}	V_{IL}	Ai	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X (1)	High Z
Standby	V_{IH}	X (1)	X	High Z
Rapid Program (2)	V_{IL}	V_{PP}	Ai	D_{IN}
PGM Inhibit	V_{IH}	V_{PP}	X (1)	High Z
Product Identification (4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A15 = V_{IL}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming Characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27C512R					
		-45	-55	-70	-90	-12	-15
Operating Temp.(Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{SB}	V_{CC} [1] Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		20	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

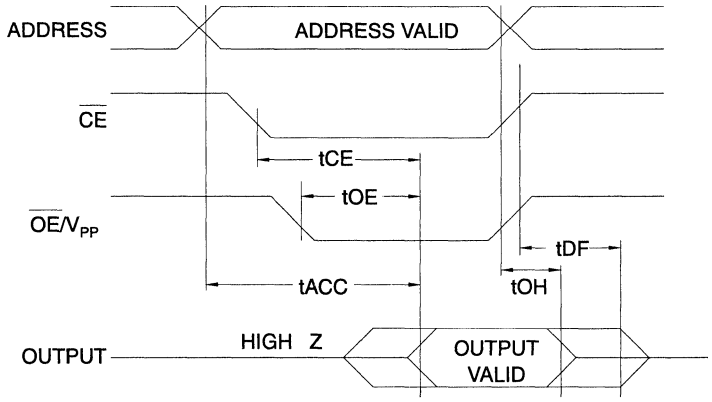
Note: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

AC Characteristics for Read Operation

			AT27C512R										
			-45		-55		-70		-90		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} [3]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}		45		55		70		90		120		150	ns
t_{CE} [2]	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$ = V_{IL}		45		55		70		90		120		150	ns
t_{OE} [2, 3]	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		25		30		35		35		40	ns
t_{DF} [4, 5]	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float, whichever occurred first			20		20		25		25		30		35	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first		7		7		7		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

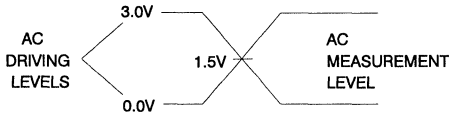
AC Waveforms for Read Operation [1]



Notes: 1. Timing measurement reference level is 1.5V for -45 and -55 devices. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

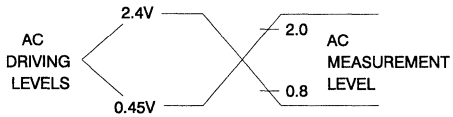
Input Test Waveforms and Measurement Levels

For -45 and -55 devices only:



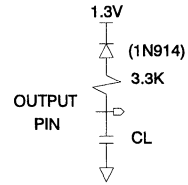
t_R, t_F < 5 ns (10% to 90%)

For -70, -90, -12, -15, and -20 devices:



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



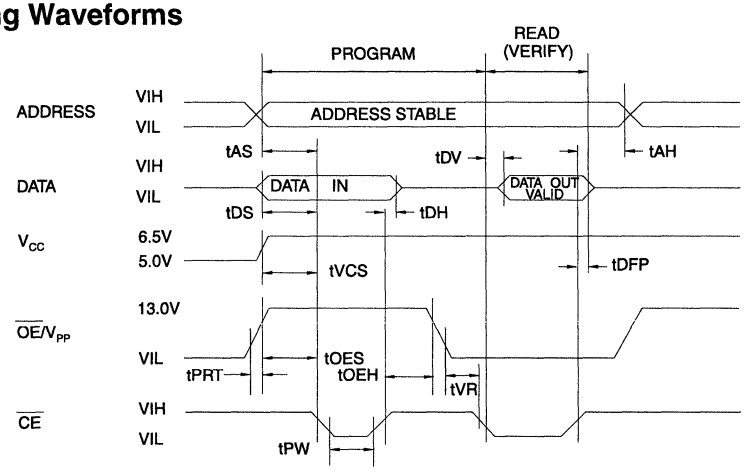
Note: CL = 100 pF including jig capacitance, except for the -45 and -55 devices, where CL = 30 pF.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, $\overline{OE}/V_{PP}$ = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE}$ = V_{IL}		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, $\overline{OE}/V_{PP}$ = 13.0 ± 0.25V

Symbol	Parameter	Test Condtions* (1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay (2)		0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		95	105	µs
t_{DV}	Data Valid from $\overline{CE}$ (2)			1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%)..... 20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

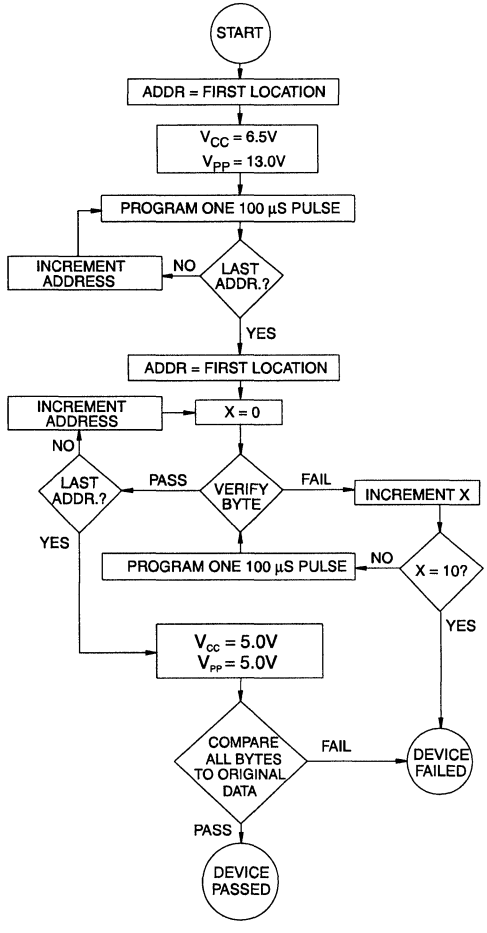
Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C512R Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	20	0.1	AT27C512R-45JC AT27C512R-45PC AT27C512R-45RC AT27C512R-45TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C512R-45JI AT27C512R-45PI AT27C512R-45RI AT27C512R-45TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)
55	20	0.1	AT27C512R-55JC AT27C512R-55PC AT27C512R-55RC AT27C512R-55TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C512R-55JI AT27C512R-55PI AT27C512R-55RI AT27C512R-55TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)
70	20	0.1	AT27C512R-70JC AT27C512R-70PC AT27C512R-70RC AT27C512R-70TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C512R-70JI AT27C512R-70PI AT27C512R-70RI AT27C512R-70TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)
90	20	0.1	AT27C512R-90JC AT27C512R-90PC AT27C512R-90RC AT27C512R-90TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C512R-90JI AT27C512R-90PI AT27C512R-90RI AT27C512R-90TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)
120	20	0.1	AT27C512R-12JC AT27C512R-12PC AT27C512R-12RC AT27C512R-12TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)
	20	0.1	AT27C512R-12JI AT27C512R-12PI AT27C512R-12RI AT27C512R-12TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)
150	20	0.1	AT27C512R-15JC AT27C512R-15PC AT27C512R-15RC AT27C512R-15TC	32J 28P6 28R 28T	Commercial (0°C to 70°C)

(continued)

Ordering Information (Continued)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	20	0.1	AT27C512R-15JI AT27C512R-15PI AT27C512R-15RI AT27C512R-15TI	32J 28P6 28R 28T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Thin Small Outline Package (TSOP)

512K (32K x 16) OTP CMOS EPROM

Features

- **Fast Read Access Time - 45 ns**
- **Low Power CMOS Operation**
  - **100 µA max. Standby**
  - **30 mA max. Active at 5 MHz**
- **JEDEC Standard Packages**
  - **44-Lead PLCC**
  - **40-Lead TSOP (10mm x 14mm)**
- **5V ± 10% Power Supply**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming Algorithm - 50 µs/word (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

Description

The AT27C516 is a low-power, high performance 524,288 bit one-time programmable read only memory (OTP EPROM) organized 32K by 16 bits. It requires only one 5V power supply in normal read mode operation. Any word can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states. The by-16 organization make this part ideal for high-performance 16 and 32 bit microprocessor systems.

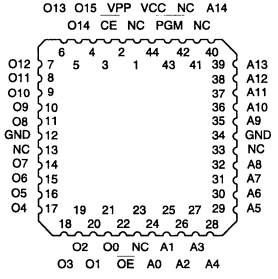
(continued)

Pin Configurations

Pin Name	Function
A0 - A14	Addresses
O0 - O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

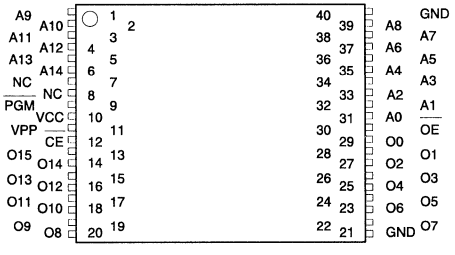
Note: Both GND pins must be connected.

PLCC Top View



Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

TSOP Top View
Type 1



0362C

Description (Continued)

In read mode, the AT27C516 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C516 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

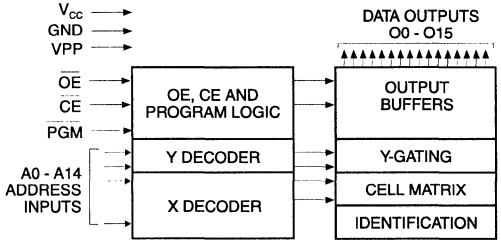
With 32K word storage capability, the AT27C516 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C516 have additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X (1)	Ai	X	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X (5)	High Z
Rapid Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	High Z
Product Identification (4)	V_{IL}	V_{IL}	X	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A14 = V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP} = V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

DC and AC Operating Conditions for Read Operation

		AT27C516				
		-45	-55	-70	-85	-10
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

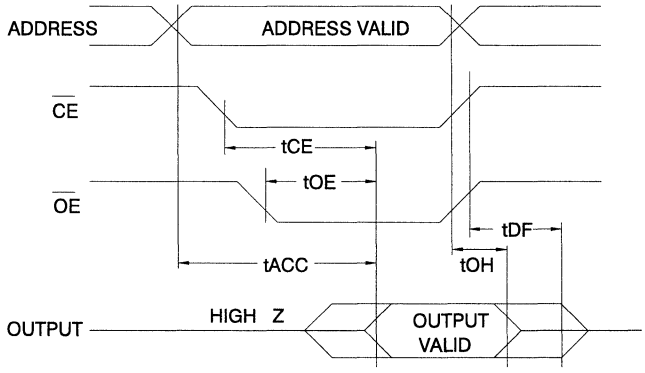
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C516										
			-45		-55		-70		-85		-10		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = VIL		45		55		70		85		100	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		45		55		70		85		100	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		25		25		30		30	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			20		25		25		30		30	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		7		7		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

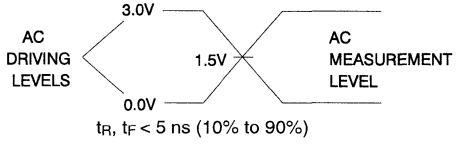
AC Waveforms for Read Operation [1]



Notes: 1. Timing measurement reference level is 1.5V for -45 and -55 devices. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

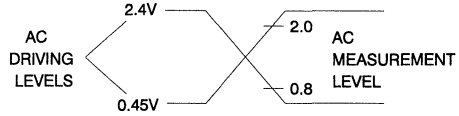
Input Test Waveforms and Measurement Levels

For -45, -55, and -70 Devices Only:



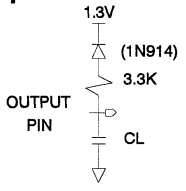
t_R, t_F < 5 ns (10% to 90%)

For -85 and -10 Devices Only:



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



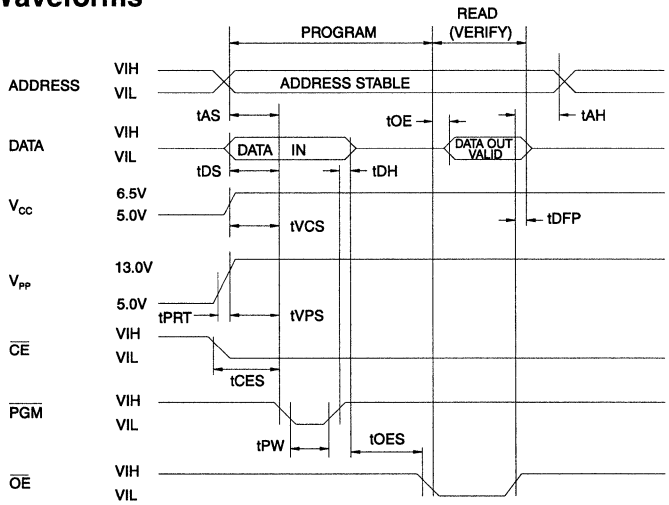
Note: CL = 100 pF including jig capacitance except -45, -55 and -70 devices, where CL = 30 pF.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C516 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limit Min	Limit Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (3)		47.5	52.5	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

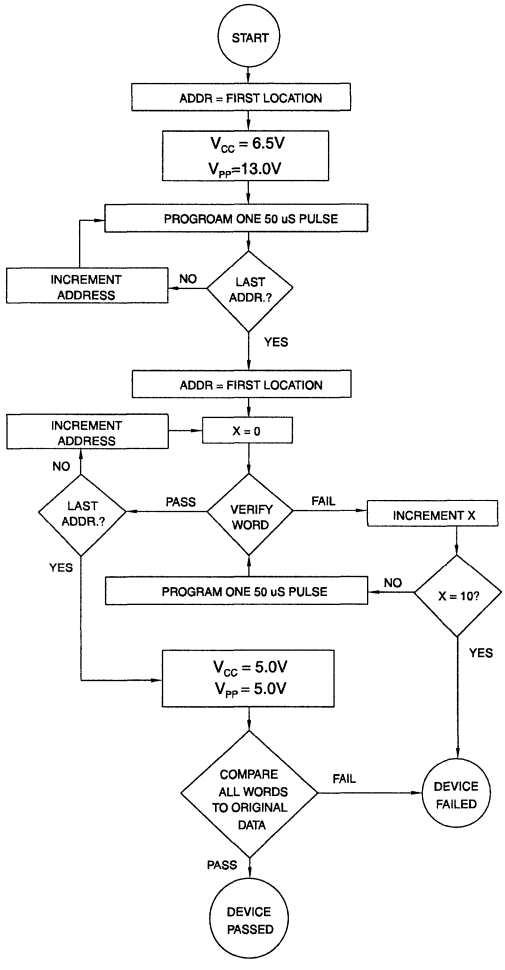
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 50 µsec ± 5%.

Atmel's 27C516 Integrated Product Identification Code

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	1	0	00F2

Rapid Programming Algorithm

A 50 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	30	0.1	AT27C516-45JC AT27C516-45VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C516-45JI AT27C516-45VI	44J 40V	Industrial (-40°C to 85°C)
55	30	0.1	AT27C516-55JC AT27C516-55VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C516-55JI AT27C516-55VI	44J 40V	Industrial (-40°C to 85°C)
70	30	0.1	AT27C516-70JC AT27C516-70VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C516-70JI AT27C516-70VI	44J 40V	Industrial (-40°C to 85°C)
85	30	0.1	AT27C516-85JC AT27C516-85VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C516-85JI AT27C516-85VI	44J 40V	Industrial (-40°C to 85°C)
100	30	0.1	AT27C516-10JC AT27C516-10VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C516-10JI AT27C516-10VI	44J 40V	Industrial (-40°C to 85°C)

Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40V	40 Lead, Plastic Thin Small Outline Package (TSOP) (10mm x 14mm)

Features

- Fast Read Access Time - 45 ns
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 25 mA max. Active at 5 MHz (AT27C010L)
  - 35 mA max. Active at 5 MHz (AT27C010)
- JEDEC Standard Packages
  - 32-Lead 600-mil PDIP
  - 32-Lead PLCC
  - 32-Lead TSOP
- 5V ± 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

1 Megabit (128K x 8) OTP CMOS EPROM

3

Description

The AT27C010/L is a low-power, high performance 1,048,576 bit one-time programmable read only memory (OTP EPROM) organized as 128K by 8 bits. They require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

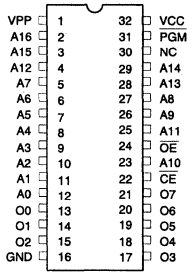
Two power versions are offered. In read mode, the AT27C010 typically consumes 25 mA while the AT27C010L requires only 8 mA. Standby mode supply current for both parts is typically less than 10 µA.

(continued)

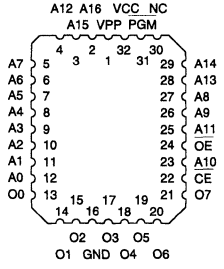
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

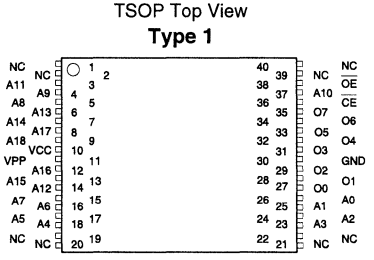
PDIP Top View



PLCC Top View



TSOP Top View
Type 1



0321H

Description (Continued)

The AT27C010/L in available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, and TSOP packages. All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

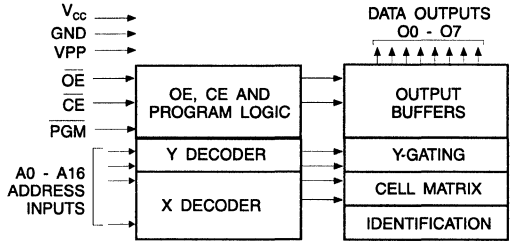
With 128K byte storage capability, the AT27C010/L allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C010/L have additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X (1)	Ai	X	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X	High Z
Rapid Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	High Z
Product Identification (4)	V_{IL}	V_{IL}	X	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A16 = V_{IL}	X	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27C010 / AT27C010L					
		-45	-55	-70	-90	-12	-15
Operating Temp. (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}			±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V			100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	AT27C010		25	mA
			AT27C010		35	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

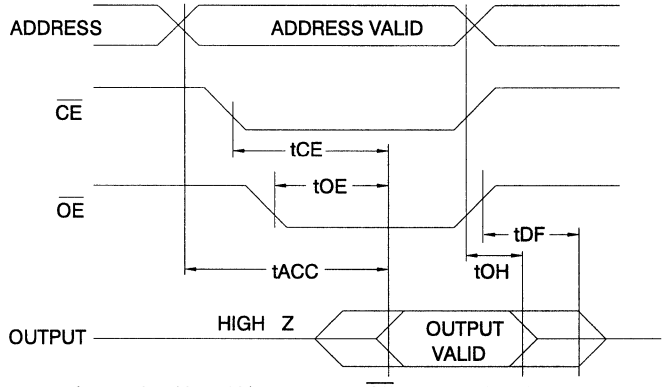
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C010 / AT27C010L										
			-45		-55		-70		-90		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		45		55		70		90		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		45		55		70		90		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		25		30		35		35		40	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			20		20		25		25		30		35	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		7		7		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

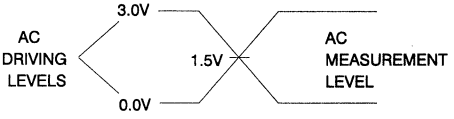
AC Waveforms for Read Operation [1]



Notes: 1. Timing measurement reference level is 1.5V for -45 and -55 devices. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

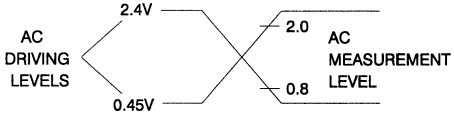
Input Test Waveforms and Measurement Levels

For -45 and -55 devices only:



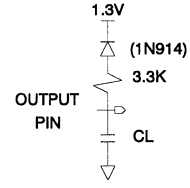
t_R, t_F < 5 ns (10% to 90%)

For -70, -90, -12, -15, and -20 devices:



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



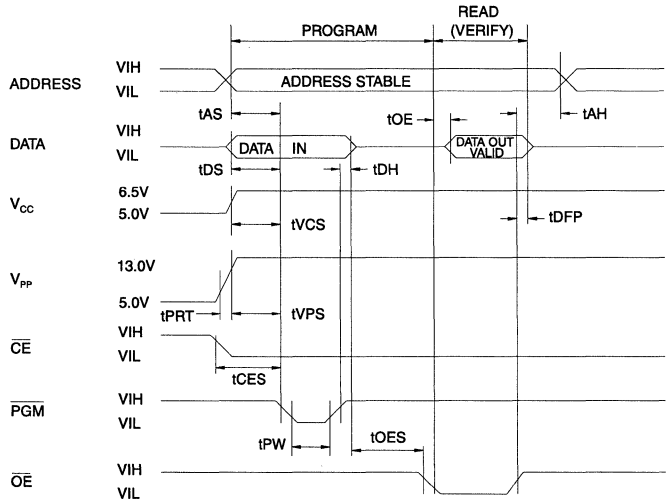
Note: CL = 100 pF including jig capacitance, except for the -45 and -55 devices, where CL= 30 pF.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C010/L, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25 V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise TIme During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

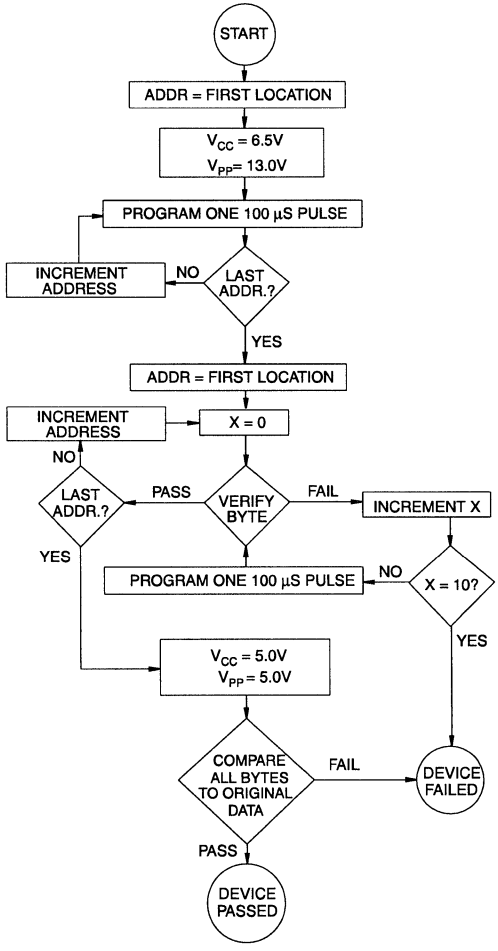
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C010/L Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	05

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	35	0.1	AT27C010-45JC AT27C010-45PC AT27C010-45TC	32J 32P6 32T	Commercial (0°C to 70°C)
	35	0.1	AT27C010-45JI AT27C010-45PI AT27C010-45TI	32J 32P6 32T	Industrial (-40°C to 85°C)
55	35	0.1	AT27C010-55JC AT27C010-55PC AT27C010-55TC	32J 32P6 32T	Commercial (0°C to 70°C)
	35	0.1	AT27C010-55JI AT27C010-55PI AT27C010-55TI	32J 32P6 32T	Industrial (-40°C to 85°C)
70	35	0.1	AT27C010-70JC AT27C010-70PC AT27C010-70TC	32J 32P6 32T	Commercial (0°C to 70°C)
	35	0.1	AT27C010-70JI AT27C010-70PI AT27C010-70TI	32J 32P6 32T	Industrial (-40°C to 85°C)
90	35	0.1	AT27C010-90JC AT27C010-90PC AT27C010-90TC	32J 32P6 32T	Commercial (0°C to 70°C)
	35	0.1	AT27C010-90JI AT27C010-90PI AT27C010-90TI	32J 32P6 32T	Industrial (-40°C to 85°C)
120	35	0.1	AT27C010-12JC AT27C010-12PC AT27C010-12TC	32J 32P6 32T	Commercial (0°C to 70°C)
	35	0.1	AT27C010-12JI AT27C010-12PI AT27C010-12TI	32J 32P6 32T	Industrial (-40°C to 85°C)
150	35	0.1	AT27C010-15JC AT27C010-15PC AT27C010-15TC	32J 32P6 32T	Commercial (0°C to 70°C)
	35	0.1	AT27C010-15JI AT27C010-15PI AT27C010-15TI	32J 32P6 32T	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	25	0.1	AT27C010L-45JC AT27C010L-45PC AT27C010L-45TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C010L-45JI AT27C010L-45PI AT27C010L-45TI	32J 32P6 32T	Industrial (-40°C to 85°C)
55	25	0.1	AT27C010L-55JC AT27C010L-55PC AT27C010L-55TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C010L-55JI AT27C010L-55PI AT27C010L-55TI	32J 32P6 32T	Industrial (-40°C to 85°C)
70	25	0.1	AT27C010L-70JC AT27C010L-70PC AT27C010L-70TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C010L-70JI AT27C010L-70PI AT27C010L-70TI	32J 32P6 32T	Industrial (-40°C to 85°C)
90	25	0.1	AT27C010L-90JC AT27C010L-90PC AT27C010L-90TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C010L-90JI AT27C010L-90PI AT27C010L-90TI	32J 32P6 32T	Industrial (-40°C to 85°C)
120	25	0.1	AT27C010L-12JC AT27C010L-12PC AT27C010L-12TC	32J 32P6 32T	Commercia (0°C to 70°C)
	25	0.1	AT27C010L-12JI AT27C010L-12PI AT27C010L-12TI	32J 32P6 32T	Industrial (-40°C to 85°C)
150	25	0.1	AT27C010L-15JC AT27C010L-15PC AT27C010L-15TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C010L-15JI AT27C010L-15PI AT27C010L-15TI	32J 32P6 32T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

1 Megabit (64K x 16) OTP CMOS EPROM

Features

- Fast Read Access Time - 45 ns
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 30 mA max. Active at 5 MHz
- JEDEC Standard Packages
  - 40-Lead 600-mil PDIP
  - 44-Lead PLCC
  - 40-Lead TSOP (10 mm x 14 mm)
- Direct Upgrade from 512K (AT27C516) EPROM
- 5V ± 10% Power Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/word (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27C1024 is a low-power, high performance 1,048,576 bit one-time programmable read only memory (OTP EPROM) organized 64K by 16 bits. It requires only one 5V power supply in normal read mode operation. Any word can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states. The by-16 organization make this part ideal for high-performance 16 and 32 bit microprocessor systems.

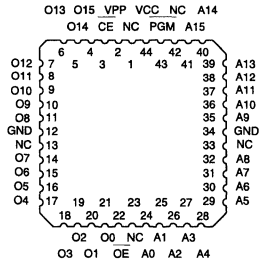
(continued)

Pin Configurations

Pin Name	Function
A0 - A15	Addresses
O0 - O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

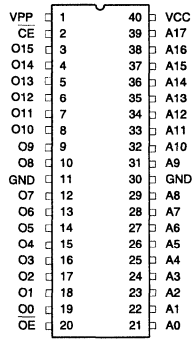
Note: Both GND pins must be connected.

PLCC Top View

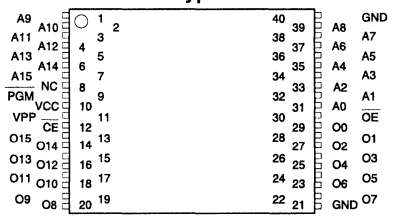


Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

PDIP Top View



TSOP Top View
Type 1



0388H

Description (Continued)

In read mode, the AT27C1024 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C1024 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, and TSOP packages. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

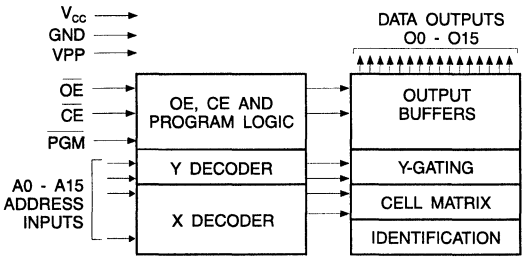
With high density 64K word storage capability, the AT27C1024 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C1024 have additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X (1)	Ai	X	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X (5)	High Z
Rapid Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	High Z
Product Identification (4)	V_{IL}	V_{IL}	X	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A15 = V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP} = V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

DC and AC Operating Conditions for Read Operation

		AT27C1024					
		-45	-55	-70	-85	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		± 1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		± 5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

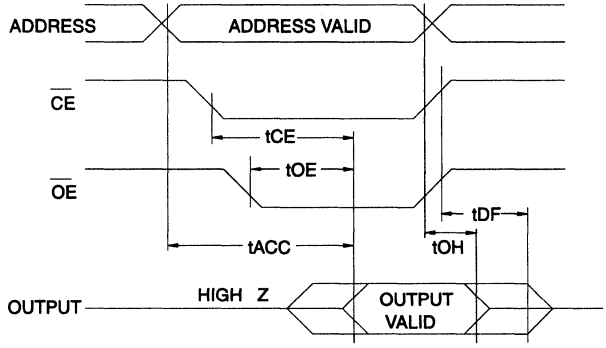
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C1024												
			-45		-55		-70		-85		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		45		55		70		85		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		45		55		70		85		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		25		25		30		35		50	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			20		25		25		30		30		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		7		7		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

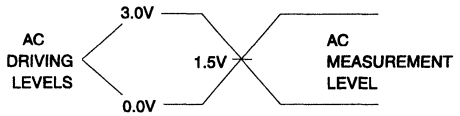
AC Waveforms for Read Operation [1]



Notes: 1. Timing measurement reference level is 1.5V for -45 and -55 devices. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

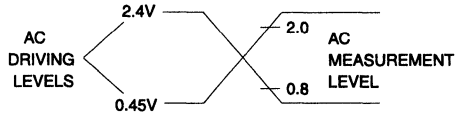
Input Test Waveforms and Measurement Levels

For -45, -55, and -70 Devices Only:



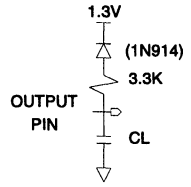
t_R, t_F < 5 ns (10% to 90%)

For -85, -10, -12, -15 Devices Only:



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



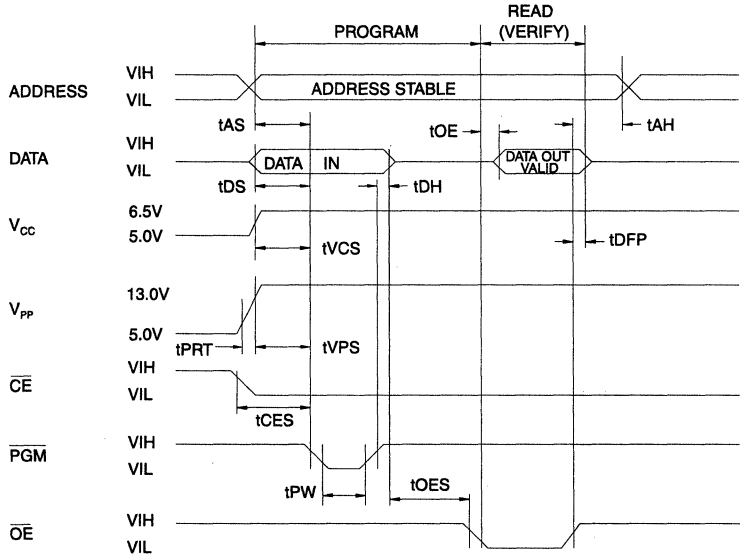
Note: CL = 100 pF including jig capacitance except -45, -55 and -70 devices, where CL = 30 pF.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C1024 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels..... 0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

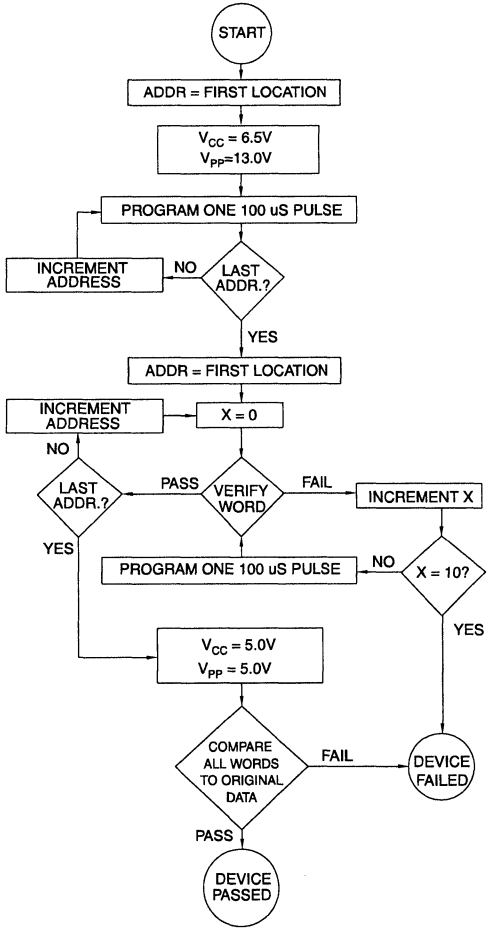
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C1024 Integrated Product Identification Code

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	0	1	00F1

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	30	0.1	AT27C1024-45JC AT27C1024-45PC AT27C1024-45VC	44J 40P6 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C1024-45JI AT27C1024-45PI AT27C1024-45VI	44J 40P6 40V	Industrial (-40°C to 85°C)
55	30	0.1	AT27C1024-55JC AT27C1024-55PC AT27C1024-55VC	44J 40P6 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C1024-55JI AT27C1024-55VI	44J 40V	Industrial (-40°C to 85°C)
70	30	0.1	AT27C1024-70JC AT27C1024-70PC AT27C1024-70VC	44J 40P6 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C1024-70JI AT27C1024-70PI AT27C1024-70VI	44J 40P6 40V	Industrial (-40°C to 85°C)
85	30	0.1	AT27C1024-85JC AT27C1024-85PC AT27C1024-85VC	44J 40P6 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C1024-85JI AT27C1024-85PI AT27C1024-85VI	44J 40P6 40V	Industrial (-40°C to 85°C)
120	30	0.1	AT27C1024-12JC AT27C1024-12PC AT27C1024-12VC	44J 40P6 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C1024-12JI AT27C1024-12PI AT27C1024-12VI	44J 40P6 40V	Industrial (-40°C to 85°C)
150	30	0.1	AT27C1024-15JC AT27C1024-15PC AT27C1024-15VC	44J 40P6 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C1024-15JI AT27C1024-15PI AT27C1024-15VI	44J 40P6 40V	Industrial (-40°C to 85°C)

Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
40V	40 Lead, Plastic Thin Small Outline Package (TSOP) 10 x 14 mm

2 Megabit (256K x 8) OTP CMOS EPROM

Features

- **Fast Read Access Time - 70 ns**
- **Low Power CMOS Operation**
  - **100 µA max. Standby**
  - **25 mA max. Active at 5 MHz**
- **JEDEC Standard Packages**
  - **32-Lead 600-mil PDIP**
  - **32-Lead PLCC**
  - **32-Lead TSOP**
- **5V ± 10% Supply**
- **High Reliability CMOS Technology**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming Algorithm - 100 µs/byte (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

Description

The AT27C020 is a low-power, high performance 2,097,152 bit one-time programmable read only memory (OTP EPROM) organized as 256K by 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 70 ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

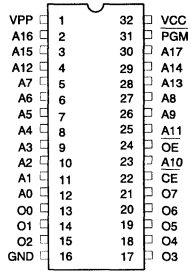
In read mode, the AT27C020 typically consumes 8 mA. Standby mode supply current is typically less than 10 µA.

(continued)

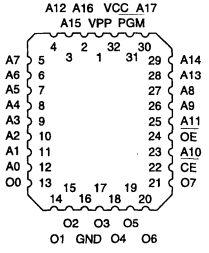
Pin Configurations

Pin Name	Function
A0 - A17	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe

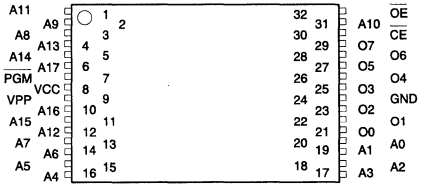
PDIP, Top View



PLCC Top View



TSOP Top View
Type 1



0570A

Description (Continued)

The AT27C020 is available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

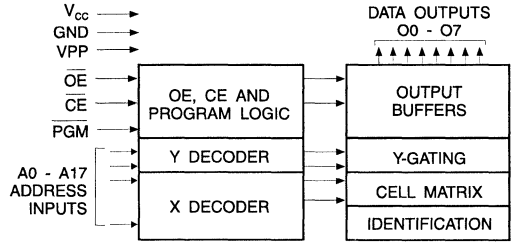
With 256K byte storage capability, the AT27C020 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C020 have additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X (1)	Ai	X	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X	High Z
Rapid Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	High Z
Product Identification (4)	V_{IL}	V_{IL}	X	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A17 = V_{IL}	X	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27C020				
		-70	-85	-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}	Com., Ind.		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	Com., Ind.		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V			100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}			25	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

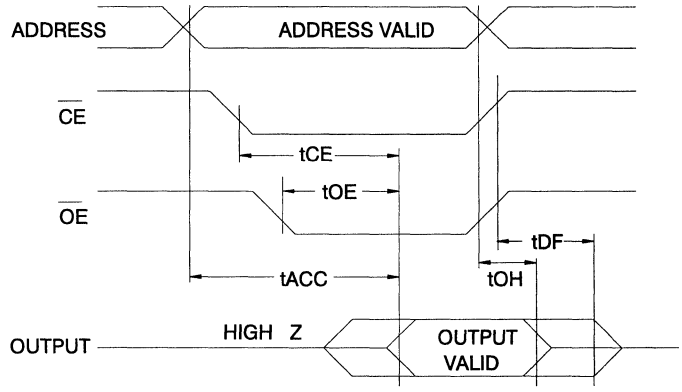
AC Characteristics for Read Operation

			AT27C020									
			-70		-85		-10		-12		-15	
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		70		85		100		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		70		85		100		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		35		35		35		35		40	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			25		25		30		35		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		0		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

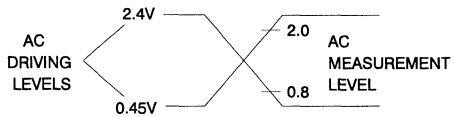
= Preliminary Information

AC Waveforms for Read Operation [1]



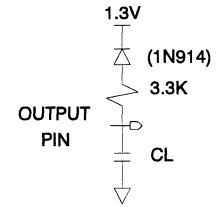
Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



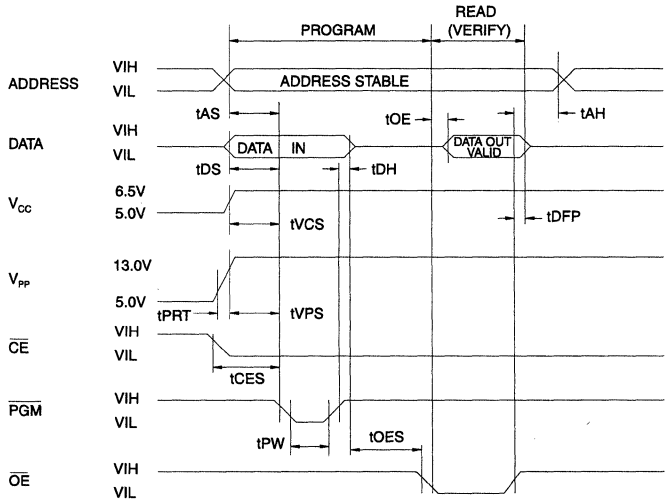
Note: CL= 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C020 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

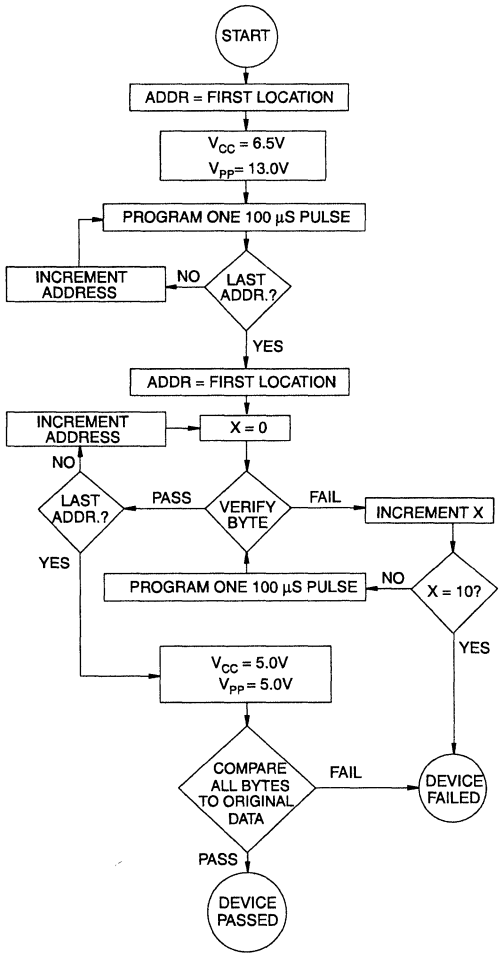
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C020 Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	0	1	1	0	86

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	25	0.1	AT27C020-70JC AT27C020-70PC AT27C020-70TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C020-70JI AT27C020-70PI AT27C020-70TI	32J 32P6 32T	Industrial (-40°C to 85°C)
85	25	0.1	AT27C020-85JC AT27C020-85PC AT27C020-85TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C020-85JI AT27C020-85PI AT27C020-85TI	32J 32P6 32T	Industrial (-40°C to 85°C)
100	25	0.1	AT27C020-10JC AT27C020-10PC AT27C020-10TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C020-10JI AT27C020-10PI AT27C020-10TI	32J 32P6 32T	Industrial (-40°C to 85°C)
120	25	0.1	AT27C020-12JC AT27C020-12PC AT27C020-12TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C020-12JI AT27C020-12PI AT27C020-12TI	32J 32P6 32T	Industrial (-40°C to 85°C)
150	25	0.1	AT27C020-15JC AT27C020-15PC AT27C020-15TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C020-15JI AT27C020-15PI AT27C020-15TI	32J 32P6 32T	Industrial (-40°C to 85°C)

= Preliminary Information

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 70 ns
- Low Power CMOS Operation
  - 100 µA Maximum Standby
  - 35 mA Maximum Active at 5 MHz
- JEDEC Standard Packages
  - 40-Lead 600 mil PDIP
  - 44-Lead PLCC
  - 40-Lead TSOP (10 mm X 14 mm)
- Direct Upgrade from 512K bit and 1M bit (AT27C516 and AT27C1024) EPROMs
- 5V ± 10% Power Supply
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 50 µs/word (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

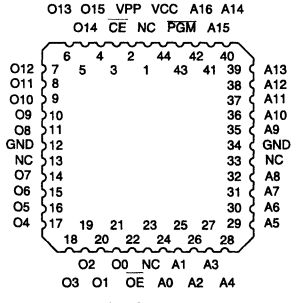
The AT27C2048 is a low-power, high performance 2,097,152 bit one-time programmable read only memory (OTP EPROM) organized as 128K by 16 bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in less than 70 ns, eliminating the need for speed-reducing WAIT states. The by-16 organization makes this part ideal for high-performance 16 and 32 bit microprocessor systems.

Pin Configurations

Pin Name	Function
A0 - A16	Addresses
O0 - O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program
NC	No Connect

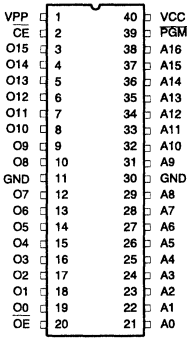
Note: Both GND pins must be connected.

PLCC Top View

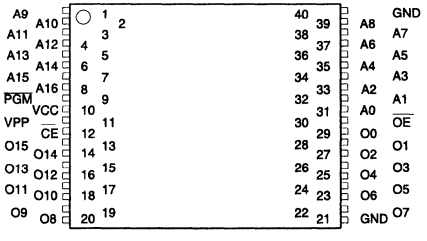


Note: PLCC package pins 1 and 23 are DON'T CONNECT.

PDIP Top View *(continued)*



TSOP Top View
Type 1



2 Megabit (128K x 16) OTP CMOS EPROM

Preliminary

3

0632A

Description (Continued)

In read mode, the AT27C2048 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C2048 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic, PDIP, PLCC, and TSOP packages. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

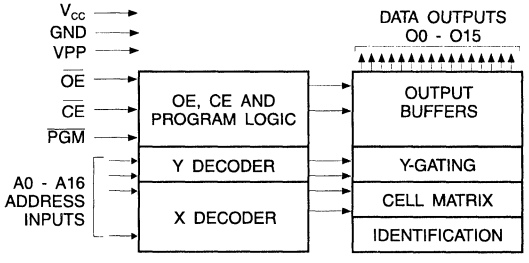
With high density 128K word storage capability, the AT27C2048 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's AT27C2048 has additional features that ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



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Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X (1)	Ai	X (1)	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X (5)	High Z
Rapid Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	High Z
Product Identification (4)	V_{IL}	V_{IL}	X	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A16 = V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to the Programming Characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9, which is set to V_H, and A0, which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP} = V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

DC and AC Operating Conditions for Read Operation

		AT27C2048			
		-70	-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		35	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

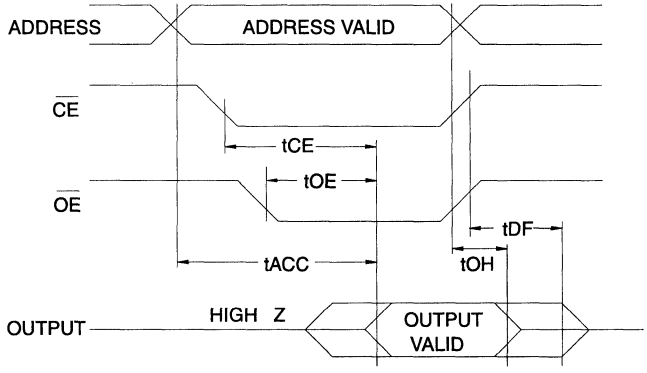
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C2048								
			-70		-90		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		70		90		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		40		40		40		50	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30		30		35		40	ns
t_{OH} (4)	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		0		0		0		ns

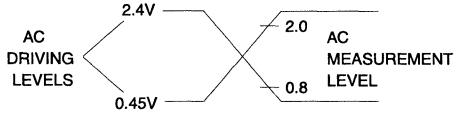
Notes: 2, 3, 4, 5. See the AC Waveforms for Read Operation diagram.

AC Waveforms for Read Operation (1)



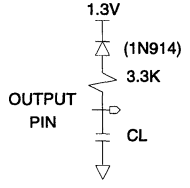
Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



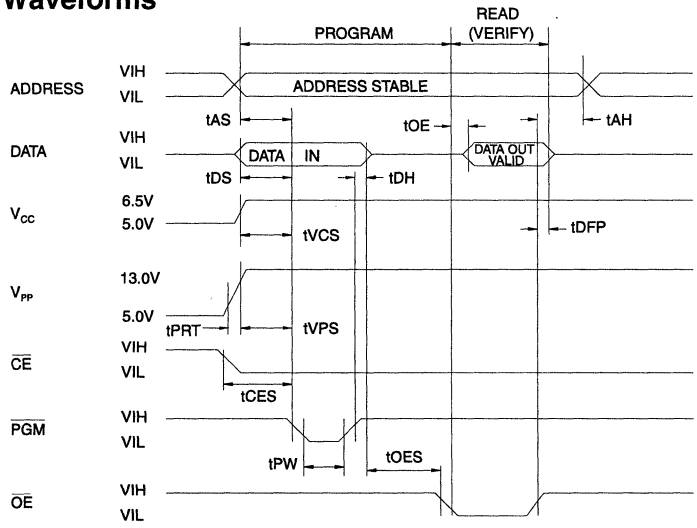
Note: CL = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C2048, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		± 10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (3)		47.5	52.5	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%) .....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level..... 0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

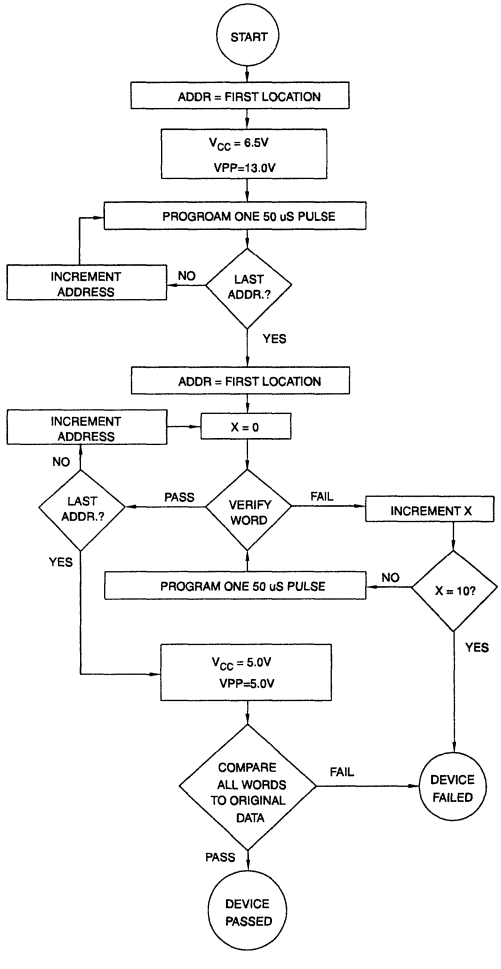
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Ouput Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 50 µsec ± 5%.

Atmel's 27C2048 Integrated Product Identification Code

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	1	1	1	00F7

Rapid Programming Algorithm

A 50 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	35	0.1	AT27C2048-70JC AT27C2048-70PC AT27C2048-70VC	44J 40P6 40V	Commercial (0°C to 70°C)
	35	0.1	AT27C2048-70JI AT27C2048-70PI AT27C2048-70VI	44J 40P6 40V	Industrial (-40°C to 85°C)
90	35	0.1	AT27C2048-90JC AT27C2048-90PC AT27C2048-90VC	44J 40P6 40V	Commercial (0°C to 70°C)
	35	0.1	AT27C2048-90JI AT27C2048-90PI AT27C2048-90VI	44J 40P6 40V	Industrial (-40°C to 85°C)
120	35	0.1	AT27C2048-12JC AT27C2048-12PC AT27C2048-12VC	44J 40P6 40V	Commercial (0°C to 70°C)
	35	0.1	AT27C2048-12JI AT27C2048-12PI AT27C2048-12VI	44J 40P6 40V	Industrial (-40°C to 85°C)
150	35	0.1	AT27C2048-15JC AT27C2048-15PC AT27C2048-15VC	44J 40P6 40V	Commercial (0°C to 70°C)
	35	0.1	AT27C2048-15JI AT27C2048-15PI AT27C2048-15VI	44J 40P6 40V	Industrial (-40°C to 85°C)

Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
40V	40 Lead, Plastic Thin Small Outline Package (TSOP) 10 x 14 mm

4 Megabit (512K x 8) OTP CMOS EPROM

Features

- Fast Read Access Time - 80 ns
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 30 mA max. Active at 5 MHz
- JEDEC Standard Packages
  - 32-Lead 600-mil PDIP
  - 32-Lead 450-mil SOIC (SOP)
  - 32-Lead PLCC
  - 32-Lead TSOP
- 5V ± 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27C040 chip is a low-power, high-performance 4,194,304 bit one-time programmable read only memory (OTP EPROM) organized as 512K by 8 bits. The AT27C040 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 80 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

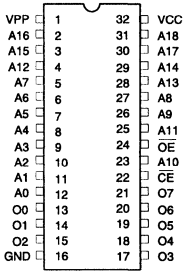
Atmel's scaled CMOS technology provides low active power consumption, and fast programming. Power consumption is typically 8 mA in active mode and less than 10 µA in standby mode.

(continued)

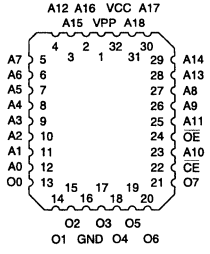
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

PDIP, SOIC Top View

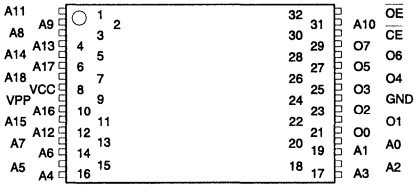


PLCC Top View



TSOP Top View

Type 1



0189D

Description (Continued)

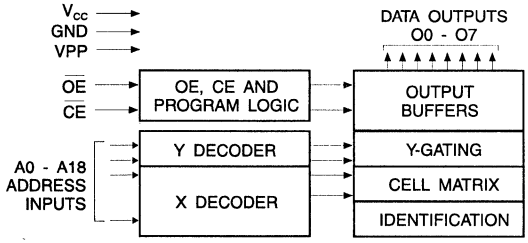
The AT27C040 is available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, SOIC (SOP), and TSOP packages. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

Atmel's AT27C040 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	Ai	X (1)	D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
Standby	V_{IH}	X	X	X	High Z
Rapid Program (2)	V_{IL}	V_{IH}	Ai	V_{PP}	D_{IN}
PGM Verify	X	V_{IL}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	V_{IH}	X	V_{PP}	High Z
Product Identification (4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A18 = V_{IL}	X	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27C040			
		-80	-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

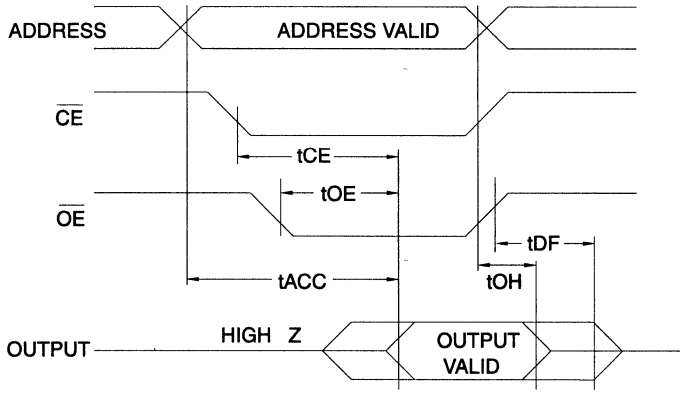
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C040								
			-80		-10		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		80		100		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		80		100		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		35		35		35		40	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30		30		30		30	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		0		0		ns

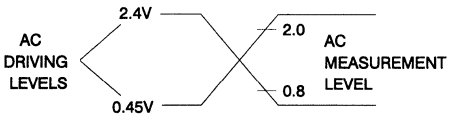
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

AC Waveforms for Read Operation [1]



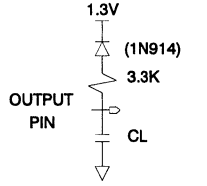
Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



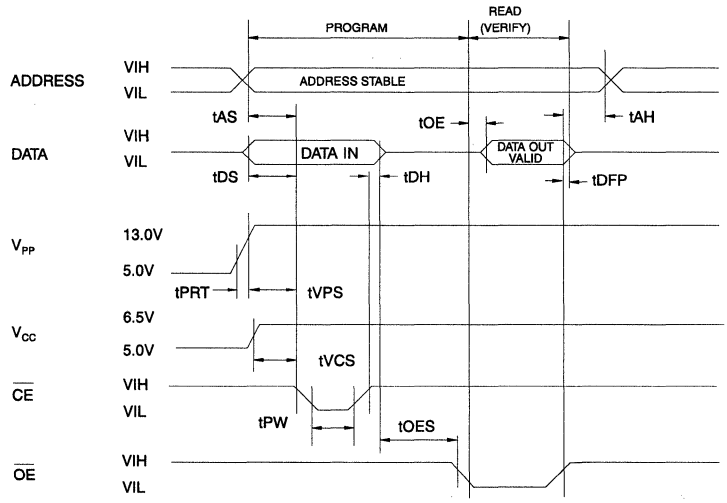
Note: CL = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C040 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.7	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Sym-bol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$ (2)			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

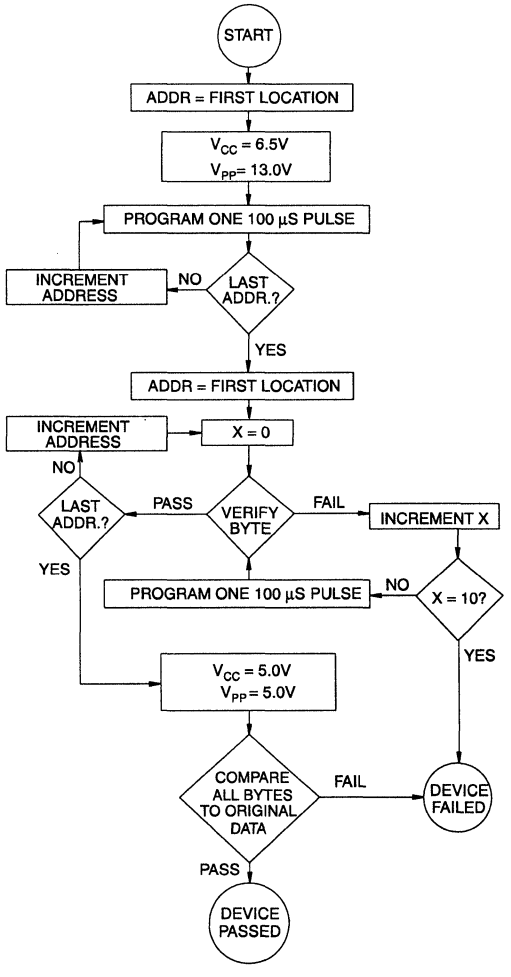
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C040 Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
80	30	0.1	AT27C040-80JC AT27C040-80PC AT27C040-80RC AT27C040-80TC	32J 32P6 32R 32T	Commercial (0°C to 70°C)
	30	0.1	AT27C040-80JI AT27C040-80PI AT27C040-80RI AT27C040-80TI	32J 32P6 32R 32T	Industrial (-40°C to 85°C)
100	30	0.1	AT27C040-10JC AT27C040-10PC AT27C040-10RC AT27C040-10TC	32J 32P6 32R 32T	Commercial (0°C to 70°C)
	30	0.1	AT27C040-10JI AT27C040-10PI AT27C040-10RI AT27C040-10TI	32J 32P6 32R 32T	Industrial (-40°C to 85°C)
120	30	0.1	AT27C040-12JC AT27C040-12PC AT27C040-12RC AT27C040-12TC	32J 32P6 32R 32T	Commercial (0°C to 70°C)
	30	0.1	AT27C040-12JI AT27C040-12PI AT27C040-12RI AT27C040-12TI	32J 32P6 32R 32T	Industrial (-40°C to 85°C)
150	30	0.1	AT27C040-15JC AT27C040-15PC AT27C040-15RC AT27C040-15TC	32J 32P6 32R 32T	Commercial (0°C to 70°C)
	30	0.1	AT27C040-15JI AT27C040-15PI AT27C040-15RI AT27C040-15TI	32J 32P6 32R 32T	Industrial (-40°C to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32R	32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline (SOIC)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

4 Megabit (256K x 16) OTP CMOS EPROM

Features

- **Fast Read Access Time - 85 ns**
- **Low Power CMOS Operation**
  - **100 µA Maximum Standby**
  - **40 mA Maximum Active at 5 MHz**
- **JEDEC Standard Packages**
  - **40-Lead 600 mil PDIP**
  - **44-Lead PLCC**
  - **40-Lead TSOP (10 mm X 14 mm)**
- **Direct Upgrade from 512K bit, 1M bit, and 2M bit (AT27C516, AT27C1024, and AT27C2048) EPROMs**
- **5V ± 10% Power Supply**
- **High Reliability CMOS Technology**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming Algorithm - 50 µs/word (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

Description

The AT27C4096 is a low-power, high performance 4,194,304 bit one-time programmable read only memory (OTP EPROM) organized 256K by 16 bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in less than 85 ns, eliminating the need for speed-reducing WAIT states. The by-16 organization makes this part ideal for high-performance 16 and 32 bit microprocessor systems.

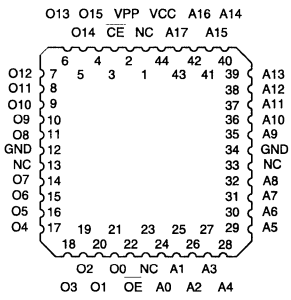
(continued)

Pin Configurations

Pin Name	Function
A0 - A17	Addresses
O0 - O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

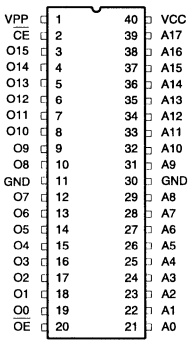
Note: Both GND pins must be connected.

PLCC Top View

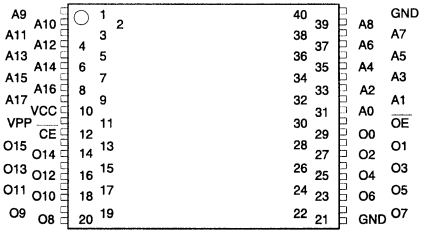


Note: PLCC pkg. pins 1 and 23 are DON'T CONNECT.

PDIP Top View



TSOP Top View
Type 1



0311D

Description (Continued)

In read mode, the AT27C4096 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C4096 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, and TSOP packages. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

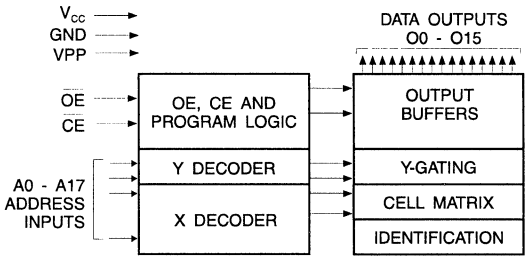
With high density 256K word storage capability, the AT27C4096 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's AT27C4096 has additional features that ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	Ai	X (1)	D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
Standby	V_{IH}	X	X	X (5)	High Z
Rapid Program (2)	V_{IL}	V_{IH}	Ai	V_{PP}	D_{IN}
PGM Verify	V_{IH}	V_{IL}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	V_{IH}	X	V_{PP}	High Z
Product Identification (4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A17 = V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to the Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9, which is set to V_H, and A0, which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP} = V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

DC and AC Operating Conditions for Read Operation

		AT27C4096			
		-85	-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		40	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

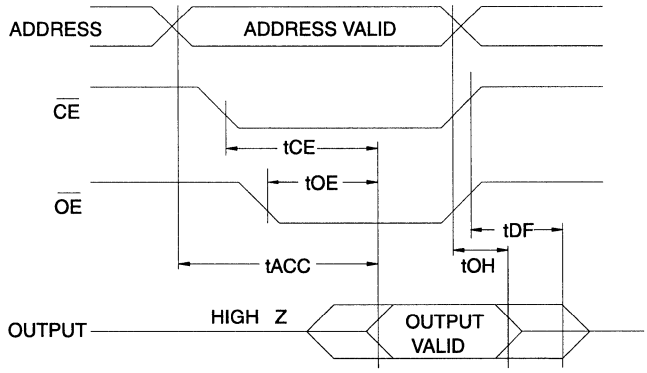
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C4096								
			-85		-10		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		85		100		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		85		100		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		40		40		40		50	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30		30		35		40	ns
t_{OH} (4)	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		0		0		0		ns

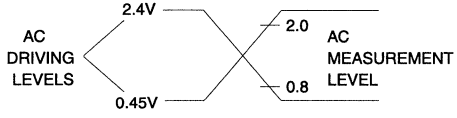
Notes: 2, 3, 4, 5. See the AC Waveforms for Read Operation diagram.

AC Waveforms for Read Operation [1]



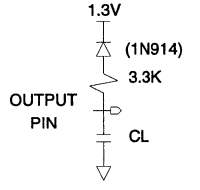
Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



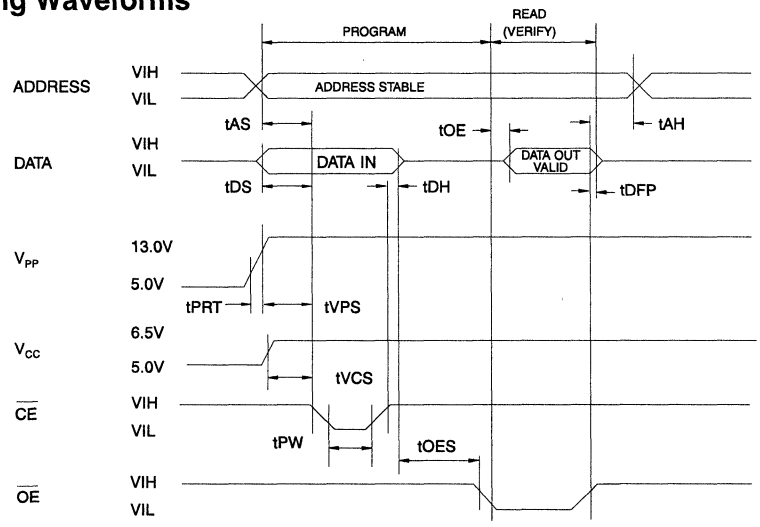
Note: CL = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C4096, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.7	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		47.5	52.5	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%) .....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level..... 0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

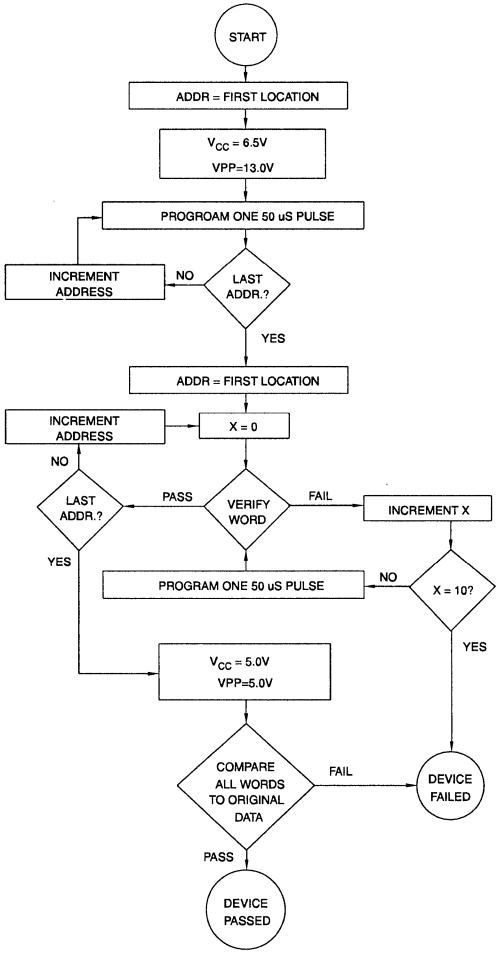
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Ouput Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 50 µsec ± 5%.

Atmel's 27C4096 Integrated Product Identification Code

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	1	0	0	00F4

Rapid Programming Algorithm

A 50 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
85	40	0.1	AT27C4096-85JC AT27C4096-85PC AT27C4096-85VC	44J 40P6 40V	Commercial (0°C to 70°C)
	40	0.1	AT27C4096-85JI AT27C4096-85PI AT27C4096-85VI	44J 40P6 40V	Industrial (-40°C to 85°C)
100	40	0.1	AT27C4096-10JC AT27C4096-10PC AT27C4096-10VC	44J 40P6 40V	Commercial (0°C to 70°C)
	40	0.1	AT27C4096-10JI AT27C4096-10PI AT27C4096-10VI	44J 40P6 40V	Industrial (-40°C to 85°C)
120	40	0.1	AT27C4096-12JC AT27C4096-12PC AT27C4096-12VC	44J 40P6 40V	Commercial (0°C to 70°C)
	40	0.1	AT27C4096-12JI AT27C4096-12PI AT27C4096-12VI	44J 40P6 40V	Industrial (-40°C to 85°C)
150	40	0.1	AT27C4096-15JC AT27C4096-15PC AT27C4096-15VC	44J 40P6 40V	Commercial (0°C to 70°C)
	40	0.1	AT27C4096-15JI AT27C4096-15PI AT27C4096-15VI	44J 40P6 40V	Industrial (-40°C to 85°C)

Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
40V	40 Lead, Plastic Thin Small Outline Package (TSOP) 10 x 14 mm

Features

- Fast Read Access Time - 100 ns
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 40 mA max. Active at 5 MHz
- JEDEC Standard Packages
  - 32-Lead 600-mil PDIP and Cerdip
  - 32-Lead 450-mil SOIC (SOP)
  - 32-Lead TSOP
- 5V ± 10% Supply
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 50 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Industrial and Commercial Temperature Ranges

8 Megabit (1M x 8) UV Erasable CMOS EPROM

3

Description

The AT27C080 chip is a low power, high performance 8,388,608 bit ultraviolet erasable programmable read only memory (EPROM) organized as 1M by 8 bits. The AT27C080 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 100 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

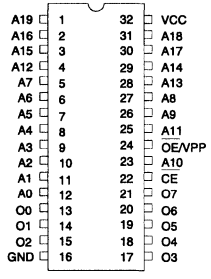
Atmel's scaled CMOS technology provides low active power consumption and fast programming. Power consumption is typically 10 mA in active mode and less than 10 µA in standby mode.

(continued)

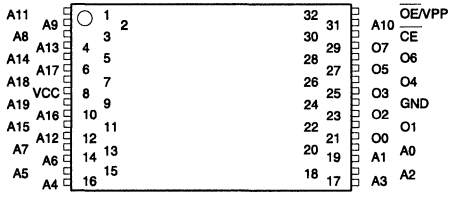
Pin Configurations

Pin Name	Function
A0 - A19	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

CDIP, PDIP, SOIC Top View



TSOP Top View
Type 1



0360D

Description (Continued)

The AT27C080 is available in a choice of packages, including; one-time programmable (OTP) plastic PDIP, SOIC (SOP), and TSOP, as well as windowed ceramic Cerdip. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 1M byte storage capability, the AT27C080 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C080 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

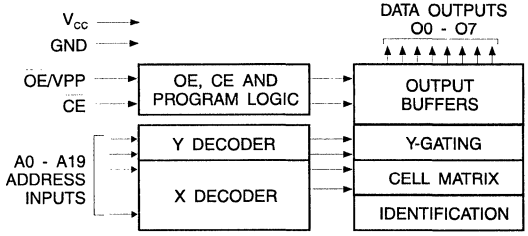
Erasure Characteristics

The entire memory array of the AT27C080 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

3

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	Outputs
Read	V_{IL}	V_{IL}	Ai	D_{OUT}
Output Disable	X	V_{IH}	X (1)	High Z
Standby	V_{IH}	X	X	High Z
Rapid Program (2)	V_{IL}	V_{PP}	Ai	D_{IN}
PGM Verify	V_{IL}	V_{IL}	Ai	D_{OUT}
PGM Inhibit	V_{IH}	V_{PP}	X	High Z
Product Identification (4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A19 = V_{IL}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27C080		
		-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}	Com., Ind.		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	Com., Ind.		±5	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V			100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}			40	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

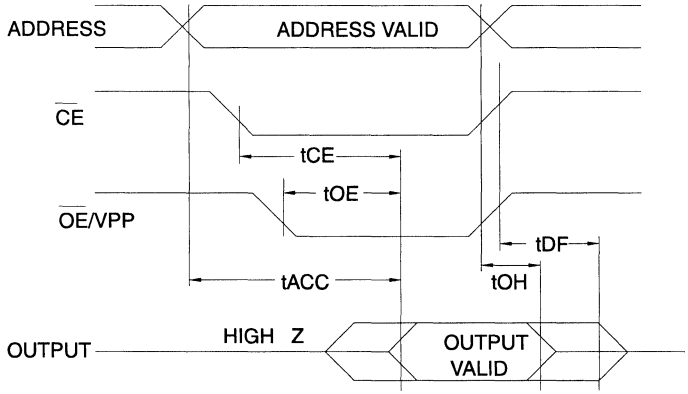
Note: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

AC Characteristics for Read Operation

			AT27C080						
			-10		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = VIL		100		120		150	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$ = V_{IL}		100		120		150	ns
t_{OE} (3, 4)	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$ = V_{IL}		35		35		40	ns
t_{DF} (2, 5)	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30		35		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first		0		0		0		ns

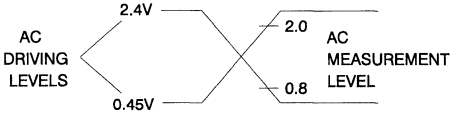
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

AC Waveforms for Read Operation [1]



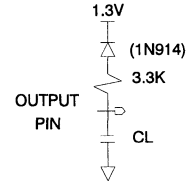
Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ /V_{PP} or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$/V_{PP} may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ /V_{PP} may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



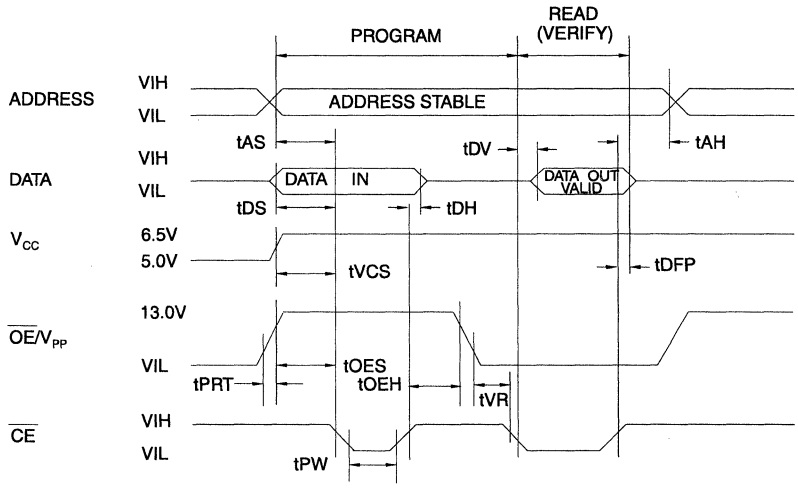
Note: CL = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, $\overline{OE}/V_{PP}$ = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, $\overline{OE}/V_{PP}$ = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay (2)		0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		47.5	52.5	µs
t_{DV}	Data Valid from $\overline{CE}$ (2)			1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

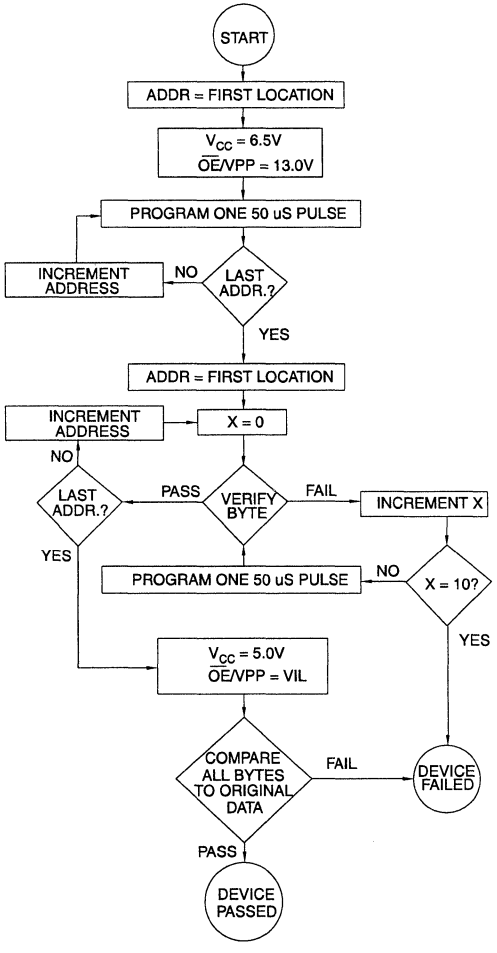
Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 50 µsec ± 5%.

Atmel's 27C080 Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	0	1	0	8A

Rapid Programming Algorithm

A 50 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	40	0.1	AT27C080-10DC AT27C080-10PC AT27C080-10RC AT27C080-10TC	32DW6 32P6 32R 32T	Commercial (0°C to 70°C)
120	40	0.1	AT27C080-12DC AT27C080-12PC AT27C080-12RC AT27C080-12TC	32DW6 32P6 32R 32T	Commercial (0°C to 70°C)
	40	0.1	AT27C080-12DI AT27C080-12PI AT27C080-12RI AT27C080-12TI	32DW6 32P6 32R 32T	Industrial (-40°C to 85°C)
150	40	0.1	AT27C080-15DC AT27C080-15PC AT27C080-15RC AT27C080-15TC	32DW6 32P6 32R 32T	Commercial (0°C to 70°C)
	40	0.1	AT27C080-15DI AT27C080-15PI AT27C080-15RI AT27C080-15TI	32DW6 32P6 32R 32T	Industrial (-40°C to 85°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32R	32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline (SOIC)
32T	32 Lead, Plastic Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 100 ns
- Word-wide or Byte-wide Configurable
- 8 Megabit Flash and Mask ROM Compatible
- Low Power CMOS Operation
  - 100 µA Maximum Standby
  - 50 mA Maximum Active at 5 MHz
- Wide Selection of JEDEC Standard Packages
  - 42-Lead 600 mil Cerdip and PDIP
  - 44-Lead SOIC (SOP)
  - 48-Lead TSOP (12 mm x 20 mm)
- 5V ± 10% Power Supply
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm- 50 µs/word (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27C8192 is a low-power, high performance 8,388,608 bit UV erasable programmable read only memory (EPROM) organized as either 512K by 16 or 1024K by 8 bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in less than 100 ns, eliminating the need for speed-reducing WAIT states. The by-16 organization makes this part ideal for high-performance 16 and 32 bit microprocessor systems.

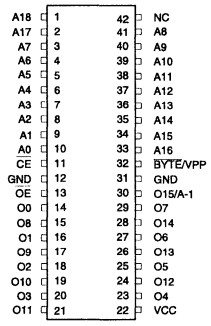
(continued)

Pin Configurations

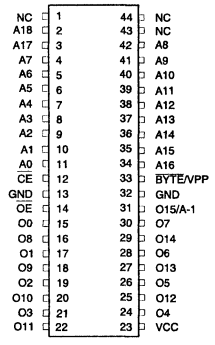
Pin Name	Function
A0 - A18	Addresses
O0 - O15	Outputs
O15/A1	Output/Address
$\overline{BYTE}$/VPP	Byte Mode/ Program Supply
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

Note: Both GND pins must be connected.

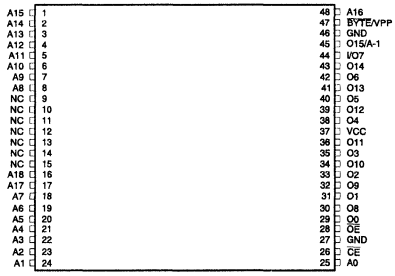
CDIP, PDIP Top View



SOIC (SOP)



TSOP
Type 1



8 Megabit (512K x 16 or 1024K x 8) UV Erasable CMOS EPROM

Preliminary

3

0643A

Description (Continued)

The AT27C8192 can be organized as either word-wide or byte-wide. The organization is selected via the $\overline{BYTE}$/VPP pin. When $\overline{BYTE}$/VPP is asserted high (V_{IH}), the word-wide organization is selected and the O15/A-1 pin is used for O15 data output. When $\overline{BYTE}$/VPP is asserted low (V_{IL}), the byte-wide organization is selected and the O15/A-1 pin is used for the address pin A-1. When the AT27C8192 is logically regarded as x16 (word-wide), but read in the byte-wide mode, then with A-1 = V_{IL} the lower 8 bits of the 16 bit word are selected and with A-1 = V_{IH} the upper 8 bits of the 16 bit word are selected.

In read mode, the AT27C8192 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C8192 is available in industry standard JEDEC-approved one-time programmable (OTP) PDIP, SOIC (SOP), and TSOP as well as UV erasable windowed Cerdip packages. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

With high density 512K word or 1024K bit storage capability, the AT27C8192 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's AT27C8192 has additional features that ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

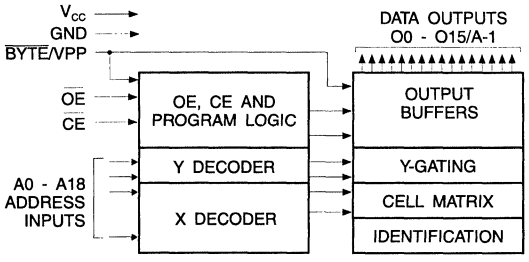
Erasure Characteristics

The entire memory array of the AT27C8192 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2,537Å. Complete erasure is assured after a minimum of 20 minutes of exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM that will be subjected to continuous fluorescent indoor lighting or sunlight.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



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Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
VPP Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)
Integrated UV Erase Dose	7258 W • sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	$\overline{BYTE}/V_{PP}$	Outputs O_0 - O_7	Outputs O_8 - O_{14}	Outputs O_{15}/A-1
Read Word-wide	V_{IL}	V_{IL}	X (1)	V_{IH}	D_{OUT}	D_{OUT}	D_{OUT}
Read Byte-wide Upper	V_{IL}	V_{IL}	X (1)	V_{IL}	D_{OUT}	High Z	V_{IH}
Read Byte-wide Lower	V_{IL}	V_{IL}	X (1)	V_{IL}	D_{OUT}	High Z	V_{IL}
Output Disable	X (1)	V_{IH}	X (1)	X	High Z		
Standby	V_{IH}	X (1)	X (1)	X (5)	High Z		
Rapid Program (2)	V_{IL}	V_{IH}	Ai	V_{PP}	D_{IN}		
PGM Verify	X	V_{IL}	Ai	V_{PP}	D_{OUT}		
PGM Inhibit	V_{IH}	V_{IH}	X (1)	V_{PP}	High Z		
Product Identification (4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A18 = V_{IL}	V_{IH}	Identification Code		

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to the programming characteristics tables in this data sheet.
3. V_H = 12.0 ± 0.5V.
4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9, which is set to V_H, and A0, which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP} = V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

DC and AC Operating Conditions for Read Operation

		AT27C8192		
		-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		± 1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		± 5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		50	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

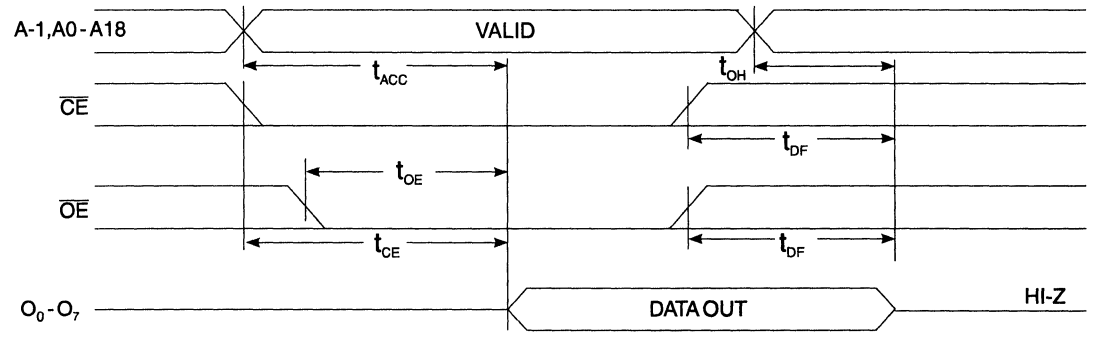
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C8192						
			-10		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		100		120		150	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		100		120		150	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		40		40		50	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30		35		40	ns
t_{OH} (4)	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		5		5		5		ns
t_{ST}	$\overline{BYTE}$ High to Output Valid			100		120		150	ns
t_{STD}	$\overline{BYTE}$ Low to Output Transition			40		50		60	ns

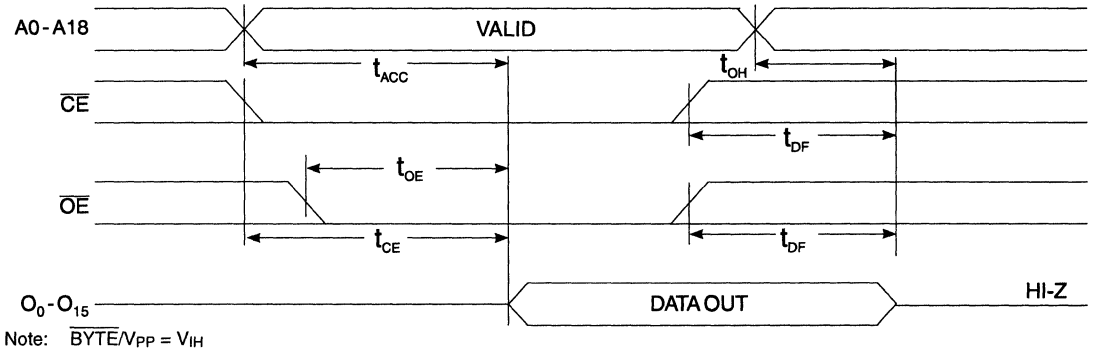
Notes: 2, 3, 4, 5. See the AC Waveforms for Read Operation diagram.

Byte-Wide Read Mode AC Waveforms



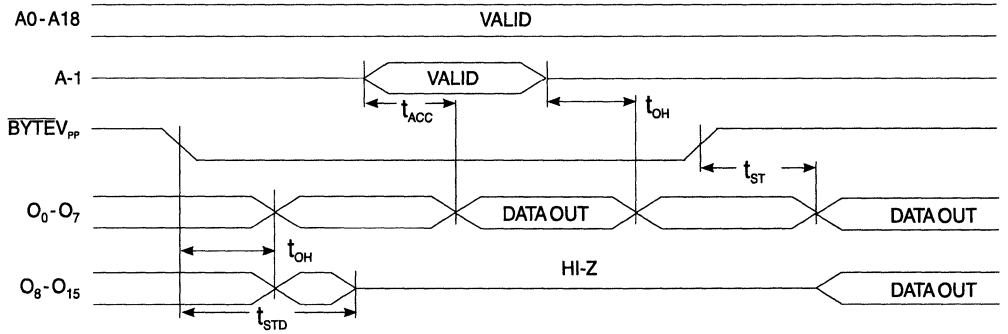
Note: $\overline{BYTE}/V_{PP} = V_{IL}$

Word-Wide Read Mode AC Waveforms



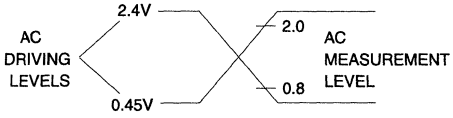
Note: $\overline{BYTE}/V_{PP} = V_{IH}$

$\overline{BYTE}$ Transition AC Waveforms



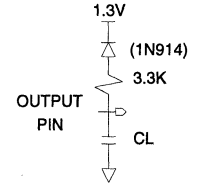
Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



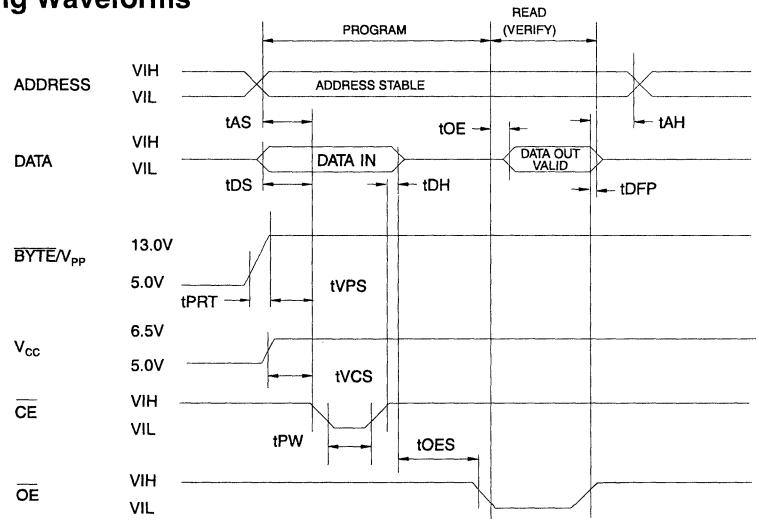
Note: CL = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C8192, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions* (1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width (3)		47.5	52.5	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	$\overline{BYTE}$/VPP Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%) .....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level..... 0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

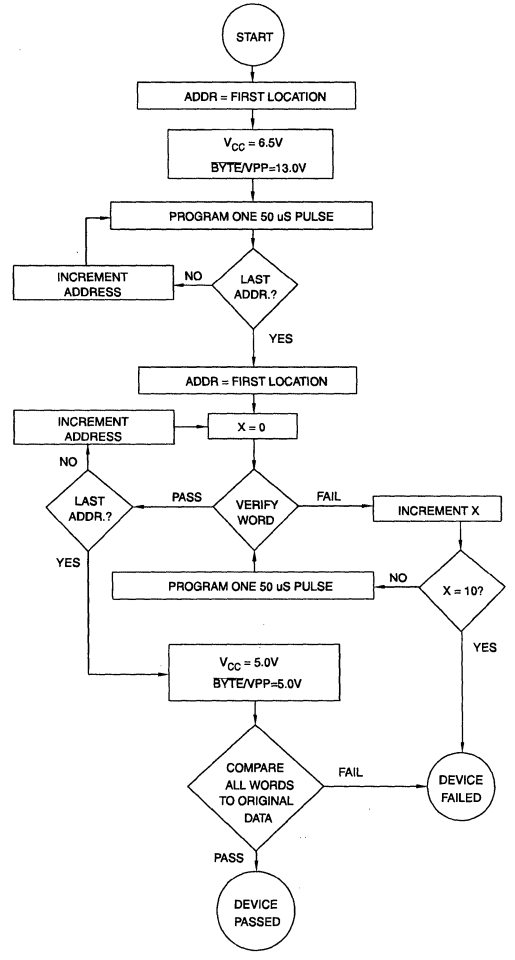
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Ouput Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 50 µsec ± 5%.

Atmel's 27C8192 Integrated Product Identification Code

Codes	Pins A0	O15 O7	O14 O6	O13 O5	O12 O4	O11 O3	O10 O2	O9 O1	O8 O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E1E
Device Type	1	1	1	1	1	1	0	0	0	F8F8

Rapid Programming Algorithm

A 50 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{BYTE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



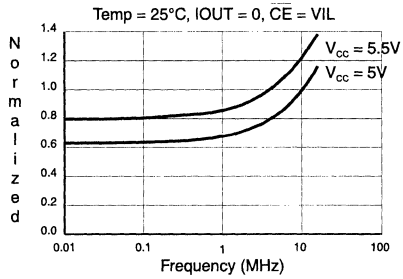
Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	50	0.1	AT27C8192-10DC AT27C8192-10PC AT27C8192-10RC AT27C8192-10TC	42DW6 42P6 44R 48T	Commercial (0°C to 70°C)
	50	0.1	AT27C8192-10DI AT27C8192-10PI AT27C8192-10RI AT27C8192-10TI	42DW6 42P6 44R 48T	Industrial (-40°C to 85°C)
120	50	0.1	AT27C8192-12DC AT27C8192-12PC AT27C8192-12RC AT27C8192-12TC	42DW6 42P6 44R 48T	Commercial (0°C to 70°C)
	50	0.1	AT27C8192-12DI AT27C8192-12PI AT27C8192-12RI AT27C8192-12TI	42DW6 42P6 44R 48T	Industrial (-40°C to 85°C)
150	50	0.1	AT27C8192-15DC AT27C8192-15PC AT27C8192-15RC AT27C8192-15TC	42DW6 42P6 44R 48T	Commercial (0°C to 70°C)
	50	0.1	AT27C8192-15DI AT27C8192-15PI AT27C8192-15RI AT27C8192-15TI	42DW6 42P6 44R 48T	Industrial (-40°C to 85°C)

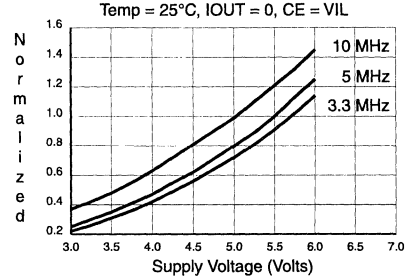
Package Type	
42DW6	42 Lead, 0.600" Wide, Ceramic Dual Inline Package (CDIP)
42P6	42 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44R	44 Lead, 0.525" Wide, Plastic Gull Wing Small Outline Package (SOIC/SOP)
48T	48 Lead, Plastic Thin Small Outline Package (TSOP) 12 x 20 mm

EPROM Product Characteristics for AT27CXXX Series Parts

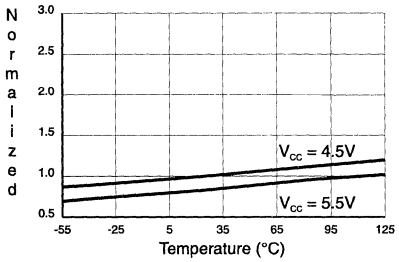
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



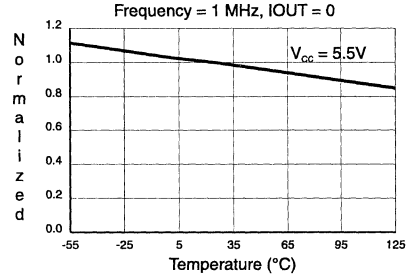
NORMALIZED SUPPLY CURRENT vs. VOLTAGE



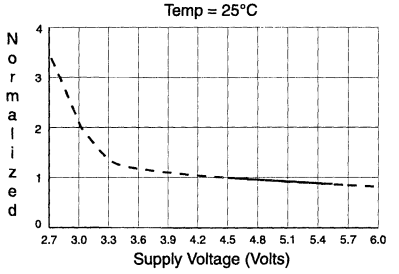
NORMALIZED ACCESS TIME vs. TEMPERATURE



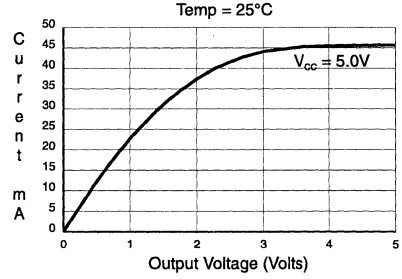
NORMALIZED SUPPLY CURRENT vs. TEMP.



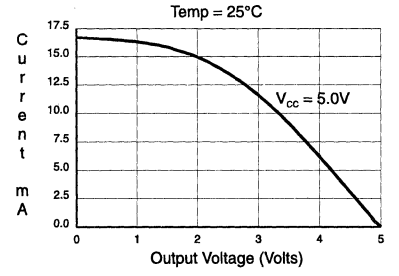
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



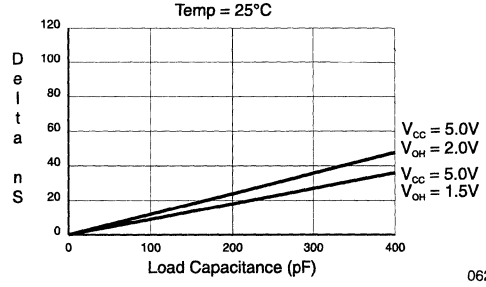
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



DELTA ACCESS TIME vs. LOAD CAPACITANCE



0623A

Interfacing Atmel LV/BV EPROMs on a Mixed 3-Volt/5-Volt Data Bus

Introduction

Interfacing Atmel Corporation's low voltage (LV/BV) EPROMs on a common data bus with standard 5-volt devices can be achieved with relative ease if a few simple guidelines are followed. By controlling the data bus voltages and currents, problems associated with latchup, electromigration and battery damage can be eliminated. This application note describes each problem, along with recommended solutions, and analyzes the associated tradeoffs.

Background

Definition of Terms:

A. *Latchup* – a destructive phenomenon associated with CMOS-based semiconductors. Parasitic SCRs (silicon-controlled rectifiers or p-n-p-n devices) exist on inputs and outputs. Once an SCR is activated, it can conduct high current. The current can only be turned off by disconnecting the power supply.

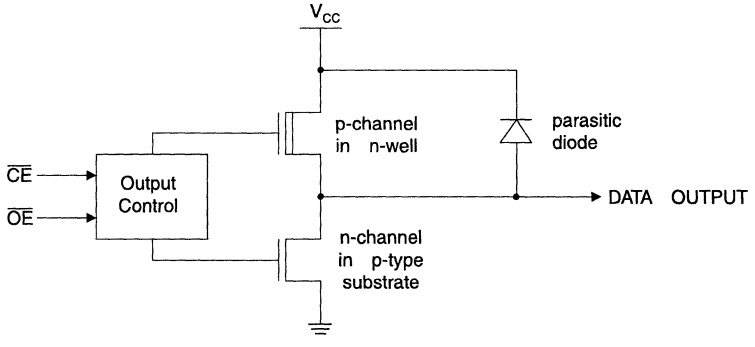
B. *Electromigration* – Metal interconnects in semiconductors are carefully sized to ensure they are wide enough to safely carry the amount of current required by the design. The interconnects may physically open up when these limits are exceeded for a long time.

C. *Venting* – When a battery overheats (as a result of dissipating excessive power) the battery case may open, allowing the contents of the battery to be "vented" or leaked to the outside world. This is both messy and potentially dangerous.

Understanding issues related to interfacing Atmel LV/BV EPROMs with standard 5-volt devices requires an understanding of the EPROM output. The output is basically a CMOS inverter constructed with p-channel pull-up and n-channel pull-down transistors (see Figure 1). The source of the p-channel and the n-well are connected to V_{CC}. The source of the n-channel and the substrate are con-

(continued)

Figure 1. Atmel LV/BV CMOS EPROM Output Buffer



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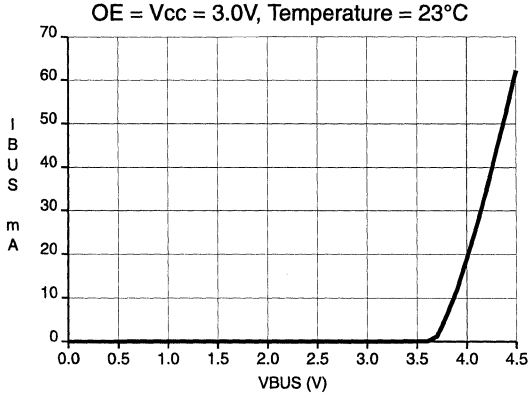
Background (Continued)

nected to ground. It is important to note that the p+ drain of the p-channel device in the n-well forms a parasitic p-n diode. The parasitic diode is between the output of the LV/BV part and the V_{CC} supply, with the diode cathode connected to V_{CC} and the anode connected to the output node. If the Atmel LV/BV EPROM is operated from a 3-volt supply and the output node rises to 3.7 volts, the parasitic p-n junction is forward biased by 0.7 volts and will conduct current. This diode current will flow even though the LV/BV EPROM output is supposed to be tri-stated (high-Z) via the CE or OE control signals. The room temperature I/V characteristic of the diode is shown in Figure 2. The y-axis of the graph, designated "IBUS," represents the DC current flowing from the bus into the Atmel LV/BV EPROM output. The x-axis, designated "VBUS," is the data bus voltage when the supply level of the LV/BV EPROM is exactly 3.0 volts. For example, if the voltage on the data bus is 4.0 volts, the corresponding diode current into the LV/BV part's output is approximately 20 mA. If VBUS is increased to 4.5 volts, the corresponding diode current in just one output increases to 60 mA, and would be destructive over time. It is important to note that the LV/BV EPROM data sheets refer to output pin voltage. The data sheet section under "Absolute Maximum Ratings" specifically states that the "Maximum output pin voltage is V_{CC} + 0.75VDC which may be exceeded if certain precautions are observed." What does this mean? It means that, because of the effects demonstrated by the parasitic diode, voltages on the output pins in excess of V_{CC} + 0.75 volts can cause large currents to flow into the EPROM outputs and short the two power supplies together (see Figure 3).

Each Atmel EPROM output is designed to withstand an IBUS current of less than 10 mA without any exposure to electromigration, and over 200 mA without latchup. Since the current capability for latchup is so much larger than the amount of current required to induce electromigration, it is clear that the electromigration requirement will dictate the maximum IBUS current. The balance of this application note focuses on ensuring by system design that the magnitude of the IBUS current into the EPROM is less than 10 mA. The effects of exceeding the normal output voltage of the LV/BV supply (over-volting) will not be discussed in detail here. Those characteristics should be obtained from the battery or voltage regulator manufacturers.

Figure 2. Atmel LV/BV EPROM IBUS versus VBUS



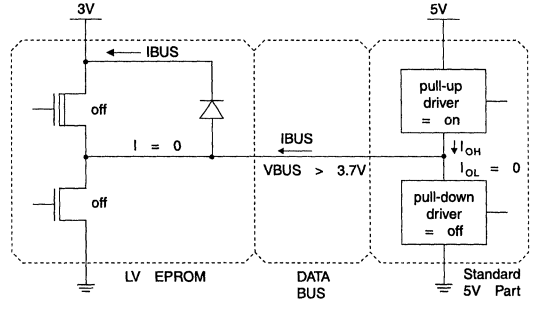
Results

Clearly, the most attractive design option is to select 5-volt bus driver devices which do not have strong output drive current (I_{OH}) capability. An example of this type of device is a 8096 microcontroller. Its I_{OH} characteristic is shown in Figure 4. We are only concerned about how much I_{OH} (= IBUS) the 8096 can supply into the LV/BV EPROM above a V_{OH} (= VBUS) of 3 volts. The maximum current the 8096 can supply when its V_{OH} is above 3 volts is less than the 10 mA allowed to safely enter the LV/BV EPROM. Therefore, electromigration is not a concern in this case. However, allowing both power supplies to couple across the parasitic diode of the LV/BV EPROM may still speed the discharge of a 5-volt battery and may cause the 3-volt battery to overheat and vent.

Contrast the 8096 example with the output characteristics of a high-current output drive 74HC00 CMOS logic gate (Figure 5). Note how the amount of I_{OH} current available above a 3-volt V_{OH} can be 30 mA, more than triple the maximum safe IBUS current to prevent electromigration. What actual IBUS will occur when such a 74HC00 part (connected to a 5-volt supply) is driving an Atmel LV/BV EPROM (connected to a 3-volt supply)? The answer can be obtained using a graphical technique called *load line analysis*.

(continued)

Figure 3. Parasitic Diode in LV/BV Output Shorts 3-Volt and 5-Volt Supplies



Results (Continued)

With load line analysis, you can find the maximum DC IBUS and VBUS values for any situation. For example, continue the analysis for the 74HC00 part to see what the actual IBUS current will be. A load line is created by simply superimposing the Atmel LV/BV EPROM IBUS versus VBUS curve (Figure 2) with the 74HC00 I_{OH} versus V_{OH} curve (Figure 5). Figure 6 is the resulting load line. The place the two curves intersect is called the *operating point* and gives an IBUS value of about 20 mA. The data bus will then sit at a VBUS voltage of about 4 volts. This analysis confirms the suspicion that using a 74HC00 will not be safe. Recall that you want an IBUS value below 10 mA to prevent reliability damage to the LV/BV EPROM.

The type of curves used in this load line analysis can be easily obtained for any conditions and any part. You should beware to use curves obtained for the worst case conditions that the system will encounter. Most I_{OH} and V_{OH} data sheet specifications are minimum values and sometimes grossly understate the real current drive capability of a part. When was the last time you encountered a CMOS part with only 400 µA I_{OH} at 2.4 volts V_{OH}? Such a specification is a holdover from the days when an NMOS design was considered fast at 500 ns. Many data sheets provide output drive curves only for typical conditions (i.e., V_{CC} = 5V, temperature = 25°C). Most data sheets also provide data for only the minimum output drive since most

(continued)

Figure 4. I_{OH} versus V_{OH} for 8096

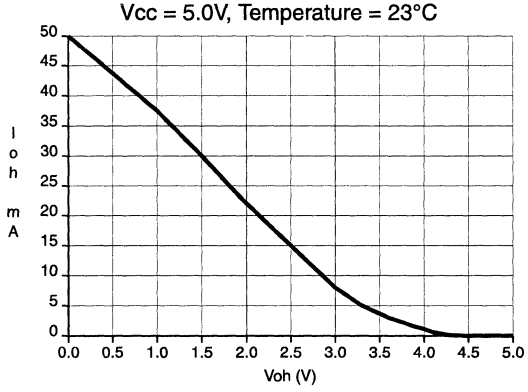


Figure 5. I_{OH} versus V_{OH} for 74HC00

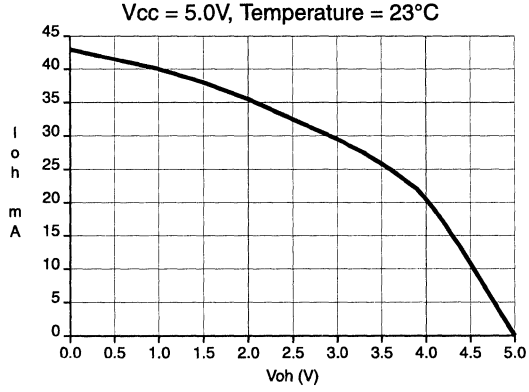


Figure 6. 74HC00 Load Line on LV/BV EPROM

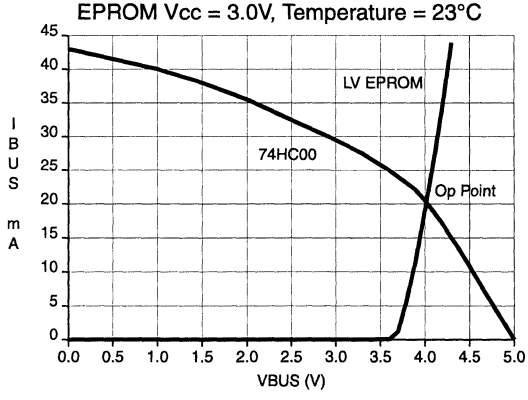
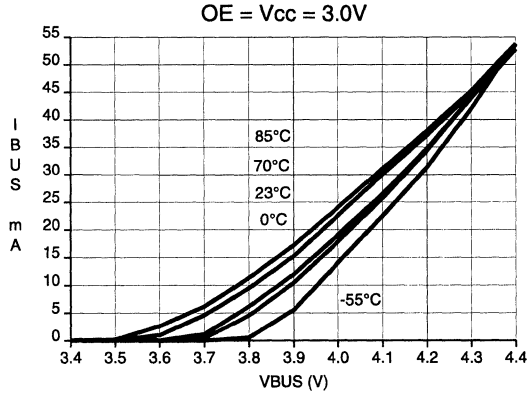


Figure 7. LV/BV IBUS versus VBUS versus Temperature



Results (Continued)

customers are worried if the part has enough current drive for a heavily loaded bus line. However, for this mixed power supply design analysis we need the maximum output drive current for the 5-volt driven part. The conditions for that maximum output current would occur at lowest temperature and highest V_{CC}, and with only one output driving. The last condition is due to the parasitic resistance in a chip's package and die metal. That resistance will cause a voltage drop inside the chip that will decrease the output current drive. On parts with more than one output, the highest I_{OH} current will occur when the internal voltage drop is minimum or when only one output is driving. The variation in I_{OH} with number of outputs driving, V_{CC}, and temperature will exceed the variations due to processing in most chips today. You may have to measure the I_{OH} characteristics yourself to get the data you need.

The Atmel LV/BV EPROM IBUS versus VBUS characteristics will also need to be measured at conditions giving the highest current for the load line operating point. That current will depend strongly on the V_{CC} used for the LV/BV parts. The higher the LV/BV V_{CC}, the higher the bus voltage can go before forward-biasing the parasitic diode in the LV/BV part. For the load line analysis, the LV/BV EPROM IBUS versus VBUS curve measured at V_{CC} = 3V is shifted to the right by the difference between the LV/BV supply voltage to be used and 3-volts. Increasing the LV/BV V_{CC} will reduce IBUS quickly since I_{OH} for the 5-volt part decreases rapidly as the operating point moves to the right. The worst case LV/BV IBUS versus VBUS curve will be obtained for highest temperature, lowest V_{CC}, and a single output high. Figure 7 shows the LV/BV EPROM IBUS as a function of VBUS for a range of temperatures from -55°C to 85°C.

In some applications, there may be requirements for a high output current 5-volt device or no alternate part available with limited I_{OH}. The following techniques may be useful in that case. One technique is to clamp the bus with respect to ground. Clamp the bus so that the parasitic p-n junction in the LV/BV part cannot be forward biased. A 3-volt zener diode with grounded anode and cathode connected to the data bus can provide protection for a mixed 3-volt/5-volt system (Figure 8). 1N4370A- or 1N746A-series zener diodes could be used. The trade-off is the power dissipated by the zeners. A 3-volt zener shunting 20 mA of current will consume 60 mW of power. For eight outputs, this could be as high as 480 mW, which is a significant amount of power to waste in a battery environment. This will speed the discharge of the 5-volt battery, but does a very good job of protecting the 3-volt supply from over-volting (or possibly venting the 3-volt battery).

Another technique is to add a small series resistor on each of the LV/BV part's outputs (Figure 9). The resistor will limit the IBUS current. Figure 10 uses the 74HC00 example again to show how the load line plot from Figure 6 is used to quickly calculate the value of series resistance needed. You want to move the IBUS operating point from

(continued)

Figure 8. Zener Clamp Bus to 3 Volts

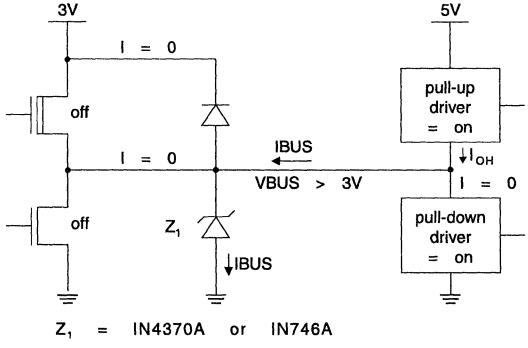
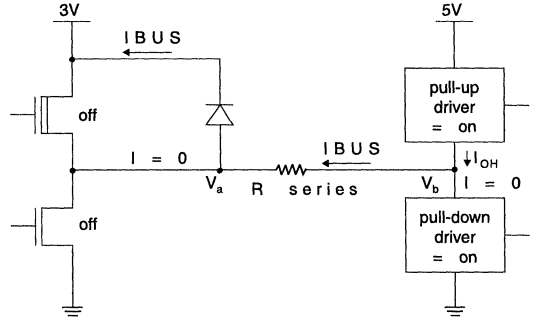


Figure 9. Series Output Resistor Reduces IBUS



Results (Continued)

the original 20 mA down to 10 mA. The circuit consists of the original 74HC00 pull-up circuit, represented by the original load line, and the new series resistor. The current in the resistor and the pull-up will be the same since they are in series and should be set to our recommended safe 10 mA level. In Figure 10 you will see two points called V_a and V_b which are where the LV/BV EPROM and 74HC00 pull-up load lines intersect the 10 mA IBUS current level. The difference between V_b and V_a will be the voltage drop across the series resistor when 10 mA of current is flowing. The series resistance Rseries is then calculated by the formula:

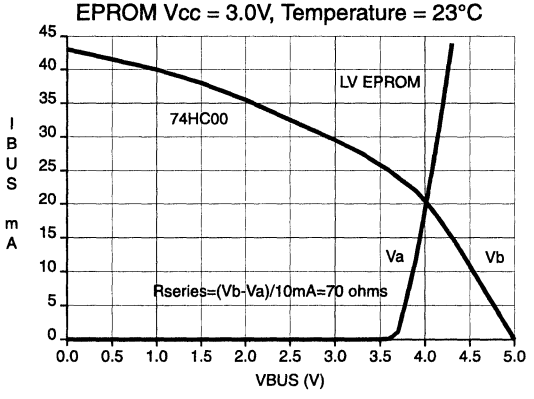
$$Rseries = (Vb - Va) / Idesired$$
$$= (4.55 - 3.85)\ V / 10\ mA$$
$$= 70\ ohms$$

The power dissipated in each resistor would be given by:

$$Pseries = Idesired^2 \times Rseries$$
$$= (10\ mA)^2 \times 70\ ohms$$
$$= 7\ mW$$

For eight outputs, the series resistor method only drains 56 mW from the 5-volt supply, which is much less power than that wasted by the zener circuit. Notice that the 3-volt supply will still be over-volted by 0.85 volts. You still need to determine if that over-volting will cause excessive battery heating and a possible venting problem. The resistor's effect on bus signal speed will probably not be detrimental since the 70 ohms needed in this example is just slightly higher than the value used for a series transmission line termination. It may be necessary to place the series resistors between the high output drive part and the common data bus. That way the resistors are only in the circuit when the high output part is driving the bus, and lower drive current parts will not be current-limited. Also, remember this example was done for room temperature and a 5-volt supply on the 74HC00. For higher temperature, the 74HC00 will have less current drive, but the parasitic LV/BV EPROM diode will start to forward bias at a lower VBUS value. You may need to do several load line models before finding a design that covers the worst case temperature and power supply conditions for a particular system.

Figure 10. Calculating Rseries for 74HC



Conclusion

Interfacing Atmel LV/BV EPROMs on a common data bus with standard 5-volt devices can be achieved if the output drives of the 5-volt powered parts are controlled through careful device selection or by adding external components. The problems to avoid are:

- failure of the LV/BV part due to electromigration, and
- battery venting of the LV/BV supply.

Following these guidelines will allow design of mixed power supply systems which exhibit sound component and system reliability.

The Benefits of Atmel's RAPID™ Programming Algorithm

Introduction

In designing and manufacturing certain modern-day products, the methods used to build these products are often as important to the design engineer as the components themselves. This is true about programmable memory devices as well, especially EPROMs. Most EPROM vendors use their own unique programming algorithm, which is based on the process used to make EPROMs, the design engineer needs to know about the algorithm during the system design cycle to insure that the EPROMs can ultimately be programmed.

This application note details the Atmel RAPID programming algorithm and briefly explains why this algorithm is superior to others. In addition, it will give an introduction to EPROM technology and the mechanics of programming. These should provide a basic understanding in the growing field of EPROMs.

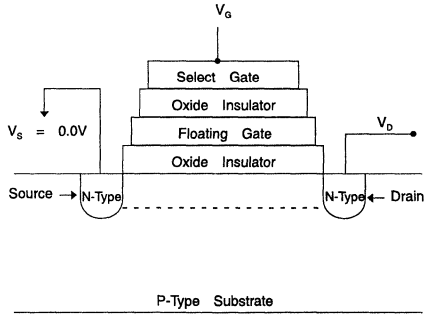
Programming EPROMs the RAPID™ Way

Several years ago, when Atmel reduced the geometry of its EPROM products from 1.5µ to 1.2µ linewidth, the Company adopted an entirely new programming algorithm for these devices. A reason for this algorithm change was to improve programming yields and lengthen long-term data retention. This was accomplished by using a shorter programming-pulse length during programming. The new RAPID algorithm reduces the 1 ms programming pulse width of the original FAST algorithm to only 100 µs, and it completely eliminates extra overprogramming pulses. The advantages of the RAPID programming algorithm are production proven even with today's advanced 0.5 micron EPROM technology.

But higher yields and increased reliability aren't the only benefits the RAPID algorithm provides, it also takes less time

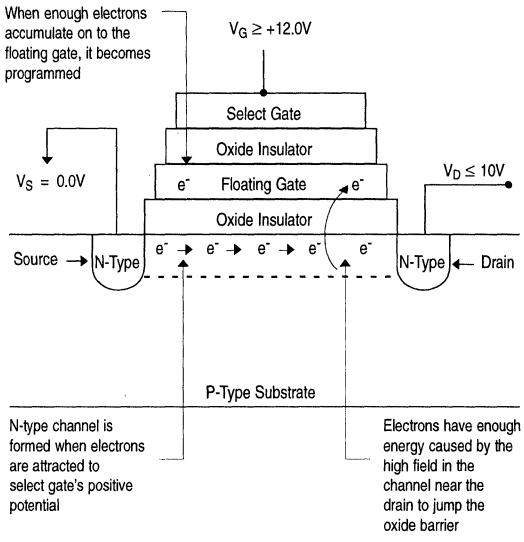
(continued)

Figure 1. Cross section of a typical EPROM cell.



0578A

Figure 2. Process of hot-electron injection.



Programming EPROMs the RAPID Way (Continued)

to program these devices. The RAPID algorithm can reduce the programming overhead costs by a factor of 40! Here's how it works:

If you program an AT27C512R, 512K EPROM in a single-device programmer, using the FAST or any other type of 1 ms algorithm (1 ms initial pulse, plus 3 ms overprogramming pulse) the time spent programming will be:

524288 bits ÷ 8 bits/byte = 65536 bytes

65536 bytes x .004 seconds/byte = 262 seconds

That's 262 seconds, or 4 minutes and 22 seconds. This works out to about a 75 cents programming cost, assuming an operator's rate of $10 per hour. Here's where the cost savings start: since we cannot reduce the number of bits to program, we reduce the total programming time by shortening the programming pulse width. Using 100 µs per byte, this is what happens:

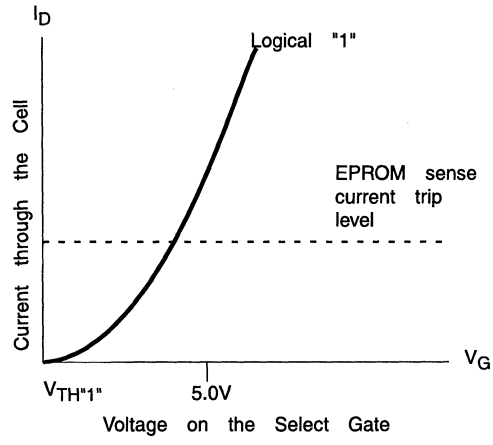
65536 bytes x .0001 seconds/byte = 6.5 seconds

This amount of programming-time savings is what can be expected when using the RAPID algorithm. The big improvement is from reducing the total byte-programming time from 4 ms to 100 µs. With this example, total programming cost is about three cents. The RAPID algorithm can actually save up to 72 cents per device. Imagine how much can be saved with 10,000 EPROMs!

There's more to the RAPID algorithm than shorter programming times and cost savings. It has a special way of checking that each cell is correctly programmed, and that cells are programmed with the required amount of charge. In fact, the RAPID algorithm even guarantees that the EPROM is correctly programmed. Programming algorithms of the FAST type, or their relatives, the QUICK-PULSE types, check each memory location for the programmed data immediately after programming that location. This check, which takes place before the final verify at the end of the programming cycle, is basically an "insurance" check, because it is performed at an elevated voltage, which is a worst-case condition. There is a flaw, however, in this type of programming algorithm: memory locations that have been previously programmed can be partially erased by programming subsequent locations (due to the elevated voltage on the same row or column in the memory array) and marginally programmed cells will go virtually undetected. The question is, doesn't the programmer check each device during verify after programming? Wouldn't those failures be caught then? Not necessarily, because when parts are checked during the program verify mode, the voltage is not elevated as high as it was during programming.

(continued)

Figure 3. Unprogrammed cell.

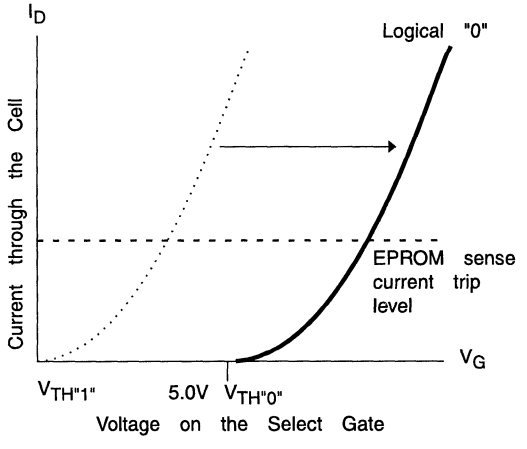


Programming EPROMs the RAPID Way (Continued)

The RAPID programming algorithm was designed to fix this oversight. First, it goes through the entire device and programs every cell without checking. Then it goes back to the beginning of the memory array and verifies the data in each cell at the elevated voltage. Once the device passes, another final verification is done at 5V. The RAPID algorithm will do a better job at preventing any marginally programmed parts from passing the programmer than other algorithms.

An important fringe benefit of the RAPID algorithm, because of the way it guarantees successful programmability, is long-term data retention. Basically, long-term data retention is how long the EPROM stays programmed, which is typically greater than ten years. Although long-term data retention is not the same as device programmability, they are related in this way: programmability tells how well the electrons have accumulated on the EPROM's floating gate, long-term data retention tells how long the electrons will stay there. The programming algorithm has an overwhelming influence on programmability, making it an overwhelming influence on long-term data retention as well. Therefore, a poor programming algorithm, one that doesn't guarantee programmability, can be responsible for poor long-term data retention. The RAPID algorithm can add years of data retention to your parts, because of the way it checks for programmability. Marginally programmed parts just don't stand a chance of getting past the programmer.

Figure 4. Programmed cell. Note how V_{TH} raises after electrons are accumulated on the EPROM floating gate from programming.



EPROM Programming, How it Works

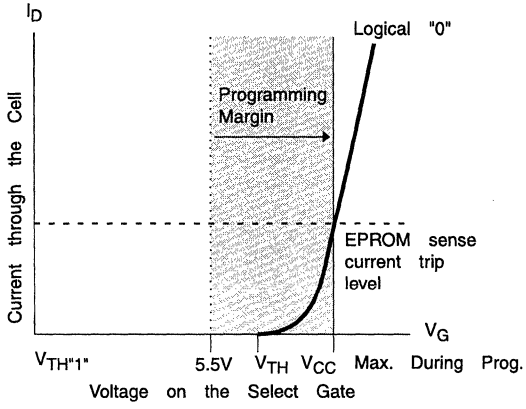
Contemporary EPROM programming algorithms can be divided into two main sections, programming and verifying (or reading). Programming begins by selecting the desired voltage levels and byte address. It continues with a programming pulse applied to that byte, followed by a verify at the elevated V_{CC} used for programming. Verifying checks the data in two passes with the original data, with V_{CC} set to 5.5V on the first pass, and 4.5V on the second.

Basically, EPROMs are programmed through the accumulation of electrons on the floating gate of an N-Channel EPROM cell (see Figure 1) by the process of hot-electron injection. Hot-electron injection is where electrons, flowing as a current between the drain and source of a saturated EPROM cell, gain enough energy from the high electric field to jump the oxide barrier between the channel and the floating gate (see Figure 2). Before programming, the MOS threshold voltage, V_{TH} (otherwise known as the gate threshold voltage) of the erased floating-gate EPROM cell is about 1.0V to 2.0V (see Figure 3). After programming, its threshold voltage is about 6.5V to 9.0V, due to the accumulated electrons on the floating gate. In read mode, the address decoding circuitry in the chip selects the desired cell by pulling the gate voltage of the cell to V_{CC}. Since V_{CC} is typically 4.5V to 5.5V, an erased cell with a V_{TH} = 1.5V would be turned on (Figure 3), while a programmed cell with a V_{TH} = 7.5V would remain off (see Figure 4). This floating-gate process is how a single MOSFET-like transistor can provide for the two logic levels used in digital circuitry.

If V_{CC} is gradually raised in voltage to a point near the threshold voltage of a programmed EPROM cell, the cell would just begin to conduct, and would no longer appear to be programmed. This point, where the programmed EPROM cell begins to look unprogrammed, is defined as the programming margin (see Figure 5). The value of the programming margin can, in some cases, be simply equal to the value of the V_{CC} voltage present during programming. This is why the RAPID algorithm holds the value of V_{CC} constant at 6.5V during programming; to insure that each EPROM cell has a programming margin of at least that voltage. This margin is verified by reading each byte twice, once during the initial programming operation and again during the final read (or verify) operation, where the data from the EPROM is compared to the desired data. The difference between the value of V_{CC} during programming (the guaranteed programming margin) and the 5.5V V_{CC} maximum supply rating (from the data sheet) serves as a reliability guardband for long-term data retention and, more importantly, for system noise immunity. Poor programming margin can reduce system noise immunity and lead to EPROM chip instability due to power-supply noise

(continued)

Figure 5. Programming margin. To find programming margin, increase gate voltage (V_{CC}) until the first "0" turns into a "1."



EPROM Programming, How it Works (Continued)

on the V_{CC} pin. This instability can cause oscillations and read-mode data glitching that can be a problem in even in the slowest and most noiseless of systems. Since power-supply noise is a somewhat random occurrence, data errors can happen intermittently, which can undermine the reliability and integrity of the host system. These problems can be avoided by using the programming algorithm recommended by the EPROM chip vendor. The higher the guaranteed programming margin, the less likely any problems will occur.

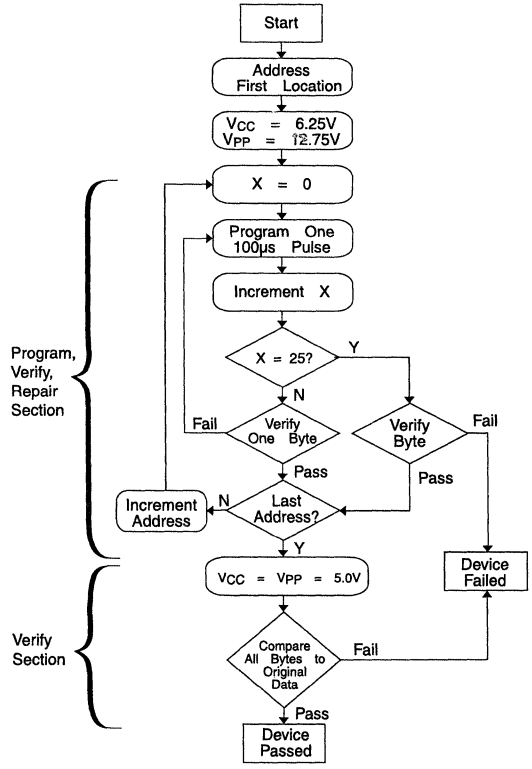
Another important benefit of high-programming margin is that it extends the long-term data retention of the device. If the 6.0V programming margin (FAST algorithm) on the EPROM gradually diminishes to 5.5V over a 10-year time span, the randomly occurring noise spikes on the V_{CC} line can cause the EPROM to yield faulty data. On the other hand, given the same discharge rate (as a function of the silicon processing), an EPROM with a programming margin of 6.5V (RAPID algorithm) would take over 20 years to reach the 5.5V threshold that would lead to faulty data yield. All things being equal, better programming margin leads to longer data retention.

Guaranteeing Programmability

Most people might ask, "What's in a programming algorithm? Aren't they all the same?" That question would have been answered with a resounding "YES" 10 years ago when, quite frankly, they were the same. But it's not true today. There are over 20 manufacturers making EPROMs, and few of them use the same programming algorithm. Today, the programming algorithm is as important to EPROM testing as the actual device testing procedure. In fact, the device test procedures are often (if not always) based upon the programming algorithm. The programming algorithm has a direct effect on EPROM test yield, and manufacturers select their programming algorithms so they can obtain the highest yield possible. Additionally, the programming algorithm is directly responsible for the number of devices that pass the customers pro-

(continued)

Figure 6. QUICK-PULSE type.



Guaranteeing Programmability (Continued)

grammer, which is called programming yield. This is of vital importance to an EPROM manufacturer like Atmel, since the worst place for an EPROM to fail programming is in the customer's programmer. With this in mind, let's look at how the RAPID algorithm can guarantee better programmability than a common type of quick-pulsing algorithm.

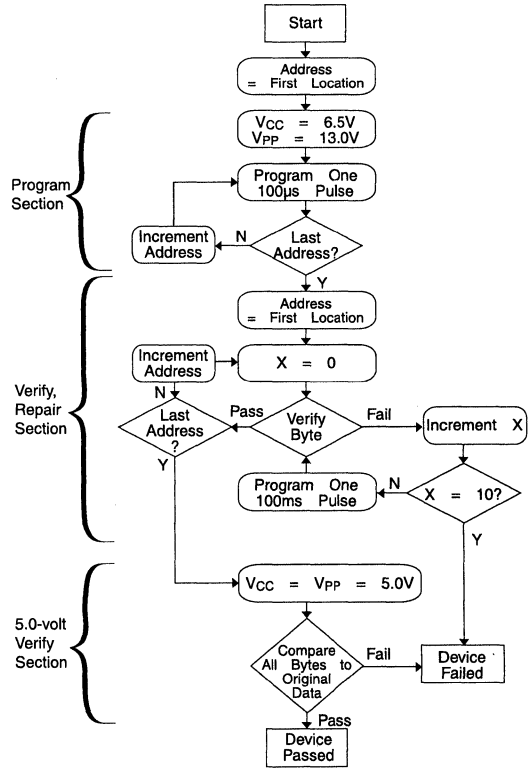
We'll begin by comparing a common type of quick-pulsing algorithm with the Atmel RAPID algorithm. Examine Figure 6, which is the flowchart for the QUICK-PULSE type of algorithm. If you look very closely you will see that the algorithm is broken up in to two major sections. The main part is the program/verify section, the other part is the final verify section. Basically, the first section starts at byte address 0000H, programs the eight EPROM cells at that address, and verifies that those cells contain the correct data with a verify at 6.25V on V_{CC}. If the byte passes, it goes on to the next byte. If it fails, it repeats everything up to 25 times before it fails the device. The second section lowers the V_{CC} voltage to 5.0V and checks if all address locations read with the correct data. Although the flowchart specifies a one-pass final verify at 5.0V, many programmers verify in two passes, one with V_{CC} at 4.75V and the other with V_{CC} at 5.25V.

Now examine Figure 7, the Atmel RAPID algorithm. It looks similar to the quick-pulsing type of algorithm, but with a slight difference. If you look closely you'll see that it consists of three sections instead of just two. The first section is the programming section, where the programmer programs every location in the EPROM without verifying. Next there is the verify/repair section, where the programmer starts at the beginning of the EPROM and verifies every location for the correct data at 6.5V. Any cells that don't pass are reprogrammed up to ten times before the device is failed. The last section lowers V_{CC} to 5.0V and does a final verify of the data (here again, most programmers verify in two passes, one with V_{CC} at 4.75V and the other with V_{CC} at 5.25V). This type of programming algorithm is called a two-pass algorithm, because it goes through the memory array twice during programming.

Well, this all sounds fine, but what difference can the programming algorithm possibly make? We can find the answer to that question in a particularly sneaky deprogramming mode that EPROMs can exhibit. We all know that EPROMs are erased by exposing them to short-wave ultraviolet light, right? Nothing more than applying Einstein's discovery of the photoelectric effect. But there is another erasure mode that can occur, one that people in the E^2PROM business know about. If you were to examine some EPROM cells in an electron microscope, you might find a few that have small, tooth-like projections (called asperities) on the top of the floating gate polysilicon. These projections won't affect the normal operation of the EPROM, but they could give you problems during programming. When you program a row of cells on an EPROM, cells that have been previously programmed still feel the full brunt of the high V_{PP} voltage on their gates when subsequent cells on the same row are programmed, because all of the cells on a row have their gates connected together. The combination of high voltage on the gate and ground on the drain and source causes an intense electric field in each previously programmed cell. If any one of the cells on that row have these tooth-like projections on their floating gate polysilicon, the resulting electric field in the oxide above the projections will be much more intense than normal. This intensified electric field can give some of the electrons on the floating gate enough energy to jump the oxide barrier, thereby partially erasing the EPROM cell. This unwanted effect, called pro-

(continued)

Figure 7. RAPID programming algorithm



Guaranteeing Programmability (Continued)

gramming erase, can be responsible for poor programming margins unless the programming algorithm takes this problem into account.

Before we continue, it's important to realize that this type of cell doesn't have a **reliability** problem, it has a **programmability** problem. This cell will have the same long-term data retention as any other cell in the device, even if it loses part of its programming charge. Although it is an EPROM, it has the same charge retention characteristics as many manufacturers' E^2PROM cells that use this type of erasure mode, and they all exhibit excellent long-term data retention. The challenge is to find these low-margin cells in the device with our programming algorithm, and to repair them so that the device functions normally.

Let's see what kind of impact a cell like this can have on programming margin by programming a row of EPROM cells from our AT27C010 one-megabit EPROM with both algorithms. The array geometry on the one-megabit is 128 columns by 1024 rows, by 8 outputs. This means that a single row from a single output has 128 EPROM cells. Let's say that the second cell on this row, bit 1 (we'll call them bits and start with bit 0), has an asperity, just like the one mentioned above. When we go to program bits 2, 3, 4, etc., the voltage present on the gate of bit 1 causes the E^2PROM-like erasure mode. Given enough subsequent bits to program, bit 1 may lose enough charge to appear unprogrammed. Let's take a look at how the QUICK-PULSE type of algorithm will fail the device, or even worse, pass it with poor programming margin. Then we'll see how the RAPID algorithm will program it such that it works perfectly!

If we examine Figure 8, we see the row of EPROM cells taken from our AT27C010 one-megabit device. Recall that bit 1 is the cell that's having the programmability problem, while the rest of the bits function normally. For the sake of example, let's say that for each subsequent bit after bit 1 that's programmed, bit 1 will lose eight millivolts (mV) of programming margin. Let's also assume that the nominal programming margin for each cell is at least the value of V_{CC} present during programming, which is 6.25V for QUICK-PULSE type algorithms and 6.5V for the RAPID algorithm. Starting with the QUICK-PULSE type of algorithm at bit 0, we program it, verify it, and find that it passes (remember our flowchart from Figure 6?) with the correct margin (see Figure 9). We move to cell 1, program it, verify it, and it passes (see Figure 10). Remember, bit 1 only loses voltage margin when subsequent cells are programmed. Now we move on to bit 2, program it, verify it, and in the process reduce bit 1's programming margin down to 6.242V (see Figure 11). Next we go to bit 3, program it, verify it, and in turn reduce bit 1's programming margin down to 6.234V (see Figure 12). This process continues until we get to bit 127. By this time bit 1 has experienced 126 subsequent cell programming cycles, and its programming margin will be reduced to 5.242V (see Figure 13). Since the QUICK-PULSE type of algorithm does its high-voltage verify immediately after programming, the algorithm has no way of knowing what has happened to bit 1, once it finishes programming it. Only when the algorithm does its final verify with V_{CC} set at 5.25V could it detect that bit 1 is not fully programmed.

Figure 8: Row of EPROM cells from AT27C010. Note that the programming margin of each cell is 0, which allows each bit to read a "1".

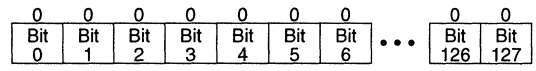


Figure 9: Bit 0 has been programmed, (QUICK-PULSE algorithm)

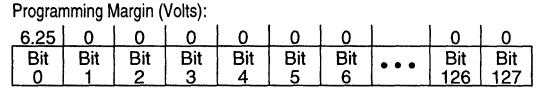
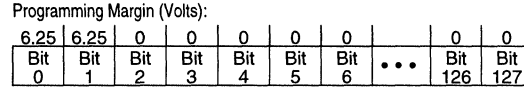


Figure 10: Bit 0 and bit 1 have been programmed.



In this example we were able to detect bit 1 as being bad, and we would fail the device. But what if bit 1's erasure rate was slightly less than 8 mV per subsequent cell, say 7.7 mV? Bit 1's margin might be somewhere around 5.3V, which would probably pass the 5.25V verify check on our programmer. But remember the problem that we discussed earlier, about the power supply noise glitches messing up the operation of devices with low programming margin? A device with only 5.3V of margin is a prime candidate for this type of problem. A small noise glitch occurring during data access on the V_{CC} line of this EPROM could easily change the output from a "0" to a "1". And, to make matters worse, this problem would probably occur

(continued)

Figure 11: Bits 0, 1 and 2 are programmed. Notice that bit 1 has been slightly erased.

Programming Margin (Volts):

6.25	6.242	6.25	0	0	0	0		0	0
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	...	Bit 126	Bit 127

Figure 12: Bit 3 has just been programmed. Notice that bit 1 has been further erased.

Programming Margin (Volts):

6.25	6.234	6.25	6.25	0	0	0		0	0
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	...	Bit 126	Bit 127

Figure 13: The entire row has been programmed. Notice how much bit 1 has been erased.

Programming Margin (Volts):

6.25	5.242	6.25	6.25	6.25	6.25	6.25		6.25	6.25
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	...	Bit 126	Bit 127

Figure 14: Bit 0 has just been reprogrammed (RAPID algorithm).

Programming Margin (Volts):

6.50	0	0	0	0	0	0		0	0
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	...	Bit 126	Bit 127

Figure 15: Bit 1 has just been programmed.

Programming Margin (Volts):

6.50	6.50	0	0	0	0	0		0	0
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	...	Bit 126	Bit 127

Figure 16: Bit 2 has just been programmed. Notice how bit 1 has been slightly erased again.

Programming Margin (Volts):

6.50	6.492	6.50	0	0	0	0		0	0
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	...	Bit 126	Bit 127

Guaranteeing Programmability (Continued)

randomly; the eventual diagnosis being that the device was intermittent. The unfortunate truth is that there is nothing wrong with the EPROM, it's the programming algorithm that's at fault.

So let's go back to our row of 128 EPROM cells, erase them, and reprogram them with the RAPID algorithm. Remember that with the RAPID algorithm the initial program and verify routines are located in different sections of the algorithm, they are not contained within the same loop. Starting at bit 0, we program it (to 6.5V this time, see Figure 14). Then move to bit 1, and program it (see Figure 15). Next to bit 2, program it, and in turn reduce bit 1's programming margin to 6.492V (see Figure 16). Then on to bit 3, program it, and further reduce bit 1's programming margin to 6.484V. We continue programming until we get to bit 127, and you'll find that the programming margin for all the cells looks similar to figure 8 (see Figure 17). But wait, we're not finished yet. We move back to the beginning of the EPROM array, which is bit 0, and verify that it has 6.5V of programming margin. Since we are verifying at 6.5V, we pass it. We now move to bit 1 and notice that its programming margin is 5.492V. This fails our 6.5V verify, so we program it one more time and raise its margin back to 6.5V, then pass it (see Figure 18). Then we move to bit 2, and pass it, since its programming margin is also 6.5V. Notice that we didn't deprogram bit 1 in the process of verifying bit 2. We only deprogram bit 1 when we program subsequent cells; reading or verifying (which is reading) doesn't generate the intense electric fields needed to deprogram EPROM cells. After verifying (and repairing) this row of cells, we return V_{CC} to 5.25V, do a final data verify, then pass the row (see Figure 18). Now compare Figure 18 with Figure 13. That's how the RAPID algorithm can guarantee programmability!

Well, you may ask, what if we had five problem cells on the same row? Wouldn't the additional programming pulses during the verify function deprogram previously programmed and verified cells? They probably would, but the maximum amount of deprogramming on the first bit (using this model) would be only 32 mV (4 x 8 mV). This gives us a programming margin of 6.468V, which is still an excellent programming margin.

(continued)

Guaranteeing Programmability (Continued)

When you compare the QUICK-PULSE type algorithms to the RAPID algorithm, there really is no comparison. The RAPID algorithm simply guarantees programmability, and we demonstrated this with the deprogramming bit example, which is one of the trickiest programming problems you can have. But the RAPID algorithm caught the problem, and repaired the bit so that the EPROM will function normally.

Figure 17: The entire row has just been programmed. Notice how much bit 1 has been erased.

Programming Margin (Volts):

6.50	5.492	6.50	6.50	6.50	6.50	6.50		6.50	6.50
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	• • •	Bit 126	Bit 127

Figure 18: The entire row has just been verified at 6.50 volts. Notice how bit 1 has been repaired, its margin being returned to 6.50 volts using the RAPID algorithm.

Programming Margin (Volts):

6.50	6.50	6.50	6.50	6.50	6.50	6.50		6.50	6.50
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	• • •	Bit 126	Bit 127

Surface Mount Programming Adapter Manufacturers

As the market for nonvolatile memory parts in surface mount packages increases, so does the interest in simple, low cost programming socket adapters. These adapters allow users of standard programming equipment to program any package type including SOIC (gull-wing), PLCC (J-Lead), and TSOP. The adapter plugs into the programmer in place of a 600 mil or 300 mil DIP package of the same part.

The two major disadvantages of building a socket adapter are:

Little or no support from programmer manufacturers.

Use of socket adapters (which are larger in width than the pins on a DIP I.C.) is not recommended. This will cause spring tension loss damage of the programmer's zero insertion force sockets, which may degrade the reliability of the programmer when the adapter is not used.

The advantages are more obvious. Some manufacturers charge up to $500 for an adapter which slides or plugs into the programmer compared to about $100 for the hardware described here.

Assembly of a custom programming adapter is very simple. Table 1 describes the typical piece-parts needed.

Table 1. Piece-Part Descriptions (see Figure 1)

Item No.	Qty.	Description
(1)	1	Zero insertion force socket.
(2)	2	Wire wrap strips with 100 mils pin centers and about 500 mils long on the end which will plug into the programmer's socket and 200 mils long on the opposite end to attach to (5) below.
(3)	2	Wire wrap strips similar to (2) above except only 100 mils and 200 mils long to connect (4) and (5) below.
(4)	1	PC board to accept the socket (1) and run traces to the edge of the card connecting to (3).
(5)	1	PC board to run traces from the card edge (3) to the two strips (2) (usually separated by 600 mils).
(6)	20"	#16-18 insulated stranded copper wire.
(7)	1-2	0.1 µF ceramic high-frequency decoupling capacitors.
(8)	1	(Recommended) Pin socket board to fit between (1) and (4) to allow easy replacement of the socket (1). (8) is soldered to (4) and (1) plugs into (8). Zero insertion force sockets wear out quickly so replaceability is a good feature to have.

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Table 2 lists sockets and piece-part sources for different package configurations. The finished adapter is about 2 inches square and 1.5 inches high.

As listed in Table 2, Emulation Technology, Inc., (408) 982-0660, can supply the adapter sockets preassembled, but we recommend you order the parts as an UNSOLDERED KIT to facilitate attaching the decoupling capacitors. The additional wire shunts (not required if a -LN kit is ordered from ET) and capacitors are essential to reduce inductive noise effects during programming and to maintain adequate programming yield. It is necessary to "beef-up" all the power (V_{CC}, V_{PP}) and ground (Gnd) connections by adding short jumpers of wire (6) running from the socket (1), around the edge of the module and finally to the pins of item (2) on the bottom of the module. Bypass capacitors (7) must be soldered between Gnd and V_{CC} or V_{PP} (if applicable). The leads on the capacitors must be trimmed as short as possible and soldered as close to the socket (1) as possible (on the wide traces on the -LN board (4)). The other end of each capacitor will be connected to short stranded wires (6) running from the top, around the edge of the adapter, and finally soldered to the ground pin of item (2).

Assembly proceeds as follows (see Figure 1 and note that jumper wires (6) are not required if a -LN kit is used):

1. Trim the leads on the jumper wires (6) to about 3.0 inches. Solder capacitors (7) with shrink-wrap insulation on the cap leads, and jumper wires (6) under the socket (1) (or under (8) if socket replaceability is needed) in such a way that they do not interfere with attaching the socket (or (8)) to the board (4). (If a -LN kit is used, just solder the capacitors on the wide traces provided on board (4).)
2. Solder the socket (or item (8)) to the PC board (4) and trim the pins on the socket flush to the board (4).
3. Solder the shorter pin strips (3) to the outside of board (4) with the spacers on the side away from the socket (1).
4. Solder the longer pin strips (2) into the other PC board (5) such that the spacers stick out of the bottom of the adapter. These longer pins will be used to plug directly into the programmer socket. Trim the shorter leads of (2) flush with the board (5) after soldering.
5. Solder the PC board (5) to the short pins protruding below PC board (4).

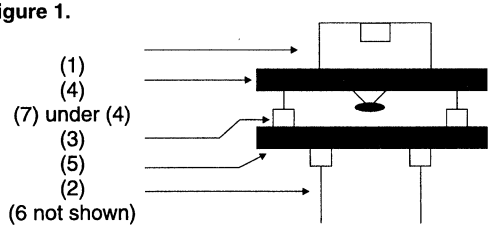
Table 2. Vendors / Part Numbers by Package Type

Package Type	Pin Count	Emulation Technology [1]	Socket Manufacturer	Part No.
PLCC	32	AS-32-28-01P-P6-LN	Yamaichi	IC51-0324-453
	44	AS-44-40-08-P6-LN	Textool	244-5292
SOIC	28	AS-28-28-015-6-GANG	Enplas	FB-28-1-27-07
	32	AS-32-32-01S	Yamaichi	IC51-0322-667
	44	AS-44-44-01S	Yamaichi	IC51-0442-1208
TSOP	28	AS-28-28-01TS-S	Yamaichi	IC51-0282-673-1
	32	AS-32-32-01TS-S	Enplas	OTS-32-0.5-02
	40	AS-40-40-01TS-S	Yamaichi	IC191-0402-002N
	48	AS-48-48-01TS-S	Yamaichi	IC191-0482-004

Notes: 1. ET can also supply finished adapter sockets built per this application note or other customer requirements.
2. Made by 3M. Check with your local distributor.

6. (Omit this step if a -LN kit is used.) Connect all the V_{CC}, VPP (if applicable) and Gnd wires which were connected in step (1) to their appropriate pins on item (2) on the underside of the assembly close to the protruding spacer in such a way that they will not interfere with plugging the completed module into the programmer DIP socket. Trim these shunt wires as short as possible to minimize inductance effects.

Figure 1.



This application note has described how to build a simple and cheap programming adapter socket to support a wide variety of nonvolatile memory product packages available from Atmel.

EPROM Programmer Firmware Support

The information on this list is based on market research information only and does not imply Atmel's suppport, approval or qualification. Please contact the programmer manufacturers directly to obtain the latest information since software and hardware changes are frequently made.

STAG			
Device	PP40	PP41	PP42M101
AT27C256R	6.0	6.0	6.0
AT27C512R	5.0	5.0	5.0
AT27C010	8.1	8.1	8.1
AT27C020	8.0	8.0	8.0
AT27C040	8.0	8.0	8.0
AT27C080	N/A	N/A	8.0
AT27C1024	5.0	5.0	5.0
AT27C4096	N/A	N/A	16.0

NEEDHAM			
Device	EMP-20	SA10/20	PB10
AT27C256R	1.8	1.49	1.53
AT27C512R	1.8	1.49	1.53
AT27C010	1.8	1.49	1.53
AT27C020	1.8	1.49	1.53
AT27C040	1.8	1.49	1.53
AT27C080	1.8	1.49	1.53
AT27C1024	1.8	1.49	1.53
AT27C4096	1.8	1.49	1.53

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ELAN SYSTEMS				
Device	142	928	932	840/940
AT27C256R	ES.00	ES.00	ES.00	N/A
AT27C512R	ES.00	ES.00	ES.00	N/A
AT27C010	ES.00	ES.00	ES.00	N/A
AT27C020	7.01	N/A	7.01	N/A
AT27C040	ES.03	ES.03	ES.03	N/A
AT27C080	N/A	N/A	N/A	N/A
AT27C1024	7.01	N/A	N/A	ES.00
AT27C4096	N/A	N/A	N/A	N/A

Data I/O							
Device	PSX-1000	S1000	Setsite	Site48/40/48H	2900	3900	Chip Lab
AT27C256R	1.0	15.0	3.0	3.0	1.2	1.0	1.01
AT27C512R	1.0	14.0	2.7	2.7	1.0	1.0	1.01
AT27C010	1.0	14.0	2.8	2.7	1.1	1.0	1.01
AT27C020	3.22	N/A	4.6	4.6	3.4	2.4	2.0
AT27C040	1.0	23.0	3.8	3.8	1.9	1.3	1.01
AT27C080	3.0	N/A	N/A	4.3	3.1	2.1	Q4 96
AT27C1024	1.0	15.0	3.9	3.9	1.0	1.0	1.0
AT27C4096	3.4	N/A	N/A	4.9	3.7	2.7	3.0
AT27C516	3.4	N/A	N/A	N/A	N/A	N/A	N/A

Data I/O							
Device	PSX-1000	S1000	Setsite	Site48/40	2900	3900	Chip Lab
AT27LV256R	2.0	26	3.9	3.9	2.0	1.4	1.01
AT27LV512R	2.0	26	3.9	3.9	2.0	1.4	1.01
AT27LV010	2.0	26	3.9	3.9	2.0	1.4	1.01
AT27LV020	3.22	N/A	N/A	4.8	3.6	2.6	3.0
AT27LV040	2.0	26	3.9	3.9	2.0	1.4	1.01
AT27LV080	3.0	N/A	N/A	4.3	3.1	2.1	Q4 96
AT27LV1024	1.0	N/A	3.9	3.9	1.0	1.0	1.0
AT27LV4096	3.4	N/A	N/A	4.9	3.7	2.7	3.0

LOGICAL DEVICES						
Device	ALLPRO088 ALLPRO040	ALLPRO 88XR	HUSKY	GANGRO - 8+	GANGRO -S MODEL II	XPRO
AT27C256R	2.1	1.0	2.2	1.0	1.0	1.02
AT27C512R	2.1	1.0	2.2	1.0	1.0	1.02
AT27C010	2.1	1.0	2.1	1.0	1.0	1.02
AT27C020	2.4	N/A	N/A	N/A	N/A	3.0
AT27C040	2.1	1.0	N/A	1.1	1.0	1.02
AT27C080	2.4	2.5	N/A	N/A	N/A	3.0
AT27C1024	2.2	1.0	N/A	1.0	1.0	1.02
AT27C4096	2.5	2.5	N/A	N/A	N/A	3.0

MINATO				
Device	1890A	1891/1892	1910	1930
AT27C256R	2.2	2.0	3.0	1.0
AT27C512R	2.2	2.0	3.0	1.0
AT27C010	2.2	2.0	3.0	1.0
AT27C020	4.02	4.01	4.2	2.8
AT27C040	3.2	3.13	4.1	1.0
AT27C080	4.02	4.01	4.2	2.8
AT27C1024	2.23	2.0	3.0	1.0
AT27C4096	4.06	4.02	4.2	2.12

SYSTEM GENERAL					
Device	TURPRO 840	TURPRO 1	TURPRO 1/FX	APRO	TURPRO 832
AT27C256R	1.1	1.0	1.0	1.0	2.0
AT27C512R	1.1	1.0	1.0	1.0	2.0
AT27C010	1.1	1.3	1.0	1.0	2.3
AT27C020	1.5	1.38	1.0	1.12	4.5
AT27C040	1.7	1.44	1.3	1.13	5.03
AT27C080	2.08	2.04	2.04	1.19	6.08
AT27C1024	1.5	1.64	1.62	1.13	N/A
AT27C4096	2.2	2.14	2.14	1.22	N/A

ADVIN SYSTEMS						
Device	PILOT -U84	PILOT -U40	PILOT -U145	PILOT GCE	PILOT 832D	PILOT -840D
AT27C256R	10.16	10.16	10.16	10.16	10.68	N/A
AT27C512R	10.14	10.14	10.14	10.14	10.68	N/A
AT27C010	10.14	10.14	10.14	10.14	10.68	N/A
AT27C020	10.74	10.74	10.74	10.74	10.75	N/A
AT27C040	10.16	10.16	10.16	10.16	10.68	N/A
AT27C080	10.74	10.74	10.74	10.74	10.75	N/A
AT27C1024	10.35	10.35	10.35	N/A	N/A	10.68
AT27C4096	10.74	10.74	10.74	N/A	N/A	10.75

B-P MICRO SYSTEMS					
Device	BP-1200	CP-1128	EP-1140	EP-1132	EP1
AT27C256R	2.0	1.83	1.83	1.83	1.83
AT27C512R	2.0	1.83	1.83	1.83	1.83
AT27C010	2.0	N/A	1.94	N/A	N/A
AT27C020	2.32	N/A	2.32	N/A	N/A
AT27C040	2.0	N/A	1.94	N/A	N/A
AT27C080	2.32	N/A	2.32	N/A	N/A
AT27C1024	2.0	N/A	1.94	N/A	N/A
AT27C4096	2.32	N/A	2.32	N/A	N/A

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AT29C256	32K x 8	256K, 5-Volt Reprogrammable ROM..... 4-93
AT29C257	32K x 8	256K, 5-Volt Reprogrammable ROM..... 4-105
AT29C512	64K x 8	512K, 5-Volt Reprogrammable ROM..... 4-117
AT29C010A	128K x 8	1M bit, 5-Volt Reprogrammable ROM 4-129
AT29C1024	64K x 16	1M bit, 5-Volt Reprogrammable ROM 4-141
AT29C020	256K x 8	2M bit, 5-Volt Reprogrammable ROM 4-153
AT29C040A	512K x 8	4M bit, 5-Volt, Reprogrammable ROM 4-165
AT49F010	128K x 8	1M bit, 5-Volt, Reprogrammable ROM 4-177
AT49F020	256K x 8	2M bit, 5-Volt, Reprogrammable ROM 4-187
AT49F2048	128K x 16	2M bit, 5-Volt, Reprogrammable ROM 4-197
AT49F040	512K x 8	4M bit, 5-Volt, Reprogrammable ROM 4-209
AT49F4096	256K x 16	4M bit, 5-Volt, Reprogrammable ROM 4-219
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1 Megabit (128K x 8) Single 2.7-volt *Battery-Voltage*™ CMOS Flash

Features

- Single Supply Voltage, Range 2.7V to 3.6V
- Single Supply for Read and Write
- Software Protected Programming
- Fast Read Access Time - 200 ns
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Sectors (128 bytes/sector)
  - Internal Address and Data Latches for 128-Bytes
- Two 8 KB Boot Blocks with Lockout
- Fast Sector Program Cycle Time - 20 ms Max.
- Internal Program Control and Timer
- DATA Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

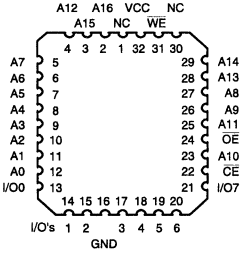
The AT29BV010A is a 2.7-volt-only in-system Flash Programmable and Erasable Read Only Memory (Flash). Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS EEPROM technology, the device offers access times up to 200 ns, and a low 54 mW power dissipation. When the device is deselected, the CMOS standby current is less than 20 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times. The programming algorithm is compatible with other devices in Atmel's Low Voltage Flash family of products.

(continued)

Pin Configurations

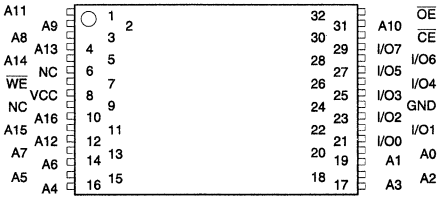
Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

PLCC Top View



TSOP Top View

Type 1



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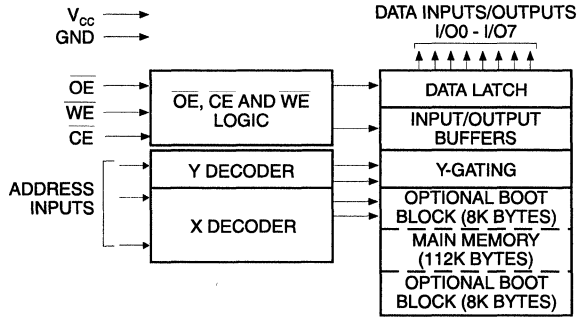
Description (Continued)

To allow for simple in-system reprogrammability, the AT29BV010A does not require high input voltages for programming. The device can be operated with a single 2.7V to 3.6V supply. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29BV010A is performed on a sector basis; 128-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128-bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29BV010A is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29BV010A has 1024 individual sectors, each 128-bytes. Using the software data protection feature, byte loads are used to enter the 128-bytes of a sector to be programmed. The AT29BV010A can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 128-byte sector must be loaded into the device. The data in any byte that is not loaded during the programming of its sector will be indeterminate. The AT29BV010A automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of twc, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

The 128-bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be indeterminate. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address

(continued)

Device Operation (Continued)

within the sector. The bytes may be loaded in any order; sequential loading is not required.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29BV010A in the following ways: (a) V_{CC} sense— if V_{CC} is below 2.0V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 2.7V to 3.6V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both methods of identification.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 (including NC Pins) with Respect to Ground	-0.6V to +13.5V

$\overline{DATA}$ POLLING: The AT29BV010A features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29BV010A provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

BOOT BLOCK PROGRAMMING LOCKOUT: The AT29BV010A has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 8K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 8K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29BV010A blocks are located in the first 8K bytes of memory and the last 8K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

(continued)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation (Continued)

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine whether programming of either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002H will show if programming the lower address boot block is locked out while reading location 1FFF2H will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

DC and AC Operating Range

		AT29BV010A-20	AT29BV010A-25	AT29BV010A-30
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply [1]		2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V

1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program [2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X [1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A16 = V_{IL}, A9 = V_H [3], A0 = V_{IL}	Manufacturer Code [4]
				A1 - A16 = V_{IL}, A9 = V_H [3], A0 = V_{IH}	Device Code [4]
Software [5]				A0 = V_{IL}, A1 - A16 = V_{IL}	Manufacturer Code [4]
				A0 = V_{IH}, A1 - A16 = V_{IL}	Device Code [4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.
4. Manufacturer Code is 1F. The Device Code is 35.
5. See details under Software Product Identification Entry/Exit.

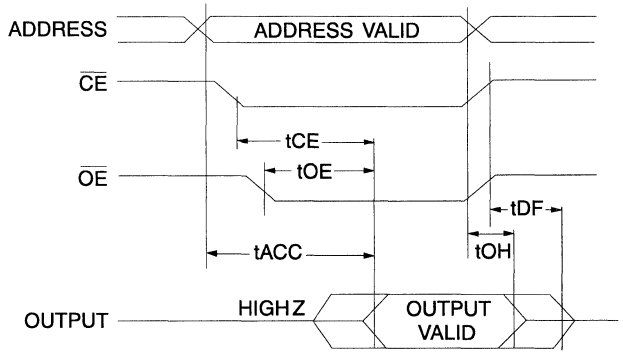
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

AC Read Characteristics

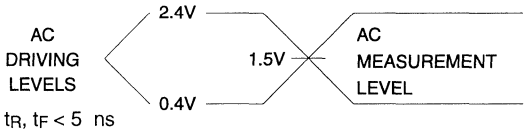
Symbol	Parameter	AT29BV010A-20 Min	AT29BV010A-20 Max	AT29BV010A-25 Min	AT29BV010A-25 Max	AT29BV010A-30 Min	AT29BV010A-30 Max	Units
t_{ACC}	Address to Output Delay		200		250		300	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		250		300	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	100	0	120	0	150	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	60	0	75	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms

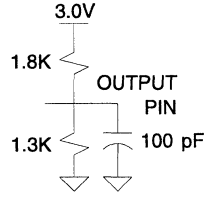


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

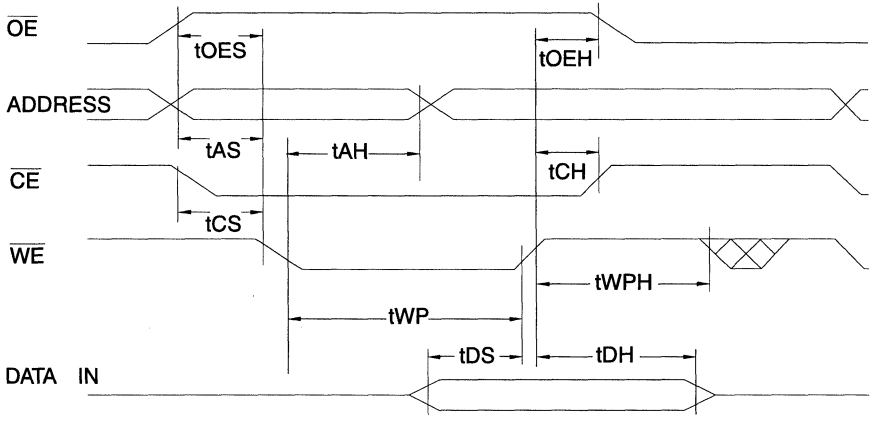
Note: 1. These parameters are characterized and not 100% tested.

AC Byte Load Characteristics

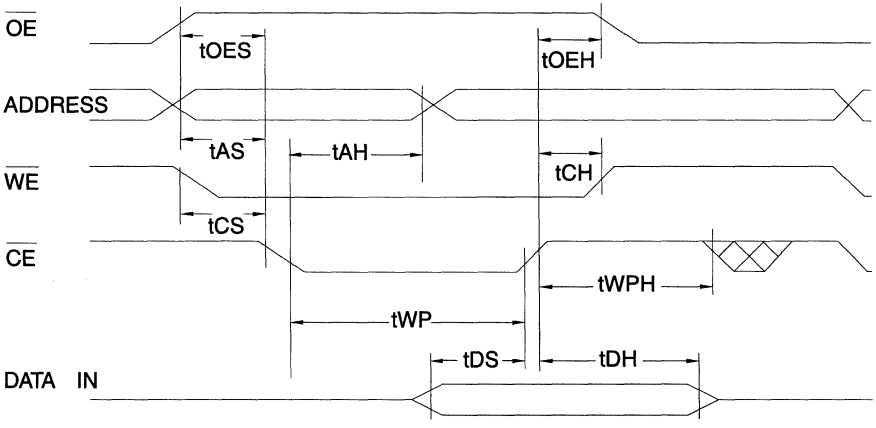
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	200		ns

AC Byte Load Waveforms [1, 2]

$\overline{WE}$ Controlled



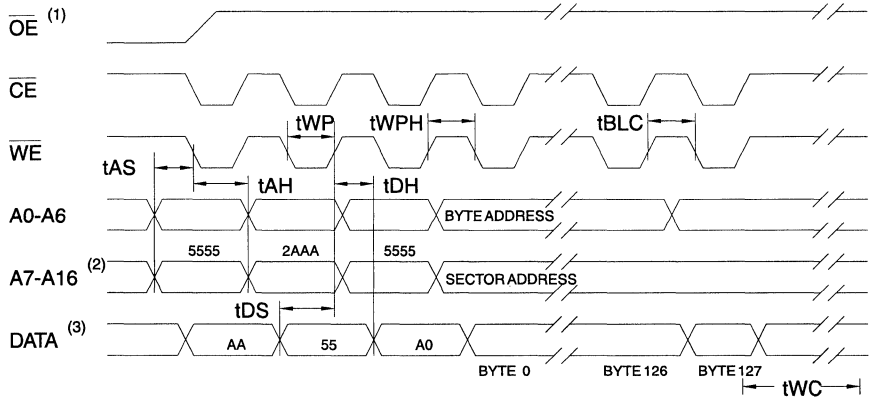
$\overline{CE}$ Controlled



Program Cycle Characteristics

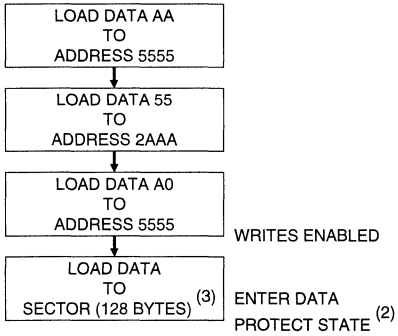
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Program Waveform



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A7 through A16 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Programming Algorithm (1)



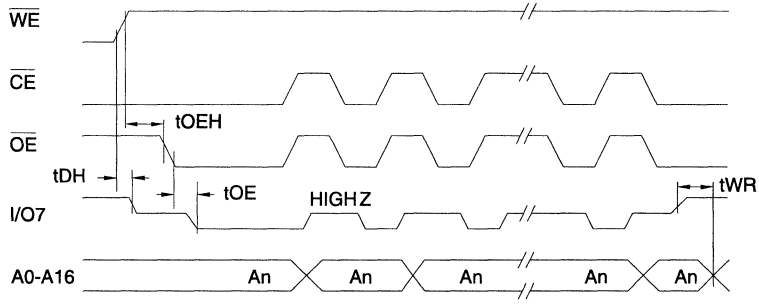
Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 128-bytes of data **MUST BE** loaded.

$\overline{\text{Data}}$ Polling Characteristics [1, 2]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

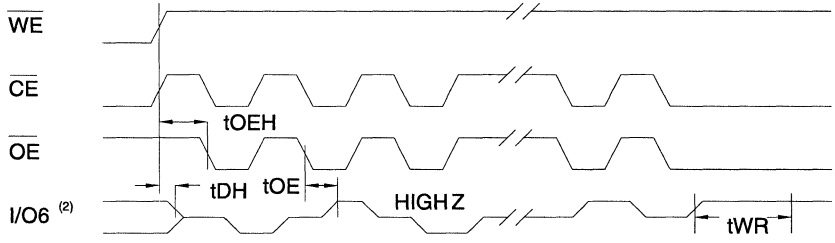


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

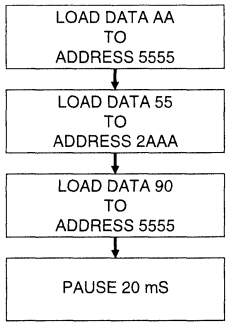
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 3]

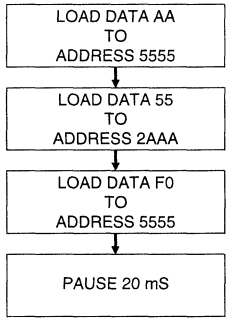


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

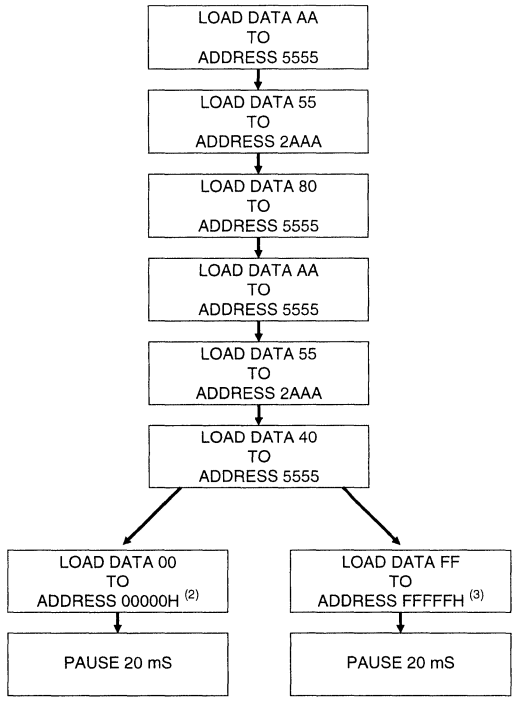


Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A16 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code is 1F. The Device Code is 35.

Boot Block Lockout Feature Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Lockout feature set on lower address boot block.
3. Lockout feature set on higher address boot block.

4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT29BV010A-20JC AT29BV010A-20TC	32J 32T	Commercial (0° to 70°C)
250	15	0.02	AT29BV010A-25JC AT29BV010A-25TC	32J 32T	Commercial (0° to 70°C)
	15	0.02	AT29BV010A-25JI AT29BV010A-25TI	32J 32T	Industrial (-40° to 85°C)
300	15	0.02	AT29BV010A-30JC AT29BV010A-30TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29BV010A-30JI AT29BV010A-30TI	32J 32T	Industrial (-40° to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Thin Small Outline Package (TSOP)

Features

- Single Supply Voltage, Range 2.7V to 3.6V
- Single Supply for Read and Write
- Software Protected Programming
- Fast Read Access Time - 250 ns
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Sectors (256 bytes/sector)
  - Internal Address and Data Latches for 256-Bytes
- Two 8 KB Boot Blocks with Lockout
- Fast Sector Program Cycle Time - 20 ms Max.
- Internal Program Control and Timer
- DATA Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

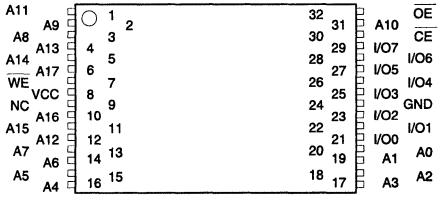
The AT29BV020 is a 2.7-volt-only in-system Flash Programmable and Erasable Read Only Memory (PEROM). Its 2 megabits of memory is organized as 262,144 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS EEPROM technology, the device offers access times up to 250 ns, and a low 54 mW power dissipation. When the device is deselected, the CMOS standby current is less than 20 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times. The programming algorithm is compatible with other devices in Atmel's Low Voltage Flash family of products.

(continued)

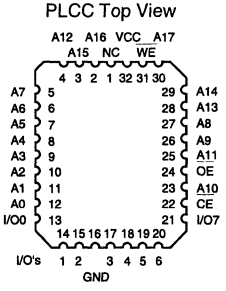
Pin Configurations

Pin Name	Function
A0 - A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

TSOP Top View
Type 1



PLCC Top View



2 Megabit (256K x 8) Single 2.7-volt *Battery-Voltage*™ CMOS Flash Memory

4

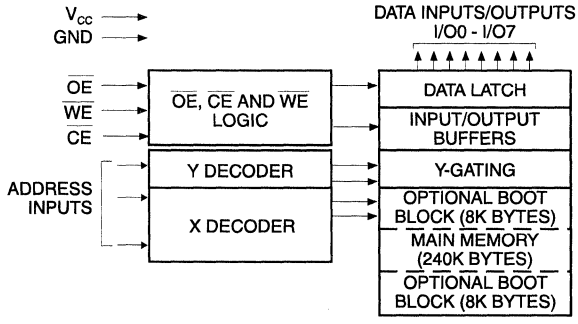
0402B

Description (Continued)

To allow for simple in-system reprogrammability, the AT29BV020 does not require high input voltages for programming. The device can be operated with a single 2.7V to 3.6V supply. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29BV020 is performed on a sector basis; 256-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 256-bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29BV020 is accessed like an EPROM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever CE or OE is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29BV020 has 1024 individual sectors, each 256-bytes. Using the software data protection feature, byte loads are used to enter the 256-bytes of a sector to be programmed. The AT29BV020 can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 256-byte sector must be loaded into the device. The data in any byte that is not loaded during the programming of its sector will be indeterminate. The AT29BV020 automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the WE or CE input with CE or WE low (respectively) and OE high. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE.

The 256-bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be indeterminate. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on WE (or CE) within 150 µs of the low to high transition of WE (or CE) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A8 to A17 specify the sector address. The

(continued)

Device Operation (Continued)

sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A7 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29BV020 in the following ways: (a) V_{CC} sense— if V_{CC} is below 2.0V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 2.7V to 3.6V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both methods of identification.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 (including NC Pins) with Respect to Ground	-0.6V to +13.5V

$\overline{DATA}$ POLLING: The AT29BV020 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29BV020 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

BOOT BLOCK PROGRAMMING LOCKOUT: The AT29BV020 has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 8K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 8K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29BV020 blocks are located in the first 8K bytes of memory and the last 8K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

(continued)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation (Continued)

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine whether programming of either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002H will show if programming the lower address boot block is locked out while reading location FFFF2H will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

DC and AC Operating Range

		AT29BV020-25	AT29BV020-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply [1]		2.7V to 3.6V	2.7V to 3.6V

1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program [2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X [1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A17 = V_{IL}, A9 = V_H [3], A0 = V_{IL}	Manufacturer Code [4]
				A1 - A17 = V_{IL}, A9 = V_H [3], A0 = V_{IH}	Device Code [4]
Software [5]				A0 = V_{IL}, A1 - A17 = V_{IL}	Manufacturer Code [4]
				A0 = V_{IH}, A1 - A17 = V_{IL}	Device Code [4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code is 1F. The Device Code is BA.
5. See details under Software Product Identification Entry/Exit.

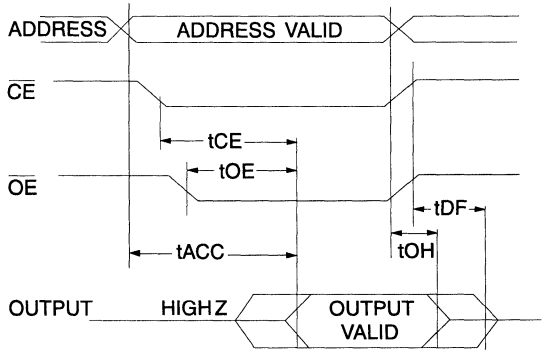
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

AC Read Characteristics

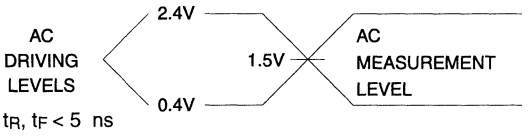
Symbol	Parameter	AT29BV020-25 Min	AT29BV020-25 Max	AT29BV020-35 Min	AT29BV020-35 Max	Units
t_{ACC}	Address to Output Delay		250		350	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		250		350	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	120	0	150	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	60	0	75	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms

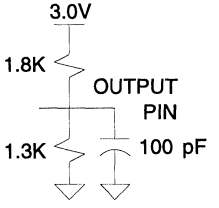


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

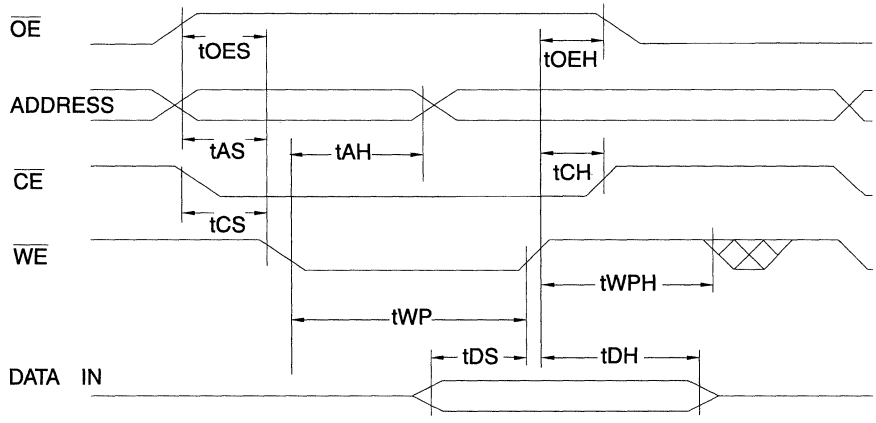
Note: 1. These parameters are characterized and not 100% tested.

AC Byte Load Characteristics

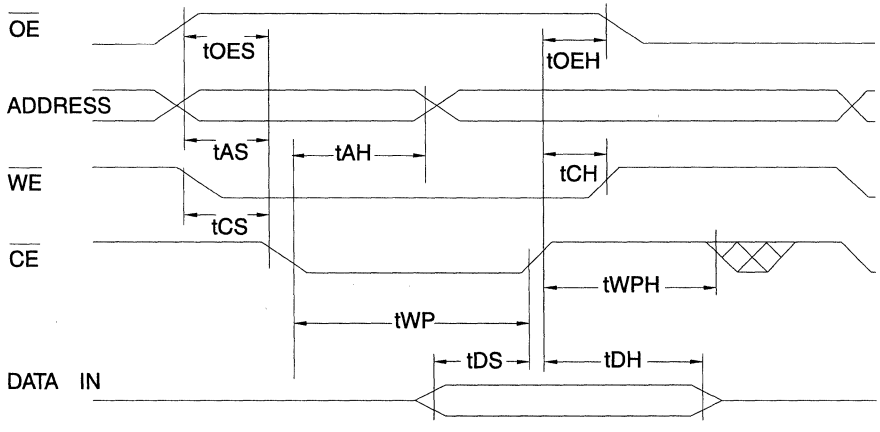
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	200		ns

AC Byte Load Waveforms [1, 2]

$\overline{WE}$ Controlled



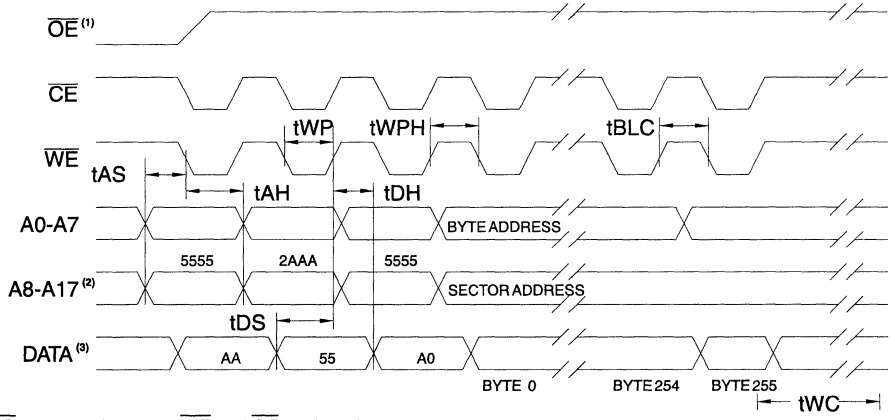
$\overline{CE}$ Controlled



Program Cycle Characteristics

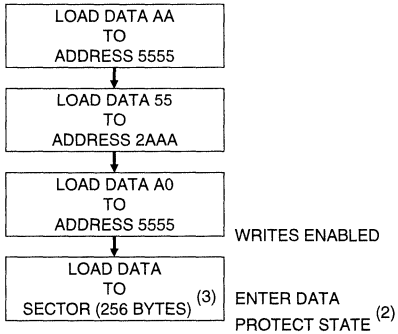
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Program Waveform



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A8 through A17 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. Data in bytes not loaded within a sector being programmed may be altered by the program operation; therefore, all bytes within a sector must be loaded.

Programming Algorithm (1)



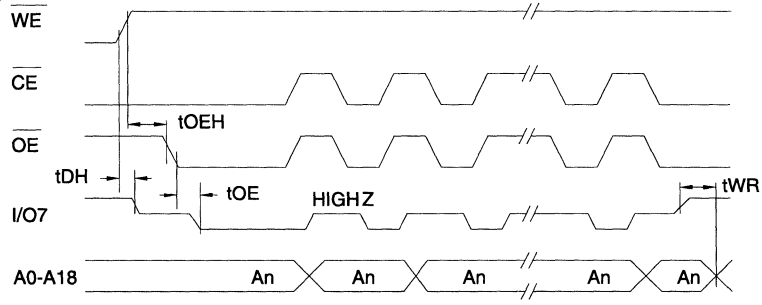
Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 256-bytes of data **MUST BE** loaded.

$\overline{\text{Data}}$ Polling Characteristics [1, 2]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

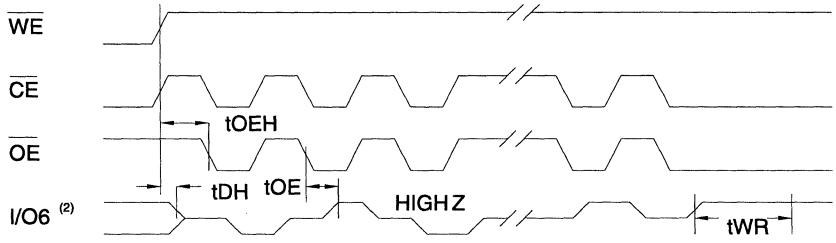


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

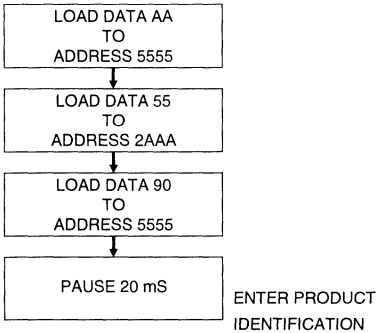
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 3]

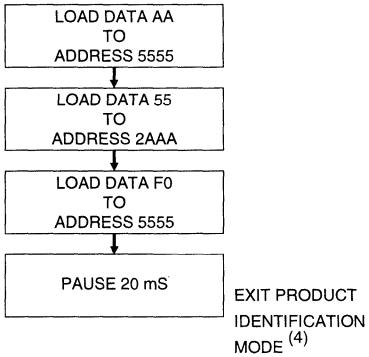


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

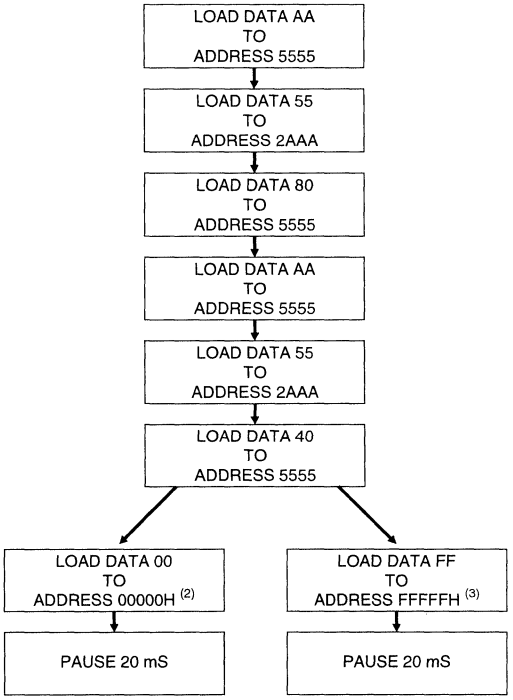


Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A17 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code is 1F. The Device Code is BA.

Boot Block Lockout Feature Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Lockout feature set on lower address boot block.
3. Lockout feature set on higher address boot block.

4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	15	0.02	AT29BV020-25JC AT29BV020-25TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29BV020-25JI AT29BV020-25TI	32J 32T	Industrial (-40° to 85°C)
350	15	0.02	AT29BV020-35JC AT29BV020-35TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29BV020-35JI AT29BV020-35TI	32J 32T	Industrial (-40° to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Thin Small Outline Package (TSOP)

Features

- Single Supply Voltage, Range 2.7V to 3.6V
- Single Supply for Read and Write
- Software Protected Programming
- Fast Read Access Time - 250 ns
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 2048 Sectors (256 bytes/sector)
  - Internal Address and Data Latches for 256-Bytes
- Two 16 KB Boot Blocks with Lockout
- Fast Sector Program Cycle Time - 20 ms Max.
- Internal Program Control and Timer
- DATA Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

The AT29BV040A is a 3-volt-only in-system Flash Programmable and Erasable Read Only Memory (PEROM). Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS EEPROM technology, the device offers access times up to 250 ns, and a low 54 mW power dissipation. When the device is deselected, the CMOS standby current is less than 20 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times. The programming algorithm is compatible with other devices in Atmel's 2.7-volt-only Flash memories.

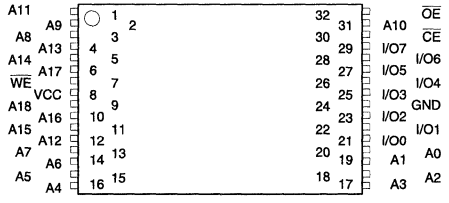
To allow for simple in-system reprogrammability, the AT29BV040A does not require high input voltages for programming. The device can be operated with a single 2.7V to 3.6V supply. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29BV040A is performed on a sector basis; 256-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 256-bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

TSOP Top View
Type 1



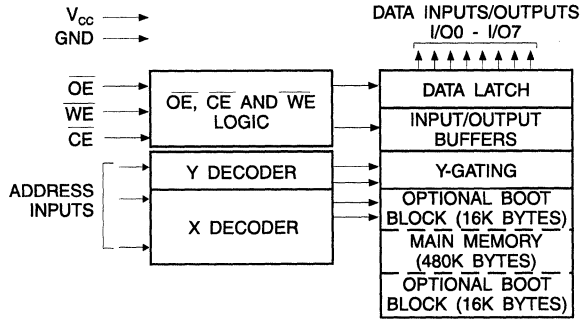
4 Megabit (512K x 8) Single 2.7-volt *Battery-Voltage*™ CMOS Flash Memory

4

Preliminary

0383B

Block Diagram



Device Operation

READ: The AT29BV040A is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29BV040 has 2048 individual sectors, each 256-bytes. Using the software data protection feature, byte loads are used to enter the 256-bytes of a sector to be programmed. The AT29BV040A can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 256-byte sector must be loaded into the device. The AT29BV040A automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

The 256-bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be indeterminate. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A8 to A18 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A7 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29BV040A in the following ways: (a) V_{CC} sense— if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 2.7V to 3.6V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

(continued)

Device Operation (Continued)

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{\text{DATA}}$ POLLING: The AT29BV040A features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT29BV040A provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

BOOT BLOCK PROGRAMMING LOCKOUT: The AT29BV040A has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 16K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 16K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29BV040A blocks are located in the first 16K bytes of memory and the last 16K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine whether programming of either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002H will show if programming the lower address boot block is locked out while reading location FFFF2H will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 (including NC Pins) with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT29BV040A-25	AT29BV040A-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply [1]		2.7V to 3.6V	2.7V to 3.6V

1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program [2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X [1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A18 = V_{IL}, A9 = V_H [3], A0 = V_{IL}	Manufacturer Code [4]
				A1 - A18 = V_{IL}, A9 = V_H [3], A0 = V_{IH}	Device Code [4]
Software [5]				A0 = V_{IL}, A1 - A18 = V_{IL}	Manufacturer Code [4]
				A0 = V_{IH}, A1 - A18 = V_{IL}	Device Code [4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code is 1F. Device Code is C4.
5. See details under Software Product Identification Entry/Exit.

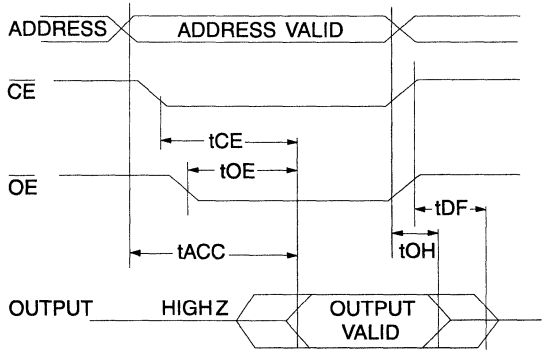
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

AC Read Characteristics

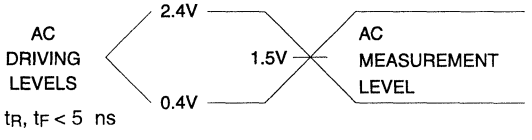
Symbol	Parameter	AT29BV040A-25 Min	AT29BV040A-25 Max	AT29BV040A-35 Min	AT29BV040A-35 Max	Units
t_{ACC}	Address to Output Delay		250		350	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		250		350	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	120	0	150	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	60	0	75	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms

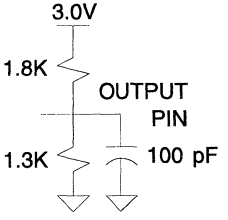


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

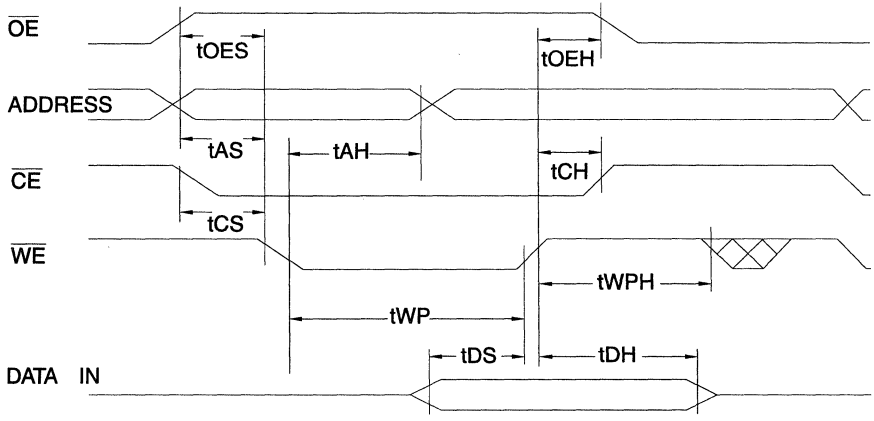
Note: 1. These parameters are characterized and not 100% tested.

AC Byte Load Characteristics

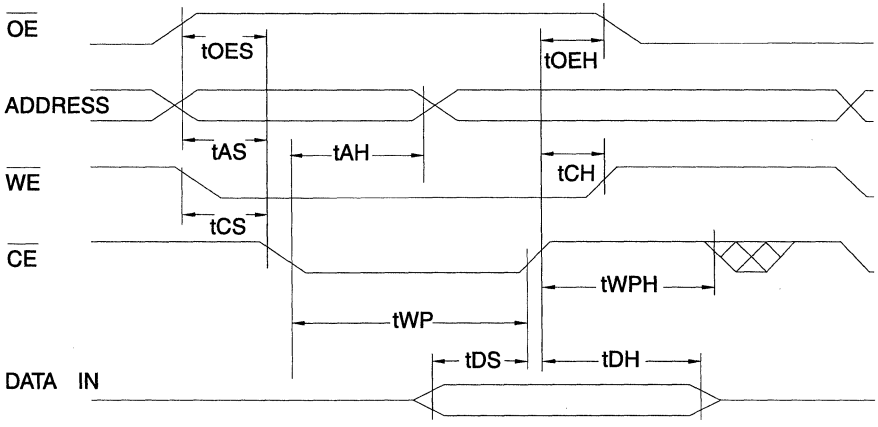
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	200		ns

AC Byte Load Waveforms [1, 2]

$\overline{WE}$ Controlled



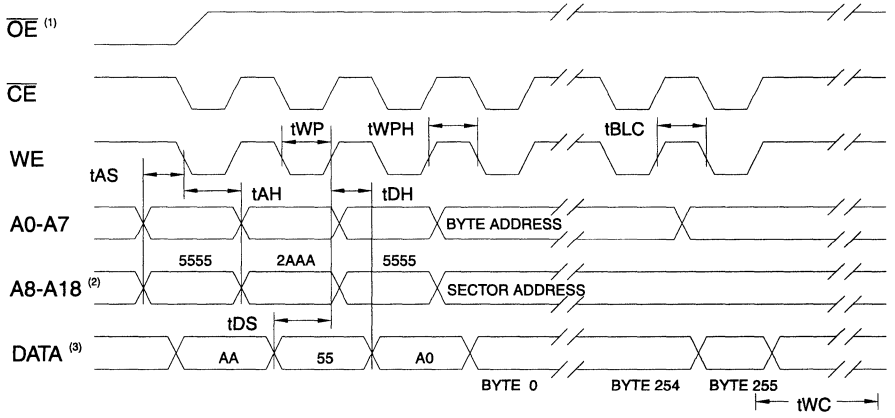
$\overline{CE}$ Controlled



Program Cycle Characteristics

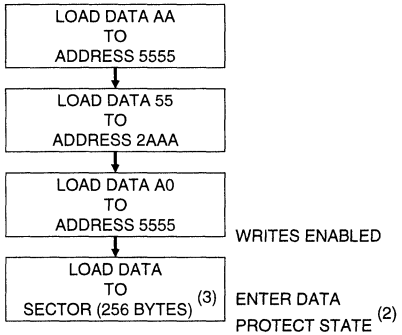
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Program Waveform



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A8 through A18 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Programming Algorithm (1)



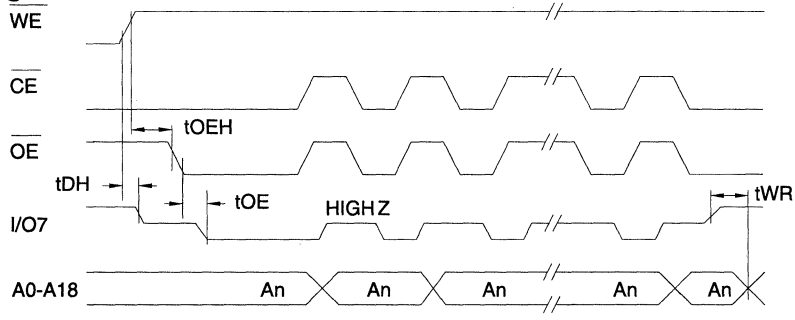
Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 256-bytes of data **MUST BE** loaded.

$\overline{\text{Data}}$ Polling Characteristics (1, 2)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

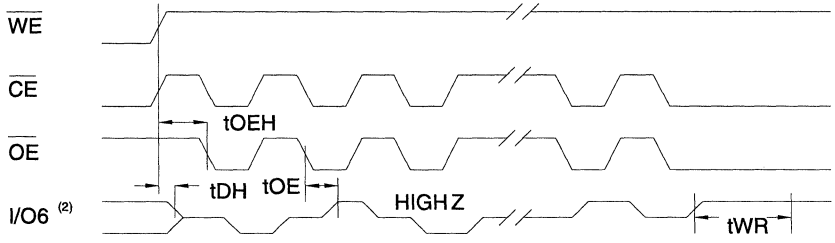


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

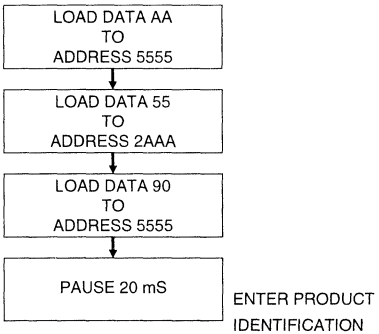
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms (1, 3)

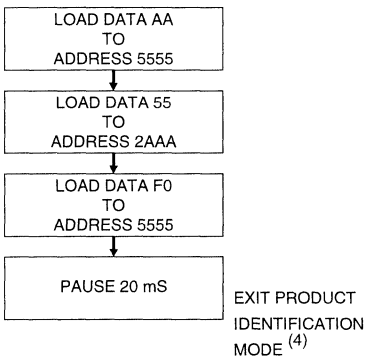


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

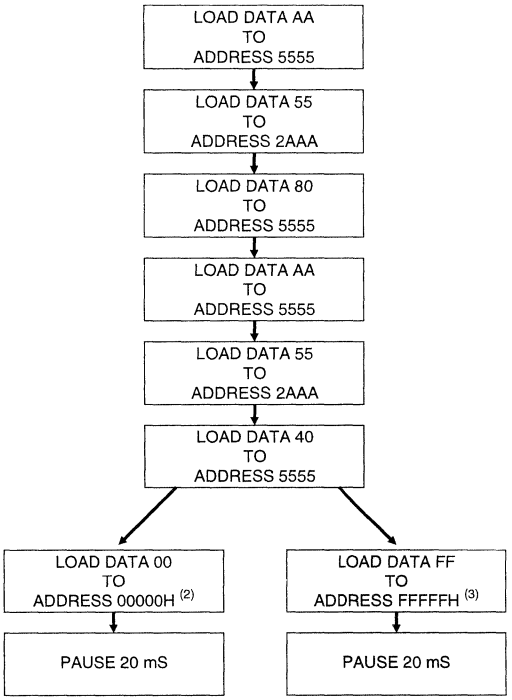


Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code is 1F. Device Code is C4.

Boot Block Lockout Feature Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Lockout feature set on lower address boot block.
3. Lockout feature set on higher address boot block.

4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	15	0.02	AT29BV040A-25TC	32T	Commercial (0° to 70°C)
	15	0.05	AT29BV040A-25TI	32T	Industrial (-40° to 85°C)
350	15	0.02	AT29BV040A-35TC	32T	Commercial (0° to 70°C)
	15	0.05	AT29BV040A-35TI	32T	Industrial (-40° to 85°C)

Package Type	
32T	32 Lead, Thin Small Outline Package (TSOP)

Features

- Single Supply Voltage, Range 3V to 3.6V
- 3-Volt-Only Read and Write Operation
- Software Protected Programming
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Fast Read Access Time - 200 ns
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 512 Sectors (64 bytes/sector)
  - Internal Address and Data Latches for 64-Bytes
- Fast Sector Program Cycle Time - 20 ms Max.
- Internal Program Control and Timer
- DATA Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

256K (32K x 8) 3-volt Only CMOS Flash Memory

4

Description

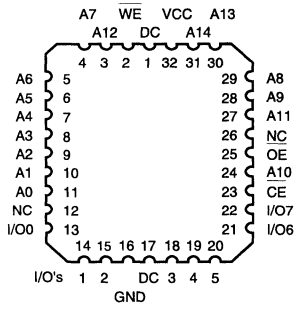
The AT29LV256 is a 3-volt-only in-system Flash Programmable Erasable Read Only Memory (PEROM). Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 20 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

(continued)

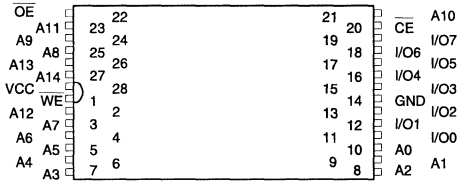
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PLCC Top View



TSOP Top View
Type 1



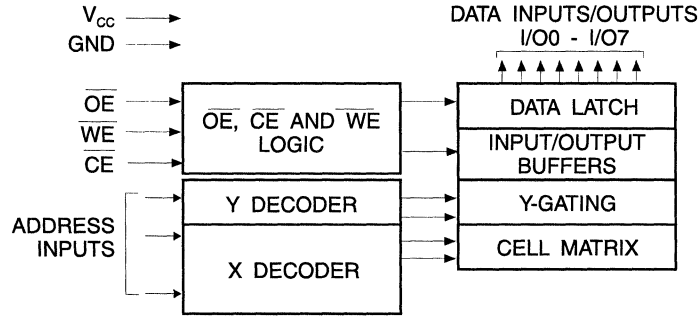
0563A

Description (Continued)

To allow for simple in-system reprogrammability, the AT29LV256 does not require high input voltages for programming. Three-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29LV256 is performed on a sector basis; 64-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 64-bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29LV256 is accessed like an EPROM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever CE or OE is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29LV256 has 512 individual sectors, each 64-bytes. Using the software data protection feature, byte loads are used to enter the 64-bytes of a sector to be programmed. The AT29LV256 can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 64-byte sector must be loaded into the device. The AT29LV256 automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the WE or CE input with CE or WE low (respectively) and OE high. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE.

The 64-bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on WE (or CE) within 150 µs of the low to high transition of WE (or CE) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the sector address. The sector address must be valid during each high to low tran-

(continued)

Device Operation (Continued)

sition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29LV256 in the following ways: (a) V_{CC} sense— if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 3.3V ±10% power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to 3.6 volts.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29LV256 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29LV256 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 (including NC Pins) with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT29LV256-15	AT29LV256-20	AT29LV256-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V	3.3V ± 0.3V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A14 = V_{IL}, A9 = V_H (3), A0 = V_{IL}	Manufacturer Code (4)
				A1 - A14 = V_{IL}, A9 = V_H (3), A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: BC.
5. See details under Software Product Identification Entry/Exit.

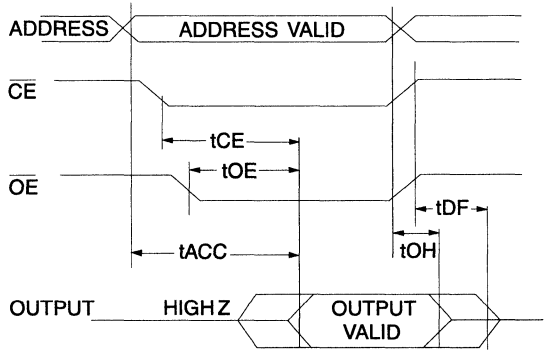
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

AC Read Characteristics

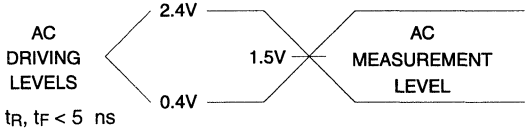
Symbol	Parameter	AT29LV256-15 Min	AT29LV256-15 Max	AT29LV256-20 Min	AT29LV256-20 Max	AT29LV256-25 Min	AT29LV256-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	100	0	120	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	50	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)

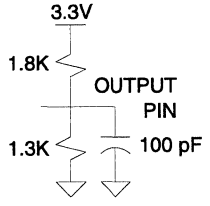


Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

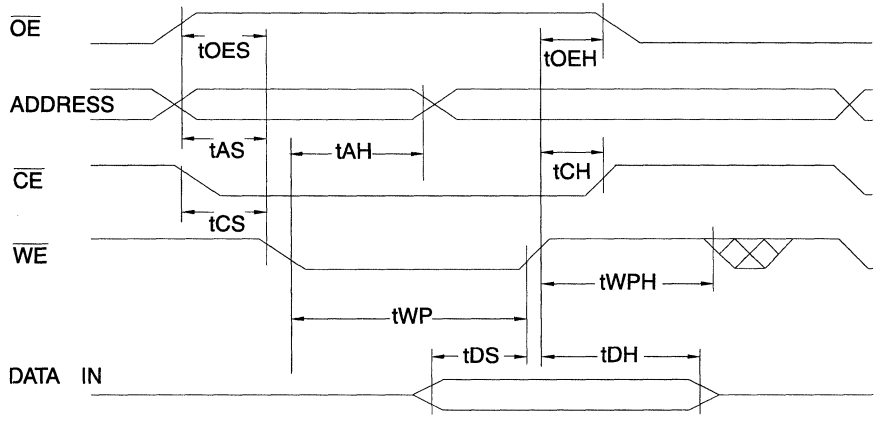
Note: 1. These parameters are characterized and not 100% tested.

AC Byte Load Characteristics

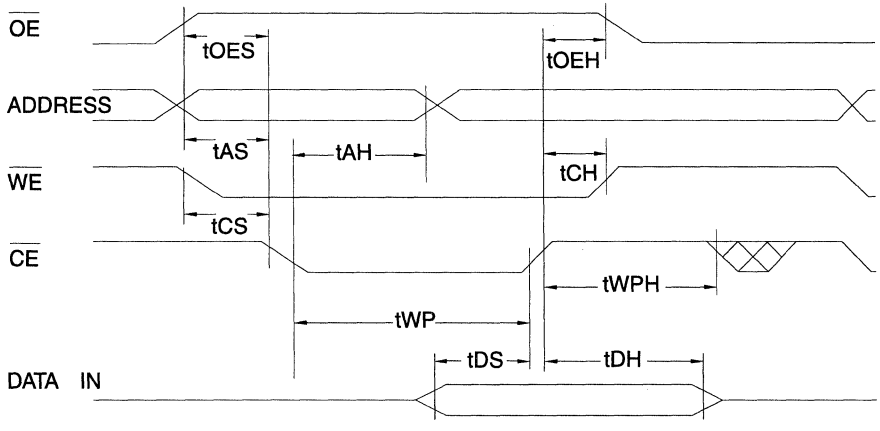
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	200		ns

AC Byte Load Waveforms [1, 2]

$\overline{WE}$ Controlled



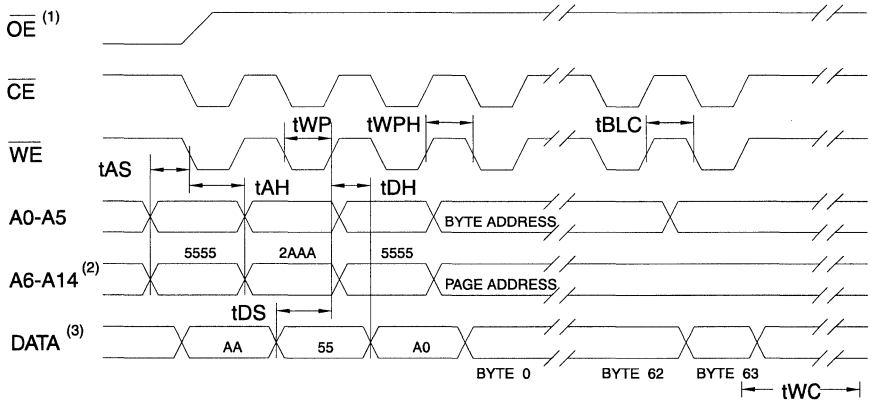
$\overline{CE}$ Controlled



Program Cycle Characteristics

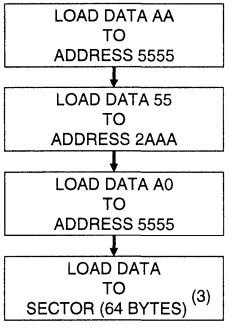
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Program Waveform (1, 2, 3)



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A6 through A14 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Programming Algorithm (1)



WRITES ENABLED

ENTER DATA PROTECT STATE (2)

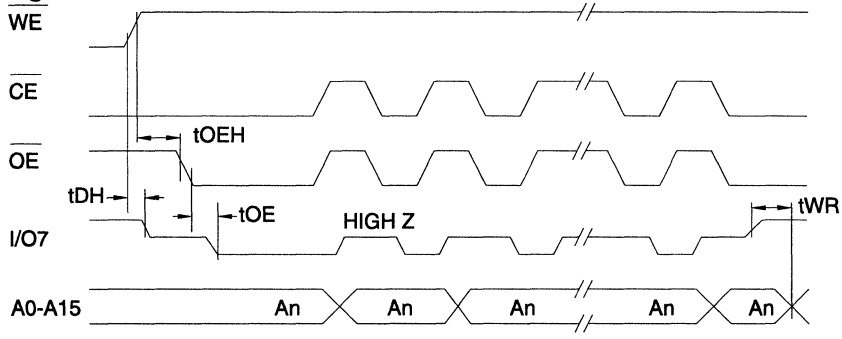
Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 64-bytes of data **MUST BE** loaded.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

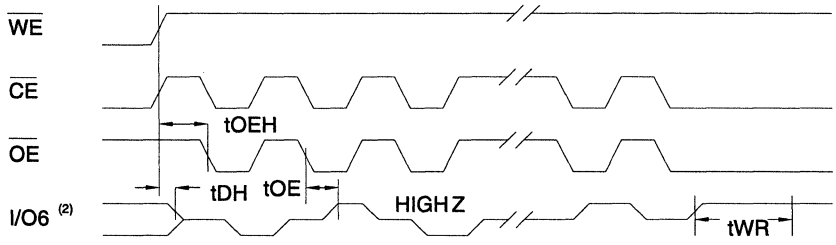


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

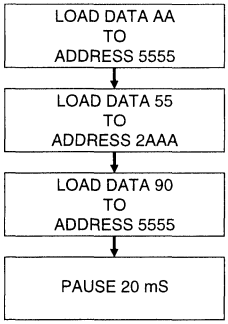
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 3]



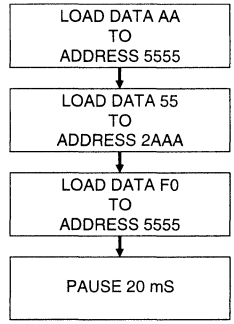
Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



ENTER PRODUCT IDENTIFICATION MODE [2, 3, 5]

Software Product Identification Exit [1]



EXIT PRODUCT IDENTIFICATION MODE [4]

Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A14 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: BC

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	15	0.02	AT29LV256-15JC AT29LV256-15TC	32J 28T	Commercial (0° to 70°C)
	15	0.05	AT29LV256-15JI AT29LV256-15TI	32J 28T	Industrial (-40° to 85°C)
200	15	0.02	AT29LV256-20JC AT29LV256-20PC AT29LV256-20TC	32J 28P6 28T	Commercial (0° to 70°C)
	15	0.05	AT29LV256-20JI AT29LV256-20PI	32J 28P6	Industrial (-40° to 85°C)
250	15	0.02	AT29LV256-25JC AT29LV256-25PC AT29LV256-25TC	32J 28P6 28T	Commercial (0° to 70°C)
	15	0.05	AT29LV256-25JI AT29LV256-25PI	32J 28P6	Industrial (-40° to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Thin Small Outline Package (TSOP)

Features

- Single Supply Voltage, Range 3V to 3.6V
- 3-Volt-Only Read and Write Operation
- Software Protected Programming
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Fast Read Access Time - 200 ns
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 512 Sectors (128 bytes/sector)
  - Internal Address and Data Latches for 128-Bytes
- Fast Sector Program Cycle Time - 20 ms Max.
- Internal Program Control and Timer
- $\overline{\text{DATA}}$ Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

512K (64K x 8) 3-volt Only CMOS Flash Memory

4

Description

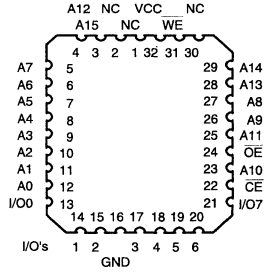
The AT29LV512 is a 3-volt-only in-system Flash programmable erasable read only memory (PEROM). Its 512K of memory is organized as 65,536 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 20 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

(continued)

Pin Configurations

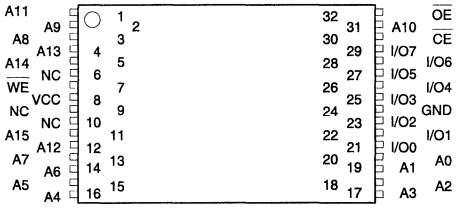
Pin Name	Function
A0 - A15	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

PLCC Top View



TSOP Top View

Type 1



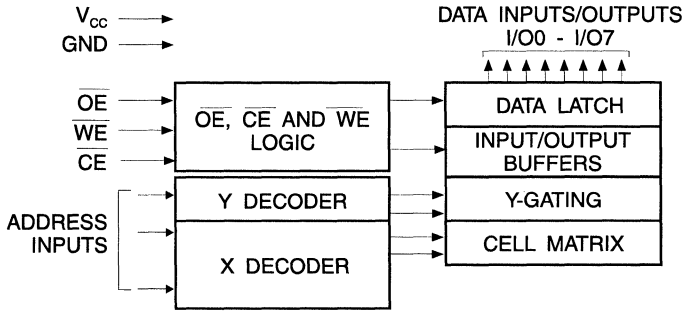
0177I

Description (Continued)

To allow for simple in-system reprogrammability, the AT29LV512 does not require high input voltages for programming. Three-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29LV512 is performed on a sector basis; 128-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128-bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29LV512 is accessed like an EPROM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever CE or OE is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29LV512 has 512 individual sectors, each 128-bytes. Using the software data protection feature, byte loads are used to enter the 128-bytes of a sector to be programmed. The AT29LV512 can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 128-byte sector must be loaded into the device. The AT29LV512 automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. After writing the three-byte command sequence (and after t_{WC}), the entire device is protected. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the WE or CE input with CE or WE low (respectively) and OE high. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE.

The 128-bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on WE (or CE) within 150 µs of the low to high transition of WE (or CE) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming

(continued)

Device Operation (Continued)

period will start. A7 to A15 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29LV512 in the following ways: (a) V_{CC} sense— if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 3.3V ±10% power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to 3.6 volts.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29LV512 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29LV512 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 (including NC Pins) with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT29LV512-15	AT29LV512-20	AT29LV512-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply (1)		3.3V ± 0.3V	3.3V ± 0.3V	3.3V ± 0.3V

1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A15 = V_{IL}, A9 = V_H (3), A0 = V_{IL}	Manufacturer Code (4)
				A1 - A15 = V_{IL}, A9 = V_H (3), A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: 3D.
5. See details under Software Product Identification Entry/Exit.

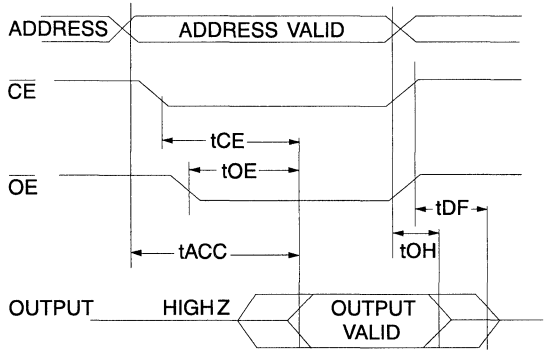
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

AC Read Characteristics

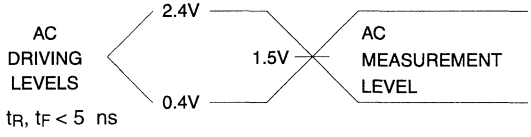
Symbol	Parameter	AT29LV512-15 Min	AT29LV512-15 Max	AT29LV512-20 Min	AT29LV512-20 Max	AT29LV512-25 Min	AT29LV512-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	100	0	120	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	50	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)

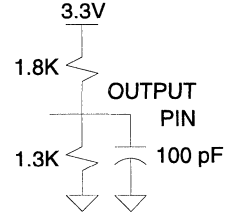


Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

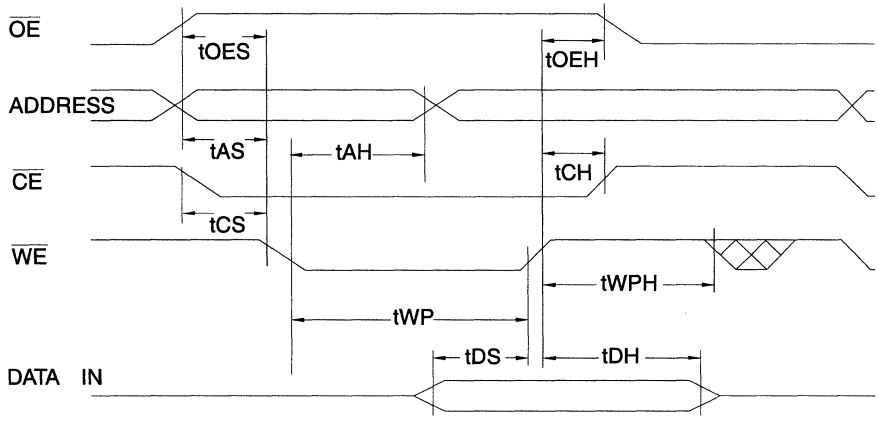
Note: 1. These parameters are characterized and not 100% tested.

AC Byte Load Characteristics

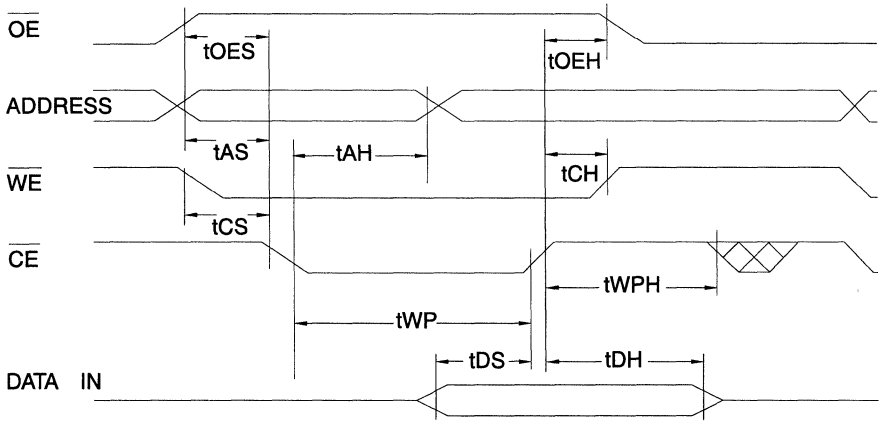
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	200		ns

AC Byte Load Waveforms [1, 2]

$\overline{WE}$ Controlled



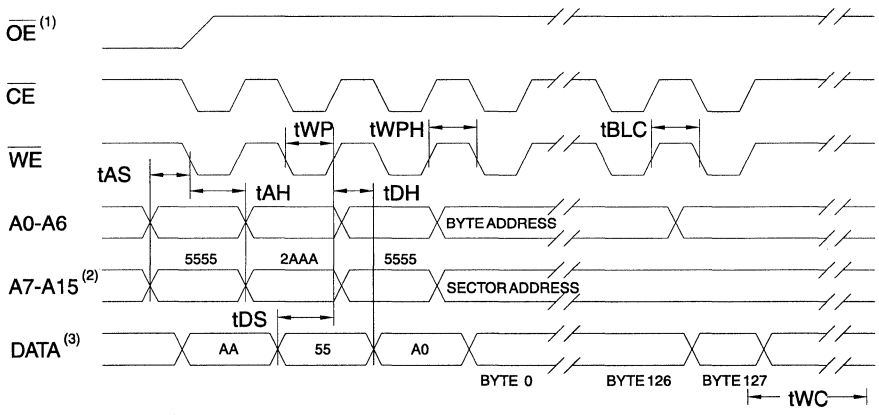
$\overline{CE}$ Controlled



Program Cycle Characteristics

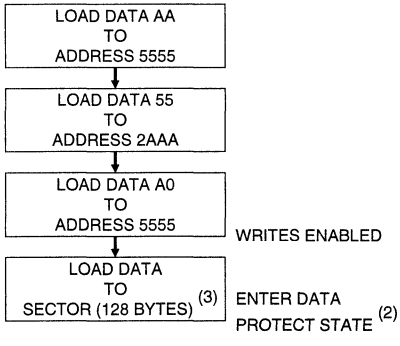
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Program Waveform (1, 2, 3)



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A7 through A15 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Programming Algorithm (1)



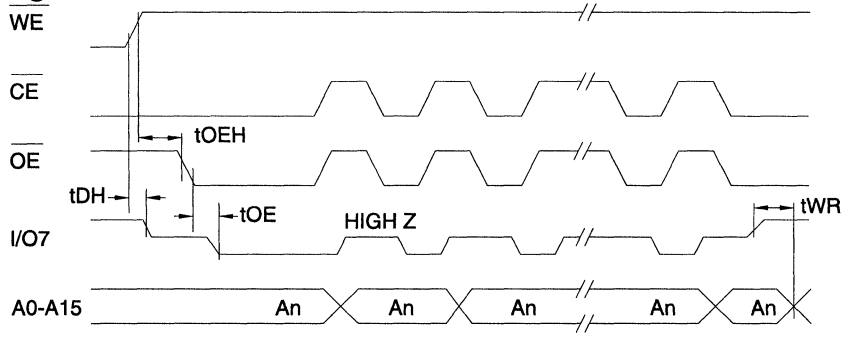
Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 128-bytes of data **MUST BE** loaded.

Data Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Data Polling Waveforms

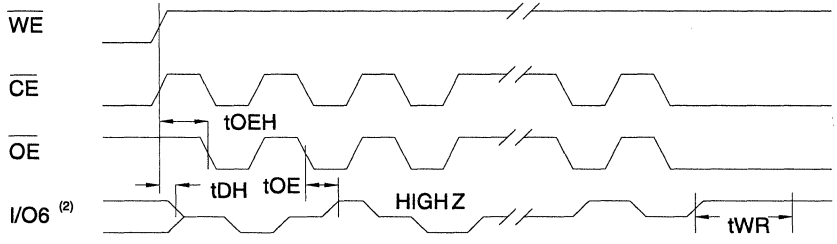


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

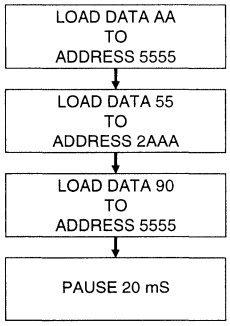
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 3]



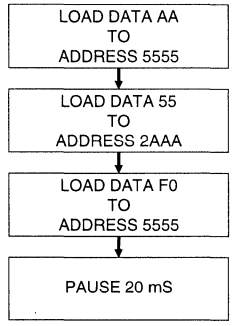
Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



ENTER PRODUCT IDENTIFICATION MODE [2, 3, 5]

Software Product Identification Exit [1]



EXIT PRODUCT IDENTIFICATION MODE [4]

Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A15 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: 3D

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	15	0.02	AT29LV512-15JC AT29LV512-15TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29LV512-15JI AT29LV512-15TI	32J 32T	Industrial (-40° to 85°C)
200	15	0.02	AT29LV512-20JC AT29LV512-20TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29LV512-20JI AT29LV512-20TI	32J 32T	Industrial (-40° to 85°C)
250	15	0.02	AT29LV512-25JC AT29LV512-25TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29LV512-25JI AT29LV512-25TI	32J 32T	Industrial (-40° to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Thin Small Outline Package (TSOP)

1 Megabit (128K x 8) 3-volt Only CMOS Flash

Features

- Single Supply Voltage, Range 3V to 3.6V
- 3-Volt-Only Read and Write Operation
- Software Protected Programming
- Fast Read Access Time - 150 ns
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Sectors (128 bytes/sector)
  - Internal Address and Data Latches for 128-Bytes
- Two 8 KB Boot Blocks with Lockout
- Fast Sector Program Cycle Time - 20 ms
- Internal Program Control and Timer
- DATA Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

The AT29LV010A is a 3-volt-only in-system Flash programmable and erasable read only memory (Flash). Its 1 megabit of memory is organized as 131,072 bytes by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 54 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 20 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

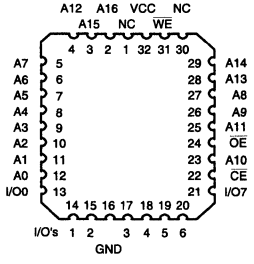
To allow for simple in-system reprogrammability, the AT29LV010A does not require high input voltages for programming. Three-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29LV010A is performed on a sector basis; 128-bytes of data are loaded into the device and then simultaneously programmed.

(continued)

Pin Configurations

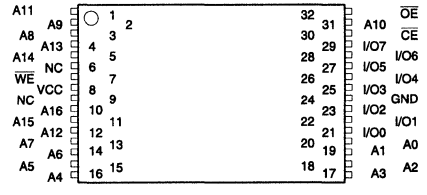
Pin Name	Function
A0 - A16	Addresses
CE	Chip Enable
OE	Output Enable
WE	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

PLCC Top View



TSOP Top View

Type 1

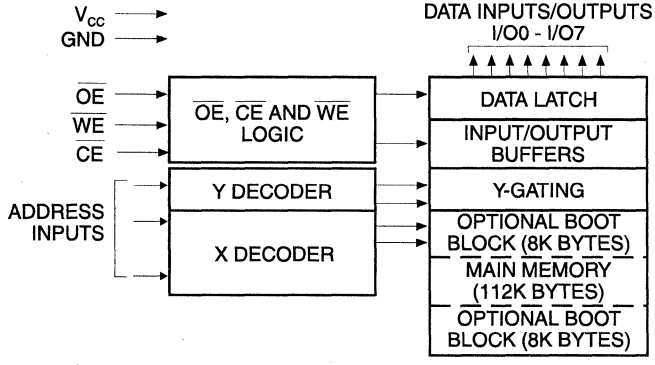


0520B

Description (Continued)

During a reprogram cycle, the address locations and 128-bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29LV010A is accessed like an EPROM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever CE or OE is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29LV010A has 1024 individual sectors, each 128-bytes. Using the software data protection feature, byte loads are used to enter the 128-bytes of a sector to be programmed. The AT29LV010A can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 128-byte sector must be loaded into the device. The data in any byte that is not loaded during the programming of its sector will be indeterminate. The AT29LV010A automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the WE or CE input with CE or WE low (respectively) and OE high. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE.

The 128-bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on WE (or CE) within 150 µs of the low to high transition of WE (or CE) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the sector address. The sector address must be valid during each high to low transition of WE (or CE). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

(continued)

Device Operation (Continued)

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29LV010A in the following ways: (a) V_{CC} sense— if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 3.3V ± 0.3V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can be driven from 0 to V_{CC} + 0.6V .

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT29LV010A features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7.

Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29LV010A provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

BOOT BLOCK PROGRAMMING LOCKOUT: The AT29LV010A has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 8K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 8K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29LV010A blocks are located in the first 8K bytes of memory and the last 8K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

(continued)

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 (including NC Pins) with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation (Continued)

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine whether programming of either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002H will show if programming the lower address boot block is locked out while reading location 1FFF2H will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

DC and AC Operating Range

		AT29LV010A-15	AT29LV010A-20	AT29LV010A-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply (1)		3.3V ± 0.3V	3.3V ± 0.3V	3.3V ± 0.3V

1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A16 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
				A1 - A16 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}, A1 - A16 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}, A1 - A16 = V_{IL}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: 35.
5. See details under Software Product Identification Entry/Exit.

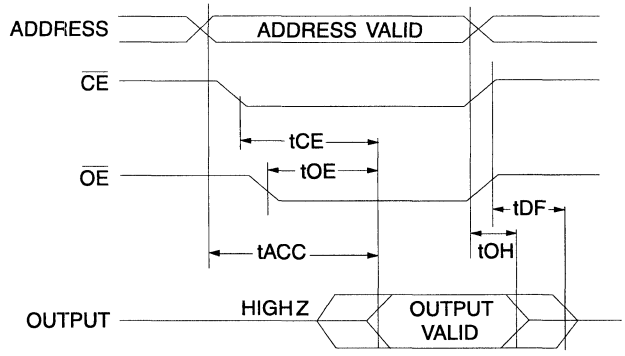
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

AC Read Characteristics

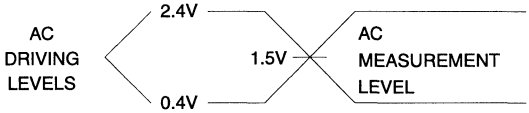
Symbol	Parameter	AT29LV010A-15 Min	AT29LV010A-15 Max	AT29LV010A-20 Min	AT29LV010A-20 Max	AT29LV010A-25 Min	AT29LV010A-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	100	0	100	0	120	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	50	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



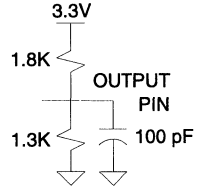
Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

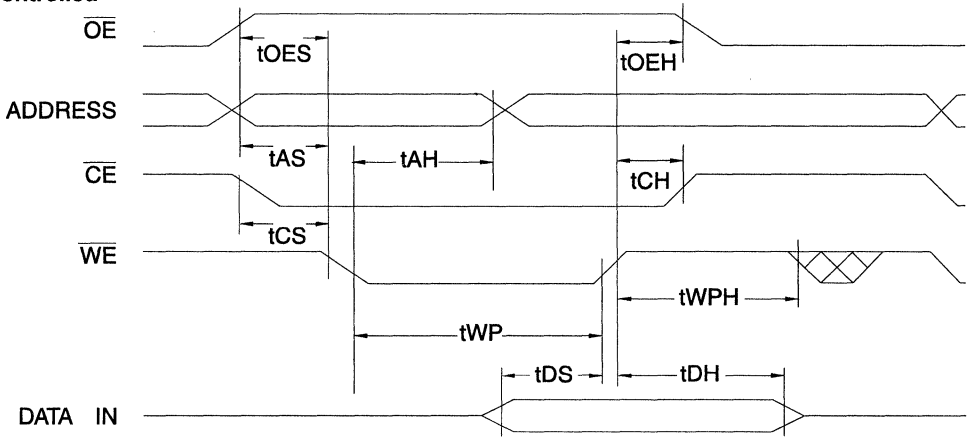
Note: 1. These parameters are characterized and not 100% tested.

AC Byte Load Characteristics

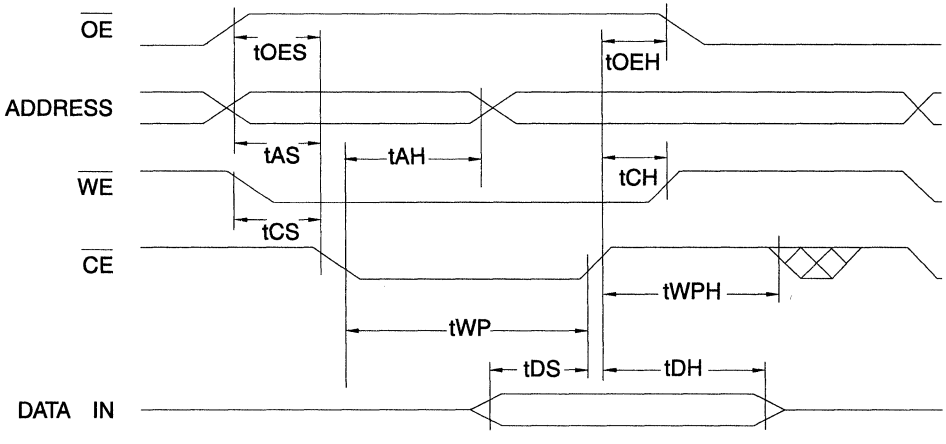
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	200		ns

AC Byte Load Waveforms [1, 2]

$\overline{WE}$ Controlled



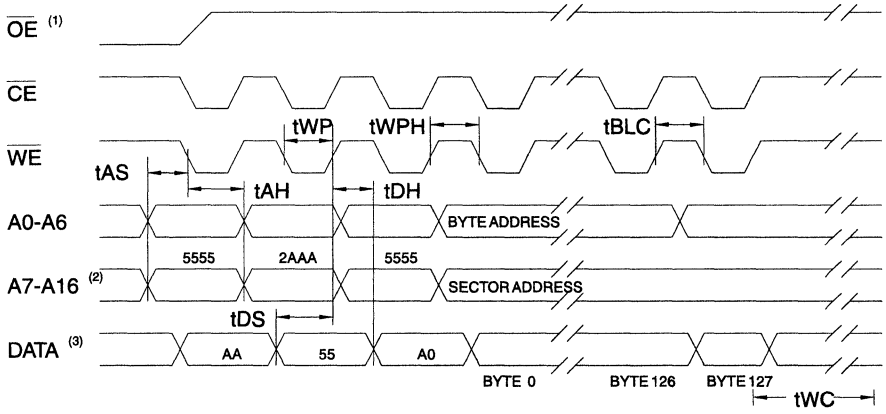
$\overline{CE}$ Controlled



Program Cycle Characteristics

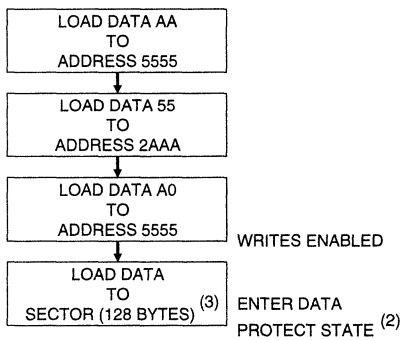
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Program Waveform



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A7 through A16 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Programming Algorithm (1)



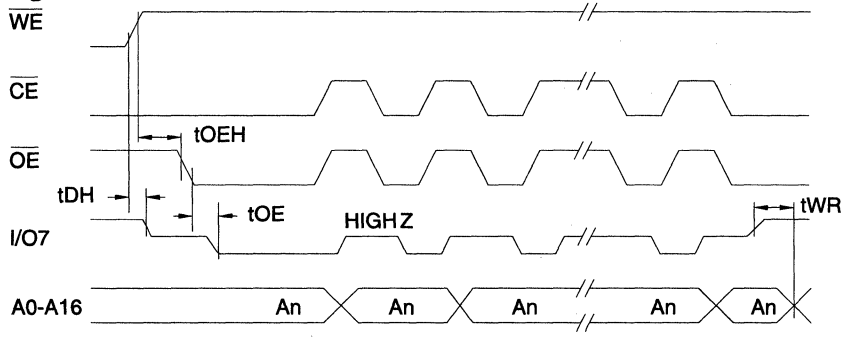
Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 128-bytes of data **MUST BE** loaded.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Data Polling Waveforms

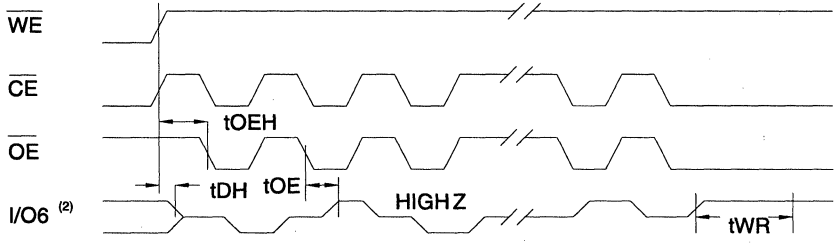


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

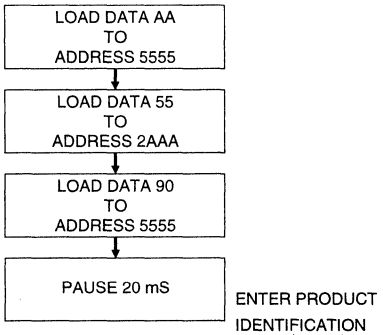
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 3]

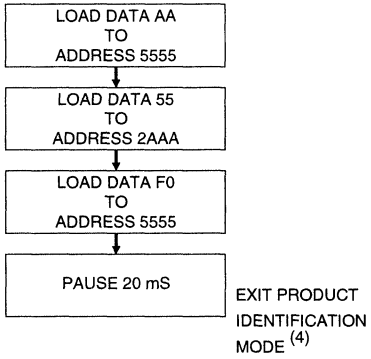


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

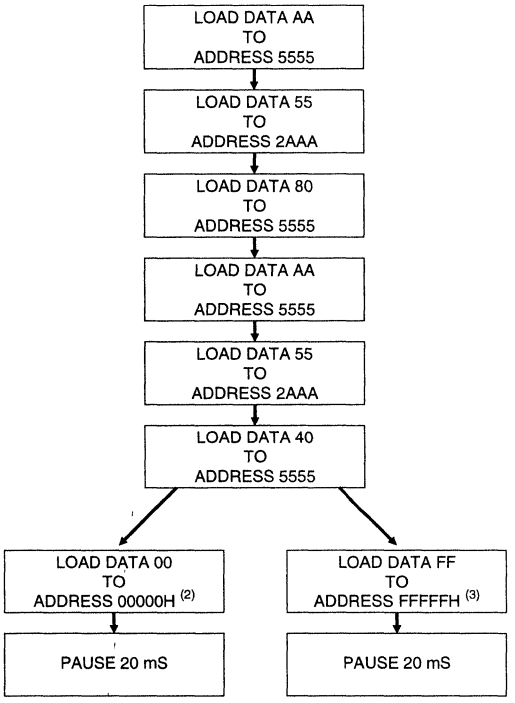


Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A16 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: 35

Boot Block Lockout Feature Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Lockout feature set on lower address boot block.
3. Lockout feature set on higher address boot block.

4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	15	0.02	AT29LV010A-15JC AT29LV010A-15TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29LV010A-15JI AT29LV010A-15TI	32J 32T	Industrial (-40° to 85°C)
200	15	0.02	AT29LV010A-20JC AT29LV010A-20TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29LV010A-20JI AT29LV010A-20TI	32J 32T	Industrial (-40° to 85°C)
250	15	0.02	AT29LV010A-25JC AT29LV010A-25TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29LV010A-25JI AT29LV010A-25TI	32J 32T	Industrial (-40° to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Thin Small Outline Package (TSOP)

1 Megabit (64K x 16) 3-volt Only CMOS Flash Memory

Features

- Single Voltage, Range 3V to 3.6V Supply
- 3-Volt-Only Read and Write Operation
- Software Protected Programming
- Fast Read Access Time - 150 ns
- Low Power Dissipation
  - 15 mA Active Current
  - 50 µA CMOS Standby Current
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 512 Sectors (128 words/sector)
  - Internal Address and Data Latches for 128 Words
- Fast Sector Program Cycle Time - 20 ms
- Internal Program Control and Timer
- DATA Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

The AT29LV1024 is a 3-volt-only in-system Flash programmable and erasable read only memory (PEROM). Its 1 megabit of memory is organized as 65,536 words by 16 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 50 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

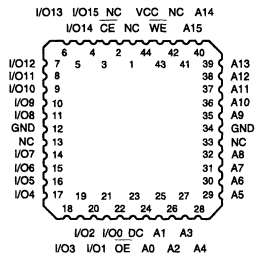
To allow for simple in-system reprogrammability, the AT29LV1024 does not require high input voltages for programming. Three-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an

(continued)

Pin Configurations

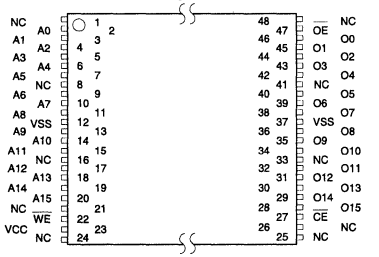
Pin Name	Function
A0 - A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PLCC Top View



TSOP Top View

Type 1



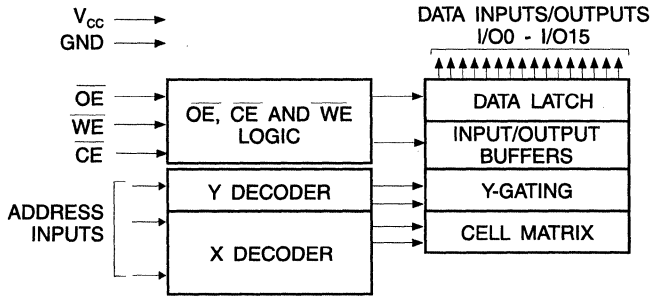
0564A

Description (Continued)

EPROM. Reprogramming the AT29LV1024 is performed on a sector basis; 128 words of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128 words of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7 or I/O15. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29LV1024 is accessed like an EPROM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever CE or OE is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29LV1024 has 512 individual sectors, each 128 words. Using the software data protection feature, word loads are used to enter the 128 words of a sector to be programmed. The AT29LV1024 can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a word of data within the sector is to be changed, data for the entire 128 word sector must be loaded into the device. The AT29LV1024 automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the 3 word command sequence will start the internal write timers. No data will be written to the device; however, for the duration of twc, a read operation will effectively be a polling operation.

After the software data protection's 3 word command code is given, a word load is performed by applying a low pulse on the WE or CE input with CE or WE low (respectively) and OE high. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE.

The 128 words of data must be loaded into each sector. Any word that is not loaded during the programming of its sector will be erased to read FFFFH. Once the words of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data word has been loaded into the device, successive words are entered in the same manner. Each new word to be programmed must have its high to low transition on WE (or CE) within 150 µs of the low to high transition of WE (or CE) of the preceding word. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A15 specify the sector address. The sector address must be valid during each high to low transition of WE (or CE). A0 to A6 specify the word address within the sector. The words may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the du-

(continued)

Device Operation (Continued)

ration of t_{WC}, a read operation will effectively be a polling operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29LV1024 in the following ways: (a) V_{CC} sense— if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 3.3V ±10% power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can be driven from 0 to 3.6V.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for various Flash densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29LV1024 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last word loaded will result in the complement of the loaded data on I/O7 and I/O15. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29LV1024 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 and I/O14 toggling between one and zero. Once the program cycle has completed, I/O6 and I/O14 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT29LV1024-15	AT29LV1024-20	AT29LV1024-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply (1)		3.3V ± 0.3V	3.3V ± 0.3V	3.3V ± 0.3V

1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A15 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
				A1 - A15 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: 26
5. See details under Software Product Identification Entry/Exit.

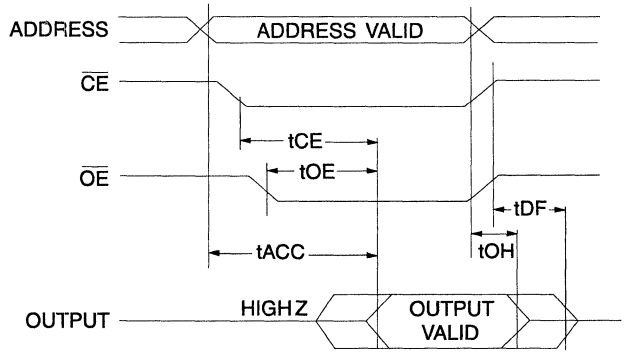
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		50	µA
			Ind.		100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA, V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = 3.0V			.45	V
V_{OH1}	Output High Voltage	I_{OH} = 100 µA, V_{CC} = 3.0V		2.4		V

AC Read Characteristics

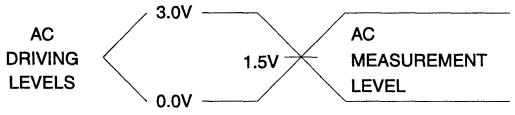
Symbol	Parameter	AT29LV1024-15		AT29LV1024-20		AT29LV1024-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	85	0	100	0	120	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	50	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



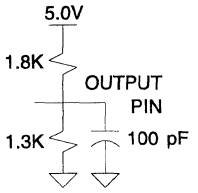
Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

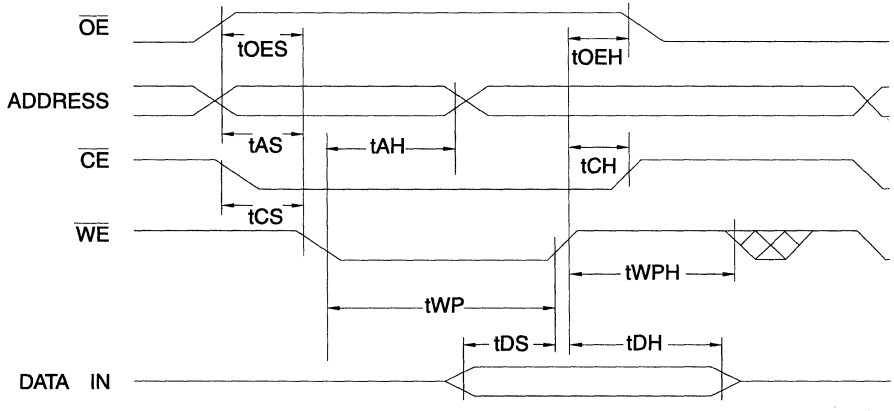
Note: 1. This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

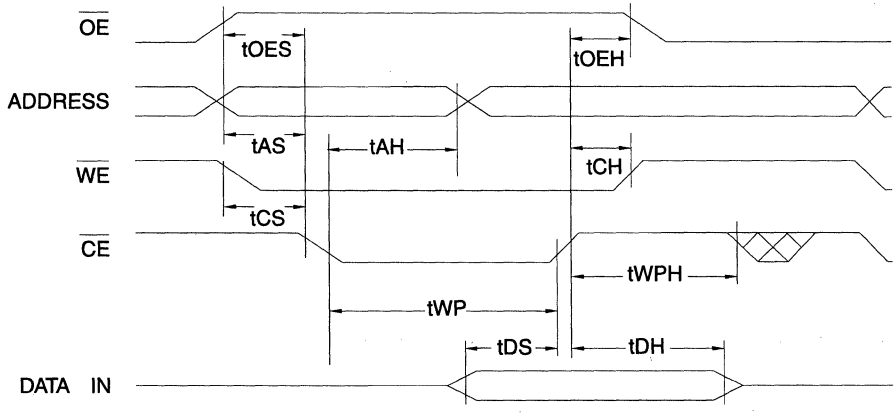
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	200		ns

AC Word Load Waveforms [1, 2]

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled



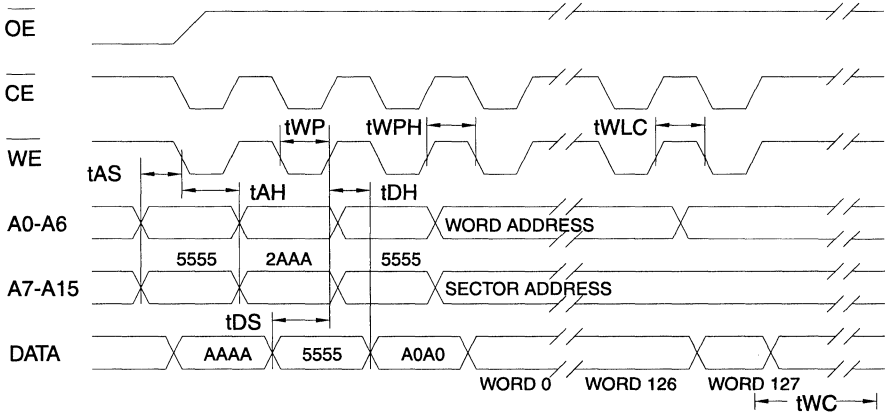
Notes: 1. The software data protection commands must be applied prior to word loads.

2. A complete sector (128 words) should be loaded using these waveforms as shown in the Software Protected Word Load waveforms (see next page).

Program Cycle Characteristics

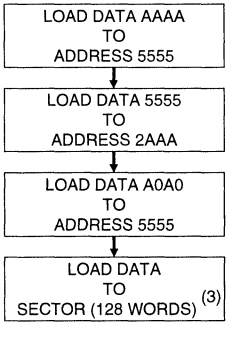
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	200		ns
t_{WLC}	Word Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Program Waveform (1, 2, 3)



Notes: 1. A7 through A15 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All words that are not loaded within the sector being programmed will be indeterminate.**

Programming Algorithm (1)



WRITES ENABLED

ENTER DATA PROTECT STATE (2)

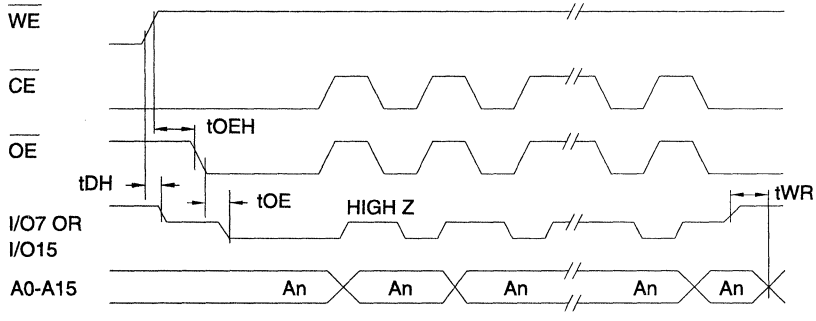
Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 128 words of data **MUST BE** loaded.

Data Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Data Polling Waveforms

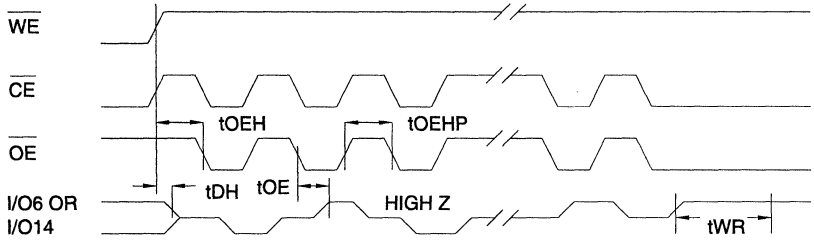


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

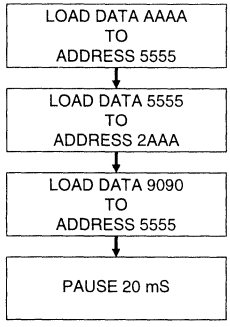
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]

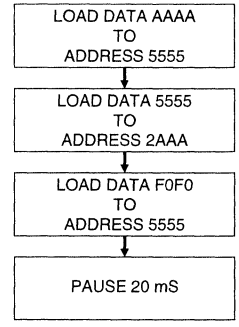


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 and I/O14 may vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O15 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A15 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: 26

4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	15	0.05	AT29LV1024-15JC AT29LV1024-15TC	44J 48T	Commercial (0° to 70°C)
	15	0.05	AT29LV1024-15JI AT29LV1024-15TI	44J 48T	Industrial (-40° to 85°C)
200	15	0.05	AT29LV1024-20JC AT29LV1024-20TC	44J 48T	Commercial (0° to 70°C)
	15	0.10	AT29LV1024-20JI AT29LV1024-20TI	44J 48T	Industrial (-40° to 85°C)
250	15	0.05	AT29LV1024-25JC AT29LV1024-25TC	44J 48T	Commercial (0° to 70°C)
	15	0.10	AT29LV1024-25JI AT29LV1024-25TI	44J 48T	Industrial (-40° to 85°C)

Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
48T	48 Lead, Thin Small Outline Package (TSOP)

2 Megabit (256K x 8) 3-volt Only CMOS Flash Memory

Features

- Single Voltage, Range 3V to 3.6V Supply
- 3-Volt-Only Read and Write Operation
- Software Protected Programming
- Fast Read Access Time - 200 ns
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Sectors (256 bytes/sector)
  - Internal Address and Data Latches for 256-Bytes
- Two 8 KB Boot Blocks with Lockout
- Fast Sector Program Cycle Time - 20 ms
- Internal Program Control and Timer
- DATA Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

The AT29LV020 is a 3-volt-only in-system Flash programmable and erasable read only memory (PEROM). Its 2 megabits of memory is organized as 262,144 bytes by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 20 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

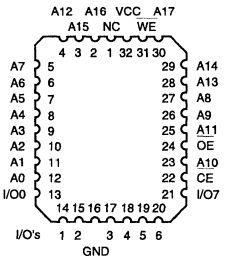
To allow for simple in-system reprogrammability, the AT29LV020 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an

(continued)

Pin Configurations

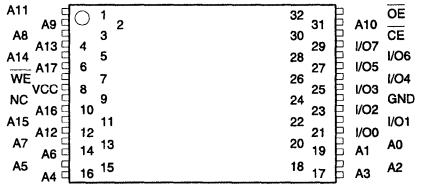
Pin Name	Function
A0 - A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

PLCC Top View



TSOP Top View

Type 1



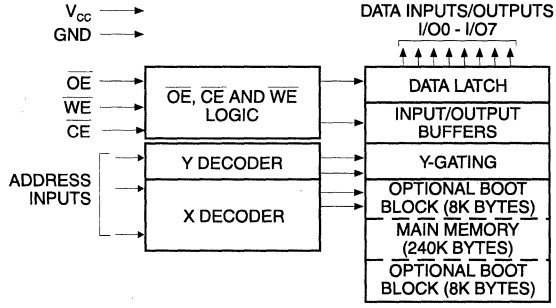
0565A

Description (Continued)

EPROM. Reprogramming the AT29LV020 is performed on a sector basis; 256-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 256-bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29LV020 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29LV020 has 1024 individual sectors, each 256-bytes. Using the software data protection feature, byte loads are used to enter the 256-bytes of a sector to be programmed. The AT29LV020 can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 256-byte sector must be loaded into the device. The AT29LV020 automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

The 256-bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFH. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A8 to A17 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A7 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

(continued)

Device Operation (Continued)

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29LV020 in the following ways: (a) V_{CC} sense— if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 3.3V ±10% power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can be driven from 0 to 3.6V.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29LV020 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29LV020 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

BOOT BLOCK PROGRAMMING LOCKOUT: The AT29LV020 has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 8K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 8K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29LV020 blocks are located in the first 8K bytes of memory and the last 8K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

(continued)

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 (including NC Pins) with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation (Continued)

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine whether programming of either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002H will show if programming the lower address boot block is locked out while reading location FFFF2H will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

DC and AC Operating Range

		AT29LV020-20	AT29LV020-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply (1)		3.3V ± 0.3V	3.3V ± 0.3V

1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A17 = V_{IL}, A9 = V_H (3), A0 = V_{IL}	Manufacturer Code (4)
				A1 - A17 = V_{IL}, A9 = V_H (3), A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: BA.
5. See details under Software Product Identification Entry/Exit.

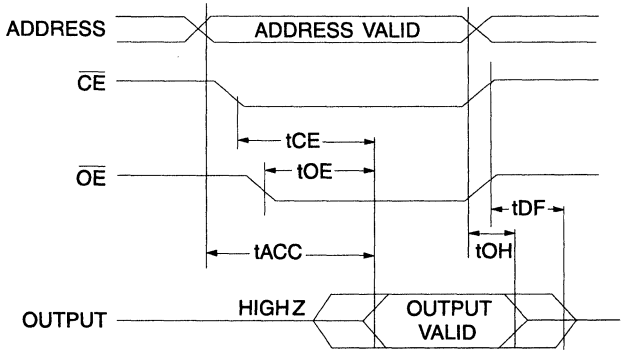
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

AC Read Characteristics

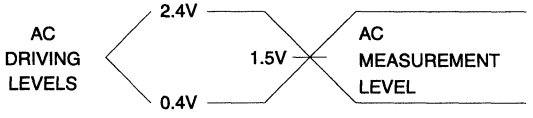
Symbol	Parameter	AT29LV020-20 Min	AT29LV020-20 Max	AT29LV020-25 Min	AT29LV020-25 Max	Units
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	100	0	120	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms (1, 2, 3, 4)



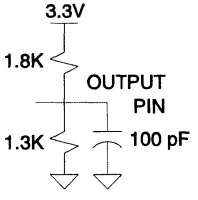
Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

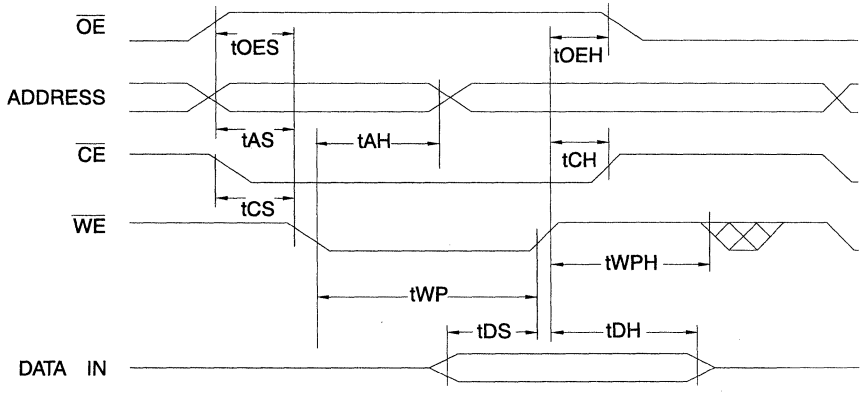
Note: 1. These parameters are characterized and not 100% tested.

AC Byte Load Characteristics

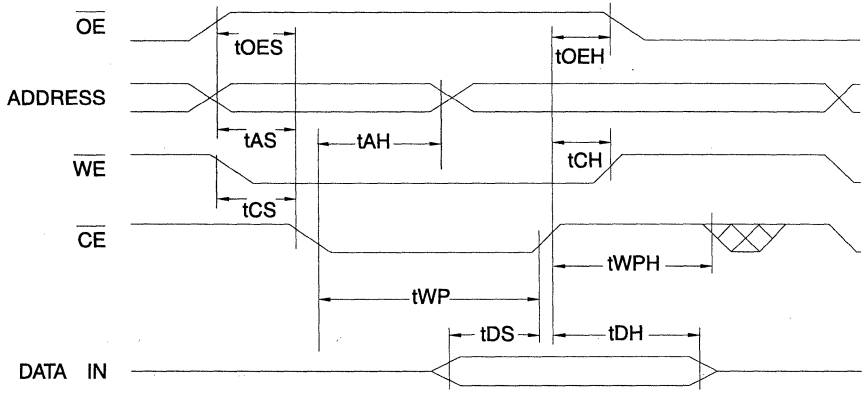
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	200		ns

AC Byte Load Waveforms [1, 2]

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled



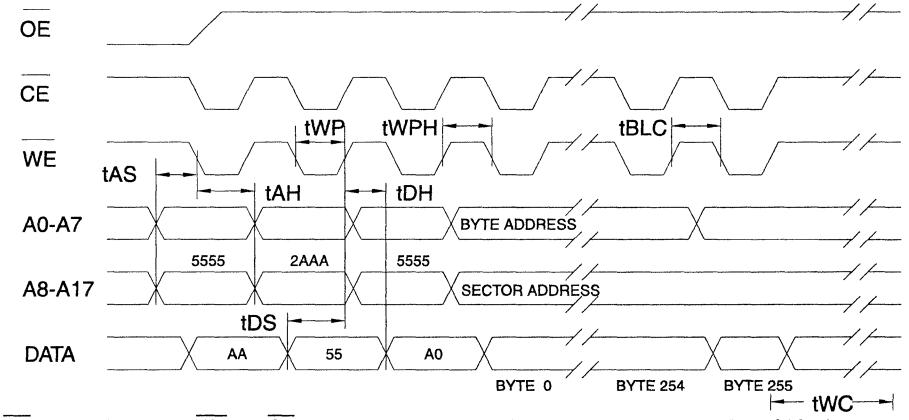
Notes: 1. The software data protection commands must be applied prior to byte loads.

2. A complete sector (256 bytes) should be loaded using these waveforms as shown in the Software Protected Byte Load waveforms (see next page).

Program Cycle Characteristics

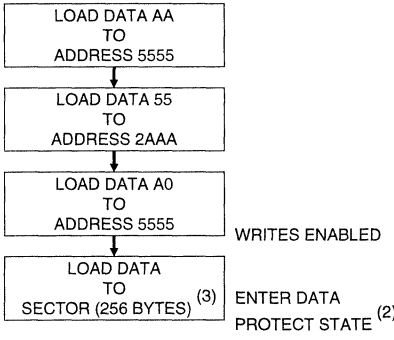
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Program Waveform



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A8 through A17 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Programming Algorithm (1)



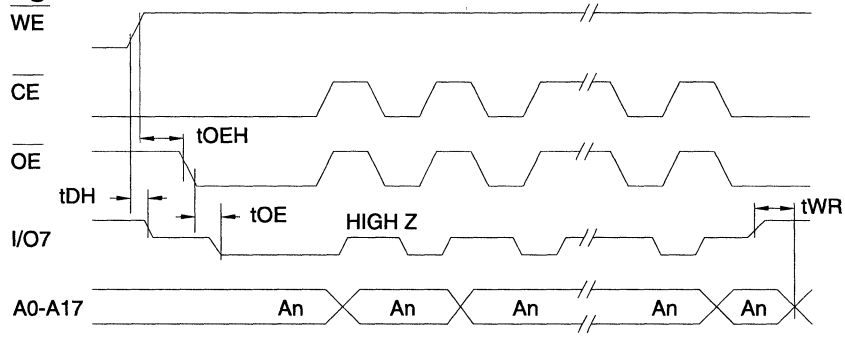
Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 256-bytes of data **MUST BE** loaded.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

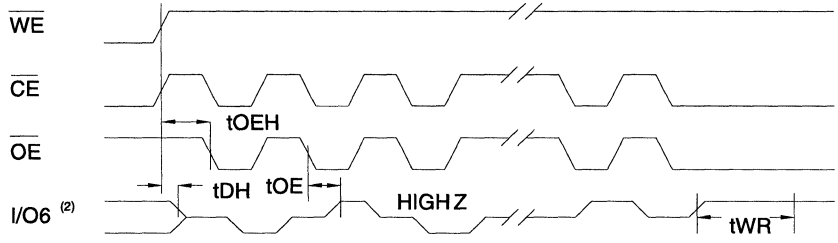


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

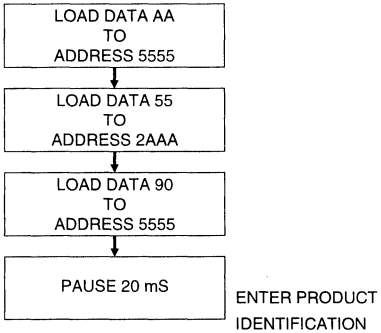
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 3]

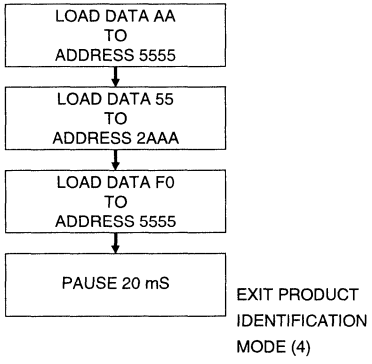


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry (1)

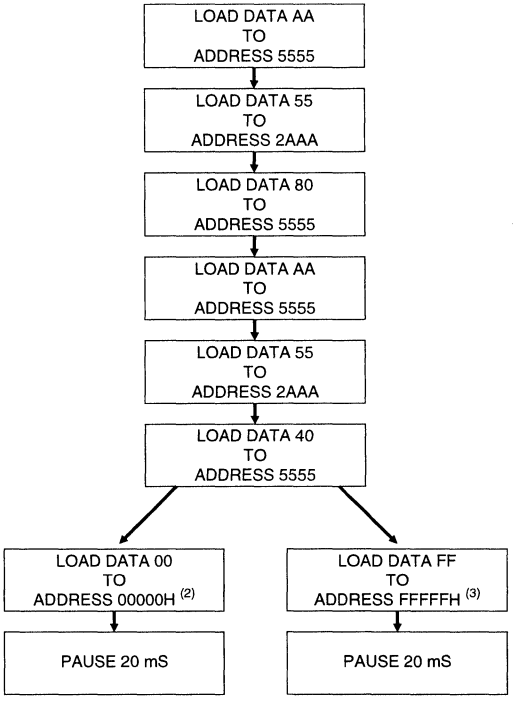


Software Product Identification Exit (1)



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A17 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: BA

Boot Block Lockout Feature Enable Algorithm (1)



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Lockout feature set on lower address boot block.
3. Lockout feature set on higher address boot block.

4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT29LV020-20JC AT29LV020-20TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29LV020-20JI AT29LV020-20TI	32J 32T	Industrial (-40° to 85°C)
250	15	0.02	AT29LV020-25JC AT29LV020-25TC	32J 32T	Commercial (0° to 70°C)
	15	0.05	AT29LV020-25JI AT29LV020-25TI	32J 32T	Industrial (-40° to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32T	32 Lead, Thin Small Outline Package (TSOP)

Features

- Single Voltage, Range 3V to 3.6V Supply
- 3-Volt-Only Read and Write Operation
- Software Protected Programming
- Fast Read Access Time - 200 ns
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 2048 Sectors (256 bytes/sector)
  - Internal Address and Data Latches for 256-Bytes
- Two 16 KB Boot Blocks with Lockout
- Fast Sector Program Cycle Time - 20 ms Max.
- Internal Program Control and Timer
- $\overline{\text{DATA}}$ Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

4 Megabit (512K x 8) 3-volt Only 256 Byte Sector CMOS Flash Memory

4

Description

The AT29LV040A is a 3-volt-only in-system Flash Programmable and Erasable Read Only Memory (PEROM). Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS EEPROM technology, the device offers access times up to 200 ns, and a low 54 mW power dissipation. When the device is deselected, the CMOS standby current is less than 20 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times. The programming algorithm is compatible with other devices in Atmel's 3-volt-only Flash memories.

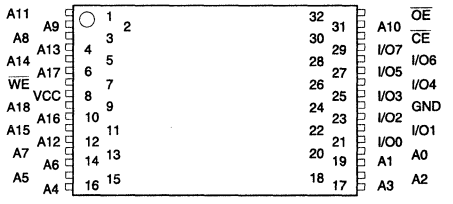
To allow for simple in-system reprogrammability, the AT29LV040A does not require high input voltages for programming. Three-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29LV040A is performed on a sector basis; 256-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 256-bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Pin Configurations

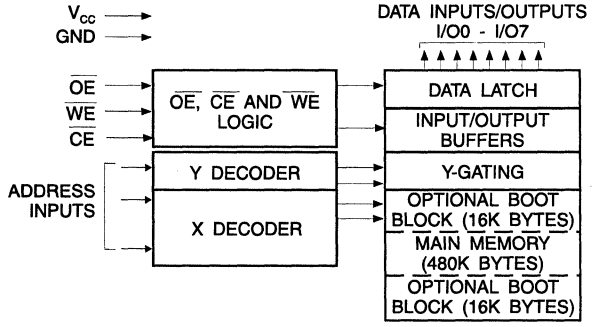
Pin Name	Function
A0 - A18	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

TSOP Top View
Type 1



0334C

Block Diagram



Device Operation

READ: The AT29LV040A is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

SOFTWARE DATA PROTECTION PROGRAMMING: The AT29LV040A has 2048 individual sectors, each 256-bytes. Using the software data protection feature, byte loads are used to enter the 256-bytes of a sector to be programmed. The AT29LV040A can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 256-byte sector must be loaded into the device. The AT29LV040A automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

The 256-bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFH. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A8 to A18 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A7 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29LV040A in the following ways: (a) V_{CC} sense— if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 3.3V ±10% power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to 3.6V.

(continued)

Device Operation (Continued)

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{\text{DATA}}$ POLLING: The AT29LV040A features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT29LV040A provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

BOOT BLOCK PROGRAMMING LOCKOUT: The AT29LV040A has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 16K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 16K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29LV040A blocks are located in the first 16K bytes of memory and the last 16K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine whether programming of either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002H will show if programming the lower address boot block is locked out while reading location

FFFF2H will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 (including NC Pins) with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT29LV040A-20	AT29LV040A-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply [1]		3.3V ± 0.3V	3.3V ± 0.3V

1. After power is applied and V_{CC} is at the minimum specified data sheet value, the sytem should wait 20 ms before an operational mode is started.

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program [2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X [1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A18 = V_{IL}, A9 = V_H [3], A0 = V_{IL}	Manufacturer Code [4]
				A1 - A18 = V_{IL}, A9 = V_H [3], A0 = V_{IH}	Device Code [4]
Software [5]				A0 = V_I	Manufacturer Code [4]
				A0 = V_{IH}	Device Code [4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: C4.
5. See details under Software Product Identification Entry/Exit.

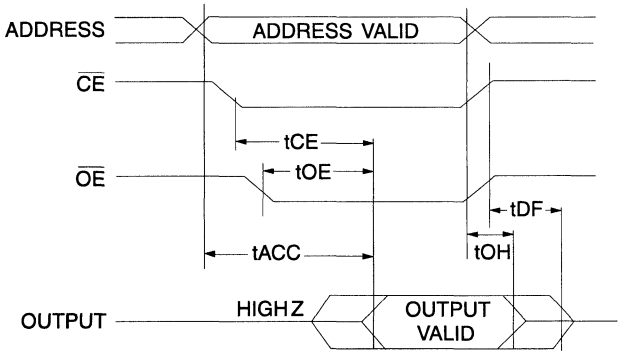
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		20	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

AC Read Characteristics

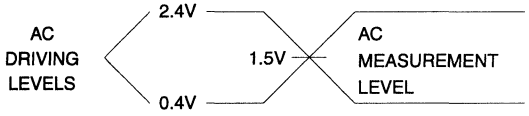
Symbol	Parameter	AT29LV040A-20 Min	AT29LV040A-20 Max	AT29LV040A-25 Min	AT29LV040A-25 Max	Units
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	100	0	120	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms (1, 2, 3, 4)



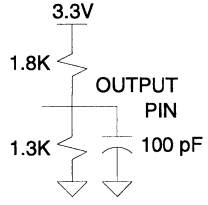
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

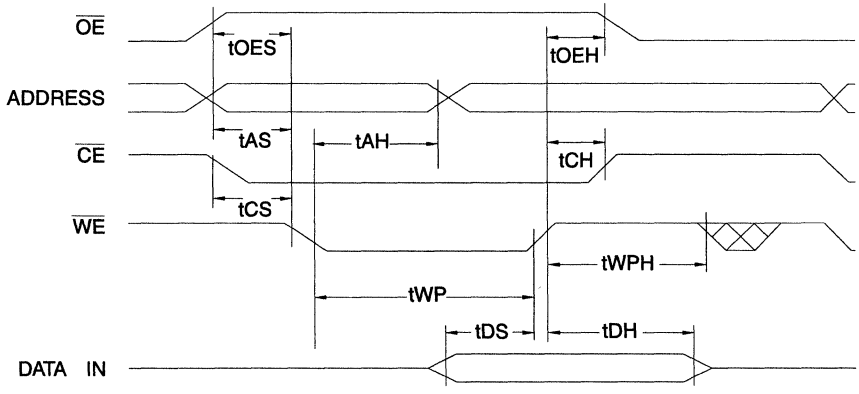
Note: 1. These parameters are characterized and not 100% tested.

AC Byte Load Characteristics

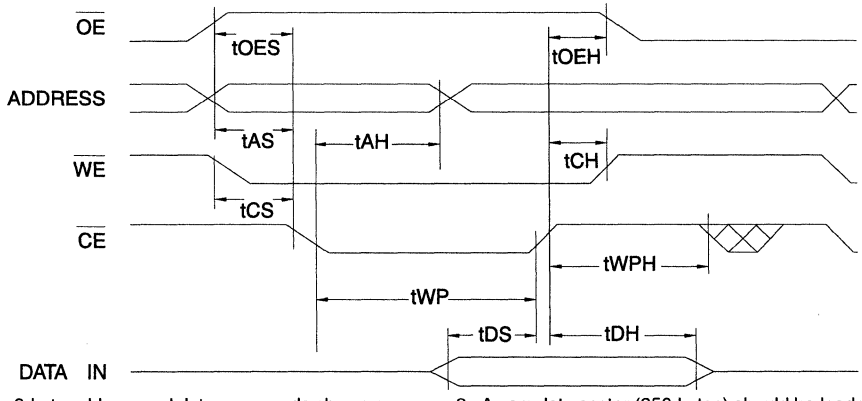
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	100		ns

AC Byte Load Waveforms [1, 2]

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled



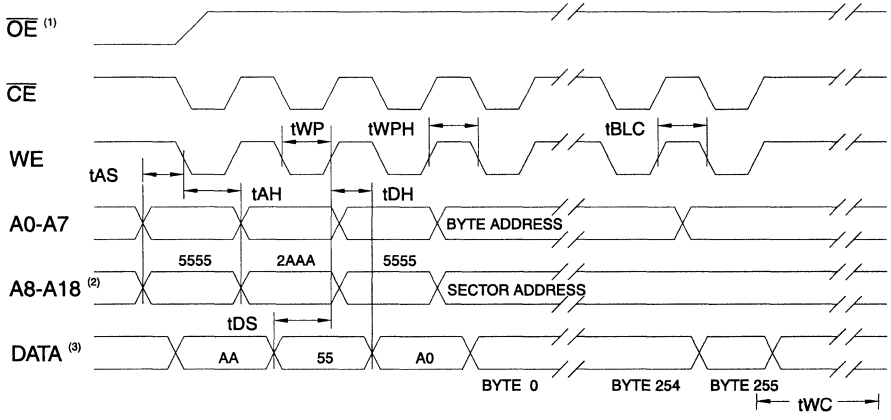
Notes: 1. The 3-byte address and data commands shown on the next page must be applied prior to byte loads.

2. A complete sector (256-bytes) should be loaded using the waveforms shown in these byte load waveform diagrams.

Program Cycle Characteristics

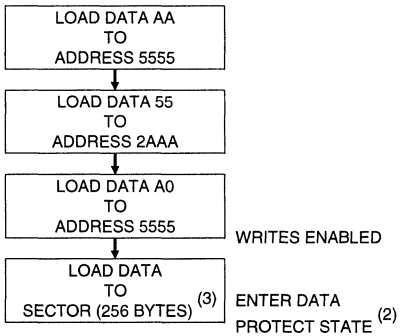
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Program Waveform



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A8 through A18 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Programming Algorithm (1)



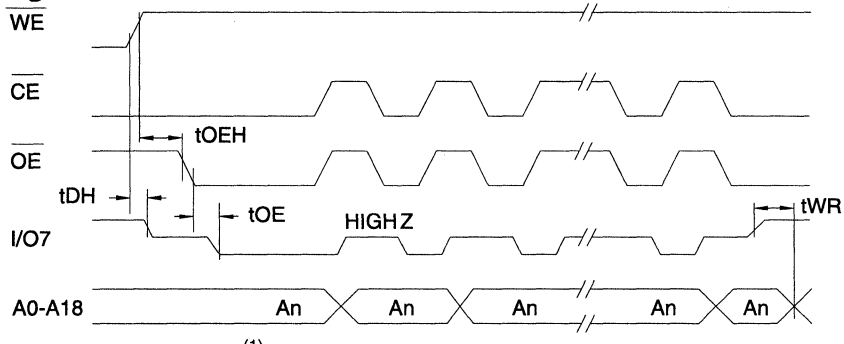
Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 256-bytes of data **MUST BE** loaded.

$\overline{\text{Data}}$ Polling Characteristicsn [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

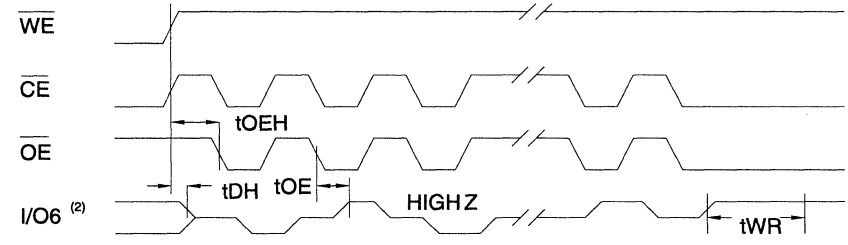


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

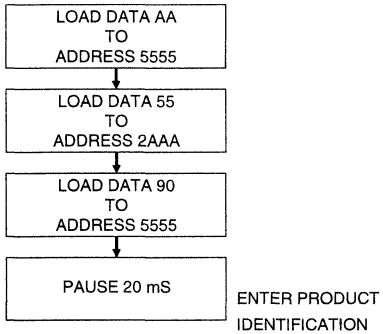
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 3]

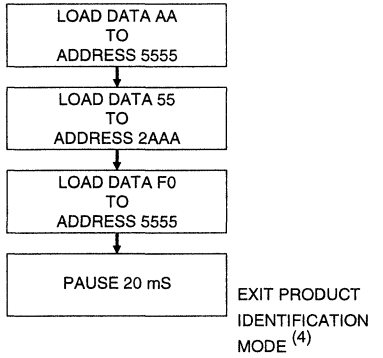


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

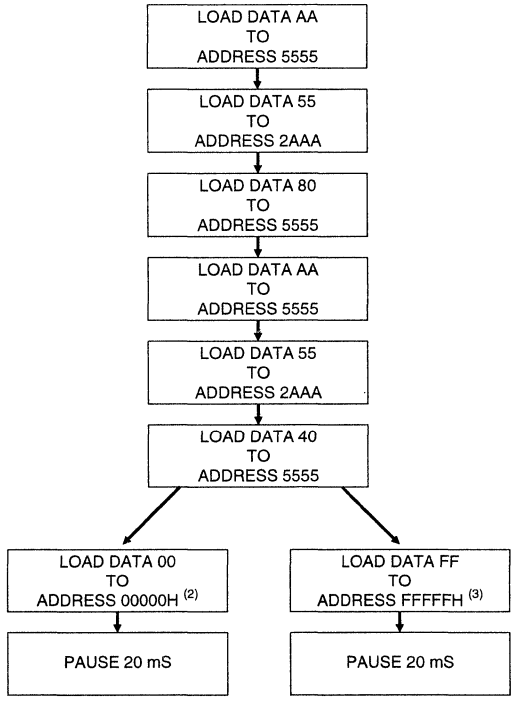


Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: C4

Boot Block Lockout Feature Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Lockout feature set on lower address boot block.
3. Lockout feature set on higher address boot block.

4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.02	AT29LV040A-20TC	32T	Commercial (0° to 70°C)
	15	0.05	AT29LV040A-20TI	32T	Industrial (-40° to 85°C)
250	15	0.02	AT29LV040A-25TC	32T	Commercial (0° to 70°C)
	15	0.05	AT29LV040A-25TI	32T	Industrial (-40° to 85°C)

Package Type	
32T	32 Lead, Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 70 ns
- 5-Volt-Only Reprogramming
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - Internal Address and Data Latches for 64-Bytes
- Internal Program Control and Timer
- Hardware and Software Data Protection
- Fast Program Cycle Times
  - Page (64-Byte) Program Time - 10 ms
  - Chip Erase Time - 10 ms
- DATA Polling for End of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 300 µA CMOS Standby Current
- Typical Endurance > 10,000 Cycles
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

256K (32K x 8) 5-volt Only CMOS Flash Memory

4

Description

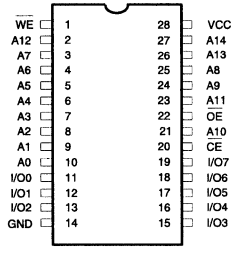
The AT29C256 is a 5-volt-only in-system Flash programmable and erasable read only memory (PEROM). Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 70 ns with power dissipation of just 275 mW. When the device is deselected, the CMOS standby current is less than 300 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

(continued)

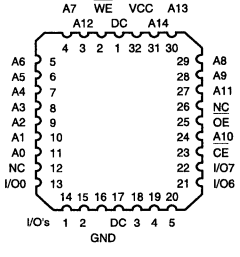
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

DIP Top View

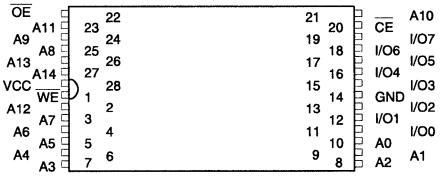


PLCC Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

TSOP Top View
Type 1



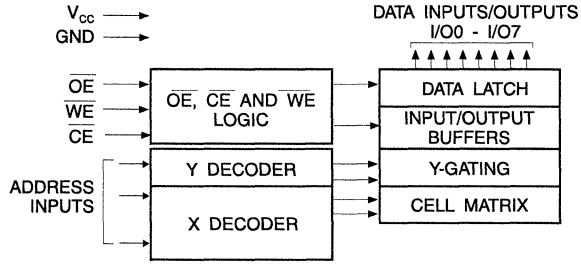
0046L

Description (Continued)

To allow for simple in-system reprogrammability, the AT29C256 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from a static RAM. Reprogramming the AT29C256 is performed on a page basis; 64-bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a 6-byte software code (although erasure before programming is not needed).

During a reprogram cycle, the address locations and 64-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Block Diagram



Device Operation

READ: The AT29C256 is accessed like a static RAM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever CE or OE is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the WE or CE input with CE or WE low (respectively) and OE high. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE. Byte loads are used to enter the 64-bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be indeterminate. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on WE (or CE) within 150 µs of the low to high transition of WE (or CE) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of WE (or CE). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C256. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

(continued)

Device Operation (Continued)

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. The 64-bytes of data must be loaded into each sector by the same procedure as outlined in the program section under device operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C256 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer and may be accessed by a hardware operation. For details, see Operating Modes or Product Identification.

$\overline{DATA}$ POLLING: The AT29C256 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C256 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT29C256-70	AT29C256-90	AT29C256-12	AT29C256-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Write Inhibit	X	X	V_{IH}		
Write Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
High Voltage Chip Erase	V_{IL}	V_H (3)	V_{IL}	X	High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A14 = V_{IL}, A9 = V_H, A0 = V_{IL}	Manufacturer Code (4)
				A1 - A14 = V_{IL}, A9 = V_H, A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: DC
5. See details under Software Product Identification Entry/Exit.

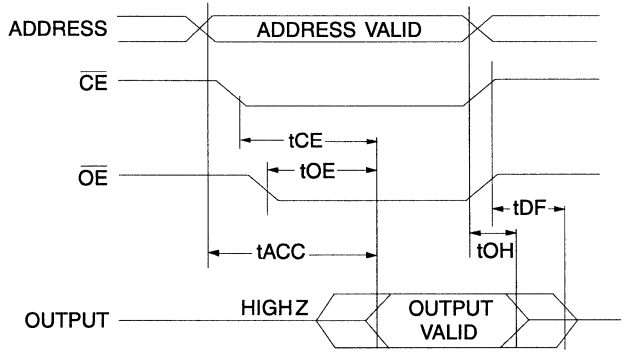
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

AC Read Characteristics

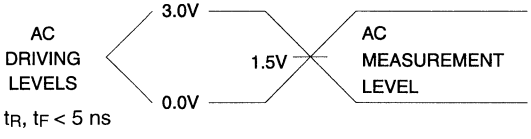
Symbol	Parameter	AT29C256-70		AT29C256-90		AT29C256-12		AT29C256-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90		120		150	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		70		90		120		150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	40	0	50	0	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



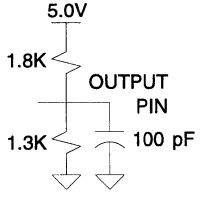
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

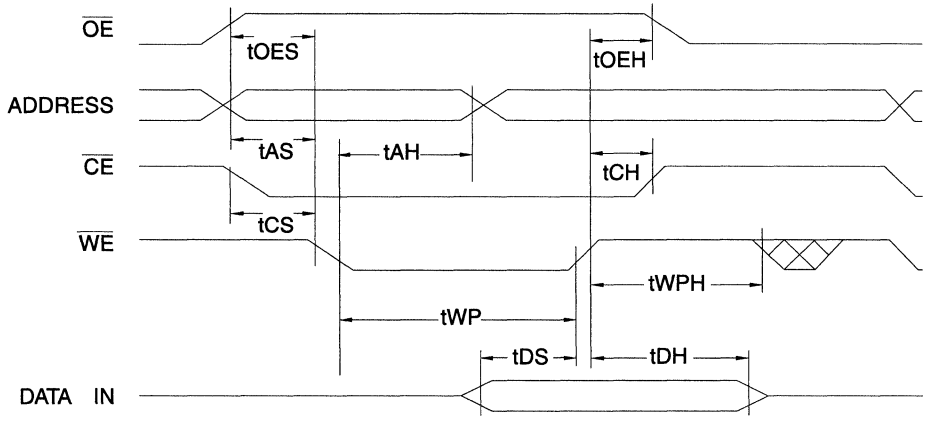
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

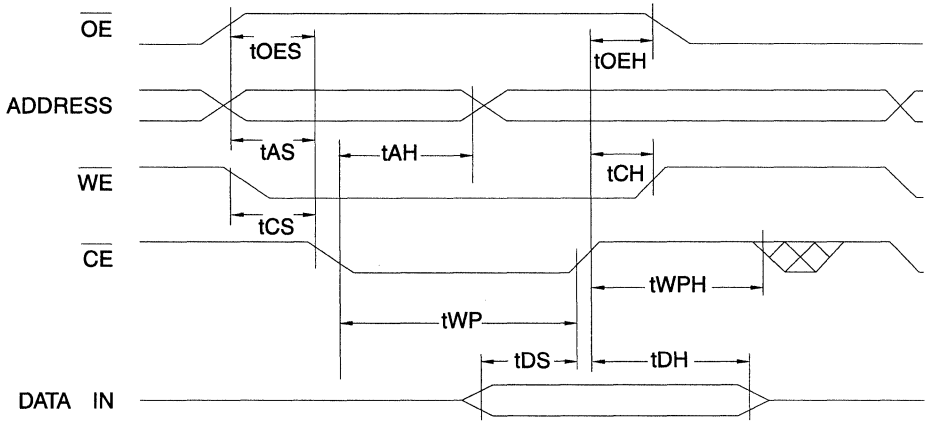
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

AC Byte Load Waveforms

$\overline{WE}$ Controlled



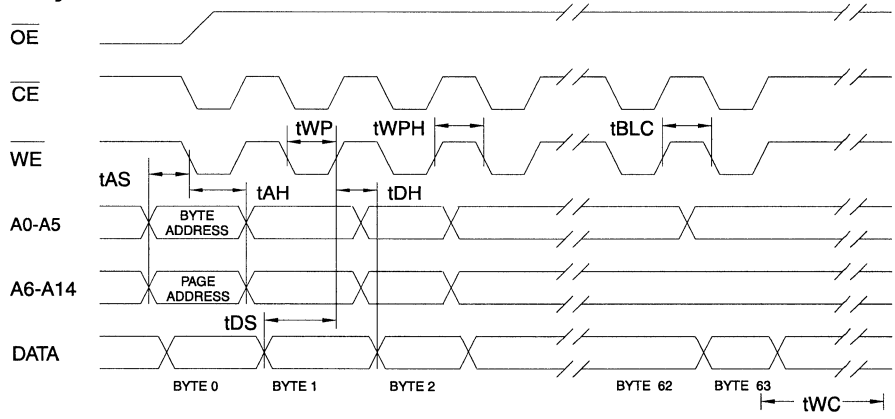
$\overline{CE}$ Controlled



Program Cycle Characteristics

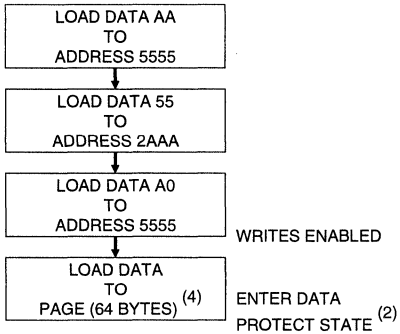
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms (1, 2, 3)



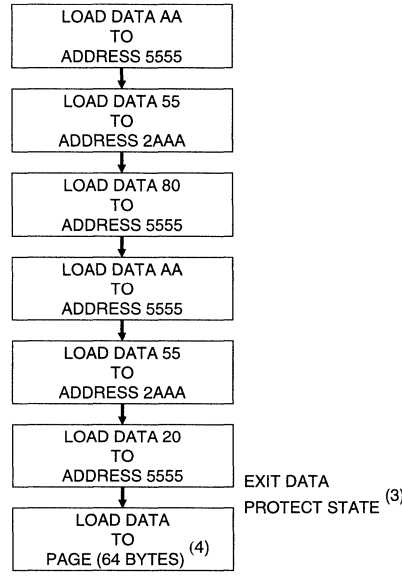
Notes: 1. A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the page being programmed will be indeterminate.**

Software Data Protection Enable Algorithm [1]

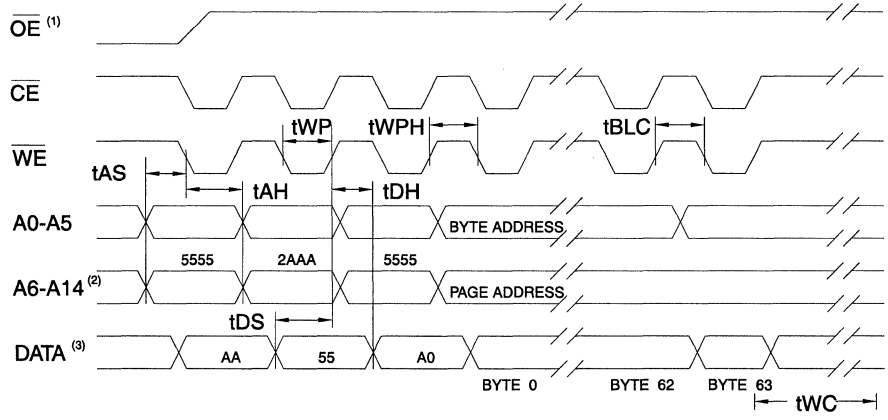


Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64-bytes of data **must be** loaded.

Software Data Protection Disable Algorithm [1]



Software Protected Program Cycle Waveform [1, 2, 3]



Notes: 1. A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.

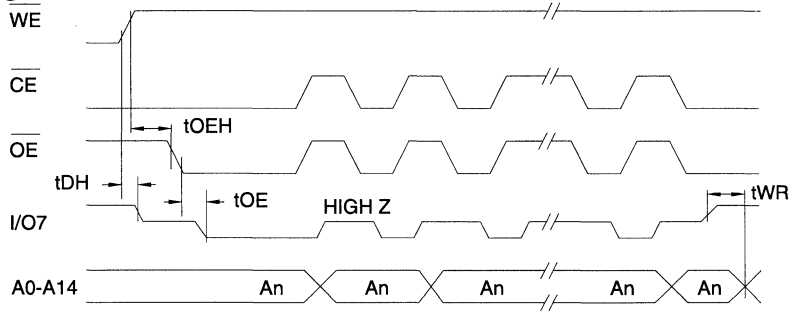
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the page being programmed will be indeterminate.**

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

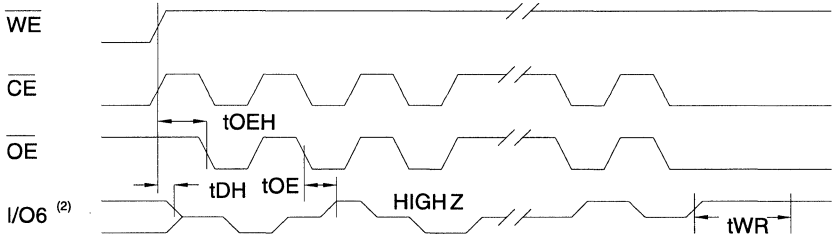


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

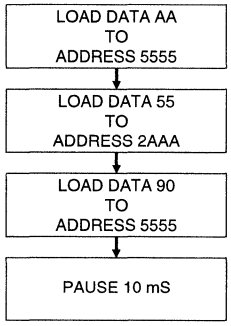
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]



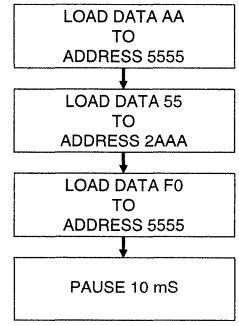
Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



ENTER PRODUCT IDENTIFICATION MODE [2, 3, 5]

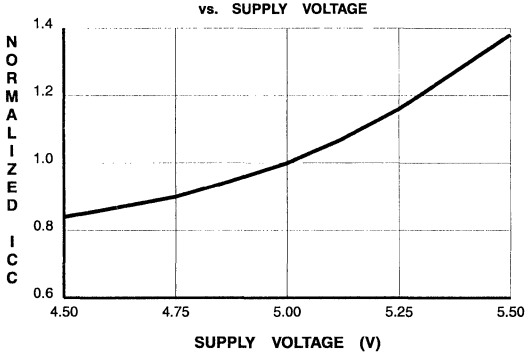
Software Product Identification Exit [1]



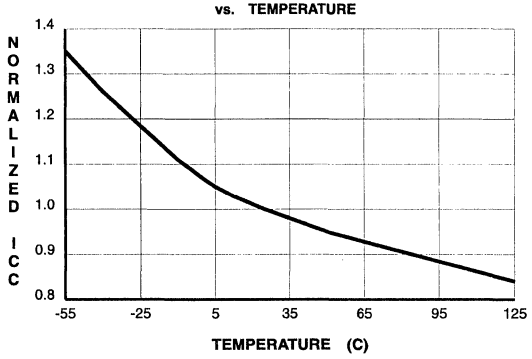
EXIT PRODUCT IDENTIFICATION MODE [4]

Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A14 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: DC

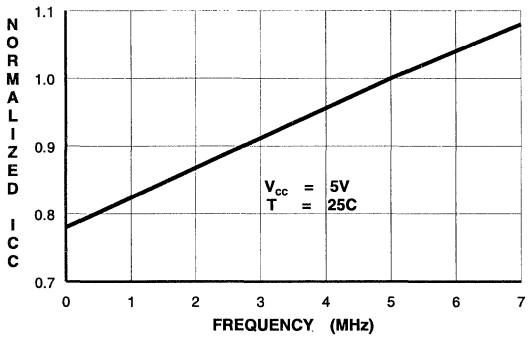
NORMALIZED SUPPLY CURRENT
vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT
vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT
vs. ADDRESS FREQUENCY



4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	0.3	AT29C256-70JC AT29C256-70PC AT29C256-70TC	32J 28P6 28T	Commercial (0° to 70°C)
	50	0.3	AT29C256-70JI AT29C256-70TI	32J 28T	Industrial (-40° to 85°C)
90	50	0.3	AT29C256-90JC AT29C256-90PC AT29C256-90TC	32J 28P6 28T	Commercial (0° to 70°C)
	50	0.3	AT29C256-90JI AT29C256-90PI AT29C256-90TI	32J 28P6 28T	Industrial (-40° to 85°C)
120	50	0.3	AT29C256-12JC AT29C256-12PC AT29C256-12TC	32J 28P6 28T	Commercial (0° to 70°C)
	50	0.3	AT29C256-12JI AT29C256-12PI AT29C256-12TI	32J 28P6 28T	Industrial (-40° to 85°C)
150	50	0.3	AT29C256-15JC AT29C256-15PC AT29C256-15TC	32J 28P6 28T	Commercial (0° to 70°C)
	50	0.3	AT29C256-15JI AT29C256-15PI AT29C256-15TI	32J 28P6 28T	Industrial (-40° to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 70 ns
- 5-Volt-Only Reprogramming
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - Internal Address and Data Latches for 64-Bytes
- Internal Program Control and Timer
- Hardware and Software Data Protection
- Fast Program Cycle Times
  - Page (64-Byte) Program Time - 10 ms
  - Chip Erase Time - 10 ms
- $\overline{\text{DATA}}$ Polling for End of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 300 µA CMOS Standby Current
- Typical Endurance > 10,000 Cycles
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Pin-Compatible with AT29C010A and AT29C512 for Easy System Upgrades

256K (32K x 8) 5-volt Only CMOS Flash Memory

4

Description

The AT29C257 is a 5-volt-only in-system Flash programmable and erasable read only memory (PEROM). Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 70 ns with power dissipation of just 275 mW. When the device is deselected, the CMOS standby current is less than 300 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

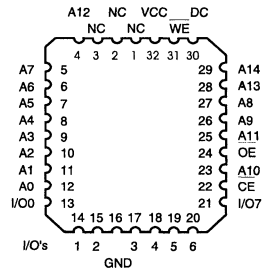
To allow for simple in-system reprogrammability, the AT29C257 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from a static RAM. Reprogramming the AT29C257 is performed on a page basis; 64-bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a 6-byte software code (although erasure before programming is not needed).

During a reprogram cycle, the address locations and 64-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Pin Configurations

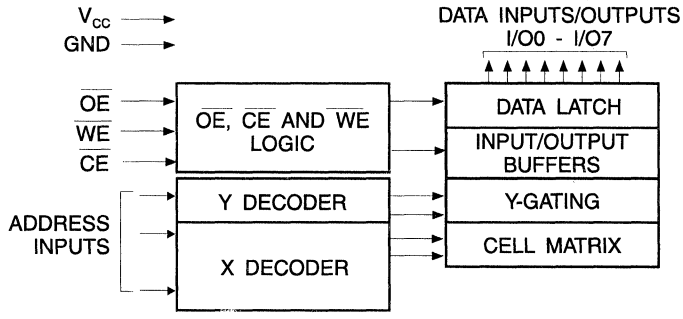
Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PLCC Top View



0012K

Block Diagram



Device Operation

READ: The AT29C257 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Byte loads are used to enter the 64-bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be indeterminate. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C257. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. The 64-bytes of data must be loaded into each sector by the same procedure as outlined in the program section under device operation.

(continued)

Device Operation (Continued)

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C257 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer and may be accessed by a hardware or software operation. For details, see Operating Modes or Software Product Identification.

$\overline{DATA}$ POLLING: The AT29C257 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C257 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT29C257-70	AT29C257-90	AT29C257-12	AT29C257-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Write Inhibit	X	X	V_{IH}		
Write Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
High Voltage Chip Erase	V_{IL}	V_H (3)	V_{IL}	X	High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A14 = V_{IL}, A9 = V_H, A0 = V_{IL}	Manufacturer Code (4)
				A1 - A14 = V_{IL}, A9 = V_H, A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: DC
5. See details under Software Product Identification Entry/Exit.

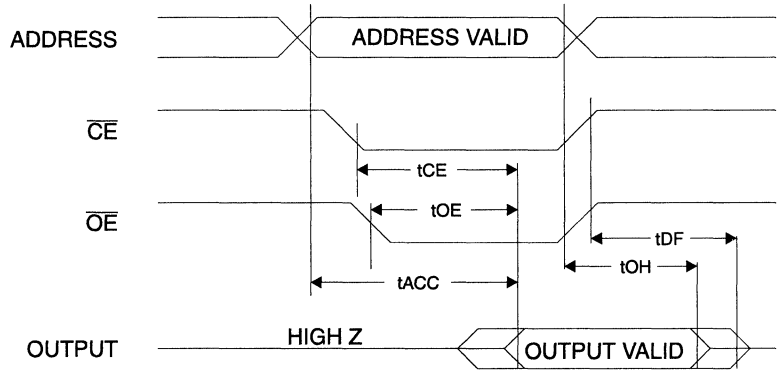
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f= 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

AC Read Characteristics

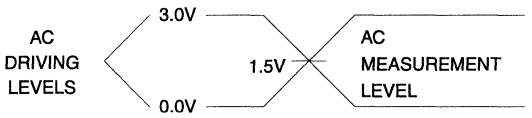
Symbol	Parameter	AT29C257-70		AT29C257-90		AT29C257-12		AT29C257-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90		120		150	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		70		90		120		150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	40	0	50	0	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



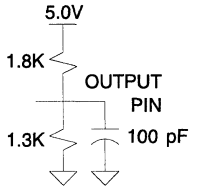
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

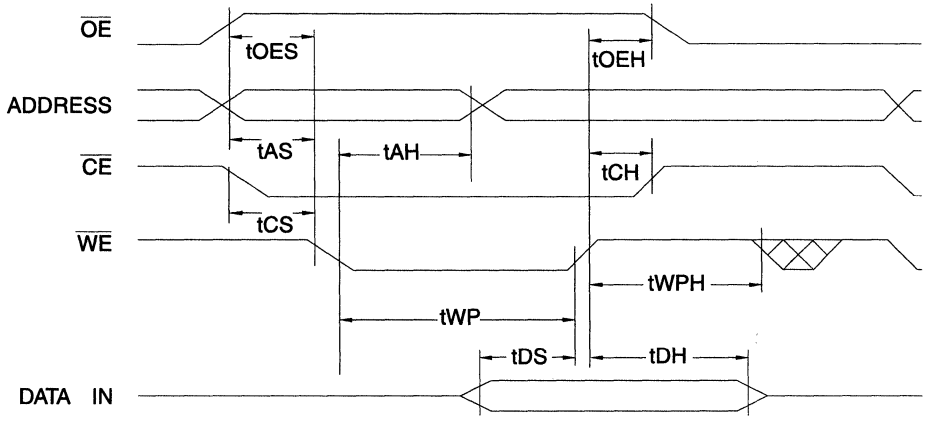
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

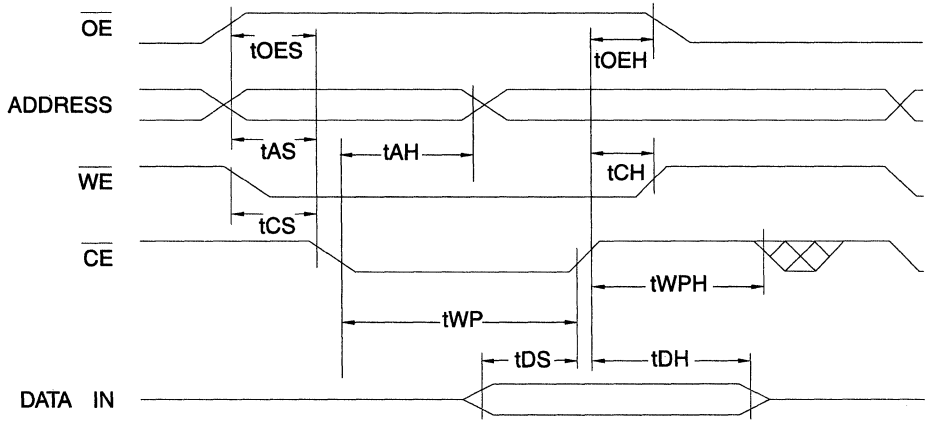
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

AC Byte Load Waveforms

$\overline{WE}$ Controlled



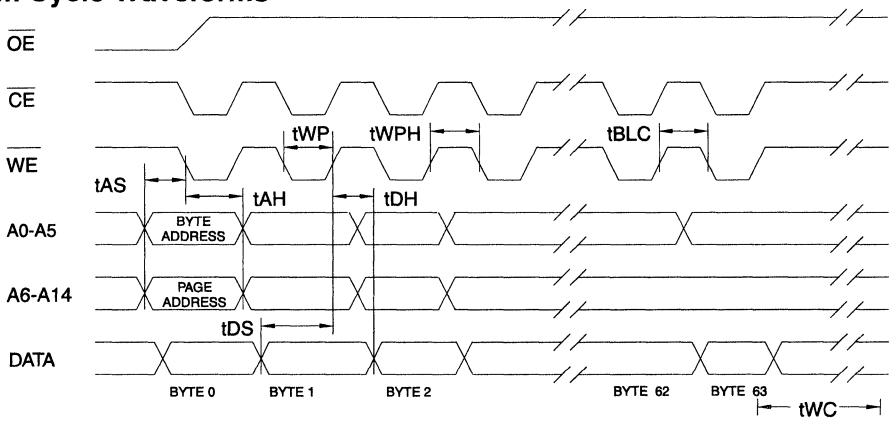
$\overline{CE}$ Controlled



Program Cycle Characteristics

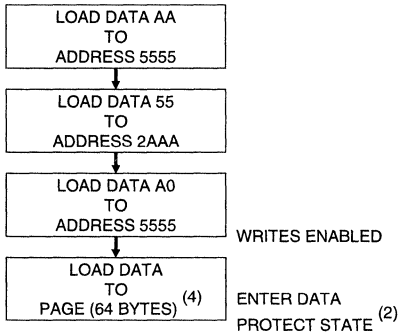
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms (1, 2, 3)



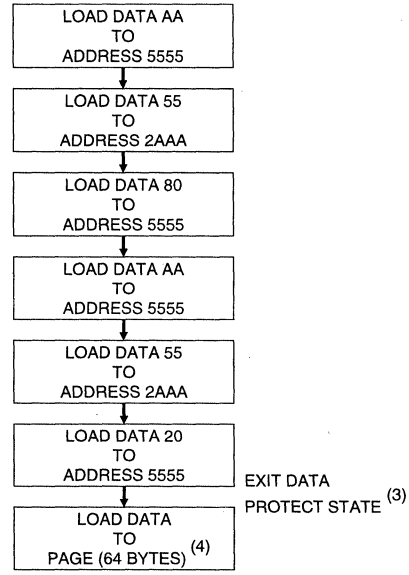
Notes: 1. A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the page being programmed will be indeterminate.**

Software Data Protection Enable Algorithm [1]

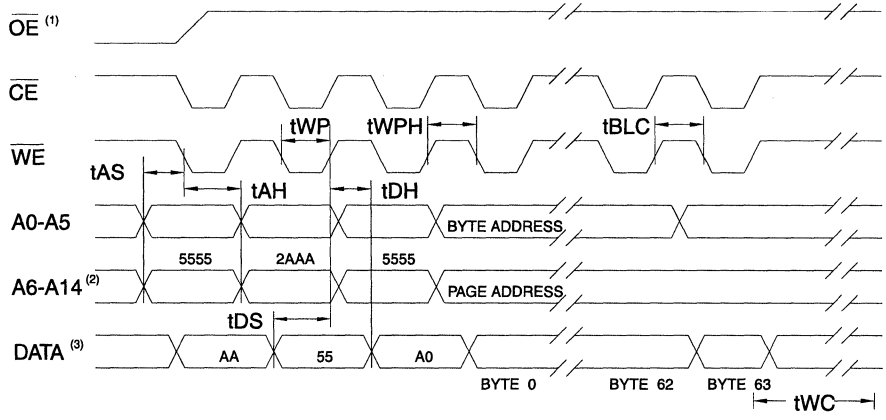


Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64-bytes of data **must be** loaded.

Software Data Protection Disable Algorithm [1]



Software Protected Program Cycle Waveform [1, 2, 3]



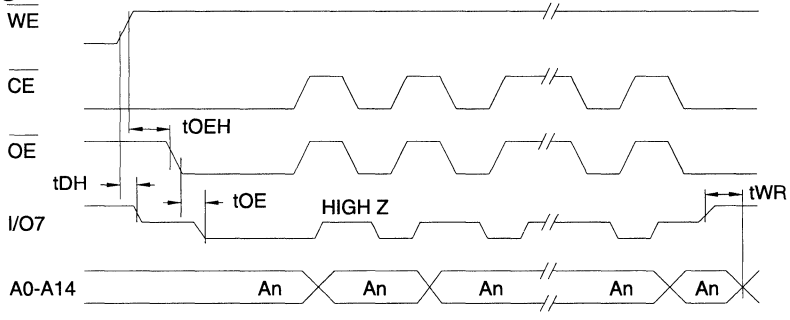
Notes: 1. A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the page being programmed will be indeterminate.**

Data Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Data Polling Waveforms

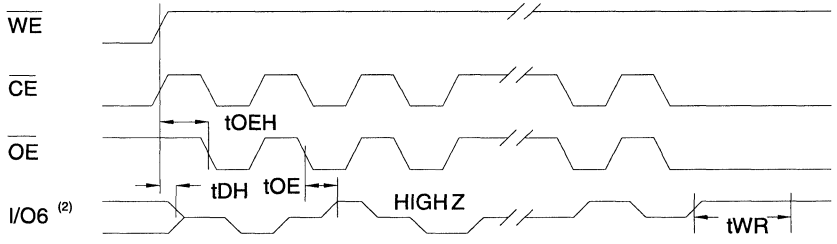


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

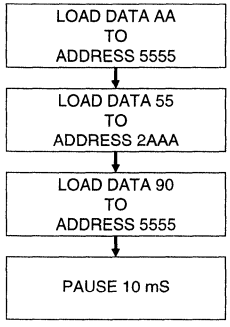
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]



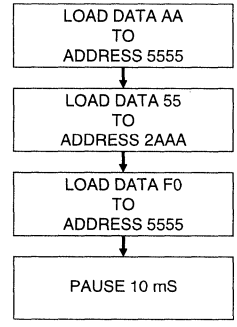
Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



ENTER PRODUCT IDENTIFICATION MODE [2, 3, 5]

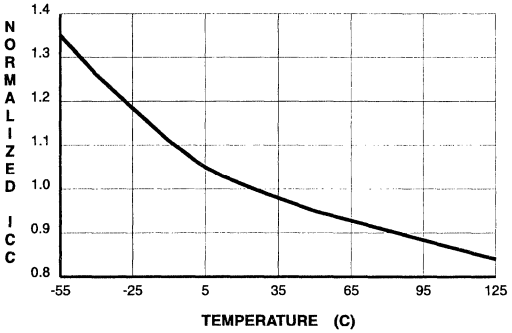
Software Product Identification Exit [1]



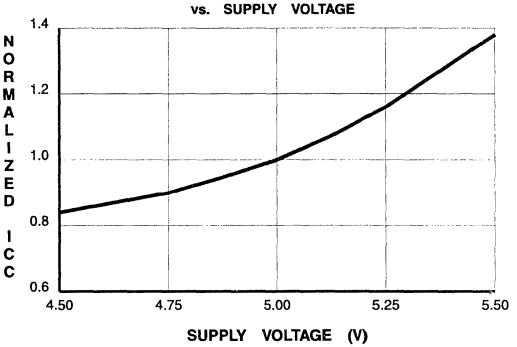
EXIT PRODUCT IDENTIFICATION MODE [4]

Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A14 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: DC

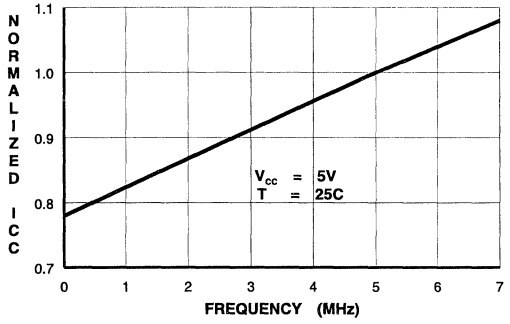
NORMALIZED SUPPLY CURRENT
vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT
vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT
vs. ADDRESS FREQUENCY



4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	0.3	AT29C257-70JC	32J	Commercial (0° to 70°C)
	50	0.3	AT29C257-70JI	32J	Industrial (-40° to 85°C)
90	50	0.3	AT29C257-90JC	32J	Commercial (0° to 70°C)
	50	0.3	AT29C257-90JI	32J	Industrial (-40° to 85°C)
120	50	0.3	AT29C257-12JC	32J	Commercial (0° to 70°C)
	50	0.3	AT29C257-12JI	32J	Industrial (-40° to 85°C)
150	50	0.3	AT29C257-15JC	32J	Commercial (0° to 70°C)
	50	0.3	AT29C257-15JI	32J	Industrial (-40° to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)

512K (64K x 8) 5-volt Only CMOS Flash Memory

Features

- Fast Read Access Time - 70 ns
- 5-Volt-Only Reprogramming
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 512 Sectors (128 bytes/sector)
  - Internal Address and Data Latches for 128-Bytes
- Internal Program Control and Timer
- Hardware and Software Data Protection
- Fast Sector Program Cycle Time - 10 ms
- DATA Polling for End of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 100 µA CMOS Standby Current
- Typical Endurance > 10,000 Cycles
- Single 5V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

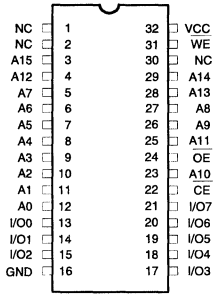
The AT29C512 is a 5-volt-only in-system Flash programmable and erasable read only memory (PEROM). Its 512K of memory is organized as 65,536 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 70 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

(continued)

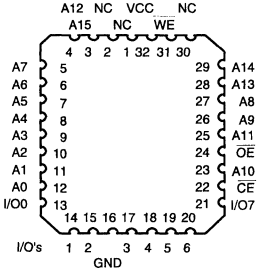
Pin Configurations

Pin Name	Function
A0 - A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

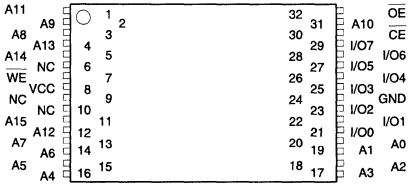
DIP Top View



PLCC Top View



TSOP Top View
Type 1



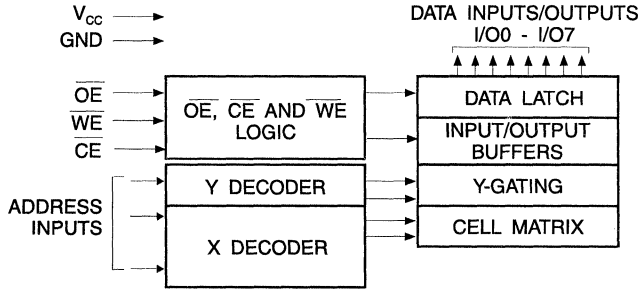
0456B

Description (Continued)

To allow for simple in-system reprogrammability, the AT29C512 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C512 is performed on a sector basis; 128-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29C512 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: Byte loads are used to enter the 128-bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

PROGRAM: The device is reprogrammed on a sector basis. If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be indeterminate. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A15 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C512. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the sector program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

(continued)

Device Operation (Continued)

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. The 128-bytes of data must be loaded into each sector by the same procedure as outlined in the program section under device operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C512 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29C512 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C512 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT29C512-70	AT29C512-90	AT29C512-12	AT29C512-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A15 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
				A1 - A15 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V
4. Manufacturer Code: 1F, Device Code: 5D
5. See details under Software Product Identification Entry/Exit.

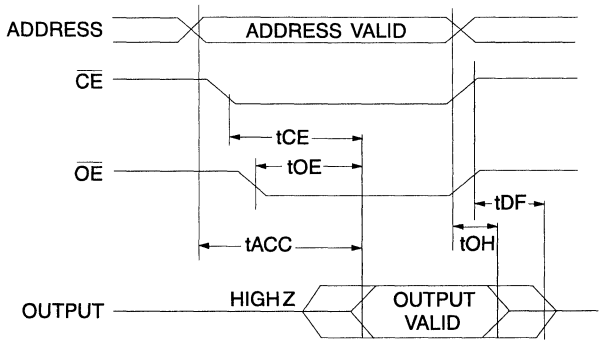
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		100	µA
			Ind.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V		4.2		V

AC Read Characteristics

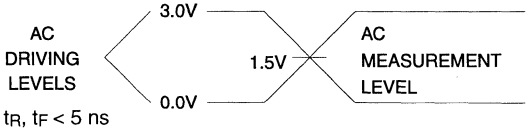
Symbol	Parameter	AT29C512-70		AT29C512-90		AT29C512-12		AT29C512-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90		120		150	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		70		90		120		150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	0	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)

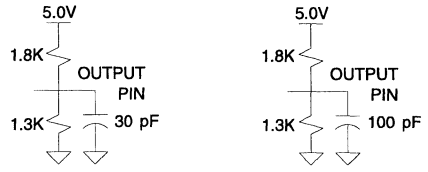


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

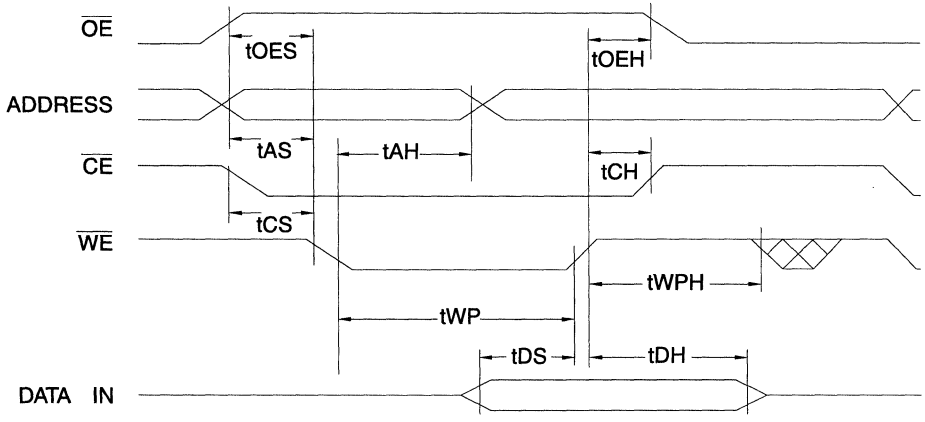
Notes: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

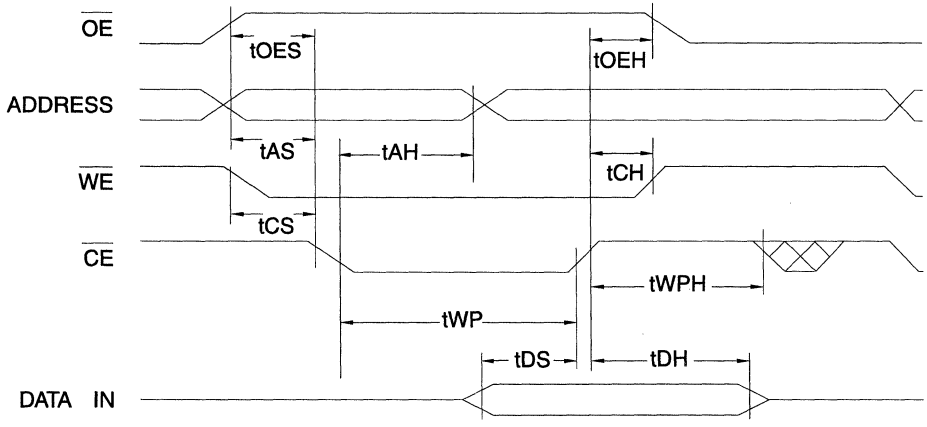
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

AC Byte Load Waveforms

$\overline{WE}$ Controlled



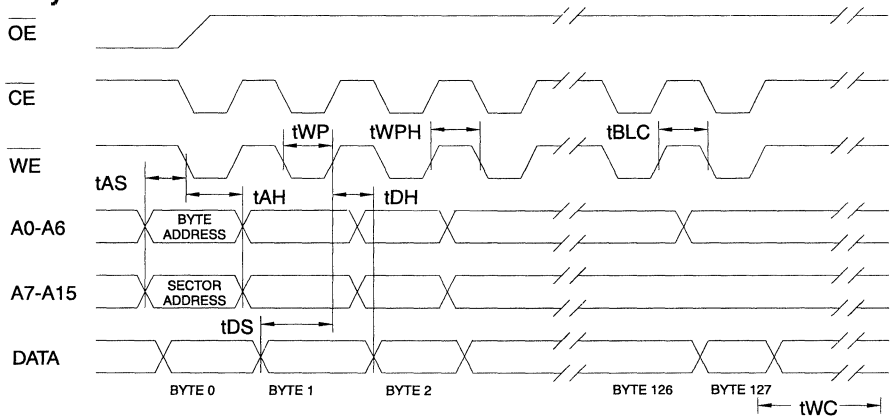
$\overline{CE}$ Controlled



Program Cycle Characteristics

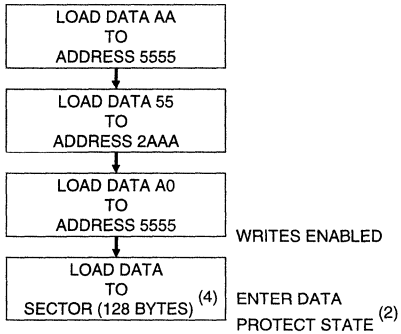
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms (1, 2, 3)



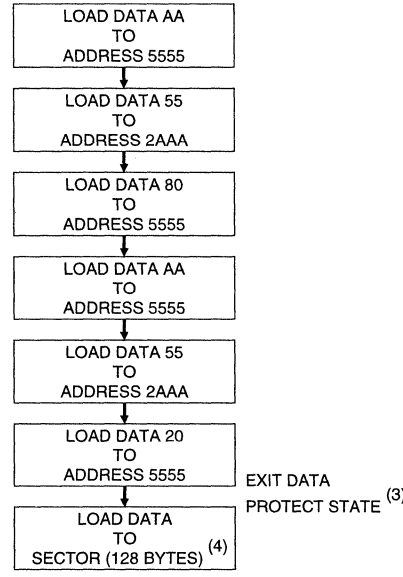
Notes: 1. A7 through A15 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Software Data Protection Enable Algorithm [1]

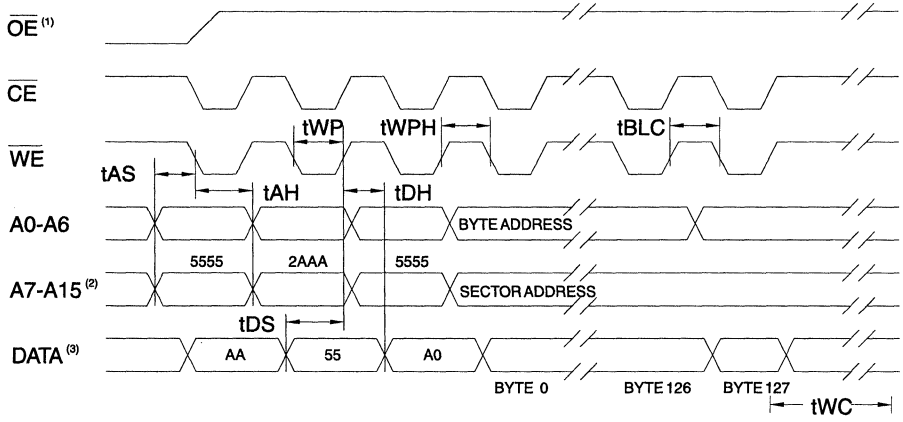


Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 128-bytes of data **MUST BE** loaded.

Software Data Protection Disable Algorithm [1]



Software Protected Program Cycle Waveform [1, 2, 3]



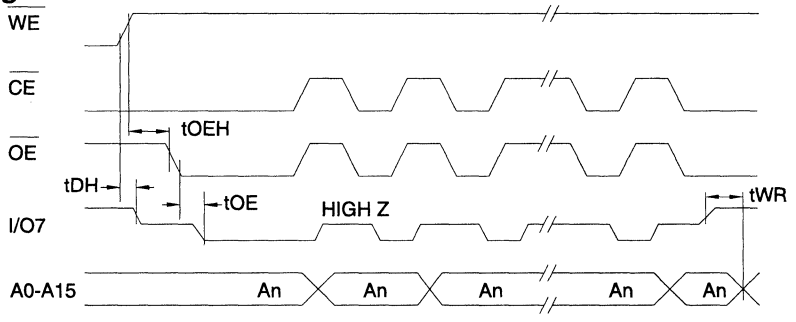
Notes: 1. A7 through A15 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Data Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Data Polling Waveforms

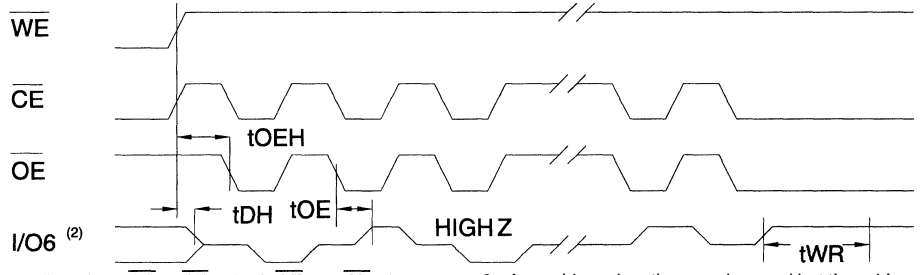


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

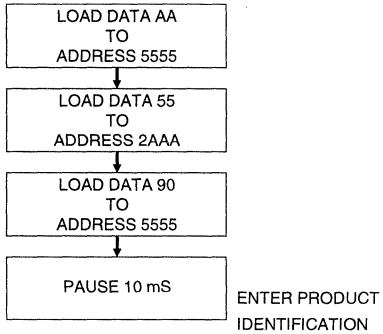
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]

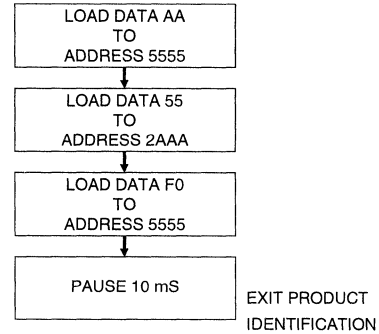


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

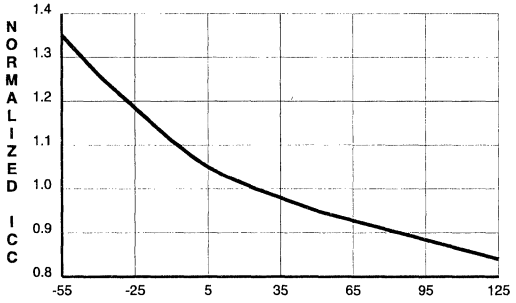


Software Product Identification Exit [1]

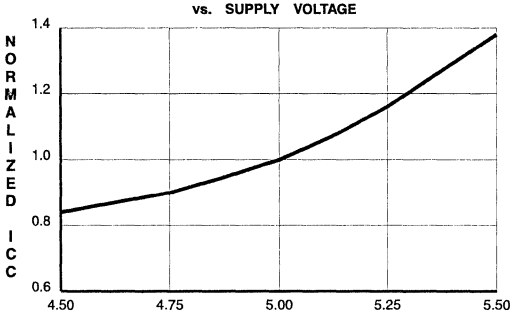


Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A15 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: 5D

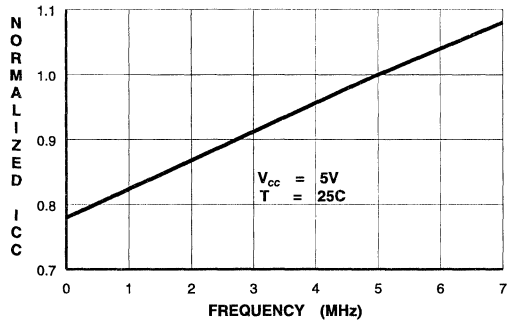
NORMALIZED SUPPLY CURRENT
vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT
vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT
vs. ADDRESS FREQUENCY



4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	0.1	AT29C512-70JC AT29C512-70PC AT29C512-70TC	32J 32P6 32T	Commercial (0° to 70°C)
90	50	0.1	AT29C512-90JC AT29C512-90PC AT29C512-90TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT29C512-90JI AT29C512-90PI AT29C512-90TI	32J 32P6 32T	Industrial (-40° to 85°C)
120	50	0.1	AT29C512-12JC AT29C512-12PC AT29C512-12TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT29C512-12JI AT29C512-12PI AT29C512-12TI	32J 32P6 32T	Industrial (-40° to 85°C)
150	50	0.1	AT29C512-15JC AT29C512-15PC AT29C512-15TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT29C512-15JI AT29C512-15PI AT29C512-15TI	32J 32P6 32T	Industrial (-40° to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

1 Megabit (128K x 8) 5-volt Only CMOS Flash Memory

Features

- Fast Read Access Time - 70 ns
- 5-Volt-Only Reprogramming
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Sectors (128 bytes/sector)
  - Internal Address and Data Latches for 128-Bytes
- Two 8 KB Boot Blocks with Lockout
- Internal Program Control and Timer
- Hardware and Software Data Protection
- Fast Sector Program Cycle Time - 10 ms
- DATA Polling for End of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 100 µA CMOS Standby Current
- Typical Endurance > 10,000 Cycles
- Single 5V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

Description

The AT29C010A is a 5-volt-only in-system Flash programmable and erasable read only memory (PEROM). Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 70 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

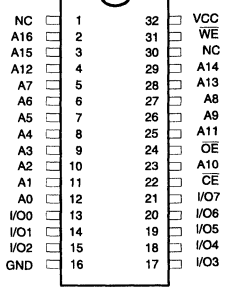
To allow for simple in-system reprogrammability, the AT29C010A does not require high input voltages for programming. Five-volt-only commands determine the opera-

(continued)

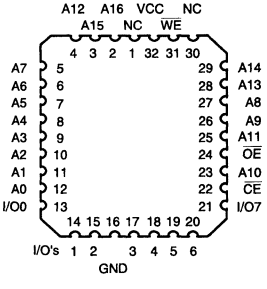
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View

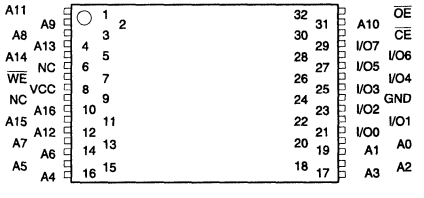


PLCC Top View



TSOP Top View

Type 1



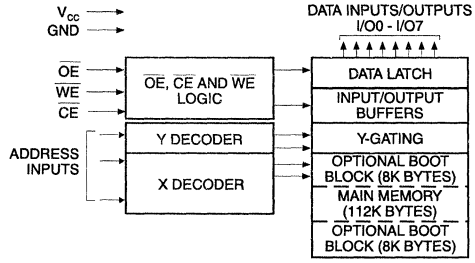
0394B

Description (Continued)

tion of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C010A is performed on a sector basis; 128-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29C010A is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: Byte loads are used to enter the 128-bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

PROGRAM: The device is reprogrammed on a sector basis. If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. The data in any byte that is not loaded during the programming of its sector will be indeterminate. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C010A. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the sector program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

(continued)

Device Operation (Continued)

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. The 128-bytes of data must be loaded into each sector by the same procedure as outlined in the program section under device operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C010A in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29C010A features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. DATA polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C010A provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

BOOT BLOCK PROGRAMMING LOCKOUT: The AT29C010A has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 8K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 8K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29C010A blocks are located in the first 8K bytes of memory and the last 8K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

(continued)

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation (Continued)

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine whether programming of either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002 will show if programming the lower address boot block is locked out while reading location FFFF2 will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

DC and AC Operating Range

		AT29C010A-70	AT29C010A-90	AT29C010A-12	AT29C010A-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A16 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
				A1 - A16 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: D5
5. See details under Software Product Identification Entry/Exit.

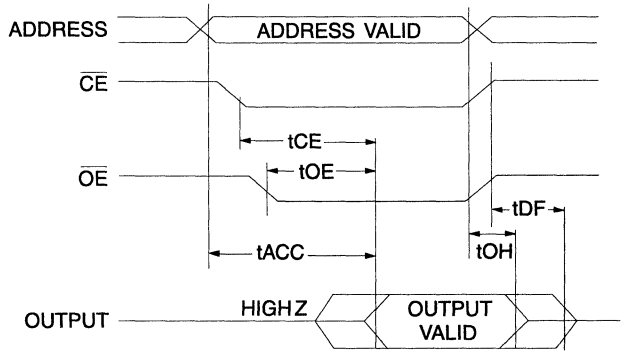
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		100	µA
			Ind.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V		4.2		V

AC Read Characteristics

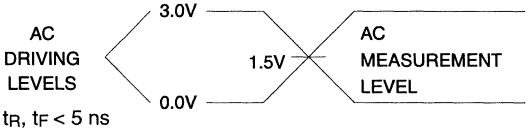
Symbol	Parameter	AT29C010A-70 Min	AT29C010A-70 Max	AT29C010A-90 Min	AT29C010A-90 Max	AT29C010A-12 Min	AT29C010A-12 Max	AT29C010A-15 Min	AT29C010A-15 Max	Units
t_{ACC}	Address to Output Delay		70		90		120		150	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		70		90		120		150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	0	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)

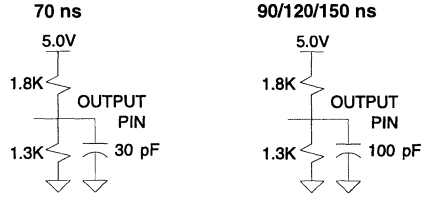


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

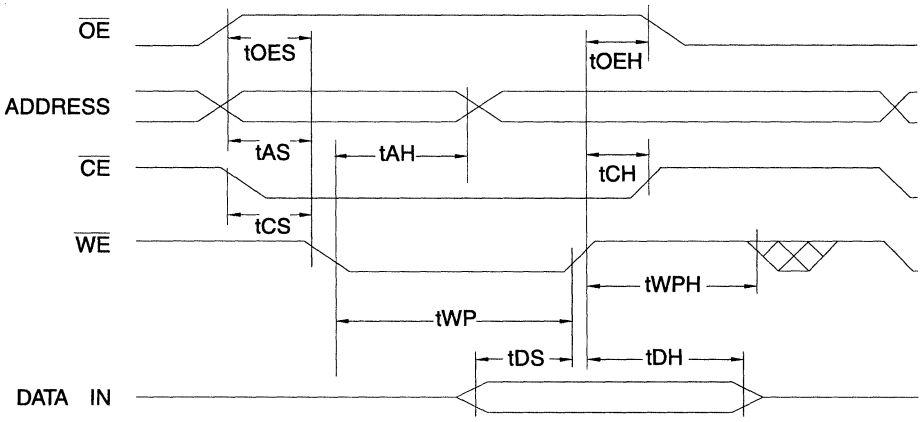
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

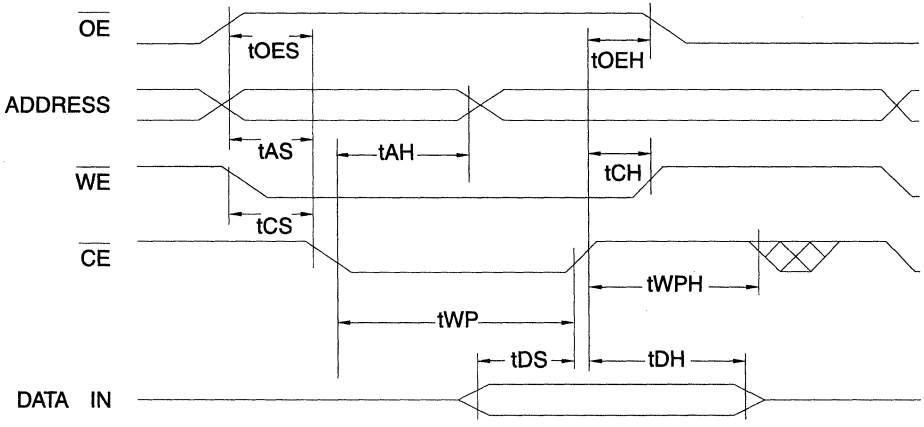
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

AC Byte Load Waveforms

$\overline{WE}$ Controlled



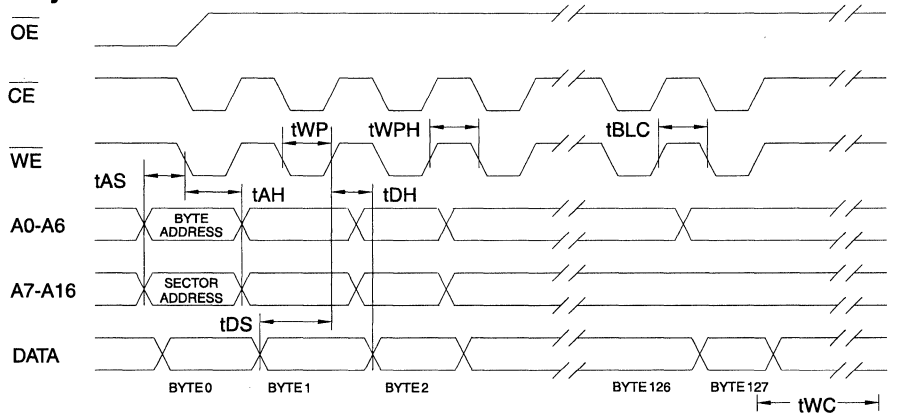
$\overline{CE}$ Controlled



Program Cycle Characteristics

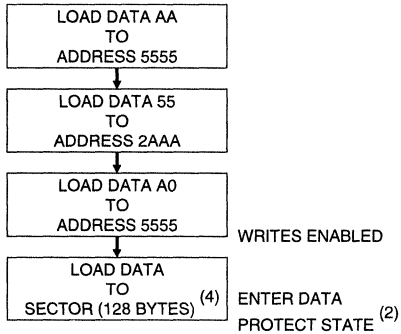
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms [1, 2, 3]



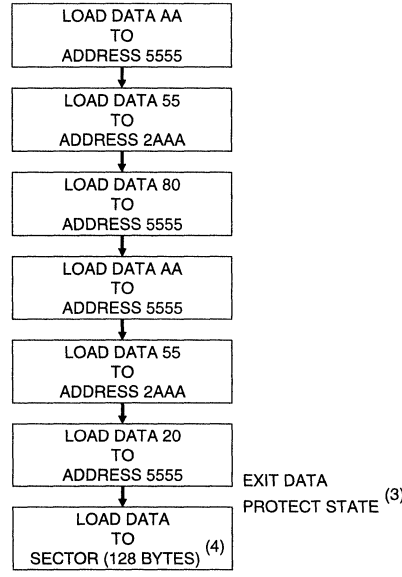
Notes: 1. A7 through A16 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Software Data Protection Enable Algorithm [1]

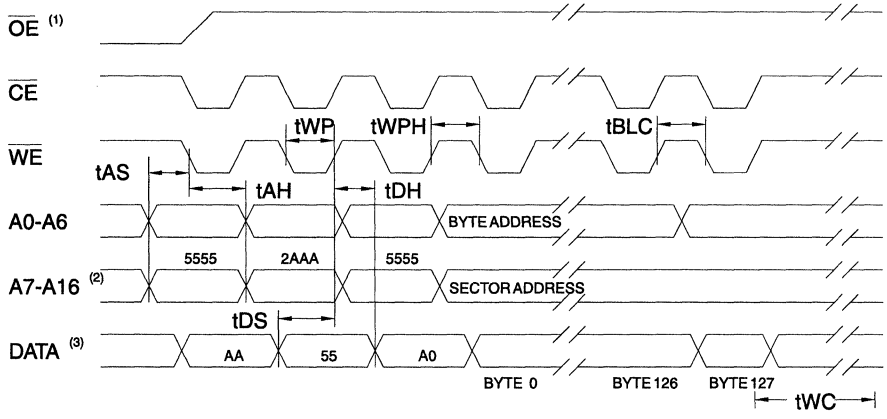


Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 128-bytes of data **MUST BE** loaded.

Software Data Protection Disable Algorithm [1]



Software Protected Program Cycle Waveform [1, 2, 3]



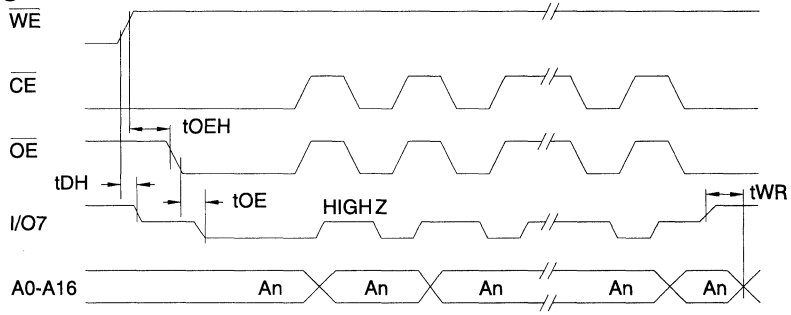
Notes: 1. A7 through A16 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

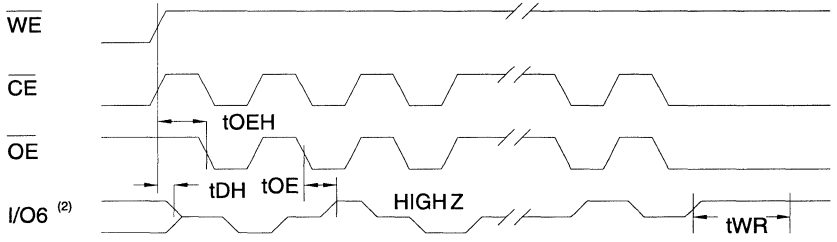


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

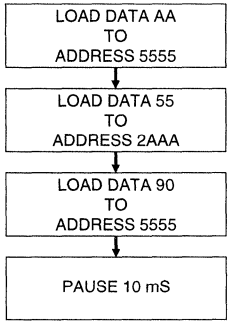
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]



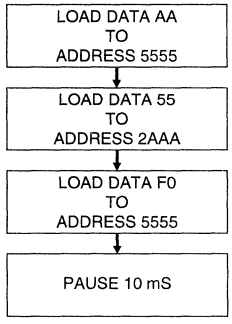
Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



ENTER PRODUCT IDENTIFICATION MODE [2, 3, 5]

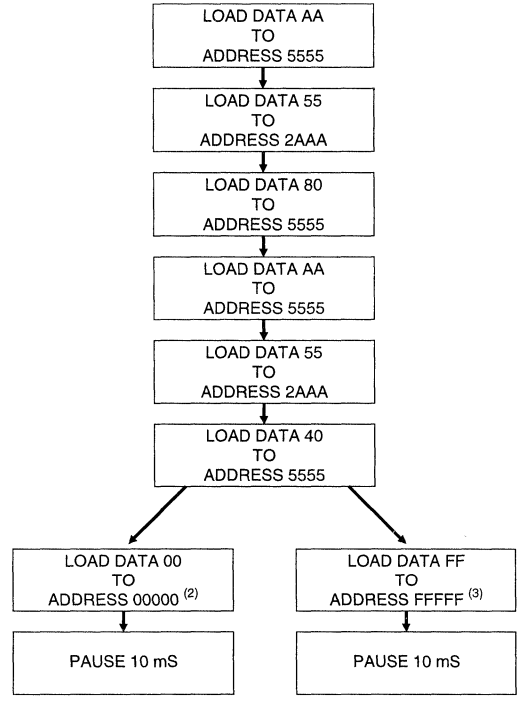
Software Product Identification Exit [1]



EXIT PRODUCT IDENTIFICATION MODE [4]

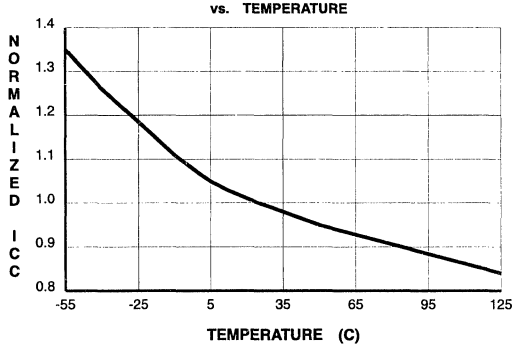
Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A16 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: D5

Boot Block Lockout Feature Enable Algorithm [1]

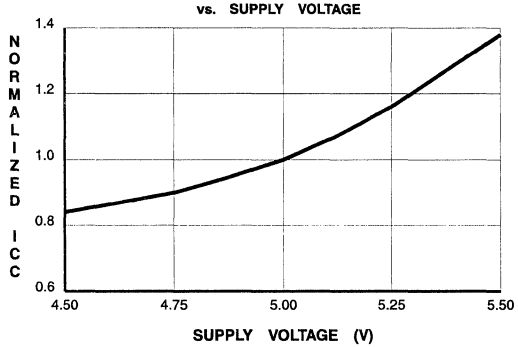


Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Lockout feature set on lower address boot block.
3. Lockout feature set on higher address boot block.

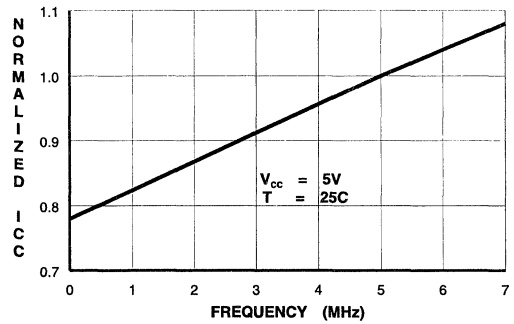
NORMALIZED SUPPLY CURRENT
vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT
vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT
vs. ADDRESS FREQUENCY



4

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	0.1	AT29C010A-70JC AT29C010A-70PC AT29C010A-70TC	32J 32P6 32T	Commercial (0° to 70°C)
90	50	0.1	AT29C010A-90JC AT29C010A-90PC AT29C010A-90TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT29C010A-90JI AT29C010A-90PI AT29C010A-90TI	32J 32P6 32T	Industrial (-40° to 85°C)
120	50	0.1	AT29C010A-12JC AT29C010A-12PC AT29C010A-12TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT29C010A-12JI AT29C010A-12PI AT29C010A-12TI	32J 32P6 32T	Industrial (-40° to 85°C)
150	50	0.1	AT29C010A-15JC AT29C010A-15PC AT29C010A-15TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT29C010A-15JI AT29C010A-15PI AT29C010A-15TI	32J 32P6 32T	Industrial (-40° to 85°C)

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 70 ns
- 5-Volt-Only Reprogramming
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 512 Sectors (128 words/sector)
  - Internal Address and Data Latches for 128 Words
- Internal Program Control and Timer
- Hardware and Software Data Protection
- Fast Sector Program Cycle Time - 10 ms
- DATA Polling for End of Program Detection
- Low Power Dissipation
  - 60 mA Active Current
  - 200 µA CMOS Standby Current
- Typical Endurance > 10,000 Cycles
- Single 5V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

1 Megabit (64K x 16) 5-volt Only CMOS Flash Memory

4

Description

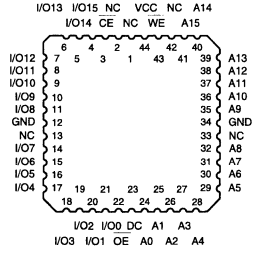
The AT29C1024 is a 5-volt-only in-system Flash programmable and erasable read only memory (PEROM). Its 1 megabit of memory is organized as 65,536 words by 16 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 70 ns with power dissipation of just 330 mW. When the device is deselected, the CMOS standby current is less than 200 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

(continued)

Pin Configurations

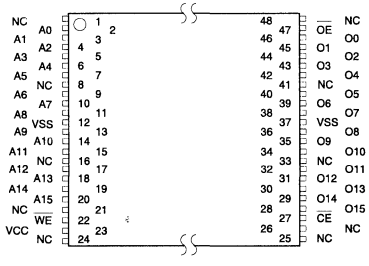
Pin Name	Function
A0 - A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PLCC Top View



TSOP Top View

Type 1



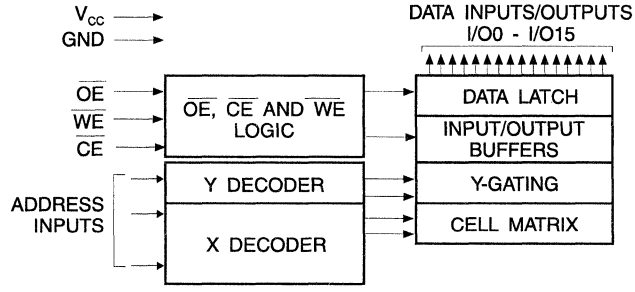
0571A

Description (Continued)

To allow for simple in-system reprogrammability, the AT29C1024 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C1024 is performed on a sector basis; 128 words of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128 words of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7 or I/O15. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29C1024 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

DATA LOAD: Data loads are used to enter the 128 words of a sector to be programmed or the software codes for data protection. A data load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

PROGRAM: The device is reprogrammed on a sector basis. If a word of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any word that is not loaded during the programming of its sector will be erased to read FFH. Once the words of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data word has been loaded into the device, successive words are entered in the same manner. Each new word to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding word. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A15 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the word address within the sector. The words may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C1024. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the sector program timing specifications. Once set, software data protection will remain active unless the disable command sequence is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

(continued)

Device Operation (Continued)

After setting SDP, any attempt to write to the device without the 3-word command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-word command code is given, a sector of data is loaded into the device using the sector programming timing specifications.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C1024 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for various Flash densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{\text{DATA}}$ POLLING: The AT29C1024 features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last word loaded will result in the complement of the loaded data on I/O7 and I/O15. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT29C1024 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 and I/O14 toggling between one and zero. Once the program cycle has completed, I/O6 and I/O14 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

4

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT29C1024-70	AT29C1024-90	AT29C1024-12	AT29C1024-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A15 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
				A1 - A15 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: 25
5. See details under Software Product Identification Entry/Exit.

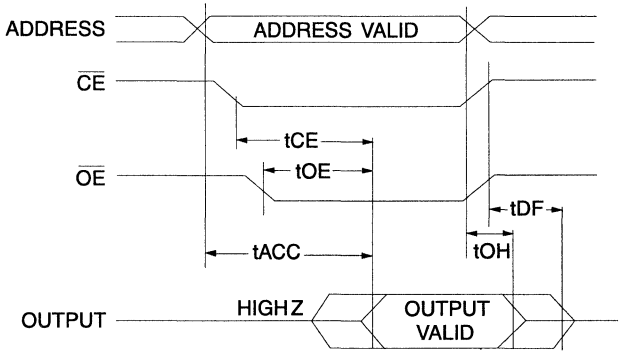
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		200	µA
			Ind.		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			60	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V		4.2		V

AC Read Characteristics

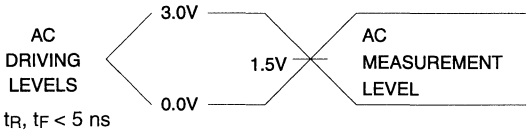
Symbol	Parameter	AT29C1024-70		AT29C1024-90		AT29C1024-12		AT29C1024-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90		120		150	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		70		90		120		150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	35	0	45	0	60	0	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



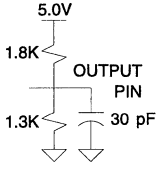
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level

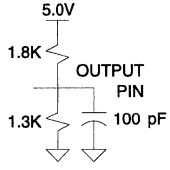


Output Test Load

70 ns



90/120/150 ns



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

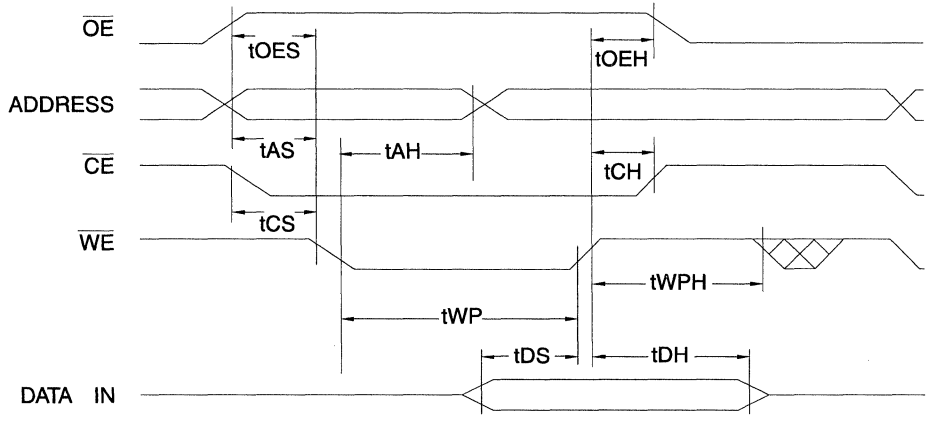
Note: 1. This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

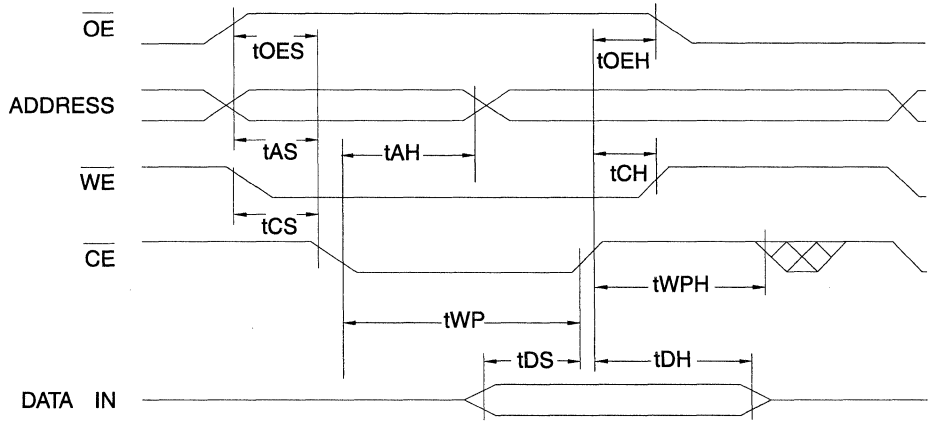
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	70		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



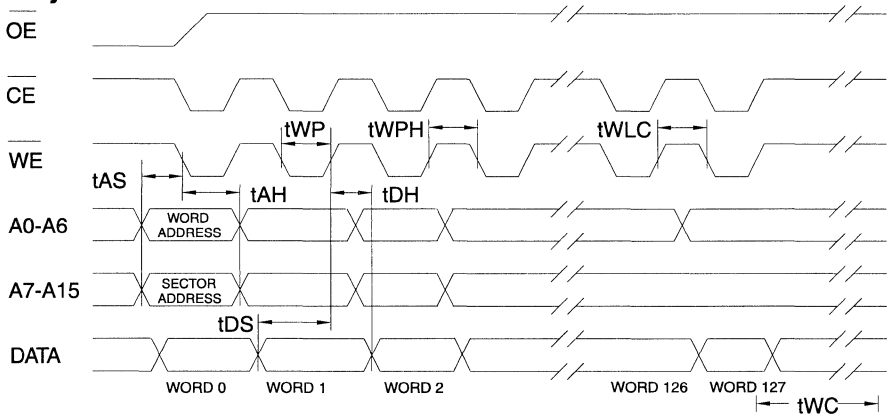
$\overline{CE}$ Controlled



Program Cycle Characteristics

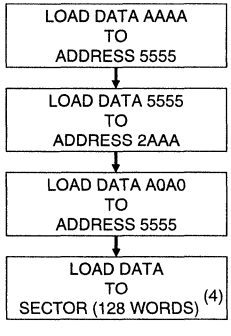
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	70		ns
t_{WLC}	Word Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms (1, 2, 3)



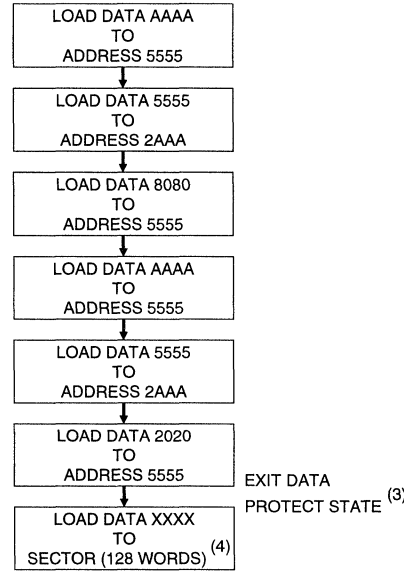
Notes: 1. A7 through A15 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All words that are not loaded within the sector being programmed will be indeterminate.**

Software Data Protection Enable Algorithm [1]

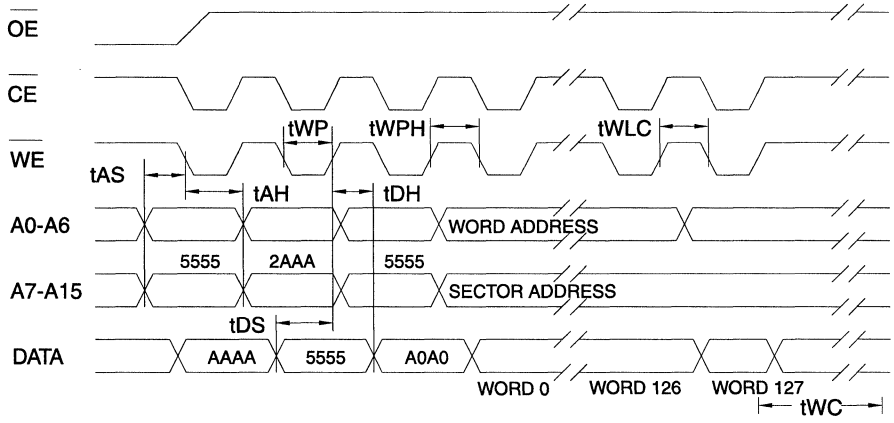


Notes for software program code:
1. Data Format: I/O15 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write period even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 128 words of data **MUST BE** loaded.

Software Data Protection Disable Algorithm [1]



Software Protected Program Cycle Waveform [1, 2, 3]



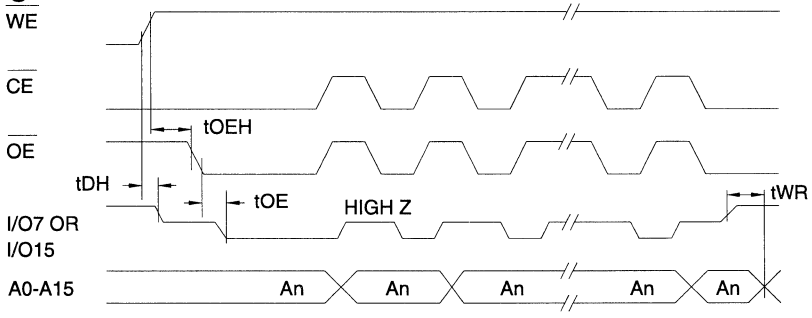
Notes: 1. A7 through A15 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All words that are not loaded within the sector being programmed will be indeterminate.**

Data Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Data Polling Waveforms

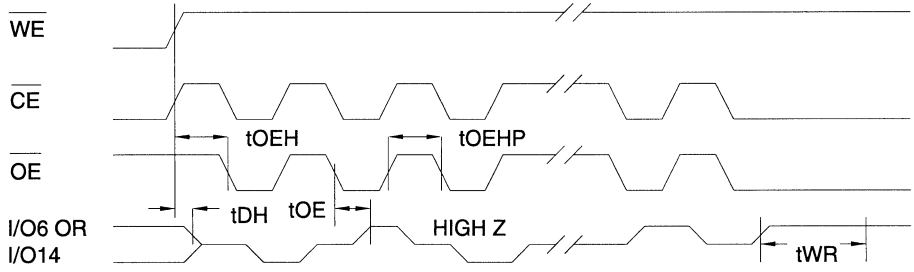


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

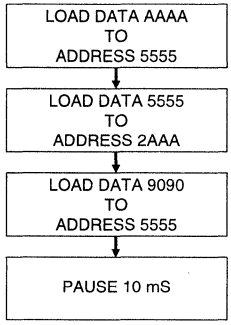
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]



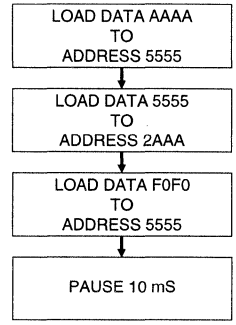
Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 and I/O14 may vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



ENTER PRODUCT IDENTIFICATION MODE [2, 3, 5]

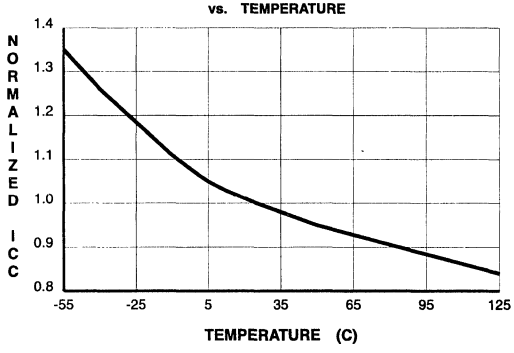
Software Product Identification Exit [1]



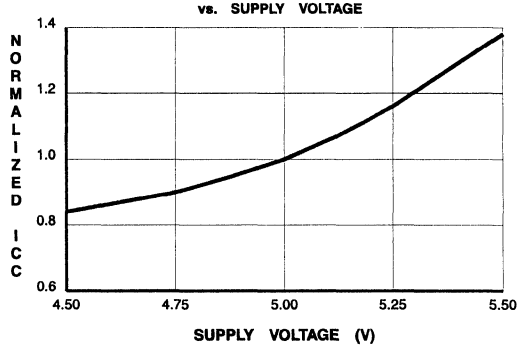
EXIT PRODUCT IDENTIFICATION MODE [4]

Notes for software product identification:
1. Data Format: I/O15 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A15 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: 25

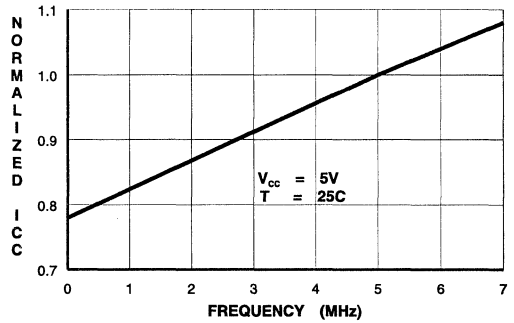
NORMALIZED SUPPLY CURRENT
vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT
vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT
vs. ADDRESS FREQUENCY



4

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	60	0.1	AT29C1024-70JC AT29C1024-70TC	44J 48T	Commercial (0° to 70°C)
	60	0.3	AT29C1024-70JI AT29C1024-70TI	44J 48T	Industrial (-40° to 85°C)
90	60	0.1	AT29C1024-90JC AT29C1024-90TC	44J 48T	Commercial (0° to 70°C)
	60	0.3	AT29C1024-90JI AT29C1024-90TI	44J 48T	Industrial (-40° to 85°C)
120	60	0.1	AT29C1024-12JC AT29C1024-12TC	44J 48T	Commercial (0° to 70°C)
	60	0.3	AT29C1024-12JI AT29C1024-12TI	44J 48T	Industrial (-40° to 85°C)
150	60	0.1	AT29C1024-15JC AT29C1024-15TC	44J 48T	Commercial (0° to 70°C)
	60	0.3	AT29C1024-15JI AT29C1024-15TI	44J 48T	Industrial (-40° to 85°C)

Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
48T	48 Lead, Thin Small Outline Package (TSOP)

Features

- Fast Read Access Time - 90 ns
- 5-Volt-Only Reprogramming
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 1024 Sectors (256 bytes/sector)
  - Internal Address and Data Latches for 256-Bytes
- Internal Program Control and Timer
- Hardware and Software Data Protection
- Two 8 KB Boot Blocks with Lockout
- Fast Sector Program Cycle Time - 10 ms
- DATA Polling for End of Program Detection
- Low Power Dissipation
  - 40 mA Active Current
  - 100 µA CMOS Standby Current
- Typical Endurance > 10,000 Cycles
- Single 5V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

2 Megabit (256K x 8) 5-volt Only CMOS Flash Memory

4

Description

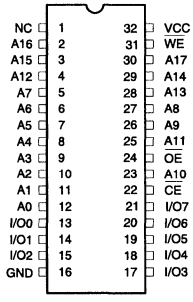
The AT29C020 is a 5-volt-only in-system Flash programmable and erasable read only memory (PEROM). Its 2 megabits of memory is organized as 262,144 bytes. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 220 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA. Device endurance is such that any sector can typically be written to in excess of 10,000 times.

(continued)

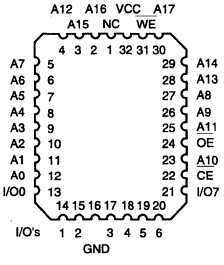
Pin Configurations

Pin Name	Function
A0 - A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

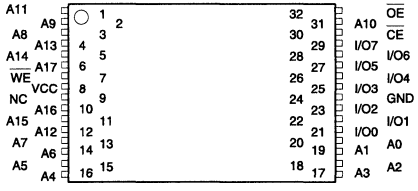
DIP Top View



PLCC Top View



TSOP Top View
Type 1



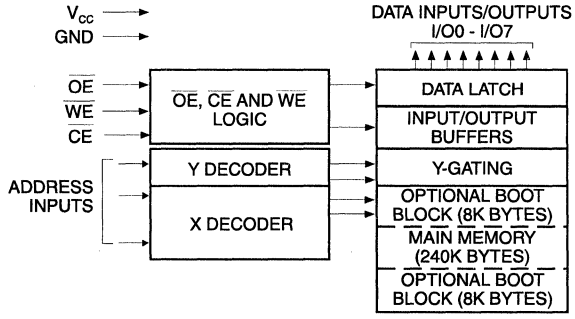
0291H

Description (Continued)

To allow for simple in-system reprogrammability, the AT29C020 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C020 is performed on a sector basis; 256-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 256-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29C020 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: Byte loads are used to enter the 256-bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

PROGRAM: The device is reprogrammed on a sector basis. If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be indeterminate. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A8 to A17 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A7 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C020. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the sector program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal

(continued)

Device Operation (Continued)

write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a sector of data is loaded into the device using the sector program timing specifications.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C020 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29C020 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C020 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

BOOT BLOCK PROGRAMMING LOCKOUT: The AT29C020 has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 8K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 8K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29C020 blocks are located in the first 8K bytes of memory and the last 8K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine whether programming of

(continued)

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation (Continued)

either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002H will show if programming the lower address boot block is locked out while reading location FFFF2H will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

DC and AC Operating Range

		AT29C020-90	AT29C020-10	AT29C020-12	AT29C020-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A17 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
				A1 - A17 = V_{IL}, A9 = V_H, A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: DA
5. See details under Software Product Identification Entry/Exit.

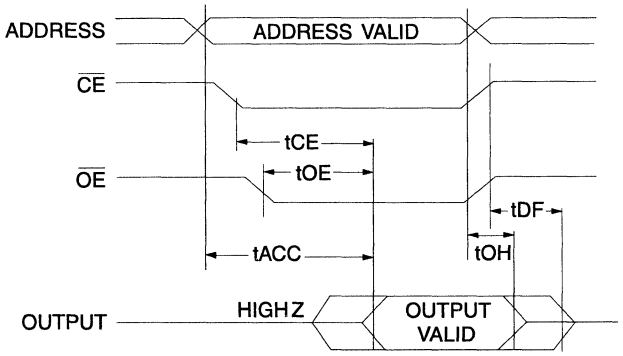
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		100	µA
			Ind.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			40	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V		4.2		V

AC Read Characteristics

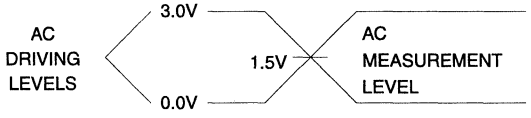
Symbol	Parameter	AT29C020-90		AT29C020-10		AT29C020-12		AT29C020-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	0	90		100		120		150	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		100		120		150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	0	50	0	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



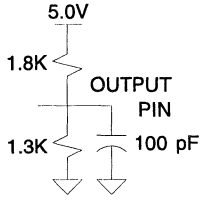
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

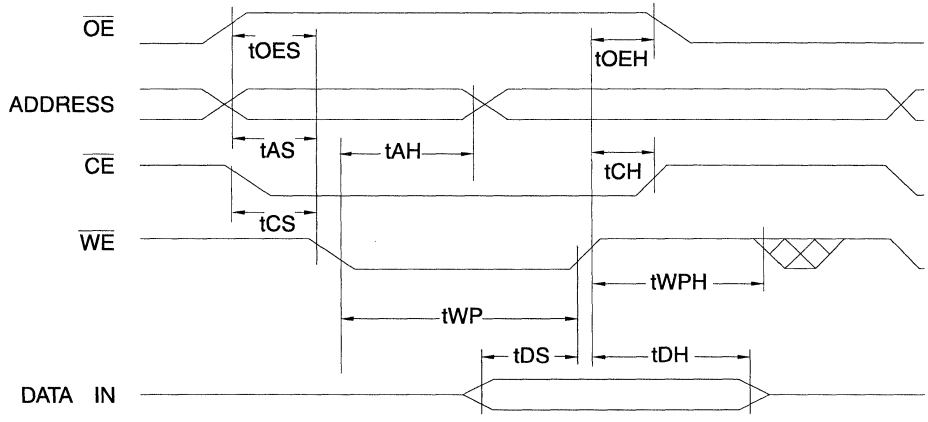
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

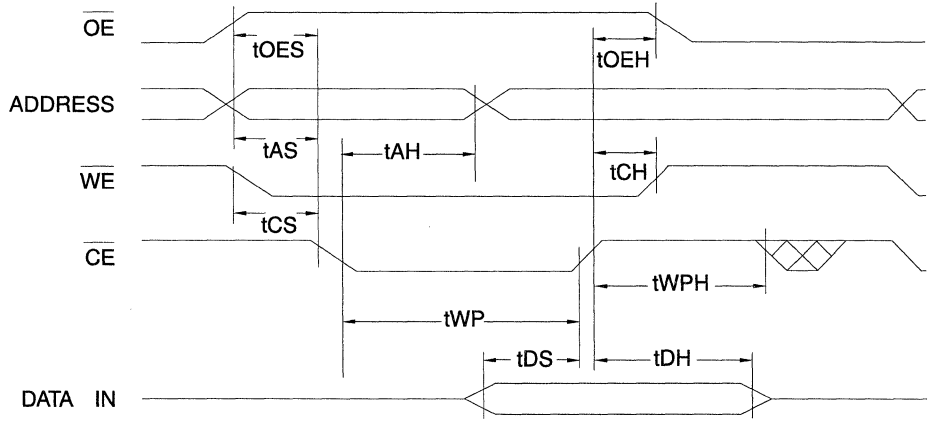
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

AC Byte Load Waveforms

$\overline{WE}$ Controlled



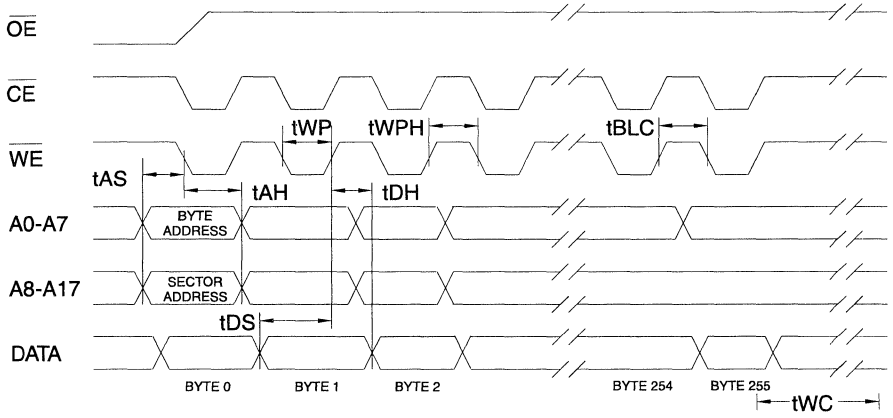
$\overline{CE}$ Controlled



Program Cycle Characteristics

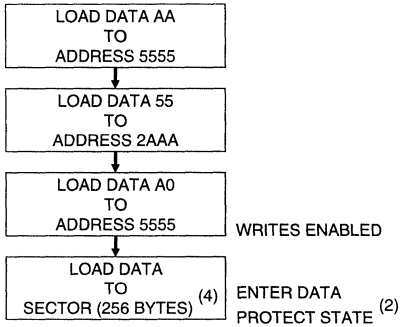
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms (1, 2, 3)



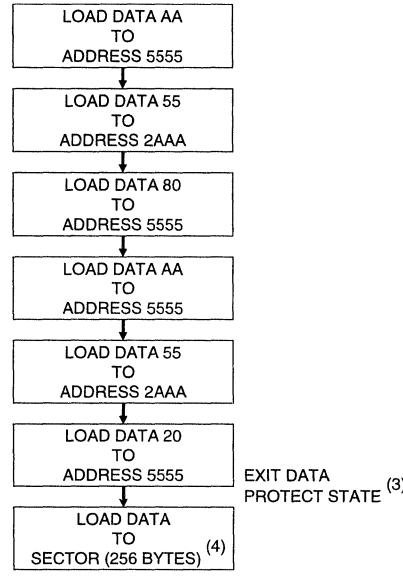
Notes: 1. A8 through A17 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Software Data Protection Enable Algorithm [1]

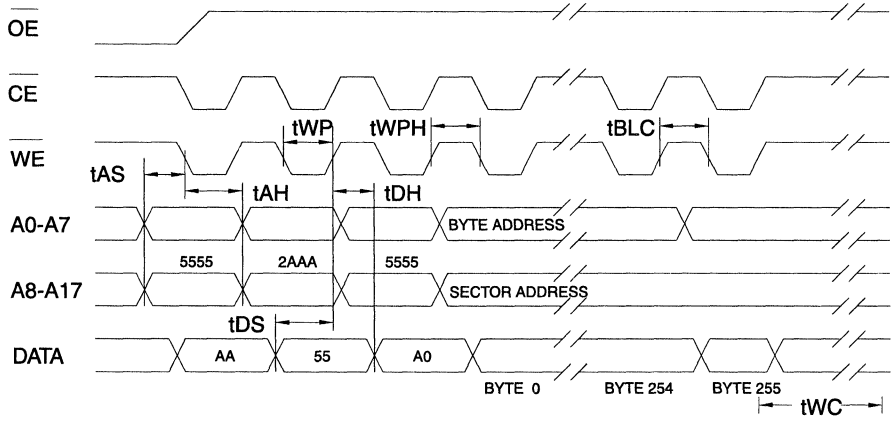


Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 256-bytes of data **MUST BE** loaded.

Software Data Protection Disable Algorithm [1]



Software Protected Program Cycle Waveform [1, 2, 3]



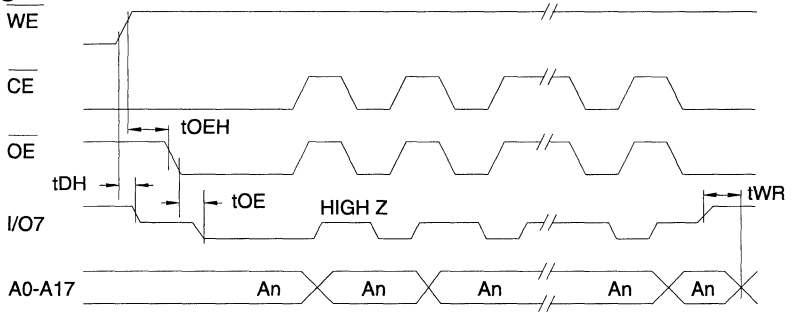
Notes: 1. A8 through A17 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

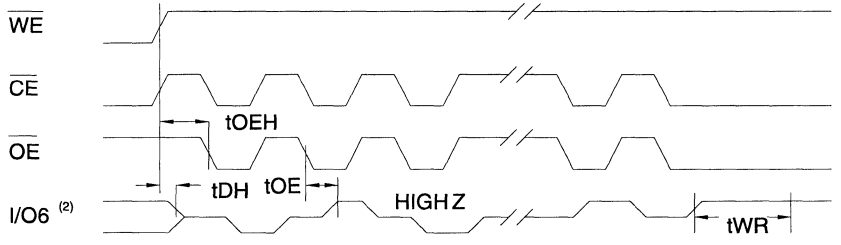


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

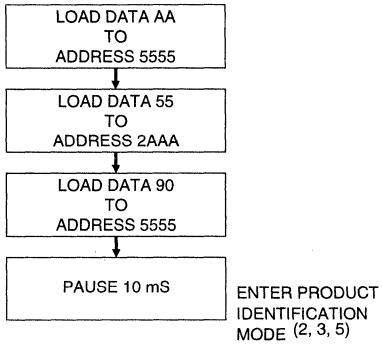
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]

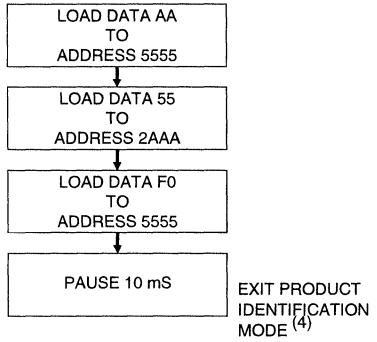


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry (1)

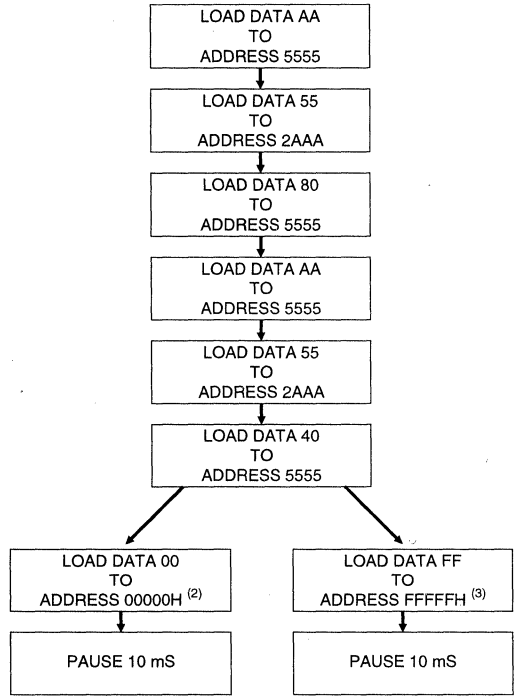


Software Product Identification Exit (1)



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A17 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: DA

Boot Block Lockout Feature Enable Algorithm (1)



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Lockout feature set on lower address boot block.
3. Lockout feature set on higher address boot block.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	40	0.1	AT29C020-90JC AT29C020-90PC AT29C020-90TC	32J 32P6 32T	Commercial (0° to 70°C)
100	40	0.1	AT29C020-10JC AT29C020-10PC AT29C020-10TC	32J 32P6 32T	Commercial (0° to 70°C)
	40	0.3	AT29C020-10JI AT29C020-10PI AT29C020-10TI	32J 32P6 32T	Industrial (-40° to 85°C)
120	40	0.1	AT29C020-12JC AT29C020-12PC AT29C020-12TC	32J 32P6 32T	Commercial (0° to 70°C)
	40	0.3	AT29C020-12JI AT29C020-12PI AT29C020-12TI	32J 32P6 32T	Industrial (-40° to 85°C)
150	40	0.1	AT29C020-15JC AT29C020-15PC AT29C020-15TC	32J 32P6 32T	Commercial (0° to 70°C)
	40	0.3	AT29C020-15JI AT29C020-15PI AT29C020-15TI	32J 32P6 32T	Industrial (-40° to 85°C)

4

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

4 Megabit (512K x 8) 5-volt Only 256-Byte Sector CMOS Flash Memory

Features

- Fast Read Access Time - 120 ns
- 5-Volt-Only Reprogramming
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 2048 Sectors (256 bytes/sector)
  - Internal Address and Data Latches for 256-Bytes
- Internal Program Control and Timer
- Hardware and Software Data Protection
- Two 16 KB Boot Blocks with Lockout
- Fast Sector Program Cycle Time - 10 ms
- DATA Polling for End of Program Detection
- Low Power Dissipation
  - 40 mA Active Current
  - 100 µA CMOS Standby Current
- Typical Endurance > 10,000 Cycles
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs

Description

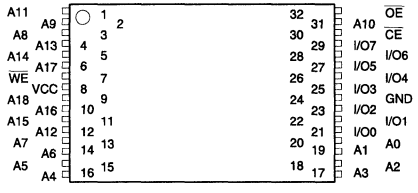
The AT29C040A is a 5-volt-only in-system Flash Programmable and Erasable Read Only Memory (PEROM). Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS EEPROM technology, the device offers access times up to 120 ns, and a low 220 mW power dissipation. When the device is deselected, the CMOS standby current is less than 100 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times. The programming algorithm is compatible with other devices in Atmel's 5-volt-only Flash family.

(continued)

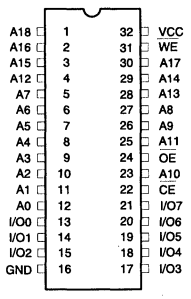
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

TSOP Top View
Type 1



DIP Top View



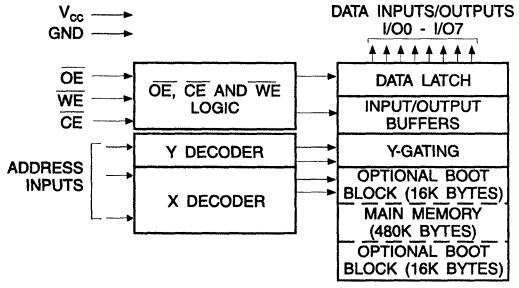
0333D

Description (Continued)

To allow for simple in-system reprogrammability, the AT29C040A does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C040A is performed on a sector basis; 256-bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 256-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29C040A is accessed like an EPROM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever CE or OE is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: Byte loads are used to enter the 256-bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by applying a low pulse on the WE or CE input with CE or WE low (respectively) and OE high. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE.

PROGRAM: The device is reprogrammed on a sector basis. If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be erased to read FFH. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on WE (or CE) within 150 µs of the low to high transition of WE (or CE) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A8 to A18 specify the sector address. The sector address must be valid during each high to low transition of WE (or CE). A0 to A7 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C040A. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the sector program timing specifications. The SDP feature protects all sectors, not just a single sector. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

(continued)

Device Operation (Continued)

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. The 256-bytes of data must be loaded into each sector by the same procedure as outlined in the program section under device operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C040A in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29C040A features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C040A provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

BOOT BLOCK PROGRAMMING LOCKOUT: The AT29C040A has two designated memory blocks that have a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. Each of these blocks consists of 16K bytes; the programming lockout feature can be set independently for either block. While the lockout feature does not have to be activated, it can be activated for either or both blocks.

These two 16K memory sections are referred to as *boot blocks*. Secure code which will bring up a system can be contained in a boot block. The AT29C040A blocks are located in the first 16K bytes of memory and the last 16K bytes of memory. The boot block programming lockout feature can therefore support systems that boot from the lower addresses of memory or the higher addresses. Once the programming lockout feature has been activated, the data in that block can no longer be erased or programmed; data in other memory locations can still be changed through the regular programming methods. To activate the lockout feature, a series of seven program commands to specific addresses with specific data must be performed. Please see Boot Block Lockout Feature Enable Algorithm.

If the boot block lockout feature has been activated on either block, the chip erase function will be disabled.

(continued)

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation (Continued)

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine whether programming of either boot block section is locked out. See Software Product Identification Entry and Exit sections. When the device is in the software product identification mode, a read from location 00002H will show if programming the lower address boot block is locked out while reading location FFFF2H will do so for the upper boot block. If the data is FE, the corresponding block can be programmed; if the data is FF, the program lockout feature has been activated and the corresponding block cannot be programmed. The software product identification exit mode should be used to return to standard operation.

DC and AC Operating Range

		AT29C040A-12	AT29C040A-15	AT29C040A-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A18 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
				A1 - A18 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: A4
5. See details under Software Product Identification Entry/Exit.

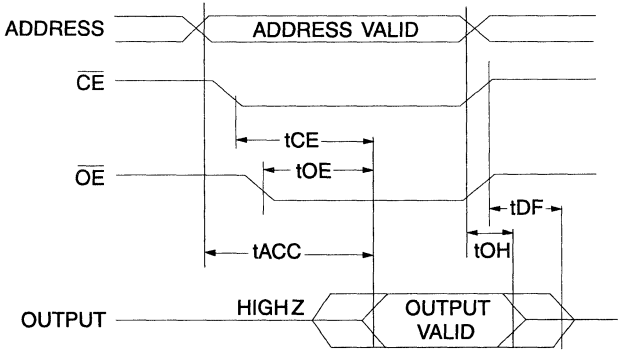
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		100	µA
			Ind.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			40	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V		4.2		V

AC Read Characteristics

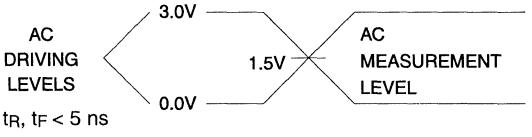
Symbol	Parameter	AT29C040A-12 Min	AT29C040A-12 Max	AT29C040A-15 Min	AT29C040A-15 Max	AT29C040A-20 Min	AT29C040A-20 Max	Units
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	70	0	80	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	30	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)

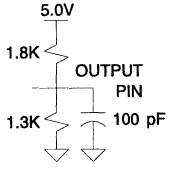


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

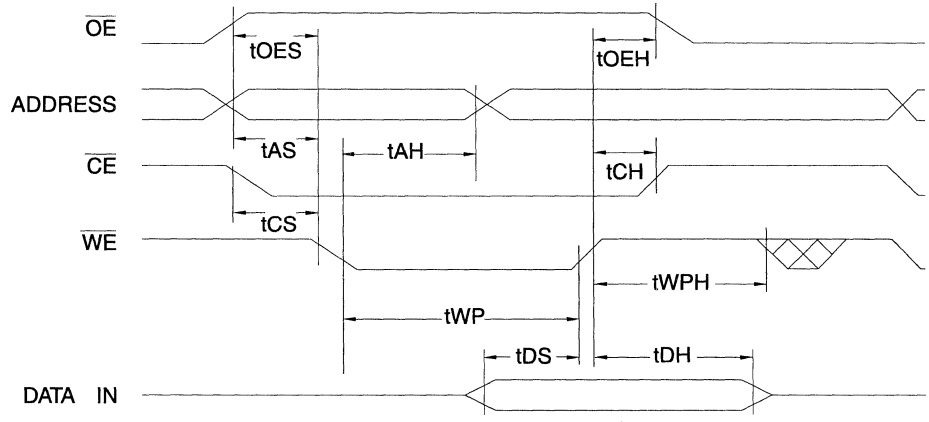
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

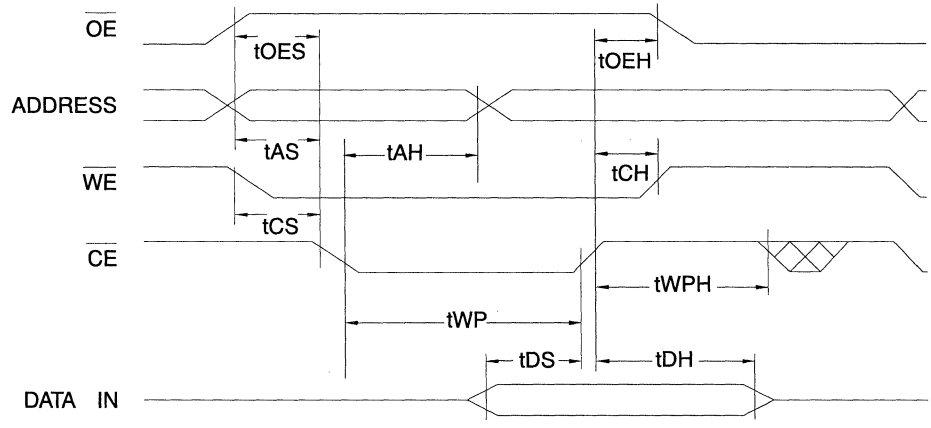
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	100		ns

AC Byte Load Waveforms (1)

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

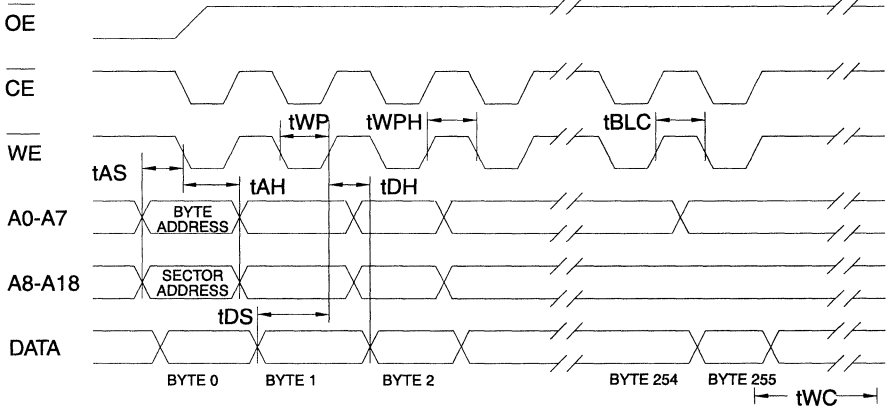


Note: 1. A complete sector (256-bytes) should be loaded using the waveforms shown in these byte load waveform diagrams.

Program Cycle Characteristics

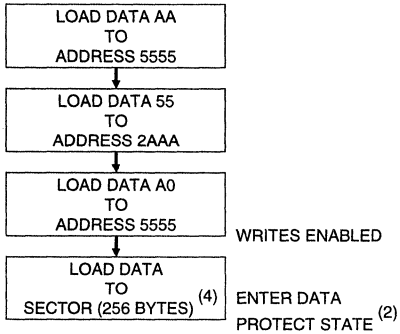
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms (1, 2, 3)



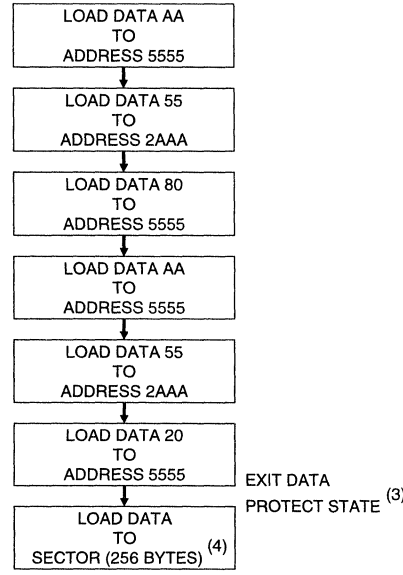
Notes: 1. A8 through A18 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Software Data Protection Enable Algorithm [1]

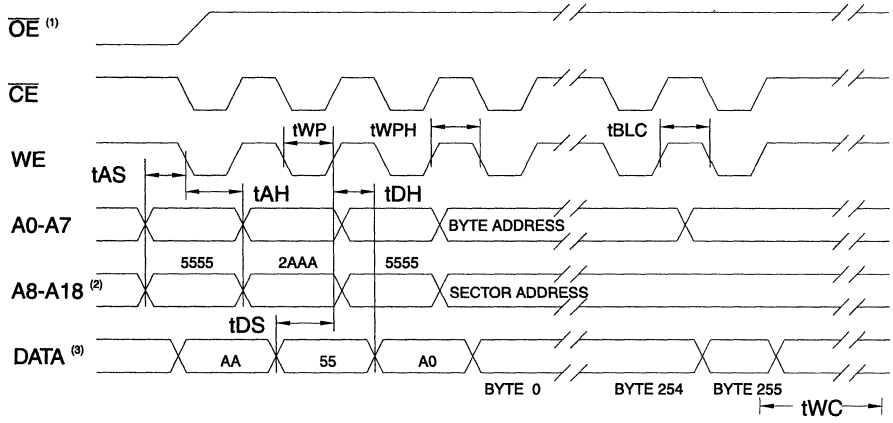


Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 256-bytes of data **MUST BE** loaded.

Software Data Protection Disable Algorithm [1]



Software Protected Program Cycle Waveform [1, 2, 3]



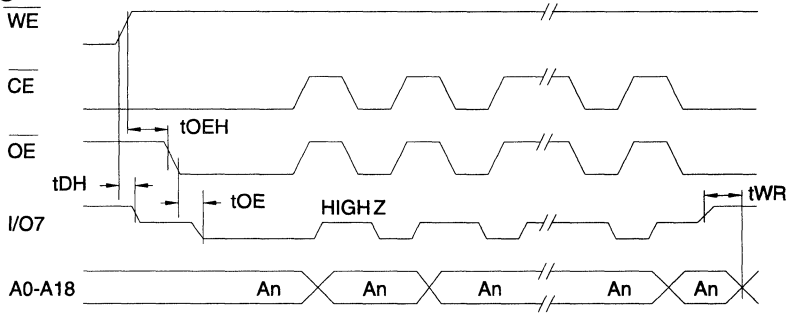
Notes: 1. A8 through A18 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

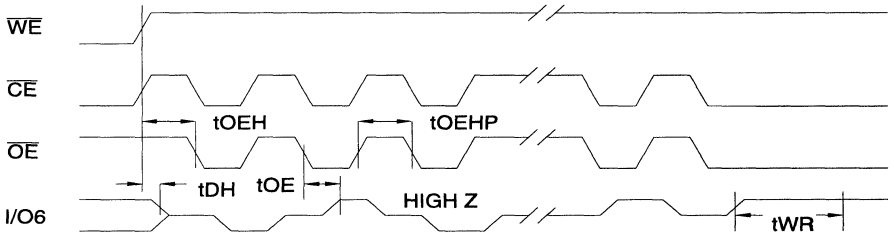


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

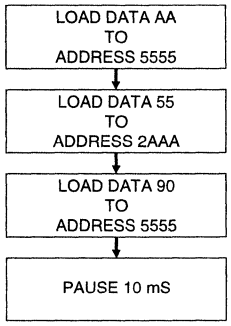
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]

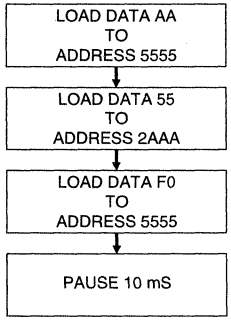


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

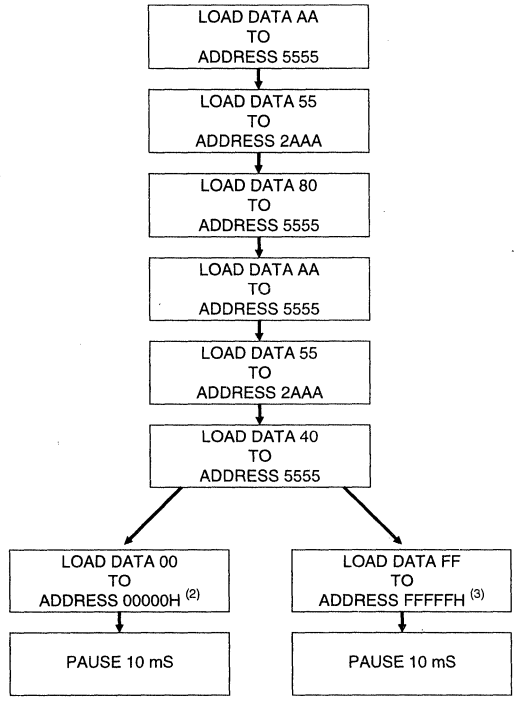


Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: A4

Boot Block Lockout Feature Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Lockout feature set on lower address boot block.
3. Lockout feature set on higher address boot block.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	40	0.1	AT29C040A-12PC AT29C040A-12TC	32P6 32T	Commercial (0° to 70°C)
	40	0.3	AT29C040A-12PI AT29C040A-12TI	32P6 32T	Industrial (-40° to 85°C)
150	40	0.1	AT29C040A-15PC AT29C040A-15TC	32P6 32T	Commercial (0° to 70°C)
	40	0.3	AT29C040A-15PI AT29C040A-15TI	32P6 32T	Industrial (-40° to 85°C)
200	40	0.1	AT29C040A-20PC	32P6	Commercial (0° to 70°C)
	40	0.3	AT29C040A-20PI	32P6	Industrial (-40° to 85°C)

4

Package Type	
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

Features

- Single Voltage Operation
  - 5V Read
  - 5V Reprogramming
- Fast Read Access Time - 70 ns
- Internal Program Control and Timer
- 8K bytes Boot Block With Lockout
- Fast Erase Cycle Time - 10 seconds
- Byte By Byte Programming - 50 µs/Byte
- Hardware Data Protection
- DATA Polling For End Of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 100 µA CMOS Standby Current
- Typical 10,000 Write Cycles

Description

The AT49F010 is a 5-volt-only in-system Flash Memory. Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 70 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA.

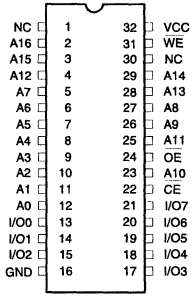
To allow for simple in-system reprogrammability, the AT49F010 does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT49F010 is performed by erasing the entire 1 megabit of memory and then programming on a byte by byte basis. The byte programming time is a fast 50 µs. The end of a program cycle can be optionally detected by the DATA polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

(continued)

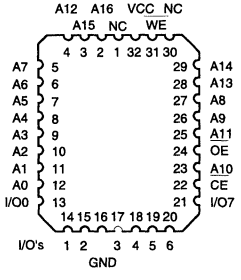
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View

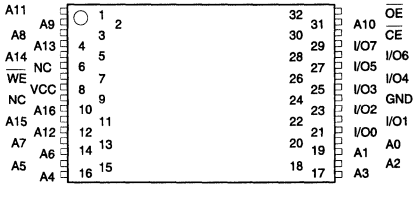


PLCC Top View



TSOP Top View

Type 1



1 Megabit (128K x 8) 5-volt Only CMOS Flash Memory

4

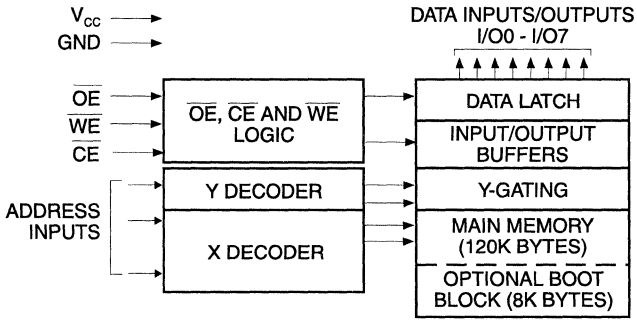
Preliminary

0566A

Description (Continued)

The optional 8K bytes boot block section includes a reprogramming write lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

Block Diagram



Device Operation

READ: The AT49F010 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

ERASURE: Before a byte can be reprogrammed, the 128K bytes memory array (or 120K bytes if the boot block featured is used) must be erased. The erased state of the memory bits is a logical "1". The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with a specific data pattern (please refer to the Chip Erase Cycle Waveforms).

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC}. If the boot block lockout feature has been enabled, the data in the boot sector will not be erased.

BYTE PROGRAMMING: Once the memory array is erased, the device is programmed (to a logical "0") on a byte-by-byte basis. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is accomplished via the internal device command register and is a 4 bus cycle operation (please refer to the Command Definitions table). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K bytes. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000H to 01FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification code should be used to return to standard operation.

(continued)

Device Operation (Continued)

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49F010 features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT49F010 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F010 in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (c) Noise filter: Pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

4

Command Definition (in Hex)

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Byte Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout (1)	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit (2)	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit (2)	1	XXXX	F0										

Note: 1. The 8K byte boot sector has the address range 00000H to 01FFFH.
2. Either one of the Product ID exit commands can be used.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49F010-70	AT49F010-90	AT49F010-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A16 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
				A1 - A16 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}, A1 - A16 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}, A1 - A16 = V_{IL}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 17H
5. See details under Software Product Identification Entry/Exit.

DC Characteristics

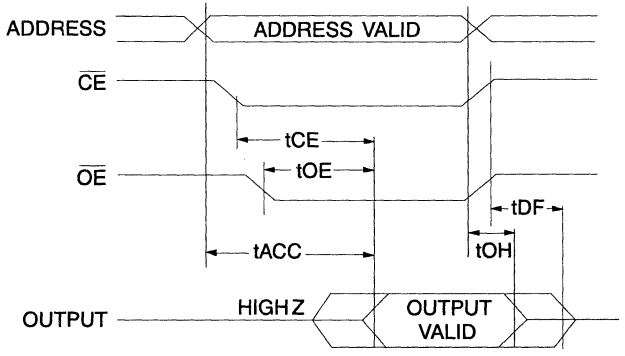
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		100	µA
			Ind.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			3	mA
I_{CC} (1)	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V		4.2		V

Note: 1. In the erase mode, I_{CC} is 90 mA.

AC Read Characteristics

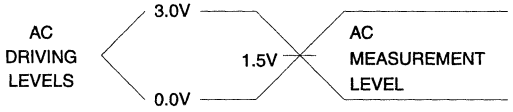
Symbol	Parameter	AT49F010-70 Min	AT49F010-70 Max	AT49F010-90 Min	AT49F010-90 Max	AT49F010-12 Min	AT49F010-12 Max	Units
t_{ACC}	Address to Output Delay		70		90		120	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		70		90		120	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay		35	0	40	0	50	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	0	30	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



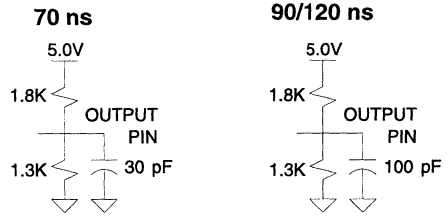
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

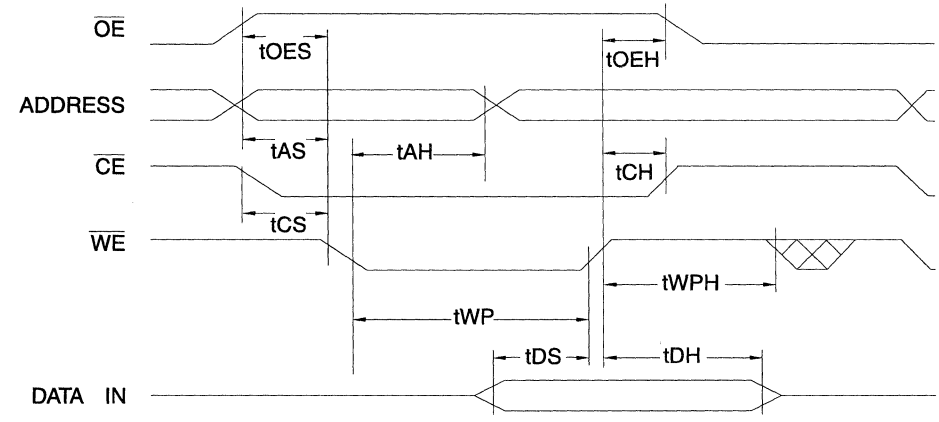
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

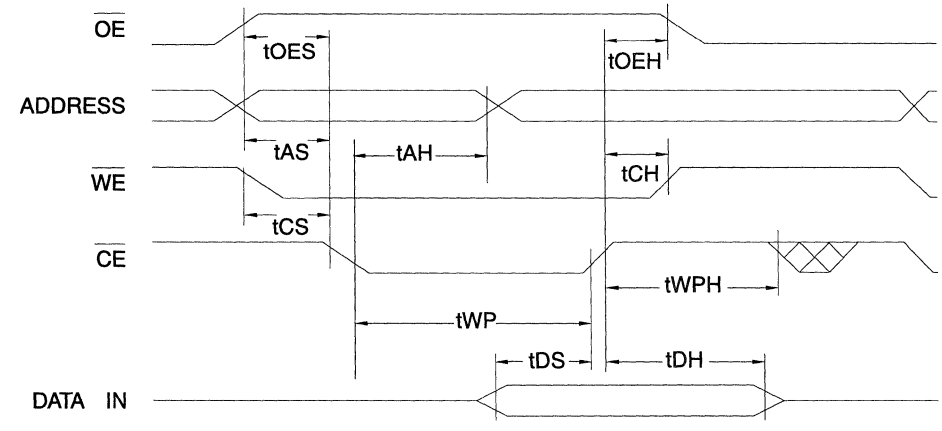
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	90		ns

AC Byte Load Waveforms

$\overline{WE}$ Controlled



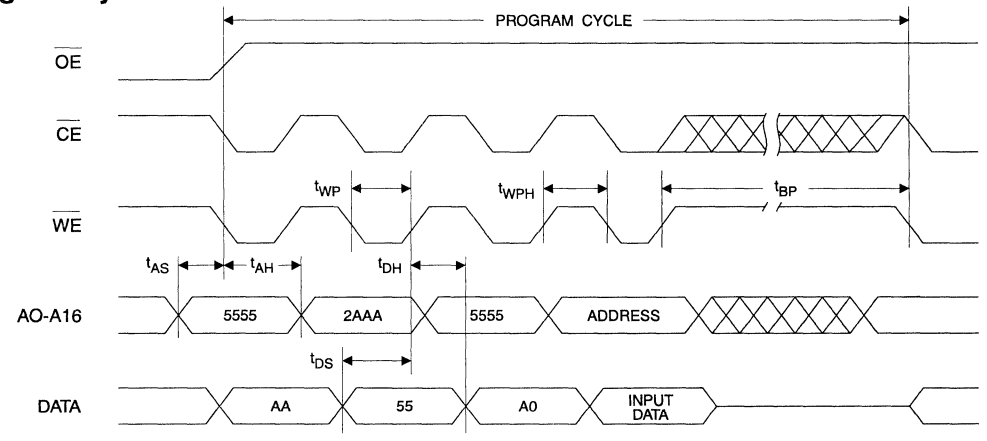
$\overline{CE}$ Controlled



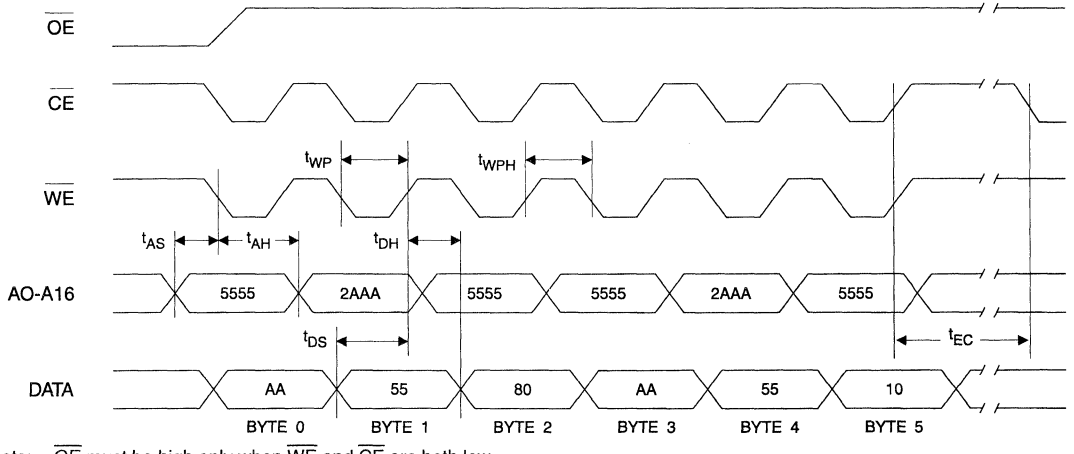
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte Programming Time		10	50	µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	90			ns
t_{WPH}	Write Pulse Width High	90			ns
t_{EC}	Erase Cycle Time			10	seconds

Program Cycle Waveforms



Chip Erase Cycle Waveforms



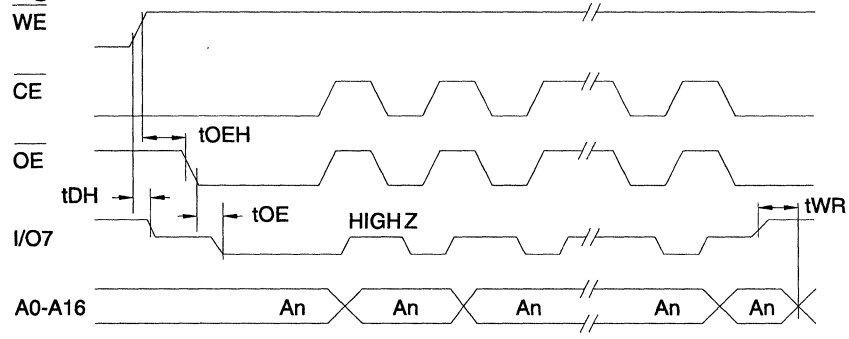
Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Data Polling Waveforms

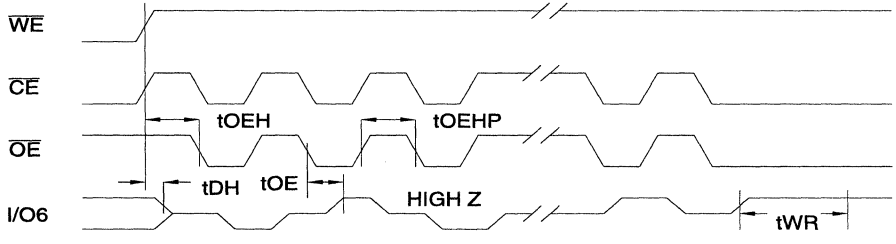


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

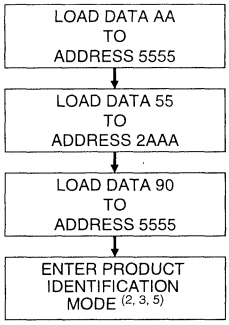
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]

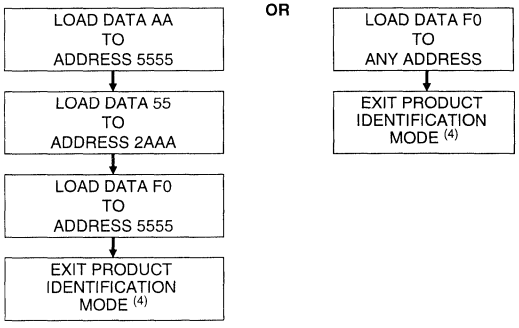


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

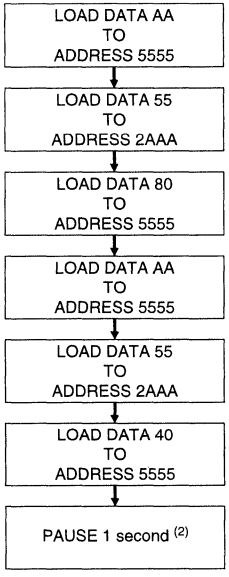


Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A16 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 17H

Boot Block Lockout Feature Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Boot block lockout feature enabled.

4

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	0.1	AT49F010-70JC AT49F010-70PC AT49F010-70TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT49F010-70JI AT49F010-70PI AT49F010-70TI	32J 32P6 32T	Industrial (-40° to 85°C)
90	50	0.1	AT49F010-90JC AT49F010-90PC AT49F010-90TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT49F010-90JI AT49F010-90PI AT49F010-90TI	32J 32P6 32T	Industrial (-40° to 85°C)
120	50	0.1	AT49F010-12JC AT49F010-12PC AT49F010-12TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT49F010-12JI AT49F010-12PI AT49F010-12TI	32J 32P6 32T	Industrial (-40° to 85°C)

Note: 1. The AT49F010 has as optional boot block feature. The part number shown in the Ordering Information table is for devices with the boot block in the lower address range (i.e., 00000H to 01FFFH). Users requiring the boot block to be in the higher address range should contact Atmel.

Package Type	
32J	32 Lead, Plastic, J-Leaded Chip Carrier Package (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

Features

- Single Voltage Operation
  - 5V Read
  - 5V Reprogramming
- Fast Read Access Time - 90 ns
- Internal Program Control and Timer
- 8K bytes Boot Block With Lockout
- Fast Erase Cycle Time - 10 seconds
- Byte By Byte Programming - 50 µs/Byte
- Hardware Data Protection
- DATA Polling For End Of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 100 µA CMOS Standby Current
- Typical 10,000 Write Cycles

Description

The AT49F020 is a 5-volt-only in-system Flash Memory. Its 2 megabits of memory is organized as 262,144 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA.

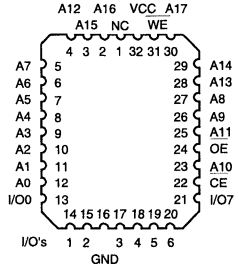
To allow for simple in-system reprogrammability, the AT49F020 does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT49F020 is performed by erasing the entire 2 megabits of memory and then programming on a byte by byte basis. The byte programming time is a fast 50 µs. The end of a program cycle can be optionally detected by the DATA polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

(continued)

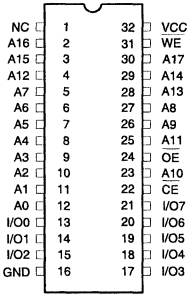
Pin Configurations

Pin Name	Function
A0 - A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

PLCC Top View

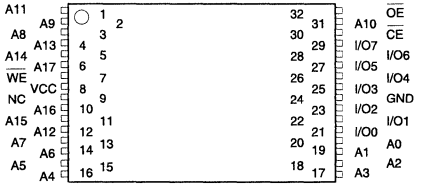


DIP Top View



TSOP Top View

Type 1



2 Megabit (256K x 8) 5-volt Only CMOS Flash Memory

4

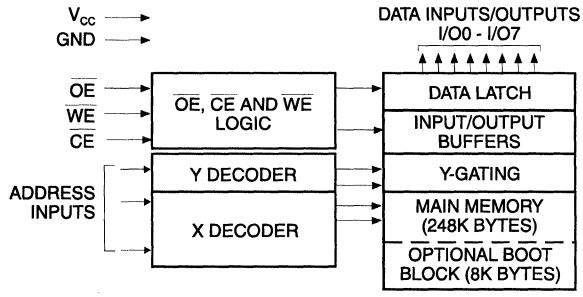
Preliminary

0567A

Description (Continued)

The optional 8K bytes boot block section includes a reprogramming write lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

Block Diagram



Device Operation

READ: The AT49F020 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

ERASURE: Before a byte can be reprogrammed, the 256K bytes memory array (or 248K bytes if the boot block featured is used) must be erased. The erased state of the memory bits is a logical "1". The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with a specific data pattern (please refer to the Chip Erase Cycle Waveforms).

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC}. If the boot block lockout feature has been enabled, the data in the boot sector will not be erased.

BYTE PROGRAMMING: Once the memory array is erased, the device is programmed (to a logical "0") on a byte-by-byte basis. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is accomplished via the internal device command register and is a 4 bus cycle operation (please refer to the Command Definitions table). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K bytes. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000H to 01FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification code should be used to return to standard operation.

(continued)

Device Operation (Continued)

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49F020 features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT49F020 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F020 in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (c) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

4

Command Definition (in Hex)

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Byte Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout (1)	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit (2)	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit (2)	1	XXXX	F0										

Note: 1. The 8K byte boot sector has the address range 00000H to 01FFFH.
2. Either one of the Product ID exit commands can be used.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49F020-90	AT49F020-12	AT49F020-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A17 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
				A1 - A17 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}, A1 - A17=V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}, A1 - A17=V_{IL}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 0BH
5. See details under Software Product Identification Entry/Exit.

DC Characteristics

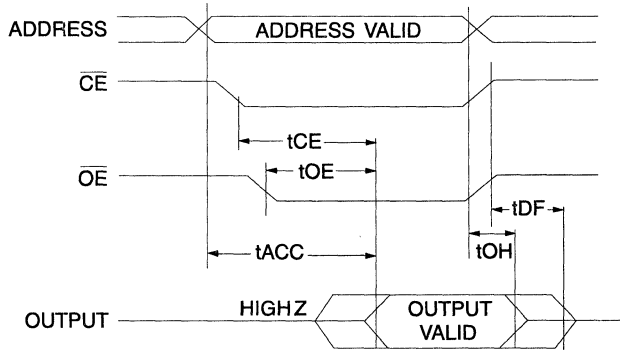
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		100	µA
			Ind.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			3	mA
I_{CC} (1)	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V		4.2		V

Note: 1. In the erase mode, I_{CC} is 90 mA.

AC Read Characteristics

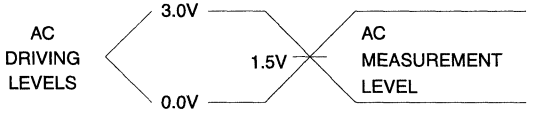
Symbol	Parameter	AT49F020-90 Min	AT49F020-90 Max	AT49F020-12 Min	AT49F020-12 Max	AT49F020-15 Min	AT49F020-15 Max	Units
t_{ACC}	Address to Output Delay		90		120		150	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120		150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	0	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



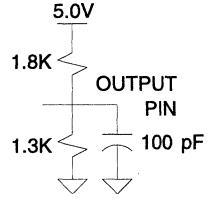
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

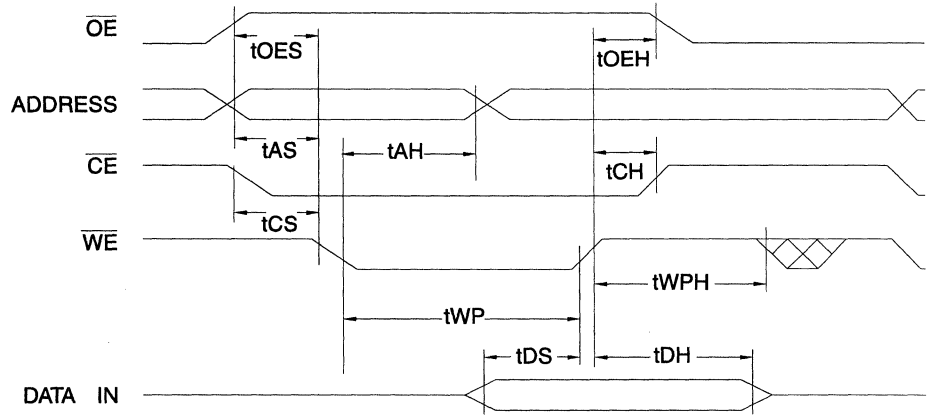
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

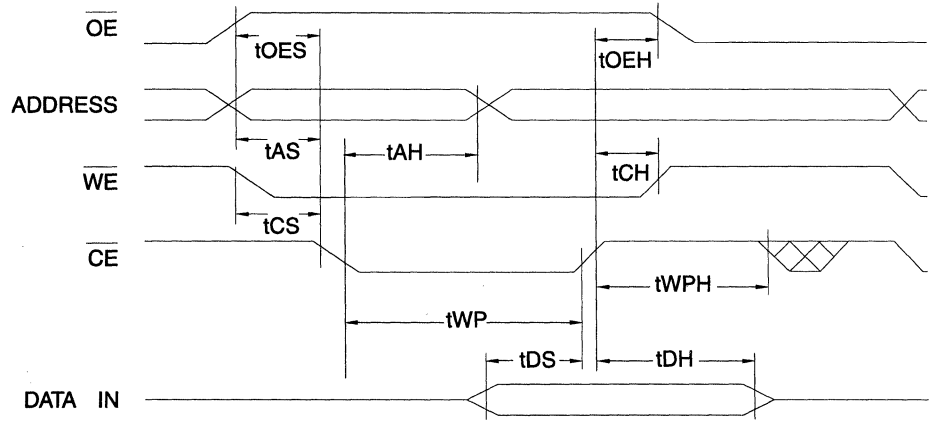
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	90		ns

AC Byte Load Waveforms

$\overline{WE}$ Controlled



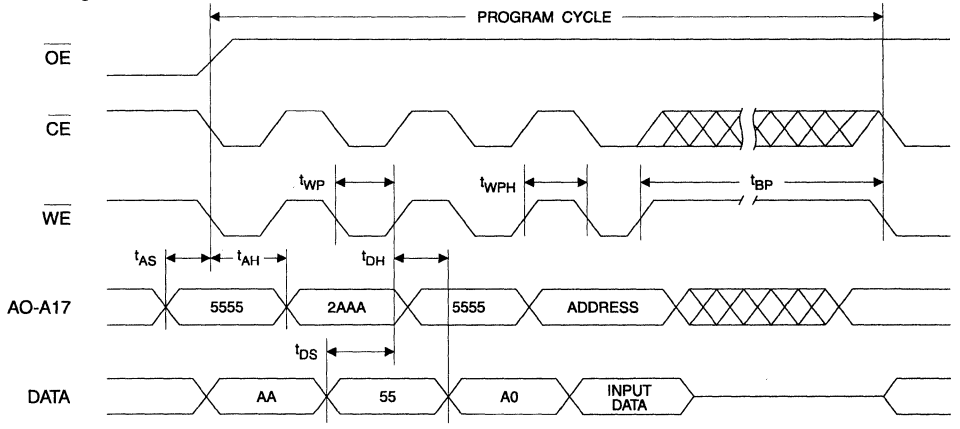
$\overline{CE}$ Controlled



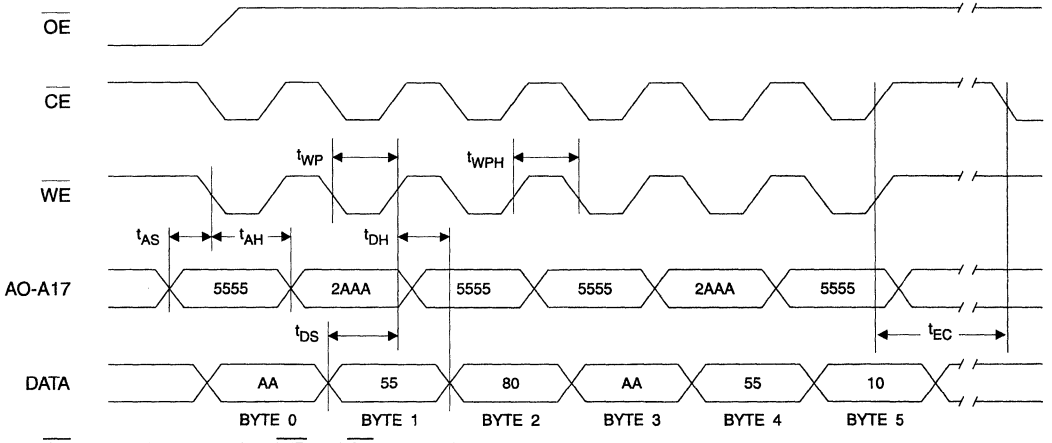
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte Programming Time		10	50	µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	90			ns
t_{WPH}	Write Pulse Width High	90			ns
t_{EC}	Erase Cycle Time			10	seconds

Program Cycle Waveforms



Chip Erase Cycle Waveforms



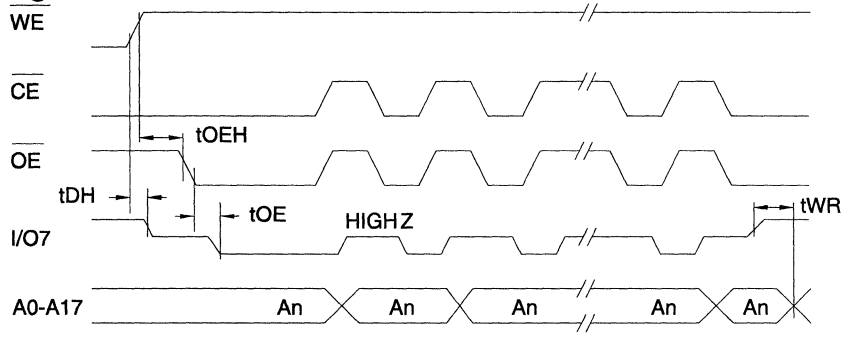
Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Data Polling Waveforms

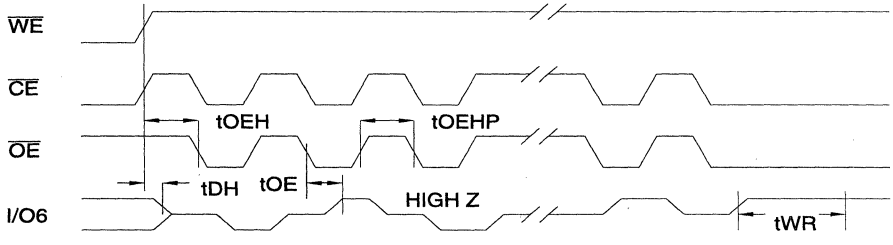


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

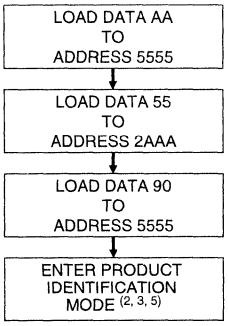
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]

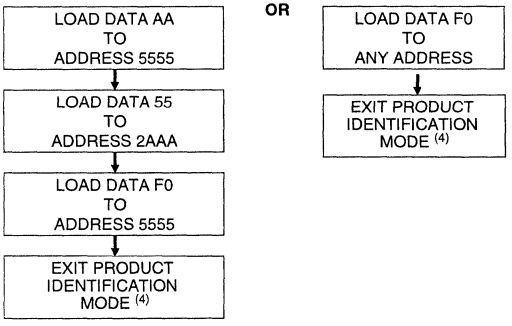


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

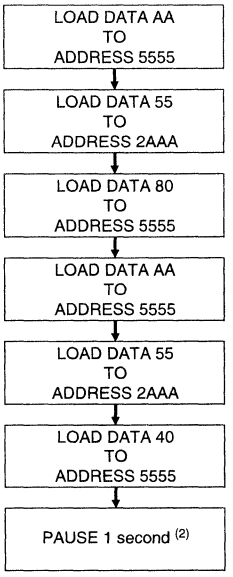


Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A17 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 0BH

Boot Block Lockout Feature Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Boot block lockout feature enabled.

4

Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	50	0.1	AT49F020-90JC AT49F020-90PC AT49F020-90TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT49F020-90JI AT49F020-90PI AT49F020-90TI	32J 32P6 32T	Industrial (-40° to 85°C)
120	50	0.1	AT49F020-12JC AT49F020-12PC AT49F020-12TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT49F020-12JI AT49F020-12PI AT49F020-12TI	32J 32P6 32T	Industrial (-40° to 85°C)
150	50	0.1	AT49F020-15JC AT49F020-15PC AT49F020-15TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT49F020-15JI AT49F020-15PI AT49F020-15TI	32J 32P6 32T	Industrial (-40° to 85°C)

Note: 1. The AT49F020 has as optional boot block feature. The part number shown in the Ordering Information table is for devices with the boot block in the lower address range (i.e., 00000H to 01FFFH). Users requiring the boot block to be in the higher address range should contact Atmel.

Package Type	
32J	32 Lead, Plastic, J-Leaded Chip Carrier Package (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

Features

- Single Voltage Operation
  - 5V Read
  - 5V Reprogramming
- Fast Read Access Time - 90 ns
- Internal Erase/Program Control
- Sector Architecture
  - One 8K Words (16K bytes) Boot Block with Programming Lockout
  - Two 8K Words (16K bytes) Parameter Blocks
  - One 104K Words (208K bytes) Main Memory Array Block
- Fast Sector Erase Time - 10 seconds
- Word-By-Word Programming - 50 µs/Word
- Hardware Data Protection
- DATA Polling For End Of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 300 µA CMOS Standby Current
- Typical 10,000 Write Cycles

Description

The AT49F2048 is a 5-volt-only, 2 megabit Flash Memory organized as 128K words of 16 bits each. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 275 mW. When deselected, the CMOS standby current is less than 300 µA.

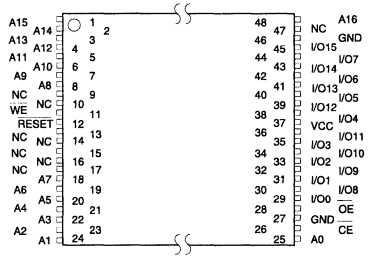
To allow for simple in-system reprogrammability, the AT49F2048 does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs to avoid bus con-

(continued)

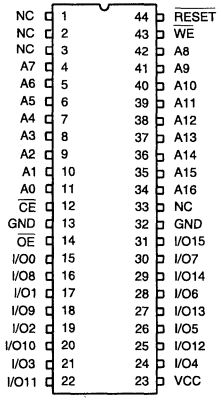
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$	Reset
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

TSOP Top View
Type 1



SOIC (SOP)



2 Megabit (128K x 16) 5-volt Only CMOS Flash Memory

Preliminary

4

0568B

Description (Continued)

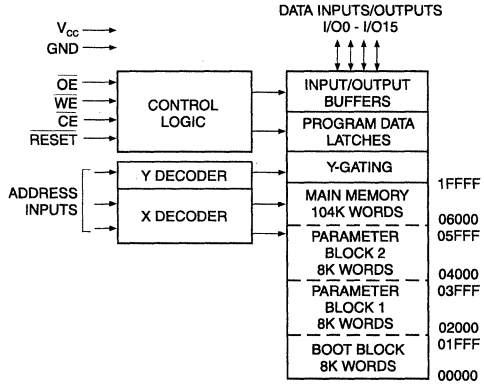
tention. Reprogramming the AT49F2048 is performed by first erasing a block of data and then programming on a word-by-word basis.

The device is erased by executing the erase command sequence; the device internally controls the erase operation. The memory is divided into three blocks for erase operations. There are two 8K word parameter block sections and one sector consisting of the boot block and the main memory array block. The AT49F2048 is programmed on a word-by-word basis.

The device has the capability to protect the data in the boot block; this feature is enabled by a command sequence. Once the boot block programming lockout feature is enabled, the data in the boot block cannot be changed when input levels of 5.5 volts or less are used. The typical number of program and erase cycles is in excess of 10,000 cycles.

The optional 8K word boot block section includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is protected from being reprogrammed.

Block Diagram



Device Operation

READ: The AT49F2048 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the Read or Standby mode, depending upon the state of the control inputs. By applying a 12V ± 0.5V input signal to the $\overline{RESET}$ pin the boot block array can be reprogrammed even if the boot block program lockout feature has been enabled (see Boot Block Programming Lockout Override section).

ERASURE: Before a word can be reprogrammed, it must be erased. The erased state of the memory bits is a logical "1". The entire device can be erased at one time by using a 6-byte software code.

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC}.

(continued)

Device Operation (Continued)

CHIP ERASE: If the boot block lockout has been enabled, the Chip Erase function is disabled; sector erases for the parameter blocks and main memory block will still operate. After the full chip erase the device will return back to read mode. Any command during chip erase will be ignored.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into three sectors that can be individually erased. There are two 8K word parameter block sections and one sector consisting of the boot block and the main memory array block. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling WE edge of the sixth cycle while the 30H data input command is latched at the rising edge of WE. The sector erase starts after the rising edge of WE of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together (from the same sector erase command). Once the boot region has been protected, only the main memory array sector will erase when its sector erase command is issued.

WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical "0") on a word-by-word basis. Programming is accomplished via the internal device command register and is a 4 bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified tBP cycle time. The DATA polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K words. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000H to 01FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed when input levels of 5.5V or less are used. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been enabled and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

BOOT BLOCK PROGRAMMING LOCKOUT OVERRIDE: The user can override the boot block programming lockout by taking the RESET pin to 12 volts. By doing this protected boot block data can be altered through a chip erase, sector erase or word programming. When the RESET pin is brought back to TTL levels the boot block programming lockout feature is again active.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49F2048 features DATA polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. DATA polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to DATA polling the AT49F2048 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

(continued)

Device Operation (Continued)

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F2048 in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

Command Definition (in Hex) (1)

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA (4, 5)	30
Word Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout (2)	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit (3)	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit (3)	1	xxxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
2. The 8K word boot sector has the address range 00000H to 01FFFH.
3. Either one of the Product ID Exit commands can be used.
4. SA = sector addresses:
   SA = 03XXX for PARAMETER BLOCK 1
   SA = 05XXX for PARAMETER BLOCK 2
   SA = 1FXXX for MAIN MEMORY ARRAY
5. When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together (from the same sector erase command). Once the boot region has been protected, only the main memory array sector will erase when its sector erase command is issued.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49F2048-90	AT49F2048-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	D_{OUT}
Program/Erase (2)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	V_{IH}	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}		
Program Inhibit	X	V_{IL}	X	V_{IH}		
Output Disable	X	V_{IH}	X	V_{IH}		High Z
Reset	X	X	X	V_{IL}	X	High Z
Product Identification						
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A1 - A16 = VIL, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
					A1 - A16 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				V_{IH}	A0 = VIL, A1 - A16 = V_{IL}	Manufacturer Code (4)
					A0 = V_{IH}, A1 - A16 = V_{IL}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 82H
5. See details under Software Product Identification Entry/Exit.

DC Characteristics

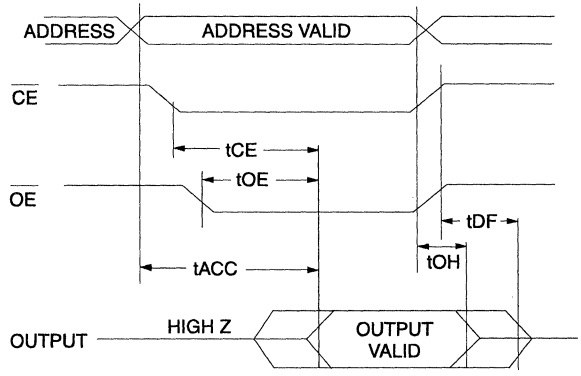
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		3	mA
I_{CC} (1)	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

Note: 1. In the erase mode, I_{CC} is 90 mA.

AC Read Characteristics

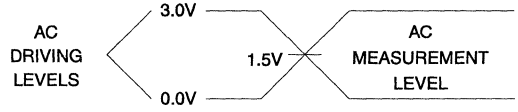
Symbol	Parameter	AT49F2048-90 Min	AT49F2048-90 Max	AT49F2048-12 Min	AT49F2048-12 Max	Units
t_{ACC}	Address to Output Delay		90		120	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms (1, 2, 3, 4)



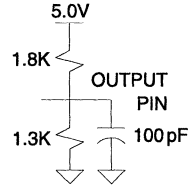
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

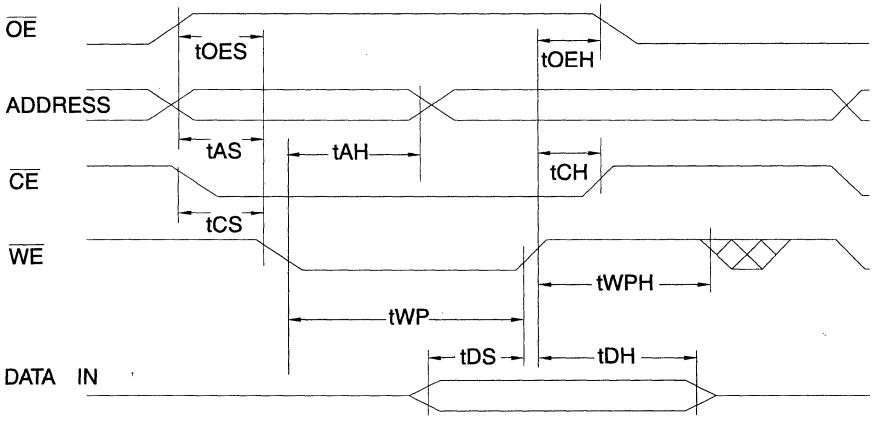
Note: 1. This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

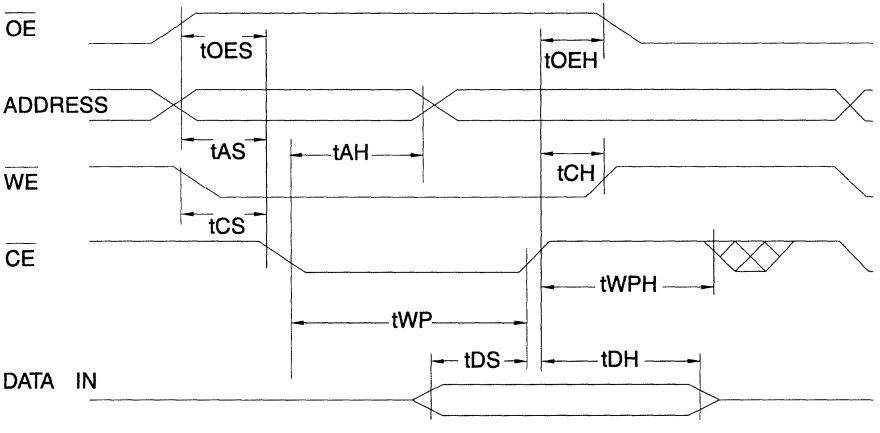
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	90		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



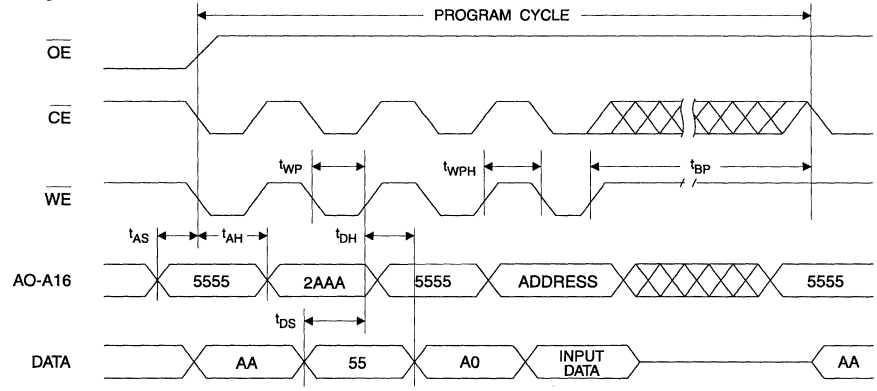
$\overline{CE}$ Controlled



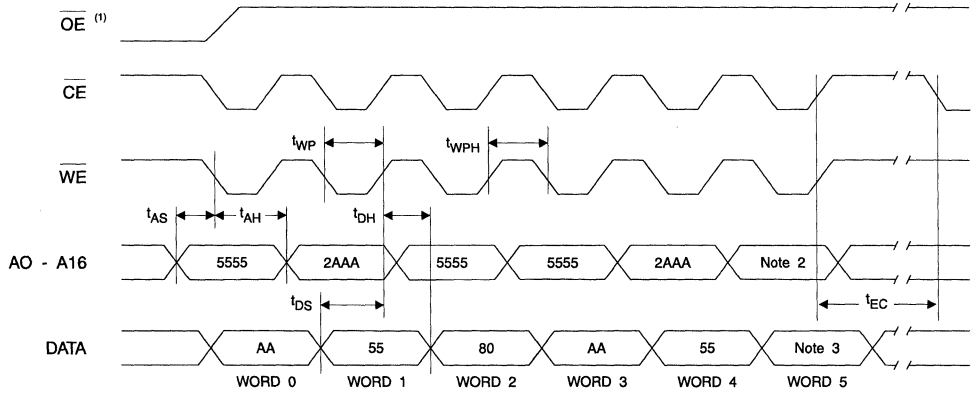
Program Cycle Characteristics

Symbol	Parameter	Min	Max	Units
t_{BP}	Word Programming Time		50	µs
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	90		ns
t_{WPH}	Write Pulse Width High	90		ns
t_{EC}	Erase Cycle Time		10	seconds

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



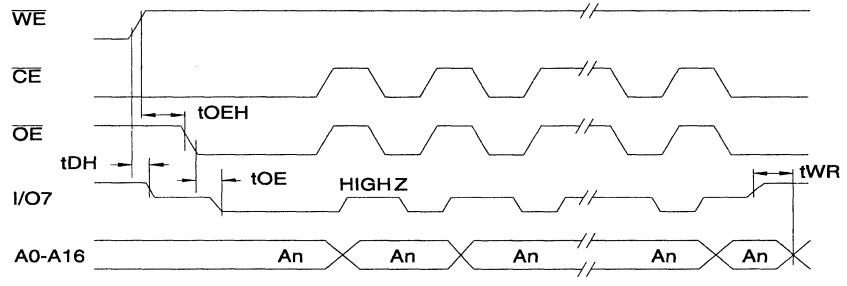
Notes: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 4 under command definitions.)
3. For chip erase, the data should be 10_H, and for sector erase, the data should be 30_H.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

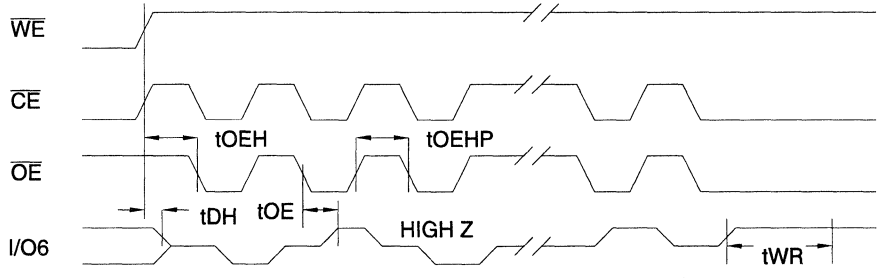


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

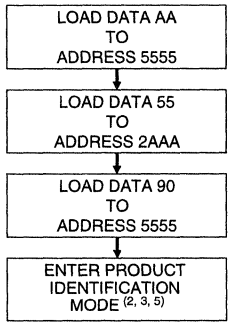
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]

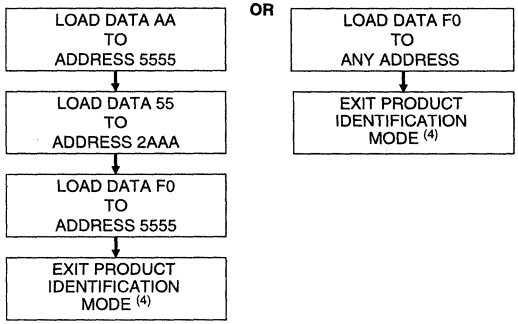


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

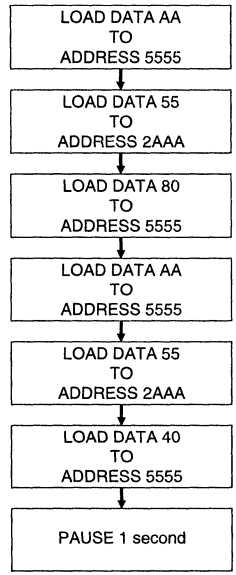


Software Product Identification Exit [1, 6]



Notes for software product identification:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A14 - A0 (Hex).
2. A1 - A16 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 82H
6. Either one of the Product ID Exit commands can be used.

Boot Block Lockout Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A14 - A0 (Hex).
2. Boot block lockout feature enabled.

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	50	0.3	AT49F2048-90TC AT49F2048-90RC	48T 44R	Commercial (0° to 70°C)
	50	0.3	AT49F2048-90TI AT49F2048-90RI	48T 44R	Industrial (-40° to 85°C)
120	50	0.3	AT49F2048-12TC AT49F2048-12RC	48T 44R	Commercial (0° to 70°C)
	50	0.3	AT49F2048-12TI AT49F2048-12RI	48T 44R	Industrial (-40° to 85°C)

Note: 1. The AT49F2048 has as optional boot block feature. The part number shown in the Ordering Information table is for devices with the boot block in the lower address range (i.e., 00000H to 01FFFH). Users requiring the boot block to be in the higher address range should contact Atmel.

4

Package Type	
48T	48 Lead, Thin Small Outline Package (TSOP)
44R	44 Lead, 0.525" Wide, Plastic Gull Wing Small Outline Package (SOIC/SOP)

Features

- Single Voltage Operation
  - 5V Read
  - 5V Reprogramming
- Fast Read Access Time - 90 ns
- Internal Program Control and Timer
- 16K bytes Boot Block With Lockout
- Fast Erase Cycle Time - 10 seconds
- Byte By Byte Programming - 50 µs/Byte
- Hardware Data Protection
- DATA Polling For End Of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 100 µA CMOS Standby Current
- Typical 10,000 Write Cycles

Description

The AT49F040 is a 5-volt-only in-system Flash Memory. Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA.

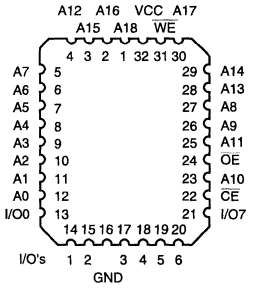
To allow for simple in-system reprogrammability, the AT49F040 does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT49F040 is performed by erasing the entire 4 megabits of memory and then programming on a byte by byte basis. The byte programming time is a fast 50 µs. The end of a program cycle can be optionally detected by the DATA polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

(continued)

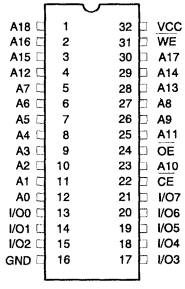
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs

PLCC Top View

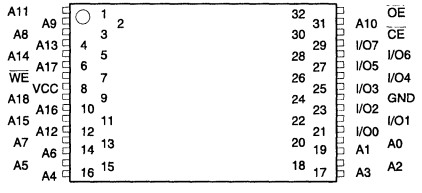


DIP Top View



TSOP Top View

Type 1



4 Megabit (512K x 8) 5-volt Only CMOS Flash Memory

4

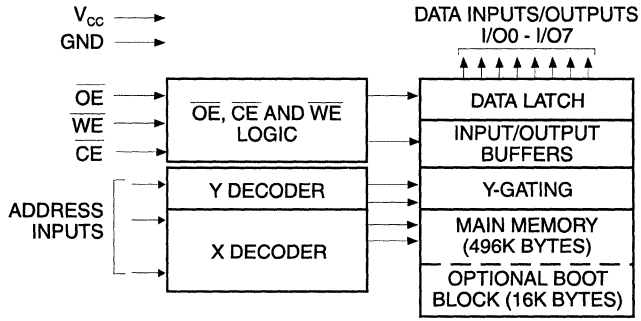
Preliminary

0359C

Description (Continued)

The optional 16K bytes boot block section includes a reprogramming write lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

Block Diagram



Device Operation

READ: The AT49F040 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

ERASURE: Before a byte can be reprogrammed, the 512K bytes memory array (or 496K bytes if the boot block featured is used) must be erased. The erased state of the memory bits is a logical "1". The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with a specific data pattern (please refer to the Chip Erase Cycle Waveforms).

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC}. If the boot block lockout feature has been enabled, the data in the boot sector will not be erased.

BYTE PROGRAMMING: Once the memory array is erased, the device is programmed (to a logical "0") on a byte-by-byte basis. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is accomplished via the internal device command register and is a 4 bus cycle operation (please refer to the Command Definitions table). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 16K bytes. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000H to 03FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification code should be used to return to standard operation.

(continued)

Device Operation (Continued)

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49F040 features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT49F040 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F040 in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (c) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

4

Command Definition (in Hex)

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Byte Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout (1)	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit (2)	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit (2)	1	XXXX	F0										

Note: 1. The 16K byte boot sector has the address range 00000H to 03FFFH.
2. Either one of the Product ID exit commands can be used.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ with Respect to Ground	-0.6V to + 13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49F040-90	AT49F040-12	AT49F040-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A18 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
				A1 - A18 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				A0 = V_{IL}, A1 - A18 = V_{IL}	Manufacturer Code (4)
				A0 = V_{IH}, A1 - A18 = V_{IL}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 13H
5. See details under Software Product Identification Entry/Exit.

DC Characteristics

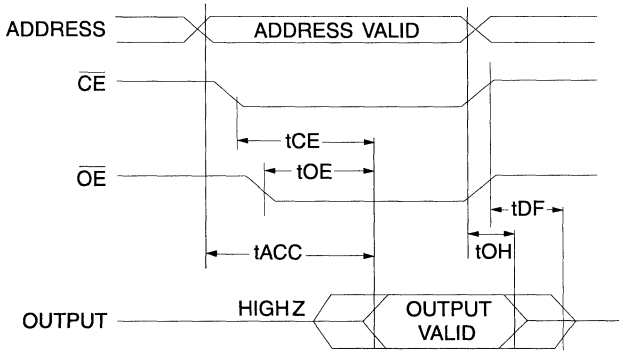
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		100	µA
			Ind.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			3	mA
I_{CC} (1)	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V		4.2		V

Note: 1. In the erase mode, I_{CC} is 90 mA.

AC Read Characteristics

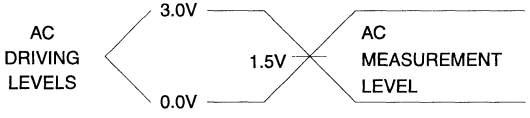
Symbol	Parameter	AT49F040-90 Min	AT49F040-90 Max	AT49F040-12 Min	AT49F040-12 Max	AT49F040-15 Min	AT49F040-15 Max	Units
t_{ACC}	Address to Output Delay		90		120		150	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120		150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	0	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



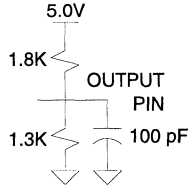
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

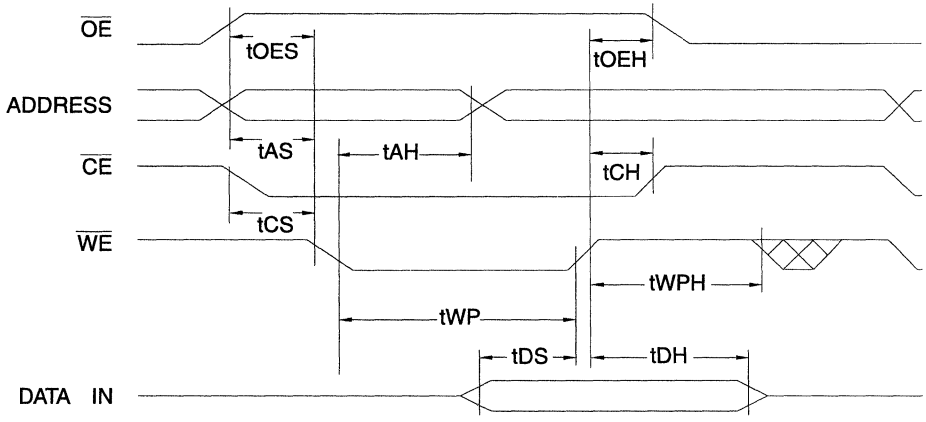
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

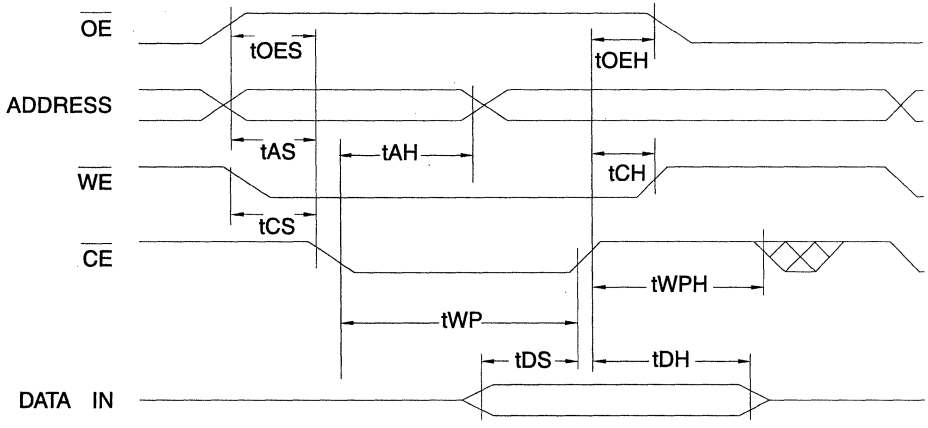
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	90		ns

AC Byte Load Waveforms

$\overline{WE}$ Controlled



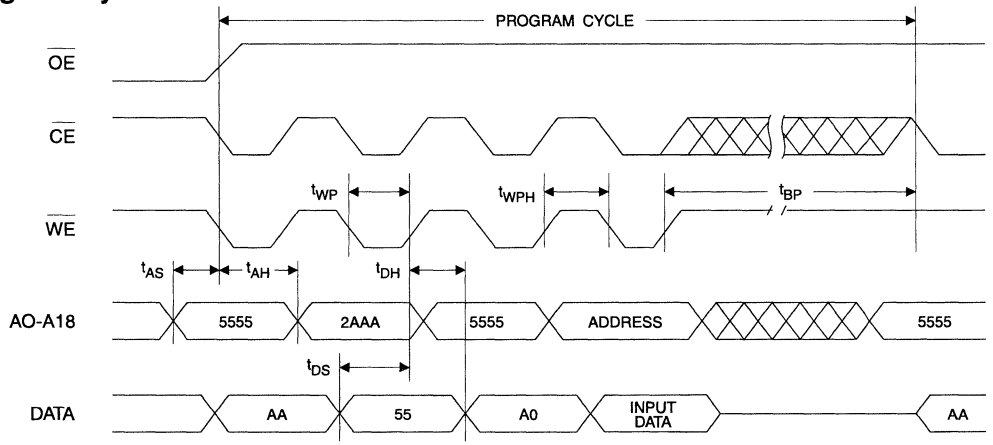
$\overline{CE}$ Controlled



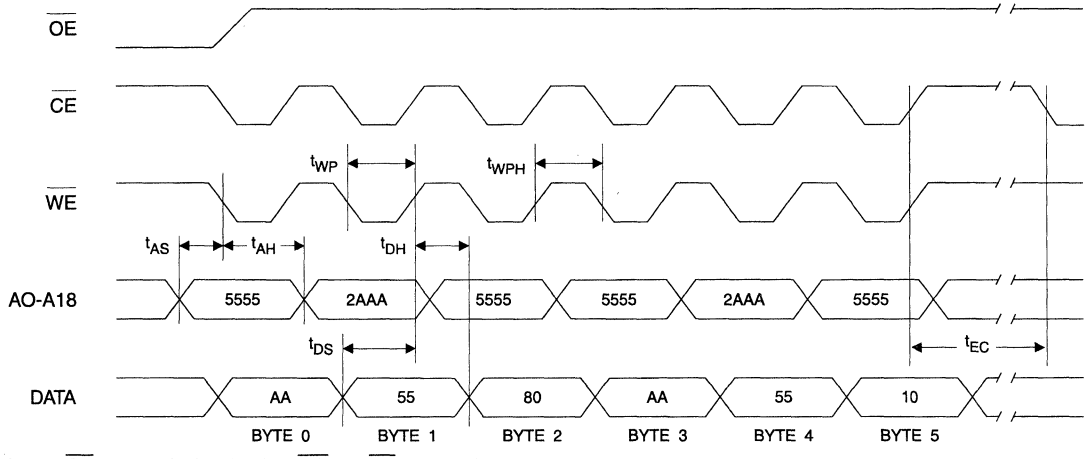
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte Programming Time		10	50	µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	90			ns
t_{WPH}	Write Pulse Width High	90			ns
t_{EC}	Erase Cycle Time			10	seconds

Program Cycle Waveforms



Chip Erase Cycle Waveforms



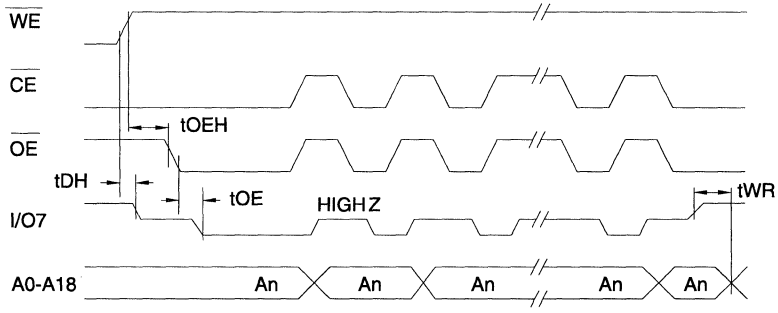
Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

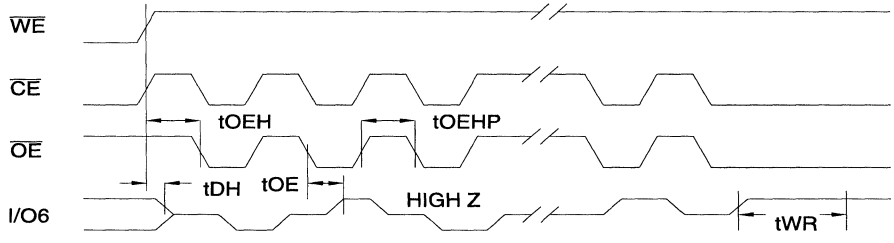


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

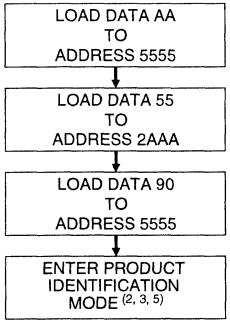
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]

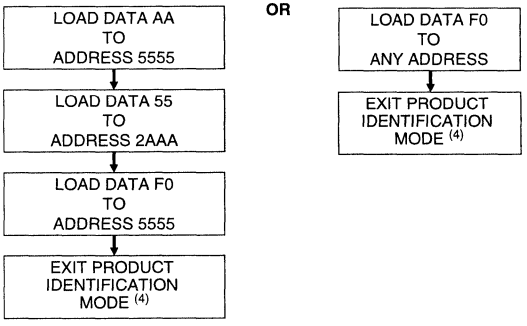


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

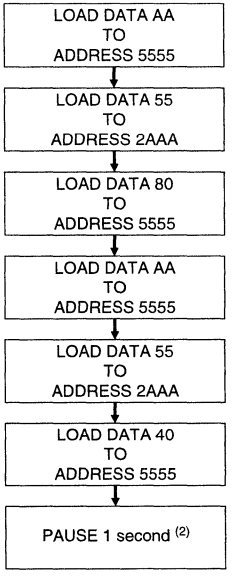


Software Product Identification Exit [1]



Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 13H

Boot Block Lockout Feature Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Boot block lockout feature enabled.

4

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	50	0.1	AT49F040-90JC AT49F040-90PC AT49F040-90TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT49F040-90JI AT49F040-90PI AT49F040-90TI	32J 32P6 32T	Industrial (-40° to 85°C)
120	50	0.1	AT49F040-12JC AT49F040-12PC AT49F040-12TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT49F040-12JI AT49F040-12PI AT49F040-12TI	32J 32P6 32T	Industrial (-40° to 85°C)
150	50	0.1	AT49F040-15JC AT49F040-15PC AT49F040-15TC	32J 32P6 32T	Commercial (0° to 70°C)
	50	0.3	AT49F040-15JI AT49F040-15PI AT49F040-15TI	32J 32P6 32T	Industrial (-40° to 85°C)

Note: 1. The AT49F040 has as optional boot block feature. The part number shown in the Ordering Information table is for devices with the boot block in the lower address range (i.e., 00000H to 03FFFH). Users requiring the boot block to be in the higher address range should contact Atmel.

Package Type	
32J	32 Lead, Plastic, J-Leaded Chip Carrier Package (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

4 Megabit (256K x 16) 5-volt Only CMOS Flash Memory

Preliminary

Features

- Single Voltage Operation
  - 5V Read
  - 5V Reprogramming
- Fast Read Access Time - 90 ns
- Internal Erase/Program Control
- Sector Architecture
  - One 8K Words (16K bytes) Boot Block with Programming Lockout
  - Two 8K Words (16K bytes) Parameter Blocks
  - One 232K Words (464K bytes) Main Memory Array Block
- Fast Sector Erase Time - 10 seconds
- Word-By-Word Programming - 50 µs/Word
- Hardware Data Protection
- DATA Polling For End Of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 300 µA CMOS Standby Current
- Typical 10,000 Write Cycles

Description

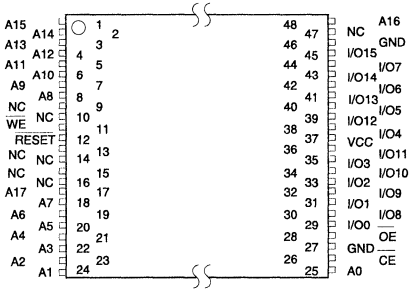
The AT49F4096 is a 5-volt-only, 4 megabit Flash Memory organized as 256K words of 16 bits each. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 275 mW. When deselected, the CMOS standby current is less than 300 µA.

(continued)

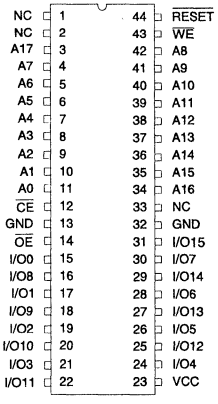
Pin Configurations

Pin Name	Function
A0 - A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$	Reset
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

TSOP Top View
Type 1



SOIC (SOP)



0569C

Description (Continued)

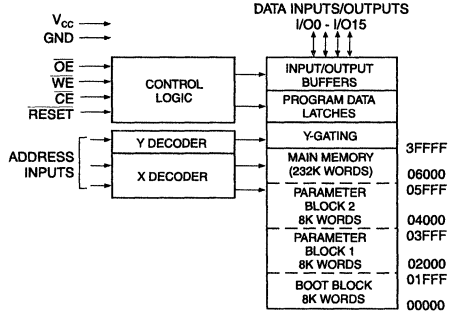
To allow for simple in-system reprogrammability, the AT49F4096 does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs to avoid bus contention. Reprogramming the AT49F4096 is performed by first erasing a block of data and then programming on a word-by-word basis.

The device is erased by executing the erase command sequence; the device internally controls the erase operation. The memory is divided into three blocks for erase operations. There are two 8K word parameter block sections and one sector consisting of the boot block and the main memory array block. The AT49F4096 is programmed on a word-by-word basis.

The device has the capability to protect the data in the boot block; this feature is enabled by a command sequence. Once the boot block programming lockout feature is enabled, the data in the boot block cannot be changed when input levels of 5.5 volts or less are used. The typical number of program and erase cycles is in excess of 10,000 cycles.

The optional 8K word boot block section includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is protected from being reprogrammed.

Block Diagram



Device Operation

READ: The AT49F4096 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the Read or Standby mode, depending upon the state of the control inputs. By applying a 12V ± 0.5V input signal to the $\overline{RESET}$ pin the boot block array can be reprogrammed even if the boot block program lockout feature has been enabled (see Boot Block Programming Lockout Override section).

ERASURE: Before a word can be reprogrammed, it must be erased. The erased state of the memory bits is a logical "1". The entire device can be erased at one time by using a 6-byte software code.

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC}.

(continued)

Device Operation (Continued)

CHIP ERASE: If the boot block lockout has been enabled, the Chip Erase function is disabled; sector erases for the parameter blocks and main memory block will still operate. After the full chip erase the device will return back to read mode. Any command during chip erase will be ignored.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into three sectors that can be individually erased. There are two 8K word parameter block sections and one sector consisting of the boot block and the main memory array block. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched at the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together (from the same sector erase command). Once the boot region has been protected, only the main memory array sector will erase when its sector erase command is issued.

WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical "0") on a word-by-word basis. Programming is accomplished via the internal device command register and is a 4 bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K words. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000H to 01FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed when input levels of 5.5V or less are used. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been enabled and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

BOOT BLOCK PROGRAMMING LOCKOUT OVERRIDE: The user can override the boot block programming lockout by taking the $\overline{RESET}$ pin to 12 volts. By doing this protected boot block data can be altered through a chip erase, sector erase or word programming. When the $\overline{RESET}$ pin is brought back to TTL levels the boot block programming lockout feature is again active.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49F4096 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT49F4096 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

(continued)

Device Operation (Continued)

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F4096 in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

Command Definition (in Hex) (1)

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA (4, 5)	30
Word Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout (2)	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit (3)	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit (3)	1	xxxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
2. The 8K word boot sector has the address range 00000H to 01FFFH.
3. Either one of the Product ID Exit commands can be used.
4. SA = sector addresses:
   SA = 03XXX for PARAMETER BLOCK 1
   SA = 05XXX for PARAMETER BLOCK 2
   SA = 3FXXX for MAIN MEMORY ARRAY
5. When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together (from the same sector erase command). Once the boot region has been protected, only the main memory array sector will erase when its sector erase command is issued.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49F4096-90	AT49F4096-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	D_{OUT}
Program/Erase (2)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	V_{IH}	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}		
Program Inhibit	X	V_{IL}	X	V_{IH}		
Output Disable	X	V_{IH}	X	V_{IH}		High Z
Reset	X	X	X	V_{IL}	X	High Z
Product Identification						
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A1 - A17 = VIL, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
					A1 - A17 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				V_{IH}	A0 = V_{IL}, A1 - A17 = V_{IL}	Manufacturer Code (4)
					A0 = V_{IH}, A1 - A17 = V_{IL}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 92H
5. See details under Software Product Identification Entry/Exit.

DC Characteristics

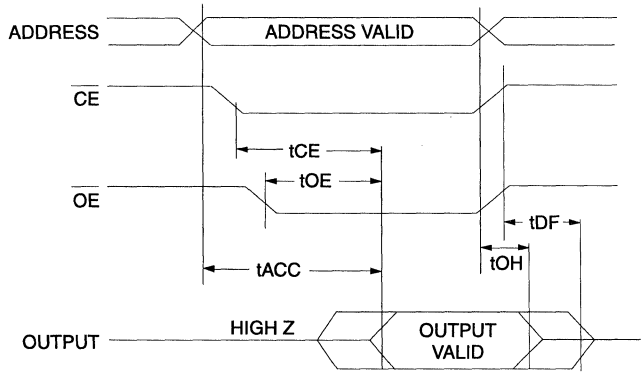
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		3	mA
I_{CC} (1)	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

Note: 1. In the erase mode, I_{CC} is 90 mA.

AC Read Characteristics

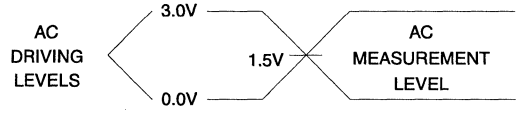
Symbol	Parameter	AT49F4096-90 Min	AT49F4096-90 Max	AT49F4096-12 Min	AT49F4096-12 Max	Units
t_{ACC}	Address to Output Delay		90		120	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms (1, 2, 3, 4)



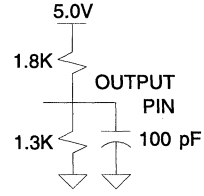
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

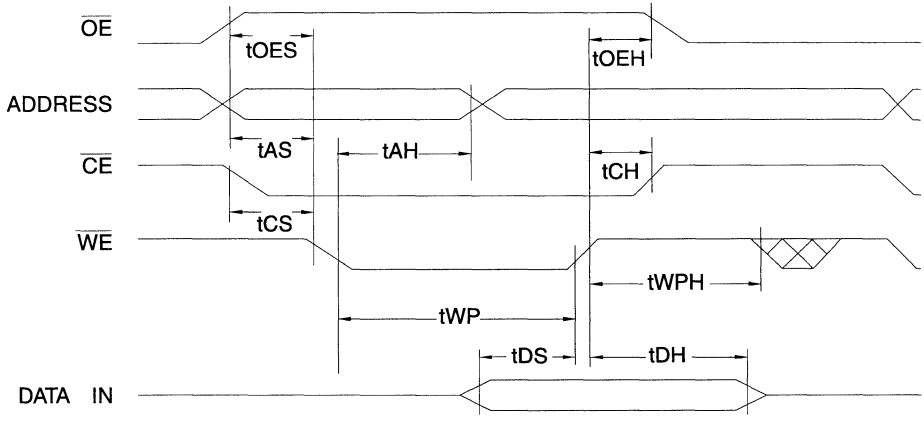
Note: 1. This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

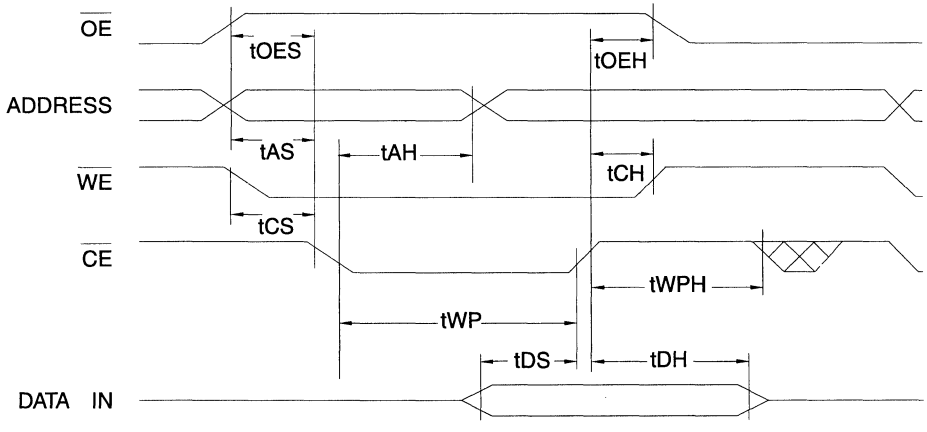
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	90		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



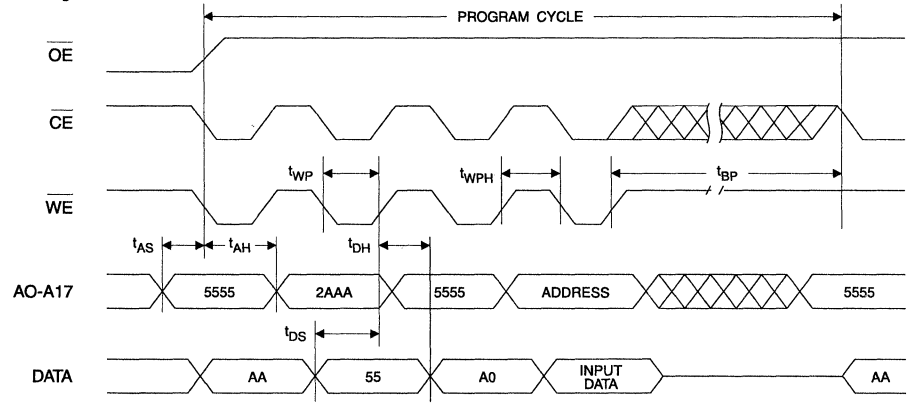
$\overline{CE}$ Controlled



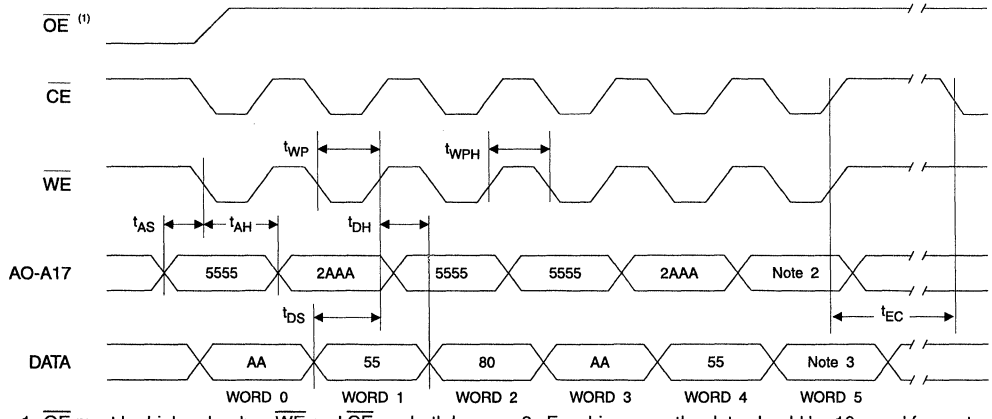
Program Cycle Characteristics

Symbol	Parameter	Min	Max	Units
t_{BP}	Word Programming Time		50	µs
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	90		ns
t_{WPH}	Write Pulse Width High	90		ns
t_{EC}	Erase Cycle Time		10	seconds

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



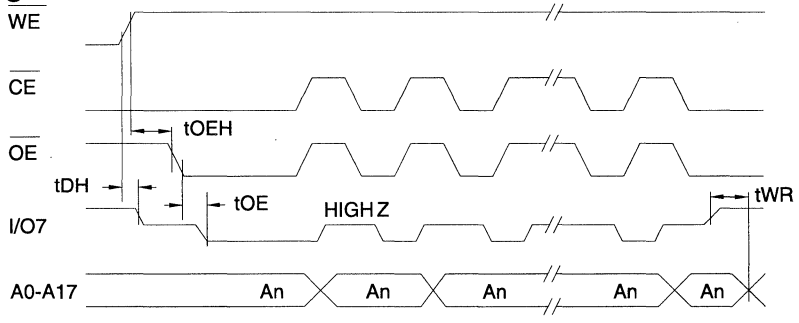
Note: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 4 under command definitions.)
3. For chip erase, the data should be 10_H, and for sector erase, the data should be 30_H.

$\overline{\text{Data}}$ Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

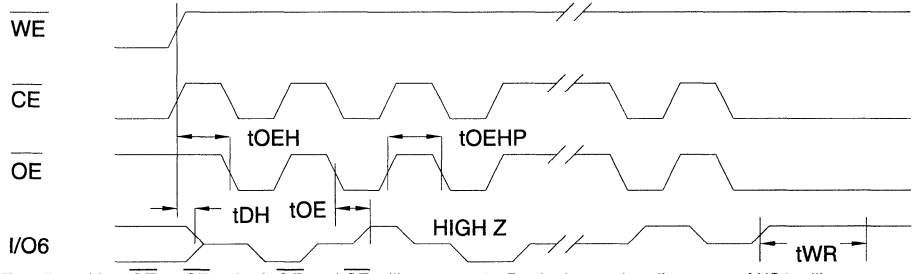


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

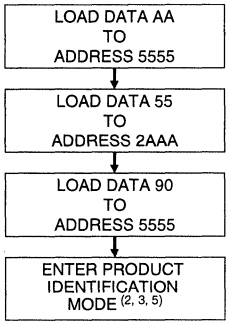
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms (1, 2, 3)

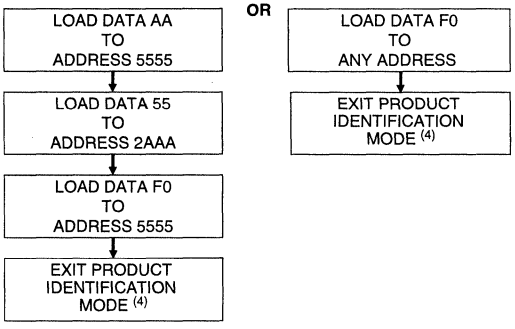


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

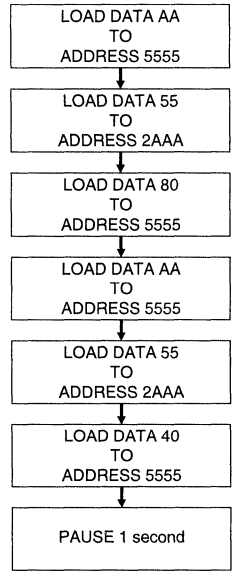


Software Product Identification Exit [1, 6]



Notes for software product identification:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A14 - A0 (Hex).
2. A1 - A17 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 92H
6. Either one of the Product ID Exit commands can be used.

Boot Block Lockout Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A14 - A0 (Hex).
2. Boot block lockout feature enabled.

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	50	0.3	AT49F4096-90TC AT49F4096-90RC	48T 44R	Commercial (0° to 70°C)
	50	0.3	AT49F4096-90TI AT49F4096-90RI	48T 44R	Industrial (-40° to 85°C)
120	50	0.3	AT49F4096-12TC AT49F4096-12RC	48T 44R	Commercial (0° to 70°C)
	50	0.3	AT49F4096-12TI AT49F4096-12RI	48T 44R	Industrial (-40° to 85°C)

Note: 1. The AT49F4096 has as optional boot block feature. The part number shown in the Ordering Information table is for devices with the boot block in the lower address range (i.e., 00000H to 01FFFH). Users requiring the boot block to be in the higher address range should contact Atmel.

4

Package Type	
48T	48 Lead, Thin Small Outline Package (TSOP)
44R	44 Lead, 0.525" Wide, Plastic Gull Wing Small Outline Package (SOIC)

Features

- Single Voltage Operation
  - 5V Read
  - 5V Reprogramming
- Fast Read Access Time - 120 ns
- Internal Program Control and Timer
- 16K bytes Boot Block With Lockout
- Fast Chip Erase Cycle Time - 10 seconds
- Byte-By-Byte Programming - 50 µs/Byte Maximum
- Hardware Data Protection
- DATA Polling For End Of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 100 µA CMOS Standby Current
- Typical 10,000 Write Cycles

8 Megabit (1M x 8) 5-volt Only CMOS Flash Memory

4

Preliminary

Description

The AT49F008 is a 5-volt-only in-system Flash Memory. Its 8 megabits of memory is organized as 1,024,576 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 120 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA.

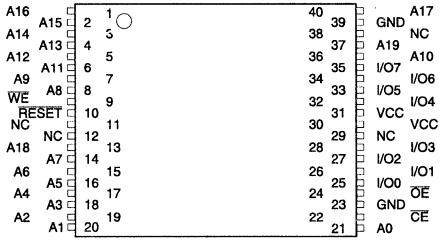
To allow for simple in-system reprogrammability, the AT49F008 does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT49F008 is performed by erasing the entire 8 megabits of memory and then programming on a byte-by-byte basis. The maximum byte programming time is a fast 50 µs. The end of a program cycle can be optionally detected by the DATA polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

The optional 16K bytes boot block section includes a reprogramming write lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

Pin Configurations

Pin Name	Function
A0 - A19	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$	Reset
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

TSOP Top View
Type 1



0604A

8 Megabit (512K x 16) 5-volt Only CMOS Flash Memory

Preliminary

4

Features

- Single Voltage Operation
  - 5V Read
  - 5V Reprogramming
- Fast Read Access Time - 90 ns
- Internal Erase/Program Control
- Sector Architecture
  - One 8K Words (16K bytes) Boot Block with Programming Lockout
  - Two 8K Words (16K bytes) Parameter Blocks
  - One 488K Words (976K bytes) Main Memory Array Block
- Fast Sector Erase Time - 10 seconds
- Word-By-Word Programming - 50 µs/Word
- Hardware Data Protection
- DATA Polling For End Of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 300 µA CMOS Standby Current
- Typical 10,000 Write Cycles

Description

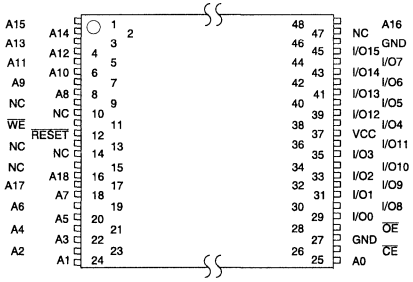
The AT49F8192 is a 5-volt-only, 8 megabit Flash Memory organized as 512K words of 16 bits each. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 275 mW. When deselected, the CMOS standby current is less than 300 µA.

(continued)

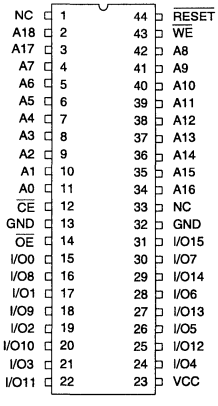
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$	Reset
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

TSOP Top View
Type 1



SOIC (SOP)



0588C

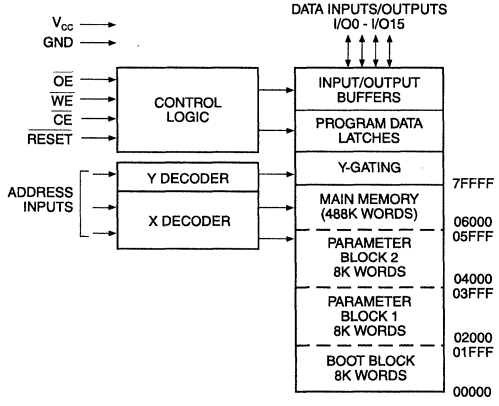
Description (Continued)

To allow for simple in-system reprogrammability, the AT49F8192 does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs to avoid bus contention. Reprogramming the AT49F8192 is performed by first erasing a block of data and then programming on a word-by-word basis.

The device is erased by executing the erase command sequence; the device internally controls the erase operation. The memory is divided into three blocks for erase operations. There are two 8K word parameter block sections and one sector consisting of the boot block and the main memory array block. The AT49F8192 is programmed on a word-by-word basis. The device has the capability to protect the data in the boot block; this feature is enabled by a command sequence. Once the boot block programming lockout feature is enabled, the data in the boot block cannot be changed when input levels of 5.5 volts or less are used. The typical number of program and erase cycles is in excess of 10,000 cycles.

The optional 8K word boot block section includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

Block Diagram



Device Operation

READ: The AT49F8192 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the Read or Standby mode, depending upon the state of the control inputs. By applying a 12V ± 0.5V input signal to the $\overline{RESET}$ pin the boot block array can be reprogrammed even if the boot block program lockout feature has been enabled (see Boot Block Programming Lockout Override section).

ERASURE: Before a word can be reprogrammed, it must be erased. The erased state of the memory bits is a logical "1". The entire device can be erased at one time by using a 6-byte software code.

(continued)

Device Operation (Continued)

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC}.

CHIP ERASE: If the boot block lockout has been enabled, the Chip Erase function is disabled; sector erases for the parameter blocks and main memory block will still operate. After the full chip erase the device will return back to read mode. Any command during chip erase will be ignored.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into three sectors that can be individually erased. There are two 8K word parameter block sections and one sector consisting of the boot block and the main memory array block. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched at the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together (from the same sector erase command). Once the boot region has been protected, only the main memory array sector will erase when its sector erase command is issued.

WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical "0") on a word-by-word basis. Programming is accomplished via the internal device command register and is a 4 bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified tBP cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K words. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000H to 01FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed when input levels of 5.5V or less are used. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been enabled and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

BOOT BLOCK PROGRAMMING LOCKOUT OVERRIDE: The user can override the boot block programming lockout by taking the $\overline{RESET}$ pin to 12 volts. By doing this protected boot block data can be altered through a chip erase, sector erase or word programming. When the $\overline{RESET}$ pin is brought back to TTL levels the boot block programming lockout feature is again active.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49F8192 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT49F8192 provides another method for determining the end of a program or erase cycle. During a program or

(continued)

Device Operation (Continued)

erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F8192 in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

Command Definition (in Hex) (1)

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA (4, 5)	30
Word Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout (2)	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit (3)	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit (3)	1	xxxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
2. The 8K word boot sector has the address range 00000H to 01FFFH.
3. Either one of the Product ID Exit commands can be used.
4. SA = sector addresses:
   SA = 03XXX for PARAMETER BLOCK 1
   SA = 05XXX for PARAMETER BLOCK 2
   SA = 7FXXX for MAIN MEMORY ARRAY
5. When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together (from the same sector erase command). Once the boot region has been protected, only the main memory array sector will erase when its sector erase command is issued.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49F8192-90	AT49F8192-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	D_{OUT}
Program/Erase (2)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	V_{IH}	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}		
Program Inhibit	X	V_{IL}	X	V_{IH}		
Output Disable	X	V_{IH}	X	V_{IH}		High Z
Reset	X	X	X	V_{IL}	X	High Z
Product Identification						
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A1 - A18 = VIL, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
					A1 - A18 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)				V_{IH}	A0 = V_{IL}, A1 - A18 = V_{IL}	Manufacturer Code (4)
					A0 = V_{IH}, A1 - A18 = V_{IL}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: A0H
5. See details under Software Product Identification Entry/Exit.

DC Characteristics

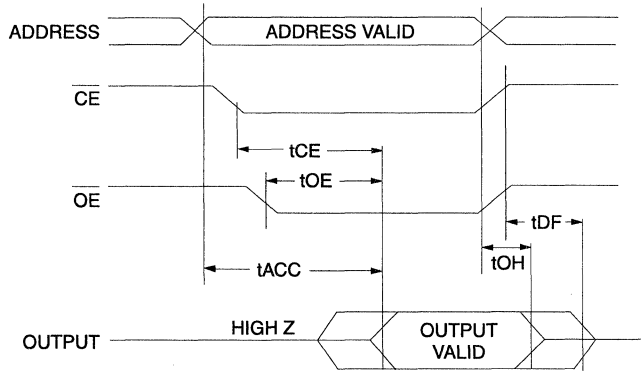
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		3	mA
I_{CC} (1)	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

Note: 1. In the erase mode, I_{CC} is 90 mA.

AC Read Characteristics

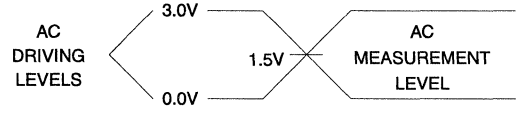
Symbol	Parameter	AT49F8192-90		AT49F8192-12		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms (1, 2, 3, 4)



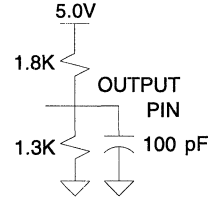
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

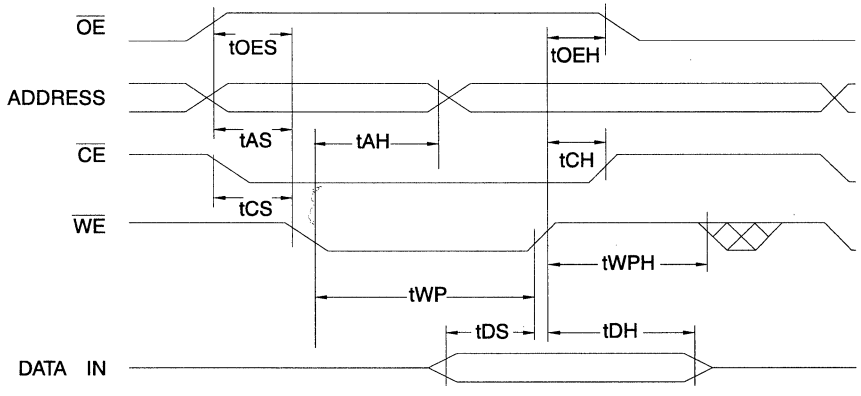
Note: 1. This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

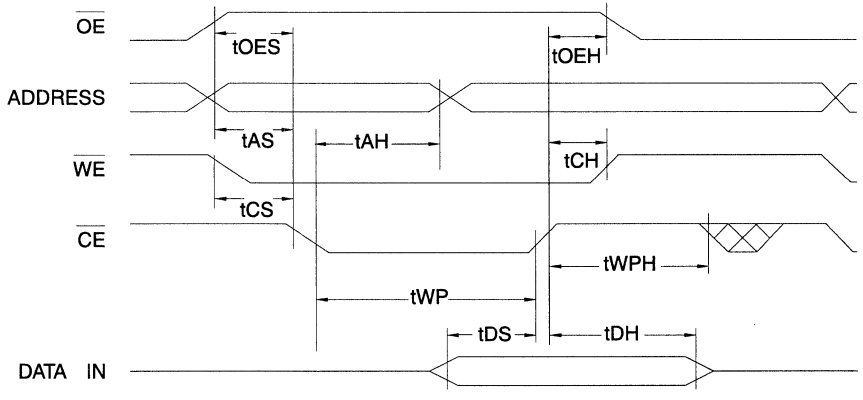
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	90		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



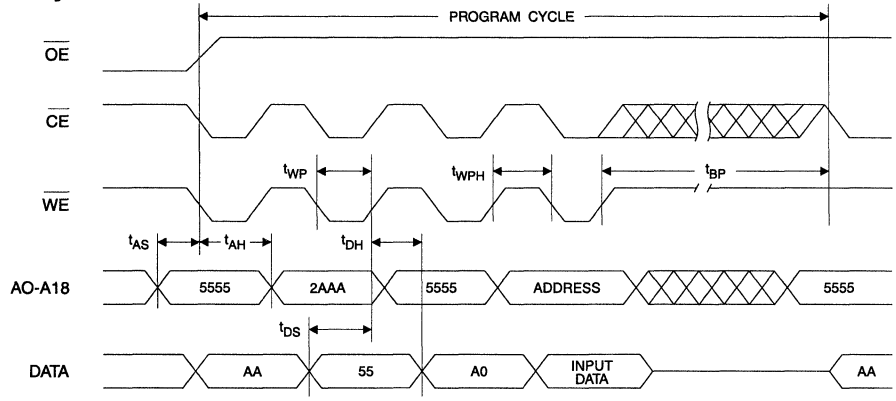
$\overline{CE}$ Controlled



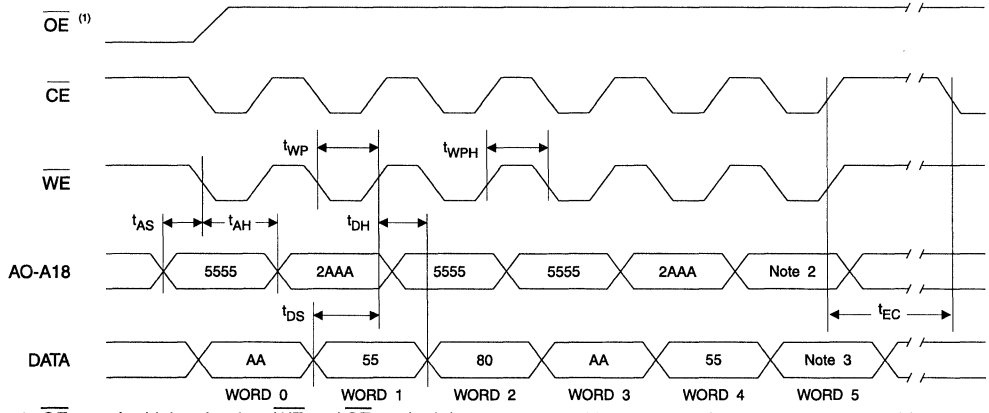
Program Cycle Characteristics

Symbol	Parameter	Min	Max	Units
t_{BP}	Word Programming Time		50	µs
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	90		ns
t_{WPH}	Write Pulse Width High	90		ns
t_{EC}	Erase Cycle Time		10	seconds

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



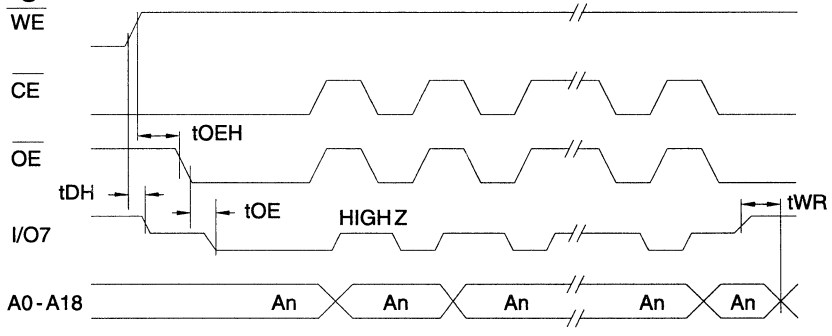
Notes: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 4 under command definitions.)
3. For chip erase, the data should be 10_H, and for sector erase, the data should be 30_H.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

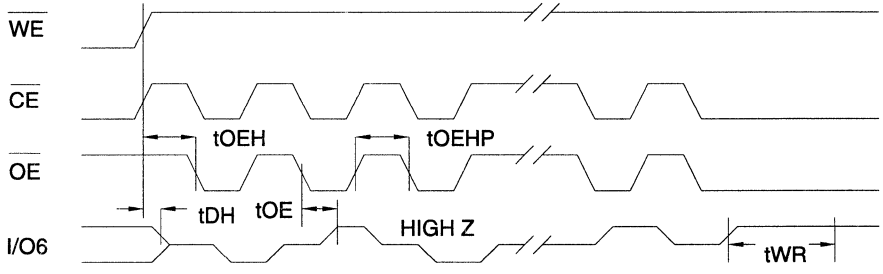


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

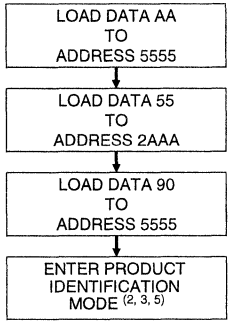
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]

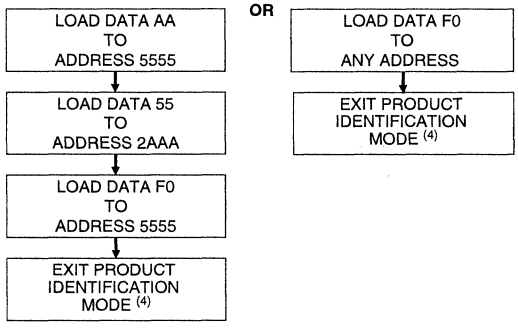


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

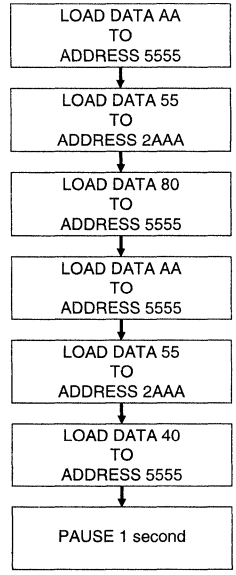


Software Product Identification Exit [1, 6]



Notes for software product identification:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A14 - A0 (Hex).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: A0H
6. Either one of the Product ID Exit commands can be used.

Boot Block Lockout Enable Algorithm [1]



Notes for boot block lockout feature enable:
1. Data Format: I/O15 - I/O8 (Don't Care);
   I/O7 - I/O0 (Hex) Address Format: A14 - A0 (Hex).
2. Boot block lockout feature enabled.

Ordering Information [1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	50	0.3	AT49F8192-90TC AT49F8192-90RC	48T 44R	Commercial (0° to 70°C)
	50	0.3	AT49F8192-90TI AT49F8192-90RI	48T 44R	Industrial (-40° to 85°C)
120	50	0.3	AT49F8192-12TC AT49F8192-12RC	48T 44R	Commercial (0° to 70°C)
	50	0.3	AT49F8192-12TI AT49F8192-12RI	48T 44R	Industrial (-40° to 85°C)

Note: 1. The AT49F8192 has as optional boot block feature. The part number shown in the Ordering Information table is for devices with the boot block in the lower address range (i.e., 00000H to 01FFFH). Users requiring the boot block to be in the higher address range should contact Atmel.

4

Package Type	
48T	48 Lead, Thin Small Outline Package (TSOP)
44R	44 Lead, 0.525" Wide, Plastic Gull Wing Small Outline Package (SOIC/SOP)

Atmel AT29 Flash Memories

Introduction

As the industry recognizes the benefits of field reprogrammability for systems, the need for a cost effective, easy to update non-volatile memory arises. To fill this role, Flash memory devices have shown great promise to become the memory of choice. But, as with the early days of EPROM and E^2PROM devices, there is much confusion about what features and voltages the ideal Flash memory device should contain. The ideal Flash device provides the designer the cleanest hardware implementation, requiring the fewest number of external components. In addition the device should provide the software designer with the highest level of flexibility, yet very simple and straightforward commands for programming. Atmel has developed their Flash memories with these ideas in mind.

Atmel Flash memories (programmable erasable read-only memories) are implemented on an advanced sub-micron process using a highly efficient memory cell to store each bit of data. Unlike first generation Flash memories, Fowler-Nordheim tunneling is used in both the erasing and programming of the memory cell. This programming method requires only nanoamps of high voltage (15V to 20V) programming current, allowing the use of an on-chip charge pump to generate the necessary programming voltages. The low programming current also permits sector programming. Typical first generation Flash devices are made with EPROM cell structures which use hot electron injection for programming. Hot electron injection typically requires several milliamps of high voltage programming current. This current requirement is why multiple external voltages are required for programming and why only one byte at a time can be programmed for first generation Flash devices.

Flash Memory Device Features

The Atmel AT29 family of Flash PEROM devices consists of five capacities ranging from 256K to 4 megabit. All devices are single voltage, either 3-volt-only or 5-volt-only, and can be programmed using the same deterministic (i.e., fixed maximum time) programming algorithm.

The Atmel AT29 Flash memory devices are all designed as large memory arrays

(continued)

Table 1. Atmel AT29 Series Flash Memory Devices

Devices		Memory Size	Number of Sectors	Sector Size (bytes)	Manufacturer ID	Device ID	
5V	3V					5V	3V
AT29C256/7	AT29LV256/7	32K x 8	512	64	1F	DC	BC
AT29C512	AT29LV512	64K x 8	512	128	1F	5D	3D
AT29C010A	AT29LV010A	128K x 8	1024	128	1F	D5	35
AT29C1024	AT29LV1024	64K x 16	512	128 (1)	1F	25	26
AT29C020	AT29LV020	256K x 8	1024	256	1F	DA	BA
AT29C040A	AT29LV040A	512K x 8	2048	256	1F	A4	C4

Note: 1. 128 Words.

Flash Programmable Erasable ROM

Application Note

(AN-1)

4

0572A

Flash PEROM Device Features (Continued)

broken up into small individually reprogrammable sectors. For example, the AT29C010A (128K x 8) is divided into 1024 sectors of 128-bytes. Table 1 describes this organization for each AT29 Flash PEROM device.

Key features are implemented on a Flash memory to improve system performance and simplify hardware and software development, as described below:

Small Sectors

Atmel AT29 Flash memories are organized into small sectors for reprogramming. Unlike first generation devices that require erasing large blocks of memory before reprogramming (at least several thousand bytes to as much as the entire chip capacity), Atmel's sector organization allows for fast and easy data updates. Each sector's contents may be altered independently by simply loading new data into the on-chip sector buffer, at full bus speed, then waiting 10 to 20 ms while the chip's built-in sequencer programs the contents of the newly loaded buffer into the array. No pre-erase is required. When only a small portion of the total memory must be altered, the small sector approach saves considerable time. It also eliminates the need for large system buffer memory space to hold unchanging information that would have to be copied out of a large area of the Flash component and rewritten back into it after the small portion is updated. These differences can be very significant: Write time for the Atmel Flash PEROM is always 10 ms per sector (20 ms for 3-volt write), while write time for large-sectored or whole chip Flash devices is variable and can extend to several minutes. The several-hundred-byte Flash memory sector typically requires no additional buffering, while the large sector devices require tens to hundreds of Kbytes of system memory or extra hardware memory to contain not-to-be-changed memory contents during the mandatory pre-erase activity.

Data Protection

The Atmel Flash memory has both hardware and software data protection on-chip to prevent the contents of memory from being inadvertently altered. The following five mechanisms exist on each Flash memory:

1. **Noise Filter:** All control line inputs have filtering circuitry to eliminate any noise spikes less than 15 ns in duration.
2. **V_{CC} sense:** If V_{CC} falls below 3.8 volts, (typical), programming will be inhibited. For LV (low voltage) devices V_{CC} sense is typically 1.8 volts.
3. **Power on Delay:** When V_{CC} rises above the V_{CC} sense level a 5-ms timer is started which will inhibit programming until it has completed its time-out, allowing all system power transients to settle and initialization routines to proceed without disturbing the Flash PEROM contents.
4. **Three-Line Control:** To initiate a write cycle all three control lines must be in the correct state. If $\overline{OE}$ is not high, or $\overline{CE}$ is not low, or if $\overline{WE}$ is not low a write cycle will be inhibited.
5. **Software Data Protection (SDP):** This protection mechanism is the only one that may be optionally activated or disabled under software control. When it is activated, the Flash memory requires a specific 3-byte temporary unlock write sequence prior to each sector load cycle to enable programming. If a sector load cycle is executed without the 3-byte write sequence, no information will be altered and the device will lock out all activity, (reads and writes), for 10 ms. Activation is accomplished by the first occurrence of the specific 3-byte temporary unlock write sequence. Thereafter, all sector writes must be preceded by the same 3-byte write sequence. SDP can be explicitly disabled by a specific 6-byte write sequence.

Product ID

Built into every Flash memory is the ability to interrogate the device to determine the manufacturer and device type. Simply write the proper 3-byte code into the device, wait the write cycle time (t_{WC}), and read from locations 0000H and 0001H. No special voltages are required. Reading from location 0000H will access the manufacturer code. All Atmel devices read 1F. Reading from location 0001H will access the device ID code. See Table 1 for the device ID codes for each Flash device. Note that device ID codes are different for the standard 5-volt parts and for the 3-volt (LV) devices. Product ID information can also be accessed by applying a 12-volt signal to pin A9. This is available to maintain compatibility with high voltage Flash or EPROMs when used with external programming hardware.

Data Polling

Maximum programming time for a Flash memory is specified as 10 ms, (20 ms for LV devices). Typically, this programming time is only 5 to 7 ms, (10 to 15 ms for LV devices). To take advantage of this typical programming time and to speed up the overall programming process, a data polling feature is available in the Flash memory device. To utilize this feature, the user must read from the final address written following a sector write. During programming, Bit 7 will be inverted from the state in which it was written. When a read produces true data on all outputs, the programming process is complete. The device is then ready for the next operation.

(continued)

Flash PEROM Device Features (Continued)

Toggle Bit

An alternate method of indicating when programming is complete is to use the toggle bit. Programming completion is indicated by monitoring Bit 6 of any byte location. On successive reads from a fixed location, Bit 6 will toggle logic states during programming. When Bit 6 does not change on successive reads, the device has completed programming.

AT29 Flash Memory Programming Description

Atmel AT29 Flash memories are designed to allow all devices to be programmed using the same deterministic algorithm. As shown in the accompanying flow charts, Figure 1 through Figure 4, the user simply has to interrogate the device ID code and set the sector size. This operation need only be done once if the sector size variable is saved. The sector size variable can be hard-set in software and the device ID interrogation eliminated if only one density device will ever be used.

Following sector size determination, a sector load cycle can be initiated. The following will describe programming the 3V Flash and the 5V Flash using software data protection. Programming begins with a 3-byte sequence to temporarily unlock the software data protection, followed by loading the sector of data to the device. This sequence of activity is shown in Figure 5. If a complete sector of data is not loaded, the byte locations within the sector that were not loaded will be cleared to FF during programming. All addresses must be within the same physical sector or errors may occur. It is not necessary to load the sector buffer in any address order. A random addressing sequence is perfectly acceptable, with each byte accompanied by its address within the sector. During the sector load cycle, a maximum time of 150 µs (t_{BLC}) is allowed between successive byte loads. If this byte load time is exceeded, the device will begin programming mode prematurely.

t_{BLC} time after loading the sector, the Flash memory device will enter its programming mode. While programming, the device will ignore any further write commands and any attempt to read will output only $\overline{\text{Data}}$ Poll and toggle bit data.

Before entering into a polling loop, it is good practice to start a programming cycle watchdog timer. This will prevent your software from being caught in an endless loop if something goes wrong with programming the device.

The polling loop should consist of two operations. The first is to check status of the watchdog timer, and the second to check $\overline{\text{Data}}$ Poll data. The watchdog timer should never time-out in normal programming. If a time-out does occur, check the hardware and software for possible problems. To check $\overline{\text{Data}}$ Poll, simply read the device at the address of the last byte programmed in the sector. The data should be compared against the data that was written. When the data matches, the programming is complete.

Before going on to another operation, it is recommended to verify that the sector was properly programmed.

Summary

Programming the Atmel AT29 Flash memory is a simple process, akin to loading an SRAM. Facilities in the device minimize the software and system overhead and architectural and circuit features simplify the interface and speed performance, while improving system integrity. The programming procedures described above will insure that devices will always be properly programmed, and require only about one-tenth of the typical software, buffer memory and performance overhead of first generation Flash components.

Figure 1. Software Product Identification Entry

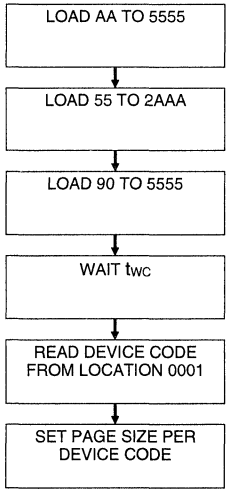


Figure 2. Software Product Identification Exit

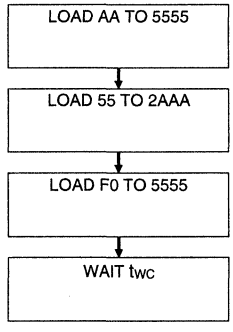


Figure 3. Page Loop

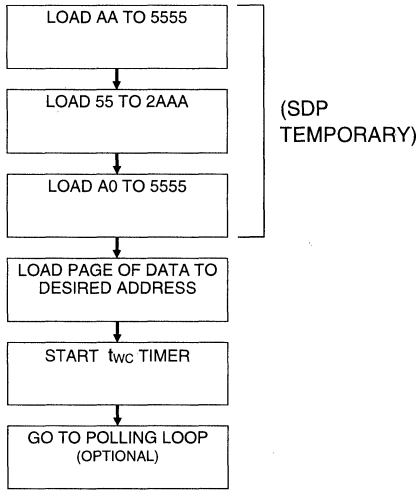


Figure 4. Polling Loop

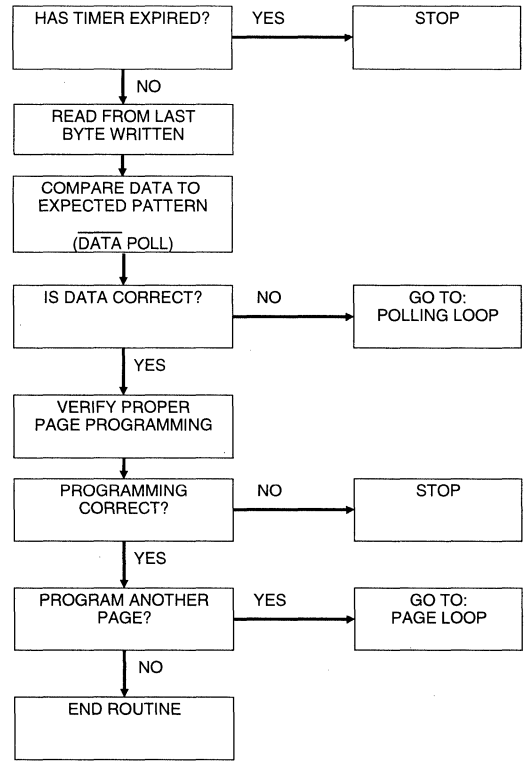
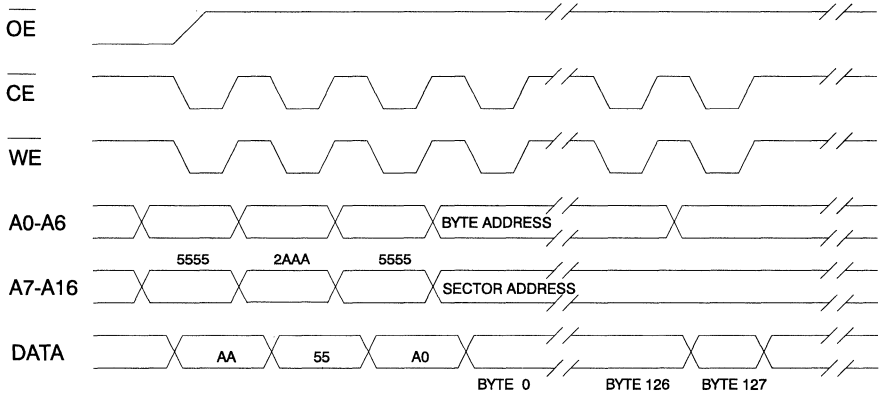


Figure 5. Timing Sequence for Protected Sector Write (AT29C010A 1M bit Example)



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A7 through A16 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. **All bytes that are not loaded within the sector being programmed will be indeterminate.**

Software Chip Erase (for AT29 Series Flash Family)

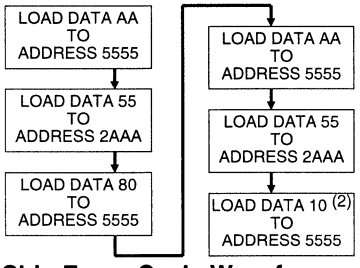
The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFH). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time required to erase the whole chip is t_{EC} (20 ms). The software data protection is still enabled even after the software chip erase is performed. If the boot block lockout feature has been eabled, the 6-byte software chip erase algorithm will not function.

Chip Erase Cycle Characteristics

Symbol	Parameter	
t_{EC}	Chip Erase Cycle Time	20 ms Max

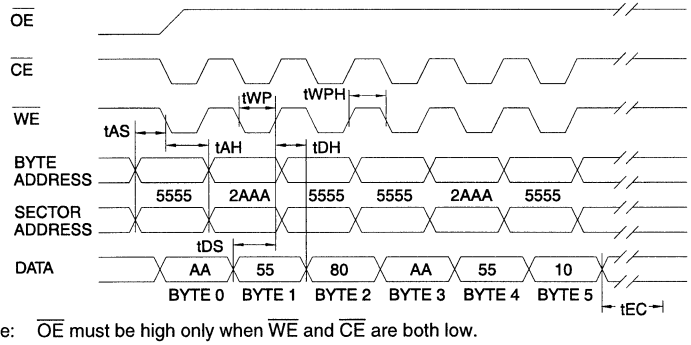
Note: Please refer to individual data sheets for the minimum and maximum values of the t_{AS}, t_{AH}, t_{DS}, t_{DH}, t_{WP}, t_{BLC}, and t_{WPH} parameters.

Chip Erase Software Algorithm (1, 3)



Notes for software erase code:
1. Data Format: (Hex); Address Format: (Hex).
2. After loading the 6-byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion in 20 ms (max).
3. The flow diagram shown is for a x8 part. For a x16 part, the data should be 16 bits long (e.g., the data to be loaded should be AAAA for step 1 in the algorithm).

Chip Erase Cycle Waveforms



Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

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Programming Atmel's AT29 Flash Family

Introduction

Atmel offers a diverse family of small sector Flash memory devices ranging in density from 256K to 4M bits. These devices read and program with a single voltage supply. The nominal supply voltage is 5V for the AT29CXXX, 3.3V for the "low voltage" AT29LVXXX, and 3V for the "Battery Voltage" AT29BVXXX Flash memory family. The entire Flash PEROM product line is designed to allow users to have one common programming algorithm for all three Flash voltage families. Therefore, upgrading from one density to another and from a higher voltage to a lower voltage device is simplified.

This application note describes the design benefits of Atmel's AT29 Flash architecture as well as how the device ID feature is used to adjust for varying densities and supply voltages. In addition, Atmel's Software Data Protection (SDP) feature, which prevents inadvertent writes, is described. An example is given to illustrate the ease with which the programming software can be written to accommodate four different 4M bit Flash devices: the AT29C040, the AT29LV040, and the newer generation Flash devices, the AT29C040A and the AT29LV040A.

Hardware and software has been developed to demonstrate the relevant design issues. The demo uses an AT89C51 Flash-based microcontroller (which has the same pinout and instruction set as an 80C51) as the host processor and a "C" language program for the software. The software automatically adjusts the amount of time required for programming the varying voltage versions of the 4M bit Flash devices in addition to accommodating for their different sector sizes.

The AT89C51, a member of Atmel's growing family of Flash microcontroller devices, features 4K bytes of in-system reprogrammable Flash memory (see Atmel application note "AT89C51 In-Circuit Programming" for additional information). Current and future versions of Atmel's microcontroller family incorporate from as little as 1K byte of Flash memory to as much as 128K bytes, providing many density options for different applications. Other versions will also include special architectures such as a combination of Flash and parallel EEPROM memory on board.

Programming Flash Devices

Unlike Atmel's Flash memories, previous generations of Flash memories had large sectors, typically 4K to 128K bytes, and required that an entire sector be erased prior to programming. Generally, the sector erase cycle time was hundreds or thousands of milliseconds and could be as long as 30 seconds for the entire memory array. In addition, a separate high voltage supply was required for a write and erase operation. Atmel's AT29 Flash memory family has simplified usage by having only one supply voltage, reducing the sector size, having the programming similar to an SRAM write operation, and decreasing significantly the total programming time.

Small sector sizes reduce the amount of system resources necessary for programming. When only a few bytes in a Flash memory need to be altered, a RAM image of the Flash sector must be created. The RAM must then be altered with the new data, and the image transferred back into the Flash device. Be-

(continued)

Programming AT29 Flash Devices (Continued)

cause Atmel's Flash devices have small sector sizes (from 64- to 512-bytes, depending on the memory density), the RAM requirements are much less than those of large sector Flash devices. Often, the system RAM available is sufficient for Atmel's Flash, whereas large sector Flash devices usually require an additional SRAM.

A second advantage of Atmel's AT29 Flash is that an entire sector can be updated during a single program operation, instead of the byte-by-byte programming of previous generation Flash memories. This saves significant programming time when updating an entire sector, especially when comparing Atmel's small sector devices with large sector devices. In addition, Atmel's devices do not require a sector erase prior to writing, thus saving additional programming time. The maximum sector program time is 10 msec for the AT29CXXX family and 20 msec for the AT29LVXXX/AT29BVXXX families.

AT29C040 and AT29C040A Architecture

The AT29C040 provides operation similar to a byte-wide SRAM. The device has eight data lines and 19 address lines. The familiar three input control lines are also present ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$). Read operations are identical to an SRAM, but write operations are somewhat different due to the write cycle time (t_{WC}) requirements of all Flash memories. Flash write operations take several milliseconds to complete, compared to the nanosecond writes of SRAM devices. It should be noted that Atmel's AT29 Flash PEROMs require only a write operation; the erase operation is automatically performed internally in the device.

Data is loaded into the AT29C040 one sector at a time, with each sector consisting of 512-bytes. The sector chosen for modification is defined by the upper order address bits (A9-A18). The entire sector must be loaded during the write operation. Any byte not loaded during the sector load will contain FF (hex) after the write operation has completed. Address lines A0 through A8 define the location of the bytes within a sector. All data must be loaded into the same sector (A9 through A18 must remain constant) and can be randomly loaded within that sector.

The AT29C040A is identical to the AT29C040 except for the sector size and the Device ID Code (the Device ID Code is described later). The AT29C040A has a 256-byte sector (instead of a 512-byte sector) which is defined by address lines A8 through A18; the bytes within the sector are determined by address lines A0 through A7.

Software Data Protection (SDP)

One concern of systems designers when using nonvolatile programmable memories is the possibility of inadvertent write operations that can be caused by noise or by power-up and power-down sequences. Atmel's Flash memories provide a feature called Software Data Protection (SDP) that addresses this issue. The user can enable SDP upon receipt of the device from Atmel, and its usage is highly recommended. Data can be written into a sector with or without SDP enabled. However, once SDP has been enabled, the device requires that all subsequent write operations perform a series of "dummy" write operations before loading the chosen sector with data. The "dummy" writes consist of loading three known data values into three predefined addresses. This 3-byte sequence preceding a write operation virtually eliminates the chance of inadvertent write operations. The sequence is described below.

1. Load Data AA (hex) into Address 05555 (hex)
2. Load Data 55 into Address 02AAA
3. Load Data A0 into Address 05555
4. Load desired sector with data
5. Pause t_{WC} (device write cycle time)
6. Continue with next operation.

If SDP is enabled, any attempt to write to the device without the 3-byte command sequence will start a write cycle. However, no data will actually be written to the device, and during this "write" cycle time (t_{WC}), valid data cannot be read from the Flash.

Product and Manufacturer ID

Atmel's Flash memory devices allow the user to access both device and manufacturer information. This feature allows a system to determine exactly which Flash memory is being used. Once this is known, the host system can choose different algorithms for write operations in order to accommodate for differences in device density, V_{CC} requirements, sector size, and required write cycle time.

Product and manufacturer ID information is determined with the Software Product Identification procedure, which is similar to the Software Data Protection sequence. The sequence is described below.

1. Load Data AA (hex) into Address 05555 (hex)
2. Load Data 55 into Address 02AAA
3. Load Data 90 into Address 05555
4. Pause t_{WC} (device write cycle time)
5. Read Address 00000
   Data read is the Manufacturer Code
6. Read Address 00001
   Data read is the Device ID Code
7. Load Data AA into Address 05555
8. Load Data 55 into Address 02AAA
9. Load Data F0 into Address 05555
10. Pause t_{WC} (device write cycle time)
11. The device is returned to standard operating mode

(continued)

Product and Manufacturer ID (Continued)

The following table uses the 4M bit Flash as an example to illustrate the pertinent device information that can be determined once the Device ID Code is known. Please refer to the table at the end of this application note for information on other Flash devices.

Device	ID	V_{CC}	Sector Size	t_{WC}
AT29C040	5B	5.0V ± 10%	512-bytes	10 ms
AT29C040A	A4	5.0V ± 10%	256-bytes	10 ms
AT29LV040	3B	3.3V ± 0.3V	512-bytes	20 ms
AT29LV040A	C4	3.3V ± 0.3V	256-bytes	20 ms
AT29BV040	3B	3.0V ± 10%	512-bytes	20 ms
AT29BV040A	C4	3.0V ± 10%	256-bytes	20 ms

Programming Demonstration

Hardware and software descriptions have been prepared to demonstrate how Atmel's AT29 Flash memories can be reprogrammed. The descriptions are provided in the following two sections. A circuit schematic of the demonstration hardware and a source code listing of the software are also included.

Hardware Description

The demo hardware consists of a 12 MHz AT89C51 Flash-based microcontroller with 4K bytes of on-board Flash memory. The internal AT89C51 Flash memory is used for boot code, and the external 8K x 8 SRAM and the AT29C040A are mapped as data memory. The AT29C040A is also mapped as program memory to facilitate off-chip program execution. The AT89C51 can only access a maximum of 64K bytes of data memory space, while the AT29C040A has 512K bytes of storage capacity. To solve this size mismatch, the AT29C040A is bank switched into the AT89C51 data memory map in 8K byte blocks. The bank switching is performed with six general purpose I/O port bits on the AT89C51. The system address map is shown below.

System Address Map

AT89C51 Microcontroller	0000-1FFF	Internal program memory
8K x 8 Static RAM	2000-3FFF	Data memory
AT29C040A Flash	4000-5FFF	Program and data memory

Software Description

The software demonstrates how the Device ID Code can be used to allow a single program to work with different Atmel Flash memories. The program uses Atmel's 4M bit Flash (AT29C040, AT29LV040, AT29C040A, and AT29LV040A) as an example, but the software can be easily adapted to accommodate other device densities.

In order to program the Flash memory, the software must first determine which Flash device is being used. This is accomplished by first putting the device into the Software Product Identification mode (described in the "Product and Manufacturer ID" section of this application note). The program subsequently reads the Device ID Code and executes the 3-byte command sequence to return the Flash to the standard operating mode. Using the Device ID Code, the program then determines the appropriate sector size and write cycle time (t_{WC}) for the particular 4M bit Flash being used.

To demonstrate a sector write, the program proceeds to load the SRAM with "dummy" data. After the data has been loaded, the program transfers the data from the SRAM to a predefined sector (within one of the mapped 8K byte blocks) of the 4M bit Flash. After pausing the required write cycle time (t_{WC}), the sector that was just written is transferred back to the SRAM buffer.

Summary

Atmel's AT29 Flash memories are designed to allow all densities and device configurations to be programmed using the same programming algorithm. The user has to simply determine the Device ID Code and set the appropriate sector size and write cycle time. This operation need only be performed once provided the sector size and write cycle information is saved. If only one density or configuration will ever be used, then reading of the Device ID Code can be eliminated, and the sector size and write cycle information can be predefined in the software. The table at the end of this application note details the device information and the Device ID Codes for Atmel's AT29XXX Series of Flash PEROMs.

As demonstrated, programming Atmel's AT29 Flash is a simple process, similar to loading an SRAM. Architectural and circuit features within the devices minimize software and system overhead while simplifying programming procedures. Atmel's AT29 Flash memories require only about one-tenth of the typical software, buffer memory, and performance overhead of previous generation Flash, thus providing substantial system cost savings.

Atmel AT29 Flash Memories

Device	Memory Size	Device ID Code	Number Of Sectors	Sector Size	Write Cycle Time (t_{wc})	Comments
AT29C256	32K x 8	DC	512	64-bytes	10 ms	
AT29LV256	32K x 8	BC	512	64-bytes	20 ms	
AT29C257	32K x 8	DC	512	64-bytes	10 ms	
AT29C512	64K x 8	5D	512	128-bytes	10 ms	
AT29LV512	64K x 8	3D	512	128-bytes	20 ms	
AT29C010A	128K x 8	D5	1024	128-bytes	10 ms	
AT29LV010A	128K x 8	35	1024	128-bytes	20 ms	
AT29BV010A	128K x 8	35	1024	128-bytes	20 ms	
AT29C1024	64K x 16	25	512	128-words	10 ms	
AT29LV1024	64K x 16	26	512	128-words	20 ms	
AT29C020	256K x 8	DA	1024	256-bytes	10 ms	
AT29LV020	256K x 8	BA	1024	256-bytes	20 ms	
AT29BV020	256K x 8	BA	1024	256-bytes	20 ms	
AT29C040	512K x 8	5B	1024	512-bytes	10 ms	Use **AT29C040A** for new designs
AT29LV040	512K x 8	3B	1024	512-bytes	20 ms	Use **AT29LV040A** for new designs
AT29BV040	512K x 8	3B	1024	512-bytes	20 ms	Use **AT29BV040A** for new designs
AT29C040A	512K x 8	A4	2048	256-bytes	10 ms	
AT29LV040A	512K x 8	C4	2048	256-bytes	20 ms	
AT29BV040A	512K x 8	C4	2048	256-bytes	20 ms	

```
/*****************************************************************/
/* This program demonstrates how a sector in one of the 512K X 8 */
/* variants can be programmed.  The program first determines     */
/* exactly which device is available by reading the device ID.   */
/* A sector is then programed with data that is copied from an   */
/* SRAM buffer.  After waiting for the programming cycle to      */
/* complete the data is copied back from the 29C040 to the SRAM  */
/* buffer.                                                       */
/*                                                               */
/* The sector size and programming time are determined    */
/* by examining the device ID.  The different 512K X 8 devices   */
/* have either a 256- or 512-byte sector size and a 10 mS or 20  */
/* mS tWC.                                                       */
/*****************************************************************/

/***********************/
/* COMPILER DIRECTIVES */
/***********************/

        .asm
        .linklist
        .symbols
        .endasm

#include        "c8051sr.h"

/********************/
/* GLOBAL VARIABLES */
/********************/

unsigned char part_id;                  /* DEVICE ID VALUE */
int sector_size;                        /* DEVICE SECTOR SIZE */
int twc;                                /* DEVICE PROGRAMMING TIME REQUIRED */
unsigned char data_buffer[512];         /* SRAM DATA BUFFER */
unsigned char block_number;             /* WHICH BLOCK TO PROGRAM */
unsigned int sector_address;            /* ADDRESS WITHIN SECTOR TO PROGRAM */
unsigned int address_pointer;           /* SCRATCH PAD ADDRESS REGISTER */
unsigned char temp_byte;                /* SCRATCH PAD DATA REGISTER */

/***********************/
/* SUPPORT SUBROUTINES */
/***********************/

/*********************************************************************/
/* DELAYMS performs a time delay.  The variable ticks indicates the */
/* length of the delay in mS.  This routine is dependant upon the   */
/* clock rate of the 89C51.  If a clock rate other than 12 MHz is   */
/* used the variable 'count' must be modified.                      */
/*********************************************************************/

void delayms(char ticks)

{
char count;

  for (ticks = ticks; ticks >= 0; ticks--)
  {
      for (count = 0; count <= 13; count++)
      {
```

```
      }
  }
}

/*****************************************************************/
/* ENTER_ID_MODE is used to put the 29C040 into Software Product */
/* Identification mode.  The three step sequence is performed in */
/* assembly because of tBLC requirements of the 29C040.          */
/*****************************************************************/

void enter_id_mode()

{
  .asm
  mov   a,#05h
  mov   p1,a
  mov   dptr,#4555h
  mov   a,#aah
  movx  @dptr,a                         ;write AAh to address 05555h
  mov   a,#02h
  mov   p1,a
  mov   dptr,#4aaah
  mov   a,#55h
  movx  @dptr,a                         ;write 55h to address 02AAAh
  mov   a,#05h
  mov   p1,a
  mov   dptr,#4555h
  mov   a,#90h
  movx  @dptr,a                         ;write 90h to address 05555h
  .endasm
}

/*****************************************************************/
/* LEAVE_ID_MODE is used to remove the 29C040 from Software Product */
/* Identification mode.  The three step sequence is performed in    */
/* assembly because of tBLC requirements of the 29C040.             */
/*****************************************************************/

void leave_id_mode()

{
  .asm
  mov   a,#05h
  mov   p1,a
  mov   dptr,#4555h
  mov   a,#aah
  movx  @dptr,a                         ;write AAh to address 05555h
  mov   a,#02h
  mov   p1,a
  mov   dptr,#4aaah
  mov   a,#55h
  movx  @dptr,a                         ;write 55h to address 02AAAh
  mov   a,#05h
  mov   p1,a
  mov   dptr,#4555h
  mov   a,#f0h
```

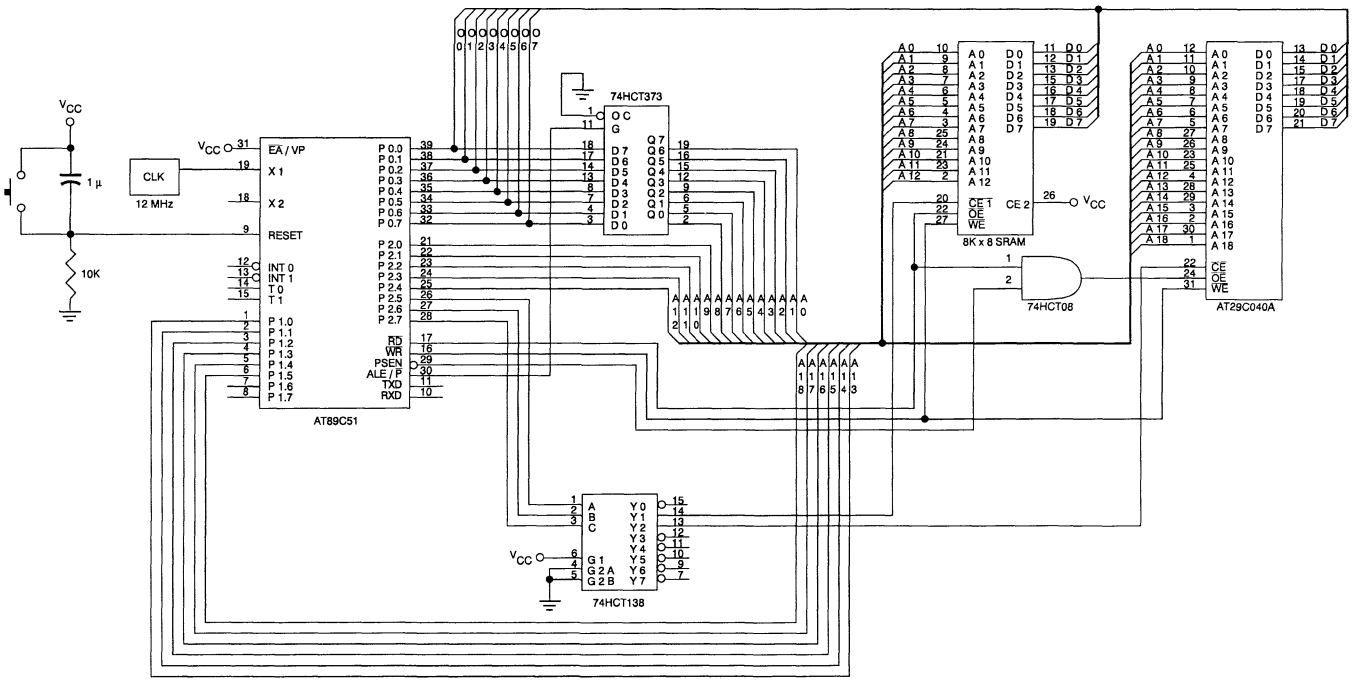
```
  movx  @dptr,a                         ;write F0h to address 05555h
  .endasm
}

/*********************************************************************/
/* GET_ID is used read the value at location 00001 of the 20C040.    */
/* The value read from the device is returned to the calling routine */
/*********************************************************************/

unsigned char get_id()

{
  P1 = 0x00;                            /* read from block 00h */
  .asm
  mov   dptr,#4001h                     ;read from address 00001h
  movx  a,@dptr                         ; (flash offset = 4000h)
  .endasm
  return(A);                            /* return data value */
}

/*********************************************************************/
/* GET_PART_ID determines the device ID of the 29C040 being used. */
/* The ID value is returned to the calling routine                   */
/*********************************************************************/

unsigned char get_part_id()

{
unsigned char part_id;

  enter_id_mode();                      /* enter Identification mode */
  delayms(20);                          /* delay 20mS */
  part_id = get_id();                   /* read device ID from address 1 */
  leave_id_mode();                      /* exit from Identification mode */
  delayms(20);                          /* delay 20mS */
  return(part_id);                      /* return device ID value */
}

/*****************************************************************/
/* SET_PARAMETERS is used to define what sector size and write   */
/* cycle is required for the particular 29C040 being used        */
/* The sector size is stored in the global variable SECTOR_SIZE, */
/* and the programming time is stored in the global variable TWC.*/
/*****************************************************************/

void set_parameters(unsigned char part_id)

{
  switch(part_id)
  {
    case 0x5b : sector_size = 512;      /* is the device a 29C040 */
                twc = 10;
                break;
    case 0xa4 : sector_size = 256;      /* is the device a 29C040A */
                twc = 10;
                break;
    case 0x3b : sector_size = 512;      /* is the device a 29LV040 */
                twc = 20;
                break;
```

```
    case 0xc4 : sector_size = 256;      /* is the device a 29LV040A */
                twc = 20;
                break;
    default   : sector_size = 0;        /* variables default to 0 */
                twc = 0;
  }
}

/*****************************************************************/
/* DUMMY_BUFFER_LOAD simply loads the SRAM buffer with the value */
/* passed in IN_VALUE.  Although the SRAM buffer has 512-bytes,  */
/* only the number of bytes required to fill a sector are loaded.*/
/*****************************************************************/

void dummy_buffer_load(char in_value)

{
int count;

  for (count = 0; count <= sector_size; count++)
  {
    data_buffer[count] = in_value;
  }
}

/*****************************************************************/
/* WRITE_SECTOR copies data from the SRAM buffer into the sector */
/* specified in the 29C040.  After loading the sector the routine*/
/* paused the required tWC for the programming cycle to complete.*/
/*****************************************************************/

void write_sector()

{
  .asm
        mov     a,#05h                  ;perform 3 step SDP sequence
        mov     p1,a
        mov     dptr,#4555h
        mov     a,#aah
        movx    @dptr,a                 ;write AAh to address 05555h
        mov     a,#02h
        mov     p1,a
        mov     dptr,#4aaah
        mov     a,#55h
        movx    @dptr,a                 ;write 55h to address 02AAAh
        mov     a,#05h
        mov     p1,a
        mov     dptr,#4555h
        mov     a,#A0h
        movx    @dptr,a                 ;write A0h to address 05555h
        mov     dptr,#_block_number
        movx    a,@dptr
        mov     P1,a                    ;set up block address
        mov     dptr,#_sector_size      ;load sector size
        movx    a,@dptr
        mov     r0,a
        inc     dptr
        movx    a,@dptr
        mov     r1,a
```

```
        mov     dptr,#_sector_address   ;load first sector address to write
        movx    a,@dptr
        add     a,#40h
        mov     r3,a
        inc     dptr
        movx    a,@dptr
        mov     r2,a
        mov     dptr,#_data_buffer      ;load pointer to data_buffer
nextwr: movx    a,@dptr                 ;load data to write to 29C040
        inc     dptr                    ;increment data_buffer pointer
        push    dpl
        push    dph
        mov     dpl,r2
        mov     dph,r3
        movx    @dptr,a                 ;write data to 29C040
        inc     dptr                    ;increment flash address pointer
        mov     r2,dpl
        mov     r3,dph
        pop     dph
        pop     dpl
        djnz    r1,nextwr               ;decrement byte counter
        djnz    r0,nextwr               ; loop until sector has been loaded
  .endasm
  delayms(twc);                         /* delay for the programming cycle */
}

/*********************************************************************/
/* READ_SECTOR copies a sector from the 29C040 into the SRAM buffer */
/* Either 256- or 512-bytes are transfered depending on the size of */
/* the sector.                                                       */
/*********************************************************************/

void read_sector()

{
unsigned int count;

  P1 = block_number;                                /* initial block # */
  address_pointer = sector_address + 0x4000;        /*create address pointer*/
  for (count = 0; count < sector_size; count++)     /*transfer sector to SRAM*/
  {
    .asm
    mov         dptr,#_address_pointer  ;load address pointer's address
    movx        a,@dptr                 ;load address pointer high byte
    mov         b,a
    inc         dptr
    movx        a,@dptr                 ;load address pointer low byte
    mov         dpl,a
    mov         dph,b
    movx        a,@dptr                 ;read data from 29C040
    mov         dptr,#_temp_byte
    movx        @dptr,a                 ;store data from 29C040 into temp_byte
    .endasm
    data_buffer[count] = temp_byte;             /*place data into SRAM*/
    address_pointer = address_pointer + 1;      /*increment address pointer*/
  }
}

/************/
```

```
/* MAINLINE */
/************/

main()

{
  part_id = get_part_id();              /* GET PART ID */
  set_parameters(part_id);              /* DETERMINE WRITE PARAMETERS */
  dummy_buffer_load(0x55);              /* LOAD SRAM BUFFER WITH DUMMY DATA */
  block_number = 0x1f;                  /* SPECIFY BLOCK NUMBER TO WRITE */
  sector_address = 0x0400;              /* SPECIFY ADDRESS WITHIN BLOCK */
  write_sector();                       /* COPY SRAM BUFFER TO 29C040 */
  read_sector();                        /* COPY 29C040 SECTOR TO SRAM */
}
```

Atmel AT29C040A Demo Circuit



Note: If the Flash is to be used as external program memory, then pin 31 (EA/ Vpp) of the AT89C51 cannot be connected to V_{CC}.

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Features

- E^2 Programmable 65,536 x 1, 131,072 x 1, and 262,144 x 1 bit Serial Memories Designed To Store Configuration Programs For Programmable Gate Arrays
- Simple Interface to SRAM FPGAs Requires Only One User I/O Pin
- Compatible With AT6000 FPGAs, ATT3000 FPGA, EPF8000 FPGAs, ORCA FPGAs, XC2000, XC3000, XC4000, XC5000 FPGAs
- Cascadable To Support Additional Configurations or Future Higher-density Arrays (17C128 and 17C256 only)
- Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- Available In the Space-efficient Plastic DIP or Surface-mount PLCC and SOIC Packages
- In-system Programmable Via 2-Wire Bus
- Emulation of 24CXX Serial E^2PROMs

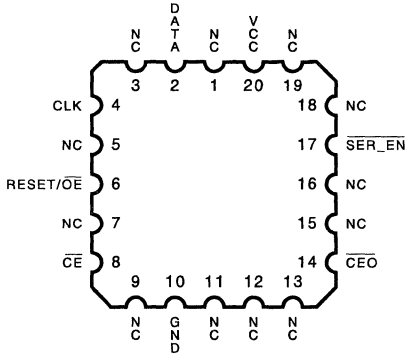
Description

The AT17C65/128/256 (AT17CXXX family) FPGA Configuration E^2PROMS (Configurator) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. Both the AT17C65 and the AT17C128 are packaged in the 8-pin DIP and the popular 20-pin Plastic Leaded Chip Carrier, and SOIC. The AT17C256 is available in 14-pin SOIC or 20-pin PLCC or SOIC packages. The AT17CXXX family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17CXXX organization supplies enough memory to configure one or multiple smaller FPGAs. Using a special feature of the AT17CXXX, the user can select the polarity of the reset function by programming a special E^2PROM bit.

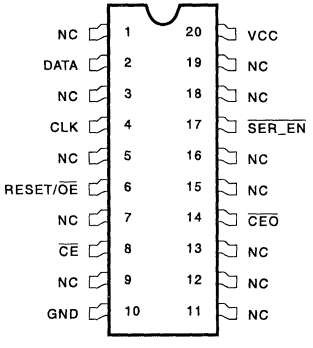
The AT17C65/128/256 can be programmed with the standard programmers from other manufacturers.

Pin Configurations

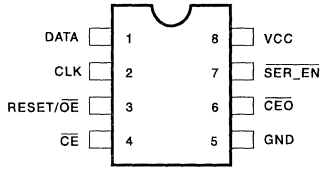
20-Pin PLCC



20-Pin SOIC



8-Pin DIP



FPGA Configuration E^2PROM

65K, 128K, and 256K

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Controlling The AT17C65/128/256 Serial E²PROMs

Most connections between the FPGA device and the Serial E²PROM are simple and self-explanatory:

- The DATA output of the AT17C65/128/256 drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17C65/128/256.
- The $\overline{CEO}$ output of any AT17C128/256 drives the $\overline{CE}$ input of the next AT17C128/256 in a cascade chain of PROMs.
- $\overline{SER\_EN}$ must be connected to V_{CC}.

There are, however, two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$, as shown in the AC Characteristics Waveform.

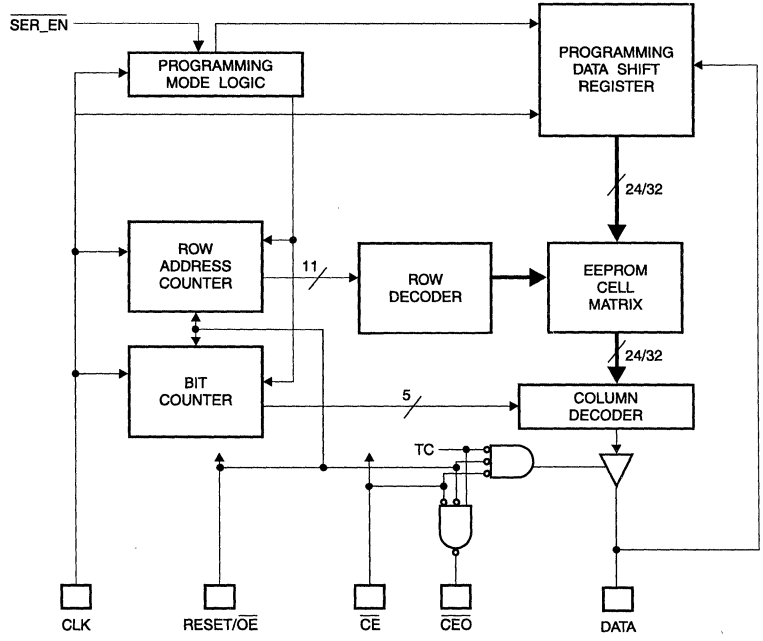
Condition 1

The simplest connection is to have the FPGA D/$\overline{P}$ output drive both $\overline{CE}$ and RESET/$\overline{OE}$ in parallel. Due to its simplicity, however, this method will fail if the FPGA receives an external reset condition during the configuration cycle. If a system reset is applied to the FPGA, it will abort the original configuration and then reset itself for a new configuration, as intended. Of course, the AT17C65/128/256 does not see the external reset signal and will not reset its internal address counters and, consequently, will remain out of sync with the FPGA for the remainder of the configuration cycle.

Condition 2

The FPGA D/$\overline{P}$ output drives only the CE input of the AT17C65/128/256, while its $\overline{OE}$ input is driven by the inversion of the FPGA $\overline{RESET}$ input. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. A high level on the RESET/$\overline{OE}$ input to the AT17CXXX during FPGA reset clears the PROM internal address pointer, so that the reconfiguration starts at the beginning. The AT17C65/ 128/256 does not require an inverter since the RESET polarity is programmable.

Block Diagram



Pin Configurations

PLCC/SOIC	DIP			
Pin	**Pin**	**Name**	**I/O**	**Description**
2	1	DATA	I/O	Three-state DATA output for reading. Input/Output pin for programming.
4	2	CLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
6	3	RESET/$\overline{OE}$	I	RESET/Output Enable input. A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or RESET/$\overline{OE}$. This document describes the pin as RESET/$\overline{OE}$.
8	4	$\overline{CE}$	I	Chip Enable input. Used for device selection. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode.
10	5	GND		Ground pin.
14	6	$\overline{CEO}$	O	Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter $\overline{CEO}$ will stay High until the entire PROM is read again and senses the status of RESET polarity.
17	7	$\overline{SER\_EN}$	I	Serial enable is normally high during FPGA loading operations. Bringing SER_EN low, enables the two wire serial interface mode for programming.
20	8	V_{CC}		+5V power supply input.

FPGA Master Serial Mode Summary

The I/O and logic functions of the FPGA and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Mode, the Logic Cell Array automatically loads the configuration program from an external memory. The Serial Configuration E^2PROM has been designed for compatibility with the Master Serial Mode.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} + 0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 s @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Cascading Serial Configuration E²PROMs (AT17C128 and AT17C256)

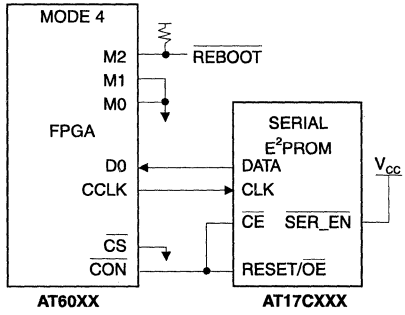
For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory (17C128 and 17C256 only).

After the last bit from the first Configurator is read, the next clock signal to the Configurator asserts its $\overline{CEO}$ output Low and disables its DATA line. The second Configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded Configurators are reset if $\overline{RESET}$ goes Low forcing the RESET/$\overline{OE}$ on each Configurator to go High.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground.

Mode 4 Configuration



Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ low. In this mode the chip can be programmed by a 2-wire interface. The programming is done at V_{CC} supply only. Programming (High) voltages are generated inside the chip. See the Programming Specification for Atmel's Configuration Memories Application Note for further information.

AT17CXXX Reset Polarity

The AT17CXXX lets the user choose the reset polarity as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE.

Standby Mode

The AT17CXXX enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the Configurator consumes less than 1.0 mA of current. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

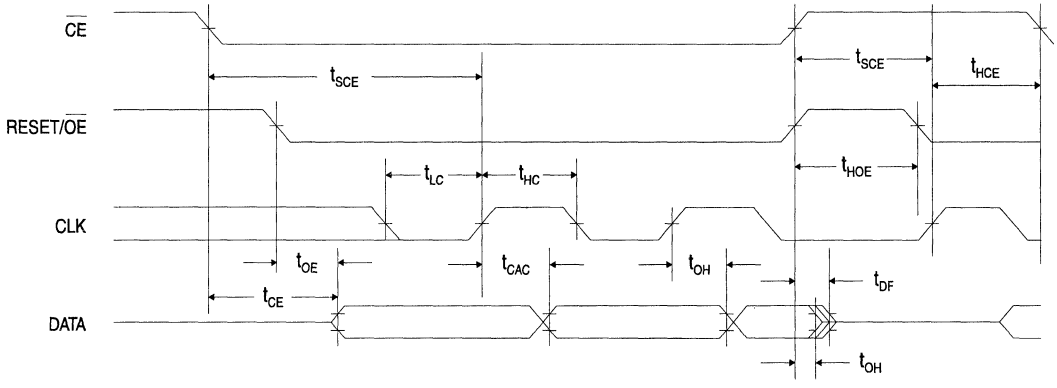
Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	4.75	5.25	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5	5.5	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5	5.5	V

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode			10	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		1	mA
		Industrial/Military		2	mA

AC Characteristics Over Operating Conditions

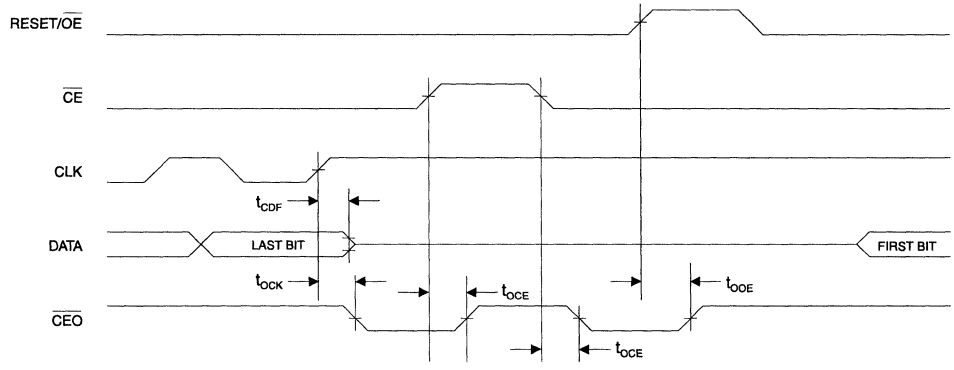


AC Characteristics Over Operating Conditions

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{OE}	$\overline{OE}$ to Data Delay		110		150	ns
T_{CE}	$\overline{CE}$ to Data Delay		50		50	ns
T_{CAC}	CLK to Data Delay		50		55	ns
T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	30		35		ns
T_{HC}	CLK High Time	30		35		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	45		50		ns
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		5		ns
T_{HOE}	$\overline{OE}$ High Time (Guarantees Counter Is Reset)	50		60		ns
F_{MAX}	MAX Input Clock Frequency		10		10	MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±500 mV from steady state active levels.

AC Characteristics Over Operating Conditions When Cascading



AC Characteristics Over Operating Conditions When Cascading

Symbol		Description	Commercial		Industrial/Military		Units
			Min	Max	Min	Max	
1	T_{CDF}	CLK to Data Float Delay		50		50	ns
2	T_{OCK}	CLK to $\overline{CEO}$ Delay		65		75	ns
3	T_{OCE}	CE to $\overline{CEO}$ Delay		55		60	ns
4	T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		55		55	ns

Ordering Information

Memory Size (K)	Ordering Code	Package	Operation Range
64K	AT17C65-10PC AT17C65-10JC AT17C65-10SC	8P3 20J 20S	Commercial (0°C to 70°C)
	AT17C65-10PI AT17C65-10JI AT17C65-10SI	8P3 20J 20S	Industrial (-40°C to 85°C)
128K	AT17C128-10PC AT17C128-10JC AT17C128-10SC	8P3 20J 20S	Commercial (0°C to 70°C)
	AT17C128-10PI AT17C128-10JI AT17C128-10SI	8P3 20J 20S	Industrial (-40°C to 85°C)
256K	AT17C256-10JC AT17C256-10SC	20J 20S	Commercial (0°C to 70°C)
	AT17C256-10JI AT17C256-10SI	20J 20S	Industrial (-40°C to 85°C)

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Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20J	20 Lead, Plastic J-Leaded Chip Carrier (PLCC)
20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Programming Specification for Atmel's FPGA Configuration E²PROMs AT17C65/128/256

The FPGA Configurator

The Configurator is a serial E²PROM memory which also can be used to load programmable devices. This document describes the features needed to program the Configurator.

Serial Bus Overview

The serial bus is a two wire bus; one wire (CLOCK) functions as a clock and is provided by the programmer, the second wire (DATA) is a bi-directional signal and is used to provide data and control information.

Information is transmitted on the serial bus in messages. Each MESSAGE is preceded by a START BIT and is ended with a STOP BIT. The message consists of an integer number of bytes, each byte consists of 8 bits of data and is followed by a ninth ACKNOWLEDGE BIT. This ACKNOWLEDGE BIT is provided by the recipient of the data. This is possible because devices only drive DATA low, the system (in the programming case the Programmer) provides a small pull-up current (3k Ohm equivalent) for the Data Pin.

The MESSAGE FORMAT consists of the bytes shown in the Message Bytes table below. The MESSAGE FORMAT is preceded by a start bit and ended by a stop bit.

The programmer provides all the bytes except for the data bytes when the device is being read. Note that each byte is individually acknowledged. This acknowledgment is provided by the Configurator in all cases except for the data bytes in the read mode, in which case the acknowledge is provided by the programmer.

Bit Format

Data on the DATA pin may change only during CLOCK low times.

Message Bytes

DEVICE ADDRESS	1ST ADDRESS WORD	2ND ADDRESS WORD	DATA BYTE(S)

Message Format

START BIT	DEVICE ADDRESS	1ST ADDRESS WORD	2ND ADDRESS WORD	DATA BYTE(S)	STOP BIT

FPGA Configuration E²PROM Programming Specification

Application Note

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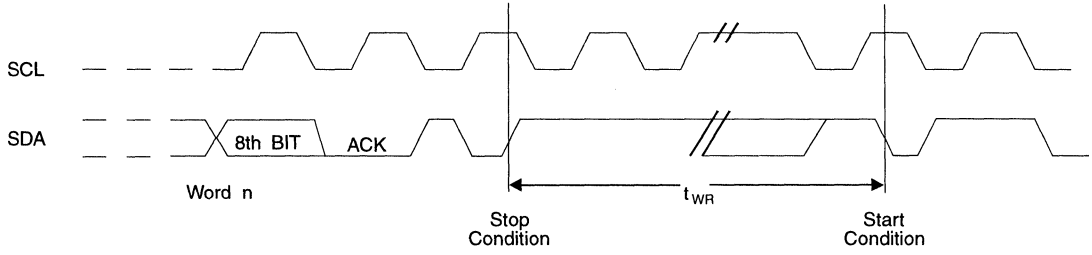
Start and Stop Bits

The START BIT is indicated by a high-to-low transition of DATA when CLOCK is high. Similarly, the STOP BIT is generated by a low-to-high transition of DATA when CLOCK is high, as shown below.

Start and Stop Bits



Acknowledge Bit

The ACKNOWLEDGE BIT is shown in the above figure. Note that the ACKNOWLEDGE BIT is provided by the device receiving the byte. The receiving device can accept the byte, by asserting a low value, on DATA or it can refuse the byte by asserting (not driving the signal) a 1 on DATA. All bytes must be terminated by either the ACKNOWLEDGE BIT or a STOP BIT.

Bit Ordering Protocol

The most significant bit is the first bit of a byte transmitted on DATA for the DEVICE ADDRESS BYTE and the EEPROM ADDRESS BYTES. It is followed by the lesser significant bits until the eighth bit, the least significant bit is transmitted. This is followed by the acknowledge bit. However, for DATA BYTES (both writing and reading) the first bit transmitted is the least significant bit. This protocol is shown in the tables below.

Device Address Byte

The contents of the Device Address Byte are shown below, along with the order in which the bits are clocked into the device. The A_2 bit is provided to allow 2 devices to share a common bus; when programming a single device, the A_2 bit and the A_2 pin on the device will usually both be at 0V.

Device Address Byte

MSB							*LSB*
1	0	1	0	A_2	1	1	R/W#
1st	2nd	3rd	4th	5th	6th	7th	8th

Where: R/W# = 1 Read
= 0 Write
A2 = 1 if A2 pin is at V_{CC}
= 0 if A2 pin is at GROUND

EEPROM Address

The EEPROM address consists of two bytes, each of which is followed by an acknowledge bit. These two bytes define a 14 bit address A_{14} - A_0. The order in which each byte is clocked into the device is also indicated. A_{14} is MSB for 256, A_{13} is MSB for 128 and A_{12} is MSB for 64.

MSB							*LSB*	
0	$0/A_{14}$	$0/A_{13}$	A_{12}	A_{11}	A10	A_9	A_8	Ack
1st	2nd	3rd	4th	5th	6th	7th	8th	

MSB							*LSB*	
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Ack
1st	2nd	3rd	4th	5th	6th	7th	8th	

Data Byte

The organization of the Data Byte is shown below. Note that in this case, the data byte is clocked into the device LSB first and MSB last.

Writing

All writing takes place in pages. A page is 64-bytes long and the page boundaries are addresses where A5 - 0 are all zero. Writing can start at any address within a page and the number of bytes written is the number of data bytes transmitted and must be 64. The first byte is written at the transmitted address. The address is incremented in the device following the receipt of each data word received. Only the lower six bits of the address are incremented and if the address is incremented after the 64th byte in the page is sent, then the next byte to be written is the first byte of the page.

Data Byte

LSB							*MSB*
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
1st	2nd	3rd	4th	5th	6th	7th	8th

A write action consists of
- a Start Bit
- a Device Address with R/W# = 0
  - An Acknowledge Bit From the device
- First Word of the Address
  - An Acknowledge Bit From the device
- Second Word of the Address
  - An Acknowledge Bit From the device
- One or more data bytes (sent to the device)
  - Each followed by an Acknowledge Bit From the device
- a Stop bit

WRITE POLLING: On receipt of the stop bit, the device enters an internally timed write cycle. While the device is busy with this write cycle it will not acknowledge any transfers. Thus the programmer can start the next page write by sending the Start Bit followed by the Device Address. If this is not acknowledged, then the programmer should abandon the transfer without asserting a stop bit. The programmer can then repeat this until an acknowledge is received. When this is received the write action can proceed, i.e. the next byte to be sent is the device address.

Reading

Read operations are initiated the same way as write operations with the exception that the R/W# bit in the device address is set to one. There are three read operations: current address read, random read and sequential read.

A current address read action consists of
- a Start Bit
- a Device Address with R/W# = 1
  - An Acknowledge Bit From the device
- a data byte from the device
- a stop bit from the programmer.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained and the device remains in 2-wire access mode. If the last operation was a read at address n, then the current address would be n + 1. If the final operation was a write at address n, then the current address would again be n + 1 with one exception. If address n was the 64th byte address in the page, the incremented address n + 1 would "roll over" to the 1st byte address on the next page.

Once the device address with the R/W# select bit set is clocked in and acknowledged by the device the current address word is serially clocked out. The programmer does not acknowledge the read but does generate a following stop condition.

(continued)

Reading (Continued)

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the device, the programmer must generate another start condition. The programmer now initiates a current address read by sending a device address with the R\W# bit high. The device acknowledges the device address and serially clocks out the data word. The programmer does not acknowledge the read but does generate a following stop condition.

```
A random address read action consists of
    a Start Bit
    a Device Address with R/W# = 0
         An Acknowledge Bit From the device
    First Word of the Address
         An Acknowledge Bit From the device
    Second Word of the Address
         An Acknowledge Bit From the device
    a Start Bit
    a Device Address with R/W# = 1
         An Acknowledge Bit From the device
    a data byte from the device
    a stop bit from the programmer.
```

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the programmer receives a data word, it responds with an acknowledge. As long as the device receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over", "on devices that support cascading" and the sequential read will continue. The sequential read operation is terminated when the programmer does not respond with an acknowledge but generates a stop condition.

Programming Pins

Eight pins are used to program the devices. These eight pins, and their mapping to the package pins are shown in the following table.

Pin	8-Pin Device	20-Pin Device
DATA	1	2
CLOCK	2	4
RESET/OE#	3	6
CE#	4	8
GROUND	5	10
A2 OR CEO#	6	14
SER_EN#	7	17
V_{CC}	8	20

Programmer Functions

The programmer needs to perform the following functions in the order given below:

1. Check the Manufacturers Code and the Device Code
2. Program the device
3. Verify the device
4. AT17CXXX only: Set the Reset Polarity option.

The functions are performed in the following manner.

Reading Manufacturers and Device Code

These two bytes are read from addresses 0 and 1 respectively with:

```
RESET/OE   =    0V
CE         =    11.5 ± 0.5V
A2         =    (Same as applied to A2 Pin, usually 0V)
SER_EN     =    0V
```

The correct codes are (1)

```
Manufacturers Code   -   Byte 0   1E
Device Code          -   Byte 1   FF   17C128
                                  7F   17C65
                                  77   17C256
```

Note: 1. The Manufacturer's Code and Device Code are read using the same byte ordering specified in the beginning of this document; i.e. LSB first, MSB last.

Programming the Device

All the bytes in the device's 64-byte page must be written. The order is not important but it is suggested that the device be written sequentially from Byte 0. Writing is accomplished by using the DATA and CLOCK pins and setting the other programming pins as follows:

```
RESET/OE   =    0V
CE         =    0V
A2         =    (Same as applied to A2 Pin, usually 0V)
SER_EN     =    0V
```

Verifying the Device

All bytes in the device must be read and compared to their intended values. Reading is done using the CLOCK and DATA pins with the other programming pins set to the same value as in programming:

```
RESET/OE   =    0V
CE         =    0V
A2         =    (Same as applied to A2 Pin, usually 0V)
SER_EN     =    0V
```

AT17CXXX - Setting the Polarity Option

Setting the Polarity Option Active High:

Write a byte of data set to FF to address 3FFF, using the previously defined 2-wire write algorithm, with the other programming pins set to the following:

RESET/$\overline{OE}$	=	5 ± 0.25V
$\overline{CE}$	=	5 ± 0.25V
A2	=	(Same as applied to A2 Pin, usually 0V)
$\overline{SER\_EN}$	=	0V

This will change RESET/$\overline{OE}$ pin functionality to $\overline{RESET}$/OE, i.e. active high OE and active low RESET.

Setting the Polarity Option Active Low:

Write a byte of data set to FF to address 3FFF, using the previously defined 2-wire write algorithm, with the other programming pins set to the following:

RESET/$\overline{OE}$	=	0V
$\overline{CE}$	=	5 ± 0.25V
A2	=	(Same as applied to A2 Pin, usually 0V)
$\overline{SER\_EN}$	=	0V

This will change $\overline{RESET}$/OE functionality to RESET/$\overline{OE}$, i.e. active low OE and active high RESET (the default condition). After RESET polarity has been modified the AT17CXXX device must be powered down before the modified RESET polarity takes effect.

Verifying the RESET/OE Polarity

If a programmed (master) device is to be used as the source for the data to be programmed into some new devices, then the programmer can read the data from the master. The polarity of the RESET/$\overline{OE}$ must be known before this can be done successfully for the AT17CXXX. Depending on the capabilities of the programming device, one of the following algorithms can be used to read the programmed polarity of the RESET/$\overline{OE}$ pin.

1. If the programmer is able to sense a tri-state condition:

Switch the power on with

RESET/$\overline{OE}$	=	0V
$\overline{CE}$	=	0V
A2 ($\overline{CEO}$)	=	Input to programmer (High Z)
$\overline{SER\_EN}$	=	5 ± 0.25V
CLOCK	=	0
DATA	=	Input to programmer

In this condition, if the SDA pin is tri-stated, then the RESET/$\overline{OE}$ fuse is ACTIVE HIGH; if the SDA pin reads a "0" or a "1", then the RESET/$\overline{OE}$ fuse is ACTIVE LOW.

2. If the programmer is NOT able to sense a tri-state condition:

Switch the power on with

RESET/$\overline{OE}$	=	5 ± 0.25V
$\overline{CE}$	=	0V
A2 ($\overline{CEO}$)	=	Input to programmer
$\overline{SER\_EN}$	=	5 ± 0.25
CLOCK	=	0
DATA	=	Input to programmer

(continued)

Verifying the RESET/OE Polarity (Continued)

Hold this configuration for 10 ms after V_{CC} reaches 5V. Then set RESET/$\overline{OE}$ to low and pulse the clock 131,072 (128K) (262,144 for 17C256;65,536 for 17C65) times reading the data provided at each clock pulse. After the last clock has been issued $\overline{CEO}$ should drop from high to low. If it does so then the polarity is RESET/$\overline{OE}$ (ACTIVE LOW). If $\overline{CEO}$ remains high, then the polarity is $\overline{RESET}$/OE (ACTIVE HIGH). In this latter case, none of the data read is reliable and it should be discarded. The procedure should be redone with RESET/$\overline{OE}$ = 0V on power up and switched to 5 ± 0.25V before starting the clock. The data read is now good data.

DC Characteristics

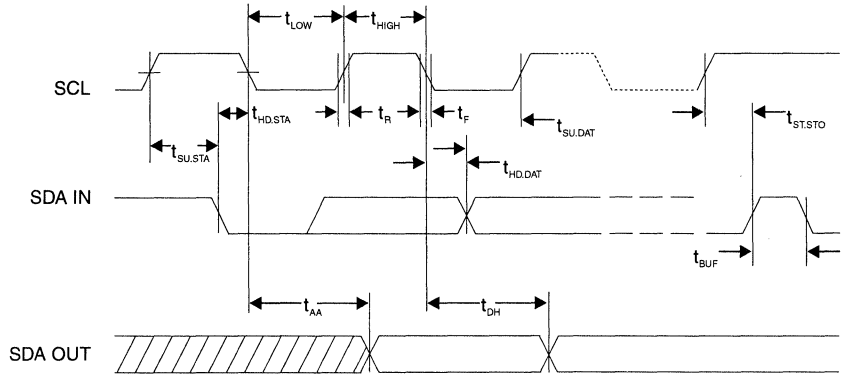
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
I_{CC}	Supply Current	V_{CC} = 5V		2.0	3.0	mA
I_{LL}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IH}	High-Level Input Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Low-Level Input Voltage		-1.0		0.4	V

5

AC Characteristics

Symbol	Parameter	Min	Max	Units
f_{CLOCK}	Clock Frequency, Clock		400	kHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	0.6		µs
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		µs
$t_{HD;STA}$	Start Hold Time	0.6		µs
$t_{SU;STA}$	Start Set-Up Time	0.6		µs
$t_{HD\ DAT}$	Data In Hold Time	0		µs
$t_{SU\ DAT}$	Data In Set-up Time	100		ns
t_R	Inputs Rise Time		0.3	µs
t_F	Inputs Fall Time		300	ns
$t_{SU\ STO}$	Stop Set-up Time	0.6		µs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		10	ms

Serial Data Timing Diagram



AT17CXXX Configurator In-System Programming Applications

For standard in-system programming, where the RESET/OE polarity does not need to be changed, Figure 1 shows a typical circuit arrangement. A 74HCT157 multiplexer is used to steer the appropriate signals of the configurator, the device(s) programmed by the configurator (typically a FPGA or EPLD), and the ISR (In System Reprogrammable) port connector. The ISR port may be a connection to a microcontroller on-board or an off-board programmer. The signals need to be muxed to avoid contention and to avoid possible disruption to the EPLD/FPGA operation. Bringing SER_EN low puts the configurator into ISR mode and also switches the multiplexer.

For applications where the RESET/OE polarity may also need to be programmed, Figure 2 shows the expanded ISR port and the associated connections to the multiplexer. Refer to the device programming section in this document for specific details.

Figure 1. Standard Configuration

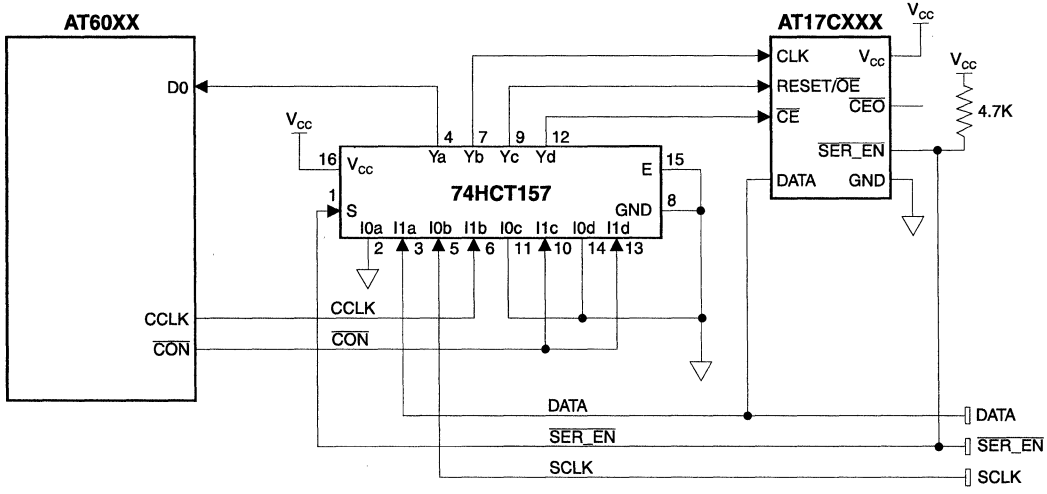


Figure 2. RESET/OE Programming Configuration (Recommended for use with XC4000/XC5000 devices.)

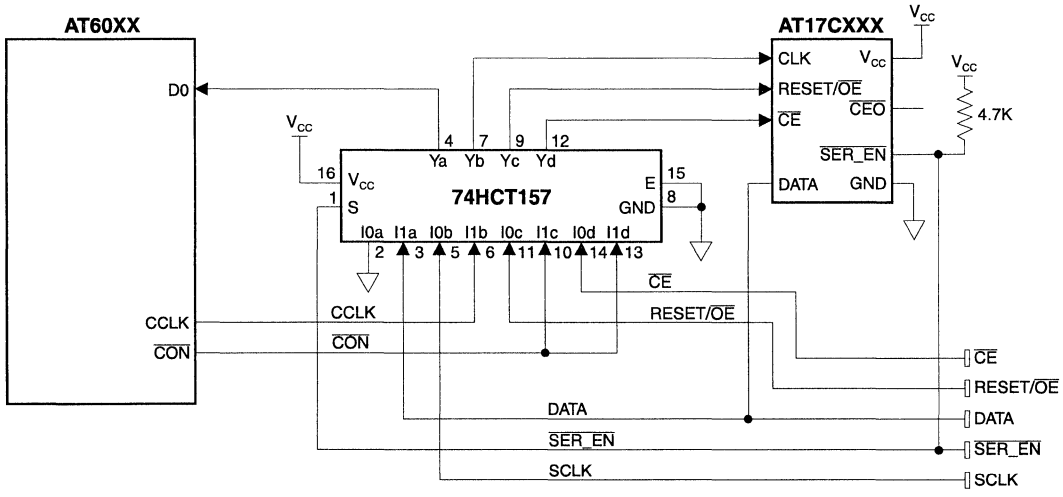


Figure 3. Atmel AT6000 - Cascaded Configuration Memories

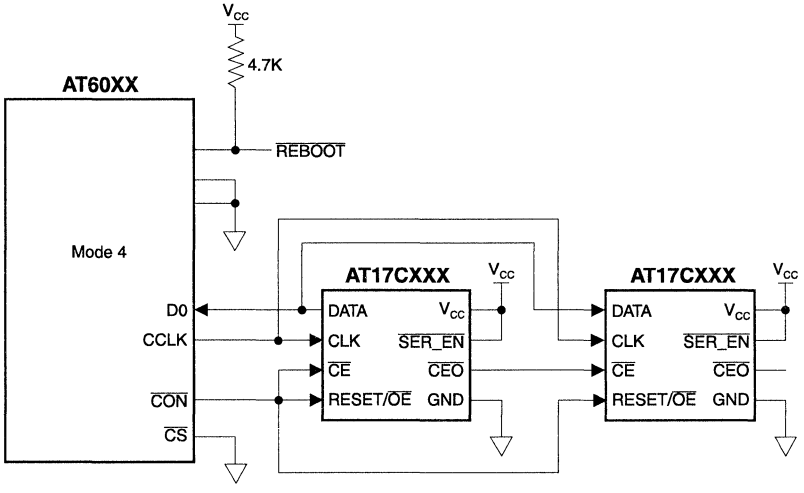


Figure 4. Atmel AT6000 - Multiple FPGAs with Identical Configuration

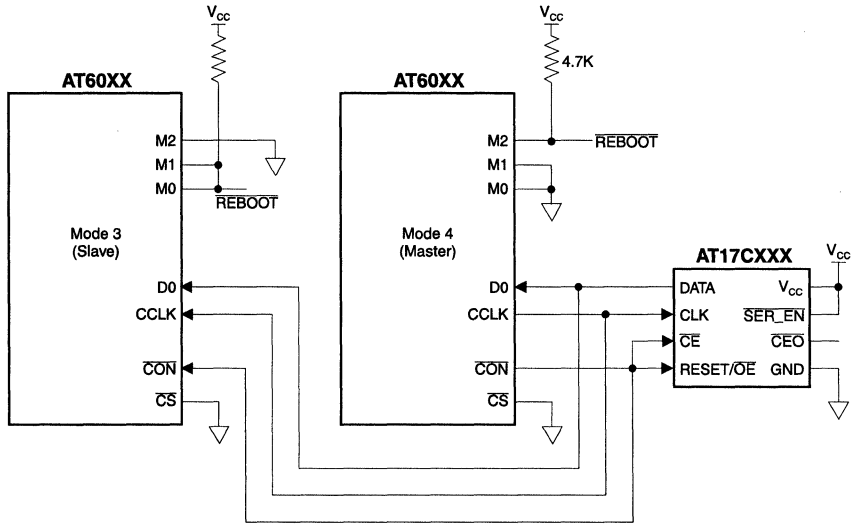


Figure 5. Atmel AT6000 - Multiple FPGAs with Individual Configurations

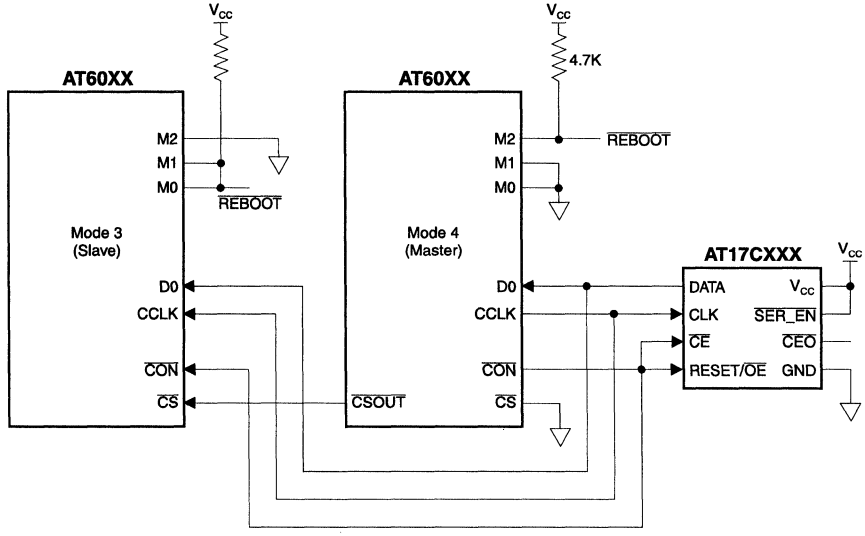
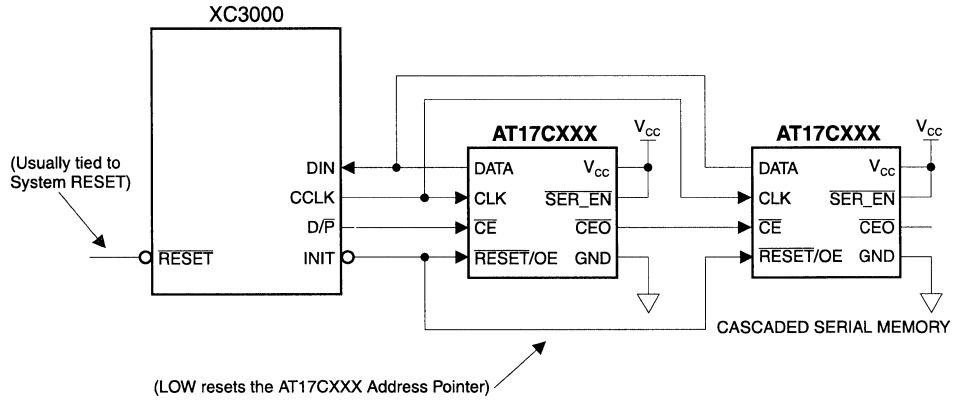
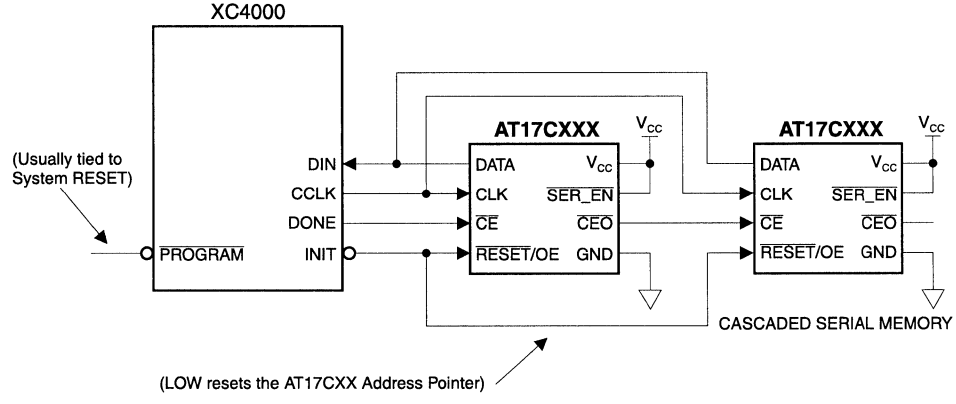


Figure 6. Xilinx XC3000 - Series Configuration



5

Figure 7. Xilinx XC4000 - Series Configuration



Pin Configurations

PLCC/SOIC	DIP			
Pin	**Pin**	**Name**	**I/O**	**Description**
2	1	DATA	I/O	Three-state DATA output for reading. Input/Output pin for programming.
4	2	CLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
6	3	RESET/$\overline{OE}$	I	RESET/Output Enable input. A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or RESET/OE. This document describes the pin as RESET/$\overline{OE}$.
8	4	$\overline{CE}$	I	Chip Enable input. Used for device selection. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode.
10	5	GND		Ground pin.
14	6	$\overline{CEO}$	O	Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter CEO will stay High until the entire PROM is read again and senses the status of RESET polarity.
17	7	$\overline{SER\_EN}$	I	Serial enable is normally high during FPGA loading operations. Bringing $\overline{SER\_EN}$ low, enables the two wire serial interface mode for programming.
20	8	V_{CC}		+5V power supply input.

FPGA Configuration E²PROM Programming Board

AT17C65
AT17C128
AT17C256

5

Features

Hardware

- Supports programming for Atmel E²PROM AT17CXXX series of devices
- Fast programming time (approx. 5 seconds)
- Connection to allow direct in system device programming via 10-pin header
- Runs off portable 9V DC power supply

Software

- Runs on any X86 PC
- Support for programmable reset polarity
- Industry standard Intel-HEX input format
- Risk free read and retarget EPROM-based 17CXXX devices
- Verification routines to validate correct programming

System Contents

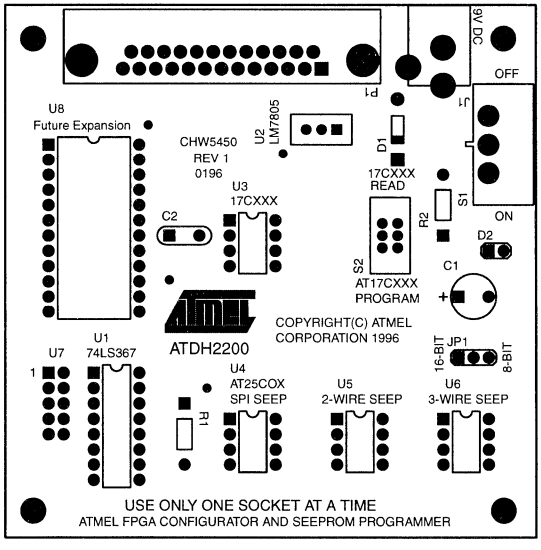
- Standard (PC printer port) parallel cable
- Serial programming board (ATDH2200) Revision 1.0
- 9V DC/200 mA 2.1 mm center positive power supply (supplied in US)
- Atmel AT17CXXX device
- 8-pin dip to 20-pin PLCC adapter (optional)
- 8-pin dip to 20-pin SOIC adapter (optional)
- AT17CXXX device datasheet
- AT17CXXX device programming datasheet
- ATDH2200 programming software (CF.EXE) revision 2.1 or above

Description

The ATDH2200 programming board and associated software allows designers to quickly and economically program Atmel's family of E²PROM FPGA configuration memories. The ATDH2200 board connects to any X86 PC via the parallel port. The associated software allows designers control over reading, writing (Atmel only) and verifying industry standard 17CXXX serial FPGA configuration support memories.

(continued)

Figure 1. ATDH2200 Configurator Programming Board



0642B

Description (Continued)

The software allows the designer to set the 17CXXX devices programmable reset polarity and supports flexible data input formats. The source data for programming can be obtained by reading a previously programmed 17CXXX part via the programming board or can be loaded as a file in Intel-Hex format or Atmel's proprietary .BST file format.

Connection of the ATDH2200 Programming Board

Please refer to figure 1.

Connect a 25-pin parallel printer cable (female) to the connector P1. This must be plugged into the PC's first parallel port (LPT1). Ensure that the power switch S1 is in the OFF position. connect the 9V DC (ground shields) power connector to J1. Insert an AT17CXXX device into the 8 pin socket U3 in the center of the board.

Switching Between 17CXXX READ Mode and 17CXXX PROGRAM Mode

The programming board supports the two modes of operation of the AT17CXXX devices. The $\overline{\text{SEREN}}$ pin on the AT17CXXX device is connected to the switch S2 on the programming board. This switch provides control of the device in the socket U3.

AT17CXXX PROGRAM (program mode) - when the switch (S2) is in this position (down) the device is enabled to be programmed and verified through a standard 2-wire programming interface built into the AT17CXXX device and is the mode used by the Atmel software to program the part. This mode can only be used with Atmel AT17CXXX serial E^2PROMs. You must not put other manufacturer parts in the (U3) socket in this mode - you may cause severe damage to those parts.

17CXXX READ (read mode) - when the switch (S2) is in this position (up) the device in socket U3 will act as a standard 17CXXX part. This mode is used if you wish to verify the reset polarity of the AT17CXXX part or you wish to read other manufacturer's EPROM based FPGA serial programming devices into the PC for retargetting to an Atmel E^2PROM part. You can not program the Atmel part when the switch is in this position.

Programming Software Options

To install the programming software:

Copy **CF.EXE** to the required area on your PC.

The software executable is called **CF.EXE** and should be run from the DOS command line:

The command line can be one of the following formats:
CF filename
CF filename {cmd}
CF filename {cmd} {polarity}

cmd options:

No cmd	Program and Verify ATMEL device with polarity default Reset/$\overline{\text{OE}}$
P	Program and verify ATMEL device
V	Verify ATMEL device only (program mode)
R	Read ATMEL device and save to file (program mode)
X	Read other manufacturer part (read mode) and save to file
U	Verify other manufacturer part (read mode)
H	Convert Intel Hex file to .BST file

polarity options:

Reset polarity is significant during read (X option), verify (U option) and program (default/P option) commands only. If no polarity given, then default is Reset/$\overline{\text{OE}}$ (or H).

H	Reset polarity is HIGH ($\overline{\text{OE}}$/Reset)
L	Reset polarity is LOW (OE/Reset)

Programming an AT17CXXX Part

1. Connect the ATDH2200 programming board to the parallel port on the PC using a standard parallel printer cable.
2. Make sure that switch S2 is in program mode.
3. Insert the AT17CXXX part in the socket marked 17CXXX (U3) in the center of the board. Only have one serial device in the board at any time.
4. Switch on the power supply to the board - the red LED (D2) should illuminate.
5. Type one of the following commands on the PC:

   If Reset polarity is to be high (Reset/$\overline{OE}$),

   ```
   cf <filename> p h
   or  cf <filename> p
   or  cf <filename>
   e.g. cf design.bst p h
   ```

   If Reset polarity is to be low ($\overline{Reset}$/OE),

   ```
   cf <filename> p l
   e.g. cf design2.bst p l
   ```

6. The software will show the programming progress as the data is downloaded, report on the selected Reset polarity and then verify the AT17CXXX device contents against the original design file.
7. The AT17CXXX is now programmed and ready for use.

Converting a Xilinx/AT&T/Microchip 17CXXX EPROM Device to an Atmel AT17CXXX EEPROM Part

This is a two stage process:

Stage 1: Reading a 17CXXX Device to a File via the PC Parallel Port

1. Connect the ATDH2200 programming board to the parallel port on the PC using a standard parallel printer cable.
2. Make sure that switch S2 is in READ MODE.
3. Insert the EPROM 17CXXX part in the socket marked 17CXXX (U3) in the middle of the board (e.g. a Xilinx/Microchip/AT&T 17CXXX serial EPROM).
4. Connect the power supply to the board - the red LED should illuminate.
5. If the device reset polarity is high type the following command

   ```
   cf <filename> x h
   e.g. cf att_part.bst x h
   ```

   If the device reset polarity is low type the following command:

   ```
   cf <filename> x l
   e.g. cf att_part.bst x l
   ```

   Failure to use the correct reset polarity will result in incorrect data being read from the serial memory.

   You will be prompted for the size of the serial memory that you are reading. Select the required memory size.

   The data will be transferred from the serial memory to the PC via the parallel port and stored in the filename specified in the command line. This file is in a modified Atmel .BST format.
6. To validate (read verify) that the data read and stored on the PC is the same as in the serial memory it was read from type the following command if the device reset polarity is high:

   ```
   cf <filename> u h
   e.g. cf att_part.bst u h
   ```

   If the device reset polarity is low type the following command:

   ```
   cf <filename> u l
   e.g. cf att_part.bst u l
   ```

   Failure to use the correct reset polarity will result in a verify failure.

Stage 2: Programming the AT17CXXX Device

The data is stored in a modified .BST file format on the PC after the device read and is suitable for direct download to the AT17CXXX serial memory.

Reset polarity is not stored in any file so it is the responsibility of the user to set the correct Reset polarity at time of programming.

1. Remove the EPROM 17CXXX device before trying to program the AT17CXXX device. Failure to do this may result in server damage to this part.
2. Follow the AT17CXXX programming procedure as detailed above.

Converting an Altera 1064/1213 EPROM Device to an Atmel AT17CXXX E²PROM Part (Requires Version 2.2 of CF.EXE)

This is a two stage process:

Stage 1: Reading an Altera 1064/1213 Device to a File via the PC Parallel Port

Note this conversion is only available for pin compatible 8 pin dip versions of the Altera 1064/1213 devices.

1. Connect the ATDH2200 programming board to the parallel port on the PC using a standard parallel printer cable.
2. Make sure that switch S2 is in READ MODE.
3. Insert the Altera 1064/1213 part in the socket marked 17CXXX (U3) in the middle of the board.
4. Connect the power supply to the board - the red LED should illuminate.
5. The device reset polarity is low. Type the following command:

   ```
   cf <filename> x l
   e.g. cf altera.bst x l
   ```

   You will be prompted for the size of the serial memory that you are reading. Select the required memory size.

   The data will be transferred from the serial memory to the PC via the parallel port and stored in the filename specified in the command line. This file is in a modified Atmel .BST format.
6. To validate (read verify) that the data read and stored on the PC is the same as in the serial memory it was read from type the following command:

   ```
   cf <filename> u l
   e.g. cf att_part.bst u l
   ```

Stage 2: Programming the AT17CXXX Device

The data is stored in .BST file format on the PC after the device read and is suitable for direct download to the AT17CXXX serial memory.

Reset polarity is not stored in any file, so it is the responsibility of the user to set the correct Reset polarity at time of programming the Atmel device.

1. Remove the Altera device before trying to program the AT17CXXX device. Failure to do this may result in severe damage to this part.
2. Follow the AT17CXXX programming procedure as detailed above.

Hex File Conversions

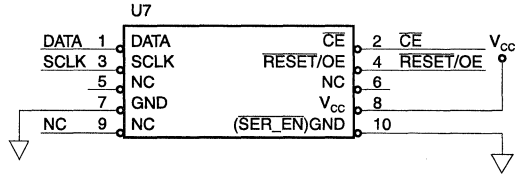
It is possible to take an industry standard Intel Hex file and convert that to a .BST file format using the cf.exe software. To convert the file use the following command:

```
cf <filename> h
e.g. cf design.hex h
```

This will create a .bst file with the name design.bst which can then be used to program the AT17CXXX parts as described earlier. Conversion of a hex file for Altera parts will be supported with Version 2.2 of the CF program.

In-System Programming Connector

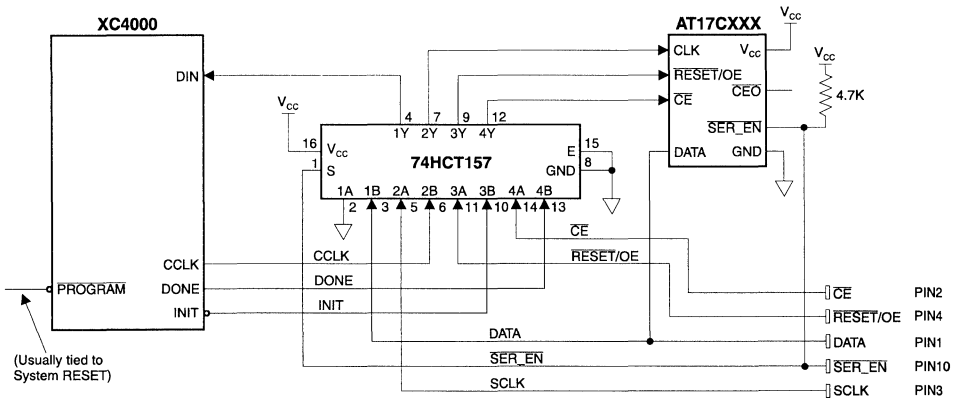
Figure 2. In-Circuit Reprogramming Interface



Note: 1. Pin 10 activates $\overline{\text{SER\_EN}}$ on target board.

The FPGA programming board has a 10 pin header (0.1" spacing) to facilitate in-system programming (figure 2) of the 17CXXX parts. The control signals generated by the software are fed to the header, as well as to the socket U3 on the board. By placing a similar socket on the target system and connecting the programming board to that target system, the programming algorithms written by Atmel can be used to program a 17CXXX device in system. Figure 3 below shows an example of the typical systems connects required to achieve in system programming.

Figure 3. In-System Programming Applications Diagram



Troubleshooting

1. Check that the board is connected to the parallel port and has power.
2. Only the first parallel port (LPT1, Port 378) is supported.
3. Make sure that switch S2 is in correct mode.
4. If the part verifies correctly, but fails in the target system check that Reset polarity has been correctly set at all stages of read, write and verify of the serial memories.

Technical Support

- Check each of the items listed in the troubleshooting section above.
- Contact your local Atmel Representative or Distributor who provided the serial programming board for technical support.
- Contact your local Atmel FAE (available at most sales offices).
- Contact Atmel FPGA technical support hotline: (408) 436-4119 (9-6 PST).
- E-mail Atmel FPGA tech. support: **fpga@atmel.com**
- Fax your inquires to **'FPGA Tech Support'** at: (408) 436-4300.

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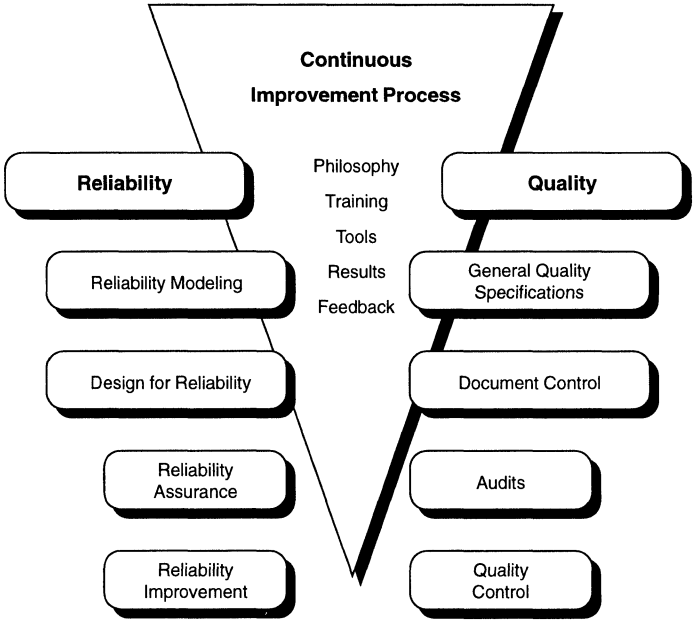
Atmel's Policy on Quality

Dedicated to Customer Satisfaction

It seems like such a simple request - *to get what you want, when you want it, and for a reasonable price.* However, in the complex world of integrated circuits, thousands of factors influence the design and manufacture of a part and can affect how the device will perform. At Atmel, every employee is committed to making sure the customer gets what he wants. From the executive level and throughout the organization, the Company's goal is one hundred percent customer satisfaction.

To achieve this goal, Atmel's employees have developed the philosophy, structure, training and tools necessary to sustain product quality and reliability. The result is two interrelated functions, one dedicated to quality and one dedicated to reliability. The "thread" that ties these functions to each other and to the rest of the Company is the Continuous Improvement Process.

Atmel's corporate philosophy of continuous improvement insures that you get not only high quality, reliable devices, but that every group within the Company is operating with your requirements in mind. Atmel's hall-mark is excellence: quality and reliability from its circuits and service from its employees.



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ISO 9000 Certification

Certification to ISO 9001 and ISO 9002 for product design and Manufacturing Processes is just one example of how Atmel strives to meet the needs of its customers around the world.

Certification is not easy and it is the result of an ever-present commitment to quality, reliability, and continuous improvement.

Atmel's commitment to ISO 9000 extends to our major contractors and distributors as well. Most are ISO 9000 certified. Atmel is continuing to work with others to become certified.

Continuous Improvement

Accepting the Malcolm Baldrige National Quality Award, one recipient said that "we are in a race without a finish line." That is a good synopsis of Atmel's philosophy of continuous improvement. The key responsibility of the executives, managers and employees of Atmel is to constantly and forever improve the quality of products and services delivered.

The Company's objectives include providing the leadership and training required to sustain a process of continuous quality improvement; implementing a total quality system that will allow Atmel to compete for and win the Malcolm Baldrige National Quality Award; implementing and utilizing SPC throughout the organization; and understanding and integrating the concepts of "six sigma" into the culture and processes.

In the past, the organization has gone through formal training in the Crosby 14-Step Quality Program; the Alamo Problem Solving, Planning and Decision Making Program; General Quality Specifications; Statistical Process Control (SPC); Statistical Design of Experiments (DOE); and in-house training for managerial and supervision skills.

Today, training continues with an emphasis on SPC, DOE, six sigma concepts and team building. The figure below represents the steps Atmel has already taken along the journey of continuous improvement. Each year, new organizational goals and functional strategies elevate the Company's level of quality even higher.

In addition to training, the journey of continuous improvement involves integrating SPC, DOE, just-in-time (JIT) and other techniques into everyday operations. Use of these techniques throughout the corporation, not just in manufacturing, is proof of Atmel's commitment to continuous improvement. Whether it is order entry, wafer fabrication, review of customer specifications, government compliance testing or even returning a customer's phone call, Atmel strives for "zero defects."

Statistical Process Control

Control of process parameters is the heart of Atmel's continuous improvement system. SPC involves the portrayal of process parametric values in a graphical form to display whether an operation is in control or out of control. Through experimentation and evaluation, upper and lower control limits are established for each parametric value of

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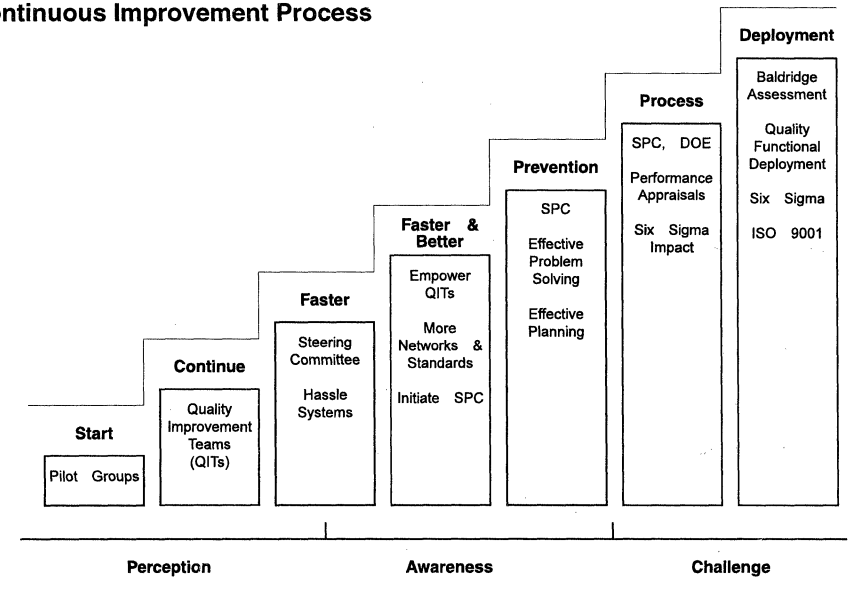
Atmel's Continuous Improvement Process



Continuous Improvement (Continued)

a given process step. The parametric values are charted on a continual basis and the result is an easy-to-interpret graph which allows for immediate corrections or adjustments by the person closest to the operation. This type of quality measurement can be applied to almost any operation within the Company.

Currently over 500 SPC charts are monitored throughout wafer fabrication, test and packaging operations. Used at crucial points in the fabrication process, SPC insures compliance with pre-set control limits. Measurements taken at critical steps in the process are used in the development of engineering models and applied to current design. Process SPC data is monitored to insure the integrity of each wafer and the resulting statistics are used to constantly improve the process.

Statistical Design of Experiments (DOE)

The DOE technique has been successfully used for many years by the agriculture and chemical industries. Only recently has the technique been used in high-technology industries.

Using DOE, various problems can be solved simultaneously by determining variables that are statistically significant, interaction between variables and the amount of variation possible in the process or product. DOE can greatly reduce the time required for process qualification and optimization. This is especially useful in wafer fabrication where quality depends on the interaction of hundreds of different process steps and materials.

When DOE is coupled with computer-aided design and process models, it can be used to predict relationships and outcomes by running experiments. Actual experiments are run on only those processes which show the most promise. This, in turn, reduces the time and cost of designing new products and processes or improving existing ones.

Just-in-time

The concept of receiving products exactly when they are needed for the system is what JIT is all about. In order for this technique to succeed, however, a significant commitment is made by both the supplier and the customer. JIT implies a partnership that gives the customer quality devices, reliable deliveries and lower costs compared with carrying inventory. Atmel performs design and fabrication tasks with such predictability that circuits may go directly to the customer's work floor, eliminating incoming inspection.

The Payoff

Quality and reliability at Atmel cannot be separated from the life cycle of the product. The Company recognizes that quality and reliability must be maintained at all levels of the organization and must be constantly improved. Through continuous improvement and a focus on customer requirements, Atmel has established dock-to-stock programs with several high-performance computer and military system companies.

The bottom line for Atmel customers is lower system life-cycle cost and faster time-to-market. Atmel's culture puts customer requirements and continuous improvement above all else, insuring that indeed you get what you want, when you want it, and at a reasonable price.

Atmel's Quality System

The foundation of Atmel's quality system is MIL-M-38535 and MIL-STD-883. These specifications are translated into company policies covering all areas of design, qualification, manufacturing and customer service. Atmel has chosen to operate to the high standards of the military in order to meet or exceed the needs of commercial and industrial customers. The Company's employees are trained, certified and audited on these policies, which are outlined in Atmel's Quality Manual.

Quality Control

Atmel's quality efforts focus on the customer and their system. For example, through strict attention to customers' component and system requirements Atmel has achieved preferred supplier status. To attain this level of customer confidence the Company demonstrates a com-

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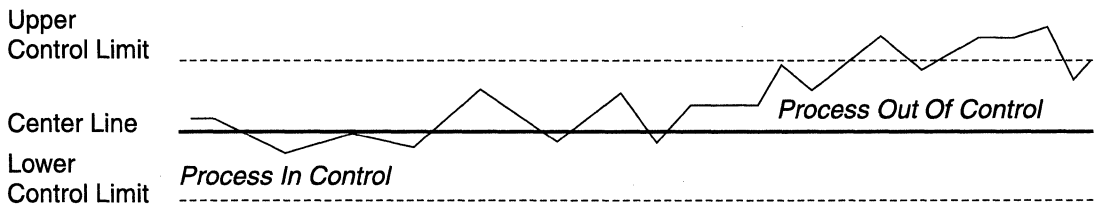
Example of a Process Control Chart



Atmel's Quality System (Continued)

mitment to quality control in all areas of the operation. This includes purchase control, in-process quality control, and statistical quality control.

Purchase Control
Every manufacturing process relies on its raw materials, and incoming inspection plays a vital role in the quality of those raw materials. At Atmel, incoming inspection is supplemented by supplier audits, historical review of supplier quality and insistence that suppliers use SPC.

In-process Quality Control
Once raw materials are controlled, the processes that transform them into a final product must also be controlled. This is done through inspection of product at critical, interim stages of manufacturing. Also included is the auditing of personnel and operations to insure that the proper procedures are being followed.

Statistical Quality Control
Immediate action is taken by the manufacturing organization when discrepancies are found during an inspection. At Atmel, a typical discrepancy results in permanent corrective action.

However, another vital function of quality control is the reporting of longer-term trends and statistics based upon individual control functions. Statistical quality control can be used to highlight increases in defects or errors in a department, for example. Atmel uses this information to take preventative action when a negative trend is detected.

Audits

Atmel maintains a self-audit group that continually monitors compliance to internal procedures and to customer specifications. The findings of this group are routinely reported to management to insure that adequate corrective actions are taken for any deficiencies.

Understanding Reliability

For integrated circuits, reliability is commonly defined as the probability that a device will operate properly for a given period of time, under specific environmental and electrical conditions. Although various methods exist for expressing reliability, it is most commonly presented in terms of probability of failure.

Reliability Modeling

Applying test data to general failure distribution curves, such as Weibull or lognormal curves, requires that the data fit the distribution and that the model is physically and mathematically reasonable with respect to the failure mechanism. Developing an accurate reliability model requires consideration of non-test-related failures as well as unidentified failure mechanisms. Atmel's reliability program is built on an understanding of the assumptions and restrictions inherent in practical reliability testing.

Design for Reliability

Many reliability concerns can be minimized with proper design techniques. For example ESD, which contributes to production yield loss and is a potential reliability problem, can be reduced or eliminated through the establishment of adequate design rules. Atmel's reliability assurance systems insure that data taken from actual product testing is fed back to design groups for verification of models and design rule updates.

Reliability Assurance Concepts

Accelerated Testing
During its life cycle, an integrated circuit passes through three distinct phases which are best defined by the failure rate of the device. In order to determine the actual interval associated with each phase, a significant number of cumulative failures (usually 50 percent) must be observed. Due to the dramatically small failure rates of integrated circuits, testing under normal operating conditions provides little or no useful data for forecasting reliability. An alternative is to increase stress levels above normal, thereby accelerating the development of failure mechanisms over time. Determining proper stress conditions that lead to realistic failures (those that could occur under normal conditions) without introducing unwanted mechanisms is a primary concern of the Reliability Engineer.

Atmel's Reliability group uses a variety of tests designed to accelerate specific failures and reduce the probability of spurious results. Variables such as temperature, voltage, currents, humidity and radiation can be controlled during testing to influence operational parameters of the device. Stress also can be selectively increased to affect specific circuit elements. To quantify the degree of failure acceleration due to increased stress, the industry has developed a number of physical models. By utilizing these models, relatively short-term, high-stress test results can be used to predict device performance under normal operating conditions.

Failure Rates
Because the failure rate of an integrated circuit varies during its life span, product reliability is best described as the failure rate of units operating after a specified number of hours. This is called Instantaneous Failure Rate, or IFR. Other measures include Average Failure Rate, the average of the IFR over a period of time, and Cumulative Failure Rate, the total number of failures occurring during operation. Because the integrated circuit failure rates are remarkably low, they are normally measured with respect to billions of device hours. This value, referred to as a FIT, is

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Reliability Assurance Concepts (Continued)

defined as failures per one billion hours of device operation.

Failure Mechanisms

Integrated circuit failure mechanisms can be classified as either process anomalies or wear-out mechanisms. Process anomalies result from less than ideal process conditions and include product defects such as contamination, step coverage deficiencies and electrostatic discharge (ESD) damage. Often termed "quality" problems, these mechanisms are normally detected through process screens such as visual inspection, thermal cycling and burn-in. Process anomalies that escape manufacturing screens often accelerate or encourage wear-out mechanisms. For example, ESD can weaken insulating oxides or thin metallization allowing dielectric breakdown or electromigration failures to occur earlier in the life cycle.

Wear-out mechanisms are directly related to the useful life of device materials, their physical properties, and interactions occurring at material interfaces. Because wear-out mechanisms result from intrinsic physical properties of the materials, reducing these failures requires attention at the design level, strict control of process variation, and use of high quality materials and composites.

Of the failure mechanisms studied by Reliability, electromigration, time-dependent dielectric breakdown and latch-up are the primary concerns.

ELECTROMIGRATION: One of the more studied problems in integrated circuit design and production is electromigration. Devices utilizing aluminum conductors are most susceptible to the phenomena. Electrons flowing in the conductor effectively collide with aluminum atoms, pushing them away and eventually forming an open circuit. Design, wafer process control, metal composition, temperature and current density determine how long a device will operate before electromigration results in a failure. Atmel's experimental electromigration models and associated research have resulted in design and production techniques which decrease this risk. One such technique adds a small quantity of copper to the aluminum. This greatly enhances the current carrying capability of the metal, reducing the occurrence of electromigration.

TIME-DEPENDENT DIELECTRIC BREAKDOWN: Reduced dielectric strength in MOS capacitors is caused by the accumulation of electric charge in a gate oxide, which limits the operational life of the device. Experiments performed on CMOS and Bipolar Enhanced MOS (BEMOS) devices indicate that Atmel's dielectrics and related processes provide excellent resistance to long-term degradation and failure, even at the high voltage levels typical in non-digital circuit applications.

LATCH-UP: Latch-up in a CMOS device allows extremely high current to flow, often resulting in open circuit traces or bond wires. The condition can occur in any PNPN structure. Proper design and Atmel's proprietary process have eliminated this problem before it occurs.

The Bathtub Curve

The traditional "bathtub" curve used to describe the failure rate of a product is actually a combination of two exponential failure rate models. The first model begins with a high failure rate and rapidly declines to a low, nearly constant level. This model describes the early-life reliability of an integrated circuit. Atmel's incoming material inspection, production test and process controls identify and remove potential phase one failures before they are shipped to a customer. Test and screening limits have been established through characterization and qualification of the

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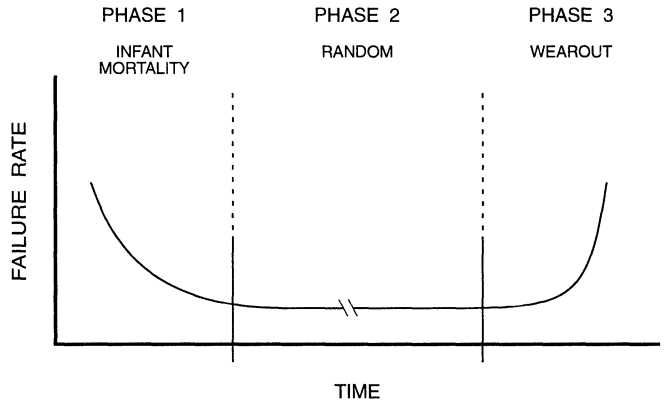
Reliability Life (Bathtub) Curve



The Bathtub Curve (Continued)

processes used in fabrication. DOE and SPC are used to maintain process stability and repeatability throughout design, product development and production.

The second model that makes up the "bathtub curve" starts with a low, relatively constant failure rate and climbs exponentially after some period of time. This is the phase three wear-out stage where mechanisms such as electromigration and oxide breakdown predominate. Through rigorous analysis of phase three failures, Atmel has developed techniques to optimize material life. The result is a forestalled phase three period and consequently, an increased phase two period.

By combining these two models, a bathtub-shaped curve representing the lifetime of the product is formed. The nearly flat portion of the curve is the result of a mathematical summation of the "tails" of the two models and represents phase two. A low, stable failure rate is characteristic of this stage as failures observed during this period are random in nature. These random failures are usually the result of sudden exposure to over-stress conditions or rare occurrences of wear-out type mechanisms. Devices shipped to the customer are in this stable portion of their lifetime.

Manufacturing for Quality and Reliability

All ceramic Atmel products are manufactured to the standards of Military Standard 883D, Class B through wafer fabrication and assembly as shown in Figure 1. The products then follow different test flows that correspond to the different classes of products that Atmel offers.

1. Commercial Grade. This product follows Test Flow (1), Figure 2 and is guaranteed over the temperature range of 0°C to +70°C.
2. Industrial Grade. This product follows Test Flow (2), Figure 3 and is guaranteed over the temperature range of -40°C to +85°C.
3. Quality Enhancement Flow. This product follows Test Flow (3), Figure 4 which specifies burn-in of industrial product in a standard flow.
4. Military Grade. Three classes of military products are offered by Atmel (MIL-STD-883D, Class B standard product, Standard Military Drawing (SMD) product, and Source Control Drawing (SCD) product). The Military Section discusses test procedures for these products in detail.

The Payoff

The focus of Atmel's quality and reliability efforts is the customer and his system. The common goals of highest field reliability and lowest system life cycle cost are achieved through close working relationships using programs such as "ship to stock", "just in time", and "failure trend analysis". Under these programs incoming Atmel circuits go straight to the customers' workfloors— they do not go through an incoming inspection cycle. This, of course, lowers manufacturing costs and is a testimony of the trust that has been established. In addition, long term field failures are analyzed so that corrective action plans can be implemented. Atmel has developed programs such as these with many major customers.

Figure 1. MIL-STD-883D, Class B, Product Flow.
All ceramic Atmel products are manufactured to these standards.

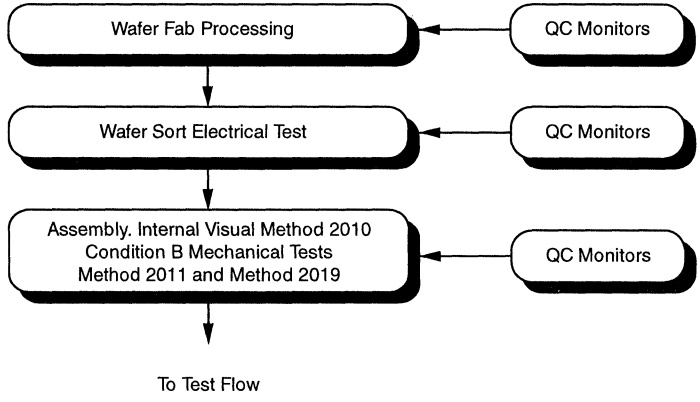


Figure 2. Test Flow (1), Commercial Grade Test Flow.

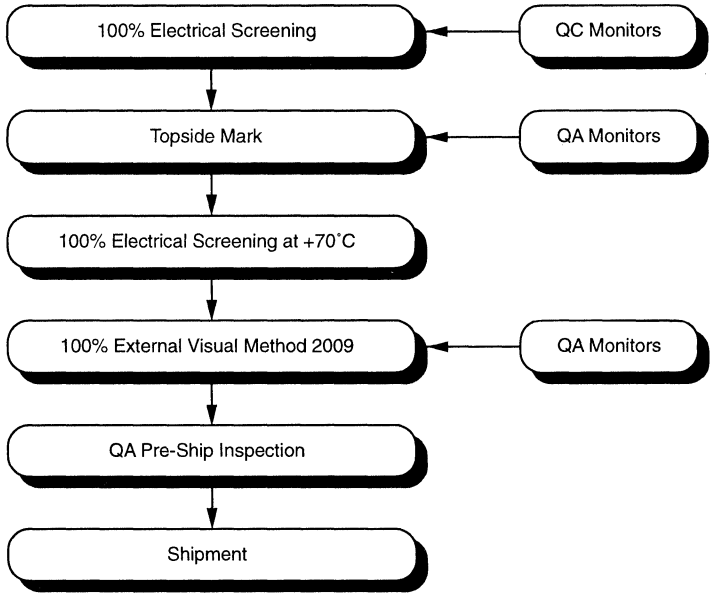


Figure 3. Test Flow (2), Industrial Grade Test Flow.

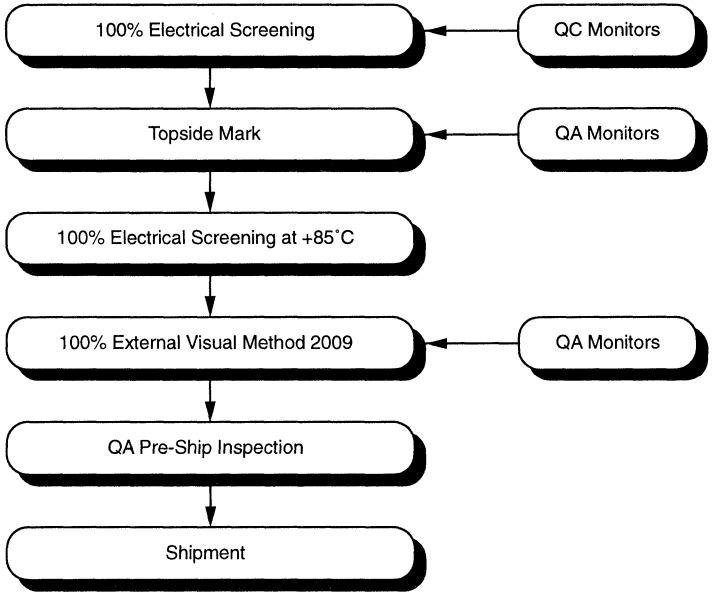
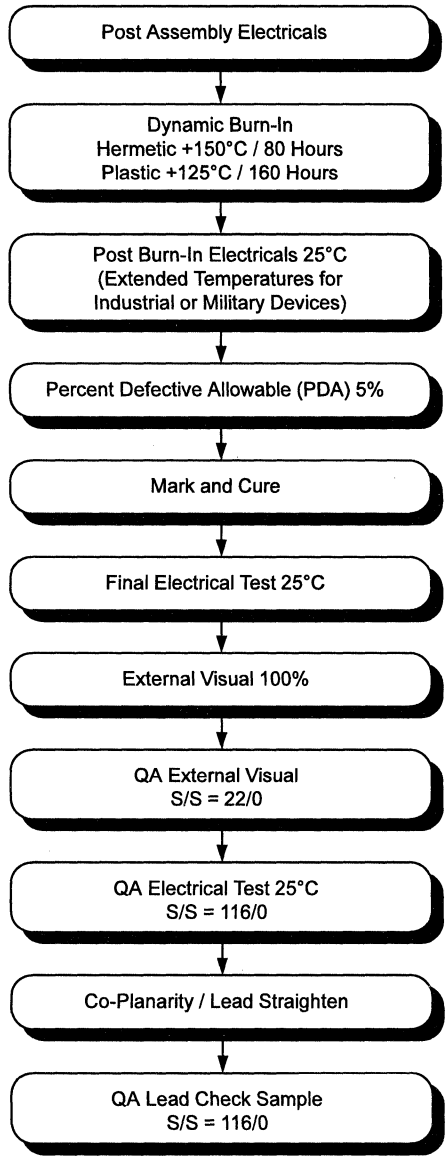


Figure 4. Test Flow (3), Quality Enhancement Flow (-9).



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Manufacturing and Test Overview of Military Products

Atmel is committed to producing products to the highest quality standards achievable through the constant use of Statistical Process Control techniques and a very active Continuous Improvement System. These systems influence the entire product life cycle from the initial product definition, through the subsequent product design and fabrication process, to the final test procedures.

Assembly and Screening

Without regard for the products' final end use all wafers produced by Atmel are fabricated with the assumption that they are destined for high reliability applications in the military marketplace. After fabrication, products directed towards use by the military will enter into special flows, beginning with the assembly operation, that will insure full compliance for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

Figure 1 and 2 illustrate the standard flow for military products. It conforms to the requirements set forth in MIL-STD-883 method 5504.

Quality Conformance Inspection

As shown in Table 1, Atmel performs all the quality conformance inspections specified by MIL-STD-883 method 5005 for class B products. This testing includes Groups A and B on each individual inspection lot and Groups C and D on a periodic basis as defined in MIL-I-38535, Appendix A.

Lot specific Group A, Group B and preconditioning data and generic Group C and Group D data are available for customer procurement.

Military Product Programs

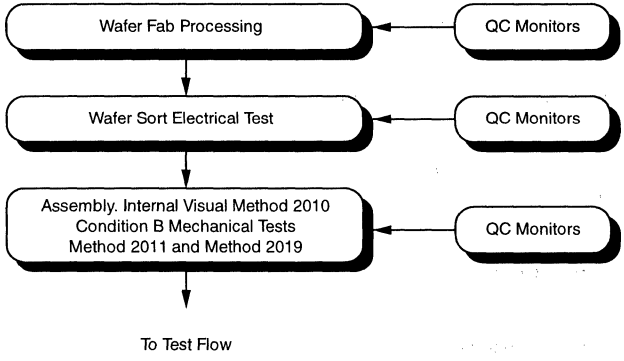
Atmel offers three programs for the procurement of military products:

(1) MIL-STD-883, Class B Program

Products procured to Atmel's MIL-STD-883 program are fully compliant with

(continued)

Figure 1. MIL-STD-883, Class B, Product Flow.
All Atmel products are manufactured to these standards.



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Military Product Programs (Continued)

MIL-STD-883 paragraph 1.2.1, with no exceptions. These products are categorized as Atmel standard "883" products and may be procured by specifying the Atmel part number appended with the suffix /883. A Certificate of Compliance (C of C) is enclosed with each shipment. Refer to the product's data sheet for specific ordering information.

(2) Standard Microcircuit Drawing (SMD) Program

Products procured to the Standard Microcircuit Drawing are class B products fully compliant with MIL-STD-883 paragraph 1.2.1. In addition, these products are in full compliance with the applicable Standard Microcircuit Drawing. Atmel's test philosophy is to screen and test both Atmel Standard /883 products and products ordered by the SMD number identically.

Section 2, Table 1 lists currently approved Atmel SMD parts, organized by their Atmel part number. Section 2, Table 2 lists currently approved Atmel SMD parts, organized by their SMD number.

(3) Source Control Drawing (SCD) Program

Program procured to a source control drawing are class B products fully compliant with MIL-STD-883 paragraph 1.2.1 with optional additional tests as specified by the customer drawing. Atmel must review and accept a customer's SCD prior to order acceptance to assure compliance.

Figure 2. Test Flow (3), MIL-STD-883, Class B, SMD and SCD Test Flow.

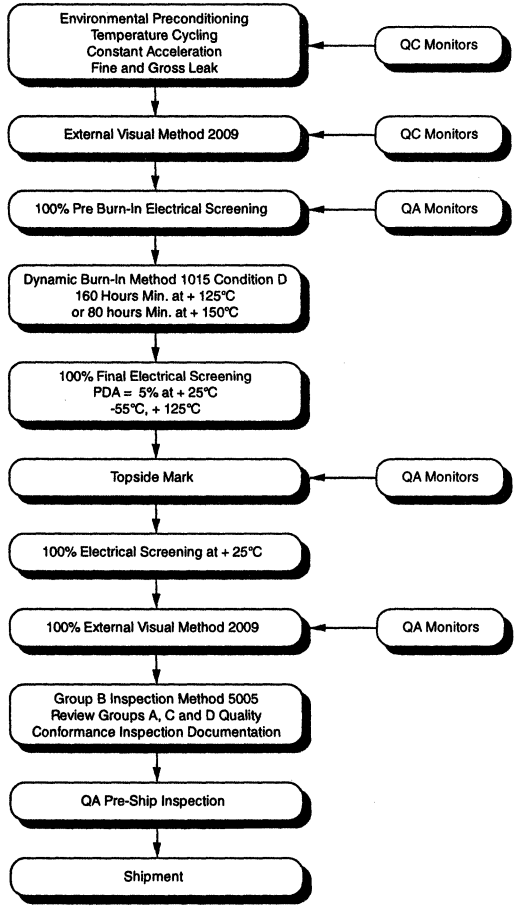


Table 1. Quality Conformance Inspections, Method 5005

Group A: Electrical Tests

Performed On Each Lot

Screen	MIL-STD-883 Table 1 Subgroups	LTPD
Static Tests at +25°C	1	2
Static Tests at +125°C	2	2
Static Tests at -55°C	3	2
Dynamic Tests at +25°C	4	2
Function Tests at +25°C	7	2
Function Tests at +125°C	8A	2
Function Tests at -55°C	8B	2
Switching Tests at +25°C	9	2
Switching Tests at +125°C	10	2
Switching Tests at -55°C	11	2

Group B: Assembly Integrity Tests

Performed On Each Lot

Screen	MIL-STD-883 Test Method	Conditions	Quantity (Accept No. or LTPD)
SUBGROUP 2			
Resistance to Solvents	2015	Top and Bottom Marks	4(0)
SUBGROUP 3			
Solderability	2003	+245°C +/-5°C	10
SUBGROUP 5			
Bond Strength	2011	Condition D	15

Group C: Die Related Tests

Screen	MIL-STD-883 Test Method	Conditions	LTPD
SUBGROUP 1			
Steady State Life Test	1005	Condition D	5
End Point Electricals	5005	As specified in the applicable device specification	

Table 1. Quality Conformance Inspections, Method 5005

Group D: Package Related Tests

By Package Type, Assembly Location, and Exterior Lead Finish

Screen	MIL-STD-883 Test Method	Conditions	Quantity (Accept No. or LTPD)
SUBGROUP 1			
Physical Dimensions	2016	MIL-M-38510, Appendix C	15
SUBGROUP 2			5
Lead Integrity	2004	Condition B2 (Condition D for LCC)	
Seal: Fine	1014	Conditon A or B	
Seal: Gross	1014	Condition C	
SUBGROUP 3			15
Thermal Shock	1011	Condition B, 15 Cycles	
Temperature Cycling	1010	Condition C, 100 Cycles	
Moisture Resistance	1004	10 Cycles	
End Point Electricals	5005	As specified in the applicable device specification (within 42 hrs)	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination		Per Visual of Method 1004 and 1010	
SUBGROUP 4			15
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E, 30 KG., Y1	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination	1010		
End Point Electricals	5005	As specified in the applicable device specification	
SUBGROUP 5			15
Salt Atmosphere	1009	Condition A	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination		Per Visual of Method 1009	
SUBGROUP 6			3 (0) or 5 (1)
Internal Water Vapor Content	1018	5,000 PPM Maximum Water Content at 100°C	
SUBGROUP 7			15
Adhesion of Lead Finish	2025	Glass Frit Seal Only (LTPD for Number of Leads)	
SUBGROUP 8			5 (0)
Lid Torque	2024	Glass Frit Seal Only	

Standard Microcircuit Drawing Product Offering

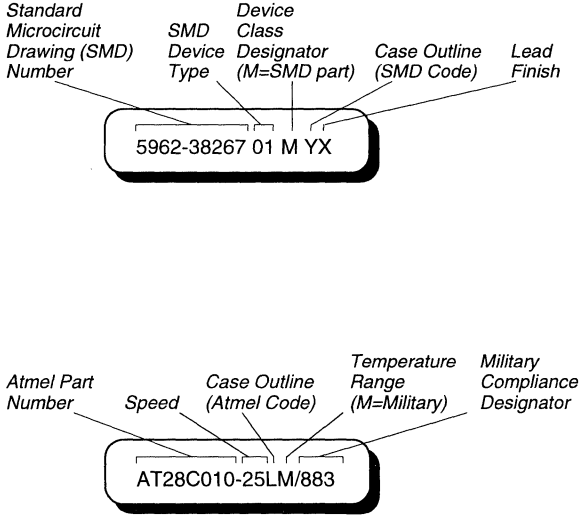
Introduction to the SMD Product Listing

Each Standard Microcircuit Drawing (SMD) part number that Atmel supplies corresponds to an Atmel /883 part number. SMD products are compliant to MIL-STD-883, paragraph 1.2.1 and to the requirements of the applicable standard microcircuit drawing. The tables in this section list the currently approved Atmel SMD parts by Atmel part number (Table 1) and by SMD part number (Table 2). They define and cross reference the Atmel /883 part number with the SMD part number for your ordering convenience.

Figure 1 (below) shows how an Atmel SMD order number defines a part, compared to the components of the Atmel similar part number.

Please note that some SMD part numbers contain the letter "M" between the device type and the case outline designator. The "M" is part of the one part-one number system, set up by DESC. It is a device class designator which indicates the part is an SMD part number as opposed to being a JAN part number.

Figure 1. Components of an SMD number (top) compared to the Atmel similar part number (bottom).



0553A

How to Use the Atmel Part Type Reference Table

The organization of Table 1 enables the purchaser to order a standardized military part by using the Atmel generic part type to locate the correct SMD drawing number. The SMD part number is the order number for SMD devices. The Atmel generic part type, which begins with the prefix "AT," heads Table 1. There are four sections in this table (see sample table below):

SMD Options

The first section lists the SMD options available at Atmel. It includes the industry generic part type, the SMD drawing number, and the SMD device type. The SMD case outline options, the lead finish options, the circuit description, and the access time that correspond to that device type are also included. The tables for the E^2PROM in this section include the end write indicator in the circuit description column and the write mode for the specific device type.

Order Code Cross-Reference

The next section of the table cross-references each optionally complete SMD part number (see ❶ below) with the Atmel similar /883 part number (see ❷ below).

Case Outline Legend

The third section gives the SMD case outline options available for the device.

Lead Finish Legend

The last section lists the SMD lead finish options available for the device.

SMD Options with Part Description and Specifications

AT28C64B

Generic Number	Standard Microcircuit Drawing Number				Description				
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Speed (ms)	Endurance (Cycles)
28C64B	5962-87514	08	X	X, A	8K x 8 E^2PROM Data Polling	Byte/Page	250	10	10K
	5962-87514	09	X	X, A	8K x 8 E^2PROM Data Polling	Byte/Page	200	10	10K

Order Code Cross-Reference

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	❶ 5962-87514 08 XX	❷ AT28C64B-25DM/883
	5962-87514 09 XX	AT28C64B-20DM/883

Case Outline Legend

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)

Lead Finish Legend

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: Finish letter "X" shall not be marked on the microcircuit or its packaging. This designation is provided for use in drawings, part lists, purchase orders, or other documentation where lead finishes A, B or C are all considered acceptable and interchangeable without preference. For Government logistic support, the A lead finish will be acquired and supplied to the end user when the X is included in the PIN for lead finish. If the PIN is not available with the A lead finish, the same PIN will be acquired except with the B or C lead finish designator as determined by availability. Type C terminal material is a fired on metallization used with leadless chip carriers.

How to Use the Atmel SMD Number Reference Table

Table 2 allows quick reference to the Atmel /883 similar part number when the SMD part number is known by the purchaser. The head for Table 2 is the SMD drawing number (see the example table below). The only section in this table is a cross-reference between the optionally complete SMD drawing number (see ❶ below) and the corresponding Atmel similar /883 part number (see ❷ below). It also includes the circuit description and access time for that part number. The E^2PROM tables include the end write indicator (which is in the circuit description column) the write mode, the write speed, and the endurance cycles for the specific part number.

Order Codes | Part Description and Specifications

5962-87514

Order Code Cross-Reference

❶ Atmel Order Number	❷ Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time (ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 08 XX	AT28C64B-25DM/883	8K x 8 E^2PROM Data Polling	Byte/Page	250	10	10K
5962-87514 09 XX	AT28C64B-20DM/883	8K x 8 E^2PROM Data Polling	Byte/Page	200	10	10K
5962-87514 10 XX	AT28HC64B-12DM/883	8K x 8 E^2PROM Data Polling	Byte/Page	120	2	10K

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C64

Generic Number	Standard Microcircuit Drawing Number				Description				
28C64	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	13	X, Y, Z	X, A	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	350	1	10K
	5962-87514	14	X, Y	X, A	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	300	1	10K
	5962-87514	15	X, Y, Z	X, A	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	250	1	10K
	5962-87514	16	X, Y	X, A	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	200	1	10K
	5962-87514	17	X, Y	X, A	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	150	1	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **13 XX**	AT28C64-35DM/883
	5962-87514 **13 YX**	AT28C64-35LM/883
	5962-87514 **13 ZX**	AT28C64-35FM/883
	5962-87514 **14 XX**	AT28C64-30DM/883
	5962-87514 **14 YX**	AT28C64-30LM/883
	5962-87514 **15 XX**	AT28C64-25DM/883
	5962-87514 **15 YX**	AT28C64-25LM/883
	5962-87514 **15 ZX**	AT28C64-25FM/883
	5962-87514 **16 XX**	AT28C64-20DM/883
	5962-87514 **16 YX**	AT28C64-20LM/883
	5962-87514 **17 XX**	AT28C64-15DM/883
	5962-87514 **17 YX**	AT28C64-15LM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: New designs to use AT28C256 product SMD 5962-88525.

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Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C64F

Generic Number	Standard Microcircuit Drawing Number				Description				
28C64F	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	28	X, Y, Z	X, A	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	200	0.2	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **28 XX**	AT28C64F-20DM/883
	5962-87514 **28 YX**	AT28C64F-20LM/883
	5962-87514 **28 ZX**	AT28C64F-20FM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: New designs to use AT28C256 product SMD 5962-88525.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C64X

Generic Number	Standard Microcircuit Drawing Number				Description				
28C64X	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	18	X, Y	X, A	8K x 8 E^2PROM Data Polling	Byte	350	1	10K
	5962-87514	19	X, Y	X, A	8K x 8 E^2PROM Data Polling	Byte	300	1	10K
	5962-87514	20	X, Y, Z	X, A	8K x 8 E^2PROM Data Polling	Byte	250	1	10K
	5962-87514	21	X, Y	X, A	8K x 8 E^2PROM Data Polling	Byte	200	1	10K
	5962-87514	22	X, Y	X, A	8K x 8 E^2PROM Data Polling	Byte	150	1	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **18 XX**	AT28C64X-35DM/883
	5962-87514 **18 YX**	AT28C64X-35LM/883
	5962-87514 **19 XX**	AT28C64X-30DM/883
	5962-87514 **19 YX**	AT28C64X-30LM/883
	5962-87514 **20 XX**	AT28C64X-25DM/883
	5962-87514 **20 YX**	AT28C64X-25LM/883
	5962-87514 **20 ZX**	AT28C64X-25FM/883
	5962-87514 **21 XX**	AT28C64X-20DM/883
	5962-87514 **21 YX**	AT28C64X-20LM/883
	5962-87514 **22 XX**	AT28C64X-15DM/883
	5962-87514 **22 YX**	AT28C64X-15LM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: New designs to use AT28C256 product SMD 5962-88525.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C64B

Generic Number	Standard Microcircuit Drawing Number				Description				
28C64B	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	08	X	X, A	8K x 8 E^2PROM Data Polling	Byte/Page	250	10	10K
	5962-87514	09	X	X, A	8K x 8 E^2PROM Data Polling	Byte/Page	200	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **08 XX**	AT28C64B-25DM/883
	5962-87514 **09 XX**	AT28C64B-20DM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: New designs to use AT28C256 product SMD 5962-88525.

AT28HC64B

Generic Number	Standard Microcircuit Drawing Number				Description				
28HC64B	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	10	X	X, A	8K x 8 E^2PROM Data Polling	Byte/Page	120	10	10K
	5962-87514	11	X	X, A	8K x 8 E^2PROM Data Polling	Byte/Page	90	10	10K
	5962-87514	12	X	X, A	8K x 8 E^2PROM Data Polling	Byte/Page	70	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **10 XX**	AT28HC64B-12DM/883
	5962-87514 **11 XX**	AT28HC64B-90DM/883
	5962-87514 **12 XX**	AT28HC64B-70DM/883

Case Outline	
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: New designs to use AT28C256 product SMD 5962-88634.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256

Generic Number	Standard Microcircuit Drawing Number				Description				
28C256	Drawing Number	Device Type	Case Outline	Lead Finish	Circui Description End Write Indicator	Write Mode	Access Time(ns	Write Speed(ms)	Endurance (Cycles)
	5962-88525	01	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	350	10	10K
	5962-88525	02	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	300	10	10K
	5962-88525	03	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	250	10	10K
	5962-88525	04	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	200	10	10K
	5962-88525	06	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	150	10	10K
	5962-88525	09 (1)	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	350	10	10K
	5962-88525	10 (1)	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	300	10	10K
	5962-88525	11 (1)	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	250	10	10K
	5962-88525	12 (1)	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	200	10	10K
	5962-88525	14 (1)	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	150	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88525 **01 UX**	AT28C256-35UM/883
	5962-88525 **01 XX**	AT28C256-35DM/883
	5962-88525 **01 YX**	AT28C256-35LM/883
	5962-88525 **01 ZX**	AT28C256-35FM/883
	5962-88525 **02 UX**	AT28C256-30UM/883
	5962-88525 **02 XX**	AT28C256-30DM/883
	5962-88525 **02 YX**	AT28C256-30LM/883
	5962-88525 **02 ZX**	AT28C256-30FM/883
	5962-88525 **03 UX**	AT28C256-25UM/883
	5962-88525 **03 XX**	AT28C256-25DM/883
	5962-88525 **03 YX**	AT28C256-25LM/883
	5962-88525 **03 ZX**	AT28C256-25FM/883
	5962-88525 **04 UX**	AT28C256-20UM/883
	5962-88525 **04 XX**	AT28C256-20DM/883
	5962-88525 **04 YX**	AT28C256-20LM/883
	5962-88525 **04 ZX**	AT28C256-20FM/883

Note: 1. SMD specifies Software Data Protection feature for device type, although Atmel product supplied to *every* device type on the SMD is 100% tested for this feature.

(continued)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256 (Continued)

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88525 **06 UX**	AT28C256-15UM/883
	5962-88525 **06 XX**	AT28C256-15DM/883
	5962-88525 **06 YX**	AT28C256-15LM/883
	5962-88525 **06 ZX**	AT28C256-15FM/883
	5962-88525 **09 UX**	AT28C256-35UM/883
	5962-88525 **09 XX**	AT28C256-35DM/883
	5962-88525 **09 YX**	AT28C256-35LM/883
	5962-88525 **09 ZX**	AT28C256-35FM/883
	5962-88525 **10 UX**	AT28C256-30UM/883
	5962-88525 **10 XX**	AT28C256-30DM/883
	5962-88525 **10 YX**	AT28C256-30LM/883
	5962-88525 **10 ZX**	AT28C256-30FM/883
	5962-88525 **11 UX**	AT28C256-25UM/883
	5962-88525 **11 XX**	AT28C256-25DM/883
	5962-88525 **11 YX**	AT28C256-25LM/883
	5962-88525 **11 ZX**	AT28C256-25FM/883
	5962-88525 **12 UX**	AT28C256-20UM/883
	5962-88525 **12 XX**	AT28C256-20DM/883
	5962-88525 **12 YX**	AT28C256-20LM/883
	5962-88525 **12 ZX**	AT28C256-20FM/883
	5962-88525 **14 UX**	AT28C256-15UM/883
	5962-88525 **14 XX**	AT28C256-15DM/883
	5962-88525 **14 YX**	AT28C256-15LM/883
	5962-88525 **14 ZX**	AT28C256-15FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256E

Generic Number	Standard Microcircuit Drawing Number				Description				
28C256E	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88525	05	U, X, Y, Z	X, A	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
	5962-88525	08	U, X, Y, Z	X, A	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	100K
	5962-88525	13 (1)	U, X, Y, Z	X, A	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
	5962-88525	16 (1)	U, X, Y, Z	X, A	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	100K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88525 **05 UX**	AT28C256E-25UM/883
	5962-88525 **05 XX**	AT28C256E-25DM/883
	5962-88525 **05 YX**	AT28C256E-25LM/883
	5962-88525 **05 ZX**	AT28C256E-25FM/883
	5962-88525 **08 UX**	AT28C256E-15UM/883
	5962-88525 **08 XX**	AT28C256E-15DM/883
	5962-88525 **08 YX**	AT28C256E-15LM/883
	5962-88525 **08 ZX**	AT28C256E-15FM/883
	5962-88525 **13 UX**	AT28C256E-25UM/883
	5962-88525 **13 XX**	AT28C256E-25DM/883
	5962-88525 **13 YX**	AT28C256E-25LM/883
	5962-88525 **13 ZX**	AT28C256E-25FM/883
	5962-88525 **16 UX**	AT28C256E-15UM/883
	5962-88525 **16 XX**	AT28C256E-15DM/883
	5962-88525 **16 YX**	AT28C256E-15LM/883
	5962-88525 **16 ZX**	AT28C256E-15FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: 1. SMD specifies Software Data Protection feature for device type, although Atmel product supplied to *every* device type on the SMD is 100% tested for this feature.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256F

Generic Number	Standard Microcircuit Drawing Number				Description				
28C256F	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88525	07	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	150	3	10K
	5962-88525	15 (1)	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	150	3	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88525 **07 UX**	AT28C256F-15UM/883
	5962-88525 **07 XX**	AT28C256F-15DM/883
	5962-88525 **07 YX**	AT28C256F-15LM/883
	5962-88525 **07 ZX**	AT28C256F-15FM/883
	5962-88525 **15 UX**	AT28C256F-15UM/883
	5962-88525 **15 XX**	AT28C256F-15DM/883
	5962-88525 **15 YX**	AT28C256F-15LM/883
	5962-88525 **15 ZX**	AT28C256F-15FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Note: 1. SMD specifies Software Data Protection feature for device type, although Atmel product supplied to *every* device type on the SMD is 100% tested for this feature.

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28HC256

Generic Number	Standard Microcircuit Drawing Number				Description				
28HC256	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88634	01	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	120	10	10K
	5962-88634	03	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	90	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88634 **01 UX**	AT28HC256-12UM/883
	5962-88634 **01 XX**	AT28HC256-12DM/883
	5962-88634 **01 YX**	AT28HC256-12LM/883
	5962-88634 **01 ZX**	AT28HC256-12FM/883
	5962-88634 **03 UX**	AT28HC256-90UM/883
	5962-88634 **03 XX**	AT28HC256-90DM/883
	5962-88634 **03 YX**	AT28HC256-90LM/883
	5962-88634 **03 ZX**	AT28HC256-90FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28HC256F

Generic Number	Standard Microcircuit Drawing Number				Description				
28HC256F	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88634	02	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	120	3	10K
	5962-88634	04	U, X, Y, Z	X, A	32K x 8 E^2PROM Data Polling	Byte/Page	90	3	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88634 **02 UX**	AT28HC256F-12UM/883
	5962-88634 **02 XX**	AT28HC256F-12DM/883
	5962-88634 **02 YX**	AT28HC256F-12LM/883
	5962-88634 **02 ZX**	AT28HC256F-12FM/883
	5962-88634 **04 UX**	AT28HC256F-90UM/883
	5962-88634 **04 XX**	AT28HC256F-90DM/883
	5962-88634 **04 YX**	AT28HC256F-90LM/883
	5962-88634 **04 ZX**	AT28HC256F-90FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number

AT28C010

Generic Number	Standard Microcircuit Drawing Number				Description				
28C010	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd(ms)	Endurance (Cycles)
	5962-38267	01	T, U, X, Y, Z	X, A	128K x 8, 1M bit E^2PROM Data Polling	Byte/ Page	250	10	10K
	5962-38267	03	T, U, X, Y, Z	X, A	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
	5962-38267	05	T, U, X, Y, Z	X, A	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
	5962-38267	07	U, X, Y, Z	X, A	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-38267 **01M TX**	AT28C010-25UM/883
	5962-38267 **01M UX**	AT28C010-25EM/883
	5962-38267 **01M XX**	AT28C010-25DM/883
	5962-38267 **01M YX**	AT28C010-25LM/883
	5962-38267 **01M ZX**	AT28C010-25FM/883
	5962-38267 **03M TX**	AT28C010-20UM/883
	5962-38267 **03M UX**	AT28C010-20EM/883
	5962-38267 **03M XX**	AT28C010-20DM/883
	5962-38267 **03M YX**	AT28C010-20LM/883
	5962-38267 **03M ZX**	AT28C010-20FM/883
	5962-38267 **05M TX**	AT28C010-15UM/883
	5962-38267 **05M UX**	AT28C010-15EM/883
	5962-38267 **05M XX**	AT28C010-15DM/883
	5962-38267 **05M YX**	AT28C010-15LM/883
	5962-38267 **05M ZX**	AT28C010-15FM/883
	5962-38267 **07M UX**	AT28C010-12EM/883
	5962-38267 **07M XX**	AT28C010-12DM/883
	5962-38267 **07M YX**	AT28C010-12LM/883
	5962-38267 **07M ZX**	AT28C010-12FM/883

Case Outline	
T	30U, 30 Pin, Ceramic Pin Grid Array (PGA)
U	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
X	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32F, 32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Denotes no preference in lead finish; Finish A will be supplied (per paragraph 30.6.2.7 of MIL-I-38535B Appendix A)
A	Hot Solder Dip

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-38267						
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time(ns)**	**Write Spd. (ms)**	**Endur. (Cycles)**
5962-38267 01M XX	AT28C010-25DM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 01M YX	AT28C010-25LM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 01M ZX	AT28C010-25FM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 03M XX	AT28C010-20DM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 03M YX	AT28C010-20LM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 03M ZX	AT28C010-20FM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 05M XX	AT28C010-15DM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 05M YX	AT28C010-15LM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 05M ZX	AT28C010-15FM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 07M XX	AT28C010-12DM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-38267 07M YX	AT28C010-12LM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-38267 07M ZX	AT28C010-12FM/883	128K x 8, 1M bit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-87514

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 08 XX	AT28C64B-25DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-87514 09 XX	AT28C64B-20DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-87514 10 XX	AT28HC64B-12DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	2	10K
5962-87514 11 XX	AT28HC64B-90DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	2	10K
5962-87514 12 XX	AT28HC64B-70DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	70	2	10K
5962-87514 13 XX	AT28C64-35DM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
5962-87514 13 YX	AT28C64-35LM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
5962-87514 13 ZX	AT28C64-35FM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
5962-87514 14 XX	AT28C64-30DM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	300	1	10K
5962-87514 14 YX	AT28C64-30LM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	300	1	10K
5962-87514 15 XX	AT28C64-25DM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
5962-87514 15 YX	AT28C64-25LM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
5962-87514 15 ZX	AT28C64-25FM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
5962-87514 16 XX	AT28C64-20DM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	200	1	10K
5962-87514 16 YX	AT28C64-20LM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	200	1	10K
5962-87514 17 XX	AT28C64-15DM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	150	1	10K
5962-87514 17 YX	AT28C64-15LM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	150	1	10K
5962-87514 18 XX	AT28C64X-35DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	350	1	10K
5962-87514 18 YX	AT28C64X-35LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	350	1	10K

(continued)

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-87514 (Continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 19 XX	AT28C64X-30DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
5962-87514 19 YX	AT28C64X-30LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
5962-87514 20 XX	AT28C64X-25DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 20 YX	AT28C64X-25LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 20 ZX	AT28C64X-25FM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
5962-87514 21 XX	AT28C64X-20DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
5962-87514 21 YX	AT28C64X-20LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
5962-87514 22 XX	AT28C64X-15DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K
5962-87514 22 YX	AT28C64X-15LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K
5962-87514 28 XX	AT28C64F-20DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	0.2	10K
5962-87514 28 YX	AT28C64X-20LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	0.2	10K
5962-87514 28 ZX	AT28C64X-20FM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	0.2	10K

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-88525

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-88525 01 UX	AT28C256-35UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 01 XX	AT28C256-35DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 01 YX	AT28C256-35LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte Page	350	10	10K
5962-88525 01 ZX	AT28C256-35FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 02 UX	AT28C256-30UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 XX	AT28C256-30DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 YX	AT28C256-30LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 ZX	AT28C256-30FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 03 UX	AT28C256-25UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 XX	AT28C256-25DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 YX	AT28C256-25LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 ZX	AT28C256-25FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 04 UX	AT28C256-20UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 XX	AT28C256-20DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 YX	AT28C256-20LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 ZX	AT28C256-20FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 05 UX	AT28C256E-25UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 XX	AT28C256E-25DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 YX	AT28C256E-25LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 ZX	AT28C256E-25FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K

(continued)

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-88525 (Continued)						
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time(ns)**	**Write Spd. (ms)**	**Endur. (Cycles)**
5962-88525 06 UX	AT28C256-15UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 06 XX	AT28C256-15DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 06 YX	AT28C256-15LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 06 ZX	AT28C256-15FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 07 UX	AT28C256F-15UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 XX	AT28C256F-15DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 YX	AT28C256F-15LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 ZX	AT28C256F-15FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 08 UX	AT28C256E-15UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	100K
5962-88525 08 XX	AT28C256E-15DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	100K
5962-88525 08 YX	AT28C256E-15LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	100K
5962-88525 08 ZX	AT28C256E-15FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	100K
5962-88525 09 UX (1)	AT28C256-35UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 09 XX (1)	AT28C256-35DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 09 YX (1)	AT28C256-35LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 09 ZX (1)	AT28C256-35FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 10 UX (1)	AT28C256-30UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 10 XX (1)	AT28C256-30DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 10 YX (1)	AT28C256-30LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 10 ZX (1)	AT28C256-30FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K

(continued)

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-88525 (Continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-88525 11 UX (1)	AT28C256-25UM/883	32K x 8 E²PROM Data Polling	Byte/Page	250	10	10K
5962-88525 11 XX (1)	AT28C256-25DM/883	32K x 8 E²PROM Data Polling	Byte/Page	250	10	10K
5962-88525 11 YX (1)	AT28C256-25LM/883	32K x 8 E²PROM Data Polling	Byte/Page	250	10	10K
5962-88525 11 ZX (1)	AT28C256-25FM/883	32K x 8 E²PROM Data Polling	Byte/Page	250	10	10K
5962-88525 12 UX (1)	AT28C256-20UM/883	32K x 8 E²PROM Data Polling	Byte/Page	200	10	10K
5962-88525 12 XX (1)	AT28C256-20DM/883	32K x 8 E²PROM Data Polling	Byte/Page	200	10	10K
5962-88525 12 YX (1)	AT28C256-20LM/883	32K x 8 E²PROM Data Polling	Byte/Page	200	10	10K
5962-88525 12 ZX (1)	AT28C256-20FM/883	32K x 8 E²PROM Data Polling	Byte/Page	200	10	10K
5962-88525 13 UX (1)	AT28C256E-25UM/883	32K x 8 E²PROM Data Polling	Byte/Page	250	10	100K
5962-88525 13 XX (1)	AT28C256E-25DM/883	32K x 8 E²PROM Data Polling	Byte/Page	250	10	100K
5962-88525 13 YX (1)	AT28C256E-25LM/883	32K x 8 E²PROM Data Polling	Byte/Page	250	10	100K
5962-88525 13 ZX (1)	AT28C256E-25FM/883	32K x 8 E²PROM Data Polling	Byte/Page	250	10	100K
5962-88525 14 UX (1)	AT28C256-15UM/883	32K x 8 E²PROM Data Polling	Byte/Page	150	10	10K
5962-88525 14 XX (1)	AT28C256-15DM/883	32K x 8 E²PROM Data Polling	Byte/Page	150	10	10K
5962-88525 14 YX (1)	AT28C256-15LM/883	32K x 8 E²PROM Data Polling	Byte/Page	150	10	10K
5962-88525 14 ZX (1)	AT28C256-15FM/883	32K x 8 E²PROM Data Polling	Byte/Page	150	10	10K
5962-88525 15 UX (1)	AT28C256F-15UM/883	32K x 8 E²PROM Data Polling	Byte/Page	150	3	10K
5962-88525 15 XX (1)	AT28C256F-15DM/883	32K x 8 E²PROM Data Polling	Byte/Page	150	3	10K
5962-88525 15 YX (1)	AT28C256F-15LM/883	32K x 8 E²PROM Data Polling	Byte/Page	150	3	10K
5962-88525 15 ZX (1)	AT28C256F-15FM/883	32K x 8 E²PROM Data Polling	Byte/Page	150	3	10K

(continued)

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-88525 (Continued)						
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time(ns)**	**Write Spd. (ms)**	**Endur. (Cycles)**
5962-88525 16 UX (1)	AT28C256E-15UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	100K
5962-88525 16 XX (1)	AT28C256E-15DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	100K
5962-88525 16 YX (1)	AT28C256E-15LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	100K
5962-88525 16 ZX (1)	AT28C256E-15FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	100K

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-88634						
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time(ns)**	**Write Spd. (ms)**	**Endur. (Cycles)**
5962-88634 01 UX	AT28HC256-12UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	10	10K
5962-88634 01 XX	AT28HC256-12DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	10	10K
5962-88634 01 YX	AT28HC256-12LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	10	10K
5962-88634 01 ZX	AT28HC256-12FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	10	10K
5962-88634 02 UX	AT28HC256F-12UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	3	10K
5962-88634 02 XX	AT28HC256F-12DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	3	10K
5962-88634 02 YX	AT28HC256F-12LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	3	10K
5962-88634 02 ZX	AT28HC256F-12FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	3	10K
5962-88634 03 UX	AT28HC256-90UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	10	10K
5962-88634 03 XX	AT28HC256-90DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	10	10K
5962-88634 03 YX	AT28HC256-90LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	10	10K
5962-88634 03 ZX	AT28HC256-90FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	10	10K
5962-88634 04 UX	AT28HC256F-90UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	3	10K
5962-88634 04 XX	AT28HC256F-90DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	3	10K
5962-88634 04 YX	AT28HC256F-90LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	3	10K
5962-88634 04 ZX	AT28HC256F-90FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	3	10K

Nonvolatile Memory Product Information 1

E^2PROMS 2

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Section 8 Die Products

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E^2PROM Die Products

Features

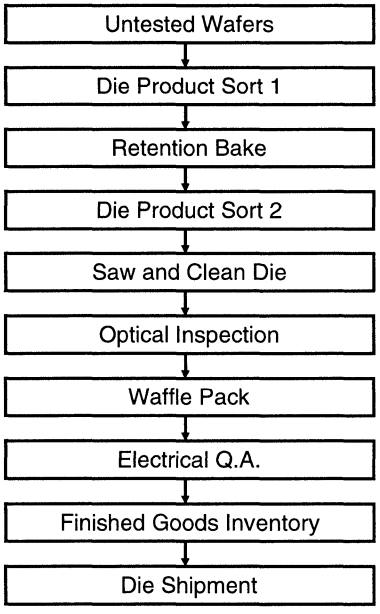
- **High Performance CMOS Technology**
- **Low Power Dissipation - Active and Standby**
- **Hardware Data Protection Features**
- **DATA Polling for End of Write Detection**
- **High Reliability**
  - **Endurance: 10^4 Cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS Compatible Inputs and Outputs**
- **0°C to +70°C Operating Range**
- **Typical Die Thickness of 22 Mils**

Description

To facilitate custom packaging, some Atmel E^2PROMS are available in die form. All Atmel E^2PROM die products are 100% electrically tested in wafer form and visually inspected after saw and clean. Atmel's E^2PROM die products are processed with an advanced CMOS floating gate technology. As with all Atmel products, they are designed and tested to ensure high quality and manufacturability. The devices may include such features as internal error correction for extended endurance and improved data retention characteristics.

Test Flow

Atmel's die product sort testing incorporates comprehensive functional and parametric tests into wafer level tests. The typical Atmel E^2PROM die test flow is outlined below.



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Testing

Die product sort test 1 includes checks for basic DC parameters such as I_{CC} and input leakage as well as for AC switching parameters. Data pattern testing is included to guarantee the functionality of each bit and to guard against pattern sensitivity. Several oxide stress tests are included to reduce the likelihood of infant mortality failures.

The data retention bake is included to ensure the integrity of the core cell oxides. A pattern is written to each die at the end of die sort test 1. The wafers are then subjected to a high temperature bake. After the bake, the pattern written in die sort test 1 is verified by die sort test 2.

A final quality assurance test is performed on each assembly lot. A sample of the die ready to ship is selected and electrically examined.

Die Product Offering

Die products are guaranteed across the commercial temperature operating range. The following E^2PROM die products are currently available from Atmel [1]:

AT28C16	AT28LV64B
AT28C17	AT28C256
AT28C64	AT28HC256
AT28C64B	AT28LV256
AT28HC64B	AT28C010
AT28BV64	AT28BV16
	AT28LV010

Handling and Die Information

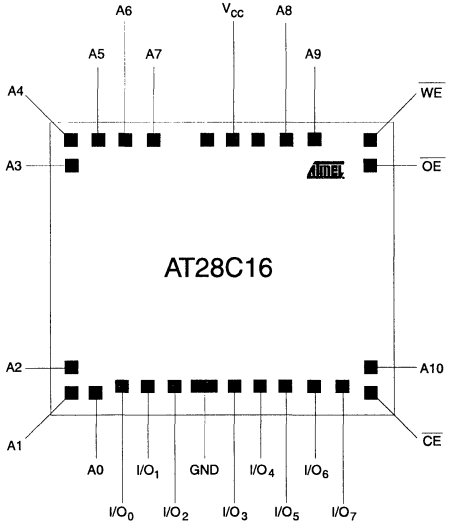
Handling instructions for E^2PROM die and other information needed for using E^2PROM die are available from Atmel.

Note: 1. The Atmel logo on the following die maps is not to scale and is only shown as a reference to properly orient the die.

AT28C16 Die Map

Die Size: 137 X 117 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (µ)	Y (µ)
A_0	-1130	-1270
A_1	-1420	-1270
A_2	-1420	-920
A_3	-1370	950
A_4	-1370	1230
A_5	-1140	1230
A_6	-900	1230
A_7	-660	1230
A_8	680	1230
A_9	920	1230
A_{10}	1630	-1000
I/O_0	-870	-1190

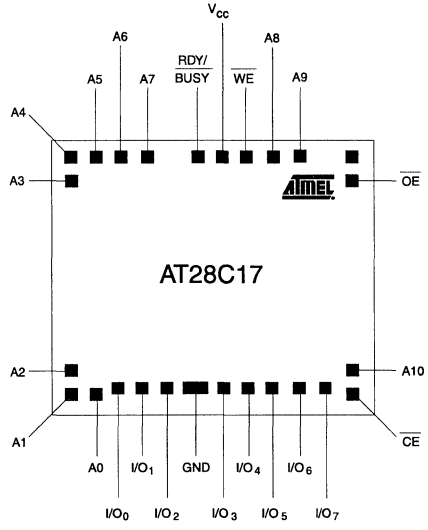
Signal Name	X (µ)	Y (µ)
I/O_1	-610	-1190
I/O_2	-360	-1190
I/O_3	230	-1190
I/O_4	480	-1190
I/O_5	740	-1190
I/O_6	990	-1190
I/O_7	1250	-1190
GND	-60	-1190
V_{CC}	210	1230
$\overline{WE}$	1630	1230
$\overline{OE}$	1630	1000
$\overline{CE}$	1630	-1220

* Coordinates are calculated from die center point

AT28C17 Die Map

Die Size: 137 X 117 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (µ)	Y (µ)
A_0	-1130	-1270
A_1	-1420	-1270
A_2	-1420	-920
A_3	-1370	950
A_4	-1370	1230
A_5	-1140	1230
A_6	-900	1230
A_7	-660	1230
A_8	680	1230
A_9	920	1230
A_{10}	1630	-1000
I/O_0	-870	-1190
I/O_1	-610	-1190

Signal Name	X (µ)	Y (µ)
I/O_2	-360	-1190
I/O_3	230	-1190
I/O_4	480	-1190
I/O_5	740	-1190
I/O_6	990	-1190
I/O_7	1250	-1190
RDY/$\overline{BSY}$	-100	1230
GND	-60	-1190
V_{CC}	210	1230
$\overline{WE}$	450	1230
$\overline{OE}$	1630	1000
$\overline{CE}$	1630	-1220

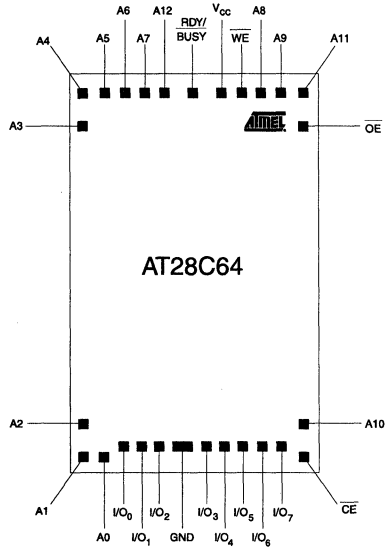
* Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

AT28C64 Die Map

Die Size: 88 X 139 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (μ)	Y (μ)
A_0	-861	-1604
A_1	-1015	-1613
A_2	-1016	-1459
A_3	-987	1308
A_4	-992	1461
A_5	-838	1461
A_6	-685	1461
A_7	-532	1461
A_8	343	1461
A_9	496	1461
A_{10}	908	-1406
A_{11}	872	1506
A_{12}	-378	1461
I/O_0	-655	-1557

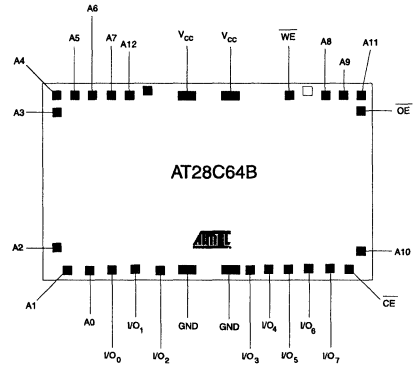
Signal Name	X (μ)	Y (μ)
I/O_1	-494	-1557
I/O_2	-337	-1557
I/O_3	58	-1557
I/O_4	223	-1557
I/O_5	389	-1557
I/O_6	546	-1557
I/O_7	703	-1557
RDY/$\overline{BSY}$	-122	1496
GND	-141	-1634
V_{CC}	32	1471
$\overline{WE}$	189	1461
$\overline{OE}$	870	1294
$\overline{CE}$	903	-1557

* Coordinates are calculated from die center point

AT28C64B Die Map

Die Size: 178 X 120 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (μ)	Y (μ)
A_0	-1721	-1401
A_1	-1966	-1401
A_2	-2142	-1131
A_3	-2142	939
A_4	-2125	1171
A_5	-1884	1171
A_6	-1440	1171
A_7	-1237	1171
A_8	1657	1171
A_9	1832	1171
A_{10}	2035	-1128
A_{11}	2035	1171
A_{12}	-1063	1171
I/O_0	-1425	-1362

Signal Name	X (μ)	Y (μ)
I/O_1	-1126	-1362
I/O_2	-796	-1362
I/O_3	406	-1362
I/O_4	735	-1362
I/O_5	1035	-1362
I/O_6	1365	-1362
I/O_7	1664	-1362
GND	57	-1353
GND	-446	-1353
V_{CC}	-443	1240
V_{CC}	-98	1240
$\overline{WE}$	1272	1171
$\overline{OE}$	2039	939
$\overline{CE}$	1954	-1401

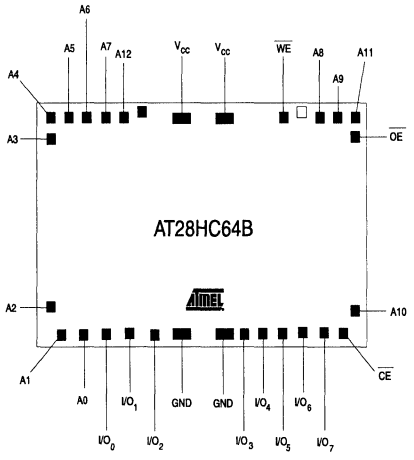
* Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

AT28HC64B Die Map

Die Size: 178 X 120 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (µ)	Y (µ)
A_0	-1721	-1401
A_1	-1966	-1401
A_2	-2142	-1131
A_3	-2142	939
A_4	-2125	1171
A_5	-1884	1171
A_6	-1440	1171
A_7	-1237	1171
A_8	1657	1171
A_9	1832	1171
A_{10}	2035	-1128
A_{11}	2035	1171
A_{12}	-1063	1171
I/O_0	-1425	-1362

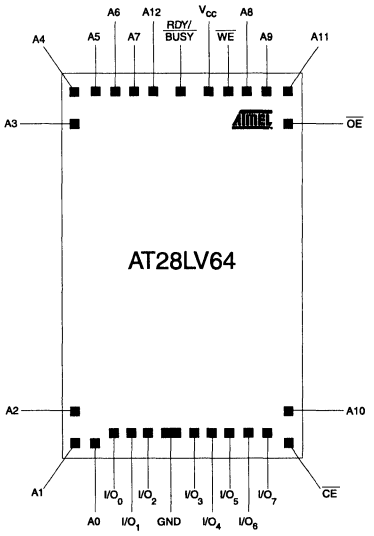
Signal Name	X (µ)	Y (µ)
I/O_1	-1126	-1362
I/O_2	-796	-1362
I/O_3	406	-1362
I/O_4	735	-1362
I/O_5	1035	-1362
I/O_6	1365	-1362
I/O_7	1664	-1362
GND	57	-1353
GND	-446	-1353
V_{CC}	-443	1240
V_{CC}	-98	1240
$\overline{WE}$	1272	1171
$\overline{OE}$	2039	939
$\overline{CE}$	1954	-1401

* Coordinates are calculated from die center point

AT28LV64 Die Map

Die Size: 100 X 168 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (µ)	Y (µ)
A_0	-921	-1867
A_1	-1078	-1867
A_2	-1113	-1710
A_3	-1080	1702
A_4	-1075	1870
A_5	-882	1870
A_6	-721	1870
A_7	-528	1870
A_8	446	1870
A_9	607	1870
A_{10}	1097	-1720
A_{11}	1070	1924
A_{12}	-367	1870
I/O_0	-693	-1826

Signal Name	X (µ)	Y (µ)
I/O_1	-507	-1826
I/O_2	-326	-1826
I/O_3	124	-1826
I/O_4	315	-1826
I/O_5	506	-1826
I/O_6	688	-1826
I/O_7	869	-1826
RDY/$\overline{BSY}$	-77	1924
GND	-100	-1910
V_{CC}	89	1895
$\overline{WE}$	253	1870
$\overline{OE}$	1060	1679
$\overline{CE}$	1090	-1872

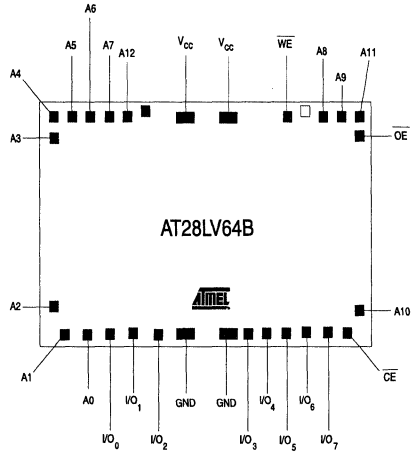
* Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

AT28LV64B Die Map

Die Size: 178 X 120 mils

Connect Substrate to Ground



Die Pad Coordinates *

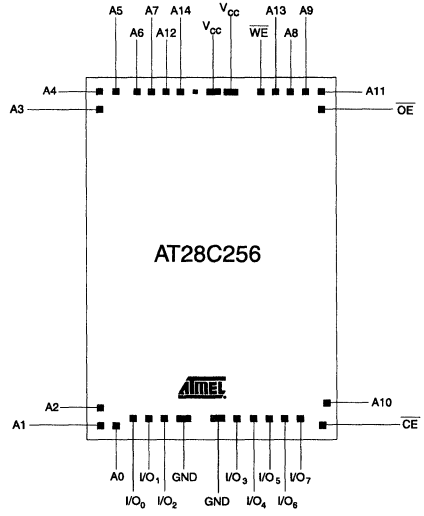
Signal Name	X (μ)	Y (μ)	Signal Name	X (μ)	Y (μ)
A_0	-1721	-1401	I/O_1	-1126	-1362
A_1	-1966	-1401	I/O_2	-796	-1362
A_2	-2142	-1131	I/O_3	406	-1362
A_3	-2142	939	I/O_4	735	-1362
A_4	-2125	1171	I/O_5	1035	-1362
A_5	-1884	1171	I/O_6	1365	-1362
A_6	-1440	1171	I/O_7	1664	-1362
A_7	-1237	1171	GND	57	-1353
A_8	1657	1171	GND	-446	-1353
A_9	1832	1171	V_{CC}	-443	1240
A_{10}	2035	-1128	V_{CC}	-98	1240
A_{11}	2035	1171	$\overline{WE}$	1272	1171
A_{12}	-1063	1171	$\overline{OE}$	2039	939
I/O_0	-1425	-1362	$\overline{CE}$	1954	-1401

* Coordinates are calculated from die center point

AT28C256 Die Map

Die Size: 178 X 242 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (μ)	Y (μ)	Signal Name	X (μ)	Y (μ)
A_0	-1792	-2951	I/O_0	-1416	-2911
A_1	-2037	-2951	I/O_1	-1117	-2911
A_2	-2126	-2711	I/O_2	-787	-2911
A_3	-2126	2490	I/O_3	415	-2911
A_4	-2108	2722	I/O_4	745	-2911
A_5	-1868	2722	I/O_5	1044	-2911
A_6	-1432	2722	I/O_6	1374	-2911
A_7	-1228	2722	I/O_7	1673	-2911
A_8	1658	2722	GND	-438	-2902
A_9	1832	2722	GND	66	-2902
A_{10}	2035	-2677	V_{CC}	-435	2790
A_{11}	2035	2722	V_{CC}	-89	2790
A_{12}	-1054	2722	$\overline{WE}$	1280	2722
A_{13}	1454	2722	$\overline{OE}$	2039	2490
A_{14}	-851	2722	$\overline{CE}$	2035	-2951

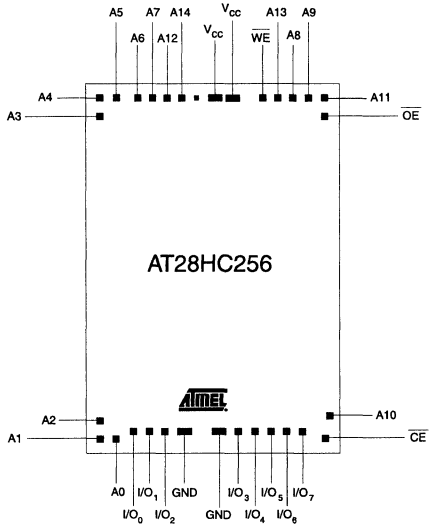
* Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

AT28HC256 Die Map

Die Size: 178 X 242 mils

Connect Substrate to Ground



Die Pad Coordinates *

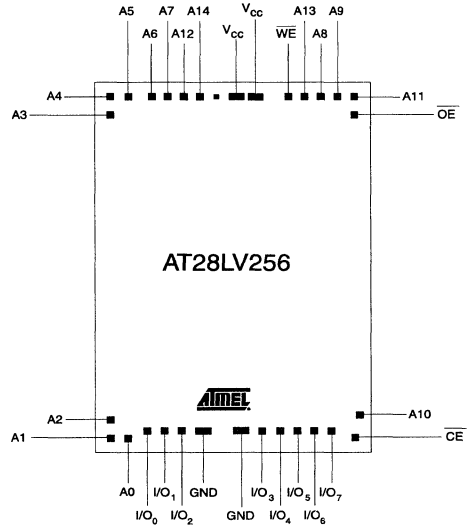
Signal Name	X (µ)	Y (µ)	Signal Name	X (µ)	Y (µ)
A_0	-1792	-2951	I/O_0	-1416	-2911
A_1	-2037	-2951	I/O_1	-1117	-2911
A_2	-2126	-2711	I/O_2	-787	-2911
A_3	-2126	2490	I/O_3	415	-2911
A_4	-2108	2722	I/O_4	745	-2911
A_5	-1868	2722	I/O_5	1044	-2911
A_6	-1432	2722	I/O_6	1374	-2911
A_7	-1228	2722	I/O_7	1673	-2911
A_8	1658	2722	GND	-438	-2902
A_9	1832	2722	GND	66	-2902
A_{10}	2035	-2677	V_{CC}	-435	2790
A_{11}	2035	2722	V_{CC}	-89	2790
A_{12}	-1054	2722	$\overline{WE}$	1280	2722
A_{13}	1454	2722	$\overline{OE}$	2039	2490
A_{14}	-851	2722	$\overline{CE}$	2035	-2951

* Coordinates are calculated from die center point

AT28LV256 Die Map

Die Size: 178 X 242 mils

Connect Substrate to Ground



Die Pad Coordinates *

Signal Name	X (µ)	Y (µ)	Signal Name	X (µ)	Y (µ)
A_0	-1792	-2951	I/O_0	-1416	-2911
A_1	-2037	-2951	I/O_1	-1117	-2911
A_2	-2126	-2711	I/O_2	-787	-2911
A_3	-2126	2490	I/O_3	415	-2911
A_4	-2108	2722	I/O_4	745	-2911
A_5	-1868	2722	I/O_5	1044	-2911
A_6	-1432	2722	I/O_6	1374	-2911
A_7	-1228	2722	I/O_7	1673	-2911
A_8	1658	2722	GND	-438	-2902
A_9	1832	2722	GND	66	-2902
A_{10}	2035	-2677	V_{CC}	-435	2790
A_{11}	2035	2722	V_{CC}	-89	2790
A_{12}	-1054	2722	$\overline{WE}$	1280	2722
A_{13}	1454	2722	$\overline{OE}$	2039	2490
A_{14}	-851	2722	$\overline{CE}$	2035	-2951

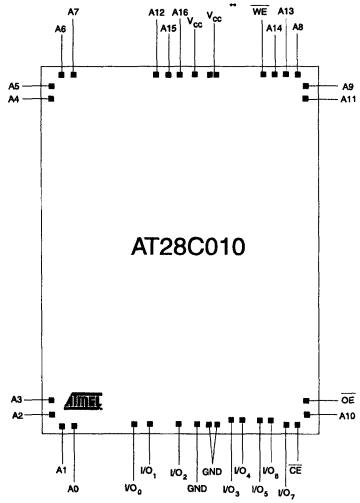
* Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

AT28C010 Die Map

Die Size: 245 X 361 mils

Connect Substrate to Ground



** Indicates Double Bonding

Die Pad Coordinates *

Signal Name	X (μ)	Y (μ)
A_0	-2647	-4318
A_1	-2875	-4318
A_2	-2960	-4053
A_3	-2960	-3825
A_4	-2973	3847
A_5	-2973	4112
A_6	-2673	4280
A_7	-2433	4280
A_8	2611	4274
A_9	2857	4067
A_{10}	2783	-4200
A_{11}	2857	3839
A_{12}	-454	4274
A_{13}	2384	4274
A_{14}	2156	4274
A_{15}	-226	4274
A_{16}	2	4274

Signal Name	X (μ)	Y (μ)
I/O_0	-609	-4399
I/O_1	-274	-4399
I/O_2	62	-4399
I/O_3	950	-4399
I/O_4	1288	-4399
I/O_5	1623	-4399
I/O_6	1961	-4399
I/O_7	2296	-4399
GND	311	-4399
GND	530	-4405
GND	688	-4405
V_{CC}	286	4310
V_{CC}	575	4286
$\overline{WE}$	1928	4274
$\overline{OE}$	2783	-3973
$\overline{CE}$	2716	-4444

* Coordinates are calculated from die center point

Note: Die size is subject to change. Contact the Atmel Sales Representative to confirm die size.

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Each Atmel data sheet includes an Ordering Information Section which specifies the package types available. This section provides size specifications and outlines for all package types.[1]

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28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)	9-5
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)	9-5
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)	9-5
42DW6	42 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)	9-6
28F	28 Lead, Non-Windowed, Ceramic Button-Brazed Flat Package (Flatpack)	9-6
32F	32 Lead, Non-Windowed, Ceramic Button-Brazed Flat Package (Flatpack)	9-6
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32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)	9-7
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)	9-8
42P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)	9-8
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)	9-8
32R	32 Lead, 0.440" Wide, Plastic Gull Wing Small Outline (SOIC)	9-8
44R	44 Lead, 0.440" Wide, Plastic Gull Wing Small Outline (SOIC)	9-10

(continued)

Note: 1. Dimensions shown do not include lead plating or mold flash.

Standard Package Outlines

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Package	Description	See Page
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20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)	9-10
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)	9-10
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)	9-11
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)	9-11
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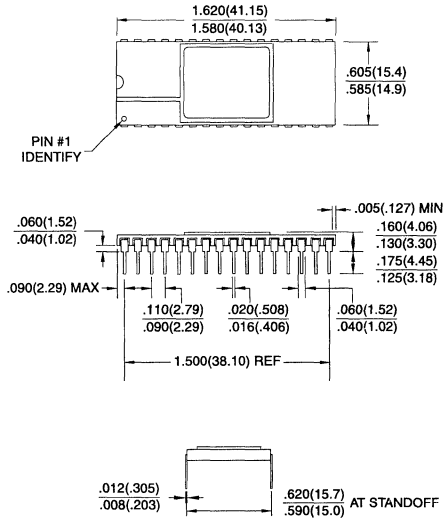
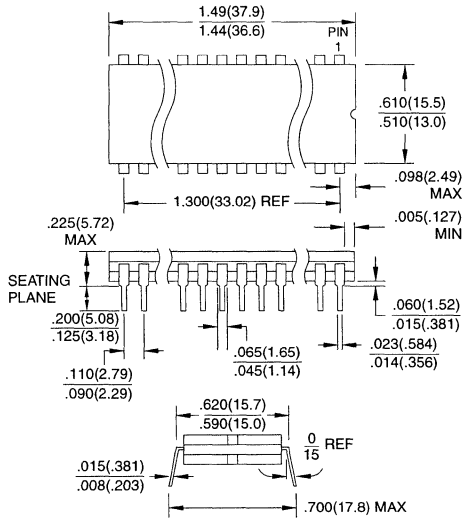
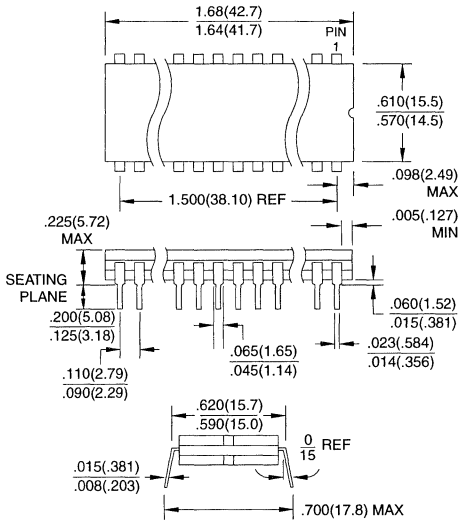
32B, 32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-16 CONFIG C



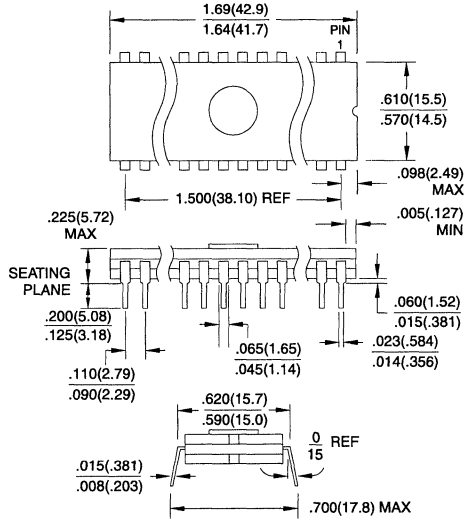
28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-10 CONFIG A



32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-16 CONFIG A

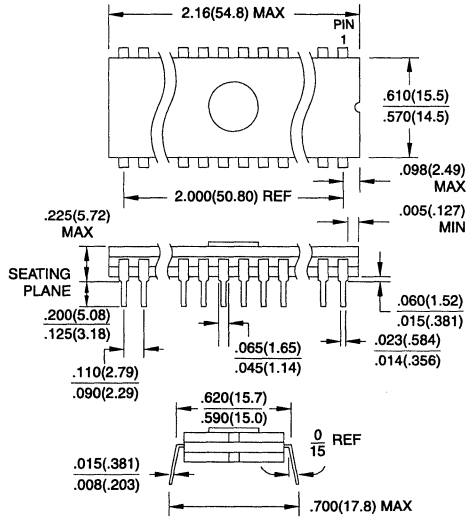


32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-16 CONFIG A

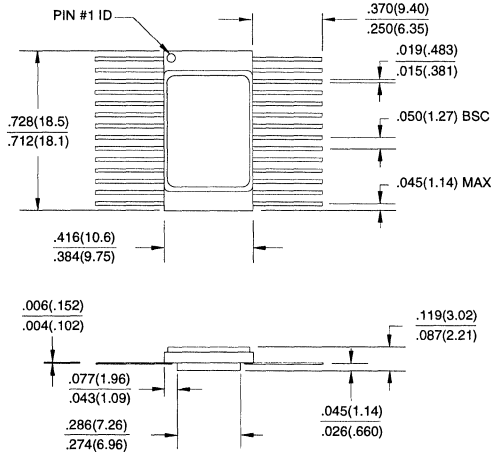


9

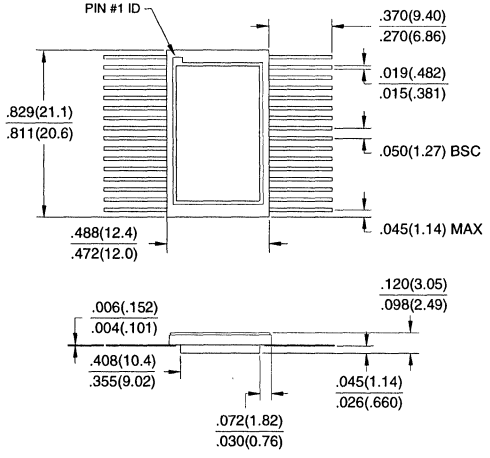
42DW6, 42 Lead, 0.600" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)



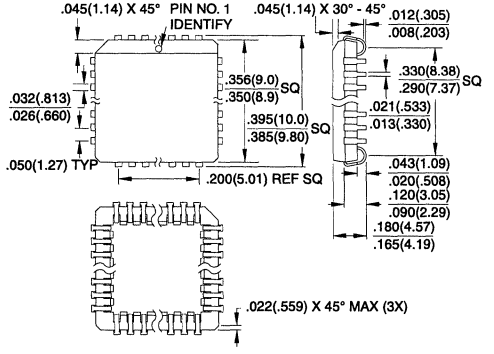
28F, 28 Lead, Non-Windowed,
Ceramic Bottom-Brazed Flat Package (Flatpack)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 F-12 CONFIG B



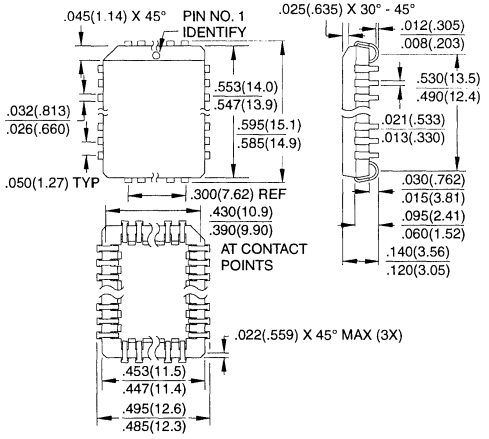
32F, 32 Lead, Non-Windowed,
Ceramic Bottom-Brazed Flat Package (Flatpack)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 F-18 CONFIG B
JEDEC OUTLINE MO-115



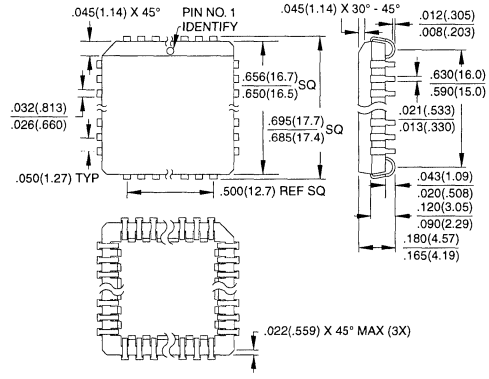
20J, 20 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



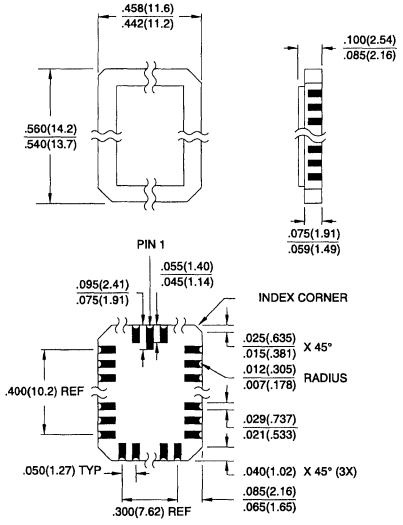
32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-016 AE



44J, 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC

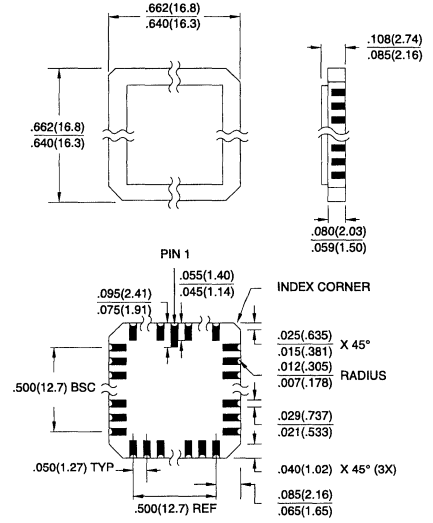


32L, 32 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-12



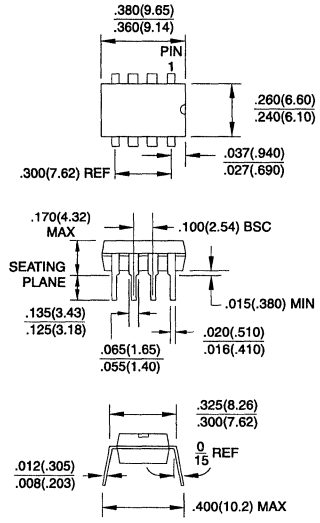
*Ceramic lid standard unless specified.

44L, 44 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-5

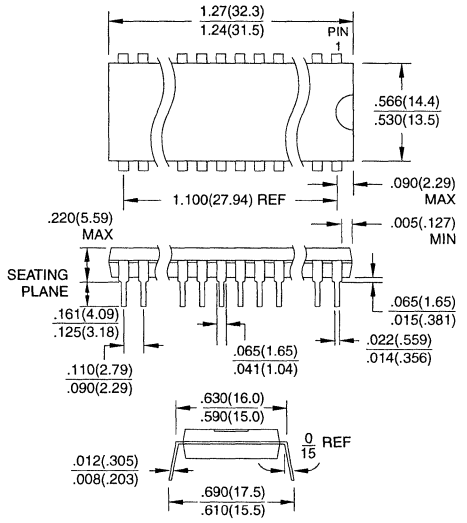


*Ceramic lid standard unless specified.

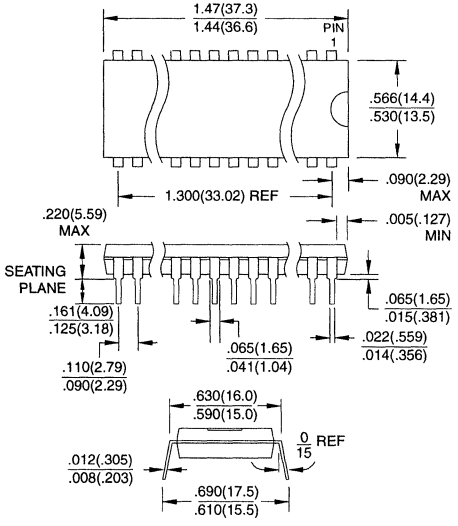
8P3, 8 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 BA



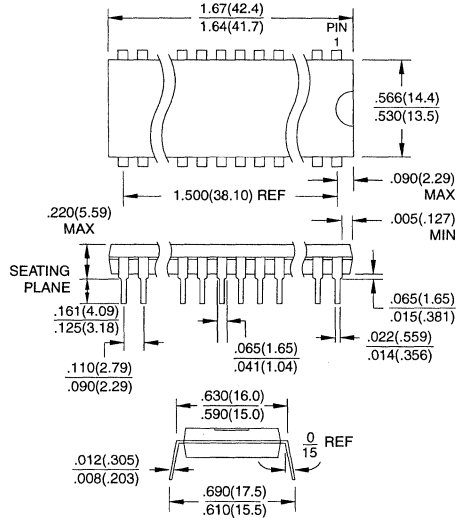
24P6, 24 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AA



28P6, 28 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AB

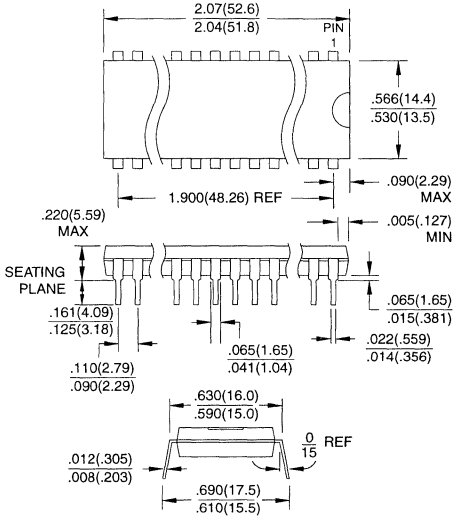


32P6, 32 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)

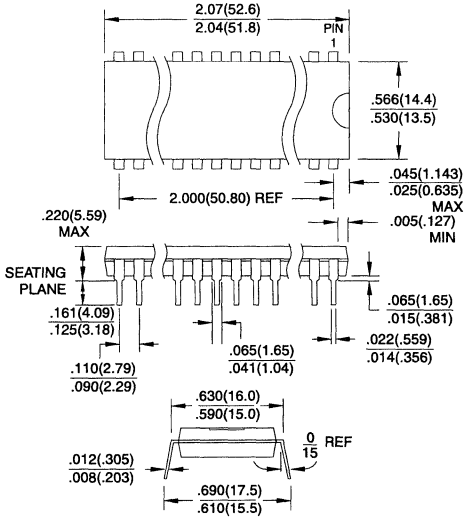


40P6, 40 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)

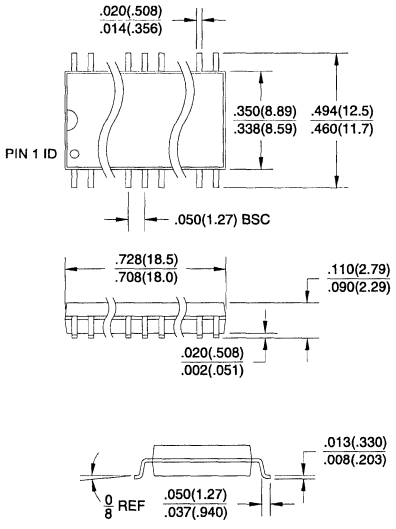
JEDEC STANDARD MS-011 AC



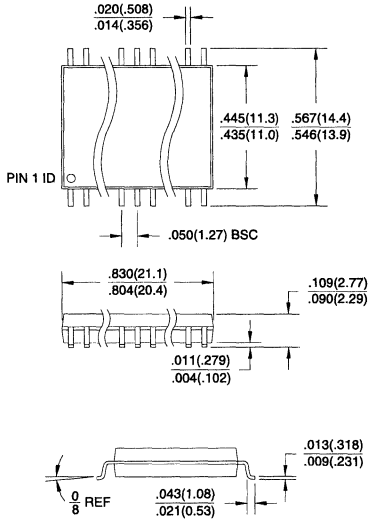
42P6, 42 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



28R, 28 Lead, 0.330" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)

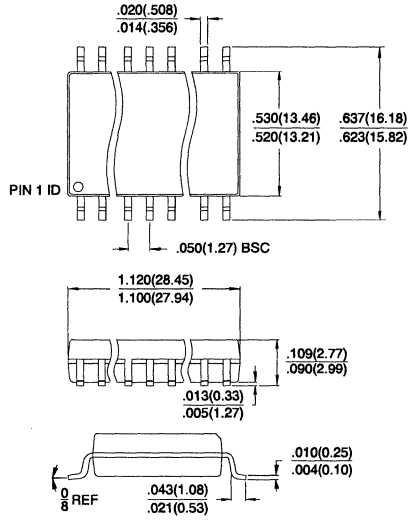


32R, 32 Lead, 0.440" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)

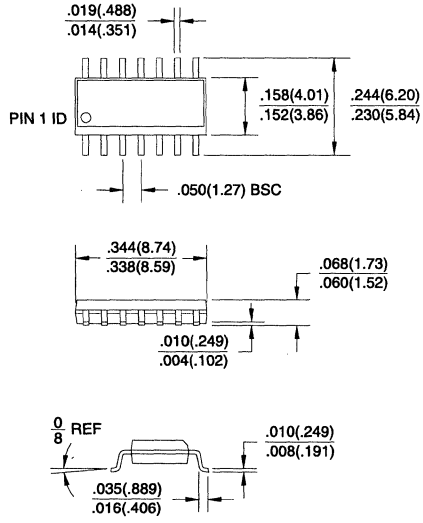


9

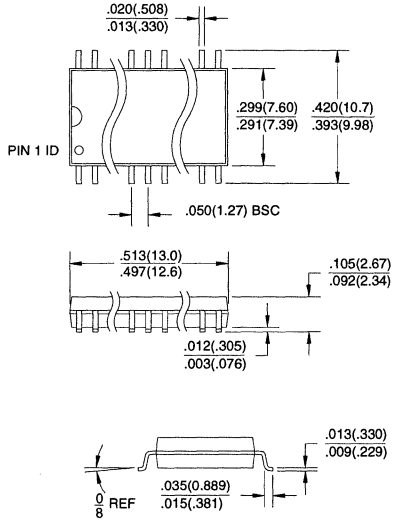
44R, 44 Lead, 0.525" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



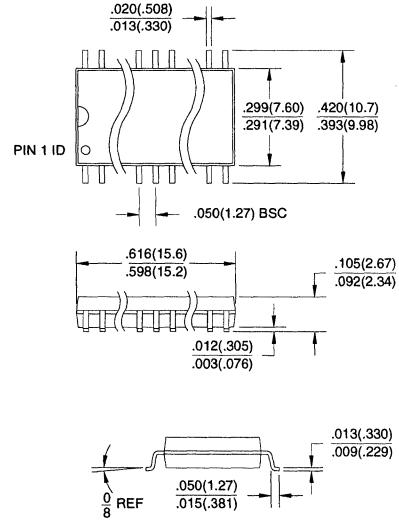
14S, 14 Lead, 0.150" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



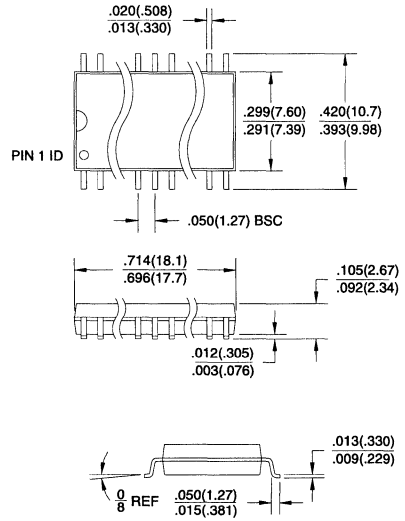
20S, 20 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



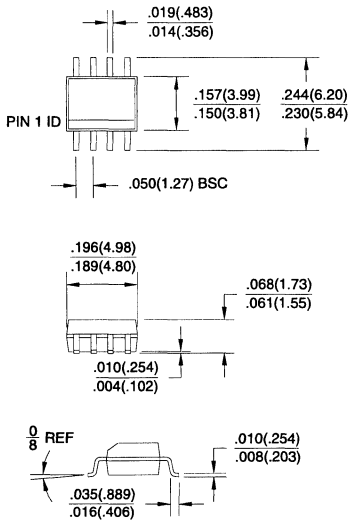
24S, 24 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



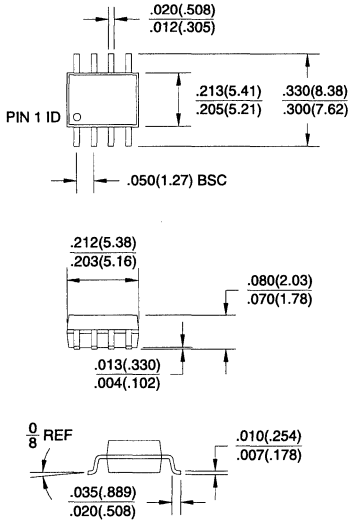
28S, 28 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



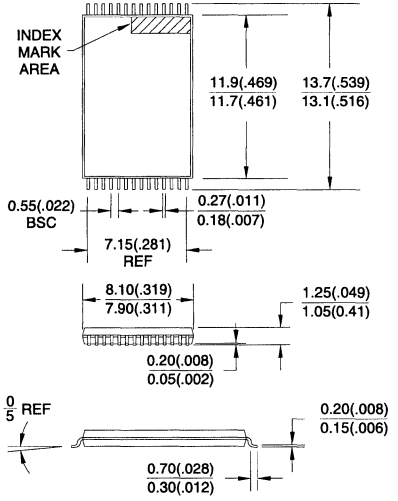
8S1, 8 Lead, 0.150" Wide,
Plastic Gull Wing Small Outline (JEDEC SOIC)
Dimensions in Inches and (Millimeters)



8S2, 8 Lead, 0.200" Wide,
Plastic Gull Wing Small Outline (EIAJ SOIC)
Dimensions in Inches and (Millimeters)



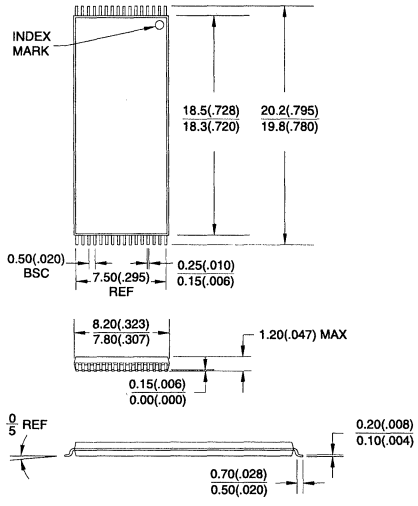
28T, 28 Lead, Plastic Thin Small Outline Package
(TSOP)
Dimensions in Millimeters and (Inches) *



*Controlling dimension: millimeters

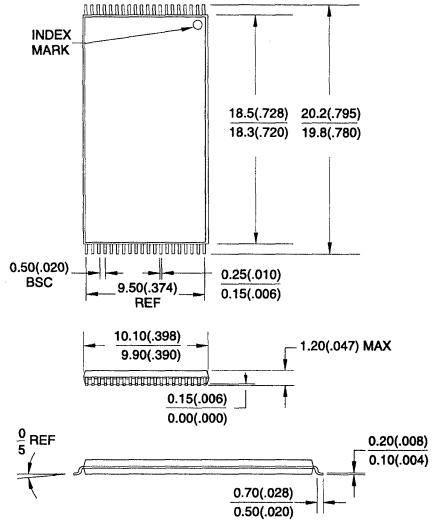
32T, 32 Lead, Plastic Thin Small Outline Package (TSOP) Dimensions in Millimeters and (Inches) *

JEDEC OUTLINE MO-142 BD



*Controlling dimension: millimeters

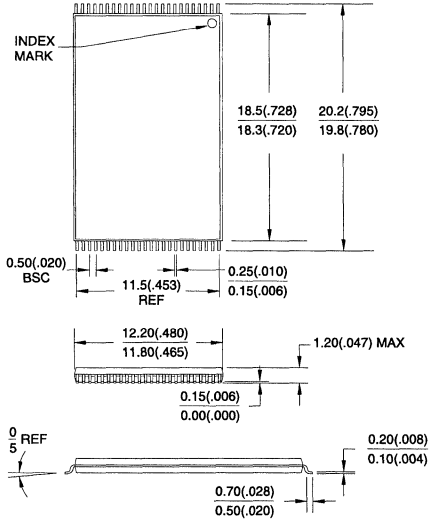
40T, 40 Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches) *



*Controlling dimension: millimeters

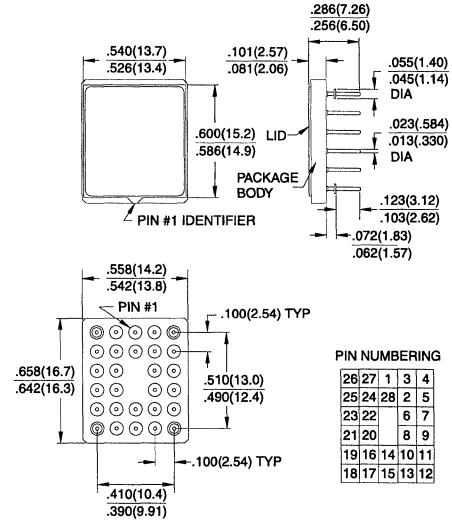
48T, 48 Lead, Plastic Thin Small Outline Package (TSOP) Dimensions in Millimeters and (Inches) *

JEDEC OUTLINE MO-142 DD

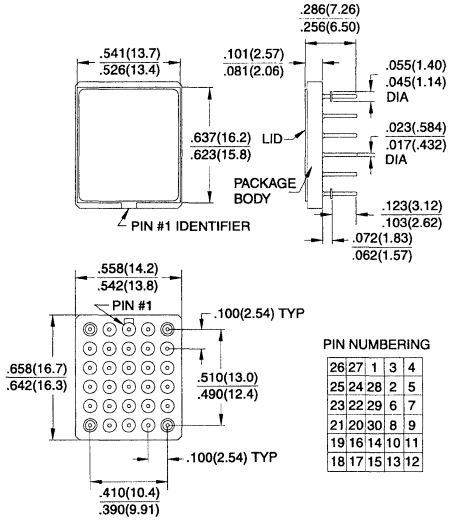


*Controlling dimension: millimeters

28U, 28 Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



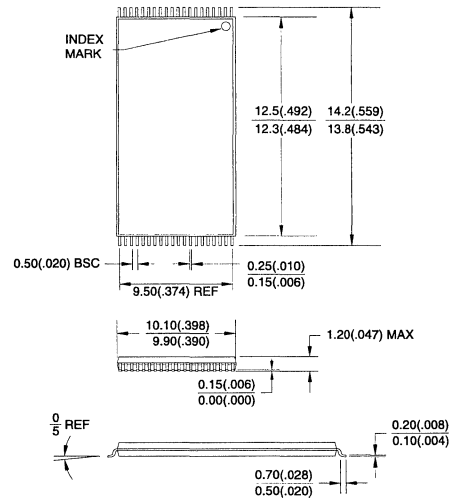
30U, 30 Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



PIN NUMBERING

26	27	1	3	4
25	24	28	2	5
23	22	29	6	7
21	20	30	8	9
19	16	14	10	11
18	17	15	13	12

40V, 40 Lead, Plastic Thin Small Outline Package
(TSOP) Dimensions in Millimeters and (Inches) *
JEDEC OUTLINE MO-142 CA



*Controlling dimension: millimeters

Thermal Characteristics of Atmel Packages

The thermal performance of the semiconductor package is a very important consideration for the board designer. The reliability and functional life of the device is directly related to its junction operating temperature. As the temperature of the device increases, the stability of its junctions decline, as does its reliable life. The thermal performance is also important to the board design, because it may limit the board density, or dictate the board location of high power-dissipating devices, or require expensive cooling methods for the system. As devices have become more complex and boards have become denser, the need to account for the thermal characteristics of packages has shifted from being a minor consideration to being a necessary consideration.

The thermal performance of a package is measured by its ability to dissipate the power required by the device into its surroundings. The electrical power drawn by the device generates heat on the top surface of the die. This heat is conducted through the package to the surface and then transferred to the surrounding air by convection. Each heat transfer step has a corresponding resistance to the heat flow, which is given the value θ, the thermal resistance coefficient. Subscripts are added to the coefficient to specify the two points that the heat is transferred between. Commonly used coefficients are θ_{JA} (junction to ambient air), θ_{JC} (junction to package case), and θ_{CA} (case to ambient air).

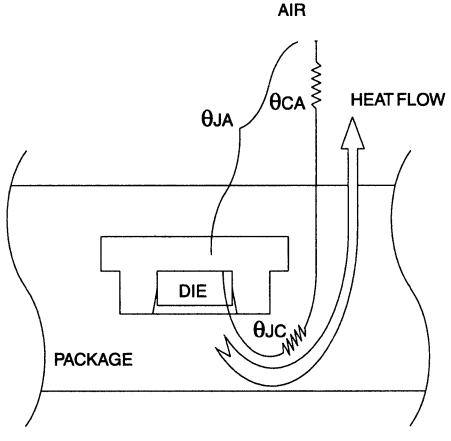
An electrical analogy can be made, as shown in the figure below, to illustrate the heat flow of a package. The heat transfer can be characterized mathematically by the following equation,

$$Tj - Ta = P \times \theta_{JA}$$

where,

P = *Device operating power [watts]*
Tj = *Temperature of a junction on the device [°C]*
Ta = *Temperature of the surrounding ambient air [°C]*

(continued)



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Thermal Characteristics of Atmel Packages (Continued)

Two conclusions can be made after examining this analogy. First, the lower the value of θ_{JA}, the better the heat dissipation of the package. Secondly, the value of θ_{JA} is directly dependent upon both the conductive (θ_{JC}) and convective (θ_{CA}) properties of the package. θ_{JC} is a function of the package material, the adhesion between the package materials, and device size. θ_{CA} is a function of the package size and configuration, package mounting method, and air flow across the package. Lower θ_{JA} values can be achieved by specifying ceramic packages instead of plastic packages, choosing larger packages, or improving air flow across the package.

The thermal resistance values of Atmel standard packages are listed on the following page. The figures shown are maximum values for θ, typical values are lower dependent upon the device type.

Thermal Resistance Coefficients

		θ_{JC} [°CW]	θ_{JA} [°CW] Airflow = 0 ft/min
Ceramic DIP	24D3/DW3	9	65
	24D6/DW6	10-15	45
	28D6/DW6	10-15	45
	32D6/DW6	10	45
	40D6/DW6	7	40
Plastic DIP	24P3	22	82
	24P6	39	82
	28P6	36	77
	32P6	34	72
	40P6	30	68
Leadless Chip Carrier (LCC)	28L/LW	12	68
	32L/LW	10	65
	44L/LW	8-10	60
	68L/LW	6-8	50-60
Plastic Leaded Chip Carrier (PLCC)	28J	16	60
	32J	16	60
	44J	14	50
J-Leaded Chip Carrier (JLCC)	28K/KW	16	72
	32K/KW	16	72
	44K/KW	16	68
	44K/KW	10-14	47
Cerpack	24C/CW	15	81
Flatpack	28F	10	65
	32F	8-10	60
PGA	28U	10	65
Sidebraze	32S	8-10	40-50
TSOP	28T	66	141
	32T	45	113

Available Packing Methods and Quantities

Atmel provides four different packing methods to provide maximum protection for our product and to best suit our customer's needs: 1) Shipping Tubes, 2) Shipping Trays, 3) Unit Packing, and 4) Tape and Reel. These first three methods are our standard pack, but we also provide tape and reel upon customer request.

1. Shipping Tubes

- **Material: Clear polyvinyl chloride**
- **ESD: Topically coated with anti-static solution**

Quantity Per Tube

PACKAGE	LEAD COUNT	PKG CODE	QTY/TUBE
Cerdip (300 mil)	16	D3/DW3	24
	20	D3/DW3	19
	24	D3/DW3	15
Cerdip (600 mil)	24	D6/DW6	16
	28	D6/DW6	14
	32	D6/DW6	12
	40	D6/DW6	10
	42	DW6	9
Flatpack	28	F	15
	32	F	15
LCC	20	L/LW	54
	28	L/LW	42
	32	L/LW	34
	44	L/LW	29
Plastic Dip (300 mil)	8	P3	50
	20	P3	19
	24	P3	15
Plastic Dip (600 mil)	24	P6	16
	28	P6	14
	32	P6	12
	40	P6	10
	42	P6	10
PLCC	20	J	48
	28	J	38
	32	J	32
	44	J	27

(continued)

Quantity Per Tube (Continued)

PACKAGE	LEAD COUNT	PKG CODE	QTY/TUBE
SOIC (150 mil)	8	S1	100
	14	S	56
SOIC (210 mil)	8	S2	94
SOIC (300 mil)	20	S	31
	24	S	31
	28	S	27
SOIC (330 mil)	28	R	26
	32	R	22
SOIC (450 mil)	32	R	23
Sidebraze	32	B	12

2. Shipping Trays

- **Conforms to JEDEC Thin Matrix Tray outlines**
- **Bakeable and Conductive**

Quantity Per Tray

PACKAGE	LEAD COUNT	PKG CODE	QTY/TRAY
TSOP	28	T	234
	32	T	156
	40	T	120
	40	V	160
	48	T	96

3. Unit Pack/Boxes

- **In order to maximize protection, each unit is packed in specially designed carriers/boxes.**

Quantity Per Unit Pack/Box

PACKAGE	LEAD COUNT	PKG CODE	METHOD	QTY
Pin Grid Array	28	U	Box	20
	30	U	Box	20

4. Tape and Reel

- **Meets or exceeds the requirements of EIA-481-x, Carrier Taping of SMC for Automated Handling**
- **Material: Carrier Tape = Black, conductive PVC or polystyrene**
  Cover Tape = Clear, anti-static polyester film
  Reel = 13 inch diameter plastic reel; 7 inch diameter plastic reel used for 500 piece quantities
- **Each reel is individually packed into its own box, with a bar code label attached to both the reel and box**

Quantity Per Reel

PACKAGE	LEAD COUNT	PKG CODE	WIDTH	PITCH	QTY
PLCC	28	J	24 mm	16 mm	750
	32	J	24 mm	16 mm	750
	44	J	32 mm	24 mm	500
SOIC(150 mil)	8	S1	12 mm	8 mm	Up to 3000 in 500 piece increments
	14	S	12 mm	8 mm	
SOIC(210mil)	8	S2	16 mm	12 mm	Up to 2000 in 500 piece increments
SOIC(300mil)	20	S	24 mm	12 mm	1000
	24	S	24 mm	12 mm	1000
	28	S	24 mm	12 mm	1000
SOIC(330mil)	28	R	24 mm	16 mm	1000
TSOP	28	T	24 mm	12 mm	2000
	32	T	32 mm	16 mm	1500
	40	T	32 mm	16 mm	1250

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E^2 Logic Family: E^2PROM + Gate Array

Device Name	E^2PROM Bits	Number of Usable Gates	Number of I/O	Package Type
AT88SC200	2,048	800	8	PDIP/SOIC
AT88SC210	2,048	1,000	64	PQFP/TQFP/PLCC
AT88SC230	2,048	3,300	100	PQFP/TQFP/PLCC
AT88SC2100	2,048	10,000	48	PQFP/TQFP/PLCC
AT88SC410	4,096	1,300	24	PDIP/SOIC
AT88SC1610	16,384	1,500	8	PDIP/SOIC
AT88SC16350	16,384	35,000	144	PQFP/TQFP

Microcontrollers

Part Number	Memory Size	Description
AT89C51	4K x 8	80C31 Microcontroller with 4K bytes Flash
AT89LV51	4K x 8	2.7-Volt, 80C31 Microcontroller with 4K bytes Flash
AT89C52	8K x 8	80C32 Microcontroller with 8K bytes Flash
AT89LV52	8K x 8	2.7-Volt, 80C32 Microcontroller with 8K bytes Flash
AT89C1051	1K x 8	80C31 Microcontroller with 1K bytes Flash, 20-Pin Package
AT89C2051	2K x 8	80C31 Microcontroller with 2K bytes Flash, 20-Pin Package
AT89S8252	8K x 8	Downloadable Microcontroller with 8K bytes Flash and 2K bytes E^2PROM
AT89C55	20K x 8	80C32 Microcontroller with 20K bytes Flash

Flash Memory Cards

Part Number	Organization	Vcc	Description
AT5FC001	1M byte	5-Volt	PCMCIA Compatible Flash Memory Card
AT5FC002	2M byte	5-Volt	PCMCIA Compatible Flash Memory Card
AT5FC004	4M byte	5-Volt	PCMCIA Compatible Flash Memory Card
AT5FC008	8M byte	5-Volt	PCMCIA Compatible Flash Memory Card

(Cache Logic™ FPGAs)

Part Number	Registers	Usable Gates	Frequency	Description
AT6002	1.024	2K-4K	250 MHz	96 I/O Pins, 5-Volt, Very Low Power
AT6003	1,600	3K-6K	250 MHz	120 I/O Pins, 5-Volt, Very Low Power
AT6005	3,136	5K-10K	250 MHz	108 I/O Pins, 5-Volt, Very Low Power
AT6010	6,400	10K-20K	250 MHz	204 I/O Pins, 5-Volt, Very Low Power
Low Voltage				
AT6002LV	1.024	2K-4K	250 MHz	96 I/O Pins, 3-Volt, Very Low Power
AT6003LV	1,600	3K-6K	250 MHz	120 I/O Pins, 3-Volt, Very Low Power
AT6005LV	3,136	5K-10K	250 MHz	108 I/O Pins, 3-Volt, Very Low Power
AT6010LV	6,400	10K-20K	250 MHz	204 I/O Pins, 3-Volt, Very Low Power

FPGA Design Development Software

FPGA design tools are available across a broad range of CAE tool vendors and PC and workstation platforms. Design methods supported include: schematic capture, logic synthesis (VHDL and Verilog), PLD entry (ABEL and CUPL), and automatic component generation of hard macros for user-parametrized structured logic (arithmetic elements, counters, registers, encoders, decoders, and other common functions). Refer to current Configurable Logic Data Book.

CAE Tool Support:

Cadence, Exemplar, Intergraph, Mentor, Synopsys, ViewLogic.

Platform Support:

PC, SUN Workstations, HP Workstations.

0573A

Gate Arrays/Embedded Arrays

Part Number	Gates	Description
ATL50 Series	4K-1120K	0.5-Micron CMOS Gate Array, 2.0-Volt & 3.3-Volt Mixed Voltage Operation, 16 Versions with Various Pin & Gate Counts, Memory, Megacells
ATLS60 Series	12.5K-150K	0.6-Micron CMOS Gate Array, 3.3-Volt & 5.0-Volt Operation, Staggered Row Bond Pads, 8 Versions with Various Pin & Gate Counts, Memory, Megacells
ATL60 Series	4K-1120K	0.6-Micron CMOS Gate Array, 3.3-Volt & 5.0-Volt Operation, 16 Versions with Various Pin & Gate Counts, Memory, Megacells
ATL80 Series	2K-600K	0.8-Micron CMOS Gate Array, 3.3-Volt & 5.0-Volt Operation, 12 Versions with Various Pin & Gate Counts, Memory, Megacells
ATLV Series	2K-35K	1.0-Micron CMOS Gate Array, 1.0-Volt & 3.3-Volt Operation, 8 Underlayers with Various Pin & Gate Counts, Memory, Megacells

Cell-Based ICs

Part Number	Description
ECDM05	0.5-Micron CMOS Cell-Based IC Family, 3.3-Volt Operation, Digital, Analog, Memory, Megacells
ECLP07	0.7-Micron CMOS Cell-Based IC Family, 3.3-Volt Operation, Digital, Analog, Memory, Megacells
ECPD07	0.7-Micron CMOS Cell-Based IC Family, 5.0-Volt Operation, Digital, Analog, Memory, Megacells
ECPD10	1.0-Micron CMOS Cell-Based IC Family, 5.0-Volt Operation, Digital, Analog, Memory, Megacells

Programmable Logic Devices

Part Number	Packages	Speeds	Description
Flash-Based			
ATF16V8B	20-Pin	7.5-25 ns	8 FFs, 8 I/O Pins, Standard Power
ATF16V8BQ,BQL	20-Pin	10-25 ns	8 FFs, 8 I/O Pins, Quarter Power, Low Power
ATF16V8C	20-Pin	5-7.5 ns	8 FFs, 8 I/O Pins, Standard Power
ATF16V8CZ	20-Pin	10-15 ns	8 FFs, 8 I/O Pins, Zero Power
ATF20V8B	24-Pin, 28-Pin	7.5-25 ns	8 FFs, 8 I/O Pins, Standard Power
ATF20V8BQ,BQL	24-Pin, 28-Pin	10-25 ns	8 FFs, 8 I/O Pins, Quarter Power, Low Power
ATF22V10B	24-Pin, 28-Pin	7.5-25 ns	10 FFs, 10 I/O Pins, Standard Power
ATF22V10BQ,BQL	24-Pin, 28-Pin	15-25 ns	10 FFs, 10 I/O Pins, Quarter Power, Low Power
ATF22V10C	24-Pin, 28-Pin	5-7.5 ns	10 FFs, 10 I/O Pins, Standard Power
ATF22V10CZ	24-Pin, 28-Pin	10-15 ns	10 FFs, 10 I/O Pins, Zero Power
ATF1500,L	44-Pin	7.5-25 ns	32 FFs, 32 I/O Pins, Standard Power & Low Power
Low Voltage			
ATF16LV8C	20-Pin	10-15 ns	8 FFs, 8 I/O Pins, Low Voltage
ATF16LV8CZ	20-Pin	15-25 ns	8 FFs, 8 I/O Pins, Low Voltage, Zero Power
AT22LV10,L	24-Pin, 28-Pin	20-30 ns	10 FFs, 10 I/O Pins, Standard & Low Power
ATLV750B,BL	24-Pin, 28-Pin	10-15 ns	20 FFs, 10 I/O Pins, Standard & Low Power
ATF1500LV,L	44-Pin	12-25 ns	32 FFs, 32 I/O Pins, Standard & Low Power
5-Volt, EPROM-Based			
AT22V10,L	24-Pin, 28-Pin	15-25 ns	10 FFs, 10 I/O Pins, Standard & Low Power
AT22V10B	24-Pin, 28-Pin	7.5-10 ns	10 FFs, 10 I/O Pins, Standard Power
ATV750,L	24-Pin, 28-Pin	20-25 ns	20 FFs, 10 I/O Pins, Standard & Low Power
ATV750B,BL	24-Pin, 28-Pin	7.5-25 ns	20 FFs, 10 I/O Pins, Standard & Low Power
ATV2500H,L	40-Pin, 44-Pin	25-35 ns	48 FFs, 24 I/O Pins, Standard & Low Power
ATV2500B,BL	44-Pin	12-20 ns	48 FFs, 24 I/O Pins, Standard & Low Power
ATV2500BQ,BQL	40-Pin, 44-Pin	20-25 ns	48 FFs, 24 I/O Pins, Quarter Power, Low Power

Programmable Logic Device Design Software

Part Number	Description
ATDS1100PC	Atmel - Synario Entry
ATDS1120PC	Atmel - Synario Verilog Simulation
ATDS1130PC	Atmel - Synario VHDL Synthesis
ATDS1110PC	Atmel - ABEL (Windows Version)
ATDS1210PC	Atmel - ABEL (DOS Version)
ATDS1320PC	Atmel - ProPLD ViewLogic System

Secure Memory ICs

Part Number	Memory Size	Description
AT88SC101	1024 x 1	1K Serial E^2PROM with Security, 1 Memory Zone, 1024 Bits
AT88SC102	1024 x 1	1K Serial E^2PROM with Security, 2 Memory Zones, 512 Bits Each
AT88SC103	1536 x 1	1K Serial E^2PROM with Security, 3 Memory Zones, 512 Bits Each
AT88SC1601	15,872 x 1	16K Serial E^2PROM with Security, 1 Memory Zone, 15,872 Bits
RF ID ASICs	Up to 16K x 1	Analog, Digital & Memory on Single-Chip ASIC

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PIONEER STANDARD ELECTRONICS
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ARROW/SCHWEBER ELECTRONICS
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37 Skyline Dr.
Lake Mary, FL 32746
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INSIGHT ELECTRONICS, INC.
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Altamonte Springs, FL 32701
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2840 Scherer Drive, Suite 410
St. Petersburg, FL 33716
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MARSHALL INDUSTRIES
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MILGRAY/CHICAGO
Kennedy Corporate Center 1
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Fairfield, NJ 07004
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Townline Road
Rochester, NY 14623
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Endicott, NY 13760
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1250 Scottsville Road
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Farmingdale, NY 11735
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840 Fairport Park
Fairport, NY 14450
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FAX (212) 971-0374

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Woodbury, NY 11797
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ZEUS ELECTRONICS
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MARSHALL INDUSTRIES
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