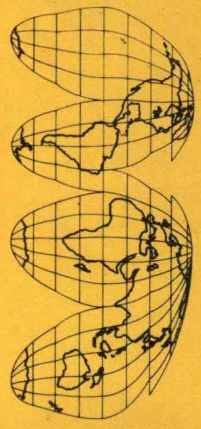
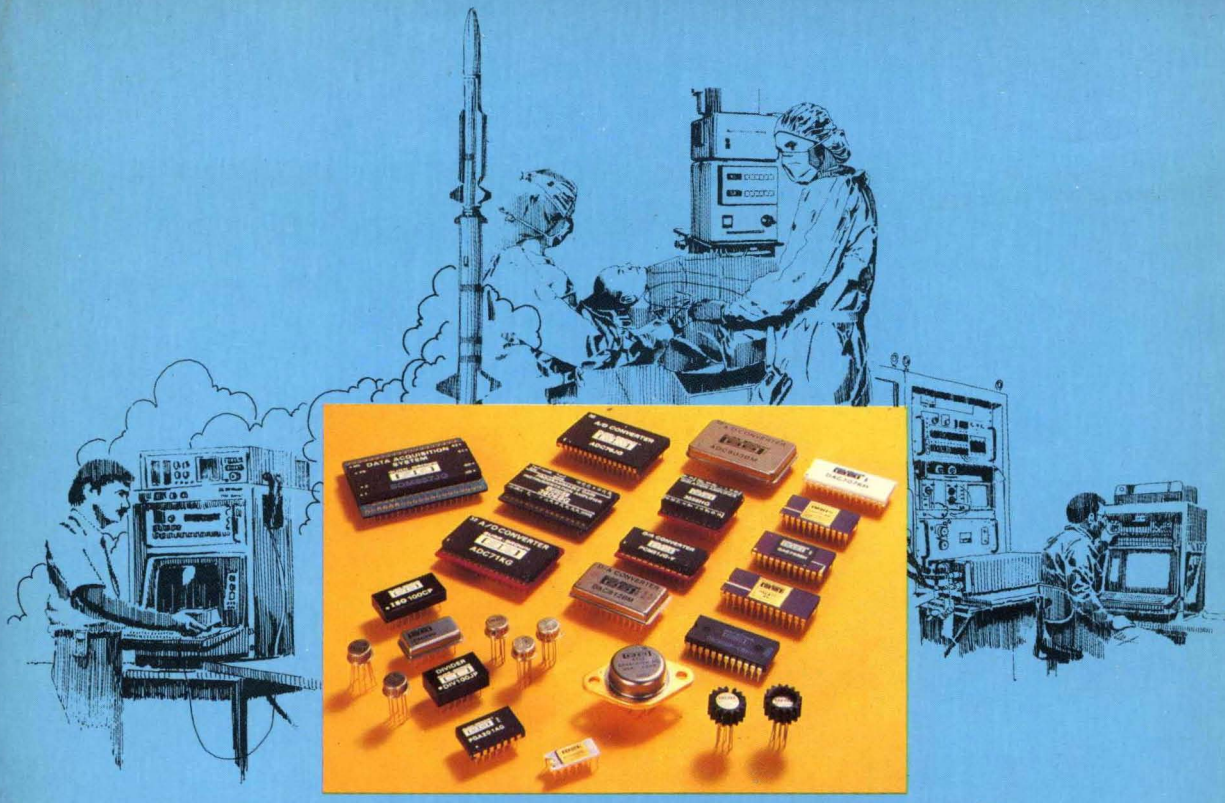
BURR-BROWN®



BURR-BROWN product data book



product data book

BURR-BROWN®

MODEL INDEX

A complete price list for these products is located inside the back cover.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734
Telephone 602-746-1111 - TWX 910-952-1111 - Cable BBRCORP - Telex 66-6491

PRODUCT DATA BOOK

The information in this publication has been carefully checked and is believed to be reliable; however, no responsibility is assumed for possible inaccuracies or omissions. Specifications and prices are subject to change without notice. No patent rights are granted to any of the circuits described herein.

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LI-300

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Building An Unequalled Reputation, Worldwide, for Quality, Performance, Reliability

Data acquisition, signal conditioning, and computer I/O components and systems from Burr-Brown are recognized and used worldwide. Over the past two decades these products have earned a reputation for superior quality, exceptional performance, and consistent reliability—perhaps the best reputation for workmanship in our industry.

Cost effectiveness of our products has been proven in a host of applications: in industrial and process control, test instrumentation, aerospace systems, environmental monitoring, medical-clinical, and analytical instrumentation.

We have built our credibility by being totally responsive to our customers' requirements. Knowing the problems encountered in the real world, we apply the best, most appropriate, and proven technologies to achieve practical solutions.

Our components have become more complex, more sophisticated as we continue to combine and vertically integrate multiple functions into smaller, space-saving packages. When you select these versatile "mini-systems" your design and assembly time is decreased while your products' performance and reliability are increased. And today you pay less, per function, as these microcircuits and subsystems work more efficiently for you.

At Burr-Brown, quality and reliability are built-in by conservative designs, carefully selected components and manufacturing processes, by intensive, thorough testing, and stringent quality control.

Customers also give Burr-Brown high marks for service and support. Our technical literature is among the best in the industry and our global applications and sales force is factory trained—highly qualified to help you in product selection and use. Wherever in the world you contact us, you can be assured of prompt, courteous, efficient service—and superb product performance.

BURR-BROWN PRODUCT DATA BOOK

The Burr-Brown Product Data Book contains detailed product data sheets for our broad line of precision components for signal processing, data acquisition, and data transmission. In addition, it includes supplementary data for these components, such as screening programs available, a list of other technical literature that you may order, accessories, and information on how to interface with Burr-Brown.

To acquaint you with the full breadth of the Burr-Brown product line, we also include information on the products from our Data Acquisition And Control Systems Division. Additional detailed manuals are available for most of these products upon request. Contact your local Burr-Brown Sales Office listed inside the back cover.

For your convenience the Data Book is separated into 17 major sections: Operational Amplifiers, Instrumentation Amplifiers, Isolation Amplifiers, Analog Circuit Functions, Analog-to-Digital Converters, Digital-to-Analog Converters, Sample/Hold Amplifiers, Data Acquisition Subsystems, CMOS Multiplexers, Voltage-to-Frequency Converters, Military Products, Modular Power Supplies, Data Entry and Display Terminals, Microcomputer Input/Output Systems, Data Acquisition and Control Systems, Personal Computer Instrumentation, and Accessories. Each right-hand page has a margin tab on the outer edge which indicates both product type and part number. The tab index on page V provides a visual guide to the major sections.

At the beginning of each product section, you will find explanatory material and a selection guide to assist you in selecting the product most suitable for your applications. The selection guide also contains page numbers for individual product data sheets.

An index of products in this Data Book, listed in alphanumeric order, is found on the inside of the front cover. A general table of contents appears on page IV.

TABLE OF CONTENTS

TAB INDEX

INTERFACING WITH BURR-BROWN

PLACING AN ORDER

Orders may be placed via mail, telephone, TWX or TELEX with any authorized Burr-Brown field sales office, sales representative, or our headquarters in Tucson. Our offices are listed inside the back cover of this Data Book. When placing your order, please provide complete information, including model number with all option designations, product description or name, quantity desired, and ship-to and bill-to addresses.

TECHNICAL ASSISTANCE

Burr-Brown has a large and competent field sales force, backed-up by an experienced staff of applications specialists. They will be most happy to assist you in selecting the right product for your application. This service is available, without charge, from all sales offices and from our headquarters in Tucson.

DATA SHEETS/LITERATURE

Product data sheets or manuals, similar to those in this Data Book but perhaps containing more recent revisions, are available for most of the products listed in this Data Book. Application Notes and other supporting literature are also available on request. If you wish a copy of any of these items simply contact your nearest Burr-Brown sales office or representative.

PRICES AND TERMS

Prices listed in this catalog, unless otherwise noted, apply only to domestic USA customers; all other customers should contact their local Burr-Brown representative for price information.

All prices are FOB Tucson, Arizona, USA, in U.S. dollars. Applicable federal, state, and local taxes are extra. Terms are net 30 days. Prices and specifications are subject to change without notice.

QUOTATIONS

Price quotations made by Burr-Brown or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement.

RETURNS AND WARRANTY SERVICE

When returning products for any reason, it is necessary to contact Burr-Brown, prior to shipping, for authorization and shipping instructions. In the U.S., contact our Tucson headquarters. In other countries, contact your nearest Burr-Brown field sales office or representative. Returned units should be shipped prepaid and must be accompanied by the original purchase order number and date, and an explanation of the malfunction. Upon receipt of the returned unit, Burr-Brown will verify the malfunction and will inform you of the warranty status, cost to repair or replace, credits, and status of replacement units where applicable.

HIGH RELIABILITY PROGRAMS

Burr-Brown is committed to providing products of high quality and reliability. This is manifested by designing for conservative stress levels, careful selection of components and processes, comprehensive testing procedures, thorough quality control practices, and optional programs of military screening. The Burr-Brown Q-Progam, described below, is intended as a reliable enhancement of standard Burr-Brown products by subjecting them to a defined program of environmental stresses.

An even more comprehensive reliability program, aimed particularly at the needs of military customers, is the /MIL program which includes manufacturing procedures per MIL-M-38510 and screening procedures per MIL-STD-883. This program, and the products available under it, are described in section eleven of this Data Book.

THE Q-PROGRAM

The Burr-Brown Q-Program is designed to further enhance the reliability of Burr-Brown microcircuits at a reasonable cost. The Q-Program is appropriate for some military and aerospace applications, industrial control systems, medical patient monitoring instrumentation, and other applications where failure may be expensive or where replacement of parts is difficult and inconvenient. The Q-Program consists of the screening of standard Burr-Brown microcircuits in accordance with applicable test methods of MIL-STD-883. The screening sequences shown below identify the mechanical, electrical, and thermal stresses applied to all Q-Products.

Q-SCREENING SEQUENCE

STEP	SCREEN	PROCEDURE
Routinely performed 100% on all Burr-Brown products	INTERNAL VISUAL INSPECTION (precap)	Burr-Brown QC4118 (copies available on request)
	ELECTRICAL TEST, 100% (postcap)	Per appropriate Burr-Brown product data sheet
①	STABILIZATION BAKE	MIL-STD-883, Method 1008
②	TEMPERATURE CYCLING	MIL-STD-883, Method 1010
③	HERMETICITY, GROSS LEAK	MIL-STD-883, Method 1014
④	HERMETICITY, FINE LEAK	MIL-STD-883, Method 1014
⑤	BURN-IN	MIL-STD-883, Method 1015
⑥	CONSTANT ACCELERATION (centrifuge)	MIL-STD-883, Method 2001
⑦	FINAL ELECTRICAL TEST	Per appropriate Burr-Brown product data sheet

Explanation of Screening Steps...

- **INTERNAL VISUAL INSPECTION**

This is a microscopic examination of the product performed prior to capping in order to verify conformance to Burr-Brown standards of quality for material, methods of construction, and workmanship. Its purpose is to detect and eliminate devices with internal defects which could lead to failures under the thermal, mechanical, and electrical stresses of extended operation.

- **100% ELECTRICAL TEST**

Each product is tested in accordance with the appropriate Burr-Brown product data sheet. These tests will normally include static and dynamic tests at +25°C, as well as drift tests over the operating temperature range.

①STABILIZATION BAKE

In this step the product is stored at an elevated temperature without electrical stress applied. The purpose is to stabilize circuit parameters through accelerated aging.

②TEMPERATURE CYCLING

The product is alternately exposed to extremes of high and low temperature such as would be experienced when parts or equipment are transferred to and from heated shelters in arctic areas. The purpose is to check for permanent changes in operating characteristics and physical damage resulting principally from variation in dimensions and other physical properties.

③④HERMETICITY - GROSS AND FINE LEAK

The purpose of these two tests is to verify the hermeticity of the seal of integrated circuits having internal cavities which are evacuated or filled with gas. The test is intended to determine those devices which, when exposed for long periods to atmosphere containing high concentration of water vapor or other gaseous contaminants, would degrade in performance and become latent failures.

⑤BURN-IN

During burn-in the device is subjected to a high temperature for an extended period of time, with power applied. The burn-in screen is performed in order to eliminate marginal devices with inherent defects. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions.

⑥CONSTANT ACCELERATION

This test subjects the product to a constant acceleration force in a centrifuge. The purpose is to detect and eliminate devices having structural and mechanical weaknesses that could lead to failure when subjected to mechanical stresses during application.

⑦FINAL ELECTRICAL TEST

This is a repetition of the 100% electrical test above. Devices which pass this test, after successfully passing the above screening test, are qualified as Q-parts.

HANDLING PROCEDURES FOR MICROCIRCUITS

In developing handling procedures for microcircuits it is well to keep in mind that virtually all semiconductor devices are vulnerable in some degree to damage from the discharge of electrostatic energy. This is due to the small dimensions involved. It should be noted that electrostatic damage (ESD) to semiconductor devices can cause effects ranging from a degradation in performance, to latent failure, or immediate failure, of the device involved.

We at Burr-Brown are directly concerned with this subject because our products are designed to achieve the highest performance and precision. Often, this depends upon a high degree of device matching or precision within the microcircuit and any degradation due to ESD is unacceptable. Accordingly, we have developed a set of guidelines that will minimize the exposure of our products to possible electrostatic damage during manufacturing and handling at Burr-Brown. We strongly recommend that our customers adopt similar procedures throughout their handling and utilization of these and other semiconductor products. These guidelines are summarized below:

GUIDELINES

1. Eliminate souces of ESD by removing static generating materials from all areas that handle products, by grounding all operators, equipment, and work stations where products are handled or stored, and by transporting and shipping products in static-free containers.
2. Shield products from potential damage by using a conductive Faraday shield where practical.
3. Shunt electrostatic charges and voltage potentials to zero where practical by connecting together all leads of each device by means of a conductive material.

ELIMINATE SOURCES OF ESD

It is highly desirable to eliminate static-generating materials from close proximity to products. This includes the elimination of all plastics, such as wrapping and packing materials, which have not been properly treated to achieve antistatic properties.

Antistatic is a term used to describe insulators which have been treated to reduce their very high surface resistance from a value in excess of a million meghoms to a value in the vicinity of one megohm.

The human body has been electrically characterized as a capacitor ranging from 100 to 200 picofarads and a resistance ranging from 500 ohms to several thousand ohms. As in electrical applications, the best way to prevent an accumulation of charge, or to drain the accumulation of existing charge on a capacitor, is to short the capacitor terminals together. The body is one plate of the capacitor with earth being the other. The only way to effectively short this capacitor is to connect the body to earth ground. For reasons of safety, this connection should include approximately one megohm of series resistance, or a ground fault interrupter. There should be periodic measurement to assure proper continuity all the way from the wrist strap connection to earth ground, and that the safety protection is operational. The wrist strap must have continuity to the skin in order to drain off the accumulated charge. Work station surfaces should be metallic or conductive plastic and should also be grounded through one megohm of series resistance, or have ground fault interrupters.

Static-free containers are important in storing and transporting product because the product could act as one plate of the capacitor and the container the other plate. Thus, it is possible to induce a charge, and therefore create a voltage, on the product without ohmic contact. Because of area and spacing considerations only unusual situations could cause damage, but it is nevertheless a possibility.

SHIELDING

In even the most optimum environments, there is always the potential for some accumulation of charge. The most positive control is to shield the product from potentially damaging electrostatic fields by use of a highly conductive (Faraday) shield. Antistatic enclosures or wrappers are only low enough in resistance to disperse accumulated charge. The Faraday shield must be low enough in resistance to completely conduct any electrostatic field around the product and prevent any field inside the enclosure. To be totally effective the Faraday shield must completely enclose the product. In addition, only antistatic materials may be used inside the container to assure that internal charge is not developed.

SHUNTING

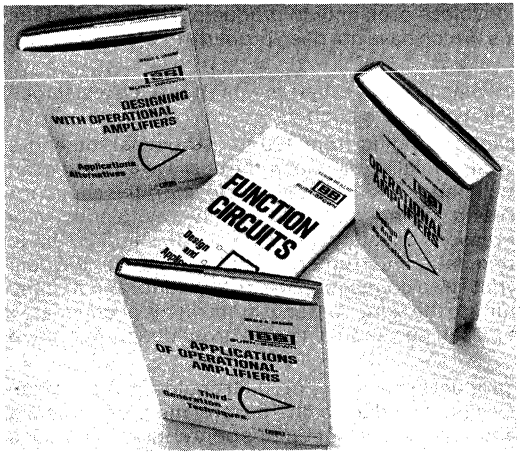
Shunting is one of the most cost-effective ways to protect products during assembly, testing, packing, unpacking, and handling. With a short circuit across sensitive terminals, it is nearly impossible to develop the voltages required for damage to occur. The limitation to this occurs when it is possible to induce large voltages internally in complex microcircuits. We can only shunt or short the exterior connections.

OTHER MEASURES

To help minimize the buildup of electrostatic charge it is desirable to control relative humidity to as high a value as practical (50% is recommended). In addition, where it is not possible to ground all surfaces, or where non-conducting surfaces cannot be completely eliminated, a good alternative may be the use of ionized air blowers.

BURR-BROWN TECHNICAL LIBRARY

The Burr-Brown engineering staff, in cooperation with McGraw-Hill have authored the world's most extensive and authoritative library dealing with the art of analog signal conditioning, conversion, and computation. These books, respected and referenced throughout the international engineering community, are available to you directly from Burr-Brown.



FUNCTION CIRCUITS

Design and Applications

This new volume in the growing Burr-Brown series is the first to deal with the multi-faceted area of analog function circuits. FUNCTION CIRCUITS explores in depth both the design theory and numerous applications for such analog functions as Multipliers, Dividers, Logarithmic Amplifiers, Exponentiators, RMS Converters, and Active Filters. It also shows clearly how to specify and test these functions, which are increasingly becoming available in the form of integrated circuits. As in previous Burr-Brown books, the emphasis is on practicality while maintaining a rigorous treatment of theory. Numerous graphs and formulas are presented to allow the user to obtain optimum circuit performance (over 300 pages and 200 illustrations).

DESIGNING WITH OPERATIONAL AMPLIFIERS

Applications Alternatives

This latest volume in Burr-Brown's well-known series on Operational Amplifiers presents a wealth of new applications and circuit techniques which have evolved since publication of the previous two books. The applications are presented in a manner that will aid the user in developing further circuits. In addition to providing completed designs, the applications include explanations of circuit operation. Practical limitations are discussed and pertinent design equations presented to allow adaptation to specific application requirements.

New applications include amplifier performance improvement techniques, signal analyzers, signal conditioners, absolute-value circuits, signal generators, computing circuits, data transmission circuits, and test an measurement circuits (approximately 270 pages and 200 illustrations).

OPERATIONAL AMPLIFIERS

Design and Applications

Covering basic theory, test methods, amplifier design techniques, and applications, this pioneer work provides *practical* information which can be directly applied to instrumentation design.

The book is divided into two principal parts and two appendices. Part I considers the design of operational amplifiers, offers insight into the factors determining performance characteristics, and outlines the techniques available for their control. Part II presents a wide range of practical operational amplifier applications, and provides sufficient descriptions of operation to permit design adaption from the specific circuits described. In Appendix A the basic theory of operational amplifiers is reviewed to provide an accompanying reference. Appendix B gives concise definitions of the performance parameters used to characterize operational amplifiers, and provides associated test circuits (over 470 pages and 300 illustrations).

APPLICATIONS OF OPERATIONAL AMPLIFIERS

Third Generation Techniques

This is the second volume in the operational amplifier series. More than just a collection of circuit or theoretical analysis, the book presents numerous applications of operational amplifiers in a variety of electronic equipment: specialized amplifiers, signal controls, processors, waveform generators, and special purpose circuits. It is a storehouse of detailed practical information, featuring numerous circuit diagrams, circuit values, pertinent design equations, error sources, and test-based comments on the efficiency of the arrangements and devices (over 230 pages and 170 illustrations).

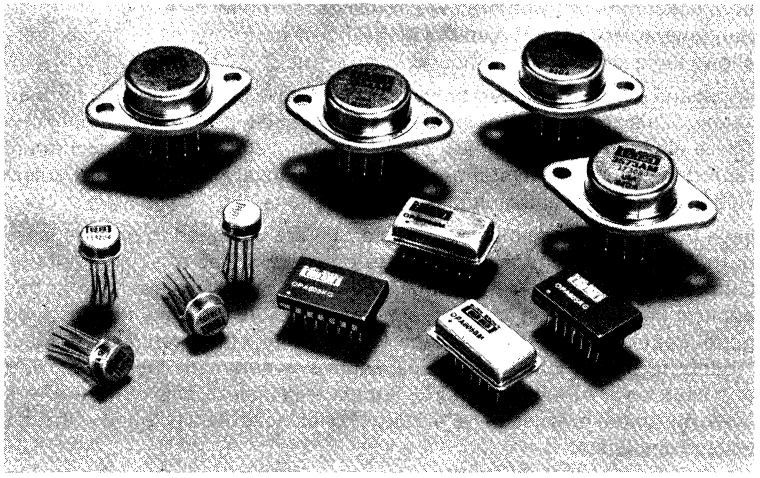
BURR-BROWN *UPDATE*

The Burr-Brown *Update* is published several times per year to keep our customers informed about new product developments, literature, and applications. If you would like to receive this publication on a regular basis, please contact your nearest Burr-Brown sales office or representative and ask to be put on our *Update* mailing list.

APPLICATION NOTES

Burr-Brown engineers have compiled a library of Application Notes to assist you in your designs. These notes are listed below and are available on request.

OPERATIONAL AMPLIFIERS



Burr-Brown operational amplifiers are listed in eight applications groups and are described below. This enables the user to determine and select the best operational amplifier available for a design requirement. Instrumentation amplifiers and isolation amplifiers are described in sections 2 and 3 respectively

General Purpose - General purpose operational amplifiers are suited for a wide variety of applications. They give moderately good performance over a wide range of parameters at moderate cost. This applications group contains both FET and bipolar input models with frequency responses from 0.5mHz to 1.5MHz and offset voltages as low as 1mV.

Low Drift - Low Drift operational amplifiers are best suited for applications where accuracy must be preserved over a substantial temperature range. These amplifiers are optimized to minimize the initial input offset voltage and input offset voltage change with temperature. Input offset drifts from 0.1μV/°C to 10μV/°C are available within this group. Chopper-stabilized operational amplifiers represent the best available in overall accuracy and long term stability.

Low Bias Current - Low bias current operational amplifiers consist of a group of varactor diode and FET input designs. This group includes amplifiers with input bias currents from 0.01pA to 1nA. Applications with large feedback resistances or large source resistances (long time constants, integrators, current sources, etc.) and buffer applications will benefit by the use of low bias current amplifiers.

Low Noise - This group contains low noise FET input operational amplifiers. Burr-Brown units offer guaranteed noise spectral density, 100% tested. In applications like low noise signal conditioning, light measurements, radiation measurements, photodiode circuits or low noise data acquisition the fully characterized and tested voltage noise performance of these units allows the designer to truly bound noise errors.

Wideband - Wideband operational amplifiers have bandwidths greater than 10MHz. This group also contains fast settling and high slew rate amplifiers. These amplifiers reduce phase errors at high frequencies and accurately reproduce complex waveforms. These amplifiers are well suited for pulse, video, fast settling, and multiplexing applications.

High Voltage - The amplifiers in this group are designed to provide large output voltage swings and to operate on wide ranges of supply voltage. Output voltages greater than ±10V and up to ±145V are available in this applications group (up to 290V, single supply). These amplifiers provide good frequency response and performance in other parameters. Most models have electrically isolated packages and automatic thermal sensing and shutdown. All units have FET inputs to minimize bias current errors when the amplifier is used with the large resistances usually found with high voltage amplifiers.

High Current - These amplifiers provide output currents from ±10mA to ±10A. They are used with small load resistances, coax cable impedances, and with power booster applcations. Many units have self-contained thermal sensing and shutdown to automatically protect the amplifiers from overheating and damage. All of these units have electrically isolated packages.

Unity-Gain Buffer (Power Booster) - Unity-gain buffer amplifiers have a wide variety of applications. They are used to boost the output current capability of another amplifier, to buffer an impedance that might load a critical circuit or to be an input impedance converter from an input which must not be loaded. These amplifiers may also be used inside the feedback loop of another operational amplifier to form a current-boosted, composite amplifier.

SELECTION GUIDE

GENERAL PURPOSE

These moderately priced FET and bipolar op amps offer good performance over a wide range of parameters. These are good options when a special function op amp is not required. You can be confident that Burr-Brown's quality and reliability are inherent in their design.

GENERAL PURPOSE												
		Offset Voltage		Bias	Open	Frequency Response		Rated Output				
Description	Model[1]	At 25°C ±mV max	Temp Drift ±μV/°C max	Current (25°C) nA max	Loop Gain dB min	Unity Gain MHz	Slew Rate V/μsec	±V min	±mA min	Temp Range[2]	Package	Page
Bipolar	3500A	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99	1-96
	3500B	2	5	±20	93	1.5	0.8	10	10	Ind	TO-99	1-96
	3500C	1	3	±15	93	1.5	1.0	10	10	Ind	TO-99	1-96
	3500R, (Q)	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99	1-96
	3500S, (Q)	2	10	±20	93	1.5	0.8	10	10	MIL	TO-99	1-96
	3500T, (Q)	1	5	±15	93	1.5	1.0	10	10	MIL	TO-99	1-96
Military	3500/MIL Series	See Military Products										
Bipolar	3501A, (Q)	5	20	±15	93	0.5	0.1	10	5	Ind	TO-99	1-105
	3501B, (Q)	2	10	±7	93	0.5	0.1	10	5	Ind	TO-99	1-105
	3501C, (Q)	2	5	±3	93	0.5	0.1	10	5	Ind	TO-99	1-105
	3501R	5	20	±15	93	0.5	0.1	10	5	MIL	TO-99	1-105
	3501S	2	10	±7	93	0.5	0.1	10	5	MIL	TO-99	1-105
Low Power	OPA21AJ	0.1	1	25	120	0.3	0.2	13.7	1.4	MIL	TO-99	1-13
	OPA21AZ	0.1	1	25	120	0.3	0.2	13.7	1.4	MIL	DIP	1-13
	OPA21BJ	0.2	2	40	114	0.3	0.2	13.7	1.4	MIL	TO-99	1-13
	OPA21BZ	0.2	2	40	114	0.3	0.2	13.7	1.4	MIL	DIP	1-13
	OPA21GJ	0.5	5	50	114	0.3	0.2	13.6	1.3	Ind	TO-99	1-13
	OPA21GZ	0.5	5	50	114	0.3	0.2	13.6	1.3	Ind	DIP	1-13
	OPA21EJ	0.1	1	25	120	0.3	0.2	13.7	1.4	Ind	TO-99	1-13
	OPA21EZ	0.1	1	25	120	0.3	0.2	13.7	1.4	Ind	DIP	1-13
	OPA21FJ	0.2	2	40	114	0.3	0.2	13.7	1.4	Ind	TO-99	1-13
	OPA21FZ	0.2	2	40	114	0.3	0.2	13.7	1.4	Ind	DIP	1-13
Switchable Input	OPA201AG	0.5	5	50	114	0.5[3]	0.1	13.5	5	Com	DIP	1-61
	OPA201BG	0.2	2	40	114	0.5[3]	0.1	13.5	5	Com	DIP	1-61
	OPA201CG	0.1	1	25	120	0.5[3]	0.1	13.5	5	Com	DIP	1-61
	OPA201RG	0.5	5	50	114	0.5[3]	0.1	13.5	5	MIL	DIP	1-61
	OPA201SG	0.2	2	40	114	0.5[3]	0.1	13.5	5	MIL	DIP	1-61
FET	OPA103AM	0.50	25	−0.002	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103BM	0.50	15	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103CM	0.25	5	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103DM	0.25	2	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	3542J, (Q)	20	50	−0.025	88	1.0	0.5	10	10	Com	TO-99	1-143
	3542S, (Q)	20	50	−0.025	88	1.0	0.5	10	10	MIL	TO-99	1-143
Wide Temp Range	OPA11HT	5	5[3]	±25	94	12.0	7.0	10	15	−55°C to +175°C	TO-99	1-9

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Typical.

LOW DRIFT

Low offset voltage drift vs temperature performance in both FET and bipolar input types is obtained by our sophisticated drift compensation techniques. First, the drift is measured and then special laser trim techniques are used to minimize the drift and the initial offset voltage at 25°C. Finally, "max drift" performance is retested for conformance with specifications.

0.1μV/°C to 10μV/°C input offset voltage change with temperature.

LOW DRIFT												
		Offset Voltage		Bias	Open	Frequency Response		Rated Output				
Description	Model[1]	At 25°C ±mV max	Temp Drift ±μV/°C max	Current (25°C) nA max	Loop Gain dB min	Unity Gain MHz	Slew Rate V/μsec	±V min	±mA min	Temp Range[2]	Package	Page
Inverting Only[3]	3291/14	0.02	0.10	±0.05	140	3	6	10	5	Ind	Module	1-86
	3292/14	0.05	0.30	±0.05	140	3	6	10	5	Ind	Module	1-86
	3293/14	0.10	1.0	±0.10	140	3	6	10	5	Ind	Module	1-86

LOW DRIFT												
		Offset Voltage		Bias	Open	Frequency Response		Rated Output				
Description	Model[1]	At 25°C ±mV max	Temp Drift ±μV/°C max	Current (25°C) nA max	Loop Gain dB min	Unity Gain MHz	Slew Rate V/μsec	±V min	±mA min	Temp Range[2]	Package	Page
FET	OPA103AM	0.50	25	−0.002	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103BM	0.50	15	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103CM	0.25	5	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103DM	0.25	2	−0.001	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA111AM	0.5	5	0.002	114	2	2	10	5	Ind	TO-99	1-51
	OPA111BM	0.25	1	0.001	120	2	2	10	5	Ind	TO-99	1-51
	OPA111SM	0.5	5	0.002	114	2	2	10	5	Mil	TO-99	1-51
Bipolar	OPA27A,	0.025	0.6	40	120	8	2.8	10	17.6	MIL		1-17
	OPA37A,	0.025	0.6	40	120	40[4]	17	10	17.6	MIL		1-17
	OPA27B,	0.060	1.3	55	120	8	2.8	10	17.6	MIL		1-17
	OPA37B,	0.060	1.3	55	120	40[4]	17	10	17.6	MIL		1-17
	OPA27C,	0.100	1.8	80	97	8	2.8	10	17.6	MIL		1-17
	OPA37C,	0.100	1.8	80	97	40[4]	17	10	17.6	MIL	TO-99/	1-17
	OPA27E	0.025	0.6	40	120	8	2.8	10	17.6	Ind	DIP	1-17
	OPA37E	0.025	0.6	40	120	40[4]	17	10	17.6	Ind		1-17
	OPA27F	0.060	1.3	55	120	8	2.8	10	17.6	Ind		1-17
	OPA37F	0.060	1.3	55	120	40[4]	17	10	17.6	Ind		1-17
	OPA27G	0.100	1.8	80	97	8	2.8	10	17.6	Ind		1-17
	OPA37G	0.100	1.8	80	97	40[4]	17	10	17.6	Ind		1-17
	3510AM	0.15	2	±35	120	0.4	0.5	10	10	Ind	TO-99	1-117
	3510BM	0.12	1	±25	120	0.4	0.5	10	10	Ind	TO-99	1-117
	3510CM	0.06	0.5	±15	120	0.4	0.5	10	10	Ind	TO-99	1-117
Military	3510VM/MIL, /883B						See Military Products					
Bipolar	3500B	2	5	±20	93	1.5	0.8	10	10	Ind	TO-99	1-96
	3500C	1	3	±15	93	1.5	1.0	10	10	Ind	TO-99	1-96
	3500R, (Q)	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99	1-96
	3500S, (Q)	2	10	±20	93	1.5	0.8	10	10	MIL	TO-99	1-96
	3500T, (Q)	1	3	±15	93	1.5	1.0	10	10	MIL	TO-99	1-96
	3500E	0.50	1	±50	100[6]	1.5	0.8	10	10	Ind	TO-99	1-96
	3500MP	0.20[5]	1[5]	±50	100[6]	1.5	0.8	10	10	Ind	TO-99	1-96
	3501A, (Q)	5	20	±15	93	0.5	0.1	10	5	Ind	TO-99	1-105
	3501B, (Q)	5	10	±7	93	0.5	0.1	10	5	Ind	TO-99	1-105
	3501C, (Q)	2	5	±3	93	0.5	0.1	10	5	Ind	TO-99	1-105
	3501R	5	20	±15	93	0.5	0.1	10	5	MIL	TO-99	1-105
	3501S	2	10	±7	93	0.5	0.1	10	5	MIL	TO-99	1-105
High Voltage	3271/25	0.05	1.0	±0.08	140	1	20	110	20	Ind	Module	1-183

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Chopper-stabilized. (4) Gain-bandwidth product for OPA37. (5) These specifications apply to the match between two devices. The 3500MP is a matched pair of amplifiers. (6) Typical.

HIGH VOLTAGE—HIGH CURRENT

These IC op amp designs set the pace for the industry and are a product of our extensive hybrid circuit technology. Output currents up to ±5A peak and voltages up to ±145V are available.

Output voltages > ±10V to ±145V.

HIGH VOLTAGE												
		Rated Output		Offset Voltage		Bias	Frequency Response		Open			
Description	Model[1]	±V min	±mA min	At 25°C ±mV max	Temp Drift ±μV/°C max	Current (25°C) pA max	Unity Gain MHz	Slew Rate V/μsec	Loop Gain dB	Temp Range[2]	Package	Page
FET	3584JM, (Q)	145	15	3	25	−20	20[3]	150	120	Com	TO-3	1-185
	3583AM, (Q)	140	75	3	25	−20	5	30	118	Ind	TO-3	1-181
	3583JM	140	75	3	25	−20	5	30	118	Com	TO-3	1-177
	3582J	145	15	3	25	−20	5	20	118	Com	TO-3	1-177
	3581J	70	30	3	25	−20	5	20	112	Com	TO-3	1-177
	3580J	30	60	10	30	−50	5	15	106	Com	TO-3	1-177
	3571AM, (Q)	30	1A[4]	2	40	−100	0.5	3	94	Ind	TO-3	1-167
	3572AM	30	2A[5]	2	40	−100	0.5	3	94	Ind	TO-3	1-167
	3573AM	20	2A[5]	10	65	40nA	1	2.6	94	Ind	TO-3	1-173
Chopper-Stabilized	3271/25	110	20	0.05	1	±80	1	20	140	Ind	Module	1-83

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) 2A peak. (5) 5A peak. (6) Typical.

Output currents > ±15mA to ±10A.

HIGH CURRENT													
		Rated Output		Offset Voltage		Bias Current	Frequency Response		Open Loop				
				At 25°C	Temp Drift	(25°C)	Unity	Slew	Gain	Temp		
Description	Model[1]	±V min	±mA min	±mV max	±μV/°C max	pA max	Gain MHz	Rate V/μsec	dB	Range[2]	Package	Page
High Power	OPA501AM	20	10A	10	65	40nA	1	1.5	94	Ind	TO-3	1-69
	OPA501BM	26	10A	5	40	20nA	1	1.5	98	Ind	TO-3	1-69
	OPA501RM	20	10A	10	65	40nA	1	1.5	94	MIL	TO-3	1-69
	OPA501SM	26	10A	5	40	20nA	1	1.5	98	MIL	TO-3	1-69
	3573AM	20	2A[5]	10	65	40nA	1	2.6	94	Ind	TO-3	1-173
	3572AM	30	2A[5]	2	40	−100	0.5	3	94	Ind*	TO-3	1-167
	3571AM, (Q)	30	1A[4]	2	40	−100	0.5	3	94	Ind	TO-3	1-167
Wideband	3554AM, (Q)	10	100	2	50	−50	1700[3]	1200	100	Ind	TO-3	1-159
	3554BM, (Q)	10	100	1	15	−50	1700[3]	1200	100	Ind	TO-3	1-159
	3554SM, (Q)	10	100	1	25	−50	1700[3]	1200	100	MIL	TO-3	1-159
High Voltage	3584JM, (Q)	145	15	3	25	−20	20[3]	150	126	Com	TO-3	1-185
	3583AM	140	75	3	25	−20	5	30	118	Ind	TO-3	1-181
	3583JM	140	75	3	25	−20	5	30	118	Com	TO-3	1-181
	3582J	145	15	3	25	−20	5	20	118	Com	TO-3	1-173
	3581J	70	30	3	25	−20	5	20	112	Com	TO-3	1-173
	3580J	30	60	10	30	−50	5	15	106	Com	TO-3	1-173
Booster (Buffer)	3553AM, (Q)	10	200	50	300[6]	−200	300	2000	NA	Ind	TO-3	1-155
	3329/03	10	100	50	—	Bipolar	5	—	NA	Ind.	DIP	1-92

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) 2A peak. (5) 5A peak. (6) Typical.

LOW BIAS CURRENT

Our many years of experience in designing, manufacturing and testing FET amplifiers gives us unique abilities in providing low and ultra low bias current op amps. These amplifiers offer bias currents as low as 75fA (75×10^{-15} amps) and low voltage drift as low as 2μV/°C. With offset voltage laser-trimmed to as low as 250μV, the need for expensive trim pot adjustments is eliminated.

0.01pA to 1nA bias current.

LOW BIAS CURRENT												
		Offset Voltage		Bias	Open	Frequency Response		Rated Output				
		At 25°C	Temp Drift	Current (25°C)	Loop Gain	Unity	Slew Rate	±V	±mA	Temp		
Description	Model[1]	±mV max	±μV/°C max	pA max	dB min	Gain MHz	V/μsec	min	min	Range[2]	Package	Page
Low Drift	OPA103AM	0.50	25	−2	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103BM	0.50	15	−1	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103CM	0.25	5	−1	106	1	1.3	10	5	Ind	TO-99	1-43
	OPA103DM	0.25	2	−1	106	1	1.3	10	5	Ind	TO-99	1-43
Low Noise	OPA101AM	0.50	10	−15	94	10	6.5	12	12	Ind	TO-99	1-31
	OPA101BM	0.25	5	−10	94	10	6.5	12	12	Ind	TO-99	1-31
	OPA102AM	0.50	10	−15	94	40[3]	14	12	12	Ind	TO-99	1-31
	OPA102BM	0.25	5	−10	94	40[3]	14	12	12	Ind	TO-99	1-31
	OPA111AM	0.5	5	2	114	2	2	10	5	Ind	TO-99	1-51
	OPA111BM	0.25	1	1	120	2	2	10	5	Ind	TO-99	1-51
	OPA111SM	0.5	5	2	114	2	2	10	5	MIL	TO-99	1-51
Ultra-Low Bias Current	OPA104AM	1.0	25	−0.300	106	1	2.2	10	5	Ind	TO-99	1-47
	OPA104BM	0.50	15	−0.150	106	1	2.2	10	5	Ind	TO-99	1-47
	OPA104CM	0.50	10	−0.075	106	1	2.2	10	5	Ind	TO-99	1-47
	3528AM, (Q)	0.50	15	−0.300	88	0.7	0.3	10	5	Ind	TO-99	1-137
	3528BM, (Q)	0.25	5	−0.150	92	0.7	0.3	10	5	Ind	TO-99	1-137
	3528CM, (Q)	0.50	10	−0.075	90	0.7	0.3	10	5	Ind	TO-99	1-137
	3523J, (Q)	1.0	50	−0.50	100	1	0.6	10	10	Com	TO-99	1-129
	3523K	0.50	25	−0.25	100	1	0.6	10	10	Com	TO-99	1-129
	3523L, (Q)	0.50	25	−0.10	100	1	0.6	10	10	Com	TO-99	1-129
Inverting Only	3430J	Adjus. to 0	30	±0.01	100	2kHz	0.4V/ msec	10	5	Com	Module	1-94
	3430K		10	±0.01	100	2kHz		10	5	Com	Module	1-94
Noninverting Only	3431J	Adjus. to 0	30	±0.01	100	2kHz	0.4V/ msec	10	5	Com	Module	1-94
	3431K		10	±0.01	100	2kHz		10	5	Com	Module	1-94
Low Cost	OPA100AM	1	15	±3	94	1	2	10	5	Ind	TO-99	1-25
	OPA100BM	0.5	10	±2	100	1	2	10	5	Ind	TO-99	1-25
	OPA100CM	0.25	5	±1	106	1	2	10	5	Ind	TO-99	1-25

LOW BIAS CURRENT													
		Offset Voltage		Bias	Open	Frequency Response		Rated Output					
Description	Model[1]	At 25°C ±mV max	Temp Drift ±μV/°C max	Current (25°C) pA max	Loop Gain dB min	Unity Gain MHz	Slew Rate V/μsec	±V min	±mA min	Temp Range[2]	Package	Page
	3542J	20	50	−25	88	1	0.5	10	10	Com	TO-99	1-143
	3542S	20	50	−25	88	1	0.5	10	10	MIL	TO-99	1-143
Chopper-Stabilized	3291/14	0.02	0.1	±50	140	3	6	10	5	Ind	Module	1-86
	3292/14	0.05	0.3	±50	140	3	6	10	5	Ind	Module	1-86
	3293/14	0.10	1	±100	140	3	6	10	5	Ind	Module	1-86
	3271/25	0.05	1	±80	140	1	20	110	20	Ind	Module	1-83
Wideband	3554AM, (Q)	2	50	−50	100	1000[3]	1000	10	100	Ind	TO-3	1-159
	3554BM, (Q)	1	15	−50	100	1000[3]	1000	10	100	Ind	TO-3	1-159
	3554SM, (Q)	1	25	−50	100	1000[3]	1000	10	100	MIL	TO-3	1-159
Buffer	3553AM, (Q)	50	300	−200	NA	300[4]	2000	10	200	Ind	TO-3	1-155
High Current	3571AM, (Q)	2	40	−100	94	0.5	3	30	1A	Ind	TO-3	1-167
	3572AM	2	40	−100	94	0.5	3	30	2A	Ind	TO-3	1-167
High Voltage	3580J	10	30	−50	86	5	15	30	60	Com	TO-3	1-177
	3581J	3	25	−20	94	5	20	70	30	Com	TO-3	1-177
	3582J, (Q)	3	25	−20	100	5	20	145	15	Com	TO-3	1-177
	3583AM, (Q)	3	25	−20	105	5	30	140	75	Ind	TO-3	1-181
	3583JM	3	25	−20	94	5	30	140	75	Com	TO-3	1-181
	3584JM, (Q)	3	25	−20	100	20[3]	150	145	15	Com	TO-3	1-185
General Purpose	3522J	1.0	50	−10	94	1	0.6	10	10	Com	TO-99	1-123
	3522K	0.50	10	−5	94	1	0.6	10	10	Com	TO-99	1-123
	3522L	0.50	25	−1	94	1	0.6	10	10	Com	TO-99	1-123
	3522S, (Q)	0.50	25	−5	94	1	0.6	10	10	MIL	TO-99	1-123
Ultra-low Drift	3527AM, (Q)	0.50	10	−5	100	1	0.6	10	10	Ind	TO-99	1-133
	3527BM, (Q)	0.25	5	−2	100	1	0.6	10	10	Ind	TO-99	1-133
	3527CM, (Q)	0.25	2	−5	100	1	0.6	10	10	Ind	TO-99	1-133
	3521H	0.50	10	−20	94	1.5	0.6	10	10	Com	TO-99	1-123
	3521J, (Q)	0.25	5	−20	94	1.5	0.6	10	10	Com	TO-99	1-123
	3521K	0.25	2	−15	94	1.5	0.6	10	10	Com	TO-99	1-123
	3521L	0.25	1	−10	94	1.5	0.6	10	10	Com	TO-99	1-123
	3521R, (Q)	0.25	5	−20	94	1.5	0.6	10	10	MIL	TO-99	1-123

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) −3dB bandwidth.

LOW NOISE

Now both FET and bipolar input op amps are offered with guaranteed low noise specifications. Until now the designer had to rely on "typical" specs for his demanding low noise designs. These fully characterized parts allow a truly complete error budget calculation.

LOW NOISE													
				Offset Voltage			Frequency Response		Rated Output				
Description	Model	Noise Voltage nV/√Hz at 10kHz max	Bias Current (25°C) pA max	At 25°C ±mV max	Temp Drift ±μV/°C max	Open Loop Gain dB min	GBW MHz	Slew Rate V/μsec min	±V min	±mA min	Temp Range [1]	Package	Page
OPA27 [2]	OPA27A	3.8	±40k	0.025	0.6	120	8	1.7	10.0	17.6	MIL		1-17
$A_{CL} > 1V/V$	OPA37A	3.8	±40k	0.025	0.6	120	40	11	10.0	17.6	MIL		1-17
	OPA27B	3.8	±55k	0.060	1.3	120	8	1.7	10.0	17.6	MIL		1-17
OPA37 [2]	OPA37B	3.8	±55k	0.060	1.3	120	40	11	10.0	17.6	MIL		1-17
$A_{CL} > 5V/V$	OPA27C	4.5	±80k	0.100	1.8	97	8	1.7	10.0	17.6	MIL		1-17
	OPA37C	4.5	±80k	0.100	1.8	97	40	11	10.0	17.6	MIL	TO-99/	1-17
	OPA27E	3.8	±40k	0.025	0.6	120	8	11	10.0	17.6	Ind	DIP	1-17
	OPA37E	3.8	±40k	0.025	0.6	120	40	11	10.0	17.6	Ind		1-17
	OPA27F	3.8	±55k	0.060	1.3	120	8	1.7	10.0	17.6	Ind		1-17
	OPA37F	3.8	±55k	0.060	1.3	120	40	11	10.0	17.6	Ind		1-17
	OPA27G	4.5	±80k	0.100	1.8	97	8	1.7	10.0	17.6	Ind		1-17
	OPA37G	4.5	±80k	0.100	1.8	97	40	11	10.0	17.6	Ind		1-17
$A_{CL} > 1V/V$ [3]	OPA101AM	8	−15	0.5	10	94	20	5	12	12	Ind	TO-99	1-31
	OPA101BM	8	−10	0.25	5	94	20	5	12	12	Ind	TO-99	1-31
$A_{CL} > 3V/V$ [3]	OPA102AM	8	−15	0.5	10	94	40	10	12	12	Ind	TO-99	1-31
	OPA102BM	8	−10	0.25	5	94	40	10	12	12	Ind	TO-99	1-31
$A_{CL} > 1V/V$ [3]	OPA111AM	8	2	0.5	5	114	2	2	10	5	Ind	TO-99	1-51
	OPA111BM	8	1	0.25	1	120	2	2	10	5	Ind	TO-99	1-51
	OPA111SM	8	2	0.5	5	114	2	2	10	5	MIL	TO-99	1-51

NOTES: (1) Ind = −25°C to +85°C; MIL = −55°C to +125°C. (2) A, B, C grades available with /883 screening. (3) FET input.

UNITY-GAIN BUFFER (Power Booster)

These versatile amplifiers: boost the output current capability of another amplifier; buffer an impedance that might load a critical circuit; may be used inside the feedback loop of another op amp to form a current-boosted, composite amplifier. Currents as high as ±100mA are available with speeds of 2000V/μsec.

UNITY-GAIN BUFFER												
		Rated Output		Frequency Response								
Description	Model	±V min	±mA min	−3dB MHz	Full Power BW MHz	Slew Rate V/μsec	Gain V/V	Input Impedance Ω	Open Loop Gain dB	Temp Range[1]	Package	Page
Noninverting	3553AM	10	200	300	32	2000	≈1	10^{11}	NA	Ind	TO-3	1-155
	3329/03	10	100	5	1	—	≈1	10k	NA	Ind	DIP	1-92

NOTES: (1) Ind = −25°C to +85°C.

WIDE BANDWIDTH

Design expertise in wideband circuits combines with our fully developed hybrid technology to create cost effective wideband op amps. Hybrid IC performance—in bandwidth, settling time and output current—cannot be duplicated in less expensive monolithic designs.

WIDE BANDWIDTH													
		Frequency Response				Rated Output		Offset Voltage					
Description	Model[1]	GBW MHz	Slew Rate V/μsec min	t_s ±0.1% nsec	Compensation	±V min	±mA min	At 25°C ±mV max	Temp Drift ±μV/°C max	Open Loop Gain dB	Temp Range[2]	Package	Page
Differential	3554AM, (Q)	1700,	1000	120	ext.	10	100	2	50	100	Ind	TO-3	1-159
	3554BM, (Q)	A=	1000	120	ext.	10	100	1	15	100	Ind	TO-3	1-159
	3554SM, (Q)	1000	1000	120	ext.	10	100	1	25	100	MIL	TO-3	1-159
	3551J	50, A=10	250	400	ext.	10	10	1	50[3]	100	Com	TO-99	1-151
	3551S, (Q)	50, A=10	250	400	ext.	10	10	1	50[3]	100	MIL	TO-99	1-151
	3550J	10, A=10	65	400	int.	10	10	1	50[3]	100	Com	TO-99	1-147
	3550K	20, A=1	100	400	int.	10	10	1	50[3]	100	Com	TO-99	1-147
	3550S, (Q)	10, A=1	65	400	int.	10	10	1	50[3]	100	MIL	TO-99	1-147
	3508J	100, A=100	20	—	ext.	10	10	5	30[3]	103	Com	TO-99	1-113
	3507J, (Q)	20, A=10	80	200	ext.	10	10	10	30[3]	83	Com	TO-99	1-109
	OPA605H	200, A=1000	300[3]	300	ext.	10	30	1	25	96	Com	DIP	1-77
	OPA605A	200, A=1000	300[3]	300	ext.	10	30	1	25	96	Ind	DIP	1-77
	OPA605K	200, A=1000	300[3]	300	ext.	10	30	0.5	5	96	Com	DIP	1-77
	OPA605C	200, A=1000	300[3]	300	ext.	10	30	0.5	5	96	Ind	DIP	1-77
	OPA27A	8	1.7	—	int.[4]	10	16	0.025	0.6	120	MIL		1-17
	OPA37A	40	11	—	int.[4]	10	16	0.025	0.6	120	MIL		1-17
	OPA27B	8	1.7	—	int.[4]	10	16	0.060	1.3	120	MIL		1-17
	OPA37B	40	11	—	int.[4]	10	16	0.060	1.3	120	MIL		1-17
	OPA27C	8	1.7	—	int.[4]	10	16	0.100	1.8	97	MIL		1-17
	OPA37C	40	11	—	int.[4]	10	16	0.100	1.8	97	MIL	TO-99/	1-17
	OPA27E	8	1.7	—	int.[4]	10	16	0.025	0.6	120	Ind	DIP	1-17
	OPA37E	40	11	—	int.[4]	10	16	0.025	0.6	120	Ind		1-17
	OPA27F	8	1.7	—	int.[4]	10	16	0.060	1.3	120	Ind		1-17
	OPA37F	40	11	—	int.[4]	10	16	0.060	1.3	120	Ind		1-17
	OPA27G	8	1.7	—	int.[4]	10	16	0.100	1.8	97	Ind		1-17
	OPA37G	40	11	—	int.[4]	10	16	0.100	1.8	97	Ind		1-17
Low Noise	OPA101AM	20, A=100	5	2.5	int.	12	12	0.5	10	105	Ind	TO-99	1-31
	OPA101BM	20, A=100	5	2.5	int.	12	12	0.25	5	105	Ind	TO-99	1-31
	OPA102AM	40, A=100	10	1.5	int.	12	12	0.5	10	105	Ind	TO-99	1-31
	OPA102BM	40, A=100	10	1.5	int.	12	12	0.25	5	105	Ind	TO-99	1-31
Military	OPA600/MIL Series				See Military Products								
Unity-Gain Buffer	3553AM, (Q)	32	2000	—	—	10	200	50	300[3]	NA	Ind	TO-3	1-155
Wide Temp	OPA11HT	12, A=1	4	1500	int.	10	15	5[3]	5	98	+175°C	TO-99	1-9

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Typical. (4) G = 5 min for OPA37.

GLOSSARY OF TERMS AND DEFINITIONS
Operational Amplifiers

COMMON-MODE INPUT IMPEDANCE
The effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground terminal.

COMMON-MODE REJECTION (CMR)
When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$\text{CMR (in dB)} = 20 \log_{10} \text{CMV/Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE VOLTAGE (CMV)
That portion of an input signal which is common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$\text{CMV} = (e_1 + e_2)/2$$

COMMON-MODE VOLTAGE GAIN
The ratio of the output signal voltage (ideally zero) to the common-mode input signal voltage.

COMMON-MODE VOLTAGE RANGE
The range of input voltage for linear, nonsaturated operation.

DIFFERENTIAL INPUT IMPEDANCE
The apparent impedance, resistance in parallel with capacitance, between the two input terminals.

FULL POWER FREQUENCY RESPONSE
The maximum frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN-BANDWIDTH PRODUCT
A product of small signal, open-loop gain and frequency at that gain.

INPUT BIAS CURRENT
The DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT VS SUPPLY VOLTAGE
The sensitivity of input bias current to the power supply voltages.

INPUT BIAS CURRENT VS TEMPERATURE
The sensitivity of input bias current to temperature.

INPUT CURRENT NOISE
The input current which would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are large.

INPUT OFFSET CURRENT
The difference of the two input bias currents of a differential amplifier.

INPUT OFFSET VOLTAGE
The DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT OFFSET VOLTAGE VS SUPPLY VOLTAGE I/PSRR
The sensitivity of input offset voltage to the power supply voltages. Both power supply magnitudes are changed in the same direction and over the operating voltage range.

INPUT OFFSET VOLTAGE VS TEMPERATURE (DRIFT)
The rate of change of input offset voltage with temperature. At Burr-Brown, this is the change in input offset voltage from 25°C to the maximum specification temperature, plus the change in input offset voltage from 25°C to the minimum specification temperature, this quantity divided by the specification temperature range.

INPUT OFFSET VOLTAGE VS TIME
The sensitivity of input offset voltage to time.

INPUT VOLTAGE NOISE
The differential input voltage which would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are small.

MAXIMUM SAFE INPUT VOLTAGE
The maximum, peak value, continuous voltage that may be applied at, or between, the inputs without damage.

OPEN-LOOP GAIN
The ratio of the output signal voltage to the differential input signal voltage.

OPERATING TEMPERATURE RANGE
The temperature range, ambient unless otherwise indicated, over which the amplifier may be safely operated.

OUTPUT RESISTANCE
The open-loop output source resistance with respect to ground.

POWER SUPPLY RATED VOLTAGE
The normal value of power supply voltage at which the amplifier is designed to operate.

POWER SUPPLY VOLTAGE RANGE
The range of power supply voltage over which the amplifier may be safely operated.

QUIESCENT CURRENT
The current required from the power supply to operate the amplfiier with no load and with the output at zero.

RATED OUTPUT
The peak output voltage and current which can be continuously, simultaneously supplied.

SETTLING TIME
The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE
The maximum rate of charge of the output voltage when supplying rated output.

SPECIFICATION TEMPERATURE RANGE
The temperature range over which the "versus temperature" specifications are specified.

STORAGE TEMPERATURE RANGE
The temperature range over which the amplifier may be safely stored, unpowered.

UNITY-GAIN FREQUENCY RESPONSE
The frequency at which the open-loop becomes unity.

BURR-BROWN®

OPA11HT

Wide Temperature-Range General Purpose OPERATIONAL AMPLIFIER

FEATURES

- −55°C TO +175°C SPECIFICATIONS
- 30nA MAX, INPUT BIAS CURRENT AT +175°C
- ±6mV, MAX, INPUT OFFSET VOLTAGE AT +175°C
- ±5μV/°C TYP, INPUT OFFSET VOLTAGE COEFFICIENT
- 12MHz BANDWIDTH, TYPICAL
- HERMETIC PACKAGE WITH STANDARD PINOUT (741-TYPE)

DESCRIPTION

These specifications give you a versatile operational amplifier that will work in circuits that are subjected to extremely wide temperature ranges. Typical applications for OPA11HT include general purpose gain blocks, high-speed pulse amplifiers, audio amplifiers, high-frequency active filters, high-speed integrators, and photodiode amplifiers.

You're assured of this product's performance over the -55°C to +175°C range because we conduct 100% screening procedures in accordance with MIL-STD-883, method 5004, class B. Burn-in is performed at 200°C. Our sample and inspection procedures include both destructive and nondestructive bonding wire pull tests in accordance with Method 2011 of MIL-STD-883. The product is assembled in a clean-room environment.

Model OPA11HT is internally compensated for stability at all gains. Pins are available for special tailoring of the bandwidth compensation. Significant advantages in high gain, wide bandwidth, low-bias current, high output current and high common-mode rejection are provided by OPA11HT. Inputs are protected against common-mode voltages up to the value of the power supplies while the output is current limited to offer short circuited protection. TO-99 hermetic package has standard 741-type pinout arrangement.

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SPECIFICATIONS

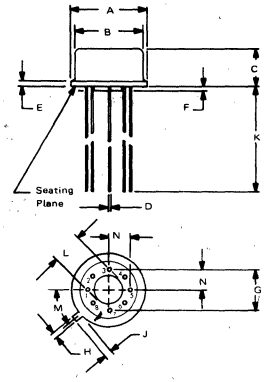
ELECTRICAL

Specifications at ±15VDC and T_A = +175°C unless otherwise noted.

MODEL		OPA11HT			
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
OPEN LOOP GAIN, DC, single-ended	A_V				
No load			103		dB
R_L= 2kΩ		94	100		dB
RATED OUTPUT					
Voltage, R_L= 2kΩ	V_{om}	±10	±12		V
Current (T_A = 25°C)	I_{om}	±15	±23		mA
DYNAMIC RESPONSE (T_A = 25°C)					
Small-Signal Bandwidth (0dB)			12		MHz
Full-Power Bandwidth, V_{OUT} = ±10V	BW_{fp}	50	75		kHz
Slew Rate, R_L = 2kΩ	SR	4	7		V/μsec
Settling Time (0.1%)			1.5		μsec
Rise Time (10% to 90%, small-signal)			30		nsec
INPUT OFFSET VOLTAGE	V_{io}				
Initial (without adj. at 25°C)			±1	±5	mV
Over Temperature					
T_A = +175°C				±6	mV
T_A = −55°C				±7	mV
Average V_{io} coefficient			±5		μV/°C
Average V_{io} coefficient vs supply voltage (T_A = 25°C)			±10	±200	μV/V
INPUT BIAS CURRENT	I_{ib}				
Initial at +25°C			±10	±25	nA
Over Temperature					
T_A = +175°C				±30	nA
T_A = −55°C				±40	nA
Average I_{ib} coefficient			±0.1		nA/°C
INPUT DIFFERENCE CURRENT	I_{io}				
Initial at +25°C			±10	±25	nA
Over Temperature					
T_A = +175°C				±30	nA
T_A = −55°C				±40	nA
Average I_{io} coefficient			±0.1		nA/°C
INPUT IMPEDANCE (T_A = 25°C)					
Differential	r_i	100	300		MΩ
	c_i		3		pF
Common Mode	$r_{i(CM)}$		1000		MΩ
	$c_{i(CM)}$		3		pF
INPUT VOLTAGE RANGE					
Common Mode				±11	V
Differential Mode				±12	V
Common-Mode Rejection	CMR	80	100		dB
Over Temperature (-55°C ≤ T_A ≤ +175°C)			100		dB
POWER SUPPLY (T_A = 25°C)					
Rated Voltage	V_{CC}			±15	V
Voltage Range, derated			±8 to ±22		V
Current, quiescent	I_q		±3	±3.7	mA
Over Temperature (-55°C ≤ T_A ≤ +175°C)			±3		mA
Power Supply Rejection Ratio (T_A = +175°C)	PS_{rr}	80	100		dB
TEMPERATURE RANGE					
Specification			−55°C ≤ T_A ≤ +175°C		
Operating			−55°C ≤ T_A ≤ +200°C		
Storage			−65°C ≤ T_A ≤ +250°C		

MECHANICAL

TO-99 PACKAGE

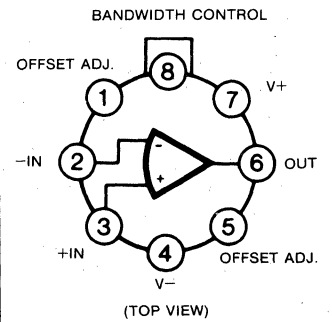


NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM



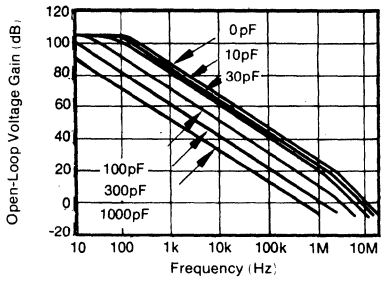
(TOP VIEW)

PIN 4 IS CONNECTED TO CASE

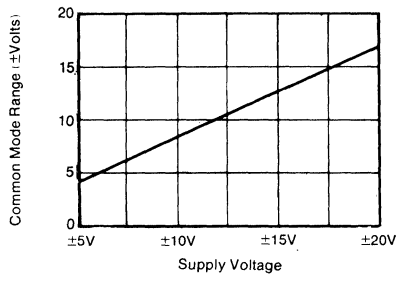
TYPICAL PERFORMANCE CURVES

(at ±15VDC and T_A = +25°C unless otherwise specified)

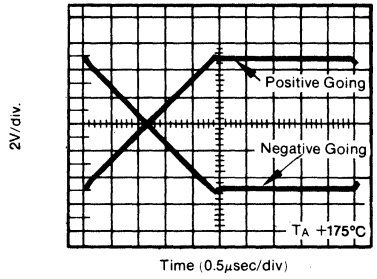
OPEN LOOP FREQUENCY RESPONSE[1]



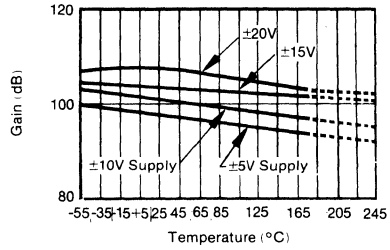
COMMON MODE VOLTAGE RANGE vs. SUPPLY VOLTAGE



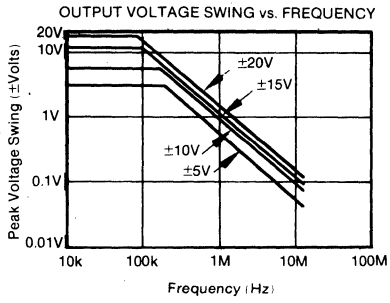
STEP RESPONSE IN FOLLOWER CONFIGURATION[2]



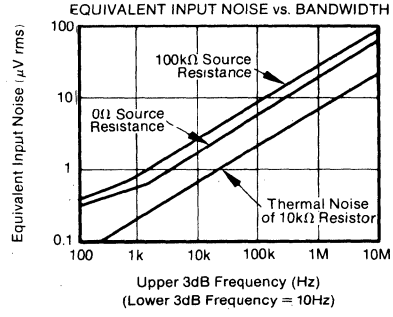
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



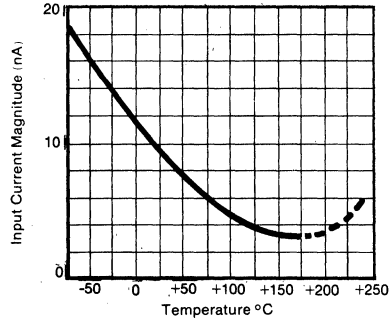
OUTPUT VOLTAGE SWING vs. FREQUENCY



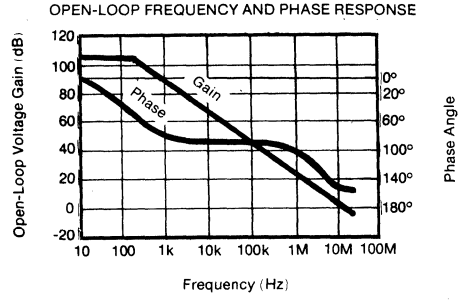
EQUIVALENT INPUT NOISE vs. BANDWIDTH



INPUT BIAS CURRENT AND DIFFERENCE CURRENT AS A FUNCTION OF TEMPERATURE



OPEN-LOOP FREQUENCY AND PHASE RESPONSE



1. Capacitance values shown are compensation from pin 8 to common. Not required for stability. See Figure 1. 2. See Figure 3.

APPLICATIONS

BANDWIDTH COMPENSATION

The frequency response of the OPA11HT can be adjusted by use of an external compensation capacitor from pin 8 to common as shown in Figure 1. The open-loop frequency response curves illustrate the effect of various values of capacitance. The OPA11HT is stable at any gain level without the use of compensation, provided that stray wiring capacitance and/or load capacitance are not excessive, and that moderate values of feedback resistance are used ($R_{FB} \leq 10k\Omega$). A load capacitance of ≈50pF is desirable in all feedback configurations.

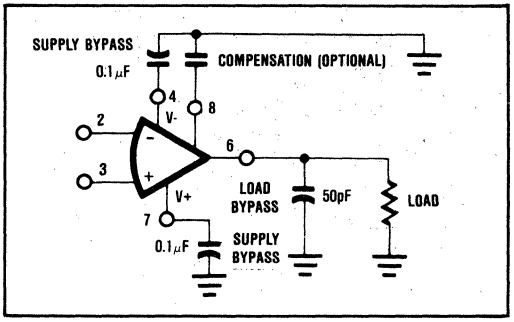


FIGURE 1. Compensated Amplifier with Supply Load Bypassing.

STABILITY

Because the OPA11HT is an extremely-fast amplifier with high gain, stray wiring capacitance and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly by passing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50pF capacitor, see Figure 1.

OFFSET VOLTAGE AND ADJUSTMENT

Although the offset voltage of these amplifiers is only a few millivolts, it may in some cases be desirable to null this offset. This is done by use of a 100kΩ potentiometer as shown in Figure 2.

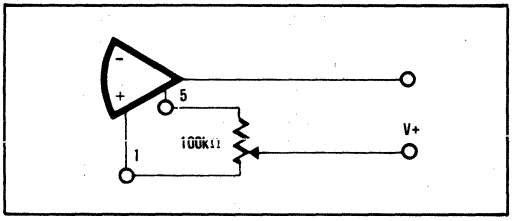


FIGURE 2. External Adjustment of Offset Voltage.

TEST CIRCUIT - DYNAMIC RESPONSE

The test circuit of Figure 3 is used for measurement of slew rate, settling time, rise time and overshoot. Both rise time and overshoot are measured for a small output signal (V_{OUT} = ±100mV). Slew rate and settling time are measured for a 10V, p-p, square wave.

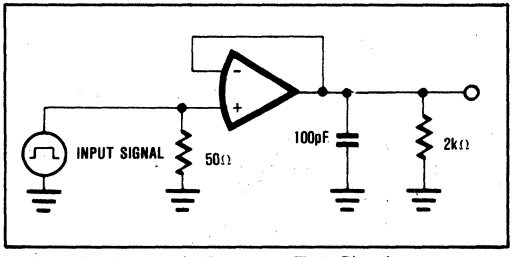


FIGURE 3. Dynamic Response Test Circuit.

VOLTAGE REGULATOR AT 200°C

In many applications, a regulated source of ±15V is needed. A voltage regulator that typically will operate up to +175°C is shown in Figure 4. This regulator accepts +16V to +30V at its input and provides +15V at 20mA at its output. A complementary version may be constructed to provide -15V by using the OPA11HT with a 2N1711 transistor. Short-circuit protection should be added if required.

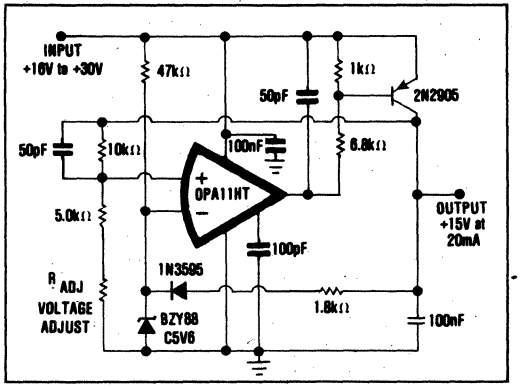


FIGURE 4. A +15V Voltage Regulator that will Operate at +175°C.

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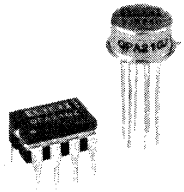


OPA21

High-Speed Low-Power Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW SUPPLY CURRENT
  230μA max at V_{CC} = ±15V
- HIGH SLEW RATE
  0.2V/μsec typ
- WIDE SUPPLY RANGE
  ±2.5V to ±18V
- LOW OFFSET VOLTAGE
  100μV max
- LOW OFFSET VOLTAGE DRIFT
  1.0μV/°C max
- HIGH CMRR AND PSRR
  110dB typ
- HIGH OPEN-LOOP GAIN
  120dB min

APPLICATIONS

- LOW POWER INSTRUMENTATION AMPLIFIERS
- ISOLATION AMPLIFIERS
- PORTABLE EQUIPMENT
- BATTERY OPERATION

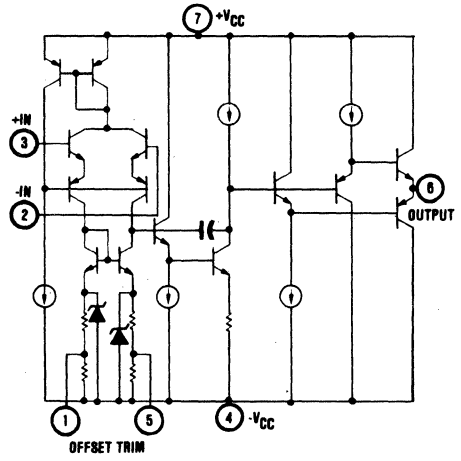
DESCRIPTION

A unique circuit design, state-of-the-art monolithic processing and advanced laser-trimming techniques are used to provide a low power amplifier with outstanding parameters - truly "instrumentation grade" performance.

The OPA21 maintains excellent performance features over a wide supply voltage range.

A maximum I_Q of 230μA means only 6.9mW of power consumption at the V_{CC} = ±15V and 1.1mW at V_{CC} = ±2.5V.

This design also has lower input bias and offset currents than other low power op amps. This is particularly important in low power applications where the high resistor values used can create large voltage errors due to bias current. The OPA21 is internally compensated and has excellent frequency stability characteristics.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 2.5VDC to 15VDC unless otherwise noted.

PARAMETERS	CONDITIONS	OPA21A, OPA21E MIN	OPA21A, OPA21E TYP	OPA21A, OPA21E MAX	OPA21B, OPA21F MIN	OPA21B, OPA21F TYP	OPA21B, OPA21F MAX	OPA21G MIN	OPA21G TYP	OPA21G MAX	UNITS
INITIAL OFFSET VOLTAGE ($\pm V_{CC}$ = 15VDC)											
Initial Offset[1]			40	100		150	200		300	500	µV
Over Temperature[2]			75	200		200	500		500	1000	µV
Average vs Temperature[2]			0.5	1.0		1.0	2.0		2.5	5.0	µV/°C
Offset Adjustment Range			±4			*			*		mV
INPUT OFFSET CURRENT											
Initial Offset			0.3	1		0.8	2		1.2	4	nA
Over Temperature[2]			0.5	2		2.0	4		2	6	nA
INPUT BIAS CURRENT											
Initial Bias			7	25		10	40		15	50	nA
Over Temperature[2]			9	40		12	60		18	75	nA
INPUT NOISE											
Voltage	0.1Hz to 10Hz		1.0			*			*		µV, p-p
Voltage Density	f_o = 1Hz		60			*			*		nV/√Hz
	f_o = 10Hz		20			*			*		nV/√Hz
	f_o = 100Hz		20			*			*		nV/√Hz
Current Density	f_o = 1Hz		0.7			*			*		pA/√Hz
	f_o = 10Hz		0.25			*			*		pA/√Hz
	f_o = 100Hz		0.07			*			*		pA/√Hz
INPUT RESISTANCE											
Differential			6			5			4		MΩ
Common-Mode			10^{10} ‖ 2			*			*		Ω ‖ pF
INPUT VOLTAGE RANGE ($\pm V_{CC}$ = 15VDC)											
Initial Input Voltage		-12.5			*			*			V
		+14.3			*			*			V
Over Temperature[2]		-12.0			*			*			V
		+14.0			*			*			V
COMMON-MODE REJECTION RATIO ($\pm V_{CC}$ = 15VDC, No Load, $-12 \leq V_{CM} \leq +14V$)											
Initial Rejection Ratio		100	110		90	105		84	100		dB
Over Temperature[2]		96	105		86	100		80	95		dB
POWER SUPPLY REJECTION RATIO ($\pm V_{CC}$ = 2.5V to 18V, No load											
Initial Rejection Ratio		104	114		100	108		90	100		dB
Over Temperature[2]		100	108		95	104		85	95		dB
LARGE SIGNAL VOLTAGE GAIN ($\pm V_{CC}$ = 15VDC, R_L = 10kΩ)											
Initial Voltage Gain		1000	2000		500	1500		500	1000		V/mV
		120	126		114	124		114	120		dB
Over Temperature[2]		500	1500		250	1300		250	1000		V/mV
		114	124		108	122		108	120		dB
RATED OUTPUT ($\pm V_{CC}$ = 15VDC, R_L = 10kΩ)											
Initial Voltage Swing		-13.7	-14.2		-13.7	*		-13.6	*		V
		+14.0	+14.1		+13.9	*		+13.8	*		V
Over Temperature[2]		-13.5			-13.5			-13.5			V
		+13.8			+13.7			+13.6			V
Output Resistance	Open-Loop		500			*			*		Ω
DYNAMIC RESPONSE											
Slew Rate	C_L = 100pF, R_L = 25kΩ		0.2			*			*		V/µsec
Closed-Loop Bandwidth	A_{CL} = +1, R_L = 10kΩ		300			*			*		kHz
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range		2.5		18	*		*	*		*	VDC
Current, Quiescent	No Load										
Initial	$\pm V_{CC}$ = 2.5V		(3)	210		*	225		*	250	µA
	$\pm V_{CC}$ = 15V		(3)	230		*	250		*	275	µA
Over Temperature[2]	$\pm V_{CC}$ = 2.5V		(3)	275		*	300		*	325	µA
	$\pm V_{CC}$ = 15V		(3)	325		*	350		*	375	µA
Power Consumption	$\pm V_{CC}$ = 15V, T_A = +25°C			6.9			7.5			8.3	mW
TEMPERATURE RANGE											
Specification A, B		-55		+125	*		*	*		*	°C
E, F, G		-25		+85	*		*	*		*	°C
Operating A, B		-55		+125	*		*	*		*	°C
E, F, G		-25		+85	*		*	*		*	°C
Storage	"J" and "Z" Packages	-65		+125	*		*	*		*	°C

*Specification same as OPA21A, OPA21E

NOTES:

1. 100% tested. Guaranteed fully warmed-up 2. Over temperature specifications are -55°C ≤ T_A ≤ +125°C for A and B grades and -25°C ≤ T_A ≤ +85°C for E, F, and G grades. 3. See Typical Performance Curves

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation(1)	500mW
Input Voltage	Supply Voltage
Differential Input Voltage	±30V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
A, B,	-55°C to +125°C
E, F, G	-25°C to +85°C
Lead Temperature Range	
(Soldering, 60sec)	+300°C

NOTES:

1. Maximum package power dissipation vs ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	+80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	+75°C	6.7mW/°C

ORDERING INFORMATION

OPA21 Y Z

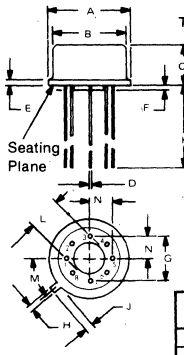
Basic Model Number

Performance Grade Code
- A, B -55°C to +125°C
- E, F, G -25°C to +85°C

Package Code
- J TO-99
- Z 8-Pin Hermetic DIP

TO-99 (J Suffix)	Hermetic DIP (Z Suffix)
OPA21AJ	OPA21AZ
OPA21BJ	OPA21BZ
OPA21EJ	OPA21EZ
OPA21FJ	OPA21FZ
OPA21GJ	OPA21GZ

MECHANICAL



TO-99 PACKAGE
("J" SUFFIX)

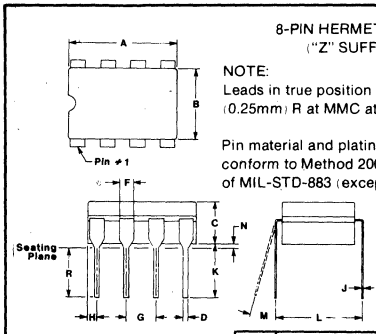
NOTE:
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

The TO-99 can and leads are bright acid tin plated.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67



8-PIN HERMETIC DIP
("Z" SUFFIX)

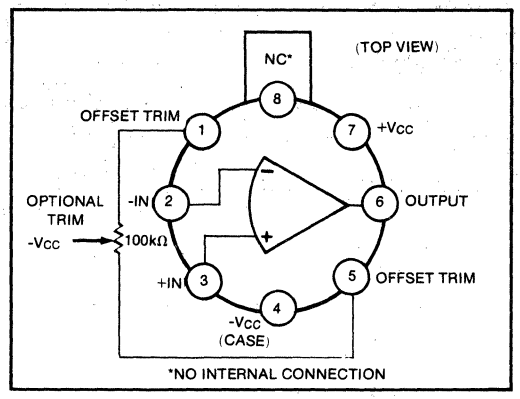
NOTE:
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

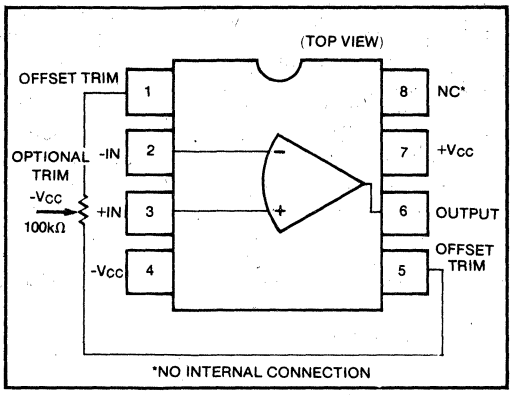
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	-	.098	-	2.49
J	.008	.012	0.20	0.30
K	.150	-	3.80	-
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.126	.175	3.18	4.45

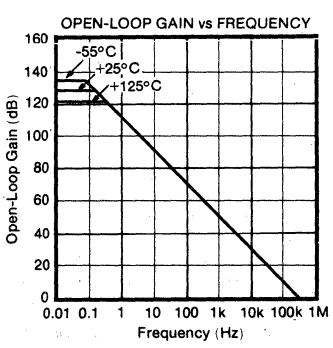
PIN CONFIGURATION

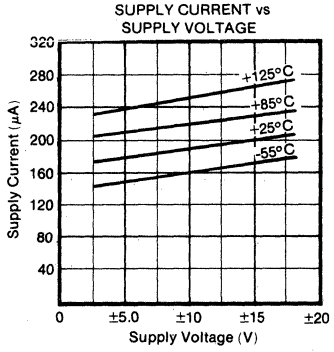


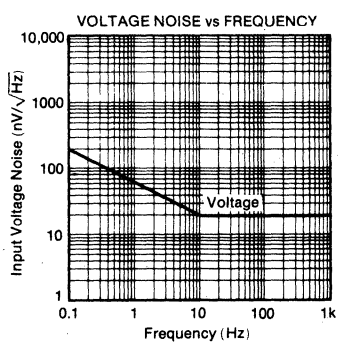


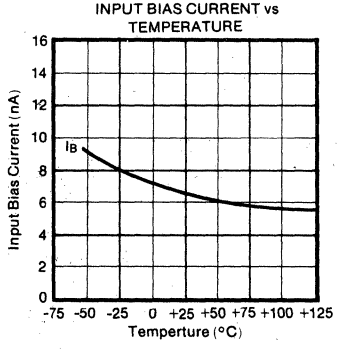
TYPICAL PERFORMANCE CURVES

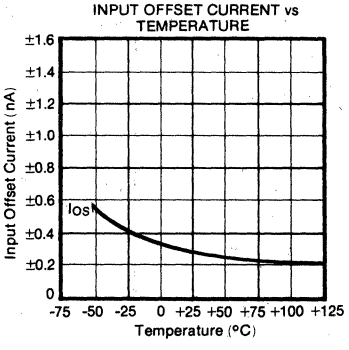
(T_A = +25°C, ±V_{CC} = 15VDC unless otherwise noted)

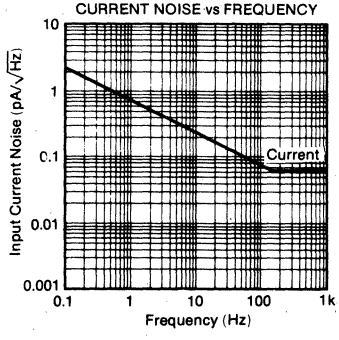




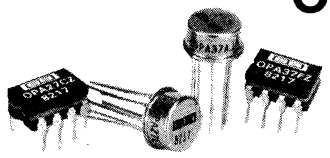








BURR-BROWN®



OPA27/OPA37

Ultra-Low Noise Precision OPERATIONAL AMPLIFIERS

FEATURES

- EXTREMELY-LOW NOISE
  - 3nV/$\sqrt{Hz}$ at 1kHz
  - 80nV, p-p from 0.1Hz to 10Hz
- LOW OFFSET VOLTAGE
  - 10μV
  - 0.2μV/°C
- HIGH SPEED
  - OPA27, 2.8V/μsec
  - OPA37, 17V/μsec
- EXCELLENT CMRR
  - 126dB over ±11V Input
- HIGH GAIN
  - 1800V/mV (125dB)
- FITS OP-07, OP-05, 725, AD510, AD517 SOCKETS

APPLICATIONS

- TRANSDUCER AMPLIFIER
- LOW NOISE INSTRUMENTATION AMPLIFIER
- DATA ACQUISITION PREAMPLIFIER
- PHONO AND TAPE PREAMPLIFIER
- FAST D/A CONVERTER OUTPUT
- WIDE BANDWIDTH INSTRUMENTATION AMPLIFIERS
- PRECISION COMPARATOR

DESCRIPTION

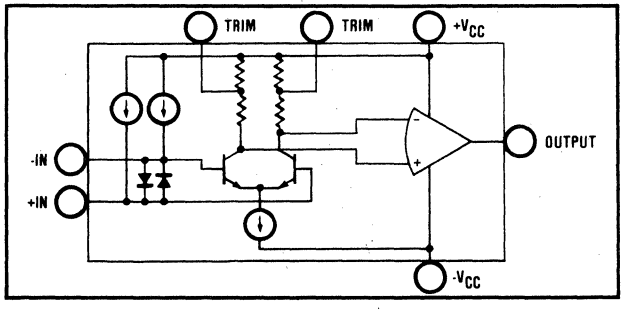
Low noise integrated processing, a unique circuit design, and advanced wafer level trimming techniques are combined in the OPA27/37 to produce an extremely-high performance "instrumentation grade" operational amplifier.

The OPA27/37 provide superior performance in three areas - low noise, excellent DC performance, and high speed (OPA37 is stable in gains > 5).

Noise is typically only 3nV/$\sqrt{Hz}$ at 1kHz with an exceptionally low 1/f corner frequency of 2.7Hz. Peak-to-peak noise is just 80nV in a 0.1Hz to 10Hz bandwidth.

Offset voltage is typically just 10μV and drift is only 0.2μV/°C. 125dB open-loop gain is matched with 125dB common-mode rejection ratio. Power consumption is only 3mA.

The same basic op amp comes in two frequency compensation versions. The OPA37 is lightly compensated and provides 17V/μsec slew rate and 63MHz gain-bandwidth product. The OPA27 is more heavily compensated for better frequency stability in low gain applications. It has a 2.8V/μsec slew rate and an 8MHz unity gain frequency.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

PARAMETERS	CONDITIONS	OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INITIAL OFFSET VOLTAGE											
Initial Offset[1]	T_A = +25°C		10	25		20	60		30	100	µV
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C		30	60		50	200		70	300	µV
Average vs Temperature	A, B, C -55°C ≤ T_A ≤ +125°C[2]		0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Over Temperature	E, F, G -25°C ≤ T_A ≤ +85°C		20	50		40	140		55	22	µV
Average vs Temperature	E, F, G -25°C ≤ T_A ≤ +85°C[2]		0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Long Term Stability[3]			0.2	1.0		0.3	1.5		0.4	2.0	µV/mo
Offset Adjustment Range			±4			•			•		mV
INPUT OFFSET CURRENT											
Initial Offset	T_A = +25°C		7	35		9	50		12	75	nA
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C		15	50		22	85		30	135	nA
	E, F, G -25°C ≤ T_A ≤ +85°C		10	50		14	85		20	135	nA
INPUT BIAS CURRENT											
Initial Bias	T_A = +25°C		±10	±40		±12	±55		±15	±80	nA
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C		±20	±60		±28	±95		±35	±150	nA
	E, F, G -25°C ≤ T_A ≤ +85°C		±14	±60		±18	±95		±25	±150	nA
INPUT NOISE											
Voltage	0.1Hz to 10Hz[4][5]		0.08	0.18		•	•		0.09	0.25	µV, p-p
Voltage Density	f_o = 10Hz[4]		3.5	5.5		•	•		3.8	8.0	nV $\sqrt{Hz}$
	f_o = 30Hz[4]		3.1	4.5		•	•		3.3	5.6	nV $\sqrt{Hz}$
	f_o = 1000Hz[4]		3.0	3.8		•	•		3.2	4.5	nV $\sqrt{Hz}$
Current Density	f_o = 10Hz[4][6]		1.7	4.0		•	•		•		pA $\sqrt{Hz}$
	f_o = 30Hz[4][6]		1.0	2.3		•	•		•		pA $\sqrt{Hz}$
	f_o = 1000Hz[4][6]		0.4	0.6		•	•		•	•	pA $\sqrt{Hz}$
INPUT RESISTANCE											
Differential[7]		1.5	6		1.2	5		0.8	4		MΩ
Common-Mode			3			2.5			2		GΩ
INPUT VOLTAGE RANGE											
Initial Input Voltage	T_A = +25°C	±11.0	±12.3		•	•		•	•		V
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C	±10.3	±11.5		•	•		•	•		V
	E, F, G -25°C ≤ T_A ≤ +85°C	±10.5	±11.8		•	•		•	•		V
COMMON-MODE REJECTION RATIO											
Initial Rejection Ratio	V_{CM} = ±11V	114	126		106	123		100	120		dB
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C	108	122		100	119		94	116		dB
Over Temperature	E, F, G -25°C ≤ T_A ≤ +85°C	110	124		102	121		96	118		dB
POWER SUPPLY REJECTION RATIO											
Initial Rejection Ratio	$\pm V_{CC}$ = 4V to 18V	100	120		•	•		94	118		dB
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C $\pm V_{CC}$ = 4.5V to 18V	96	116		94	114		86	110		dB
Over Temperature	E, F, G -25°C ≤ T_A ≤ +85°C $\pm V_{CC}$ = 4.5V to 18V	97	118		96	116		90	114		dB
LARGE SIGNAL VOLTAGE GAIN[8]											
Initial Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	1000	1800		•	•		700	1500		V/mV
	R_L ≥ 1kΩ, V_O = ±10V	800	1500		•	•		•	•		V/mV
	R_L ≥ 600Ω, V_O = ±1V, V_{CC} = ±4V[7]	250	700		•	•		200	500		V/mV
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C R_L ≥ 2kΩ, V_O = ±10V	600	1200		500	1000		300	800		V/mV
Over Temperature	E, F, G -25°C ≤ T_A ≤ +85°C R_L ≥ 2kΩ, V_O = ±10V	750	1500		700	1300		450	1000		V/mV
RATED OUTPUT											
Initial Voltage Swing	R_L ≥ 2kΩ	±12.0	±13.8		•	•		±11.5	±13.5		V
	R_L ≥ 600Ω	±10.0	±11.5		•	•		•	•		V
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C R_L ≥ 2kΩ	±11.5	±13.5		±11.0	±13.2		±10.5	±13.0		V
Over Temperature	E, F, G -25°C ≤ T_A ≤ +85°C R_L ≥ 2kΩ	±11.7	±13.6		±11.4	±13.5		±11.0	±13.3		V
Output Resistance	Open Loop		70			•			•		Ω
DYNAMIC RESPONSE											
Slew Rate	OPA27	1.7	2.8		•	•		•	•		V/µsec
	OPA37	11	17		•	•		•	•		V/µsec
Gain-Bandwidth Product	OPA27	5	8		•	•		•	•		MHz
	OPA37		40			•			•		MHz

ELECTRICAL (CONT)

PARAMETERS	CONDITIONS	OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY											
Rated Voltage			±15								VDC
Voltage Range		±4		±22							VDC
Current, Quiescent			±3	±4.7					±3.3	±5.7	mA
Power Consumption			90	140					100	170	mW
TEMPERATURE RANGE											
Specification A, B, C		-55		+125							°C
E, F, G		-25		+85							°C
Operating A, B, C		-55		+125							°C
E, F, G		-25		+85							°C
Storage		-65		+150							°C

*Specification same as OPA27/37A and OPA27/37E.

NOTES: (1) The input offset voltage tests are done on automatic test equipment approximately 0.5 seconds after power is applied to the device. The A and E grades have guaranteed specifications under full warm up conditions. (2) Offset voltage drift with temperature specification holds for the unnulled condition or when nulled with R_p = 8kΩ to 20kΩ. (3) Long term offset voltage stability is defined by an average, extended time, trend line (V_{os} vs temp.) after 30 days of initial operation. As shown in the typical performance curves, V_{os} changes approximately 2.5μV in the first 30 days excluding the initial hour of operation. (4) Parameter is not 100% tested; 90% of units meet this specification. (5) See Figures 1 and 2. (6) See Figure 1 for current noise measurement. (7) Parameter is guaranteed by design and is not tested. (8) Closed-loop gain ≥ 5 is required for stability in the OPA37. OPA27 is stable at unity gain.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation(1) 500mW
Input Voltage(2) ..... ±22V
Output Short Circuit Duration(3) ..... Indefinite
Differential Input Voltage(4) ..... ±0.7V
Differential Input Current(4) ..... ±25mA
Storage Temperature Range .... −65°C to +150°C
Operating Temperature Range
A, B, C ..... -65°C to +150°C
E, F, G ..... -25°C to +85°C
Lead Temperature Range
(Soldering, 60sec) ..... 300°C

NOTES:

1. Maximum package power dissipation vs ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. To common with $\pm V_{cc}$ = 15V.
4. The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

ORDERING INFORMATION

OPAXX Y Z

Basic Model Number
Performance Grade Code
A, B, C: −55°C to +125°C
E, F, G: −25°C to +85°C
Package Code
J = TO-99
Z = 8-Pin Hermetic DIP

TO-99 J SUFFIX		8-PIN HERMETIC DIP	
OPA27AJ	OPA27EJ	OPA27AZ	OPA27EZ
OPA27BJ	OPA27FJ	OPA27BZ	OPA27FZ
OPA27CJ	OPA27GJ	OPA27CZ	OPA27GZ
OPA37AJ	OPA37EJ	OPA37AZ	OPA37EZ
OPA37BJ	OPA37FJ	OPA37BZ	OPA37FZ
OPA37CJ	OPA37GJ	OPA37CZ	OPA37GZ

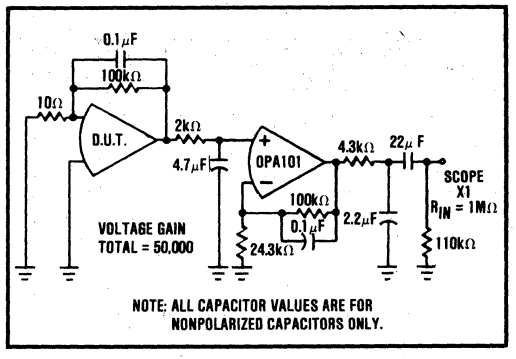


FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

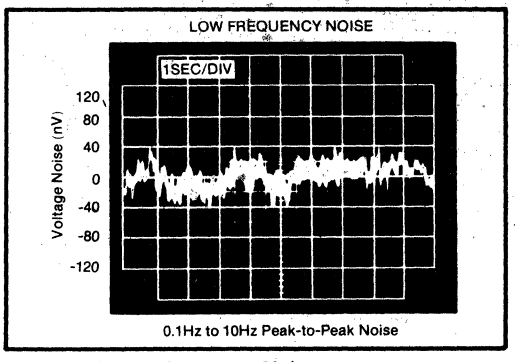
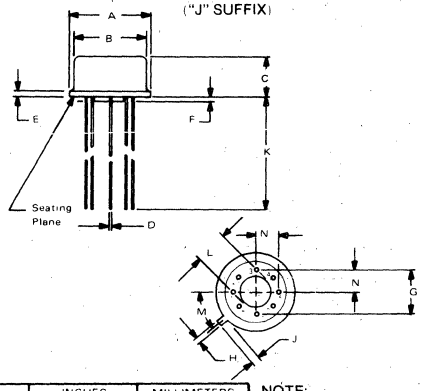


FIGURE 2. Low Frequency Noise.

MECHANICAL

TO-99 PACKAGE
("J" SUFFIX)



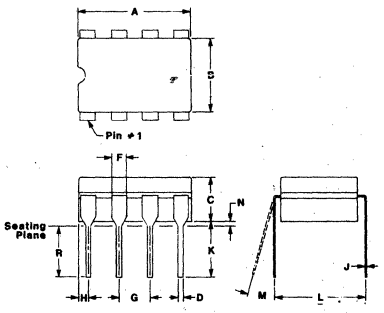
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to Method 2003. (solderability) of MIL-STD-883 except paragraph 3.2).

8-PIN HERMETIC DIP
("Z" SUFFIX)

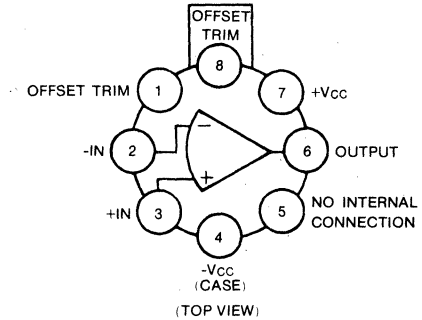


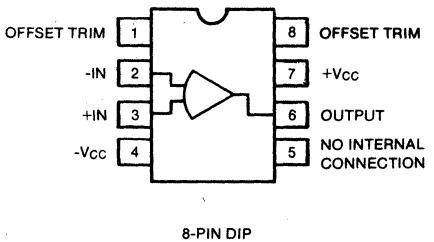
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.375	.405	9.53	10.28
B	.245	.261	6.22	6.38
C	.140	.170	3.56	4.32
D	.016	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	-	.095	-	2.49
J	.008	.012	0.20	0.30
K	.150	-	3.80	-
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 except paragraph 3.2).

PIN CONFIGURATION

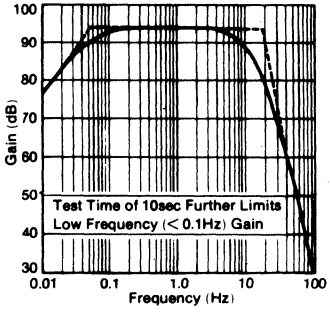




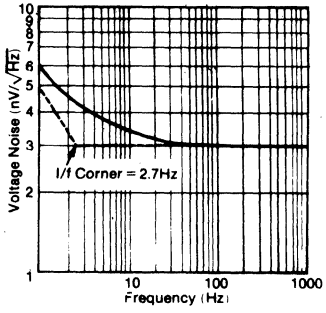
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = 15VDC unless otherwise noted)

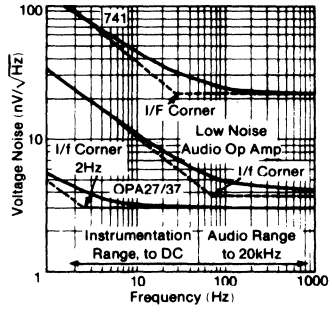
0.1Hz TO 10Hz, p-p NOISE TESTER FREQUENCY RESPONSE



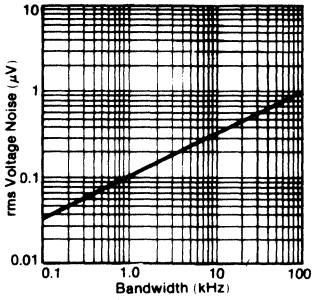
VOLTAGE NOISE VS FREQUENCY



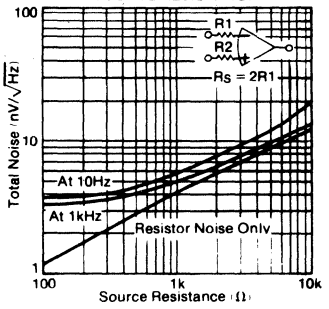
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRUMS



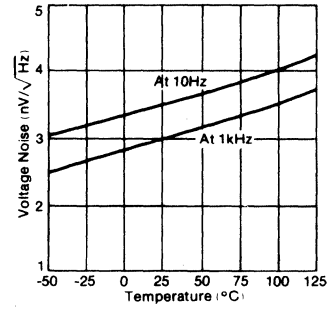
INPUT WIDEBAND VOLTAGE NOISE VS BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



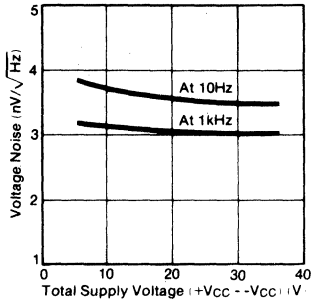
TOTAL NOISE VS SOURCE RESISTANCE



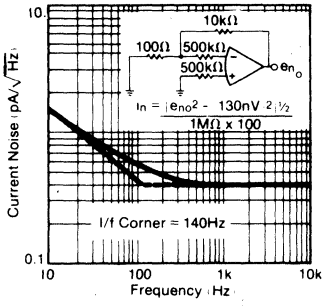
VOLTAGE NOISE VS TEMPERATURE



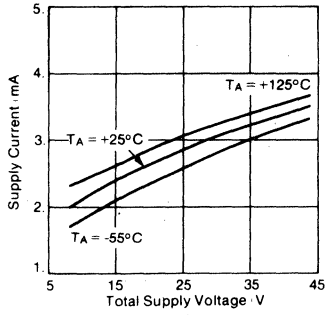
VOLTAGE NOISE VS SUPPLY VOLTAGE



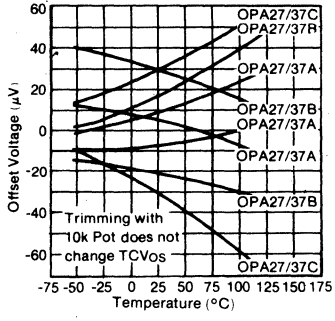
CURRENT NOISE VS FREQUENCY



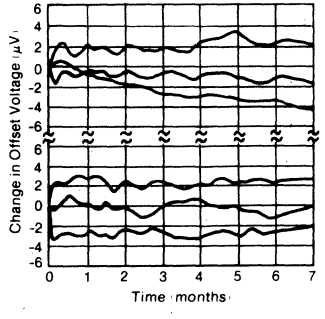
SUPPLY CURRENT VS SUPPLY VOLTAGE



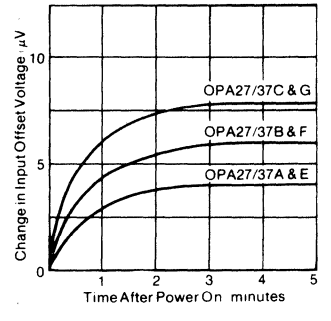
OFFSET VOLTAGE DRIFT OF REPRESENTATIVE UNITS



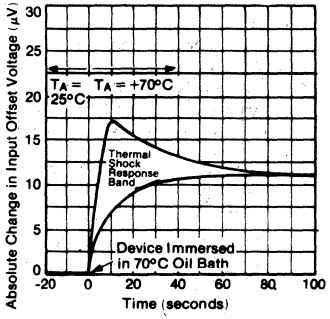
LONG TERM DRIFT OF REPESENTATIVE UNITS



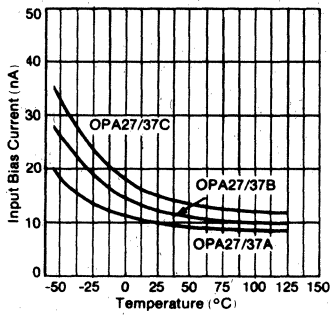
WARM-UP DRIFT



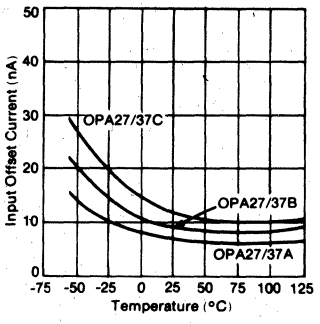
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



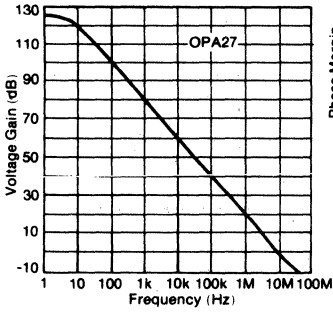
INPUT BIAS CURRENT VS TEMPERATURE



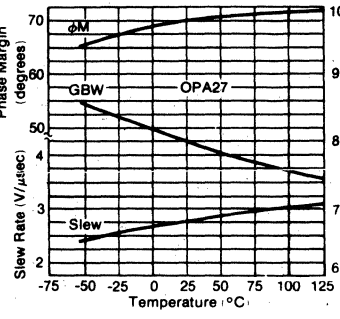
INPUT OFFSET CURRENT VS TEMPERATURE



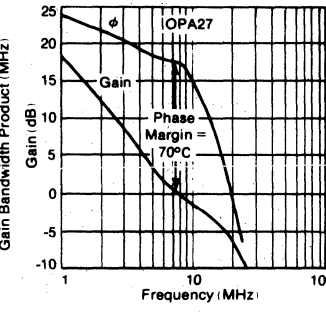
OPEN-LOOP GAIN VS FREQUENCY



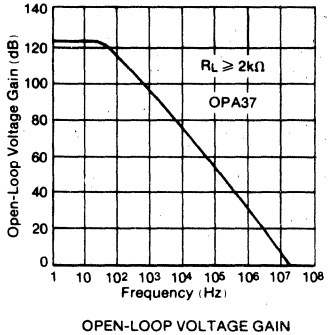
SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN VS TEMPERATURE



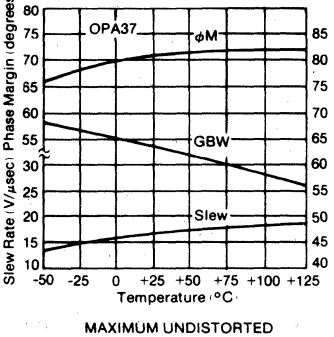
GAIN, PHASE SHIFT VS FREQUENCY



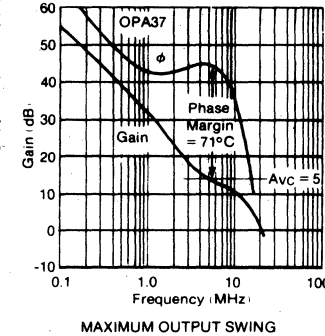
OPEN-LOOP GAIN VS FREQUENCY



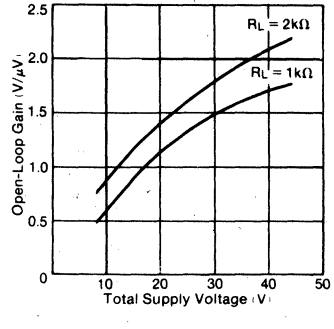
SLEW RATE, GAIN BANDWIDTH PRODUCT PHASE MARGIN VS TEMPERATURE



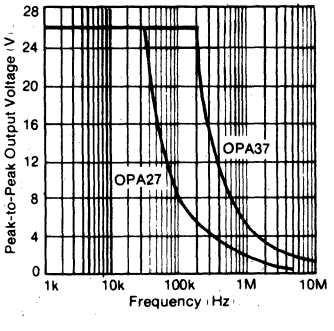
GAIN, PHASE VS FREQUENCY



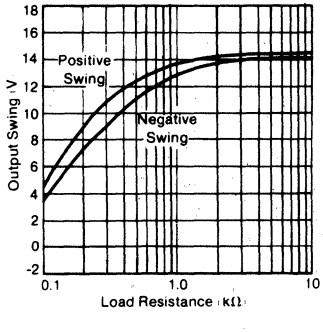
OPEN-LOOP VOLTAGE GAIN VS SUPPLY VOLTAGE



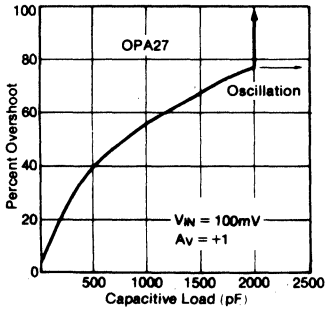
MAXIMUM UNDISTORTED OUTPUT VS FREQUENCY



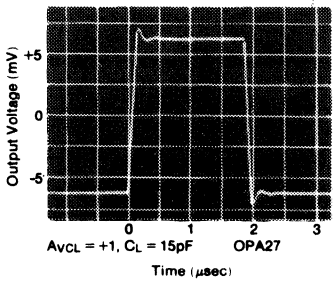
MAXIMUM OUTPUT SWING VS RESISTIVE LOAD



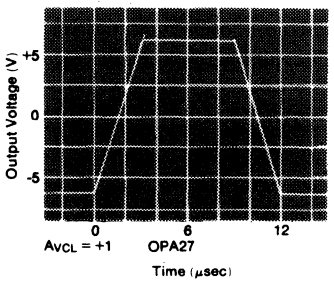
SMALL SIGNAL OVERSHOOT VS CAPACITIVE LOAD



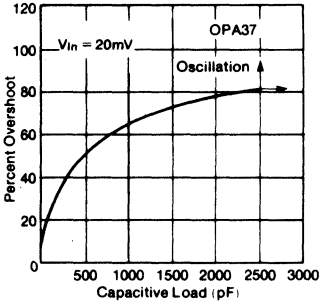
SMALL SIGNAL TRANSIENT RESPONSE



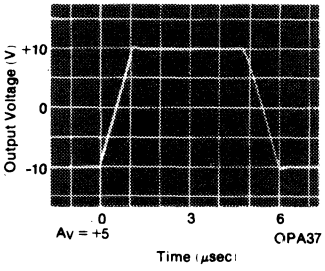
LARGE SIGNAL TRANSIENT RESPONSE



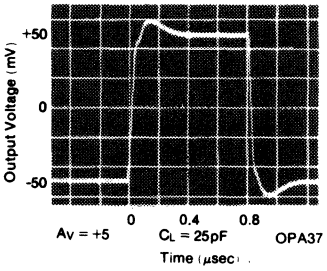
SMALL SIGNAL OVERSHOOT VS CAPACITIVE LOAD



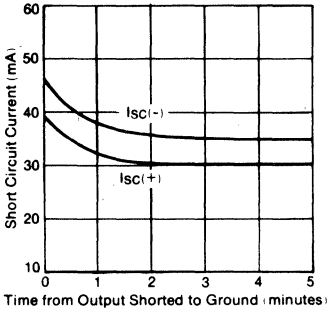
LARGE SIGNAL TRANSIENT RESPONSE



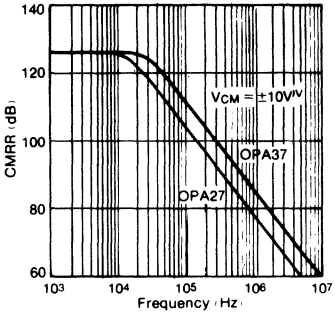
SMALL SIGNAL TRANSIENT RESPONSE



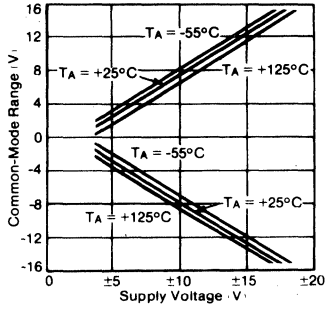
SHORT CIRCUIT CURRENT VS TIME



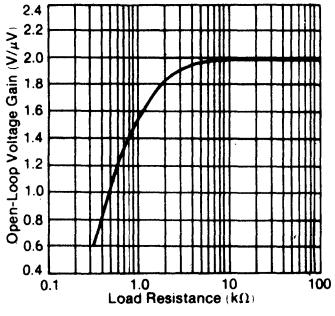
CMRR VS FREQUENCY



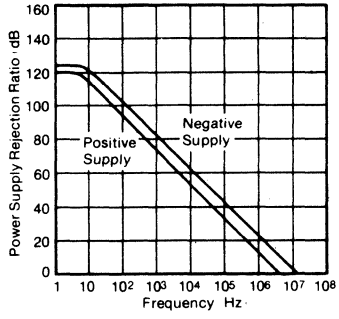
COMMON-MODE INPUT RANGE VS SUPPLY VOLTAGE



OPEN-LOOP VOLTAGE GAIN VS LOAD RESISTANCE



PSRR VS FREQUENCY



APPLICATION INFORMATION

The OPA27/37 are ideally suited for general purpose or high performance low voltage noise applications where input impedances are moderate. These amplifiers fit directly into the sockets of the 725, OP-05, OP-06, OP-07, AD510, and AD517 without changing compensation or nulling components. Typical 741 nulling circuitry, however, will require modification (or removal if not needed) as shown in Figure 3.

Stable operation is inherently provided with capacitive loads up to 2000pF at ±10V output swing, but a series 50Ω decoupling resistor should be used with larger capacitances.

In high performance low noise applications, it is important to observe proper PC board layout techniques such as short runs to the input pins and substantial ground connections converging at a single point. Also, to achieve the specified drift, careful attention must be paid to minimizing thermoelectric voltages resulting from dissimilar metals at the pin contacts. Best results can be obtained by maintaining equal temperatures at both input contacts which are equal to the temperature of the package. Also a 5-minute warm-up and minimization of air currents are recommended.

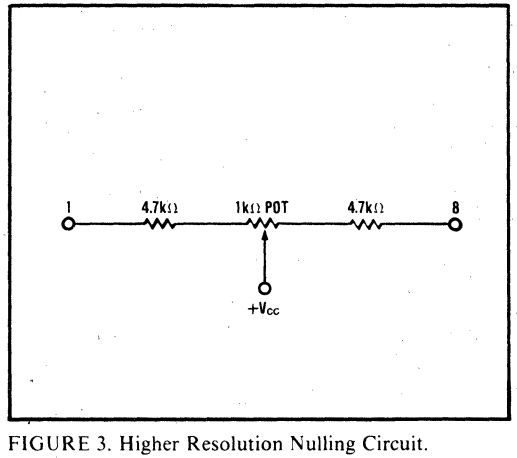


FIGURE 3. Higher Resolution Nulling Circuit.

OFFSET VOLTAGE ADJUSTMENT

The OPA27/37's input offset voltage and drift with temperature have been precisely trimmed internally at the time of manufacture, but should a refinement in trimming be necessary, a potentiometer (see Figure 4) can be used without degrading $\Delta V_{OS}/\Delta$temp. A minor degradation in drift (0.1 to 0.2μV/°C) will occur, however, if other values from 1kΩ to 1MΩ are used. Also trimming a nonzero value will result in an additional drift of $V_{OS}/300\mu V/°C$. For example, an adjustment of V_{OS} to 100μV will cause a 0.33μV/°C drift change. Higher resolution in V_{OS} adjustment can be realized by a smaller potentiometer value plus series resistors as shown in Figure 3 (+280μV adjustment range shown).

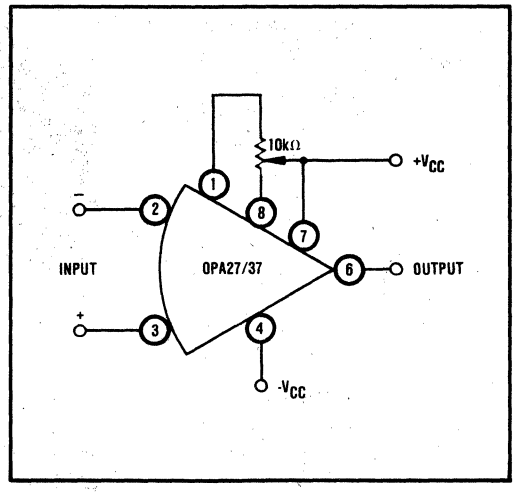


FIGURE 4. Offset Nulling Circuit.

UNITY GAIN BUFFER APPLICATIONS—OPA27

Figure 5 shows the output waveform shape when the feedback resistor, R_f, is less than 100Ω and the input voltage is a fast rising large signal greater than 1V. The break voltage appears as "feedthrough" and results from

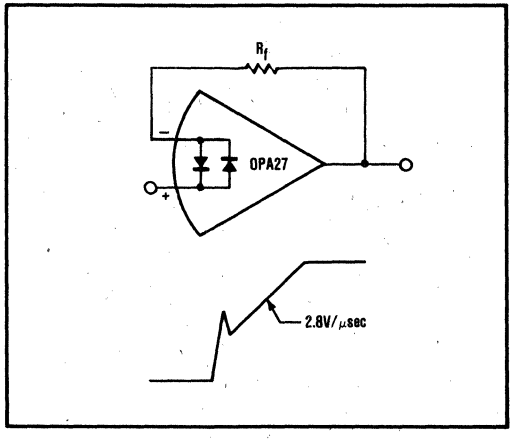


FIGURE 5. Pulsed Operation.

the conduction of the input protection diodes which effectively shorts the output to the input. A short circuit current is then drawn by the input source. When the feedback is greater than 500Ω, the output is capable of driving the required current (less than 20mA at 10V) and the amplifier remains in its linear region producing a smooth transition.

All op amps have input capacitance, so the feedback resistor in combination with this causes a pole to be generated which gives an additional phase shift. Greater than 2kΩ and 8pF adversely reduces the phase margin, but this problem can be eliminated with a 20pF to 50pF capacitor in parallel with R_f.

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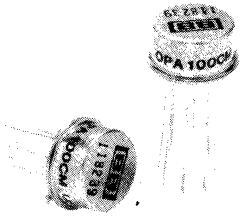


OPA100

Low Bias Current JFET Monolithic OPERATIONAL AMPLIFIER

FEATURES

- LOW INITIAL BIAS CURRENT
  1pA max at +25°C
- LOW BIAS CURRENT vs TEMPERATURE
  20pA max at +85°C
- HIGH INPUT IMPEDANCE, $10^{12}\Omega$
- LOW OFFSET VOLTAGE, 250μV max
- LOW OFFSET VOLTAGE DRIFT, 5μV/°C max

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS SUCH AS:
  pH electrodes
  Biological probes/transducers
- PHOTO DETECTOR CIRCUITS
- LONG-TERM PRECISION INTEGRATION
- HIGH IMPEDANCE BUFFER
- PRECISION SAMPLE/HOLD

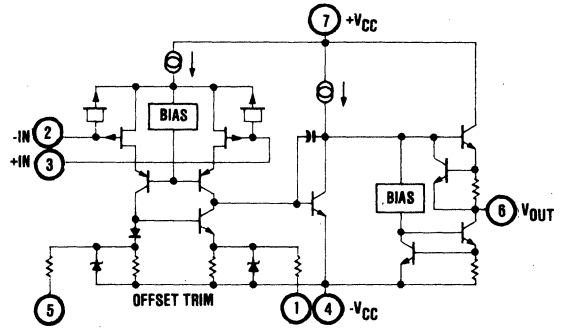
DESCRIPTION

The OPA100 is a precision monolithic low bias current operational amplifier. An enhanced bipolar FET process with JFET input transistors and dielectric isolation is used to achieve low input bias current. Additionally, bias current compensation circuitry is used to reduce the bias current even further. In addition to lowering the bias current at +25°C, this compensation significantly reduces the bias current at higher temperatures.

Low offset voltage (250μV max) and low voltage drift (5μV/°C) are also guaranteed. This performance is achieved by active laser-trimming the amplifiers thin-film resistors.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to supply terminals without damage.

The standard pin configuration (741-type) of the OPA100 allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

PARAMETER	CONDITIONS	OPA100AM			OPA100BM			OPA100CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN, DC	V_{OUT} = ±10V										
Rated Load, $R_L \geq 2k\Omega$	T_A = +25°C	94	100		100	106		106	110		dB
	$T_A = T_{MIN}$ to T_{MAX}	88	100		94	106		100	110		dB
RATED OUTPUT											
Voltage at $R_L = 2k\Omega$	$T_A = T_{MIN}$ to T_{MAX}	±10	±12		•	•		•	•		V
Current	$T_A = T_{MIN}$ to T_{MAX}	±5	±10		•	•		•	•		mA
Output Impedance			100			•			•		Ω
Load Capacitance[1]		500	1000		•	•		•	•		pF
Short Circuit Current		10	40		•	•		•	•		mA
FREQUENCY RESPONSE											
Unity Gain, Small Signal			1			•			•		MHz
Full Power Response		10	32		•	•		•	•		kHz
Slew Rate		0.6	2		•	•		•	•		V/µsec
Settling Time 0.1%	10V step		6			•			•		µsec
Settling Time 0.01%	10V step		10			•			•		µsec
Overload Recovery, 50% overdrive[2]			5			•			•		µsec
INPUT OFFSET VOLTAGE[3]											
Initial Offset	T_A = +25°C		±200	±1000		±100	±500		±50	±250	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±15		•	±10		±1	±5	µV/°C
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}			±2			±1/±1.5		•	±0.5	mV
vs Supply	$T_A = T_{MIN}$ to T_{MAX}		±10	±100		•	±25		•	±25	µV/V
INPUT BIAS CURRENT[3]											
Initial Bias Current	T_A = +25°C		±1	±3		±0.6	±2		±0.3	±1	pA
Over Temperature	T_A = +85°C		±10	±100		•	±40		±5	±20	pA
INPUT OFFSET CURRENT											
Initial Difference Current	T_A = +25°C		±0.5			•			•		pA
Over Temperature	T_A = +85°C		±10			•			±5		pA
INPUT IMPEDANCE											
Differential			$10^{12} \| 6$			•			•		Ω || pF
Common-Mode			$10^{13} \| 6$			•			•		Ω || pF
INPUT NOISE											
Voltage: f_O = 10Hz			60			•			•		nV/√Hz
f_O = 100Hz			35			•			•		nV/√Hz
f_O = 1kHz			20			•			•		nV/√Hz
f_O = 10kHz			20			•			•		nV/√Hz
f_B = 0.1Hz to 10Hz			1			•			•		µV, p-p
Current: f_B = 0.1Hz to 10Hz			0.01			•			•		pA, p-p
f_B = 10Hz to 10kHz			0.03			•			•		pA, rms
f_O = 1kHz			0.6			•			•		fA/√Hz
INPUT VOLTAGE RANGE											
Differential		±18			•			•			V
Common-Mode	$T_A = T_{MIN}$ to T_{MAX}	±10	±12		•	•		•	•		V
Common-Mode Rejection, V_{IN} = ±10V	$T_A = T_{MIN}$ to T_{MAX}	76	82		88	94		94	100		dB
Maximum Safe Input Voltage			$\pm V_{CC}$			•			•		V
POWER SUPPLY											
Rated Voltage			±15			•			•		VDC
Voltage Range, Derated Performance		±5		±18	•		•	•		•	VDC
Current, Quiescent	$T_A = T_{MIN}$ to T_{MAX}		1.0	3		•	2		•	1.5	mA
TEMPERATURE RANGE	Ambient										
Specification		−25		+85	•		•	•		•	°C
Operating		−55		+125	•		•	•		•	°C
Storage		−65		+150	•		•	•		•	°C
θ Junction-Ambient			300			•			•		°C/W

*Specification same as for OPA100AM.

NOTES: (1) Stability guaranteed with load capacitance ≤500pF. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (3) Offset voltage and bias current are guaranteed after 1 minute of operation at T_A = +25°C. They are 100% tested.

ORDERING INFORMATION

OPA100 X X

Basic model number

Performance grade
A, B, C -25°C to +85°C

Package code
TO-99 metal can, M

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal power Dissipation(1)	500mW
Differential Input Voltage(2)	±36VDC
Input Voltage Range(2)	±18VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration(3)	Continuous
Junction Temperature	+175°C

NOTES:
1. Package must be derated based on: θ_{JC} = 150°C/W or θ_{JA} = 300°C/W.
2. For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to power supply common only. Rating applies to +25°C ambient.

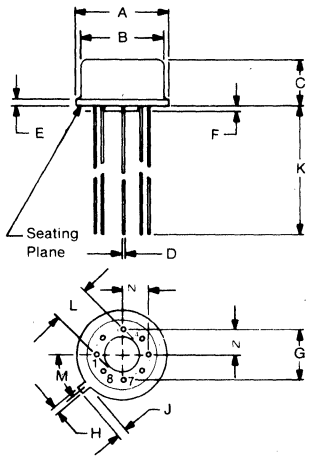
MECHANICAL

TO-99 PACKAGE

NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

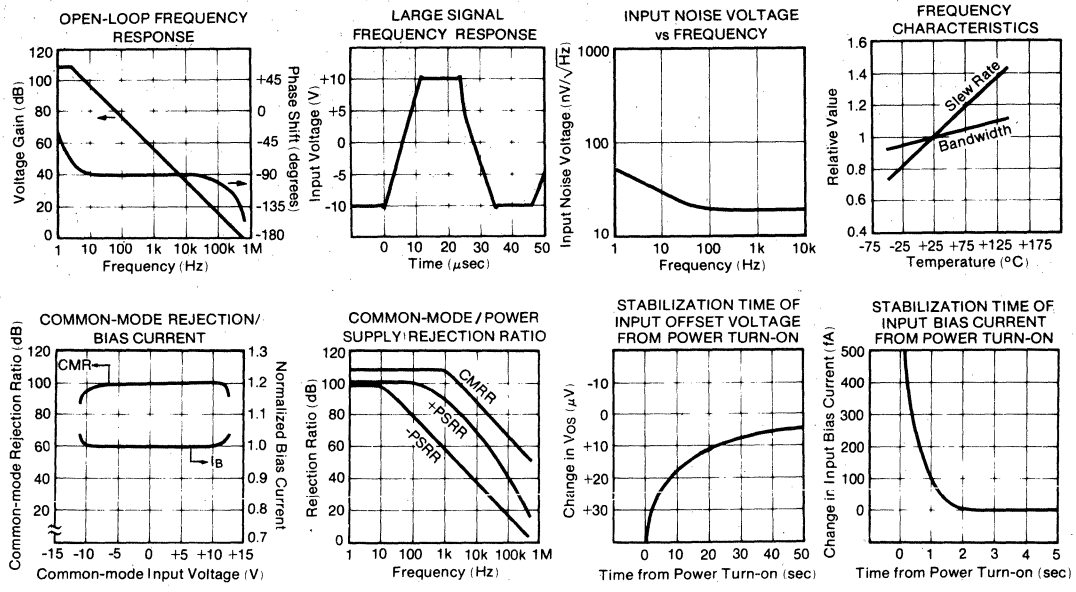
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

TYPICAL PERFORMANCE CURVES

At T_A = +25°C and ±V_{CC} = 15VDC unless otherwise noted.



APPLICATIONS INFORMATION

INPUT BIAS CURRENT

The OPA100 uses FET input transistors with dielectric isolation to achieve low input bias currents. Additionally, bias current compensation circuitry is used to reduce the bias current even further. In addition to lowering the bias current at +25°C, this compensation makes significant reduction in the bias current at higher temperatures. Figure 1 shows an improvement of over a decade for temperatures above +75°C.

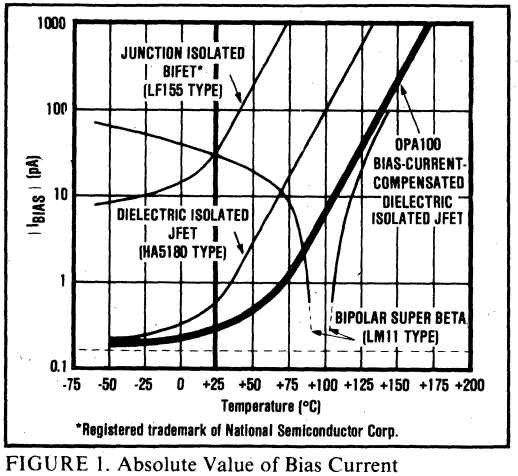


FIGURE 1. Absolute Value of Bias Current vs Temperature.

The compensation causes the polarity of the bias current to be indeterminate (note the "±" signs for I_B in the electrical specifications). This means that the bias current may flow into or out of the amplifier inputs.

VOLTAGE NOISE

In many FET amplifier applications the voltage noise is a critical parameter. The bias current cancellation design of the OPA100 allows low noise without sacrificing low bias current. Figure 2 shows the noise of various types of

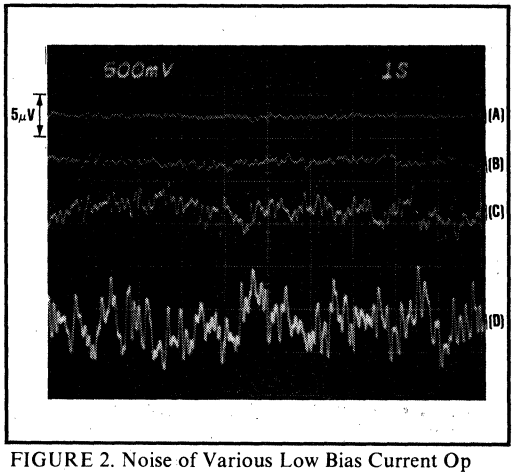


FIGURE 2. Noise of Various Low Bias Current Op Amps. (A) OPA100, (B) LF155 type, (C) LM11 type, (D) HA 5180 type.

low bias current operational amplifiers. The noise test circuit used has a gain of 100kV/V with a 1-pole filter at 0.1Hz and a 5-pole filter at 10Hz.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA100. To avoid leakage problems, it is recommended that the signal input lead of the OPA100 be wired to a Teflon standoff. If the OPA100 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 3).

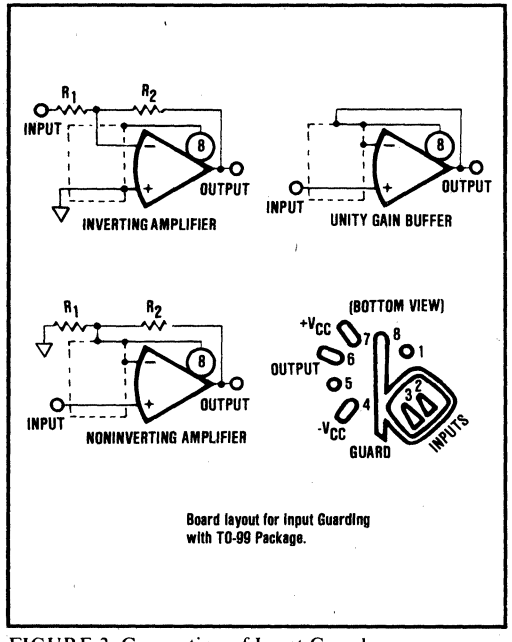


FIGURE 3. Connection of Input Guard.

OFFSET VOLTAGE ADJUSTMENT

Although the OPA100 has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. External offset voltage adjustment changes the drift by approximately 0.3μV/°C, for every 100μV of offset adjusted. See Figure 4.

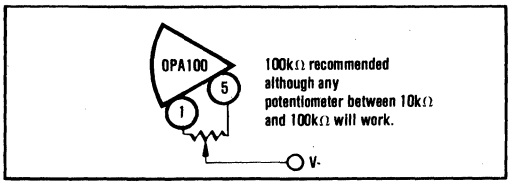


FIGURE 4. External Nulling of Offset Voltage.

APPLICATION CIRCUITS

The OPA100 is ideally suited for low bias current, high input impedance applications. Also because the noise and offset drift errors are low, total high performance can be achieved. Figures 5 through 8 show a photodiode, pH probe, isolation, and integrator amplifier.

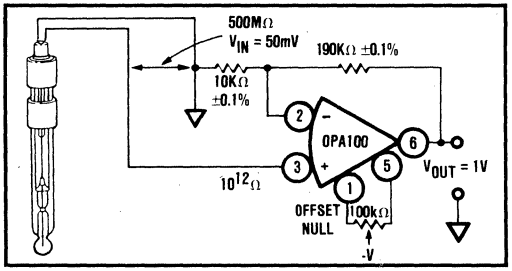


FIGURE 5. pH Probe Amplifier.

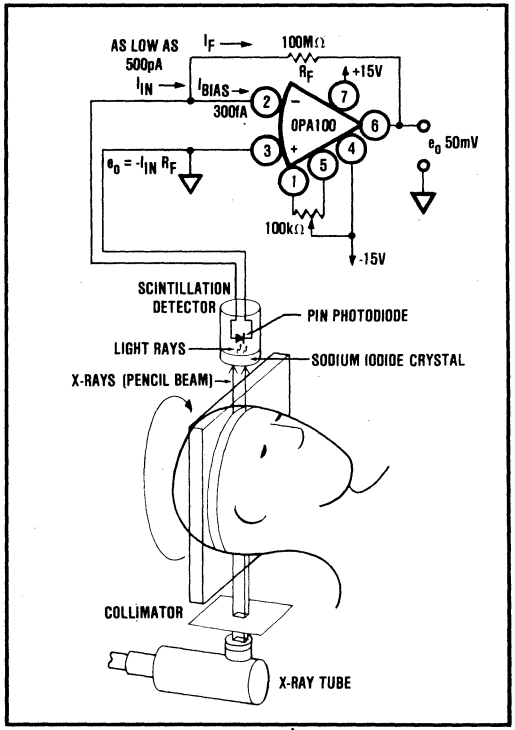


FIGURE 6. Computerized Axial Tomography (CAT) Scanner Channel Amplifier.

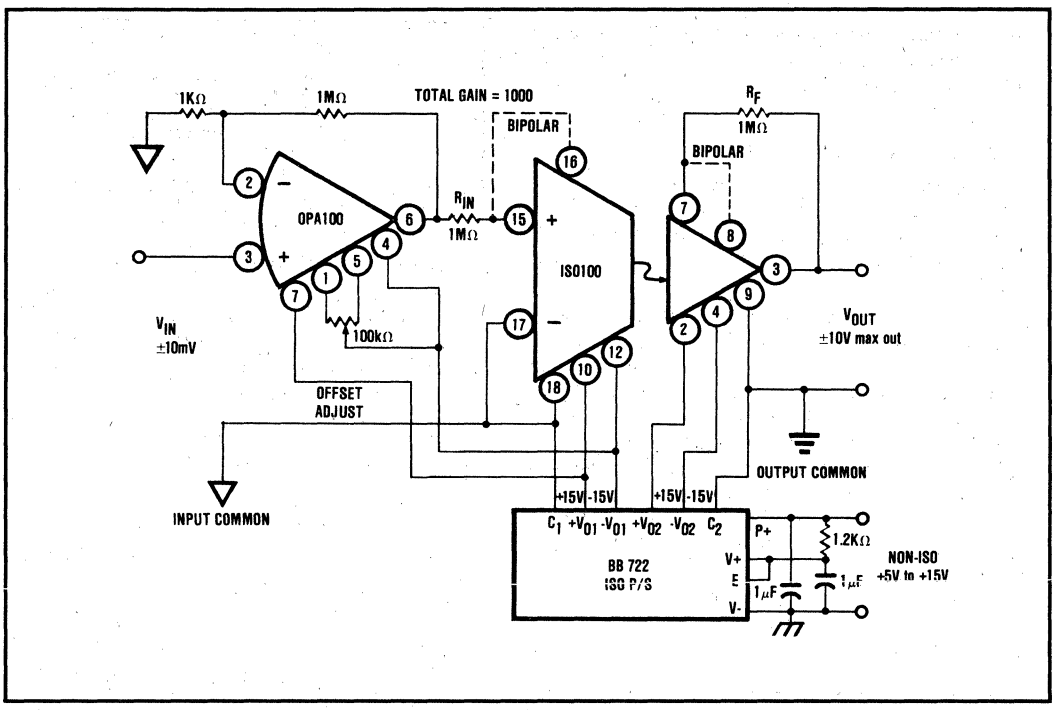


FIGURE 7. Low Level High Impedance Isolation Amplifier.

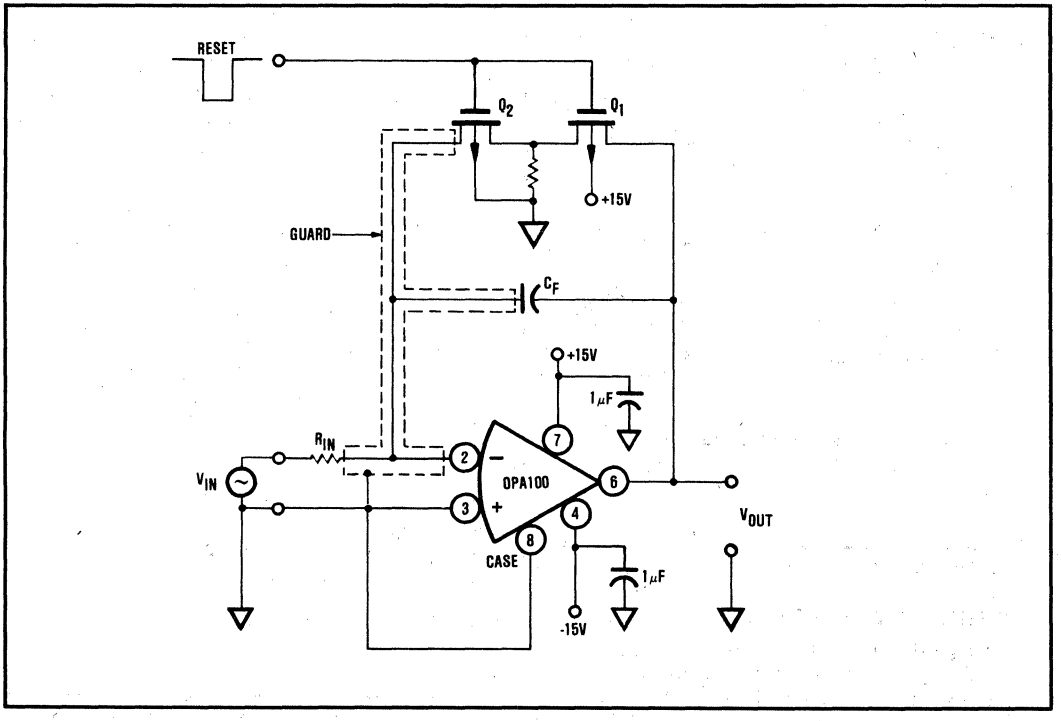


FIGURE 8. High Accuracy Integrator with Reset.

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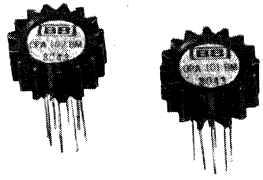


OPA101
OPA102

Low Noise - Wideband
PRECISION JFET INPUT OPERATIONAL AMPLIFIER

FEATURES

- GUARANTEED NOISE SPECTRAL DENSITY - 100% Tested
- LOW VOLTAGE NOISE - 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW VOLTAGE DRIFT - 5μV/°C max (B grade)
- LOW OFFSET VOLTAGE - 250μV max (B grade)
- LOW BIAS CURRENTS - 10pA max at 25°C Ambient (B Grade)
- HIGH SPEED - 10V/μsec min (OPA102)
- GAIN BANDWIDTH PRODUCT - 40MHz (OPA102)

APPLICATIONS

- LOW NOISE SIGNAL CONDITIONING
- LIGHT MEASURMENTS
- RADIATION MEASUREMENTS
- PIN DIODE APPLICATIONS
- DENSITOMETERS
- PHOTODIODE/PHOTOMULTIPLIER CIRCUITS
- LOW NOISE DATA ACQUISITION

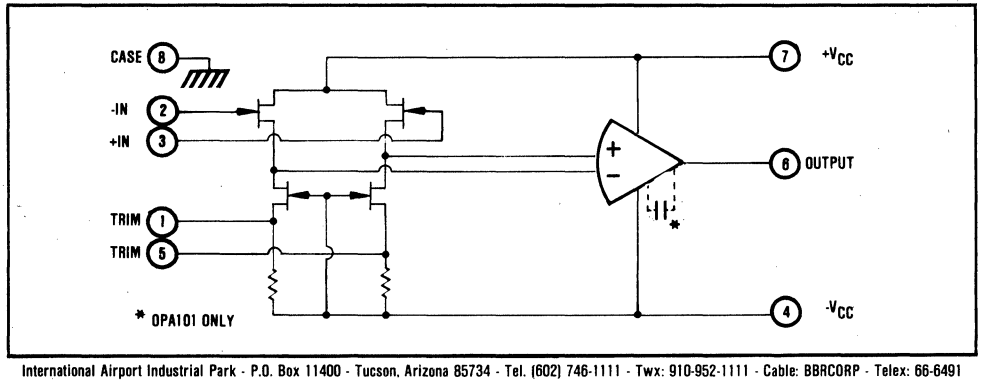
DESCRIPTION

The OPA101 and OPA102 are the first FET operational amplifiers available with noise characteristics (voltage spectral density) guaranteed and 100% tested.

The amplifiers have a complementary set of specifications permitting low errors in signal conditioning applications; low noise, low bias current, high open-loop gain, high common-mode rejection, low offset voltage, low offset voltage drift, etc.

In addition, the amplifiers have moderately high speed. The OPA101 is compensated for unity gain stability and has a slew rate of 5V/μsec, min. The OPA102 is compensated for gains of 3V/V and above and has a slew rate of 10V/μsec, min.

Each unit is laser-trimmed for low offset voltage and low offset voltage drift versus temperature. Bias currents are specified with the units fully warmed up at +25°C ambient temperature.



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SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT NOISE								
Voltage Noise Density	f_o = 1Hz(1)		100	200		80	100	nV/√Hz
	f_o = 10Hz		32	60		25	30	nV/√Hz
	f_o = 100Hz		14	30		11	15	nV/√Hz
	f_o = 1kHz		9	15		8	12	nV/√Hz
	f_o = 10kHz		7	8		7	8	nV/√Hz
	f_o = 100kHz		6.5	8		6.5	8	nV/√Hz
f_C; 1/f Corner Frequency			125			100		Hz
Voltage Noise	f_B = 0.1Hz to 10Hz(1)		1.3	2.6		1.0	1.3	μV, p-p
	f_B = 10Hz to 10kHz		1.0	1.2		0.8	1.0	μV, rms
	f_B = 10Hz to 100kHz		2.1	2.6		2.1	2.6	μV, rms
Current Noise Density	f_o = 0.1Hz thru 10kHz		2.0			1.4		fA/√Hz
Current Noise	f_B = 0.1Hz to 10Hz		38			26		fA, p-p
	f_B = 10Hz to 10kHz		200			140		fA, rms
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal							
OPA101			10			*		MHz
OPA102			Note 2			*		
Gain-Bandwidth Product	A_{CL} = 100							
OPA101			20			*		MHz
OPA102			40			*		MHz
Full Power Bandwidth	V_o = 20V, p-p; R_L = 1kΩ							
OPA101		80	100		*	*		kHz
OPA102		160	210		*	*		kHz
Slew Rate	V_o = ±10V; R_L = 1kΩ							
OPA101	A_{CL} = -1	5	6.5		*	*		V/μsec
OPA102	A_{CL} = -3	10	14		*	*		V/μsec
Settling Time (OPA101)	V_o = ±5V; A_{CL} = -1; R_L = 1kΩ							
ε = 1%			2			*		μsec
ε = 0.1%			2.5			*		μsec
ε = 0.01%			10			*		μsec
Settling Time (OPA102)	V_o = ±5V; A_{CL} = -3; R_L = 1kΩ							
ε = 1%			1			*		μsec
ε = 0.1%			1.5			*		μsec
ε = 0.01%			8			*		μsec
Small-Signal Overshoot	R_L = 1kΩ; C_L = 100pF							
OPA101	A_{CL} = +1		15			*		%
OPA102	A_{CL} = +3		20			*		%
Rise Time	10% to 90%, Small Signal							
OPA101			40			*		nsec
OPA102			30			*		nsec
Phase Margin	R_L = 1kΩ							
OPA101	A_{CL} = +1		60			*		Degrees
OPA102	A_{CL} = +3		45			*		Degrees
Overload Recovery(3)								
OPA101	A_{CL} = -1, 50% overdrive		1			*		μsec
OPA102	A_{CL} = -3, 50% overdrive		0.8			*		μsec
OPEN-LOOP GAIN, DC								
Full Load	V_o = ±10V; R_L = 1kΩ	94	105		*	*		dB
No Load	V_o = ±10V; R_L ≥ 10kΩ	96	108		*	*		dB
RATED OUTPUT								
Voltage	I_o = ±12mA	±12	±13		*	*		V
Current	V_o = ±12V	±12	±30		*	*		mA
Output Resistance	Open-Loop, f = DC		500			*		Ω
Short-Circuit Current			±45			*		mA
Capacitive Load Range	Phase Margin ≥ 25°							
OPA101	A_{CL} = +1		500			*		pF
OPA102	A_{CL} = +3		300			*		pF
INPUT OFFSET VOLTAGE								
Initial Offset	T_A = +25°C		±100	±500		±50	±250	μV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6	±10		±3	±5	μV/°C
vs Supply Voltage	±5VDC ≤ | V_{CC} | ≤ ±20VDC		±10	±50		*	*	μV/V
vs Time			±10			*		μV/mo.
Adjustment Range	Circuit in "Connection Diagram"		±1			*		mV
INPUT BIAS CURRENT								
Initial Bias	T_A = +25°C		-12	-15		-6	-10	pA
vs Temperature			Note 4			*		
vs Supply Voltage			Note 5			*		

ELECTRICAL (CONT)

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT DIFFERENCE CURRENT								
Initial Difference	T_A = +25°C		±3	±6		±1.5	±4	pA
vs Temperature			Note 4			*		
vs Supply Voltage			Note 5			*		
INPUT IMPEDANCE								
Differential								
Resistance			10^{12}			*		Ω
Capacitance			1			*		pF
Common-mode								
Resistance			10^{13}			*		Ω
Capacitance			3			*		pF
INPUT VOLTAGE RANGE								
Common-mode Voltage Range	Linear Operation		±(| V_{CC} | -3)			*		V
Common-mode Rejection	f_O = DC, V_{CM} = ±10V	80	105		*	*		dB
POWER SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range	Derated Performance	±5		±20	*		*	VDC
Current, Quiescent			5.8	8		*	*	mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Operating	Derated Performance	-55		+125	*		*	°C
Storage		-65		+150	*		*	°C

NOTES: *Specifications same as for OPA101/102AM.
1. Parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
2. Minimum stable gain for the OPA102 is 3V/V.
3. Time required for output to return from saturation to linear operation following the removal of an input overdrive signal.
4. Doubles approximately every 8.5°C.
5. See Typical Performance Curves.

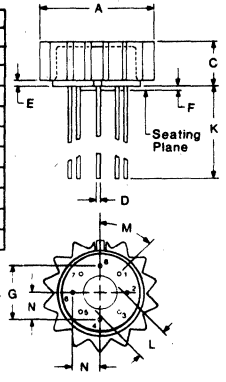
ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	750mW
Differential Input Voltage(2)	±20VDC
Input Voltage, Either Input(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration(3)	60 seconds
Junction Temperature	+175°C

NOTES:
1. Package must be derated according to the details in the Application Information section.
2. For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage.
3. Short-circuit may be to ground only. See discussion of Thermal Model in the Application Information section.

MECHANICAL SPECIFICATIONS

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.489	.522	12.42	13.26
C	.243	.307	6.17	7.80
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

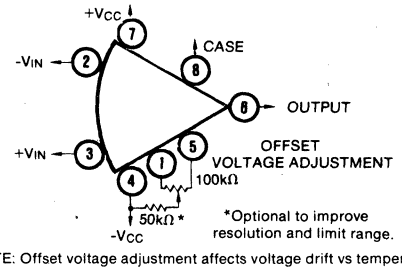


NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.
Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

Weight: 2 grams

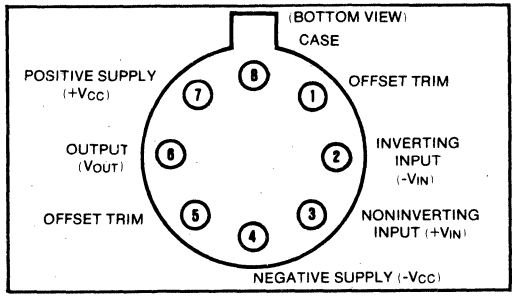
Order Number:
OPA101AM OPA101BM
OPA102AM OPA102BM

CONNECTION DIAGRAM



NOTE: Offset voltage adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted.

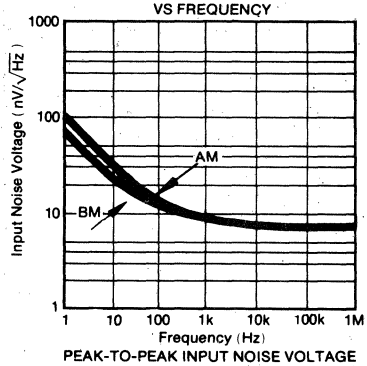
PIN CONFIGURATION



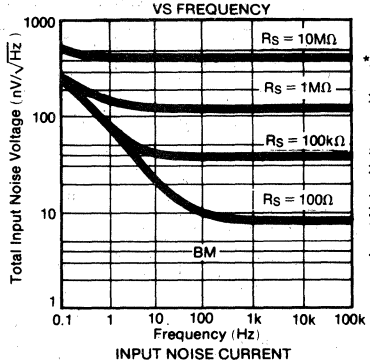
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = ±15VDC, unless otherwise noted. Performance curves apply to both OPA101 and OPA102 unless otherwise noted.)

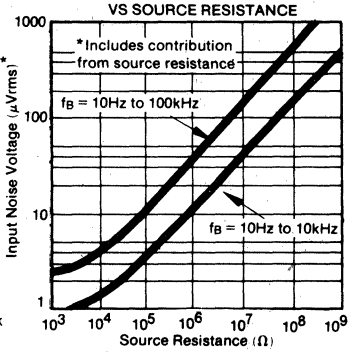
INPUT NOISE VOLTAGE VS FREQUENCY



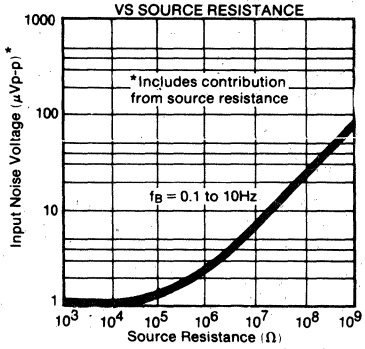
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



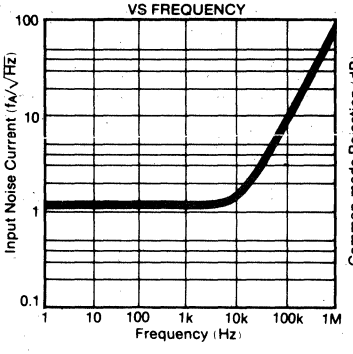
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



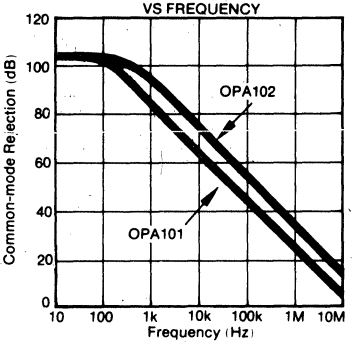
PEAK-TO-PEAK INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



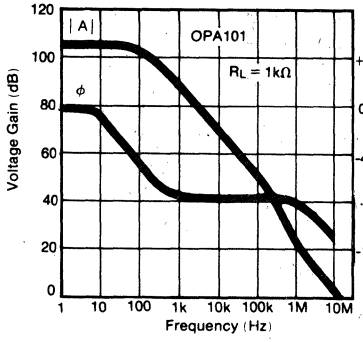
INPUT NOISE CURRENT VS FREQUENCY



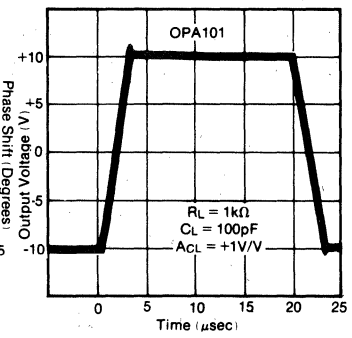
COMMON-MODE REJECTION VS FREQUENCY



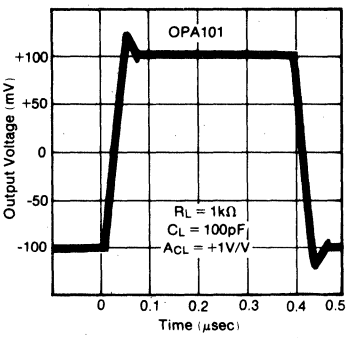
OPEN-LOOP FREQUENCY RESPONSE



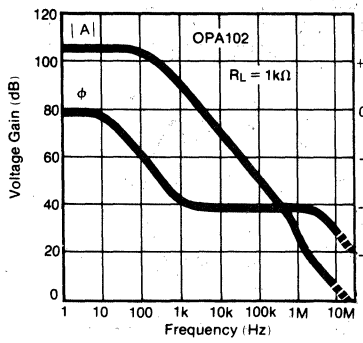
LARGE SIGNAL TRANSIENT RESPONSE



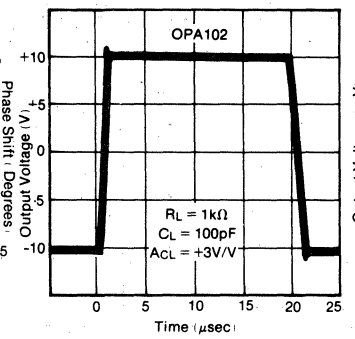
SMALL SIGNAL TRANSIENT RESPONSE



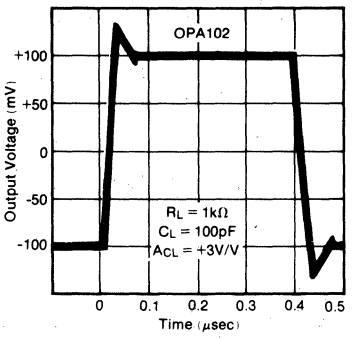
OPEN-LOOP FREQUENCY RESPONSE



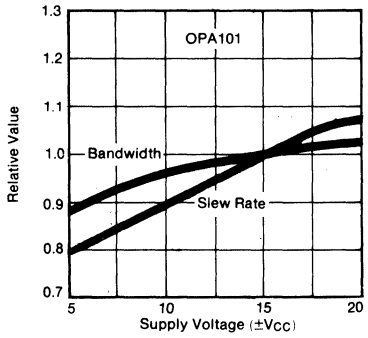
LARGE SIGNAL TRANSIENT RESPONSE



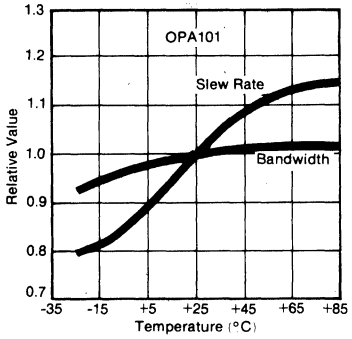
SMALL SIGNAL TRANSIENT RESPONSE



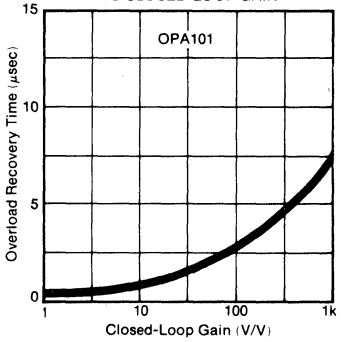
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



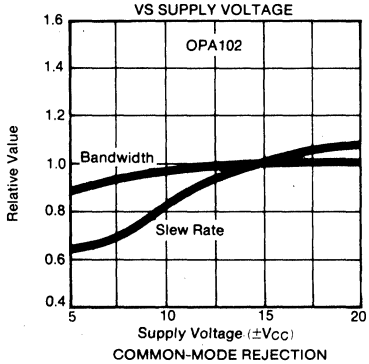
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



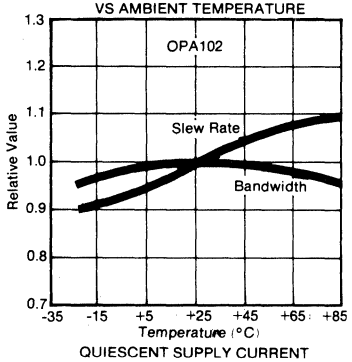
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



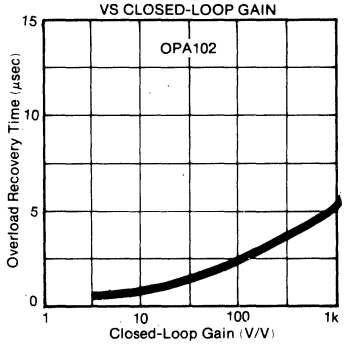
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



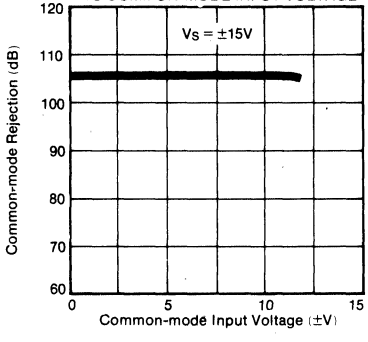
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



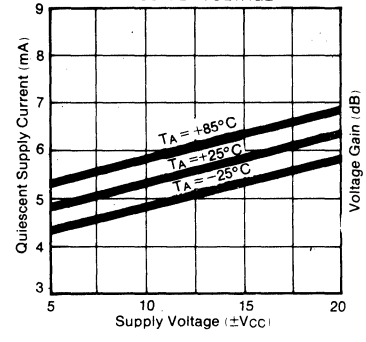
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



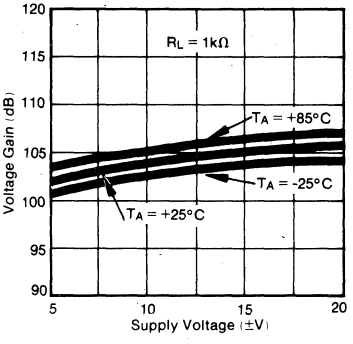
COMMON-MODE REJECTION VS COMMON-MODE INPUT VOLTAGE



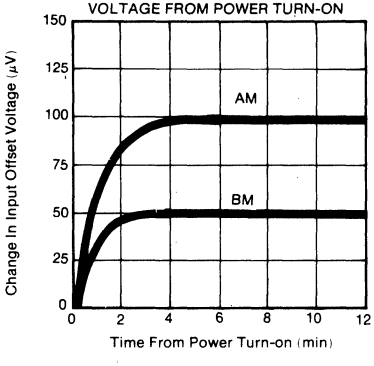
QUIESCENT SUPPLY CURRENT VS SUPPLY VOLTAGE



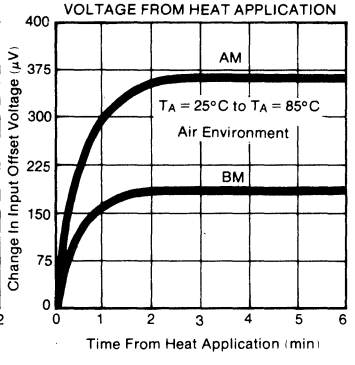
VOLTAGE GAIN VS SUPPLY VOLTAGE



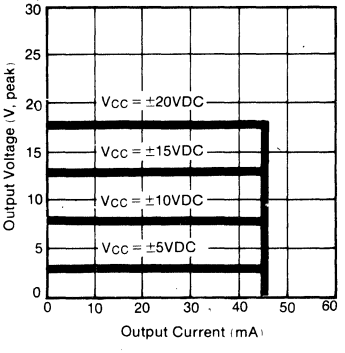
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



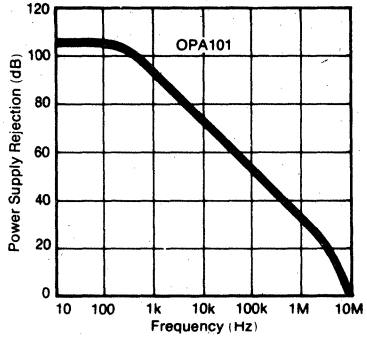
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



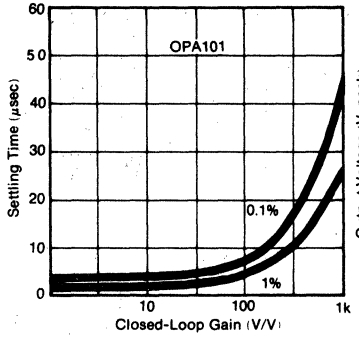
OUTPUT VOLTAGE VS OUTPUT CURRENT



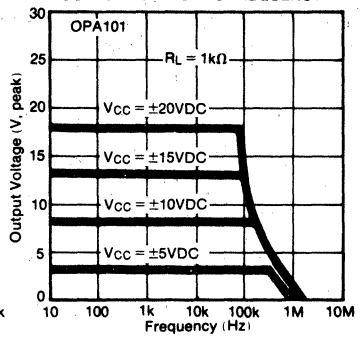
POWER SUPPLY REJECTION VS FREQUENCY



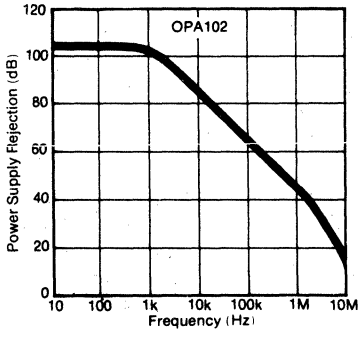
SETTLING TIME VS CLOSED-LOOP GAIN



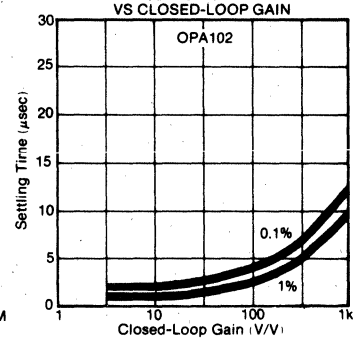
OUTPUT VOLTAGE VS FREQUENCY



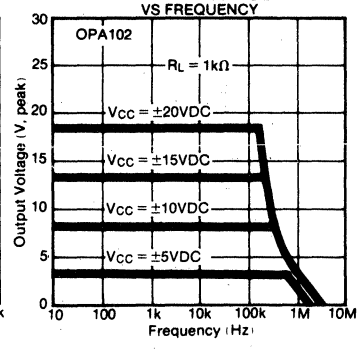
POWER SUPPLY REJECTION VS FREQUENCY



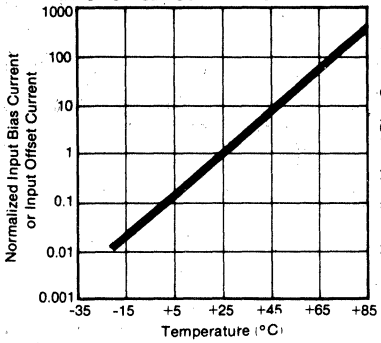
SETTLING TIME VS CLOSED-LOOP GAIN



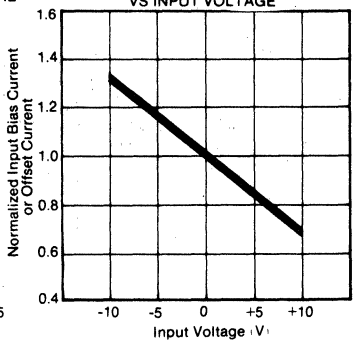
OUTPUT VOLTAGE VS FREQUENCY



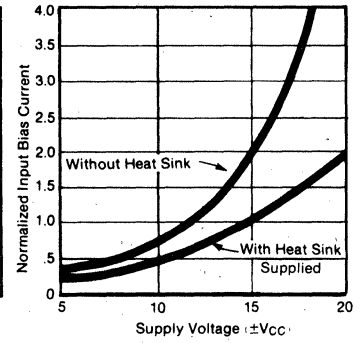
INPUT BIAS CURRENT VS TEMPERATURE AND INPUT OFFSET CURRENT VS TEMPERATURE



INPUT BIAS CURRENT VS INPUT VOLTAGE AND INPUT OFFSET CURRENT VS INPUT VOLTAGE



INPUT BIAS CURRENT VS SUPPLY VOLTAGE



APPLICATION INFORMATION

INTRODUCTION

The availability of detailed noise spectral density characteristics for the OPA101/102 amplifiers allows an accurate noise error analysis in a variety of different circuit configurations. The fact that the spectral characteristics are guaranteed maximums allows absolute noise errors to be truly bounded. Other FET amplifiers normally use simpler specifications of rms noise in a given bandwidth (typically 10Hz to 10kHz) and peak-to-peak noise (typically specified in the band 0.1Hz to 10Hz). These specifications do not contain enough information to allow accurate analysis of noise behavior in any but the simplest of circuit configurations.

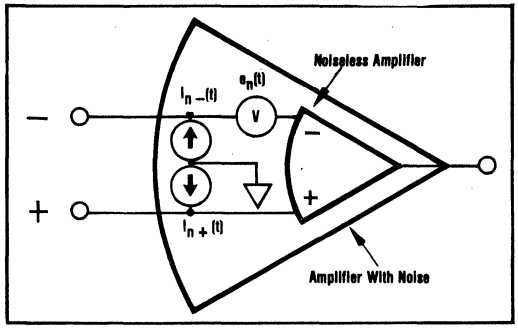


FIGURE 1. Noise Model of OPA101/102.

Noise in the OPA101/102 can be modeled as shown in Figure 1. This model is the same form as the DC model for offset voltage (E_{OS}) and bias currents (I_B). In fact, if the voltage $e_n(t)$ and currents $i_n(t)$ are thought of as general instantaneous error sources, then they could represent either noise or DC offsets. The error equations for the general instantaneous model are shown in Figure 2 below.

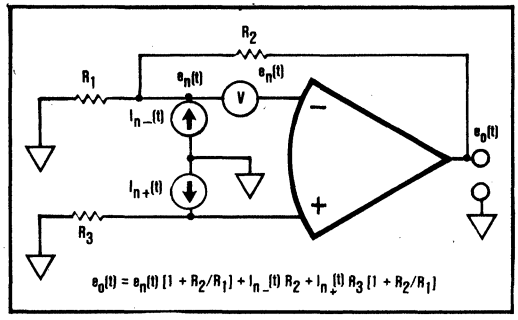


FIGURE 2. Circuit With Error Sources.

If the instantaneous terms represent DC errors (i.e., offset voltage and bias currents) the equation is a useful tool to compute actual errors. It is not, however, useful in the same direct way to compute noise errors. The basic problem is that noise cannot be predicted as a function of time. It is a random variable and must be described in probabilistic terms. It is normally described by some type of average - most commonly the rms value.

$$N_{rms} \triangleq \sqrt{1/T \int_0^T n^2(t)\, dt} \qquad (1)$$

where N_{rms} is the rms value of some random variable n(t). In the case of amplifier noise, n(t) represents either $e_n(t)$ or $i_n(t)$.

The internal noise sources in operational amplifiers are normally uncorrelated. That is, they are randomly related to each other in time and there is no systematic phase relationship. Uncorrelated noise quantities are combined as root-sum-squares. Thus, if $n_1(t)$, $n_2(t)$, and $n_3(t)$ are uncorrelated then their combined value is

$$N_{TOTAL_{rms}} = \sqrt{N_1^2{}_{rms} + N_2^2{}_{rms} + N_3^2{}_{rms}} \qquad (2)$$

The basic approach in noise error calculations then is to identify the noise sources, segment them into conveniently handled groups (in terms of the shape of their noise spectral densities), compute the rms value of each group, and then combine them by root-sum-squares to get the total noise.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. It will be used to demonstrate the above noise calculation method.

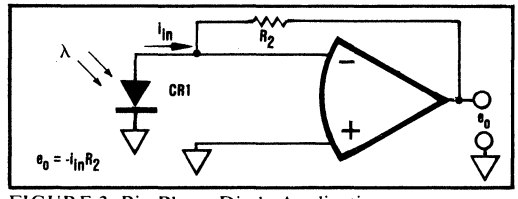


FIGURE 3. Pin Photo Diode Application.

CR1 is a PIN photo diode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{in} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 is what would be expected from stray capacitance with moderately careful layout (0.5pF to 2pF). A larger value of C_2 would normally be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

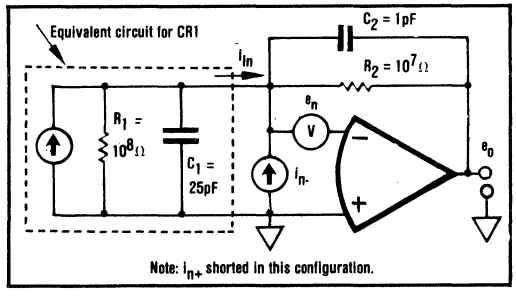


FIGURE 4. Noise Model of Photo Diode Application.

In Figure 4, e_n and i_n represent the amplifier's voltage and current spectral densities, $e_n(\omega)$ and $i_n(\omega)$ respectively. These are shown in Figure 5.

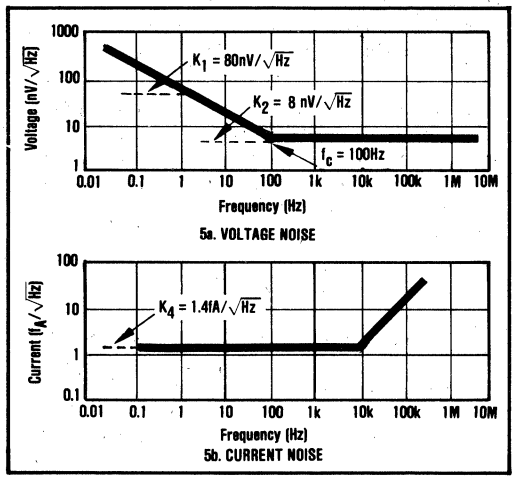


FIGURE 5. Noise Voltage and Current Spectral Density.

Figure 6 shows the desired "gain" of the circuit (transimpedance of $e_o/i_{in} = Z_2(s)$). It has a single-pole rolloff at $f_2 = 1/(2\pi R_2C_2) = \omega_2/2\pi$. Output noise is minimized if f_2 is made smaller. Normally R_2 is chosen for the desired DC transimpedance based on the full scale input current (i_{in} full scale) and maximum output (e_o max). Then C_2 is chosen to make f_2 as small as possible consistent with the necessary signal frequency response.

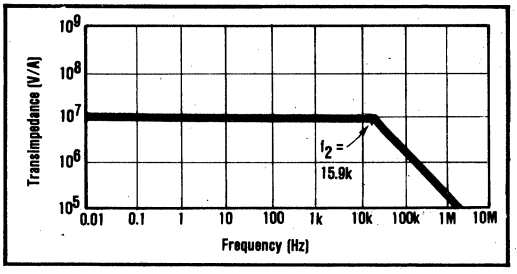


FIGURE 6. Transimpedance.

Voltage Noise

Figure 7 shows the noise voltage gain for the circuit in Figure 4. It is derived from the equation

$$e_o = e_n\left[\frac{A}{1+A\beta}\right] = e_n\,\frac{1}{\beta}\left[\frac{1}{1+\frac{1}{A\beta}}\right] \qquad (3)$$

where:

$A = A(\omega)$ is the open-loop gain

$\beta = \beta(\omega)$ is the feedback factor. It is the amount of output voltage feedback to the input of the op amp.

$A\beta = A(\omega)\,\beta(\omega)$ is the loop gain. It is the amount of the output voltage feedback to the input and then amplified and returned to the output.

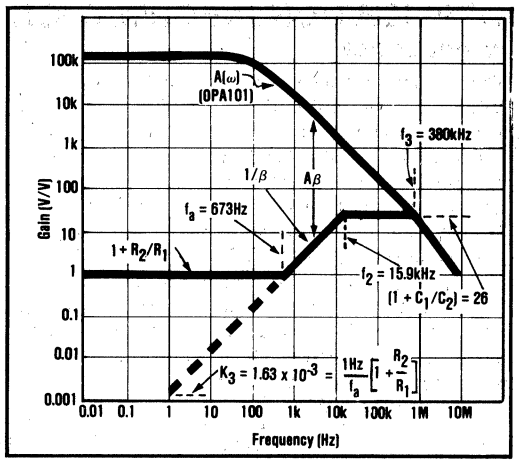


FIGURE 7. Noise Voltage Gain.

Note that for large loop gain ($A\beta >> 1$)

$$e_o \cong e_n\,\frac{1}{\beta} \qquad (4)$$

For the circuit in Figure 4 it can be shown that

$$\frac{1}{\beta} = 1 + \frac{R_2(R_1C_1s+1)}{R_1(R_2C_2s+1)} \qquad (5)$$

This may be rearranged to

$$\frac{1}{\beta} = \frac{R_2+R_1}{R_1}\left[\frac{\tau_a s+1}{\tau_2 s+1}\right] \qquad (5a)$$

where $\tau_a = (R_1 \parallel R_2)(C_1 \parallel C_2)$ (5b)

$$= \left[\frac{R_1R_2}{R_1+R_2}\right](C_1+C_2)$$

and $\tau_2 = R_2C_2$ (5c)

Then, $f_a = \dfrac{1}{2\pi\tau_a}$ and $f_2 = \dfrac{1}{2\pi\tau_2}$ (5d)

For very low frequencies ($f << f_a$), s approaches zero and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1} \qquad (6)$$

For very high frequencies ($f >> f_2$), s approaches infinity and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{C_1}{C_2} \qquad (7)$$

The noise voltage spectral density at the output is obtained by multiplying the amplifier's noise voltage spectral density (Figure 5a) times the circuits noise gain (Figure 7). Since both curves are plotted on log-log scales the multiplication can be performed by the addition of the two curves. The result is shown in Figure 8.

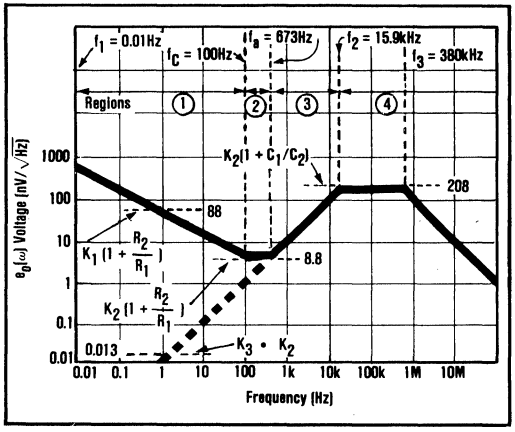


FIGURE 8. Output Noise Voltage Spectral Density.

The total rms noise at the amplifier's output due to the amplifier's internal voltage noise is derived from the $e_o(\omega)$ function in Figure 8 with the following expression:

$$E_{o\ rms} = \sqrt{\int_{-\infty}^{+\infty} e_o^2(\omega)\, d\omega} \qquad (8)$$

It is both convenient and informative to calculate the rms noise using a piecewise approach (region-by-region) for each of the four regions indicated in Figure 8.

Region 1; $f_l = 0.01Hz$ to $f_c = 100Hz$

$$E_{n1\ rms} = K_1 \left(1 + \frac{R_2}{R_1}\right) \sqrt{\ln(f_c/f_l)} \qquad (9)$$

$$= 80nV/\sqrt{Hz} \left(1 + \frac{10^7}{10^8}\right) \sqrt{\ln \frac{100}{0.01}} \qquad (9a)$$

$$= 2.67\mu V$$

This region has the characteristic of 1/f or "pink" noise (slope of -10dB per decade on the log-log plot of $e_n(\omega)$). The selection of 0.01Hz is somewhat arbitrary but it can be shown that for this example there would be only negligible additional contribution by extending f_l several decades lower. Note that $K_1(1 + R_2/R_1)$ is the value of e_o at f = 1Hz.

Region 2; $f_c = 100Hz$ to $f_a = 673Hz$

$$E_{n2\ rms} = K_2 \left(1 + \frac{R_2}{R_1}\right) \sqrt{f_a - f_c} \qquad (10)$$

$$= 8nV/\sqrt{Hz} \left(1 + \frac{10^7}{10^8}\right) \sqrt{673 - 100} \qquad (10a)$$

$$= 0.21\mu V$$

This is a region of "white" noise which leads to the form of equation (10).

Region 3; $f_a = 673Hz$ to $f_2 = 15.9kHz$

$$E_{n3\ rms} = K_2 \cdot K_3 \sqrt{\frac{f_2^3}{3} - \frac{f_a^3}{3}} \qquad (11)$$

$$= 8nV/\sqrt{Hz} (1.63 \times 10^{-3}) \sqrt{\frac{(15.9k)^3}{3} - \frac{(673)^3}{3}} \qquad (11a)$$

$$= 15.1\mu V$$

This is the region of increasing noise gain (slope of +20dB/decade on the log-log plot) caused by the lead network formed by the resistance $R_1 || R_2$ and the capacitance $(C_1 + C_2)$. Note that $K_3 \cdot K_2$ is the value of the $e_o(\omega)$ function for this segment projected back to 1Hz.

Region 4; f > 15.9kHz

$$E_{n4\ rms} = K_2 \left(1 + \frac{C_1}{C_2}\right) \sqrt{\left[\frac{\pi}{2}\right] f_3 - f_2} \qquad (12)$$

$$= 8nV/\sqrt{Hz} \left(1 + \frac{25}{1}\right) \sqrt{\left[\frac{\pi}{2}\right] 380k - 15.9k} \qquad (12a)$$

$$= 158.5\mu V$$

This is a region of white noise with a single order rolloff at $f_3 = 380kHz$ caused by the intersection of the $1/\beta$ curve and the open-loop gain curve. The value of 380kHz is obtained from observing the intersection point of Figure 7. The $\pi/2$ applied to f_3 is to convert from a 3dB corner frequency to an effective noise bandwidth.

Current Noise

The output voltage component due to current noise is equal to:

$$E_{ni} = i_n \times Z_2(s) \qquad (13)$$

where $Z_2(s) = R_2 || X_{C_2}$ (13a)

This voltage may be obtained by combining the information from figures 5 (b) and 6 together with the open loop gain curve of Figure 7. The result is shown in Figure 9 below.

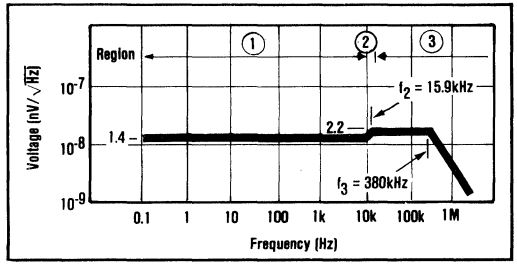


FIGURE 9. Output Voltage Due to Noise Current.

Using the same techniques that were used for the voltage noise:

Region 1; 0.1Hz to 10kHz

$$E_{ni1} = 1.4 \times 10^{-8} \sqrt{10k - 0.1} \quad (14)$$

$$= 1.4\mu V$$

Region 2; 10kHz to 15.9kHz

$$E_{ni2} = 1.4 \times 10^{-12} \sqrt{\frac{(15.9k)^3}{3} - \frac{(10k)^3}{3}} \quad (14a)$$

$$= 1.4\mu V$$

Region 3; f > 15.9kHz

$$E_{ni3} = 2.2 \times 10^{-8} \sqrt{\frac{\pi}{2} 380k - 15.9k} \quad (14b)$$

$$= 16.8\mu V$$

$$E_{ni\ total} = 10^{-6} \sqrt{(1.4)^2 + (1.4)^2 + (16.8)^2} \quad (14c)$$

$$= 16.9\mu V_{rms}$$

Resistor Noise

For a complete noise analysis of the circuit in Figure 4, the noise of the feedback resistor, R_2, must also be included. The thermal noise of the resistor is given by:

$$E_{R\ rms} = \sqrt{4kTRB} \quad (15)$$

K = Boltzmann's constant = 1.38×10^{-23} Joules/°Kelvin
T = Absolute temperature (degrees Kelvin)
R = Resistance (ohms)
B = Effective noise bandwidth (Hz) (ideal filter assumed)

At 25°C this becomes

E_R rms $\cong 0.13 \sqrt{RB}$
E_R rms in μV
R in MΩ
B in Hz

For the circuit in Figure 4

$R_2 = 10^7\Omega = 10M\Omega$

$$B = \frac{\pi}{2}(f_2) = \frac{\pi}{2} 15.9k$$

Then

$$E_R\ rms = (411nV/\sqrt{Hz}) \sqrt{B}$$

$$= (411nV/\sqrt{Hz}) \sqrt{\frac{\pi}{2} 15.9kHz}$$

$$= 64.9\mu V\ rms$$

Total Noise

The total noise may now be computed from

$$E_{n\ total} = \sqrt{E_{n1}^2 + E_{n2}^2 + E_{n3}^2 + E_{n4}^2 + E_{nR}^2 + E_{ni}^2} \quad (16)$$

$$= \sqrt{2.67^2 + 0.21^2 + 15.1^2 + 158.5^2 + 64.9^2 + 16.9^2} \quad (16a)$$

$$= \sqrt{7.1 + 0.04 + 228 + 25122 + 4212 + 286} \quad (16b)$$

$$= 173\mu V\ rms$$

Conclusions

Examination of the results in equation (16b) together with the curves in Figure 8 leads to some interesting conclusions. In this example 84% of the noise comes from E_{n4}. From Figure 8 it is seen that this is the area beyond the pole formed by R_2 and C_2.

The E_{n4} contribution could be reduced several ways. The most common method is to increase C_2. This reduces f_2 and the value of K2(1 + C1/C2) (see Figure 8). It also reduces the signal bandwidth (see Figure 6) and the final value of C_2 is normally a compromise between noise gain and necessary signal bandwidth.

It should be noted that increasing C_2 will also affect f_a since f_a is determined by $(C_1 + C_2)$ (see equation (5b)). Normally C_2 is larger than C_1 and f_2 will change more than f_a for a given change in C_2.

The other means of reducing the noise in region 4 involves changing amplifier parameters. For example, the use of a slower amplifier would move the open-loop gain curve to the left and decrease f_3. Of course, reducing the value of K_2, the noise floor, would also reduce the noise in this region.

The second largest component is the resistor noise E_{nR} (14% of the total noise). A lower resistor value decreases resistor noise as a function of $\sqrt{R}$, but it also lowers the desired signal gain as a direct function of R. Thus, lowering R reduces the signal-to-noise ratio at the output which shows that the feedback resistor should be as large as possible. The noise contribution due to R_2 can be decreased by raising the value of C_2 (lowering f_2) but this reduces signal bandwidth.

It is interesting to note that the current noise of the amplifier accounted for only 1% of the total E_n. This is different than would be expected when comparing the current and voltage spectral densities with the size of the feedback resistor. For example, if we define a characteristic value of resistance as

$$R_{characteristic} = \frac{e_n(\omega)}{i_n(\omega)} \text{ at } f = 10kHz \quad (17)$$

$$= \frac{8nV/\sqrt{Hz}}{1.4fA/\sqrt{Hz}}$$

$$= 5.7M\Omega$$

Thus, in simple transimpedance circuits with feedback resistors greater than the characteristic value, the amplifier's current noise would cause more output noise than the amplifier's voltage noise. Based on this and the 10MΩ feedback resistor in the example, the amplifier noise current would be expected to have a higher contribution than the noise voltage. The reason it does not in the example of Figure 4 is that the noise voltage has high gain at higher frequencies (Figure 7) and the noise current does not (Figure 6).

The fourth largest component of total noise comes from E_{n3} (0.8%). Decreasing C_1 will also lower the term $K_2(1 + C_1/C_2)$. In this case, f_2 will stay fixed and f_a will move to the right (i.e., the +20dB/decade slope segment will move

to the right). This can have a significant reduction on noise without lowering the signal bandwidth. This points out the importance of maintaining low capacitance at the amplifier's input in low noise applications.

Shielding and Guarding

The low noise, low bias current and high input impedance of the OPA101/102 are well suited to a number of precision applications. In order to fully benefit from the outstanding specifications of this unit, careful layout, shielding, and guarding are required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the OPA101/102.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the OPA101/102 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pickup.

Unless care is used, leakage currents across printed circuit boards can easily exceed the bias current of the OPA101/102. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the amplifier be wired to a Teflon standoff. If this is not done and instead the OPA101/102 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 10). The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents. In addition, noise pickup is also reduced.

Figures 11, 12, and 13 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two-part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.

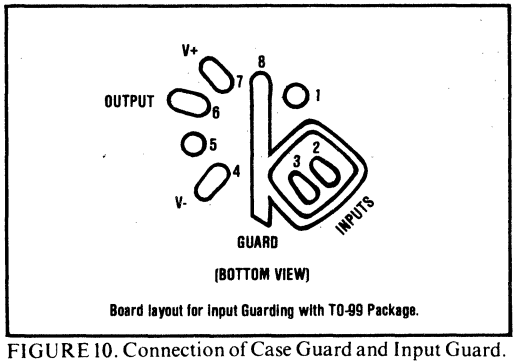


FIGURE 10. Connection of Case Guard and Input Guard.

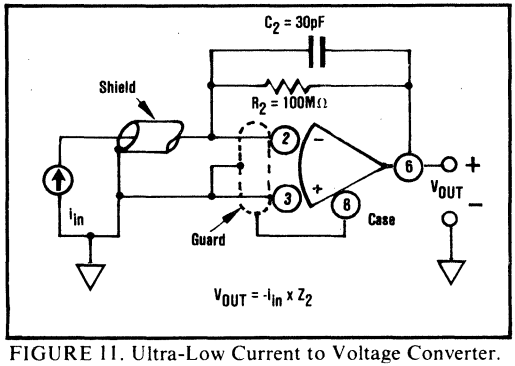


FIGURE 11. Ultra-Low Current to Voltage Converter.

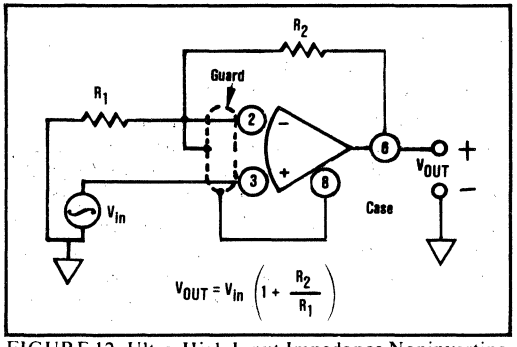


FIGURE 12. Ultra-High Input Impedance Noninverting Circuit.

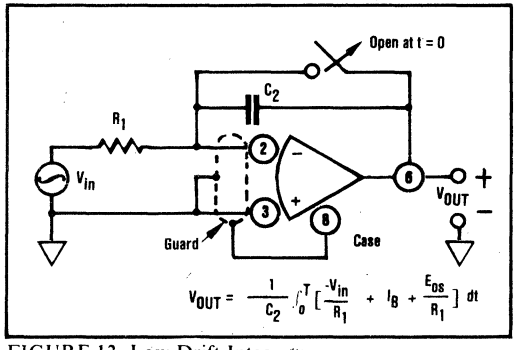


FIGURE 13. Low Drift Integrator.

Thermal Model

Figure 14 is the thermal model for the OPA101/102 where:

T_J = Junction temperature (output load)
T_J* = Junction temperature (no load)
T_C = Case temperature
T_A = Ambient temperature
θ_{CA} = Thermal resistance, case-to-ambient

θ_{HS} = Effective thermal resistance of the heat sink
P_{DQ} = Quiescent power dissipation
$= |+V_{CC}| I_{+QUIESCENT} + |-V_{CC}| I_{-QUIESCENT}$
P_{DX} = Power dissipation in the output transistor
$= (V_{OUT} - V_{CC}) I_{OUT}$
(In a complementary output stage only one output transistor is conducting current at a time.)

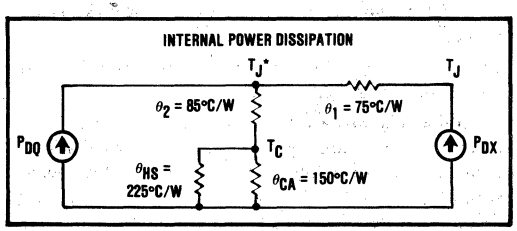


FIGURE 14. OPA101/102 Thermal Model

This model is obviously not the simple one-power source model used with most linear integrated circuits. It is, however, a more accurate model for multichip hybrid integrated circuits where the quiescent power is dissipated in the input stage and the internal power dissipation due to the load is dissipated in a somewhat physically separated output stage.

The model in Figure 14 must be used in conjunction with the OPA101/102's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem: Determine the output transistor junction temperature when the output has its maximum load resistance and is operated at the worst-case output voltage conditions. Assume $V_{CC} = \pm 15$VDC and $T_A = 25°C$.

Maximum P_{DX} occurs where $V_{OUT} = 1/2 V_{CC}$. Then

$$P_{DX\ max} = \frac{(V_{CC})^2}{4R_{load}} \qquad (18)$$

$$T_j = T_A + P_{DQ}[\theta_2 + (\theta_{HS} \parallel \theta_{CA})] + P_{DX}[\theta_1 + \theta_2 + (\theta_{HS} \parallel \theta_{CA})] \qquad (19)$$

where $(\theta_{HS} \parallel \theta_{CA}) = \frac{\theta_{HS}\theta_{CA}}{\theta_{HS} + \theta_{CA}} = 90°C/W$

Substituting appropriate values yields

$$T_j = 25° + (30V \times 8mA)[85°C/W + 90°C/W] + \frac{(15V)^2}{4 \times 1k\Omega}[75°C/W + 85°C/W + 90°C/W]$$

$$= 25°C + 42°C + 14°C = T_A + 56°C$$

$$= 81°C$$

The conclusion is that under a worst-case output voltage condition and with a 1kΩ load the junction temperature rise is 56°C above ambient. Thus, under these conditions, the device could be operated in an ambient up to 119°C without exceeding the 175°C junction temperature rating.

A similar analysis for conditions of the output short-circuited to ground where

$$P_{DX\ SS} = V_{CC}\ I_{(output\ limit)} \qquad (20)$$

shows that the maximum junction temperature rating of 175°C is exceeded. Thus, the output should not be shorted to ground for sustained periods of time.

HEAT SINK

The heat sink used on the OPA101/102 should not be removed. It has the effect of reducing the package thermal resistance from 150°C/W to about 90°C per watt. Removing the heat sink would naturally increase the junction temperature of the amplifier which would in turn raise the input bias current. The change in thermal resistance also affects the noise performance. Removing the heat sink would increase the noise in the 1 f region.

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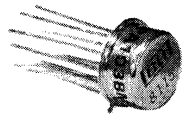


OPA103

Low Drift - Low Bias Current FET Input OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, 1pA, max
- HIGH INPUT IMPEDANCE, $10^{15}\Omega$
- ULTRA-LOW DRIFT, $2\mu V/°C$, max
- LOW OFFSET VOLTAGE, 0.25mV, max
- LOW QUIESCENT CURRENT, 1.5mA, max
- HERMETICALLY SEALED TO-99 PACKAGE

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS SUCH AS:
  - photo current detectors
  - pH electrodes
  - biological probes/transducers

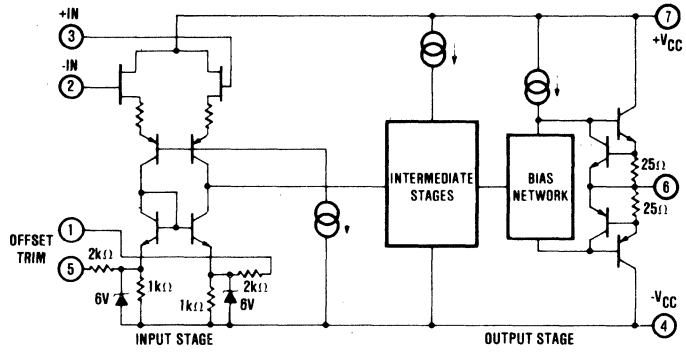
DESCRIPTION

The OPA103 is a precision low bias current operational amplifier. Guaranteed low initial offset voltage (0.25mV, max) and associated drift versus temperature ($2\mu V/°C$, max) is achieved by laser-adjusting the amplifier during manufacturing. This feature, and guaranteed low bias current (1pA, max), allow greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA103 include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA103 allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL	OPA103AM			OPA103BM			OPA103CM			OPA103DM			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OPEN-LOOP GAIN, DC, V_{OUT} + ±10V													
Rated Load, $R_L \geqslant 2k\Omega$	100	106		*	*		*	*		*	*		dB
$R_L \geqslant 10k\Omega$		112			*			*			*		dB
T_A = -25°C to +85°C, $R_L \geqslant 2k\Omega$	94	100		*	*		*	*		*	*		dB
RATED OUTPUT													
Voltage at R_L = 2kΩ, T_A = -25°C to +85°C	±10	±12		*	*		*	*		*	*		V
R_L = 10kΩ, T_A = -25°C to +85°C	±12	±13		*	*		*	*		*	*		V
Current, T_A = -25°C to +85°C; V_O = ±10V	±5	±10		*	*		*	*		*	*		mA
Output Impedance		3			*			*			*		kΩ
Load Capacitance(1)	500	1000		*	*		*	*		*	*		pF
Short Circuit Current	10	25		*	*		*	*		*	*		mA
FREQUENCY RESPONSE													
Unity Gain, Small Signal		1			*			*			*		MHz
Full Power Response	14	20		*	*		*	*		*	*		kHz
Slew Rate	0.9	1.3		*	*		*	*		*	*		V/µsec
Settling Time (0.1%)		9			*			*			*		µsec
Settling Time (0.01%)		20			*			*			*		µsec
Overload Recovery(2), 50% overdrive		4	15		*	*		*	*		*	*	µsec
INPUT OFFSET VOLTAGE													
Initial Offset, T_A = +25°C		±200	±500		±200	±500		±100	±250		±100	±250	µV
vs Temperature, T_A = -25°C to +85°C		±15	±25		±10	±15		±3	±5		±1	±2	µV/°C
vs Supply Voltage, T_A = -25°C to +85°C		±20	±200		*	*		*	*		*	*	µV/V
INPUT BIAS CURRENT(3)													
Initial Bias, T_A = +25°C						-1			-1			-1	pA
vs Supply Voltage		0.005			*			*			*		pA
INPUT DIFFERENCE CURRENT													
Initial Difference, T_A = +25°C		±0.3			±0.2			±0.2			±0.2		pA
INPUT IMPEDANCE													
Differential		10^{13}‖0.8			*			*			*		Ω ‖ pF
Common-mode		10^{15}‖1.6			*			*			*		Ω ‖ pF
INPUT NOISE													
Voltage, f_O = 10Hz		55			*			*			*		nV/√Hz
f_O = 100Hz		35			*			*			*		nV/√Hz
f_O = 1kHz		30			*			*			*		nV/√Hz
f_O = 10kHz		25			*			*			*		nV/√Hz
f_B = 0.1Hz to 10Hz		3.0			*			*			*		µV (p-p)
Current, f_B = 0.1Hz to 10Hz		0.01			*			*			*		pA (p-p)
f_B = 10Hz to 10kHz		0.003			*			*			*		pA, rms
f_O = 1kHz		0.6			*			*			*		fA/√Hz
INPUT VOLTAGE RANGE													
Differential	±20			*			*			*			V
Common-mode, T_A = -25°C to +85°C	±10	±12		*	*		*	*		*	*		V
Common-mode Rejection, V_{IN} = ±10V	76	86		*	*		*	*		*	*		dB
Maximum Safe Input Voltage		$\pm V_{CC}$			*			*			*		V
POWER SUPPLY													
Rated Voltage		±15			*			*			*		VDC
Voltage Range, derated performance	±5		±20	*		*	*		*	*		*	VDC
Current, quiescent T_A = -25°C to +85°C		1.0	1.5		*	*		*	*			*	mA
TEMPERATURE RANGE (ambient)													
Specification	-25		+85	*		*	*		*	*		*	°C
Operating	-55		+125	*		*	*		*	*		*	°C
Storage	-65		+150	*		*	*		*	*		*	°C
θ junction - ambient		235			*			*			*		°C/W

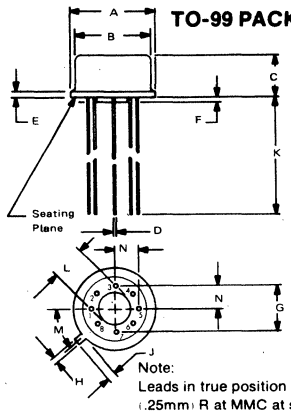
*Specifications same as for OPA103AM.

NOTES:

1. Stability guaranteed with load capacitance ≤ 500pF.
2. Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.
3. Bias current is tested and guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperature the bias current doubles every +10°C.

MECHANICAL

TO-99 PACKAGE

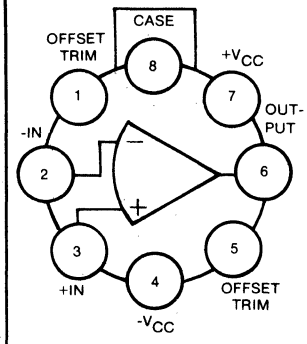


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Weight: 1 gram

Note:
Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

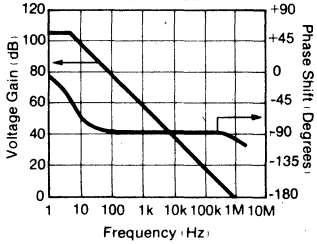
CONNECTION DIAGRAM



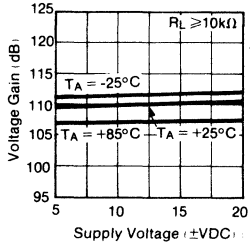
(TOP VIEW)

TYPICAL PERFORMANCE CURVES

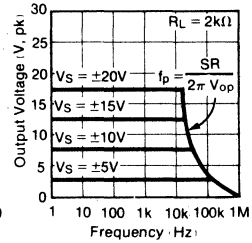
OPEN-LOOP FREQUENCY RESPONSE



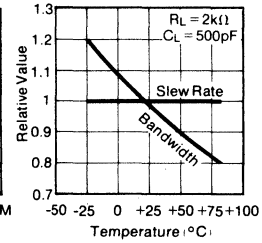
VOLTAGE GAIN



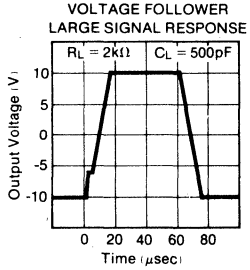
OUTPUT VOLTAGE vs FREQUENCY



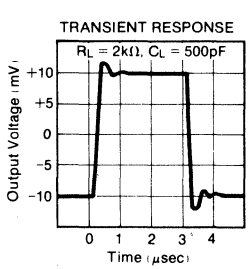
FREQUENCY CHARACTERISTICS



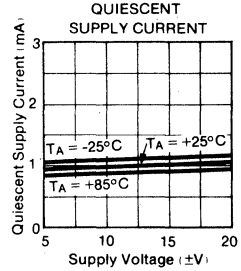
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



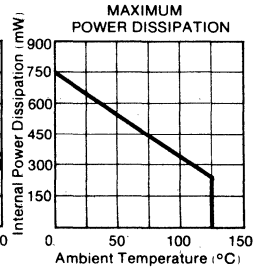
TRANSIENT RESPONSE



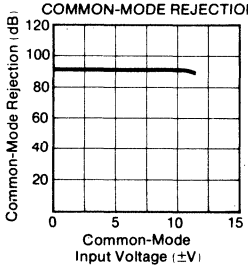
QUIESCENT SUPPLY CURRENT



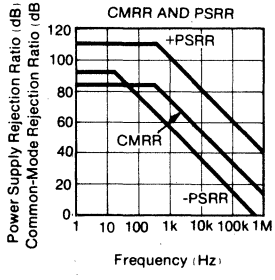
MAXIMUM POWER DISSIPATION



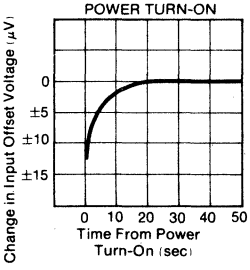
COMMON-MODE REJECTION



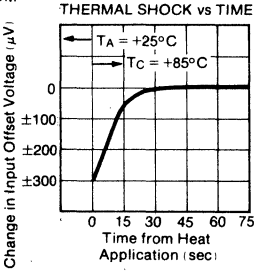
CMRR AND PSRR



STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



INPUT OFFSET VOLTAGE vs THERMAL SHOCK vs TIME



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the OPA103. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA103 is approximately 20 seconds (see Typical Performance Curves).

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the OPA103 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA103.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA103. To avoid leakage problems, it is recommended that the signal input lead of the OPA103 be wired to a Teflon standoff. If the OPA103 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard. The resistor R_3 shown in Figure 1 is optional. It may be used to compensate effects of very large source resistances. However, note that its use would also increase the noise due to the thermal noise of R_3.

OFFSET VOLTAGE ADJUSTMENT

Although the OPA103 has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 2 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C, for every 100μV of offset adjustment.

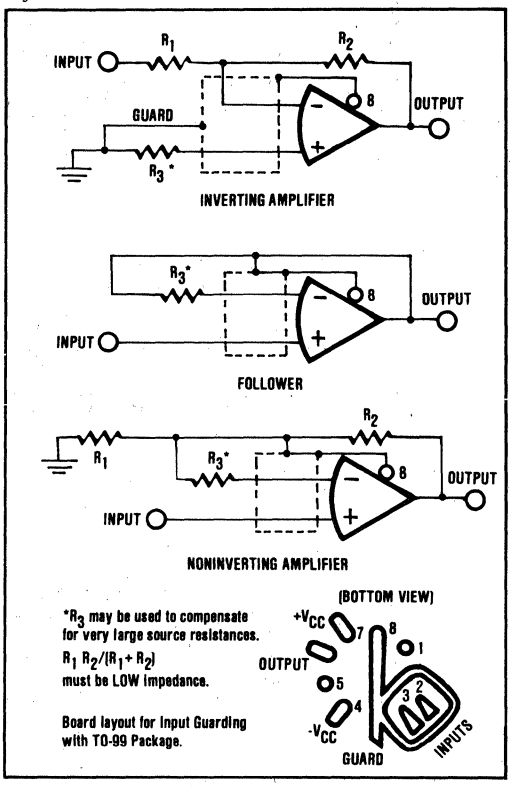


FIGURE 1. Connection of Input Guard.

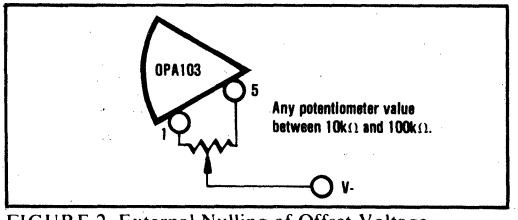
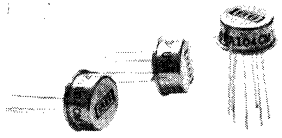


FIGURE 2. External Nulling of Offset Voltage.

BURR-BROWN®

OPA104



Ultra-Low Bias Current Low Drift FET Input OPERATIONAL AMPLIFIER

FEATURES

- SPECIFICATIONS GUARANTEED OVER TEMPERATURE
- ULTRA-LOW BIAS CURRRENT, 75fA, max
- HIGH INPUT IMPEDANCE, $10^{15}\Omega$
- LOW DRIFT, $10\mu V/°C$, max
- LOW OFFSET VOLTAGE, 0.5mV, max
- LOW QUIESCENT CURRENT, 1.5mA, max

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS SUCH AS:
  - photo current detectors
  - pH electrodes
  - biological probes/transducers

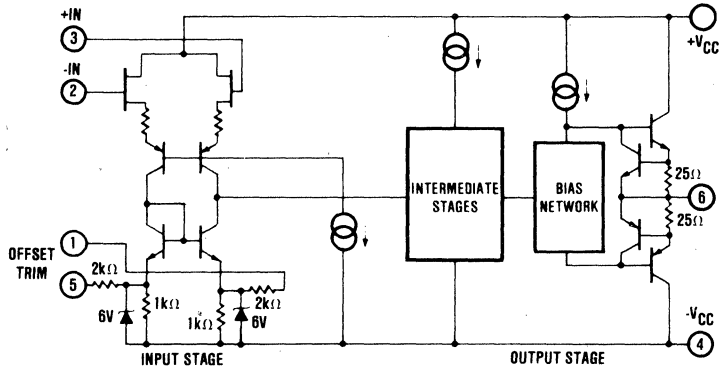
DESCRIPTION

The OPA104 is a precision low bias current operational amplifier. Guaranteed low initial offset voltage (0.5mV, max) and associated drift versus temperature ($10\mu V$ °C, max) is achieved by laser-adjusting the amplifier during manufacturing. The low offset, in addition to the guaranteed low bias current (75fA, max), allows greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA104 include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or ambient temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidently shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA104 allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±V_{CC} = ±15VDC unless otherwise noted.

MODEL	OPA104AM			OPA104BM			OPA104CM			
PARAMETERS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OPEN-LOOP GAIN, DC, V_{OUT} = ±10V										
Rated Load, $R_L \geq 2k\Omega$	100	106		*	*		*	*		dB
$R_L \geq 10k\Omega$	106	112		*	*		*	*		dB
T_A = -25°C to +85°C, $R_L \geq 2k\Omega$	92	100		*	*		*	*		dB
RATED OUTPUT										
Voltage at R_L = 2kΩ, T_A = -25°C to +85°C	±10	±12		*	*		*	*		V
R_L = 10kΩ, T_A = -25°C to +85°C	±12	±13		*	*		*	*		V
Current T_A = −25°C to +85°C, V_O = ±10V	±5	±10		*	*		*	*		mA
Output Impedance		3			*			*		kΩ
Load Capacitance(1)	500	1000		*	*		*	*		pF
Short Circuit Current	10	25		*	*		*	*		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			*			*		MHz
Full Power Response	25	35		*	*		*	*		kHz
Slew Rate	1.6	2.2		*	*		*	*		V/µsec
Settling Time (0.1%), A_V = -1, V_O = 0 to ±10V		6			*			*		µsec
Settling Time (0.01%), A_V = -1, V_O = 0 to ±10V		18			*			*		µsec
Overload Recovery(2), 50% overdrive		4	15		*	*		*	*	µsec
INPUT OFFSET VOLTAGE										
Initial Offset, T_A = +25°C		±200	±1000		±200	±500		±200	±500	µV
vs Temperature, T_A = -25°C to +85°C		±15	±25		±10	±15		±5	±10	µV/°C
vs Supply Voltage, T_A = +25°C		±10	±100		*	*		*	*	µV/V
vs Supply Voltage, T_A = -25°C to +85°C		±20	±150		*	*		*	*	µV/V
INPUT BIAS CURRENT(3)										
Initial Bias, T_A = +25°C			-300			-150			-75	fA
vs Supply Voltage		1				*			*	fA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, T_A = +25°C		±80			±80			±40		fA
INPUT IMPEDANCE										
Differential		10^{14} ‖ 0.5			*			*		Ω ‖ pF
Common-mode		10^{15} 1.0			*			*		Ω ‖ pF
INPUT NOISE										
Voltage, f_O = 10Hz		75			*			*		nV/√Hz
f_O = 100Hz		55			*			*		nV/√Hz
f_O = 1kHz		35			*			*		nV/√Hz
f_O = 10kHz		35			*			*		nV/√Hz
f_B = 0.1Hz to 10Hz		6			*			*		µV, p-p
Current, f_B = 0.1Hz to 10Hz		3			*			*		fA, p-p
f_B = 10Hz to 10kHz		10			*			*		fA, rms
f_O = 1kHz		0.25			*			*		fA/√Hz
INPUT VOLTAGE RANGE										
Differential	±20			*			*			V
Common-mode, T_A = -25°C to +85°C	±10	±12		*	*		*	*		V
Common-mode Rejection at V_{IN} = ±10V	66	76		*	*		80	90		dB
Maximum Safe Input Voltage		±V_{CC}			*			*		V
POWER SUPPLY										
Rated Voltage		±15			*			*		VDC
Voltage Range, derated performance	±5		±20	*		*	*		*	VDC
Current, quiescent T_A = -25°C to +85°C		1.0	1.5		*	*		*	*	mA
TEMPERATURE RANGE (ambient)										
Specification	-25		+85	*		*	*		*	°C
Operating	-55		+125	*		*	*		*	°C
Storage	-65		+150	*		*	*		*	°C
θ junction - ambient		235			*			*		°C/W

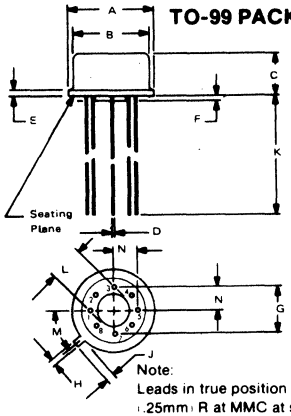
*Specifications same as for OPA104AM.

NOTES:

1. Stability guaranteed with load capacitance ≤ 500pF.
2. Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.
3. Bias current is tested and guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperature the bias current doubles approximately every +10°C.

MECHANICAL

TO-99 PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
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B	.305	.335	7.75	8.51
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D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
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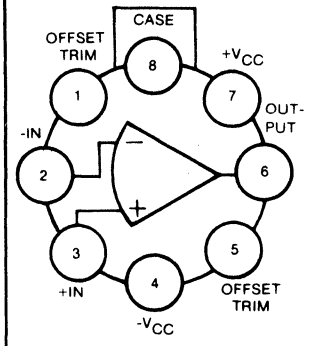
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Weight: 1 gram

Note:
Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.
Pin material and plating composition conform to Method 2003 solderability of MIL-STD-883 (except paragraph 3.2).

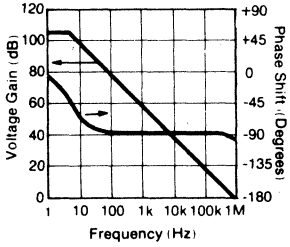
CONNECTION DIAGRAM



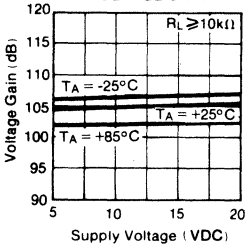
(TOP VIEW)

TYPICAL PERFORMANCE CURVES

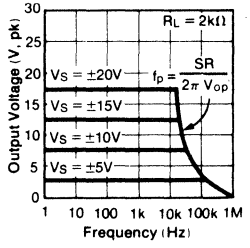
OPEN-LOOP FREQUENCY RESPONSE



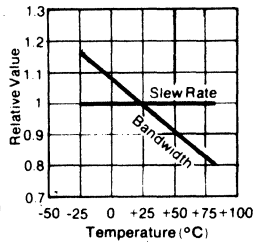
VOLTAGE GAIN



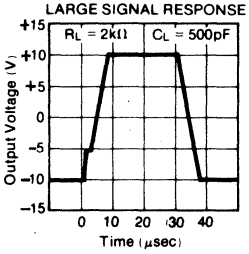
OUTPUT VOLTAGE vs FREQUENCY



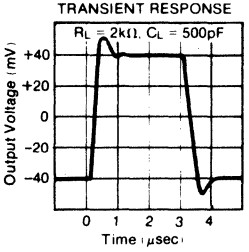
FREQUENCY CHARACTERISTICS



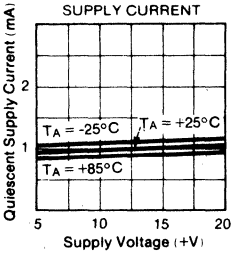
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



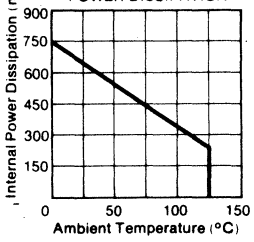
TRANSIENT RESPONSE



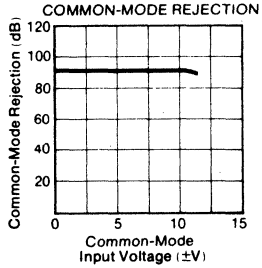
QUIESCENT SUPPLY CURRENT



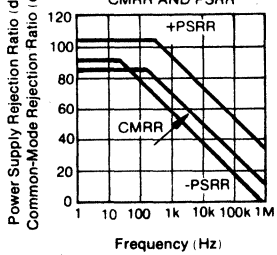
MAXIMUM POWER DISSIPATION



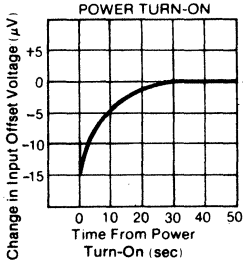
COMMON-MODE REJECTION



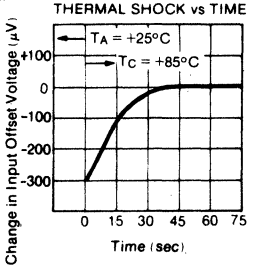
CMRR AND PSRR



STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



INPUT OFFSET VOLTAGE vs THERMAL SHOCK vs TIME



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the OPA104. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA104 is approximately 20 seconds (see Typical Performance Curves).

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the OPA104 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA104.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA104. To avoid leakage problems, it is recommended that the signal input lead of the OPA104 be wired to a Teflon standoff. If the OPA104 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard.

OFFSET VOLTAGE ADJUSTMENT

Although the OPA104 has a low initial offset voltage (500μV), some applications may require external nulling of this small offset. Figure 2 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C, for every 100μV of offset adjustment.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. Noise calculations are often important when using low current photodiodes.

CR1 is a PIN photodiode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{in} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 (0.5pF to 2pF) is what would be typically required to compensate for the pole generated by the capacitance at the input node. A larger value of C_2 could be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

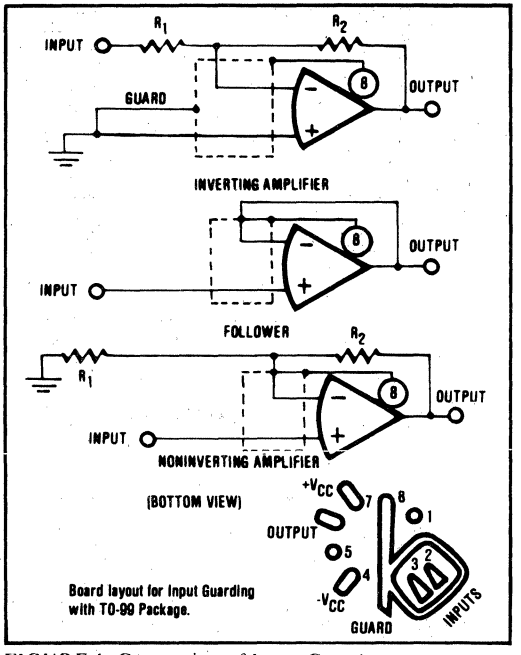


FIGURE 1. Connection of Input Guard.

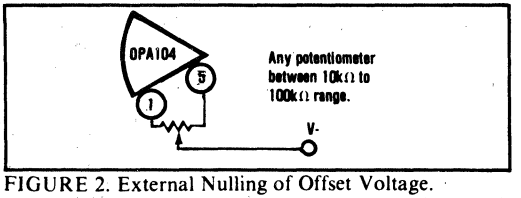


FIGURE 2. External Nulling of Offset Voltage.

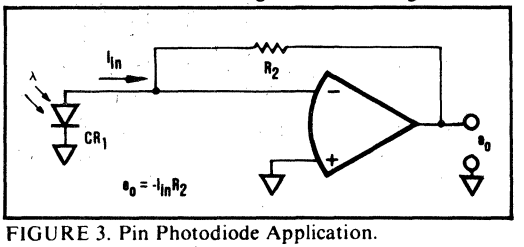


FIGURE 3. Pin Photodiode Application.

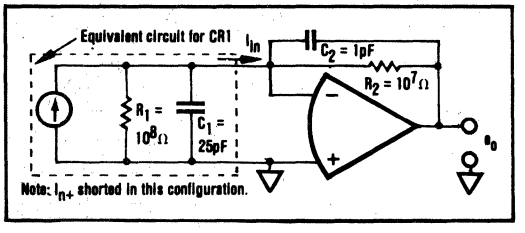
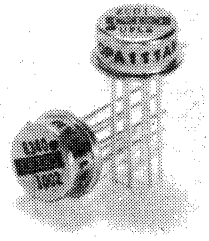


FIGURE 4. Model of Photodiode Application.

BURR-BROWN®



OPA111

Low Noise Precision *Difet*™ OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% tested, 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW BIAS CURRENT: 1pA max
- LOW OFFSET: 250μV max
- LOW DRIFT: 1μV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 100dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT—CAT SCANNER
- RADIATION HARD EQUIPMENT

DESCRIPTION

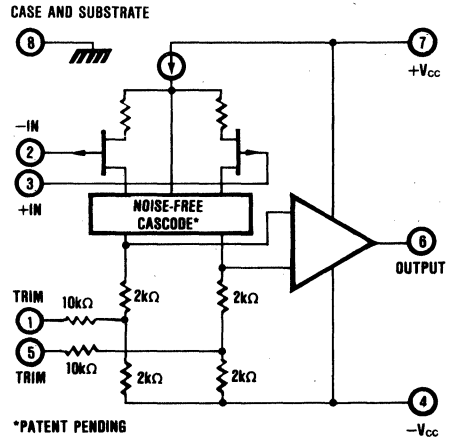
The OPA111 is a precision monolithic dielectrically-isolated FET (*Difet*™) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patent pending). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



OPA111 SIMPLIFIED CIRCUIT

BIFET® National Semiconductor Corp., *Difet*™ Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA111AM MIN	OPA111AM TYP	OPA111AM MAX	OPA111BM MIN	OPA111BM TYP	OPA111BM MAX	OPA111SM MIN	OPA111SM TYP	OPA111SM MAX	UNITS
INPUT											
NOISE											
Voltage, f_o = 10Hz	100% tested		40	80		30	60		40	80	nV/√Hz
f_o = 100Hz	100% tested		15	40		11	30		15	40	nV/√Hz
f_o = 1kHz	100% tested		8	15		7	12		8	15	nV/√Hz
f_o = 10kHz	100% tested		6	8		6	8		6	8	nV/√Hz
f_B = 10Hz to 10kHz	100% tested		0.7	1.2		0.6	1.0		0.7	1.2	µV, rms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3	µV, p-p
Current, f_B = 0.1Hz to 10Hz	(1)		9.5	15		7.5	12		9.5	15	fA, p-p
f_o = 0.1Hz thru 20kHz	(1)		0.5	0.8		0.4	0.6		0.5	0.8	fA/√Hz
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{cm} = 0VDC		±100	±500		±50	±250		±100	±500	µV
Average Drift	T_A = T_{MIN} to T_{MAX}		±2	±5		±0.5	±1		±2	±5	µV/°C
Supply Rejection		90	110		100	110		90	110		dB
			±3	±31		±3	±10		±3	±31	µV/V
BIAS CURRENT[2]											
Input Bias Current	V_{cm} = 0VDC		±0.8	±2		±0.5	±1		±0.8	±2	pA
OFFSET CURRENT[2]											
Input Offset Current	V_{cm} = 0VDC		±0.5	±1.5		±0.25	±0.75		±0.5	±1.5	pA
IMPEDANCE											
Differential			10^{13} || 1			10^{13} || 1			10^{13} || 1		Ω || pF
Common-Mode			10^{14} || 3			10^{14} || 3			10^{14} || 3		Ω || pF
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		100	110		90	110		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	114	125		120	125		114	125		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			2			2			2		MHz
Full Power Response	20V p-p, R_L = 2k	16	32		16	32		16	32		kHz
Slew Rate	V_o = ±10V, R_L = 2k	1	2		1	2		1	2		V/µsec
Settling Time, 0.1%	Gain = −1, R_L = 2k		6			6			6		µsec
0.01%	10V step		10			10			10		µsec
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5			5		µsec
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10	±11		±10	±11		±10	±11		V
Current Output	V_o = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_o = 0mADC		2.5	3.5		2.5	3.5		2.5	3.5	mA
TEMPERATURE RANGE											
Specification	Ambient temp.	−25		+85	−25		+85	−55		+125	°C
Operating	Ambient temp.	−55		+125	−55		+125	−55		+125	°C
Storage	Ambient temp	−65		+150	−65		+150	−65		+150	°C
θ Junction-Ambient			200			200			200		°C/W

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

ELECTRICAL [FULL TEMPERATURE RANGE SPECIFICATIONS]

At V_{CC} = ±15VDC and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA111AM			OPA111BM			OPA111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient temp.	−25		+85	−25		+85	−55		+125	°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{cm} = 0VDC		±220	±1000		±110	±500		±300	±1500	µV
Average Drift			±2	±5		±0.5	±1		±2	±5	µV/°C
Supply Rejection		86	100		90	100		86	100		dB
			±10	±50		±10	±32		±10	±50	µV/V
BIAS CURRENT[1]											
Input Bias Current	V_{cm} = 0VDC		±50	±250		±30	±130		±820	±4100	pA
OFFSET CURRENT[1]											
Input Offset Current	V_{cm} = 0VDC		±30	±200		±15	±100		±510	±3100	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 2kΩ	110	120		114	120		110	120		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10	±11		±10	±11		±10	±11		V
Current Output	V_o = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Short Circuit Current	V_o = 0VDC	10	40		10	40		10	40		mA
POWER SUPPLY											
Current, Quiescent	I_o = 0mADC		2.5	3.5		2.5	3.5		2.5	3.5	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES:
(1) Packages must be derated based on θ_{JC} = 150°C/W or θ_{JA} = 200°C/W.
(2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

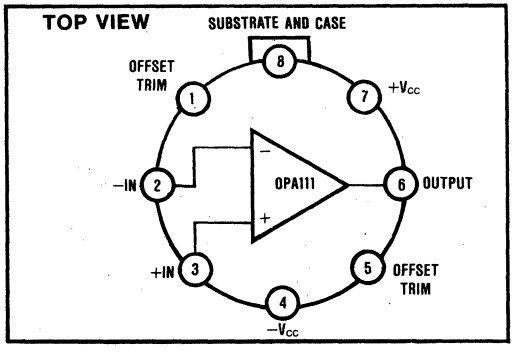
OPA111 X M

Basic model number

Performance grade
A, B = −25°C to +85°C
S = −55°C to +125°C

Package code
M = TO-99 metal can

CONNECTION DIAGRAM

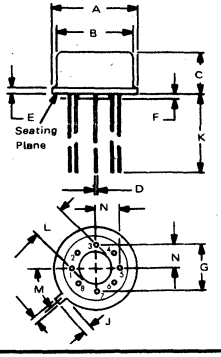


MECHANICAL "M" PACKAGE TO-99 (Hermetic)

NOTE:
Leads in true position within .010" (.25mmR) at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

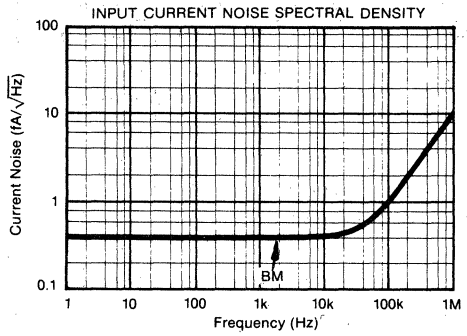


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

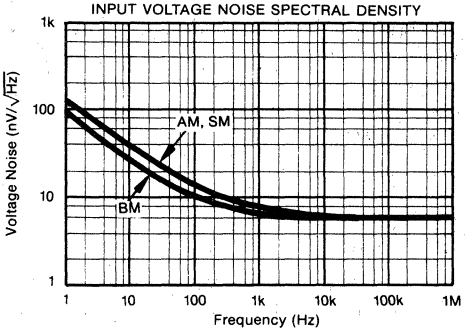
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

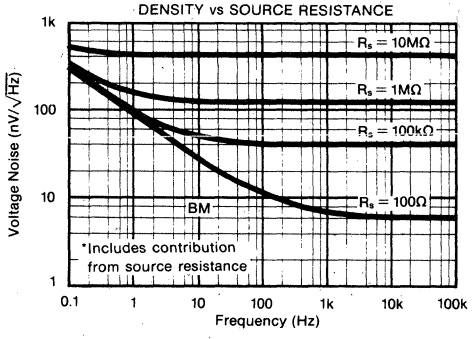
INPUT CURRENT NOISE SPECTRAL DENSITY



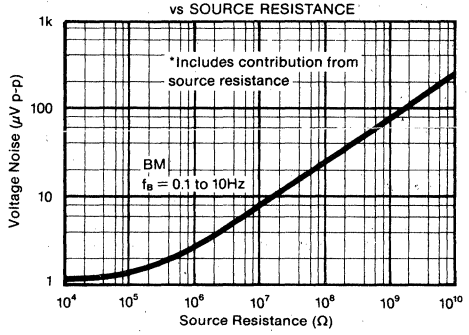
INPUT VOLTAGE NOISE SPECTRAL DENSITY



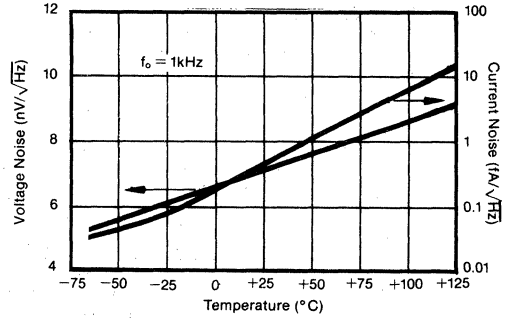
TOTAL* INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



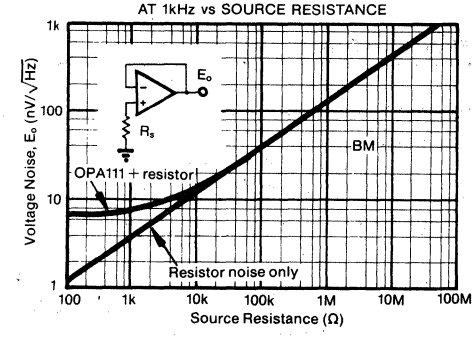
TOTAL* INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



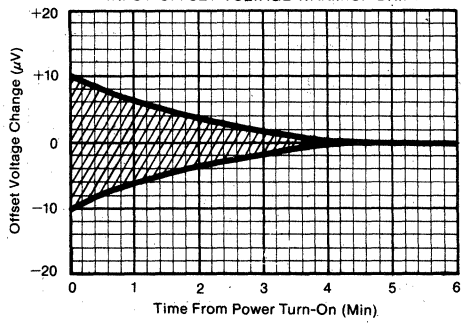
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



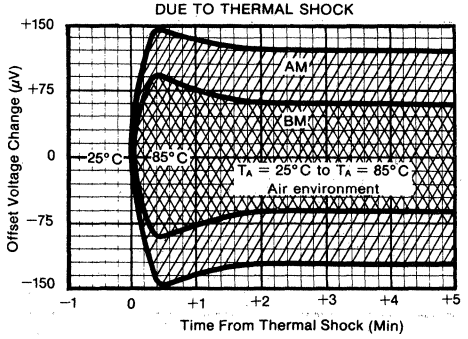
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



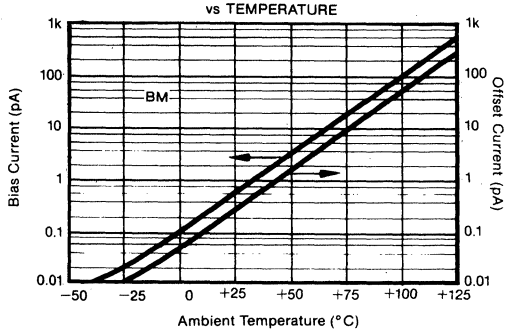
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



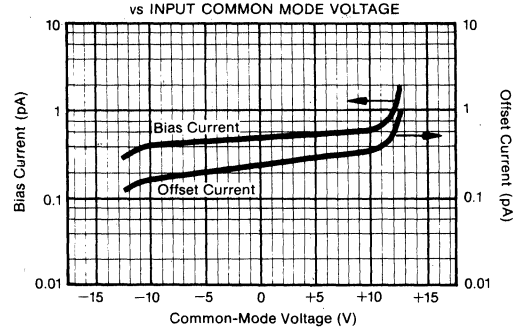
TYPICAL PERFORMANCE CURVES [CONT]

$T_A = +25°C$, $V_{CC} = \pm 15VDC$ unless otherwise noted.

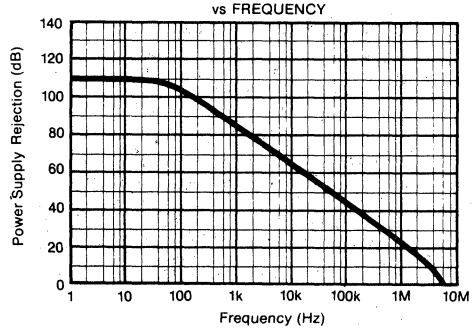
BIAS AND OFFSET CURRENT vs TEMPERATURE



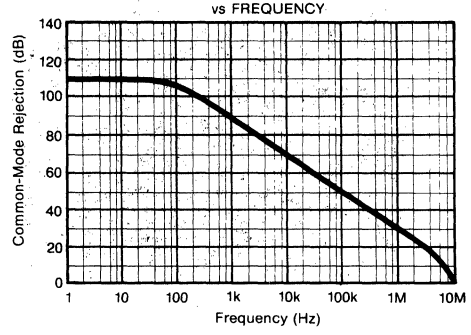
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



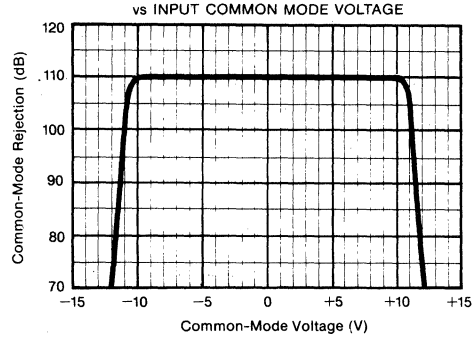
POWER SUPPLY REJECTION vs FREQUENCY



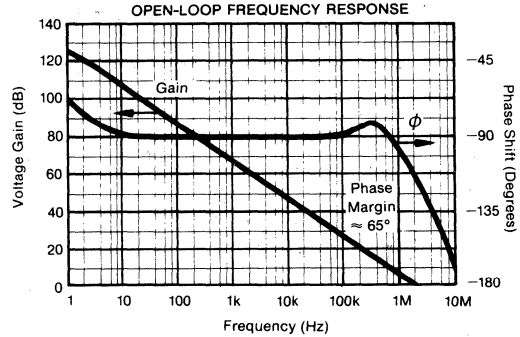
COMMON-MODE REJECTION vs FREQUENCY



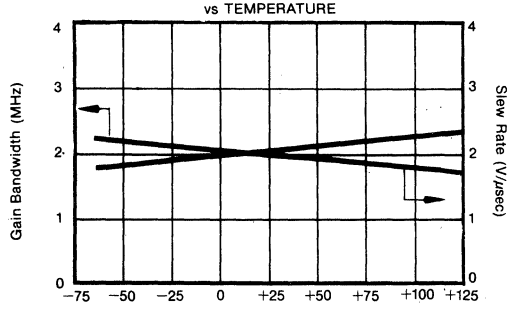
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



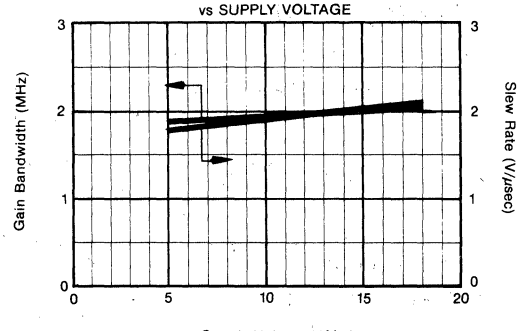
OPEN-LOOP FREQUENCY RESPONSE



GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



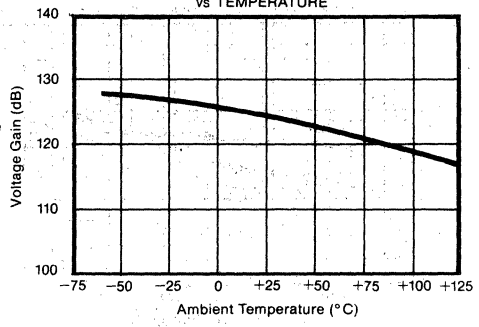
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



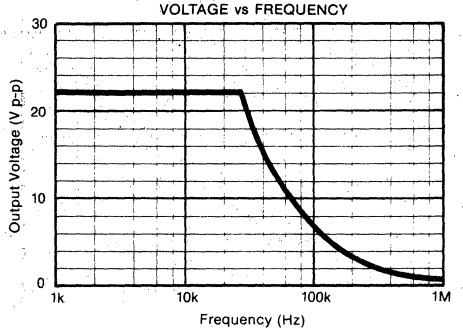
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

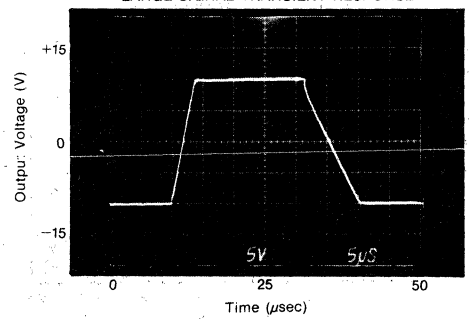
OPEN-LOOP GAIN vs TEMPERATURE



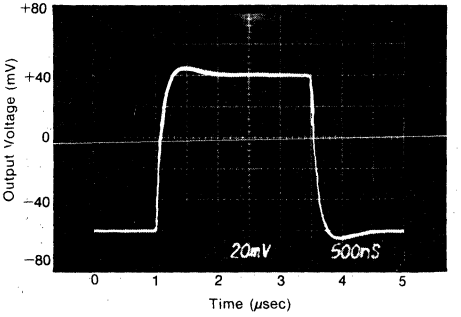
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



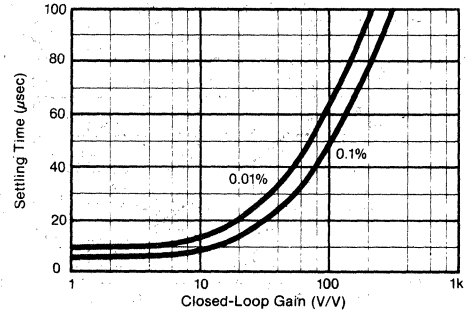
LARGE SIGNAL TRANSIENT RESPONSE



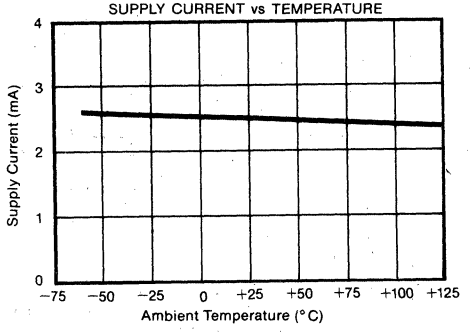
SMALL SIGNAL TRANSIENT RESPONSE



SETTLING TIME vs CLOSED-LOOP GAIN



SUPPLY CURRENT vs TEMPERATURE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA111 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3µV/°C for each 100µV of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA111 can replace most other amplifiers by leaving the external null circuit unconnected.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers

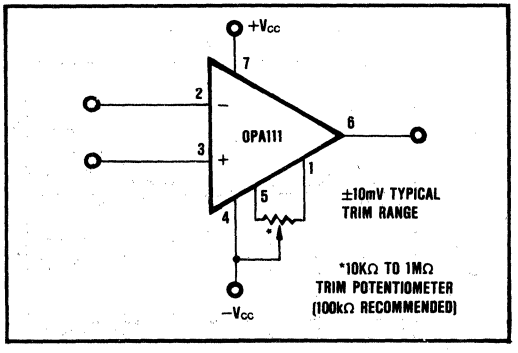


FIGURE 1. Offset Voltage Trim.

require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA111. Of course, the differential and common-mode voltage limits should be observed.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is rquired to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias curent of the OPA111. To avoid leakage problems, it is recommended that the signal input lead of the OPA111 be wired to a Teflon standoff. If the OPA111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

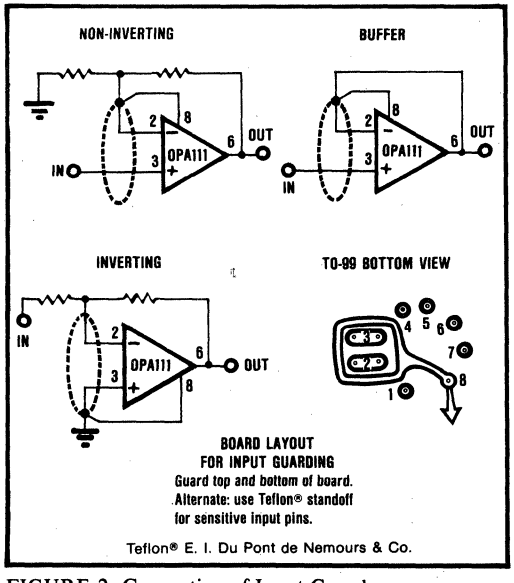


FIGURE 2. Connection of Input Guard.

NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the OPA111 will have lower total noise than an OP-27 (see Figure 3).

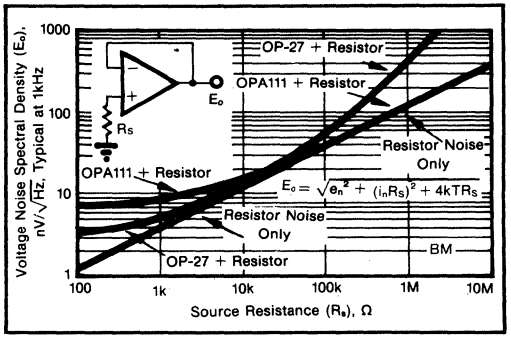


FIGURE 3. Voltage Noise Spectral Density Versus Source Resistance.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA111 is not compromised by common-mode voltage.

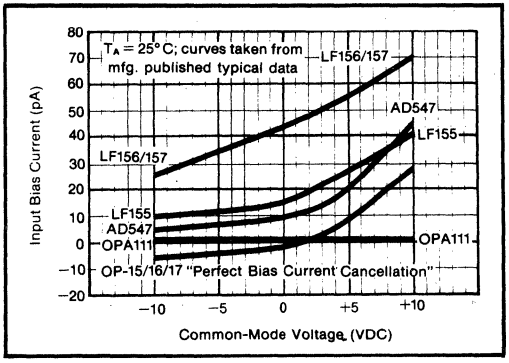


FIGURE 4. Input Bias Current Versus Common-Mode Voltage.

APPLICATIONS CIRCUITS

Figures 5 through 15 are circuit diagrams of various applications for the OPA111.

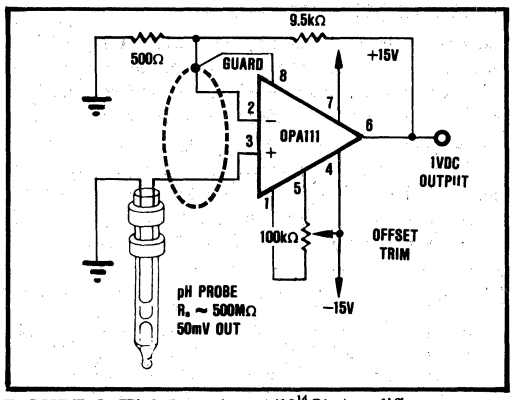


FIGURE 5. High Impedance ($10^{14}\Omega$) Amplifier.

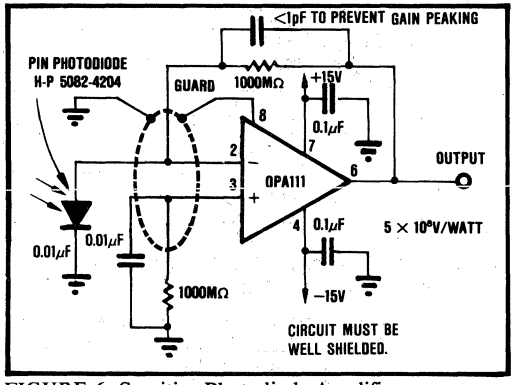


FIGURE 6. Sensitive Photodiode Amplifier.

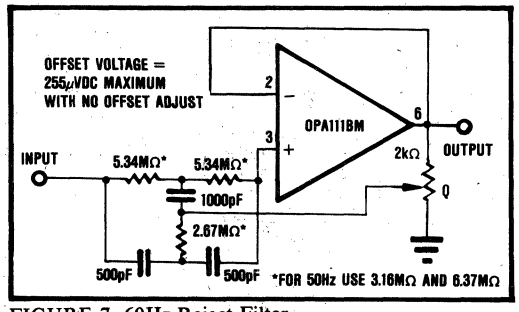


FIGURE 7. 60Hz Reject Filter.

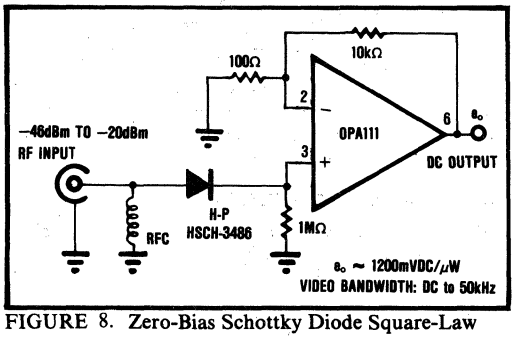


FIGURE 8. Zero-Bias Schottky Diode Square-Law RF Detector.

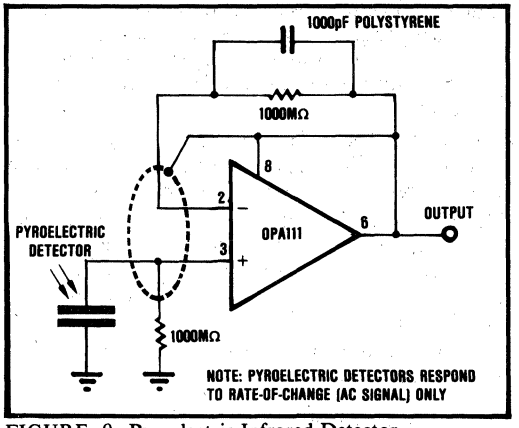


FIGURE 9. Pyroelectric Infrared Detector.

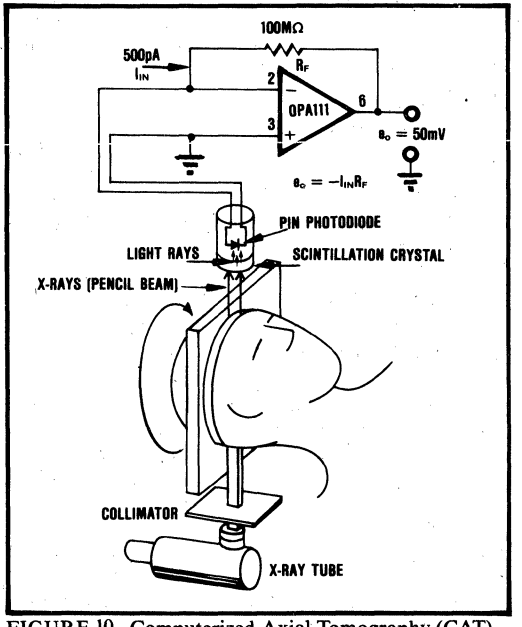


FIGURE 10. Computerized Axial Tomography (CAT) Scanner Channel Amplifier.

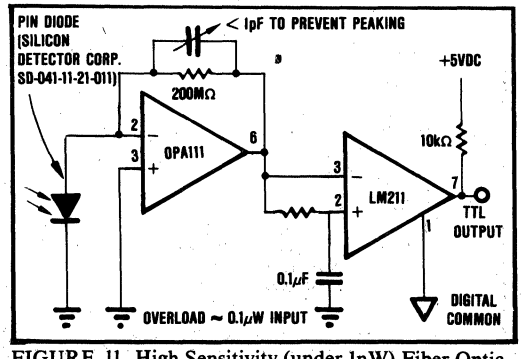


FIGURE 11. High Sensitivity (under 1nW) Fiber Optic Receiver for 9600 Baud Manchester Data.

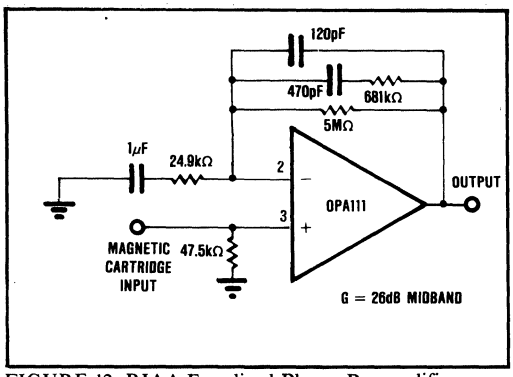


FIGURE 12. RIAA Equalized Phono Preamplifier.

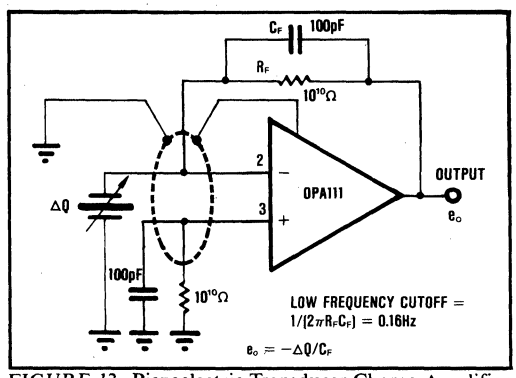


FIGURE 13. Piezoelectric Transducer Charge Amplifier.

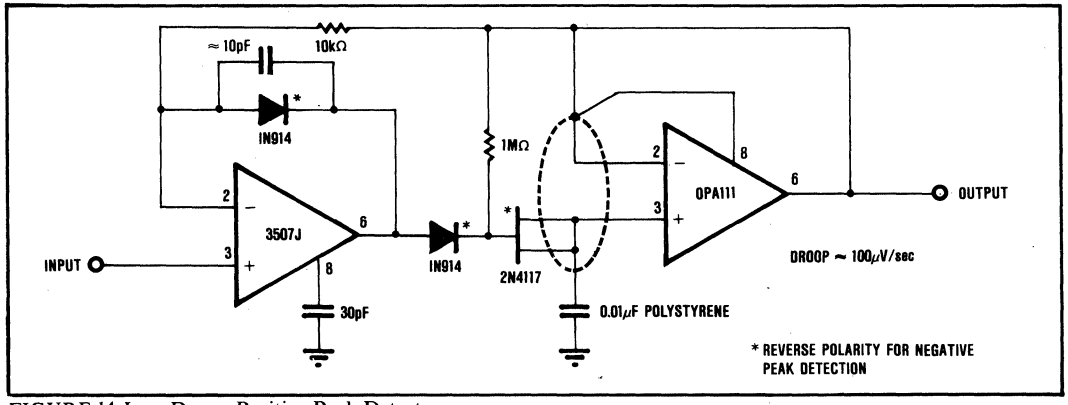


FIGURE 14. Low-Droop Positive Peak Detector.

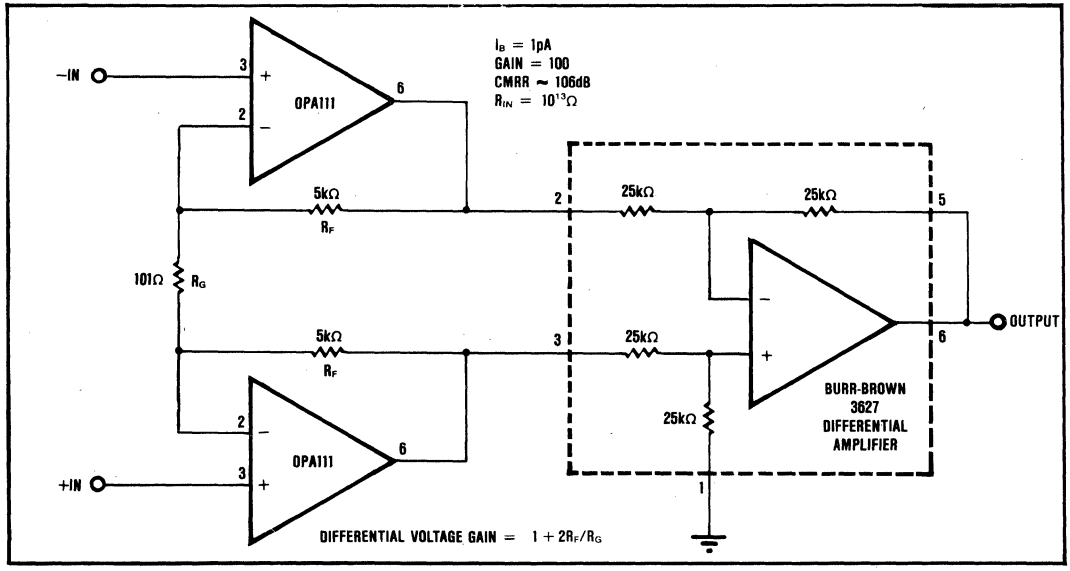


FIGURE 15. FET Input Instrumentation Amplifier.

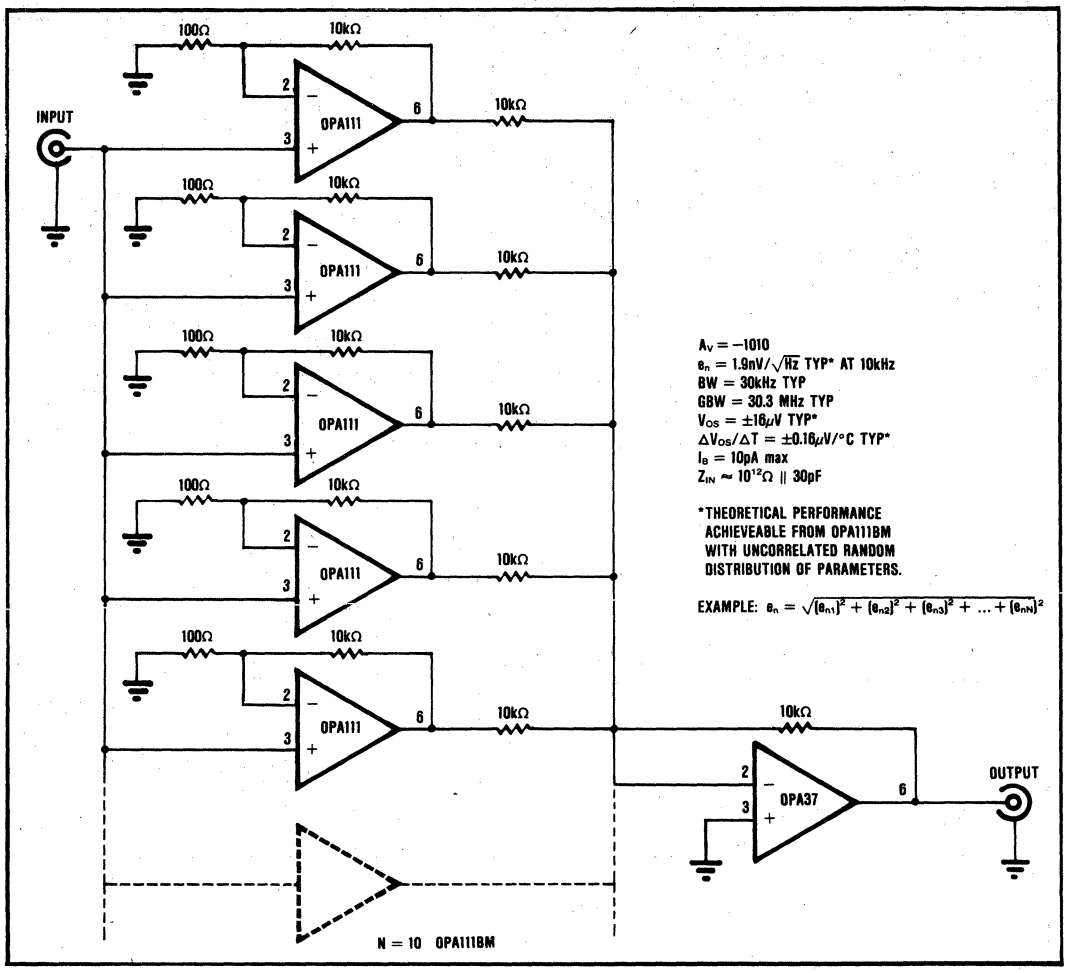


FIGURE 16. 'N' Stage Parallel-Input Amplifier.

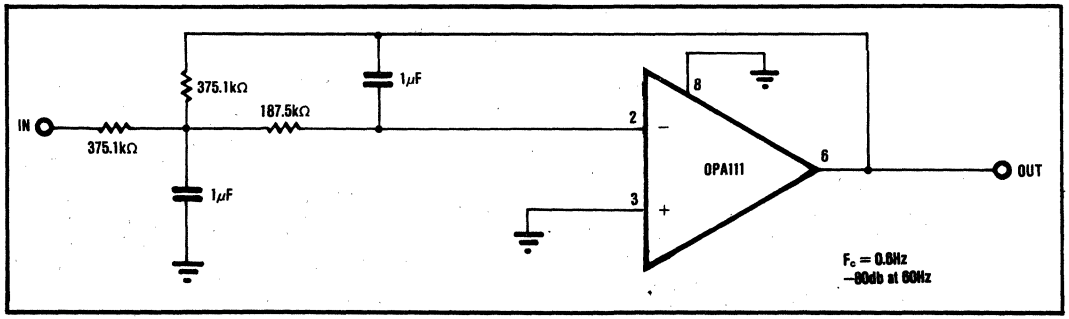


FIGURE 17. 0.6Hz Second Order Low-Pass Filter.

BURR-BROWN®

OPA201

PAT. PEND.

Switchable-Input Operational Amplifier SWOP AMP™

FEATURES

- TWO PRECISION INPUT STAGES SELECTABLE WITH CONTROL SIGNAL
- EXCELLENT INPUT SPECIFICATIONS
  - V_{OS} 100μV max (C Grade)
  - $\Delta V_{OS}/\Delta T$ 1μV/°C max (C Grade)
  - I_B 25nA max (C Grade)
- LOW POWER
  - $\pm V_{CC}$ 2.5V to 18V
  - I_Q 500μA max
- EASY TO USE

APPLICATIONS

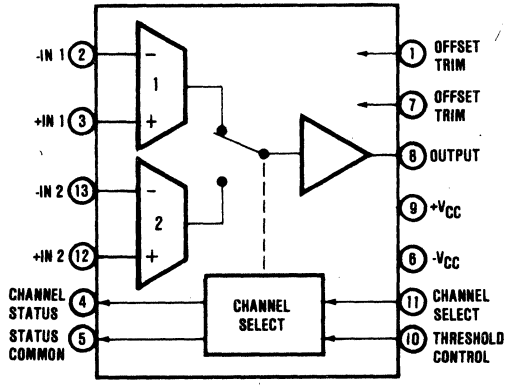
- AUTO-ZERO SYSTEMS
- TWO-CHANNEL MULTIPLEXER WITH GAIN
- SELECTABLE-INPUT INSTRUMENTATION AMPLIFIER
- SWITCHABLE-GAIN CIRCUITS
- SWITCHABLE-BANDWIDTH CIRCUITS
- SYNCHRONOUS MODULATOR/DEMODULATOR
- ISOLATION CIRCUITS
- BATTERY OPERATED SYSTEMS

DESCRIPTION

The OPA201 is a switchable-input operational amplifier (Swop Amp™). It contains two independent differential input stages and one output stage. Either of the input stages may be connected to the output stage under the control of the Channel Select digital input signal which is TTL-compatible or user-programmable. The OPA201 is easy to use and functions as an operational amplifier that can switch between two sets of inputs.

Each input stage provides excellent input characteristics: low offset voltage (100μV, max), low offset voltage drift versus temperature (1μV/°C, max), and low bias current (25nA, max).

Additionally, the Swop Amp is a low power device. It draws less than 500μA (max) over the supply range $\pm$2.5V to $\pm$18V. It is well suited for portable, remote, and other battery powered applications. Also, its low power consumption and excellent specifications make it well suited for isolation circuit applications. Burr-Brown's state-of-the-art monolithic design and processing, compatible thin-film resistors, and active laser trimming produce a truly unique highly versatile circuit. The unique switchable input stage design allows minimum hardware and minimum cost solutions to some very demanding analog circuit design problems.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted. Specifications are for either channel 1 or 2 unless otherwise noted.

PARAMETER	CONDITIONS	OPA201AG/RG			OPA201BG/SG			OPA201CG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN, DC	$V_{OUT} = \pm 10V$										
Rated Load, R_L = 10kΩ	T_A = +25°C	114	130		*	*		120	*		dB
	$T_A = T_{MIN}$ to T_{MAX}	110			*			114			dB
RATED OUTPUT											
Voltage at R_L = 10kΩ	$T_A = T_{MIN}$ to T_{MAX}	±13.5	±14		*	*		*	*		V
Current, $V_{OUT} = \pm 10V$			5			*			*		mA
Output Impedance			0.5			*			*		kΩ
Short Circuit Current			10			*			*		mA
INPUT OFFSET VOLTAGE[1]											
Either Channel											
Initial Offset[2]	T_A = +25°C		120	500		70	200		35	100	μV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		1.4	5.0		0.9	2.0		0.5	1.0	μV/°C
Over Temperature[3]	$T_A = T_{MIN}$ to T_{MAX}		150	1000		100	500		55	200	μV
vs Supply	$\pm V_{CC} = \pm 2.5V$ to ±18V										
	T_A = +25°C		8	32		5	18		4	10	μV/V
	$T_A = T_{MIN}$ to T_{MAX}		10	60		6	32		5	16	μV/V
Match Between											
Channels 1 and 2											
Initial	T_A = +25°C		150	500		65	100		25	50	μV
Over Temperature[3]			150	1000		90	200		30	100	μV
INPUT BIAS CURRENT											
Initial Bias Current	T_A = +25°C		15	50		13	40		12	25	nA
Over Temperature[3]				60			50			30	nA
INPUT OFFSET CURRENT											
Initial Offset Current	T_A = +25°C		1.4	4		0.75	2		0.7	1	nA
Over Temperature[3]				6			4			2	nA
FREQUENCY RESPONSE											
Unity Gain, Small Signal			500			*			*		kHz
Full Power Response			4			*			*		kHz
Slew Rate	$T_A = T_{MIN}$ to T_{MAX}	0.1			*			*			V/μsec
Settling Time 0.1%	10V Step		49			*			*		μsec
Settling Time 0.01%	10V Step		52			*			*		μsec
INPUT IMPEDANCE											
Differential			6			*			*		MΩ
Common-Mode			$10^{10} \parallel 2$			*			*		Ω ‖ pF
INPUT NOISE											
Voltage	f_B = 0.1 to 10Hz		1			*			*		μV, p-p
Voltage Density	f_o = 1Hz		85			*			*		nV/√Hz
	f_o = 10Hz		27			*			*		nV/√Hz
	f_o = 100Hz		27			*			*		nV/√Hz
	f_o = 1kHz		27			*			*		nV/√Hz
Current	f_B = 0.1 to 10Hz		1.5			*			*		pA, p-p
Current Density	f_o = 1Hz		1000			*			*		fA/√Hz
	f_o = 10Hz		300			*			*		fA/√Hz
	f_o = 100Hz		100			*			*		fA/√Hz
	f_o = 1kHz		100			*			*		fA/√Hz
INPUT VOLTAGE RANGE											
Common-Mode	T_A = +25°C	−12.5		+12.5	*		*	*		*	V
Common-Mode	$T_A = T_{MIN}$ to T_{MAX}	−12		+12	*		*	*		*	V
Common-Mode Rejection,	T_A = +25°C	85	94		90	98		95	98		V
V_{IN} = ±10V	$T_A = T_{MIN}$ to T_{MAX}	80	92		85	95		90	97		dB
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range,											
derated performance		±2.5		±18	*		*	*		*	VDC
Current, quiescent			425	500		*	*		*	*	μA
DIGITAL SIGNALS											
Threshold control											
(TC) Voltage Range		$-V_{CC}$		$+V_{CC} - 5$	*		*	*		*	V
Channel Select (CSEL)[4]											
Voltage Range		$-V_{CC}$		$+V_{CC}$	*		*	*		*	V
V_{IH} (selects ch. 1)		$V_{TC} + 2$		$+V_{CC}$	*		*	*		*	V
V_{IL} (selects ch. 2)		$-V_{CC}$		$V_{TC} + 0.8$	*		*	*		*	V
	$T_A = T_{MIN}$ to T_{MAX}	$-V_{CC}$		$V_{TC} + 0.6$	*		*	*		*	V
I_{IH}	$V_{CSEL} = +V_{CC}$		<1	50		*	*		*	*	μA
I_{IL}	$V_{CSEL} = V_{TC} = 0V$		25	60		*	*		*	*	μA
Status Common (SC)											
Voltage Range		$-V_{CC}$		[5]	*		*	*		*	V
Channel Status											
(CSTA = $\overline{CSEL}$)[4]											
V_{OL}	I_{OL} = 1mA, V_{SC} = 0V			0.4			*			*	V
V_{OH}	V_{pullup} = 15V, V_{SC} = 0V	2.0	15		*	*		*	*		V

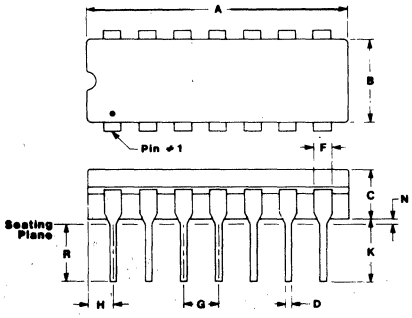
ELECTRICAL (CONT)

PARAMETER	CONDITIONS	OPA201AG/RG			OPA201BG/SG			OPA201CG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL SIGNALS											
I_{OH} (OFF)			<1	20		·	·		·	·	µA
Switching Time											
Between Channels	$T_{MIN} \leq T_A \leq T_{MAX}$		5			·			·		µsec
CROSSTALK											
DC	V_{IN} to OFF	−100	130		120	·		120	·		dB
60Hz	Channel = ±12V		108			·			·		dB
TEMPERATURE RANGE (ambient)											
Specification											
A, B, C Grades		25		+85	·		·	·		·	°C
S Grade					55		+125				°C
Operating		55		+125	·		·	·		·	°C
Storage		65		+150	·		·	·		·	°C

NOTES:
1. 100% tested guaranteed fully warmed-up.
2. Without external adjustment. See Offset Adjustment section.
3. Over temperature specifications are $-55°C < T_A \leq +125°C$ for the S grade and $-25°C \leq T_A \leq +85°C$ for A, B, and C grades.
4. V_{TC} = Voltage on threshold control, pin 10. V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{OH}, I_{OL}, refers to voltage and current, input and output, high and low logic states.
5. Maximum voltage at Status Common must not be more positive than the Channel Select voltage (pin 11) or Threshold Control voltage (pin 10).

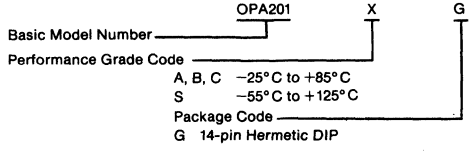
MECHANICAL

NOTES: 1. Leads in true position within 0.01" (0.25mm) R at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.753	.767	19.13	19.48
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.085	—	2.16
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	0.3 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

ORDERING INFORMATION

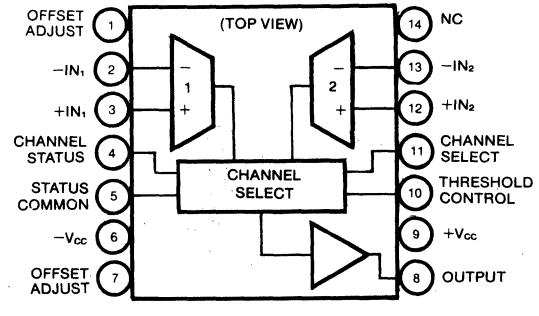


ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES:
1. $\theta_{JA} = 100°C/W$
2. For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to power supply common or $\pm V_{CC}$.

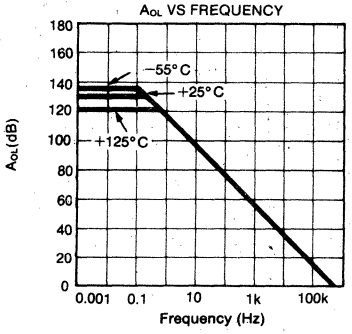
PIN CONFIGURATION



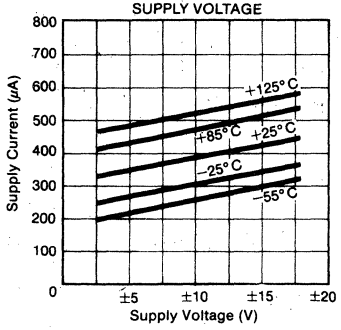
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = 15VDC, specifications are for either channel 1 or 2 unless otherwise noted.

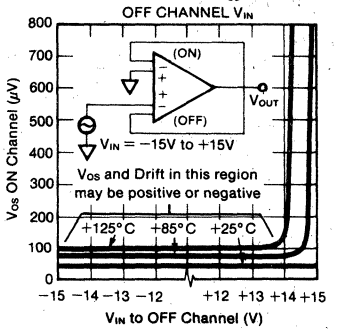
A_{OL} VS FREQUENCY



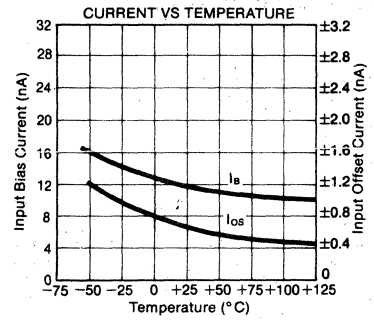
SUPPLY CURRENT VS SUPPLY VOLTAGE



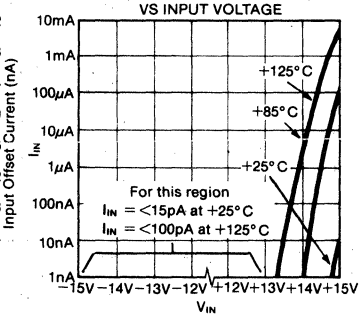
ON CHANNEL V_{OS} VS OFF CHANNEL V_{IN}



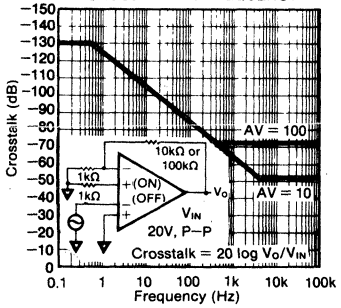
INPUT BIAS AND OFFSET CURRENT VS TEMPERATURE



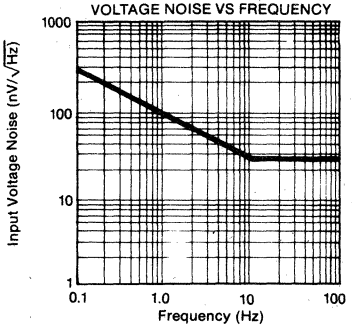
OFF CHANNEL INPUT CURRENT VS INPUT VOLTAGE



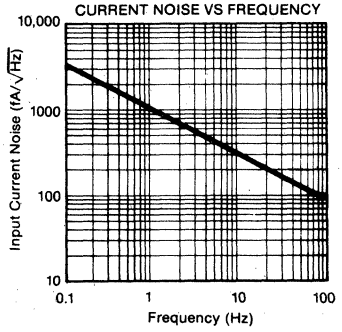
CROSSTALK VS FREQUENCY



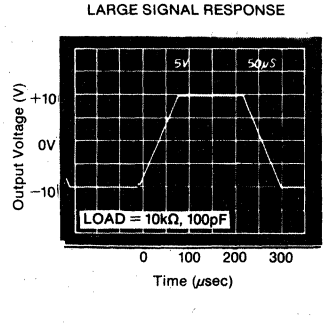
VOLTAGE NOISE VS FREQUENCY



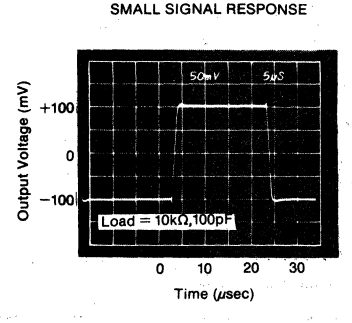
CURRENT NOISE VS FREQUENCY



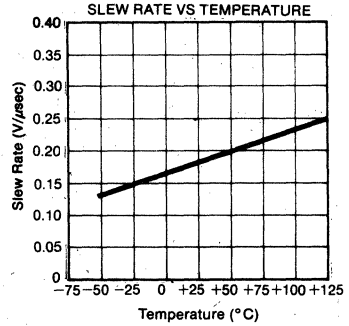
LARGE SIGNAL RESPONSE



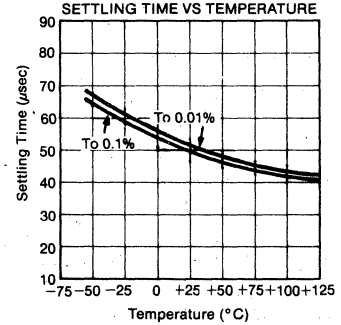
SMALL SIGNAL RESPONSE



SLEW RATE VS TEMPERATURE



SETTLING TIME VS TEMPERATURE



THEORY OF OPERATION

A simplfied schematic of the OPA201 Swop Amp is shown in Figure 1. The circuit has four main parts: (A) input stage 1, (B) input stage 2, (C) active load and output amplifier, and (D) channel select circuit. The two precision differential input stages are identical, with offset and drift laser-trimmed for very-tight matching. The input stages share a balanced, high precision active load and external offset adjust pins, so offset trim affects both channels (see "Using the Swop Amp" section for independent trim techniques). The input stages also share a gain stage and complementary output stage. The biasing circuits for the two input stages are well matched, so the characteristics of the two amplifiers are very nearly identical.

so the channel status can be referenced to ground or −V.

The complete circuit functions as a high precision operational amplifier which can switch between two sets of inputs under control of a 1-bit logic signal.

USING THE SWOP AMP

Designing with the Swop Amp is basically the same as designing with any precision operational amplifer, with the added versatility of switchable inputs. Feedback is connected from the output to each differential input to configure each channel as an inverting or noninverting amplifier, integrator, or other analog circuit function. The transfer functions for channels 1 and 2 may be identical to the point of sharing feedback elements, or they may be completely independent. Feedback resistors for the off channel are driven by the output as part of

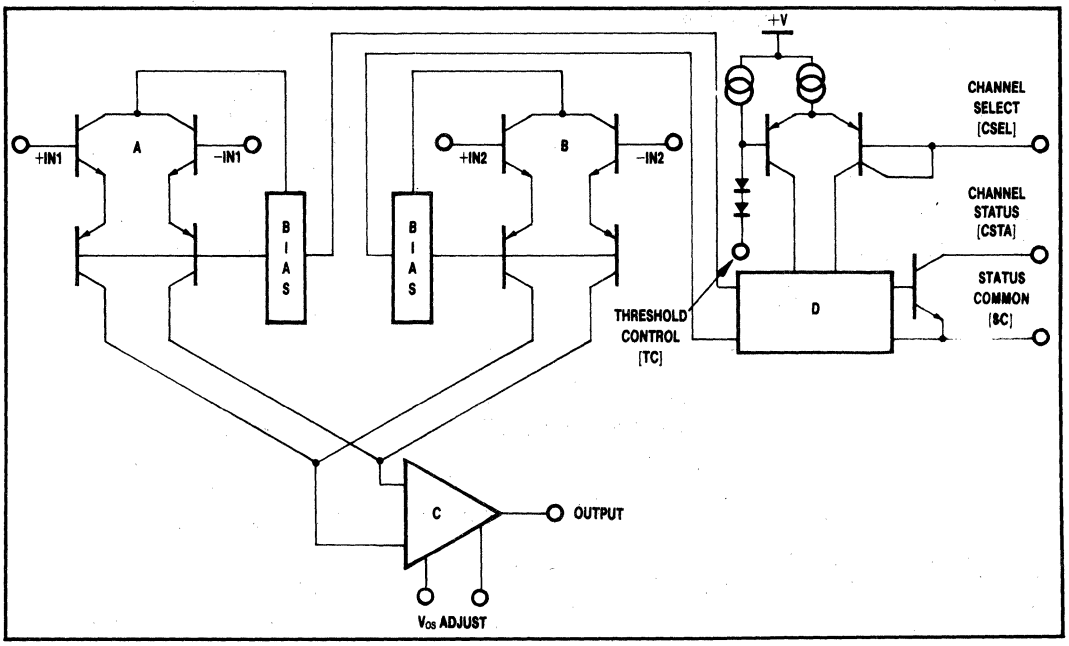


FIGURE 1. OPA 201 Simplified Schematic.

Under control of the channel select circuitry, only one input stage at a time is active. The selected input stage controls the output amplifier, while the unselected input stage is turned off by deactivating its bias circuitry. With no current in the unselected stage, it has negligible input bias current, and the OFF channel cannot send signals to the output amplifier (see Crosstalk specifications and Typical Performance Curves).

The channel select circuitry is simple but versatile, and its use is fully described in the "Using the Swop Amp" section. The trip point for changing channels is set by the threshold control, pin 10. This provides TTL-compatible levels for the channel select voltage on pin 11 when pin 10 is grounded. An open collector output transistor provides the logic inverse of the channel select voltage at the channel status pin. The emitter of this transistor, status common, is also brought out to a pin

the load resistance. Error analysis involving E_{os}, I_B, I_{os}, and V_{cm} is the same as for any operational amplifier.

The OFF channel may be modeled as an open circuit in most applications, with input currents typically under 15pA for input voltages within the specified common-mode range (see Typical Performance Curves). Although crosstalk is specified for OFF channel input voltages equal to the common-mode input range extremes, the same crosstalk characteristics are typically observed for all input voltages between $-V_{CC}$ and ($+V_{CC}$ −1VDC). Rejection of signals applied to the OFF channel's inputs is outstanding, as shown by the −120dB Crosstalk specifications and Typical Performance Curves for crosstalk versus frequency.

CHANNEL SELECTION

Four pins are involved in the channel select logic,

providing programmable input logic levels for channel select and an output status indicating which channel has been selected. Programmable logic levels allow the logic to be referenced to ground or virtually any voltage. Referencing the logic to −V is especially useful in applications where the supply voltage is low, for example ±3V. The pin-by-pin description and recommended connections describe the versatile but simple channel select techniques (refer to Figures 2 and 3).

Pin 10 - Threshold Control

Pin 10 sets the threshold voltage for channel switching, such that the switching point is two diode drops (≈1.3V) more positive than the Threshold Control voltage. This results in TTL compatibility when pin 10 is grounded. Pin 10 must be at least 5V more negative than $+V_{CC}$, and should be tied to $-V_{CC}$ when the minimum supply voltages are used (±2.5V or +5V). This results in TTL compatibility for logic referenced to $-V_{CC}$.

Pin 11 - Channel Select

The voltage on pin 11 determines which input stage is active. A logic high selects channel 1, logic low selects channel 2. Logic voltages are referenced to the Threshold Control, pin 10, and are TTL-, CMOS-, and open collector-compatible.

Pin 4 - Channel Status

Channel Status is an open collector output indicating which channel has been selected. It is the logic inverse of the Channel Select input referenced to Status Common, pin 5. This function is not required in many applications, and pin 4 should be left unconnected if not used. When using Channel Status, a pullup resistor is connected between pin 4 and a potential more positive than pin 5 (usually +V or ground). The logic low (indicating channel 1 selected) will be less than 0.4V more positive than pin 5 if the pullup resistor sets a current of 1mA or less. Logic high will be the voltage connected to the pullup resistor.

Pin 5 - Status Common

Status Common sets the reference point for Channel Status, and is usually connected to the same potential as the Threshold Control. Pin 5 must be more negative than pins 10 and 11 at all times, and should be connected to $-V_{CC}$ if the Channel Status function is not used. Status Common must be at least 5V more negative than $+V_{CC}$.

OFFSET ADJUSTMENT

The input offset voltage is laser-trimmed and will not require user-adjustment for most applications. Pins 1 and 7 may be used to adjust the offset of the active channel to zero (see Figure 4). This will also affect the offset of the inactive channel (both offsets move in the same direction as the pot is adjusted). This technique may be used to make the offset for each channel equal in magnitude and opposite in polarity, which is desirable in many applications. Besides the complementary nature of the adjusted offsets, their magnitudes will now be less than one-half of the V_{os} match specification.

An inexpensive CMOS IC, CD4007 (dual-Complementary Pair Plus Inverter), may be used to alternately connect dual-offset adjust potentiometers (see Figure 5) allowing independent V_{os} adjustment. In this circuit, the channel status output from the Swop Amp is used to drive the CMOS logic, which connects one wiper or the

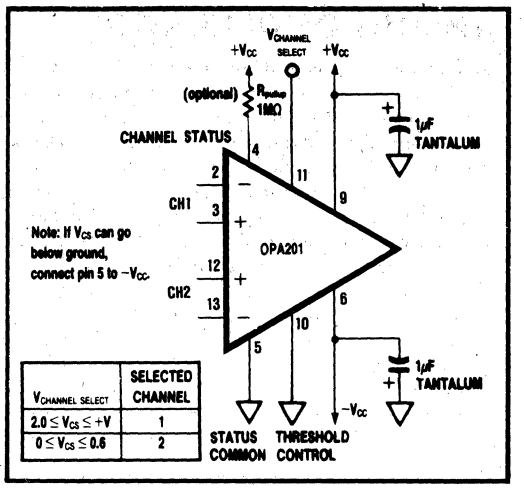


FIGURE 2. Channel Selection for Ground-Referenced Channel Select Signals.

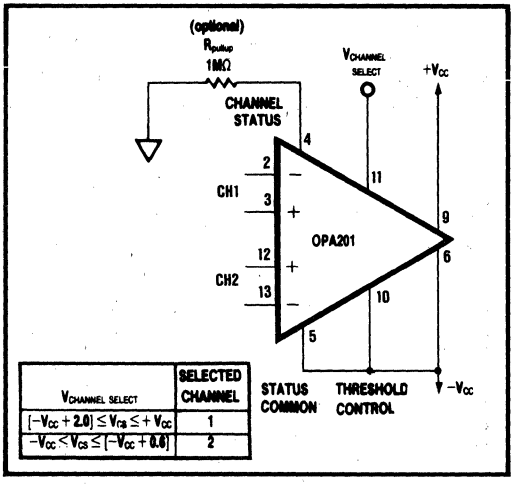


FIGURE 3. Channel Selection for $-V_{CC}$ Referenced Logic Signals.

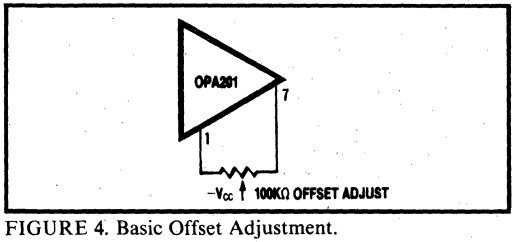


FIGURE 4. Basic Offset Adjustment.

other to $-V_{CC}$. Thus R_1 adjusts the offset of channel 1 while R_2 affects the offset only when channel 2 is selected.

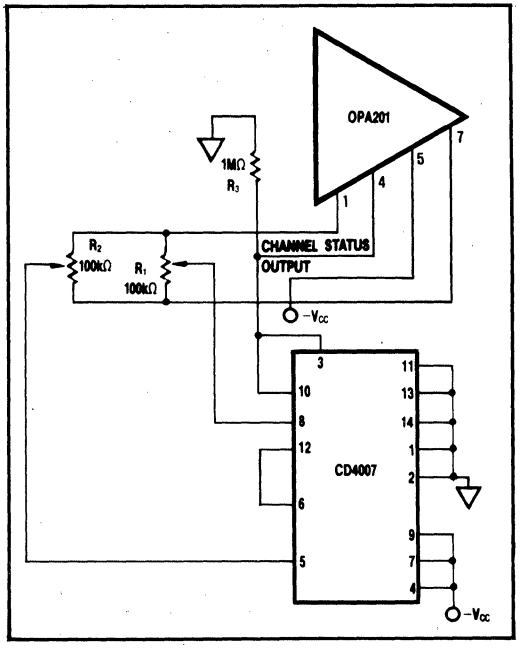


FIGURE 5. Independent Dual-Offset Adjustment.

Note: The CMOS logic requires $-V_{CC}$ (3V minimum) and common. The Status Common (pin 5) must be connected to $-V_{CC}$.

APPLICATIONS

The OPA201 is ideal for a variety of applications where a precision amplifier and switch are needed. Since the two input stages are contained on the same IC and are precision laser-trimmed, their offsets match very closely. Therefore, the OPA201 can be used as an auto-zeroing circuit as well as a dual-channel or switchable-gain amplifier. It can also be extended to become a low power 4-channel Swop Amp or dual-channel instrumentation amplifier under control of TTL level logic. General purpose and unique applications are only limited by the user's imagination.

Software auto-zeroing using the Swop Amp is easy to perform (Figure 6). One channel processes signals and the other channel has the input grounded (both channels have the same gain). The system generating the error signal may be a VFC, Iso Amp, ADC, Modulator, etc. When the zero-input channel is selected,

$$V_{out} = V_{error} + A_V V_{os2}$$

V_{error} = system error voltage
V_{os2} = Channel 2 V_{os}
A_V = Swop Amp voltage gain $= 1 + (R_2/R_1)$

When the signal channel is selected,

$$V_{out} = V_{error} + A_V V_{os1} + A_V V_{IN}$$

Subtracting the "zero" V_o from signal V_o leaves a corrected output voltage

$$V_{out} = A_V V_{IN} + A_V (V_{os1} - V_{os2})$$
$$= A_V (V_{IN} + \Delta V_{os})$$

Using this technique, system errors may be reduced to the V_{os} match error (50μV for CG grade) of the Swop Amp. Obviously the channel used for zeroing could have a voltage reference or AC waveform for gain calibration for an input, instead of ground.

Auto-zeroing may be free-running, with the Swop Amp functioning as a chopper, by connecting an oscillator to the channel select. Figure 6 shows pin 10 grounded, which allows TTL level interfacing. By programming this pin with a voltage level, other logic levels can be accommodated.

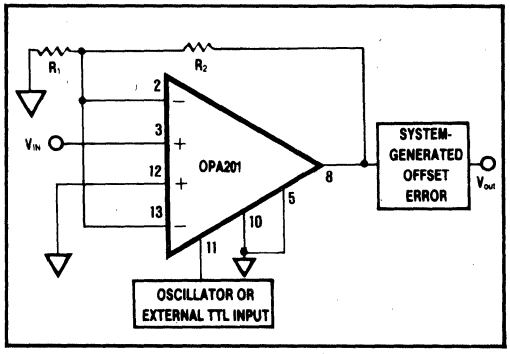


FIGURE 6. Input Amplifier for Auto-Zeroing Systems.

The OPA201 requires only external resistors to make a dual-channel amplifier (2-channel multiplexer with gain). Gain for either channel may be noninverting (Figure 7) or inverting (Figure 8) with the usual operational amplifier gain equations applying in each case. In the noninverting case, feedback is connected from the output to each input, with a common feedback resistor for equal gains. The advantage, in inverting gain circuits, is that the signal does not produce a common-mode voltage which can introduce error or input swing limitations. This is especially important in low supply voltage applications where common-mode range becomes limited. Also one channel can be noninverting and the other inverting, which is particularly useful in absolute value circuits. Note that in order to achieve the specified open-loop gain and maximum output voltage swing, the total output load including both feedback networks should not exceed 10kΩ (see Figures 7 and 8).

Amplifiers with switchable transfer functions are designed much like dual-channel amplifiers, except both inputs are connected in parallel, with each channel configured for a different transfer function. Figure 9 shows a circuit that has a gain of 10 for Channel Select HIGH (channel 1 selected) and a gain of 1000 for Channel Select LOW (channel 2 selected). In this case, the channel select may be thought of as a gain select.

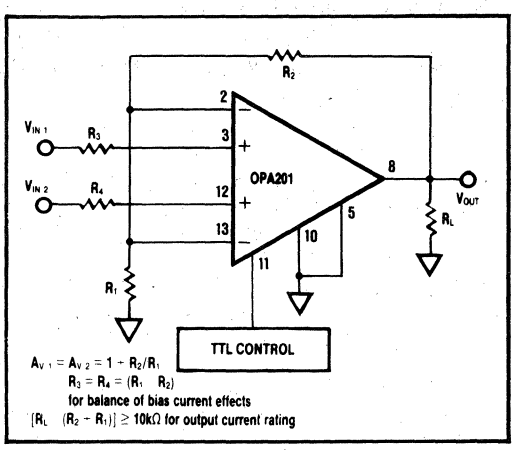


FIGURE 7. Selectable Input Amplifier, Noninverting.

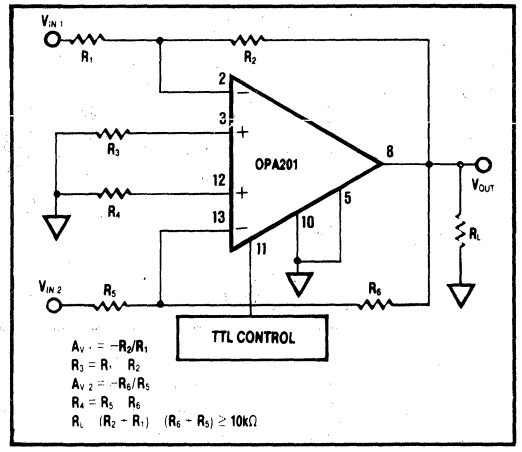


FIGURE 8. Selectable Input Amplifier, Inverting.

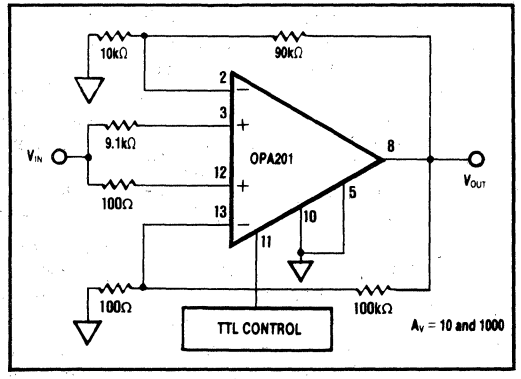


FIGURE 9. Switchable Gain Amplifier.

This concept also applies to switchable bandwidth circuits, where AC coupling (high-pass) or smoothing (low-pass) characteristics need to be switched in under digital control. A wide variety of operational amplifier function circuits may be made selectable or switchable using these techniques.

Figure 10 shows a two-channel differential amplifier. This concept can be expanded to a full high input impedance instrumentation amplifier by adding four input buffer amplifiers or by using two front end Swop Amps followed by an operational amp (Figure 11).

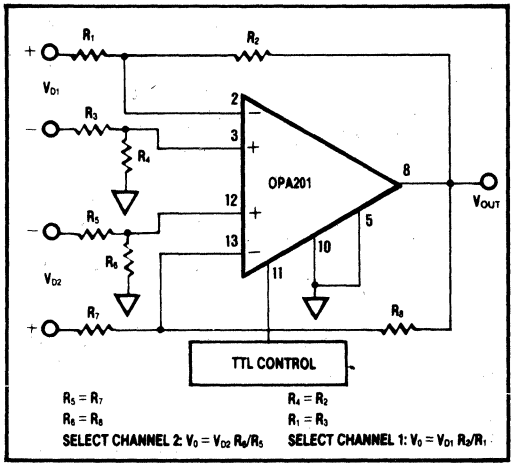


FIGURE 10. Low Power Dual-Channel Differential Amplifier.

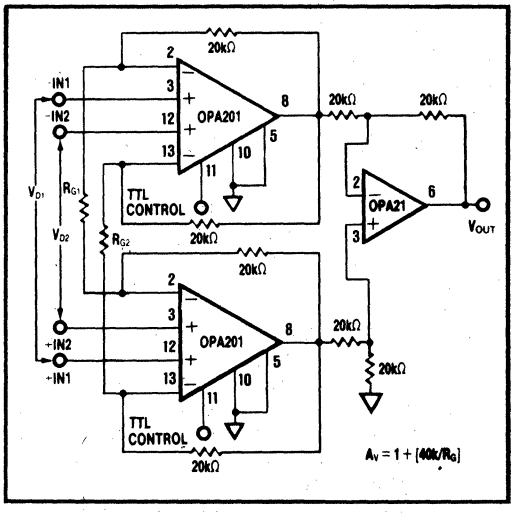
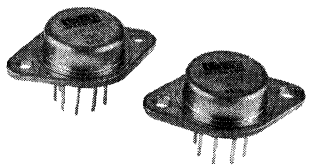


FIGURE 11. Low Power Dual-Channel Instrumentation Amplifier.

BURR-BROWN®



OPA501

High Current - High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE
  ±10 to ±40 Volts
- HIGH OUTPUT CURRENT
  ±10 Amps Peak
- HIGH OUTPUT POWER
  260 Watts Peak
- SMALL SIZE: TO-3 PACKAGE

APPLICATIONS

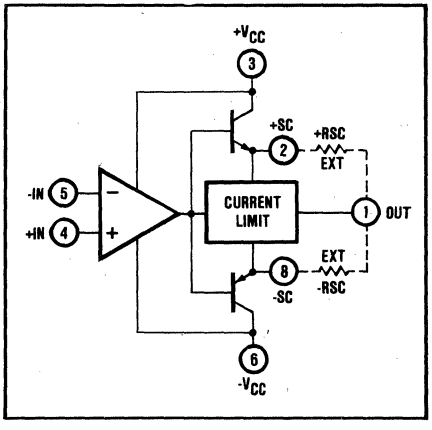
- SERVO AMPLIFIER
- MOTOR DRIVER
- ACTUATOR CONTROL
- AUDIO AMPLIFIER
- SYNCRO DRIVER
- POWER SUPPLY REGULATOR

DESCRIPTION

The OPA501 is a high power operational amplifier. Its high current output stage delivers ±10A yet the amplifier is unity-gain stable and it can be used in any operational amplifier configuration. The 260W peak output capability allows the OPA501 to drive loads (such as motors) with a greater safety margin.

Safe operating area is fully specified and output current limiting is provided to protect both the amplifier and the load from excessive current.

This hybrid IC is housed in an 8-pin hermetic TO-3 package. The electrically-isolated package allows direct mounting to chassis or heat sink without an insulating washer or spacer which would increase thermal resistance.



SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and $\pm V_{CC}$ = 28VDC (OPA501RM/AM); $\pm V_{CC}$ = 34VDC (OPA501SM/BM) unless otherwise noted.

PARAMETER	CONDITIONS	OPA501RM/AM			OPA501SM/BM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RATED OUTPUT(1)(2)								
Output Current,	R_L = 2Ω (RM/AM)	±10			*			A
Continuous(3)	R_L = 2.6Ω (SM/BM)	±10			*			A
Output Voltage(3)	I_o = 10A peak	±20	23		±26	±29		V
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal		1			*		MHz
Full Power Bandwidth	V_o = 40Vp-p, R_L = 8Ω	10	16		*	*		kHz
Slew Rate	R_L = 5Ω (RM/AM)	1.5			*			V/µsec
	R_L = 6.5Ω (SM/BM)	1.5			*			V/µsec
INPUT OFFSET VOLTAGE								
Initial Offset			±5	±10		±2	±5	mV
vs Temperature	−25°C < T < +85°C (AM/BM)		±10	±65				µV/°C
	−55°C < T < +125°C (RM/SM)					±10	±40	µV/°C
vs Supply Voltage			±35			*		µV/V
INPUT BIAS CURRENT								
Initial	T_{case} = +25°C		15	40		*	20	nA
vs Temperature			±0.05			*		nA/°C
vs Supply Voltage			±0.02			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	T_{case} = +25°C		±5	±10		±2	±3	nA
vs Temperature	−25°C < T < +85°C (AM/BM)		±0.01					nA/°C
	−55°C < T < +125°C (RM/SM)					±0.01		nA/°C
OPEN-LOOP GAIN, DC	R_L = 5Ω (RM/AM)	94	115					dB
	R_L = 6.5Ω (SM/BM)				98	115		dB
INPUT IMPEDANCE								
Differential			10			*		MΩ
Common-mode			250			*		MΩ
INPUT NOISE								
Voltage Noise	f_n = 0.3Hz to 10Hz		3			*		µV, p-p
	f_n = 10Hz to 10kHz		5			*		µV, rms
Current Noise	f_n = 0.3Hz to 10Hz		20			*		pA, p-p
	f_n = 10Hz to 10kHz		4.5			*		pA, rms
INPUT VOLTAGE RANGE								
Common-mode Voltage(4)	Linear Operation	±(|V_{CC}|-6)	±(|V_{CC}|-3)		*	*		V
Common-mode Rejection	F = DC, V_{CM} = ±(|V_{CC}|-6)	70	110		80	*		dB
POWER SUPPLY								
Rated Voltage			±28			±34		V
Operating Voltage Range		±10		±36	*		±40	V
Current, quiescent			±2.6	±10		*	*	mA
TEMPERATURE RANGE	case							
Specification, RM/SM		-55		+125	*		*	°C
AM/BM		-25		+85	*		*	°C
Operating, derated performance, AM/BM		-55		+125	*		*	°C
Storage		-65		+150	*		*	°C
THERMAL RESISTANCE	Steady State θ_{JC}		2.0	2.2		*	*	°C/W

*Specification same as for OPA501RM/AM.

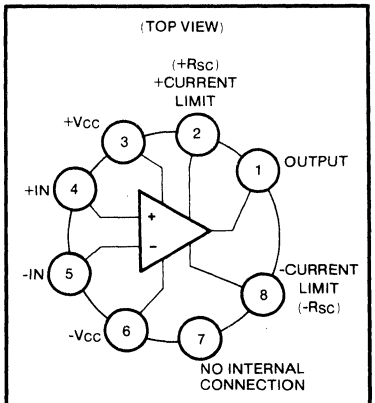
NOTES:
1. Package must be derated based on a junction to case thermal resistance of 2.2°C/W or a junction to ambient thermal resistance of 30°C/W.
2. Safe Operating Area and Power Derating Curves must be observed.
3. With $\pm R_{SC}$ = 0. Peak output current is typically greater than 10A if duty cycle and pulse width limitations are observed. Output current greater than 10A is not guaranteed.
4. The absolute maximum voltage is 3V less than supply voltage.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage (V_{CC})	±40V DC
Power dissipation at +25°C[1][2]	79W
Differential input voltage	$\pm V_{CC}$-3V
Common-mode input voltage	$\pm V_{CC}$
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10sec)	+300°C
Junction temperature	+200°C
Output short-circuit duration[3]	continuous

NOTES:
1. At case temperature of +25° C. Derate at 2.2° C/W above case temperature of +25° C.
2. Average dissipation.
3. Within safe operating area and with appropriate derating.

CONNECTION DIAGRAM



ORDERING INFORMATION

OPA501 X M

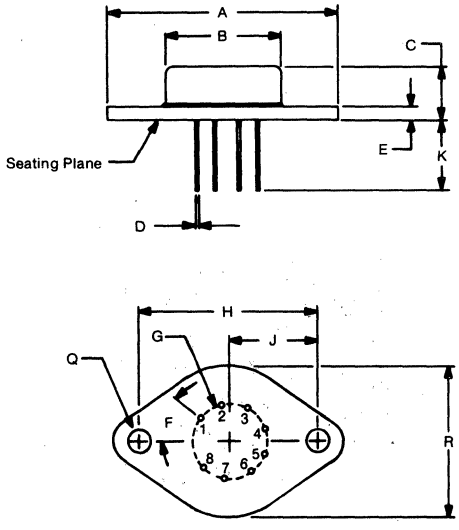
Basic Model Number

Performance Grade Code
- A, B = -25° C to +85° C
- R, S = -55° C to +125° C

Package Code
- TO-3

OPA501AM	
OPA501BM	
OPA501RM	
OPA501SM	

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

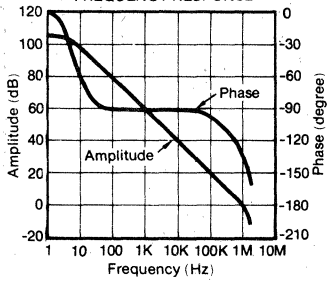
Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

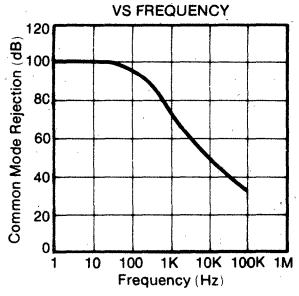
TYPICAL PERFORMANCE CURVES

(Typical at +25° case and ±V_{CC} = 28VDC unless otherwise noted.)

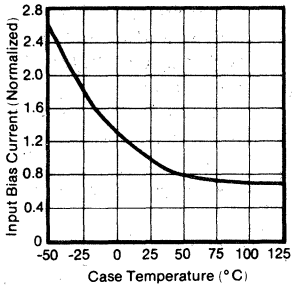
OPEN-LOOP FREQUENCY RESPONSE



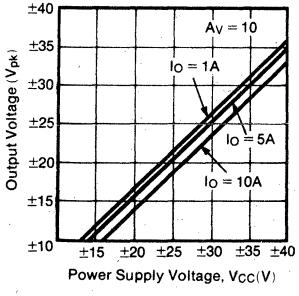
COMMON MODE REJECTION VS FREQUENCY



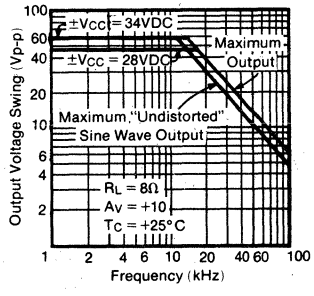
INPUT BIAS CURRENT VS TEMPERATURE



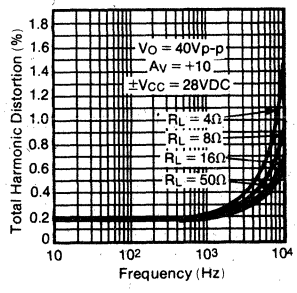
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE



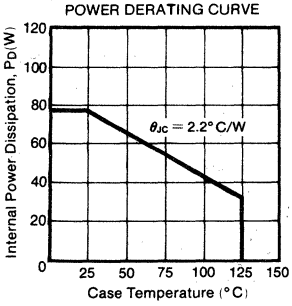
FULL POWER RESPONSE



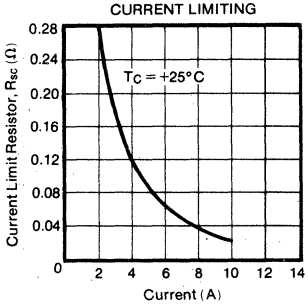
HARMONIC DISTORTION



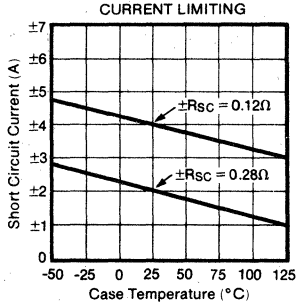
POWER DERATING CURVE



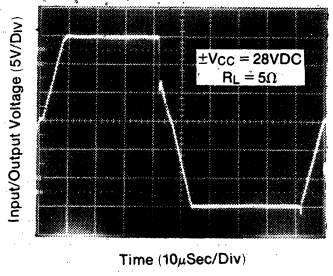
CURRENT LIMITING



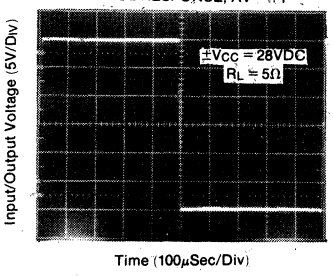
CURRENT LIMITING



PULSE RESPONSE, AV = +1



PULSE RESPONSE, AV = +1



INSTALLATION AND OPERATING INSTRUCTIONS

PROPER GROUNDING AND POWER SUPPLY BYPASSING

Particular attention should be given to proper grounding practices because the large output currents can cause significant ground-loop errors. Figure 1 illustrates proper connections.

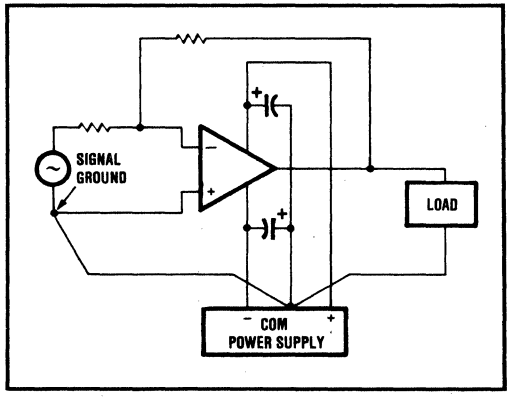


FIGURE 1. Proper Power Supply Connections.

Note that the connections are such that the load curent does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power-supply-bypassed with 10μF tantalum capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The OPA501 amplifier is designed so that both the positive and negative load current limits can be set independently with external resistors R_{+SC} and R_{-SC} respectively. The approximate value of these resistors is given by the equation:

$$R_{SC} = \left(\frac{0.65}{I_{LIMIT}} - 0.0437\right) \text{ ohms}$$

I_{LIMIT} is the desired maximum current in amperes. The power dissipation of the current limit resistor is:

$$P_{max} = R_{SC} (I_{LIMIT})^2 \text{ watts}$$

R_{SC} is in ohms and I_{LIMIT} is in amperes.

Current limit resistors carry the full amplifier output current so lead lengths should be minimized. Highly inductive resistors can cause loop instability. Variation in I_{LIMIT} with case temperature is shown in the Typical Performance Curves.

The amplifier should be used with as low a current limit as possible for its particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and will increase reliability by limiting internal power dissipation.

The current limits may be used to generate other functions such as constant current supplies and torque or stall current limits for servomotor applications.

HEAT SINKING

The OPA501 requires a heat sink to limit output transistor junction temperature (T_J) to an absolute maximum of +200°C. The steady-state thermal circuit is illustrated in Figure 2.

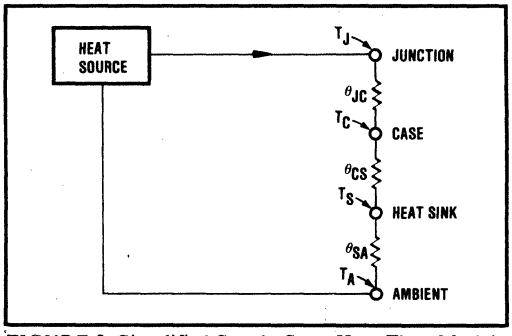


FIGURE 2. Simplified Steady-State Heat Flow Model.

Junction temperature (T_J) is found from the equation:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

Where P_D = average amplifier power dissipation (W)
θ_{JC} = junction to case thermal resistance (°C/W)
θ_{CS} = device mounting thermal resistance (°C/W)
θ_{SA} = heat sink thermal resistance (°C/W)
T_A = ambient temperature (°C)

For most heat sink calculations the quiescent power dissipation is very low (<1 watt) and can be disregarded with only a small error.

The minimum size heat sink can be found from the equation:

$$\theta_{SA} = \frac{T_J - T_A}{P_D} - \theta_{CS} - \theta_{JC}$$

Example: Find the maximum thermal resistance (smallest heat sink) that can be used for an OPA501 with $\pm V_{CC}$ = 28VDC. Output voltage is +10VDC across a 10Ω resistor and ambient temperature is +50°C:

$$P_D = [(+28\text{VDC}) - (+10\text{VDC})] \times \frac{+10\text{VDC}}{10\Omega} = 18\text{W}$$

$$\theta_{SA} = \frac{200°\text{C} - 50°\text{C}}{18\text{W}} - 0.1°\text{C/W} - 2.2°\text{C/W}$$

θ_{SA} = 6.03°C/W maximum

As large a heat sink as possible should be used. θ_{CS} depends on the flatness of the heat sink, the thermal compound used, and the roughness of the mating surfaces. Typical values are between 0.1°C/W and 0.3°C/W for a TO-3 package properly mounted on a heat sink.

The OPA501 mounting flange is electrically-isolated and can be mounted directly to a heat sink without insulating washers or spacers. Screws with Bellville spring washers are recommended to maintain positive clamping pressure on heat sink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase θ_{CS}.

The output transistor thermal resistance (θ_{JC}) is a function of output current pulse width, pulse shape, and duty cycle. Long duration pulses allow the junction temperature to approach its steady state value while shorter pulses cause a lower peak junction temperature due to the junction's thermal time constant. Heat is conducted rapidly away from the junction so that as duty cycle decreases, junction temperature decreases.

Steady state θ_{JC} is rated at 2.2°C/W maximum. In applications where the amplifier's output current alternates between output transistors–for example, an AC amplifier–the transistor θ_{JC} will depend on frequency as shown in Figure 3.

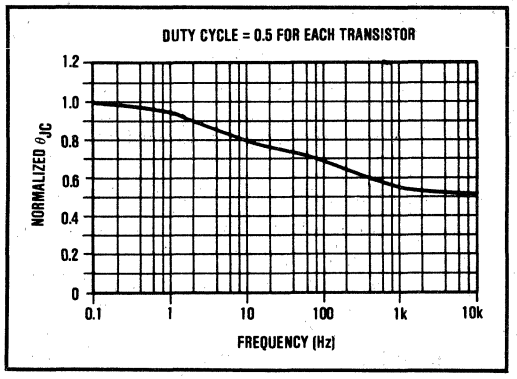


FIGURE 3. Effective θ_{JC} for Applications Where Output Current Alternates Between Output Transistors.

Example: OPA501SM with $\pm V_{CC}$ = 28VDC; heat sink θ_{SA} = 0.4°C/W; output = 11.2VAC, rms 400Hz at 5A, rms; Power Factor = 1.0; assume a mounting resistance of 0.1°C/W and an ambient temperature of +25°C.

Peak output voltage is: (11.2V, rms) $\sqrt{2}$ = 15.84V,pk
Peak voltage across each output transistor is:
28V - 15.84V = 12.16V, pk
Peak output current is: (5A, rms) $\sqrt{2}$ = 7.07A, pk
Peak power dissipated by each output transistor is:
(12.16V, pk) (7.07A, pk) (1.0) = 85.97W, pk
From Figure 3, the effective value of θ_{JC} is 0.60 × rated θ_{JC}, therefore,
θ_{JC} = 1.32°C/W for this example.
The peak junction temperature will be:
T_J = 85.97W (1.32°C/W + 0.1°C/W + 0.4°C/W) +25°C
T_J = 181.5°C/W

This is below the maximum junction temperature limits of +200°C, but a lower T_J will increase the amplifier's reliability. In this case, a lower $\pm V_{CC}$ could be used to reduce dissipation.

At lower frequencies, the junction temperature can show greater modulation as the output power transistor dissipation increases and decreases with output voltage and current swing. To ensure that the maximum junction temperature is not exceeded, use the appropriate value of effective θ_{JC} from Figure 3.

To illustrate the importance of considering frequency, consider the previous example, but with the amplifier operating at 60Hz:

For a 60Hz output
the effective θ_{JC} = 0.72 × rated θ_{JC} = 1.58°C/W
T_J = 85.97W (1.58°C/W + 0.1°C/W + 0.4°C/W) + 25°C
T_J = 204°C: UNACCEPTABLE

NOTE: Maximum dissipation does not occur at maximum output.

SAFE OPERATING AREA (SOA)

In addition to the limits imposed by power dissipation, the amplifier's output transistors are also limited by a second breakdown region. This occurs because of increased emitter current density due to current crowding at higher operating voltages. Both the dissipation and second breakdown limits depend on time and temperature. Figure 4 shows each output transistor's SOA at a case temperature of +25°C.

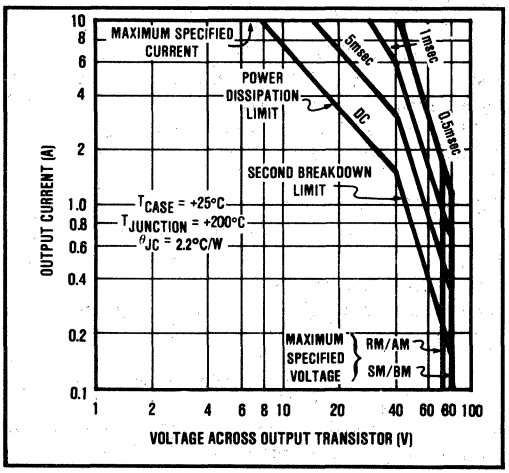


FIGURE 4. Transistor Safe Operating Area at +25°C Case Temperature.

Limits for short pulse widths are substantially greater than for steady state (DC). At a case temperature of +125°C the SOA limits are reduced (see Figure 5). The SOA shown in these curves is based on a conservative linear derating of both the power dissipation and the second breakdown region.

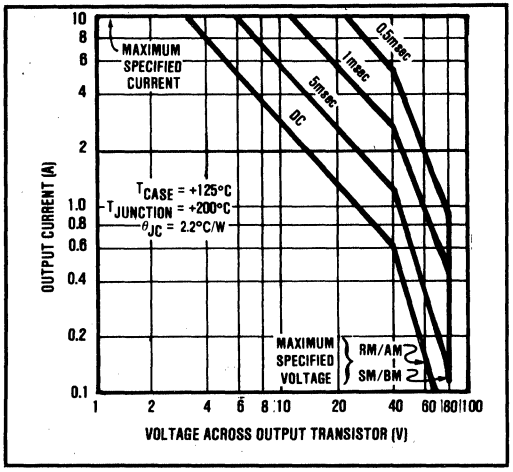


FIGURE 5. Transistor Safe Operating Area at +125°C Case Temperature.

Resistive loads are easy to analyze by simply plotting load lines on the SOA curve. If the curve representing the load line stays within the OPA501 output transistor SOA curve and all other parameters are observed, such as case temperature, etc., the amplifier will be safe. The load line can swing through the larger SOA limits if their time duration constraints are strictly observed.

Reactive loads present a more complex problem since the output voltage and current are not in phase. This results in the reactive load line becoming elliptical (when plotted on linear axes) which requires a larger SOA for safe operation.

Although detailed analysis is beyond the scope of this data sheet, the load line can be viewed on an oscilloscope as shown in Figure 6. The X-Y display is driven by the voltage across the load and by the current into the load.

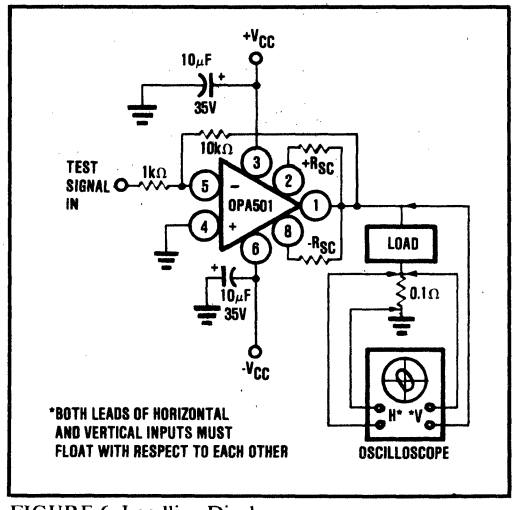


FIGURE 6. Loadline Display.

This set up can also display voltage and current stress across the OPA501 output transistors as shown in Figure 7. This data can then be compared to the SOA limits.

The amplifier is designed to operate with electromotive-force-generating loads such as servomotors, relays, and actuators. Careful attention must be paid to both the load characteristics and the amplifier's SOA to ensure safe operation.

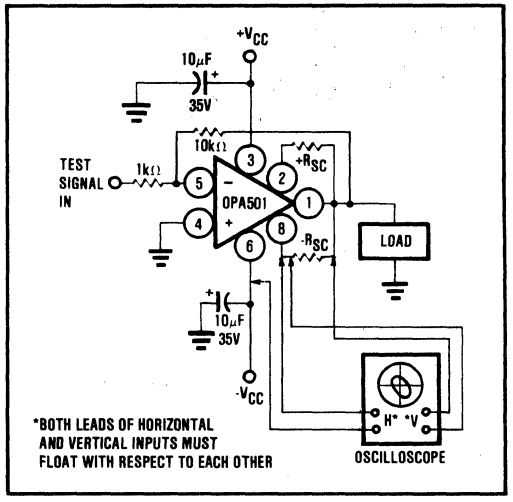


FIGURE 7. Output Transistor Safe Operating Area Stress Display.

Figure 8 shows the OPA501 configured as a DC permanent magnet motor driver. The armature current (I_A) and motor voltage (V_m) are monitored within an oscilloscope in the X-Y mode displaying I_A and V_m respectively. Slewing the motor with a 4Hz sine wave results in the motor power ellipse of Figure 9. The input level has been adjusted to give ±20V, pk, across the motor. An examination of the power ellipse indicates that the instan-

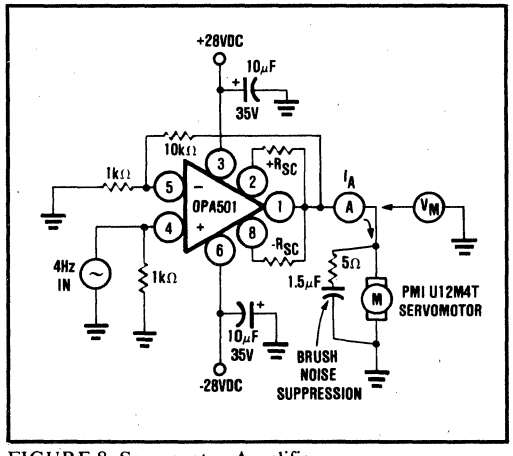


FIGURE 8. Servomotor Amplifier.

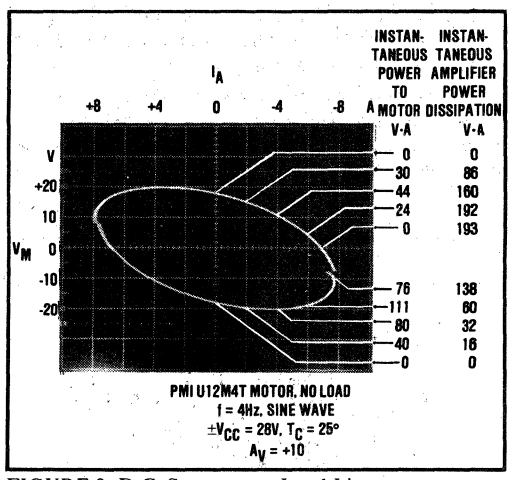


FIGURE 9. D.C. Servomotor Load Line.

taneous power delivered to the motor exceeds the amplifier output transistor's safe operating area at a case temperature of +25° C. The point at which the motor shows 0V at -6.9A is a problem. The voltage across the output transistor is 28V - 0V = 28V. Checking the SOA curve shows that the amplifier can safely withstand this condition for slightly under 5msec. At 4Hz this transient swing outside the DC SOA region is exceeded for much longer than 5msec. Continued operation under these conditions will result in failure. Peak junction temperatures should not exceed +200° C. Perhaps a motor with a higher impedance winding should be considered for this application. Current limiting and lower supply voltage can also reduce dissipation.

Motors used in servo applications often required a surprisingly large current to accelerate quickly. Worst case conditions occur when the motor is operating at full speed and is suddenly slammed into reverse ("plugging"). This condition is illustrated in Figure 10 when a DC servomotor is driven by a bipolar square wave. As the motor reverses direction a large surge current flows, causing very high peak power dissipation in the amplifier. After several time constants (determined by the inertia moment) the current drops to a lower steady-state value. Loading the motor increases the motor average power and amplifier dissipation. SOA curves should be checked for safe operation under these surge conditions.

The OPA501 current limits may be set to clip the high surge currents to a safe level. This is shown in Figure 11. Note that the current limit does limit the servo motor peak acceleration.

Inductive loads should be investigated for high peak transients generated by a collapsing magnetic field. Resistive damping can reduce this problem and although the amplifier has substrate diodes as part of the Darlington output transistor structure, external diodes are recommended for heavy clamping.

Fast diodes such as those normally used as rectifiers in switching power supplies are suitable.

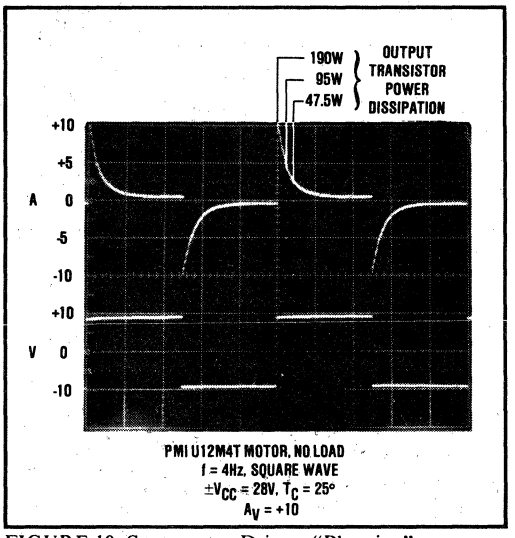


FIGURE 10. Servomotor Drive – "Plugging"

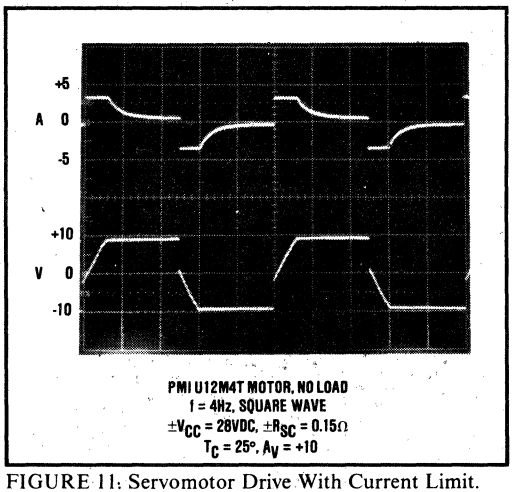


FIGURE 11: Servomotor Drive With Current Limit.

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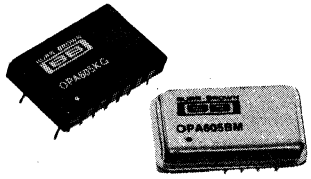
OPA605



Wideband - Fast Settling OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING - 500nsec max to 0.1%
- WIDE BANDWIDTH - 200MHz Gain - Bandwidth Product
- FAST SLEWING - 300V/μsec slew rate, $A_{CL} \geq 50$
- LARGE OUTPUT CURRENT - ±30mA min at ±10V
- HIGH GAIN - 80dB min at ±30mA output
- LOW VOLTAGE OFFSET AND DRIFT - 500μV max, 5μV/°C max

APPLICATIONS

- PULSE AMPLIFIERS
- FAST D/A CONVERTERS
- LINE DRIVERS
- WAVEFORM GENERATORS
- HIGH SPEED TEST EQUIPMENT

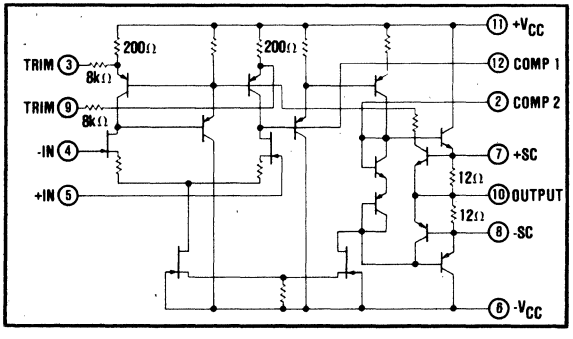
DESCRIPTION

The OPA605 is designed to offer a well balanced set of both AC and DC specifications. Versatility in fast settling, wideband and steady state AC applications is provided by the use of a single external compensation capacitor. This allows the user to optimize speed and stability for any particular application.

The full ±30mA guaranteed minimum output current (at ±10V) allows the user to realize the high speed features of the OPA605. Unlike most integrated circuit wideband amplifiers additional current booster circuitry is not needed for most applications.

The 500nsec max to 0.1% settling time specification is guaranteed with a load of 500Ω and 100pF. Also the open-loop gain is guaranteed at the full ±30mA output.

In addition to the excellent wideband and fast settling characteristics, the OPA605 also offers outstanding DC performance. Offset voltages are as low as 500μV max and offset voltage drift versus temperature of only 5μV °C max is available.



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SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL		OPA605GH/OPA605AM			OPA605KG/OPA605CM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OPEN-LOOP GAIN, DC								
Full Load	V_O = ±10V; R_L = 330Ω	80	96		*	*		dB
No Load	V_O = ±10V; $R_L \geq$ 10kΩ		102			*		dB
RATED OUTPUT								
Voltage	I_O = ±30mA	±10	±12		*	*		V
Current	V_O = ±10V	±30	±50		*	*		mA
Output Resistance	Open Loop		200			*		Ω
Short Circuit Current	Internal Limits(1)	±30	±50	±80	*	*	*	mA
Capacitive Load(2)	A_{CL} = -1, C_C = 20pF	500			*			pF
DYNAMIC RESPONSE								
Gain-Bandwidth Product								
A_{CL} = 1000, C_C = 0			200			*		MHz
A_{CL} = -1, C_C = 20pF			20			*		MHz
Slew Rate	R_L = 330Ω, V_O = 0 to +10V,							
$A_{CL} \geq$ 50, C_C = 0	0 to -10V		300			*		V/μsec
A_{CL} = -1, C_C = 20pF		80	94		*	*		V/μsec
Full Power Bandwidth	R_L = 330Ω, V_O = ±10V,	1.3	1.5		*	*		MHz
	A_{CL} = -1, C_C = 20pF							
Settling Time, A_V = -1(3)	C_C = 20pF, R_L = 500Ω,							
	C_L = 100pF, V_O = 0 to +10V,							
	0 to -10V							
ε = 1%			200			*		nsec
ε = 0.1%			300	500		*	*	nsec
ε = 0.01%			400			*		nsec
Small-Signal Overshoot	A_V = -1, C_C = 20pF, R_L = 500Ω		0	20		*	*	%
	C_L = 100pF							
INPUT OFFSET VOLTAGE								
Initial Offset	T_A = +25°C		±0.25	±1.0		*	±0.5	mV
vs Temperature	T_L to T_H, V_{CM} = 0			±25			±5	μV/°C
vs Supply Voltage			±30	±200		*	*	μV/V
Adjustment Range(4)	Circuit in		±9			*		mV
	"Connection Diagram"							
INPUT BIAS CURRENT								
Initial Bias	T_A = +25°C, V_{CM} = 0		-10	-35		*	*	pA
vs Temperature	T_L to T_H		Note 5			*		
vs Supply Voltage			0.2			*		pA/V
vs V_{CM}			Note 6			*		
INPUT DIFFERRENCE CURRENT								
Initial Difference	T_A = +25°C, V_{CM} = 0		±2			*		pA
vs Temperature			Note 5			*		
vs Supply Voltage			0.05			*		pA/V
VOLTAGE NOISE DENSITY $R_S \leq$ 100Ω								
	f_O = 10Hz		80			*		nV/√Hz
	f_O = 100Hz		30			*		nV/√Hz
	f_O = 1kHz		20			*		nV/√Hz
	f_O = 10kHz		12			*		nV/√Hz
	f_O = 100kHz		12			*		nV√Hz
INPUT IMPEDANCE								
Differential								
Resistance			10^{11}			*		Ω
Capacitance			3			*		pF
Common-Mode								
Resistance			10^{11}			*		Ω
Capacitance			3			*		pF
INPUT VOLTAGE RANGE								
Common-Mode Voltage	Linear Operation							
Range		±10	±12		*	*		V
Common-Mode Rejection		70	90		80	90		dB
POWER SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range	Derated Performance	±5		±18	*		*	VDC
Current, Quiescent			±7.2	±9		*	*	mA
TEMPERATURE RANGE								
Specification								
GH, KG Grades	T_L to T_H	0		+70	*		*	°C
AM, CM Grades	T_L to T_H	-25		+85	*		*	°C
Operating	Derated Performance	-55		+125	*		*	°C
Storage		-65		+150	*		*	°C

NOTES: *Specifications same as for OPA605H/OPA605A. (1) Current limit may be increased with external resistors. (2) Allowable capacitive load depends on several factors. See Compensation section. (3) Settling Time measured in circuit of Figure 4. (4) Adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted. (5) Doubles approximately every 8.5°C. (6) See Typical Performance Curves.

ABSOLUTE MAXIMUM RATINGS

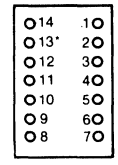
Supply	±20VDC
Internal Power Dissipation	(1)
Differential Input Voltage(2)	±20VDC
Input Voltage, Either Input(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration(3)	Continuous
Junction Temperature	+175°C

NOTES:
1. Package must be derated according to details in the Applications Information section.
2. For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage.
3. Short circuit to ground only. See Short Circuit Protection discussion in the Application Information section.

PIN CONFIGURATION

1. No Internal Connection.
2. Optional Frequency Compensation.
3. Offset Adjust.
4. Inverting Input.
5. Noninverting Input.
6. -Vcc.
7. Optional Short Circuit Adjust.
8. Optional Short Circuit Adjust.
9. Offset Adjust.
10. Output.
11. +Vcc.
12. Frequency Compensation.
13. No Internal Connection*.
14. No Internal Connection.

*Case on metal package

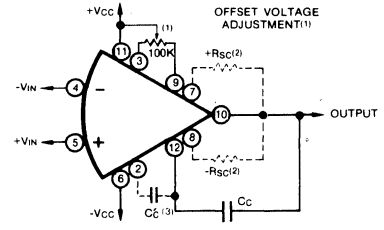


Bottom View

Pin numbers shown for reference only. Numbers are not marked on package.

Pin 13 is case on metal unit.

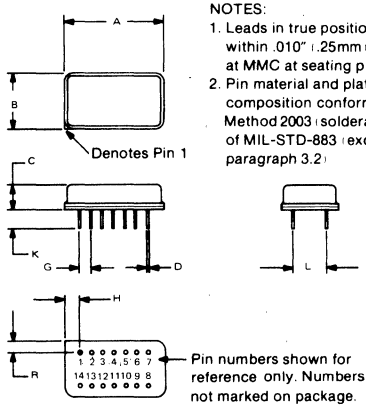
CONNECTION DIAGRAM



NOTES:
1. Offset voltage adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted.
2. Optional resistors to increase current limits. See Application Information.
3. Optional frequency compensation. See Applications Information.

MECHANICAL

METAL PACKAGE—"M"

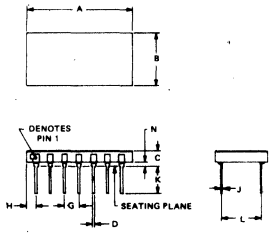


NOTES:
1. Leads in true position within .010" (.25mm) R at MMC at seating plane.
2. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

CERAMIC PACKAGE—"G"



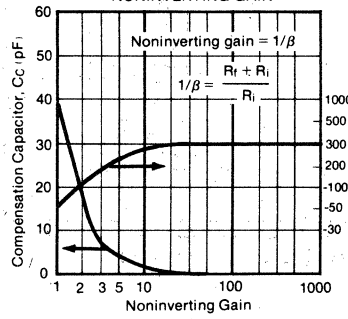
NOTES:
1. Leads in true position within .010" (.25mm) R at MMC at seating plane.
2. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.770	.810	19.56	20.57
B	.480	.500	12.19	12.70
C	.155	.215	3.94	5.46
D	.016	.020	.41	.51
G	.100 BASIC		2.54 BASIC	
H	.080	.110	2.03	2.79
J	.009	.012	.23	.30
K	.150	.210	3.81	5.33
L	.300 BASIC		7.62 BASIC	
N	.015	.035	.38	.89

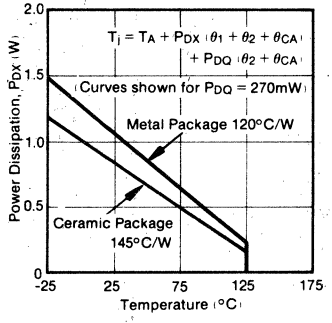
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted)

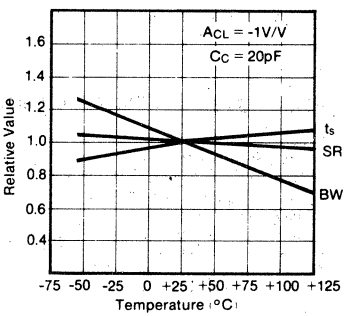
COMPENSATION CAPACITANCE AND SLEW RATE VS NONINVERTING GAIN



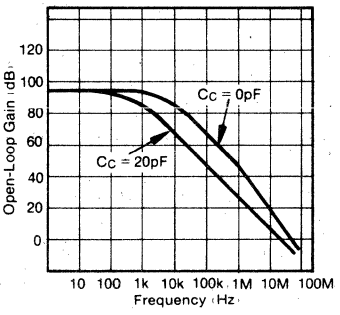
POWER DERATING



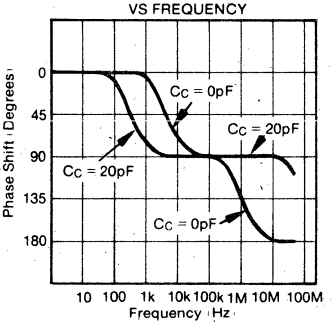
AC PARAMETERS VS TEMPERATURE



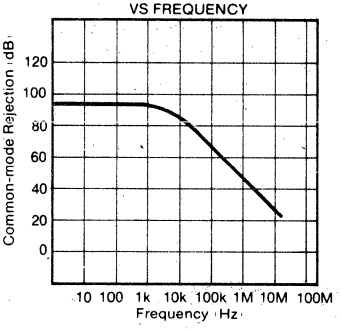
OPEN-LOOP GAIN VS FREQUENCY



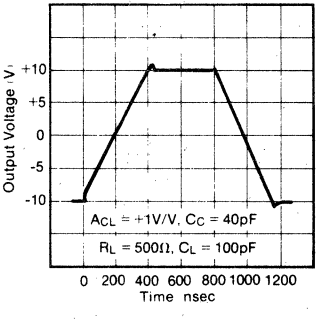
OPEN-LOOP PHASE SHIFT VS FREQUENCY



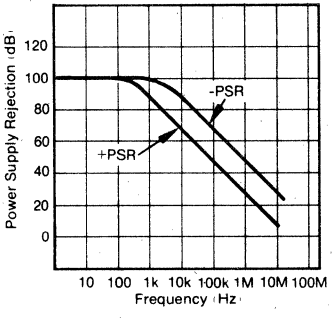
COMMON-MODE REJECTION VS FREQUENCY



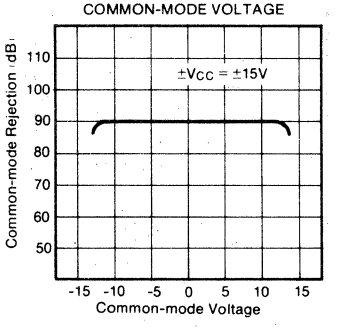
LARGE SIGNAL TRANSIENT RESPONSE



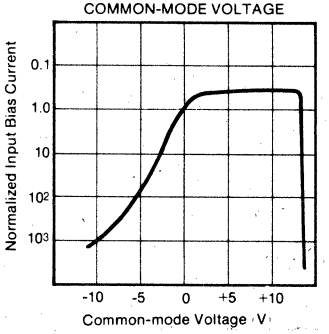
POWER SUPPLY REJECTION VS FREQUENCY



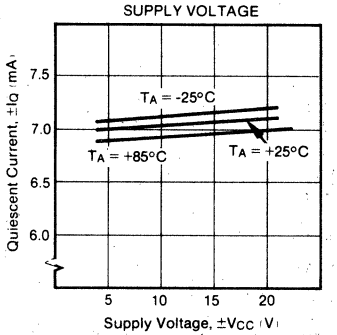
COMMON-MODE REJECTION VS COMMON-MODE VOLTAGE



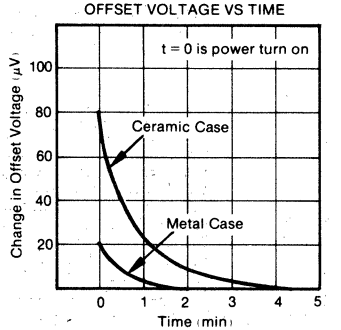
BIAS CURRENT VS COMMON-MODE VOLTAGE



QUIESCENT CURRENT VS SUPPLY VOLTAGE



OFFSET VOLTAGE VS TIME



APPLICATION INFORMATION

SLEW RATE

Slew rate is a large signal output parameter. It is primarily dependent on the compensation capacitor value (C_C) and has almost no dependence on changes in the closed loop gain or bandwidth. Typical values of slew rate versus compensation capacitor value are shown in the Typical Performance Curves. Decreasing the compensation capacitance increases the slew rate but reduces the frequency stability of the closed-loop circuit. Stray circuit capacitances may appear as added compensation to the amplifier. Therefore, stray capacitances should be minimized to avoid limiting slew rate performance.

BANDWIDTH

The closed-loop bandwidth is a small signal parameter. It is dependent on the open-loop frequency response of the op amp (which is determined by the value of the compensation capacitor, C_C) and the external closed-loop circuitry applied to the amplifier. Requirements for increased bandwidth and more frequency stability result in opposing constraints on the circuitry and generally the final selection of circuit values represents a compromise between the two needs.

SETTLING TIME

Settling time is defined as the total time required, measured from the input signal step, for the output to settle to within the specified error band around the final value. The error band is expressed as a percent of the full scale output voltage (10V) and the output transition is from 0V to +10V or 0V to -10V.

Settling time depends on slew rate (discussed above) and the time to reach the final value after the slew portion of the transition is complete. The latter is a function of the closed-loop bandwidth (discussed above) and the closed-loop gain. Thus, settling time is a function of both the open-loop frequency compensation (value of C_C) and the particular closed-loop circuit configuration. The best settling time is generally obtained at low gains.

COMPENSATION

The OPA605 uses external frequency compensation which allows the user to optimize slew rate, bandwidth and settling time for a particular application. As mentioned previously, compensation is normally a compromise between the desired speed and the necessary frequency stability - the higher the speed the lower the value of C_C and the less stable the circuit. Several of the Typical Performance Curves provide information to aid in the selection of the correct value of compensation capacitor. In addition, several typical circuits show recommended compensation in different applications.

The value of compensation capacitor required for stability is a function of the amount of negative feedback used in the particular application.

This is characterized as $1/\beta$, where β is the "feedback factor". $1/\beta$ is also equal to the gain in noninverting configurations (see figures 2 and 3).

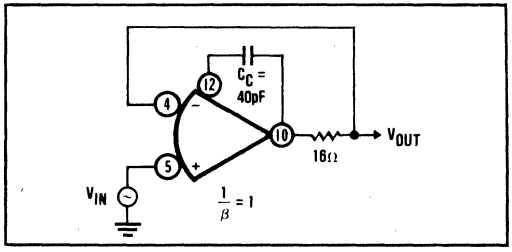


FIGURE 1. Unity Gain Follower.

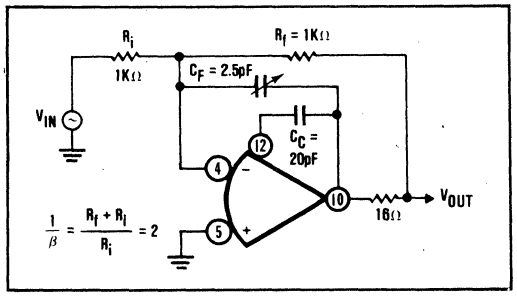


FIGURE 2. Unity Gain Inverting.

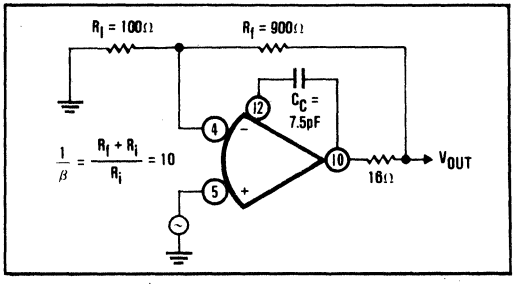


FIGURE 3. Gain of +10V.

The OPA605 may be compensated in either one of two ways. In the primary compensation method, C_C is connected between pins 10 and 12. Alternately the amplifier may be compensated with C_C' between pins 12 and 2 (see Connection Diagram). Normally the use of C_C is recommended. The use of C_C' will give lower output impedance at higher frequencies. This can be an advantage in some applications, but the effects are subtle and must be determined empirically.

Improved stability with larger capacitive loads may be obtained by connecting a small resistor (a value of 16Ω is recommended) in series with the output (see figures 2 through 4).

Flat high frequency closed-loop frequency response may be preserved and any high frequency peaking reduced by connecting a small capacitor (C_1 in the examples) in parallel with the feedback resistor. This capacitor will compensate for the high frequency closed-loop transfer function zero formed by the capacitance at the amplifier's input and the input and feedback resistors. C_1 may be a trimmer capacitor, a fixed capacitor or a planned printed circuit board capacitance. Typical values range from 0pF to 5pF.

WIRING PRECAUTIONS

Of all the wiring precautions, grounding is the most important. A good ground plane and good grounding practices should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns.

If point-to-point wiring is used (no ground plane), single point grounding should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins.

All printed circuit board conductors should be wide to provide low resistance, low inductance connections, and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitance should be minimized especially at high impedance nodes. Pin 4, the inverting input is especially sensitive to capacitance and all connections to that point must be short.

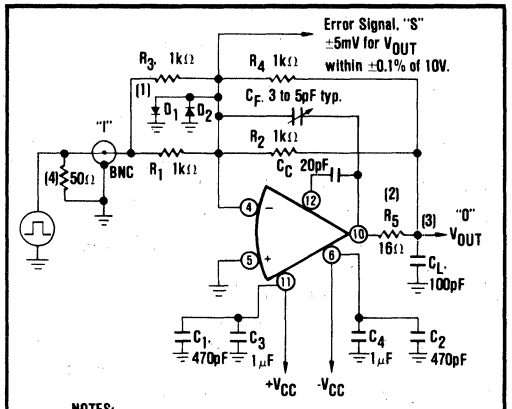


FIGURE 4. Dynamic Test Circuit.

Input and feedback resistors should be kept as small in value as practical; values less than 5.6kΩ are recommended. This will minimize performance limitations caused by the time constants formed by these resistors and circuit capacitances.

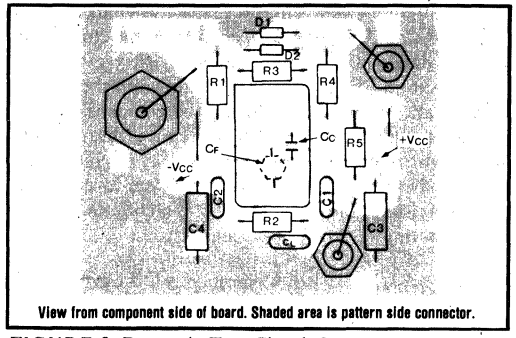


FIGURE 5. Dynamic Test Circuit Layout.

SHORT CIRCUIT PROTECTION

Short circuit protection to common is provided by internal current limiting resistors. (Output shorts to either supply can destroy the device.) The current limits may be increased by paralleling the internal resistors with external resistors, R_{EXT} connected between pins 7 and 10 and pins 8 and 10. The short-circuit current is then $I_{SC} \approx 0.05 + 0.6 / R_{EXT}$ (in amps). The power derating constraints must be observed when modifying the current limits. Details are given by the thermal model.

THERMAL MODEL

Figure 6 is the thermal model for the OPA605 where:

T_J = Junction temperature (output load)
T_J* = Junction temperature (no load)
T_C = Case temperature
T_A = Ambient temperature
θ_{CA} = Thermal resistance, case-to-ambient
P_{DQ} = Quiescent power dissipation
$|+V_{CC}|I_{QUIESCENT}| + |-V_{CC}|I_{QUIESCENT}|$
P_{DX} = Power dissipation in the output transistor
$= (V_{OUT} - V_{CC})\, I_{OUT}$

(In a complementary output stage only one output transistor is conducting current at a time.)

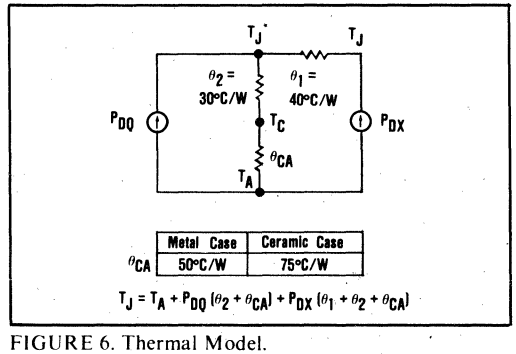


FIGURE 6. Thermal Model.

This model yields a Power Derating curve which is a function of P_{DQ}. See Typical Performance Curves.

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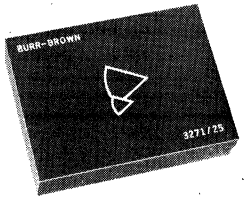


3271/25

High Voltage - Chopper-stabilized OPERATIONAL AMPLIFIERS

FEATURES

- LOW DRIFT
- OPERATES OVER WIDE SUPPLY RANGE
- HIGH OUTPUT VOLTAGE UP TO 110V
- SMALL, ENCAPSULATED PACKAGE
- ALL SOLID-STATE DESIGN

DESCRIPTION

The Model 3271/25 is a high voltage, chopper-stabilized operational amplifier in a small, encapsulated package. The module can be soldered directly on a circuit board, or may be plugged into a 1500MC connector for chassis mounting. The epoxy encapsulation insures ruggedness and resistance to environmental stresses, while the all-solid-state design, including self-contained MOSFET chopper and driver, guarantees reliable operation.

The amplifier is designed for operation on external supplies ranging anywhere from ±60VDC to ±120VDC. Output voltage range depends on the supply voltages. A low-noise chopping technique insures ultra-low DC drift as a function of temperature and time, while eliminating the noise spikes usually associated with chopper amplifiers.

The 3271/25 has input protection up to the value of supply voltage. The output stage may be shorted to common without damage to the amplifier. These features are particularly desirable when the amplifier is used in a patchable simulator.

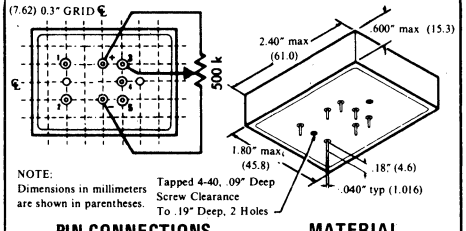
The open-loop gain exhibits a high frequency rolloff of approximately 6dB/octave, which insures stability at all feedback gain levels, or when driving capacitive loads. At the same time, the fast slewing rate and relatively wide bandwidth guarantee fast step response, with low overshoot, and low phase shift, when the 3271/25 is used as an inverter or summing amplifier.

APPLICATIONS

Typical areas of application for the 3271/25 are: integrators, summing amplifiers, inverters, sample/hold units, D/A converters, precision function generation, data amplifiers, and DC preamplifiers. The wide supply voltage tolerance and stable design enable the 3271/25 to be used as a replacement for vacuum tube amplifiers and older, solid-state amplifiers in simulators, data acquisition systems, and other systems where it is desired to increase reliability and improve performance at modest cost.

Because of the rugged construction techniques and use of silicon semiconductors, the 3271/25 is not limited to laboratory applications, but may also be used in relatively severe environments. Examples are shipboard, airborne, high vibration industrial, and remote monitoring stations.

MODEL 3271/25 ENCAPSULATED PACKAGE



NOTE:
Dimensions in millimeters are shown in parentheses.

PIN CONNECTIONS

Pin 1	Inverting Signal Input
Pin 2	Common
Pin 4	Signal Output
(+)	Positive Power
(-)	Negative Power
Pin 3	External Zero Control
Pin 5	Overload Signal

MATERIAL

Case - Black Epoxy
Pins - Gold-Flashed
Header - Alum., Hard Black Anodized
Mating Connector
Model 1500MC

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SPECIFICATIONS

Performance at 25°C and ±120 VDC supply unless otherwise noted.

* See discussion of output characteristics below.
Operating Temperature Range, -25°C to +85°C; Storage - 55°C to +100°C.

MODEL	RATED OUTPUT		DC GAIN	BANDWIDTH		SLEW RATE	INPUT OFFSET VOLTAGE					INPUT BIAS CURRENT				INPUT NOISE	OPEN LOOP IMPEDANCES		POWER SUPPLY	
	V_o	I_o		Unity Gain	Full Power		At +25°C	Over Range -25°C to +85°C	Versus Temp.	Versus Supply	Versus Time	At 25°C	Over Range -25°C to 85°C	Versus Temp.	Versus Supply	10Hz to 10kHz	Input	Output	Range	Quies. Current
	Volts min	mA min	dB min	MHz min	kHz min	V/μs min	μV max	μV max	μV/°C max	μV/V max	μV/mo typ	pA max	pA max	pA/°C max	pA/V max	μV rms max	MΩ typ	kΩ typ	Volts	mA max
3271/25	Supply less ±10V	±20	140	1.0	30*	20	±50	±110	1.0	1.0	+1	±80	±200	±2	±10	25 10(typ)	0.5	25	±60 to ±120	±20mA @±120VDC

OPEN-LOOP RESPONSE

The DC gain of the amplifier is typically 160dB because of the additional gain contributed by the DC chopper channel. This chopper channel gain rolls off at very-low frequency after which the amplifier gain is determined by the AC channel. The high frequency gain decreases at very nearly 6dB/octave. Figure 1 illustrates the open-loop gain response of a typical unit.

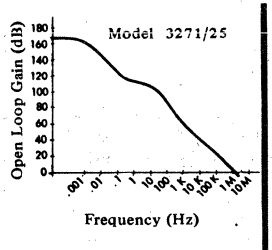

FIGURE 1. Open Loop Gain vs. Frequency.

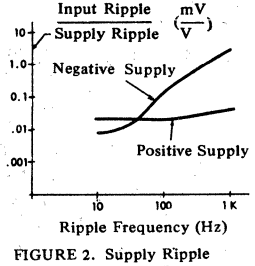

FIGURE 2. Supply Ripple Rejection vs. Frequency.

OUTPUT CHARACTERISTICS

The output stage of the amplifier is a balanced class B design which insures a minimum of quiescent drain from the power supply. The output current rating is +20mA and -20mA, regardless of the power supply level. Rated output voltage swing in either direction is 10V less than the supply voltage of the same polarity, whether equal or unequal values of supply voltage are used. For example, supply voltages of +75VDC and -90VDC could legitimately be used. The output voltage rated swing in the positive direction would be +(75-10) = +65V, while the negative rated output voltage would be -(90-10) = -80V. Full power frequency is measured with ±100V swing and ±20mA of output current, on ±120VDC supplies.

POWER SUPPLY CONSIDERATIONS

The 3271/25 will operate quite satisfactorily over a range of power supply voltages from ±60VDC to ±120VDC. In addition the supplies may have unequal values, so long as each is between 60V and 120V. Amplifier noise and drift will be minimized if the power supplies are balanced, well regulated, and have low output ripple. High frequency performance will be best, and crosstalk between adjacent amplifier channels will be least, if the supply impedance at the amplifier pins is low at all frequencies from DC to above 100kHz. If the supplies incorporate provisions for remote voltage sensing, the sense leads should be connected to the positive and negative supply buses as close as possible to the amplifier pins. The common lead should be as short as possible. Heavy gauge bus wire should be used if long supply and common leads are necessary. The addition of bypass capacitors from the supply bus to common, at the amplifier pins, will reduce the equivalent supply impedance and may be required if supply leads are long. Figure 2 illustrates the ripple induced at the amplifier input as a result of supply ripple.

INSTALLATION RECOMMENDATIONS

The input lead to the amplifier summing junction should be shielded to avoid pickup of spurious signals, particularly signals at the chopper drive frequency of 100Hz. In integrator applications, a shielded wire may be used to connect the feedback or integrating capacitor to the amplifier input terminals. The center conductor should be connected to the amplifier input, while the shield is connected to the amplifier output. The lead employed should have high insulation resistance to prevent capacitor discharge.

OFFSET VOLTAGE ZERO CONTROL

The Model 3271/25 operates with low DC input offset voltage, without the use of a zero control. An optional external zero control may be employed to accurately null the amplifier offset. This control is shown in the package drawing.

EXTERNAL OVERLOAD INDICATOR

Electrical overload signals may be detected in the chopper stabilizing channel and applied through pin 5 to an external overload indicating circuit. In the suggested circuit of Figure 3, D1 and D2 are silicon diodes; Q1 is an NPN silicon switching transistor while Q2 is a PNP silicon switch. Lamp DS1 is a 10V, 15mA indicator, G.E. #1869 or equivalent. The circuit may be adapted for latching operation by including the 100kΩ resistor and the reset switch shown in dotted lines. The indicator will then remain lighted, after the amplifier comes out of saturation, until the reset switch is closed.

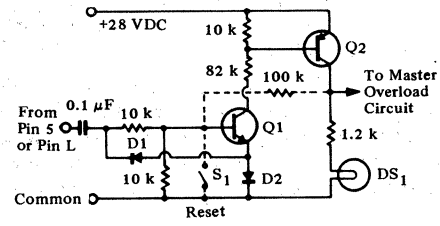

FIGURE 3. Overload Indicating Circuit.

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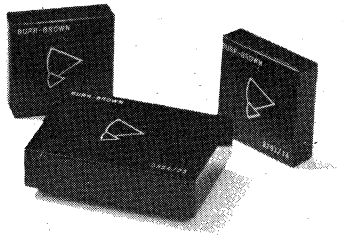

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3356

Chopper-Stabilized OPERATIONAL AMPLIFIERS

FEATURES

- DIFFERENTIAL INPUT OR SINGLE-ENDED
- VOLTAGE DRIFT AS LOW AS 0.1μV/°C
- CURRENT DRIFT AS LOW AS 0.5pA/°C

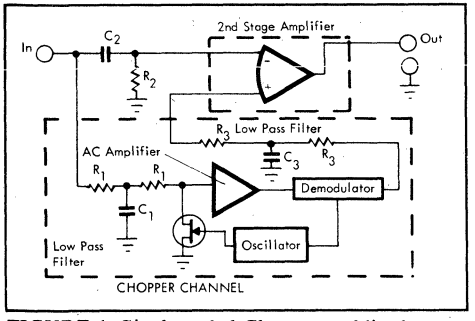

FIGURE 1. Single-ended Chopper-stablized Amplifier.

DESCRIPTION

Chopper-stabilized amplifiers achieve their ultra-low DC offset voltage and bias current by "chopping" the low frequency component of the input signal, amplifying this chopped signal in an AC amplifier and then demodulating the output of the AC amplifier. This output is then further amplified in a second stage of DC amplification. High frequency signals, which are filtered out at the input of the chopper channel, are coupled directly into the second stage amplifier. The net result of this technique is to reduce the DC offsets and drift of the second amplifier by a factor equal to the gain of the chopper channel. The AC amplifier introduces no offsets. Minor offsets and bias currents exist due to imperfect chopping, but these are extremely small.

The great strength of the chopper-stabilized amplifier is its insensitivity to component changes due to aging, temperature change, power supply variation or other environmental factors. Thus it is usually the best choice where both offset voltage and bias current must be small over long periods of time, or under significant environmental changes, and where external adjustment of offsets is undersirable or impossible. Both bias current and offset voltage can be nulled, if desired, by optional external controls. Figure 1 shows a simplified diagram of a single-ended chopper-stabilized op amp. Since the chopper channel, including switches and switch-driving oscillator, is built into the amplifier, only the DC power is supplied externally.

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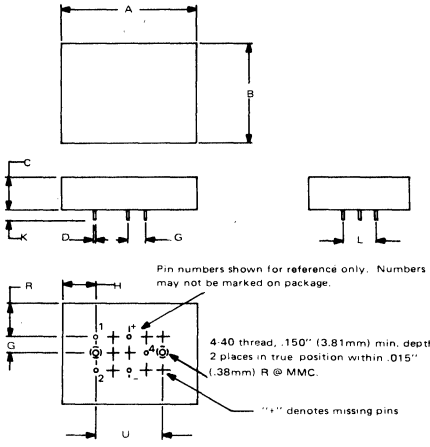
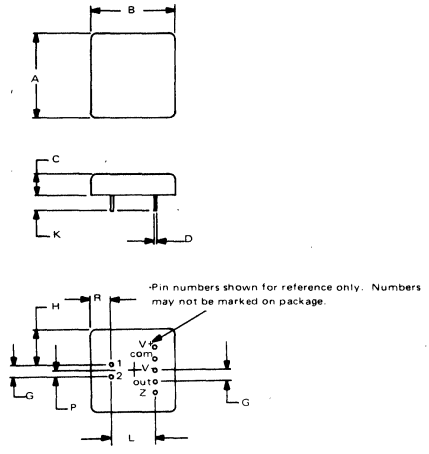
MECHANICAL SPECIFICATIONS

NOTE:
Leads in true position within .015"
(.38mm) R @ MMC at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.350	2.410	59.69	61.21
B	1.750	1.810	44.45	45.97
C	.550	.610	13.97	15.49
D	.035	.045	0.89	1.14
G	.300 BASIC		7.62 BASIC	
H	.550	.650	13.97	16.51
K	.170	.210	4.32	5.33
L	.600 BASIC		15.24 BASIC	
R	.550	.650	13.97	16.51
U	1.200 BASIC		30.48 BASIC	

NOTE:
Leads in true position within .015"
(.38mm) R @ MMC at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.450	1.510	36.83	38.35
B	1.450	1.510	36.83	38.35
C	.350	.410	8.89	10.41
D	.088	.042	0.97	1.07
G	.200 BASIC		5.08 BASIC	
H	.600	.700	15.24	17.78
K	.170	.350	4.32	8.89
L	.800 BASIC		20.32 BASIC	
P	.100 BASIC		2.54 BASIC	
R	.300	.400	7.62	10.16

ELECTRICAL SPECIFICATIONS

SPECIFICATIONS Typical at 25°C and rated supply unless otherwise noted.		MODELS	RATED OUTPUT		DC GAIN	BANDWIDTH		SLEW RATE	INPUT NOISE			
			V_o	I_o		Unity Gain	Full Power		Voltage		Current	
									0.01 Hz to 10 Hz	10 Hz to 10 kHz	0.01 Hz to 10 Hz	10 Hz to 10 kHz
			Volts min	mA min	dB min	MHz min	kHz min	V/μsec min	μV p-p	μV rms	pA p-p	pA rms
	Low Cost Inverting Only	3291/14 3292/14 3293/14	±10	±5	140	3 typ	100	6.0	2	3	10	80
	Differential Input	3354/25 3355/25 3356/25	±10	±5	140	3	100	6.0	8	2	30	400

DIFFERENTIAL INPUT TYPES

Until the introudction of Burr-Brown Models 3354/25, 3355/25, and 3356/25, high performance chopper-stabilized operational amplifiers were always single-ended. In other words, they could only be used in inverting circuits. Now, with these units, the same ultra-low drift and low offset characteristics can be obtained for noninverting amplifiers, differential feedback amplifiers, sample/hold circuits, peak/hold circuits and many other applications where the amplifier must function with both differential and common-mode signals. These amplifiers are ideal for amplification of low level signals since the low drift and noise result in low input signal uncertainty. In addition, the gain and common-mode rejection ratio are very high, insuring excellent linearity of feedback gain (CMR for common-mode voltage of ±10V is typically 140dB at DC and 100dB up to 100Hz).

When the amplifier is used as a buffer for high impedance signal sources, the $10^{13}\Omega$ common-mode input impedance results in negligible loading of the source. Also, this causes the small DC input bias current to be virtually independent of input voltage - a very desirable characteristic for buffering of the memory capacitor in sample/hold and peak/hold circuits.

In general, these differential chopper-stabilized units can be used anywhere that a differential op amp would normally be used - but where both voltage and current drift must be very low.

LOW COST SINGLE-ENDED TYPES

For most inverting applications, Models 3291/14, 3292/14, or 3293/14 will be found to be the best choice. These units represent the state-of-the-art in single-ended chopper-stabilized amplifiers, featuring the lowest drift, lowest noise, lowest profile (1.5" x 1.5" x 0.4"), and the lowest prices available. Frequency response and slew rate are more than adequate for most applications.

Typical applications for these single-ended amplifiers are integrators, precision reference sources, D/A and A/D converters of high accuracy, precision comparators, current to voltage converters and high gain amplifiers for low level, low impedance signal sources.

Where a differential input is not required, these are the units to use for those applications where both low voltage drift and low bias current drift are required.

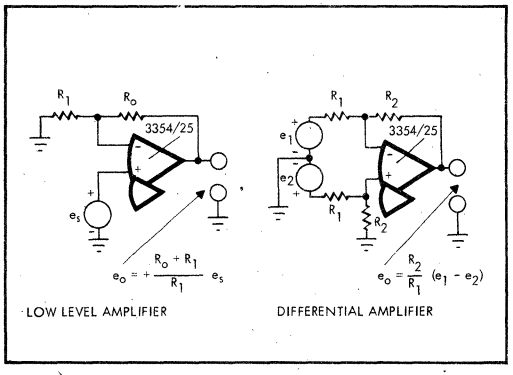


FIGURE 2. Typical Applications of Differential Chopper-stabilized Amplifiers.

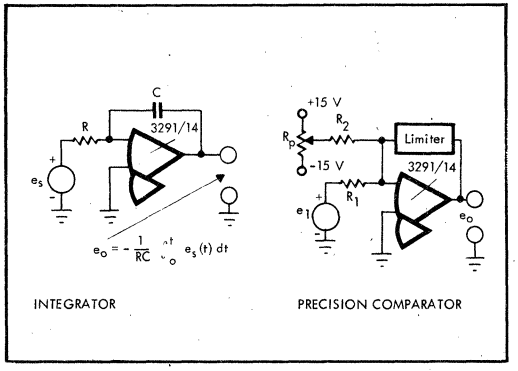


FIGURE 3. Typical Applications of Single-ended Chopper-stabilized Amplifiers.

INPUT OFFSET VOLTAGE		INPUT VOLTAGE DRIFT			INPUT BIAS CURRENT		BIAS CURRENT DRIFT		OPEN LOOP IMPEDANCES			POWER SUPPLY		
At 25°C	Over Range -25°C to +85°C	Versus Temp. -25°C to +85°C	Versus Supply	Versus Time	At 25°C	Over Range -25°C to +85°C	Versus Temp. -25°C to +85°C	Versus Supply	Input Diff.	Input CM	Output	Nom. Rated	Range	Quies. Current
μV max	μV max	μV/°C max	μV/V	μV/day	pA max	pA max	pA/°C max	pA/V	MΩ	Ω	kΩ	Volts	Volts	mA max
±20	±26	±0.1			±50	±80	±0.5							
±50	±68	±0.3	±5	1 μV/mo	±50	±110	±1.0	±10	0.5	-	1.5	±15	±12 to ±18	±10
±100	±160	±1.0			±100	±220	±2.0							
±30	±36	±0.1			±20									
±50	±80	±0.25	±10	1 μV/mo	±50	doubles / +10°C		±1	1.0	10^{13}Ω	2.0	±15	±12 to ±18	±10
±100	±160	±1.0			±50									

INSTALLATION, OPERATION AND APPLICATIONS INFORMATION

DRIFT CONSIDERATIONS

The best overall drift performance of an amplifier circuit will be achieved by minimizing impedance levels in the feedback network. The effect on output offset and drift of feedback and source impedances is illustrated in Figure 4. For very large resistances, input bias current becomes the major contributor to output voltage offset and drift. Where high input impedance and high gain are needed simultaneously, it may, therefore, not be feasible to use a single-ended inverting chopper-stabilized amplifier, because of this bias current factor. The differential input chopper-stabilized amplifier, used in the noninverting mode, then becomes the best choice. This allows the use of low impedance feedback networks while still retaining very high input impedance to prevent source loading. Note that input bias current doubles (approximately) for every +10°C temperature rise for these units.

The circuit of Figure 5 illustrates the effects of offset voltage and input bias current on integrator performance. Both parameters cause output errors which increase at a constant rate as a function of time. Additional offset voltage and input bias current caused by temperature drift will cause the output rate errors to increase with temperature. Note that the output rate error due to bias current diminishes as capacitance, C_F, increases. Usually, however, there is not much point in going beyond 10μF because of capacitor dielectric leakage. Also, as C_F is increased, R_i must decrease to maintain a given $R_i C_F$ product and there will usually be a lower limit on desirable values of R_i, since this represents the input impedance of the integrator. Also, R_i determines the amount of input and feedback current flowing for a given input level. The amplifier, and the signal source, must be capable of supplying this current. Thus a compromise set of R_i and C_F can usually be reached which takes into account these factors.

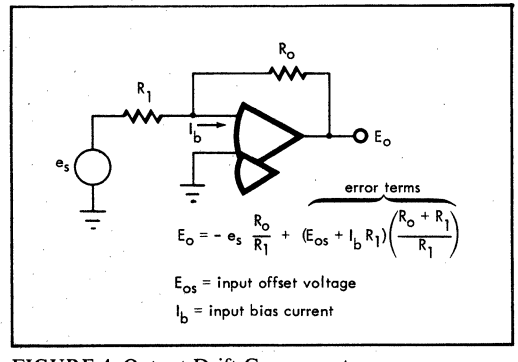


FIGURE 4. Output Drift Components.

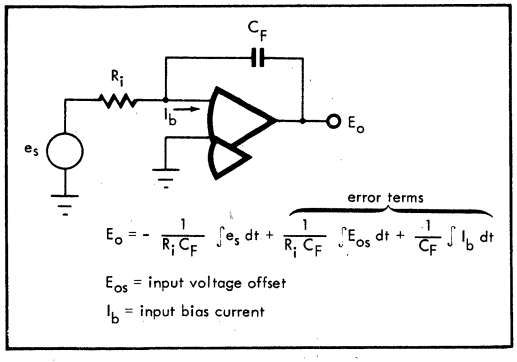


FIGURE 5. Integrator Errors Due to Offset Voltage and Bias Current.

NOISE CONSIDERATIONS

Because of the extremely low DC offset and DC drift associated with the chopper-stabilized amplifier, noise is often found to be the remaining limit on signal resolution. Thus it is desirable to design the feedback networks and external wiring to minimize the total circuit noise. This includes the proper grounding and noise decoupling as described under Wiring Recommendations. In addition it is desirable to minimize the levels of feedback impedance as a means of reducing noise "pickup" and the effects of amplifier current noise. When the full bandwidth of the amplifier is not required, it is recommended that a feedback capacitor be used to

limit the overall bandwidth and eliminate as much high frequency noise as possible.

When one of the differential input, chopper-stabilized amplifiers is used with a high impedance source, the input current noise will be the limiting factor on signal resolution. For source impedances of 1kΩ or greater it is recommended that a compensating resistance, R_C, be inserted in series with the inverting input (see Figure 6). This resistor will minimize the effect of current noise at the chopper frequency.

Shielding of feedback components is desirable and may be necessary in electrically noisy environments. Use of shielded wire for summing junction leads is also

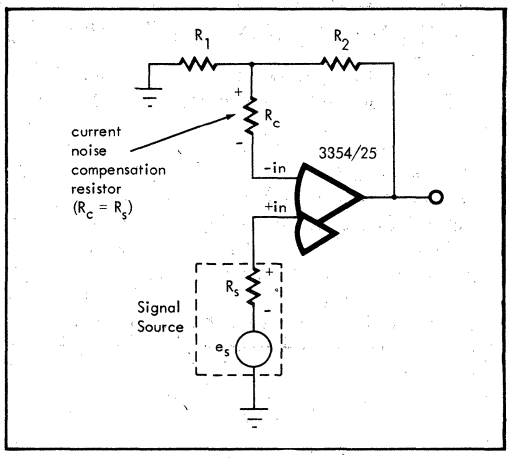


FIGURE 6. Use of a Current Noise Compensating Resistor with Differential Chopper-stabilized Operational Amplifier.

recommended in high noise environments. The shield should then be connected to the output terminal of the amplifier.

POWER SUPPLY REQUIREMENTS

The amplifiers described in this brochure are specified for operation on the rated supply voltages (±1%). They will operate with some degradation over the specified range

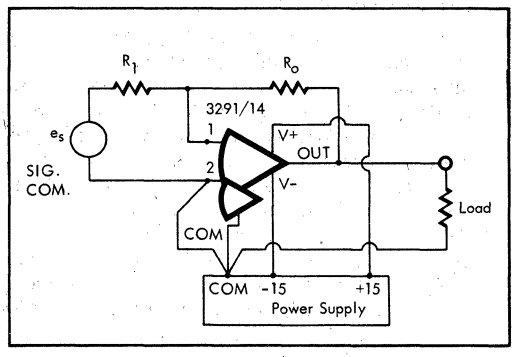


FIGURE 7. Proper Grounding of Models 3291/14, 3292/14 and 3293/14.

of supply voltages (±12VDC to ±18VDC for ±10V amplifiers).

Supply drain current is specified under quiescent conditions (no output current from the amplifier). When the amplifier is supplying current to a load, this current must be added to the quiescent current of the proper supply to determine total supply current.

WIRING RECOMMENDATIONS

Models 3291/14, 3292/14 and 3293/14 are designed with separate pins for power supply command and signal common. The diagram of Figure 7 illustrates the proper grounding techniques for these amplifiers. It is important that the signal common and power common leads be connected only at pin 2 of the amplifier. A separate lead is required from the power supply common to the COM pin of the amplifier.

Figure 8 illustrates proper grounding for noninverting circuits using the differential amplifiers (3354/25, 3355/25, 3356/25).

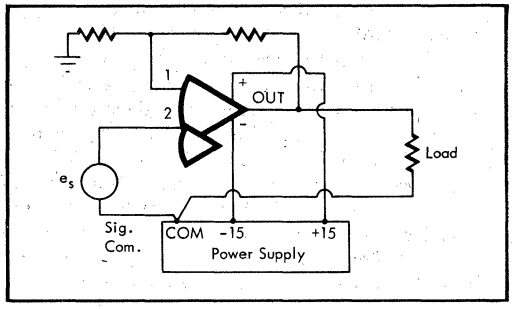


FIGURE 8. Proper Grounding of Differential Models (Noninverting Mode).

OVERLOAD CHARACTERISTICS

Because the chopper-stabilized amplifier consists of two amplifying channels, one fast and the other very slow, the overload behavior is different from that of nonchopper-stabilized op amps. If the chopper channel becomes overloaded due to a large error voltage at the summing junction, recovery may require as much as a few seconds. There are three ways in which such overloads may occur - output voltage saturation, output current limiting, and transient overload induced when power supply voltages are applied. The first of these three possible conditions arises when the amplifier output voltage is driven to its limits. When the output voltage can no longer follow the input signal, the summing junction voltage rises from its virtual ground potential. This relatively large potential is then amplified by the high gain of the chopper channel to a level of several volts, a much larger value than is encountered in the chopper channel during normal operation. Because of the very large time constants of the chopper channel filters, decay of this overvoltage, and consequently amplifier recovery, may take several seconds after removal of the overdrive signal. When the

amplifier reaches one of its output current limits, under the proper combination of loading and signal, a condition much like that of voltage saturation occurs. The output voltage fails to follow the input signal and chopper channel overload occurs.

In general, the amplifier will recover quickly from transient or short duration overloads since the relatively slow chopper channel will not become charged to high levels.

Overloads due to output voltage limiting (not current limiting) may be prevented by use of a feedback limiter such as that of Figure 9. Because the amplifier summing junction is always held at virtual ground, even when the limiter is active, the chopper channel does not overload and recovery from limiting is very rapid (1.0μsec or less is typical). The limits must, of course, be set below the output saturation levels of the amplifier itself.

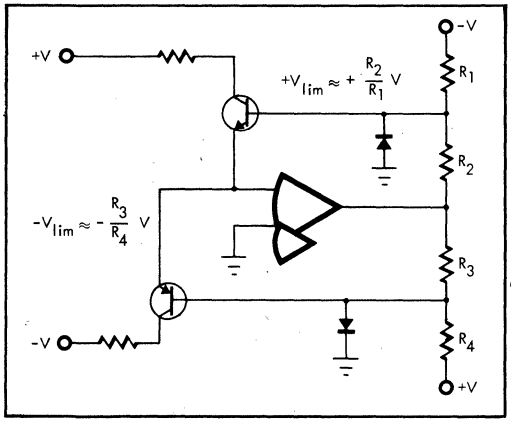


FIGURE 9. Feedback Limiter Circuit.

Overloads which occur during the application of DC power to the amplifier are a result of transient imbalances within the circuit. Recovery time from this type of overload is a function of circuit design. Where rapid recovery from such initial overloads is important, Models 3354/25, 3355/25 and 3356/25 are the best choices. These amplifiers typically recover to specified operation in less than one second. They recover equally fast from extended overload due to signal overdrive conditions for simple resistive feedback.

DC NULLING TECHNIQUES

The proper connections for nulling of the DC offset voltage are shown in the Mechanical Specifications. Note that in all cases these offset controls are optional and need not be used if the small offset voltage of the amplifier can be tolerated. The differential chopper-stabilized models (3354/25, 3355/25 and 3356/25) can be nulled as shown in Figure 10. However, the inherent offset voltage of these amplifiers is acceptably low (typically less than 10μV) for many applications and the null control may be unnecessary.

The input current of the amplifier may be nulled as in Figure 11 (for inverting circuits).

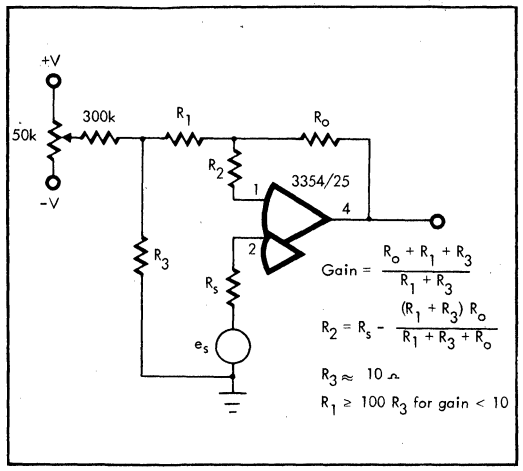


FIGURE 10. Offset Voltage Adjustment for Noninverting Circuits.

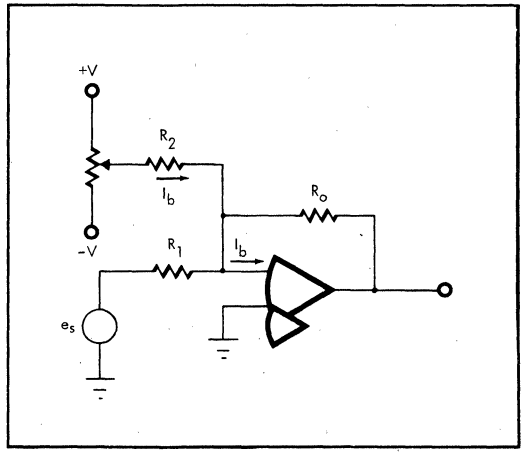


FIGURE 11. Null Adjustment of Input Current.

INPUT/OUTPUT PROTECTION

The various amplifiers described here are designed such that any voltage up to the value of power supply voltage may be applied directly to the amplifier input pin without damage to the amplifier.

Output stages of the amplifiers are current limited to prevent damage should the output pin be shorted to common. Permanent damage to the amplifier may occur, however, if the output pin is connected to a voltage of the same order of magnitude as the supply voltages.

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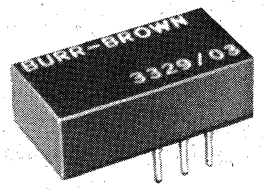
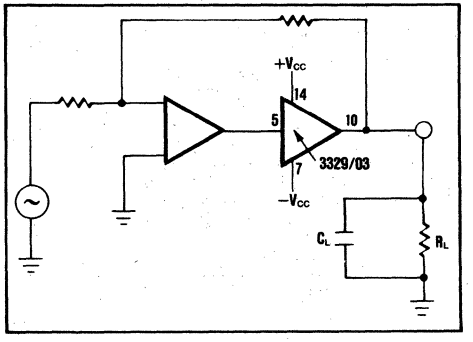


3329/03

HYBRID IC POWER BOOSTER

FEATURES

- ±100mA OUTPUT
- SHORT CIRCUIT PROTECTED
- NO HEAT SINK REQUIRED
- DUAL-IN-LINE PACKAGE



DESCRIPTION

The Model 3329/03 is a power booster amplifier designed for use in cascade with IC or discrete component operational amplifiers inside the feedback loop. Current output of up to ±100mA at ±10VDC is provided without the need for a heat sink. The unit is short circuit protected over the full temperature range or -40°C to +85°C. Output current is limited to ±15mA by internal circuitry. No external components are required. The high full power frequency (1MHz) and small signal bandwidth of 5MHz insure that the unit will not degrade the frequency response of the operational amplifier used.

The class B output stage provides high output current with a minimum of quiescent power supply drain. The low open loop output impedance (10Ω) insures stable operation with large capacitive loads, and virtually eliminates the closed loop gain loading effect of low impedance loads such as 50Ω terminated lines. Because of the 10kΩ input impedance of the booster, the current output requirements of the operational amplifier are minimal.

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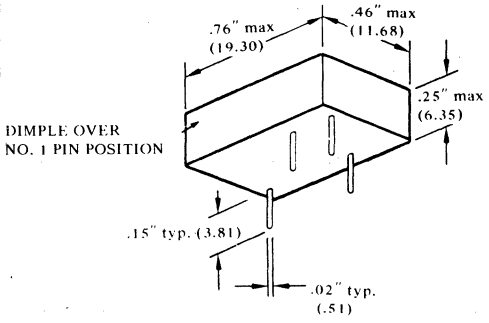
MECHANICAL SPECIFICATIONS

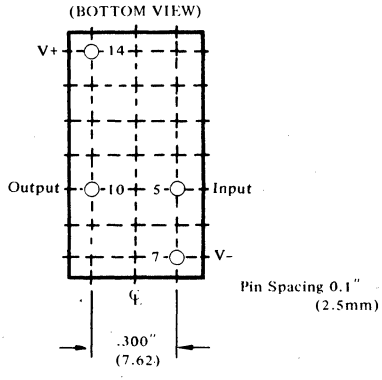
Dimensions in millimeters are shown in parentheses.

PHYSICAL DIMENSIONS



Weight: 0.12 Oz. (3.40 grams) max.
Material: Black Epoxy
Pins: Tin plated nickel
Connector: Fits any commercial dual-in-line connector

CONNECTION DIAGRAM



APPLICATIONS INFORMATION

Power Supply Requirements

The Model 3329/03 is designed to operate over a power supply range of ±12 VDC to ±18 VDC. Output voltage swing is guaranteed to be in excess of ±10 volts at full load, when operating on supplies of ±15 VDC. For other values of supply voltage, the output swing varies in proportion.

Gain and Stability

The voltage gain of the 3329/03 is approximately 1.0. The accuracy of this gain is relatively unimportant, since the booster is used inside the feedback loop of an operational amplifier. The booster by itself is completely stable under all conditions of capacitive loading. Because of it's very low output impedance, the 3329/03 tends to isolate the associated operational amplifier from the effects of capacitive load.

The input impedance of the booster is approximately equal to 100 x (load impedance). Thus, for a 100 ohm load, the input impedance is approximately 10 k ohms. The effective output impedance of the booster is approximately equal to the output impedance of the operational amplifier, divided by 100.

For most general purpose operational amplifiers the dynamic output impedance is on the order of 1 kΩ. When a low impedance load (e.g. 50Ω) is being driven, a severe loading effect occurs which greatly reduces the effective open loop gain and bandwidth. Effectively, the unloaded gain and bandwidth of the operational amplifier would be multipled by the loading factor $\frac{50}{1050} \approx .05$, if the load is 50Ω.

When the 3329/03 booster is used, however, the effective open loop output impedance is 10Ω. The loading factor now is $\frac{50}{60} = .866$, and the gain and bandwidth are reduced only slightly by this loading.

Input and Output Protection

The output stage of the 3329/03 is current limited to insure survival of the booster if the output is shunted to ground. The unit is safe even under continuous short circuit at +85°C. No heat sink is required.

The input circuitry will withstand overvoltage up to the value of supply voltage.

Temperature Range

The 3329/03 will operate over the -40°C to +85°C temperature range. Storage temperature range may vary from -55°C to +100°C.

3329/03 POWER BOOSTER SPECIFICATIONS

Rated Output		Full Power Response	-3dB Response	Input Signal Range	Input Offset Voltage	Input Impedance	Output Impedance	Power Supply Requirements		
V_O Volts (min)	I_O mA (min)	kHz (min)	MHz (min)	Volts (min)	mVolts (max)	kΩ (typ.)	Ω (typ.)	Nom. Rated Volts	Range Volts	Quies. Current mA (max)
±10	±100	1000	5	±10	±50	10	10	±15	±12 to ±18	±15

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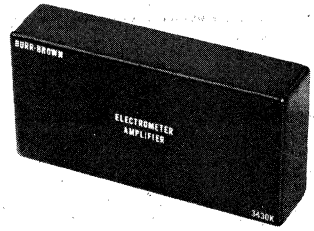

3430
3431

ELECTROMETER AMPLIFIERS

FEATURES

- ULTRA-LOW INPUT CURRENT, .01pA, max
- LOW INPUT CURRENT NOISE, .001pA, p-p
- HIGH INPUT IMPEDANCE, $10^{14}\Omega$
- INVERTING OR NONINVERTING OPERATION

DESCRIPTION

Models 3430 and 3431 are designed to minimize input bias current and input noise current through the use of a varactor diode bridge technique. Models 3430J and 3430K are intended for meaurement of very-low-level currents, long-term integrators and analog memory applications. The 3431J and 3431K are designed for measurement of sub-millivolt signals from very high source impedances such as pH and other electrochemical cells, and in long-term track/hold applications where charge stored on a capacitor is the input signal source.

The varactor bridge technique uses the voltage variable capacitance and extremely low leakage current of the two zero-biased varactor diodes to achieve input bias current and input current noise 10 to 100 times less than that of FET amplifiers.

The 3430 and 3431 out-perform amplifiers that use electrometer tubes or MOSFET input stages. Primary areas of advantage over these other devices are in voltage drift, common-mode rejection, and lower cost. An additional advantage over MOSFET's is the inherent input protection of the varactor bridge input configuration.

Operation of the 3430 and 3431 are simply explained. The amplifier input voltage, e_{in}, varies the capacitance of the varactor diodes, causing a bridge unbalance and developing a bridge output signal at the carrier frequency. This carrier frequency signal, which is proportional in amplitude to the input signal level, is amplified by the low-noise AC amplifier, phase-sensitivity demodulated to restore correct polarity and filtered to eliminate the carrier components. Additional amplification is provided by a conventional DC amplifier stage. The output is equal to the product of input signal and open-loop gain.

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SPECIFICATIONS

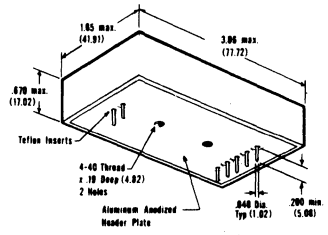
(Typical @ 25°C and ±15 VDC unless otherwise noted)

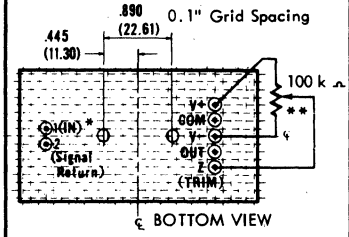
MODEL	3430J/K	3431J/K
OPEN LOOP GAIN		*
2k Ω load, min.	100 dB	
RATED OUTPUT		*
Voltage, min	±10 V	
Current, min	±5 mA	
Load Capacitance	0 to .01 μF	
Output Impedance @ DC	2 k Ω	
FREQUENCY RESPONSE		
Unity gain, small signal	2 kHz	*
Full power response, min	7 Hz	
Slewing rate, min	0.4 V/ms	
Overload recovery	10 ms	
INPUT OFFSET VOLTAGE		
External trim pot	100 k Ω	*
Avg. vs. temp (10°C to 70°C) max	±30 μV/°C (J) ±10 μV/°C (K)	±30 μV/°C (J) ±10 μV/°C (K)
vs. supply voltage	±500 μV/V	*
vs. time	±100 μV/mo.	*
Warm-up drift	75 μV (15 min)	*
INPUT BIAS CURRENT		
Initial bias, 25°C, max		
Inverting input	±0.01 pA	±1 nA
Non-inverting input	±1 nA	±0.01 pA
Avg. vs. temp (signal input only)**	x2/10°C	*
vs. supply voltage (signal input only)	±0.01 pA/V	*
INPUT IMPEDANCE		
Differential	-	3×10^{11} Ω ‖ 30 pF
Inverting input (to common)	3×10^{11} Ω ‖ 30 pF	10^9 Ω ‖ .02 μF
Non-inverting input (to common)	-	10^{14} Ω ‖ 35 pF
INPUT NOISE		*
Voltage, .01 to 1 Hz, p-p	10 μV	
1 to 100 Hz rms	5 μV	
Current, .01 to 1 Hz, p-p	.001 pA	
1 to 100 Hz, rms	.002 pA	
COMMON MODE CHARACTERISTICS		
Max safe input voltage	±300V	±300V
Max common mode	NA	±200V
Common mode rejection @ ±25V	NA	100 dB
POWER SUPPLY		*
Voltage, rated specification	±15V	
Voltage, operating	±(12 to 18)V	
Current, quiescent	+15, -6 mA	
TEMPERATURE RANGE		*
Operating, rated specifications	0° to +70°C	
Operating, derated specifications	-25° to +85°C	
Storage	-55° to +85°C	
MECHANICAL		*
Case style	28	
Mating connector	2800MC	
Weight	6 oz.	

* Specification same as 3430.
** Negative input for Model 3430; positive input for Model 3431.

PACKAGE CONFIGURATION

NOTE: Dimensions in millimeters are shown in parentheses.

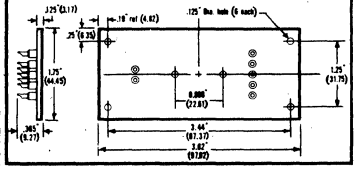




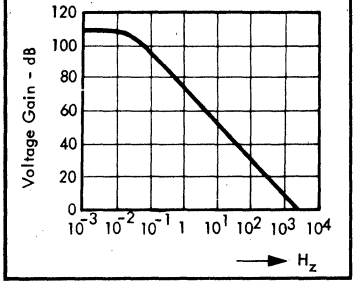
*-IN, 3430 **Optional Offset Adjust
+IN, 3431

PINS - Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATERIAL - Aluminum Case
Aluminum Anodized Header
WEIGHT - 6 oz max (170)

2800MC



OPEN LOOP FREQUENCY RESPONSE



BURR-BROWN®

3500 SERIES

Low Bias Current OPERATIONAL AMPLIFIERS

FEATURES

- LOW BIAS CURRENT, ±15nA, max
- LOW DRIFT, ±1μV/°C, max
- LOW NOISE, 1.4μV, p-p
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- REPLACES 741 TYPE AMPLIFIERS

APPLICATIONS

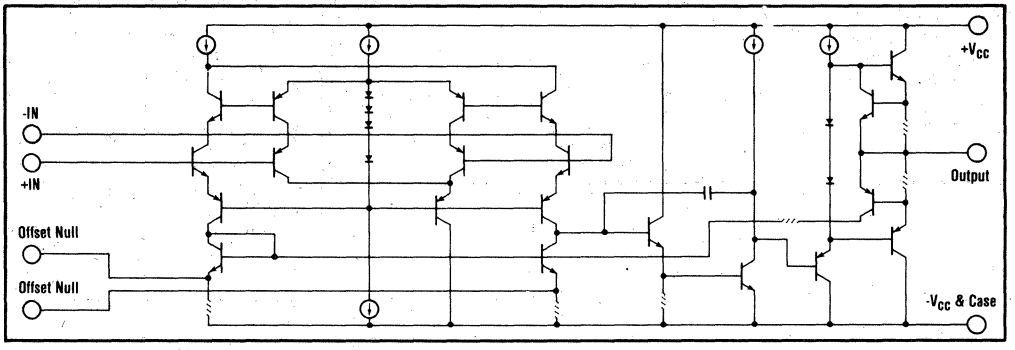
- GENERAL PURPOSE AMPLIFIER
- ANALOG COMPUTATION
- PRECISION BUFFER
- LOW DRIFT INTEGRATOR
- BRIDGE AMPLIFIER
- STABLE REFERENCE CIRCUITS

DESCRIPTION

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high impedance, both differential and common-mode. The amplifier maintains internal current levels essentially constant over the full range of power supply voltages. Thus the offset voltage and drift remain low for all combinations of supply voltage.

Both military and industrial temperature range versions are offered. Drift selected units are offered at ±1, ±3, ±5, ±10, and ±20μV/°C, max. The 3500 is also a low noise IC op amp, as illustrated by the typical performance curves. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated for unconditional stability for all feedback configurations, even with capacitive loads. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30 volts, thus the amplifier can be used as a sensitive comparator. The output stage is internally current-limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.



Equivalent Circuit Diagram

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL	3500 SERIES			
	3500A 3500R	3500B 3500S	3500C 3500T	3500E
OPEN-LOOP GAIN, DC, no load, min	93dB	•	•	100dB**
RATED OUTPUT				
Voltage, min	±10V	•	•	•
Current, min	±10mA	•	•	•
Output Impedance	2kΩ	•	•	1kΩ
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1.5MHz	•	•	•
Full Power Sine Wave, min	10kHz	12kHz	15kHz	12kHz
Slew Rate, min	0.6V/μsec	0.8V/μsec	1.0V/μsec	0.8V/μsec
INPUT OFFSET VOLTAGE				
Initial Offset at 25°C, max	±5mV	±2mV	±1mV±500μV	±500μV
Avg. vs Temp. (-25°C to +85°C) max	±20μV/°C (A)	±5μV/°C (B)	±3μV/°C (C)	+1μV/°C
(-55°C to +125°C) max	±20μV/°C (R)	±10μV/°C (S)	±5μV/°C (T)	--
vs Supply Voltage	±40μV/V	•	•	•
vs Time	±2μV/day	•	•	±5μV/mo
INPUT BIAS CURRENT				
At 25°C (either input), max	±30nA	±20nA	±15nA	±50nA
Avg. vs Temp. (-25°C to +85°C) max	±1.0nA/°C (A)	±0.5nA/°C (B)	±0.3nA/°C (C)	±0.5nA/°C
(-55°C to +125°C) max	±1.5nA/°C (R)	±1.0nA/°C (S)	±0.5nA/°C (T)	--
vs Supply Voltage	±0.2nA/V	•	•	•
INPUT DIFFERENCE CURRENT				
At 25°C	±15nA	±10nA	±7nA	±30nA, max
Avg. vs Temp. (-25°C to +85°C)	±0.5nA/°C (A)	±0.2nA/°C (B)	±0.1nA/°C (C)	±0.3nA/°C, max
(-55°C to +125°C)	±0.7nA/°C (R)	±0.5nA/°C (S)	±0.2nA/°C (T)	--
vs Supply Voltage	±0.1nA/V	•	•	•
INPUT IMPEDANCE				
Differential	$10^7\Omega$ || 3pF	•	•	•
Common Mode	$5 \times 10^9\Omega$ || 3pF	•	•	•
INPUT NOISE				
Voltage, 0.01Hz to 10Hz, p-p	2.0μV	•	•	•
10Hz to 10kHz, rms	1.4μV	•	•	•
Current, 0.01Hz, p-p	200pA	•	•	•
10Hz to 10kHz, rms	35pA	•	•	•
INPUT VOLTAGE RANGE				
Common-mode Voltage, min	±11V	•	•	•
Common-mode Rejection at ±10V	100dB	•	•	•
Maximum Safe Input Voltage***	±V_{CC}	•	•	•
POWER SUPPLY				
Voltage, rated specification	±15V	•	•	•
Operating Range	±3V to ±20V	•	•	•
Current, quiescent, max	±3.5mA	•	•	•
TEMPERATURE				
Operating, Rated Specs A, B, C	-25°C to +85°C	•	•	•
R, S, T	-55°C to +125°C	•	•	--
Storage	-65°C to +150°C	•	•	•

*Specifications the same as the 3500A or 3500R. **Typical.

***If signal voltage is applied to the input in the absence of power supply voltage, series resistance should be used to limit input current to 20mA.

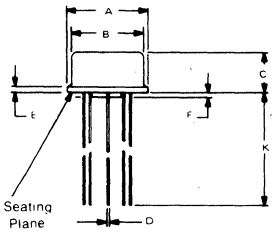
ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	-65° C to +150° C
Operating Temperature Range	-55° C to +125° C
Lead Temperature (Soldering, 10 seconds	+300° C
Output Short Circuit Duration(3)	Continuous
Junction Temperature	+150° C

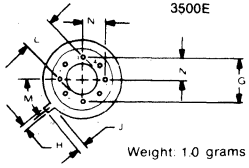
NOTES:
1. Package must be derated based on: θ_{JC} = 45°C/W or θ_{JA} = 150°C/W.
2. For supply voltages less than ±20VDC the absolute maximum input voltage is equal to the supply voltage
3. Short circuit may be to power supply common only. Rating applies to +85°C ambient.

MECHANICAL

TO-99



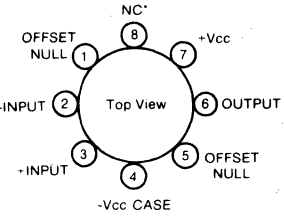
Order Number
3500A
3500B
3500C
3500R
3500S
3500T
3500E



Weight: 1.0 grams

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500		12 7	
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

PIN CONFIGURATION

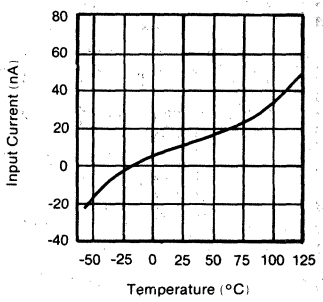


*No Internal Connection

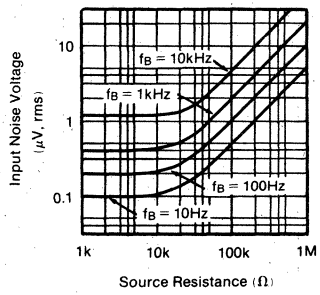
TYPICAL PERFORMANCE CURVES

(At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise specified)

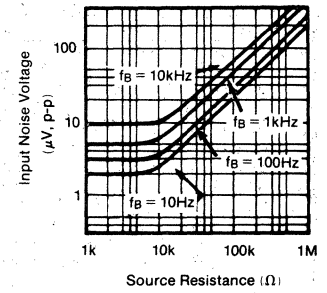
INPUT BIAS CURRENT VS TEMPERATURE



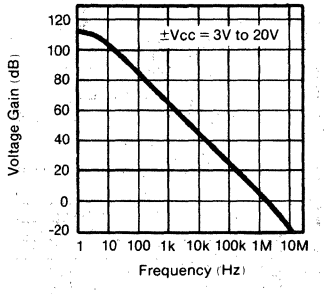
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



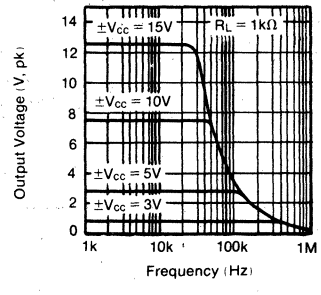
P-P INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



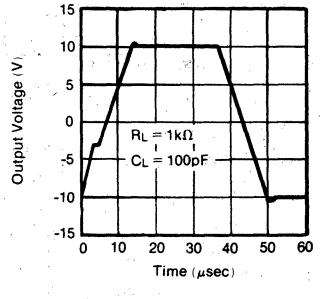
OPEN-LOOP FREQUENCY RESPONSE



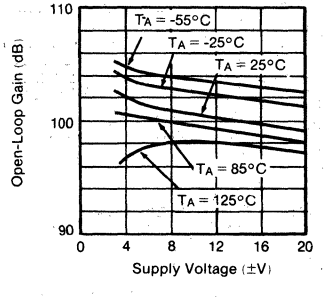
OUTPUT VOLTAGE VS FREQUENCY



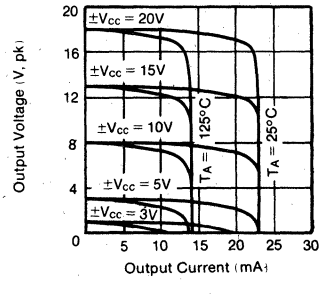
VOLTAGE FOLLOWER STEP RESPONSE



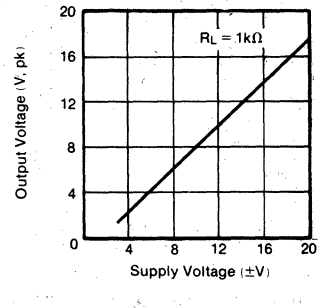
VOLTAGE GAIN VS SUPPLY VOLTAGE



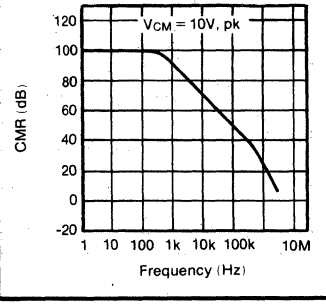
OUTPUT VOLTAGE VS OUTPUT CURRENT



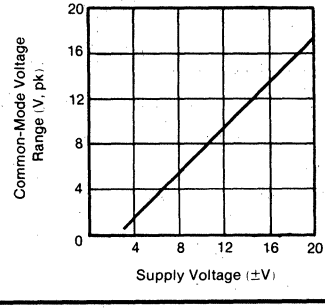
OUTPUT VOLTAGE VS SUPPLY VOLTAGE



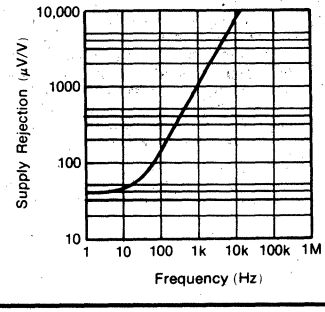
COMMON-MODE REJECTION VS FREQUENCY



COMMON-MODE RANGE VS SUPPLY VOLTAGE



POWER SUPPLY REJECTION VS FREQUENCY



APPLICATIONS INFORMATION

OFFSET ADJUSTMENT

The input offset voltage of the Model 3500 may be adjusted to zero by connecting a 50kΩ potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 1a). This provides an adjustment range of approximately ±10mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the 3500 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3μV/°C change of drift for each 1.0mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers, such as the 3500C and 3500T, this effect must be considered. By use of a transistor as in Figure 1 the effect of offset adjustment on drift can be substantially reduced (by approximately a factor of six).

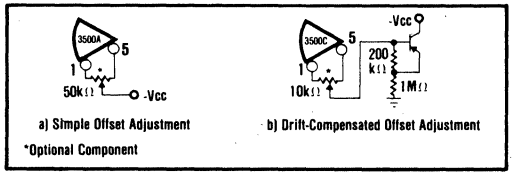


FIGURE 1. Offset Adjustment Techniques.

BIAS CURRENT EFFECTS

Input bias current of the amplifier creates additional offset voltages by flowing in the impedances of the signal source and the feedback network. Although the bias currents of the 3500 are quite small, their effects may be appreciable when these impedances are large. The bias currents at the two inputs tend to be equal and the difference current smaller than either. Thus equalizing the resistance from each input to common, as in Figure 2, is an effective means of reducing DC offset due to bias current.

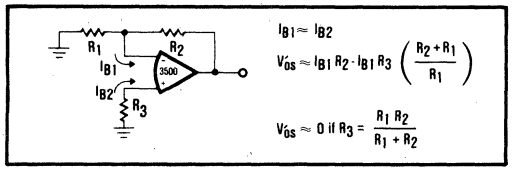


FIGURE 2. Minimization of Bias Current Effects.

OPERATION ON A SINGLE SUPPLY

Although virtually any op amp can be operated on a single supply if input and output voltage limitations are observed, the Model 3500 is particularly suitable for such use. Its wide supply range of ±3VDC to ±20VDC translates to a single supply operating range of 6VDC to 40VDC, plus or minus. Two possible modes of operation on a single supply are shown in Figure 3. The following conditions must be observed to keep the amplifier within its linear region of operation.

1) $+2 < V_O < (V_{CC} - 2)$

2) $+3 < V_{IN} < (V_{CC} - 3)$, Figure 3b

When operating on a single supply ($+V_{CC}$), shorting the output to common is equivalent to a short to supply and the internal power dissipation is approximately twice that which occurs for a short to common with balanced supplies of $\pm \frac{V_{CC}}{2}$. This dissipation may exceed safe limits for single supply voltages greater than 20V and must be prevented by use of a series limiting resistor or other device, if short circuit protection is desired.

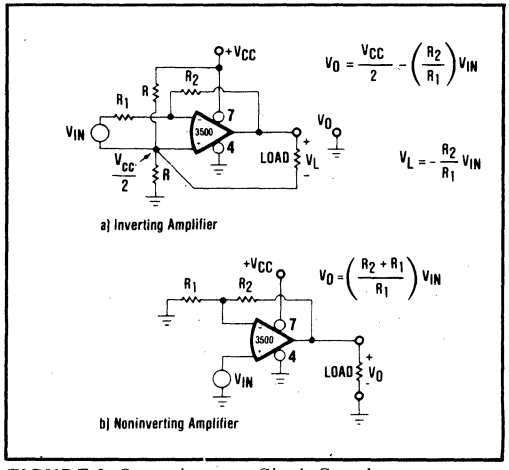
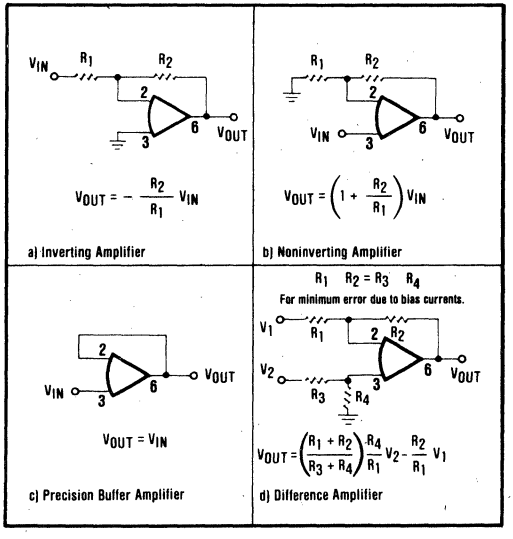


FIGURE 3. Operation on a Single Supply.

WIRING PRECAUTIONS

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 0.001μF ceramic capacitor from pins 7 and 4 to the power supply common.

TYPICAL APPLICATIONS



BURR-BROWN®

3500MP

Matched Low Bias Current IC OPERATIONAL AMPLIFIERS

FEATURES

TWO MONOLITHIC OP AMPS WITH ...

- MATCHED OFFSET VOLTAGES - △ Vos = 200μV max
- MATCHED DRIFT, △Vos vs Temp. = 1μV/°C max
- LOW NOISE, 1.4μV p-p
- LOW BIAS CURRENT, 50nA max
- INTERNAL COMPENSATION
- WIDE POWER SUPPLY RANGE

APPLICATIONS

- INSTRUMENTATION AMPLIFIERS
- MULTISTAGE ACTIVE FILTERS WITH LOW OUTPUT OFFSET
- LOW DRIFT SINGLE-ENDED AMPLIFIERS WITH LOW NOISE
- DUAL CHANNEL AMPLIFIERS WITH MATCHED DRIFT

DESCRIPTION

Close process control and careful grading by Burr-Brown make possible a new dimension in IC op amps - drift matched pairs. Drifts as low as 1μV/°C may be obtained using the 3500MP op amps. The 3500MP IC's are selected from Burr-Brown's 3500 series of op amps, thus all the features of the 3500 series are automatically found in the 3500MP. This enables the 3500MP to provide very-low drift (1μV/°C) with very-low noise (1.4μV p-p) without sacrificing speed. (Slew rate 0.8V/μsec min.)

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high input impedance, both differential and common-mode.

All units of the 3500E series are 100% temperature tested for voltage and current drift. The 3500 is also one of the lowest noise IC op amps yet produced, as illustrated by the curves on page 1-102. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated for unconditional stability for all feedback configurations, even with capacitive loads. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30V. The output stage is internally current limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

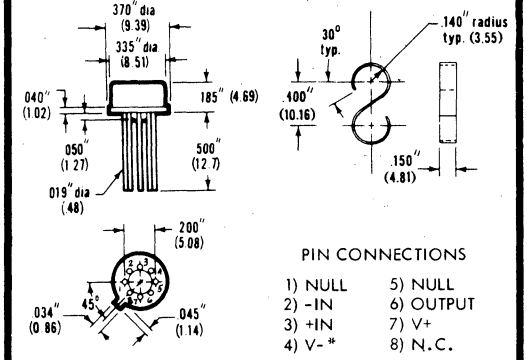
Specifications typical at 25°C and ±15 Vdc power supply unless otherwise noted.
(Two matched operational amplifiers Burr-Brown 3500 type)

MODEL	3500MP (Both Units)
OPEN LOOP GAIN	100 dB
RATED OUTPUT	
Voltage	±10 V, min.
Current	±10 mA, min.
Output Impedance	1 kΩ
FREQUENCY RESPONSE	
Unity Gain, Small Signal	1.5 MHz
Full Power Sine Wave	12 kHz, min.
Slew Rate	0.8 V/μsec, min.
INPUT OFFSET VOLTAGE V_{os1}, V_{os2}	
Initial Offset @ 25°C	±2 mV, max.
Avg. vs. Temp. (-25 to +85°C) max.	±5 μV/°C
vs. Supply Voltage	±40 μV/V
vs. Time	±5 μV/mo
DIFFERENTIAL INPUT OFFSET VOLTAGE $\Delta V_{os} = \lvert V_{os1} - V_{os2} \rvert$	
Initial Offset @ 25°C	±200 μV, max.
Avg. vs. Temp. (-25 to +85°C) max.	±1.0 μV/°C
INPUT BIAS CURRENT	
@ 25°C (either input)	±50 nA, max.
Avg. vs. Temp. (-25°C to +85°C) max.	±0.5 nA/°C
vs. Supply Voltage	±0.2 nA/V
INPUT DIFFERENCE CURRENT	
@ 25°C	±25 nA
Avg. vs. Temp. (-25°C to +85°C)	±0.25 nA/°C
vs. Supply Voltage	±0.1 nA/V
INPUT IMPEDANCE	
Differential	10^7 Ω ‖ 3 pF
Common Mode	5×10^9 Ω ‖ 3 pF
INPUT NOISE	
Voltage, 0.01 Hz to 10 Hz, p-p	2.0 μV
10 Hz to 10 kHz, rms	1.4 μV
Current, 0.01 Hz to 10 Hz, p-p	200 pA
10 Hz to 10 kHz, rms	35 pA
INPUT VOLTAGE RANGE	
Common Mode Voltage	±11 V, min.
Common Mode Rejection @ ±10 V	100 dB
Maximum Safe Input Voltage *	± supply
POWER SUPPLY	
Voltage, Rated Specification	±15 V
Operating Range	±3 to ±20 V
Current, Quiescent	±3.5 mA, max
TEMPERATURE RANGE	
Operating Ambient	-25 to +85°C
Storage	-65 to +125°C

* If signal voltage is applied to the input in the absence of power supply voltage, series resistance should be used to limit input current to 20 mA.

TO-99 PACKAGE

Dimensions in millimeters are shown in parentheses.



PIN CONNECTIONS

1) NULL	5) NULL
2) -IN	6) OUTPUT
3) +IN	7) V+
4) V- *	8) N.C.

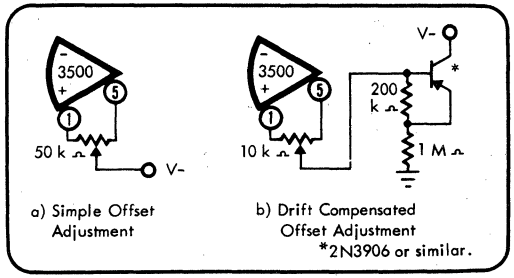
*Pin 4 is connected to case. NC is no internal connection

OFFSET ADJUSTMENT

The input offset voltage of the Model 3500 may be adjusted to zero by connecting a 50 kΩ potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 1a). This provides an adjustment range of approximately ±10 mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the Model 3500 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3 μV/°C change of drift for each 1.0 mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers this effect must be considered. By use of a transistor as in Figure 1b the effect of offset adjustment on drift can be substantially reduced (by approximately a factor of six).

Whenever possible adjust V_{os1} to equal V_{os2} (zero differential offset). Do not adjust $V_{os1} = 0 = V_{os2}$ unless absolutely necessary. If both V_{os1} and V_{os2} are adjusted to zero, the drift compensated adjustment technique (Figure 1b) must be used or the ΔV_{os} drift of 1 μV/°C will be adversely affected.



a) Simple Offset Adjustment

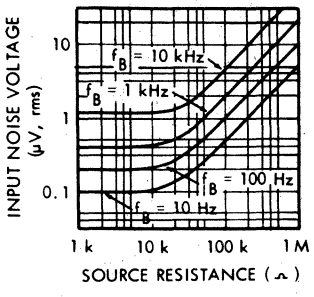
b) Drift Compensated Offset Adjustment
*2N3906 or similar.

FIGURE 1. Offset Adjustment Techniques.

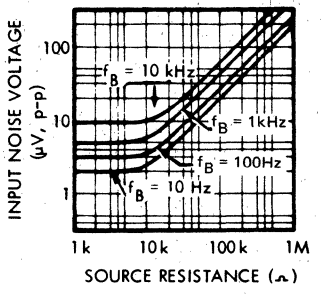
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

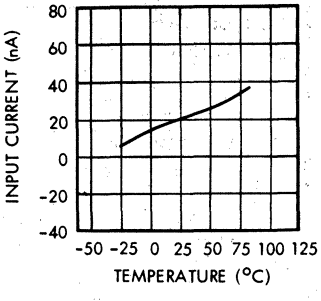
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



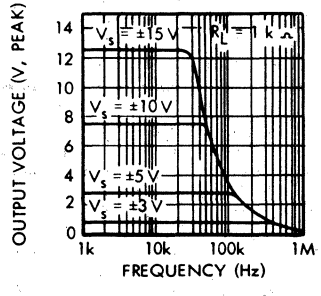
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



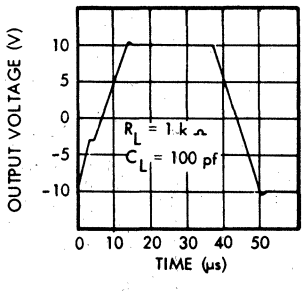
INPUT BIAS CURRENT vs. TEMPERATURE



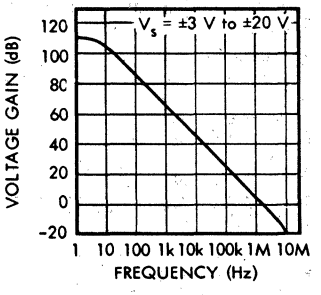
OUTPUT VOLTAGE vs. FREQUENCY



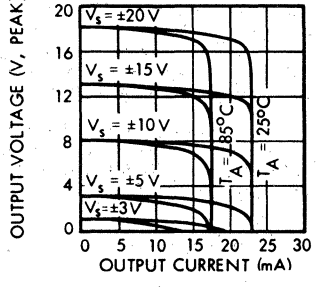
VOLTAGE FOLLOWER STEP RESPONSE



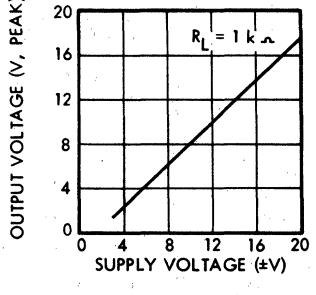
OPEN LOOP FREQUENCY RESPONSE



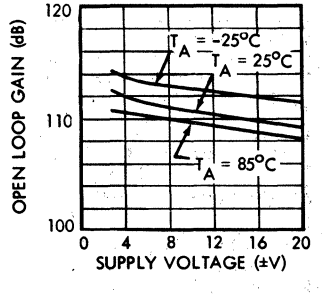
OUTPUT VOLTAGE vs. OUTPUT CURRENT



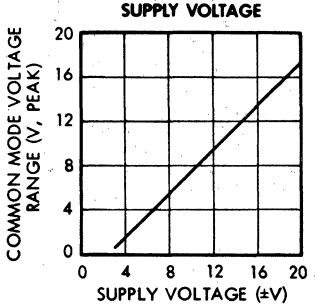
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



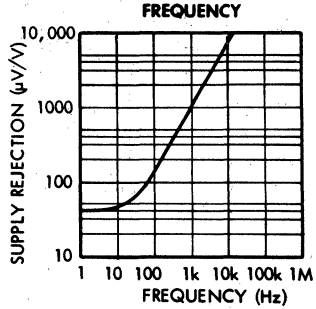
VOLTAGE GAIN vs. SUPPLY VOLTAGE



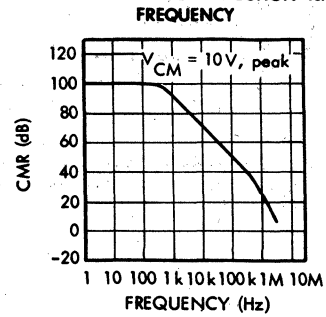
COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



COMMON MODE REJECTION vs. FREQUENCY



BIAS CURRENT EFFECTS

Input bias current of an amplifier can generate additional small offset voltages by flowing through the equivalent input source resistances. Although the bias currents for the 3500MP are quite small, the current-generated offset voltages may be significant for source resistances greater than 1 kΩ. When using the matched 3500MP amplifiers to obtain offset voltage drifts on the order of 1 μV/°C particular attention must be given to the input bias currents. Because of the great number of circuit configurations involving two operational amplifiers, it is only possible to give some general guidelines for minimizing bias current effects.

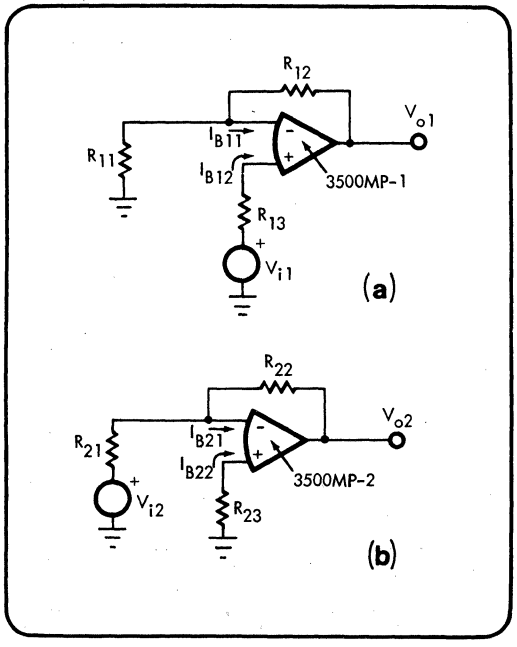


FIGURE 2. Bias Current Effects.

Bias currents generate offset voltages in two ways. If $I_{B11} = I_{B12}$ (see Figure 2a) no offset will be generated by I_{B11} and I_{B12} if $R_{13} = \frac{R_{11}R_{12}}{R_{11}+R_{12}}$

However, in general, $I_{B11} = I_{B12} + I_{os1}$ where I_{os1} is the input offset current of op amp 1. I_{os} will vary from unit to unit and I_{os} is also subject to drift with time and temperature. Fortunately I_{os} is normally much less than I_{B11}. Therefore we may minimize effects of bias current by making the Thevenin equivalent input resistances equal (i.e., $R_{13} = \frac{R_{11}R_{12}}{R_{11}+R_{12}}$) and the effects of I_{os} may be minimized by making the equivalent source resistances small. Keep in mind that in some two amplifier circuits the "differential" bias current ($\Delta I_B = I_{B11} - I_{B12}$) will generate the predominate source of bias current errors.

Similarly for the circuit configuration of Figure 2b bias current effects are minimized by setting

$$R_{23} = \frac{R_{21}R_{22}}{R_{21}+R_{22}}$$

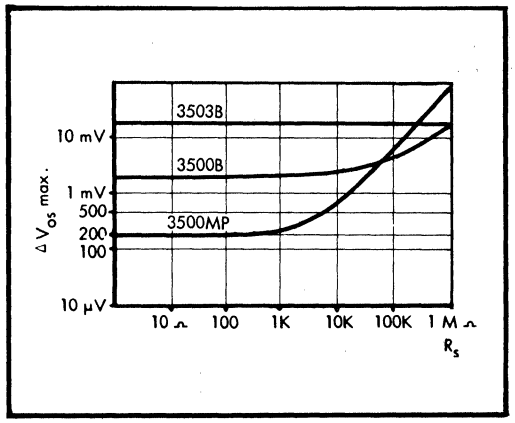


FIGURE 3. ΔV_{os} vs. Source Resistance.

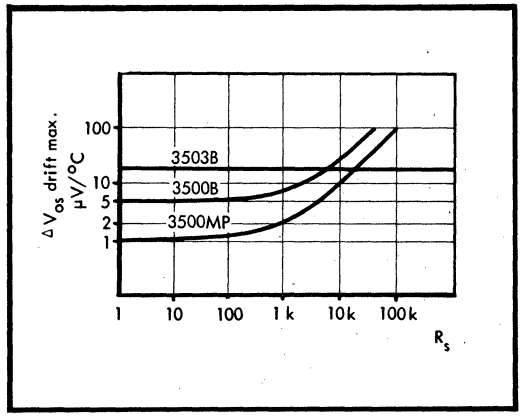


FIGURE 4. ΔV_{os} Drift vs. Source Resistance.

The effect of offset currents are summarized in Figures 3 and 4 which plot offset voltage (ΔV_{os}) between the two amplifiers and ΔV_{os} drift as a function of source resistance (R_s). Curves for a single 3500B type amplifier and an FET input 3503B) amplifier are included for comparison. Note that a 3500MP provides superior performance for low source resistance.

THERMAL CONSIDERATIONS

The very low ΔV_{os} drift specification for the 3500MP assumes both integrated circuits have the same "chip" temperature. A metal clip is furnished with the 3500MP to provide close thermal matching between the two device cases. However, care should be taken to see that each op amp drives approximately the same load or thermal offsets will result due to internal self heating. In any case thermal offsets are much less critical with the 3500MP than with matched transistors. A 1°C temperature offset will cause a voltage offset in a matched pair of transistors of about 2.5 mV but the ΔV_{os} of a 3500MP will be only 5 μV for 1°C temperature offset.

APPLICATIONS

COMPOSITE LOW DRIFT OP AMP

The two matched op amps in the 3500MP may be connected to simulate a single op amp with very low initial offset voltage and drift. The circuit shown in Figure 5a may be used in any conventional op amp circuit to obtain low drift. A typical feedback circuit with an inverting gain of 100 is shown in Figure 5c. Note the addition of R_3, R_4, and R_5 to minimize bias current effects on the offset voltage.

The composite op amp will be stable in circuits with voltage gains greater than about three. For lower voltage gains the compensation shown in Figure 5b may be used if required. For unity gain non-inverting operation, the compensation technique of Figure 5b will not decrease the composite amplifier bandwidth below the bandwidth of the individual op amps.

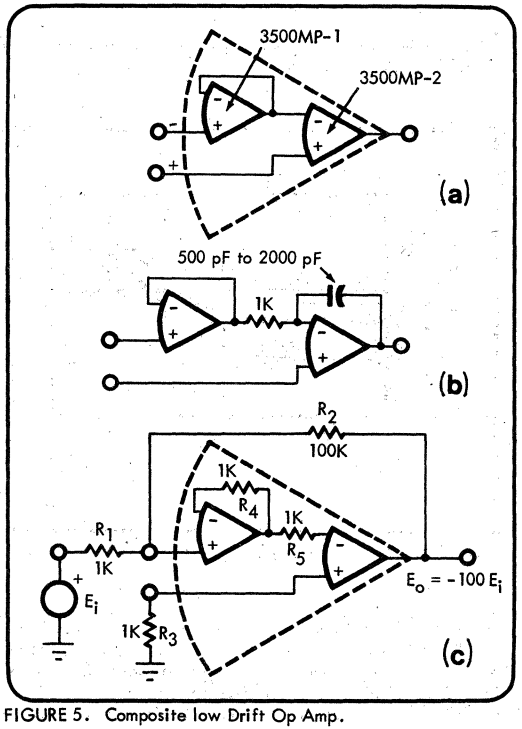


FIGURE 5. Composite low Drift Op Amp.

HIGH INPUT IMPEDANCE DIFFERENTIAL AMPLIFIER

The circuit in Figure 7 acts as a high input impedance differential amplifier provided $R_1 / R_2 = R_4 / R_3$. A mismatch of resistance ratios results in a common mode gain A_C as shown below. In addition to finite common mode gain, a resistance mismatch causes a differential gain error equal to A_C/A_D. Notice that the output offset error is proportional to ΔV_{os} which is made very small by the matching of the two op amps. (In most practical cases $A_D \Delta V_{os} >> A_C (V_{os1} + V_{os2}) / 2$.)

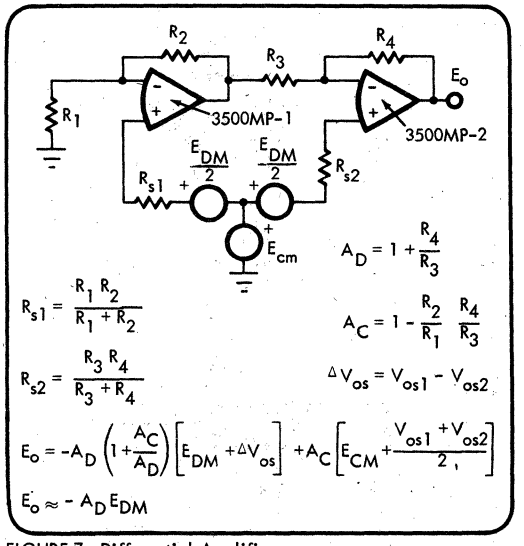


FIGURE 7. Differential Amplifier.

LOW PASS FILTER WITH LOW DC ERROR

Multistage low pass active filters often have large amounts of d.c. offset and drift because the offsets of the op amps used tend to add. The inverting synthesis technique shown in Figure 6 to realize each pole pair causes the amplifier offset voltages to cancel if they are matched. The net offset error without trimming will be less than 400 μV and the total drift of the filter is less than 2 μV/°C. The output d.c. error is made essentially independent of bias current effects by choosing small resistor values. However the small resistance values limit the maximum output voltage to about 1.0 V p-p and $R_L > 125\ \Omega$.

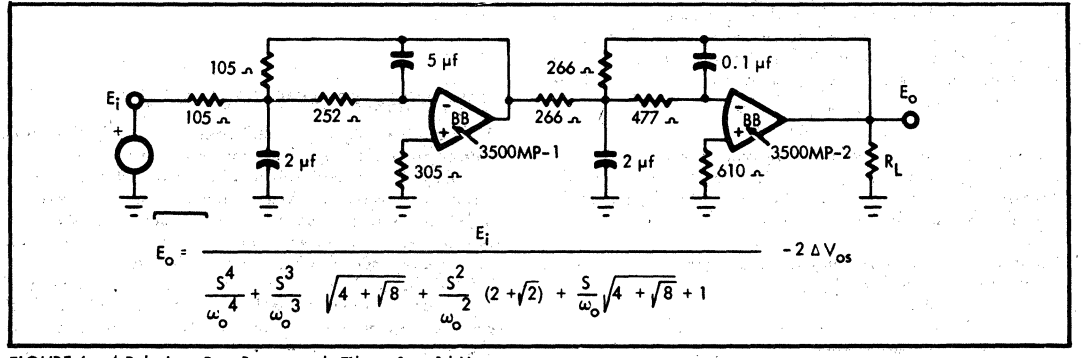
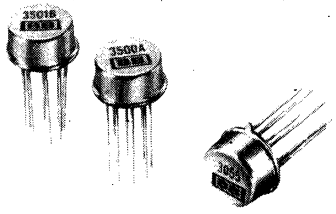


FIGURE 6. 4 Pole Low Pass Butterworth Filter; f_o = 1 kHz.

BURR-BROWN®



3501

Low Bias Current OPERATIONAL AMPLIFIERS

FEATURES

- LOW BIAS CURRENT, ±3nA, max
- LOW DRIFT, ±5μV/°C, max ±30pA/°C, max
- LOW NOISE, 0.8μV, p-p 30pA, p-p
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- REPLACES 108 AND 741 TYPE AMPLIFIERS

DESCRIPTION

The 3501 series is designed to minimize input voltage drift and input bias current, without resorting to exotic processing. The low input bias current is achieved by a current cancellation technique developed by Burr-Brown's IC Engineering Group. The same input circuitry gives the 3501 very-high input impedance, both differential and common-mode. Internal current levels of the amplifier are maintained essentially constant over the full range of supply voltages by relying on basic semiconductor properties and device matching. The result is that major performance parameters - open-loop gain, bias current, voltage drift, slew rate and output current - are affected only slightly by wide variations of supply voltage. Quiescent power drain is quite low over the supply voltage range.

The 3501 is internally compensated for unconditional stability in all feedback configurations, even with capacitive loads. Thus it is interchangeable with both 741 and 108 type amplifiers (eliminating the external frequency compensation required of 108 type amplifiers).

Because of the unique input stage design of the 3501, its common-mode rejection is very-high (100dB). The result is excellent linearity (.01% or better) as a noninverting buffer. Also the input stage exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high for input voltages up to the value of the supply voltages.

The output stage is internally current limited to provide protection against continuous circuits.

All units of the 3501 series are 100% tested to all min/max specifications - including voltage and current drift versus temperature. Units are drift selected with maximum specifications at ±5μV/°C, ±10μV/°C and ±20μV/°C. Both military and industrial temperature range versions are offered.

The 3501 is also a very-low noise amplifier. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually dictate against the use of utility op amps, such as the 741, for low-level signal processing.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

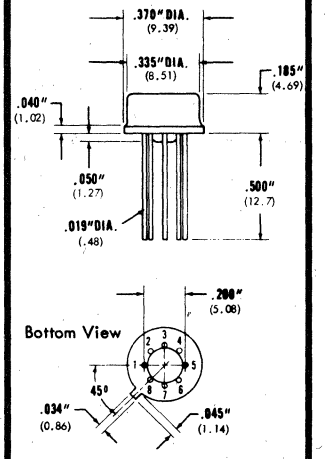
Typical at 25°C and ±15 Vdc unless otherwise noted.

MODEL	3501A 3501R	3501B 3501S	3501C
OPEN LOOP GAIN, dc, no load	93 dB, min	*	*
RATED OUTPUT		*	*
Voltage	±10V, min		
Current	±5 mA, min		
Capacitive Load Range	0 to 1000 pF		
Output Impedance	2 kΩ		
FREQUENCY RESPONSE		*	*
Unity Gain, Open Loop	0.5 MHz		
Full Power Sine Wave	1.6 kHz, min		
Slew Rate	0.1 V/μsec, min		
INPUT OFFSET VOLTAGE			
Initial Offset @ 25°C	±5 mV, max	±2 mV, max	±2 mV, max
Avg. vs. Temp. (-25° to +85°C) max	±20 μV/°C (A)	±10μV/°C (B)	±5 μV/°C (C)
(-55° to +125°C) max	±20 μV/°C (R)	±10 μV/°C (S)	
vs. Supply Voltage	±40 μV/V	*	*
vs. Time	±2 μV/day	*	*
INPUT BIAS CURRENT			
@ 25°C	±15 nA, max	±7 nA, max	±3 nA, max
Avg. vs. Temp. (-25° to +85°C) max	±0.2 nA/°C (A)	±0.15 nA/°C(B)	±0.1 nA/°C(C)
(-55° to +125°C) max	±0.2 nA/°C (R)	±0.15 nA/°C(S)	
vs. Supply Voltage	±30 pA/V	*	*
INPUT DIFFERENCE CURRENT			
@ 25°C	±5 nA	±3 nA	±2 nA
Avg. vs. Temp. (-25° to +85°C)	±0.1 nA/°C (A)	±0.05 nA/°C(B)	±0.03nA/°C(C)
(-55° to +125°C	±0.1 nA/°C (R)	±0.05 nA/°C(S)	
vs. Supply Voltage	±10 pA/V	*	*
INPUT IMPEDANCE		*	*
Differential	5×10^7 Ω ‖ 3 pF		
Common Mode	10^{10} Ω ‖ 3 pF		
INPUT NOISE		*	*
Voltage, .01 Hz to 10 Hz, p-p	2 μV		
10 Hz to 10 kHz, rms	1.4 μV		
Current, .01 Hz to 10 Hz, p-p	66 pA		
10 Hz to 10 kHz, rms	12 pA		
INPUT VOLTAGE RANGE		*	*
Common Mode Voltage	±11 V, min		
Common Mode Rejection @ ±10V	100 dB		
Max. Safe Input Voltage	±supply**		
POWER SUPPLY		*	*
Voltage, rated specification	±15 Vdc		
Operating Range	±3V to ±20V		
Absolute Max	±22 Vdc		
Current, quiescent	±1.5 mA, max.		
TEMPERATURE RANGE			
Operating, Rated Specs A, B, C	-25° to +85°C	*	*
R, S	-55° to +125°C	*	*
Storage	-65° to +150°C	*	*

* Specifications same for all models. ** If input voltage is applied in the absence of power supply voltage, series resistance should be added to limit current flow to ±20 mA.

TO-99 PACKAGE

Specify 3501A, etc.



Note: Dimensions in millimeters are shown in parentheses.

PIN CONNECTIONS

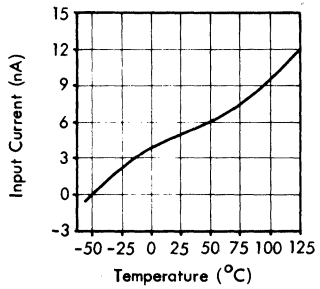
1) NULL	5) NULL
2) -IN	6) OUTPUT
3) +IN	7) V+
4) V-*	8) N.C.

*Pin 4 connected to case

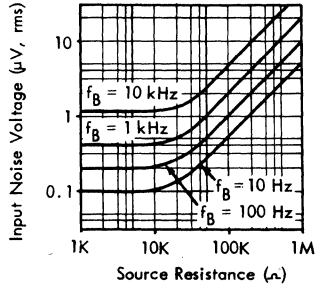
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

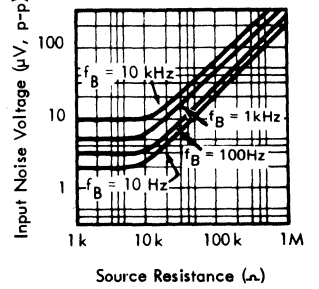
INPUT BIAS CURRENT vs. TEMPERATURE



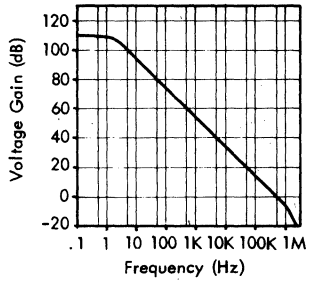
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



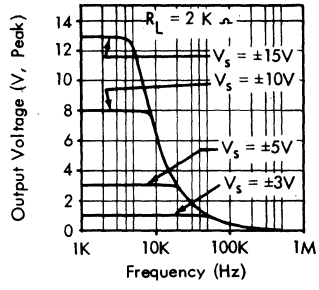
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



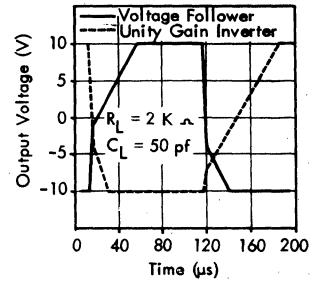
OPEN LOOP FREQUENCY RESPONSE



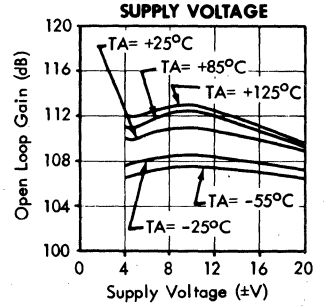
OUTPUT VOLTAGE vs. FREQUENCY



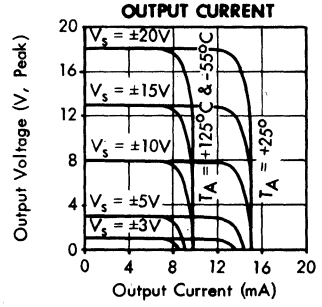
LARGE SIGNAL STEP RESPONSE



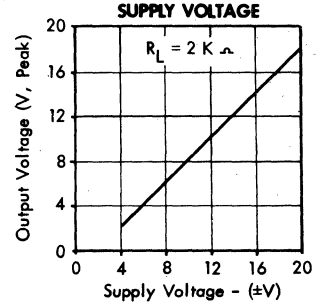
VOLTAGE GAIN vs. SUPPLY VOLTAGE



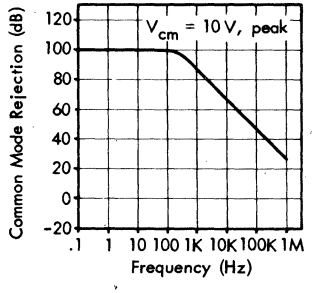
OUTPUT VOLTAGE vs. OUTPUT CURRENT



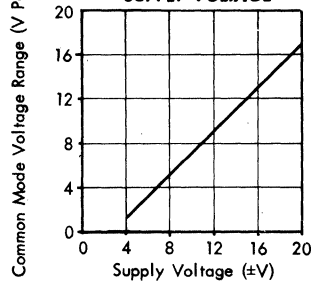
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



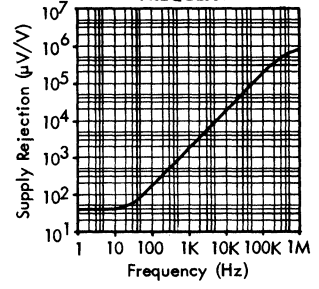
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY

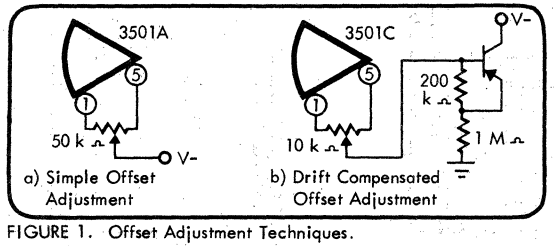


APPLICATIONS INFORMATION

OFFSET ADJUSTMENT

The input offset voltage of the Model 3501 may be adjusted to zero by connecting a 50 k Ω potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 1a). This provides an adjustment range of approximately ±10 mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the 3501 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3 μV/°C change of drift for each 1.0 mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers, such as the 3501C, this effect must be considered. By use of a transistor as in Figure 1 the effect of offset adjustment on drift can be substantially reduced (by approximately a factor of six).



a) Simple Offset Adjustment

b) Drift Compensated Offset Adjustment

FIGURE 1. Offset Adjustment Techniques.

BIAS CURRENT EFFECTS

Input bias current of the amplifier creates additional offset voltages by flowing in the impedances of the signal source and the feedback network. Although the bias currents of the 3501 are quite small, their effects may be appreciable when these impedances are large. The bias currents at the two inputs tend to be equal and the difference current smaller than either. Thus equalizing the resistance from each input to common, as in Figure 2, is an effective means of reducing DC offset due to bias current.

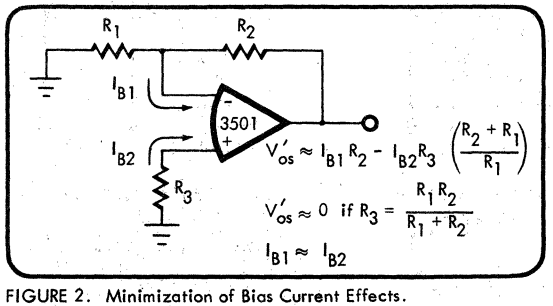


FIGURE 2. Minimization of Bias Current Effects.

OPERATION ON A SINGLE SUPPLY

Although virtually any op amp can be operated on a single supply if input and output voltage limitations are observed, the Model 3501 is particularly suitable for such use. It's wide supply range of ±3 to ±20 Vdc translates to a single supply operating range of 6 to 40 Vdc, plus or minus. Two possible modes of operation on a single supply are shown in Figure 3. The following conditions must be observed to keep the amplifier within its linear region of operation.

1) $+2 < e_o < (V_s - 2)$

2) $+3 < e_s < (V_s - 3)$, Figure 3b

When operating on a single supply (V_s), shorting the output to common is equivalent to a short to supply and the internal power dissipation is approximately twice that which occurs for a short to common with balanced supplies of $\pm \frac{V_s}{2}$. This dissipation may exceed safe limits for single supply voltages greater than 20 volts and must be prevented by use of a series limiting resistor or other device, if short circuit protection is desired.

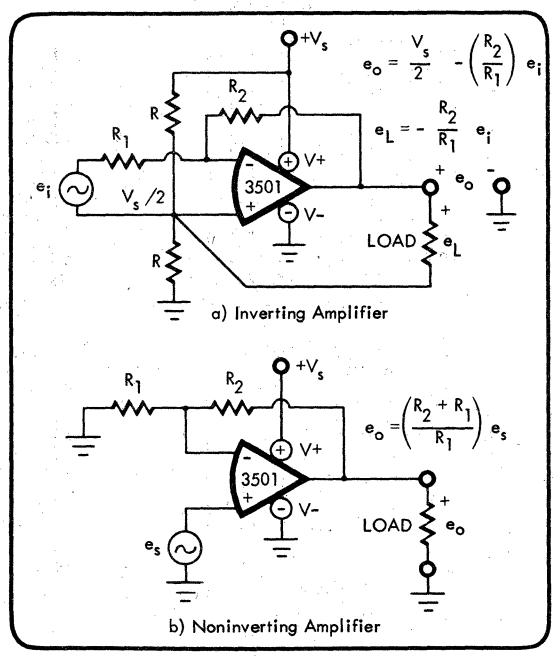


FIGURE 3. Operation on a Single Supply.

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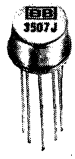

3507J

Fast-Slewing OPERATIONAL AMPLIFIER

FEATURES

- 120V/μsec SLEW RATE
- 20MHz GAIN-BANDWIDTH PRODUCT
- INTERCHANGEABLE WITH 741 TYPES

DESCRIPTION

Burr-Brown model 3507J is intended for use in circuits requiring fast transient response-pulse amplifiers, D/A converters, comparators, fast followers, etc. Key parameters such as slew rate, settling time and bandwidth are orders of magnitude better than for most other IC op amps.

The 3507J is compensated to allow faster slewing and greater bandwidth for gains of 3 or more. For gains greater than 3, the gain rolloff is 6dB/octave. By use of a single external 20pF compensation capacitor the 3507J can be stabilized at all gains including unity. In addition, by use of an alternate compensation technique, it is possible to stabilize the 3507J at unity gain without sacrificing its faster slew rate.

The 3507J is pin-compatible with other standard IC op amps while offering greater speed and higher output current. It also is input- and output-protected to prevent damage if the output is shorted to common, or the input is shorted to supply voltage.

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SPECIFICATIONS

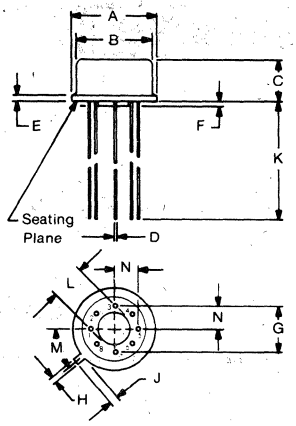
ELECTRICAL

Typical at ±15VDC and +25°C unless otherwise noted.

MODEL	3507J	
	TYPICAL	GUARANTEED
OPEN-LOOP GAIN, DC		
No Load	90dB	
2kΩLoad	83dB	77dB
RATED OUTPUT		
Voltage (1kΩ load)	±12V	±10V
Current	±20mA	±10mA
DYNAMIC RESPONSE		
Small Signal Bandwidth (0dB)	--	
Gain-Bandwidth Product (A_{CL} = 10)	20MHz	
Full Power Bandwidth	1.6MHz	1.2MHz
Slew Rate	120V/μsec	80V/μsec
Settling Time (0.1%)	200nsec	
Rise Time (10-90%, small signal)	25nsec	50nsec
Overshoot	--	--
INPUT OFFSET VOLTAGE		
Initial (without adjust) at +25°C	±5mV	±10mV
Over Temperature		±14mV
(avg. 0°C to +70°C)	±30μV/°C	
vs Supply Voltage	±30μV/V	200μV/V
vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at +25°C	+50nA	+250nA
Over Temperature		+500nA
(avg. 0°C to +70°C)	±0.5nA/°C	
INPUT DIFFERENCE CURRENT		
Initial at +25°C	±20nA	±50nA
Over Temperature		±100nA
(avg. 0°C to +70°C)	±0.1nA/°C	
INPUT IMPEDANCE		
Differential	100MΩ ‖ 3pF	40MΩ
Common-Mode	1000MΩ ‖ 3pF	
INPUT VOLTAGE RANGE		
Common-Mode (linear operation)	±12V	±10V
Differential (between inputs)		±15V
Absolute Max (either input)		±Supply
Common-Mode Rejection	90dB	74dB
POWER SUPPLY		
Rated Voltage		±15VDC
Voltage Range, derated	±8V to ±20V	
Current, quiecscent	±4mA	±6mA
TEMPERATURE RANGE		
Specifications		0°C to +70°C
Operating		-25°C to +85°C
Storage		-65°C to +150°C

MECHANICAL

TO-99 PACKAGE

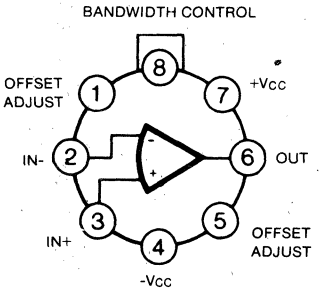


NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM

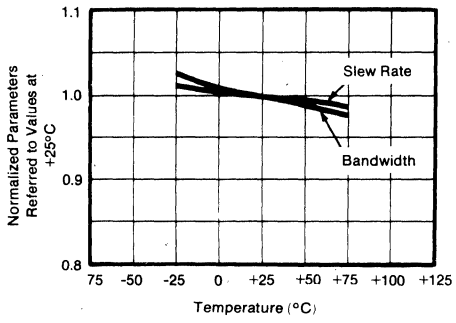


(TOP VIEW)

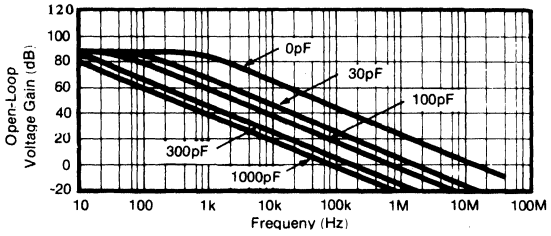
TYPICAL PERFORMANCE CURVES

(At +25°C and ±15VDC, unless otherwise specified)

NORMALIZED AC PARAMETERS
VS TEMPERATURE

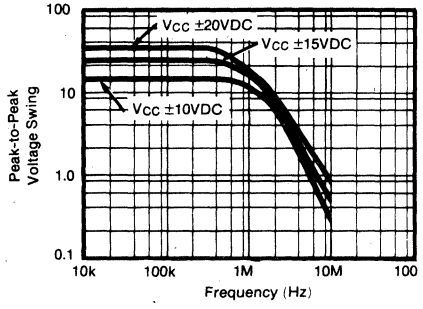


OPEN-LOOP FREQUENCY RESONSE*



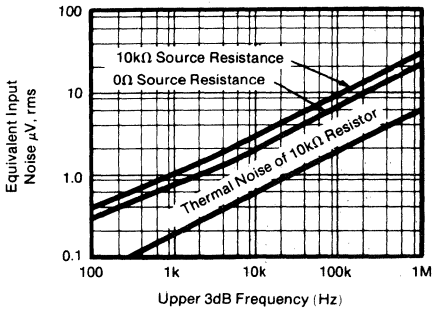
*Capacitance values shown are external compensation from pin 8 to Common.

OUTPUT VOLTAGE SWING
VS FREQUENCY*

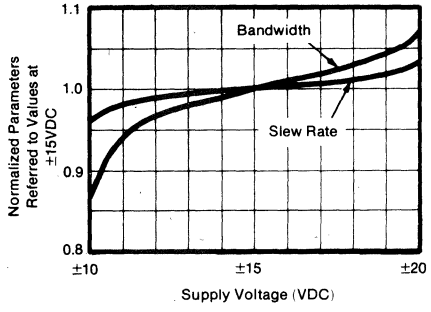


*With no external compensation capacitance.

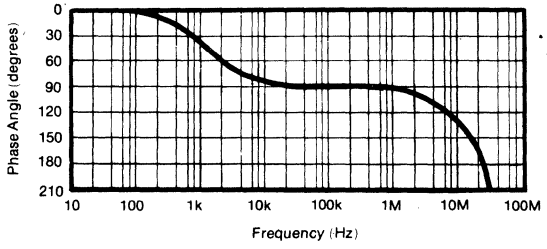
EQUIVALENT INPUT NOISE
VS BANDWIDTH



NORMALIZED AC PARAMETERS
VS SUPPLY VOLTAGE AT +25°C



OPEN-LOOP PHASE RESPONSE



APPLICATIONS

BANDWIDTH COMPENSATION

The frequency response of the 3507J can be adjusted by use of an external compensation capacitor from pin 8 to common, as shown in Figure 1. The open-loop frequency response curves illustrate the effect of various values of capacitance. The 3507J is stable for gains of 3 or greater without external compensation (subject to the same limits on stray and load capacitance and resistance levels). A 20pF compensation capacitor will stabilize the 3507J for all values of gain, at the sacrifice of bandwidth and slew rate.

The circuit of Figure 2 illustrates another approach to compensation of the 3507J. This method yields unity gain stability without sacrificing slew rate.

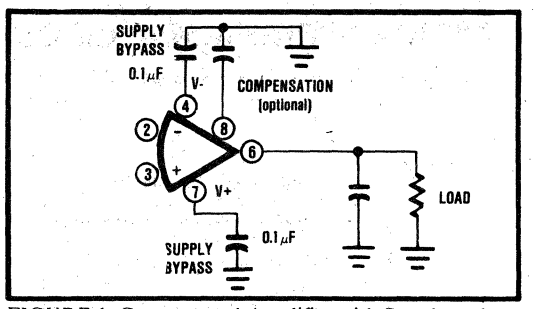


FIGURE 1. Compensated Amplifier with Supply and Load Bypassing.

STABILITY

Because the 3507J is an extremely fast amplifier with high gain, stray wiring capacitance and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly by-passing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50pF capacitor; see Figure 1.

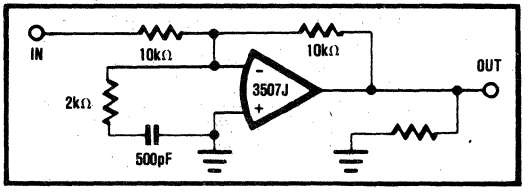


FIGURE 2. Alternate Method for Unity - Gain Compensation of 3507J.

OFFSET VOLTAGE ADJUSTMENT

Although the offset voltage of this amplifier is only a few millivolts, it may be desirable in some cases to null this offset. This is done by use of a 20kΩ potentiometer as shown in Figure 3.

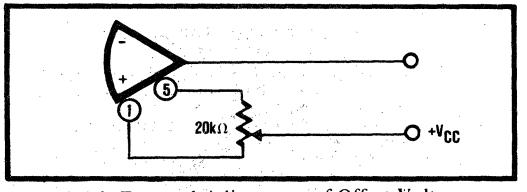


FIGURE 3. External Adjustment of Offset Voltage.

TEST CIRCUIT - DYNAMIC RESPONSE

The test circuits of Figure 4 are used for measurement of slew rate, settling time, rise time and overshoot. Both rise time and overshoot are measured under small signal conditions (V_{OUT} = ±200mV). Slew rate and settling time are measured for a 10V, p-p, square wave.

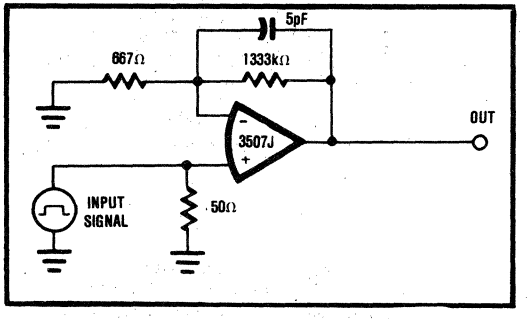


FIGURE 4. Dynamic Response Test Circuits.

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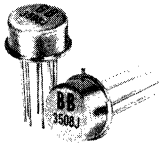

3508J

Wideband OPERATIONAL AMPLIFIER

FEATURES

- 100mHz GAIN BANDWIDTH PRODUCT
- 5nA INPUT BIAS CURENT
- 103dB OPEN-LOOP GAIN
- INTERCHANGEABLE WITH 741 TYPES

DESCRIPTION

Burr-Brown model 3508J is a wideband operational amplifier intended for use in circuits requiring extended bandwidth and high gain. Typical examples of applications are: RF signal amplifiers, fast recovery voltage references, high speed integrators, high frequency active filters, and photodiode amplifiers.

Model 3508J is internally compensated for stability at gains greater than five. The 3508J can be externallv compensated by use of a single capacitor, and can thus be stabilized at any value of gain. By use of an alternate compensation scheme the 3508J can be stabilized at unity gain without sacrificing slew rate.

In addition to its wide bandwidth and high gain the amplifier has a number of other significant advantages over other IC op amps; low bias current, high output current, and high common-mode rejection. Inputs are protected against voltages up to the value of the power supplies. The output is current-limited to provide short-circuit protection.

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SPECIFICATIONS

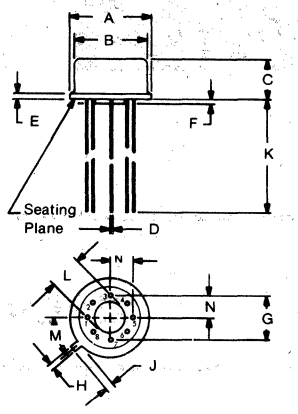
ELECTRICAL

Typical at ±15VDC and +25°C unless otherwise noted.

MODEL	3508J	
	TYPICAL	GUARANTEED
OPEN-LOOP GAIN, DC		
No Load	106dB	
2kΩLoad	103dB	98dB
RATED OUTPUT		
Voltage	±12V	±10V
Current	±18mA	±10mA
DYNAMIC RESPONSE		
Small Signal Bandwidth (0dB)	--	
Gain-Bandwidth Product (A_{CL} = 10)	100MHz	
Full Power Bandwidth	600kHz	320kHz
Slew Rate	35V/μsec	20V/μsec
Settling Time (0.1%)	--	--
Rise Time (10-90%, small signal)	17nsec	45nsec
Overshoot	--	--
INPUT OFFSET VOLTAGE		
Initial (without adjust) at +25°C	±3mV	±5mV
Over Temperature		±7mV
(avg. 0°C to +70°C)	±30μV/°C	
vs Supply Voltage	±30μV/V	200μV/V
vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at +25°C	+15nA	+25nA
Over Temperature		+40nA
(avg. 0°C to +70°C)	±0.5nA/°C	
INPUT DIFFERENCE CURRENT		
Initial at +25°C	±5nA	±25nA
Over Temperature		±40nA
(avg. 0°C to +70°C)	±0.2nA/°C	
INPUT IMPEDANCE		
Differential	300MΩ ‖ 3pF	40MΩ
Common-Mode	1000MΩ ‖ 3pF	
INPUT VOLTAGE RANGE		
Common-Mode (linear operation)	±13V	±11V
Differential-Mode (between inputs)		±12V
Absolute Max (either input)		±Supply
Common-Mode Rejection	100dB	74dB
POWER SUPPLY		
Rated Voltage		±15VDC
Voltage Range, derated	±8V to ±22V	
Current, quiecscent	±3mA	±4mA
TEMPERATURE RANGE		
Specifications		0°C to +70°C
Operating		-25°C to +85°C
Storage		-65°C to +150°C

MECHANICAL

TO-99 PACKAGE

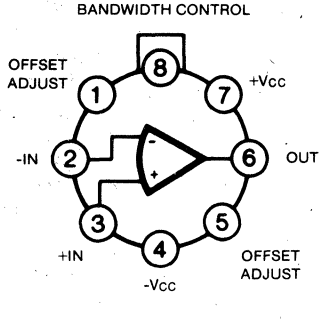


NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM

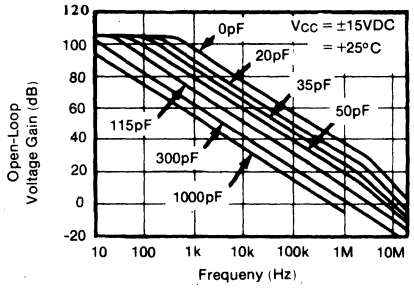


(TOP VIEW)

TYPICAL PERFORMANCE CURVES

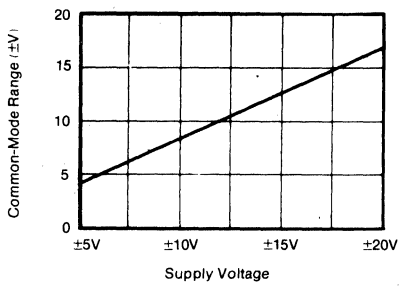
(At +25°C and ±15VDC, unless otherwise specified)

OPEN-LOOP FREQUENCY RESONSE*

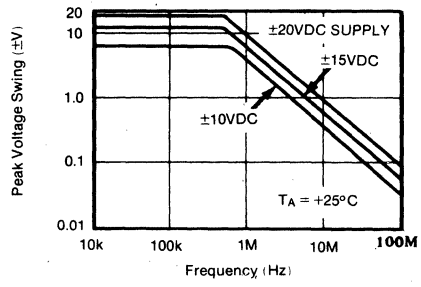


*Capacitance values shown are external compensation from pin 8 to Common.

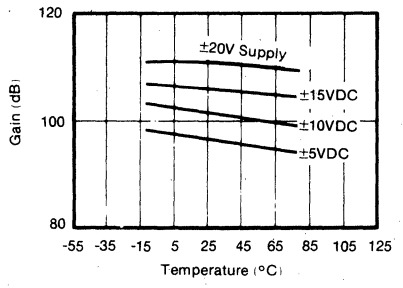
COMMON-MODE VOLTAGE RANGE VS SUPPLY VOLTAGE



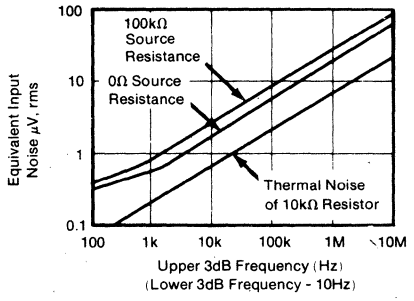
OUTPUT VOLTAGE SWING VS FREQUENCY*



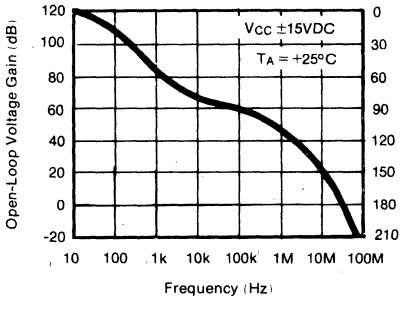
OPEN-LOOP VOLTAGE GAIN VS TEMPERATURE



EQUIVALENT INPUT NOISE VS BANDWIDTH



OPEN-LOOP GAIN AND PHASE ANGLE VS FREQUENCY



APPLICATIONS

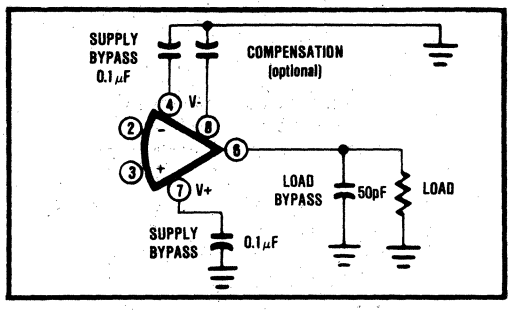


FIGURE 1. Compensated Amplifier with Supply and Load Bypassing.

BANDWIDTH COMPENSATION

The frequency response of the 3508J can be adjusted by use of an external compensation capacitor from pin 8 to common as shown in Figure 1. The open-loop frequency response curves included in the Typical Performance Curves illustrate the effect of various values of capacitance. The 3508J is stable for gains of 5 or greater without external compensation (subject to the same limits on stray and load capacitance and resistance levels). A 20pF compensation capacitor will stabilize the 3508J for all values of gain, at the sacrifice of bandwidth and slew rate.

The circuit of Figure 2 illustrates another approach to compensation of the 3508J. This method yields unity gain stability without sacrificing slew rate.

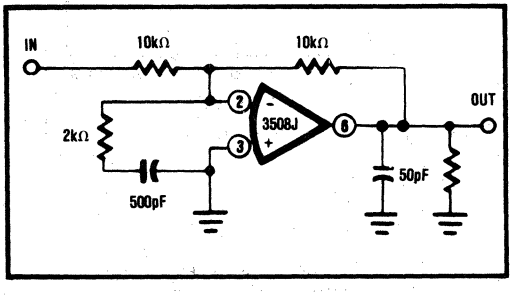


FIGURE 2. Alternate Method for Unity - Gain Compensation of 3508J.

STABILITY

Because the 3508J is an extremely fast amplifier with high gain, stray wiring capacitance and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly bypassing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50pF capacitor; (see Figure 1).

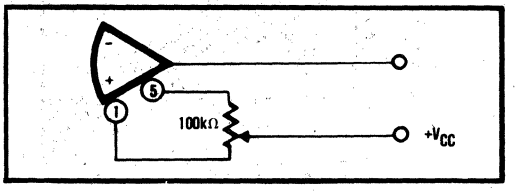


FIGURE 3. External Adjustment of Offset Voltage.

OFFSET VOLTAGE ADJUSTMENT

Although the offset voltage of this amplifier is only a few millivolts, it may be desirable in some cases to null this offset. This is done by use of a 100kΩ potentiometer as shown in Figure 3.

TEST CIRCUIT - DYNAMIC RESPONSE

The test circuits of Figure 4 are used for measurement of slew rate, settling time, rise time and overshoot. Both rise time and overshoot are measured for a small output signal ($V_{OUT} = \pm 100mV$). Slew rate and settling time are measured for a 10V, p-p, square wave.

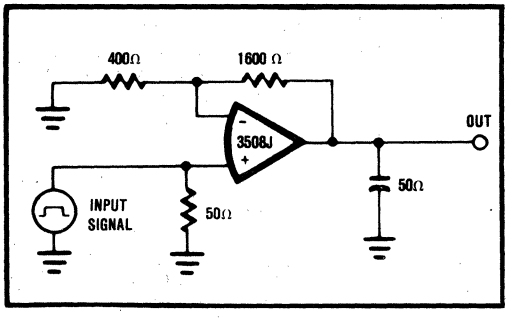


FIGURE 4. Dynamic Response Test Circuits.

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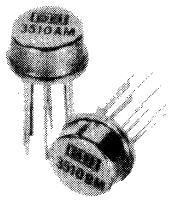


3510

Very-Low Drift - Precision OPERATIONAL AMPLIFIER

FEATURES

- VERY-LOW DRIFT - ±0.5µV/°C max
- VERY-LOW OFFSET - ±60µV max
- LOW BIAS CURRENT - ±15nA max
- HIGH OPEN-LOOP GAIN - 120dB min
- HIGH CMR - 110dB min
- VERY-LOW THERMAL FEEDBACK - ±0.1µV/V

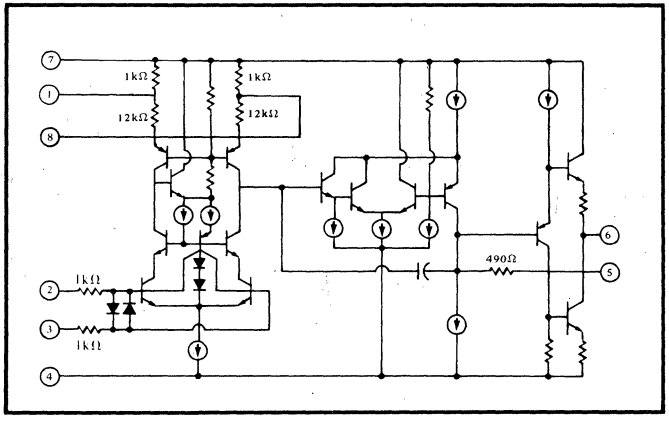
DESCRIPTION

High overall accuracy is offered by Burr-Brown's 3510 Operational Amplifier. It's designed expressly for use in high gain analog circuits where very-low drift and high accuracy are essential requirements.

This precision instrumentation grade op amp provides an economical method to maintain high circuit accuracy and reliability over temperature ranges from -25°C to +85°C, surpassing competitive units rated for only 0°C to +70°C.

Additional performance features of the 3510 include high open-loop gain, extremely-low initial offset voltage, high CMR, very-low thermal feedback, low input bias current and very-low voltage drift vs temperature.

Burr-Brown's rigid control of monolithic processing and its rigid quality control standards result in very-low voltage and current noise in the 3510. It's specifically designed for use in low level analog signal processing. Performance specifications are met exactly by precision trimming at the wafer level with complete testing before shipment. Performance of the 3510 significantly exceeds that of Burr-Brown's popular 3500 op amp.



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ELECTRICAL SPECIFICATIONS

Specifications at T_A = 25°C and ±15VDC, unless otherwise noted. Standard specifications after warm-up.

MODELS	3510AM			3510BM/3510SM			3510CM			UNITS
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN, DC										
2kΩ Load	120			*			*			dB
RATED OUTPUT										
Voltage	±10			*			*			V
Current	±10			*			*			mA
Output Resistance		300			*			*		Ω
Load Capacitance		1000			*			*		pF
FREQUENCY RESPONSE										
Unity Gain, Open Loop, Small Signal C_c = 4700pF		0.4			*			*		MHz
Closed-Loop Gain, C_c = 0, Stable Operation		≥10			*			*		V/V
Full Power Response, C_c = 0, A_{CL} = 10	7	12		*	*		*	*		kHz
Slew Rate, C_c = 0, A_{CL} = 10	0.5	0.8		*	*		*	*		V/μsec
INPUT OFFSET VOLTAGE										
Initial Offset, 25°C			150			120			60	μV
vs Temp(1) - unnulled V_{os}			2.0			1.0			0.5	μV/°C
vs Temp(1) - nulled V_{os}			2.5			1.4			0.7	μV/°C
vs Time		0.2			*			*		μV/mo
Power Supply Rejection	110	130		*	*		*	*		dB
Thermal Feedback, R_L = 2kΩ, f = 1Hz		±0.1			*			*		μV/V
INPUT BIAS CURRENT										
Initial Bias, 25°C			±35			±25			±15	nA
vs Temp(1)			±0.6			±0.4			±0.25	nA/°C
vs Supply Voltage		±0.1			*			*		nA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, 25°C			±20			±15			±10	nA
vs Temp(1)			±0.4			±0.25			±0.15	nA/°C
vs Supply Voltage		±10			*			*		pA/V
INPUT IMPEDANCE										
Differential		1 ‖ 3			*			*		MΩ ‖ pF
Common-mode		10 ‖ 3			*			*		GΩ ‖ pF
INPUT NOISE										
Voltage, 0.1Hz to 10Hz		0.8			*			*		μV, p-p
f_o = 10Hz		14			*			*		$nV/\sqrt{Hz}$
f_o = 100Hz		12			*			*		$nV/\sqrt{Hz}$
f_o = 1kHz		12			*			*		$nV/\sqrt{Hz}$
Current, 0.1Hz to 10Hz		50			*			*		pA, p-p
f_o = 10Hz		0.8			*			*		$pA/\sqrt{Hz}$
f_o = 100Hz		0.46			*			*		$pA/\sqrt{Hz}$
f_o = 1kHz		0.35			*			*		$pA/\sqrt{Hz}$
INPUT VOLTAGE RANGE										
Common-mode Voltage Range, linear operation		±(|V_{cc}|-3)		*			*			V
Common-mode Rejection at ±10V	110			*			*			dB
Maximum Safe Input Voltage		±V_{cc}			*			*		V
POWER SUPPLY										
Rated Voltage		±15			*			*		VDC
Voltage Range, derated performance	±3		±20	*		*	*		*	VDC
Quiescent Current		±2.5	±3.5		*	*		*	*	mA
TEMPERATURE RANGE										
Specification, (A, B, C)	-25		+85	*		*	*		*	°C
, (S)				-55		+125				°C
Operating, derated performance	-55		+125	*		*	*		*	
Storage	-65		+150	*		*	*		*	°C
θ junction-case		40			*			*		°C/W
θ junction-ambient		190			*			*		°C/W

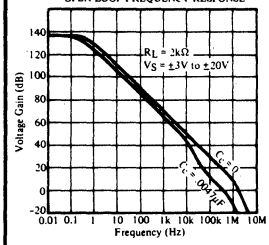
*Specification limits same as 3510A

(1) Temperature coefficient specifications: -25°C to +85°C for AM, BM, CM
-55°C to +125°C for SM

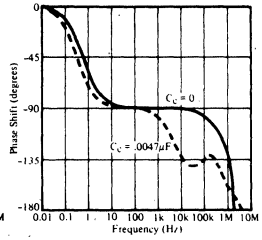
TYPICAL PERFORMANCE CURVES

Typical at T_A = 25°C and ±15VDC, unless otherwise noted.

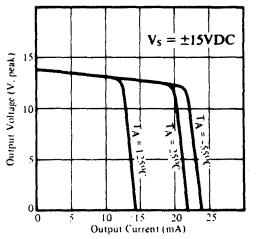
OPEN-LOOP FREQUENCY RESPONSE



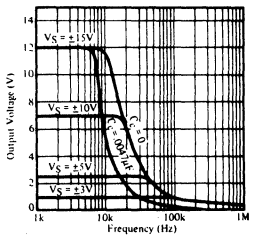
OPEN-LOOP PHASE RESPONSE



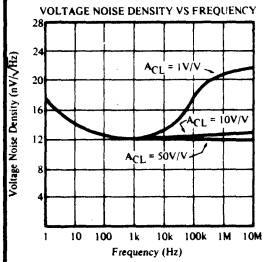
OUTPUT VOLTAGE VS OUTPUT CURRENT



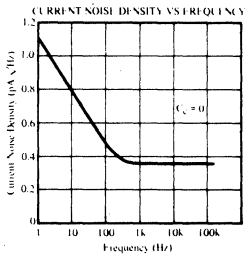
OUTPUT VOLTAGE VS FREQUENCY



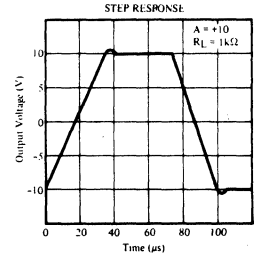
VOLTAGE NOISE DENSITY VS FREQUENCY



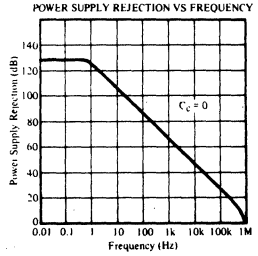
CURRENT NOISE DENSITY VS FREQUENCY



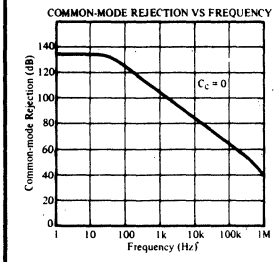
STEP RESPONSE



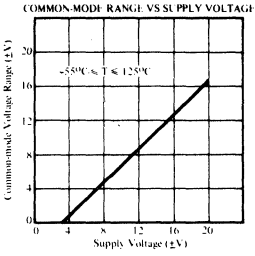
POWER SUPPLY REJECTION VS FREQUENCY



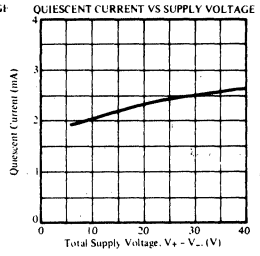
COMMON-MODE REJECTION VS FREQUENCY



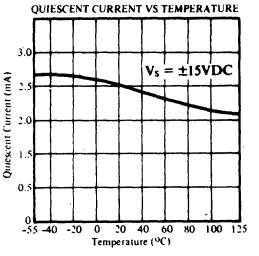
COMMON-MODE RANGE VS SUPPLY VOLTAGE



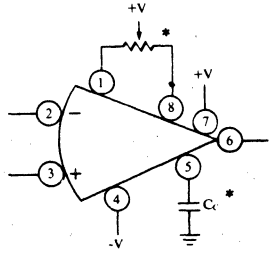
QUIESCENT CURRENT VS SUPPLY VOLTAGE



QUIESCENT CURRENT VS TEMPERATURE

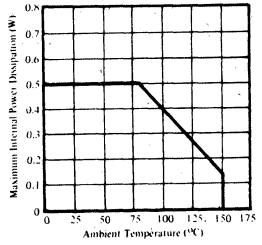


Amplifier Connections

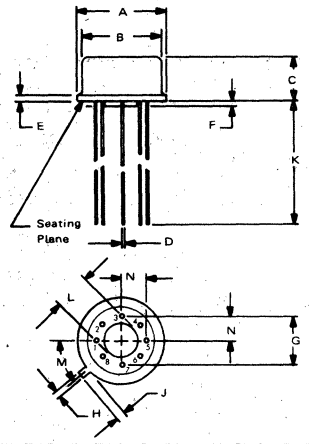


* Optional
See applications information

MAXIMUM POWER DISSIPATION VS. TEMPERATURE



MECHANICAL SPECIFICATIONS



TO-99

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTES: 1. Make no electrical connection to case.
2. Case may or may not be internally connected to V_{CC} (manufacturer's option).

APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT, NULLING AND DRIFT

Unlike some competitive models it is not necessary to null the offset voltage of the 3510 to achieve minimum voltage drift versus temperature. Drift of the 3510 is specified both nulled and unnulled.

In this op amp, the input offset voltage and the input offset voltage drift versus temperature are trimmed, at the wafer level, during manufacture. This feature, combined with the op amp's electrical design and high quality, closely controlled processing produce the low offset voltages and drifts indicated in the specifications. These figures are 100% guaranteed.

Should it be necessary to null the offset voltage to the lowest possible value this can be accomplished by inserting a potentiometer between pins 1 and 8. See "Alternate Nulling Techniques" for other methods. Nulling ultra-low offset amplifiers may, however, be undesirable when these factors are considered:

Cost of potentiometer and labor to install and null.

Decreased reliability through introduction of additional components.

Possible degradation of overall performance due to temperature coefficients of external nulling resistors (not true with 3510).

Nulling the offset voltage of most modern op amps will minimize offset voltage drift. In the 3510, an ultra low offset amplifier, a major portion of the offset voltage is trimmed during manufacture. Additional trimming by the user may increase the voltage drift slightly. Drift changes $0.33\mu V/°C$ for each $100\mu V$ of offset voltage nulled. Due to second order effects, the point of minimum voltage drift does not occur at the point of zero offset voltage in approximately 25% of the cases. In these instances, nulling the offset voltage may cause a slight increase in voltage drift, but not beyond the guaranteed nulled voltage drift specified. Nulling the offset voltage will decrease the voltage drift in approximately 75% of cases.

ALTERNATE NULLING TECHNIQUES

When it is essential to null offset voltage and achieve the lowest guaranteed voltage drift specifications, the following methods can be used:

Burr-Brown recommends nulling in a following stage as shown in Figure 1.

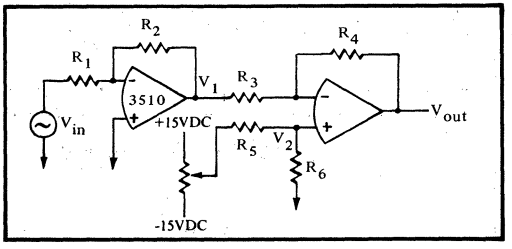


Figure 1. Multistage Nulling Circuit.

In this circuit, with $V_{in} = 0$, V_1 will be due to E_{os} and I_{bias} of 3510. The component of V_{out} due to V_1 is $\frac{V_1 R4}{R3}$. Resistors R_5 and R_6 are selected so that the component of V_{out} due to V_2 will cancel the component of V_{out} due to V_1. The specific values of R_5 and R_6 are selected to provide the desired range and resolution and will depend upon the model of the 3510 involved and the gain in each stage.

When only a single stage of amplification is used the following circuits could be employed.

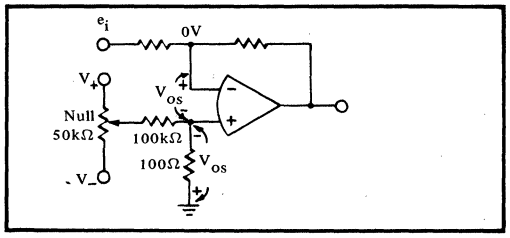


FIGURE 2. Inverting Amplifier.

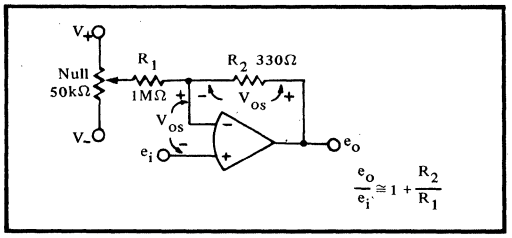


FIGURE 3. Noninverting Amplifier.

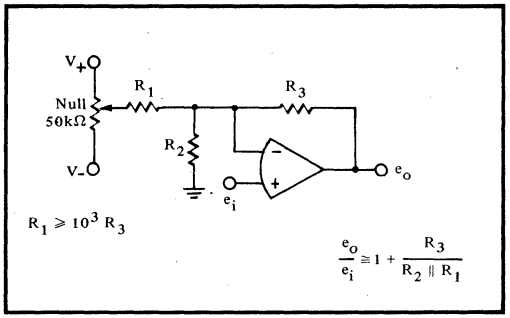


FIGURE 4. Follower Amplifier.

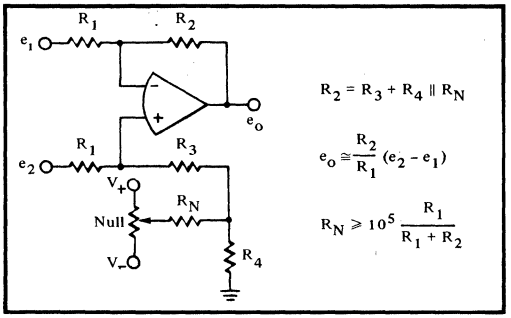


FIGURE 5. Difference Amplifier.

RESOLUTION OF NULLING POTENTIOMETER

One of the advantages of the 3510 is the ease of nulling the offset voltage, even with a low cost, single turn potentiometer. A single turn linear potentiometer can be used with good resolution. Unlike some competitive, low offset op amps, the 3510 does not require multiturn pots or fixed resistors padded with a pot to produce a high level of trim resolution.

Resolution and range of the offset trim potentiometer at various resistance values are shown in Table I.

TABLE I. Offset Potentiometer Effects

Potentiometer Value	Offset Adjustment Range		Resolution at Pot Center	Sensitivity of $\Delta V_{os}/\Delta T$ to Potentiometer (1) T.C.R. (2)
	10% - 90% Rotation	0% - 100% Rotation		
*100kΩ	±170μV	±2mV	1μV/% rotation	10^{-4}μV ppm/°C
20kΩ	±600μV	±2mV	3.5μV/% rotation	10^{-4}μV/ppm/°C
10kΩ	±800μV	±2mV	6μV/% rotation	10^{-4}μV/ppm/°C

* Recommended offset adjustment potentiometer.

(1) T.C.R. = temperature coefficient of resistance

(2) Sensitivity after nulling ±120μV of V_{os}; typically the sensitivity is one-half the value shown.

POTENTIOMETER

Because the external offset 100kΩ potentiometer parallels two internal 1kΩ resistors, the temperature coefficient of the potentiometer will affect the offset voltage temperature drift of the 3510 to a very small degree. In addition, the potentiometer halves have the same temperature coefficient, therefore the percent rotation does not drift. Sensitivity of the offset voltage to the external potentiometer is very low, only 10^{-4}μV/ppm/°C and must be added to the amplifier's drift. However, even when using a 100ppm industrial pot, this figure is ±0.01μV/°C and can be ignored.

THERMAL FEEDBACK

When an amplifier achieves the high performance levels of the 3510 some effects previously masked by larger error terms (and now reduced by the 3510's high accuracy, high performance and low error terms) may become observable. This situation exists with a condition referred to as thermal feedback.

Thermal feedback is an error generating condition which can be caused by the power dissipation and resultant temperature rise of the amplifier's output stage. This error is fed back to a previous stage of the amplifier and alters its usual operation. Normally the input stage is affected. This error is described as a change in input offset voltage per volt of output voltage change. When the 3510 has a 2kΩ load the specification is ±0.1μV/V.

This phenomena is most noticeable at frequencies below a few hertz and most easily observed on an oscilloscope. Thermal feedback can add a small error term to the "average" temperature effects normally described as input offset voltage drift versus temperature and input bias current versus temperature.

To minimize the effect of thermal feedback, the 3510 circuits are carefully laid out and thermally balanced to minimize thermal feedback.

THERMAL RESPONSE TIME

In low drift operational amplifiers like the 3510, thermal response time is an important performance parameter. In precision applications the response of the amplifier to warm-up or environmental change should be considered.

Figures 6 and 7 show typical thermal response of the 3510. Note that the offset voltage does not overshoot and that the response time is very short - less than three minutes. Some competitive low drift operational amplifiers require 15 minutes to warm up.

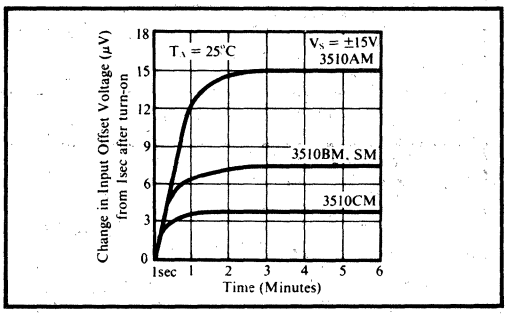


FIGURE 6. Warm-up Drift.

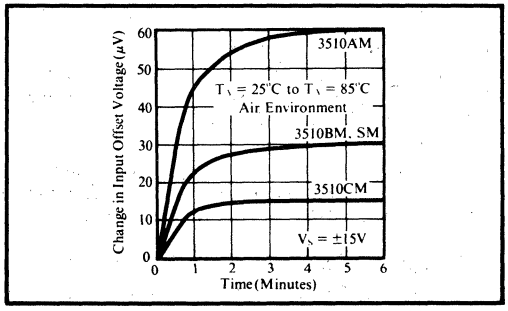


FIGURE 7. Offset Response to an Environmental Change.

NOISE

In a high performance amplifier such as the 3510, noise may well be the final and limiting criteria for system accuracy. See specifications and performance curves.

While the 3510 noise is very acceptable in low and mid-frequencies, it is fairly large above 100kHz. Whether or not this unique characteristic will cause user problems depends on the application of the 3510 and steps taken to reduce high frequency noise effects.

If circuitry following the 3510 does not respond to noise above 100kHz, no corrective steps need to be taken. This situation is common in applications where a 0.5V/μsec amplifier is satisfactory. When high frequency noise must be reduced, a low-pass filter should be installed in a stage following the 3510 (filtering at the 3510 itself has little effect).

Two high frequency filtering approaches are shown in Figures 8 and 9.

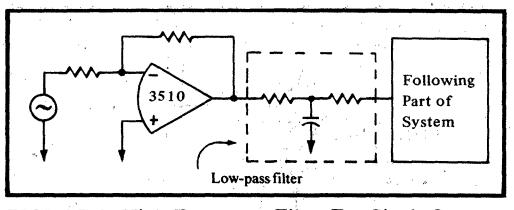


FIGURE 8. High Frequency Filter For Single Stage Amplifier.

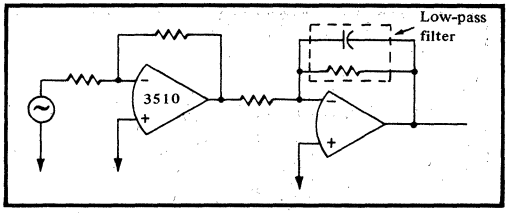


FIGURE 9. High Frequency Filter For Multistage Amplifier.

COMPENSATION

At closed loop gains above 10V/V, the 3510 op amp is stable without additional frequency compensation. The amplifier is compensated as shown in Figure 10 for gains below 10V/V.

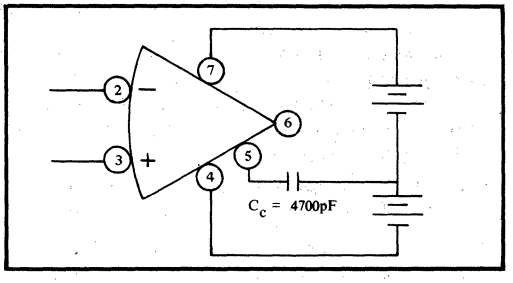


FIGURE 10. Amplifier Compensation Circuit.

Alternately, the capacitor may be connected between pin 5 and $+V_{cc}$ (pin 7) if the supply is well bypassed to ground.

SHORT CIRCUIT PROTECTION

The 3510 may be short circuited to ground continuously without damage. Output shorts other than to ground may be tolerated if the "Maximum Power Dissipation vs Temperature" ratings given in the performance curves are not exceeded. Power dissipation can be determined as the product of $(V_{cc} - V_{out}) \times I_{out}$. I_{out} under current limit conditions is specified in the "Output Voltage vs Output Current" performance curve.

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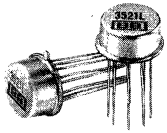


3521 SERIES
3522 SERIES

Ultra-Low Drift - FET Input OPERATIONAL AMPLIFIERS

FEATURES

- **ULTRA-LOW DRIFT, 1μV/°C max**
- **LOW INITIAL OFFSET VOLTAGE, 250μV, max**
- **LOW BIAS CURRENT, 1pA, max**
- **LOW NOISE**
- **HIGH COMMON-MODE REJECTION, 90dB, typ**
- **WIDE POWER SUPPLY RANGE, ±5VDC to ±20VDC**

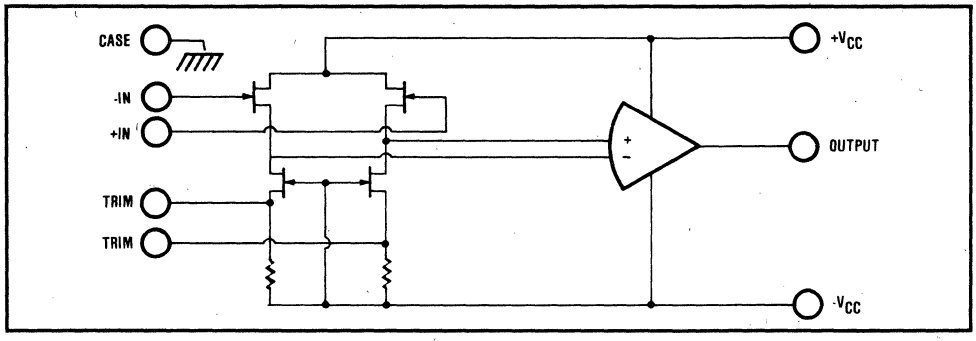
DESCRIPTION

With input offset voltage drifts as low as 1μV/°C, the Burr-Brown 3521 IC Operational Amplifier provides FET input performance combined with drift equal to the best bipolar IC's (e.g., BB3500E). The spectacular performance is achieved through truly state-of-the-art hybrid design and manufacturing, including monolithic FET pairs and active laser-trimming.

The 3521 and 3522 have an exceptionally fast thermal response. This fast warm-up is achieved without any heat-sinking.

While low drift and FET input impedance are the outstanding features of the 3521 and 3522 other specifications have not been compromised. They are internally compensated for unity-gain configuration and the initial voltage offset is guaranteed less than 250μV so for most applications the 3521 is ready to "plug-in and go." Like other low drift IC's from Burr-Brown the 3521 and 3522 have ample speed and bandwidth for most any application. (Slew rate = 0.6V/μsec). The high common-mode rejection ratio (90dB, typ.) enables them to be used as a 0.01% accurate buffer with low drift and extremely-high input impedance. The 3521/3522 also have very-low input noise to complement the low drift. The output is current limited to provide protection for continuous output shorts to common.

The 3521/3522 are pin-compatible with 741-type amplifiers, but provide FET input performance with ultra-low drift while exceeding all other specifications for general purpose operational amplifiers of the 741-type. Burr-Brown tests and guarantees all units to meet all max/min specifications.



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SPECIFICATIONS

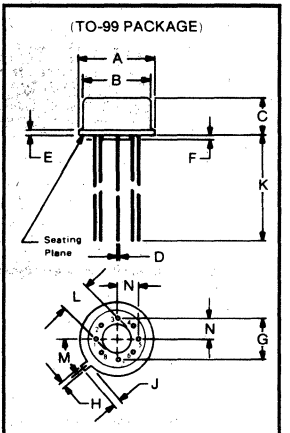
ELECTRICAL

Typical at +25°C and ±15VDC power supply unless otherwise noted.

MODELS	3521H	3521J	3521K	3521L	3521R
OPEN-LOOP GAIN, DC					
Rated Load, min	94dB	*	*	*	*
RATED OUTPUT					
Voltage, min	+10V	*	*	*	*
Current, min	±10mA	*	*	*	*
Output Impedance	100Ω	*	*	*	*
FREQUENCY RESPONSE					
Unity Gain, Open-Loop	1.5MHz	*	*	*	*
Full Power Response, min	10kHz	*	*	*	*
Slew Rate, min	0.6V/μsec	*	*	*	*
INPUT OFFSET VOLTAGE					
Initial Offset, 25°C, max	±500μV	250μV	250μV	250μV	250μV
vs Temp (0°C to +70°C), **max	±10μV/°C	±5μV/°C	2μV/°C	±1μV/°C	±5μV/°C
vs Temp (-25°C to +85°C)	±15μV/°C	±8μV/°C	±4μV/°C	±2μV/°C	±2μV/°C
vs Supply Voltage	±25μV/V	*	*	*	*
vs Time	5μV/mo	*	*	*	*
INPUT BIAS CURRENT					
Initial Bias, 25°C, max	-20pA	*	-15pA	-10pA	*
(doubles every +10°C)					
vs Supply Voltage	1pA/V	*	*	*	*
INPUT DIFFERENCE CURRENT					
Initial difference, 25°C	±2pA	*	*	*	*
INPUT IMPEDANCE					
Differential	$10^{11}\Omega$	*	*	*	*
Common-mode	$10^{12}\Omega$	*	*	*	*
INPUT NOISE					
Voltage, 0.01Hz - 10Hz, p-p	4μV	*	*	*	*
Voltage, 10Hz - 1kHz, rms	2μV	*	*	*	*
Current, 0.01Hz - 10Hz, p-p	0.3pA	*	*	*	*
Current, 10Hz - 1kHz, rms	0.6pA	*	*	*	*
INPUT VOLTAGE RANGE					
Common-mode Voltage	±10V	*	*	*	*
Common-mode Rejection	90dB	*	*	*	*
Max. Safe Input Voltage	±Supply	*	*	*	*
POWER SUPPLY					
Rated Voltage	±15VDC	*	*	*	*
Voltage Range, derated	±5 to ±20VDC	*	*	*	*
Current, quiescent	±4mA	*	*	*	*
TEMPERATURE RANGE					
Specification	0°C to +70°C	*	*	*	-55°C to +125°C
Operating	-25°C to +85°C	*	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*	*

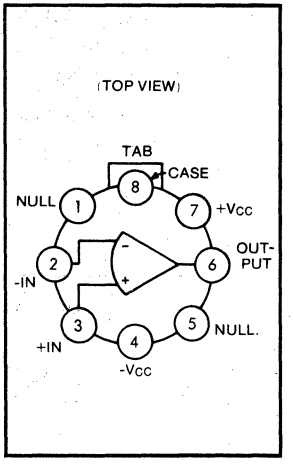
*Specification same as for 3521H.
**-55°C to +125°C for 3521R.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53*
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	–	12.7	–
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM



ELECTRICAL (CONT)

Typical at +25°C and ±15VDC power supply unless otherwise noted.

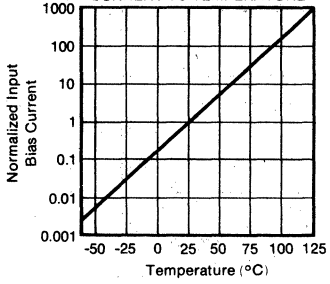
MODELS	3522J	3522K	3522L	3522S
OPEN-LOOP GAIN, DC				
Rated Load, min	94dB	*	*	*
RATED OUTPUT				
Voltage, min	±10V	*	*	*
Current, min	±10mA	*	*	*
Output Impedance	100Ω	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Open-loop	1MHz	*	*	*
Full Power Response, min	10kHz	*	*	*
Slew Rate, min	0.6V/μsec	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, 25°C, max	±1mV	±500μV	±500μV	±500μV
vs Temp (0°C to +70°C), max	±50μV/°C	±10μV/°C	±10μV/°C	
(-55°C to +125°C), max				±25μV/°C
vs Supply Voltage	±25μV/mo	*	*	*
vs Time	±10μV/mo	*	*	*
INPUT BIAS CURRENT**				
Input Bias, 25°C, max	-10pA	-5pA	-1pA	-5pA
(doubles every +10°C)				
vs Supply Voltage	±0.1pA/V	*	*	*
INPUT DIFFERENCE CURRENT				
Initial Difference, +25°C	±2pA	±1pA	±0.5pA	±1pA
INPUT IMPEDANCE				
Differential	$10^{11}\Omega$	*	*	*
Common-mode	$10^{12}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.01Hz to 10Hz, p-p	4μV	*	*	*
Voltage, 10Hz to 1kHz, rms	2μV	*	*	*
Current, 0.01Hz to 10Hz, p-p	0.3pA	*	*	*
Current, 10Hz to 1kHz, rms	0.6pA	*	*	*
INPUT VOLTAGE RANGE				
Common-mode Voltage	±10V	*	*	*
Common-mode Rejection	90dB	*	*	*
Max. Safe Input Voltage	±Supply	*	*	*
POWER SUPPLY				
Rated Voltage	±15VDC	*	*	*
Voltage Range, derated	±5VDC to ±20VDC	*	*	*
Current, quiescent	±4mA	*	*	*
TEMPERATURE RANGE				
Specification	0°C to +70°C	*	*	-55°C to +125°C
Operating	-25°C to +85°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*

*Specification same as for 3522J.
**After Warm-Up.

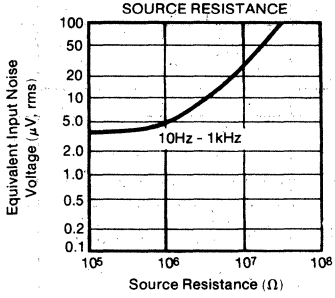
TYPICAL PERFORMANCE CURVES

(At +25°C and ±15VDC unless otherwise specified)

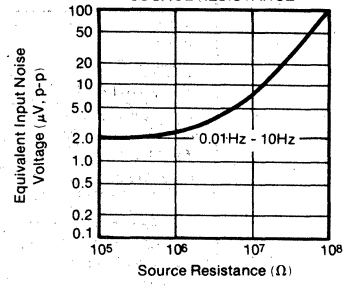
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



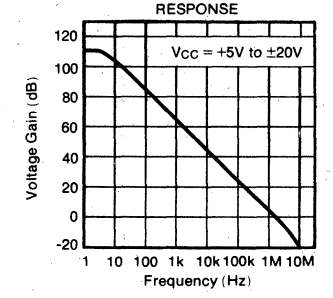
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



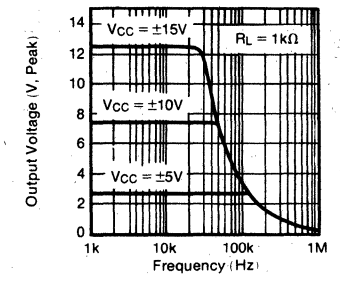
P-P INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



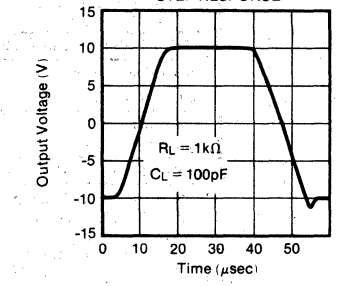
OPEN-LOOP FREQUENCY RESPONSE



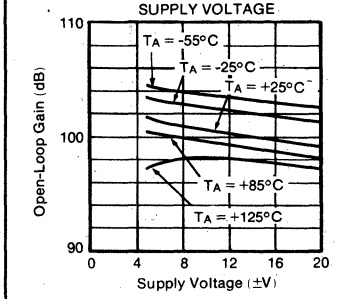
OUTPUT VOLTAGE VS FREQUENCY



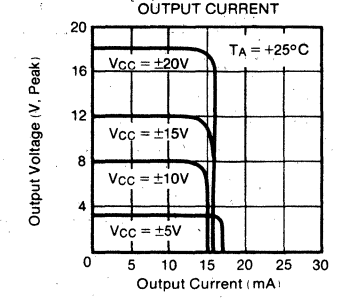
VOLTAGE FOLLOWER STEP RESPONSE



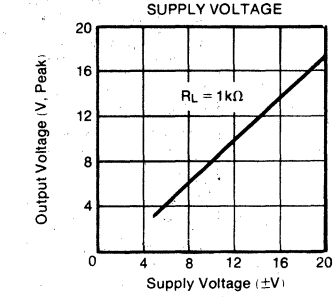
VOLTAGE GAIN VS SUPPLY VOLTAGE



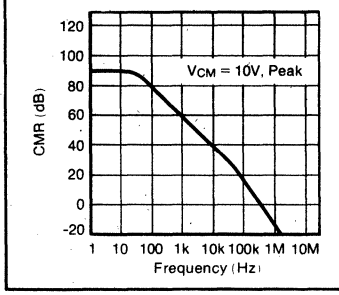
OUTPUT VOLTAGE VS OUTPUT CURRENT



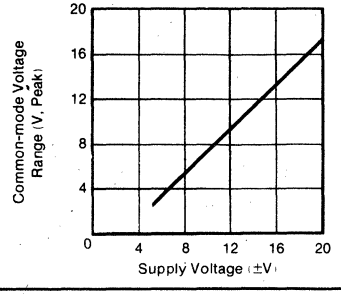
OUTPUT VOLTAGE VS SUPPLY VOLTAGE



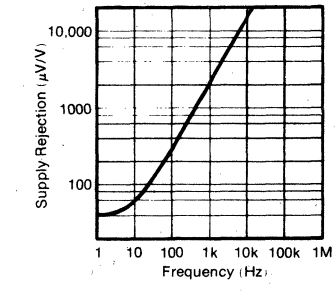
COMMON-MODE REJECTION VS FREQUENCY



COMMON-MODE RANGE VS SUPPLY VOLTAGE



POWER SUPPLY REJECTION VS FREQUENCY



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the 3521/3522. A low drift specification would be of little value if the amplifier took several hours to stabilize after turn-on or ambient temperature change. The TO-99 packaging is particularly well suited for devices requiring fast thermal response. Figure 1 shows the typical warm-up drift of the 3521. Note that the offset voltage has stabilized in less than 4 minutes. Similar warm-up times for some discrete low drift operational amplifiers range from 7 to 15 minutes.

Offset voltage response to thermal shock can provide some real suprises, particularly for amplifiers packaged in discrete modules. Again the TO-99 package proves superior. Figure 2 shows that the response to thermal shock settles very quickly. The 3521/3522 quickly and smoothly assumes a new value of offset voltage as dictated by the drift specification.

BIAS CURRENT EFFECTS

The low bias currents and offset currents of FET input stages overcome most of the source resistance limitations of bipolar operational amplifiers. However, for very large source resistances or large unbalances in source resistance (5MΩ and up) the input offset voltage and drift will be affected as shown in Figures 3 and 4.

COMMON-MODE PROPERTIES

The input stage of the 3521 is a monolithic FET pair, which affords very good matching between the two input transistors. This close matching makes the 90dB common-mode rejection ratio (CMRR) possible. Because of its excellent common-mode properties the 3521 may be used as a 0.01% accurate buffer amplifier for inputs between ±10V. Figure 5 below illustrates typical common-mode performance of the 3521.

POWER SUPPLIES AND DRIFTS

Note that a power supply change of 40mV will typically introduce an input offset voltage change of 1μV. Since power supply drift will have the same effect as offset voltage drift, the power supply temperature coefficients of ±15V supplies should be about 0.1%/°C for optimum drift performance of the 3521L.

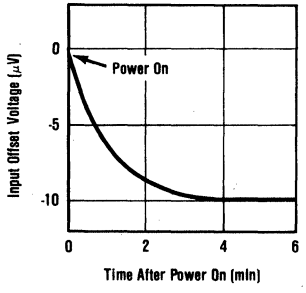


FIGURE 1. Typical Warm-up Drift.

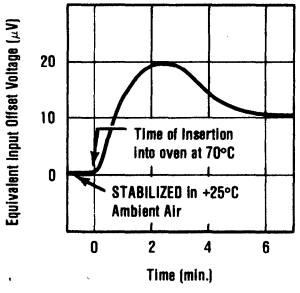
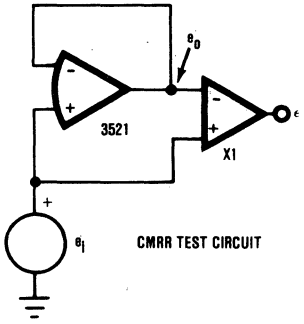


FIGURE 2. Effect of Thermal Shock on Offset Voltage.



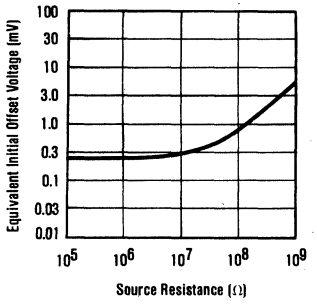


FIGURE 3. Typical Effects of Source Resistance on Initial Offset Voltage.

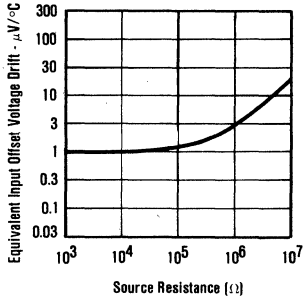


FIGURE 4. Typical Effects of Source Resistance on Equivalent Input Offset Voltage Drift.

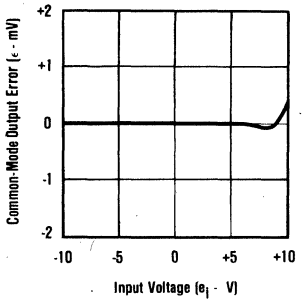


FIGURE 5. Common-Mode Performance.

WIRING CONSIDERATIONS (Shielding and Guarding)

The ultra-low drift, very-low bias current and high input impedance make the 3521/3522 well suited to a number of unique applications. However, careless signal wiring can degrade "system" performance several orders of magnitude below the 3521/3522 capability.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large value feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the units. Perhaps more important, unbalanced leakage paths (when is leakage ever balanced?) can generate significant input offset voltages when large source impedances (100kΩ and up) are involved. To avoid leakage problems, it is recommended that the inputs of the 3521 be wired to teflon standoffs. If the unit must be soldered directly into a printed circuit board, utmost care should be used in designing the board layout. A "guard" pattern should completely surround the two input leads and be connected to a low impedance point at the common-mode input voltage. Figure 6 shows suggested guard connections for various amplifier feedback configurations. The amplifier case should be connected to any input shield or guard via pin 8.

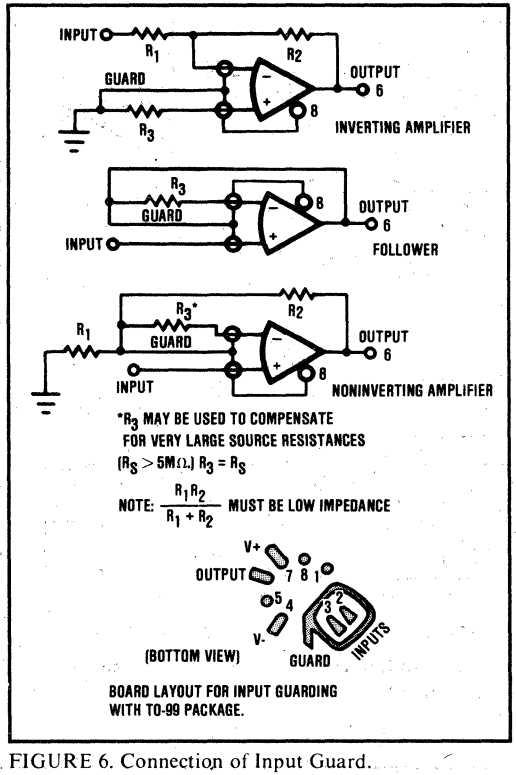


FIGURE 6. Connection of Input Guard.

OFFSET VOLTAGE ADJUSTMENT

The 3521 has a low initial offset (250μV) compatible with its low drift. However, some high accuracy applications may require external nulling of even this small initial offset voltage. Virtually any offset voltage adjustment method can increase offset voltage drift unless some care is used. For example, the initial offset voltage of most monolithic op amps (BB 3500, 741-types, 101, etc.) may be nulled using a single potentiometer, but offset voltage drift is typically increased by about 3μV/°C for each mV of offset voltage adjust. This same relationship will also hold for the 3521.

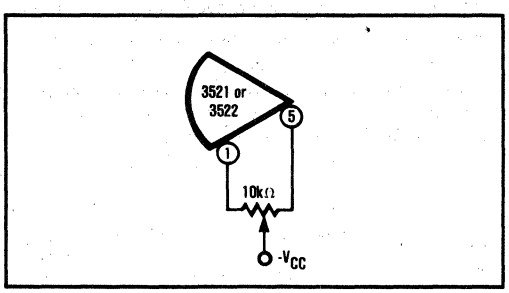


FIGURE 7. Single Potentiometer Adjust at Op Amp Trim Terminals.

Advantages:

1. Simplest circuit.
2. Compatible with most IC op amps.

Disadvantages:

1. Drift increased by circuit about 0.75μV/°C for 3521.

TEMPERATURE COMPENSATED POTENTIOMETER OFFSET VOLTAGE ADJUST

If the circuit in Figure 7 is replaced with a circuit which "drifts" with temperature, nulling the offset voltage will not increase the drift by so large an amount. The circuit shown in Figure 8 may be used to null initial offset voltage and drift will increase only about 0.5μV/°C for each mV of offset adjust. In the case of the 3521, this zeroing circuit will typically add at most 0.14μV/°C.

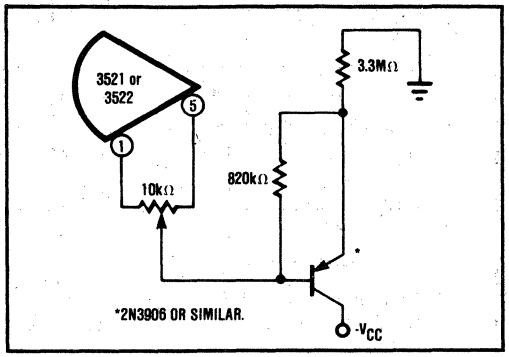
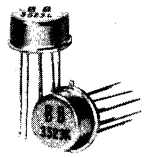


FIGURE 8. Temperature Compensated Potentiometer Null.

BURR-BROWN®

3523 SERIES



Ultra-Low Bias Current FET OPERATIONAL AMPLIFIERS

FEATURES

- BIAS CURRENT, 0.1pA, max
- OFFSET VOLTAGE, 500μV, max
- VOLTAGE DRIFT, 25μV/°C, max
- INPUT IMPEDANCE, $10^{13}\Omega$
- Noise (10Hz), 0.003pA, p-p

DESCRIPTION

The Burr-Brown 3523 Series amplifiers are the first IC operational amplifiers to achieve sub-picoampere input currents without exhibiting excessive offset voltage, voltage drift and voltage noise. The high common-mode rejection, ultra-low bias current, and $10^{13}\Omega$ input impedance of the 3523 make it the best choice for a variety of buffer and electrometer applications. These include pH measurement, photocurrent amplification, long term integration, and low droop sample/hold or track/hold applications. Because its input offset voltage is laser-trimmed to less than 500μV, the 3523 can usually be used without offset nulling. This is a distinct advantage in applications where it is desired to locate the 3523 near the signal source (e.g., in a signal probe).

The package of the 3523 is designed to preserve its ability to measure ultra-low currents and to avoid noise pickup. The case guard (pin no. 8) may be connected to a point which is at signal potential. This minimizes leakage current input from pins to case. Also, it shields the amplifier's sensitive input circuitry from power line frequency "hum", switching transients, and other sources of electrical noise.

Bias current specifications of the 3523 are guaranteed after warm-up in ambient air with no heat sink. Thus, the ultra-low bias current specifications become even more significant since internal power dissipation can easily raise case temperature by 20°C in many applications.

The bias current on many FET amplifiers is a strong function of applied common-mode voltage. This is not the case with the 3523. The input stage design of the 3523 make the input bias current virtually independent of the common-mode voltage over its full range.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

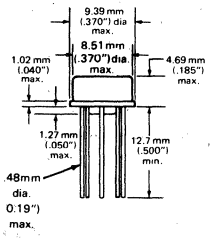
Specifications typical at 25°C and ±15 Vdc Power Supply unless otherwise noted.

ELECTRICAL

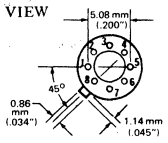
MODELS	3523J	3523K	3523L
OPEN LOOP GAIN, dc no load		100 dB	
1 kΩ, load, min		94 dB	
RATED OUTPUT			
Voltage, min		±10 V	
Current min		±10 mA	
Output Impedance		100 Ω	
FREQUENCY RESPONSE			
Unity Gain, Open Loop		1 MHz	
Full Power Response, min		10 kHz	
Slew Rate, min		0.6 V/μsec	
INPUT OFFSET VOLTAGE			
Initial Offset, 25°C, max	±1 mV	±500 μV	±500 μV
vs. Temp (0° to 70°C), max	±50 μV/°C	±25 μV/°C	±25 μV/°C
vs. Supply Voltage		±25 μV/V	
vs. Time		±5 μV/mo	
INPUT BIAS CURRENT			
Initial bias, 25°C, max	-0.5 pA	-0.25 pA	-0.1 pA
(doubles every +10°C)			
vs. Supply Voltage		±0.01 pA/V	
INPUT DIFFERENCE CURRENT			
Initial difference, 25°C	±0.2 pA	±0.1 pA	±0.05 pA
INPUT IMPEDANCE			
Differential		10^{12} Ω	
Common Mode		10^{13} Ω	
INPUT NOISE			
Voltage, .01 Hz - 10 Hz, p-p		4 μV	
10 Hz - 10 kHz, rms		2 μV	
Current, .01 Hz - 10 Hz, p-p		.003 pA	
10 Hz - 10 kHz, rms		0.01 pA	
INPUT VOLTAGE RANGE			
Common Mode Voltage		±(|V_S|-2) V	
Common Mode Rejection @ 10V		80 dB	
Max. Safe Input Voltage		± Supply	
POWER SUPPLY			
Rated Voltage		±15 Vdc	
Voltage Range, derated		±5 to ±20 Vdc	
Current, quiescent		±4 mA	
TEMPERATURE RANGE			
Specification		0° to +70°C	
Operating		-55° to +125°	
Storage		-65° to +150°C	

MECHANICAL

TO-99



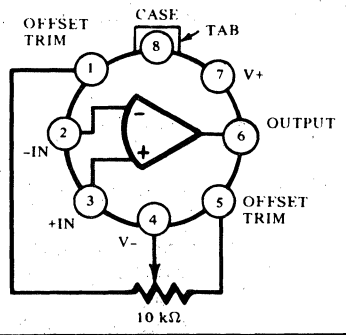
BOTTOM VIEW



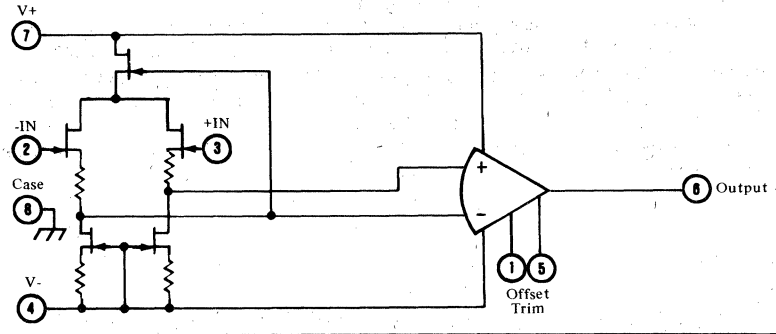
Dimensions in inches are in parentheses. Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

CONNECTION DIAGRAM

TOP VIEW



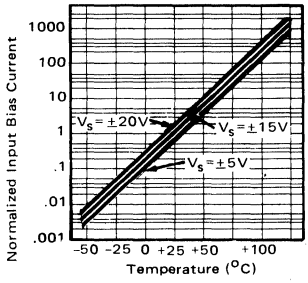
SIMPLIFIED SCHEMATIC



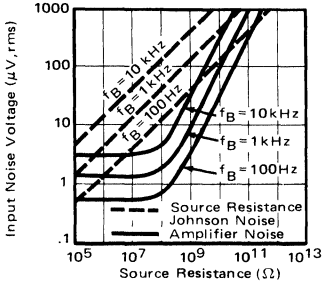
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

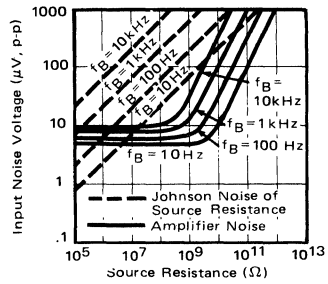
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



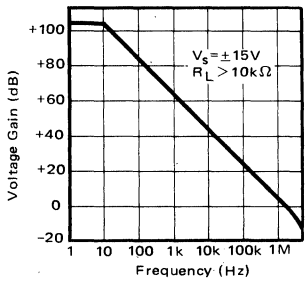
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



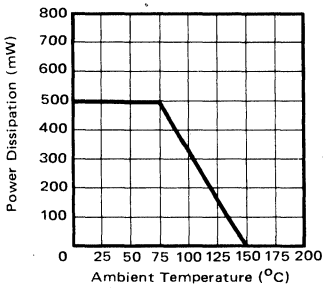
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



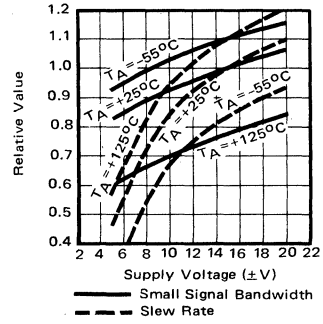
OPEN LOOP FREQUENCY REPONSE



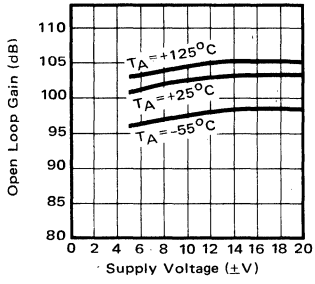
MAXIMUM POWER DISSIPATION



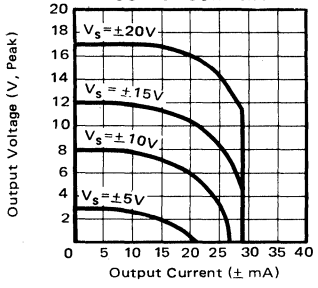
FREQUENCY CHARACTERISTICS vs. SUPPLY VOLTAGE



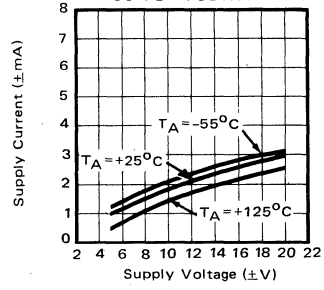
OPEN LOOP GAIN vs. SUPPLY VOLTAGE



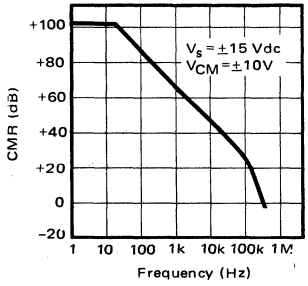
OUTPUT VOLTAGE vs. OUTPUT CURRENT



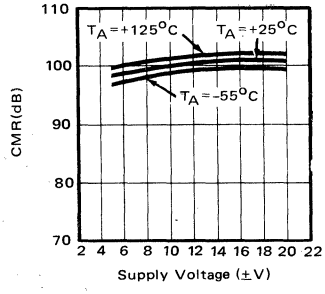
SUPPLY CURRENT vs. SUPPLY VOLTAGE



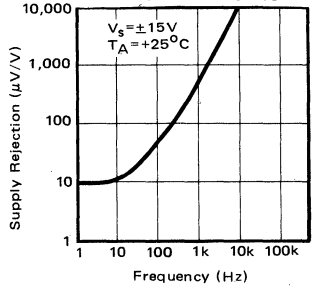
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE REJECTION vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



APPLICATION CONSIDERATIONS

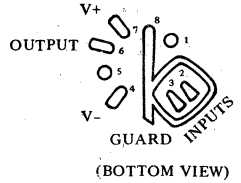
The ultra-low bias current and high input impedance of the 3523 are well suited to a number of challenging applications. In order to fully benefit from the outstanding specifications of this unit careful layout, shielding and guarding is required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the 3523.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the 3523 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pick-up.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3523. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the 3523 be wired to a Telfon standoff. If this is not done and instead the 3523 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential. (See Figure 1) The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents.

Figures 2, 3, and 4 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in ultra low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.



Board layout for Input Guarding with Guarded TO-99 Package.

FIGURE 1. Connection of Case Guard and Input Guard.

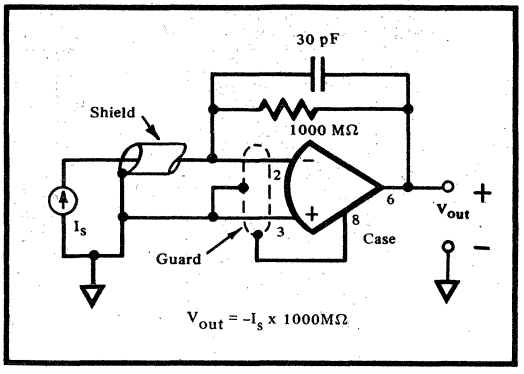


FIGURE 2. Ultra Low Current to Voltage Converter.

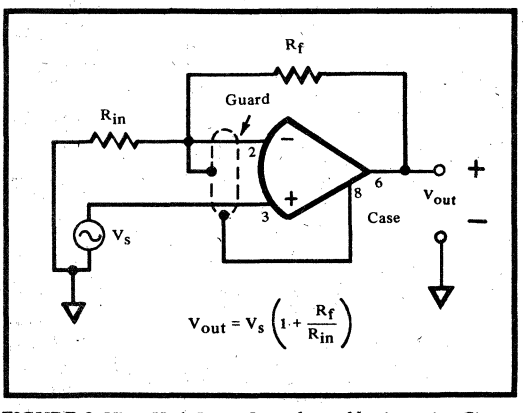


FIGURE 3. Ultra High Input Impedance Noninverting Circuit.

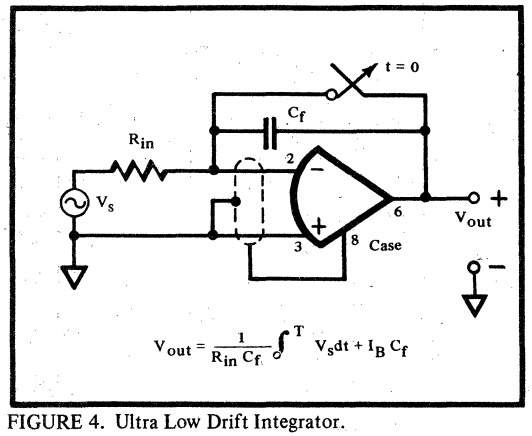


FIGURE 4. Ultra Low Drift Integrator.

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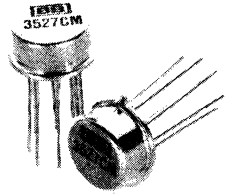


3527

Low Drift - Low Bias Current FET Input OPERATIONAL AMPLIFIER

FEATURES

- LOWER PRICED
- ULTRA-LOW DRIFT, 2μV/°C, max
- LOW INITIAL OFFSET VOLTAGE, 250μV, max
- LOW BIAS CURRENT, 2pA, max
- LOW NOISE

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- LONG TERM INTEGRATION
- LOW DROOP SAMPLE/HOLD CIRCUITS
- PRECISION VOLTAGE AMPLIFICATION
- HIGH INPUT RESISTANCE BUFFER

DESCRIPTION

The Burr-Brown 3527 is a precision operational amplifier. It offers excellent performance at moderate cost through the use of hybrid construction, monolithic ICs, matched FETs, thin-film resistors, and active laser trimming.

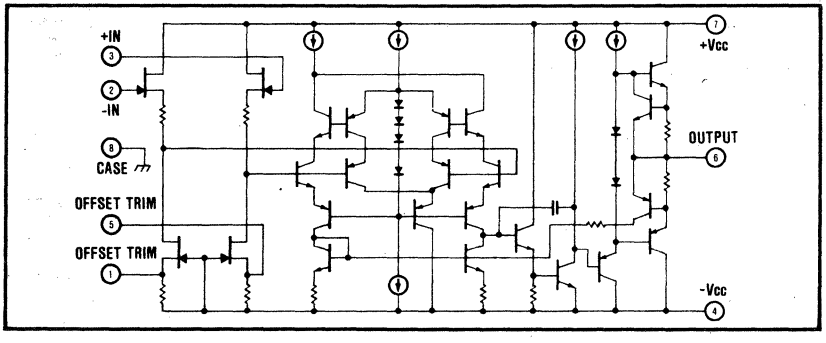
The 3527 low, initial offset voltage (250μV max) allows higher design accuracy at lower installed cost. Costly pots and external nulling of the offset voltage are not required for most applications. Also, higher system reliability is achieved by using fewer parts.

The offset voltage temperature drift of the 3527 is exceptionally low (2μV/°C max) and is compatible with the best bipolar amplifiers (BB3500E). It is achieved by laser adjusting the offset during manufacture and means that high system accuracy is maintained over the temperature range.

The low bias current (guaranteed 2pA max) allows the use of larger feedback resistor values, and smaller bias current errors are realizable.

Of course, all the other desirable features of high quality op amps are engineered into the 3527. It has low input noise, is free from latch up, is short circuit protected for continuous output shorts to common, is internally compensated for unity gain stability, and is pin compatible with 741 amplifiers. Guarding is achieved by the pin 8 case connection.

For increased reliability screening, consult Burr-Brown.



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SPECIFICATIONS

ELECTRICAL

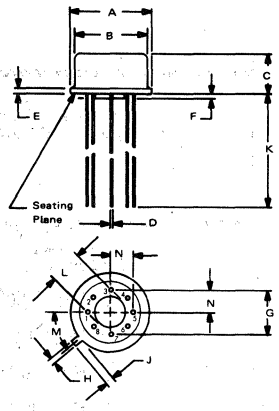
Specifications typical at T_A = 25°C and ±15VDC supplies, unless otherwise noted.

MODELS	3527AM			3527BM			3527CM			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN, DC				*	*		*	*		
No Load		112								dB
R_L = 2kΩ	100	108								dB
RATED OUTPUT				*	*		*	*		
Voltage	±10	±12								V
Current	±10	±20								mA
Output Impedance		600								Ω
Load Capacitance		1000								pF
FREQUENCY RESPONSE				*	*		*	*		
Unity Gain, Open Loop		1								MHz
Full Power Response	10	14								kHz
Slew Rate	0.6	0.9								V/μsec
Settling Time (0.01%)		45								μsec
INPUT OFFSET VOLTAGE										
Initial Offset, 25°C		±200	±500		±100	±250		±100	±250	μV
vs. Temp. (-25°C to +85°C)		±5	±10		±2	±5		±1	±2	μV/°C
vs. Supply Voltage		±75			*			*		μV/V
vs. Time		±20			*			*		μV/mo
INPUT BIAS CURRENT										
Initial Bias, 25°C		-2	-5		-0.7	-2		-2	-5	pA
vs. Temp		**			**			**		
vs. Supply Voltage		±5			*			*		pA/V
INPUT DIFFERENCE CURRENT					*			*		
Initial Difference, 25°C		±0.3								pA
INPUT IMPEDANCE					*			*		
Differential		10^{12}								Ω
Common-mode		10^{15}								Ω
INPUT NOISE					*			*		
Voltage, f_o = 10Hz		75								nV/√Hz
f_o = 100Hz		35								nV/√Hz
f_o = 1kHz		30								nV/√Hz
f_o = 10kHz		25								nV/√Hz
0.3Hz to 10Hz, p-p		2.6								μV
10Hz to 10kHz, rms		3								μV
Current, 0.3Hz to 10Hz, p-p		15								fA
10Hz to 10kHz, rms		60								fA
INPUT VOLTAGE RANGE					*			*		
Common-mode Voltage Range		±(|Vs|-3)								V
Common-mode Rejection at ±10V		76								dB
Max. Safe Input Voltage		±Vs								VDC
POWER SUPPLY				*	*	*	*	*	*	
Rated Voltage		±15								VDC
Voltage Range, derated performance	±5		±20							VDC
Current, quiescent		2.6	4							mA
TEMPERATURE RANGE (ambient)				*		*	*		*	
Specification	-25		+85							°C
Operating	-55		+125							°C
Storage	-65		+150							°C
θ junction-ambient		235								°C/W
PRICE										
1-24		12.25			16.25			28.25		$
100-999		7.95			10.65			19.85		

*Specifications same as for 3527AM.
**Doubles every +10°C.

MECHANICAL TO-99 PACKAGE

Order Number: 3527AM, 3527BM, 3527CM Weight: 1 gram



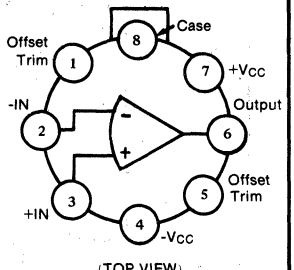
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CONNECTION DIAGRAM

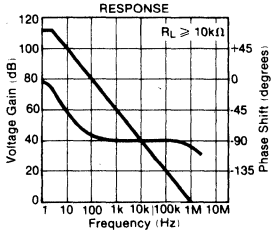


(TOP VIEW)

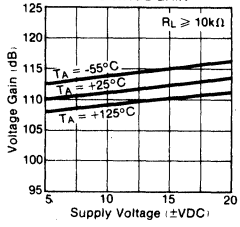
TYPICAL PERFORMANCE CURVES

At T_A = +25°C and ±15VDC supplies, unless otherwise noted.

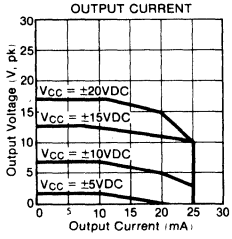
OPEN-LOOP FREQUENCY RESPONSE



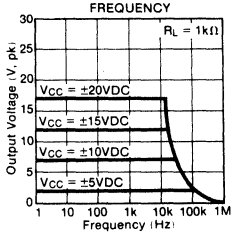
VOLTAGE GAIN



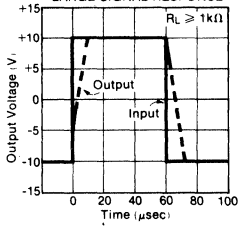
OUTPUT VOLTAGE vs OUTPUT CURRENT



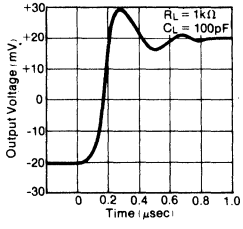
OUTPUT VOLTAGE vs FREQUENCY



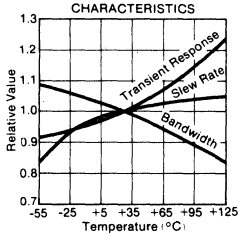
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



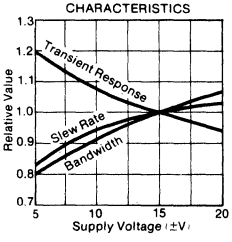
TRANSIENT RESPONSE



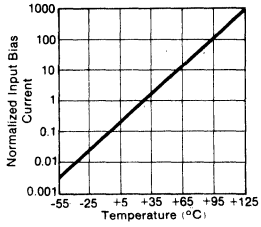
FREQUENCY CHARACTERISTICS



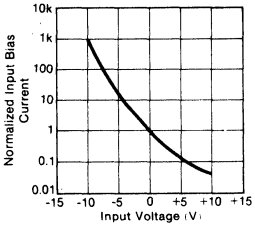
FREQUENCY CHARACTERISTICS



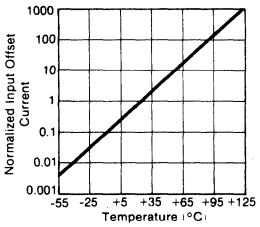
INPUT BIAS CURRENT



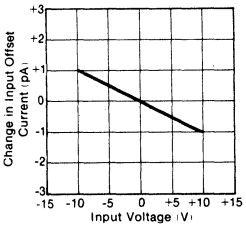
INPUT BIAS CURRENT



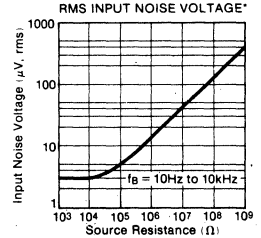
INPUT OFFSET CURRENT



INPUT OFFSET CURRENT

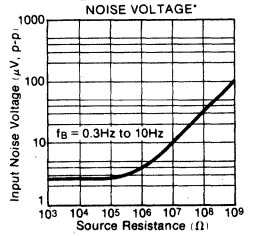


RMS INPUT NOISE VOLTAGE*

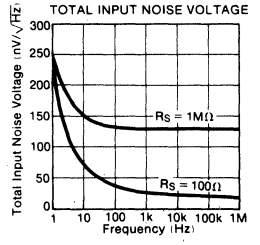


*Includes contribution from source resistance.

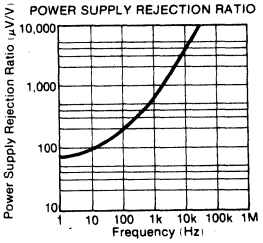
PEAK-TO-PEAK INPUT NOISE VOLTAGE*



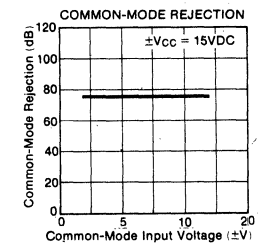
TOTAL INPUT NOISE VOLTAGE



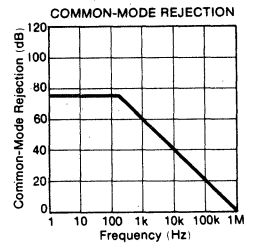
POWER SUPPLY REJECTION RATIO



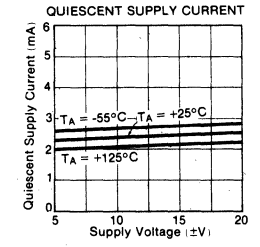
COMMON-MODE REJECTION



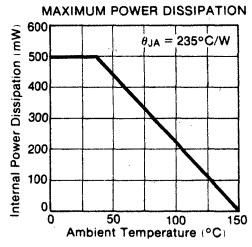
COMMON-MODE REJECTION



QUIESCENT SUPPLY CURRENT



MAXIMUM POWER DISSIPATION



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the 3527. A low drift specification would be of little value if the amplifier took several hours to stabilize after turn-on or ambient temperature change. The TO-99 packaging is particularly well suited for devices requiring fast thermal response. Figure 1 shows the typical warm-up drift of the 3527. Note that the offset voltage has stabilized in less than 1 minute. Similar warm-up times for some low drift operational amplifiers ranges from 2 to 15 minutes.

Offset voltage response to thermal shock can provide some real surprises, particularly for amplifiers packaged in discrete modules. Again the 3527 TO-99 package proves superior. Figure 2 shows that the response to thermal shock settles very quickly. The 3527 quickly and smoothly assumes a new value of offset voltage as dictated by the drift specification.

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the 3527 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the 3527.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3527. To avoid leakage problems, it is recommended that the signal input lead of the 3527 be wired to a Teflon standoff. If the 3527 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 3 illustrates the use of the guard.

OFFSET VOLTAGE ADJUSTMENT

Although the 3527 has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. For each microvolt of offset adjusted, an additional drift of $\pm 0.002\mu V/°C$ is induced.

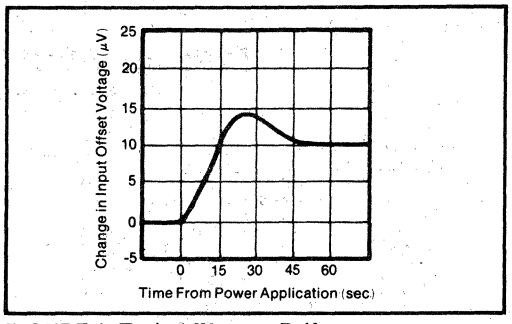


FIGURE 1. Typical Warmup Drift.

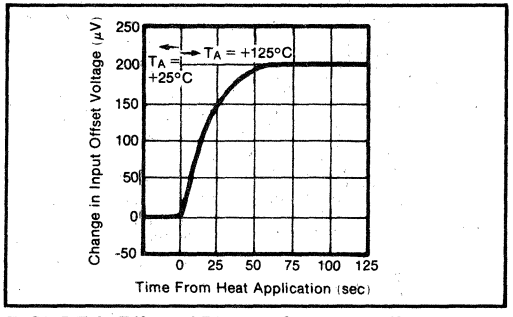


FIGURE 2. Effect of Thermal Shock on Offset Voltage.

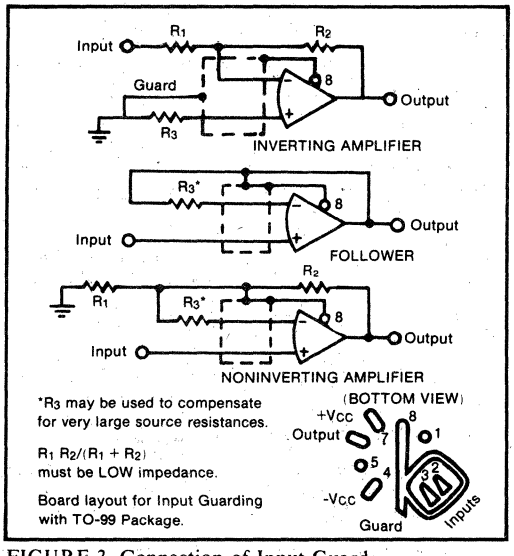


FIGURE 3. Connection of Input Guard.

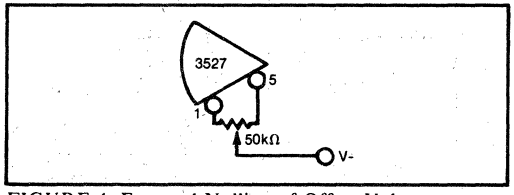
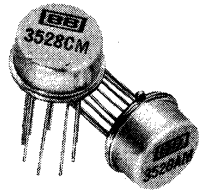


FIGURE 4. External Nulling of Offset Voltage.

BURR-BROWN®

3528



Ultra Low Bias Current FET OPERATIONAL AMPLIFIER

FEATURES

- 75fA MAX INPUT BIAS CURRENT
- 250μV MAX OFFSET VOLTAGE
- 5μV/°C MAX OFFSET VOLTAGE DRIFT

APPLICATIONS

- PHOTODIODE AMPLIFIER
- PHOTOMULTIPLIER TUBE AMPLIFIER
- LOW DRIFT INTEGRATOR
- CURRENT-TO-VOLTAGE CONVERTER

DESCRIPTION

An excellent combination of specifications for applications requiring ultra low input bias currents are provided by the 3528 amplifier family. These applications include photometers, selective ion detectors, long term integrators and low-droop sample hold circuits.

The 3528 is unique in that in addition to providing bias currents as low as 75fA (3528CM) it also provides very low offset voltage drift (5μV/°C max, 3528BM) and offset voltage (250μV, 3528BM). Thus, user trimming offset voltage with an external potentiometer is usually avoided.

The output is protected from damage due to short circuits to ground or either supply and the unit is specified over the full -25°C to +85°C temperature range rather than the more limited 0°C to 70°C range.

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ELECTRICAL SPECIFICATIONS

At T_A = 25°C and $\pm V_{cc}$ = ±15VDC unless otherwise noted.

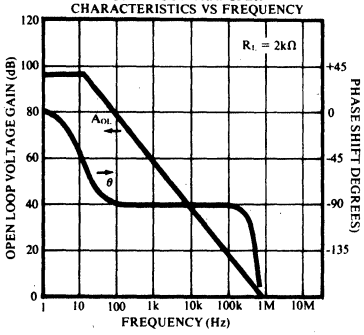
PARAMETER	CONDITIONS	3528AM			3528BM			3528CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN LOOP GAIN, DC											
$R_L \geq 2k$	V_o = 20V p-p	88	93		92	95		90	93		dB
$R_L \geq 10k$	V_o = 20V p-p	94	114		100	*		98	*		
RATED OUTPUT											
Voltage	R_L = 2kΩ	±10	±12		*	*		*	*		V
	R_L = 10k	±12	±13		*	*		*	*		V
Current	V_o = ±10V	±5	±10		*	*		*	*		mA
Output Resistance Open Loop	f = DC		1.5	3		*	*		*	*	kΩ
Short Circuit Current	R_L = 0Ω		19			*			*		mA
DYNAMIC RESPONSE											
Bandwidth, Unity Gain	Small Signal		0.7			*			*		MHz
Full Power Bandwidth	R_L = 2kΩ	5	11		*	*		*	*		kHz
Slew Rate	R_L = 2kΩ	0.3	0.7		*	*		*	*		V/μsec
Settling time	to 1%		30			*			*		μs
	to 0.1%		150			*			*		μs
	to 0.01%		1			*			*		ms
INPUT OFFSET VOLTAGE											
Initial Offset	T_A = 25°C		±200	±500		±100	±250		±200	±500	μV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±5	±15		±2	±5		±5	±10	μV/°C
vs Supply Voltage	$\pm V_{CC}$ = 15V to 20V, to 5V		±25	±100		*	*		*	*	μV/V
vs Time			20			*			*		μV/mo
INPUT BIAS CURRENT											
Initial	T_A = 25°C			-300			-150			±75	fA
at Temperature	at T_A = 85°C		-40	-60		-20	-30		-10	-15	pA
vs Supply Voltage			1			*			*		fA/V
INPUT DIFFERENCE CURRENT											
Initial	T_A = 25°C		±80			±40			±20		fA
at Temperature	at T_A = 85°C		±8			±4			±2		pA
INPUT IMPEDANCE											
Differential			10^{13} || 0.8			*			*		Ω || pF
Common-mode			10^{15} || 1			*			*		Ω || pF
INPUT NOISE											
Voltage Noise Density	f_o = 1Hz		475			*			*		nV/√Hz
	f_o = 10Hz		120			*			*		nV/√Hz
	f_o = 100Hz		55			*			*		nV/√Hz
	f_o = 1kHz		40			*			*		nV/√Hz
	f_o = 10kHz		40			*			*		nV/√Hz
Voltage Noise	f_B = 0.3Hz to 10Hz		6			*			*		μV, p-p
	f_B = 10Hz to 10kHz		4			*			*		μV, rms
Current Noise Density	f_o = 1Hz		0.25			0.2			0.15		fA/√Hz
	f_o = 10Hz		0.25			0.2			0.15		fA/√Hz
	f_o = 100Hz		0.25			0.2			0.15		fA/√Hz
	f_o = 1kHz		0.25			0.2			0.15		fA/√Hz
Current Noise	f_B = 0.3Hz to 10Hz		7			5			4		fA, p-p
	f_B = 10Hz to 10kHz		26			20			15		fA, rms
INPUT VOLTAGE RANGE											
Common-mode Voltage Range	Linear Operation		$\pm(\lvert V_{cc}\rvert$-3)			*			*		V
Common-mode Rejection	f = DC, V_{CM} = ±10V	66	74		80	86		70	86		dB
Max. Safe Input Voltage			$\pm V_{cc}$			*			*		V
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range, derated performance		±5		±20	*		*	*		*	V
Current, quiescent			1	1.5		*	*		*	*	mA
TEMPERATURE RANGE (ambient)											
Specification		-25		+85	*		*	*		*	°C
Operating, derated performance		-55		+125	*		*	*		*	°C
Storage		-65		+150	*		*	*		*	°C

TABLE I. Electrical Specifications

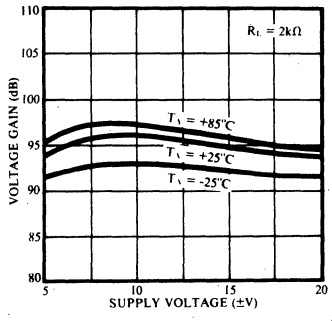
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted)

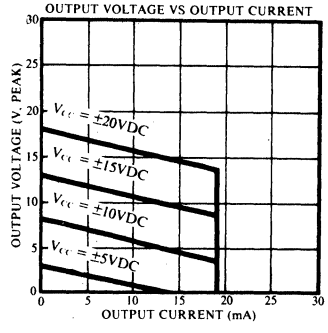
OPEN LOOP TRANSFER CHARACTERISTICS VS FREQUENCY



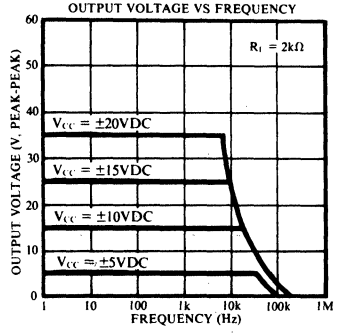
VOLTAGE GAIN VS SUPPLY VOLTAGE



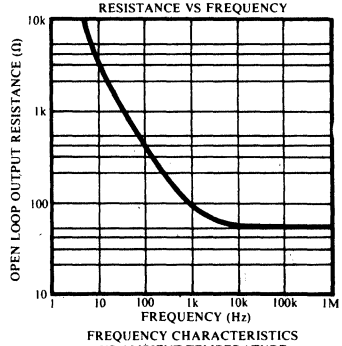
OUTPUT VOLTAGE VS OUTPUT CURRENT



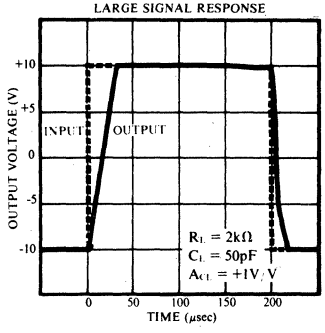
OUTPUT VOLTAGE VS FREQUENCY



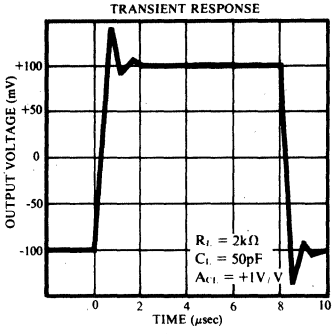
OPEN LOOP OUTPUT RESISTANCE VS FREQUENCY



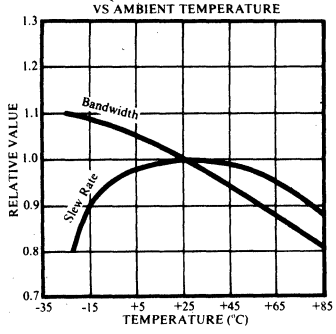
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



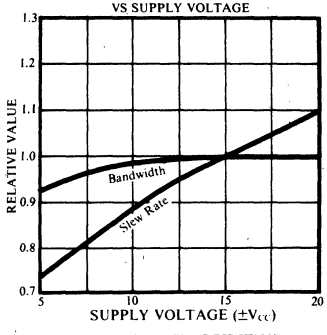
TRANSIENT RESPONSE



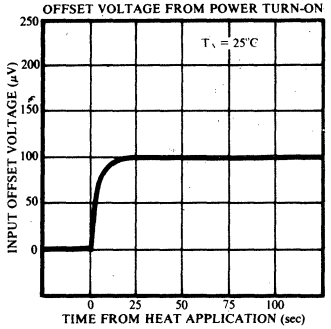
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



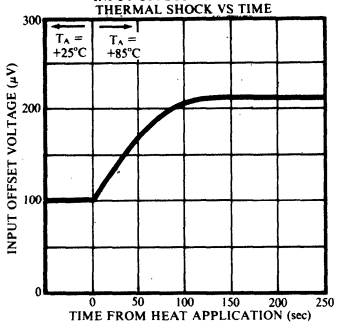
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



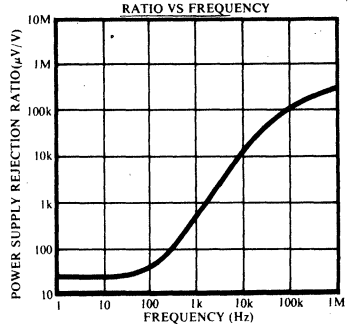
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



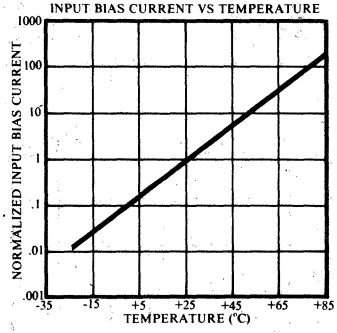
INPUT OFFSET VOLTAGE VS THERMAL SHOCK VS TIME



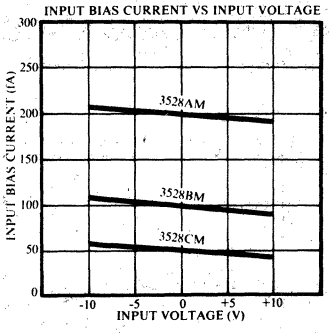
POWER SUPPLY REJECTION RATIO VS FREQUENCY



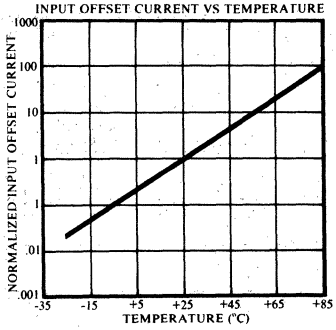
INPUT BIAS CURRENT VS TEMPERATURE



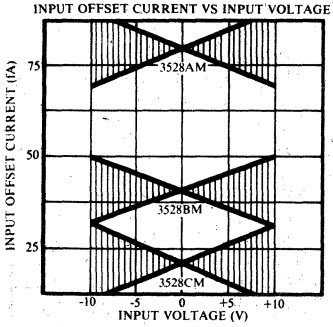
INPUT BIAS CURRENT VS INPUT VOLTAGE



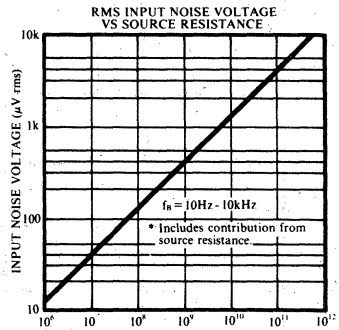
INPUT OFFSET CURRENT VS TEMPERATURE



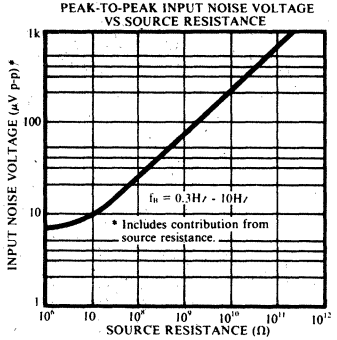
INPUT OFFSET CURRENT VS INPUT VOLTAGE



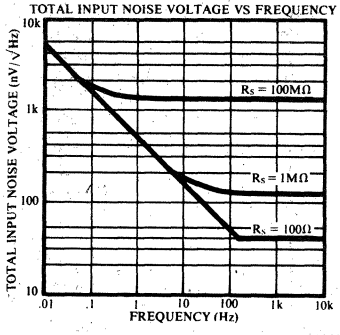
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



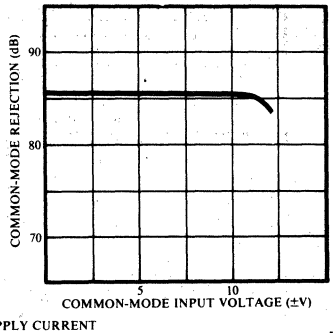
PEAK-TO-PEAK INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



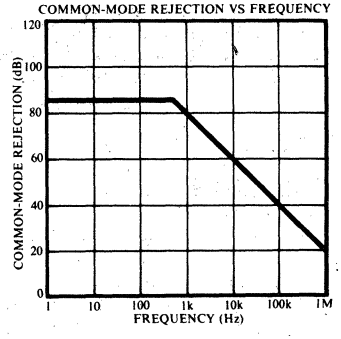
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



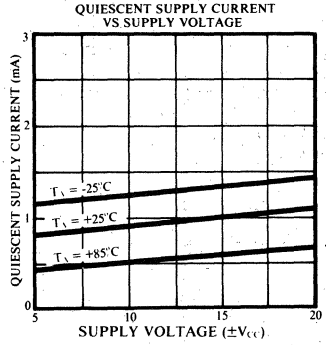
COMMON-MODE REJECTION VS COMMON MODE INPUT VOLTAGE



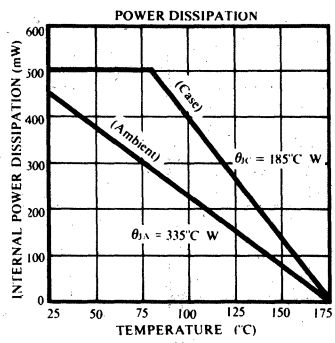
COMMON-MODE REJECTION VS FREQUENCY



QUIESCENT SUPPLY CURRENT VS SUPPLY VOLTAGE



POWER DISSIPATION



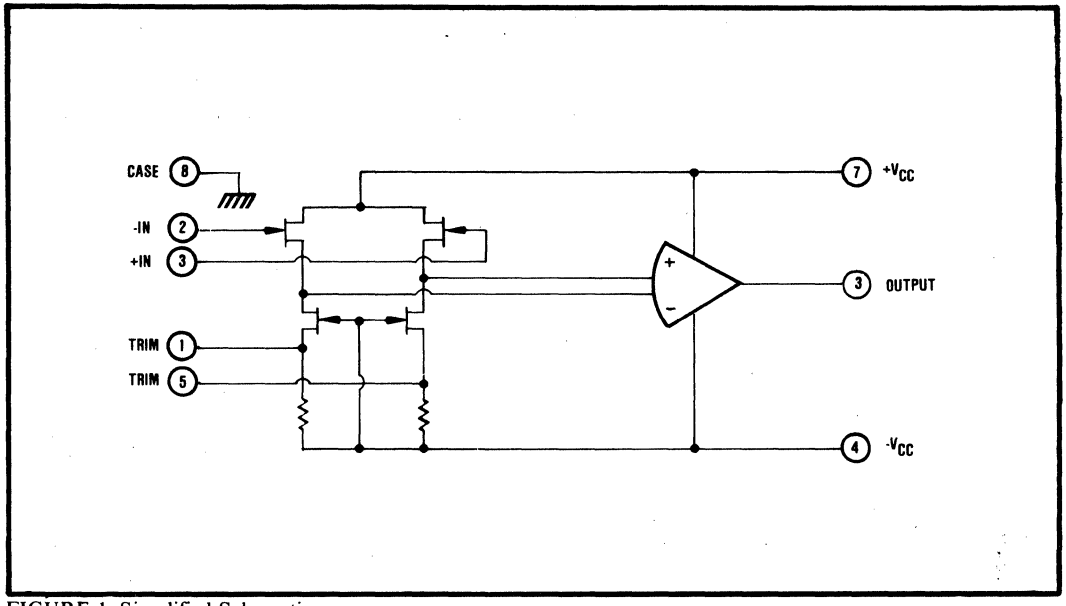


FIGURE 1. Simplified Schematic

ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation (note 1)	500mW
Differential Input Voltage (note 2)	±40VDC
Input Voltage Range (note 2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	300°C
Output Short - Circuit Duration (note 3)	Continuous
Junction Temperature	T_j = +175°C

NOTES:

1. Package must be derated based on a junction to ambient thermal resistance of 335°C/W.
2. For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +115°C case temperature or +75°C. ambient temperature.

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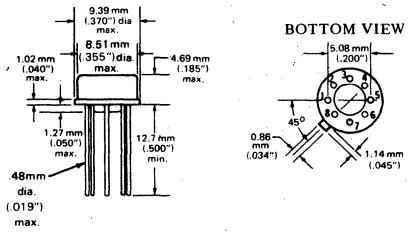

Dimensions in inches are in parentheses. Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883

FIGURE 2. Mechanical Specifications

CONNECTION DIAGRAM

TOP VIEW

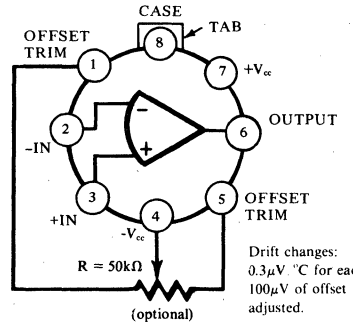

FIGURE 3. Pin Connections

APPLICATION CONSIDERATIONS

The ultra-low bias current and high input impedance of the 3528 are well suited to a number of challenging applications. In order to fully benefit from the outstanding specifications of this unit careful layout, shielding and guarding is required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the 3528.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the 3528 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pick-up.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3528. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the 3528 be wired to a Teflon standoff. If this is not done and instead the 3528 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 4). The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents.

Figures 5, 6, and 7 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in ultra-low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.

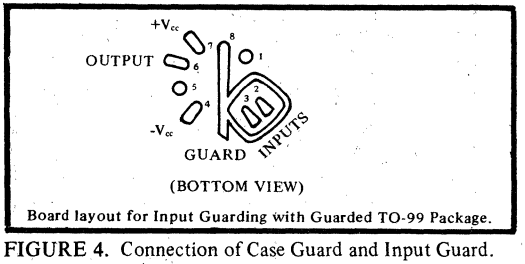

FIGURE 4. Connection of Case Guard and Input Guard.

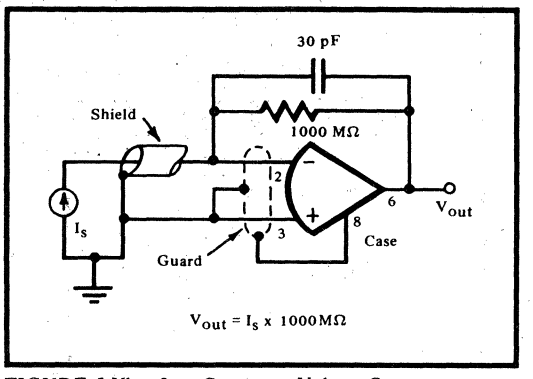

FIGURE 5.Ultra Low Current to Voltage Converter.

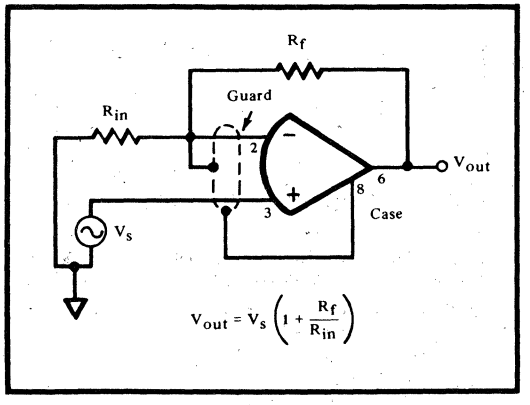

FIGURE 6. Ultra High Input Impedance Noninverting Circuit.

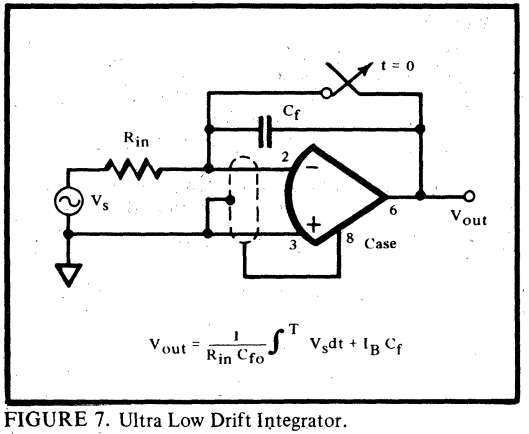

FIGURE 7. Ultra Low Drift Integrator.

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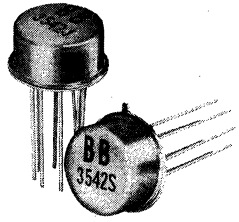


3542 SERIES

FET Input OPERATIONAL AMPLIFIERS

FEATURES

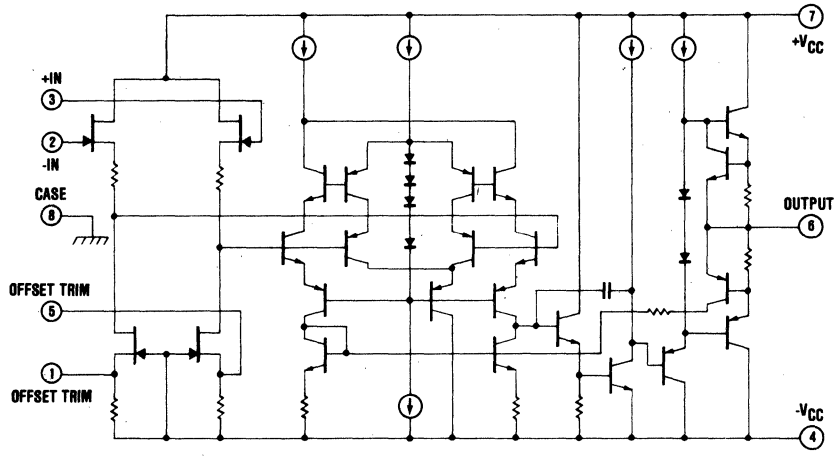
- HIGH INPUT IMPEDANCE, $10^{11}\Omega$
- LOW NOISE, 2μV, p-p
- HIGH CMR, 80dB
- WIDE SUPPLY RANGE, ±5VDC to ±20VDC
- INTERNAL FREQUENCY COMPENSATION
- INDUSTRIAL AND MILITARY VERSIONS

DESCRIPTION

These FET amplifiers offer excellent input characteristics at low cost through the use of monolithic chips and thin-film hybrid technology. Unlike other FET op amps of comparable cost, they have low input noise and moderate voltage drift. Thus they are suitable for a number of applications where previous hybrid or monolithic FET op amps were, at best marginal.

In addition, the 3542 series are extremely stable amplifiers having internal frequency compensation. Other built-in features are output short-circuit protection, input protection to supply voltage, and operation over a wide range of supply voltages.

The pin configuration of the 3542 is conventional (same as 741 type amplifiers) except for pin 8, which is connected to the case. In the usual IC operational amplifier, the case is connected to the negative supply voltage. However, in FET amplifiers it is often desirable to connect the case to a low impedance "guard" potential. This aids in eliminating noise "pickup" in high impedance circuits and preserves the low input currents of the amplifier.



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SPECIFICATIONS

ELECTRICAL

Specifications typical at 25°C and ±15VDC Power Supply unless otherwise noted.

MODEL	3542J	3542S
OPEN LOOP GAIN, DC		
Rated Load, min	88dB	
RATED OUTPUT		
Voltage, min	±10V	
Current, min	±10mA	
Output Impedance	75Ω	
FREQUENCY RESPONSE		
Unity Gain, Open Loop	1MHz	
Full Power Response	8kHz	
Slew Rate	0.5V/μsec	
INPUT OFFSET VOLTAGE		
Initial Offset, 25°C, max	±20mV	
vs. Temp (0°C to 70°C)	±10μV/°C	
vs. Supply Voltage	±50μV/V	
vs. Time	±100μV/mo	
INPUT BIAS CURRENT		
Initial Bias, 25°C	-10pA, typ; -25pA, max	
(doubles every +10°C)		
vs. Supply Voltage	1pA/V	
INPUT DIFFERENCE CURRENT		
Initial Difference, 25°C	±2pA	
INPUT IMPEDANCE		
Differential	$10^{11}\Omega$	
Common-mode	$10^{11}\Omega$	
INPUT NOISE		
Voltage, 0.01Hz to 10Hz, p-p	2μV	
Voltage, 10Hz to 1kHz, rms	3μV	
Current, 0.01Hz to 10Hz, p-p	0.3pA	
Current, 10Hz to 1kHz, rms	0.6pA	
INPUT VOLTAGE RANGE		
Common-mode Voltage	±(|Vs|-5V)	
Common-mode Rejection	80dB	
Max. Safe Input Voltage	±Vs	
POWER SUPPLY		
Rated Voltage	±15VDC	
Voltage Range, derated	±5VDC to ±20VDC	
Current, quiescent	±4mA	
TEMPERATURE RANGE		
Specification	0°C to +70°C	-55°C to +125°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	

MECHANICAL

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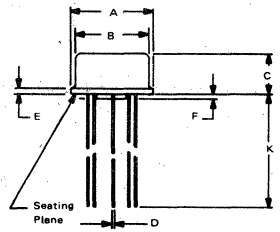
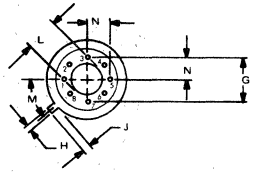
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



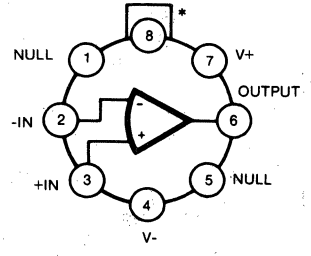


(BOTTOM VIEW)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM

(TOP VIEW)

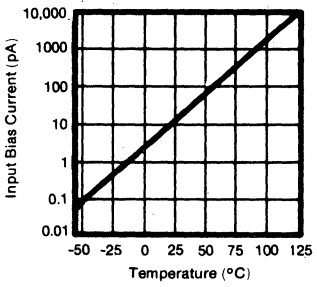


*Pin 8 is connected to case.

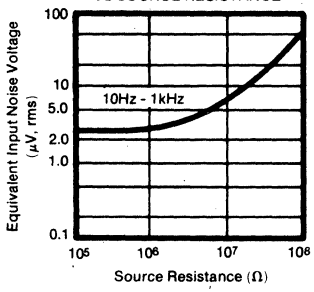
TYPICAL PERFORMANCE CURVES

(At +25°C and ±15VDC unless otherwise specified)

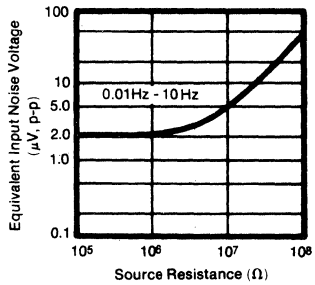
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



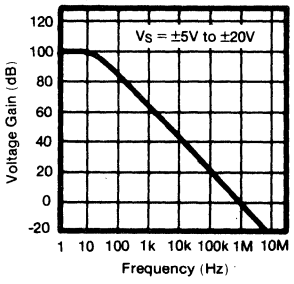
RMS INPUT VOLTAGE VS SOURCE RESISTANCE



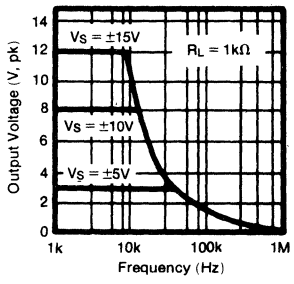
P-P INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



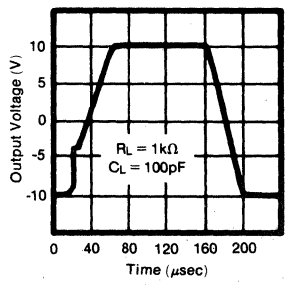
OPEN-LOOP FREQUENCY RESPONSE



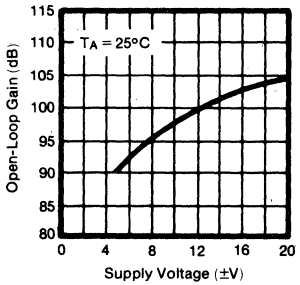
OUTPUT VOLTAGE VS FREQUENCY



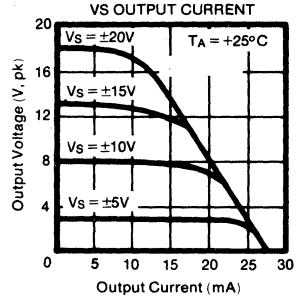
VOLTAGE FOLLOWER STEP RESPONSE



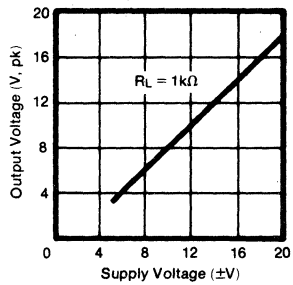
VOLTAGE GAIN VS SUPPLY VOLTAGE



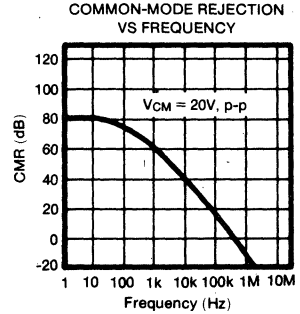
OUTPUT VOLTAGE VS OUTPUT CURRENT



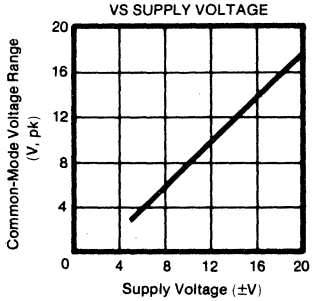
OUTPUT VOLTAGE VS SUPPLY VOLTAGE



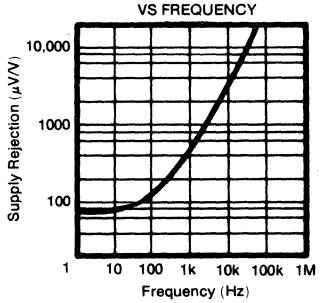
COMMON-MODE REJECTION VS FREQUENCY



COMMON-MODE RANGE VS SUPPLY VOLTAGE



POWER SUPPLY REJECTION VS FREQUENCY



WIRING CONSIDERATIONS

SHIELDING AND GUARDING

The low bias current and high input impedance of the 3542 are well-suited to a number of stringent applications. However, careless signal wiring or printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the 3542.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3542. To avoid leakage problems, it is recommended that the signal input lead of the 3542 be wired to a Teflon standoff. If the 3542 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard for both inverting and noninverting circuits.

OFFSET VOLTAGE ADJUSTMENT

Although the 3542 has a moderately low initial offset voltage (5mV, typ) compatible with its moderate voltage drift, some applications may reuire external nulling of this small offset. Figure 2 shows the recommended circuit for adjustment of the offset voltage.

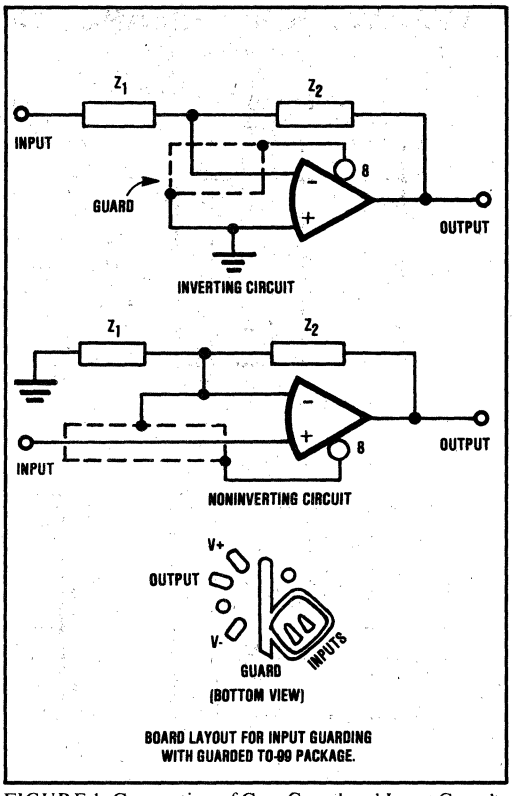


FIGURE 1. Connection of Case Guard and Input Guard.

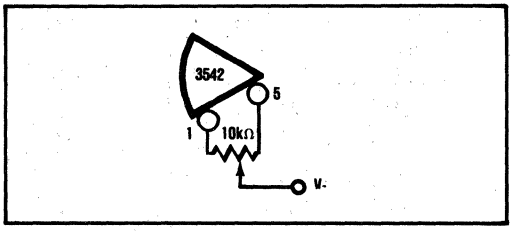


FIGURE 2. External Nulling of Offset Voltage.

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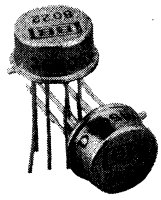
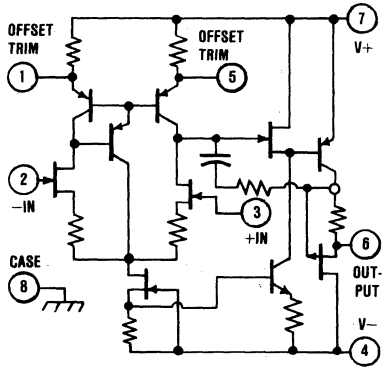


3550 SERIES

Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- SETTLING TIME (0.01%), 600nsec, max
- TRUE DIFFERENTIAL INPUT
- SLEW RATE, 100V/μsec, min
- FULL POWER, 1.5MHz, min
- INPUT IMPEDANCE, $10^{11}\Omega$
- INTERNALLY COMPENSATED
- STABLE OPERATION, 1000pF, typ



DESCRIPTION

The 3550 is specifically designed for fast transient applications such as D/A and A/D conversion, sample/hold, multiplexer buffering and pulse amplification where the primary amplifier requirements are fast settling, good accuracy, and high input impedance.

Because the 3550 is internally compensated, elaborate compensation schemes requiring external components are not necessary. The smooth 6dB/octave rolloff of open-loop gain and the low output impedance provides the excellent step response and smooth settling without sacrificing frequency stability (no oscillations even with 1000pF of capacitive load)! A 10 to 1 improvement in settling time with large capacitive loads can be obtained with the addition of a single capacitor.

Unlike many wideband and fast settling amplifiers the 3550 has a true differential input. This means it can provide its excellent transient performance in the inverting, non-inverting, current to voltage, and difference configurations.

The 3550J and S have identical specifications except for temperature range: The 3550J is specified for 0°C to +70°C and the 3550S is specified for -55°C to +125°C. The 3550K has improved dynamic specifications and is specified over the 0°C to +70°C temperature range.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

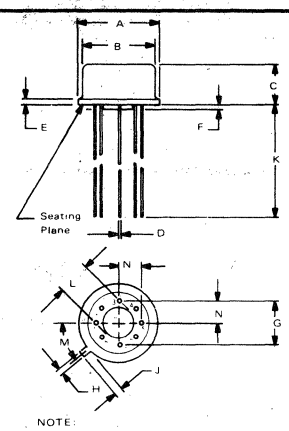
ELECTRICAL

Specifications typical at +25°C and ±15VDC Power Supply unless otherwise noted.

MODELS	3550J	3550K	3550S
OPEN LOOP GAIN, DC			
No load		100dB	
1kΩ, load min		88dB	
RATED OUTPUT			
Voltage, min		±10V	
Current, min		±10mA	
Open-loop Output Resistance		100Ω at 1MHz	
DYNAMIC RESPONSE			
Bandwidth (0dB, small signal)	10MHz	20MHz	10MHz
Full Power Response, min	1.0MHz	1.5MHz	1.0MHz
Slew Rate, min	65V/μsec	100V/μsec	65V/μsec
Settling Time (0.01%), max	1μsec	0.6μsec	1μsec
INPUT OFFSET VOLTAGE			
Initial Offset, +25°C, max		±1mV	
vs Temperature		±50μV/°C	
vs Supply Voltage		±500μV/V	
vs Time		±100μV/mo	
INPUT BIAS CURRENT			
Initial Bias, +25°C, max		−100pA (after full warm-up)	
vs Temperature		doubles every 10°C	
vs Supply Voltage		±1pA/V	
INPUT DIFFERENCE CURRENT			
Initial Difference, +25°C		±40pA	
INPUT IMPEDANCE			
Differential		$10^{11}\Omega$ || 3pF	
Common Mode		$10^{11}\Omega$ || 3pF	
INPUT NOISE			
Voltage, 0.01Hz - 10Hz, p-p		20μV	
10Hz - 10kHz, rms		4μV	
Current, 0.01Hz - 10Hz, p-p		0.2pA	
10Hz - 10kHz, rms		1.5pA	
INPUT VOLTAGE RANGE			
Common-Mode Voltage		±(|V_{cc}| −5)V	
Common-Mode Rejection		70dB at +5V, −10V	
Safe Input Voltage, max		±Supply	
POWER SUPPLY			
Rated Voltage		±15VDC	
Voltage Range, derated		±5VDC to ±20VDC	
Current, quiescent[1]		11mA	
TEMPERATURE RANGE			
Specification	0°C to +70°C		−55°C to +125°C
Operating	−55°C to +125°C		−55°C to +125°C
Storage	−65°C to +150°C		

NOTES:
1. The use of a finned heat sink is recommended.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.

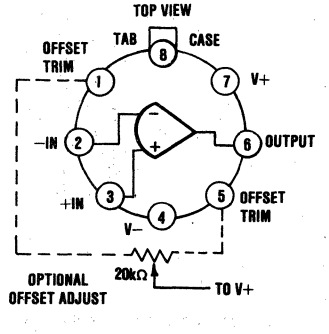
BOTTOM VIEW

Dimensions in inches are in parentheses.

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

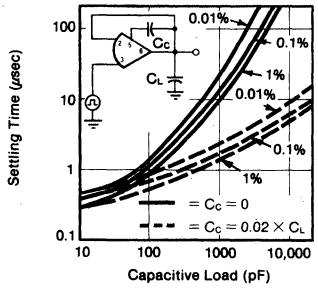
CONNECTION DIAGRAM



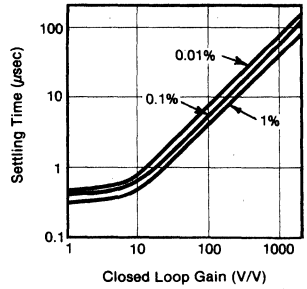
TYPICAL PERFORMANCE CURVES

$T_A = +25°C \pm V_{CC} = 15VDC$ unless otherwise indicated.

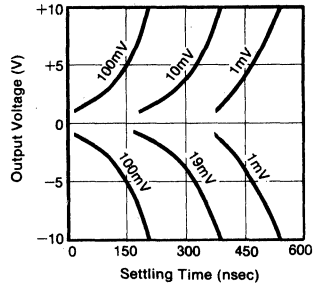
SETTLING TIME VS CAPACITIVE LOAD



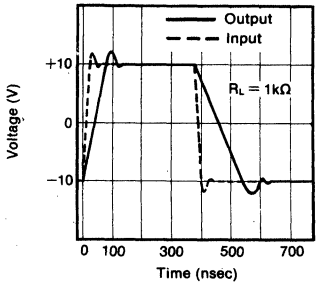
SETTLING TIME VS CLOSED LOOP GAIN



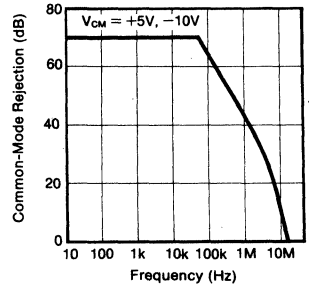
SETTLING TIME VS OUTPUT VOLTAGE CHANGE



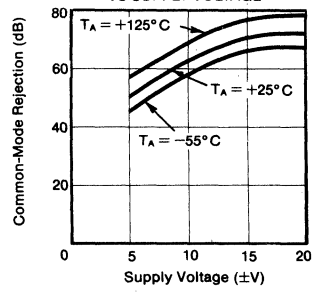
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



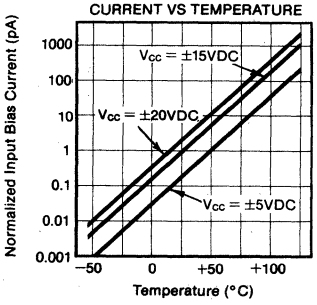
COMMON MODE REJECTION VS FREQUENCY



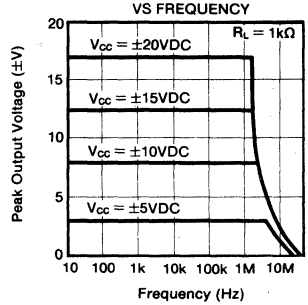
COMMON MODE REJECTION VS SUPPLY VOLTAGE



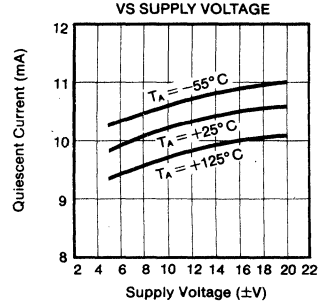
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



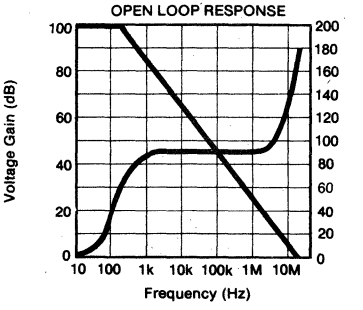
OUTPUT VOLTAGE VS FREQUENCY



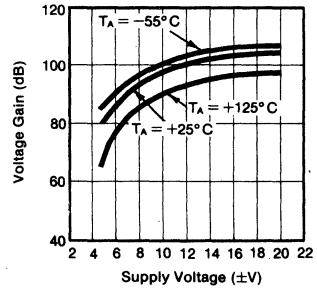
QUIESCENT CURRENT VS SUPPLY VOLTAGE



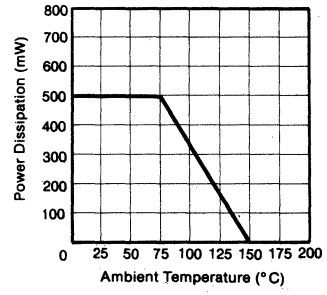
OPEN LOOP RESPONSE



OPEN LOOP GAIN VS SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

SETTLING TIME

Settling time of an amplifier is defined (see Figure 1) as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition. A recommended test circuit for settling time is shown in Figure 2. The output error signal appears, attenuated by a factor of two, at point A and may be observed at this point with the aid of an oscilloscope. The diodes act as limiters to prevent overloading the oscilloscope during the fast leading edge of the input signal. All resistors should be 2kΩ or less to eliminate degradation of performance due to stray capacitance. A typical measurement desired is the settling time to 0.01% for a 10-volt step input. This is the time required for the signal at point A to decrease to 0.5mV or less and remain below this level.

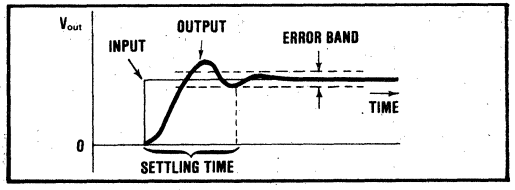


FIGURE 1. Concept of Settling Time.

Settling time for noninverting circuits can also be measured but requires the use of ultra-fast differential amplifier test fixtures. For the 3550 settling time is equal for inverting or noninverting circuits of equal gain.

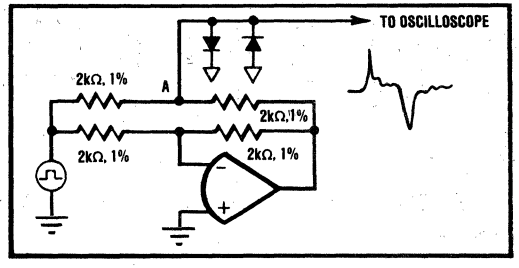


FIGURE 2. Settling Time Test Circuit.

Because settling time is affected by bandwidth which in turn is dependent upon closed-loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling Time versus Gain curves illustrate this effect for the 3550 at several levels of settling accuracy.

The 3550 is remarkably tolerant of load capacitance because of its stable, 6dB/octave gain rolloff and low output impedance. Settling Time versus Load Capacitance curves show this characteristic for the unity-gain configuration. For larger values of load capacitance the compensation technique of Figure 3 may be used to optimize the response. The slight negative feedback provided by C_C tends to reduce any ringing at the top of the output voltage waveform without significantly affecting the slew rate. See the Settling Time versus Load Capacitance curves for typcial improvements in settling time.

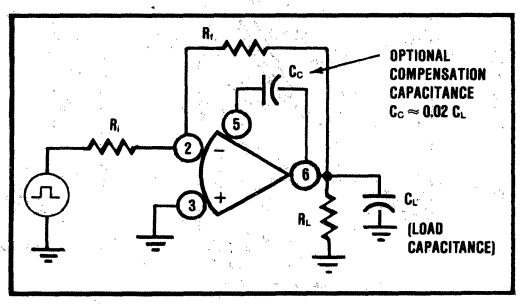


FIGURE 3. Compensation for Load Capacitance.

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3550, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the ouput to noninverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedance. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 0.001μF ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3550 is specified for best operation on power supply voltage of ±15VDC, it will operate with minor performance changes over a power supply voltage range of ±5VDC to ±20VDC. Many of the curves show performance of the 3550 when operated from supplies other than ±15VDC.

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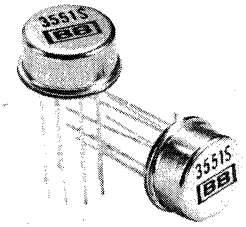
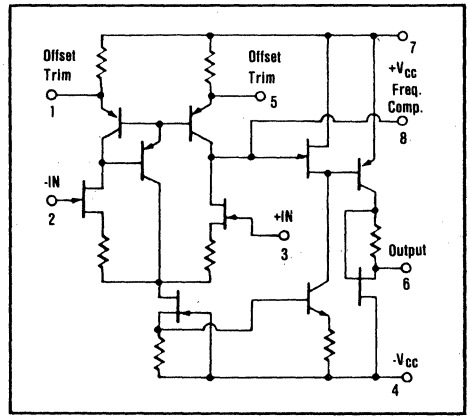


3551 SERIES

Wideband and Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- **REDUCES WIDEBAND ERRORS**
  - **50MHz Gain-bandwidth product (ACL ≥10)**
  - **250V/μs slew rate (Cf = 0)**
- **VERSATILE**
  - **Single compensation capacitor allows optimum response**
  - **True differential input**
- **PRESERVES DC ACCURACY**
  - **Bias current, 100pA, max**
  - **Laser-trimmed offset voltage**



DESCRIPTION

The 3551 is designed to offer the user versatility in wideband steady state and fast transient applications. The use of a single external compensation capacitor allows the user to optimize frequency response for maximum bandwidth for a variety of closed loop gains and capacitive loads. The amplifier is stable at closed loop gains of greater than 10V/V, with no external compensation and may be stabilized at all gains with the single 10pF compensation capacitor.

In addition to the excellent dynamic response characteristics, the 3551 also has good DC properties. The use of a monolithic FET input stage gives the 3551 very low input bias and offset currents. This is in contrast to the high input currents usually associated with fast amplifiers having bipolar input stages. Also, the input offset voltage and offset voltage drift are low as a result of Burr-Brown's laser-trimming techniques.

Unlike many wideband and fast settling amplifiers, the 3551 has a true differential input. This means it can provide its excellent wideband response in the inverting, noninverting, current-to-voltage and difference configurations.

The 3551 is an excellent choice for applications such as fast D/A and A/D converters, high speed comparators and fast sampling circuits, to name just a few.

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SPECIFICATIONS

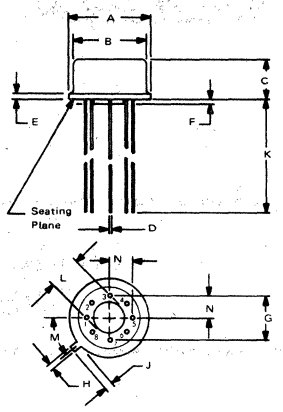
ELECTRICAL

Specifications typical at 25°C and ±15VDC Power Supply unless otherwise noted.

MODELS	3551J	3551S
OPEN LOOP GAIN, DC		
No Load	100dB	
1kΩ, Load min	88dB	
RATED OUTPUT		
Voltage, min	±10V	
Current, min	±10mA	
Open Loop Output Resistance	100Ω at 1MHz	
DYNAMIC RESPONSE		
Gain-Bandwidth Product		
Gain = 1000	50MHz	
Gain = 10	50MHz	
Slew Rate (C_f = 0)	250V/μsec	
INPUT OFFSET VOLTAGE		
Initial Offset, 25°C, max	±1mV	
vs. Temp(1)	±50μV/°C	
vs. Supply Voltage	±500μV/V	
vs. Time	±100μV/mo	
INPUT BIAS CURRENT		
Initial Bias, 25°C, max	-400pA (after full warm-up)	
vs. Temperature	doubles every 10°C	
vs. Supply Voltage	±1pA/V	
INPUT DIFFERENCE CURRENT		
Initial Difference, 25°C	±40pA	
INPUT IMPEDANCE		
Differential	$10^{11}\Omega$ || 3pF	
Common-mode	$10^{11}\Omega$ || 3pF	
INPUT NOISE		
Voltage, 0.01Hz to 10Hz, p-p	20μV	
Voltage, 10Hz to 10kHz, rms	4μV	
Current, 0.01Hz to 10Hz, p-p	0.2pA	
Current, 10Hz to 10kHz, rms	1.5pA	
INPUT VOLTAGE RANGE		
Common-mode Voltage	±(|V_{CC}|-5)V	
Common-mode Rejection	70dB at +5V, -10V	
Max. Safe Input Voltage	±Supply	
POWER SUPPLY		
Rated Voltage	±15VDC	
Voltage Range, derated	±5VDC to ±20VDC	
Current, quiescent(1)	11mA	
TEMPERATURE RANGE		
Specification	0°C to +70°C	-55°C to +125°C
Operating	-55°C to +125°C	-55°C to +125°C
Storage	-65°C to +150°C	

NOTE:
1. The use of a finned heat sink is recommended.

MECHANICAL TO-99



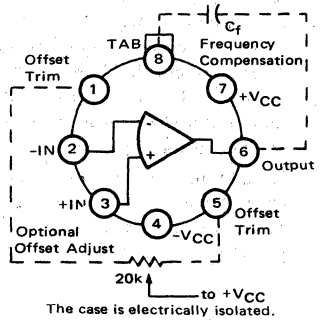
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

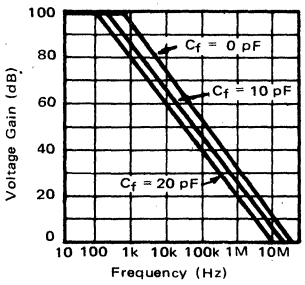


The case is electrically isolated.

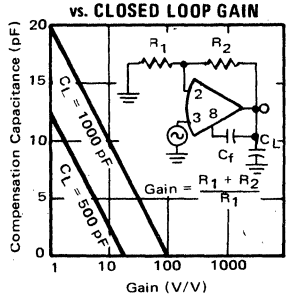
TYPICAL PERFORMANCE CURVES

$T_A = 25^oC$ $V_S = \pm 15$ VDC unless otherwise indicated.

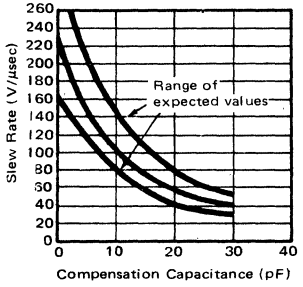
OPEN LOOP RESPONSE



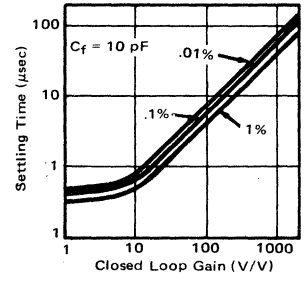
RECOMMENDED VALUES OF FREQUENCY COMPENSATION CAPACITANCE vs. CLOSED LOOP GAIN



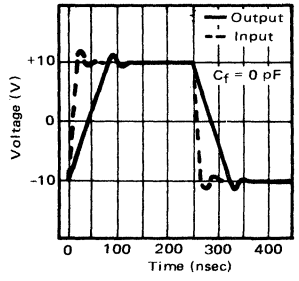
SLEW RATE vs. COMPENSATION CAPACITANCE



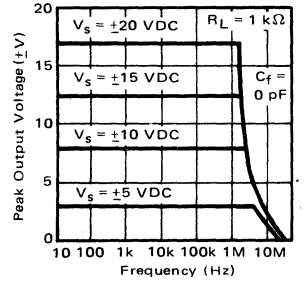
SETTLING TIME vs. CLOSED LOOP GAIN



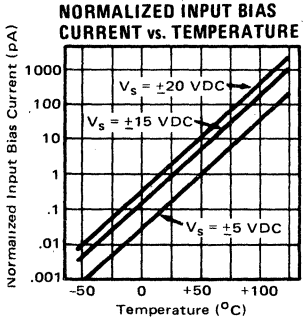
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



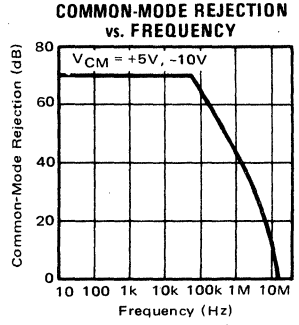
OUTPUT VOLTAGE vs. FREQUENCY



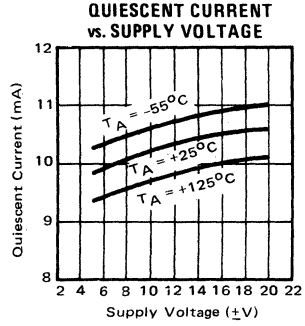
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



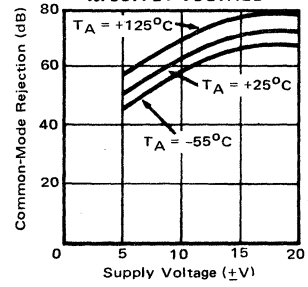
COMMON-MODE REJECTION vs. FREQUENCY



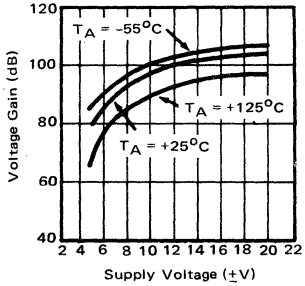
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



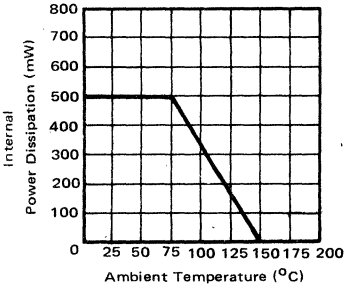
COMMON-MODE REJECTION vs. SUPPLY VOLTAGE



OPEN LOOP GAIN vs. SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3551, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the output to non-inverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedances. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

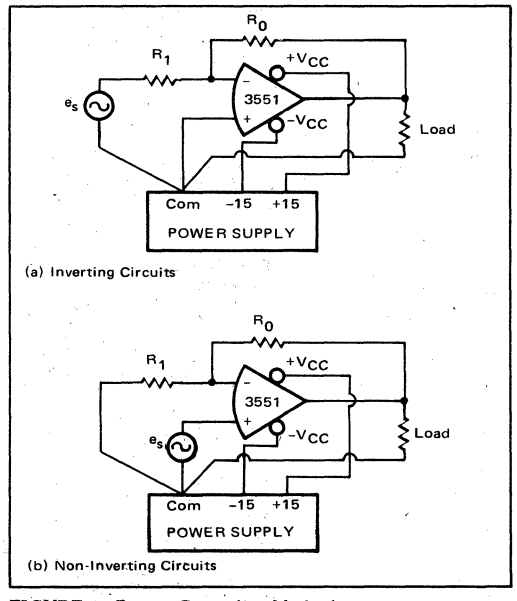


FIGURE 1. Proper Grounding Methods.

Provision for phase compensation should always be made on the PC board even if initial calculations and breadboarding may indicate that none is needed.

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10 μf tantalum capacitor in parallel with a 0.001 μf ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3551 is specified for best operation on power supply voltage of ±15 VDC, it will operate with minor performance changes over a power supply voltage range of ±5 VDC to ±20 VDC. Many of the performance curves show performance of the 3551 when operated from supplies other than ±15 VDC.

INPUT/OUTPUT PROTECTION

All of the amplifiers listed in the specification table are designed to withstand input voltages as high as the supply voltage, without damage to the amplifier. Thus, inputs may be subjected to either supply voltage, in any combination, without damage.

Output stages are internally current limited and will withstand short-circuit-to-ground conditions. However, application of nonzero potential to the output pin may cause permanent damage and should be prevented by the proper precautions.

SETTLING TIME

Settling time of an amplifier is defined as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition.

Because settling time is affected by bandwidth which in turn is dependent upon closed loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling time vs. gain curves illustrate this effect for the 3551 at several levels of settling accuracy.

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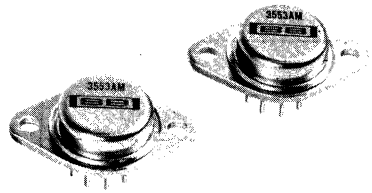

3553

Wideband - Fast-Slewing BUFFER AMPLIFIER

FEATURES

- GAIN = .99V/V
- OUTPUT CURRENT, ±200mA
- BANDWIDTH, 300MHz
- SLEW RATE, 2000V/μsec
- ELECTRICALLY ISOLATED CASE
- EXTENDS OP AMP DRIVING CAPABILITY WHILE PRESERVING BANDWIDTH & SETTLING TIME

DESCRIPTION

The 3553 is a unity-gain amplifier designed to be used either as a signal buffer, or as the power output stage for an operational amplifier. Because of its wideband response (300MHz, -3dB bandwidth) and fast slewing capability (2000V/μsec) the 3553 is capable of following very fast signals. When used inside the feedback loop of an operational amplifier, these high speed characteristics are essential in order to preserve the performance and stability of the feedback amplifier circuit.

With its ±200mA of output current capability, the 3553 is capable of driving a signal of ±10V into a 50Ω load. This power capability, coupled with its extremely high speed and wide bandwidth, makes the 3553 ideally suited for line driving applications where fast pulses or wideband signals are involved.

In addition to its fast/wideband characteristics and high output current, the 3553 has low input offset voltage and drift. This adds to its versatility, particularly in stand-alone buffer amplifier applications.

The 3553 is packaged in a reliable hermetically sealed TO-3 package for environmental ruggedness. The metal case is completely electrically isolated. This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated.

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SPECIFICATIONS

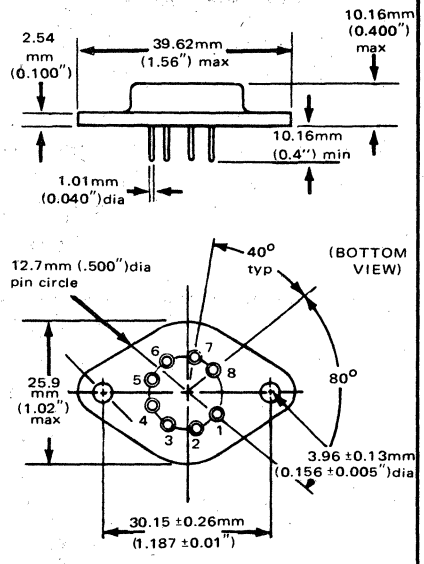
Specifications are typical at +25°C Case Temperature and ± 15 VDC power supply unless otherwise noted.

ELECTRICAL

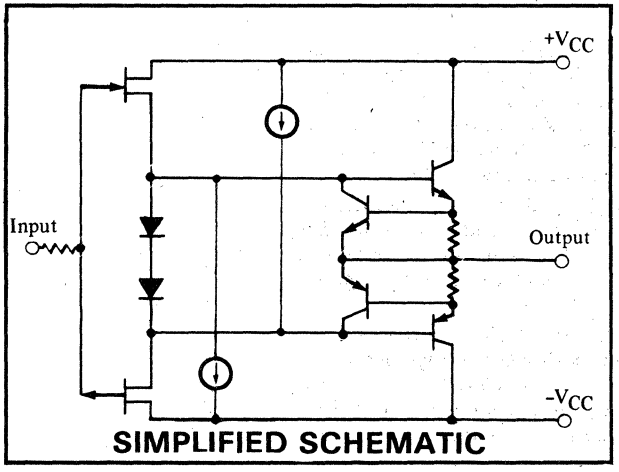
MODEL	3553AM
GAIN, DC	
No Load	0.98 V/V
50 Ω Load, min	0.92 V/V
RATED OUTPUT	
Voltage, min	±10 V
Current, min	±200 mA
Output Resistance	1 Ω
DYNAMIC RESPONSE	
Slew Rate, min	2000 V/μsec
Full Power Bandwidth, min	32 MHz
Small Signal -3dB Bandwidth	300 MHz
Settling Time to 1%	7.2 nsec
to .01%	14.5 nsec
INPUT PARAMETERS	
Input Voltage, linear range	±10 V
Input Voltage, absolute, max	±Supply Voltage
Input Impedance	10^{11} Ω
Input Bias Current @ +25°C (doubles/+10°C)	-200 pA
OUTPUT OFFSET VOLTAGE	
Initial Offset @ +25°C, max	±50 mV
vs. Temperature (average) -25°C to +85°C	±300 μV/°C
POWER SUPPLY	
Rated Voltage	±15 VDC
Voltage Range, derated	±5 VDC to ±20 VDC
Current, Quiescent, max	±80 mA
typ	±50 mA
TEMPERATURE RANGE (Case)	
Specification	-25°C to +85°C
Operation (derate above +120°C Case)	-55°C to +125°C
Storage	-65°C to +150°C
θ_{JC} Thermal Resistance, junction to case	6°C/W
θ_{JA} Thermal Resistance, junction to ambient	33°C/W

MECHANICAL

M PACKAGE (TO-3)

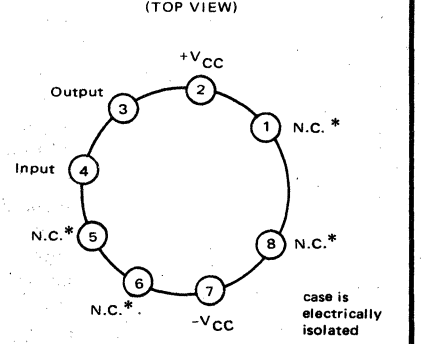


Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]



SIMPLIFIED SCHEMATIC

CONNECTION DIAGRAM



*No internal connection

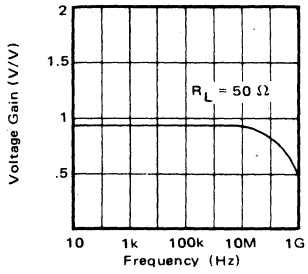
CONNECTOR: 0803MC

HEATSINKS: 0803HS 12°C/W
0804HS 4.2°C/W
0805HS 3°C/W

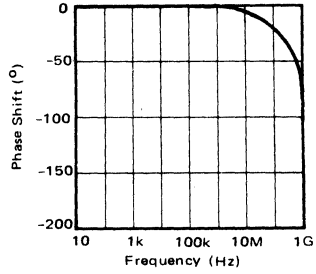
TYPICAL PERFORMANCE CURVES

Typical at 25°C and rated supply voltage unless otherwise noted.

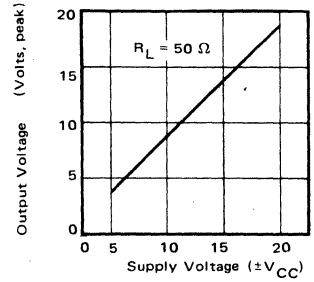
SMALL SIGNAL FREQUENCY RESPONSE



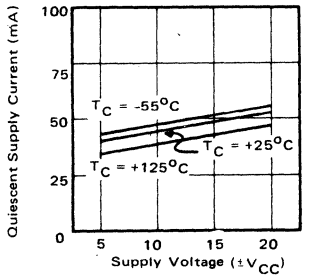
PHASE SHIFT vs FREQUENCY



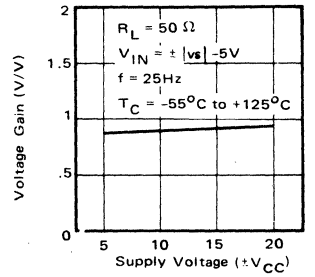
OUTPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



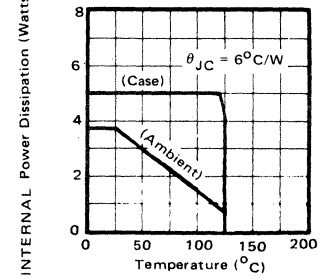
QUIESCENT POWER SUPPLY CURRENT vs SUPPLY VOLTAGE



GAIN vs SUPPLY VOLTAGE



POWER DISSIPATION



APPLICATION INFORMATION

BOOSTER AMPLIFIER

One of the primary applications for the 3553 is that of a current booster for an operational amplifier. The circuit of Figure 1 is typical of such applications. Note that the 3553 is used inside the feedback loop and becomes, effectively, the output stage of the composite amplifier. Because the 3553 has unity voltage gain, wideband response, fast slewing rate, and very little phase delay, the dynamic response of the operational amplifier is virtually unaffected by the addition of the booster.

The already low offset voltage of the 3553 is effectively reduced by a factor equal to the open loop gain of the operational amplifier and becomes a negligible factor in total offset error of the circuit.

Input impedance of the 3553 is extremely high, thus requiring almost no drive current from the operational amplifier. On the other hand, the presence of the 3553 in the circuit increases the output current capability to ±200 mA, drastically lowers the output impedance of the loop, and permits the driving of low impedance loads such as a terminated 50Ω coaxial line.

Capacitive loads, often a source of instability and oscillations in operational amplifier circuits, are buffered by the presence of the 3553. In driving heavily capacitive loads the slew rate of the 3553 will be seen to decrease. This is due simply to the large currents required by fast voltage slewing in a capacitive load,

$$I_c = C_{load} \frac{dV}{dt}.$$

The internal current limit of the 3553 (approximately 600 mA) places a limit on the slewing rate under such conditions.

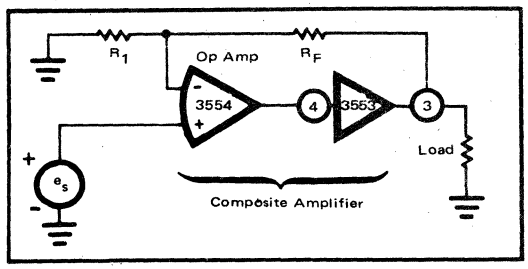


FIGURE 1. Model 3553 as a power booster.

BUFFER AMPLIFIER

The 3553 may also be used, as shown in Figure 2, as a unity gain buffer amplifier. No operational amplifier is required in this mode of operation. Since the 3553 is then operated without feedback, it's offset voltage and drift are translated to the output. While the gain is not precisely unity in this mode, the accuracy is adequate for many applications.

INPUT/OUTPUT PROTECTION

The output stage of the 3553 is current limited at approximately 600mA. This will provide a measure of output short circuit protection for the amplifier for a period of time as determined by the heatsinking used, the amplifier's thermal resistance, the ambient temperature, etc. The amplifier's output stage transistors should not be allowed to exceed 150°C (175°C absolute max).

The input stage is designed to allow the application of either supply voltage without damage to the amplifier.

POWER DISSIPATION

The power dissipation capability of the 3553 varies with ambient temperature and with the type of heat sink used. A heat sink may be used to increase the dissipation capability or to achieve a given dissipation capability at higher temperature. The power derating curve is given in the Typical Performance Curves.

WIRING RECOMMENDATIONS

No special wiring techniques are necessary with the 3553. However, it is recommended, as a good engineering practice, that the power supply lines be bypassed to common at a point near the amplifier. (A 1.0μF electrolytic in parallel with a 1000pF ceramic is recommended.) If the 3553 is used with a wideband operational amplifier, all leads must be kept as short as possible to minimize stray capacitance and unwanted feedback paths.

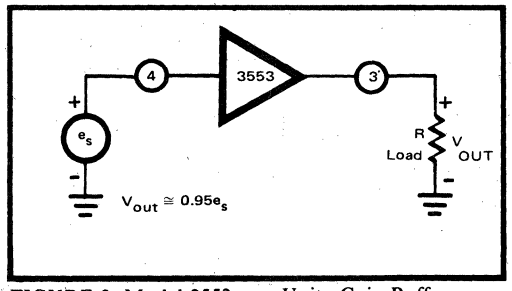


FIGURE 2. Model 3553 as a Unity Gain Buffer.

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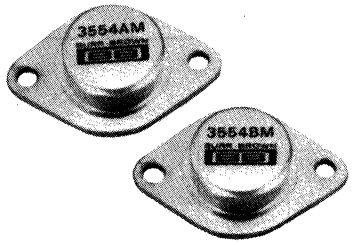


3554

Wideband - Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- SLEW RATE, 1000V/μsec
- FAST SETTLING, 150nsec, max (to ±.05%)
- GAIN-BANDWIDTH PRODUCT, 1.7GHz
- FULL DIFFERENTIAL INPUT

APPLICATIONS

- PULSE AMPLIFIERS
- TEST EQUIPMENT
- WAVEFORM GENERATORS
- FAST D/A CONVERTERS

DESCRIPTION

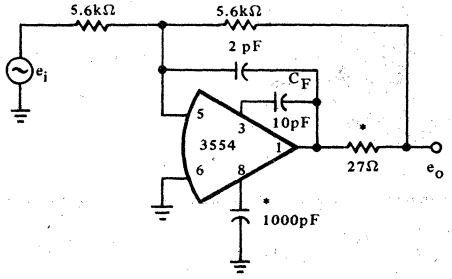
The 3554 is a full differential input, wideband operational amplifier. It is designed specifically for the amplification or conditioning of wideband data signals and fast pulses. It features an unbeatable combination of gain-bandwidth product, settling time and slew rate. It uses hybrid construction. On the beryllia substrate are matched input FETs, thin-film resistors and high speed silicon dice. Active laser trimming and complete testing provide superior performance at a very moderate price.

The 3554 has a slew rate of 1000V/μsec and will output ±10V and ±100mA. When used as a fast settling amplifier, the 3554 will settle to ±0.05% of the final value within 150nsec. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate or settling time in the particular application.

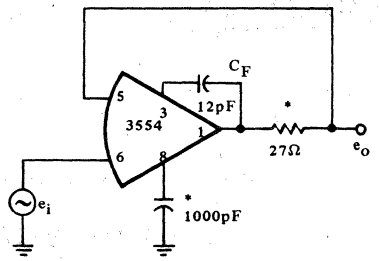
The 3554 is reliable and rugged and addresses almost any application when speed and bandwidth are serious considerations. It is particularly a good choice for use in fast settling circuits, fast D/A converters, multiplexer buffers, comparators, waveform generators, integrators, and fast current amplifiers. It is available in several grades to allow selection of just the performance required.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

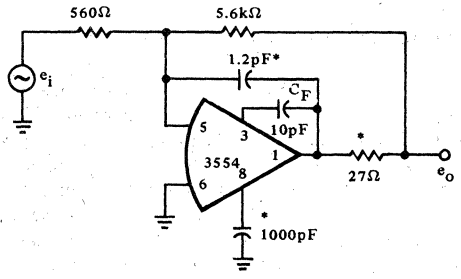
TYPICAL CIRCUITS



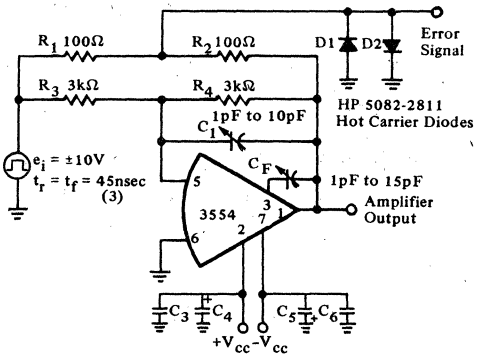
X1 Inverters



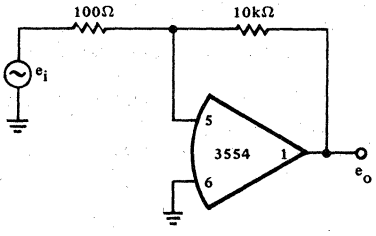
X1 Non-Inverter



X10 Inverter

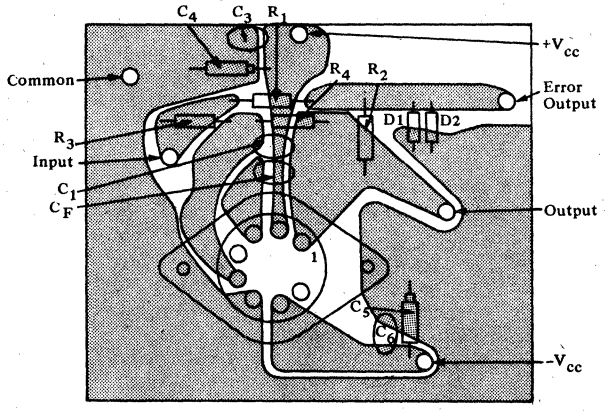


Settling Time Test Circuit Schematic



X100 Inverter

View from Component Side.
Shaded area is the pattern side conductor.



Settling Time Test Circuit Layout

NOTES:

1. These circuits are optimized for driving large capacitive loads (to 470pF).
2. The 3554 is stable at gains of greater than 55 ($C_L \leq 100$pF) without any frequency compensation.
3. 45nsec is optimum. Very fast rise times (10-20nsec) may saturate the input stage causing less than optimum settling time performance.

*Indicates component that may be eliminated when large capacitive loads are not being driven by the device.

ELECTRICAL SPECIFICATIONS

At T_{CASE} = 25°C and ±15VDC, unless otherwise noted.

PARAMETERS	CONDITIONS	3554AM			3554BM			3554SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN LOOP GAIN,DC					*	*	*	*	*	*	
No Load		100	106								dB
Rated Load	R_L = 100Ω	90	96								dB
RATED OUTPUT					*	*	*	*	*	*	
Voltage	I_O = ±100mA	±10	±11								V
Current	V_O = ±10V	±100	±125								mA
Output Resistance, open loop	f = 10MHz		20								Ω
DYNAMIC RESPONSE					*	*	*	*	*	*	
Bandwidth (0dB, small signal)	C_F = 0	70†	90								MHz
Gain-bandwidth Product	C_F = 0, G = 10 V/V	150	225								MHz
	C_F = 0, G = 100 V/V	425	725								MHz
	C_F = 0, G = 1000 V/V	1000	1700								MHz
Full Power Bandwidth	C_F = 0, V_o = 20Vp-p, R_L = 100Ω	16	19								MHz
Slew Rate	C_F = 0, V_o = 20Vp-p, R_L = 100Ω	1000	1200								V/μsec
Settling Time to ±1%	A = -1		60								nsec
to ±.1%	A = -1		120								nsec
to ±.05%	A = -1		140	150							nsec
to ±.01%	A = -1		200	250							nsec
INPUT OFFSET VOLTAGE											
Initial offset, T_A = 25°C			±0.5	±2		±0.2	±1		±0.2	±1	mV
vs. Temp (T_A = -25°C to +85°C)			±20	±50		±8	±15				μV/°C
vs. Temp (T_A = -55°C to +125°C)									±12	±25	μV/°C
vs. Supply Voltage			±80	±300		*	*		*	*	μV/V
INPUT BIAS CURRENT					*	*	*	*	*	*	
Initial bias, 25°C		0	-10	-50							pA
vs. Temp			**								
vs. Supply Voltage			±1								pA/V
INPUT DIFFERENCE CURRENT					*	*	*	*	*	*	
Initial difference, 25°C			±2	±10							pA
INPUT IMPEDANCE						*			*		
Differential			10^{11} ‖ 2								Ω ‖ pF
Common-mode			10^{11} ‖ 2								Ω ‖ pF
INPUT NOISE					*	*	*	*	*	*	
Voltage, f_o = 1Hz	R_S = 100Ω		125	450†							$nV/\sqrt{Hz}$
f_o = 10 Hz	R_S = 100Ω		50	160†							$nV/\sqrt{Hz}$
f_o = 100 Hz	R_S = 100Ω		25	90†							$nV/\sqrt{Hz}$
f_o = 1 kHz	R_S = 100Ω		15	50†							$nV/\sqrt{Hz}$
f_o = 10 kHz	R_S = 100Ω		10	35†							$nV/\sqrt{Hz}$
f_o = 100 kHz	R_S = 100Ω		8	25†							$nV/\sqrt{Hz}$
f_o = 1 MHz	R_S = 100Ω		7	25†							$nV/\sqrt{Hz}$
f_B = .3 Hz to 10 Hz	R_S = 100Ω		2	7†							μV, p-p
f_B = 10 Hz to 1 MHz	R_S = 100Ω		8	25							μV, rms
Current, f_B = .3 Hz to 10 Hz	R_S = 100Ω		45								fA, p-p
f_B = 10 Hz to 1 MHz	R_S = 100Ω		2								pA, rms
INPUT VOLTAGE RANGE					*	*	*	*	*	*	
Common-mode Voltage Range	Linear Operation		±(V_{CC}+4)								V
Common-mode Rejection	f = DC, V_{CM} = +7V, -10V	44	78								dB
Max. Safe Input Voltage			±Supply								V
POWER SUPPLY					*	*	*	*	*	*	
Rated Voltage			±15								VDC
Voltage Range, derated performance		±5		±18							VDC
Current, quiescent		±17	±35	±45							mA
TEMPERATURE RANGE (ambient)											
Specification		-25		+85	-25		+85	-55		+125	°C
Operating, derated performance		-55		+125	-55		+125	-55		+125	°C
Storage		-65		+150	-65		+150	-65		+150	°C
θ junction-case			15			15			15		°C/W
θ junction-ambient			45			45			45		°C/W

* Specifications same as for 3554AM

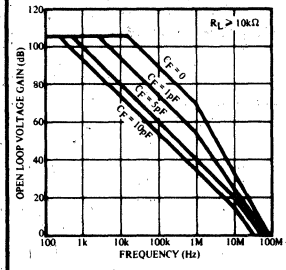
** Doubles every +10°C

† This parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.

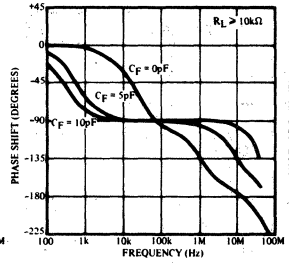
TYPICAL PERFORMANCE CURVES

at T_C = +25°C and ±15VDC unless otherwise noted.

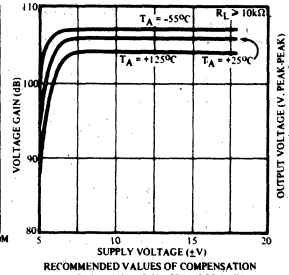
OPEN LOOP RESPONSE



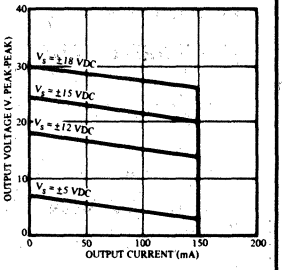
OPEN LOOP RESPONSE



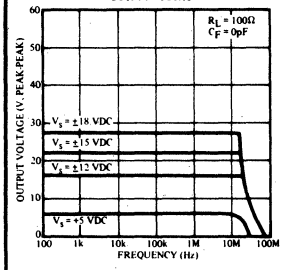
VOLTAGE GAIN



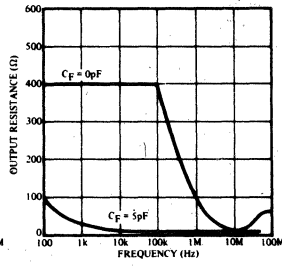
OUTPUT VOLTAGE VS OUTPUT CURRENT



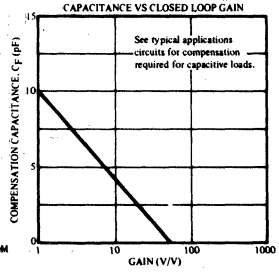
OUTPUT VOLTAGE



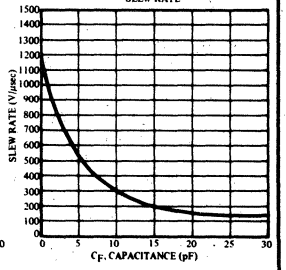
OPEN LOOP OUTPUT RESISTANCE VS FREQUENCY



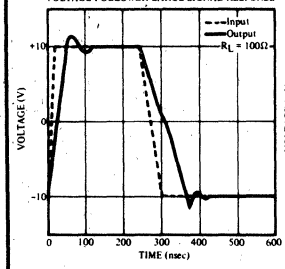
RECOMMENDED VALUES OF COMPENSATION CAPACITANCE VS CLOSED LOOP GAIN



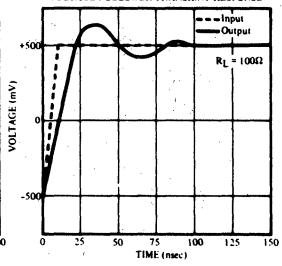
SLEW RATE



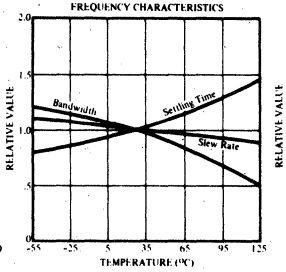
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



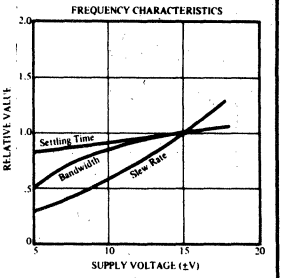
VOLTAGE FOLLOWER TRANSIENT RESPONSE



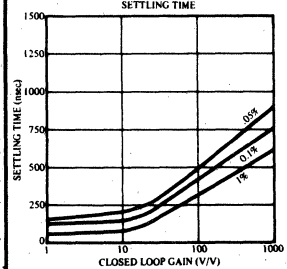
FREQUENCY CHARACTERISTICS



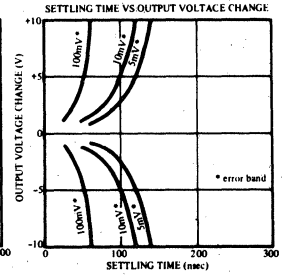
FREQUENCY CHARACTERISTICS



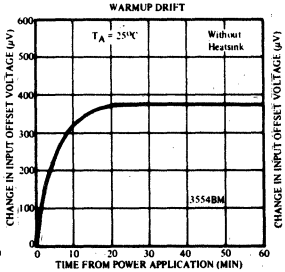
SETTLING TIME



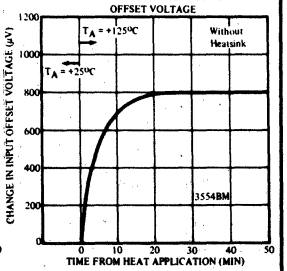
SETTLING TIME VS OUTPUT VOLTACE CHANGE



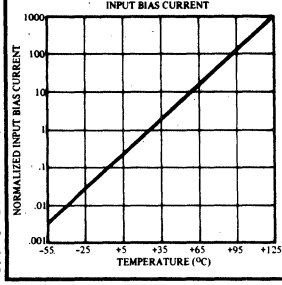
WARMUP DRIFT



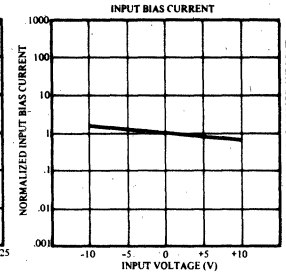
EFFECT OF THERMAL SHOCK ON OFFSET VOLTAGE



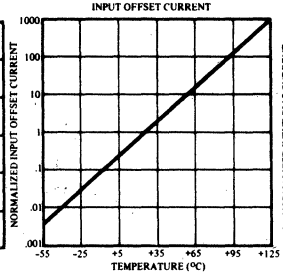
INPUT BIAS CURRENT



INPUT BIAS CURRENT



INPUT OFFSET CURRENT



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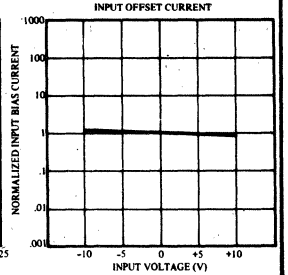
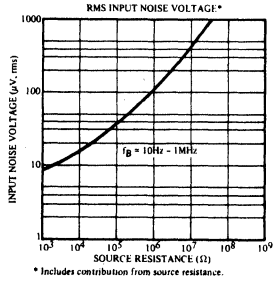
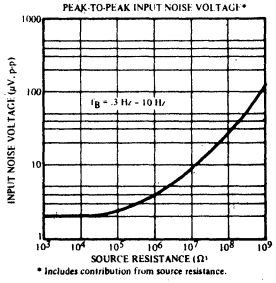
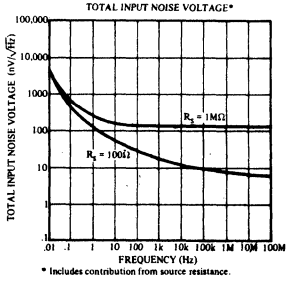
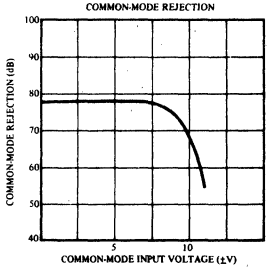
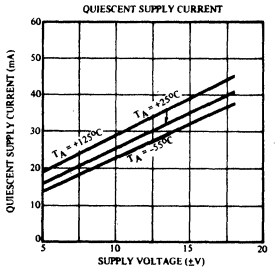


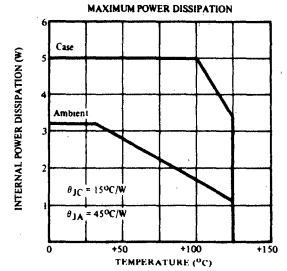




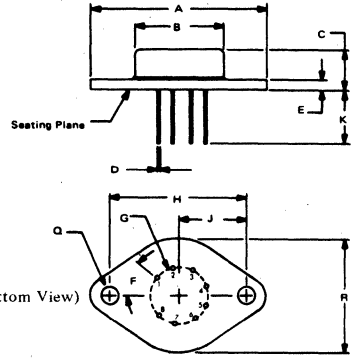








MECHANICAL



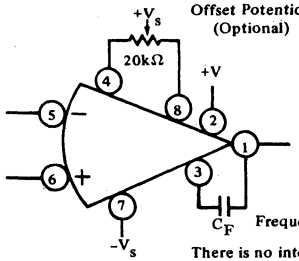
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.55
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

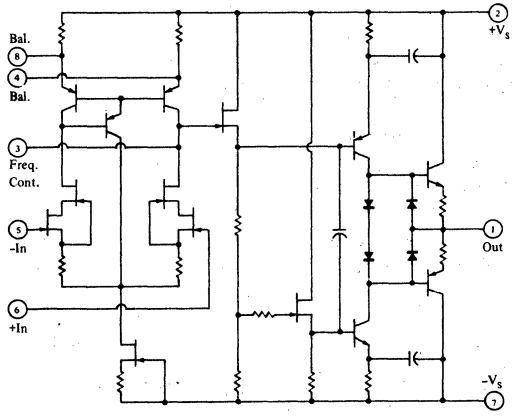
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

AMPLIFIER CONNECTIONS



There is no internal case connection.



APPLICATIONS INFORMATION

WIRING PRECAUTIONS

The 3554 is a wideband, high frequency operational amplifier that has a gain-bandwidth product exceeding 1 Gigahertz. The full performance capability of this amplifier will be realized by observing a few wiring precautions and high frequency techniques.

Of all the wiring precautions, grounding is the most important and is described in an individual section. The mechanical circuit layout also is very important. All circuit element leads should be as short as possible. All printed circuit board conductors should be wide to provide low resistance, low inductance connections and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitances should be minimized especially at high impedance nodes such as the input terminals of the amplifier. Pin 5, the inverting input, is especially sensitive and all associated connections must be short. Stray signal coupling from the output to the input or to pin 8 should be minimized. A recommended printed circuit board layout is shown with the TYPICAL CIRCUITS. It also may be used for test purposes as described below.

When designing high frequency circuits low resistor values should be used; resistor values less than 5.6kΩ are recommended. This practice will give the best circuit performance as the time constants formed with the circuit capacitances will not limit the performance of the amplifier.

GROUNDING

As with all high frequency circuits a ground plane and good grounding techniques should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pick up. An example of an adequate ground plane and good high frequency techniques is the Settling Time Test Circuit Layout shown with the TYPICAL CIRCUITS.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A combination of a 1μF tantalum capacitor in parallel with a 470pF ceramic capacitor is a suitable bypass.

In inverting applications it is recommended that pin 6, the non-inverting input, be grounded rather than being connected to a bias current compensating resistor. This assures a good signal ground at the non-inverting input. A slight offset error will result; however, because the resistor values normally used in high frequency circuits are small and the bias current is small, the offset error will be minimal.

If point to point wiring is used or a ground plane is not, single point grounding should be used. The input signal return and the load signal return and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

It is recommended that the case of the 3554 not be grounded during use (it may, if desired). A grounded case will add a slight capacitance to each pin. To an already functional circuit grounding the case will probably require slight compensation readjustment and the compensation capacitor values will be slightly different from those recommended in the typical performance curves. There is no internal connection to the case.

Proper grounding is the single most important aspect of high frequency circuitry.

GUARDING

The input terminals of the 3554 may be surrounded by a guard ring to divert leakage currents from the input terminals. This technique is particularly important in low bias current and high input impedance applications. The guard, a conductive path that completely surrounds the two amplifier inputs, should be connected to a low impedance point which is at the input signal potential. It blocks unwanted printed circuit board leakage currents from reaching the input terminals. The guard also will reduce stray signal coupling to the input.

In high frequency applications guarding may not be desirable as it increases the input capacitance and can degrade performance. The effects of input capacitance, however, can be compensated by a small capacitor placed across the feedback resistor. This is described further in the COMPENSATION section.

COMPENSATION

The 3554 uses external frequency compensation so that the user may optimize the bandwidth or slew rate or settling time for his particular application. Several typical performance curves are provided to aid in the selection of the correct compensation capacitance value. In addition several typical circuits show recommended compensation in different applications.

The primary compensation capacitor, C_F, is connected between pins 1 and 3. As the performance curves show, larger closed loop gain configurations require less capacitance and an improved gain-bandwidth product will be realized. Note that no compensation capacitor is required for closed loop gains above 55 V/V and when the load capacitance is less than 100 pF.

When driving large capacitive loads, 470 pF and greater,

an additional capacitor, C_8, is connected between pin 8 and ground. This capacitor is typically 1000 pF. It is particularly necessary in low closed loop voltage gain configurations. The value may be varied to optimize performance and will depend upon the load capacitance value. In addition, the performance may be optimized by connecting a small resistance in series with the output and a small capacitor from pin 1 to 5. See the TYPICAL CIRCUITS for the X10 Inverter.

The flat high frequency response of the 3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2 pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving the phase margin. Resistor values less than 5.6kΩ are recommended. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed loop gain. It will typically be 2 pF for a clean layout using low resistances (1kΩ) and up to 10 pF for circuits using larger resistances.

SETTLING TIME

Settling time is truly a complete dynamic measure of the 3554's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open loop gain. The settling time may be optimized for the particular application by selection of the closed loop gain and the compensation capacitance. The best settling time is observed in low closed loop gain circuits. A performance curve shows the settling time to three different error bands.

Settling time is defined as the total time required, from the signal input step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition.

SLEW RATE

Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed loop gain or the bandwidth, per se. It is dependent upon compensation. Decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve. Stray capacitances may appear to the amplifier as compensation. To avoid limiting the slew rate performance, stray capacitances should be minimized.

CAPACITIVE LOADS

The 3554 will drive large capacitive loads (up to 1000 pF) when properly compensated. See the APPLICATIONS INFORMATION section on COMPENSATION. The effect of a capacitive load is to decrease the phase margin of the amplifier. With compensation the amplifier will provide stable operation even with large capacitive loads.

The 3554 is particularly well suited for driving 50Ω loads connected via coaxial cables due to its ±100mA output drive capability.The capacitance of the coaxial cable, 29 pF/foot of length for RG-58, does not load the amplifier when the coaxial cable or transmission line is terminated in the characteristic impedance of the transmission line.

OFFSET VOLTAGE ADJUSTMENT

The offset voltage of the 3554 may be adjusted to zero by connecting a 20kΩ linear potentiometer between pins 4 and 8 with the wiper connected to the positive supply. A small, non-inductive potentiometer is recommended. The leads connecting the potentiometer to pins 4 and 8 should be no longer than 6 inches to avoid stray capacitance and stray signal pickup. Stray coupling from the output, pin 1, to pin 4 (negative feedback) or to pin 8 (positive feedback) should be avoided.

The potentiometer is optional and may be omitted when the guaranteed offset voltage is considered sufficiently low for the particular application.

For each microvolt of offset voltage adjusted, the offset voltage temperature drift will change by ±0.004 μV/°C.

HEATSINKING

The 3554 does not require a heatsink for operation in most environments. The use of a heatsink, however, will reduce the internal thermal rise and will result in cooler operating temperatures. At extreme temperature and under full load conditions a heatsink will be necessary as indicated in the MAXIMUM POWER DISSIPATION curve. A heatsink with 8 holes for the 8 amplifier pins should be used. Burr-Brown has heatsinks available in three sizes – 3°C/W, 4.2°C/W and 12°C/W. A separate product data sheet is available upon request.

When heatsinking the 3554, it is recommended that the heatsink be connected to the amplifier case and the combination not connected to the ground plane. For a single sided printed circuit board, the heatsink may be mounted between the 3554 and the non-conductive side of the PC board, and insulating washers, etc., will not be required. The addition of a heatsink to an already functional circuit will probably require slight compensation readjustment for optimum performance due to the change in stray capacitances. The added stray capacitance from the heatsink to each pin will depend on the thickness and type of heatsink used.

SHORT CIRCUIT PROTECTION

The 3554 is short circuit protected for continuous output shorts to common. Output shorts to either supply will destroy the device, even for momentary connections. Output shorts to other potential sources are not recommended as they may cause permanent damage.

TESTING

The 3554 may be tested in conventional operational amplifier test circuits; however, to realize the full performance capabilities of the 3554, the test fixture must not limit the full dynamic performance capability of the amplifier. High frequency techniques must be employed. The most critical dynamic test is for settling time. The 3554 Settling Time Test Circuit Schematic and a test circuit layout is shown with the "Typical Circuits." The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. The layout exemplifies the high frequency considerations that must be observed. The layout also may be used as a guide for other test circuits. Good grounding, truly square drive signals, minimum stray coupling and small physical size are important.

Every 3554 is thoroughly tested prior to shipment assuring the user that all parameters equal or exceed their specifications.

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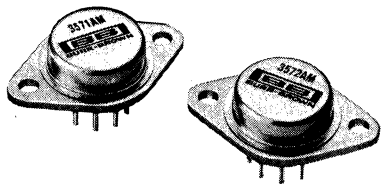
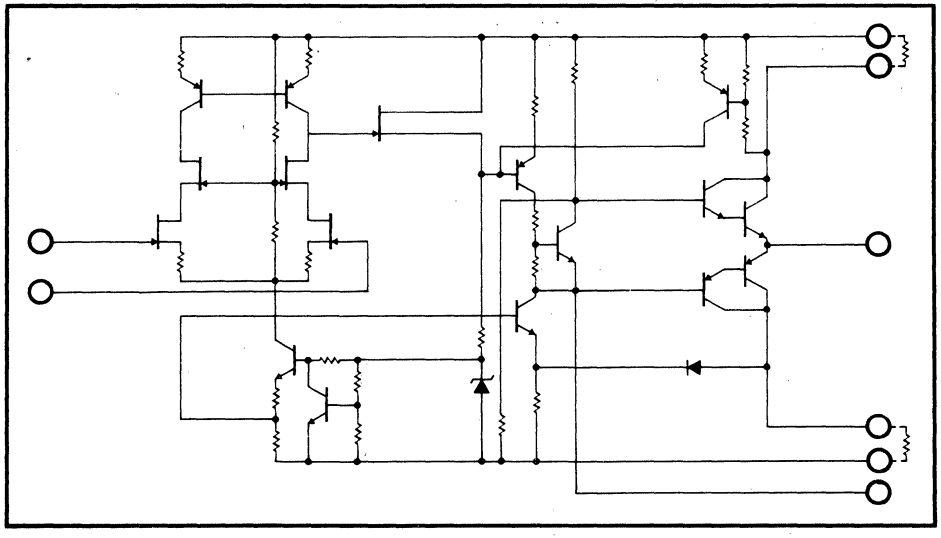


3571
3572

High Current — High Power OPERATIONAL AMPLIFIERS

FEATURES

- HIGH CURRENT
  Up to 5A Peak, 2A Continuous
- EASY TO USE
  Adjustable Current Limits
  Electrically Isolated Case
  Small Size — 8-Pin TO-3 Package
- HIGH VOLTAGE
  Up to 70V p-p Output
- SELF-PROTECTED
  Self-Contained Automatic Thermal Sensing and Shutdown
- HIGH POWER
  Delivers up to 70W to Load



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DESCRIPTION

The 3571AM and 3572AM are high output current integrated circuit operational amplifiers. Their performance, ease of use and compact size make them ideal to use in a variety of high current applications. They are especially well suited for driving permanent magnet DC servo and torque motors.

The equivalent circuit for the 3571AM and 3572AM is shown in Figure 1. The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The high input impedance provides negligible source impedance loading errors when the noninverting circuit configuration is used. The low bias currents minimize offset errors when large values of source and feedback resistors are used.

The input offset voltage at 25°C and the input offset voltage drift versus temperature are compensated by state-of-the-art laser trimming techniques. The offset voltage is low enough so that trimming will not be required in most applications. The excellent input characteristics and the high gain available mean that the use of a preamplifier, sometimes required with other servo type amplifiers, will not be necessary with the 3571AM and 3572AM.

The output stage is a class AB design which provides low distortion and minimizes quiescent current drain. The output circuitry provides for external current limiting resistors for both positive and negative output currents. This allows the user to select the current limit value suited to his particular application. This is especially desirable for driving permanent magnet motors where the high current seen during direction reversal (plugging) can demagnetize the motor.

The 3571AM and 3572AM have been designed to operate over a relatively wide supply range (±15VDC to ±40VDC) while still maintaining the high output current capability. This allows the user a wide range for the selection of the proper output voltage and current and makes the amplifiers useful for many different types of loads.

The output circuit has a unique protection feature which is practical only in integrated circuit amplifiers - self-contained automatic thermal-sensing and shut-off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the amplifiers biasing network when the temperature reaches 150°C. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases. The output current may remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal load condition is removed.

Internal thermal protection removes some of the constraints of power derating for abnormal operating conditions. The amplifier will protect itself for many conditions of excess power dissipation (see Power Derating Curve). This allows the use of a smaller heat sink to protect against abnormal output conditions since the amplifier has its own internal protection for many conditions of excess power dissipation. The output constraints of the Safe Operating Area Curves must still be observed.

The 3571AM and 3572AM have several other features that improve their utility. For instance, the metal case of the units is completely electrically isolated. (This can be contrasted to most power semiconductors where the case is connected to the collector of the device.) This simplifies mounting and reduces cost because the need for insulating spacers and bushings is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better than discrete component amplifiers. The small package size makes mounting more convenient.

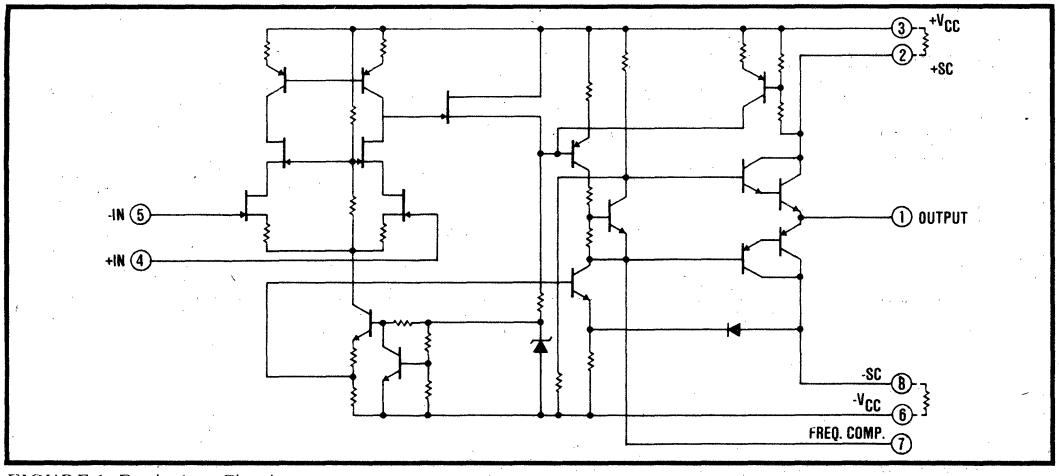


FIGURE 1. Equivalent Circuit

SPECIFICATIONS

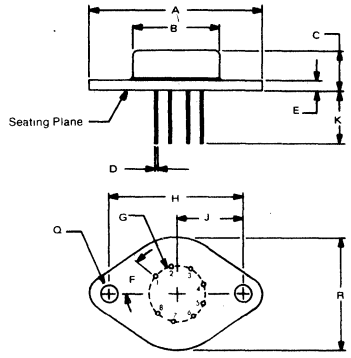
ELECTRICAL

Typical at T_{case} = 25°C and $\pm V_{CC}$ = ±35VDC max unless otherwise noted.

MODELS	3571AM	3572AM
RATED OUTPUT (to load)		
Power to Load		
Continuous, min(1)	30W	60W
Peak, min(1)	60W	150W
Output Voltage, ±(|V_{CC}|-5)V		
Continuous, min(1)	±30V at ±1A	±30V at ±2A
Peak, min(1)	±30V at 2A	±30A at 5A
Load Capacitance, min. C_C = 0	3300pF	
C_C = 1000pF	15µF	
DISSIPATION RATING		
At 25°C Case Temperature	33W	50W
Derating Above 25°C	See Typical Performance Curves	
Thermal Resistance, Case to Free Air	30°C/W	
Thermal Time Constant (no heat sink)	2 minutes	
Thermal Resistance, Junction to Case	2.5°C/W	
POWER SUPPLY		
Voltage, ±V_{CC}	±15VDC to ±40VDC	
Quiescent Current, max	±35mA	
OPEN LOOP		
Gain min, at R_{load} = 30Ω (3572AM)	94dB	
R_{load} = 60Ω (3571AM)		
Output Impedance	2.5Ω	
FREQUENCY RESPONSE		
Unity Gain Bandwidth, Small Signal	500kHz	
Full Power Bandwidth	16kHz at Vpk = 30V	
Slew Rate, C_C = 1000pF	3V/µsec	
INPUT OFFSET VOLTAGE		
Initial at 25°C, max	±2mV	
Drift vs. Temp., max	±40µV/°C	
Drift vs. Supply Voltage	±100µV/V	
Drift vs. Time	50µV/mo	
Drift vs. Power Dissipation (T_C constant)	20µV/W	
INPUT BIAS CURRENT		
Initial at 25°C, max	-100pA	
Drift vs. Temp.	doubles every 10°C	
Drift vs. Supply Voltage	0.5pA/V	
INPUT OFFSET CURRENT		
Initial at 25°C	±50pA	
Drift vs. Temp.	doubles every 10°C	
Drift vs. Supply Voltage	0.5pA/V	
INPUT IMPEDANCE		
Differential	10^{11}Ω || 10pF	
Common-mode	10^{11}Ω	
INPUT NOISE		
Voltage 0.01Hz to 10Hz, p-p	4µV	
10Hz to 1kHz, rms	3µV	
Current 0.01Hz to 10Hz, p-p	1pA	
10Hz to 1kHz, rms	0.1pA	
INPUT VOLTAGE RANGE		
Max Safe Differential Voltage	(+V_{CC} + |-V_{CC}|)	
Max Safe Common-mode Voltage	+V_{CC} to -V_{CC}	
Common-mode Voltage, Linear Operation	±(|V_{CC}| -10)V	
Common-mode Rejection	80dB min., 90dB, typ.	
TEMPERATURE RANGE (Case)		
Specification	-25°C to +85°C	
Operating	-55°C to +125°C	
Storage	-55°C to +125°C	

NOTE:
1. Safe Operating Area and Power Derating limitations must be observed.

MECHANICAL



NOTE:
Leads in true position within 0.010" 0.25mm R at MMC at seating plane.

Pin numbers shown for reference only
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
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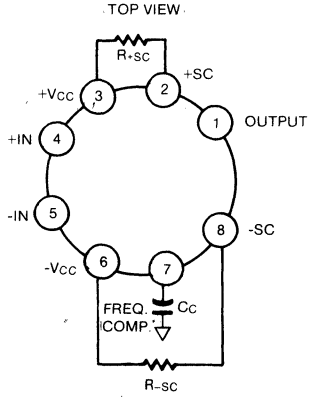
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

CONNECTION DIAGRAM



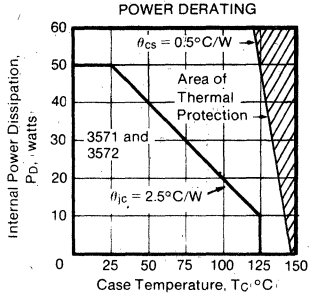
The case is electrically isolated. It is recommended that the case be grounded during use.

*A 1000pF ±20% ceramic capacitor is recommended for all circuit configurations and at all amplifier gains. The capacitor's lead lengths should be short. For gains above 10V/V, C_C is not absolutely required but is recommended.

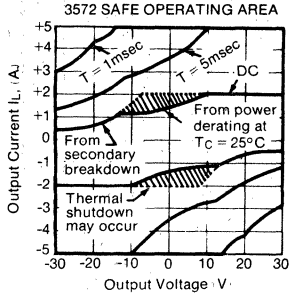
TYPICAL PERFORMANCE CURVES

(Typical T_{case} = 25°C and $\pm V_{CC}$ = ±35VDC unless otherwise noted.)

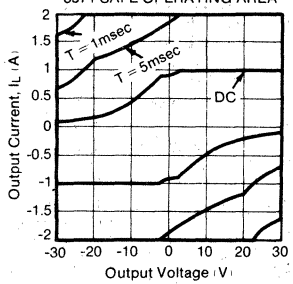
POWER DERATING



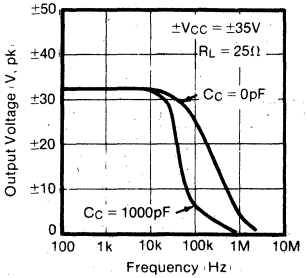
3572 SAFE OPERATING AREA



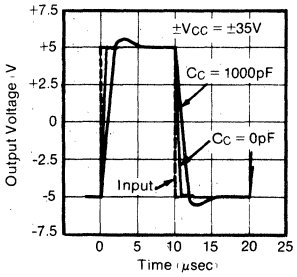
3571 SAFE OPERATING AREA



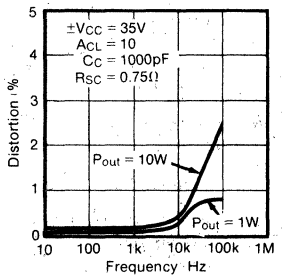
OUTPUT VOLTAGE VS. FREQUENCY



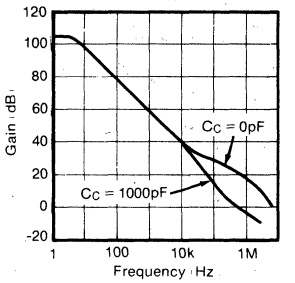
VOLTAGE FOLLOWER PULSE RESPONSE



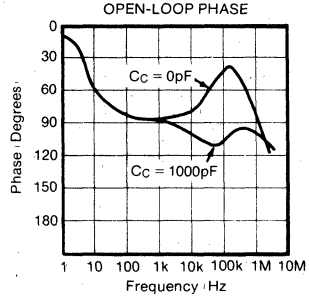
DISTORTION VS FREQUENCY



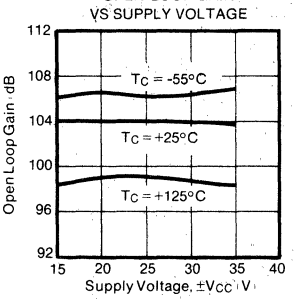
OPEN-LOOP GAIN VS FREQUENCY



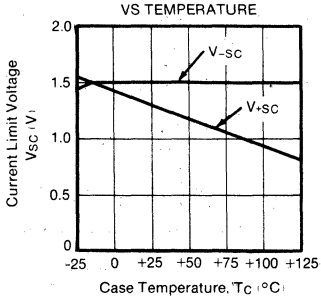
OPEN-LOOP PHASE



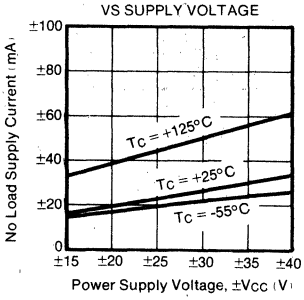
OPEN-LOOP GAIN VS SUPPLY VOLTAGE



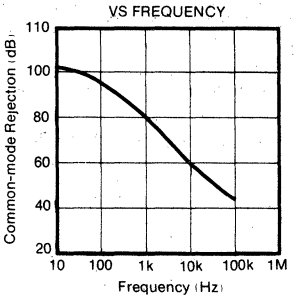
CURRENT LIMIT VOLTAGE VS TEMPERATURE



QUIESCENT CURRENT VS SUPPLY VOLTAGE



COMMON-MODE REJECTION VS FREQUENCY



INSTALLATION AND OPERATING INSTRUCTIONS

GENERAL PRECAUTIONS

Current Limiting

It is recommended that during initial amplifier setup, particularly in breadboarding and when a lack of familiarity with the amplifier exists, that the current limit be set at about 250mA ($R_{SC} \cong 5.6\Omega$). This will allow verification of the circuit and will minimize the possibility of damaging the amplifier. Later, when the circuit configuration and connections have been proven, the current limits can be raised to the desired value.

Minimum Heat Sink

The 3571AM and 3572AM require a minimum heat sink of 16°C W or lower in order to insure thermal stability (mounting on a 3" x 3" x 0.06" piece of 80% copper-clad printed circuit board material will be sufficient). Normally, this will not be a consideration since a larger heat sink will be used to provide the proper power dissipation as described in the Thermal Considerations section which follows.

Proper Grounding and Power Supply Bypassing

Particular attention should be given to proper grounding practices because the large output currents can cause significant grounding-loop errors. Proper connections are shown in Figure 2.

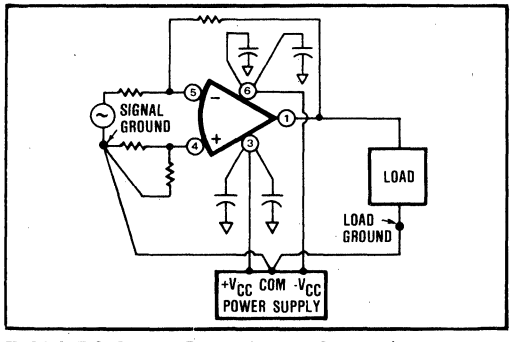


FIGURE 2. Proper Power Supply Connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be physically separated from the amplifier input and signal leads.

The amplifier power supply should be bypassed with 50μF tantalum capacitors connected in parallel with 0.01μF ceramic capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The amplifiers are designed so that both the positive and negative load current limits can be adjusted with external resistors, R_{+SC} and R_{-SC} respectively. The value of the resistors are given by the following equations:

$$R_{+SC} = \frac{1.3\ (\text{volts})}{I_{+limit}(\text{amps})},\quad R_{-SC} = \frac{1.5\ (\text{volts})}{I_{-limit}(\text{amps})}$$

I_{limit} is the desired maximum current. The maximum power dissipation of the resistors is $P_{max} = R_{SC}(I_{limit})^2$. The current limits determined by the equations above are accurate to about ±10%. The variation of I_{limit} versus temperature is shown in the Typical Performance Curves. Both $+V_{CC}$ and $-V_{CC}$ must be on for the current limits to function.

To avoid introducing unwanted inductance into the current limit circuitry, which may introduce oscillations and permanent damage, both current limit resistors must be noninductive. Do not use wire wound resistors. Carbon composition resistors are preferred and paralleling them can provide a wide current limit range at the wattage needed.

The maximum value of the negative current limit resistor is 15Ω (100mA, min). Exceeding this value, or an open circuit, could permanently damage the internal 75Ω, thin-film resistor which parallel R_{-SC}.

The amplifier should be used with as low a current limit as possible for the particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and increase reliability by limiting the internal power dissipation of the amplifier.

THERMAL CONSIDERATIONS

The 3571AM and 3572AM are rated for 150°C maximum junction temperature. The thermal resistance from junction to case (θ_{jc}) is 2.5°C W. The corresponding Power Derating Curve is given in the Typical Performance Curves.

The internal power dissipation of the amplifier is given by the equation $P_D = P_{DQ} + P_{DL}$ where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipated in the output stage due to the load. (For $\pm V_{CC} = \pm 40V$, $P_{DQ} = 80 \times 0.035 = 2.8W$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{out}$) the maximum value of P_{DL} occurs at $\pm V_{out} = \pm V_{CC}$ 2 and is equal to $P_{DL\ max} = (\pm V_{CC})^2$ $4R_L$. Figure 3 shows P_D as function of the output voltage with the load resistance as a running parameter.

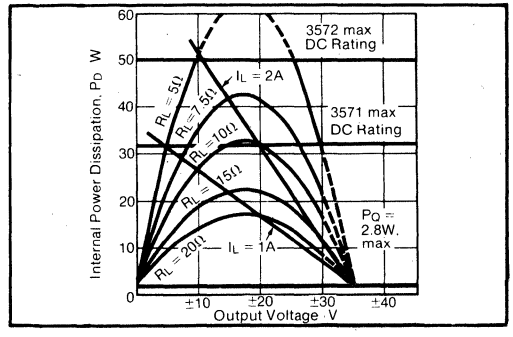


FIGURE 3. Internal Power Dissipation vs. Output Voltage.

P_{DL} for any other value of V_{out} can be computed from

$$P_{DL} = (\pm V_{CC} - \pm V_{out}) \cdot I_L = (\pm V_{CC} - \pm V_{out}) \left(\frac{\pm V_{out}}{R_L} \right).$$

The use of an adequate heat sink is mandatory and thermal resistance of the heat sink (θ_{hs}) can be determined from the equation:

$$\theta_{hs} = (T_J - T_A P_D) - \theta_{jc}$$

where T_J is the desired amplifier junction temperature (+150°C, max), T_A is the ambient temperature, P_D is the amplifiers dissipation, $P_D = P_{DO} + P_{DL}$, and θ_{jc} is the junction to case thermal resistance of the amplifier. Burr-Brown Application Note AN-83 entitled, "How to Determine What Heat Sink to Use", is available for additional information.

The electrically isolated case of the 3571AM and 3572AM simplifies mounting the amplifiers to the heat sink (and the heat sink to any other assemblies) since there is no need for electrical insulation. Thermal joint compound and lock washers should be used to prevent mechanical relaxation due to thermal stresses.

Safe Operating Area

There are additional constraints on the output voltage and current other than those just due to the maximum internal power dissipation of the amplifiers. These are related to the prevention of secondary breakdown in the output stage transistors. These restrictions are shown in the Safe Operating Area Curves in the Typical Performance Curves.

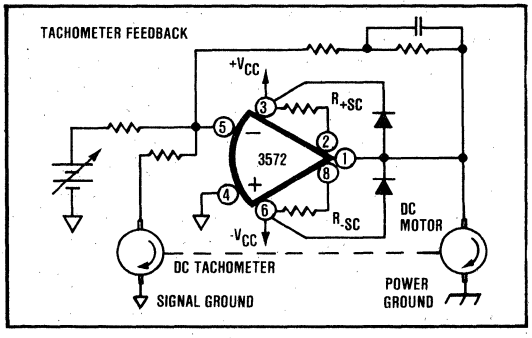
Application Constraint

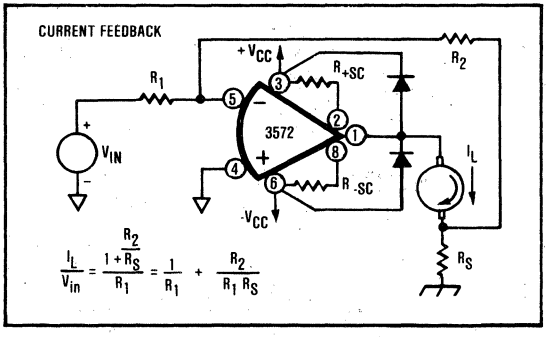
Because of the possibility of damaging the output stage if frequency instability (oscillations) occurs, applications with an inductive load which will activate the current limit of the amplifier, are limited to a load impedance phase angle of less than 60°C leading, over the frequency band of 10kHz to 100kHz. Increasing the load's series resistance will decrease the angle, if necessary. Larger inductive loads may be applied if current limit is not activated.

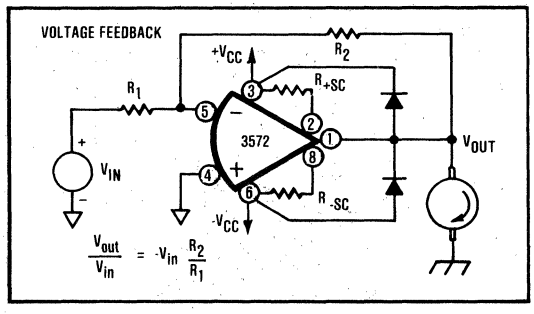
Frequency Compensation

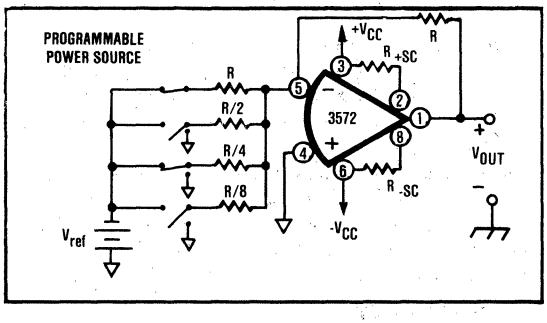
The optimum value of the compensation capacitor is 1000pF. A ±20% tolerance ceramic capacitor is recommended. The compensation capacitor should be used with all circuit configurations and at all amplifier gains (see note on Connection Diagram).

TYPICAL APPLICATIONS



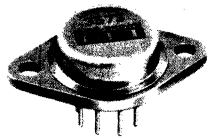






BURR-BROWN®

3573



High Current - High Power OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT POWER
  100 Watts Peak
  40 Watts Continuous
- WIDE SUPPLY RANGE
  ±10 to ±34 Volts
- HIGH OUTPUT CURRENT
  ±5 Amps Peak
  ±2 Amps Continuous
- SMALL SIZE: TO-3 PACKAGE
- LOW COST

APPLICATIONS

- DC MOTORS
- AC MOTORS
- ACTUATORS
- ELECTRONIC VALVES
- SYNCROS

DESCRIPTION

If you need to supply 100 watts peak or 40 watts continuous, yet must choose a small, easy to use op amp, you'll find the 3573 a logical solution. This hybrid IC delivers ±5A peak minimum at ±20V minimum to the load when operated from ±28V power supplies. The design of this op amp has been optimized for low cost while preserving moderately good input and distortion characteristics.

Output circuitry provides for external current limiting resistors for both positive and negative currents. This allows current limits to be set to values dictated by the op amp's application. 3573 is internally frequency compensated and is unconditionally stable with capacitive loads to 3300pF.

Housed in a small, rugged, hermetically sealed 8-lead TO-3 package, 3573 will withstand severe environments far better than discrete component amplifiers. The metal case is completely electrically isolated from the amplifier circuitry. Thus, mounting is easier (no isolation washers or spacers) and the hazards of a case connected to the output or supply voltage is eliminated.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

ELECTRICAL SPECIFICATIONS

At T_{case} = 25°C and $\pm V_{CC}$ = ±28VDC unless otherwise noted.

PARAMETER	CONDITIONS	3573AM MIN	3573AM TYP	3573AM MAX	UNITS
OPEN LOOP GAIN, DC	$R_L \geq 30\Omega$	94	115		dB
RATED OUTPUT					
Power to Load[1]					
Continuous		40			W
Peak		100			W
Output Current					
Continuous		±2			A
Peak		±5			A
Output Voltage	$I_{out} = \pm 5A$[4]	±20	±23		V
DYNAMIC RESPONSE					
Bandwidth, Unity Gain	Small Signal		1		MHz
Full Power Bandwidth		15	23		kHz
Slew Rate		1.5	2.6		V/µs
INPUT OFFSET VOLTAGE					
Initial Offset			±5	±10	mV
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±10	±65	µV/°C
vs Supply Voltage			±35		µV/V
INPUT BIAS CURRENT					
Initial	T_{case} = 25°C		15	40	nA
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±0.05		nA/°C
vs Supply Voltage			±0.02		nA/V
INPUT DIFFERENCE CURRENT					
Initial	T_{case} = 25°C		±5	±10	nA
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±0.01		nA/°C
INPUT IMPEDANCE					
Differential			10		MΩ
Common-mode			250		MΩ
INPUT NOISE					
Voltage Noise	f_n = 0.3Hz to 10Hz		3		µV p-p
	f_n = 10Hz to 10kHz		5		µVrms
Current Noise	f_n = 0.3Hz to 10Hz		20		pA p-p
	f_n = 10Hz to 10kHz		4.5		pA rms
INPUT VOLTAGE RANGE					
Common-mode Voltage	Linear Operation	±(V_{CC}-6)	±(V_{CC}-3)		V
Common-mode Rejection	f = DC, V_{CM} = ±22	70	110		dB
POWER SUPPLY					
Rated Voltage			±28		V
Voltage Range, derated		±10		±34	V
Current, quiescent			±2.6	±5	mA
TEMPERATURE RANGE					
Operating	T_{case}	-25		+85	°C
Storage		-65		+150	°C

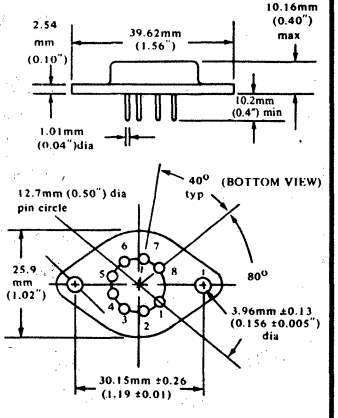
ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	±34VDC
Internal Power Dissipation[1]	45W
Differential Input Voltage[2]	±62VDC
Input Voltage Range[2]	±31VDC
Storage Temperature Range	-65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Output Short-Circuit Duration[3]	Continuous
Junction Temperature	150°C

1. Package must be derated based on a junction to case thermal resistance of 2.8°C/W, or a junction to ambient thermal resistance of 30°C/W.
2. For supply voltages less than ±34VDC, the absolute maximum voltage is three volts less than supply voltage.
3. Safe Operating Area and Power Derating Curves must be observed.
4. With R±SC = 0.

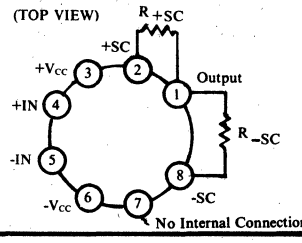
MECHANICAL

TO-3



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

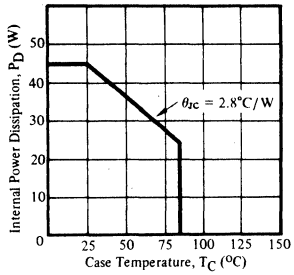
CONNECTION DIAGRAM



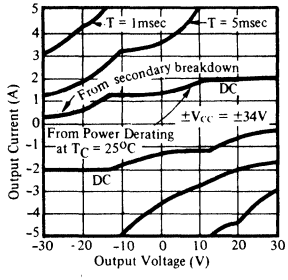
TYPICAL PERFORMANCE CURVES

(Typical at 25°Case and $\pm V_{CC} = \pm 28$ VDC unless otherwise noted.)

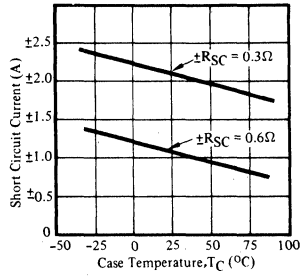
POWER DERATING CURVE



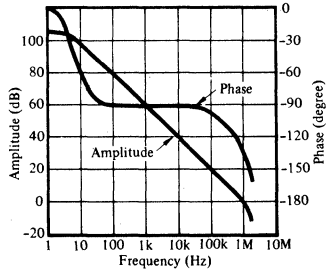
SAFE OPERATING AREA



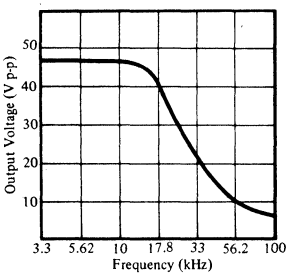
CURRENT LIMITING



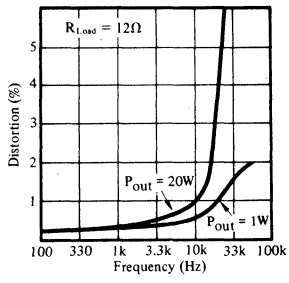
OPEN LOOP FREQUENCY RESPONSE



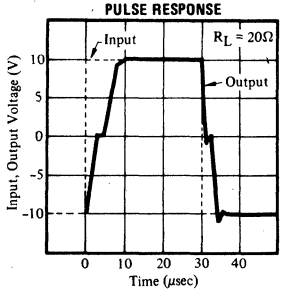
OUTPUT VOLTAGE VS FREQUENCY



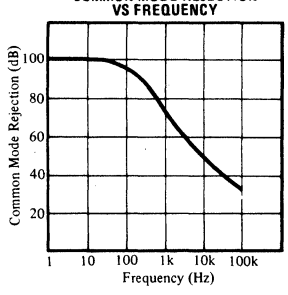
HARMONIC DISTORTION



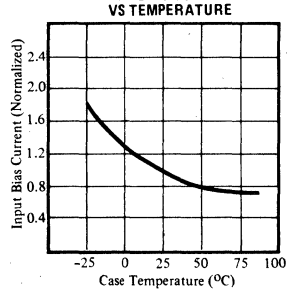
VOLTAGE FOLLOWER PULSE RESPONSE



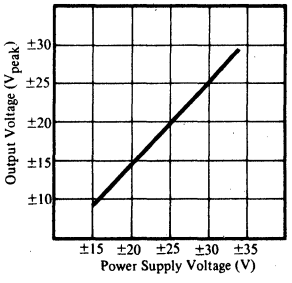
COMMON MODE REJECTION VS FREQUENCY



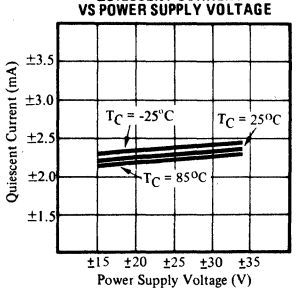
INPUT BIAS CURRENT VS TEMPERATURE



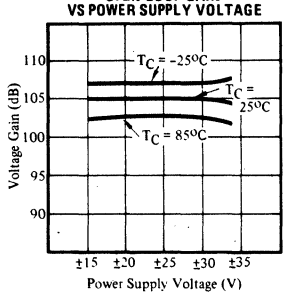
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE



QUIESCENT CURRENT VS POWER SUPPLY VOLTAGE



OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



INSTALLATION AND OPERATING INSTRUCTIONS

GENERAL PRECAUTIONS

CURRENT LIMITING

It is recommended that during initial amplifier setup, particularly in breadboarding and when a lack of familiarity with the amplifier exists, that the current limit be set at about 250mA ($R_{SC} \cong 2.6\Omega$). This will allow verification of the circuit and will minimize the possibility of damaging the amplifier. Later, when the circuit configuration and connections have been proven, the current limits can be raised to the desired value.

PROPER GROUNDING & POWER SUPPLY BYPASSING

Particular attention should be given to proper grounding practices because the large output currents can cause significant ground loop errors. Figure 1 illustrates proper connections.

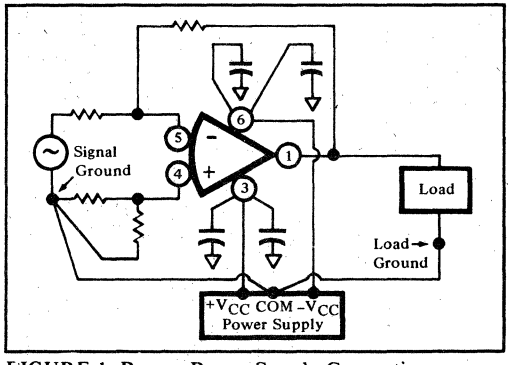


FIGURE 1. Proper Power Supply Connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power supply bypassed with 50μF tantalum capacitors connected in parallel with 0.01 μF ceramic capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The amplifier is designed so that both the positive and negtive load current limits can be adjusted with external resistors, R_{+SC} and R_{-SC} respectively. The value of the resistors are given by the following equation:

$$R_{SC} = \frac{0.65 \text{ (volts)}}{I_{limit} \text{ (amps)}}$$

I_{limit} is the desired maximum current. The maximum power dissipation of the resistors is $P_{max} = R_{SC} (I_{limit})^2$. The current limits determined by the equations above are accurate to about $\pm 10\%$. The variation of I_{limit} vs temperature is shown in the Typical Performance Curves.

The amplifier should be used with as low a current limit as possible for the particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and increase reliability by limiting the internal power dissipation of the amplifier.

THERMAL CONSIDERATIONS

The 3573AM is rated for 150°C maximum junction temperature. The thermal resistance from junction to case (θ_{jc}) is 2.8°C/W per watt. The corresponding Power Derating Curve is given in the Typical Performance Curves section.

The internal power dissipation of the amplifier is given by the equation $P_D = P_{DQ} + P_{DL}$ where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipated in the output stage due to the load.

The thermal resistance of the required heat sink (θ_{hs}) can be determined from the equation:

$$\theta_{hs} = \frac{T_J - T_A}{P_D} - \theta_{jc}$$

where T_J is the desired amplifier junction temperature (+150°C max), T_A is the ambient temperature, P_D is the amplifier's dissipation, $P_D = P_{DQ} + P_{DL}$, and θ_{jc} is the junction to case thermal resistance of the amplifier.

The electrically isolated case of the 3573AM simplifies mounting the amplifiers to the heat sink (and the heat sink to any other assemblies) since there is no need for electrical insulation. Thermal joint compound and lock washers should be used to prevent mechanical relaxation due to thermal stresses.

SAFE OPERATING AREA

There are additional constraints on the output voltage and current other than those just due to the maximum internal power dissipation of the amplifiers. These are related to the prevention of secondary breakdown in the output stage transistors. These restrictions are shown in the SAFE OPERATING AREA CURVES in the Typical Performance Curves.

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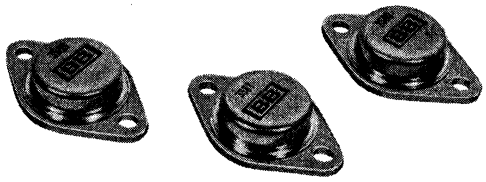


3580
3581
3582

High Voltage
OPERATIONAL AMPLIFIERS

FEATURES

- HIGH OUTPUT SWINGS, up to ±145V (3582)
- LARGE LOAD CURRENTS, up to ±60mA (3580)
- DIFFICULT TO DAMAGE, automatic thermal shutoff
- REDUCES SOURCE LOADING, $10^{11}\Omega$ Input Z
- PRESERVES SYSTEM ACCURACY, 110dB CMR 20pA bias current

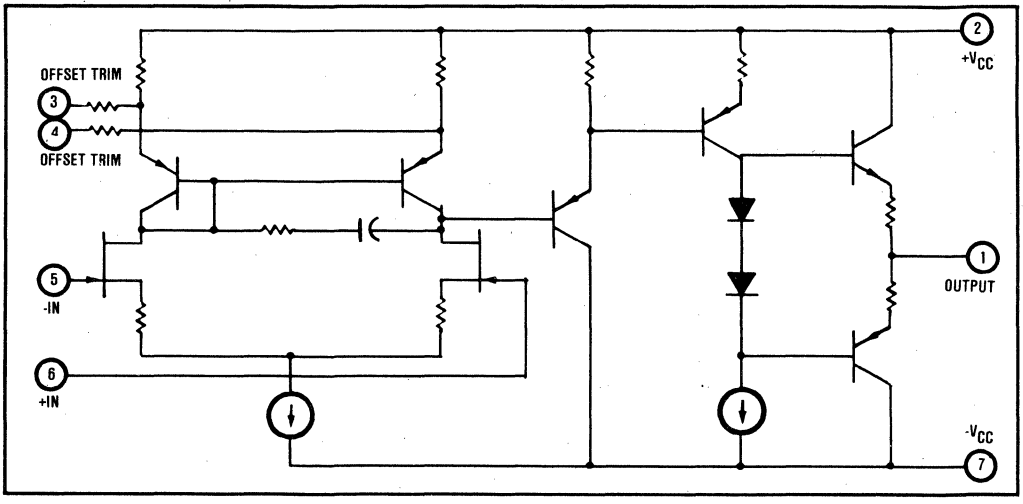
DESCRIPTION

The 3580 series is the first family of Integrated Circuit operational amplifiers which will provide output voltage swings of up to ±145V.

The monolithic FET input stage has low bias currents (20pA) which minimizes the offset voltages caused by the bias current and the large resistance normally associated with high voltage circuits.

The 3580 series is packaged in a TO-3 package which will dissipate over 3W of power without a heat sink and 4.5W with a suitable heat sink.

The input stage is protected against overvoltages and the output stage is protected against short-circuits-to-ground. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.



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THEORY OF OPERATION

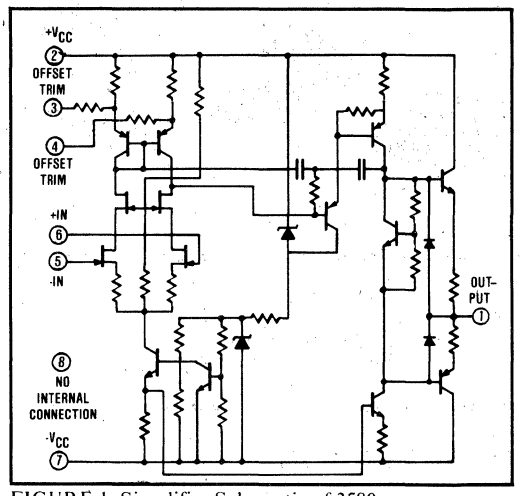


FIGURE 1. Simplifier Schematic of 3580.

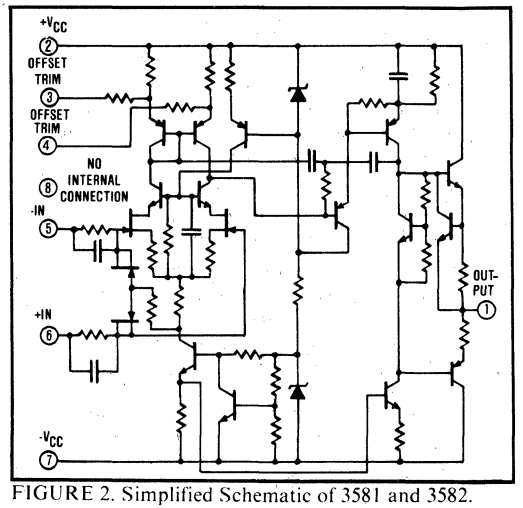


FIGURE 2. Simplified Schematic of 3581 and 3582.

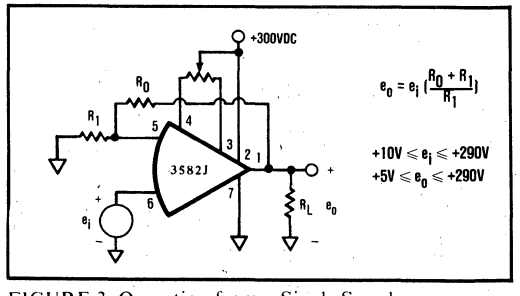


FIGURE 3. Operation from a Single Supply.

The 3580 family of integrated circuit high voltage amplifiers provides performance which previously was only available in bulky modular packages (see Figures 1 and 2). In addition to the smaller size and inherent reliability, the integrated circuit construction offers other advantages not normally available in modular or discrete component units. The amplifiers have thermal sensing and shut-off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the input stage current source when the temperature reaches a critical level. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases.

If the cause of the abnormal power dissipation is continuous (such as a short circuit across the load) the output current may remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal condition is removed.

The incorporation of thermal sensing and shut-off in the amplifier will allow the use of a smaller heat sink than would otherwise be required. This is due to the fact that the amplifier will protect itself and does not require a massive heat sink for protection under abnormal conditions.

Another unique feature of the 3580 family is the thorough testing of the unit receiver. In addition to the normal tests, all amplifiers are 100% tested for input protection at the full rated differential voltage ($+V_{CC}$ -V_{CC}). Each unit is also 100% tested for output short circuit to common at maximum supply voltage.

The 3581 and 3582 have a unique feature that is important in many high voltage applications. In these two models the input bias current is virtually independent of the applied common-mode voltage. This is accomplished by the true cascode input stage which keeps the drain-to-source voltage of the input transistors constant as the common-mode voltage changes.

OPERATION FROM A SINGLE SUPPLY

It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 3 illustrates a typical application.

Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should be noted that when the 3581 and 3582 amplifiers are operated from a single supply, the output stage, which is still short-circuit-current limited and thermally protected, is not protected against short circuits to ground (the 3580 will still be short circuit protected under these conditions). When the amplifiers are operated from a single supply, the voltage across one of the output transistors is high enough that secondary breakdown is a consideration. The output current must be limited in order to prevent damage. This can be done by keeping the load resistor larger than 5kΩ for the 3582 and greater than 1kΩ for the 3581.

SPECIFICATIONS

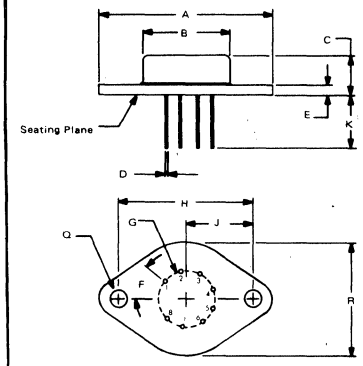
ELECTRICAL

Typical at T_{CASE} = +25°C max unless otherwise noted.

MODELS	3580J	3581J	3582J
POWER SUPPLY			
Voltage, $\pm V_{CC}$	±15VDC to ±35VDC	±32VDC to ±75VDC	±70VDC to ±150VDC
Quiescent Current, max	±10mA	±8mA	±6.5mA
RATED OUTPUT			
Voltage, $\pm\|V_{CC}\|$ -5 VDC, min	±10VDC to ±30VDC	±27VDC to ±70VDC	±65VDC to ±145VDC
Current, min	±60mA	±30mA	±15mA
Current, Short Circuit	±100mA	±50mA	±25mA
Load Capacitance, max		10nF	
OPEN-LOOP GAIN			
No Load, DC	10dB	112dB	118dB
Rated Load, DC, min	86dB	94dB	100dB
FREQUENCY RESPONSE			
Unity Gain Bandwidth, Small Signal		5MHz, min	
Full Power Bandwidth	100kHz	60kHz	30kHz
Slew Rate	15V/μsec	20V/μsec	20V/μsec
Settling Time, 0.1%		12μsec	
INPUT OFFSET VOLTAGE			
Initial at T_{CASE} = +25°C, max	±10mV	±3mV	±3mV
Drift vs Temp, max	±30μV/°C	±25μV/°C	±25μV/°C
Drift vs Supply Voltage	100μV/V	20μV/V	20μV/V
Drift vs Time	100μV/mo	50μV/mo	50μV/mo
INPUT BIAS CURRENT			
Initial at T_{CASE} = +25°C, max	-50pA	-20pA	-20pA
Drift vs Temp		doubles every 10°C	
Drift vs Supply Voltage	0.5pA/V	0.2pA/V	0.2pA/V
INPUT OFFSET CURRENT			
Initial at T_{CASE} = +25°C, max		±20pA	
Drift vs Temp		doubles every 10°C	
Drift vs Supply Voltage	0.5pA/V	0.2pA/V	0.2pA/V
INPUT IMPEDANCE			
Differential		$10^{11}\Omega$. 10pF	
Common-mode		$10^{11}\Omega$	
INPUT NOISE			
Voltage 0.01Hz to 10Hz, p-p		5μV	
10Hz to 1kHz, rms	1μV	1.7μV	1.7μV
Current 0.01Hz to 10Hz, p-p	1pA	0.3pA	0.3pA
INPUT VOLTAGE RANGE			
Max Safe Differential Voltage(1)		$+V_{CC}+\|-V_{CC}\|$	
Max Safe Common-mode Voltage		$+V_{CC}$ to $-V_{CC}$	
Common-mode Voltage, Linear Operation	$\pm\|V_{CC}\|$ -8 V	$\pm\|V_{CC}\|$ -10 V	$\pm\|V_{CC}\|$ -10 V
Common-mode Rejection	86dB	110dB	110dB
TEMPERATURE (Case)			
Specification		0°C to 70°C	
Operating		-55°C to +125°C	
Storage		-55°C to +150°C	

NOTE:
1. On Models 3581 and 3582 the inputs may be damaged by pulses at pins 5 or 6 with dV/dt≥1V/nsec. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins. No external protection is needed for slower voltage.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

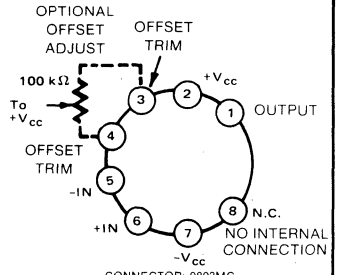
ORDER NUMBER: 3580J
3581J
3582J

WEIGHT: 15 GRAMS

CASE: METAL

PIN CONFIGURATION

TOP VIEW



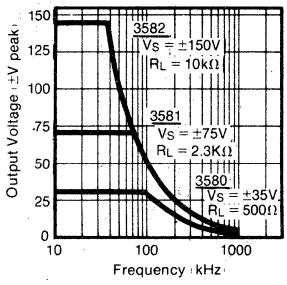
CONNECTOR: 0803MC
HEAT SINK: 0803HS
0804HS
0805HS

*The case is electrically isolated. It is recommended that the case be grounded during use.

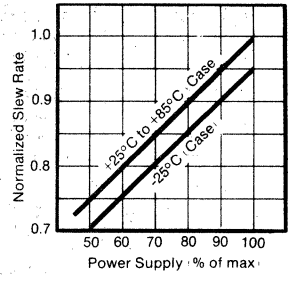
TYPICAL PERFORMANCE CURVES

T_{CASE} = +25°C and $\pm V_{CC}$ max unless otherwise noted.

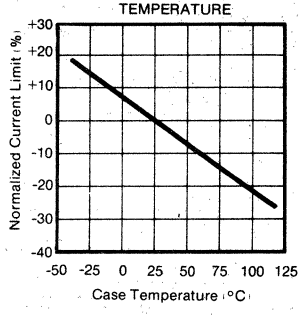
OUTPUT VOLTAGE VS FREQUENCY



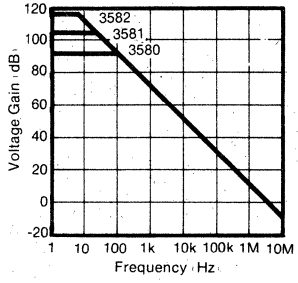
SLEW RATE VS SUPPLY VOLTAGE AT FULL LOAD



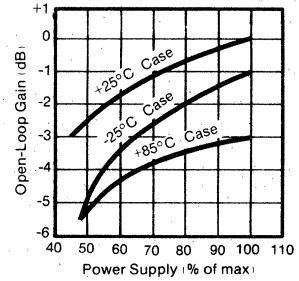
CURRENT LIMIT VS TEMPERATURE



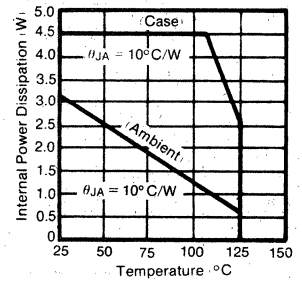
OPEN-LOOP FREQUENCY RESPONSE-FULL LOAD



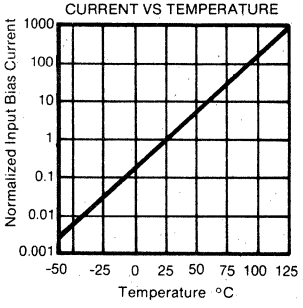
OPEN-LOOP GAIN VS SUPPLY VOLTAGE AT MAX LOAD



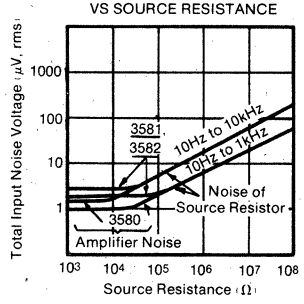
MAXIMUM POWER DISSIPATION



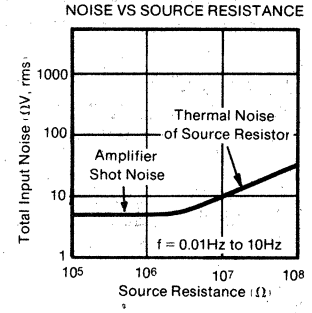
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



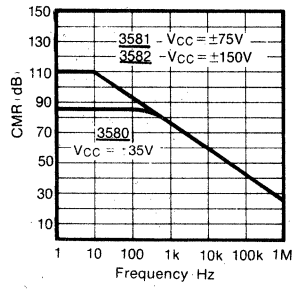
TOTAL INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



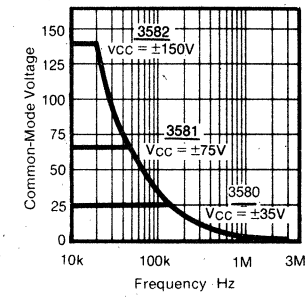
TOTAL LOW FREQUENCY INPUT NOISE VS SOURCE RESISTANCE



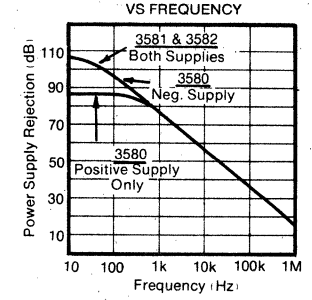
COMMON-MODE REJECTION VS FREQUENCY



MAXIMUM COMMON-MODE VOLTAGE VS FREQUENCY

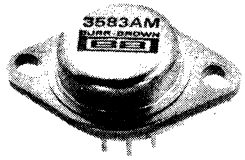


POWER SUPPLY REJECTION VS FREQUENCY



BURR-BROWN®

3583



High Voltage - High Current OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT SWINGS, Up to ±140V
- LARGE LOAD CURRENTS, ±75mA
- PROTECTED OUTPUT STAGE, Automatic Thermal Shutoff
- REDUCES SOURCE LOADING, $10^{11}\Omega$ Input Z
- PRESERVES SYSTEM ACCURACY, 110dB CMR 20pA Bias Current

APPLICATIONS

- PROGRAMMABLE POWER SUPPLY OUTPUT AMPLIFIER
- HIGH VOLTAGE CURRENT SOURCE
- POWER BOOSTER
- HIGH VOLTAGE INTEGRATOR
- DIFFERENTIAL AMPLIFIER FOR HIGH COMMON-MODE VOLTAGE CIRCUITS

DESCRIPTION

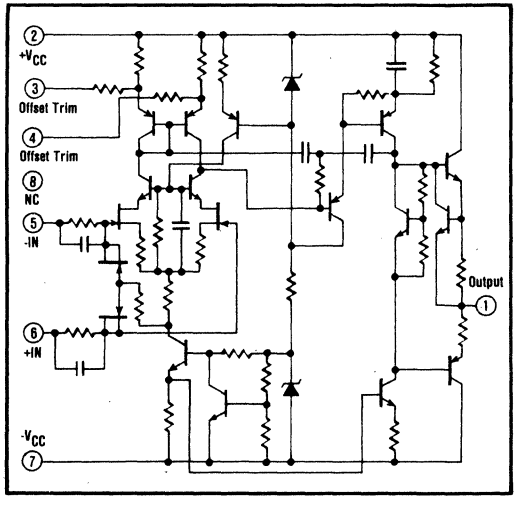
The 3583 is the first integrated circuit operational amplifier to provide output voltage swings of ±140V with currents as high as ±75mA.

The amplifier operates over a wide supply range (±50VDC to ±150VDC) and has excellent input characteristics (110dB CMR, 3mV V_{OS}, 25μV/°C $\Delta V_{OS}/\Delta T$).

The monolithic FET input stage has low bias current (20pA) which minimizes the offset voltages caused by the bias current and the large resistances normally associated with high voltage circuits.

The input stage is protected against overvoltages and the output stage is protected against short-circuits to ground for supply voltages below ±100VDC. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

Two temperature ranges are available: 0°C to +70°C (3583JM) and -25°C to +85°C (3583AM).



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SPECIFICATIONS

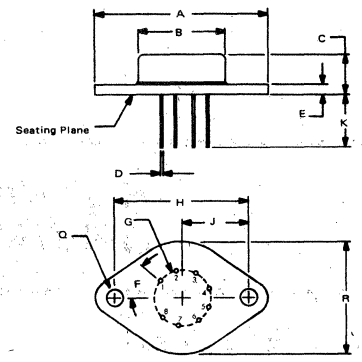
ELECTRICAL

Specifications typical at T_{CASE} = +25°C and $\pm V_{CC}$ = 150VDC unless otherwise noted.

MODELS	3583AM	3583JM
POWER SUPPLY		
Voltage, $\pm V_{CC}$	±50VDC to ±150VDC	
Quiescent Current, max	8.5mA	
RATED OUTPUT		
Voltage, $\pm\|V_{CC}\| - 10$VDC, min	±40VDC to ±140VDC	
Current, min	±75mA	
Current, Short Circuit	±100mA	
Load Capacitance, max	10nF	
OPEN-LOOP GAIN		
No Load, DC	118dB	
Rated Load, DC	94dB, min; 105dB, typ	
FREQUENCY RESPONSE		
Unity Gain Bandwidth, Small Signal	5MHz	
Full Power Bandwidth, R_L = 10kΩ	60kHz	
Slew Rate	30V/μsec	
Settling Time, 0.1%	12μsec	
INPUT OFFSET VOLTAGE T_A = +25°C		
Initial at 25°C, max	±3mV	
Drift vs Temp, max	±23μ/°C	
Drift vs Supply Voltage	±20μV/V	
Drift vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at 25°C, max	-20pA	
Drift vs Temp	doubles every 10°C	
Drift vs Supply Voltage	0.2pA/V	
INPUT OFFSET CURRENT		
Initial at 25°C	±20pA	
Drift vs Temp	doubles every 10°C	
Drift vs Supply Voltage	0.2pA/V	
INPUT IMPEDANCE		
Differential	$10^{11}\Omega \| 10$pF	
Common-mode	$10^{11}\Omega$	
INPUT NOISE		
Voltage 0.01Hz to 10Hz, p-p	5μV	
10Hz to 1kHz, rms	1.7μV	
Current 0.01Hz to 10Hz, p-p	0.3pA	
INPUT VOLTAGE RANGE		
Max Safe Differential Voltage(1)	$\|+V_{CC} + \|-V_{CC}\|$	
Max Safe Common-mode Voltage	$+V_{CC}$ to $-V_{CC}$	
Common-mode Voltage, Linear Operation	$\pm\|V_{CC}\| - 10$V	
Common-mode Rejection	110dB	
TEMPERATURE RANGE (Case)		
Specification	-25°C to +85°C	0°C to 70°C
Operating	-55°C to +125°C	
Storage	-55°C to +125°C	

NOTES:
1. The inputs may be damaged by pulses at pins 5 or 6 with dV/dt ≥ 1V/nsec. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins. No external protection is needed for slower voltage changes.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only.
Numbers may not be marked on package.

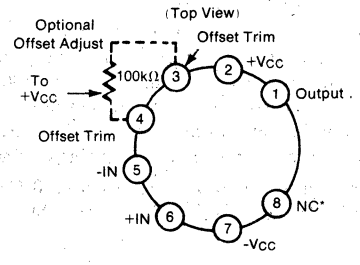
ORDER NUMBER:
3583AM 3583JM

WEIGHT:
15.1 Grams

MATING CONNECTOR:
0803MC

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

CONNECTION DIAGRAM

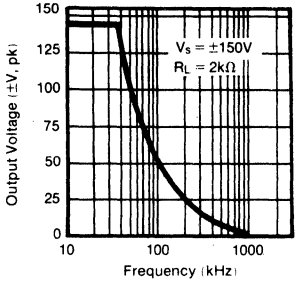


* No internal connection.
The metal case is electrically isolated. It is recommended that the case be grounded during use.

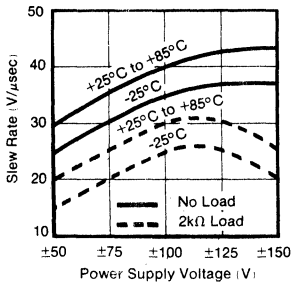
TYPICAL PERFORMANCE CURVES

Typical at T_{CASE} = +25°C and $\pm V_{CC}$ = 150VDC unless otherwise noted.

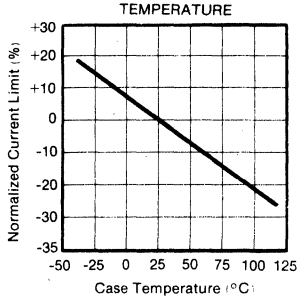
OUTPUT VOLTAGE vs FREQUENCY



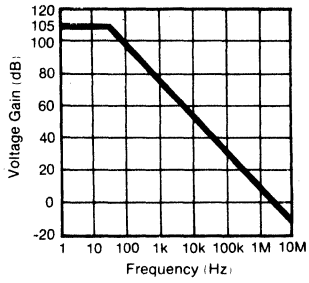
SLEW RATE vs SUPPLY VOLTAGE



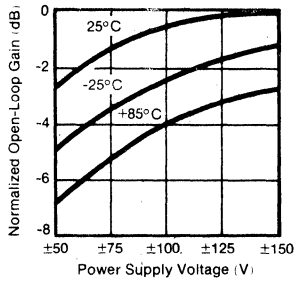
CURRENT LIMIT vs TEMPERATURE



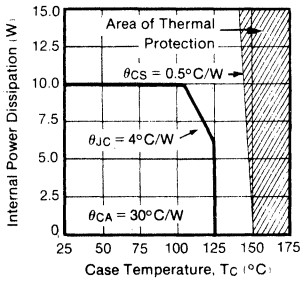
OPEN-LOOP FREQUENCY RESPONSE-FULL LOAD



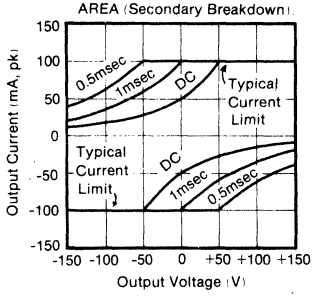
OPEN-LOOP GAIN vs SUPPLY VOLTAGE AT FULL LOAD



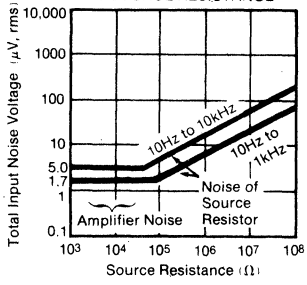
RECOMMENDED POWER DERATING



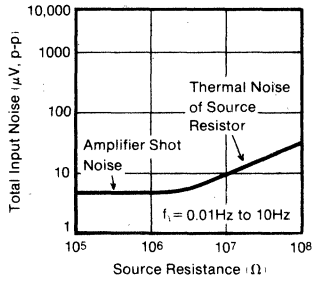
RECOMMENDED SAFE OPERATING AREA (Secondary Breakdown)



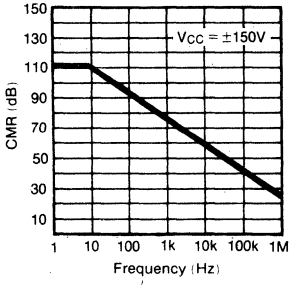
TOTAL INPUT NOISE VOLTAGE vs SOURCE RESISTANCE



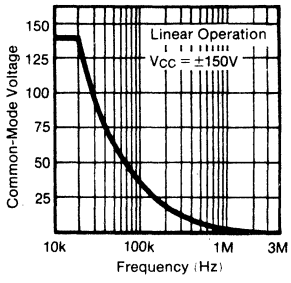
TOTAL LOW FREQUENCY INPUT NOISE vs SOURCE RESISTANCE



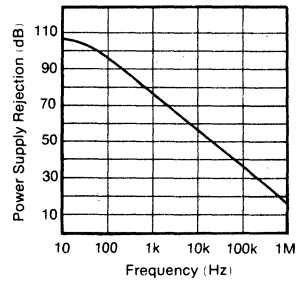
COMMON-MODE REJECTION vs FREQUENCY



COMMON-MODE VOLTAGE vs FREQUENCY



POWER SUPPLY REJECTION vs FREQUENCY



APPLICATIONS INFORMATION

The 3583 is a high voltage, high output current integrated circuit operational amplifier. Its ease of use, compact size, and excellent input and output specifications makes it well suited for a wide variety of high voltage applications.

The equivalent circuit for the 3583 is shown in Figure 1. The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The offset voltage at 25°C and the drift versus temperature are compensated by state-of-the-art laser-trimming techniques. They are low enough so that user-trimming will not be required in most applications. The high input impedance provides negligible source impedance loading errors when the noninverting circuit configuration is used. The low bias currents minimize offset errors when large values of source and feedback resistors are used.

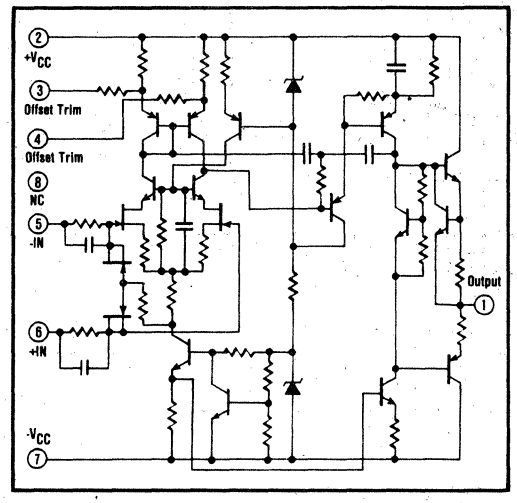


FIGURE 1. 3583 Equivalent Circuit.

A true cascade input stage is used together with considerable protection circuitry. There are voltage limiting transistors to prevent damage due to reverse bias breakdown of the input pair and current limiting resistors to limit the input current to 1mA with the inputs at ±150 volts. The units are conservatively rated (and 100% tested) at full rated differential voltage (+150V and -150V) but typically will withstand a 50% overvoltage without damage.

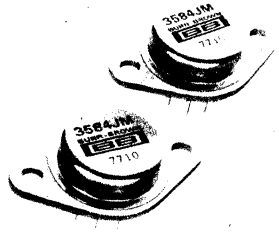
The unit operates over a wide supply range (±50V to ±150V) with outstanding common-mode rejection (110dB). It also has another feature which is important in many high voltage applications. The input bias current is virtually independent of applied common-mode voltage. The output circuit has a unique protection feature which is only practical in integrated-circuit amplifiers - self-contained automatic thermal sensing and shutoff circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the amplifier's biasing network when the temperature reaches 150°C. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases. The output current will remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal load condition is removed.

The internal thermal protection removes some of the constraints of power derating for abnormal operating conditions. The amplifier will protect itself for many conditions of excess power dissipation (see the Power Derating Curve). This allows the use of a smaller heat sink to protect against abnormal output conditions since the amplifier has its own internal protection for many conditions of excess power dissipation. The output constraints of the Recommended Safe Operating Area curves must still be observed.

The 3583 has several other features that improve its utility. For instance, the metal case of the unit is completely electrically isolated. (This can be contrasted to most power semiconductors where the case is connected to the collector of the device.) This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated. The hermetically sealed package improves reliability and will more easily withstand severe environments than do discrete component amplifiers. The small package size reduces weight and makes mounting more convenient.

Burr-Brown offers three heat sinks as accessories; 0803HS with a thermal resistance of .12°C/watt, 0804HS at 4.2°C/watt, and 0805HS at 3°C/watt. A convenient mating connector, 0803MC is also available.

BURR-BROWN®



3584

High Voltage OPERATIONAL AMPLIFIER

FEATURES

- TYPICAL GAIN-BANDWIDTH, 50MHz
- OUTPUT, +145V
- PROTECTED OUTPUT, automatic thermal shutoff
- BIAS CURRENT, -20pA
- CMR, 110dB
- SLEW RATE, 150V/usec

APPLICATIONS

- ANALOG SIMULATORS
- DIGITALLY-CONTROLLED POWER SUPPLIES
- CRT DEFLECTION
- ELECTROSTATIC TRANSDUCERS

DESCRIPTION

The 3584 is a high voltage, integrated circuit operational amplifier that will provide up to ±145V output.

The amplifier will provide a gain-bandwidth product of 20MHz minimum, 50MHz typical. The amplifier uses external frequency compensation (one R and one C) so that the user may optimize the bandwidth and slew rate for his particular application.

The amplifier operates over a wide supply range (±70VDC to ±150VDC) and has excellent input characteristics (110dB CMR, 3mV E_{os}, and 25μV/°C E_{os} Drift). The input stage is a FET. The low -20pA bias current minimizes the offset errors caused by the large value resistors normally used in high voltage circuits.

The input stage is protected against overvoltages and the output stage is protected against short circuits to ground. A special thermal sensing circuit helps to prevent damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DISCUSSION

The 3584 is a high voltage, integrated circuit operational amplifier. Its ease of use, compact size, and excellent input and output specifications makes it well suited for a wide variety of high voltage and high speed applications.

The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The offset voltage and the drift are laser trimmed. They are low enough so that user trimming will not be required in most applications.

To achieve the high common-mode voltage capability and rejection a true cascode input stage is used together with considerable protection circuitry. There are voltage limiting diodes to prevent damage due to reverse bias breakdown of the input pair and current limiting resistors to limit the steady state input current to 1mA with the inputs at ±150 volts. The units are conservatively rated (and 100% tested) at full rated differential voltage (+150 and -150V) but typically will withstand a 50% overvoltage without damage.

It also has another feature which is important in many high voltage applications. The input bias current is virtually independent of applied common-mode voltage. This is a benefit of the true cascode input stage which keeps the drain to source voltage of the input transistors constant as the common-mode voltage changes.

The amplifier contains automatic thermal sensing and shut-off circuitry which automatically turns the amplifier off when the internal (substrate) temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating all current sources when the temperature reaches a critical level. As this happens, the output current gradually decreases to zero. The output current may remain at a low value or oscillate between 2 values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal condition is removed.

The incorporation of thermal sensing and shut-off in the amplifier will require a smaller heat sink than normal. This is due to the fact that the amplifier will protect itself and does not require a massive heat sink for protection under abnormally high power dissipation.

The 3584 has several other features that improve its utility. The metal case of the unit is completely electrically isolated. This simplifies mounting and reduces cost since the need for insulating spacers is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better. And the small package size reduces weight and makes mounting more convenient.

OPERATION FROM A SINGLE SUPPLY

It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 1 illustrates a typical application. Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should be noted that when the amplifier is operated from a single supply, the output stage, which is still short circuit current limited and thermally protected, is not protected for short circuits to ground under all operating conditions. Consult the safe operating area curve.

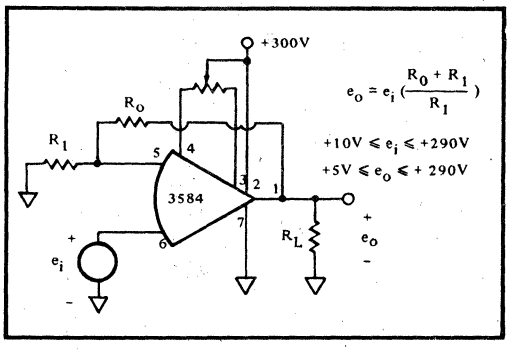


FIGURE 1. Operation from a single supply.

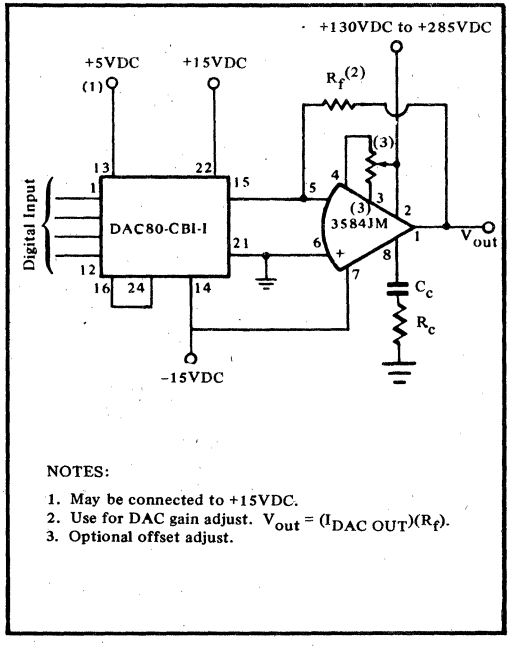


FIGURE 2. High Speed, High Voltage DAC.

SPECIFICATIONS

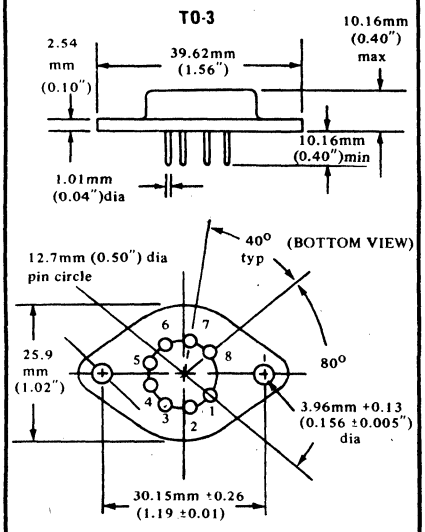
ELECTRICAL

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

MODELS	3584JM
POWER SUPPLY	
Voltage, $\pm V_{cc}$	±70 to ±150 VDC
Quiescent Current, max	±6.5mA
RATED OUTPUT	
Voltage, ± (| V_{cc} | -5)VDC, min	±65 to ±145 VDC
Current, min	±15mA
Current, Short Circuit	±25mA
Load Capacitance, max	10 nF
OPEN LOOP GAIN	
No Load, DC	120 dB
Rated Load, DC, min	100dB
FREQUENCY RESPONSE	
Unity Gain Bandwidth, Small Signal	7 MHz
Gain-bandwidth Product, f = 1 kHz, G = 100	20 MHz, min
Full Power Bandwidth, G = 100	135 kHz
Slew Rate, G = 100	150 V/μs
Settling Time, 0.1%, G = 100	12 μs
INPUT OFFSET VOLTAGE	
Initial @ 25°C, max	3 mV
Drift vs Temp, max	25 μV/°C
Drift vs Supply Voltage	20 μV/V
Drift vs Time	50 μV/mo
INPUT BIAS CURRENT	
Initial @ 25°C, max	-20 pA
Drift vs Temp	doubles every 10°C
Drift vs Supply Voltage	0.2 pA/V
INPUT OFFSET CURRENT	
Initial @ 25°C	±20 pA
Drift vs Temp	doubles every 10°C
Drift vs Supply Voltage	0.2 pA/V
INPUT IMPEDANCE	
Differential	10^{11} Ω || 10 pF
Common Mode	10^{11} Ω
INPUT NOISE	
Voltage 0.01 Hz to 10 Hz p-p	5 μV
10 Hz to 1 kHz rms	1.7 μV
Current 0.01 Hz to 10 Hz p-p	0.3 pA
INPUT VOLTAGE RANGE	
Max Safe Differential Voltage(1)	(+V_{cc} + | -V_{cc} |)
Max Safe Common Mode Voltage	+V_{cc} to -V_{cc}
Common Mode Voltage, Linear Operation	±(| V_{cc} | -10)V
Common Mode Rejection	110dB
TEMPERATURE RANGE (Case)	
Specification:	0°C to 70°C
Operating	-55°C to +125°C
Storage	-55°C to +150°C

(1) The inputs may be damaged by pulses at pins 5 or 6 with dV/dt ≥ 1 V/ns. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins. No external protection is needed for slower voltage changes.

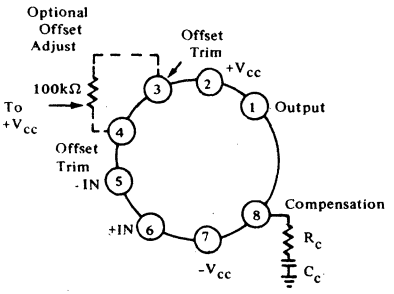
MECHANICAL



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

(TOP VIEW)



Connector: 0803MC
Heatsinks: 0803HS, 0804HS, or 0805HS

Compensation		
Gain	C_c	R_c
1	10 nF	200Ω
10	500 pF	2kΩ
100	50 pF	20kΩ
1000	not required	

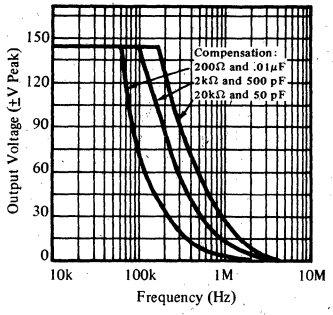
For intermediate values of gain, R and C values may be interpolated.

The case is electrically isolated. It is recommended that the case be grounded during use.

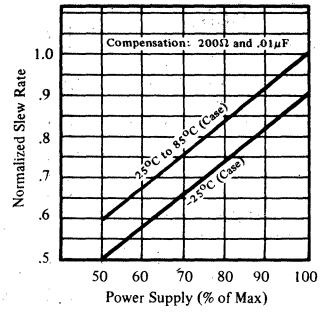
TYPICAL PERFORMANCE CURVES

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

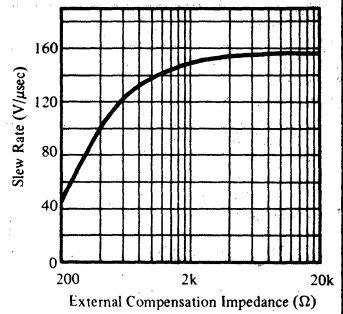
OUTPUT VOLTAGE vs FREQUENCY



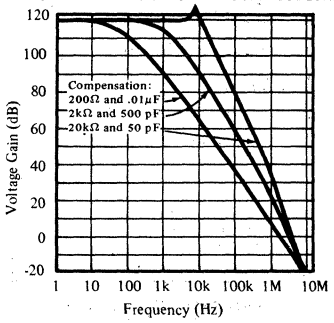
SLEW RATE vs SUPPLY VOLTAGE @ FULL LOAD



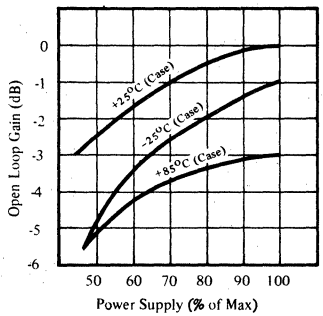
SLEW RATE vs COMPENSATION



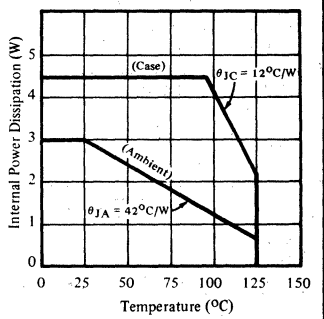
OPEN LOOP FREQUENCY RESPONSE FULL LOAD



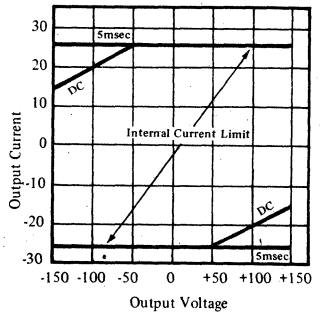
OPEN LOOP GAIN vs SUPPLY VOLTAGE @ MAX LOAD



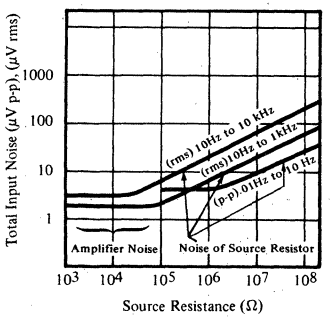
POWER DISSIPATION



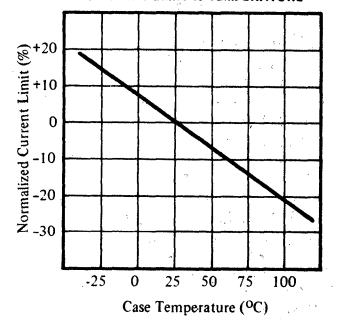
SAFE OPERATING AREA (Secondary Breakdown)



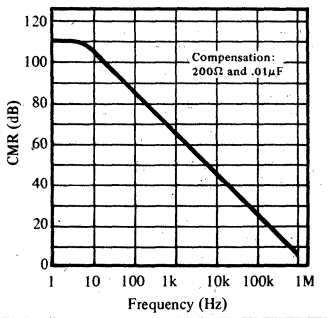
NOISE vs SOURCE RESISTANCE



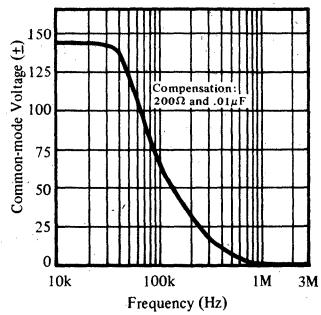
CURRENT LIMIT vs TEMPERATURE



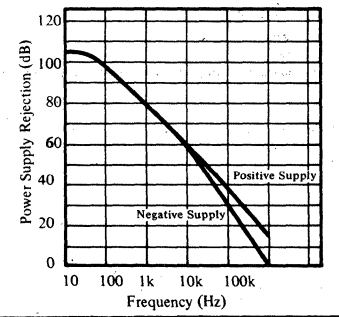
COMMON-MODE REJECTION



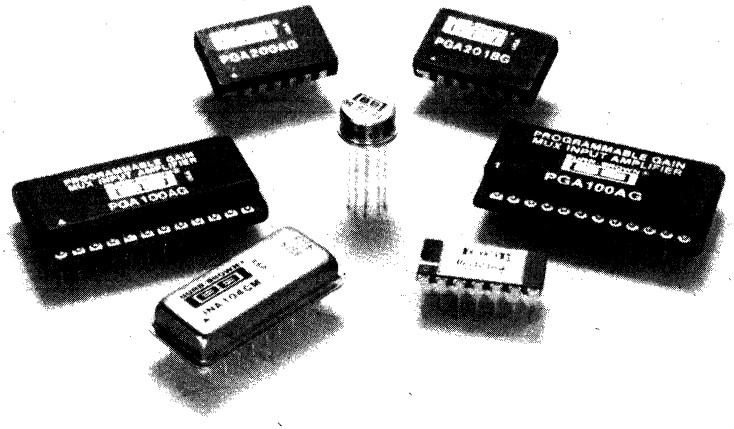
MAXIMUM COMMON-MODE VOLTAGE vs FREQUENCY



POWER SUPPLY REJECTION



INSTRUMENTATION AMPLIFIERS



WHAT IS AN INSTRUMENTATION AMPLIFIER?

An instrumentation amplifier is a closed-loop, differential input gain block. It is a committed circuit with the primary function of accurately amplifying the voltage applied to its inputs.

Ideally, the instrumentation amplifier responds only to the difference between the two input signals and exhibits extremely-high impedances between the two input terminals, and from each terminal to ground. The output voltage is developed single-ended with respect to ground and is equal to the product of amplifier gain and the difference of the two input voltages (see Figure 1).

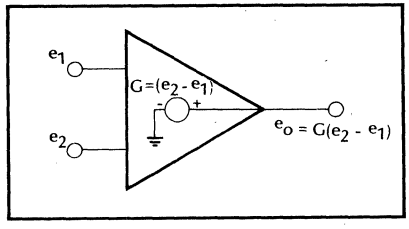


FIGURE 1. Idealized Model of an Instrumentation Amplifier.

The amplifier gain G is normally set by the user with a single external resistor. The properties of this model may be summarized as infinite input impedance, zero output impedance, the output voltage proportional to only the difference voltage ($e_2 - e_1$), a precisely known gain constant (implying no nonlinearity), and unlimited bandwidth. This amplifier would completely reject signal components common to both inputs (common-mode rejection) and would exhibit no DC offset voltage or drift.

CHARACTERISTICS OF INSTRUMENTATION AMPLIFIERS

It is desirable to achieve, as close as possible, the characteristics of the ideal instrumentation amplifier. The following paragraphs are a discussion of the, other-than-ideal, characteristics of the instrumentation amplifiers.

Input Impedance - A simple model of realistic instrumentation amplifier is shown in Figure 2. The impedance Z_{id} represents the differential input impedance. The common-mode input impedance Z_{icm} is represented as two

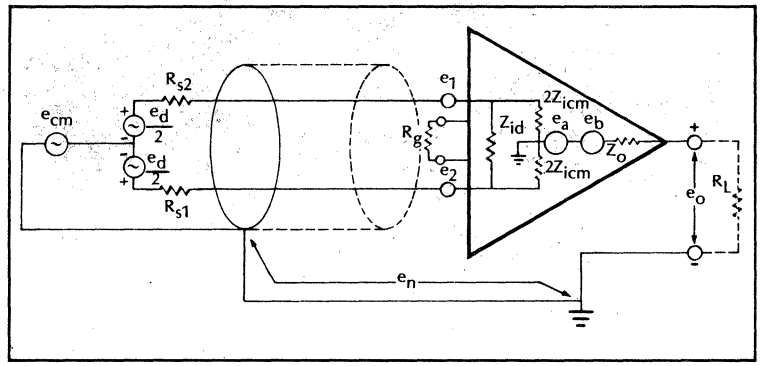


FIGURE 2. Simple Model of an Instrumentation Amplifier Shown in a Typical Application Configuration.

equal components, $2Z_{icm}$, *from each input to ground. These finite resistances contribute an effective gain error due to loading of the source resistance. The instrumentation amplifier provides a load on the source of* $Z_i = Z_{id} \parallel Z_{icm}$. If source impedance is $R_S = R_{s1} + R_{s2}$, the gain error caused by this loading is:

$$\text{Gain Error} = 1 - \frac{Z_i}{Z_i + R_s} = \frac{R_s}{Z_i + R_s} \cong \frac{R_s}{Z_i} \text{ if } Z_i \gg R_s$$

If R_S is 10kΩ and Z_i is 10MΩ,

$$\text{Gain Error} \cong \frac{10 \times 10^3}{10 \times 10^6} = 0.1\%$$

The DC common-mode input impedance Z_{icm} will be independent of gain. The DC differential input impedance Z_{id} may vary as a function of gain. Specifications give the worst-case value. The nonzero output impedance of the amplifier will also create a gain error, the value of which depends on the load resistance.

Nonlinearity - The linearity of gain is possibly of more importance than the gain accuracy, since the value of the gain can be adjusted to compensate for simple gain errors. The nonlinearity is specified to be the peak deviation from a "best fit" straightline, expressed as a percent of peak-to-peak full scale output.

Common-mode Rejection - As illustrated in Figure 2, the output voltage has two components. One component is proportional to the differential input voltage $e_d = (e_2 - e_1)$. The second component is proportional to the common-mode input voltage. The common-mode voltage which appears at the amplifier's input terminals is defined as $E_{cm} = e_2 + e_1/2$. This may consist of some common-mode voltage in the source itself, e_{cm}, (such as bridge excitation) plus any noise voltage, e_n, between the source common and the amplifier common. As shown in Figure 2, the constant G represents the

differential amplifier gain factor (fixed by the external gain-setting resistor). The constant (G/CMRR) represents the commo-mode signal gain of the amplifier. The CMRR (common-mode rejection ratio) is the ratio of differential gain to common-mode gain. Thus CMRR is proportional to the differential gain and CMRR increases as the differential (gain G) increased. Hence, CMRR is usually specified for the maximum and the minimum values of gain of the amplifier. The common-mode rejection may be expressed in dB as - CMRR (dB) = 20 $\log_{10}$ CMRR.

For an ideal instrumentation amplifier the output voltage component due to common-mode voltage should be zero. For a realistic instrumentation amplifier, the CMRR though very high, is still not infinite and so will cause an error voltage of E_{cm}/CMRR x G to appear at the output.

Source Impedance Unbalance - If the source impedances are unbalanced the source voltages ($e_{cm} + e_n$) are divided unequally upon the common-mode impedances and a differential signal is developed at the amplifier's input. This error signal cannot be separated from the desired signal. In the circuit in Figure 2 if $R_{s2} = 0$, $R_{s1} = 1k\Omega$, $e_{cm} + e_n = 10V$, and $Z_{cm} = 100M\Omega$, then the effect of unbalance is to generate a voltage.

$$e_2 - e_1 = 10V - 10V\frac{10^8}{10^8 + 10^3} = 10V\frac{10^3}{10^8 + 10^3} \cong \frac{10V}{10^5} = 0.1mV$$

If e_d full scale is 10mV then this error is:

$$\text{Error} = \frac{0.1mV}{10mV} = 1\% \text{ of full scale.}$$

Offset Voltage and Drift - Most instrumentation amplifiers are two stage devices - they have a variable gain input stage and a fixed gain output stage. If V_i and V_o are the offset voltages of the input and output stages respectively, then the amplifiers total offset voltage referred to the input (RTI) = $V_i + V_o/G$ where G is the amplifier's gain. [Note that E_{os} (RTI) x G.]

The initial offset voltage is usually adjustable to zero and therefore, the voltage drift is the more significant term since it cannot be nulled. The offset voltage drift also has two components - one due to the input stage of the amplifier and the other due to the output stage. When the amplifier is operated at high gain, the drift of the input stage predominates. At low values of gain, the drift of the output stage will be the major component of drift. When the total output drift is referred to the input, the effective input voltage drift is largest for low values of gain. Output voltage drift will always be lowest at low gains. If $\Delta V_i/\Delta T = 2\mu V/°C$ and $\Delta V_o/\Delta T = 500\mu V/°C$ and the amplifier in a gain of 1000V/V is nulled at 25°C, then at 65°C the offset voltage will be:

$$E_{os}\,(RTI)_{65^o} = 40^oC\,[2\mu V/^oC + (500\mu V/^oC/1000V/V)]$$
$$= 40^oC\,(2.5\mu V/^oC) = 100\mu V = 0.1mV$$

If the full scale input is 10mV then the error due to voltage drift is:

$$\text{Error} = 0.1mV/10mV = 1\% \text{ of full scale.}$$

Input Bias and Offset Currents - The input bias currents are the currents that flow out of (or into) either of the two inputs of the amplifier. They are the base currents for bipolar input stages and the JFET leakage currents for FET input stage. Offset currents are the difference of the two bias currents.

The bias currents flowing into the source resistances will generate offset voltages of $E_{os2} = 1_{B2} \times R_{s2}$ and $E_{os1} = 1_{B1} \times R_{s1}$. If $R_{s1} = R_{s2} = R_s/2$ the offset voltage at the input is $E_{os2} - E_{os1} = I_{os} \times R_x/2$. This input referred offset error may be compared directly with the input voltage to compute percent error. (Note that the source must be returned to power supply common or R_s will be infinite and the amplifier will saturate.)

APPLICATIONS OF INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are generally used in applications where extracting and accurately amplifying low level differential signals riding on high common-mode voltages (±10V) is very important. Such applications require high input impedance, high CMRR, low input noise, and excellent DC levels stability (low offset voltage drift).

Instrumentation amplifiers are used as transducer amplifiers for various types of transducers such as strain gage bridges, load cells, thermistor networks, thermocouples, current shunts, biological probes, weather gauges and so forth. Other applications include recorder preamplifiers, multiplexer buffers, servo error amplifiers, current sensors, signal conditioners in process control and data acquisition systems, and in general measurements of small differential signals riding on common-mode voltages.

The small size, low cost, and high performance of these amplifiers offer an attractive approach for data acquisition applications, that is, assigning a fixed-gain amplifier to each transducer and locating the amplifier physically near the transducer. This approach largely eliminates common-mode noise pickup problems since a high level signal (rather than a low level transducer signal) is then retransmitted to the data gathering station. The result is a higher signal/noise ratio at the output. Using one amplifier per point may well be more economical, as well as offering better peformance and flexibility, than the approach of using low level multiplexers.

SELECTION GUIDE

INSTRUMENTATION AMPLIFIERS												
						Input Parameters						
Description	Model	Gain Range	Gain Accuracy G = 100, 25°C max	Gain Drift G = 100 ppm/°C	Non-Linearity G=100 max %	CMR, DC to 60Hz, G = 10 1kΩ Unbal...min	Offset Voltage vs Temp max (μV/°C)	Dynamic Response G = 100 ±3dB BW (kHz)	Temp Range [1]	Package	Page
Very-High Accuracy	INA104HP	1-1000[2]	0.15	22	±0.007	96dB	±(2 ± 20/G)	25	Com	DIP	2-15
	INA104JP	1-1000[2]	0.15	22	±0.003	96dB	±(0.25 ± 10/G)	25	Com	DIP	2-15
	INA104KP	1-1000[2]	0.15	22	±0.003	96dB	±(0.75 ± 10/G)	25	Com	DIP	2-15
	INA104AM	1-1000[2]	0.15	22[5]	±0.007	96dB	±(2 ± 20/G)	25	Ind	DIP	2-15
	INA104BM	1-1000[2]	0.15	22[5]	±0.003	96dB	±(0.75 ± 10/G)	25	Ind	DIP	2-15
	INA104CM	1-1000[2]	0.15	22[5]	±0.003	96dB	±(0.25 ± 10/G)	25	Ind	DIP	2-15
	INA104SM	1-1000[2]	0.15	22[5]	±0.003	96dB	±(0.75 ± 10/G)	25	MIL	DIP	2-15
	INA101AM	1-1000[2]	0.03	22[3]	±0.007	96dB	±(2 + 20/G)	25	Ind	TO-100	2-7
	INA101CM	1-1000[2]	0.03	22[3]	±0.004	96dB	±(0.25 + 10/G)	25	Ind	TO-100	2-7
	INA101SM	1-1000[2]	0.03	22[3]	±0.004	96dB	±(0.25 + 10/G)	25	MIL	TO-100	2-7
	INA101AG	1-1000[2]	0.03	22[5]	±0.007	96dB	±(2 + 20/G)	25	Ind	DIP	2-7
	INA101CG	1-1000[2]	0.03	22[5]	±0.003	96dB	±(0.25 + 10/G)	25	Ind	DIP	2-7
	INA101SG	1-1000[2]	0.03	22[5]	±0.003	96dB	±(0.25 + 10/G)	25	MIL	DIP	2-7
	3630AM	1-1000[2]	0.1	125[3]	±0.007	96dB	±(2 + 20/G)	25	Ind	DIP	2-74
	3630BM	1-1000[2]	0.05	125[3]	±0.003	96dB	±(0.75 + 10/G)	25	Ind	DIP	2-74
	3630CM	1-1000[2]	0.05	125[3]	±0.003	96dB	±(0.25 + 10/G)	25	Ind	DIP	2-74
	3630SM	1-1000[2]	0.05	125	±0.003	96dB	±(0.75 + 10/G)	25	Ind	DIP	2-74
General Purpose	3626AP	5-1000[2]	0.5	35[3]	±0.05	74dB	±(6 + 10/G)	14	Ind	DIP	2-60
	3626BP	5-1000[2]	0.5	35[3]	±0.04	80dB	±(3 + 5/G)	14	Ind	DIP	2-60
	3626CP	5-1000[2]	0.5	35[3]	±0.04	80dB	±(1 + 5/G)	14	Ind	DIP	2-60
	3629AM	5-1000[2]	0.1	45[3]	±0.007	106dB[4]	±(3 + 10/G)	30	Ind	DIP	2-68
	3629AP	5-1000[2]	0.1	45[3]	±0.007	106dB[4]	±(3 + 10/G)	30	Ind	DIP	2-68
	3629BM	5-1000[2]	0.1	45[3]	±0.004	106dB[4]	±(1.5 + 7.5/G)	30	Ind	DIP	2-68
	3629BP	5-1000[2]	0.1	45[3]	±0.004	106dB[4]	±(1.5 + 7.5/G)	30	Ind	DIP	2-68
	3629CM	5-1000[2]	0.1	45[3]	±0.004	106dB[4]	±(0.75 + 5/G)	30	Ind	DIP	2-68
	3629CP	5-1000[2]	0.1	45[3]	±0.004	106dB[4]	±(0.75 + 5/G)	30	Ind	DIP	2-68
	3629SM	5-1000[2]	0.1	45[3]	±0.004	106dB[4]	±(1.5 + 7.5/G)	30	Ind	DIP	2-68
Buffer, Unity-Gain Differential	3627AM	1V/V, fixed	0.01	5	±0.001[5]	90dB	30	800[5]	Ind	TO-99	2-64
	3627BM	1V/V, fixed	0.01	5	±0.001[5]	100dB	20	800[5]	Ind	TO-99	2-64
PROGRAMMABLE GAIN AMPLIFIERS											
Noninverting Multiplexed Input	PGA100AG	Gain set with 4-bit word 1, 2, 4, 8,...128	0.05	10	±0.01	NA	6[6]	5MHz	Ind	DIP	2-26
	PGA100BG		0.02	10	±0.005	NA	6[6]	5MHz	Ind	DIP	2-26
Instrumentation Amplifier Input	PGA200AG	Gain set with 2-bit word 1, 10, 100, 1000	0.05	20	±0.007	96dB	2(G = 100)	30	Ind	DIP	2-34
	PGA200BG		0.02	10	±0.003	96dB	0.4(G = 100	30	Ind	DIP	2-34
Differential Input	3606AG	Gain set with 3-bit word 1, 2, 4 8...1024	0.05	10	0.004	90dB, G = 1	±(3 + 50/G)	40	Ind	DIP	2-52
	3606AM		0.05	10	0.004	90dB, G = 1	±(3 + 50/G)	40	Ind	DIP	2-52
	3606BG		0.02	10	0.004	90dB, G = 1	±(1 + 20/G)	40	Ind	DIP	2-52
	3606BM		0.02	10	0.004	90dB, G = 1	±(1 + 20/G)	40	Ind	DIP	2-52

PRECISION TWO-WIRE TRANSMITTER												
	Span			Input Parameters			Output Parameters					
Model	Untrimmed Error max	Non-Linearity max	Temp Drift ppm%/°C	Offset Voltage max	Offset Voltage vs Temp max μV/°C	CMR DC, min	Current Range mA	Offset Current Error μA, max	FS Output Current Error μA, max	Temp Range [1]	Package	Page
XTR100AM	−3%	0.01%	±100	±50μV	±1	90dB	4-20	±4	±20	Ind	DIP	2-40
XTR100AP	−3%	0.01%	±100	±50μV	±1	90dB	4-20	±4	±20	Ind	DIP	2-40
XTR100BM	−3%	0.01%	±100	±25μV	±0.5	90dB	4-20	±4	±20	Ind	DIP	2-40
XTR100BP	−3%	0.01%	±100	±25μV	±0.5	90dB	4-20	±4	±20	Ind	DIP	2-40

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (2) Set with external resistor. (3) With zero TC external resistor. (4) DC only. (5) Unity-gain. (6) Typical.

GLOSSARY OF TERMS & DEFINITIONS
Instrumentation Amplifiers

COMMON-MODE INPUT IMPEDANCE
The effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground, terminal.

COMMON-MODE REJECTION (CMR)
When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$\text{CMR (in dB)} = 20 \log_{10} \text{CMV/Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the differential voltage gain of an amplifier to its common-mode voltage gain.

COMMON-MODE VOLTAGE (CMV)
That portion of an input signal which is common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$\text{CMV} = e_1 + e_2/2$$

FEEDBACK
The return of a portion of the output signal from a device to the input of the device.

FULL POWER FREQUENCY RESPONSE
The maximum sinewave frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN
The ratio of the output signal to the associated input signal of a device.

GAIN ERROR
The difference between the actual gain of an amplifier and the one predicted by the ideal gain expression.

INPUT BIAS CURRENT
The DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT DRIFT
The rate of change of input bias current with temperature or time.

INPUT GUARDING
The use of an input shield that is sometimes driven to follow the voltage level of the input signal and, thereby, remove leakage and loss-inducing voltage differences between the input signal path and surrounding stray conduction paths.

INPUT OFFSET CURRENT
The difference of the two input bias currents in a differential amplifier.

INPUT OFFSET VOLTAGE
The DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT PROTECTION
A means of protecting an input of a device from damage due to the application of excessive input voltage.

INSTRUMENTATION AMPLIFIER
A closed-loop differential input gain block exhibiting high input impedance and high common-mode rejection. Its primary function is to accurately amplify the voltage applied to its inputs.

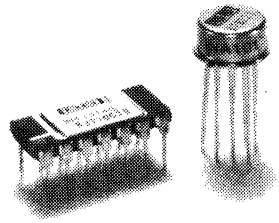
NONLINEARITY
The peak deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

OVERLOAD RECOVERY TIME
The time required for the output of an amplifier to return from saturation to linear operation, following the removal of an input overdrive signal.

SETTLING TIME
The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE
The maximum rate of change of an output voltage when supplying the rated output.

BURR-BROWN®



INA101

Very-High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- ULTRA-LOW VOLTAGE DRIFT - 0.25μV/°C
- LOW OFFSET VOLTAGE - 25μV
- LOW NONLINEARITY - 0.002%
- LOW NOISE - 13nV/√Hz at f_0 = 1kHz
- HIGH CMR - 106dB at 60Hz
- HIGH INPUT IMPEDANCE - $10^{10}\Omega$
- LOW COST

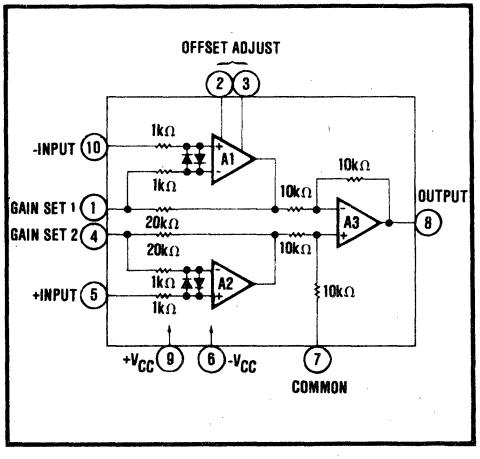
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS
- MEDICAL INSTRUMENTATION

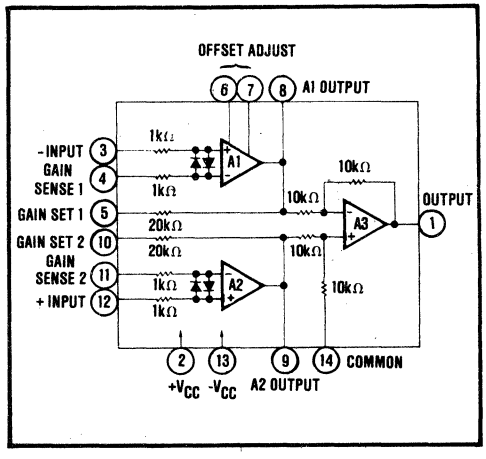
DESCRIPTION

The INA101 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired. All circuits, including the interconnected laser-trimmed thin-film resistors, are integrated on a single monolithic substrate.

A multiamplifier design is used to provide the highest performance and maximum versatility with monolithic construction for low cost. The input stage uses Burr-Brown's ultra-low drift, low noise technology to provide exceptional input characteristics.



M Package



G Package

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

MODEL	INA101AM/AG			INA101SM/SG			INA101CM/CG			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN										
Range of Gain	1		1000	*		*	*		*	V/V
Gain Equation		G = 1 + (40k/R_G)			*			*		V/V
Error From Equation, DC[1][2]		±(0.04±0.00016G - 0.02/G)	±(0.1±0.003G - 0.05/G)		*	*		*	*	% of FS
Gain Temp. Coefficients[3]										
G = 1		2	5		*	*		2	5	ppm/°C
G = 10		20	100		*	*		10	50	ppm/°C
G = 100		22	110		*	*		11	55	ppm/°C
G = 1000		22	110		*	*		11	55	ppm/°C
Nonlinearity, DC[2]		±(0.002 + 10^{-5}G)	±(0.005 + 2 × 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)	% of p-p FS
RATED OUTPUT										
Voltage	±10	±12.5		*	*		*	*		V
Current	±5	±10		*	*		*	*		mA
Output Impedance		0.2			*			*		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at +25°C[2]		±25 +200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	µV
vs. Temperature[2]			±2 ±20/G			±0.75 ±10/G			±0.25 ±10/G	µV/°C
vs. Supply		±(1 + 20/G)			*			*		µV/V
vs. Time		±(1 +20/G)			*			*		µV/mo
INPUT BIAS CURRENT										
Initial Bias Current[2] (each input)		±15	±30		±10	±30		±5	±20	nA
vs. Temperature		±0.2			*			*		nA/°C
vs. Supply		±0.1			*			*		nA/V
Initial Offset Current[2]		±15	±30		±10	±30		±5	±20	nA
vs. Temperature		±0.5			*			*		nA/°C
INPUT IMPEDANCE										
Differential		10^{10} || 3			*			*		Ω || pF
Common-mode		10^{10} || 3			*			*		Ω || pF
INPUT VOLTAGE RANGE										
Range, Linear Response	±10			*	*		*	*		V
CMR with 1kΩ Source Imbal.										
DC to 60Hz, G = 1[2]	80	90		*	*		*	*		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		dB
INPUT NOISE										
Input Voltage Noise										
f_B = 0.01Hz to 10Hz		0.8			*			*		µV, p-p
Density, G = 1000										
f_O = 10Hz		18			*			*		nV/√Hz
f_O = 100Hz		15			*			*		nV/√Hz
f_O = 1kHz		13			*			*		nV/√Hz
Input Current Noise										
f_B = 0.01Hz to 10Hz		50			*			*		pA, p-p
Density										
f_O = 10Hz		0.8			*			*		pA/√Hz
f_O = 100Hz		0.46			*			*		pA/√Hz
f_O = 1kHz		0.35			*			*		pA/√Hz
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness										
G = 1		300			*			*		kHz
G = 10		140			*			*		kHz
G = 100		25			*			*		kHz
G = 1000		2.5			*			*		kHz
Small Signal, ±1% Flatness										
G = 1		20			*			*		kHz
G = 10		10			*			*		kHz
G = 100		1			*			*		kHz
G = 1000		200			*			*		Hz
Full Power, G = 1 to 100		6.4			*			*		kHz
Slew Rate, G = 1 to 100[2]	0.2	0.4		*	*		*	*		V/µsec
Settling Time (0.1%)										
G = 1		30	40		*	*		*	*	µsec
G = 100		40	55		*	*		*	*	µsec
G = 1000		350	470		*	*		*	*	µsec
Settling Time (0.01%										
G = 1		30	45		*	*		*	*	µsec
G = 100		50	70		*	*		*	*	µsec
G = 1000		500	650		*	*		*	*	µsec

ELECTRICAL (CONT)

MODEL	INA101AM/AG			INA101SM/SG			INA101CM/CG			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY										
Rated Voltage		±15			•			•		V
Voltage Range	±5		±20	•		•	•		•	V
Current, Quiescent [3]		±6.7	±8.5		•	•		•	•	mA
TEMPERATURE RANGE										
Specification	-25		+85	-55		+125	•		•	°C
Operation	-55		+125	•		•	•		•	°C
Storage	-65		+150	•		•	•		•	°C

*Specifications same as for INA101AM/AG.

NOTES:
1. Typically the tolerance of R_a will be the major source of gain error.
2. Specifically tested for /883.
3. Not including the TCR of R_a.
4. Adjustable to zero at any one gain.

ABSOLUTE MAXIMUM RATINGS

Supply	±20V
Internal Power Dissipation	600mW
Input Voltage Range	±Vcc
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration	Continuous to ground

ORDERING INFORMATION

INA101 C G

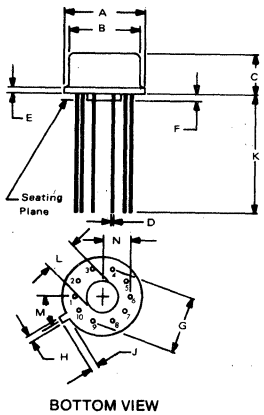
Basic Model Number
Performance Grade Code
S: -55°C to +125°C
A, C: -25°C to +85°C
Package Code
M: TO-100
G: 14-Pin Hermetic DIP

TO-100 (M Suffix)	Hermetic DIP (G Suffix)
INA101AM	INA101AG
INA101CM	INA101CG
INA101SM	INA101SG

MECHANICAL

M Package

TO-100



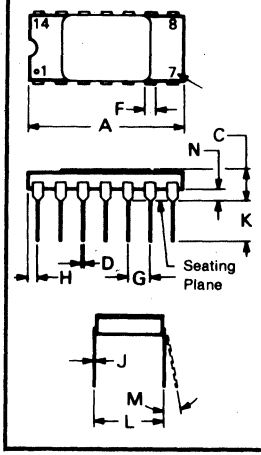
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

G Package

Hermetic DIP

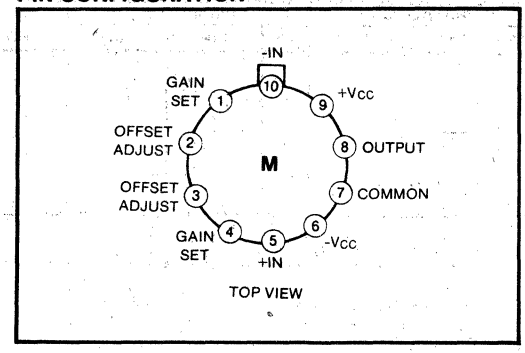


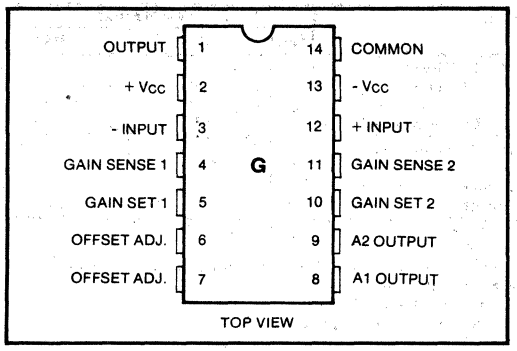
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

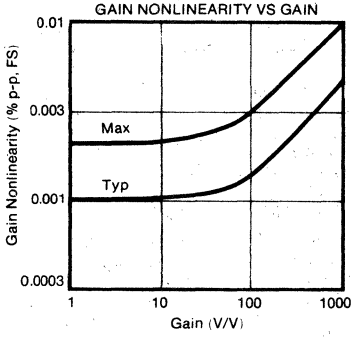
PIN CONFIGURATION

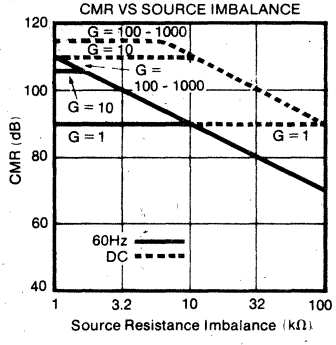


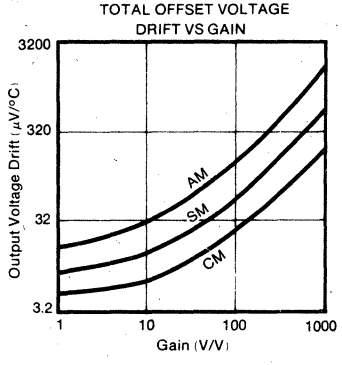


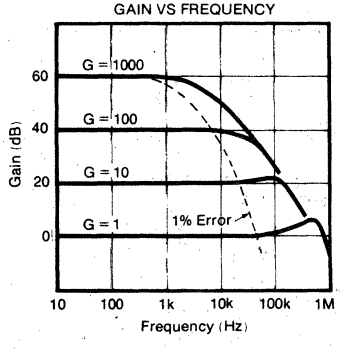
TYPICAL PERFORMANCE CURVES

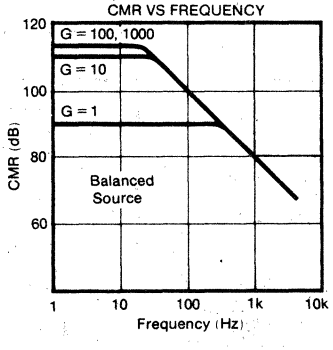
At +25°C and in circuit of Figure 2 unless otherwise noted.

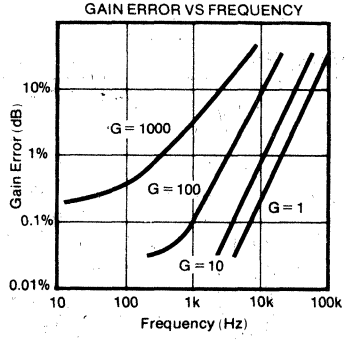


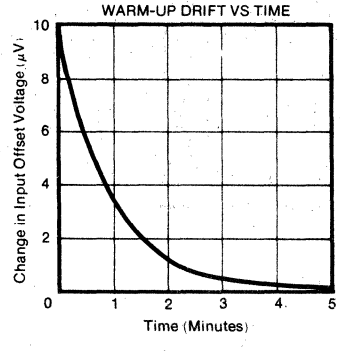


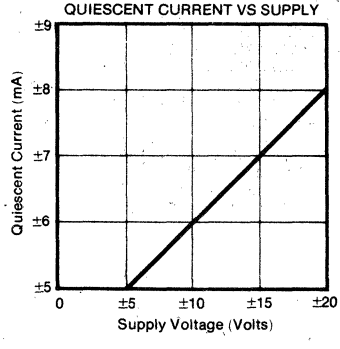


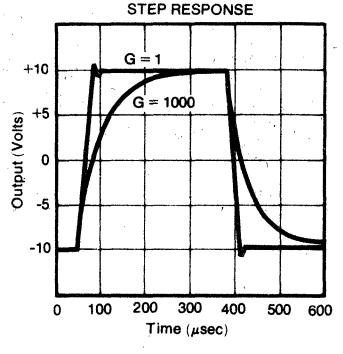




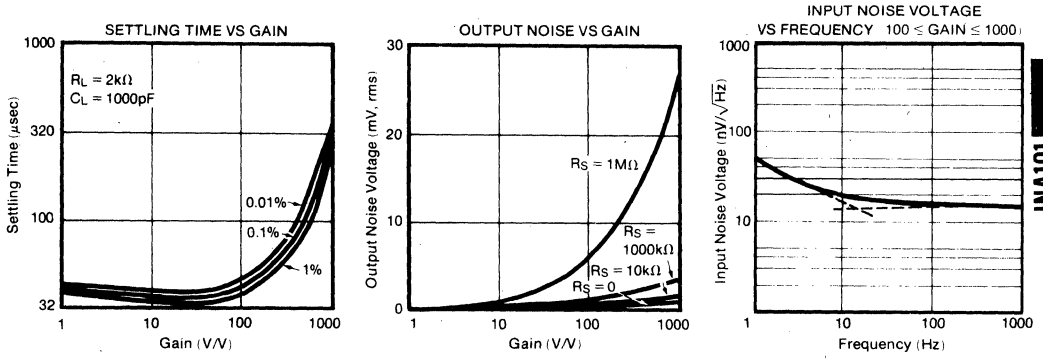








TYPICAL PERFORMANCE CURVES (CONT)



DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems.

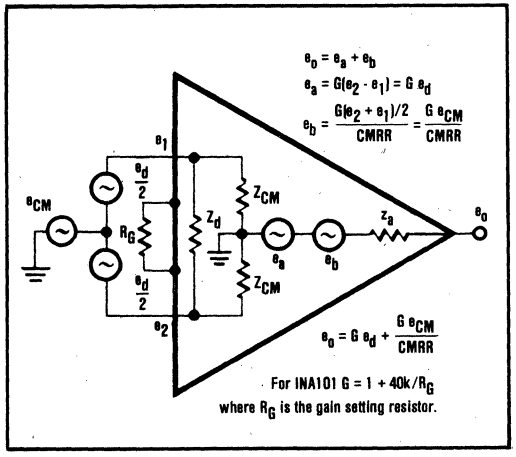


FIGURE 1. Model of an Instrumentation Amplifier.

THE INA101

Simplified schematics of the INA101 are shown on the first page. It is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature is low due to the monolithic design and improved even further by the state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA101 is operated over wide temperature ranges.

USING THE INA101

Figure 2 shows the simplest configuration of the INA101. The gain is set by the external resistor, R_G with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally between pins 1 and 4. At high gains where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

The optional offset null capability is shown in Figure 2. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately $0.31\mu V/^{\circ}C$ per $100\mu V$ of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offsetting can be accomplished in Figure 3 by applying a voltage to Common (pin 7) through a buffer amplifier. This limits the resistance in series with pin 7 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 106dB. Be certain to keep this resistance low.

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately $\pm 10V$ or nonlinear operation will result.

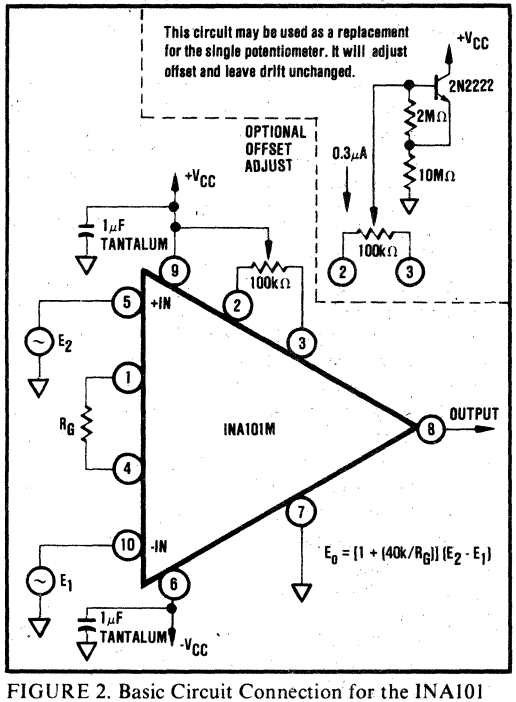


FIGURE 2. Basic Circuit Connection for the INA101 Including Optional Input Offset Null Potentiometer.

BASIC CIRCUIT CONNECTION

The basic circuit connection for the INA101 is shown in Figure 2. The output voltage is a function of the differential input voltage times the gain.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is frequently desirable to null the input component of offset (Figure 2) and occasionally that of the output (Figure 3). The quality of the potentiometer will affect the

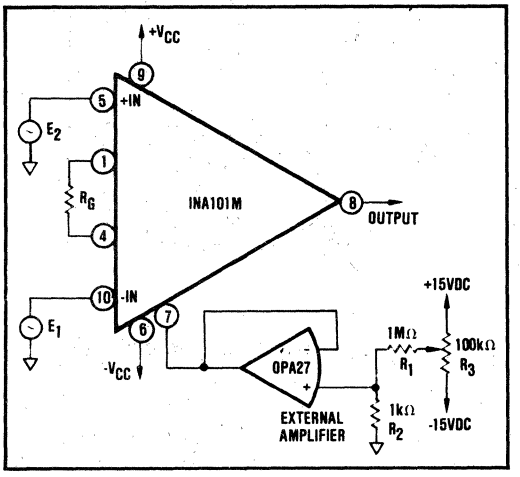


FIGURE 3. Optional Output Offset Nulling or Offsetting Using External Amplifier (Low Impedance to Pin 7).

results, therefore, choose one with good temperature and mechanical-resistance stability. The procedure is as follows:

1. Set $E_1 = E_2 = 0V$ (be sure a good ground return path exists to the input).
2. Set the gain to the desired value by choosing R_G.
3. Adjust to $100k\Omega$ potentiometer in Figure 2 until the output reads $0V \pm 1mV$ or desired setting. Note that the offset will change when the gain is changed. If the output component of offset is to be removed or if it is desired to establish an intentional offset, adjust the $100k\Omega$ potentiometer in Figure 3 until the output reads $0V \pm 1mV$ or desired setting. Note that the offset will not change with gain, but be sure to use a stable external amplifier with good DC characteristics. The range of adjustment is $\pm 15mV$ as shown. For larger ranges change the ratio of R_1 to R_2.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low level differential signals from bridges and transducers such as strain gages, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA101 accomplishes all of these with high precision.

Figures 4 through 9 show some typical applications circuits.

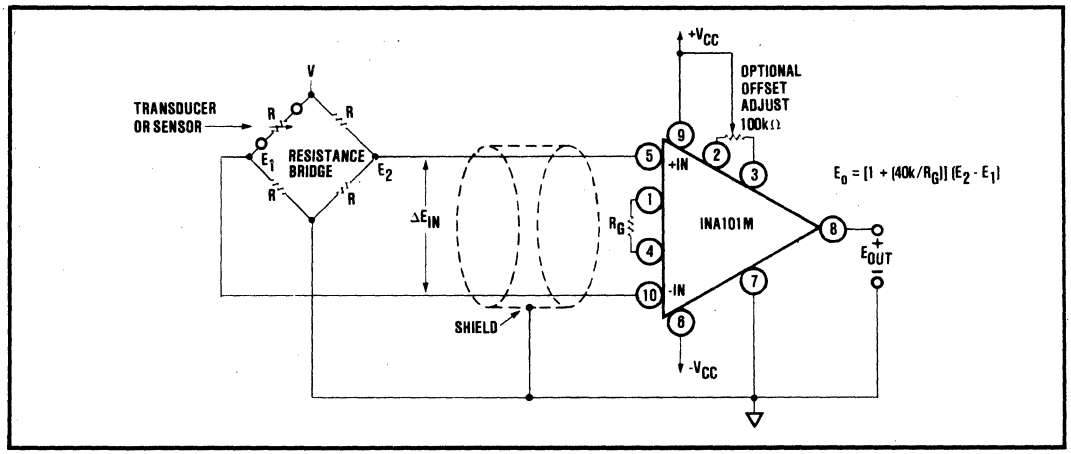


FIGURE 4. Amplification of a Differential Voltage from a Resistance Bridge.

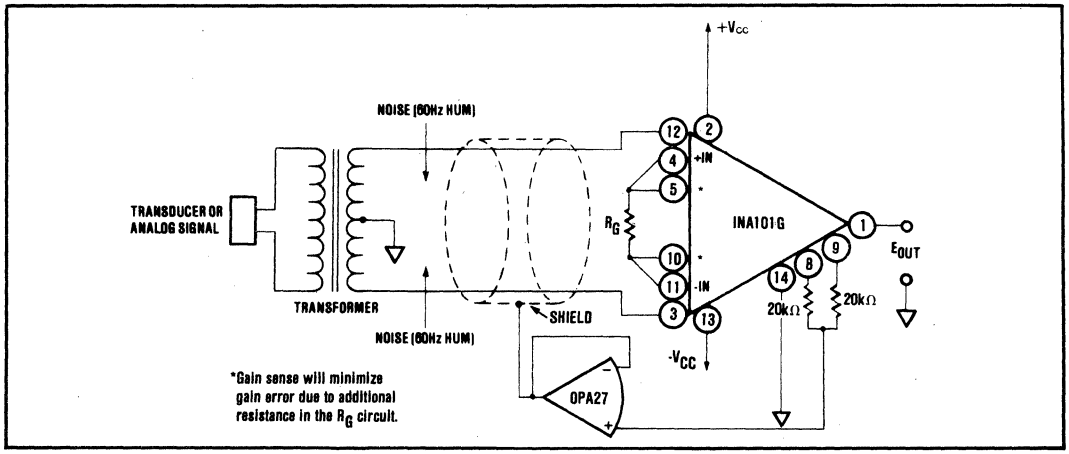


FIGURE 5. Amplification of a Transformer Coupled Analog Signal.

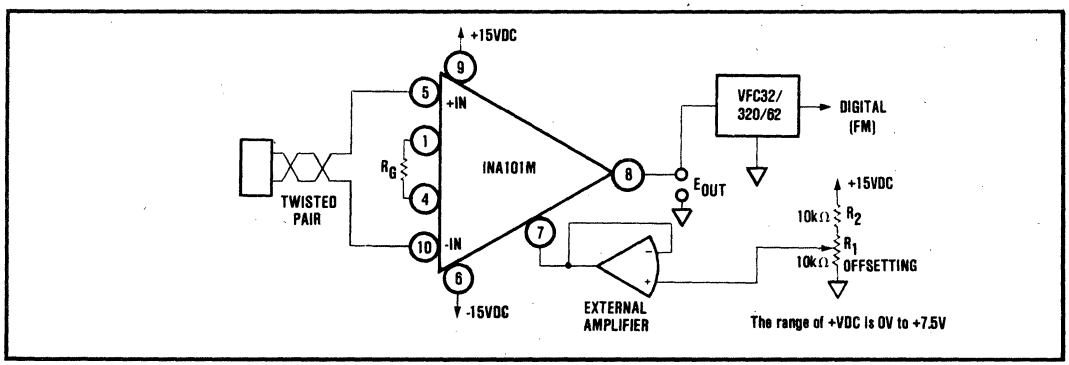


FIGURE 6. Output Offsetting Used to Introduce a DC Voltage for Use with a Voltage-to-Frequency Converter.

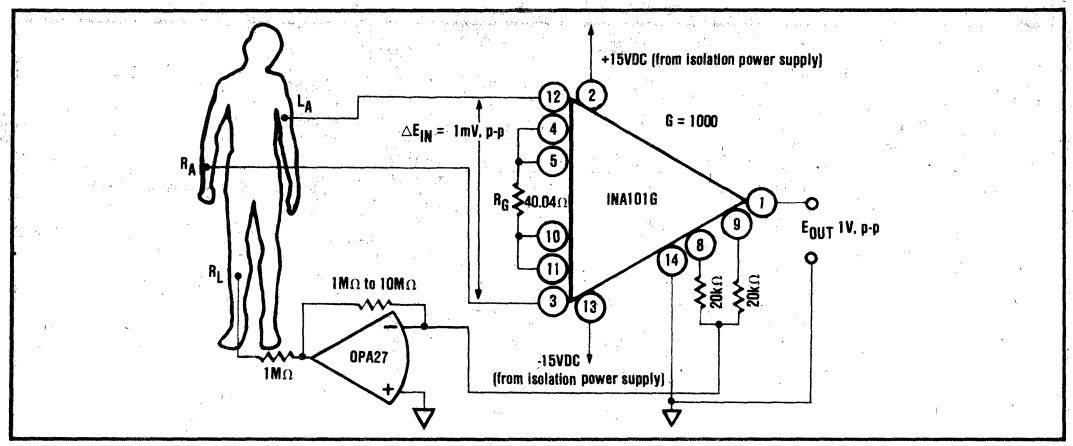


FIGURE 7. ECG Amplifier or Recorder Preamp for Biological Signals.

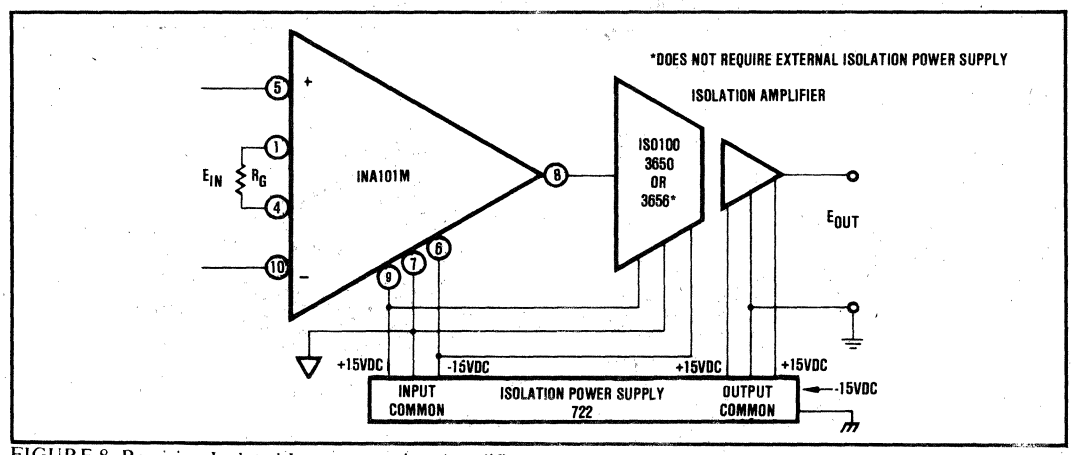


FIGURE 8. Precision Isolated Instrumentation Amplifier.

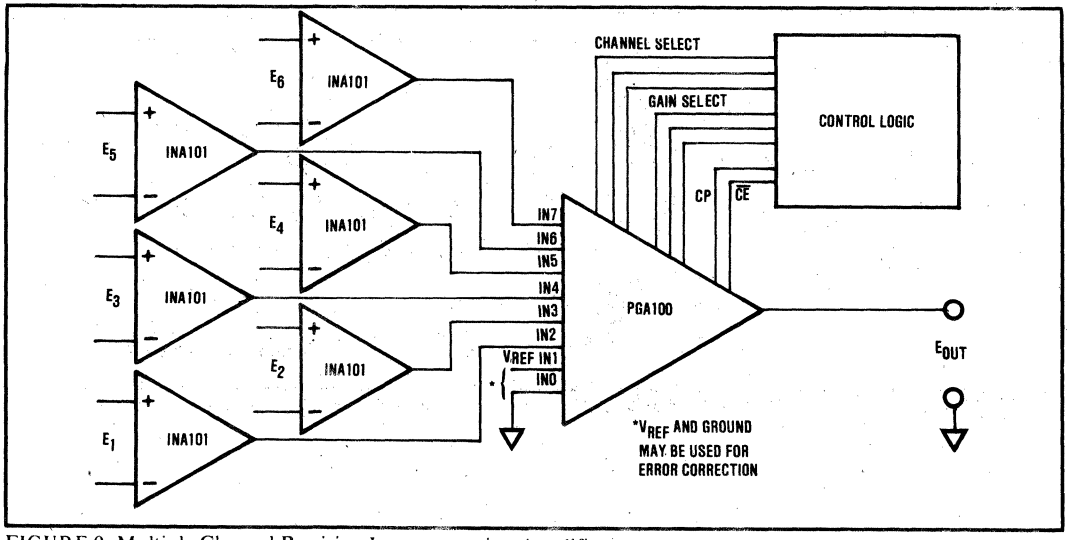


FIGURE 9. Multiple Channel Precision Instrumentation Amplifier.

BURR-BROWN®

INA104

Very-High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- VERSATILE FOUR-OP AMP DESIGN
- ULTRA-LOW VOLTAGE DRIFT - 0.25μV/°C, max
- LOW OFFSET VOLTAGE - 25μV, max
- LOW NONLINEARITY - 0.002%, max
- LOW NOISE - 13nV/$\sqrt{Hz}$ at f_0 = 1kHz
- HIGH CMR - 106dB at 60Hz, min
- HIGH INPUT IMPEDANCE - $10^{10}\Omega$
- LOW COST

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCER AMPLIFIER
- LOW LEVEL SIGNAL CONDITIONER
- MEDICAL INSTRUMENTATION

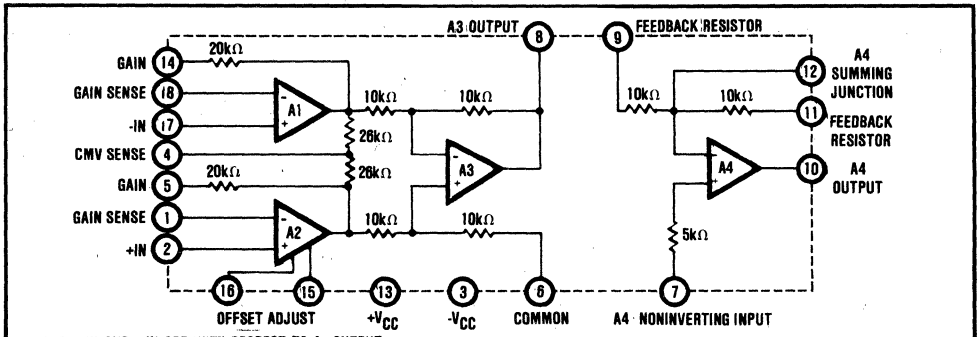
DESCRIPTION

The INA104 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired.

A multiamplifier, monolithic design, which uses Burr-Brown's ultra-low drift, low noise technology, provides the highest performance with maximum versatility at the lowest cost and this makes the INA104 ideal for even high volume applications.

Burr-Brown's compatible thin-film resistors and state-of-the-art wafer level laser-trimming techniques are used for minimizing offset voltage and temperature drift. This advanced technique also maximized common-mode rejection and gain accuracy.

The INA104 also contains a fourth operational amplifier, specified separately, which can conveniently be used for some important applications such as single capacitor active low-pass filtering, easy output level shifting, Common-mode voltage active guard drive, and increased gain (x 10,000 and greater).



NOTE: +IN AND −IN ARE WITH RESPECT TO A_3 OUTPUT.
IF A_4 IS USED INVERTING, +IN AND −IN ARE REVERSED.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 1 unless otherwise noted.

MODEL	INA104AM/HP MIN	INA104AM/HP TYP	INA104AM/HP MAX	INA104BM/SM/JP MIN	INA104BM/SM/JP TYP	INA104BM/SM/JP MAX	INA104CM/KP MIN	INA104CM/KP TYP	INA104CM/KP MAX	UNITS
INSTRUMENTATION AMPLIFIER										
GAIN										
Range of Gain	1		1000	*		*	*		*	V/V
Gain Equation		G = 1 + (40k/R_G)			*			*		V/V
Error From Equation, DC[1]		±(0.08 - 0.05/G)	±(0.15 - 0.1/G)		*	*		*	*	% of FS
Gain Temp. Coefficient[2]										
G = 1		2	5		*	*		*	*	ppm/°C
G = 10		20	100		*	*		10	50	ppm/°C
G = 100		22	110		*	*		11	55	ppm/°C
G = 1000		22	110		*	*		11	55	ppm/°C
Nonlinearity, DC		±(0.002 + 10^{-5}G)	±(0.005 + 2 x 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)	% of p-p FS
RATED OUTPUT										
Voltage	±10	+11.5, −12.5		*	*		*	*		V
Current	±5	+11.5, −12.5		*	*		*	*		mA
Output Impedance		0.2			*			*		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at +25°C[3]		±25 ±200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	µV
vs Temperature			±2 ±20/G			±0.75 ±10/G			±0.25 ±10/G	µV/°C
vs Supply		±(1 + 50/G)			*			*		µV/V
vs Time		±(1 + 20/G)			*			*		µV/mo
INPUT BIAS CURRENT										
Initial Bias Current (each input)		±15	±30		±10	*		±5	±20	nA
vs Temperature		±0.2			*			*		nA/°C
vs Supply		±0.1			*			*		nA/V
Initial Offset Current		±5	±30		±2	*		±2	±20	nA
vs Temperature		±0.5			*			*		nA/°C
INPUT IMPEDANCE										
Differential		10^{10} || 3			*			*		Ω || pF
Common-mode		10^{10} || 3			*			*		Ω || pF
INPUT VOLTAGE RANGE										
Range, Linear Response	±10			*			*			V
CMR with 1kΩ Source Imbal.										
DC to 60Hz, G = 1	80	90		*	*		*	*		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		dB
INPUT NOISE										
Input Voltage Noise										
f_B = 0.1Hz to 10Hz		0.8			*			*		µV, p-p
Density, G = 1000										
f_O = 10Hz		18			*			*		nV/√Hz
f_O = 100Hz		15			*			*		nV/√Hz
f_O = 1kHz		13			*			*		nV/√Hz
Input Current Noise										
f_B = 0.01Hz to 10Hz		50			*			*		pA, p-p
Density										
f_O = 10Hz		0.8			*			*		pA/√Hz
f_O = 100Hz		0.46			*			*		pA/√Hz
f_O = 1kHz		0.35			*			*		pA/√Hz
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness										
G = 1		300			*			*		kHz
G = 10		140			*			*		kHz
G = 100		25			*			*		kHz
G = 1000		2.5			*			*		kHz
Small Signal, ±1% Flatness										
G = 1		20			*			*		kHz
G = 10		10			*			*		kHz
G = 100		1			*			*		kHz
G = 1000		200			*			*		Hz
Full Power, G = 1 - 100		6.4			*			*		kHz
Slew Rate, G = 1 - 100	0.2	0.4		*	*		*	*		V/µsec
Settling Time (0.1%)										
G = 1		30	40		*	*		*	*	µsec
G = 100		40	55		*	*		*	*	µsec
G = 1000		350	470		*	*		*	*	µsec
Settling Time (0.01%)										
G = 1		30	45		*	*		*	*	µsec
G = 100		50	70		*	*		*	*	µsec
G = 1000		500	650		*	*		*	*	µsec

ELECTRICAL (CONT)

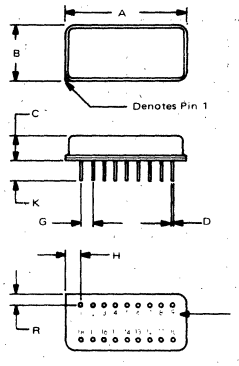
MODEL	INA104AM/HP MIN	INA104AM/HP TYP	INA104AM/HP MAX	INA104BM/SM/JP MIN	INA104BM/SM/JP TYP	INA104BM/SM/JP MAX	INA104CM/KP MIN	INA104CM/KP TYP	INA104CM/KP MAX	UNITS
OUTPUT AMPLIFIER, A_4										
OPEN-LOOP GAIN, $V_O = \pm 100$										
Rated Load $R_L \geq 2k\Omega$	100	115		•	•		•	•		dB
$R_L \geq 10k\Omega$	110	125		•	•		•	•		dB
RATED OUTPUT										
Voltage at $R_L = 2k\Omega$	10	+13, −14.5		•	•		•	•		V
$R_L = 10k\Omega$		+13, −14.5			•			•		V
Current	5	7.5		•	•		•	•		mA
Output Impedance		2			•			•		kΩ
Load Capacitance (unity-gain inverting)		2000			•			•		pF
Short Circuit Current		10			•			•		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			•			•		MHz
Full Power		9			•			•		kHz
Slew Rate	0.35	0.55		•	•		•	•		V/μsec
Settling Time (unity gain)										
0.1%		37			•			•		μsec
0.01%		40			•			•		μsec
INPUT OFFSET VOLTAGE										
Initial, $T_A = +25°C$		±1	±2		•	•		•	•	mV
vs Temperature		±5			•			•		μV/°C
INPUT BIAS CURRENT		+55	+150							nA
INPUT IMPEDANCE										
Differential		500			•			•		kΩ
Common-Mode		100			•			•		MΩ
RESISTORS, 10kΩ										
Accuracy		0.5	5		•			•		%
Drift		30	50		•	•		•	•	ppm/°C
Ratio Match		0.06	0.12		•	•		•	•	%
Drift		5			•			•		ppm/°C
INPUT VOLTAGE NOISE										
F_B = 0.1Hz to 10Hz		1.5			•			•		μV,p-p
Density										
f_O = 10Hz		35			•			•		$nV\sqrt{Hz}$
f_O = 100Hz		33			•			•		$nV\sqrt{Hz}$
f_O = 1kHz		32			•			•		$nV\sqrt{Hz}$
POWER SUPPLY, TOTAL										
Rated Voltage		±15			•			•		V
Voltage Range	±5		±20	•		•	•		•	V
Current, Quiescent		±8.1	±9.6		•	•		•	•	mA
TEMPERATURE RANGE										
Specification										
INA104HP/JP/KP	0		+70							°C
INA104AM/BM/CM	−25		+85							°C
INA104SM	−55		+125							°C
Operation										
INA104HP/JP/KP	−40		+85							°C
INA104AM/BM/CM/SM	−55		+85							°C
Storage										
INA104HP/JP/KP	−40		+85							°C
INA104AM/BM/CM/SM	−65		+150							°C
θ_{J-C}		115			•			•		0°C/W
θ_{J-A}		350			•			•		0°C/W

*Specifications same as for INA104HP.

NOTES:
1. Typically the tolerance of R_G will be the major source of gain error. 2. Not including the TCR of R_G. 3. Adjustable to zero at any one gain.

MECHANICAL

METAL HERMETIC DIP

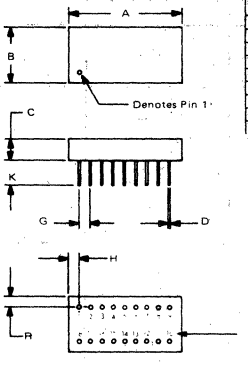


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.060	1.080	26.92	27.43
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

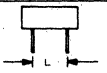
NOTE: Leads in true position within 0.01" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

PLASTIC DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.990	1.010	25.15	25.65
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92



NOTE: Leads in true position within 0.01" (.25mm) R at MMC at seating plane.

Pin numbers shown fo reference only. Numbers are not marked on package.

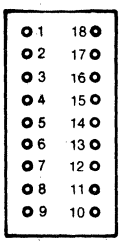
ABSOLUTE MAXIMUM RATINGS

Supply	±20V
Internal Power Dissipation	980mW
Input Voltage Range	±Vcc
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground

PIN DESIGNATIONS

1. GAIN SENSE
2. +IN
3. NEGATIVE SUPPLY
4. COMMON-MODE VOLTAGE SENSE
5. GAIN
6. COMMON
7. NONINVERTING INPUT TO A_4
8. OUTPUT
9. FEEDBACK RESISTOR
10. OUTPUT OF A_4
11. FEEDBACK RESISTOR
12. SUMMING JUNCTION OF A_4
13. POSITIVE SUPPLY
14. GAIN
15. OFFSET ADJUST
16. OFFSET ADJUST
17. -IN
18. GAIN SENSE

(TOP VIEW)



ORDERING INFORMATION

INA104 X X

Basic Model Number

Performance Grade Code
H, J, K: 0°C to +70°C
A, B, C: −25°C to +85°C
S: −55°C to +125°C

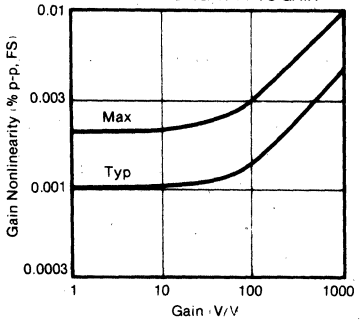
Package Code
P - Plastic DIP
M - Metal Hermetic DIP

Plastic DIP (Hybripak):	Metal DIP
INA104HP	INA104AM
INA104JP	INA104BM
INA104KP	INA104CM
	INA104SM

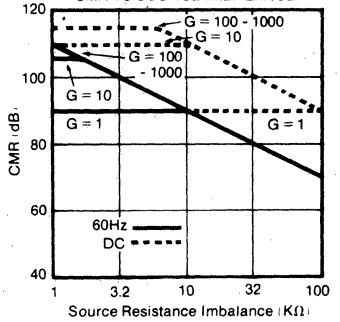
TYPICAL PERFORMANCE CURVES

At +25°C, ±Vcc = 15VDC, and in circuit of Figure 1 unless otherwise specified.

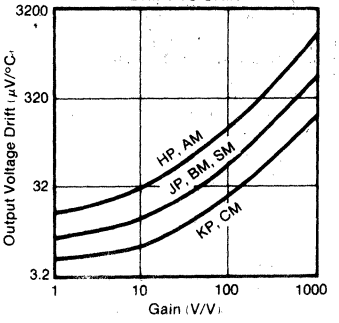
GAIN NONLINEARITY VS GAIN

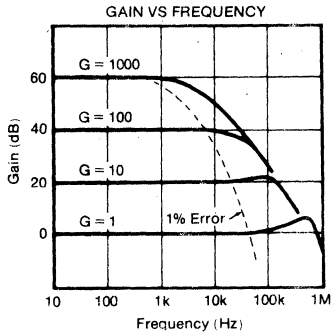


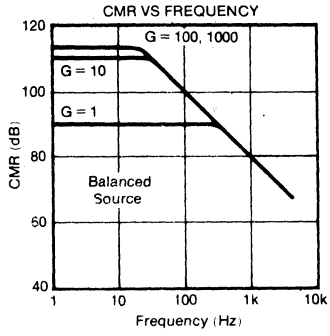
CMR VS SOURCE IMBALANCE

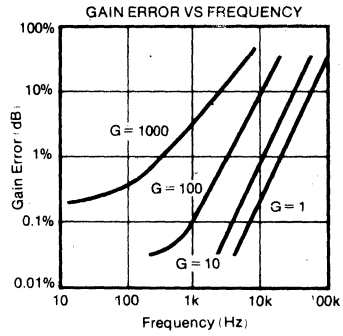


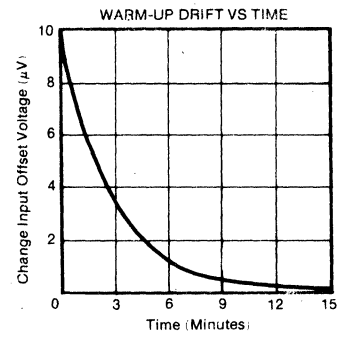
TOTAL OFFSET VOLTAGE DRIFT VS GAIN

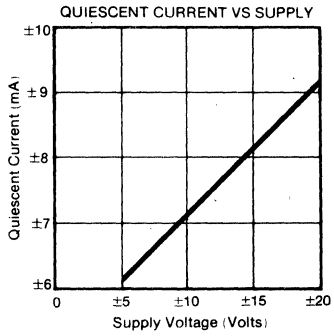


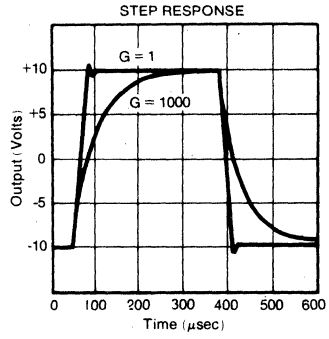


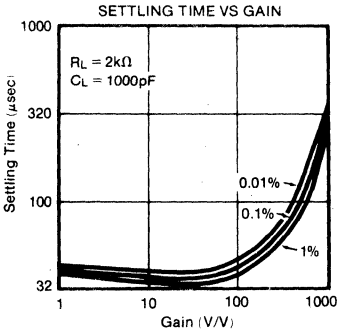


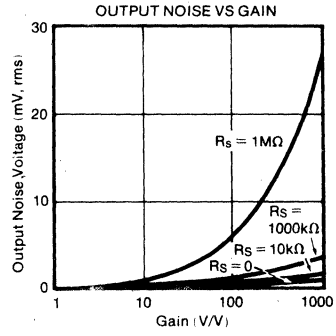


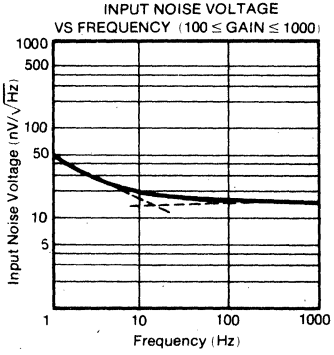












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are closed-loop gain blocks whose committed circuitry accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While operational amplifiers can be used to achieve the same basic function as instrumentation amplifiers, it is difficult to reach the same level of performance. Using operational amplifiers often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances.

THE INA104

A simplified schematic of the INA104 is shown on the first page of this data sheet. It is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found on integrated circuit instrumentation amplifiers.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide

the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature is low due to the monolithic design and improved even further by the state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA104 is operated over wide temperature ranges.

The fourth op-amp (A4) of the INA104 adds a great deal of versatility and convenience to the amplifier. Its use allows easy implementation of active low-pass filtering, [illegible] pin connections make the use of this stage optional and the specifications appear separately in the table of Electrical Specifications.

USING THE INA104

Figure 1 shows the simplest configuration of the INA104. The gain is set by the external resistor, R_G, with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally between pins 5 and 14. At high gains where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect. However, this error can be virtually eliminated with the INA104 by using the gain sense circuit connection.

Pins 1, 5, 14, and 18 are accessible so that a four-terminal connection can be made to R_G. (Pins 1 and 18 are the voltage sense terminals since no signal current flows into the operational amplifiers' inputs.) This may be useful at high gains where the value of R_G becomes small.

The optional offset adjust capability is shown in Figure 1. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed (if input offset is not adjusted to zero) when the gain is changed. Also, the input drift will be affected by approximately $0.31\mu V/°C$ per $100\mu V$ of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is frequently desirable to null the input component of offset (Figure 1) and occasionally that of the output

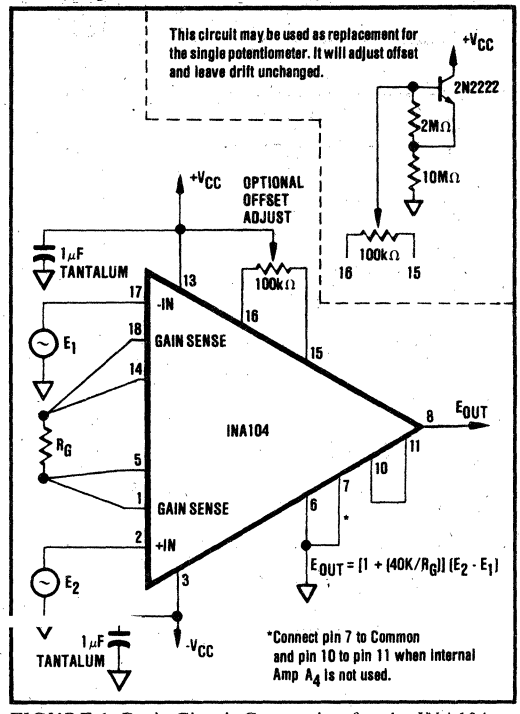


FIGURE 1. Basic Circuit Connection for the INA104 Including Optional Input Offset Null Potentiometer.

(Figure 2). The quality of the potentiometer will affect the results, therefore, choose one with good temperature and mechanical-resistance stability. The procedure is as follows:

1. Set $E_1 = E_2 = 0V$ (be sure a good ground return path exists to the input).
2. Set the gain to the desired value (greater than 1) by choosing R_G.
3. Adjust the 100kΩ potentiometer in Figure 1 until the output reads 0V ±1mV or desired setting. Note that the offset will change when the gain is changed. If the output component of offset is to be removed or if it is desired to establish an intentional offset, adjust the 100kΩ potentiometer in Figure 2 until the output reads 0V ±1mV or desired setting. Note that the offset will not change with gain, but be sure to use a stable amplifier with good DC characteristics. The range of adjustment is ±15mV as shown. For larger ranges change the ratio of R_1 to R_2. The op amp is used to maintain a low resistance (<0.1Ω) from pin 6 to Common to avoid CMR degradation.

BASIC CIRCUIT CONNECTION

The basic circuit connection for the INA104 is shown in Figure 1. The output voltage is a function of the differential input voltage times the gain.

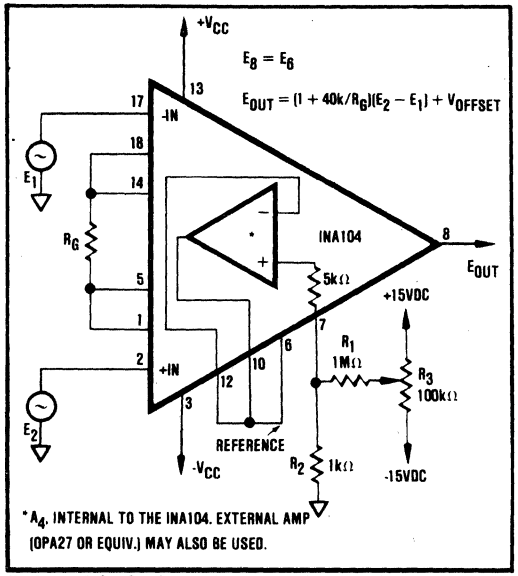


FIGURE 2. Optional Output Offset Nulling or Offsetting Using an Amplifier(Low Impedance to Pin 6).

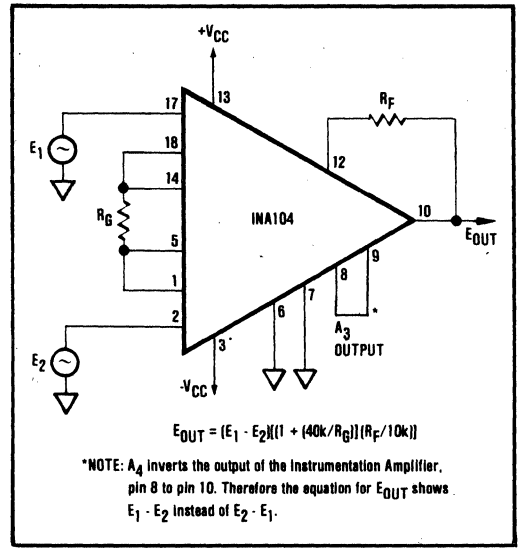


FIGURE 3. Additional Gain From Output Stage.

Figure 1 does not include additional internal op amp A_4. Power supply bypassing with a 1μF tantalum capacitor or equivalent is always recommended.

In applications which do not use the fourth internal amplifier (A_4 - pins 7, 9, 10, 11, and 12), pin 7 should be connected to Common and pins 10 and 11 should be connected together. This will prevent the output of A_4 from saturating ("locking-up") and affecting the offset of the instrumentation amplifier, A_1, A_2, and A_3.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gages, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA104 accomplishes all of these with high precision.

Figures 3 through 13 show some typical applications circuits.

Figure 3 shows how the output stage may be used to provide additional gain. If gains greater than 1000V/V (10,000 up to 100,000 and greater) are desired it is better to place some gain in the output amplifier rather than the input stage due to the low values of R_G required ($R_G < 40\Omega$ for $(1 + 40k/R_G) > 1000$). Note, however, that accuracy can degrade due to very-high amplification of offset, drift, and noise errors.

Output offsetting ("zero suppression" or "zero elevation") may be more easily accomplished with the INA104 than with most other IC instrumentation amplifiers as shown in Figure 4. The use of the extra internal op amp, A_4, means that CMR of the instrument amp is not disturbed, and that a convenient value of variable resistor can be used. The circuit shown in Figure 2 can also be used to achieve the desired offsetting by scaling the resistors R_1 and R_2. A low impedance path from pin 6 to Common should be provided to achieve the high CMR specified. Resistance above 0.1Ω will cause the CMR to fall below 106dB.

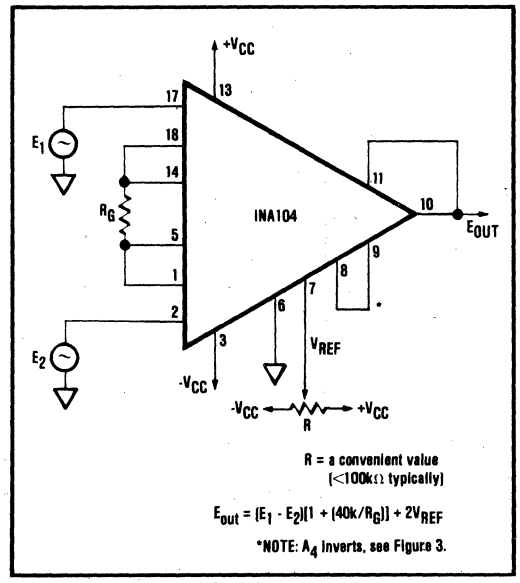


FIGURE 4. Output Offsetting.

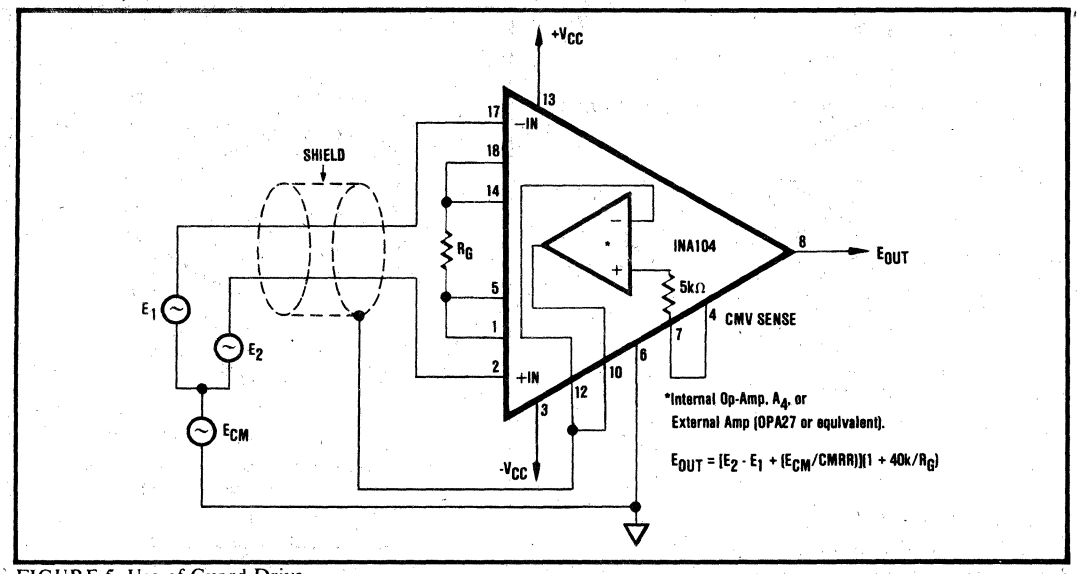


FIGURE 5. Use of Guard Drive.

Amplifier A_4 also allows active low-pass filtering to be implemented conveniently with a single capacitor. Filtering can be used for noise reduction or band-limiting of the output signal as shown in Figure 6.

The common-mode voltage from the 26kΩ resistors in the input section appears at pin 4. Figure 5 shows how this voltage can be used to drive the shield of the input cable. Since the cable is driven at the common-mode voltage, the effects of distributed capacitance is reduced and the AC system common-mode rejection may be improved. Amplifier A_4 buffers the CMV at pin 4 from the input cable.

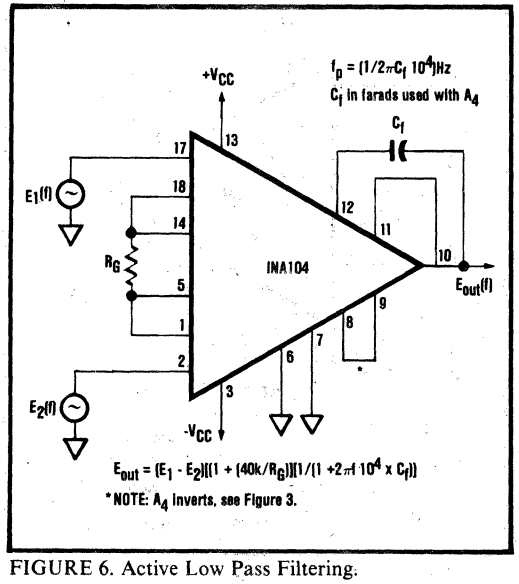


FIGURE 6. Active Low Pass Filtering.

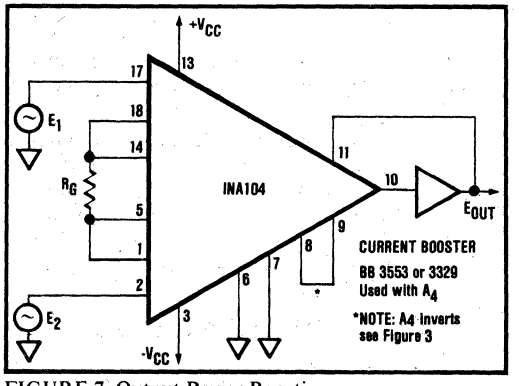


FIGURE 7. Output Power Boosting.

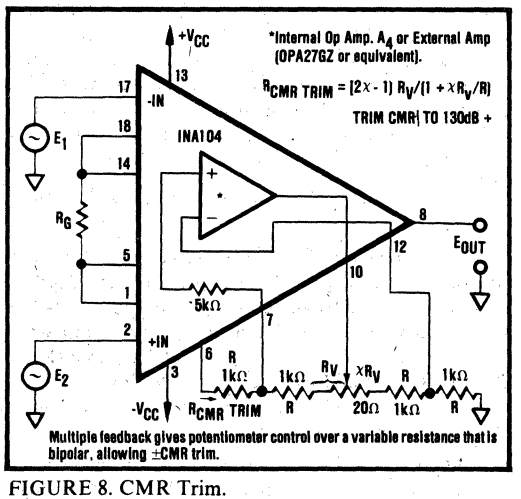


FIGURE 8. CMR Trim.

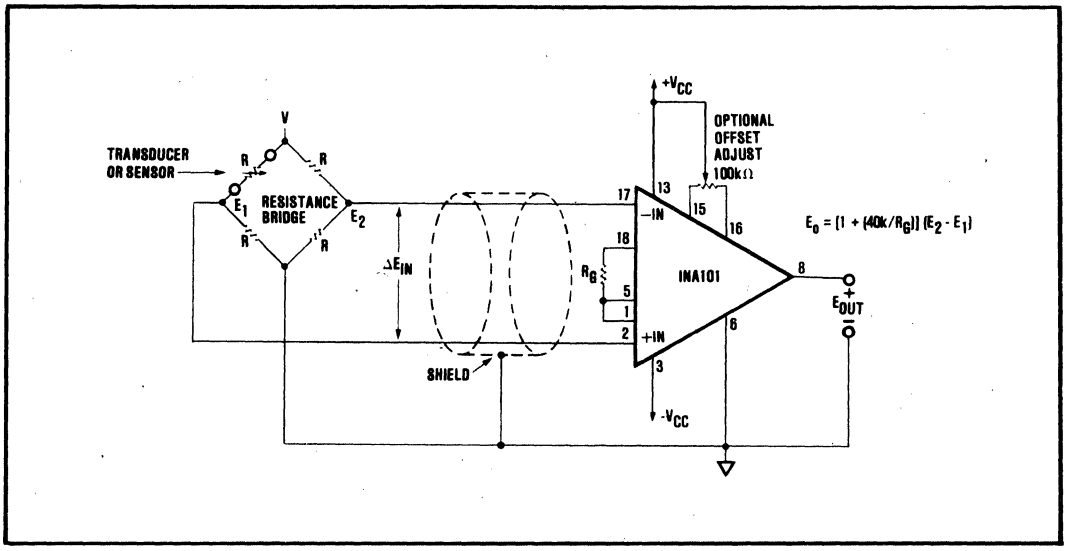


FIGURE 9. Amplification of a Differential Voltage from a Resistance Bridge.

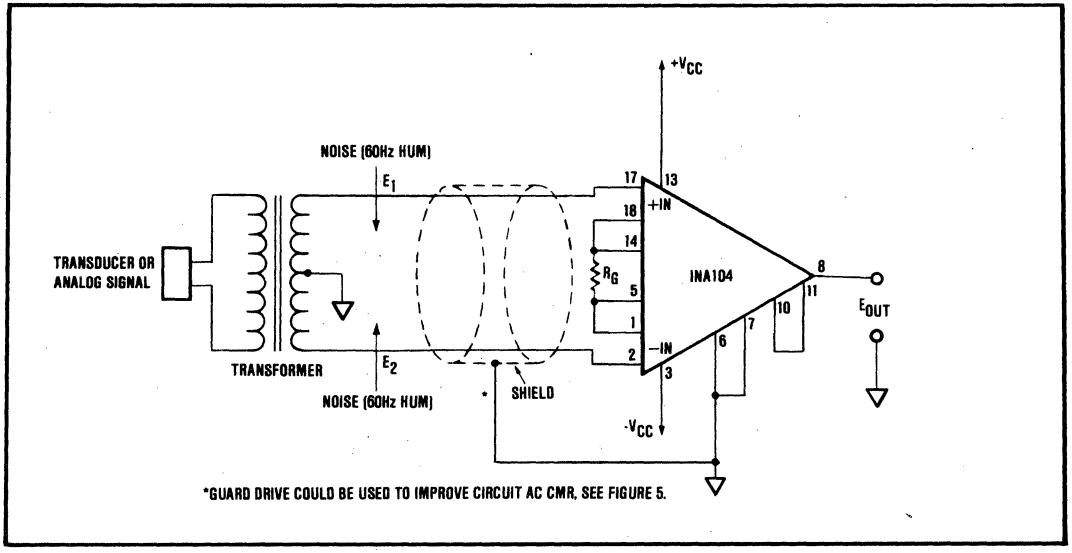


FIGURE 10. Amplification of a Transformer Coupled Analog Signal.

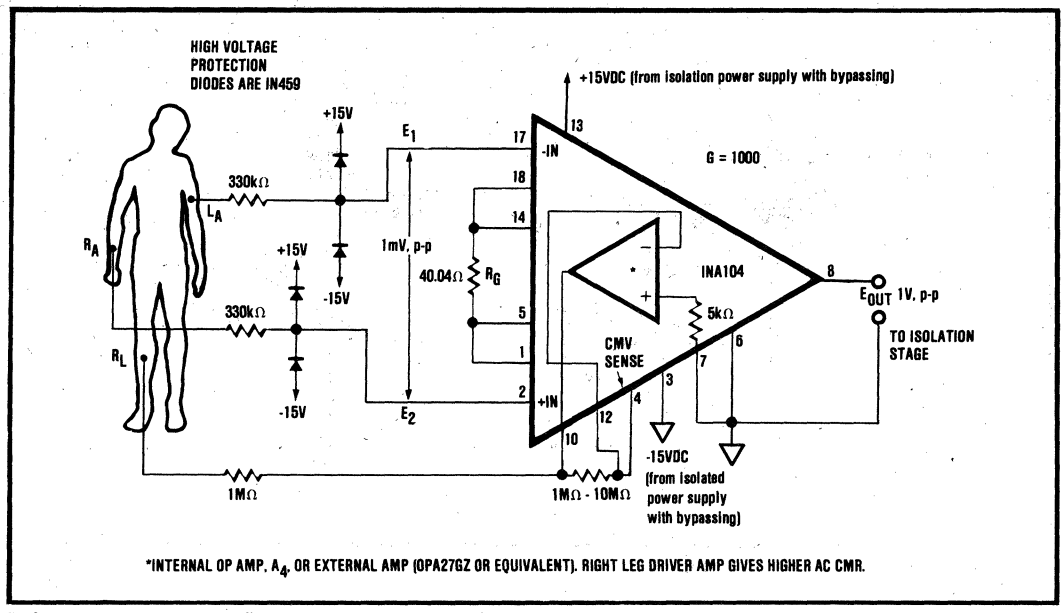


FIGURE 11. ECG Amplifier or Recorder Preamp for Biological Signals.

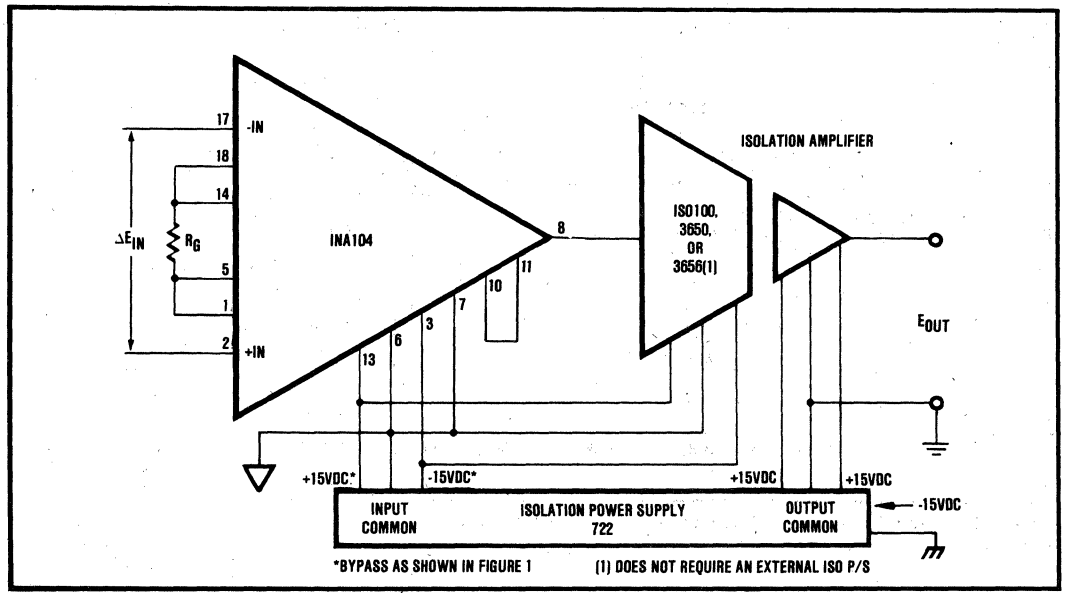


FIGURE 12. Precision Isolated Instrumentation Amplifier.

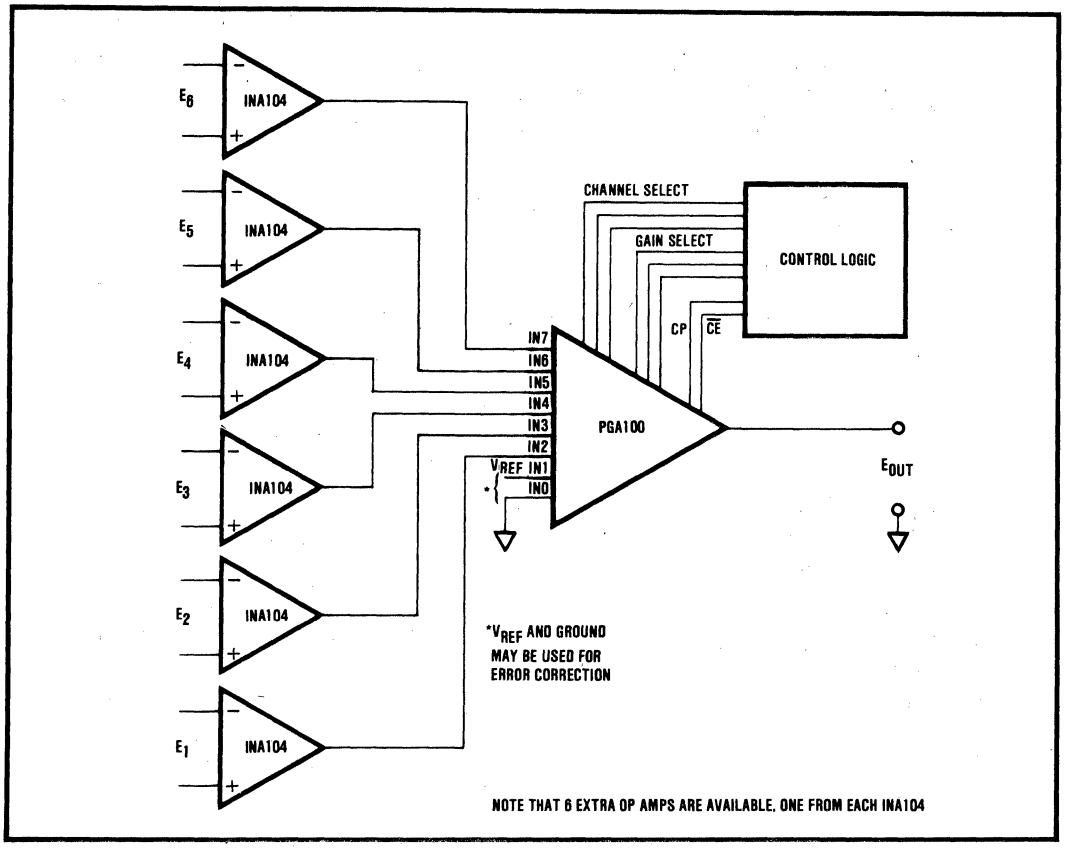


FIGURE 13. Multiple Channel Precision Instrumentation Amplifier.

GENERAL RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damaging can cause performance degradation or failure, either immediate or latent. As a general practice we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove static-generating materials, such as untested plastics, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% is recommended).

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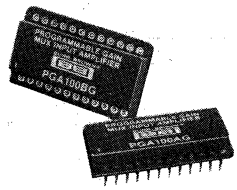


PGA100

Digitally-Controlled Programmable Gain/Multiplexed Input OPERATIONAL AMPLIFIER

FEATURES

- HIGH GAIN ACCURACY, ±0.02%, max (B grade)
- LOW NONLINEARITY, ±0.005%, max (B grade)
- FAST SETTLING, 5μsec to 0.01%
- LOW CHANNEL-TO-CHANNEL CROSSTALK, ±0.003%
- INPUT PROTECTION, ±20V, max above $\pm V_{CC}$
- 8 ANALOG INPUT CHANNELS WITH HIGH Z_{IN}, $10^{11}\Omega$
- 8 BINARY GAINS 1, 2, 4, 8, 16, 32, 64, 128 (V/V)
- FULLY MICROPROCESSOR-COMPATIBLE

APPLICATIONS

- DATA ACQUISITION SYSTEM AMPLIFIER
- SOFTWARE ERROR CORRECTION
- AUTO-ZEROING CAPABILITY
- DIGITALLY-CONTROLLED AUTORANGING SYSTEM
- TEST EQUIPMENT
- REMOTE INSTRUMENTATION SYSTEM
- SYSTEM DYNAMIC RANGE AND RESOLUTION IMPROVEMENT

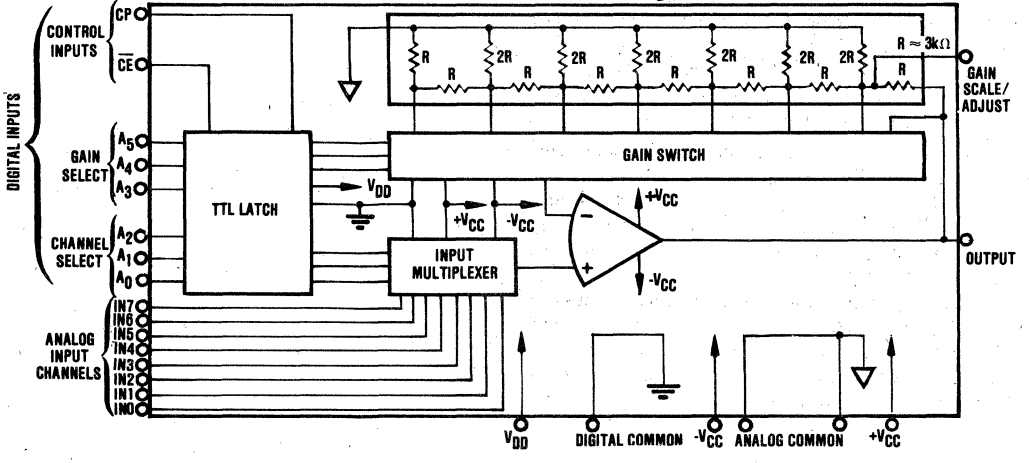
DESCRIPTION

The PGA100 is a precision, digitally-programmable-gain multiplexed-input amplifier. The user can select any one of eight analog input channels simultaneously with any one of eight noninverting binarily weighted gain steps from 1 to 128 (V/V). The digital gain and channel select are latchable for microprocessor interface. Also, the fast 5μsec settling time is ideal for rapid channel scanning in data acquisition systems.

Precision laser-trimming of both offset voltage and gain accuracy, with good temperature tracking of feedback resistor ratios, permits direct use without adjustments. However, hardware or software correction of errors is readily achievable.

In addition, gain scaling to gains other than 1 to 128V/V can easily be accomplished.

Microcircuit construction and the use of laser-trimmed thin-film feedback resistors achieve high accuracy, small size, and low cost not obtained with discrete designs.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC unless otherwise noted.

PARAMETER	CONDITIONS	PGA100AG MIN	PGA100AG TYP	PGA100AG MAX	PGA100BG MIN	PGA100BG TYP	PGA100BG MAX	UNITS
GAIN, G								
Inaccuracy(1)	G = 1 to 128, I_o = 1mA		±0.01	±0.05		±0.005	±0.02	%
vs Temperature(2)	-25°C ≤ T_A ≤ +85°C		±5	±10		"	"	ppm/°C
vs Time			±0.001			"		%/1000 hrs.
Nonlinearity(3)	G = 1 to 128, I_o = 1mA		±0.004	±0.01		±0.002	±0.005	% of FS
vs Temperature(2)	-25°C ≤ T_A ≤ +85°C		±2	±5		"	"	ppm/°C
vs Time			±0.001			"		%/1000 hrs.
Warm-up Time		1			"			min
RATED OUTPUT								
Voltage	I_o = ±2mA	±10			"			V
Current	V_o = ±10V	±2			"			mA
Output Resistance	G ≤ 128		0.05			"		Ω
Short Circuit Current			±15			"		mA
Capacitive Load Range	Phase Margin ≥ 25°		1000			"		pF
INPUT OFFSET VOLTAGE								
Initial	T_A = +25°C		±0.1	±1		±0.05	±0.5	mV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6			"		µV/°C
vs Supply Voltage	±8VDC ≤ | V_{CC} | ≤ ±18VDC		±10	±80		"	"	µV/V
vs Time			±15			"		µV/mo.
INPUT BIAS CURRENT								
Initial	T_A = +25°C							
"OFF" Channel			±10			"		pA
"ON" Channel			±0.1			"	±1	nA
vs Temperature			Note 4			"		
INPUT DIFFERENCE CURRENT, BETWEEN CHANNELS								
Initial	T_A = +25°C							
"OFF" Channel			±20			"		pA
"ON" Channel			±0.2			"	±2	nA
vs Temperature			Note 4			"		
ANALOG INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			±(|V_{CC}|+20)			"	V
Input Voltage Range	Linear operation	±10			"			V
Input Impedance								
"OFF" Channel			10^{12} || 5			"		Ω || pF
"ON" Channel			10^{11} || 25			"		Ω || pF
INPUT NOISE								
Voltage Noise Density	f_o = 1Hz		200			"		nV/√Hz
	f_o = 10Hz		60			"		nV/√Hz
	f_o = 100Hz		25			"		nV/√Hz
	f_o = 1kHz		18			"		nV/√Hz
	f_o = 10kHz		18			"		nV/√Hz
	f_o = 100kHz		18			"		nV/√Hz
Voltage Noise	f_B = 0.1Hz to 10Hz		2.6			"		µV, p-p
Current Noise Density	f_o = 0.1Hz thru 8kHz		6			"		fA/√Hz
Current Noise	f_B = 0.1Hz to 10Hz		115			"		fA, p-p
DYNAMIC RESPONSE								
Gain Bandwidth Product			5			"		MHz
Full Power Bandwidth	G = 1, V_o = 20V, p-p, R_L = 5kΩ		220		80	"		kHz
Slew Rate	G = 1, V_o = ±10V, R_L = 5kΩ		14		5	"		V/µsec
Settling Time(5)	G = 1, V_o = ±10V, R_L = 5kΩ							
ε = 1%			2.5			"		µsec
ε = 0.1%			3			"		µsec
ε = 0.01%			5			"		µsec
Rise Time	10% to 90%, small signal		70			"		nsec
Phase Margin	G = 1, R_L = 5kΩ		60			"		Degrees
Overload Recovery (6)	G = 1, 50% overdrive		2			"		µsec
Crosstalk, RTI(5)(7)	20V, p-p, 1kHz sine, R_S = 1kΩ on all OFF channels		±0.003			"		%
DIGITAL INPUT(8)								
Input "Low" Threshold, V_{IL}				0.8			"	V
Input "High" Threshold, V_{IH}		2.0			"			V
f_{max}, Maximum Clock Frequency		30			"			MHz
t_{WL}, Clock Pulse Width (Low)	Figure 1	20			"			nsec
t_{s_1}, Setup Time (Data to CP)	Figure 1	20			"			nsec
t_{h_1}, Hold Time (Data to CP)	Figure 1	5			"			nsec
t_{s_2}, Setup Time ($\overline{CE}$ to CP)	Figure 1	25			"			nsec
t_{h_2}, Hold Time ($\overline{CE}$ to CP)	Figure 1	5			"			nsec

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	PGA100AG MIN	PGA100AG TYP	PGA100AG MAX	PGA100BG MIN	PGA100BG TYP	PGA100BG MAX	UNITS
ANALOG SUPPLY								
Rated Voltage			±15					VDC
Voltage Range	Derated performance	±8		±18	*	*	*	V
Positive Quiescent Current			+20	+27		+15	+20	mA
Negative Quiescent Current			-10	-16		-7.5	-12	mA
DIGITAL SUPPLY								
Rated Voltage			+5			*		VDC
Voltage Range		+4.75		+5.25	*		*	V
Quiescent Current	V_{DD} = +5.25V		15	27		*	*	mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Operating	Derated performance	-55		+125	*		*	°C
Storage		-55		+125	*		*	°C

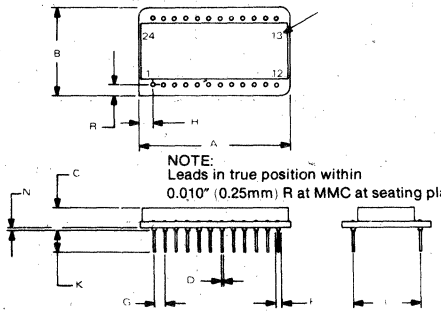
*Specifications same as PGA100AG.

NOTES:

1. Inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero.
2. Parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
3. Nonlinearity is the maximum peak deviation from a "best straight line" (curve fitting on input-output graph) expressed as a percent of the full scale peak-to-peak output. Gain constant, V_{OUT} ranges from -10V to +10V.
4. Doubles approximately every 10°C.
5. See Typical Performance Curves.
6. Time required for the output to return from saturation to linear operation following the removal of an input overdrive signal.
7. Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is expressed as a percent of the signal applied to all OFF channels.
8. All digital inputs are one 74LSTTL load.

MECHANICAL

Pin numbers shown for reference only.
Numbers may not be marked on package.



NOTE:
Leads in true position within
0.010" (0.25mm) R at MMC at seating plane.

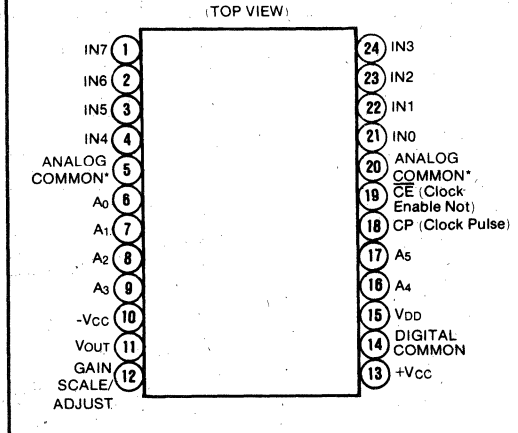
CASE: Black Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 6.3 grams (0.225 oz.)
HERMETICITY: Conform to method 1014 Condition C Step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

ABSOLUTE MAXIMUM RATINGS

Analog Supply	±18V
Digital Supply	+7V
Input Voltage Range, Analog	±(|V_{CC}| +20)V
Input Voltage Range, Digital	+7V
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

PIN DESIGNATIONS

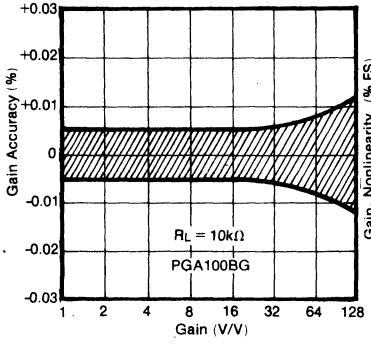


*Connected internally. Use pin 20 as the primary analog common.

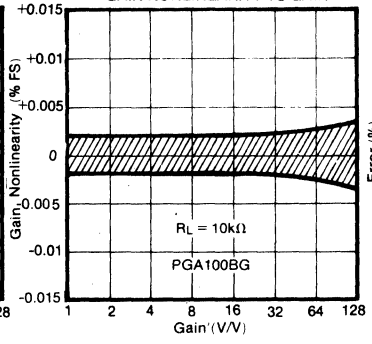
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC, unless otherwise noted.)

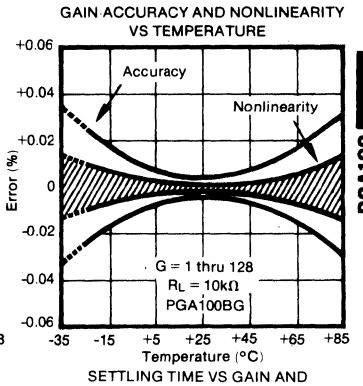
GAIN ACCURACY VS GAIN



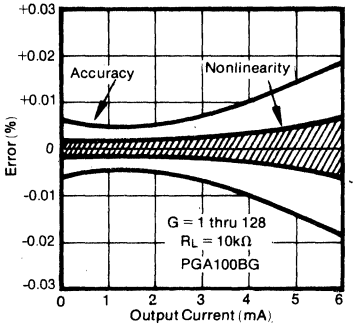
GAIN NONLINEARITY VS GAIN



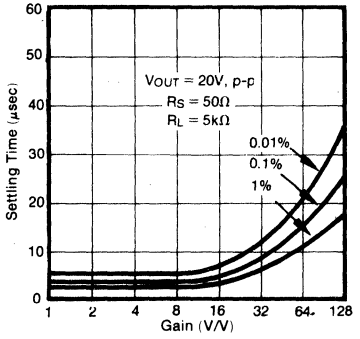
GAIN ACCURACY AND NONLINEARITY VS TEMPERATURE



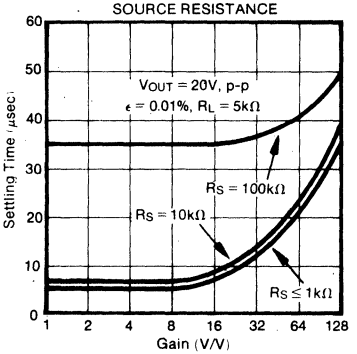
GAIN ACCURACY AND NONLINEARITY VS OUTPUT CURRENT



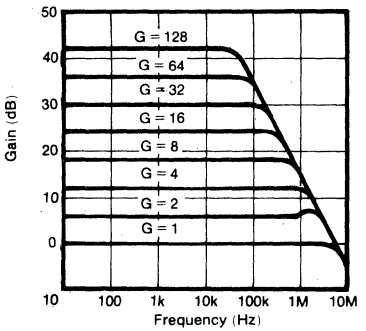
SETTLING TIME VS GAIN



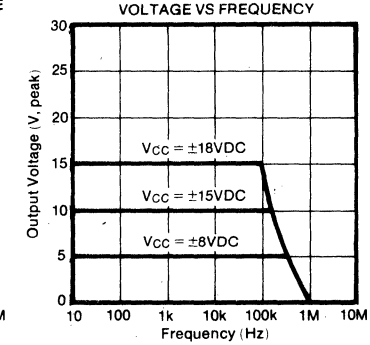
SETTLING TIME VS GAIN AND SOURCE RESISTANCE



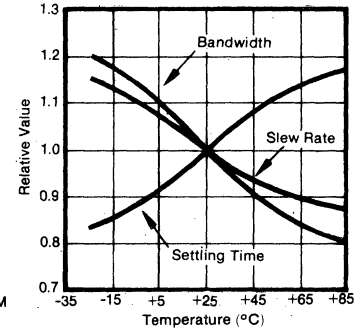
SMALL SIGNAL FREQUENCY RESPONSE



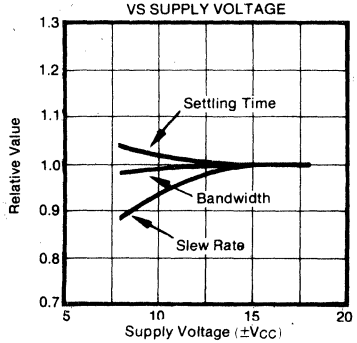
LARGE SIGNAL OUTPUT VOLTAGE VS FREQUENCY



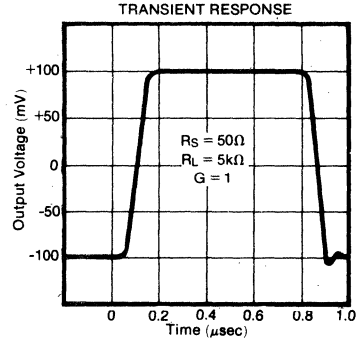
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



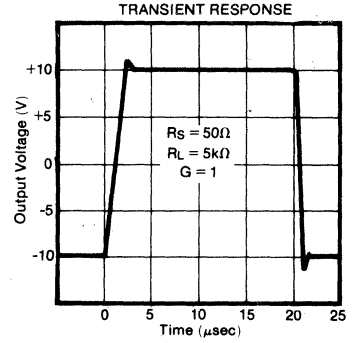
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



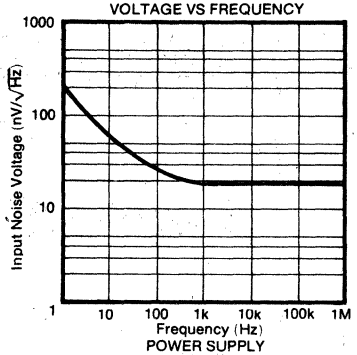
SMALL SIGNAL TRANSIENT RESPONSE



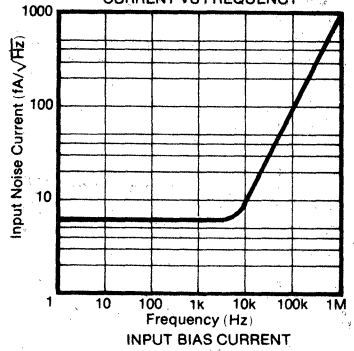
LARGE SIGNAL TRANSIENT RESPONSE



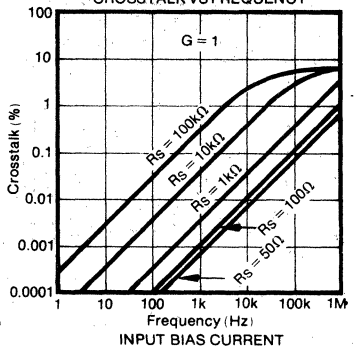
INPUT NOISE VOLTAGE VS FREQUENCY



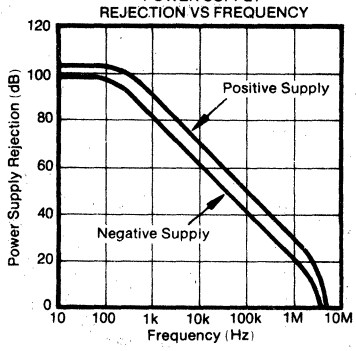
INPUT NOISE CURRENT VS FREQUENCY



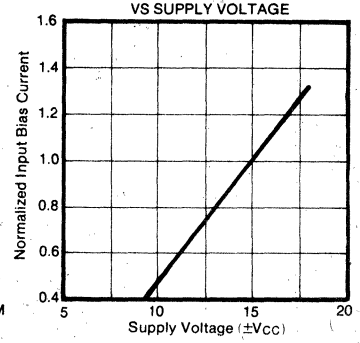
CHANNEL-TO-CHANNEL CROSSTALK VS FREQUENCY



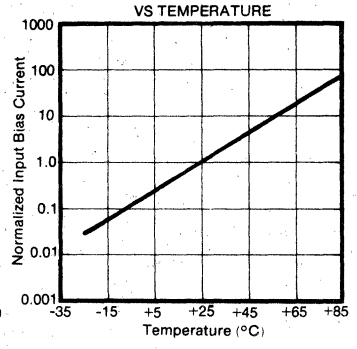
POWER SUPPLY REJECTION VS FREQUENCY



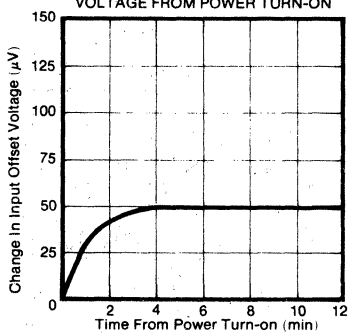
INPUT BIAS CURRENT VS SUPPLY VOLTAGE



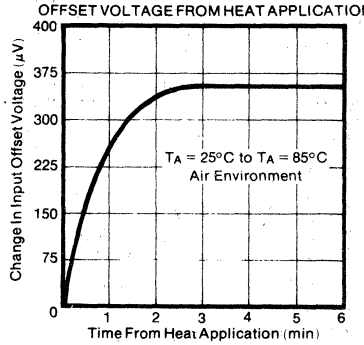
INPUT BIAS CURRENT VS TEMPERATURE



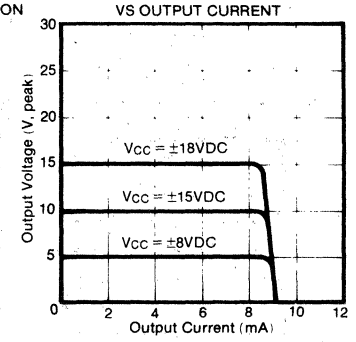
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



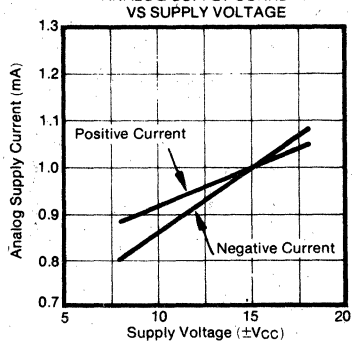
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



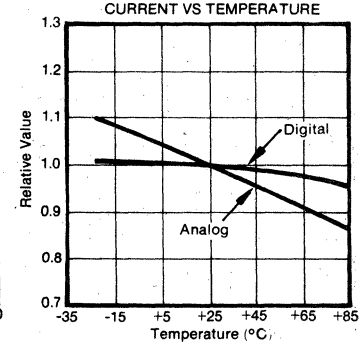
OUTPUT VOLTAGE VS OUTPUT CURRENT



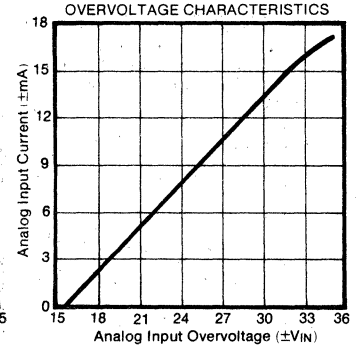
ANALOG SUPPLY CURRENT VS SUPPLY VOLTAGE



QUIESCENT SUPPLY CURRENT VS TEMPERATURE



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



DISCUSSION OF PERFORMANCE

The PGA100 is a self-contained programmable-gain amplifier whose gain can be changed in 8 binarily weighted steps from 1 to 128 or as scaled externally through the gain scale/adjust pin. The gain control is accomplished by the gain switch (break-before-make) whose position is determined by the 3-bit TTL address, A_3, A_4, and A_5. When selected, 1 of 8 positions connects the thin-film resistor network to the feedback loop of the op amp. This establishes the desired gain. (See Installation and Operating Instructions for gain scaling.)

Similarly, the 8 analog input channels are switched by the input multiplexer (break-before-make) whose position is determined by the 3-bit TTL address, A_0, A_1, and A_2. Gain and channel selection appear in Table I. 64-channel/gain combinations are possible.

The digital inputs are latched by the positive transition of the clock pulse, pin 18, when the clock enable, pin 19, is low. The relative set up and holding times specified in the Electrical Specifications are shown in Figure 1. The internal latch is similar to the industry standard 74LS378. Figure 2 shows a timing diagram for selected addresses indicating: the enable function, changing channel and gain, changing channel/constant gain, and constant channel/changing gain.

TABLE I. Gain and Channel Select Truth Table.

GAIN SELECT			GAIN	CHANNEL SELECT			CHANNEL
A_5	A_4	A_3		A_2	A_1	A_0	
0	0	0	1	0	0	0	IN0
0	0	1	2	0	0	1	IN1
0	1	0	4	0	1	0	IN2
0	1	1	8	0	1	1	IN3
1	0	0	16	1	0	0	IN4
1	0	1	32	1	0	1	IN5
1	1	0	64	1	1	0	IN6
1	1	1	128	1	1	1	IN7

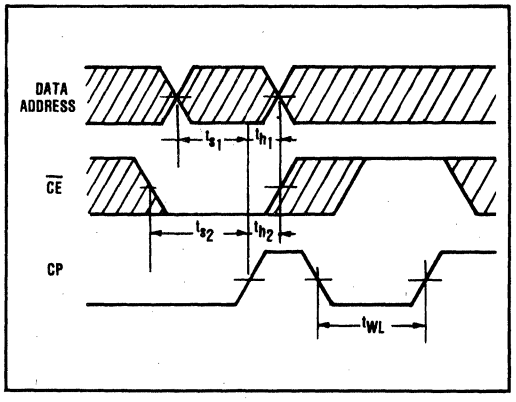


FIGURE 1. Data Address and Clock Enable Setup and Hold Times.

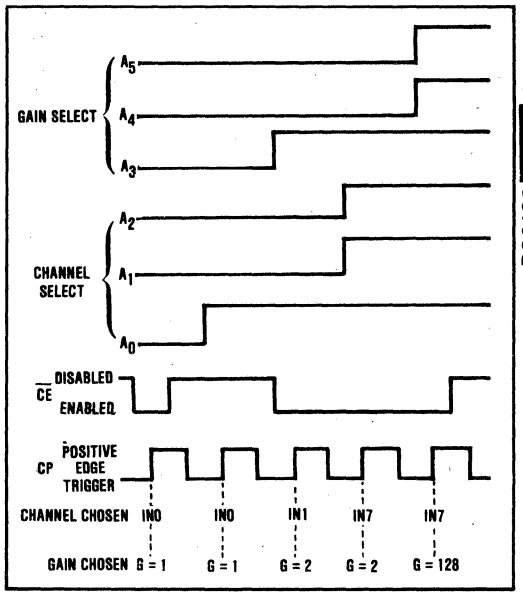


FIGURE 2. Timing Diagram for Selected Addresses.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

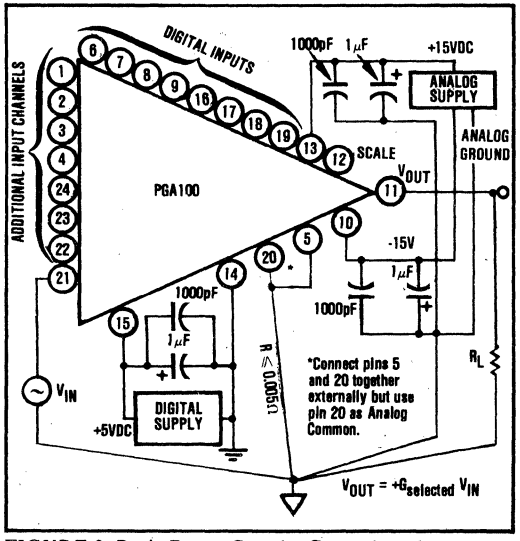


FIGURE 3. Basic Power Supply, Ground, and Signal Connections.

Figure 3 shows the proper analog and digital power supply connections. The supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. To avoid gain errors connect grounds as indicated being sure to minimize ground resistance. Note that a resistance of greater than

0.005Ω in series with the analog common will degrade the specified gain accuracy. IMPORTANT: Normally the digital ground is brought in from the digital power supply on a separate line. However, the analog and digital commons must be connected together somewhere in the system.

OPTIONAL GAIN SCALE/ADJUST

The gain scale/adjust pin is shown in Figure 4. When no connection is made, gains appear as in Table I. At least two functions can be performed. First, the gain range can be scaled to gains other than 1 to 128, for example, 1 to 100 or 1 to 1024. Gain steps, however, retain binary weighting. Some examples are: (1, 1, 2, 4, 8, 16, 32, 64 with pins 11 and 12 connected together), (1, 1.5625, 3.125, 6.25, 12.5, 25, 50, 100), (1, 12.5, 25, 50, 100, 200, 400, 800), and (1, 16, 32, 64, 128, 256, 512, 1024). Scaling is accomplished by using a potentiometer, R_1, shown in Figure 4. Be certain to use a potentiometer of good mechanical and thermal stability. Additional gain drift with temperature should be minimal since it depends on the thermal tracking of the resistance ratio, R_A to R_B, set by the potentiometer.

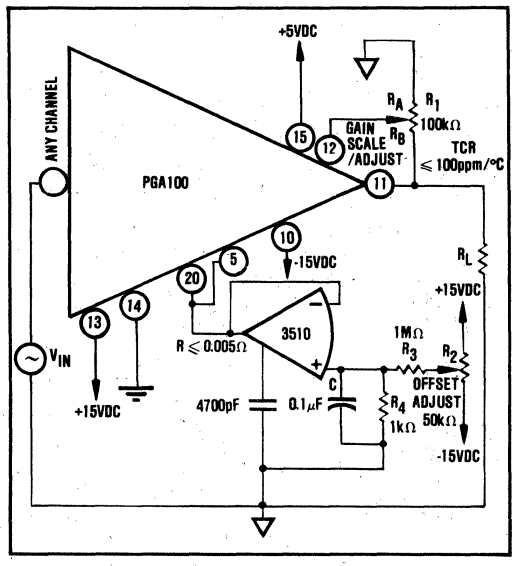


FIGURE 4. External Gain and Offset Adjustment.

Second, the gain inaccuracy, remaining after laser trimming at the factory, can be adjusted to zero at any gain other than unity. To improve resolution and limit adjustment range, a resistor may be added in series with the wiper of the potentiometer and pin 12. This will, however, increase gain drift. Figure 5 shows the effect of gain adjustment. R_1 does not affect gain linearity.

OPTIONAL OFFSET ADJUSTMENT

Figure 4 also illustrates a technique for offset adjustment. This adjustment has no effect at unity gain. R_2 will trim the offset to zero and have neglible effect on the gain accuracy. For best results, trim the offset at the highest

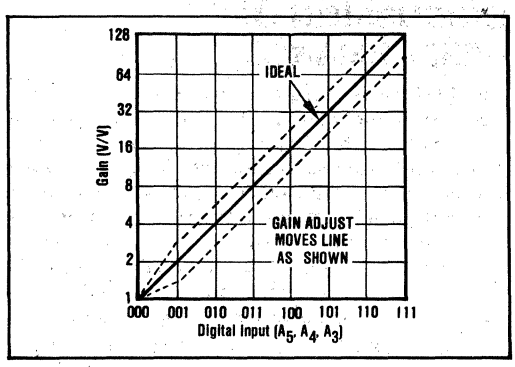


FIGURE 5. Effect of Gain Adjustment.

gain. If R_3 is made smaller, output offsetting can be accomplished. This can be used to introduce an intentional DC voltage at the output. The external amplifier used will add to the input noise, therefore, use one with a noise level of at least three times lower than that specified for the PGA100.

LAYOUT CONSIDERATIONS

Proper attention to layout is necessary to achieve the specified performance of the PGA100. Major goals are to reduce crosstalk, noise pickup, noise coupled from the power supply, and gain errors.

Be certain to separate analog and digital runs to avoid coupling of digital transients. To reduce gain errors, connect analog grounds with a ground plane or a low resistance star configuration as shown in Figure 3. Analog and digital commons must be connected at some point in the system to insure proper operation.

GAIN INACCURACY AND NONLINEARITY

As shown in Figure 3, connect pins 5 and 20 directly together at the unit and use pin 20 as the primary analog common. Ground resistance in series with pin 20 also appears in series with the internal gain-setting resistors and will decrease the magnitude of all gains except unity. The resulting accuracy error varies nonlinearly with the gain selected and therefore cannot be externally adjusted to zero for more than one gain at a time. Gain linearity is not affected by external ground resistance (see Performance Curves.)

CROSSTALK

Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is expressed as a percent of the input signal applied to all OFF channels. For example, the 0.003% specification indicates that 0.6mV, p-p, out of a 20V, p-p, 1kHz sine wave (applied to 7 OFF channels) will appear at the noninverting input of the internal op amp. Note that crosstalk increases with high frequencies due to the capacitive coupling between ON and OFF channels. It also increases with greater source resistance. However, because both the input signal and crosstalk noise are amplified equally, the resulting output signal-to-noise

ratio is independent of gain. Unused input channels should be grounded in order to reduce crosstalk and extraneous noise pickup. (See Performance Curves.)

SETTLING TIME

Settling time is the time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value. It is a very important consideration since this will be the limiting parameter in determining the maximum channel scanning or throughput rate. The PGA100 specification includes the effects of both the multiplexer and amplifier. Note that settling time increases with increasing source resistance and gain. Minimum settling time is achieved by choosing a low source resistance, for example, $R_S \leq 10k\Omega$ and gains ≤ 16. (See Performance Curves.)

INPUT OVERVOLTAGE PROTECTION

The PGA100 provides input overvoltage protection of 20V in excess of either power supply voltage expressed as $\pm(|V_{CC}|+20)$. This is achieved in the dielectrically isolated analog multiplexer which will withstand overvoltage even when the power supplies are off. As a consequence the PGA100 is protected against high input levels and brief transient spikes of up to several hundred volts that can result from signals originating from outside the system. (See Performance Curves.)

TYPICAL APPLICATIONS

The PGA100 is ideal for a variety of applications, especially where low channel-to-channel crosstalk is required. In many applications the PGA100 will not require trimming of offset and gain errors. However, these can be minimized utilizing hardware or software error correction techniques. Figures 6 and 7 show applications of the PGA100 separately and in a data acquisition system.

Figure 7 shows a Data Acquisition System. In this system the PGA100 allows the user to deal with signals of wide dynamic range while maintaining high system resolution. For example: When used with a 12-bit A/D converter in a "floating point" system, the 2^7 gain range of the PGA100 plus the 2^{12} range of the converter produces a total system resolution of 2^{19} (524,000 to 1).

Also the user can modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated amplifiers are not required for various input channels, the PGA100 also saves space and overall system costs. Software correction virtually eliminates system offset and gain errors over both time and temperature.

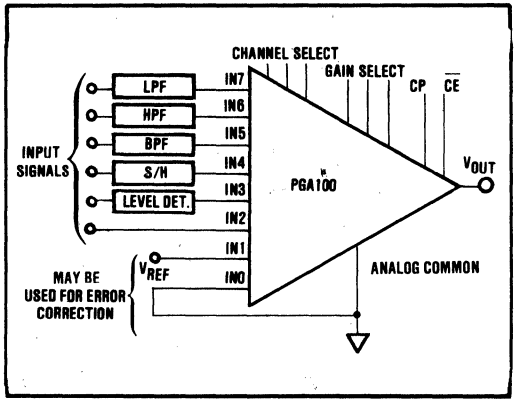


FIGURE 6. Digitally Selectable Function Amplifier.

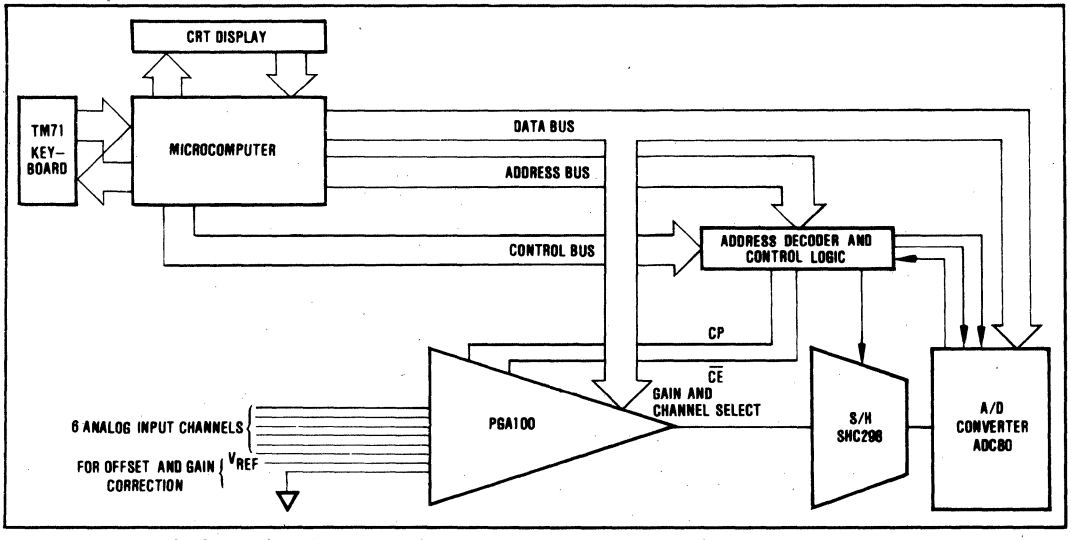
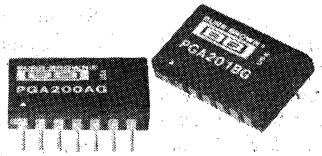


FIGURE 7. Use of PGA100 in a Data Acquisition System with Software Auto-zero and Gain Calibration.

BURR-BROWN®

PGA200/201



Digitally-Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

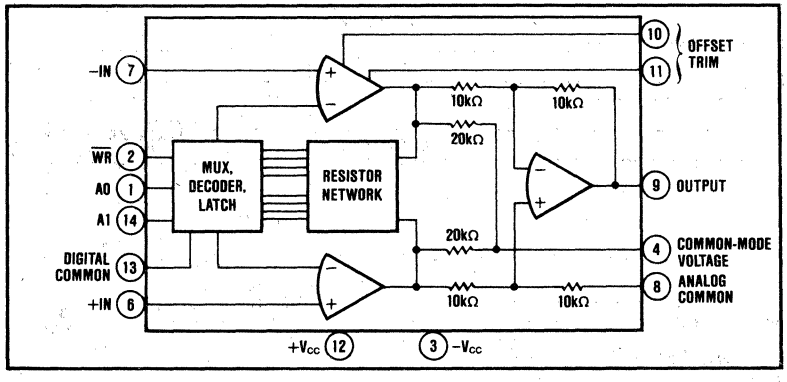
- DIGITALLY-PROGRAMMABLE GAIN
  - — Decade Model - PGA200
    Gains of 1, 10, 100, 1000
  - — Binary Model - PGA201
    Gains of 1, 8, 64, 512
- EXCELLENT GAIN ACCURACY (0.02%, max)
- LOW GAIN NONLINEARITY (0.012%, max; G = 1000)
- LOW GAIN DRIFT (10ppm/°C, max; G = 1000)
- 2-BIT LATCHED TTL-COMPATIBLE GAIN CONTROL
- LOW OFFSET VOLTAGE (25μV RTI, max; G = 1000)
- LOW OFFSET VOLTAGE DRIFT (0.30μV/°C, max; G = 1000)

APPLICATIONS

- DATA ACQUISITION SYSTEM AMPLIFIER
- DIGITALLY-CONTROLLED AUTORANGING SYSTEM
- SYSTEM DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION SYSTEM
- TEST EQUIPMENT

DESCRIPTION

The PGA200 is a hybrid IC instrumentation amplifier with digitally-controlled decade gain steps of 1, 10, 100, and 1000. The PGA201 differs only by providing binary steps of 1, 8, 64, and 512. Both have TTL-compatible latched inputs for microprocessor interface. The logic section has high input impedance and functions without a separate logic power supply. Precision laser-trimmed offset and gain permits use without external adjustments. High performance thin-film resistors with excellent tracking assure low gain drift and excellent stability.



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SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply unless otherwise noted.

MODEL[1]		PGA200/201AG			PGA200/201BG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
GAIN								
Inaccuracy[2] G = 1			0.02	0.05		0.01	0.02	%
G = 10			0.02	0.05		0.01	0.02	%
G = 100			0.02	0.05		0.01	0.02	%
G = 1000			0.02	0.05		0.01	0.02	%
Nonlinearity, G = 1			0.002	0.005		0.001	0.002	%
G = 10			0.002	0.005		0.001	0.002	%
G = 100			0.003	0.007		0.002	0.003	%
G = 1000			0.012	0.025		0.011	0.012	%
Drift vs Temperature, G = 1			10	20		5	10	ppm/°C
G = 10			10	20		5	10	ppm/°C
G = 100			10	20		5	10	ppm/°C
G = 1000			10	20		5	10	ppm/°C
Stability vs Time			0.01			*		%/1khr
RATED OUTPUT								
Voltage	I_o = 5mA	10	12.5		*	*		V
Current	V_o = 10V	5	10.0		*	*		mA
Impedance			0.3			*		Ω
ANALOG INPUT CHARACTERISTICS								
Common-Mode Range		10						V
Absolute Maximum Voltage	No Damage			V_{CC}	*		*	V
Impedance, Differential			10^{10} || 3			*		Ω || pF
Common-Mode			10^{10} || 3			*		Ω || pF
OFFSET VOLTAGE [RTI]								
Initial Offset, max[3], G = 1			225	450		110	225	µV
G = 10			45	90		20	45	µV
G = 100			27	54		11	27	µV
G = 1000			25	50		10	25	µV
vs Temperature, G = 1			10	22		5	10	µV/°C
G = 10			2	4		0.75	1.5	µV/°C
G = 100			1	2		0.20	0.40	µV/°C
G = 1000			1	2		0.15	0.30	µV/°C
vs Time			1 + (20/G)			*		µV/mo
vs Supply	10 < V_{CC} < 18V		1 + (20/G)			*		µV/V
INPUT BIAS CURRENT								
Initial at 25°C	Each input		10	30		5	20	nA
vs Temperature			0.2			*		nA/°C
vs Supply			0.1			*		nA/V
Offset Current			10	30		5	20	nA
vs Temperature			0.5			*		nA/°C
COMMON-MODE REJECTION								
G = 1	DC to 60Hz,	80	95		*	*		dB
G = 10	1kΩ Source	96	110		*	*		dB
G = 100	Imbalance	106	120		*	*		dB
G = 1000		106	120		*	*		dB
INPUT NOISE[4]								
Input Voltage Noise, f_B = 0.1Hz to 10Hz			0.8			*		µV, p-p
Density, f_o = 10Hz			18			*		$NV/\sqrt{Hz}$
f_o = 100Hz			15			*		$NV/\sqrt{Hz}$
f_o = 1kHz			13			*		$NV/\sqrt{Hz}$
Input Current Noise, f_B = 0.1Hz to 10Hz			50			*		pA, p-p
Density, f_o = 10Hz			0.8			*		$pA/\sqrt{Hz}$
f_o = 100Hz			0.46			*		$pA/\sqrt{Hz}$
f_o = 1kHz			0.35			*		$pA/\sqrt{Hz}$
DYNAMIC RESPONSE								
±3dB Flatness	Small signal							
G = 1			500			*		kHz
G = 10			150			*		kHz
G = 100			30			*		kHz
G = 1000			2.4			*		kHz
±1% Flatness	Small signal							
G = 1			50			*		kHz
G = 10			25			*		kHz
G = 100			3			*		kHz
G = 1000			300			*		Hz

ELECTRICAL [CONT]

MODEL	CONDITIONS	PGA200/201AG			PGA200/201BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Full Power	G = 1 to 100		6.4			*		kHz
Slew Rate	G = 1 to 100	0.2	0.4		*	*		V/μsec
Settling Time (0.1%), G = 1			35			*		μsec
G = 10			35			*		μsec
G = 100			50			*		μsec
G = 1000			480			*		μsec
Settling Time (0.01%), G = 1			40			*		μsec
G = 10			40			*		μsec
G = 100			80			*		μsec
G = 1000[5]			670			*		μsec
Overload Recovery Time	50% overdrive							
G = 1 to 100			12			*		μsec
G = 1000			22			*		μsec
DIGITAL INPUT CHARACTERISTICS								
Input Low Threshold				0.8			*	V
Input Low Current				30			*	μA
Input High Threshold		2.4			*			V
Input High Current				30			*	μA
T_{ww}, Write Pulse Width		300			*			nsec
T_s, Data Setup Time		180			*			nsec
T_h, Data Hold Time		30			*			nsec
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		10		18	*		*	V
Quiescent Current			±10	±12		*	*	mA
TEMPERATURE RANGE								
Specification		−40		+85	*		*	°C
Operating		−55		+125	*		*	°C
Storage		−55		+150	*		*	°C

*Specifications same as for PGA200/201AG.

NOTES: (1) All specifications pertain to both PGA200 and PGA201. Values for gains of 10, 100, and 1000 for the PGA200 are the same for gains of 8, 64 and 512. for the PGA201. (2) Measured with a 10kΩ load. (3) Adjustable to zero. This offset is the total offset including both input and output components referred to the input. (4) Noise due to the input stage. There is also an output component which becomes significant in low gain (see Typical Performance Curves). (5) Settling time of the average value of the output waveform since the noise floor in a gain of 1000 is on the order of 0.01% of full scale.

ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18VDC
Internal Power Dissipation 600mW
Analog And Digital Inputs ..... ±V_{CC}
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering 10 Seconds) ..... +300°C
Output Short-Circuit Duration ..... Continuous To Ground
Junction Temperature ..... 175°C

PIN DESIGNATIONS

1. AO
2. $\overline{WR}$
3. $-V_{CC}$
4. Common-Mode Voltage
5. NC
6. +IN
7. −IN
8. Analog Common
9. Output
10. Offset Trim
11. Offset Trim
12. $+V_{CC}$
13. Digital Common
14. A1

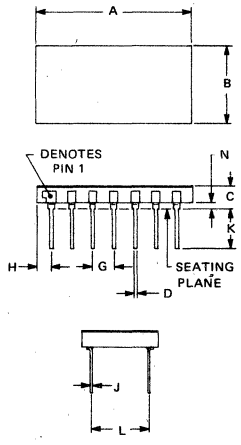
ORDERING INFORMATION

PGA200 or PGA201 X G

Grade: A, B

14-pin DIP, G package

MECHANICAL



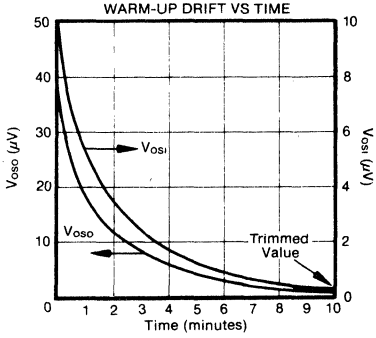
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.770	.810	19.56	20.57
B	.480	.500	12.19	12.70
C	.155	.215	3.94	5.46
D	.016	.020	.41	.51
G	.100 BASIC		2.54 BASIC	
H	.080	.110	2.03	2.79
J	.009	.012	.23	.30
K	.150	.210	3.81	5.33
L	.300 BASIC		7.62 BASIC	
N	.015	.035	.38	.89

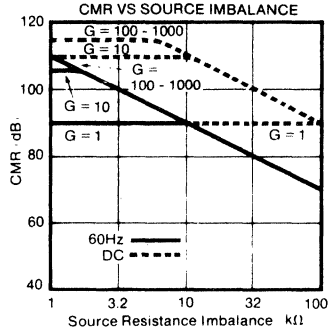
TYPICAL PERFORMANCE CURVES

T_A = +25°C, $\pm V_{CC}$ = 15VDC, unless otherwise noted.

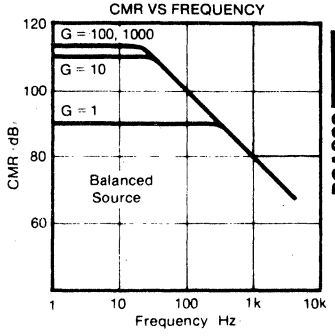
WARM-UP DRIFT VS TIME



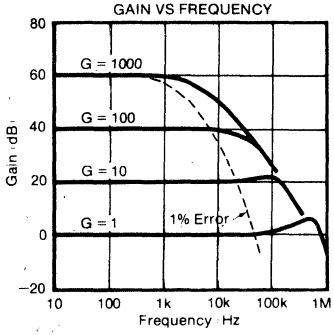
CMR VS SOURCE IMBALANCE



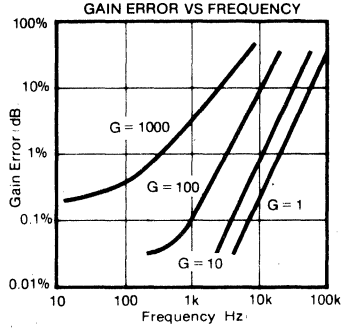
CMR VS FREQUENCY



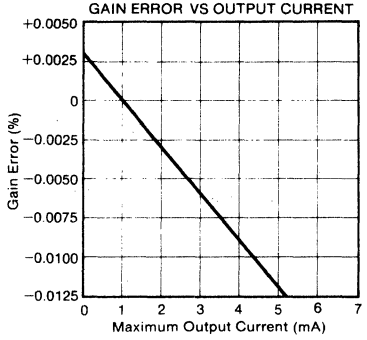
GAIN VS FREQUENCY



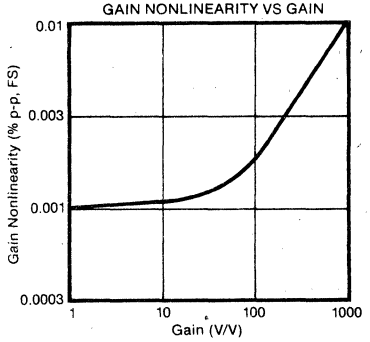
GAIN ERROR VS FREQUENCY



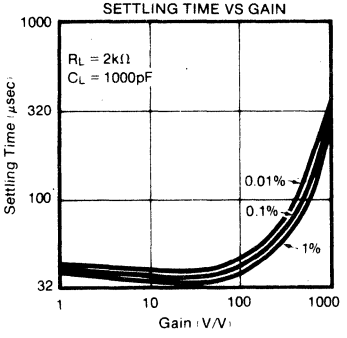
GAIN ERROR VS OUTPUT CURRENT



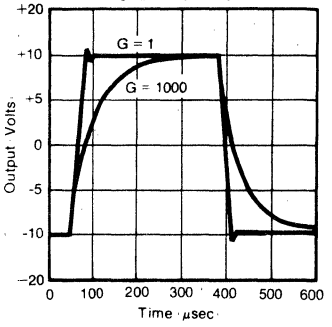
GAIN NONLINEARITY VS GAIN



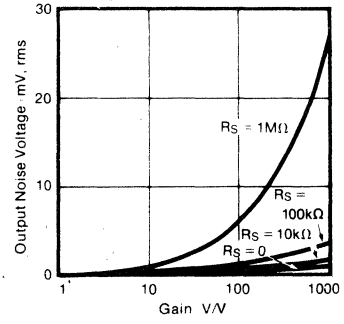
SETTLING TIME VS GAIN



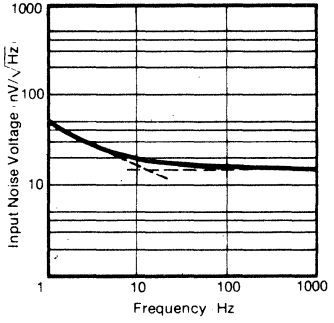
STEP RESPONSE



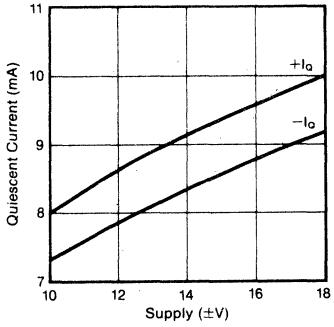
OUTPUT NOISE VS GAIN



INPUT NOISE VOLTAGE VS FREQUENCY 100 GAIN 1000



IQ VS SUPPLY



THEORY OF OPERATION

A simplified block diagram of the PGA200/201 appears on the first page. The diagram consists of three distinct parts. Together these parts form a high-perfomance, differential-input, digitally-programmable dedicated gain block. Each of the parts is optimized for a specific function.

The operational amplifiers are arranged on a monolithic substrate in the classical three-op-amp IA configuration. A nitride-passivated compatible thin-film bipolar process is used to achieve excellent offset and common-mode rejection stability over time and temperature. Advanced laser trimming techniques are used to minimize both the initial input offset and the input offset drift which are typically below 10μV and 0.15μ/V°C respectively. Additionally, careful layout techniques assure input stage thermal tracking with varying load conditions.

The gain-setting resistors are arranged on a separate substrate which is thermally isolated from the output stage. This results in minimum thermal interaction and a layout optimized for resistor tracking. All gains are dependent on the ratio of resistors which are composed of combinations of equal valued segments. The segmented approach provides the ultimate in accuracy and stability.

The latch and multiplexer, which set the gain, are implemented in CMOS. This provides high impedance logic inputs, low quiescent current and TTL compatibility without the need for a separate logic power supply. The logic threshold is internally derived from the $+V_{CC}$ power supply and is referenced to digital common. The circuit is arranged so that multiplexer ON resistance is in series with the high input impedance of the input amplifiers and hence contributes negligible gain error.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper analog and digital power supply connections. The analog supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors with connections made as close as possible to the amplifier supply terminals and load common connection.

Because the amplifier is direct-coupled, it must have a ground return path for the bias currents associated with the amplifier inputs at pins 6 and 7. If the ground return path is not inherent in the signal source (floating source), it must be provided externally. The ground return resistance (R_{gr}) should be kept as low as practical. The upper limit is approximately 50MΩ because of the input bias current of the amplifier and its common-mode voltage range.

In order to maintain linear operation of the input amplifiers the common-mode input voltage must be kept within the following limits:

$$-10V + (E_{in} \times G)/2 < E_{cm} < +10V - (E_{in} \times G)/2.$$

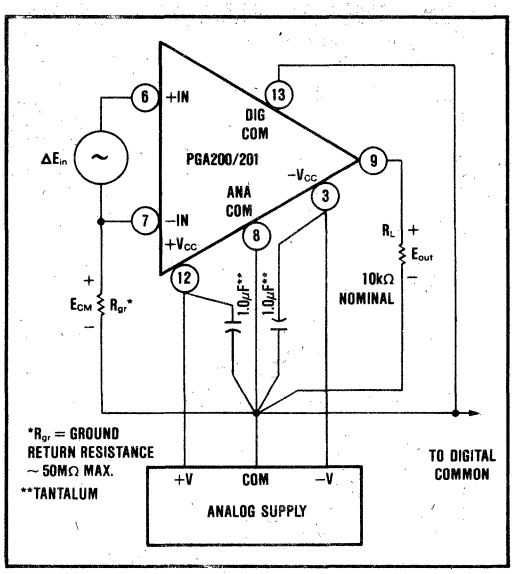


FIGURE 1. Power Supply and Signal Connections.

GAIN SETTING

Gain is determined by a 2-bit digital word applied to the A0 and A1 inputs (see Table I). The $\overline{WR}$ (pin 2) provides a latch function. When $\overline{WR}$ is a logic low, the latch is transparent and the gain directly follows the code on A0 and A1. When $\overline{WR}$ goes to a logic high, the gain is latched according to the previous state of A0 and A1. The timing requirements illustrated in Figure 2 must be observed. The minimum write pulse width is 300nsec while the data setup and hold times are 180nsec and 30nsec respectively. Although the logic inputs are TTL compatible, they are high impedance and the allowable logic high voltage extends to $+V_{CC}$.

Table I shows the gain select truth table. The gains for the PGA201 are shown in parenthesis.

TABLE I. Gain Select Truth Table.

A1	A0	$\overline{WR}$	GAIN PGA200 [PGA201]
X	X	⎍	Maintains previous gain
0	0	0	1 (1)
0	1	0	10 (8)
1	0	0	100 (64)
1	1	0	1000 (512)

Logic "1": $V_{AH} \geq 2.4V$
Logic "0": $V_{AL} \leq 0.8V$

INPUT AND OUTPUT OFFSETTING

Figure 3 illustrates the appropriate connections for offset adjustment. Since the instrumentation amplifier is a two-stage device, the total offset is composed of two parts, an input and an output component. Because both are actively laser trimmed, adjustment is not required in most applications. The input component is due to the mismatch in the offset voltage of the two input amplifiers

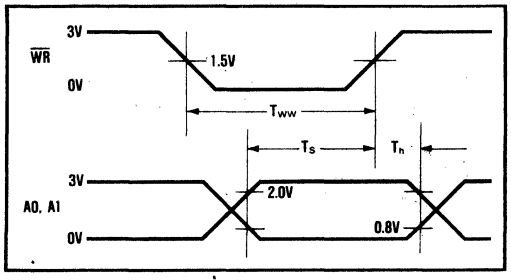


FIGURE 2. Timing Diagrams.

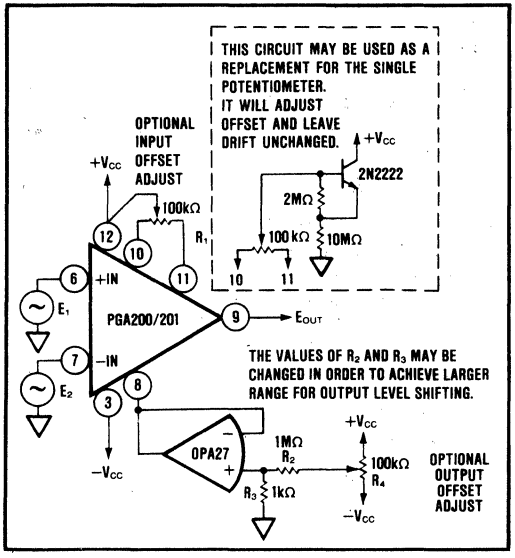


FIGURE 3. Optional Input/Output Offset Adjust.

and changes with gain. The output component is due to the offset of the second stage amplifier and is constant.

R_1 may be used to null the input offset. Its quality will affect the results; therefore, choose a potentiometer with good temperature and mechanical resistance stability. The wiper should be connected to $+V_{CC}$ at a point as close as possible to the $+V_{CC}$ terminal of the instrumentation amplifier. Null the offset as follows:

1. Set $E_1 = E_2 = 0$ (be sure a good ground return path exists to the inputs).
2. Set the gain to 1000 (or 512 for PGA201).
3. Adjust R_1 until the output reaches 0V ±1mV or desired value.

Input offset adjustment will affect the offset drift by approximately 3.1μV/°C/mV of offset that is trimmed. This effect can be greatly reduced by using the alternate offset adjust circuit shown inside the dashed line.

The output offset may be nulled or, alternately, the output can be level shifted with R_4. R_2 and R_3 divide the wiper voltage of R_4 down for increased sensitivity. Their ratio may be changed in order to increase the range of adjustment if desired. The buffer amplifier is required in order to keep the impedance at pin 8 low so that the gain and common-mode rejection will not be disturbed.

GUARD DRIVE

Use of the guard drive connection in Figure 4 can improve system common-mode rejection when the distributed capacitance of the input lines is significant.

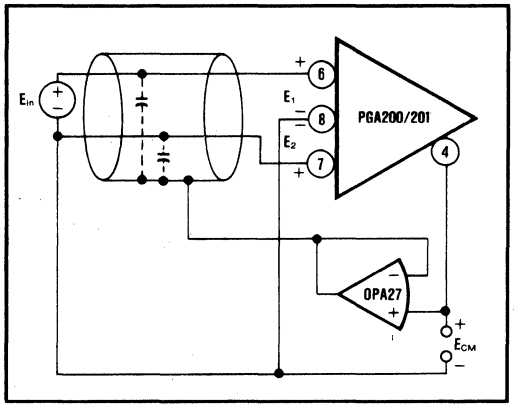


FIGURE 4. Guard Drive.

The common-mode voltage which appears on pin 4 is resistively derived from the output of the first stage amplifiers and has the value $(E_1 - E_2)/2$. This voltage is used to drive the shield which preferably should extend up to and around the input pins 6 and 7. This configuration improves common-mode rejection by reducing the common-mode current flow. The buffer amplifier is used in order to supply more current than the internal 20kΩ resistors can provide so that the guard can accurately track the actual common-mode voltage.

TYPICAL APPLICATIONS

The PGA200 and PGA201 are ideal for computer-controlled data acquisition systems as shown in Figure 5.

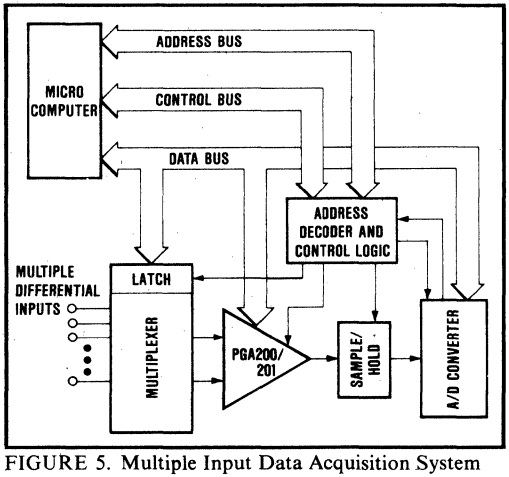
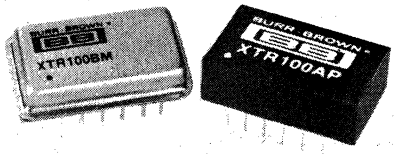


FIGURE 5. Multiple Input Data Acquisition System With Various Input Ranges.

BURR-BROWN®



XTR100

Precision, Low Drift 4mA to 20mA TWO-WIRE TRANSMITTER

FEATURES

- INSTRUMENTATION AMPLIFIER INPUT
  - Low Offset Voltage, 25μV max
  - Low Voltage Drift, 0.5μV/°C max
  - Low Nonlinearity, 0.01% max
- TRUE TWO-WIRE OPERATION
  - Power and Signal on One Wire Pair
  - Current Mode Signal Transmission
  - High Noise Immunity
- DUAL MATCHED CURRENT SOURCES
- WIDE SUPPLY RANGE, 11.6V to 40V
- -40°C TO +85°C SPECIFICATION RANGE
- SMALL 14-PIN DIP PACKAGE

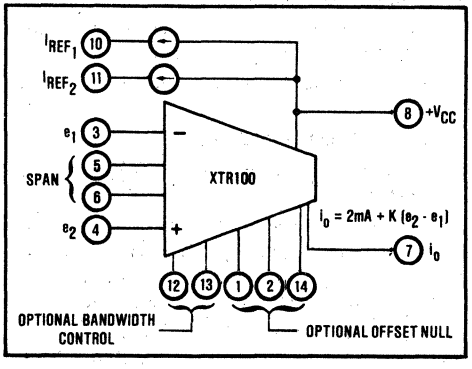
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  - Pressure Transmitters
  - Temperature Transmitters
  - Millivolt Transmitters
- RESISTANCE BRIDGE INPUTS
- THERMOCOUPLE INPUTS
- RTD INPUTS
- CURRENT SHUNT (mV) INPUTS
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR100 is a microcircuit, 4mA to 20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage controlled output current source, and dual-matched precision current references. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTD's, thermistors, and strain gauge bridges. State-of-the art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers. Also, the XTR100 is generally very useful for low noise, current-mode signal transmission.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{CC}$ = 24VDC, R_L = 100Ω unless otherwise noted.

PARAMETER	CONDITIONS/DESIGNATION	XTR100AM/AP MIN	XTR100AM/AP TYP	XTR100AM/AP MAX	XTR100BM/BP MIN	XTR100BM/BP TYP	XTR100BM/BP MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS								
Current	Linear Operating Region	4		20	*		*	mA
Current	Derated Performance	3.8		22	*		*	mA
Current Limit	I_O min		28	38		*	*	mA
Offset Current Error	I_{OS}, I_O = 4mA		±1.5	±4		*	*	µA
Offset Current Error vs Temp.	$\Delta I_{OS}/\Delta T$		±5	±10		*	*	ppm, FS/°C
Full Scale Output Current Error	Full Scale = 20mA			±20			*	µA
Power Supply Rejection		110	135		*	*		dB
Power Supply Voltage	V_{CC}, pins 7 & 8, compliance(1)	+11.6		+40	*		*	VDC
Load Resistance	At V_{CC} = +24V, I_O = 20mA			600			*	Ω
	At V_{CC} = +40V, I_O = 20mA			1400			*	Ω
SPAN								
Equation	R_S in Ω, e_1 and e_2 in V	$i_O = 4mA + [0.016\,\Omega + (40/R_S)](e_2 - e_1)$						
Untrimmed Error(2)	ϵ_{SPAN}	-5	-2.5	0	*	*	*	%
Nonlinearity	$\epsilon_{NONLINEARITY}$			0.01			*	%
Hysteresis			0			*		%
Dead Band			0			*		%
Temperature Effects			30	±100		*	*	ppm %/°C
INPUT CHARACTERISTICS								
Impedance								
Differential			0.4 ‖ 0.047			*		GΩ ‖ µF
Common-Mode			10 ‖ 180			*		GΩ ‖ pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)$(3)	0		1	*		*	V
Offset Voltage	V_{OS}			±50			±25	µV
vs Temperature	$\Delta V_{OS}/\Delta T$		±0.7	±1		±0.25	±0.5	µV/°C
Bias Current	I_B		60	150		*	*	nA
vs Temperature	$\Delta I_B/\Delta T$		0.30	1		*	*	nA/°C
Offset Current	I_{OSI}		10	±30		*	±20	nA
vs Temperature	$\Delta I_{OSI}/\Delta T$		0.1	0.3		*	*	nA/°C
Common-Mode Rejection(4)	DC	90	100		*	*	*	dB
Common-Mode Range	e_1 and e_2 with respect to pin 7	4		6	*		*	V
CURRENT SOURCES								
Magnitude			1			*		mA
Accuracy	V_{CC} = 24V, $V_{PIN\ 8}$ - $V_{PIN\ 10,\ 11}$ = 19V, R_2 = 5kΩ, Fig. 3		±0.03	±0.1		±0.015	±0.05	%
vs Temperature				±30			*	ppm/°C
vs Time			±8			*		ppm/mo.
Ratio Match	Tracking							
Accuracy	1 - I_{REF1}/I_{REF2}		±0.006	±0.02			*	%
vs Temperature				±15			10	ppm/°C
vs Time			±1			*		ppm/mo.
Output Impedance		10	20		*			MΩ
TEMPERATURE RANGE								
Specification		-40		+85	*		*	°C
Operating (AM, BM)		-55		+125	*		*	°C
(AP, BP)		-40		+85	*		*	°C
Storage (AM, BM)		-55		+165	*		*	°C
(AP, BP)		-40		+85	*		*	°C

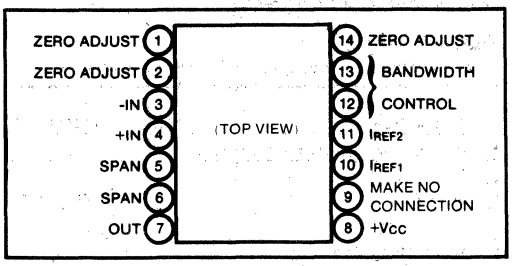
*Same as XTR100AM/AP.

NOTES:
1. See Typical Performance Curves.
2. Span error shown is untrimmed and may be adjusted to zero.
3. e_1 and e_2 are signals on the -IN and +IN terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR100A and XTR100B grades respectively. 2mV FS is also possible with the B grade; but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise.
4. Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Application Information section.

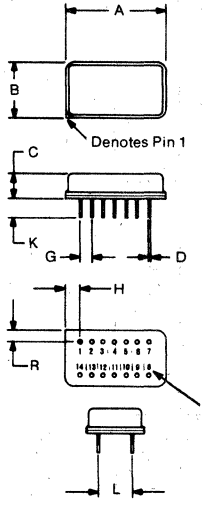
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC}	40V
Input Voltage, e_1, or e_2	≥ V_{OUT}, ≤ +V_{CC}
Storage Temperature Range, metal	-55°C to +165°C
Storage Temperature Range, plastic	-40°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	+165°C

PIN DESIGNATIONS



MECHANICAL



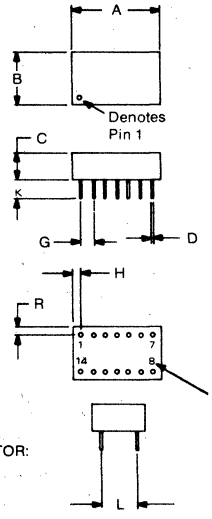
XTR100AM/BM (Metal)

NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Pin numbers shown for reference only. Numbers are not marked on package.

MATING CONNECTOR: 0145MC



XTR100AP/BP (Plastic)

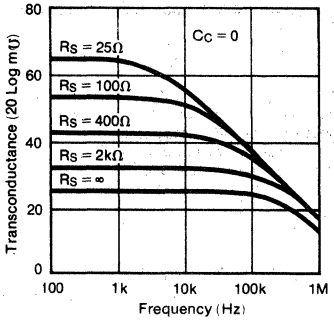
NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

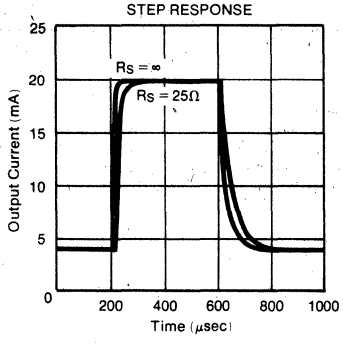
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

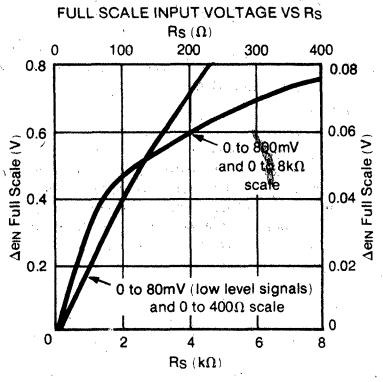
Pin numbers shown for reference only. Numbers are not marked on package.

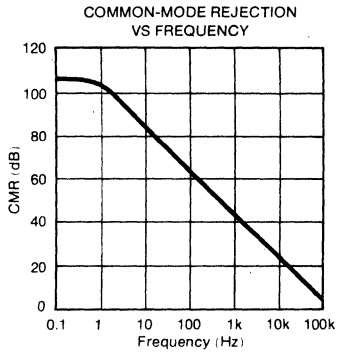
TYPICAL PERFORMANCE CURVES

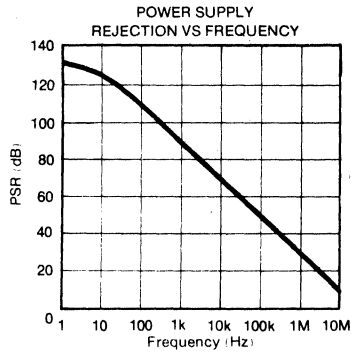
(T_A = +25°C, +V_{CC} = 24VDC unless otherwise noted)

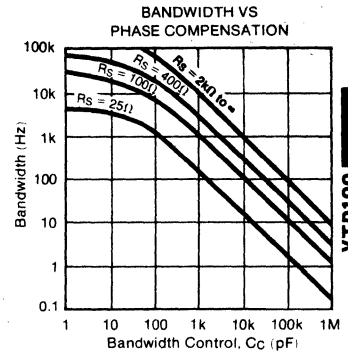


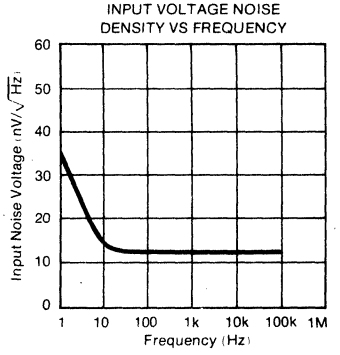


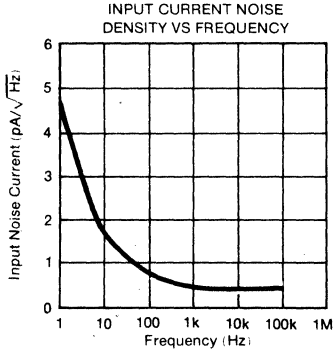


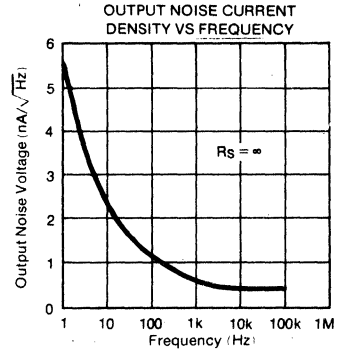












THEORY OF OPERATION

A simplified schematic of the XTR100 is shown in Figure 1. Basically the amplifiers, A_1 and A_2, act as an instrumentation amplifier controlling a current source, A_3 and Q_1. Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S, the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3, to form I_1. The circuit is configured such that I_2 is 19 times I_1. From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0V$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN}. Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., $(0.016\Omega + 40/R_S)(e_{IN}$ full scale$) = 16mA$. Note that since I_O is unipolar e_2 must be kept larger than e_1; i.e., $e_2 \geq e_1$ or $e_{IN} \geq 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

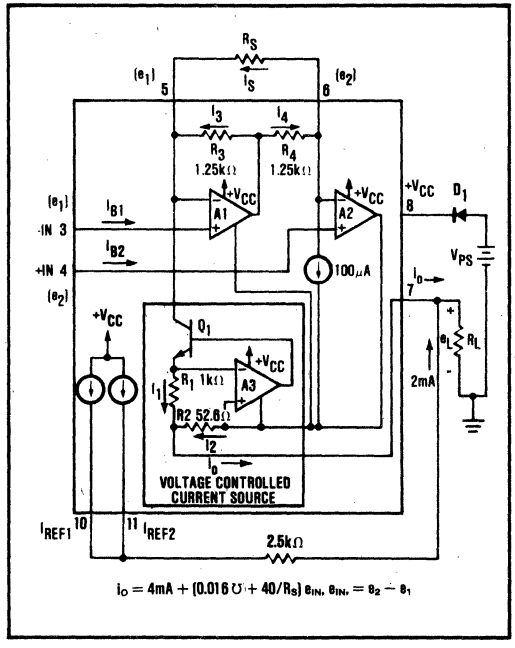


FIGURE 1. Simplified Schematic of the XTR100.

INSTALLATION AND OPERATING INSTRUCTIONS

Major points to consider when designing with the XTR100:

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. $+V_{CC}$ should be bypassed with a $0.01\mu F$ capacitor as close to the unit at possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation
$$+4V \leqslant e_1 \leqslant +6V$$
$$+4V \leqslant e_2 \leqslant +6V$$
(e_1 and e_2 measured with respect to pin 7).
4. The maximum input signal level ($e_{IN_{FS}}$) is 1V with $R_S = \infty$ and proportionally less as R_S decreases.
5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation connect them together and through a $1k\Omega$ resistor to pin 7. Each reference must have between +1V and $+(V_{CC} - 4V)$ with respect to pin 7. Filter with one $0.01\mu F$ or two $0.0047\mu F$ capacitors.
6. Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 ($+V_{CC}$) remains within the 11.6V to 40V range as the output changes between the 4mA to 20mA range (see Figure 2).
7. It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR100 caused by momentary (e.g., transient) or long term application of the wrong polarity of voltage between pins 7 and 8.
8. When the XTR100 is in high gain, use a compensation capacitor, pins 12 and 13, and consider PC board layout which minimizes parasitic capacitance.

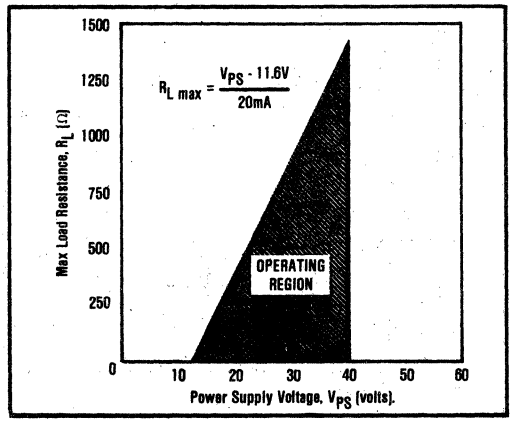


FIGURE 2. Power Supply Operating Range.

SELECTING R_S

R_{SPAN} is chosen so that a given full scale input span $e_{IN_{FS}}$ will result in the desired full scale output span of ΔI_{OFS}, $[(0.016\mho) + (40/R_S)]\ \Delta e_{IN} = \Delta I_O = 16mA$.

Solving for R_S;

$$R_S = \frac{40}{\Delta I_O/\Delta e - 0.016\mho} \qquad (1)$$

For example, if $\Delta e_{IN_{FS}} = 100mV$ for $\Delta I_{O_{FS}} = 16mA$

$$R_S = \frac{40}{(16mA/100mV)} = \frac{40}{0.16 - 0.016} = \frac{40}{0.144} = 278\Omega$$

See Typical Performance Curves for a plot of R_S vs $\Delta e_{IN_{FS}}$. Note that in order not to exceed the 20mA upper range limit e_{IN} must be less than 1V when $R_S = \infty$ and proportionately smaller as R_S decreases.

BIASING THE INPUTS

The internal circuitry of the XTR100 is such that both e_1 and e_2 must be kept approximately 5V above the voltage at pin 7. This is easily done by using one or both current sources and an external resistor R_2. Figure 3 shows the simplest case - a floating voltage source e'_2. The 2mA from the current sources flows through the $2.5k\Omega$ value of R_2 and both e_1 and e_2 are raised by the required 5V with respect to pin 7. For linear operation the constraint is

$$+4V \leqslant e_1 \leqslant +6V$$
$$+4V \leqslant e_2 \leqslant +6V$$

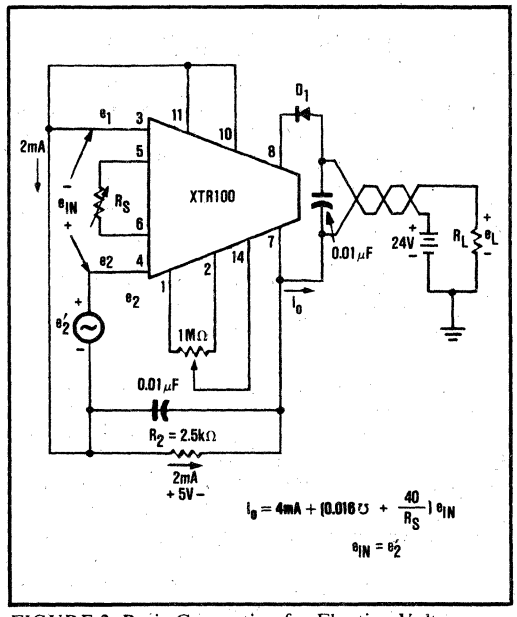


FIGURE 3. Basic Connection for Floating Voltage Source.

Figure 4 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources.

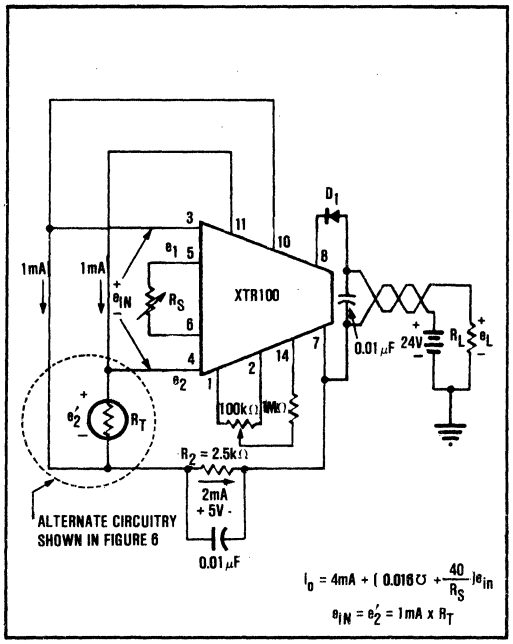


FIGURE 4. Basic Connection for Resistive Source.

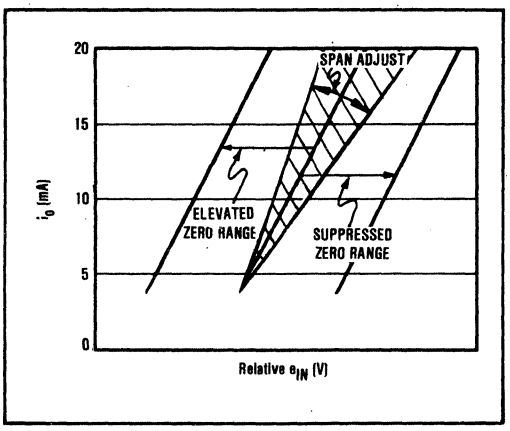


FIGURE 5. Elevation and Suppression Graph.

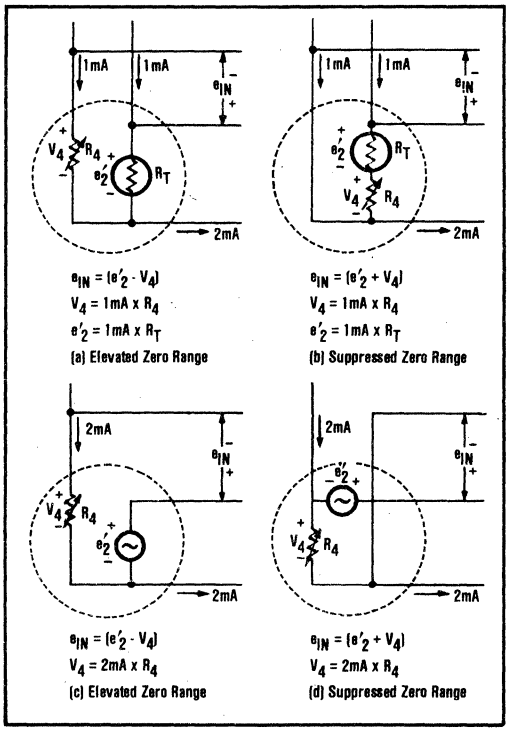


FIGURE 6. Elevation and Suppression Circuits.

CMV AND CMR

Thus the XTR100 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications. If the inputs are biased at some other CMV then an input offset error term is (CMV - 5)/CMRR; CMR is in dB, CMRR is in V/V.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR100 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 5 and 6(a). In this example the sensor voltage is derived from R_T (a thermistor, RTD or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 6(b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2, and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20μV) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by ±0.3μV/°C per 100μV of induced offset.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR100 ideal for a variety of two-wire transmitter applications. It can be used by OEM's producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise

interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR100 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1 - RTD Transducer shown in Figure 7. Given a process with temperature limits of +25°C and +150°C, configure the XTR100 to measure the temperature with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

Computing R_S.

The sensitivity of the RTD is $\Delta R/\Delta T = 100\Omega/266°C$. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span) the span of e_{IN} is 1mA x (100Ω/266°C) x 125°C = 47mV = Δe_{IN}.

$$\text{From equation 1, } R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{in}} - 0.016\,\mho}$$

$$R_S = \frac{40}{\frac{16mA}{47mV} - 0.016\,\mho} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S.

Computing R_4:

$$\text{At 25°C, } e'_2 = 1mA \times [100\Omega + (\frac{100\Omega}{266°C} \times 25°C)]$$
$$= 1mA \times 109.4\Omega$$
$$= 109.4mV$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA the input circuitry shown in Figure 7 is used.

e_{IN} is made 0 at 25°C
or $e'_{2\,25°C} - V_4 = 0$
thus, $V_4 = e'_{2\,25°C} = 109.4mV$

$$R_4 = \frac{V_4}{1mA} = \frac{109.4mV}{1mA} = 109.4\Omega$$

Computing R_2 and checking CMV:

At 25°C, $e'_2 = 109.4mV$

$$\text{At 150°C, } e'_2 = 1mA \times [100\Omega + (\frac{100\Omega}{266°C} \times 150°C)]$$
$$= 156.4mV$$

Since both e'_2 and V_4 are small relative to the desired 5V common-mode voltage they may be ignored in computing R_2 as long as the CMV is met.

$R_2 = 5V/2mA = 2.5k\Omega$

e_2 min = 5V + 0.1094V
e_2 max = 5V + 0.1564V
e_1 = 5V + 0.1094V

The +4V to +6V CMV requirement is met.

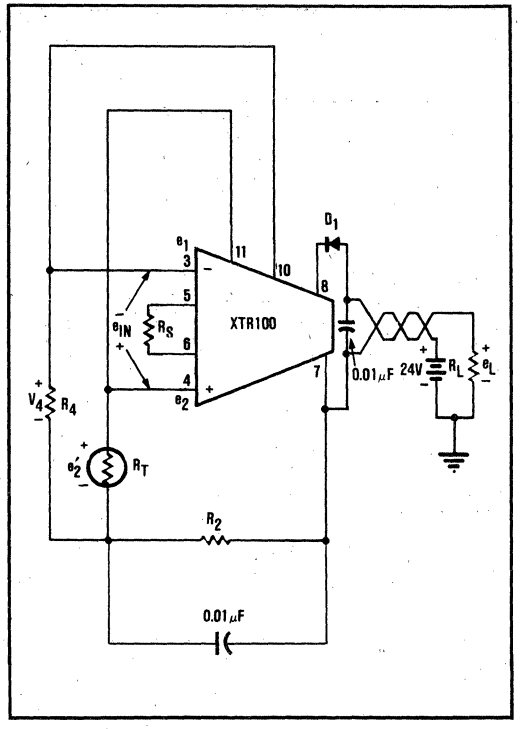


FIGURE 7. Circuit for Example 1.

EXAMPLE 2 - Thermocouple Transducer shown in Figure 8. Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the XTR100 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, V_{R6}, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of +25°C this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2.

Establishing R_S:

The input full scale span is 58mV ($\Delta e_{IN_{FS}} = 58mV$).

R_S is found from equation (1)

$$R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{IN}} - 0.016\,\mho}$$

$$= \frac{40}{\frac{16mA}{58mV} - 0.016\,\mho} = \frac{40}{0.2599}$$

$$R_S = 153.9\Omega$$

Selecting R_4:

R_4 is chosen to make the output 4mA at $T_{TC} = 0°C$ ($V_{TC} = -1.28mV$) and $T_D = 25°C$ ($V_D = 0.6V$). A circuit is shown in Figure 8.

V_{TC} will be -1.28mV when $T_{TC} = 0°C$ and the reference junction is at +25°C. e_1 must be computed for the condition of $T_D = +25°C$ to make $e_{IN} = 0V$.

$V_{D_{25°C}} = 600mV.$

$e_{1_{25°C}} = 600mV \times 51/2051 = 14.9mV$

$e_{IN} = e_2 - e_1 = + V_{TC} + V_4 - e_1$

with $e_{IN} = 0$ and $V_{TC} = -1.28mV$

$V_4 = e'_1 + e_{IN} - V_{TC} = 14.9mV + 0V - (-1.28mV)$

$1mA \times R_4 = 16.18mV$

$R_4 = 16.18\Omega$

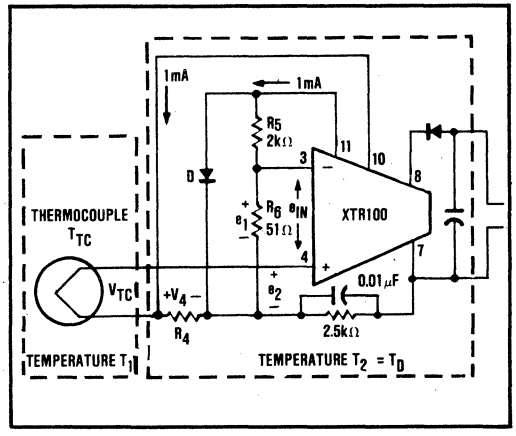


FIGURE 8. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

Cold Junction Compensation:

The temperature reference circuit is shown in Figure 9.

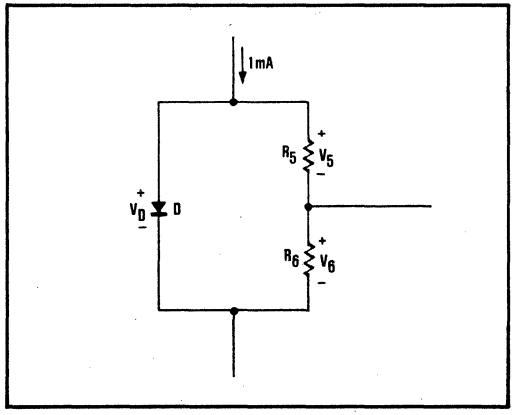


FIGURE 9. Cold Junction Compensation Circuit.

The diode voltage has the form

$$V_D = \frac{KT}{q} \ln \frac{I_{DIODE}}{I_{SAT}}$$

Typically at $T_2 = 25°C$, $V_D = 0.6V$ and $\Delta V_D/\Delta T = -2mV/°C$. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta V_D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At 25°C this is approximately $52\mu V/°C$ (obtained from standard thermocouple table) therefore,

$$\Delta V_{TC}/\Delta T = \Delta V_D/\Delta T \left(\frac{R_6}{R_5 + R_6}\right) \qquad (2)$$

$$52\mu V/°C = 2000\mu V/°C \left(\frac{R_6}{R_5 + R_6}\right)$$

R_5 is chosen as $2k\Omega$ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω.

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when the thermocouple impedance goes very high. The circuits of Figures 14 and 15 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the +input (large impedance) will cause I_O to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 16 should be used. When the TC opens the output will go to its upper range limit value (about 25mA or higher).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR100 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltage ($25\mu V$ max for the B grade, $50\mu V$ max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2, and 14 as shown in Figures 3 and 4. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommmended where possible and can be done by either one of two techniques shown in Figure 10. C_2 connect to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by,

$$f_{CO} = \frac{1.59 \times 10}{(R_1 + R_2 + R_3 + R_4)(C_2 + 0.047\mu F)}$$

with f_{CO} in Hz, all R_S in Ω and C_2 in μF. This method has the disadvantage of having f_{CO} vary with R_1, R_2, R_3, R_4, and it may require large values of R_3 and R_4. The other method, using C_1 will use smaller values of capacitance and is not a function of the input resistors. It is however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{CO} is shown in the Typical Performance Curves.

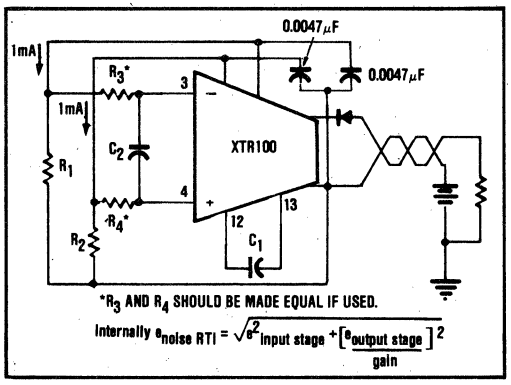


FIGURE 10. Optional Filtering.

APPLICATION CIRCUITS

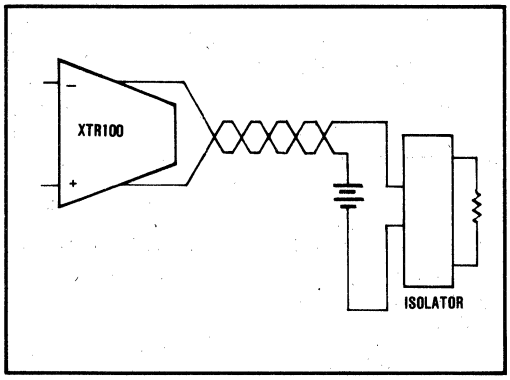


FIGURE 11. XTR100 with Loop-powered Isolation.

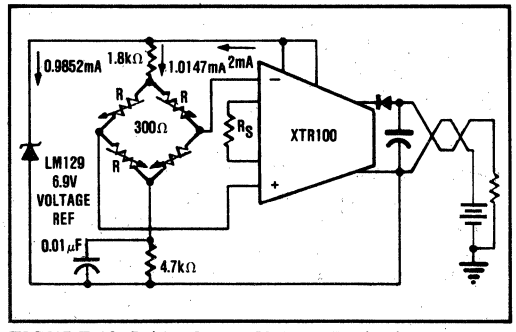


FIGURE 12. Bridge Input, Voltage Excitation.

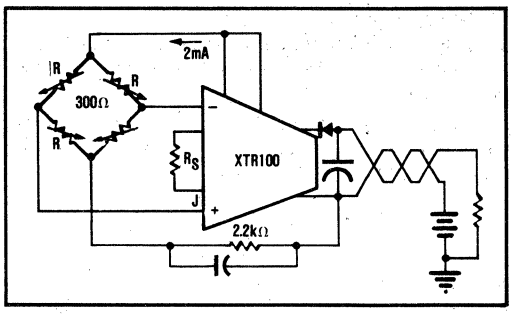


FIGURE 13. Bridge Input, Current Excitation.

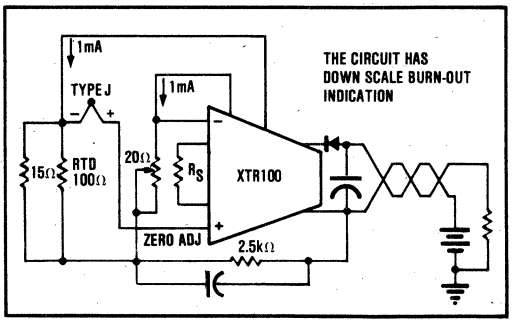


FIGURE 14. Thermocouple Input with RTD Cold Junction Compensation.

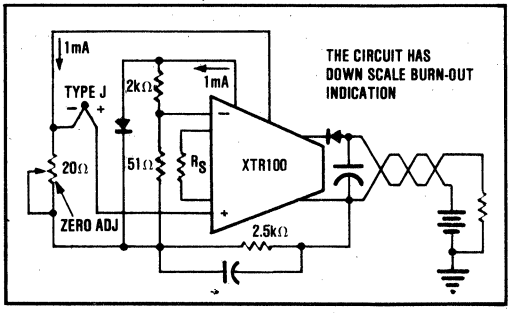


FIGURE 15. Thermocouple Input with Diode Cold Junction Compensation.

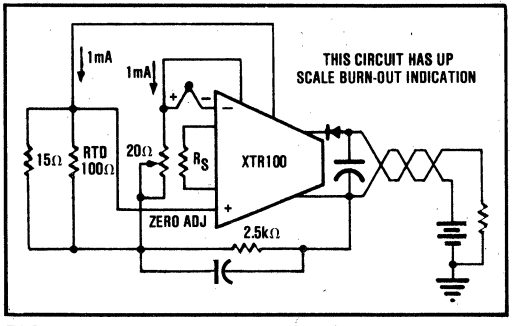


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

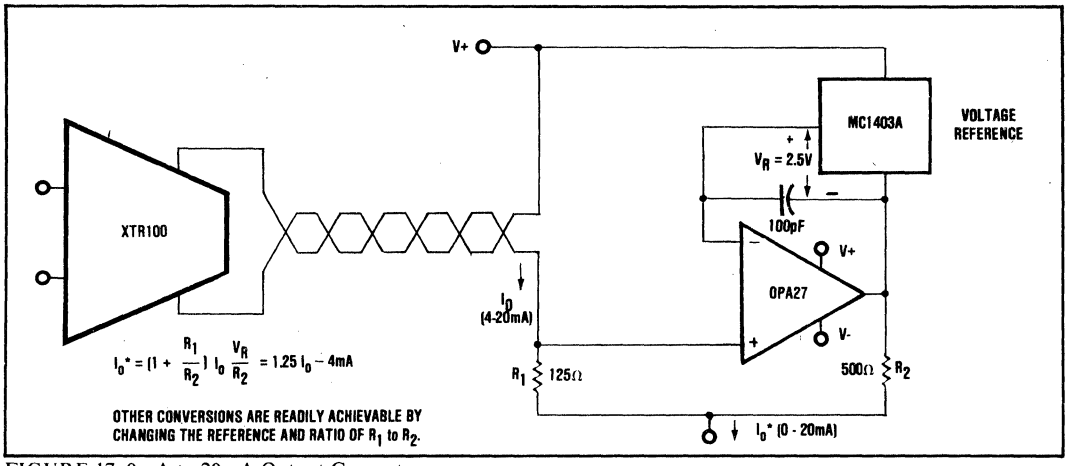


FIGURE 17. 0mA to 20mA Output Converter.

DETAILED ERROR ANALYSIS

The ideal output current is

$$i_{O\ IDEAL} = 4mA + K\ e_{IN} \quad (3)$$

K is the span (gain) term, $(0.016mA/mV) + (40/R_S)$

The nature of the XTR100 circuit is such that there are three major components of error.

σ_O = error associated with the output stage.
σ_S = errors associated with span adjustment.
σ_I = errors associated with input stage.

The transfer function including these errors is

$$I_{O\ ACTUAL} = (4mA + \sigma_O) + K\ (1 + \sigma_S)(e_{IN} + \sigma_I) \quad (4)$$

When this expression is expanded, second order terms ($\sigma_S\ \sigma_I$) dropped, and terms collected, the result is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ e_{IN} \text{ "} K\sigma_I + K\sigma_S\ e_{IN} \quad (5)$$

The error in the output current is $i_{O\ ACTUAL} - i_{O\ IDEAL}$ and can be found by subtracting equations (5) and (3).

$$i_{O\ ERROR} = \sigma_O + K\sigma_S + K\ \sigma_S\ e_{IN} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR100 and the particular circuit in which it is applied. The circuit of Figure 7 will be used to illustrate the principles.

$$\sigma_O = I_{OS_{RTO}} \quad (7)$$

$I_{OS_{RTO}}$* = the output offset error current.

For the circuit of Figure 7,

$$\sigma_I = V_{OSI} + [I_{B1}\ R_T - I_{B2}\ R_4] + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR} \quad (8)$$

The term in brackets maybe written in terms of offset current and resistor mismatches as $I_{B1}\ \Delta R + I_{OS}\ R_4$.

V_{OSI}* = input offset voltage
I_{B1},* I_{B2}* = input bias current
I_{OSI}* = input offset current
$\Delta R = R_T - R_4$ = mismatch in resistor
ΔV_{CC} = change supply voltage between pins 7 and 8 away from 24V nomimal
PSRR* = power supply rejection ratio
CMRR* = common-mode rejection ratio

$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$
ϵ_{NONLIN}* = span nonlinearity
ϵ_{SPAN}* = span equation error. Untrimmed error = 3% max. May be trimmed to zero.

*Items marked with an asterisk (*) can be found in the Electrical Specifications.

EXAMPLE 3

Given the circuit in Figure 7 with the XTR100B specifications and the following conditions: $R_T = 109.4\Omega$ at 25°C, $R_T = 156.4\Omega$ at 150°C, $I_o = 4mA$ at 25°C, $I_o = 20mA$ at 150°C, $R_S = 123.3\Omega$, $R_4 = 109\Omega$, $R_L = 250\Omega$, $R_{LINE} = 100\Omega$, $V_{D1} = 0.6V$, $V_{PS} = 24V \pm 0.5\%$. Determine the % error at the upper and lower range values.

A. At the lower range value (T = 25°C).

$$\sigma_O = I_{OS_{RTO}} = \pm 4\mu A$$

$$\sigma_I = V_{OSI} + [I_{B1}\ \Delta R + I_{OSI}\ R_4] + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5}{CMRR}$$

$$\Delta R = R_{T_{25°C}} - R_4 = 109.4 - 109 \approx 0$$

$\Delta V_{CC} = 24 \times 0.005 + 4mA\ (250\Omega + 100\Omega) + 0.6V$
$= 120mV + 1400mV + 600mV = 2120mV$
$e_1 = (2mA \times 2.5k\Omega) + (1mA \times 109\Omega) = 5.109V$
$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 109.4\Omega) = 5.1094V$
$(e_1 + e_2)/2 - 5 \approx 0$
PSRR = 3.16×10^5 for 110dB
CMRR = 31.6×10^3 for 90dB

$$\sigma_I = 25\mu V + (150nA \times 0 + 30nA \times 109\Omega) \quad (9)$$

$$+ \frac{2120mV}{3.16 \times 10^5} + \frac{0}{31.6 \times 10^3}$$

$$= 25\mu V + 3.27\mu V + 6.7\mu V + 0$$
$$= 34.97$$

$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$
$= 0.0001 + 0$ (assumes trim of R_S)
i_O error $= \sigma_O + K\,\sigma_I + K\,\sigma_S\,e_{IN}$

$$K = 0.016 + \frac{40}{R_S} = 0.016 + \frac{40}{123.3\Omega} = 0.341\,\mho$$

$e_{IN} = e_2 - V_4 = I_{REF1}\,R_{T_{25°C}} - I_{REF2}\,R_4$
since $R_{T\ 25°C} = R_4$
$e_{IN} = (I_{REF1} - I_{REF2})\,R_4 = 0.1\mu A \times 109\Omega = 10.9\mu V$

Since the maximum mismatch of the current references is 0.01% of 1mA = 0.1μA

i_O error $= 4\mu A + (0.34\,\mho \times 34.97) + (0.341 \times 0.0001)$
$\times\ 10.9\mu V = 4\mu A + 11.89\mu A + 0.0004\mu A = 15.89\mu A$

$$\%\ \text{error} = \frac{15.89}{4mA} \times 100\% = 0.4\%$$ at lower range value.

B. At the upper range value (T = 150°C)

$\Delta R = R_{T\ 150°C} - R_4 = 156.4 - 109.4 = 47\Omega$
$\Delta V_{CC} = 24 \times 0.005 + 20mA\,(250\Omega + 100\Omega) + 0.6$
$= 7720mV$
$e_1 = 5.109V$
$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 156.4\Omega) = 5.156V$
$(e_1\ e_2)/2 - 5V \approx 0$
$\Delta R = -R_{T\ 150°C} + R_4 = 156.4 - 109 = 47\Omega$
$\sigma_O = 4\mu A$
$\sigma_I = 25\mu V + (150nA \times 47\Omega + 30nA \times 109\Omega)$

$$+ \frac{7720mV}{3.16 \times 10^5} + \frac{0}{31.6 \times 10^3}$$

$= 25\mu V + 10.33\mu V + 24\mu V$ F0 $= 59.33\mu V$
$\sigma_S = 0.0001$
$e_{IN} = e_2' - V_4 = I_{REF1}\,R_{T\ 150°C} - I_{REF2}\,R_4$
$= (1mA \times 156.4\Omega) - (1mA - 109\Omega)$
$= 47mV.$

$i_{O\ ERROR} = \sigma_O + K\,\sigma_I + K\,\sigma_S \times e_{IN}$ (10)
$= 4\mu A + 0.341\,\mho \times 59.33\mu V + 0.341\,\mho \times$
$0.0001 \times 47000\mu V$
$= 4 \times 20.23 + 1.6 = 25.83\mu A$

$$\%\ \text{error} = \frac{25.83\mu A}{20mA} \times 100\% = 0.13\%$$ at upper range value or % of FS.

CONCLUSIONS

From equation (9) it is observed that the predominant error term is the input offset voltage (25μV for the B grade). This is of little consequence in many applications. $V_{OS\ RTI}$ can, however, be nulled using the pot shown in Figures 3 and 4. From equation (10), the predominant errors are $I_{OS\ RTI}$ (4μA), $V_{OS\ RTI}$ (25μV), and I_B (150nA), max, B grade.

A NOTE FOR HIGH GAIN APPLICATIONS

In applications where e_{in} full scale is small (<50mV) and R_{span} is small (<≈150Ω), caution should be taken to consider errors from the external span circuit plus high amplification of offset drift and noise.

In such applications, be sure to include the effect of the normal thermal feedback within the XTR100 package. Small additional errors occur from a change in input offset voltage and current due to a change in chip temperature resulting from a change in output current (4mA up to 20mA).

The XTR100 has two thermal resistance specifications:

$\theta_{JA} = 115°C$

This is the thermal resistance from output transistor to ambient. It is used for normal power dissipation considerations (see Figure 18).

$\theta_{JI} = 60°C/W$

This is the thermal resistance which describes the effect of output stage power dissipation in input stage temperature rise.

As an example of how θ_{JI} would be applied, we will calculate the limits with $V_{PS} = 40V$ and $R_L = 250\Omega$.

Power Dissipation:

at 20mA output: $20mA\,[40V - (20mA \times 250\Omega)] = 700mW$
at 4mA output: $4mA\,[40V - (4mA \times 250\Omega)] - 156mW$

Thermal Resistance: $\theta_{JI} = 60°C/W$

Input Stage Temperature Rise:

at 20mA output: $700mW \times 60°C/W = 42°C$
at 4mA output: $156mW \times 60°C/W = 9.4°C$

Thus under these conditions when the output changes from 4mA to 20mA the input stage temperature changes 42°C − 9.4°C = 32.6°C. The maximum input stage offset change will depend on the particular grade specification:

A Grade (1μV/°C max) = 32.6μV
B Grade (0.5μV/°C max) = 16.3μV

The amount of error that this offset voltage represents depends on how large the full scale input voltage is. It is worse, of course, for small input voltages. Table I shows the error as a percentage of full scale and in terms of output current (% FS error × 16mA FS output span).

TABLE I. Maximum Errors Due to Thermal Feedback
$V_{PS} = 40V$, $R_L = 250\Omega$.

	10mV FS	100mV FS	1V FS
A Grade	0.326% (52.2μA)	0.0326% (5.22μA)	0.0033% (0.522μA)
B Grade	0.163% (26.1μA)	0.0163% (2.61μA)	0.0016% (0.261μA)

HOW TO REDUCE ERRORS

Lower V_{PS}

The errors can be reduced by lowering the voltage at the XTR100 line terminals. The errors in the example above represent a fairly demanding condition of maximum voltage ($V_{PS} = 40V$) and minimum resistance ($R_L = 250\Omega$). If the voltage is lowered to 24V, then a 4mA to 20mA output change causes a change in input stage temperature of 17.3°C and the errors in Table I are reduced by a factor of 17.3°C/32.6°C = 0.53. (Note that this is different than the decrease in the voltage itself: 24/40 = 0.6.)

Raise Resistance

If the load or line resistance is raised the output power dissipation will also be reduced. If $R_L = 400\Omega$ (400/250 = 1.6), the change in output temperature is 29.2°C as the output changes from 4mA to 20mA (still with V_{PS} = 40V) and the errors in Table I are reduced by a factor of 29.2°C/32.6°C = 0.9.

Heat Sink

Heat sinking the package will reduce both θ_{JA} and θ_{JI}. The following is information on small-finned heat sinks that are attached with an epoxy heat sink adhesive (AHAM-985). The three models are 0.75″ × 0.4″ × 0.21″.

Model 141
AHAM
27901 Front St.
Rancho, CA 92390
(714) 676-4151

Models 141 and 142
Heat Sink Plus
28715 Via Montezuma
Temecula, CA 92390
(714) 676-3031

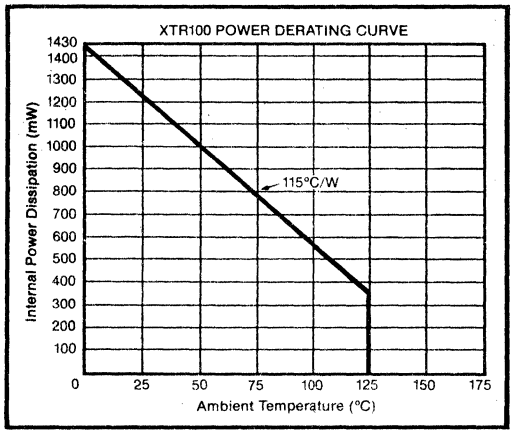


FIGURE 18. Power Derating Curve.

GENERAL RECOMMENDATIONS HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove the static-generating materials, such as untreated plastics, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% is recommended).

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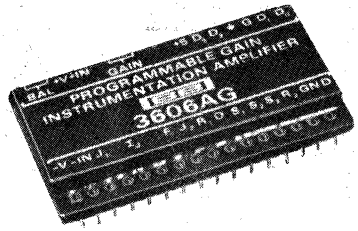
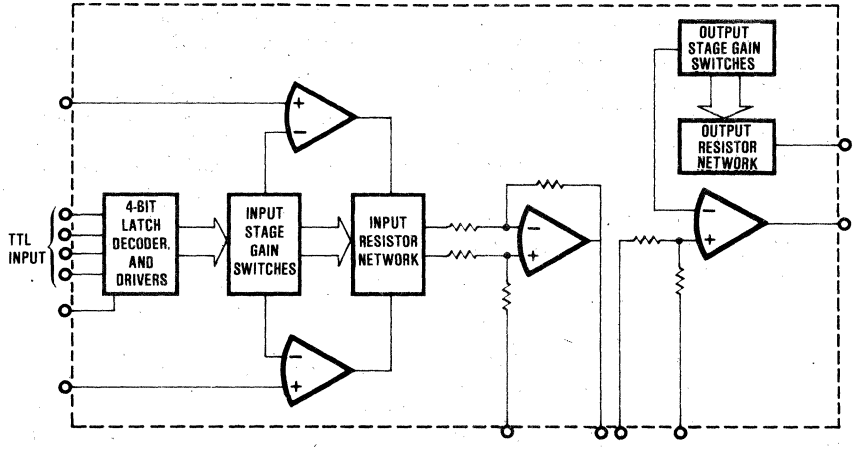


3606

Digitally Controlled Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- 11 BINARY GAINS - 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024V/V
- 4-BIT TTL GAIN CONTROL
- EXCELLENT GAIN NONLINEARITY 0.01% max at G = 1024V/V
- LOW GAIN ERRORS - 0.02% max
- LOW GAIN DRIFT - 10ppm/°C max
- LOW VOLTAGE DRIFT 1μV/°C max RTI, G = 1024V/V
- HIGH CMR - 110dB min, G = 1024V/V
- HIGH INPUT IMPEDANCE - 10 x $10^9\Omega$
- LOW OFFSET VOLTAGE 22μV max RTI, G = 1024V/V 2mV max RTI, G = 1V/V



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

The 3606 is a self-contained, Programmable Gain Instrumentation Amplifier (PGIA) whose gain can be changed in 11 binary weighted steps from 1 to 1024V/V. The gain control is accomplished through a 4-bit TTL input.

The PGIA function allows the user to deal with wide dynamic range signals while maintaining high system resolution. For example: when used with a 10-bit A to D converter in a "floating point" system, the 2^{10} gain range of the 3606, plus the 2^{10} range of the converter produces a total system resolution of 2^{20} (|| 1,000,000:1).

Desirable characteristics of a high performance instrumentation amplifier are offered by the 3606: high input impedance (10GΩ), excellent gain nonlinearity (0.01% max, G = 1024V/V; 0.02% max, G = 1V/V), high common-mode rejection (100dB min, G≥ 4V/V), low gain error (0.02% max with no trimming required), low gain temperature coefficient (10ppm/°C max), and low offset voltage drift vs temperature (1μV/°C max, RTI, G = 1024).

Added to these outstanding instrumentation amplifier characteristics is the ability to change 3606's gain under control of a 4-bit TTL input word. An important characteristic of the 3606 PGIA is its low change in offset plus laser trimming minimized this change to a maximum of ±25mV with no external adjustments. With two simple offset adjustments the change can be limited to less than 2mV (1mV typ) at the output over the entire 1V/V to 1024V/V gain range.

A simplified schematic of the 3606 is shown in Figure 1. The circuit consists of a variable gain high input impedance voltage follower input stage (A1 and A2) followed by a unity gain difference amplifier (A3) with a variable gain output stage (A4).

Common-mode voltage is derived for active guard drive to improve system common-mode rejection. Two-pole, low-pass filtering can easily be implemented on the output stage to reduce noise bandwidth and improve system signal-to-noise operation. A latch function is provided to inhibit gain changes while the digital gain control input is changed.

Burr-Brown's instrumentation grade monolithic operational amplifiers, high stability precision thin-film resistor networks and advanced laser-trimming techniques are used by the 3606 to achieve a performance, size and cost combination never before achieved in a PGIA. It is available in a 32-pin dual-in-line package in either ceramic or metal (hermetic) configurations.

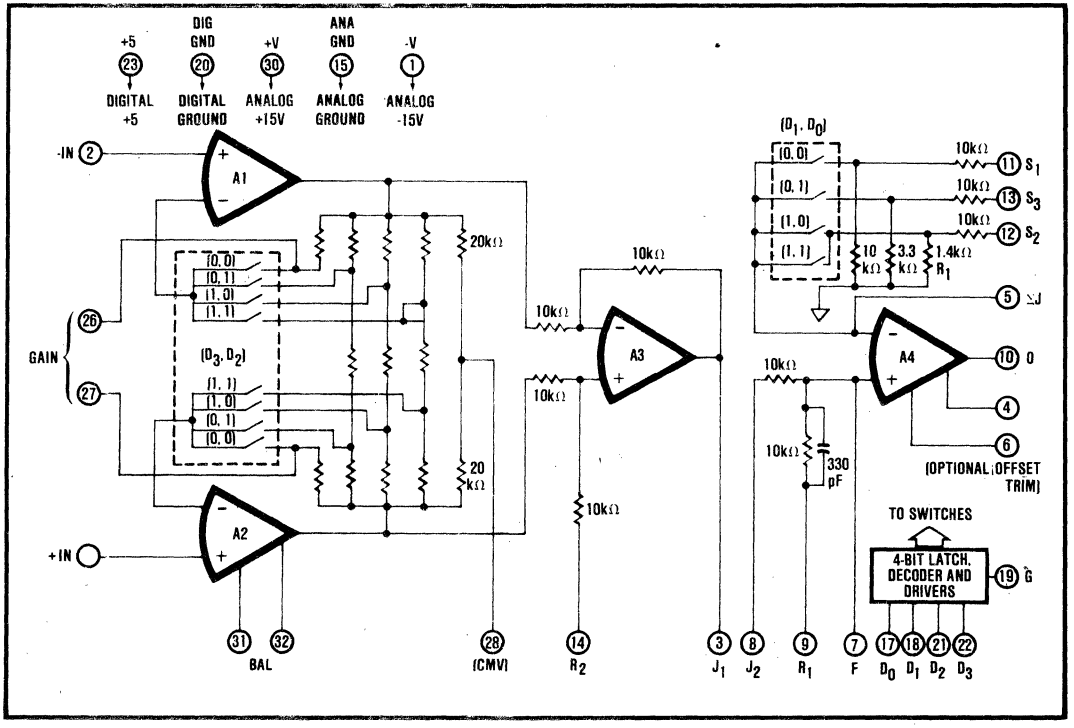


FIGURE 1. Simplified Schematic.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	3606A[1] MIN	3606A[1] TYP	3606A[1] MAX	3606B[1] MIN	3606B[1] TYP	3606B[1] MAX	UNITS
GAIN, G[2]								
Inaccuracy	G = 1 to 1024, I_O = 1mA		±0.02	±0.05		±0.01	±0.02	%
Nonlinearity[3]	G = 1 to 16		0.001	0.002		*	*	%[5]
	G = 32 to 128		0.003	0.004		*	*	%
	G = 256 to 1024		0.005	0.01		*	*	%
Drift vs Temperature	G = 1 to 1024		±5	±10		*	*	ppm/°C
vs Time	G = 1 to 1024		±0.01					%/1000 hrs
RATED OUTPUT								
Voltage	I_O = ±5mA	±10	±12		*	*		V
Current	V_O = ±10V	±5	±10		*	*		mA
Impedance			0.05			*		Ω
INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			±V_{CC}			*	V
Common-Mode Voltage Range	Linear operation	±10	±10.5		*	*		V
Differential Impedance			10 || 3			*		10^9Ω || pF
Common-Mode Impedance			10 || 3			*		10^9Ω || pF
OFFSET VOLTAGE, RTO[4]								
Initial at +25°C[5]			±(0.02G +1)	±(0.04G +2)		±(0.01G +1)	±(0.02G +2)	mV
vs Temperature	-25°C to +85°C		±0.0015G ±0.03G_2	±0.003G ±0.05G_2		±0.0005G ±0.01G_2	±0.001G ±0.02G_2	mV/°C
vs Time			±0.001G ±0.01G_2			*		mV/mo
vs Supply			±0.002G ±0.04G_2			*		mV/V
vs Gain[6]	With trimming		±1	±2		*	*	mV
INPUT BIAS CURRENT								
Initial	+25°C		±15	±50		±5	±20	nA
vs Temperature	-25°C to +85°C		±0.3			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	+25°C		±15	±50		±5	±20	nA
vs Temperature	−25°C to +85°C		±0.5			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT NOISE								
Voltage	R_{SOURCE} ≤ 5kΩ							
0.01Hz to 10Hz	G = 1024		1.4			*		μV, p-p
10Hz to 1kHz			1.0			*		μV, rms
Current								
0.01Hz to 10Hz			70			*		pA, p-p
10Hz to 1kHz			20			*		pA, rms
COMMON-MODE REJECTION								
DC, 1kΩ Source Imbalance								
G = 1, 2		80	90		90	100		dB
G = 4 to 6		90	100		100	110		dB
G = 32 to 1024		100	114		110	114		dB
60Hz, 1kΩ Source Imbalance								
G = 1, 2		80	86		*	*		dB
G = 4 to 16		90	96		*	*		dB
G = 32 to 1024		100	106		*	*		dB
DYNAMIC RESPONSE								
±3dB Response	Small Signal							kHz
G = 1			100			*		kHz
G = 32 to 128			40			*		kHz
G = 256 to 1024			10			*		kHz
±1% Response	Small Signal							
G = 1			40			*		kHz
G = 32 to 128			8			*		kHz
G = 256 to 1024			3			*		kHz
Slew Rate	G = 1	0.2	0.5		*	*		V/μsec
Settling Time	G = 128							
to 1%			75			*		μsec
to 0.1%			100			*		μsec
to 0.01%			200			*		μsec

ELECTRICAL (CONT)

Typical at +25°C, unless otherwise noted.

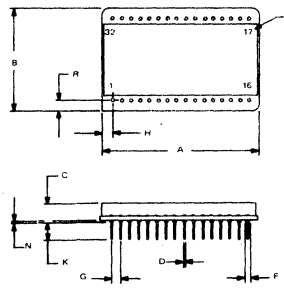
PARAMETER	CONDITIONS	3606A[1] MIN	3606A[1] TYP	3606A[1] MAX	3606B[1] MIN	3606B[1] TYP	3606B[1] MAX	UNITS
LOGIC VOLTAGES								
"0" Level[7]			0	+0.4		*	*	V
"1" Level[7]		+2.4	+5.0		*	*		V
Absolute Max	No damage			+7			*	V
ANALOG SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range, Derated Performance		±8		±18	*		*	VDC
Current, quiescent			±10	±20		*	*	mA
DIGITAL SUPPLY								
Rated Voltage			+5			*		VDC
Voltage Range		+4.5		+5.5	*		*	VDC
Current, quiescent			10			*		mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Storage		-40		+100	*		*	°C

*Specifications same as 3606A.

NOTES:
1. Specify 3606AG or 3606BG for ceramic package and 3606AM or 3606BM for metal package—see below.
2. $G = G_1 \times G_2$.
3. Nonlinearity is the maximum peak deviation from the best straight-line as a percent of full scale peak-to-peak output.
4. RTO = Referred To Output. May be referred to input by dividing by gain G.
5. May be adjusted to zero.
6. Trimmed according to Figure 8.
7. All digital inputs are 1 TTL unit load.

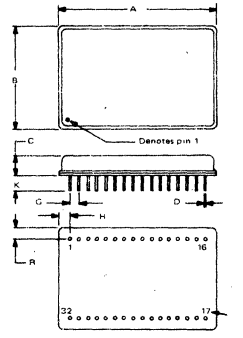
MECHANICAL

"G" PACKAGE



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.060	0.89	1.27
G	100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

"M" PACKAGE



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

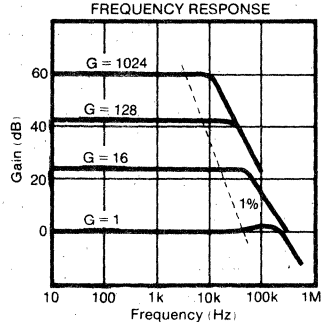
PIN DESIGNATIONS

PIN NO.	DESIG.	FUNCTION	PIN NO.	DESIG.	FUNCTION
1	-V	-15V Analog Supply	17	D_0	Digital Input, LSB
2	-IN	Inverting Input	18	D_1	Digital Input, next LSB
3	J_1	Output of A_3	19	G	Latch
4	(None)	Optional A_4 Offset Trim	20	DIG GND	Digital Ground
5	ΣJ	Summing Junction of A_4	21	D_2	Digital Input, next MSB
6	(None)	Optional A_4 Offset Trim	22	D_3	Digital Input, MSB
7	F	Low-Pass Filter Pin	23	+5	+5 Digital Supply
8	J_2	Input to A_4	24	(None)	No Internal Connection
9	R_1	Output Reference	25	(None)	No Internal Connection
10	O	Output	26	Gain	Optional External Gain
11	S_1	Sense G = 1	27	Gain	Optional External Gain
12	S_2	Sense G = 4	28	(None)	Input CMV
13	S_3	Sense G = 2	29	+IN	Noninverting Input
14	R_2	Output Reference	30	+V	+15V Analog Supply
15	ANA GND	Analog Ground	31	BAL	Optional Input Stage
16	(None)	No Internal Connection	32	BAL	Offset Null

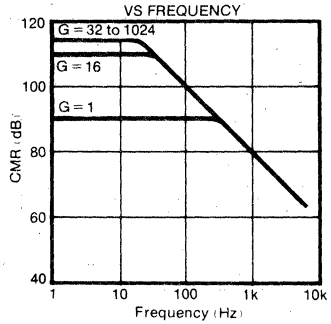
TYPICAL PERFORMANCE CURVES

Typical at +25°C unless otherwise noted.

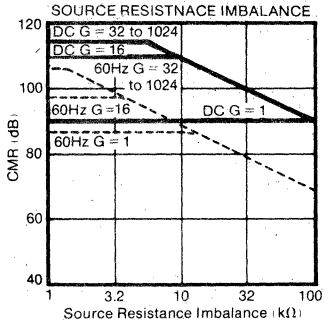
SMALL SIGNAL FREQUENCY RESPONSE



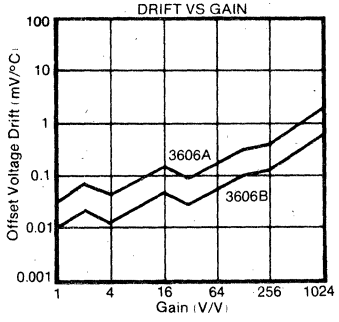
COMMON-MODE REJECTION VS FREQUENCY



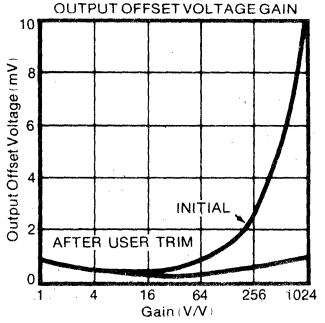
COMMON-MODE REJECTION VS SOURCE RESISTNACE IMBALANCE



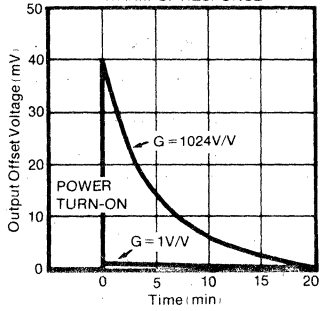
OUTPUT OFFSET VOLTAGE DRIFT VS GAIN



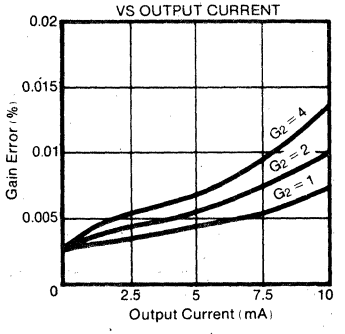
OUTPUT OFFSET VOLTAGE GAIN



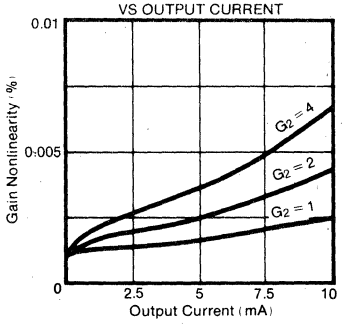
WARM-UP RESPONSE



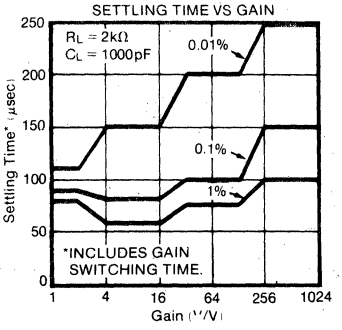
OUTPUT STAGE GAIN ERROR VS OUTPUT CURRENT



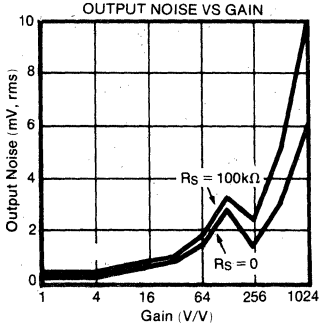
OUTPUT STAGE GAIN NONLINEARITY VS OUTPUT CURRENT



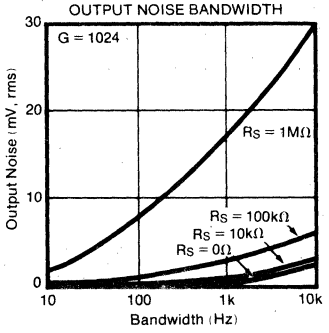
SETTLING TIME VS GAIN



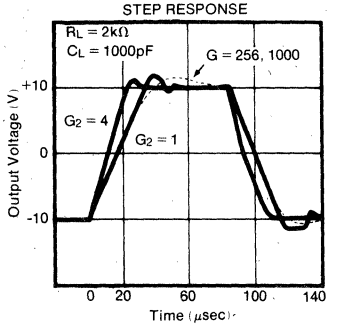
WIDEBAND OUTPUT NOISE VS GAIN



OUTPUT NOISE BANDWIDTH



STEP RESPONSE



INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Figure 2 shows the proper analog and digital power supply connections. The analog supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. Because the amplifier is direct-coupled it must have a ground return path for the bias currents associated with the amplifier inputs at pins 2 and 29. If the ground return path is not inherent in the signal source (floating source) it must be provided externally. The ground return resistance (R_{GR}) should be kept as low as practical. An upper limit of approximately 50MΩ is established by the input bias currents of the amplifier and its common-mode voltage.

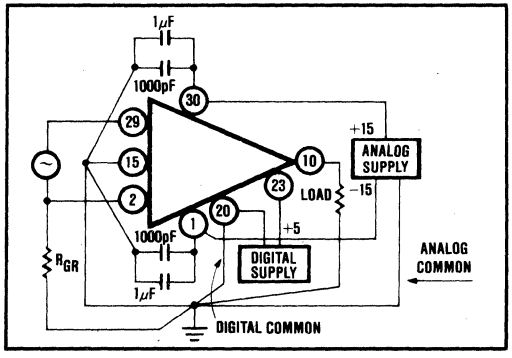


FIGURE 2. Power Supply and Ground Connections.

SIGNAL CONNECTIONS

Basic signal connections are shown in Figure 3. The connection to pin 14 completes the difference amplifier of A_3 (see Figure 1). The 3 to 8 jumper connects the output stage. The pin 9 connection provides a divide-by-two attenuator for the A_4 stage. This is necessary to limit the signal on the output stage switches to maintain signal linearity. The pin 11, 12 and 13 connections to pin 10 close the feedback loop around A_4.

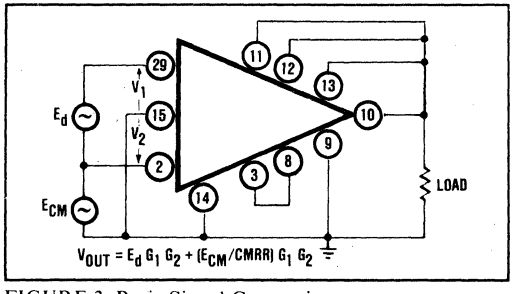


FIGURE 3. Basic Signal Connections.

In the equation shown in Figure 3, G_1 is the input stage gain and G_2 is the output stage gain. CMRR is the common-mode rejection ratio [CMR (in dB) = 20 log CMRR (in V/V)]. Common-mode voltage shown as E_{CM} is actually the average of the two voltages appearing at the two inputs (pins 29 and 2) with respect to pin 15 (V_1 and V_2).

GAIN SETTING

Gain is determined by a 4-bit digital word applied to the input D_0 through D_3 (see Figure 1). Pin 19 provides a latch function for the inputs. When pin 19 is a logic 0, changes on the D_0 through D_3 inputs are inhibited. Pin 19 should be at +5V if the latch is not used.

A gain state truth table is shown in Table 1. Gains are determined by the resistor networks shown in Figure 1. For the state D_3, D_2 = 0, 0, the input stage gain is a function of the gain setting resistor R_G connected between pins 26 and 27. If gains of 1, 2 and 4 are desired, no connection should be made to pins 26 and 27 and the resistance across these pins should be kept high with respect to 40kΩ (> 400MΩ).

Gain accuracy is established by laser-trimming the thim-film resistor networks during assembly. No external, user trimming is required.

OUTPUT OFFSET

Output offset may be varied by either of two methods shown in Figure 4. Sources at pin 9 and pin 14 apply voltages to the noninverting inputs of A_4 and A_3 respectively (see Figure 1). Since the output stage gain occurs after these points, the output voltage bias established with V_{R1} and V_{R2} will vary with the output gain, G_2. Sources connected at pins 9 and 14 must have resistances low with respect to 10kΩ in order not to disturb gain accuracy and common-mode rejection.

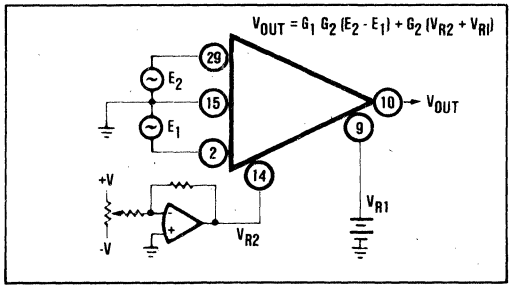


FIGURE 4. Output Offsetting.

LOW-PASS FILTER

For low frequency signals, system performance may be improved by reducing noise bandwidth in the amplifier. This may be accomplished with the addition of one or two external capacitors as shown in Figure 5. C_2 is connected to a 10k/10k attenuator and C_1 is connected as a feedback element across A4 (see Figures 1 and 5). The transfer function is:

$$\frac{V_O}{V_{IN}} = \left[\frac{10 \times 10^3}{100 \times 10^6 S(C_2 + 330 \times 10^{-12}) + 20 \times 10^3}\right]\left[1 + \frac{10 \times 10^3}{10 \times 10^3 R_1 SC_1 + R_1}\right]$$

TABLE I. Gain State Truth Table.

Digital Inputs (G_1)		(G_2)		G_1 (A_1 and A_2) (Pins 2 & 29 to 3)	G_2 (A_4) (Pin 8 to Pin 10)	$G_1 \cdot G_2$ (R_G* = ∞)	$G_1 \cdot G_2$ (R_G* ≠ ∞)
D_3	D_2	D_1	D_0				
0	0	0	0	1 + 40k R_G	1	1	1(1 + 40k R_G)
0	0	0	1		2	2	2(1 + 40k R_G)
0	0	1	0		4	4	4(1 + 40k R_G)
0	0	1	1		4	4	4(1 + 40k R_G)
0	1	0	0	4	1	4	4
0	1	0	1		2	8	8
0	1	1	0		4	16	16
0	1	1	1		4	16	16
1	0	0	0	32	1	32	32
1	0	0	1		2	64	64
1	0	1	0		4	128	128
1	0	1	1		4	128	128
1	1	0	0	256	1	256	256
1	1	0	1		2	512	512
1	1	1	0		4	1024	1024
1	1	1	1		4	1024	1024

*R_G connected between pins 26 and 27.

The first term is a first order filter. The second term is more complex. R_1 varies with the output stage gain -1.4k for $G_2 = 4$ (see Figure 1). The "1 + ..." nature of the transfer function prevents a true first order filter rolloff.

For most applications, the first order low-pass filter obtained by C_2 provides sufficient filtering. The value C_2 required for a desired cutoff frequency (f_2 in Hz) is obtained by the equation shown in Figure 5.

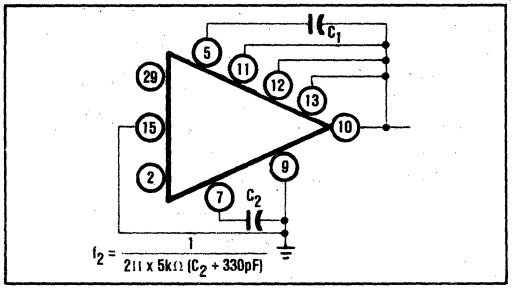


FIGURE 5. Low-Pass Filter Connections.

LARGER OUTPUT CURRENT

The output current rating of the 3606 is a minimum of ±5mA. The linearity of the gain is affected by output current. See Typical Performance Curves. Optimum linearity is achieved with $I_O \leq 1mA$, $I_O \leq 5mA$ is acceptable. Above 5mA it may be desirable to use a power or current booster as shown in Figure 6. Burr-Brown's 3329 will provide ±100mA output while Burr-Brown's 3553 will supply ±200mA. When either booster is placed inside the feedback loop as shown, the booster's offset voltage produces no significant errors since it is divided by the open-loop gain of the output stage.

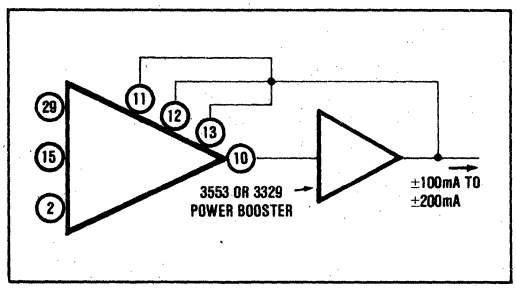


FIGURE 6. Output Current Booster.

GUARD DRIVE CONNECTIONS

Use of the guard drive connection shown in Figure 7 can improve system common-mode rejection when the distributed capacitance of the input lines is significant. The

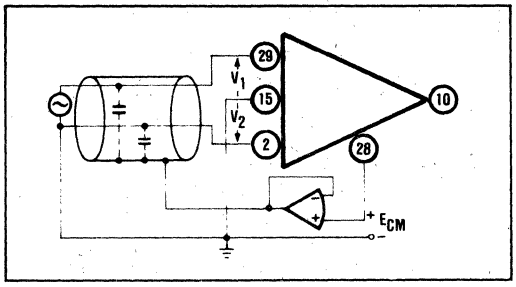


FIGURE 7. Guard Drive Connections.

common-mode voltage which appears on the input lines and on pins 29 and 2 is computed by the 3606 [(V_1 + V_2) 2] and appears at pin 28. It is then fed back to the shield so that the voltage across the distributed capacitances is minimized. This reduces the common-mode current and improves common-mode rejection. The operational amplifier in the voltage follower configuration is used to supply more current than can be obtained from the 20k resistors connected internally to pin 28 (see Figure 1).

OFFSET TRIM

Offset voltages of the 3606 are reduced by laser-trimming during assembly. This reduces the initial offset voltage and the offset voltage change with gain change to levels that are acceptable for most applications. For more critical applications the offset voltages can be externally

nulled to zero. The following steps should be followed (see Figure 8).

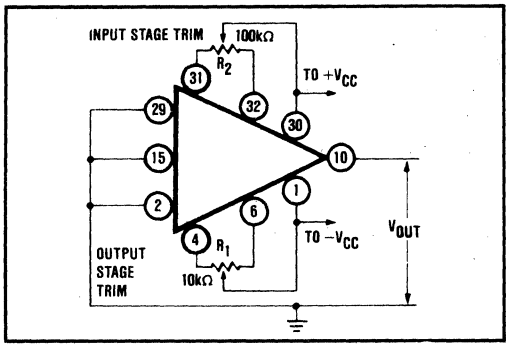


FIGURE 8. Optional Offset Trim.

1. Adjust both R_1 and R_2 to mid-range.
2. Set the gain to minimum (1V V).
3. Adjust R_1 to make V_{OUT} equal zero.
4. Set the gain to maximum (1024V V).
5. Adjust R_2 to make V_{OUT} equal zero.

By using this technique, the change in output offset voltage caused by a gain change of 1V V to 1024V V may be reduced to, typically 1mV instead of 10mV with no external trimming. Trimming may cause the offset voltage drift vs temperature to increase slightly.

APPLICATIONS

A typical application of 3606 in a microcomputer based data acquisition system is shown in the block diagram below.

The purpose of this system is to be able to acquire data from a specific analog input channel, suitably condition it (amplify it and convert it to digital form) and store it or transmit it for further processing.

Initially the Microcomputer loads the RAM (random access memory) with the required coding for various desired gains via Data Bus. The coding associates the gain state truth table for 3606 with corresponding address locations in the computer memory. So when the computer puts out an instruction to multiplex a specific analog input channel through the multiplexer via the Address Bus, the RAM also receives the same address information and puts out corresponding gain code to the PGIA 3606. The 3606 amplifies the multiplexed signal by the programmed gain value, and outputs it to S/H (sample and hold). The S/H holds the output value when it receives the control signal from the computer and the A/D converts it and outputs it to the computer via the Data Bus under computer control.

The PGIA 3606 allows the system user to modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated instruments are not required for various input channels, the PGIA also saves space and overall system costs.

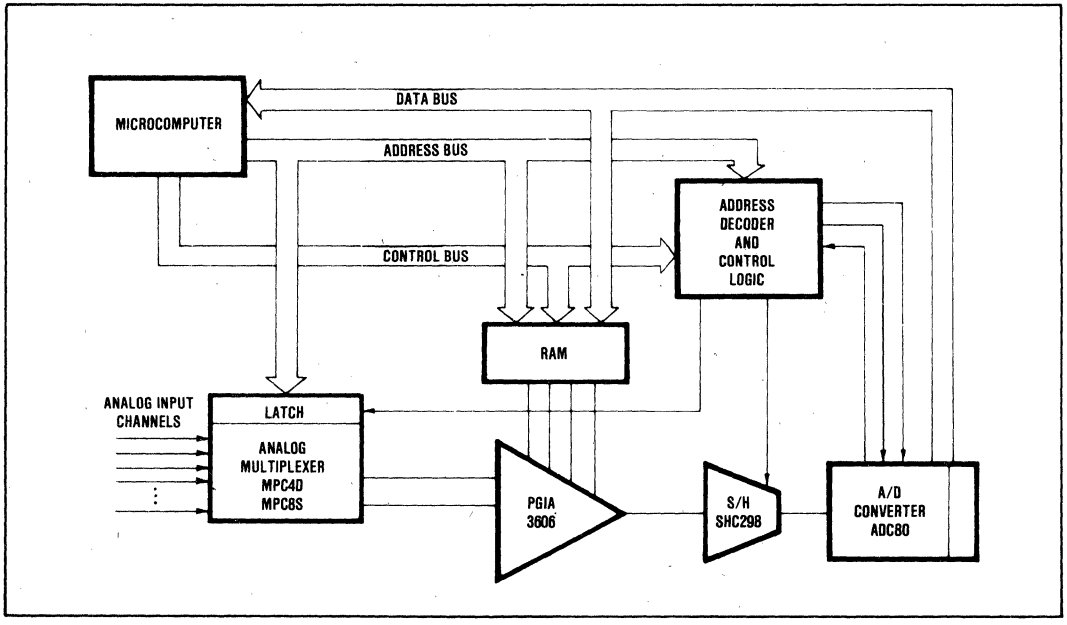
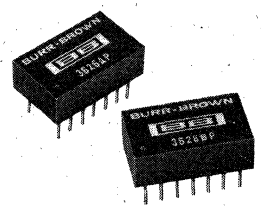


FIGURE 9. Use of 3606 in Data Acquisition System.

BURR-BROWN®

3626



Low Drift INSTRUMENTATION AMPLIFIER

FEATURES

- LOW VOLTAGE DRIFT @ LOW GAIN
  2μV/°C @ G = 5 (3626CP)
- LOW NOISE - 2μV, p-p
- HIGH CMR - > 80dB @ G = 1000
- LOW COST
- SMALL SIZE - DIP Package

DESCRIPTION

The 3626 is an integrated circuit instrumentation amplifier designed for amplifying low level signals in the presence of high common-mode voltages. Its low drift, high input impedance ($5 \times 10^9 \Omega$), easy gain adjustment (5V/V to 1000V/V) and high common-mode rejection eliminate the problems and compromises associated with using operational amplifiers to realize the same gain function.

Compared to other integrated circuit instrumentation amplifiers it has the unique feature of having low voltage drift versus temperature at low gains.

The 3626 offers many benefits to the user for his instrumentation applications:

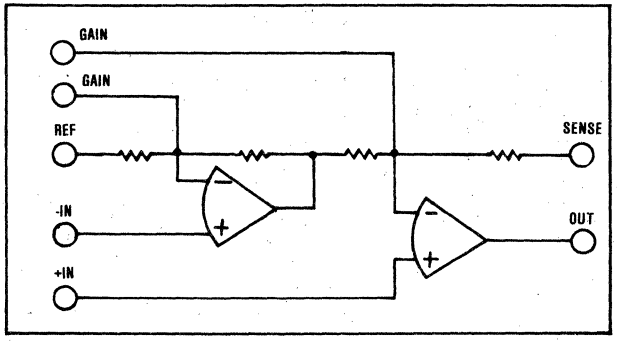
Low voltage reduces temperature errors.

High common-mode rejection preserves system accuracy.

High input impedance prevents errors due to source loading and source impedance imbalance.

Small, dual-in-line package conserves board space.

Laser-trimmed offset requires no nulling.



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DISCUSSION

An instrumentation amplifier is basically a closed-loop gain block that exhibits high input impedance and high common-mode rejection. Instrumentation amplifiers are committed devices with differential inputs and accurately predictable input-to-output relationships - all necessary feedback networks are contained in the circuit package. These characteristics distinguish instrumentation amplifiers from operational amplifiers - open-loop devices whose closed-loop performance depends upon the external networks supplied by the user.

In instrumentation amplifiers, parameters such as input and output impedances, frequency response, offset voltage drift, and common-mode rejection are specified for the closed-loop, committed configuration. One of the few parameters that the user can vary is gain (by choosing the external gain-setting resistor value). Another important difference between an operational amplifier and instrumentation amplifier is that the instrumentation amplifier has no summing junction available; you cannot make a summing amplifier or integrator out of an instrumentation amplifier.

In the past few years, choices in instrumentation amplifier designs have grown from a number of discrete modular units to include monolithic and hybrid integrated circuit versions which offer high performance at lower cost - and in smaller packages. Monolithic Integrated Circuits (IC's) were the first to break the price and performance barrier. Hybrid IC's, such as the 3626, are more expensive than monolithic IC's but they give better performance for the money.

Instrumentation amplifiers normally require at least one external resistor - the gain-setting resistor R_G. Monolithic units usually require two additional - the output feedback resistor and a resistor between feedback common and ground. Since temperature coefficient differences between these two resistors will cause output offset voltage drift, they must be matched to meet the desired drift specification. Hybrid units, such as the 3626, have the advantage that all resistors except the gain-setting R_G can be included in the package.

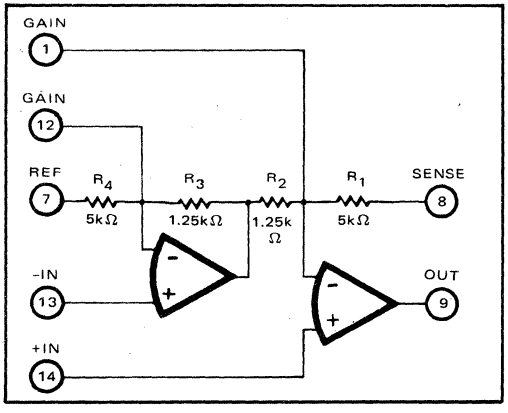


FIGURE 1. Simplified Circuit Diagram.

A simplified circuit diagram of the 3626 is shown in Figure 1. The circuit uses Burr-Brown's high performance bipolar integrated circuit amplifiers and a laser-trimmed thin-film resistor network. The excellent initial matching and temperature tracking of these components provide a level of performance difficult to obtain with even expensive discrete amplifiers and resistors. The gain accuracy, linearity, and temperature coefficient are particularly attractive.

One of the most outstanding features of the 3626 is its low voltage drift, especially at low and medium gains. Figure 2 shows the drift performance of the 3626 series compared to monolithic integrated circuit instrumentation amplifiers. The guaranteed voltage drift

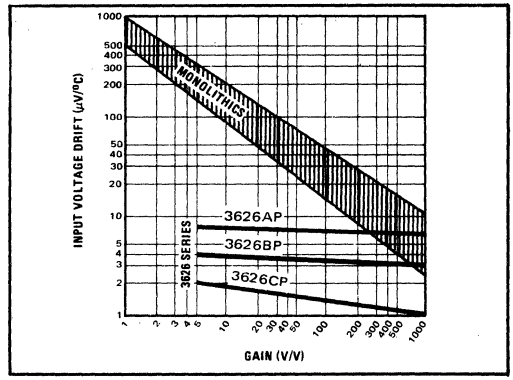


FIGURE 2. Input Offset Drift vs Gain.

performance is almost two orders of magnitude better at low gains.

The design of the 3626 is such that output biasing is easily accomplished. See Figure 3 for proper connections. The impedance of the reference source should be low compared to 5kΩ. A current booster such as the 3329 (100mA) or 3553 (200mA) can conveniently be used with the 3626 to increase its output current driving capability.

An application note, "Instrumentation Amplifiers" (AN-75) is available which has information on the use of instrumentation amplifiers. Contact your nearest sales office or our factory in Tucson to obtain a copy.

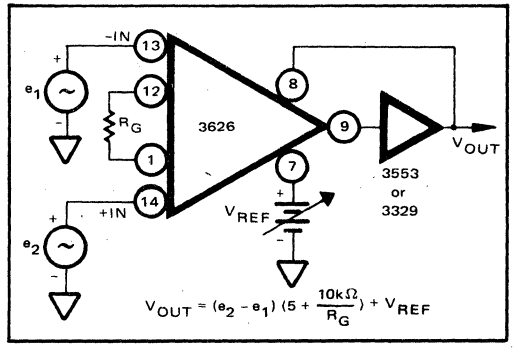


FIGURE 3. Output Offsetting and Power Boosting.

SPECIFICATIONS

ELECTRICAL

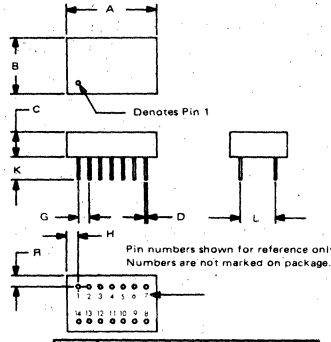
Specifications typical at 25°C and ±15VDC unless otherwise noted.

MODELS	3626AP	3626BP	3626CP
GAIN			
Gain Equation		$G = 5 + (10k\Omega/R_G)$	
Error from Equation(1)		(±0.25 - 0.003G)%	
Range of Gain, min		5 to 1000	
Gain Temp. Coefficient:			
G = 5		2ppm/°C	
G = 10		25ppm/°C	
G = 100		35ppm/°C	
G = 1000		50ppm/°C	
Nonlinearity, max (%)(2)	±(0.02 + 0.0003G)	±(0.01 + 0.0003G)	±(0.01 + 0.0003G)
OUTPUT			
Rated Output, min		±10V @ ±5mA	
Output Impedance, G = 100		2Ω	
INPUT			
Input Impedance, Diff, & CM		5 x $10^9\Omega$‖3pF	
Input Voltage Range, min		±10V	
CMR, DC to 60Hz		with 1kΩ source unbalance	
G = 5, min	68dB	74dB	74dB
G = 10 to 1000, min	74dB	80dB	80dB
INPUT OFFSET VOLTAGE			
Initial Offset, max(1)	±(0.4 + (0.4/G))mV	±(0.2 + (0.2/G))mV	±(0.2 + (0.2/G))mV
vs. Temperature, max	±(6 + (10/G))μV/°C	±(3 + (5/G))μV/°C	±(1 + (5/G))μV/°C
vs. Supply		40μV/V	
vs. Time		3μV/mo.	
INPUT BIAS CURRENTS			
Initial Bias Current, max		±50nA (either input)	
vs. Temperature, max		±0.7nA/°C	
vs. Supply		±0.1nA/V	
INPUT NOISE			
Voltage, p-p, 0.01Hz to 10Hz		2μV, p-p	
rms, 10Hz to 10kHz		2μV, rms	
Current, p-p, 0.01Hz to 10Hz		150pA, p-p	
rms, 10Hz to 10kHz		50pA, rms	
DYNAMIC RESPONSE			
Small Signal, ±3dB Flatness:			
G = 5		400kHz	
G = 10		160kHz	
G = 100		14kHz	
G = 1000		1.4kHz	
Small Signal, ±1% Flatness:			
G = 5		76kHz	
G = 10		27kHz	
G = 100		2.1kHz	
G = 1000		250Hz	
Full Power, G = 5 to 100		19kHz	
Slew Rate, G = 5 to 100		1.2V/μsec	
Settling Time (0.1%):			
G = 5		20μsec	
G = 10		30μsec	
G = 100		100μsec	
G = 1000		12ms	
POWER SUPPLY			
Rated Voltage		±15VDC	
Voltage Range		±5VDC to ±20VDC	
Quiescent Supply Current		±7mA, max	
TEMPERATURE RANGE			
Specifications, min		-25°C to +85°C	
Operation		-55°C to +125°C	
Storage		-65°C to +150°C	

NOTES:
1. May be trimmed to zero.
2. Nonlinearity is the maximum peak deviation from the best straightline as a percent of full scale peak-to-peak output.

MECHANICAL

NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.



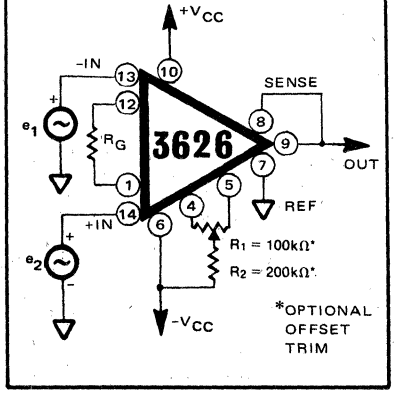
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 0145MC (14-pin DIP)
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883.

PIN CONNECTIONS

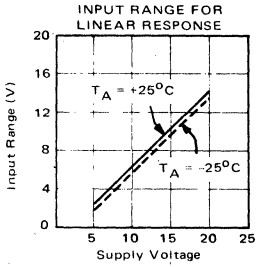
1. GAIN
2. NO INTERNAL
3. CONNECTION
4. V_{OS}
5. V_{OS}
6. $-V_{CC}$
7. REF
8. SENSE
9. OUT
10. $+V_{CC}$
11. NO INTERNAL CONNECTION
12. GAIN
13. -IN
14. +IN

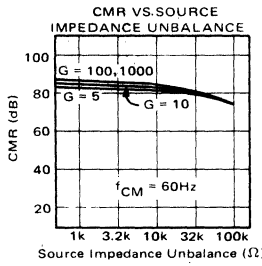
CONNECTION DIAGRAM

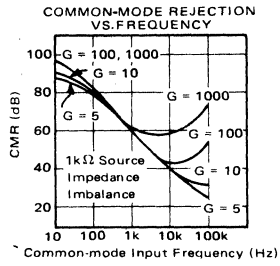


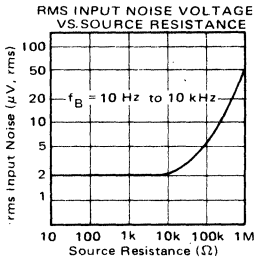
TYPICAL PERFORMANCE CURVES

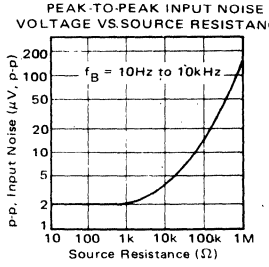
Typical @ 25°C and ±15VDC power supplies unless otherwise noted.

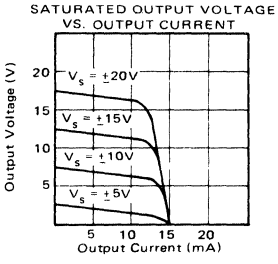


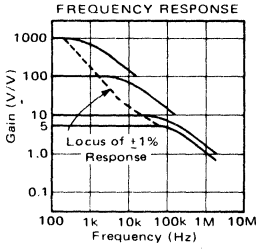


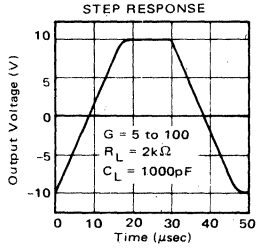


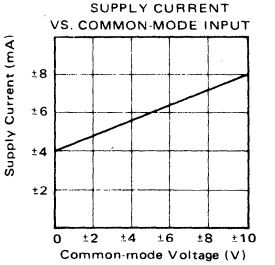












INSTALLATION AND OPERATING INSTRUCTIONS

SETTING THE GAIN

Figure 3 shows the normal operating connections for the 3626. The differential gain, G, is determined according to the equation:

$$G = 5 + \frac{10k\Omega}{R_G}$$

where R_G is the resistor shown in Figure 4. This gain equation is typically accurate to 0.25%. The temperature coefficient of R_G will directly affect the stability of G. For high gains, R_G will be quite small (R_G = 10Ω for G = 1000); thus, the wiring impedance between pins 12 and 1 should be kept as low as possible. (Trimming of R_G will eliminate the effects of wiring impedances so long as this impedance is constant.) Also, note that V_{ref} source needs to be low impedance so as not to significantly affect the gain equation.

COMMON-MODE REJECTION TRIM

The 3626 meets its CMR specifications without additional trimming; however, for improved CMR in special situations (such as imbalanced source impedances), the circuit in Figure 4 may be used. In this circuit, R_1 is added to intentionally imbalance the inverting and noninverting gains of the amplifier. R_2 is then used to rebalance them, which overcomes the effects of any residual CMR degradation due to source impedance imbalance, etc. An improvement of approximately 6 to 10dB can be typically realized at low gains.

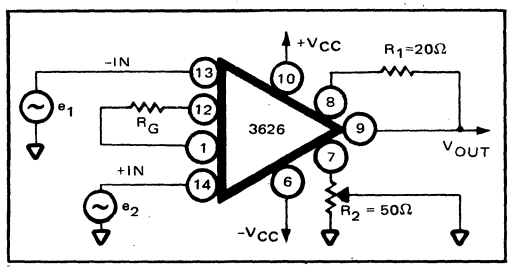


FIGURE 4. Common-mode Rejection Trim.

BURR-BROWN®

3627

High Accuracy Unity-Gain DIFFERENTIAL AMPLIFIER

FEATURES

- LOW COST
- EASY TO USE
- COMPLETELY SELF-CONTAINED
- HIGH ACCURACY
  - Gain Error, 0.005%
  - Nonlinearity, 0.0005%
  - CMR, 106dB
- NO TRIMMING REQUIRED

DESCRIPTION

The 3627 is a high accuracy committed-gain differential amplifier. It consists of a high quality monolithic operation amplifier, a low drift thin-film resistor network and laser-trimmed offset circuitry - all inside a single integrated circuit package.

The fact that the 3627 is completely self-contained in a TO-99 package has several user benefits:

The total performance is guaranteed as a single component.

No gain adjustments are required.

No offset trimming is required.

The whole circuit, including the gain setting resistors and offset trim circuitry, is protected by the environmentally rugged hermetically sealed package.

The total amplifier function is very small in size (0.108 square inches of area and 0.025 cubic inches of volume).

The 3627 is offered in two grades; the 3627AM and the 3627BM. They differ only in common-mode rejection (94dB typ. vs 106dB typ.) and offset voltage drift (15μV/°C typ. vs 10μV/°C typ.)

The 3627 offers excellent total performance with no fuss and a very-low total installed cost.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DISCUSSION OF PERFORMANCE

The 3627 is a new and unique approach to a widely occurring problem - how to get excellent performance at a low cost in a unity-gain differential amplifier circuit. Burr-Brown's solution to this problem uses its wide range of integrated circuit expertise; a high quality monolithic amplifier, low drift high stability thin-film resistor network and state-of-the-art laser-trimming techniques. The result is a completely self-contained amplifier with total guaranteed 25°C accuracy of less than ±0.015% (gain error, nonlinearity, offsets and common-mode rejection).

The simplicity of the unity-gain differential amplifier circuit may be deceiving when one considers an error analysis. Consider, for example, gain and common-mode rejection errors. The gain is determined by the ratio of R1 and R2 and the ratio of R3 and R4. The common-mode rejection of the total circuit is a function of the CMR of the operational amplifier and the matching of the resistors R1 to R3 and R2 to R4. Even if the operational amplifier is perfect (infinite CMR), in order to guarantee 100dB common-mode rejection would require resistor match of approximately 0.0005% (5ppm).

This matching (and especially maintaining the match over temperature) can be difficult and expensive to achieve. Packaged matched and tracking resistor networks are available but they are fairly expensive compared to the cost of the complete 3627 amplifier. Of course, matching can be obtained by trimming or padding some of the resistors, but this is difficult to do since each resistor affects both gain accuracy and common-mode rejection simultaneously. Unless care is used in choosing the trimming sequence a frustrating iterative trimming process can be encountered.

With the 3627 these problems no longer exist for the user. They are solved inside the package by Burr-Brown and the user has a completely self-contained plug-in-and-go amplifier to use. The excellent gain accuracy and common-mode rejection is obtained by using laser-trimming of a thin-film resistor network (R1 through R4). The outstanding gain and common-mode rejection temperature coefficients are a result of the excellent TCR tracking properties inherent in Burr-Brown's thin-film resistor networks.

The offset voltage is also laser-trimmed to a very low 250μV, max., value (100μV, typical). This low value of offset eliminates the need for external offset adjust potentiometers which reduces cost and improves reliability.

The basic approach of the 3627 as a completely self-contained amplifier has several cost saving implications. It reduces design, purchasing and inventory cost. It reduces labor costs because the gain setting resistors do not require installation and adjustment. Also, no potentiometers are required.

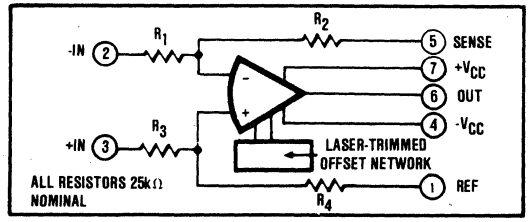
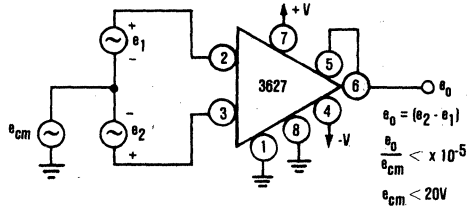
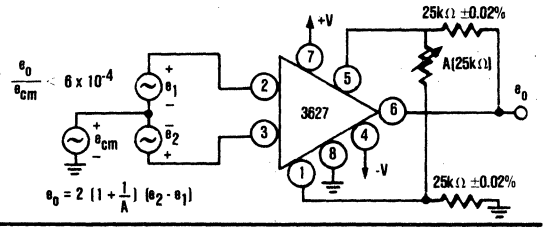


FIGURE 1. Simplified Circuit Diagram.

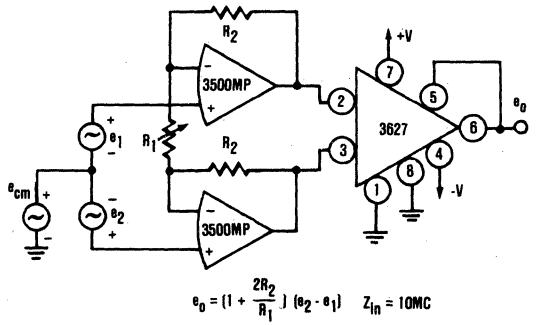
UNITY-GAIN DIFFERENCE AMPLIFIER



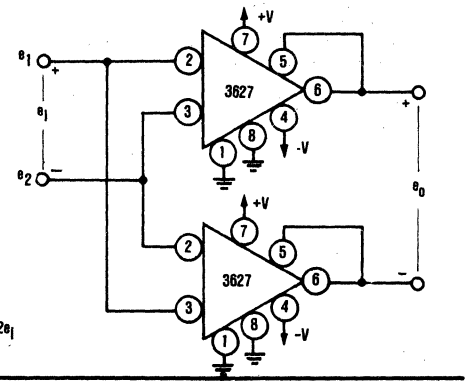
VARIABLE-GAIN DIFFERENTIAL AMPLIFIER



HIGH INPUT IMPEDANCE, VARIABLE-GAIN, INSTRUMENTATION AMPLIFIER



DIFFERENTIAL IN - DIFFERENTIAL OUT AMPLIFIER



SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and ±15VDC power supply unless otherwise noted.

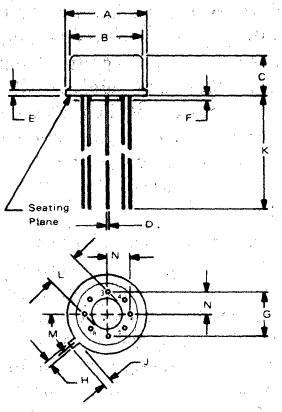
MODELS	3627AM	3627BM
GAIN		
Gain Equation	G = 1V/V(1)	
Gain Error	±0.01%, max (±0.005% typ)	
Gain Nonlinearity(2)	±0.001%, max (±0.0005% typ)	
Gain Temp. Coefficient, max	±0.0005%/°C (5ppm/°C)	
Gain Temp. Coefficient, typ	±0.0002%/°C (2ppm/°C)	
OUTPUT		
Rated Output, min	±10V at ±5mA	
Rated Output, typ	±12V at ±10mA	
Output Impedance	0.01Ω	
INPUT		
Input Impedance		
Differential	50kΩ	
Common-mode	50kΩ	
Input Voltage Range		
Differential	±20V	
Common-mode	±20V	
Common-mode Rejection, DC to 60Hz		
CMR, at 25°C	90dB, min (94dB, typ)	100dB, min (106dB, typ)
CMR, -25°C to +85°C	80dB, min (90dB, typ)	86dB, min (94dB, typ)
OFFSET AND NOISE		
Offset Voltage, RTO(4)(5)		
at 25°C	250μV, max (100μV, typ)	
vs Temperature, μV/°C	30, max (15, typ)	20, max (10, typ)
vs Supply	20μV/V	
vs Time	20μV/mo	
Noise Voltage, RTO(4)(6)		
0.01Hz to 10Hz	2μV, p-p	
10Hz to 100Hz	1.5μV, rms	
DYNAMIC RESPONSE		
Small Signal, ±1% Flatness	5kHz min (8kHz, typ)	
Small Signal, ±3dB Flatness	0.8MHz min (1.2MHz, typ)	
Full Power Bandwidth	14kHz min (18kHz, typ)	
Slew Rate	0.6V/μsec min (1V/μsec, typ)	
Settling Time, 0.1% (±10mV)	20μsec	
Settling Time, 0.01% (±1mV)	50μsec	
POWER SUPPLY		
Rated Voltage	±15VDC	
Voltage Range	±5VDC to ±18VDC	
Quiescent Supply Current	±2mA	
TEMPERATURE RANGE		
Specifications, min	-25°C to +85°C	
Operation	-55°C to +125°C	
Storage	-65°C to +150°C	

NOTES:

1. Connected as unity-gain amplifier. Several other configurations are possible. See the figures in Discussion and Typical Applications.
2. Nonlinearity is the maximum peak deviation from the best straightline as a percent of full scale peak-to-peak output.
3. With zero source impedance unbalance.
4. Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifiers offset voltage and noise voltage.
5. Includes effects of amplifiers' input bias currents.
6. Includes effects of amplifiers' input current noise.

MECHANICAL

TO-99

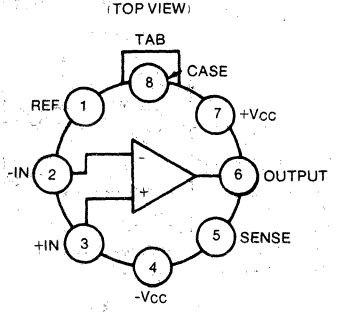


NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating compostion conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CONNECTION DIAGRAM

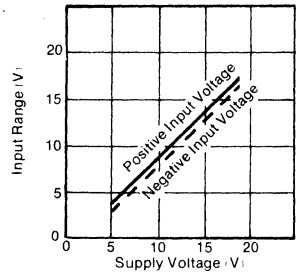


See Figure 1 for circuit diagram.

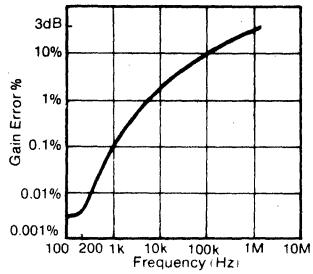
TYPICAL PERFORMANCE CURVES

Specifications at T_A = +25°C and ±15VDC power supply unless otherwise noted.

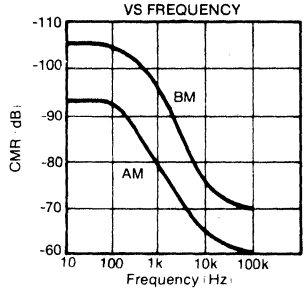
INPUT RANGE FOR LINEAR RESPONSE



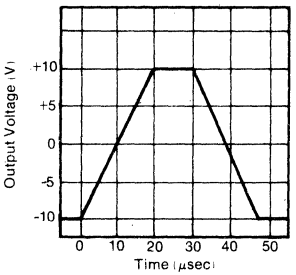
GAIN ERROR VS FREQUENCY



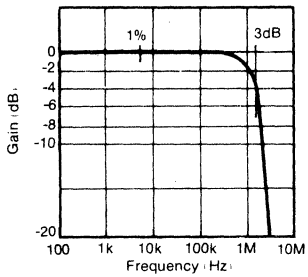
COMMON-MODE REJECTION VS FREQUENCY



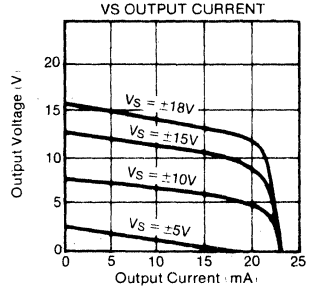
STEP RESPONSE



SMALL SIGNAL GAIN VS FREQUENCY

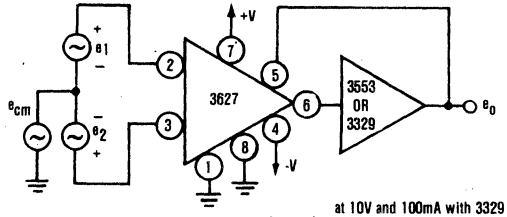


MAXIMUM OUTPUT VOLTAGE VS OUTPUT CURRENT



TYPICAL APPLICATIONS

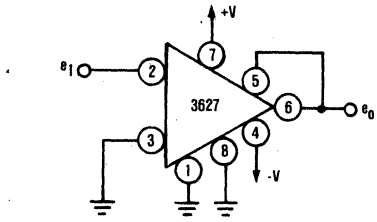
HIGH POWER DIFFERENTIAL AMPLIFIER



$e_o = (e_2 - e_1)$

at 10V and 100mA with 3329
at 10V and 200mA with 3553

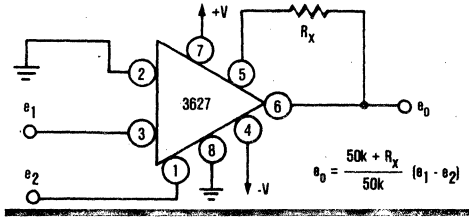
HIGH ACCURACY, LOW DRIFT, LOW OFFSET-UNIT GAIN INVERTER



$e_o = e_1$

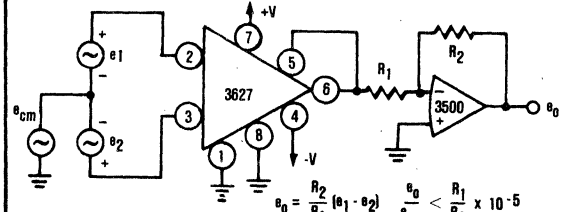
ACCURACY 0.01%
LINEARITY 0.001%
OFFSET < 250μV AT OUTPUT
OFFSET DRIFT < 20μV/°C AT OUTPUT

NONINVERTING SUMMER



$e_o = \frac{50k + R_x}{50k} (e_1 - e_2)$

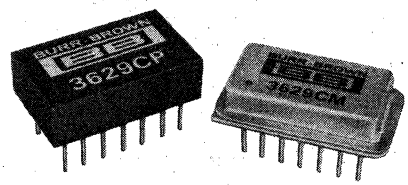
HIGHER GAIN DIFFERENCE AMPLIFIER



$e_o = \frac{R_2}{R_1} (e_1 - e_2)$ $\frac{e_o}{e_{cm}} < \frac{R_1}{R_2} \times 10^{-5}$

BURR-BROWN®

3629



Low Drift INSTRUMENTATION AMPLIFIER

FEATURES

- VERY-LOW VOLTAGE DRIFT 0.75μV/°C
- HIGH CMR - 88dB at 60Hz
- LOW BIAS CURRENT - 20mA
- LOW NOISE - 1.2μV, p-p
- SMALL SIZE - DIP Package

APPLICATIONS

- SIGNAL CONDITIONING FOR PROCESS CONTROL AND DATA ACQUISITION
- TRANSDUCER AMPLIFIERS FOR:
  - Thermocouples
  - Load Cells
  - Strain Gage Bridges
- MULTIPLEXER BUFFERS

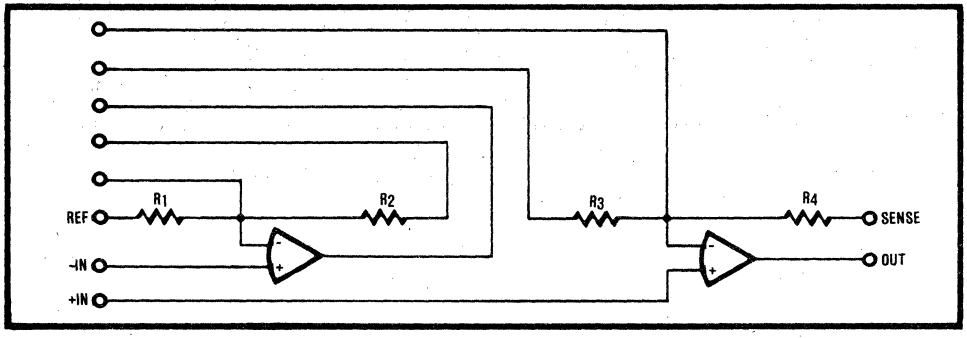
DESCRIPTION

Offering very-low voltage drift versus temperature even at low gains, the 3629 meets critical instrumentation requirements when amplifying low-level signals in the presence of high common-mode voltages. This precision integrated circuit instrumentation amplifier offers low bias current and high input impedance ($10^{10}\Omega$). A single resistor sets gain from 5V V to 1000V V.

The 3629 exceeds the performance of other IC instrumentation amplifiers and offers many benefits for instrumentation applications:

- Low voltage drift to reduce temperature errors
- High common-mode rejection to preserve system accuracy
- High input impedance to minimize errors caused by source loading and source impedance imbalance
- Small, dual-in-line plastic or hermetically sealed metal package to conserve board space
- Laser-trimmed offset to eliminate nulling

Use the 3629 to eliminate problems and compromises that arise when attempting to use operational amplifiers to achieve the same gain function.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications typical at 25°C with ±15VDC power supply unless otherwise noted.

MODEL	3629AP, 3629AM			3629BP, 3629BM, 3629SM			3629CP, 3629CM			UNITS
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN										
Range of Gain	5		1000	•		•	•		•	V/V
Gain Equation		G = 5 + (20k/RG)			•			•		V/V
Error From Equation, DC			(1)			•			•	
Gain Temp. Coefficient										
G = 5		2	5		•	•		•	•	ppm/°C
G = 10		12	25		•	•		•	•	ppm/°C
G = 100		20	45		•	•		•	•	ppm/°C
G = 1000		25	50		•	•		•	•	ppm/°C
Nonlinearity, DC		± 0.002	±(0.005		±(0.001	±(0.003		±(0.001	±(0.003	
		+ 10-5G	+ 2 x 10-5G)		+ 10-5G)	+ 10-5G)		+ 10-5G)	+ 10-5G)	% p-p FS
RATED OUTPUT										
Voltage	±10	±12.5		•	•		•	•		V
Current	±10	±12.5		•	•		•	•		mA
Output Impedance G = 100		0.01			•			•		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at 25°C		±25 ± 200/G	±50 ±(400/G)		±10 ± 100/G)	±25 ± 200/G)		±10 ±(100/G)	±25 ± 200/G)	µV
vs Temperature			±3 ±(10/G			±1.5 ±(7.5/G)			±0.75 ±(5/G)	µV/°C
vs Supply		5	10		•	•		•	•	µV/V
vs Time		±0.4			•			•		µV/mo
INPUT BIAS CURRENT										
Initial Bias Current each input		±15	±35		±10	±25		±5	±20	nA
vs Temperature		±0.30	±0.60		•	•		•	•	nA/°C
vs Supply		±0.1	±0.2		•	•		•	•	nA/V
Initial Offset Current		±15	±50		±10	±30		±5	±20	nA
vs Temperature		±0.6	±1.2		•	•		•	•	nA/°C
INPUT IMPEDANCE										
Differential		10 || 3			•			•		GΩ || pF
Common-mode		10 || 3			•			•		GΩ || pF
INPUT VOLTAGE RANGE										
Range	±10			•			•			V
CMR w/1kΩ Source Imbalance										
DC, G = 5	100	104		•	•		•	•		dB
G = 10	106	110		•	•		•	•		dB
G = 100 to 1000	110	120		•	•		•	•		dB
60Hz All Gains	88	92		•	•		•	•		dB
INPUT NOISE										
Voltage, p-p, 0.01Hz to 10Hz		1.2			•			•		µV, p-p
rms, 10Hz to 1.0kHz		1.0			•			•		µV, rms
Current, p-p, 0.01Hz to 10Hz		70			•			•		pA, p-p
rms, 10Hz to 1.0kHz		20			•			•		pA, rms
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness,										
G = 5		90			•			•		kHz
G = 10		60			•			•		kHz
G = 100		30			•			•		kHz
G = 1000		3.5			•			•		kHz
Small Signal, ±1% Flatness,										
G = 5		7.2			•			•		kHz
G = 10		3.8			•			•		kHz
G = 100		0.33			•			•		kHz
G = 1000		30			•			•		Hz
Full Power, G = 5 to 100		7.5			•			•		kHz
Slew Rate, G = 5 to 100	0.2	0.45		•	•		•	•		V/µsec
Settling Time 0.1%/0.01%										
G = 5		35/40			•			•		µsec
G = 100		85/120			•			•		µsec
G = 1000		350/400			•			•		µsec
POWER SUPPLY										
Rated Voltage		±15			•			•		VDC
Voltage Range	±5		±20	•		•	•		•	VDC
Current, Quiescent		±5	±7		•	•		•	•	mA
TEMPERATURE RANGE										
Specification(2)	-25		+85	•		•	•		•	°C
Operation	-55		+125	•		•	•		•	°C
Storage	-65		+150	•		•	•		•	°C

*Specifications same as for 3629AP, AM.

NOTES:

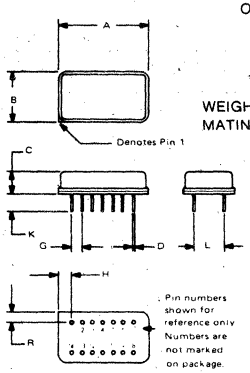
1. See Typical Performance Curves.
2. -55°C to +125°C for 3629SM.

MECHANICAL

METAL CAN PACKAGE

Order Number:
3629AM
3629BM
3629CM
3629SM

WEIGHT: 4.1 grams
MATING CONNECTOR: 0145MC



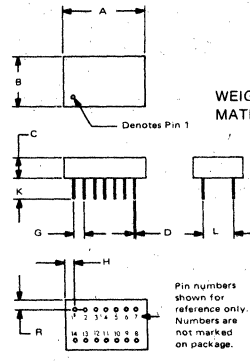
NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

PLASTIC PACKAGE

Order Number:
3629AP
3629BP
3629CP

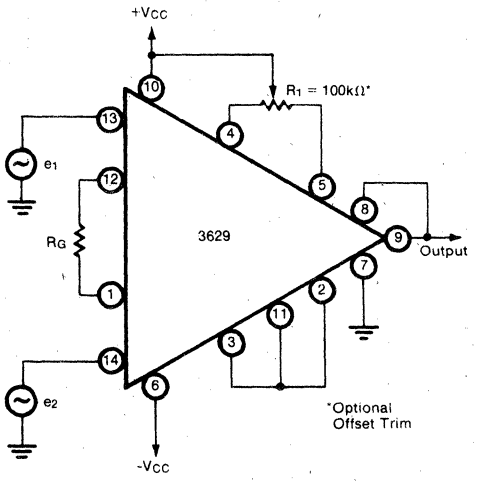
WEIGHT: 2.3 grams
MATING CONNECTOR: 0145MC



NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

CONNECTION DIAGRAM



INSTALLATION AND OPERATING INSTRUCTIONS

OFFSET VOLTAGE ADJUSTMENT

Initial offset of the 3629 is trimmed to a very-low value during production. In most applications further nulling will not be required. If it is necessary to null offset to the lowest possible value, a low cost single turn potentiometer can be connected between pins 4 and 5 as shown in the Connection Diagram. Drift changes 0.33μV/°C for each 100μV of offset voltage nulled. Due to second order effects, the point of minimum offset drift does not occur at the point of zero offset voltage in approximately 25% of the cases. In these instances nulling the offset voltage may cause a slight increase in voltage drift.

A following stage should be used if large system offsets must be nulled. This method results in the lowest possible drift. In the circuit shown in Figure 1, the offset component of V_{OUT} due to V_1 is (V_1R_2) R_1. Resistors R_1 through R_4 are selected to provide system scaling and to make the offset component of V_{OUT} due to V_2 cancel the component of V_{OUT} due to V_1.

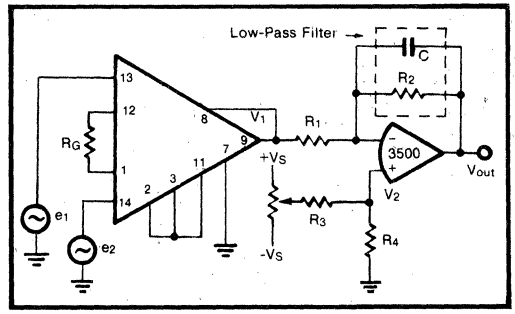


FIGURE 1. Multistage Amplifier For Offset Null and High Frequency Filtering.

NOISE

The 3629 offers very-low noise at low and mid-frequencies. See specifications and performance curves. At frequencies above 100kHz, noise increases and may cause errors if the following circuitry responds to higher frequencies. When high frequency noise must be reduced, a low-pass filter should be installed in a stage following the 3629. Figures 1 and 2 illustrate two high frequency filtering approaches.

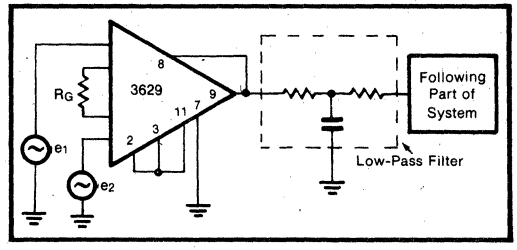
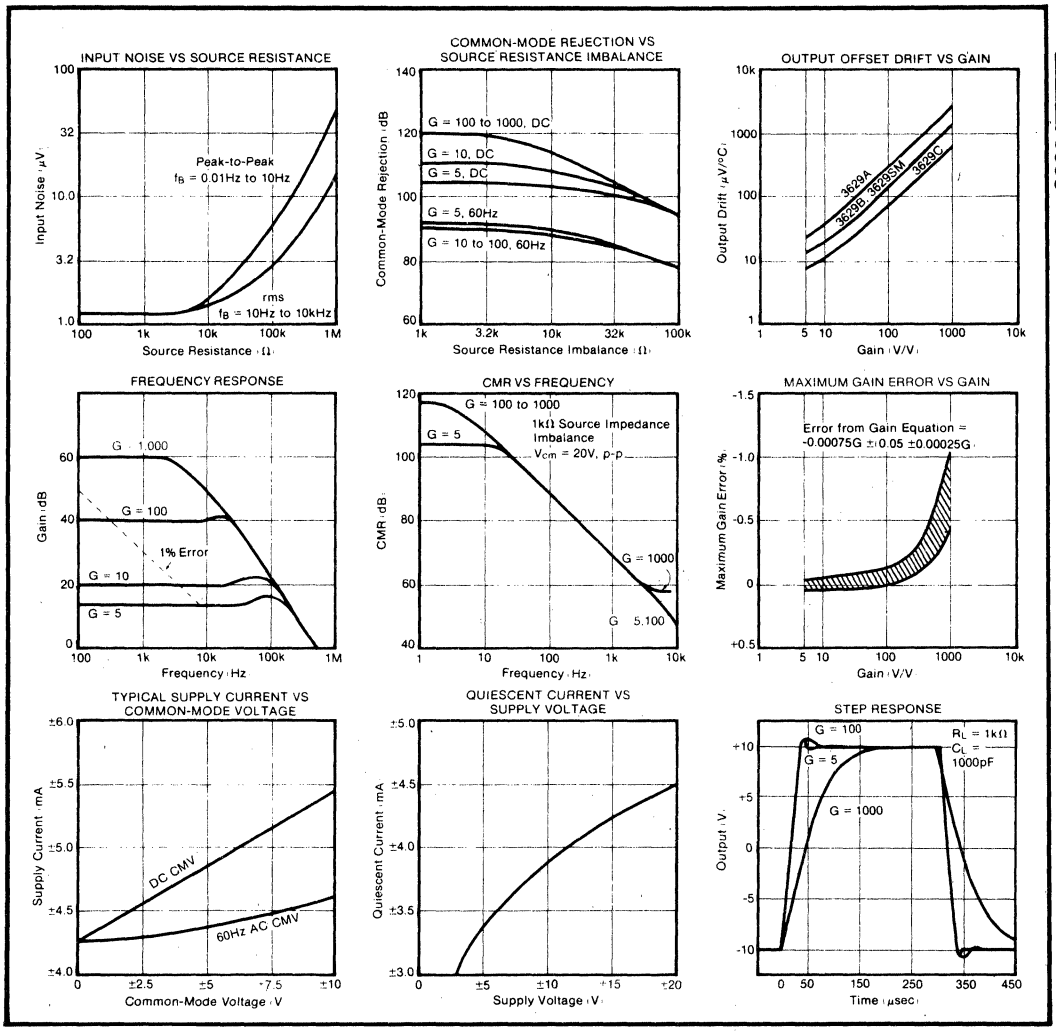


FIGURE 2. High Frequency Filter For Single Stage Amplifier.

TYPICAL PERFORMANCE CURVES



APPLICATIONS INFORMATION

Instrumentation amplifiers are closed-loop gain blocks whose committed circuitry accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high input impedances.

Figure 3 represents a simplified circuit diagram of the 3629. The circuit employs high performance bipolar IC amps and a laser-trimmed thin-film resistor network.

The 3629 offers excellent performance. Its low voltage drift reduces temperature errors, especially at low and medium gains. Figure 4 illustrates the drift performance of the 3629 compared with competitive monolithic IC instrumentation amplifiers. Note that the drift does not increase at lower gains. Compare the 3629's input offset voltage drift vs temp at 1.75μV/°C with monolithic IC instrumentation amps in the range of 100μV/°C.

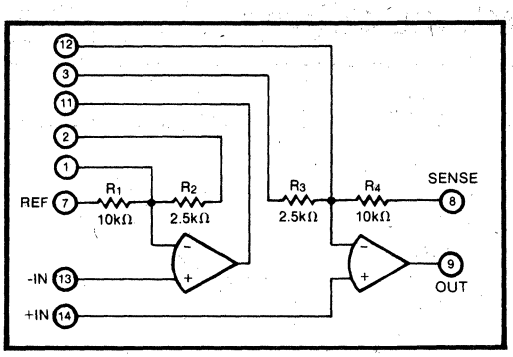


FIGURE 3. Simplified Circuit Diagram.

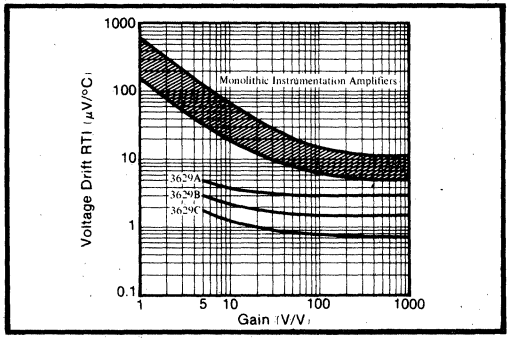


FIGURE 4. Input Offset Drift vs Gain.

Because of its design, output biasing of the 3629 is easily accomplished. See Figure 5 for connections. The impedance of the reference source should be low compared to 10kΩ. Figure 5 also shows a current booster, such as the Burr-Brown 3329 (100mA) or 3553 (200mA), used with the 3629 to increase its output current driving capability while retaining its 5V/V to 1000V/V gain characteristics. If power boosting is not required; connect pin 8 to pin 9.

DESIGN VERSATILITY

The 3629 offers additional application versatility. Its matched pair of amplifiers can be used as two independent, uncommitted op amps with a laser trimmed thin-film network present in one package.

When amplification must be extended to gains below 5, a 3629 used with a unity gain instrumentation amplifier (Burr-Brown 3627) is recommended. This connection is shown in Figure 6.

DESIGN ALTERNATIVES

To amplify signals in the presence of common-mode voltages and noise while maintaining high input impedance, you can: 1) design and build an op amp circuit with a differential input configuration; 2) design and build an instrumentation amplifier made up of multiple op amps or; 3) purchase a ready-to-install, committed instrumentation amplifier. Only the third option provides an immediate solution with the elimination of in-house design, assembly and tuning steps. The growing range of lower cost, high quality IC instrumentation amps available has answered the build or buy question.

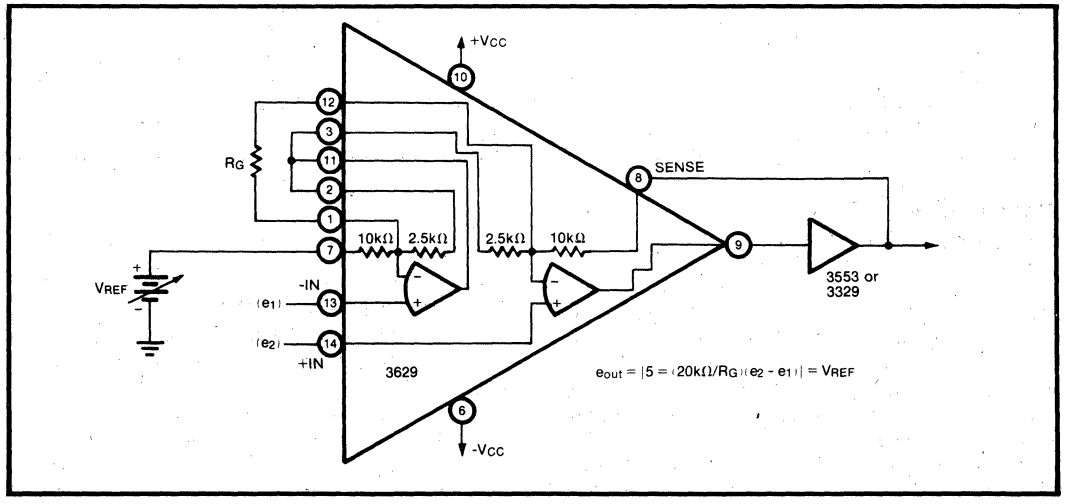


FIGURE 5. Output Biasing and Power Boosting.

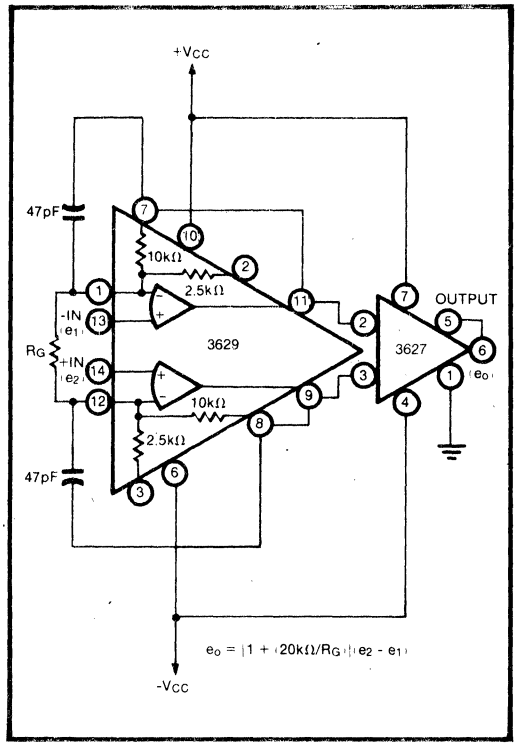


FIGURE 6. 3629 In a Composite Instrumentation Amplifier.

TRANSDUCER APPLICATION

A bridge transducer, Figure 7, with a 0 to 0.1V output requires amplification to interface with a 0 to 10V range system. The bridge introduces a 100Ω source imbalance and 0.25V of 60Hz noise is present on the ground return. Operating temperature range is 10°C to 50°C.

Absolute gain and offset errors can be trimmed to zero. The remaining error sources are tabulated in Table I as a percent of full scale.

TABLE I. Transducer Application Error Analysis.

	Absolute Error		Resolution Error	
	Max	Typ	Max	Typ
Gain Nonlinearity	0.004%	0.002%	0.004%	0.002%
CMR	0.008%	0.0063%	0.008%	0.0063%
Noise 0.1Hz to 10Hz	0.0012%	0.0012%	0.0012%	0.0012%
Voltage Offset Drift	0.032%	0.020%		
Offset Current Drift	0.0048%	0.0024%		
Gain Drift	0.18%	0.08%		
TOTAL	0.230%	0.1119%	0.0132%	0.0095%

The 3629 Instrumentation Amplifier is, therefore, capable of 1 2LSB resolution in a 12-bit system over a 10°C to 50°C range and will produce 8-bit accuracy over the full temperature range.

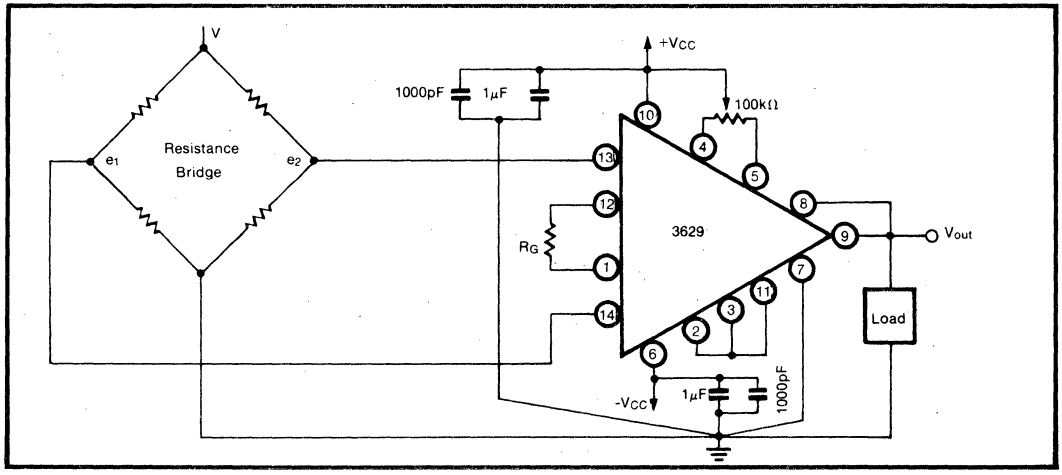
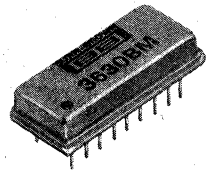


FIGURE 7. 3629 Used in a Transducer Application.

BURR-BROWN®

3630



Very High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- ULTRA LOW VOLTAGE DRIFT - 0.25μV/°C
- LOW BIAS CURRENT - 20nA
- LOW NOISE - 1.2μV p-p
- HIGH INPUT IMPEDANCE - 10 x $10^9\Omega$
- HIGH CMR - 106dB @ 60Hz
- LOW OFFSET VOLTAGE - 25μV
- LOW NONLINEARITY - 0.002%

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:

  Strain Gages
  Thermocouples
  RTDs

- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS

DESCRIPTION

The 3630 is a high accuracy, multi-stage, integrated circuit instrumentation amplifier designed for signal conditioning requirements where very high performance is desired.

A multi-stage design is used to provide excellent specifications and maximum versatility at reasonable cost. The input stage uses Burr-Brown's ultra-low drift low noise monolithic operational amplifiers to provide outstanding input characteristics.

All resistors are on a single network of Nichrome deposited on silicon. This provides high initial accuracy low TCR (temperature coefficient of resistance) and TCR matching, and outstanding stability as a function of time.

State-of-the-art laser-trimming techniques are used for reduction of offset voltage, offset voltage drift versus temperature, and for maximizing common-mode rejection.

In addition to providing an outstanding set of specifications, the 3630 offers convenience and ease of use in providing the following features: single capacitor active low pass filtering; easy output biasing (zero suppression and elevation); common-mode voltage generation for active guard drive; conveniently increased output current capability.

The unit is packaged in an 18-pin metal hermetic dual-in-line package which provides shielding, ease of installation, and environmental ruggedness.

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DISCUSSION

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are closed loop gain blocks whose committed circuitry accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high input impedances.

THE 3630

A simplified schematic of the 3630 is shown in Figure 1. It is a three-stage device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found on integrated circuit instrumentation amplifiers.

The input stage (A1 and A2) consists of two of Burr-Brown's premium grade high accuracy bipolar operational amplifiers. They are connected in the noninverting configuration to provide the high input impedance ($10 \times 10^9 \Omega$) desirable in the instrumentation amplifier function. The inherent low offset voltage and low offset voltage drift versus temperature of these amplifiers is improved even further by the state-of-the-art laser-trimming techniques.

The second stage (A3) consists of a high quality operational amplifier connected in a unity gain difference amplifier configuration. A critical part of this stage is the matching of the four 10k ohm resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to maintain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the resistors shown in Figure 1 are part of a single thin-film network of Nichrome deposited on a passivated silicon substrate. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. The single network approach provides the excellent TCR (temperature coefficient of resistance) and TCR tracking desirable to provide gain accuracy and common-mode rejection when the 3630 is operated over wide temperature ranges.

The third stage (A4) of the 3630 adds a great deal of versatility and convenience to the amplifier. Its use allows easy implementation of active low pass filtering, output offsetting, and additional gain generation. The pin connections make the use of this stage optional but the effects are included in electrical specifications.

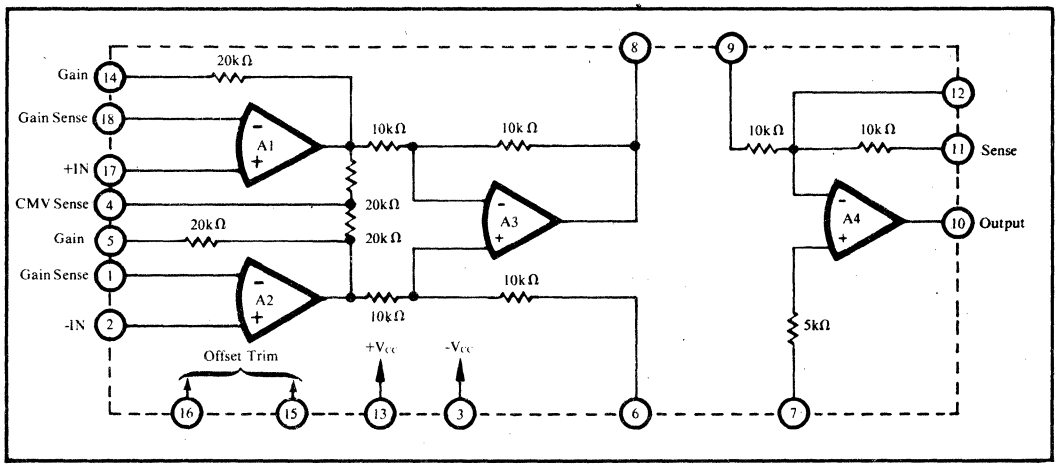


FIGURE 1. Simplified Schematic

USING THE 3630

Figure 2 shows the simplest configuration of the 3630. The gain is set by the external resistor R_G with a gain equation $G = 1 + 40k/R_G$. A low TCR resistor should be used for R_G since it contributes directly to the gain accuracy.

Pins 1, 5, 14 and 18 are accessible so that a four terminal connection can be made to R_G. (Pins 1 and 18 are the voltage sense terminals since no signal current flows into the operational amplifiers' inputs.) This may be useful at high gains where the value of R_G becomes small.

The optional offset null capability is shown in Figure 4. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed when the gain is changed. Also, the input drift will be effected by approximately $0.33\mu V/°C$ per $100\mu V$ of input offset voltage nulled.

Output offsetting ("zero suppression" or "zero elevation") may be more easily accomplished with the 3630 than with most other IC instrumentation amplifiers.

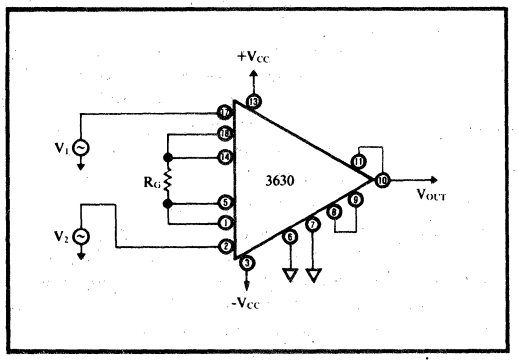


FIGURE 2. Basic Connections

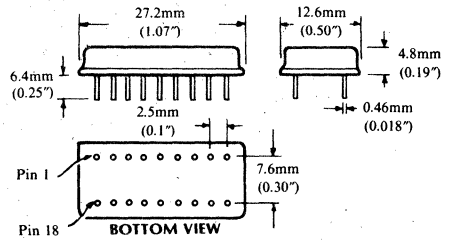
Figure 5 shows how this is done. The use of the noninverting input of the output stage means that CMR of the second stage is not disturbed and that any convenient value of variable resistor can be used.

The output stage also allows active low pass filtering to be implemented conveniently with a single capacitor. The effect this filtering has on noise reduction can be seen in the Typical Performance Curves.

The input stage contains extra resistors for the computation of input common-mode voltage. Figure 7 shows how this voltage, available at pin 4, can be used to drive the shield of the input cable. Since the cable is driven at the common-mode voltage the effects of distributed capacitance is reduced and the AC system common-mode rejection may be improved. Amplifier A1 is a buffer to supply larger currents than can be supplied by the $20k\Omega$ resistors internally connected to pin 4.

Figure 8 shows how the output stage may be used to provide additional gain. If gains greater than 1000V/V are desired it is better to obtain them from the output stage than the input stage due to the low values of R_G required ($R_G < 40\Omega$ for $(1 + 40k/R_G) > 1000$).

MECHANICAL



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

FIGURE 3. Mechanical Specifications

PIN DESIGNATIONS

1. Gain Sense
2. Inverting Input
3. Negative Supply
4. Common-mode Voltage Sense
5. Gain
6. Ground
7. Reference
8. Output of A_3
9. Input to A_4
10. Output
11. Sense
12. Summing Junction of A_4
13. Positive Supply
14. Gain
15. Offset Trim
16. Offset Trim
17. Noninverting Input
18. Gain Sense

ELECTRICAL SPECIFICATIONS

Specifications typical at 25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

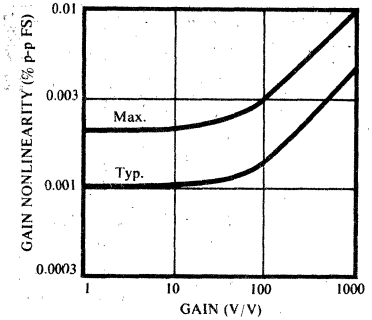
MODEL	3630AM			3630BM, 3630SM			3630CM			Units
	min	typ	max	min	typ	max	min	typ	max	
GAIN										
Range of Gain	1		1000	*		*	*		*	V/V
Gain Equation		$G = 1 + 40k/R_G$			*			*		V/V
Error From Equation, DC		(±0.05 ±0.0001G)	(±0.1 ±0.0002G)		(±0.02 ±0.00005G)	(±0.05 ±0.0001G)		(±0.02 ±0.00005G)	(±0.05 ±0.0001G)	%
Gain Temp. Coefficient[1]										
G = 1		8	20		*	*		*	*	ppm/°C
G = 10		45	115		*	*		*	*	ppm/°C
G = 100		50	125		*	*		*	*	ppm/°C
G = 1000		50	125		*	*		*	*	ppm/°C
Nonlinearity, DC		±(0.002 + 10^{-5}G)	±(0.005 + 2 x 10^{-5}G)		±(0.001 + 4 x 10^{-6}G)	±(0.002 + 10^{-5}G)		±(0.001 +4 x 10^{-6}G)	±(0.002 + 10^{-5}G)	% of p-p FS
RATED OUTPUT										
Voltage	±10	±12.5		*	*		*	*		V
Current	±5	±12.5		*	*		*	*		mA
Output Impedance		0.01			*			*		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at 25°C[2]		±25 ±200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	μV
vs. Temperature			±2 ±20/G			±0.75 ±10/G			±0.25 ±10/G	μV/°C
vs. Supply		±(1 + 20/G)			*			*		μV/V
vs. Time		±(1 + 20/G)			*			*		μV/mo
INPUT BIAS CURRENT										
Initial Bias Current (each input)		±15	±50		±10	±30		±5	±20	nA
vs. Temperature		±0.3			*			*		nA/°C
vs. Supply		±0.1			*			*		nA/V
Initial Offset Current		±15	±50		±10	±30		±5	±20	nA
vs. Temperature		±0.5			*			*		nA/°C
INPUT IMPEDANCE										
Differential		10 x 10^9 || 3			*			*		Ω || pF
Common-mode		10 x 10^9 || 3			*			*		Ω || pF
INPUT VOLTAGE RANGE										
Range, Linear Response	±10	±12		*	*		*	*		V
CMR w/1kΩ Source Imbal.										
DC to 60Hz, G = 1	80	90		*	*		*	*		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		dB
INPUT NOISE										
Voltage, p-p, 0.01Hz - 10Hz		1.2			*			*		μV p-p
rms, 10Hz - 1.0kHz		1.0			*			*		μV rms
Current, p-p, 0.01Hz - 10Hz		70			*			*		pA p-p
rms, 10Hz - 1.0kHz		20			*			*		pA rms
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness,										
G = 1		150			*			*		kHz
G = 10		90			*			*		kHz
G = 100		25			*			*		kHz
G = 1000		2.5			*			*		kHz
Small Signal, ±1% Flatness,										
G = 1		20			*			*		kHz
G = 10		10			*			*		kHz
G = 100		1			*			*		kHz
G = 1000		200			*			*		Hz
Full Power, G = 1 - 100		7.5			*			*		kHz
Slew Rate, G = 1 - 100	0.2	0.5		*	*		*	*		V/μsec
Settling Time (0.1%)										
G = 1		60			*			*		μsec
G = 100		100			*			*		μsec
G = 1000		500			*			*		μsec
Settling Time (.01%)										
G = 5		100			*			*		μsec
G = 100		150			*			*		μsec
G = 1000		1000			*			*		μsec
POWER SUPPLY										
Rated Voltage		±15			*			*		V
Voltage Range	±5		±20	*		*	*		*	V
Current, Quiescent		±8	±14		*	*		*	*	mA
TEMPERATURE RANGE										
Specification[3]	-25		+85	*		*	*		*	°C
Operation	-55		+125	*		*	*		*	°C
Storage	-65		+150	*		*	*		*	°C

NOTES:
1. With R_G TCR = 0 ppm/°C
2. Trimmable to zero at any one gain.
3. -55°C to +125°C for 3630SM.

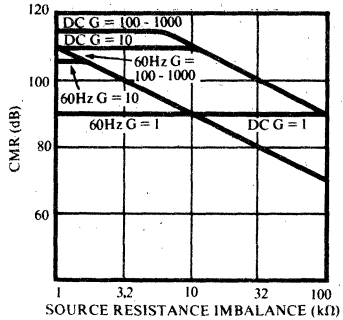
*Specifications same as for 3630AM

TYPICAL PERFORMANCE CURVES

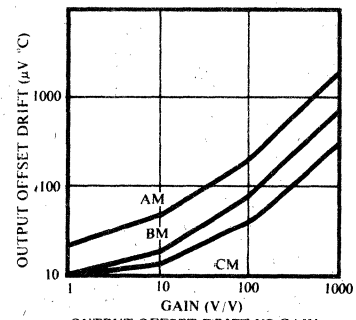
At 25°C and in circuit of Figure 2 unless otherwise noted.



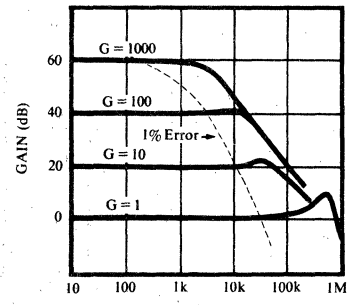
GAIN NONLINEARITY VS GAIN



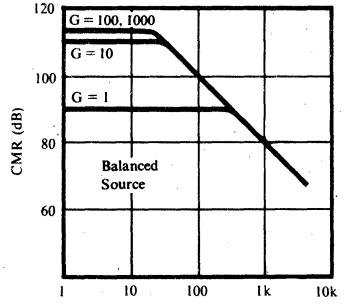
CMR VS SOURCE IMBLANCE



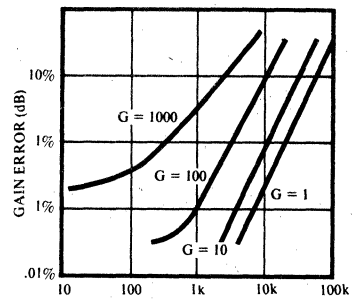
OUTPUT OFFSET DRIFT VS GAIN



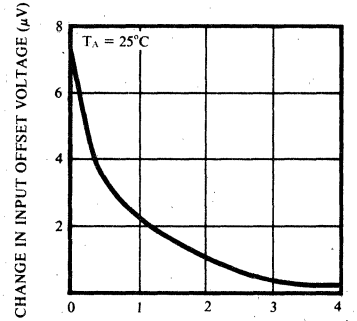
GAIN VS FREQUENCY



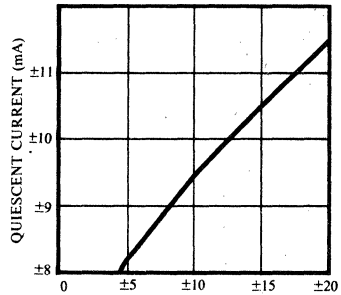
CMR VS FREQUENCY



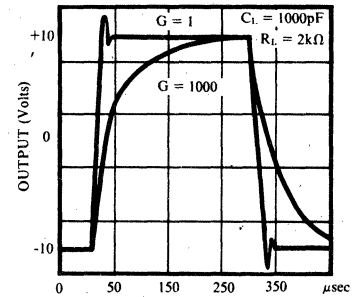
GAIN ERROR VS FREQUENCY



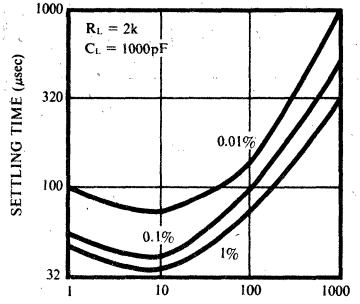
WARM-UP DRIFT VS TIME



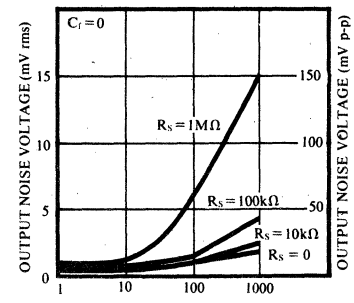
QUIESCENT CURRENT VS SUPPLY



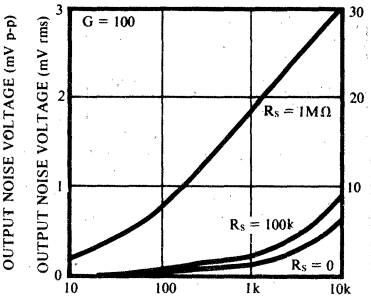
STEP RESPONSE



SETTLING TIME VS GAIN



OUTPUT NOISE VS GAIN



OUTPUT NOISE VS 3dB FREQUENCY

APPLICATIONS

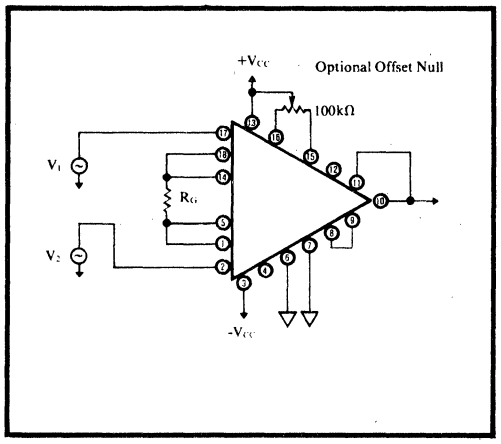


FIGURE 4. Optional Offset Null

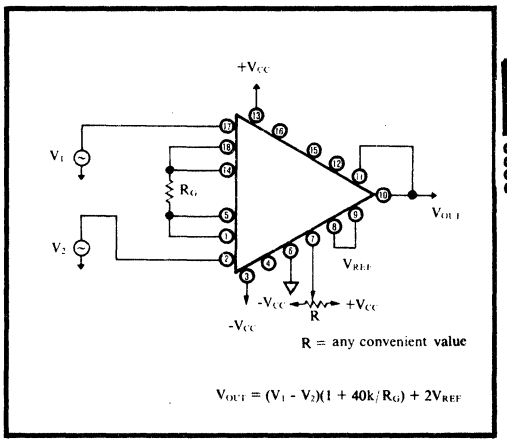


FIGURE 5. Output Offsetting

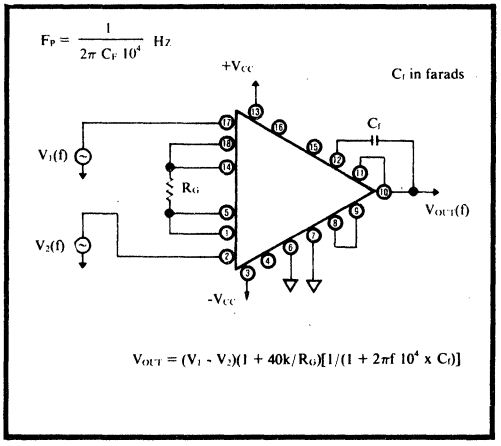


FIGURE 6. Active Low Pass Filtering

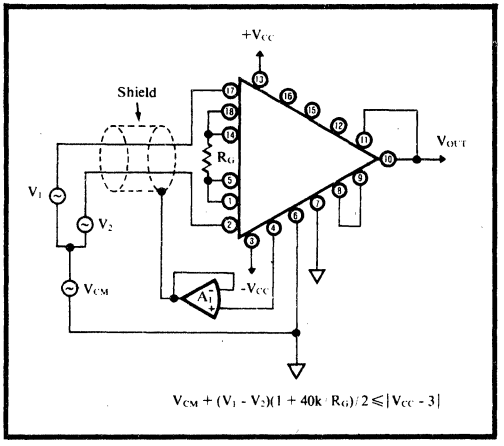


FIGURE 7. Use of Guard Drive

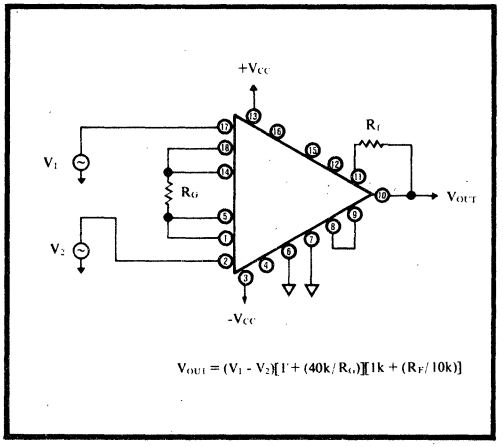


FIGURE 8. Additional Gain From Output Stage

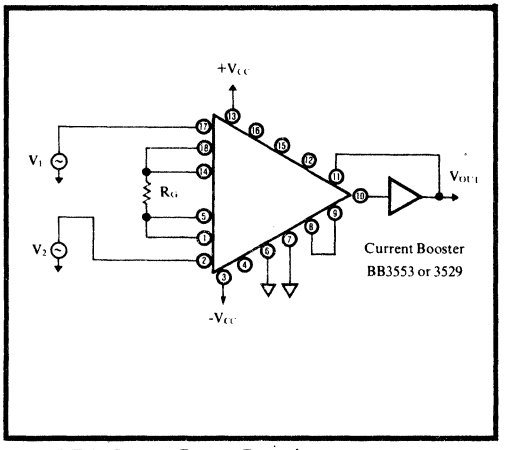
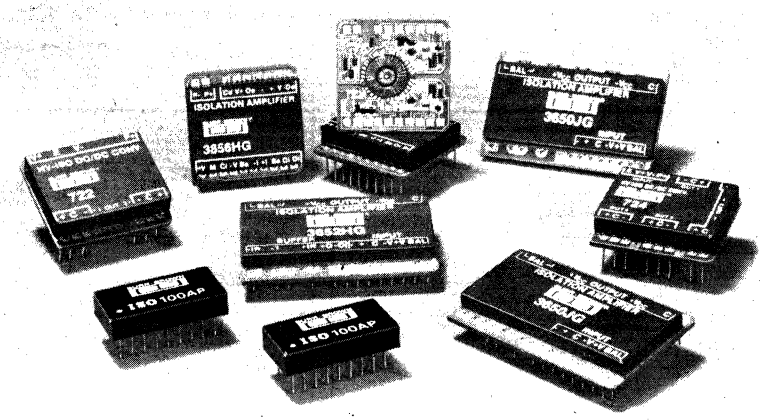


FIGURE 9. Output Power Boosting

ISOLATION AMPLIFIERS



WHAT IS AN ISOLATION AMPLIFIER?

An isolation amplifier is a device with the primary function of providing ohmic isolation (break the ohmic continuity of electrical signal) between the input signal/circuitry and the output of the amplifiers. It usually consists of an input operational amplifier or instrumentation amplifier followed by a unity-gain isolation stage. The sole purpose of the unity-gain isolation stage is to completely isolate the input from the output of the device. Ideally, the ohmic continuity of the input signal is broken (at the isolation barrier) yet accurate signal transfer without any attenuation is achieved across the unity-gain isolation stage. An important feature of an isolation amplifier is that it has a completely floating input which helps eliminate cumbersome connections to source ground in several applications.

Figures 1 and 2 show typical isolation amplifier applications. The isolation-mode voltage V_{iso} is the voltage which exists across the isolation barrier. The contribution of the output referred error caused by V_{iso} is (V_{iso}/IMRR) x Gain where IMRR is the Isolation Mode Rejection Ratio. V_{sig} is the differential input signal and V_{cm} is the common-mode voltage. The "Leakage Current" is the current which flows across the isolation barrier with some specified isolation voltage applied between the input and the output.

CHARACTERISTICS OF ISOLATION AMPLIFIERS

The following is a discussion of some of the characteristics and terms unique to isolation amplifiers.

Common-mode Voltage and Isolation Voltage - Some manufacturers (other than Burr-Brown) treat common-mode voltage and isolation voltages synonymously in describing the use and/or specifications of isolation amplifiers. It is important to understand the significance of these terms and the difference between them.

When the input common is grounded, the input signal V_d (see Figure 1) can be floated by the amount V_{cm} above the input ground. V_{cm} is the common-

mode voltage (CMV) and is generally ±10V, limited by the CMV rating of the input stage amplifier. In applications involving higher systems common-mode voltages, input common terminal is not grounded and the common-mode voltages are referenced across the isolation barrier to the output common terminal.

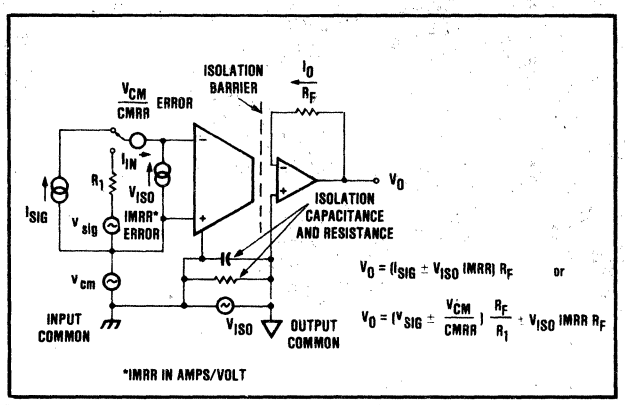


FIGURE 1. Typical Isolation Amplifier, Current (Input) Mode.

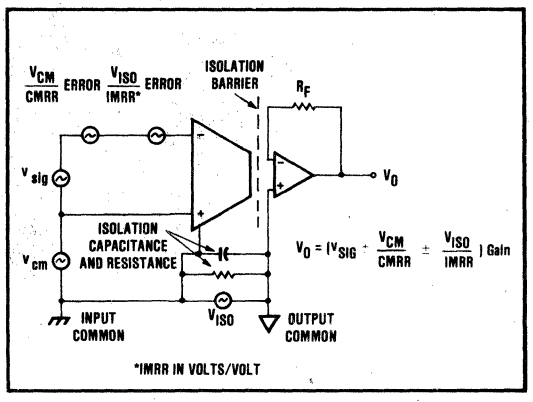


FIGURE 2. Typical Isolation Amplifier, Voltage (Input) Mode.

The isolation voltage V_{iso} as shown in Figure 1 is the potential difference between the input common and the output common terminals. The isolation voltage rating describes the amount of voltage that the isolation barrier can withstand without breakdown. This feature of the isolation amplifier allows two distinct ground connections to be made when necessary. It allows the isolation amplifier to be used in applications involving very-high common-mode voltages and in applications of breaking ground loops.

Many applications involve a large "system common-mode voltage." In such applications, the isolation amplifier's input common terminal is not connected to any ground but the output common terminal is connected to the system ground. In such a case, the term V_{cm} shown in Figures 1 and 2 becomes negligible and V_{iso} determines the safe limit for the system common-mode voltage. In this manner, the isolation amplifier can accommodate common-mode voltages of 2000V or more.

Common-mode Rejection and Isolation Rejection - Isolation-mode rejection (IMR) is another term which some other manufacturers refer to as common-mode rejection (CMR). The above discussion on the common-mode voltage and isolation voltage helps recognize the difference between CMR and the IMR. The CMR is the measure of the input stage amplifier's ability to reject common-mode input signals (common-mode with reference to the output common) while transmitting the differential signal across the isolation barrier. The isolation-mode rejection ratio (IMRR) is defined by the equation shown in Figures 1 and 2. Thus, understanding the IMR capability of isolation amplifiers allows their meaningful use in applications requiring very high common-mode rejection ratios such as 100dB to 140dB.

Isolation Voltage Ratings, Test Voltage - It is important to understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated minimum specification?" There are several rules of thumb used throughout the industry to establish this relationship. For most isolation amplifiers, Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous the user may chose to use a less conservative derating to establish a specification from the test voltage.

APPLICATIONS OF ISOLATION AMPLIFIERS

When one or more of the following conditions/requirements are present in an application, an isolation amplifier would generally be the right choice as a signal conditioning device:

- When ohmic isolation between the signal source and the output is a requirement (isolation impedance between the input and the output $> 10M\Omega$).
- When excellent common-mode noise and voltage rejection is a requirement (CMR $>$ 100dB).
- When it is necessary to process signals in the presence of, or riding on, high common-mode voltages (CMV $\gg$ 10V).

In general, most applications can be broadly categorized into the following four types:

- Amplifying and measuring low level signals in the presence of high common-mode voltages.
- Breaking ground loops and/or eliminating source ground connections. The isolation amplifier provides full floating input, eliminating the need for connections to source ground, and thus allows two-wire hook-up to the signal sources.
- Providing an interface between medical patient monitoring equipment and the transducer/devices which may be in physical contact with the patients. Such applications require high isolation voltage levels and very-low leakage currents.
- Providing isolation protection to electronic instruments/equipment. Large common-mode voltages occasionally cause hazardous electronic faults. Low leakage currents and high isolation voltage capability of isolation amplifiers help protect instruments against damage caused by such faults.

Isolation amplifier performance requirements vary significantly, depending on the type of requirement. In applications where bandwidth and speed of response are more important than gain accuracy and linearity, the optically-coupled amplifiers will be the best choice. For applications where gain accuracy and linearity are key parameters, Burr-Brown's family of transformer-coupled amplifiers are the suitable choice.

*Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111.

SELECTION GUIDE

Description	Model	Isolation Voltage (V) Continuous, peak	Isolation Voltage (V) Pulse/Test, peak	Isolation Mode Rejection, min. DC (dB)	Isolation Mode Rejection, min. 60Hz (dB)	Leakage Current at Test Voltage (μA)	Isolation Impedance Ω	Isolation Impedance pF	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift ±μV/°C max	Bias Current max	±3dB Freq. kHz	External Isolation Power Required	Temp. Range [1]	Package	Page
TRANSFORMER COUPLED AMPLIFIERS																	
Low Drift[2]	3450	±500	±2000	160	120	1	10^{12}	16	±0.005	±0.0015	100	50nA	1.5	No	Com	Module	3-19
Low Bias FET	3451	±500	±2000	160	120	1	10^{12}	16	±0.025	±0.005	100	25pA	2.5	No	Com	Module	3-19
	3452	±2000	±5000	160	120	1	10^{12}	16	±0.025	±0.005	100	10pA	2.5	No[4]	Com	Module	3-19
	3455	[3]	[3]	160	120	[3]	10^{12}	16	±0.025	±0.005	100	20pA	2.5	No[4]	Com	Module	3-19
True 3-wire Instrumentation Amplifier	3656A	±2000	±5000	160	130	25	10^{12}	14	±0.02	±0.01	2 + (150/G_1)	50nA	2.5	No	Com	Module	3-27
	3656B	±2000	±5000	160	130	25	10^{12}	14	±0.08	±0.03	1 + (75/G_1)	50nA	2.5	No	Com	Module	3-27
Highest Isolation Voltage	3656AG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	25 + (500/G_1)	100nA	30	No	Ind	DIP	3-41
	3656BG	±3500	±8000	160	125	0.5	10^{12}	6	±0.05	±0.03	5 + (1000/G_1)	100nA	30	No	Ind	DIP	3-41
	3656HG	±3500	±8000	160	125	0.5	10^{12}	6	±0.15	±0.03	200 + (1000/G_1)	100nA	30	No	Com	DIP	3-41
	3656JG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	50 + (750/G_1)	100nA	30	No	Com	DIP	3-41
	3656KG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	10 + (350/G_1)	100nA	30	No	Com	DIP	3-41
OPTICALLY COUPLED AMPLIFIERS																	
Balanced Current Input	3650HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	25	10nA	15	Yes	Ind	DIP	3-33
	3650JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.03	10	10nA	15	Yes	Ind	DIP	3-38
	3650KG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.05	±0.02	5	10nA	15	Yes	Ind	DIP	3-33
	3650MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100	10nA	15	Yes	Ind	DIP	3-33
Balanced FET Input	3652HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	50	50nA	15	Yes	Ind	DIP	3-33
	3652JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.05	25	50nA	15	Yes	Ind	DIP	3-33
	3652MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100	50nA	15	Yes	Ind	DIP	3-33
Low Drift	ISO100AP	750	2500	146[6]	108[6]	0.3	10^{12}	2.5	0.4	0.1	10[6]	10nA	60	Yes	Ind	DIP	3-6
Wide Bandwidth	ISO100BP	750	2500	146[6]	108[6]	0.3	10^{12}	2.5	0.1	0.01	4[6]	10nA	60	Yes	Ind	DIP	3-6
	ISO100CP	750	2500	146[6]	108[6]	0.3	10^{12}	2.5	0.07	0.02	4[6]	10nA	60	Yes	Ind	DIP	3-6

NOTES: (1) Com = 0°C to +70°C; Ind = −25°C to +85°C. (2) Bipolar. (3) Isolation voltage tested at 2500V, rms, 60Hz; leakage current tested for 2μA max at 240V, rms, 60Hz. (4) ±15V at ±15mA isolated power available to power external circuitry. (5) At 240V/60Hz. (6) R_{IN} = 10k, Gain =100.

GLOSSARY OF TERMS & DEFINITIONS
Isolation Amplifiers

ISOLATION AMPLIFIER

A device which provides ohmic isolation (breaks ohmic continuity of an electric signal) between the input and the output of the device. Method of coupling may be thermal, magnetic, optical, or any means other than direct ohmic coupling. Such a device allows the input circuit to be referenced separately and independent of the output circuitry.

ISOLATION BARRIER

A barrier or region between the input and the output stage of an isolatiom amplifier, where the signal transfer is achieved between the input and the output.

ISOLATION IMPEDANCE

The effective impedance between the input common terminal and the output common terminal. It is the impedance of the isolation barrier. (It is usually specified as a typical parameter. Leakage current is related to isolation impedance and is usually specified with a maximum limit.)

ISOLATION-MODE REJECTION (IMR)

The IMR is the measure of an isolation amplifier's ability to reject common-mode input signals (common-mode with reference to the output common), while transmitting the differential signal across the isolation barrier. It is the voltage or current that must be applied to the input to force the output to zero when V_{iso} is present.

For voltage input mode:

$$\text{IMRR} = \frac{V_{o\ \text{error ISO}}/G}{V_{iso}} \quad \text{with } V_o = 0$$

For current input mode:

$$\text{IMRR} = \frac{I_{o\ \text{error ISO}}}{V_{iso}} \quad \text{with } V_o = 0\ (I_o = 0)$$

ISOLATION VOLTAGE

The potential difference between the input stage common and output stage common terminals of an isolation amplifier.

ISOLATION VOLTAGE RATING

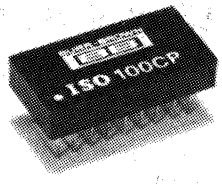
The amount of voltage that can be impressed between the input common and the output common terminals (across the isolation barrier) without resulting in breakdown.

LEAKAGE CURRENT

The current that flows between the input common terminal and the output common terminal (across the isolation barrier) with a specified voltage applied across it. (It is usually 100% tested and specified with a maximum limit.)

BURR-BROWN®

ISO100



Miniature
Low Drift - Wide Bandwidth
ISOLATION AMPLIFIER

FEATURES

- EASY TO USE, SIMILAR TO AN OP AMP
  $V_{OUT}/I_{IN} = R_F$, Current Input
  $V_{OUT}/V_{IN} = R_F/R_{IN}$, Voltage Input
- 100% TESTED FOR BREAKDOWN
  750V Continuous Isolation Voltage
- ULTRA-LOW LEAKAGE, 0.3μA, max, at 240V/60Hz
- WIDE BANDWIDTH, 60kHz
- LOW COST
- 18-PIN DIP PACKAGE

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer sensing
  (thermocouple, RTD, pressure bridges)
  4mA to 20mA loops
  Motor and SCR control
  Ground loop elimination
- BIOMEDICAL MEASUREMENTS
- TEST EQUIPMENT
- DATA ACQUISITION

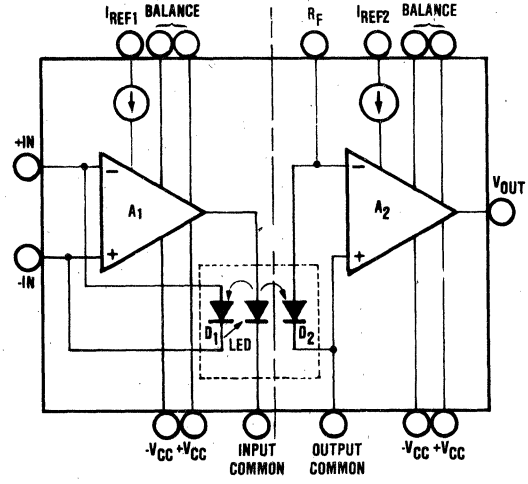
DESCRIPTION

The ISO100 is a miniature low cost optically-coupled isolation amplifier. High accuracy, linearity, and time-temperature stability are achieved by coupling light from an LED back to the input (negative feedback) as well as forward to the output. Optical components are carefully matched and the amplifier is actively laser-trimmed to assure excellent tracking and low offset errors.

The circuit acts as a current-to-voltage converter with a minimum of 750V (2500V test) between input and output terminals. It also effectively breaks the galvanic connection between input and output commons as indicated by the ultra-low 60Hz leakage current of 0.3μA at 240V. Voltage input operation is easily achieved by using one external resistor.

Versatility along with outstanding DC and AC performance provide excellent solutions to a variety of challenging isolation problems. For example, the ISO100 is capable of operating in many modes, including: noninverting (unipolar and bipolar) and inverting (unipolar and bipolar) configurations. Two precision current sources are provided to accomplish bipolar operation. Since these are not required for unipolar operation, they are available for external use (see Applications section).

Designs using the ISO100 are easily accomplished with relatively few external components. Since V_{OUT} of the ISO100 is simply $I_{IN}R_{OUT}$, gains can be changed by altering one resistor value. In addition, the ISO100 has sufficient bandwidth (DC to 60kHz) to amplify most industrial and test equipment signals.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

PARAMETER	CONDITIONS	ISO100AP MIN	ISO100AP TYP	ISO100AP MAX	ISO100BP MIN	ISO100BP TYP	ISO100BP MAX	ISO100CP MIN	ISO100CP TYP	ISO100CP MAX	UNITS
ISOLATION											
Voltage,											
Rated Continuous, AC peak or DC[1]		750			*			*			V
Test Breakdown, AC peak or DC	10sec	2500			*			*			V
Rejection[2] DC			5			*			*		pA/V
	R_{IN} =10kΩ, Gain = 100		146			*			*		dB
AC	60Hz, 480V, R_F = 1MΩ		400			*			*		pA/V
	R_{IN} = 10kΩ, Gain = 100		108			*			*		dB
Impedance			$10^{12} \| 2.5$			*			*		Ω || pF
Leakage Current	240V, rms, 60Hz			0.3			*			*	μA, rms
OFFSET VOLTAGE (RTI)											
Input Stage (V_{OSI})											
Initial Offset				500			300			200	μV
vs Temperature				5			2			2	μV/°C
vs Input Power Supplies				105			*			*	dB
vs Time			1			*			*		μV/kHr
Output Stage (V_{OSO})											
Initial Offset				500			300			200	μV
vs Temperature				5			2			2	μV/°C
vs Output Power Supplies				105			*			*	dB
vs Time			1			*			*		μV/kHr
Common-Mode Rejection Ratio[2]	60Hz, R_F = 1MΩ		3			*			*		nA/V
	R_{IN} = 10kΩ, Gain = 100		90			*			*		dB
Common-Mode Range	±10				*			*			V
REFERENCE CURRENT SOURCES											
Magnitude											
Nominal		10.5	12	12.5	*	*	*	*	*	*	μA
vs Temperature				300			300			150	ppm/°C
vs Power Supplies			0.3	3		*	*		*	*	nA/V
Matching											
Nominal			50			*			*		nA
vs Temperature			150			*			*		ppm/°C
vs Power Supplies			0.3			*			*		nA/V
Compliance Voltage	-10			+15	*		*	*		*	V
Output Resistance			2×10^9			*			*		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	Gain = 1V/μA		60			*			*		kHz
Full Power Bandwidth	Gain = 1V/μA, V_O = ±10V		5			*			*		kHz
Slew Rate		0.22	0.31		*	*		*	*		V/μsec
Settling Time	0.1%		100			*			*		μsec
TEMPERATURE RANGE											
Specification		-25		+85	*		*	*		*	°C
Operating		-40		+100	*		*	*		*	°C
Storage		-55		+100	*		*	*		*	°C
UNIPOLAR OPERATION											
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		-20		-0.02	*		*	*		*	μA
Without Damage		-1		+1	*		*	*		*	mA
Input Impedance			0.1			*			*		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	-10		0	*		*	*		*	V
Output Impedance	DC, open-loop		1200			*			*		Ω
GAIN	$V_O = R_F (I_{IN})$										
Initial Error Adjustable To Zero			2	5		1	2		1	2	% FS
vs Temperature			0.03	0.07		0.01	0.05		0.005	0.03	%/°C
vs Time			0.05			*			*		%/kHr
Nonlinearity[3]			0.1	0.4		0.03	0.1		0.02	0.07	%
CURRENT NOISE	I_{IN} = 0.2μA										
0.01Hz to 10Hz			20			*			*		pA, p-p
10Hz			1			*			*		$pA/\sqrt{Hz}$
100Hz			0.7			*			*		$pA/\sqrt{Hz}$
1kHz			0.65			*			*		$pA/\sqrt{Hz}$
INPUT OFFSET CURRENT (I_{OS})											
Initial Offset			1	10		*	*		*	*	nA
vs Temperature			0.05			*			*		nA/°C
vs Power Supplies			0.1			*			*		nA/V
vs Time			100			*			*		pA/kHr

ELECTRICAL (CONT)

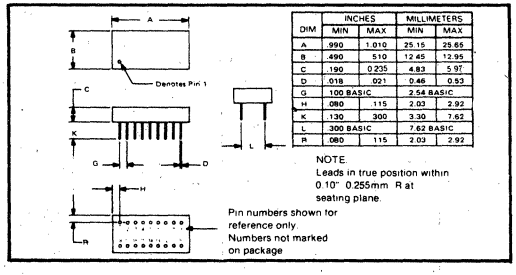
PARAMETER	CONDITIONS	ISO100AP MIN	ISO100AP TYP	ISO100AP MAX	ISO100BP MIN	ISO100BP TYP	ISO100BP MAX	ISO100CP MIN	ISO100CP TYP	ISO100CP MAX	UNITS
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	I_{IN} = -0.02μA		±1.1	±2		*	*		*	*	mA
	I_{IN} = -20μA		+8, -1.1	+13, -2		*	*		*	*	mA
Output Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	V_O = 0		±1.1	±2		*	*		*	*	mA
Short Circuit Current Limit				±40			*			*	mA
BIPOLAR OPERATION											
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		-10		+10	*		*	*		*	μA
Without Damage		-1		+1	*		*	*		*	mA
Input Impedance			0.1			*			*		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	-10		+10	*		*	*		*	V
Output Impedance			1200			*			*		Ω
GAIN	$V_O = R_F (I_{IN})$										
Initial Error (Adjustable To Zero)			2	5		1	2		1	2	% of FS
vs Temperature			0.03	0.07		0.01	0.05		0.005	0.03	%/°C
vs Time			0.05			*			*		%/kHr
Nonlinearity (3)			0.1	0.4		0.03	0.1		0.02	0.07	%
CURRENT NOISE	I_{IN} = 0.2μA										
0.01Hz to 10Hz			1.5			*			*		nA, p-p
10Hz			17			*			*		pA/√Hz
100Hz			7			*			*		pA/√Hz
1kHz			6			*			*		pA/√Hz
INPUT OFFSET CURRENT (Ios, bipolar)(4)											
Initial Offset			40	200		20	70		10	35	nA
vs Temperature				3			2			1	nA/°C
vs Power Supplies				0.7			*			*	nA/V
vs Time			250			*			*		pA/kHr
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	I_{IN} = +10μA		+2, -1.1	+3,-2		*	*		*	*	mA
	I_{IN} = -10μA		+8, -1.1	+13,-2		*	*		*	*	mA
Output Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	V_O = 0		±1.1	±2		*	*		*	*	mA
Short Circuit Current Limit				±40			*			*	mA

* Same as ISO100AP.

NOTES:

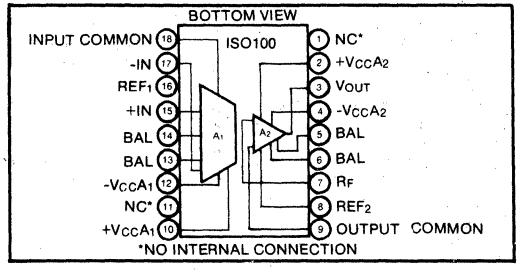
1. See Typical Performance Curves for temperature effects.
2. See Theory of Operation section for definitions. For dB see Ex. 2, CM and HV errors.
3. Nonlinearity is the peak deviation from a "best fit" straight line expressed as a percent of full scale output.
4. Bipolar offset current includes effects of reference current mismatch and unipolar offset current.

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.990	1.010	25.15	25.65
B	.490	.510	12.45	12.95
C	.190	0.235	4.83	5.97
D	.018	.021	0.46	0.53
G	100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

PIN CONFIGURATION



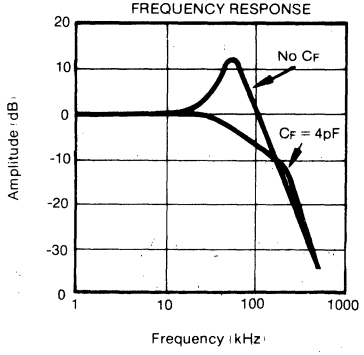
ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±18V
Isolation Voltage	2500V
Input Current	±1mA
Storage Temperature Range	-55°C to +100°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground

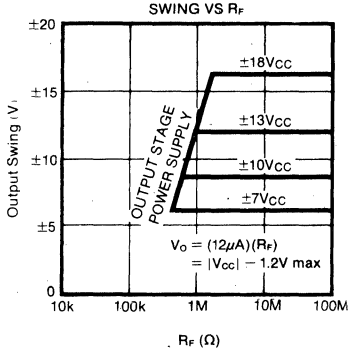
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = 15VDC unless otherwise noted)

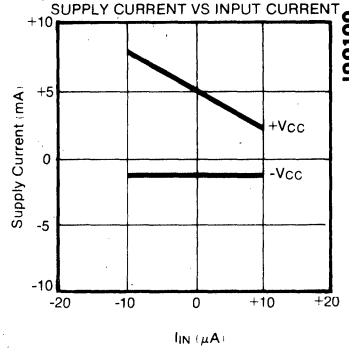
SMALL SIGNAL FREQUENCY RESPONSE



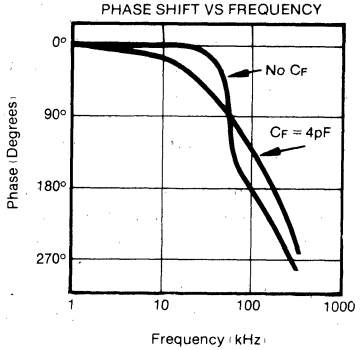
BIPOLAR OUTPUT SWING VS R_F



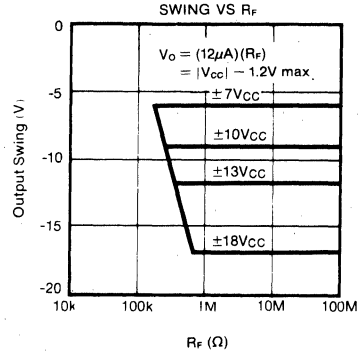
BIPOLAR INPUT STAGE SUPPLY CURRENT VS INPUT CURRENT



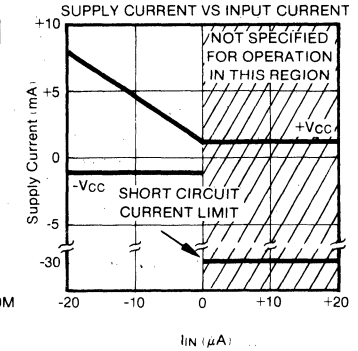
PHASE SHIFT VS FREQUENCY



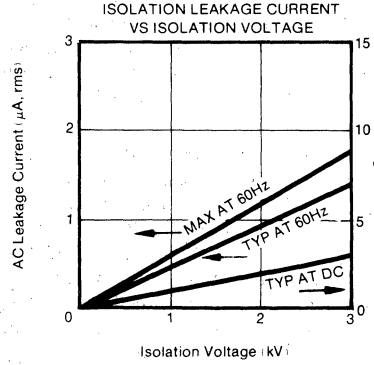
UNIPOLAR OUTPUT SWING VS R_F



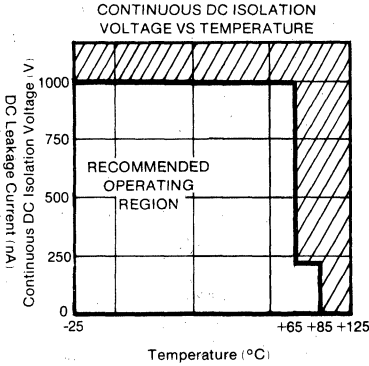
UNIPOLAR INPUT STAGE SUPPLY CURRENT VS INPUT CURRENT



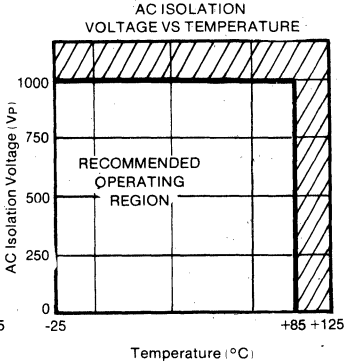
ISOLATION LEAKAGE CURRENT VS ISOLATION VOLTAGE

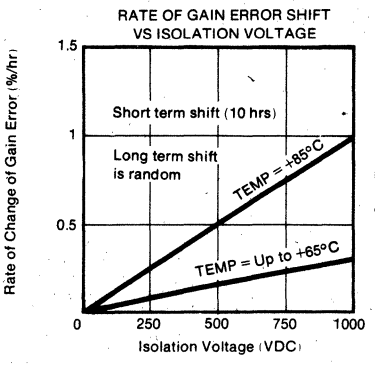


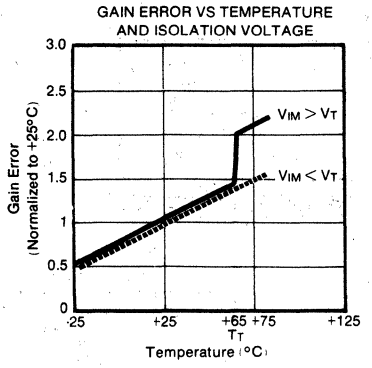
CONTINUOUS DC ISOLATION VOLTAGE VS TEMPERATURE



AC ISOLATION VOLTAGE VS TEMPERATURE







NOTES:
V_T and T_T approximate the threshold for the indicated gain shift. This is caused by the properties of the optical cavity.
T_T ≈ +65°C, V_T ≈ 200VDC. Shift does not occur for AC voltages.
V_{IM} = Isolation-mode Voltage
V_T = Threshold Voltage
T_T = Threshold Temperature

THEORY OF OPERATION

The ISO100 is fundamentally a unity gain current amplifier intended to transfer small signals between electrical circuits separated by high voltages or different references. In most applications an output voltage is obtained by passing the output current through the feedback resistor (R_F).

The ISO100 uses a single light emitting diode (LED) and a pair of photodiode detectors, coupled together, to isolate the output signal from the input.

Figure 1 shows a simplified diagram of the amplifier. I_{REF1} and I_{REF2} are required only for bipolar operation, to generate a midscale reference. The LED and photodiodes (D1 and D2) are arranged such that the same amount of light falls on each photodiode. Thus, the currents generated by the diodes match very closely. As a result, the transfer function depends upon optical match, rather than absolute performance. Laser-trimming of the components improves matching and enhances accuracy, while negative feedback improves linearity. Negative feedback around A1 occurs through the optical path formed by the LED and D1. The signal is transferred across the isolation barrier by the matched light path to D2.

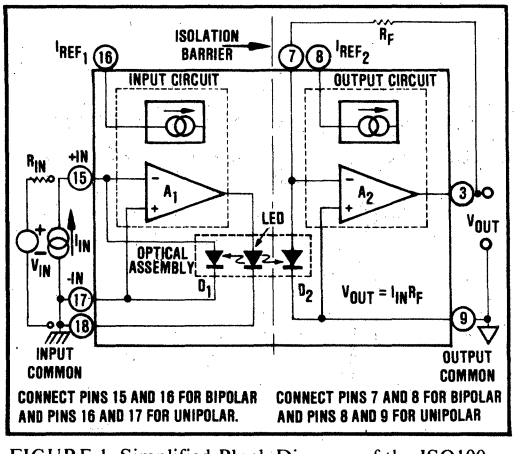


FIGURE 1. Simplified Block Diagram of the ISO100.

The overall ISO amplifier is noninverting (a positive going input produces a positive going output).

INSTALLATION AND OPERATING INSTRUCTIONS

UNIPOLAR OPERATION

In Figure 1, assume a current, I_{IN}, flows out of the ISO100 (I_{IN} must be negative in unipolar operation). This causes the voltage at pin 15 to decrease. Because the amplifier is inverting, the output of A1 increases, driving current through the LED. As the LED light output increases, D1 responds by generating an increasing current. The current increases until the sum of the currents in and out of the input node (-Input to A_1) is zero. At that point the negative feedback through D1 has stabilized the loop, and the current I_{D1} equals the input current plus the bias current. As a result no bias current flows in the source. Since D1 and D2 are matched ($I_{D1} = I_{D2}$), I_{IN} is replicated at the output via D2. Thus, A1 functions as a unity-gain current amplifier, and A2 is a current-to-voltage converter, as described below.

Current produced by D2 must either flow into A2 or R_F. Since A2 is designed for low bias current (≈10nA) almost all of the current flows through R_F to the output. The output voltage then becomes;

$$V_O = (I_{D2})\,R_F = (I_{D1} \pm I_{OS})\,R_F \approx -(-I_{IN})\,R_F = I_{IN}R_F, \quad (1)$$

where, I_{OS} is the difference between A1 and A2 bias currents. For input voltage operation I_{IN} can be replaced by a voltage source (V_{IN}) and series resistor (R_{IN}) since the summing node of the op amp is essentially at ground. Thus, $I_{IN} = V_{IN}/R_{IN}$.

Unipolar operation does have some constraints, however. In this mode the input current must be negative so as to produce a positive output voltage from A1 to turn the LED on. A current more negative than 20nA is necessary to keep the LED turned on and the loop stabilized. When this condition is not met the output may be indeterminant. Many sensors generate unidirectional signals, e.g., photoconductive and photodiode devices, as well as some applications of thermocouples. However, other applications do require bipolar operation of the ISO100.

BIPOLAR OPERATION

To activate the bipolar mode, reference currents as shown in Figure 1, are attached to the input nodes of the op amps. The input stage stabilizes just as it did in unipolar operation. Assuming $I_{IN} = 0$, the photodiode has to supply all the I_{REF1} current. Again, due to symmetry, $I_{D1} = I_{D2}$. Since the two references are matched, the current generated by D2 will equal I_{REF2}. This results in no current flow in R_F, and the output voltage will be zero. When I_{IN} either adds or substracts current from the input node, the current D1 will adjust to satisfy $I_{D1} = I_{IN} + I_{REF1}$. Because I_{REF1} equals I_{REF2} and I_{D1} equals I_{D2}, a current equal to I_{IN} will flow in R_F. The output voltage is then $V_O = I_{IN}R_F$. The range of allowable I_{IN} is limited. Positive I_{IN} can be as large as I_{REF1} (10.5μA, min). At this point, D1 supplies no current and the loop opens. Negative I_{IN} can be as large as that generated by D1 with maximum LED output (recommended 10μA, max).

DC ERRORS

Errors in the ISO100 take the form of offset currents and voltages plus their drifts with temperature. These are shown in Figure 2.

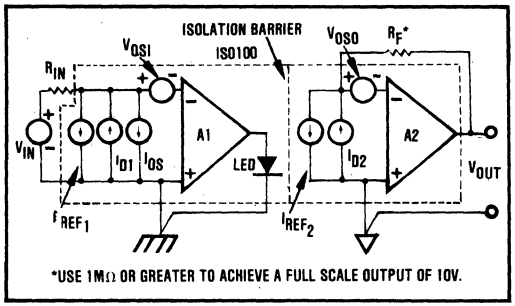


FIGURE 2. Circuit Model for DC Errors in the ISO100.

A1 and A2: are assumed to be ideal amplifiers.

V_{OSO} and V_{OSI}: are the input offset voltages of the output and input stage, respectively. V_{OSO} appears directly at the output, but, V_{OSI} appears at the output as

$$V_{OSI}\frac{R_F}{R_{IN}},$$

see equation (2).

I_{OS}: is the offset current. This is the current at the input necessary to make the output zero. It is equal to the combined effect of the difference between the bias currents of A1 and A2 and the matching errors in the optical components, in the unipolar mode.

I_{REF1} and I_{REF2}: are the reference currents that, when connected to the inputs, enable bipolar operation. The two currents are trimmed, in the bipolar mode, to minimize the $I_{OS\ bipolar}$ error.

I_{D1} and I_{D2}: are the currents generated by each photodiode in response to the light from the LED.

A_e: is the gain error.

$A_e = |\text{Ideal gain}/\text{Actual gain}| - 1$

The output then becomes:

$$V_{OUT} = R_F[(\frac{V_{IN} \pm V_{OSI}}{R_{IN}} - I_{REF1} \pm I_{OS})(1 + A_e) + I_{REF2}] \pm V_{OSO} \quad (2)$$

The total input referred offset voltage of the ISO100 can be simplified by assuming that $A_e = 0$ and $V_{IN} = 0$:

$$V_{OUT} \approx R_F[\frac{\pm V_{OSI}}{R_{IN}} \pm I_{OS} \pm \Delta I_{REF}] \pm V_{OSO} \quad (3)$$

where, $\Delta I_{REF} = I_{REF1} - I_{REF2}$.

This voltage is then referred back to the input by dividing by R_F R_{IN}.

Letting $\Delta I_{REF} - I_{OS} = I_{OS\ bipolar}$,

$$V_{OS(RTI)} = (\pm V_{OSI}) \pm R_{IN}(I_{OS\ bipolar}) + V_{OSO}/(R_F/R_{IN}) \quad (4)$$

Example 1: (Refer to Figure 2 and Electrical Specifications Table)

Given: $R_{IN} = 100k\Omega$, $R_F = 1M\Omega$ (gain = 10),
$V_{OSI} = +200\mu V$.
$I_{OS\ bipolar} = +35nA$, $V_{OSO} = +200\mu V$

Find: The total offset voltage error referred to the input and output when $V_{IN} = 0V$

V_{OS} total RTI $= \pm V_{OSI} \pm R_{IN}$ ($I_{OS\ bipolar}$), $\pm V_{OSO}/(R_F/R_{IN})$
$= +200\mu V + 100k\Omega\ (35nA) + 200\mu V/(1M\Omega/100k\Omega)$
$= 0.2mV + 3.5mV + 0.02mV$
$= 3.72mV$

V_{OS} total RTO $= V_{OS}$ total RTI x RF/RIN
$= 3.72mV$ x 10
$= 37.2mV$

(Note: This error is dominated by $I_{OS\ bipolar}$ This calculation does not include gain error. For total output offset see equation 2).

COMMON-MODE AND HIGH VOLTAGE ERRORS

Figure 3 shows a model of the ISO100 that can be used to analyze common-mode and high voltage behavior.

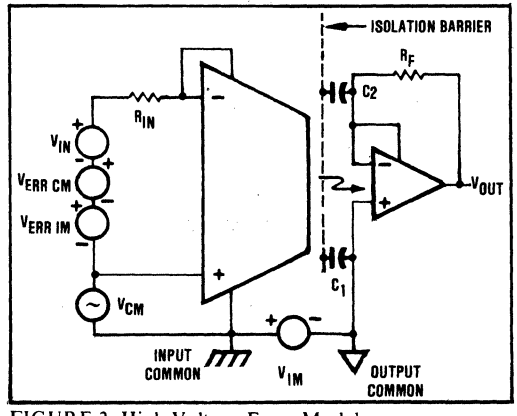


FIGURE 3. High Voltage Error Model.

Definitions of CMR and IMR

I_{OS} is defined as the input current required to make the ISO100's output zero. CMRR and IMRR in the ISO100 are expressed as conductances. CMRR defines the relationship between a change in the applied common-mode voltage (V_{CM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

$$\text{CMRR (I-mode)} = \Delta I_{OS}/\Delta V_{CM} \text{ in nA/V} \quad (5)$$

$$\text{CMRR (V-mode)} = \left[\frac{\Delta I_{OS}}{\Delta V_{CM}}\right] R_{IN} = \frac{\Delta V_{ERR\ CM}}{\Delta V_{CM}} \text{ in V/V} \quad (6)$$

IMRR defines the relationship between a change in the applied isolation mode voltage (V_{IM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

$$\text{IMRR (I-mode)} = \frac{\Delta I_{OS}}{\Delta V_{CM}} \text{ in pA/V} \quad (7)$$

$$\text{IMRR (V-mode)} = \left[\frac{\Delta I_{OS}}{\Delta V_{IM}}\right] R_{IN} = \frac{\Delta V_{ERR\ IM}}{\Delta V_{IM}} \text{ in V/V} \quad (8)$$

CMRR & IMRR in V/V are a function of R_{IN}.

V_{IM} is the voltage between input common and output common.

V_{CM} is the common-mode voltage (noise that is present on both input lines, typically 60Hz).

V_{ERR} is the equivalent error signal, applied in series with the input voltage, which produces an output error identical to that produced by application of V_{CM} and V_{IM}.

CMRR and IMRR are the common-mode and isolation-mode rejection ratios, respectively.

TOTAL CAPACITANCE (C_1 and C_2) is distributed along the isolation barrier. Most of the capacitance is coupled to low impedance or noncritical nodes and affects only the leakage current. Only a small capacitance (C_2) couples to the input of the second stage, and contributes to IMRR.

Example 2: Refer to Figure 3 and Electrical Specification Table)

Given: V_{CM} = 1VAC peak at 60Hz, V_{IM} = 200VDC, CMRR = 3nA/V, IMRR = 5pA/V, R_{IN} = 100kΩ, R_F = 1MΩ (Gain = 10)

Find: The error voltage referred to the input and output when V_{IR} = 0V

$$V_{ERR\ RTI} = (V_{CM})(CMRR)(R_{IN}) + (V_{IM})(IMRR)(R_{IN})$$
$$= 1V\,(3nA/V)\,(100k\Omega) + 200V\,(5pA/V)(100k\Omega)$$
$$= 0.3mV + 0.1mV$$
$$= 0.4mV$$

$$V_{ERR\ RTO} = V_{ERR\ RTI}\,(R_F/R_{IN})$$
$$= 0.4mV\,(10)$$
$$= 4mV \text{ (with DC IMRR)}$$

(Note: This error is dominated by the CMRR term)

For purposes of comparing CMRR and IMRR directly with dB specifications, the following calculations can be performed:

$$\text{CMRR in V/V} = \text{CMRR (I-mode)}(R_{IN})$$
$$= 3nA/V\,(100k) = 0.3mV/V$$

$$\text{CMR} = 20 \text{ LOG } (0.3mV/V) = -70dB \text{ at } 60Hz$$

$$\text{IMRR in V/V} = \text{IMRR (I-mode)}(R_{IN}) = 5pA/V(100k\Omega) = 0.5\mu V/V$$

$$\text{IMR} = 20 \text{ LOG } (0.5 \times 10^{-6} V/V) = -126dB \text{ at DC}$$

Example 3:

In Example 2, V_{IM} is an AC signal at 60Hz and

$$\text{IMRR} = \frac{400pA}{V}$$

$$V_{ERR\ RTI} = V_{ERR\ CM} + V_{ERR\ IM}$$
$$= 0.3mV + 200V\,(400pA/V)(100k\Omega)$$
$$= 8.3mV$$

$$V_{ERR\ RTO} = 83mV \text{ (with AC IMRR)}$$

Example 4:

Given: Total error RTO from Examples 1 and 3 as 120.2mV (with AC IMRR)

Find: Percent error of +10V full scale output

$$\% \text{ Error} = \frac{V_{ERR\ total}}{V_{FS}} \times 100$$
$$= \frac{120.2mV}{10V} \times 100$$
$$= 1.2\%$$

NOISE ERRORS

Noise errors in the unipolar mode are due primarily to the optical cavity. When the full 60kHz bandwidth is not needed, the output noise of the ISO100 can be limited by either a capacitor, C_F, in the feedback loop or by a low-pass filter following the output. This is shown in Figure 4. Noise in the bipolar mode is due primarily to the reference current sources, and can be reduced by the low-pass filters shown in Figure 5.

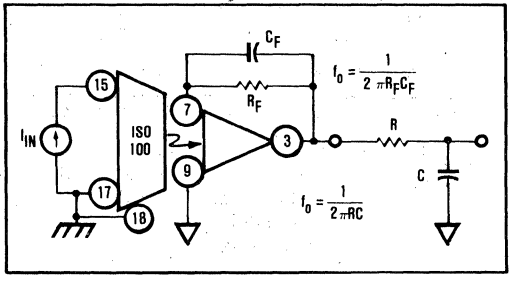


FIGURE 4. Two Circuit Techniques for Reducing Noise in the Unipolar Mode.

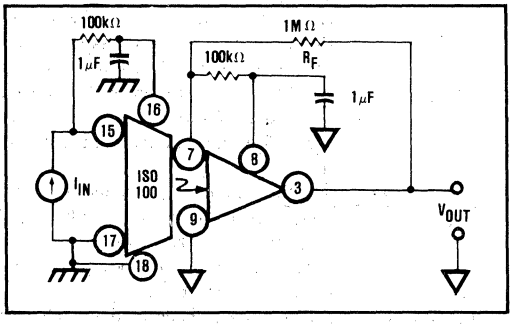


FIGURE 5. Circuit Technique for Reducing Noise from The Current Sources in the Bipolar-Mode.

OPTIONAL ADJUSTMENTS

The offset voltage of the input and output amplifiers generally need no adjustment. However, V_{OSI} and V_{OSO} can be adjusted independently using external potentiometers. An example is shown in Figure 15. Note that V_{OSO} (500μV, max) appears directly at the output, but V_{OSI} appears at the output multiplied by gain (R_F/R_{IN}). In general, one pot, usually at the input, is sufficient.

Adjustment Procedures: In the bipolar mode, set V_{IN} to 0 and adjust the offset potentiometer for a zero output voltage. In the unipolar mode, set I_{IN} to the lowest expected input current, for example 20nA, and adjust the offset potentiometer for an output voltage equal to I_{IN} x R_F.

BASIC CIRCUIT CONNECTIONS

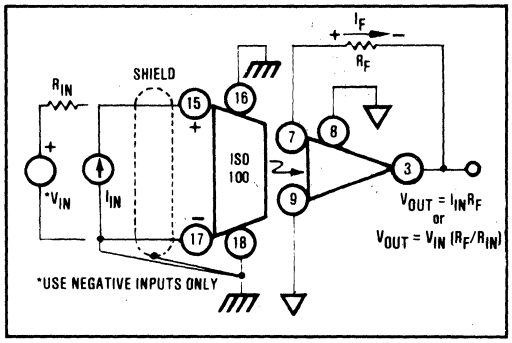


FIGURE 6. Unipolar Noninverting.

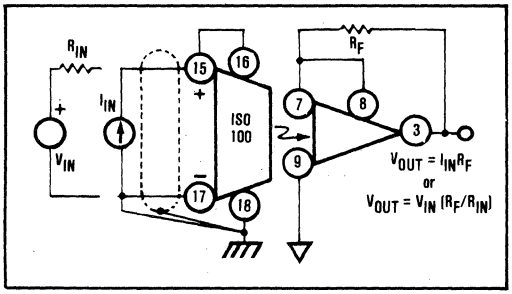


FIGURE 7. Bipolar Noninverting.

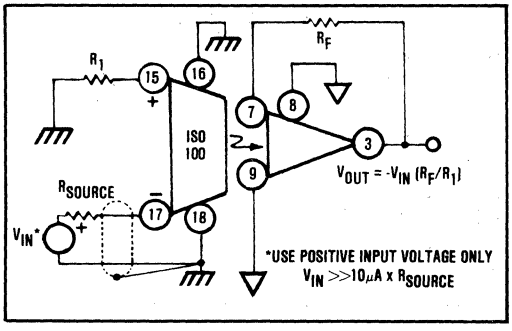


FIGURE 8. Unipolar Inverting.

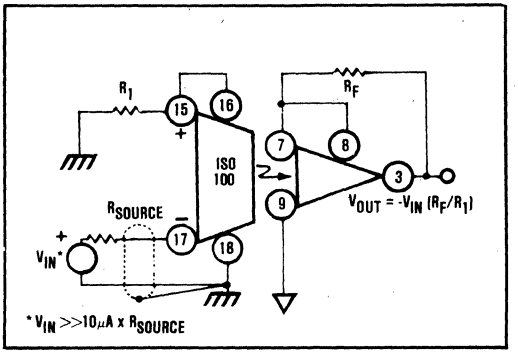


FIGURE 9. Bipolar Inverting.

APPLICATION INFORMATION

The small size, low offset and drift, wide bandwidth, ultra-low leakage, and low cost, make the ISO100 ideal for a variety of isolation applications. The basic mode of operation of the ISO100 will be determined by the type of signal and application.

Major points to consider when designing circuits with the ISO100.

1. Input Common (pin 18) and -IN (pin 17) should be grounded through separate lines. The Input Common can carry a large DC current and may cause feedback to the signal input
2. Use shielded or twisted pair cable at the input, for long lines.
3. Care should be taken to minimize external capacitance across the isolation barrier.
4. The distance across the isolation barrier, between external components, and conductor patterns, should be maximized to reduce leakage and arcing.
5. Although not an absolute requirement, the use of conformally-coated printed circuit boards is recommended.
6. When in the unipolar mode, the reference currents (pins 8 and 16) must be terminated.
7. The noise contribution of the reference currents will cause the bipolar mode to be noisier than the unipolar mode.
8. The maximum output voltage swing is determined by I_{IN} and R_F.

$$V_{SWING} = I_{IN_{max}} \times R_F$$

9. A capacitor (about 3pF) can be connected across R_F to compensate for peaking in the frequency response. The peaking is caused by the pole generated by R_F and the capacitance at the input of the output amplifier.

Figures 10 through 16 show applications of the ISO100.

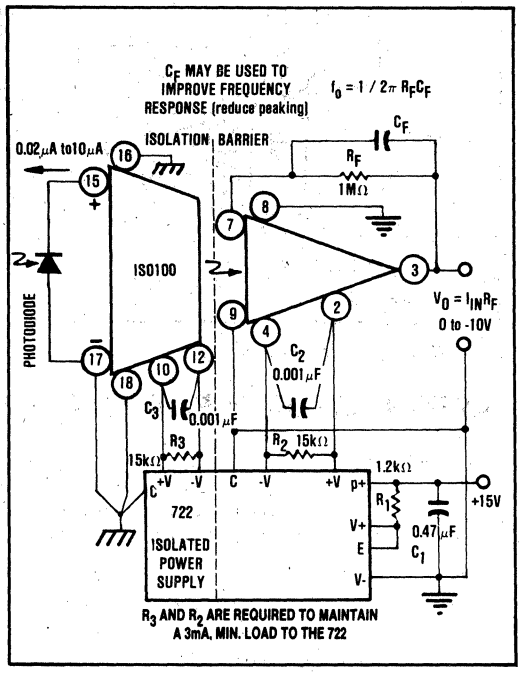


FIGURE 10. Two-Port Isolation Photodiode Amplifier (Unipolar).

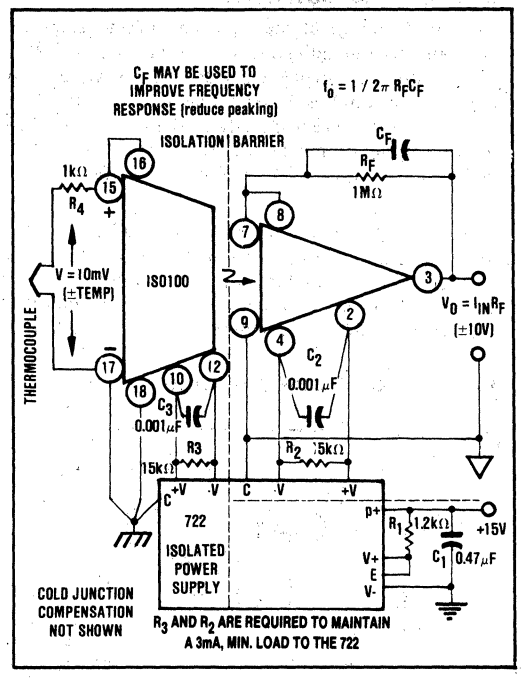


FIGURE 11. Three-Port Isolation Thermocouple Amplifier (Bipolar).

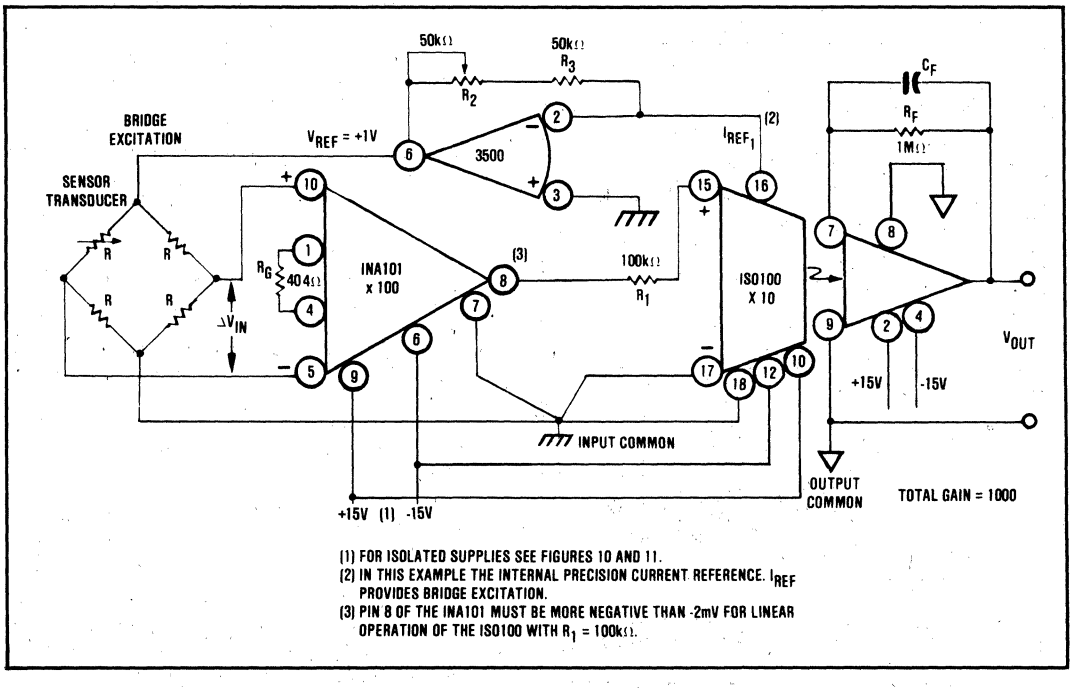


FIGURE 12. Precision Bridge Isolation Amplifier (Unipolar).

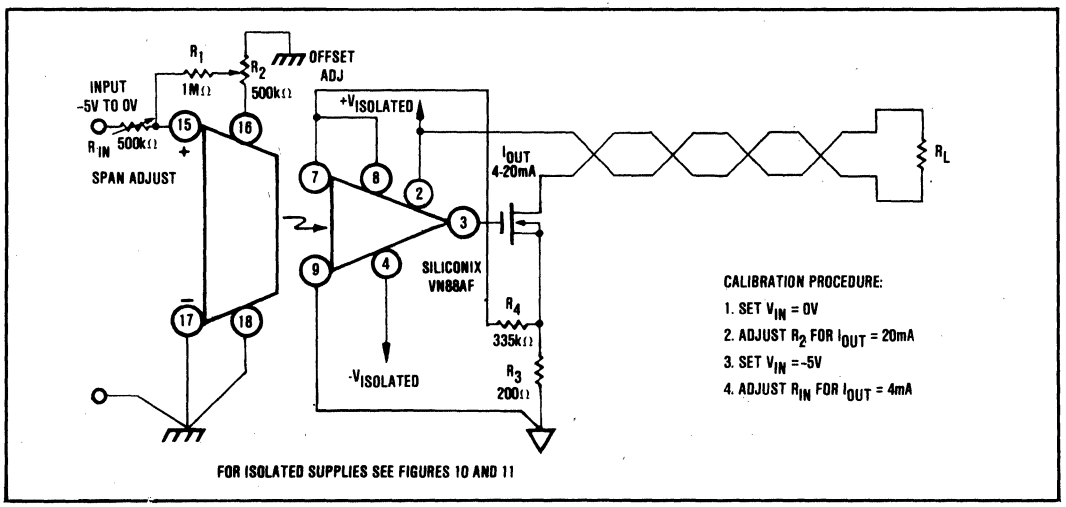


FIGURE 13. Isolated 4mA to 20mA Transmitter (Example of an isolated voltage controlled current source).

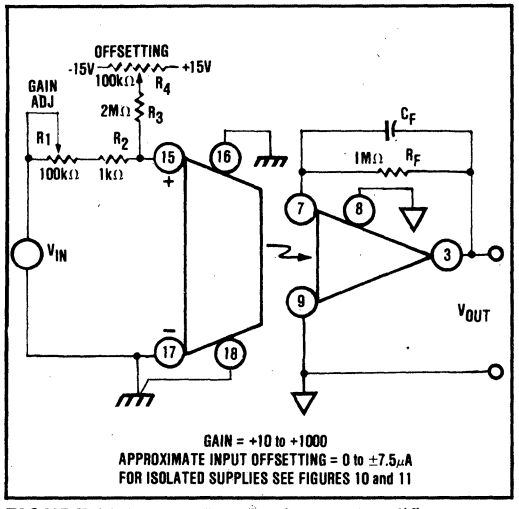


FIGURE 14. Isolated Test Equipment Amplifier (Unipolar with Offsetting).

NOTE: Offset Adjust on pins 5 and 6 are for nulling the 500μV V_{OSO} only. To adjust overall offset, including bias current effects, use nulling (offset) scheme shown in either Figure 13 or Figure 14. Reference current offset will give the best performance.

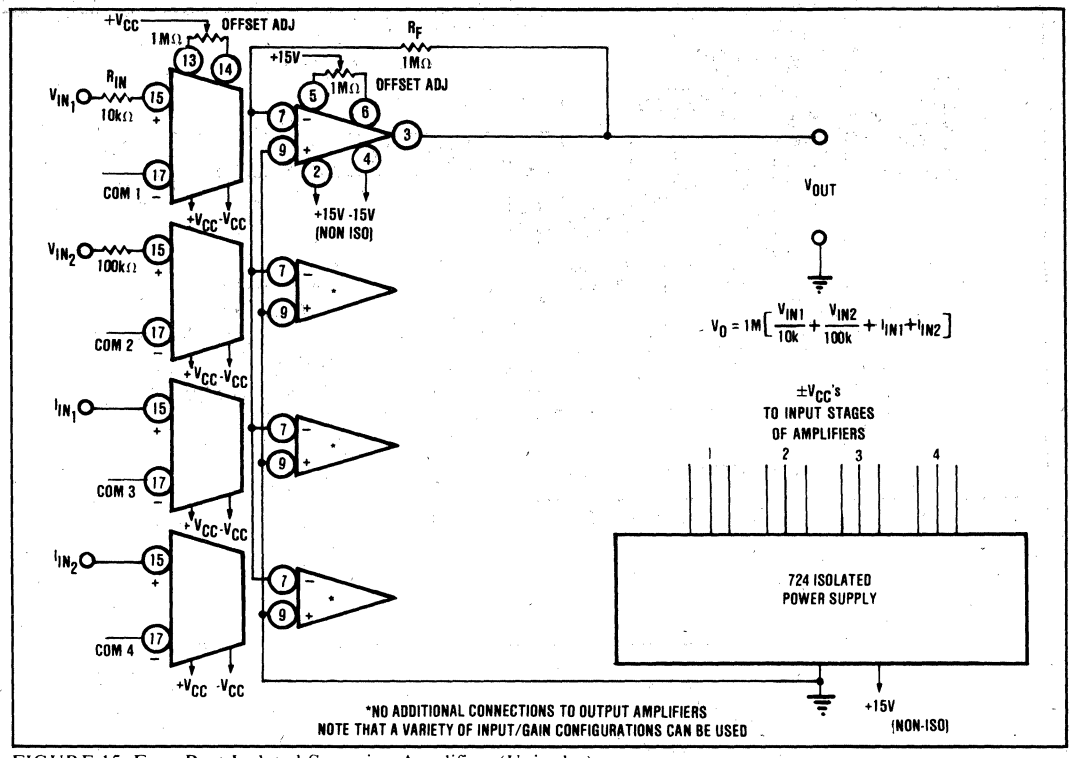


FIGURE 15. Four-Port Isolated Summing Amplifier (Unipolar).

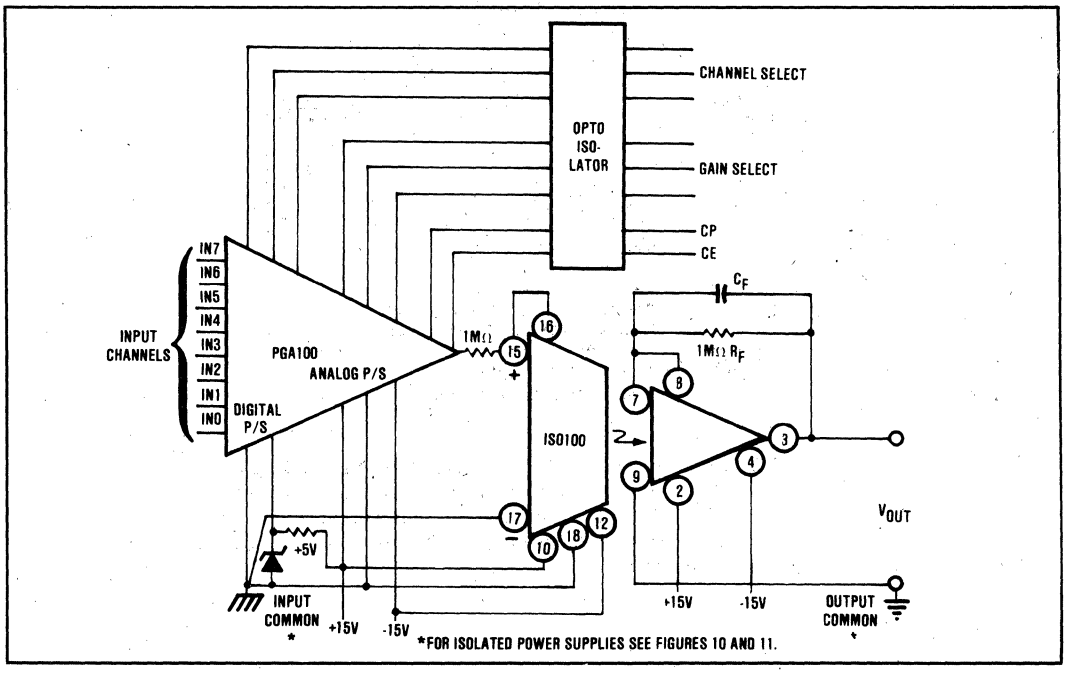


FIGURE 16. Multiple Channel Isolation Amplifier (Bipolar) with Programmable Gain (Useful in Data Acquisition Systems).

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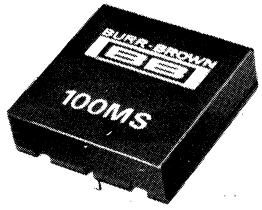

100MS

EMI SHIELD

DESCRIPTION

The 100MS is an epoxy encapsulated electromagnetic electrostatic interference (EMI) shield for use with circuits where sensitivity to EMI is critical. It was designed to attenuate EMI by converting electromagnetic field energy into heat that is absorbed by the shield and by shunting electrostatic fields to common. The 100MS may be used in applications to either confine or exclude EMI. Its cavity was designed for 28.45mm x 28.45mm x 7.24mm, 20-pin hybrid packages. The shields in the cover and base plate are in two separate halves to maintain the electrical isolation between the adjacent rows of pins of the module it encloses. Because of the spacing between the shield halves and the epoxy flow holes, the 100MS provides a partial, but adequate low reluctance path for electromagnetic flux. The 100MS is well suited for use with isolation modules such as the Burr-Brown 3656, 722, and 724.

ASSEMBLY INSTRUCTIONS

Assemble the base plate to the module by pushing the pins of the module through the beveled holes in the base plate until the base plate and bottom of the module are in contact with each other. Place the cover over the module so the tabs are aligned and fit into the slots in the base plate. Bend the four wide shield soldering tabs protruding from the cover to make contact with the bare metal on the base plate. Solder these four tabs to insure the integrity of their connection to the base plate.

The 100MS and the module it contains are mounted and secured to a printed circuit board (PCB) by soldering the two narrow PCB solder tabs to the appropriate common. The PCB solder tab closest to the input side of the module should be soldered to the input common. The other tab should be soldered to the output common. Figure 2 illustrates the assembly of the 100MS.

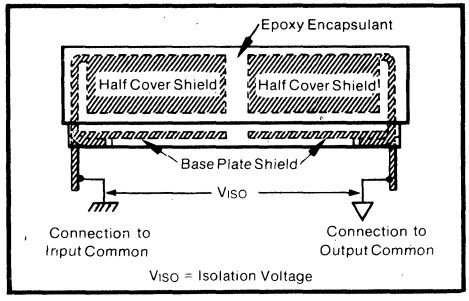

FIGURE 1. Cross-Sectional Side View of 100MS.

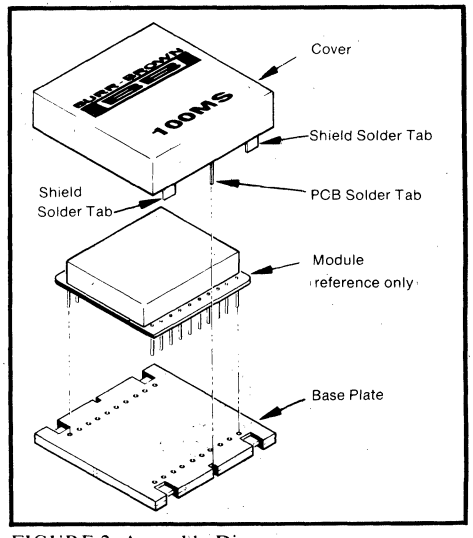

FIGURE 2. Assembly Diagram.

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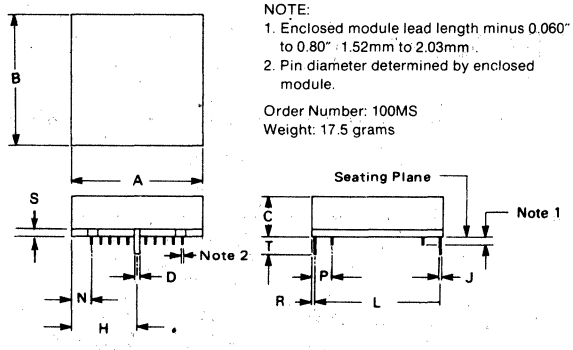
SPECIFICATIONS

ELECTRICAL - Specifications apply between solder tabs.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Isolation Voltage					
Rated Continuous, DC		3500			VDC
Rated Continuous, AC		2000			V. rms
Test	10 seconds	8000			VDC
Capacitance			5		pF
Resistance			10^{10}		Ω
Leakage Current	120V, 60Hz		0.23		μA

NOTE: Temperature changes (ΔT/Δt) greater than 1°C per minute below 0°C and long term storage above 100°C are not recommended.

MECHANICAL



NOTE:
1. Enclosed module lead length minus 0.060" to 0.80" (1.52mm to 2.03mm).
2. Pin diameter determined by enclosed module.

Order Number: 100MS
Weight: 17.5 grams

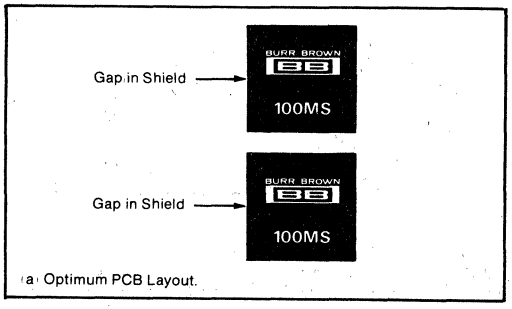
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.320	1.380	33.53	35.05
B	1.320	1.380	33.53	35.05
C	.350	.450	8.89	11.43
D	.040	.060	1.02	1.52
H	.600	.700	15.24	17.78
J	.015	.025	0.38	0.64
L	1.180	1.280	29.97	32.51
N	.150	.250	3.81	6.35
P	.150	.250	3.81	6.35
R	.015	.055	0.38	1.40
T	.130	.230	3.30	5.84
S	.060	.080	1.52	2.03

APPLICATIONS INFORMATION

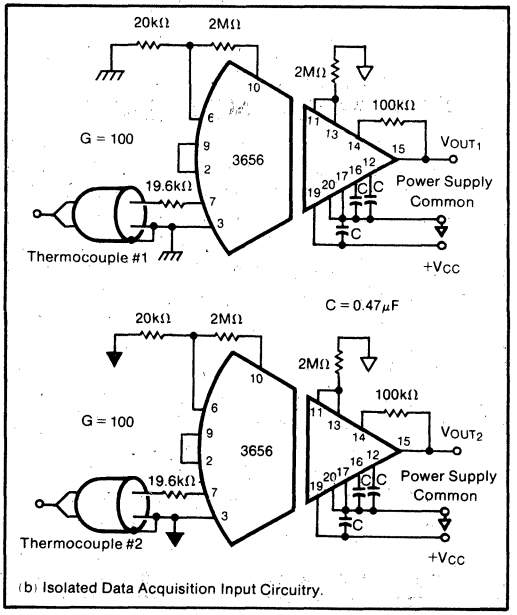
MULTIPLE DEVICE ORIENTATION

A typical application for the 100MS is shown in Figure 3. Using multiple devices within 30mm of each other can cause them to interact by forming beat frequency interference outputs. The 100MS can reduce this interference by as much as a factor of 200:1 depending on the distance between the devices and their relative orientation.

Minimum EMI results when the gaps of both shields are paralleled as in Figure 3a.



(a) Optimum PCB Layout.



(b) Isolated Data Acquisition Input Circuitry.

FIGURE 3. Orientation for Minimum EMI.

BURR-BROWN®

3450
3451
3452
3455

3450

Precision Linear ISOLATION AMPLIFIERS

FEATURES

- 2000V ISOLATION (3452)
- 160dB ISOLATION-MODE REJECTION
- DIFFERENTIAL INPUT
- 0.005% GUARANTEED GAIN LINEARITY (3450)
- 1μV/°C INPUT VOLTAGE DRIFT(3450)
- 20pA INPUT BIAS CURRENT (3452)
- PRECISION WIRE-WOUND RESISTORS FOR LONG TERM STABILITY
- LOW INTERFERENCE PICKUP - PW MODULATION

APPLICATIONS

- GROUND-LOOP ELIMINATION
- OFF-GROUND SIGNAL MEASUREMENTS
- MEDICAL INSTRUMENTATION
- PATIENT MONITORING
- INDUSTRIAL PROCESS CONTROL
- DATA ACQUISITION
- HIGH VOLTAGE MEASUREMENTS
- FAULT PROTECTION

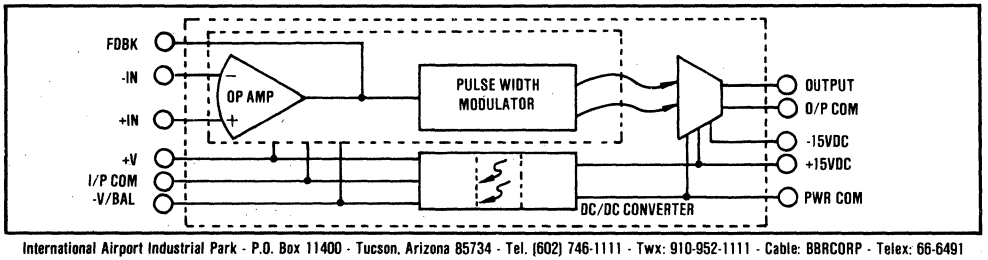
DESCRIPTION

The models 3450, 3451, and 3452 are operational amplifiers with the unique feature of having the output completely isolated from the input. This is accomplished by a high accuracy modulation demodulation stage which isolates the input from the output by $10^{12}\Omega$ in parallel with 12pF of coupling capacitance and provides gain linearity and stability far superior to that offered by ordinary isolation amplifiers.

These devices differ from other isolation amplifiers in several respects. They are true differential input operational amplifiers whereas other commercially available isolation amplifiers are simple unity-gain isolators or are capable of a few fixed gains. Thus they can be connected in all of the common op amp feedback circuits such as summing, inverting, differentiating, etc.

The 3452 differs from the 3450 and 3451 in that it has higher isolation voltage (2000V vs 500V) and has isolated ±15VDC power available at the input.

The 3450 and 3451 differ from each other primarily in their input stage characteristics. The 3450 has a low drift (1μV °C) bipolar transistor input stage while the 3451 has a low bias current (25pA)FET transistor input stage. The 3455 is identical to the 3452 except for additional isolation specifications more well suited for medical applications.



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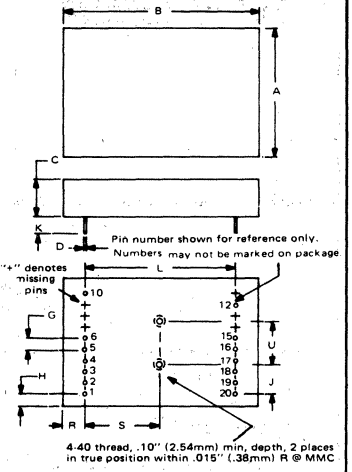
SPECIFICATIONS

ELECTRICAL

Typical at 25°C and ±15VDC unless otherwise noted.

MODEL	3450	3451	3452/3455[1]	UNITS
INPUT[2]				
Open-Loop Gain, min	94	88	94	dB
Input Offset Voltage at 25°C[3], max	±0.55	±20	±0.30	mV
vs Temperature, max	±1.0	±50	±5.0	µV/°C
vs. Supply	±50	±50	±25	µV/V
vs. Time	±10	±100		µV/mo
Input Bias Current at 25°C, max	±50	-0.025	-0.02	nA
vs Temperature, max	±0.5	doubles/10°C		nA/°C
vs. Supply	±0.2	±0.001		nA/V
Input Offset Current at 25°C	±30, max	±0.002		nA
vs Temperature max	±0.3	doubles/10°C		nA/°C
vs. Supply	±0.1	±0.0005		nA/V
Input Impedance				
Differential	10^7	10^{11}		Ω
Common-mode[4]	5×10^9 ‖ 10	10^{11} ‖ 10		Ω ‖ pF
Input Noise				
Voltage, 0.01Hz to 10Hz	0.8	2	4	µV, p-p
10Hz to 1kHz	1.2	3	2	µV, rms
Current, 0.01Hz to 10Hz	30	0.3	0.3	pA, p-p
10Hz to 1kHz	50	0.6	0.6	pA, rms
Input Voltage Range				
Common-mode[4] (operating), min		±10		V
Differential (w/o damage), min		±15		V
Common-mode Rejection[4] at 10V	100	80	90	dB
Isolated Power Available				
Voltage	--	--	±15 +0, -10%	V
Current, max	--	--	±10	mA
Ripple at 100kHz	--	--	100	mV, p-p
ISOLATION				
Gain (without trimming), max[3] 1V/V	±0.1	±0.5		%
vs Temperature, max	±10	±50		ppm/°C
Nonlinearity[5] at ±10V, max/typ	±.005/±0.0015	±0.025/±.005	±0.025/±.005	%
Frequency Response, -3dB (see Fig. 9)	1.5	2.5		kHz
Settling Time				
to 0.01%		5		msec
to 0.1%		1		msec
Isolation Impedance[6]		10^{12} ‖ 16		Ω ‖ pF
Isolation Leakage Current				
at 240V/60Hz, max		2.5[6]		µA
Isolation-mode Rejection[6]				
DC, min		160		dB
60Hz, min		120		dB
Isolation Voltage[6]				
Rated, continuous, min	±500	±2000		V, pk
Test Voltage[7]	±2000	±5000		V, pk[1]
OUTPUT				
Output Voltage, min		±10		V
Output Current, min		±5		mA
Output Impedance, DC		0.2		Ω
Output Noise				
0.01Hz to 10Hz		7		µV, p-p
10Hz to 1kHz		25		µV, rms
Output Offset Voltage at 25°C[3], max	±2	±5	±5	mV
vs Temperature, max		±100		µV/°C
vs. Supply		±500		µV/V
vs. Time		±100		µV/mo
Input Power Requirements				
Voltage		±14 to ±16		VDC
Current, quiescent, max		+30/-5		mA
Current, full load, max	+35/-10		+55/-10	mA[8]
TEMPERATURE RANGE				
Specification		-25 to +85		°C
Storage		-55 to +125		°C
Operating		-25 to +85		°C

MECHANICAL



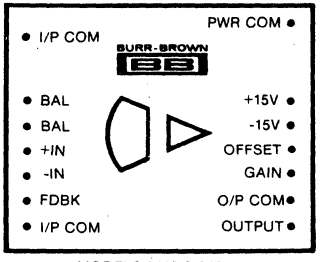
NOTE:
Leads in true position within .015" (.38mm) R @ MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.250	2.310	57.15	58.67
B	3.480	3.510	87.63	89.15
C	.650	.710	16.51	18.03
D	.038	.042	0.97	1.07
G	.200 BASIC		5.08 BASIC	
H	.200	.300	5.08	7.62
J	.525 BASIC		13.34 BASIC	
K	.170	.350	4.32	8.89
L	2.700 BASIC		68.58 BASIC	
R	.350	.450	8.89	11.43
S	1.350 BASIC		34.29 BASIC	
U	.750 BASIC		19.05 BASIC	

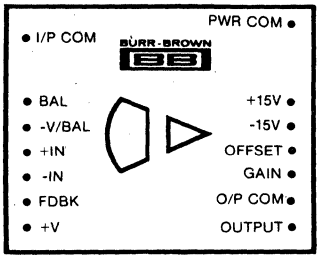
MATERIAL: Black Plastic
WEIGHT: 100g (3.5 oz.)
MATING CONNECTOR: 4400MC

NOTES:
1. The 3455 is identical to the 3452 except for two additional specifications. Each unit is tested to withstand a 2500V, rms, 60Hz sine wave isolation voltage (Ref. Dielectric Withstand Voltage, paragraph 31.11 of UL544). Each unit is specified at a maximum leakage current of 2µA with 240V, rms, 60Hz isolation voltage (Ref. Leakage Current, paragraph 27.5 of UL544).
2. For 3450 and 3451 current drawn from FDBK pin must be ≤ 5mA. For 3452 the sum of the current drawn from FDBK pin and either "-V/Bal" or "+V" pins (i.e., + or - isolated current) must be ≤ 11mA.
3. Errors may be trimmed to zero.
4. Common-mode parameters are measured at the +IN and -IN pins with respect to the I/P COM pin.
5. Nonlinearity is specified to be the peak deviation from a best straightline expressed as a percent of peak-to-peak full scale output.
6. Isolation-mode parameters are measured at the I/P COM pin with respect to the PWR COM pin and O/P COM pin.
7. All units 100% tested for 1µA max leakage current at test voltage.
8. Includes fully loaded input power.

PIN CONNECTIONS
(TOP VIEW)



MODELS 3450 & 3451



MODELS 3452 & 3455

CIRCUIT DESCRIPTION

The 3450, 3451, and 3452 operate on the same principle, basically that of an operational amplifier followed by a high accuracy isolation stage (Figure 1a). The high accuracy of the isolation stage is achieved by use of a proprietary feedback technique in combination with high-stability components.

Isolated DC power for the input amplifier is provided by an internal DC-to-DC converter which derives its power from the external +15VDC supply.

Although a DC-to-DC converter and modulation techniques are used, the output noise is typically less than 1mV (peak) as a result of careful design, internal filtering, and a shielded package. The frequency of this noise is approximately 100kHz which makes it insignificant for many applications. Pulse width modulation minimizes pickup from adjacent units. The symbol shown in Figure 1b is used to represent the complete isolated operational amplifier.

The O/P COM pin must be connected to the PWR COM pin. Figure 10a shows the power supply connections and the optional offset and gain trims.

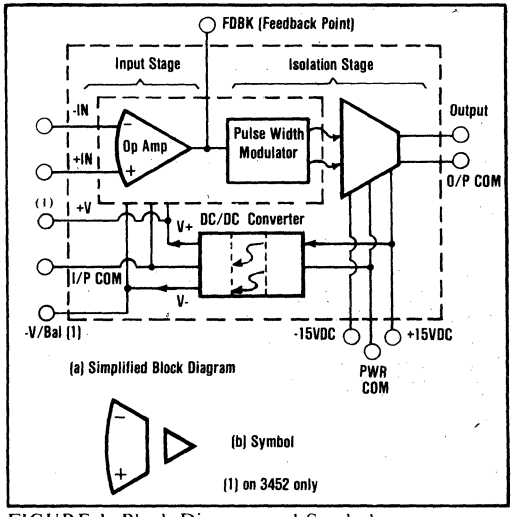


FIGURE 1. Block Diagram and Symbol.

APPLICATIONS

The isolation amplifiers may be used in the same manner as any operational amplifier except that the feedback signal is taken from the FDBK pin rather than from the output pin. No connection is required or would normally be made from input common (I/P COM) to either the power common (PWR COM) or output signal ground pins. Some typical circuit applications are shown in the following paragraphs.

NONINVERTING CIRCUITS

Two useful applications of these amplifiers are impedance buffering and pre-amplification of low-level signals. Such signals may be "riding" on several hundred volts of common-mode potential or they may simply have a significant amount of common-mode noise (power line "pickup", etc.).

Figure 2 illustrates the correct signal and feedback connections for such noninverting circuits.

For signal sources of millivolt levels and low internal impedance, the 3450 will usually be the best choice. Signal sources of this type include thermocouples, thermistors, etc. The 3451 will generally be the best choice for signal sources having large values of internal impedance. The pH cell is an example of this type of signal source.

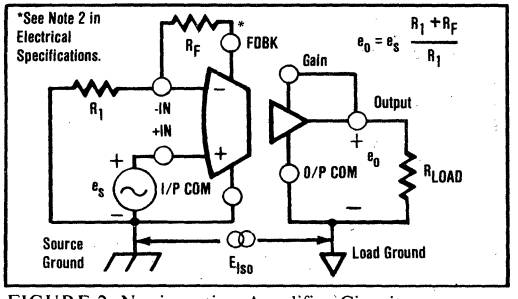


FIGURE 2. Noninverting Amplifier Circuit.

INVERTING CIRCUITS

The isolation amplifiers can be used for a variety of inverting circuit applications. Figure 3 illustrates the proper circuit connections for summing a number of signals which are all at the same common-mode level. An example of the use of such an amplifier is the computation of a weighted average of several temperature inputs.

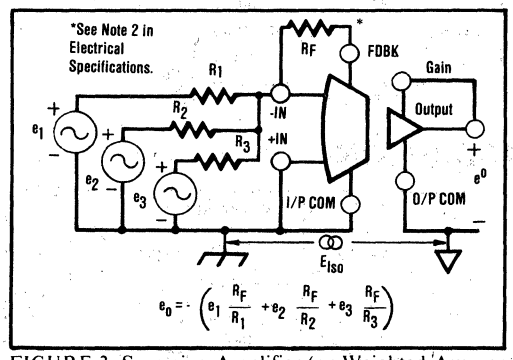


FIGURE 3. Summing Amplifier (or Weighted Averager).

DIFFERENTIAL INPUT CIRCUIT

The isolated operational amplifier can be operated in a fully differential mode as shown in Figure 4. The input impedance of the differential amplifier circuit is $2R_1$ and may cause undersirable loading of the signal source unless R_1 is much greater than the impedance of the signal sources.

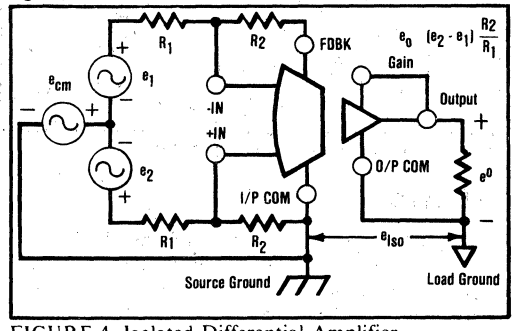


FIGURE 4. Isolated Differential Amplifier.

CURRENT AMPLIFIER

As with nonisolated operational amplifiers, the isolation amplifiers can be used to convert current source or convert current signals to output voltage. However, with these amplifiers the input signal may have a large voltage associated with it which can be completely isolated from output ground. The circuit in Figure 5 illustrates this technique.

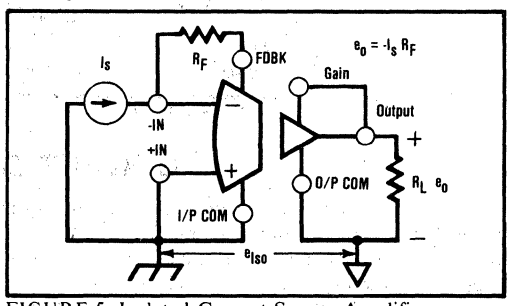


FIGURE 5. Isolated Current Source Amplifier.

BRIDGE AMPLIFIER

The circuit in Figure 6 illustrates a method of amplifying a signal from a balanced bridge which cannot be conveniently used with a nonisolated amplifier. The circuit shown provides a high input impedance so that the bridge is not loaded. The common-mode rejection of the bridge excitation voltage is not degraded by the external gain setting resistors as it would be with a difference amplifier. The gain can be changed conveniently by adjusting a single resistor (R_2). Also, the whole bridge circuit may be floated with respect to the output by a voltage equal to the isolation mode voltage specification without creating troublesome ground-loop current.

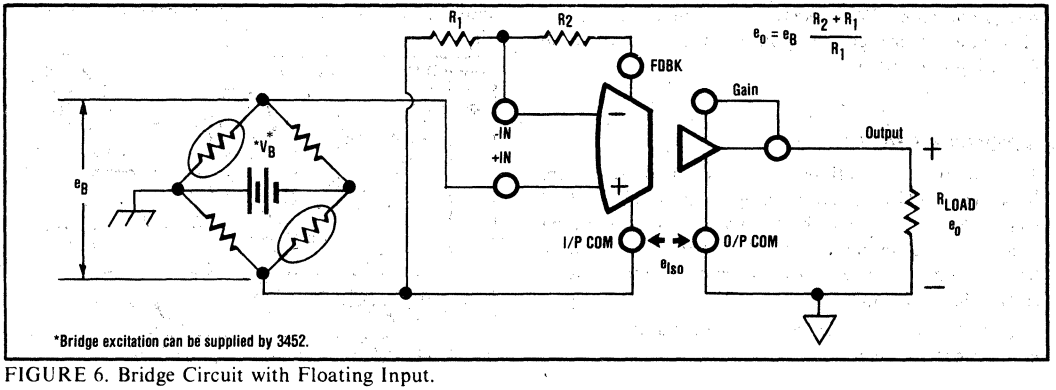


FIGURE 6. Bridge Circuit with Floating Input.

ISOLATION AMPLIFIER USED IN MEDICAL APPLICATIONS

When isolation amplifiers are used in patient monitoring medical application the considerations of 1) patient safety and 2) protection of the amplifier against defibrillator voltages require the use of additional circuitry.

The input resistors must be kept large in order to limit the leakage current in the event of a component failure in the input stage of the amplifier. The 1.2MΩ resistors will limit the current to 12.5μA (Figure 7).

The amplifier must be protected in two areas against possible damage from defibrillator overvoltages. Diodes D_1 through D_4 protect the input stage from excessive voltages and currents. The gas-filled surge voltage protection (SVP in Figure 7) will protect the isolation barrier of the amplifier from breakdown. A Siemens part number B2-B470 will limit the voltage across the isolation barrier to 470V and has high isolation resistance and low leakage capacitance characteristics.

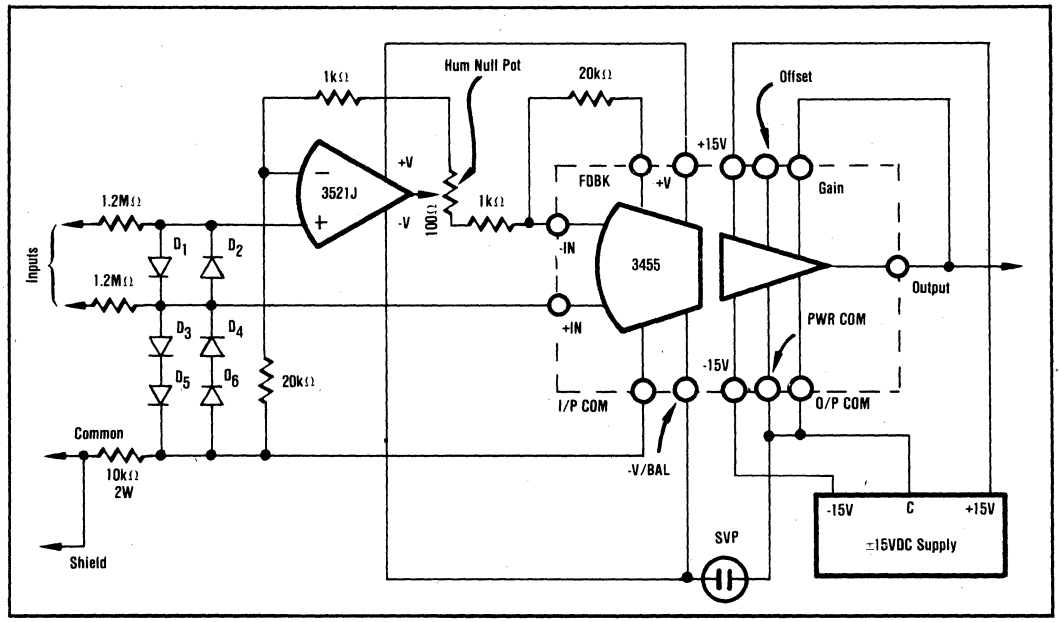


FIGURE 7. High Performance ECG Amplifier Gain = 20V V.

PERFORMANCE

OFFSET VOLTAGE AND NOISE

The total error at the output of the isolation amplifiers may be computed by treating it as two amplifier stages in cascade. One stage (the input stage) has variable gain (G_1) and the other stage (the isolation stage) has a fixed gain of 1V/V.

When this concept is applied to the circuit in Figure 2 as a typical example we see that the total DC offset voltage error at the isolation amplifier output is given by

$$V_{os} = V_{os1} \times G_1 + I_B R_1 \times G_1 + V_{os2}$$

where V_{os} = total offset voltage, referred to output (RTO)

V_{os1} = offset voltage of input stage

V_{os2} = offset voltage of isolation stage

I_B = input bias current

R_1 = input impedance

G_1 = gain of input stage, $R_1 + R_F/R_1$

A similar expression may be used to compute the total offset voltage drift, RTO.

Total output noise may be calculated in much the same way.

$$E_N(\text{rms}) = \sqrt{(E_{N1} \times G_1)^2 + (I_N R_1 \times G_1)^2 + (E_{N2})^2}$$

where E_N (rms) = total noise, RTO

E_{N1} = rms voltage noise of input stage

I_N = rms current noise of input stage

E_{N2} = rms voltage noise of output stage

The rms noise specifications in the Electrical Specifications are for a frequency band of 10Hz to 1kHz. If the bandwidth is reduced by filtering the noise will be decreased.

FREQUENCY RESPONSE

Because the isolation amplifiers are two stage amplifiers, the frequency response of both stages in cascade must be considered in determining the overall response. The curves in Figure 9 show the frequency response of each stage. Note that the frequency response of the input stage is shown under open-loop conditions: As with conventional operational amplifiers, the actual closed-loop response depends on the feedback network used.

GAIN ACCURACY AND STABILITY

The overall gain accuracy of the isolation amplifier is determined by the gain accuracies of its two stages. The input stage accuracy is determined by the open-loop gain and the feedback network (i.e., the loop gain) as with a conventional operational amplifier. The untrimmed accuracy of the isolation stage is given in the electrical specifications. Since these can be trimmed to zero the fundamental limitation on gain accuracy is the linearity and gain drift. When these limitations are considered, the isolation amplifiers are quite capable of achieving gain accuracies of 0.01% and 0.1%. The achievement of such accuracies, as always, requires the use of high quality feedback components (such as wire-wound resistors) and careful calibration techniques.

COMMON-MODE REJECTION AND ISOLATION-MODE REJECTION

The use of the common-mode rejection (CMR) and isolation-mode rejection (IMR) specifications to calculate their respective error contribution is illustrated in Figure 8.

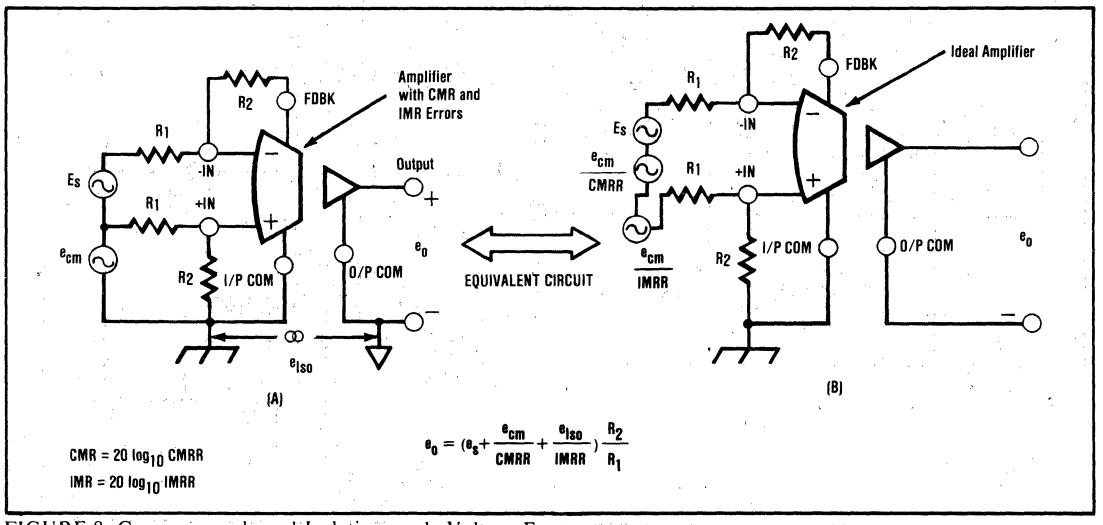


FIGURE 8. Common-mode and Isolation-mode Voltage Errors.

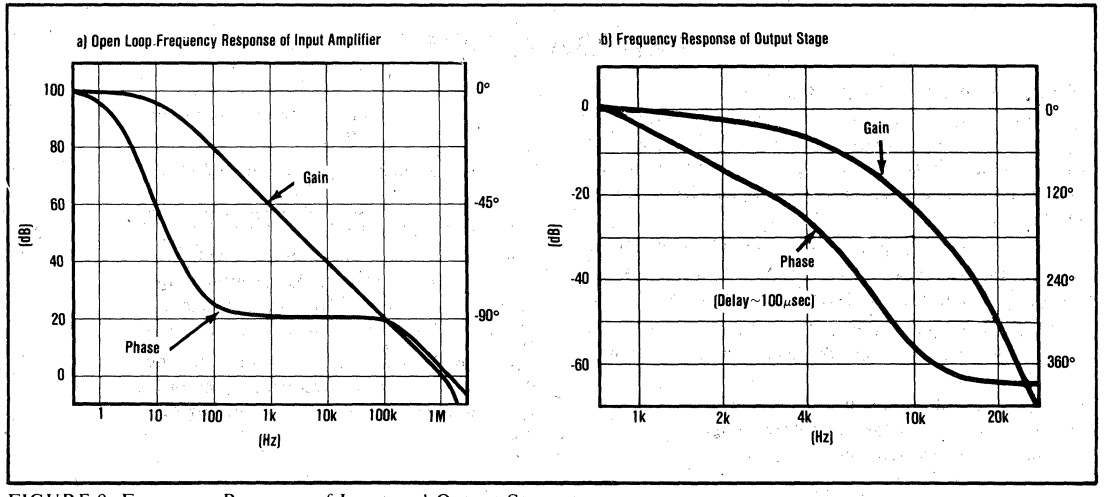


FIGURE 9. Frequency Response of Input and Output Stages.

INSTALLATION AND OPERATING INSTRUCTIONS

MOUNTING

The isolation amplifiers are plastic cased modules suitable for soldering directly on to a printed circuit board. Alternatively they may be plugged into the 4400MC mating connector which may be mounted on a panel or chassis.

Gain of the isolation amplifiers is determined primarily by the operational amplifier input stage. This allows a wide range of possible gains with the accuracy determined primarily by the feedback networks and the open-loop gain of the operational amplifiers. $R_F \geq 10k\Omega$ is recommended for best linearity. The gain of the isolation stage is nominally unity but may be trimmed over a limited range to allow easy calibration.

Offset voltages of both input and output stages are adjustable by use of external components.

Figure 10 illustrates a typical amplifier circuit where gain and offset voltages are adjusted. Proper calibration procedure for this circuit would normally be as follows:

POWER SUPPLY REQUIREMENTS

The isolation amplifiers have no unusual power supply requirements. A standard low-cost power supply such as the Burr-Brown 551 is recommended. The necessary isolated power for the input stage of the amplifier is derived internally by a DC-to-DC converter operating from the externally applied +15VDC power.

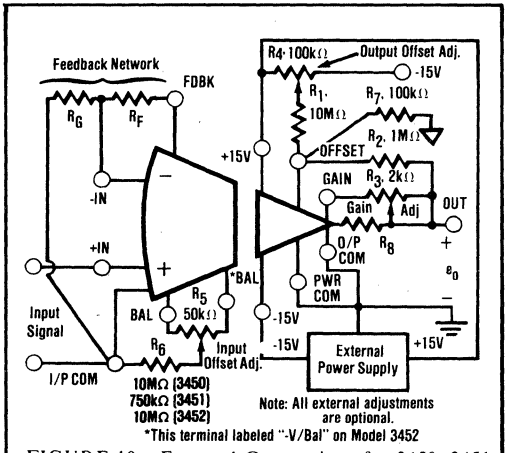


FIGURE 10a. External Connections for 3450, 3451 and 3452.

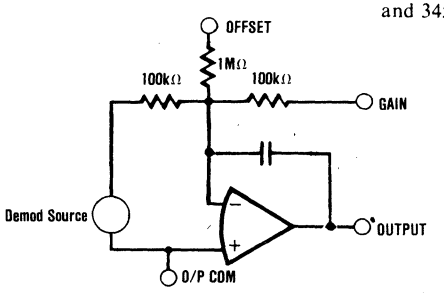


FIGURE 10b. Equivalent Circuit of O/P Stage.

CALIBRATION ADJUSTMENTS

ISOLATION STAGE OFFSET VOLTAGE NULL

Set input signal to zero (connect +IN to I/P COM) connect I/P COM to O/P COM and measure the voltage between the FDBK and OUTPUT pins with a floating DVM. Null this voltage by adjusting R4. Remove the connection between I/P COM and O/P COM.

INPUT STAGE OFFSET VOLTAGE NULL

With the input signal set to zero, adjust R5 such that the voltage between the FDBK and I/P COM pins is zero. (This is best done at a high gain value, i.e., $R_G + R_F / R_G \approx 1000$).

OVERALL GAIN ACCURACY

With R_F and R_G at the proper values to produce the desired gain $G = R_G + R_F / R_G$, apply a known calibration voltage V_R as the input signal. Adjust R_3 for the desired output $V_o = V_R \times G$.

If it is unnecessary to adjust the offset voltage of the output stage, R_1 and R_4 may be omitted. If no adjustment of input stage offset voltage is desired, omit R_5 and R_6. If the specified gain accuracy (see spec table) is adequate without further adjustment, both R_2 and R_3 may be omitted. The OUTPUT pin must then be connected to the GAIN pin for an output stage gain of unity. Omit R_7 if R_1 through R_4 is omitted.

For all applications other than unity-gain noninverting, R_2 is unnecessary and only R_3 is needed to trim the gain. However, it is then necessary to set the first stage gain slightly below the desired overall value and then use R_3 for the gain calibration.

For fixed-gain applications it may be unnecessary to null offset voltage for both input and output stages. The offset voltage of the output stage, for instance, may be used to compensate for the input stage offset, thus giving an overall null. However, if gain is to be varied over a wide range it will usually be necessary to null both offset voltages.

Appropriate safety precautions should be taken when adjusting input stage offset voltage or gain. These points will be "floating" at the isolation-mode voltage and appropriate precautions must be taken if this is a high voltage. In particular, any adjustment potentiometers used for input stage adjustment should have insulated shafts with voltage ratings in excess of any expected common-mode potential.

The output stage can be adapted to drive capacitive load of up to 10,000pF without sacrificing DC gain accuracy. Add $R_8 = 100\Omega$ as shown in Figure 10b, otherwise, $R_8 = 0\Omega$.

WIRING SHIELDING AND ISOLATION-MODE REJECTION

The capacitive coupling from input common (I/P COM) to output common (O/P COM) for the isolation amplifiers is extremely low. This is an essential element in achieving the isolation-mode rejection specifications. Therefore, it is essential that care be used in wiring and printed circuit card layout to minimize stray capacitance between input and output circuits.

Proper shielding of input leads is also essential in preserving isolation-mode rejection. When shielded cable is used the shield should be connected to the common-mode potential at the signal source.

Isolation-mode rejection at high frequencies will be degraded by resistance in series between the signal source and the I/P COM pin (e.g., wire resistance). Figure 11 illustrates the mechanism by which such degradation occurs. The isolation-mode voltage "divides" across R_W and C_C creating an isolation-mode error voltage Δe_{ISO} which appears as an unwanted differential input voltage adding to e_S. Note that this error occurs even if R_N and R_W are equal because the stray capacitance C_C exists only from the I/P COM pin to O/P COM. If this degradation of the isolation-mode rejection becomes significant (for R_W = 1kΩ and f = 60Hz, the CMR is still in excess of 97dB) a capacitance from the +IN pin to O/P COM will compensate the effect. A capacitor used in this manner must withstand whatever isolation-mode potential exists.

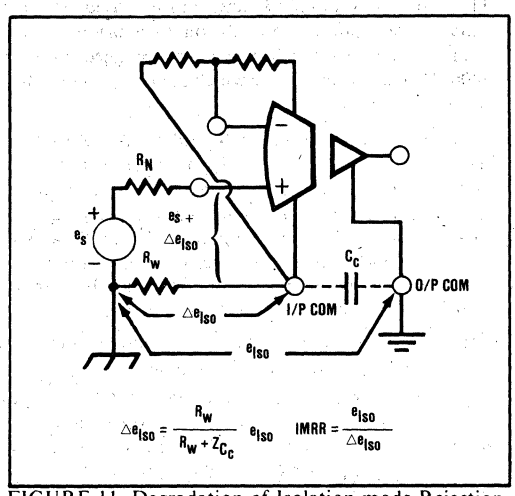


FIGURE 11. Degradation of Isolation-mode Rejection Due to Wiring Impedance and Coupling Capacitance.

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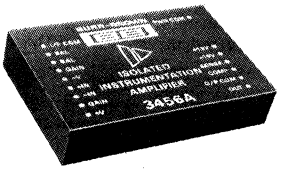
3456



ISOLATED INSTRUMENTATION AMPLIFIER

FEATURES

- TRUE 3-WIRE INSTRUMENTATION AMPLIFIER INPUT
- TRUE INSTRUMENTATION GRADE ISOLATION AMPLIFIER
- 1μV/°C INPUT VOLTAGE DRIFT
- ADJUSTABLE GAIN, 1 to 1000
- LOW NONLINEARITY, 0.02% max
- ISOLATION VOLTAGE, 2000V PEAK RATED CONTINUOUS
- 160dB ISOLATION-MODE REJECTION
- ±20mA, VOLTAGE OR CURRENT PROGRAMMABLE OUTPUT
- 2.5kHz FREQUENCY RESPONSE
- LOW INTERFERENCE PICKUP-PW. MODULATION
- FULLY SELF-CONTAINED

APPLICATIONS

- ISOLATED THERMOCOUPLE AND RTD SENSING
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT AND INSTRUMENTS
- HIGH VOLTAGE INSTRUMENTATION AMPLIFIER
- CURRENT SHUNT MEASUREMENTS
- GROUND-LOOP ELIMINATION
- BIOMEDICAL PATIENT MONITORING

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DESCRIPTION

The Models 3456A and 3456B are high performance instrumentation amplifiers which have their outputs completely isolated from the input. The front end of the unit is a high performance, DC differential-input instrumentation amplifier stage, designed for data acquisition and instrumentation use. The low drift, low noise and high CMR make it possible to accurately amplify microvolt-level signals with gains of up to 1000. The input stage is followed by a high accuracy unity gain, pulse width modulation/demodulation isolation stage. This isolation stage isolates its input from the output by $10^{12}\Omega$|| 14 pF impedance. The 3456A and 3456B differ from other isolation amplifiers in several respects. They are true instrumentation amplifiers as opposed to differential input op amps or fixed gain isolators. They offer both, the single resistor programmable gain range as well as the true 3 wire instrumentation amplifier input.

THEORY OF OPERATION

Figure 1 shows block diagram of 3456. The true 3 wire instrumentation amplifier input section shown needs only one resistor to set the required gain level. It has high input impedance, high CMR and low bias current and allows the use of inverting, non-inverting and differential input configurations. The input offset adjustment shown is optional.

Isolated DC power for the input stage is provided by an internal DC/DC converter which derives its power from the external +15 VDC supply. The isolated power is also made available (on +V and -V pins) for external use.

The modulation/demodulation stage isolates the input from the output by $10^{12}\Omega$ in parallel with 14 pF of coupling capacitance. Pulse width modulation technique is used to minimize pickup from adjacent units. This technique combined with the use of wirewound and laser trimmed thin-film resistors provides high overall accuracy and excellent drift characteristics.

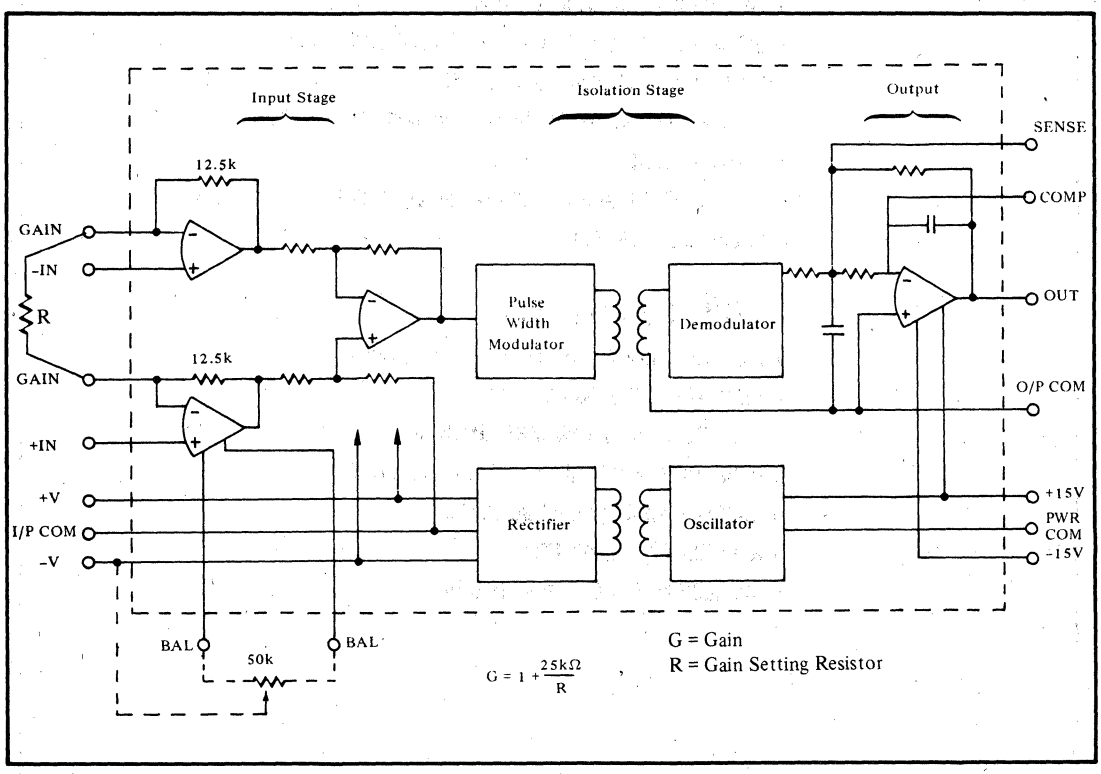


FIGURE 1. 3456 BLOCK DIAGRAM

SPECIFICATIONS

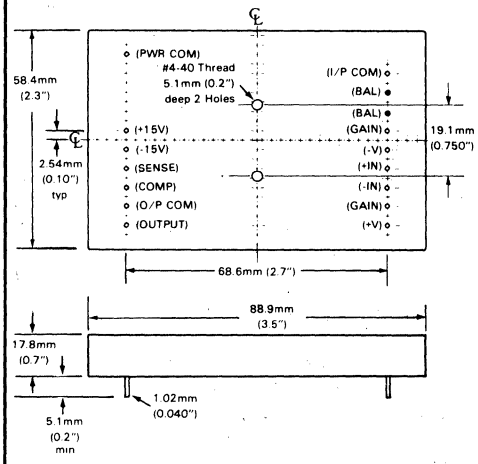
Typical at 25°C and ±15VDC supply voltage unless otherwise noted.

ELECTRICAL

MODEL	3456A	3456B
GAIN		
Gain Equation	$G = 1 + \frac{25k\Omega}{R}$	
Range of Gain	1 - 1000	
Gain Nonlinearity at G ≤ 100	±0.01% typ., ±0.02% max	
≤ 1000	±0.03% typ., ±0.08% max	
Gain Accuracy at G ≤ 100	±0.2% max	
G ≤ 1000	±0.5% typ.	
Gain vs Temperature at G ≤ 100	10 ppm/°C	
at G = 1000	50 ppm/°C	
INPUT		
Input Impedance - Differential	$10^7\Omega$ || 3 pF	
Common-mode	$5 \times 10^9\Omega$ || 3 pF	
Input Voltage Range[1]	±10V	
Absolute max	±Isolated Supply	
Common-mode Rejection, DC-100Hz		
at G = 1, 5kΩ source unbal.	80dB, min	
at G = 100, 0Ω balanced source	110dB	
Input Bias Current, Initial	±50nA, max	
vs Temperature	0.3nA/°C typ, 0.6nA/°C, max	
vs Supply	±0.2nA/V	
Input Noise		
Voltage, 0.01Hz - 10 Hz	1.5μ p-p	
10Hz - 1.0kHz	1.4μV rms	
Current, 0.01Hz - 10Hz	200pA p-p	
10Hz - 1.0kHz	50pA rms	
ISOLATED POWER		
Voltage - No load	±15.3V, max	
Voltage - ±10mA	±13.5V, min	
Current	±10mA, max	
Ripple at 100kHz	100mV, p-p	
TOTAL OFFSET VOLTAGE		
Initial[2]	±(0.5 + 5/G)mV max	±(0.25 + 2/G)mV max
vs Temperature	±(2 + 150/G)μV/°C max	±(1 + 75/G)μV/°C max
vs Supply	±(30 + 500/G)μV/V	
vs Time	±(3 + 100/G)μV/mo	
ISOLATION		
Isolation Impedance[3]	$10^{12}\Omega$ || 14 pF	
Isolation Mode Rejection, DC	160dB + I/P Gain (dB)	
,60Hz	130dB + I/P Gain (dB), min	
Isolation Voltage, Rated Continuous	±2000V Peak	
Test Voltage[4]	±5000V Peak	
FREQUENCY RESPONSE		
-3dB Response at G ≤ 400	2.5kHz	
-3dB Response for 400 ≤ G ≤ 1000	2.5kHz to 1kHz	
Setting Time to 0.01%	5msec	
to 0.1%	1msec	
OUTPUT		
Output Voltage	±10V at ±20mA, min	
Output Impedance, DC	0.04Ω	
Short Circuit Current, Duration	40mA, unlimited	
Output Noise, 0.01Hz - 10Hz	15μV p-p	
1Hz - 1kHz	25μV rms	
POWER SUPPLY		
Voltage	±14 to ±16VDC	
Current, Quiescent	+40/-8mA, max	
Full Load[5]	+85/-30mA, max	
TEMPERATURE RANGE		
Specification	-25°C to +85°C	
Operating	-25°C to +85°C	
Storage	-55°C to +125°C	

MECHANICAL

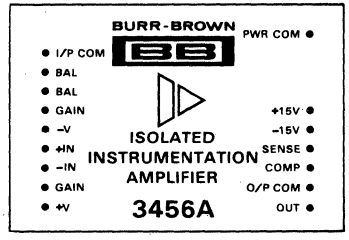
(BOTTOM VIEW)



MATERIAL: Black Plastic
WEIGHT: 100 grams (3.5 oz.)
PINS: Pin material and plating composition meet method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 4400MC.

PIN CONNECTIONS

(TOP VIEW)



NOTES:
1. The ±10V input range is subject to the limitation that $|V_{common\ mode}| + |\text{Gain} \times V_{diff}/2| \leq 10V$.
2. Both the components (input and output) of the offset voltage may be trimmed to zero.
3. Isolation mode parameters are measured at the I/P COM pin with respect to the PWR COM pin.
4. All units are 100% tested for 25μA maximum leakage at test voltage.
5. Includes full isolated power supply.

VOLTAGE OUTPUT CONFIGURATION

The 3456, when connected as shown in Figure 2, will provide output signal capable of driving up to ±20mA load. Refer to the block diagram shown in Figure 2. Notice that the demodulated signal is referenced to the O/P COM pin. The O/P COM pin is connected to the output ground (PWR COM) for voltage output configuration as is shown in Figure 2. So with this configuration, the demodulated voltage signal is fully applied across the load impedance Z_L.

If roll-off at a lower frequency (lower than 2.5kHz) is desired, an optional compensation capacitor C_C may be connected as shown between the COMP pin and the OUT pin. See Figure 4 for the selection of C_C. The output offset controls shown in Figure 2 and Figure 3 are optional. They provide approximately ±15mV offset control at the output.

The SENSE and COMP pins are subject to electrostatic noise pick-up via stray capacitance. To minimize this noise pick-up these pins and connected circuits should be shielded. If these controls are not used, we recommend the unused pins be cut off flush to the 3456 surface. This would help minimize the degradation of Isolation Mode Rejection.

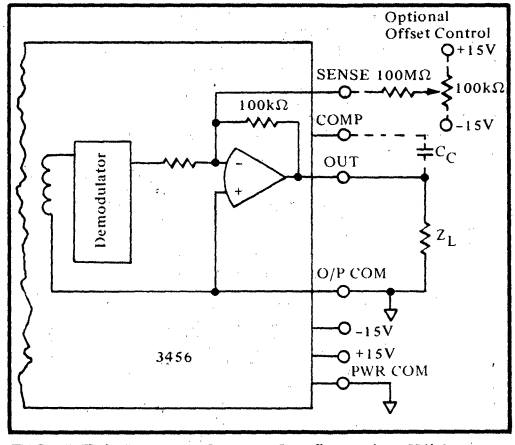


FIGURE 2. Voltage Output Configuration With Simplified Block Diagram.

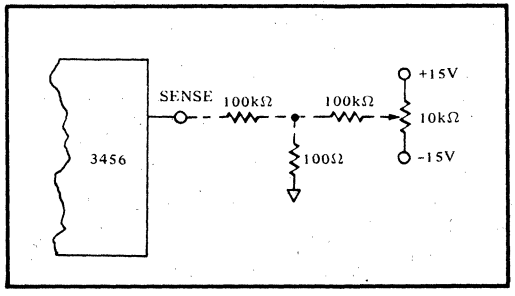


FIGURE 3. Alternate O/P Offset Control For Voltage Output Configuration.

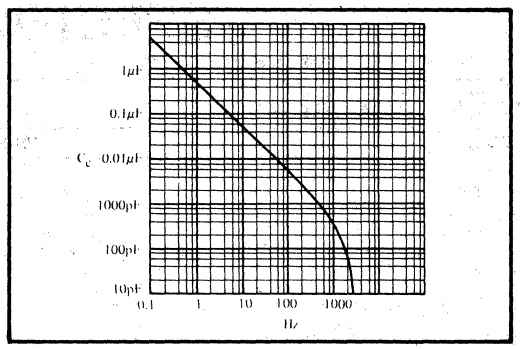


FIGURE 4. -3dB Frequency Vs C_C (Voltage Output).

ALTERNATE GAIN ADJUSTMENT

The gain adjustments are normally made by varying the gain setting resistor at the input. Since voltages at high potential may be present at the input side of the isolation barrier, some applications may require that gain adjustments or gain trimming be done at the output side of the isolation amplifier. For the voltage output configuration, such gain trimming can be done at the output. Figure 5 shows a recommended gain adjustment method. This method would provide a ±1% gain trim at the output.

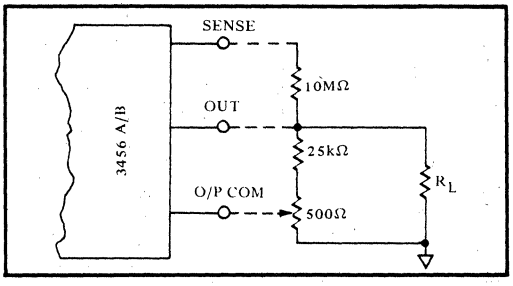


FIGURE 5. Alternate Gain Adjustment Method For Voltage Output Configuration.

CURRENT OUTPUT CONFIGURATION

Current output configuration is a configuration which gives an output current proportional to the input signal. The 3456 should be connected as shown in Figure 6 for current output configuration. In this configuration, the O/P COM pin is not connected to the output ground (PWR COM). The O/P COM pin is connected to R_L. The demodulated signal (voltage between the OUT pin and O/P COM pin) is thus applied across R_S. With a given demodulated signal and known feedback for the output amplifier, the voltage across R_S can be calculated. With known value of this voltage, the value of R_S can be fixed to give the desired output current to the load resistor R_L. The output current is thus programmed by R_S. It does not change with changes in the load resistor R_L. The feedback resistor R_F paralleled with the internal 100kΩ resistor (see Figure 6) helps achieve the required voltage rescaling at the output (the OUT pin).

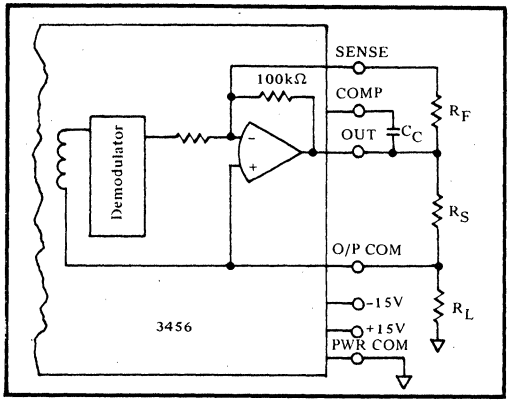


FIGURE 6. Current Output Configuration With Simplified Block Diagram

PROGRAMMING FOR CURRENT OUTPUT

The selection criteria discussed below is based on 3456 being gain programmed for ±10V full scale signal at the OUT pin (the signal as referenced to the PWR COM pin). With ±10V full scale signal, best overall accuracy is achieved.

R_L is defined as the maximum load impedance in ohms and I_o as the maximum peak output current in amperes. The common-mode voltage (an error producing term) is directly proportional to R_L. So, it is desirable to keep R_L to as minimum a value as is consistent with desired application's requirements.

Determine first the value of I_o and R_L suitable for the desired application. The values of R_S and R_F in ohms can be obtained by the expressions,

$$R_S = \frac{10 - I_o R_L}{I_o}$$

and

$$R_F = \frac{10^5 (I_o R_S 10^4 - R_S)}{10^5 - I_o R_S . 10^4 + R_S}$$

C_C, expressed in pF, can be calculated by the expression

$$C_C = \frac{220 . 10^5}{R_F}$$

where R_F is in ohms.

The above calculated value of C_C would maintain the -3dB frequency response at 2.5kHz. Roll-off at a frequency lower than 2.5kHz can be achieved by increasing the value of C_C.

The maximum allowable voltage across $R_S + R_L$ to maintain the specified accuracy, also known as "compliance" is limited to ±10V by the output swing capability of the output amplifier.

The current output configuration contains all error elements of the voltage output configuration plus additional common-mode errors introduced by raising the demodulated signal reference from output ground to the voltage developed across R_L. Hence, as discussed earlier, consistent with the requirements of desired application, it is best to keep the R_L to as minimum a value as is possible. Figure 7 shows the maximum additional peak nonlinearity errors in the current output configuration expressed as a percent of full scale peak to peak output (40mA) vs R_L/R_S.

The values of R_S and R_F as calculated above, would program the unit for the desired full scale output current I_o when the gain of 3456 is scaled for ±10V full scale ouptut. With these values of R_S and R_F the unit would comply with the performance curves shown in Figures 7, 8 and 9. Deviation from this selection procedure could result in degraded performance.

Due to the output amplifier bias currents and the demodulator currents, we recommend that the full scale output current value be ±1mA or higher (up to ±20mA).

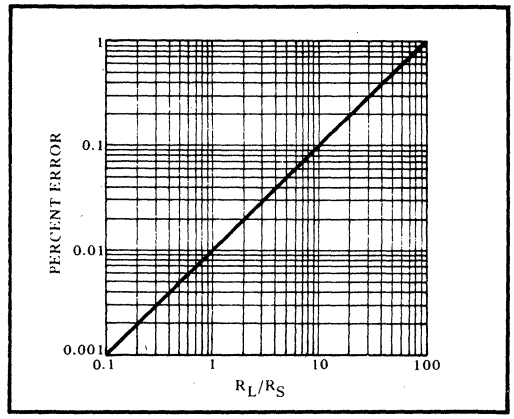


FIGURE 7. Maximum Additional Peak Nonlinearity Errors in Current Output Configuration Expressed as Percent of p-p Output Current Vs R_L/R_S.

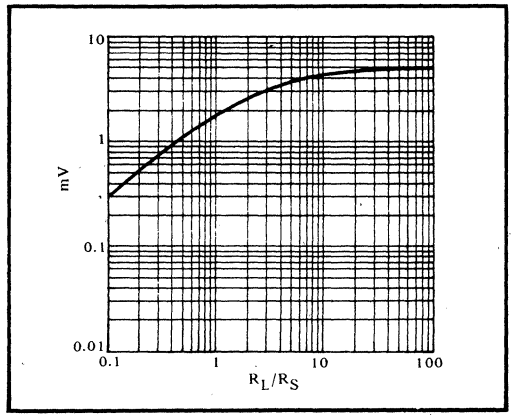


FIGURE 8. Typical Additional Offset in Current Output Configuration Vs R_L/R_S.

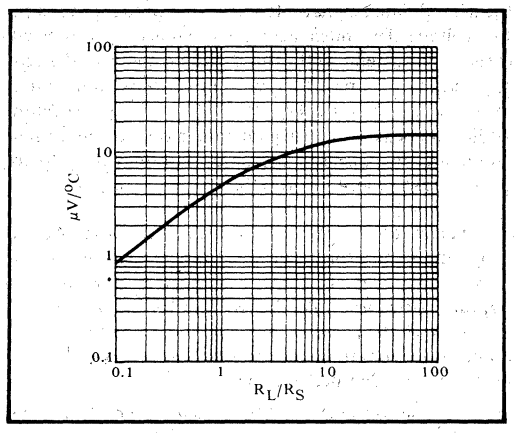


FIGURE 9. Typical Additional Temperature Drift in Current Output Configuration Vs R_L/R_S.

SPECIFICATIONS FOR CURRENT OUTPUT

When the above discussed current output configuration procedure is followed for selection of R_F, R_S, C_C and R_L, the following performance standards would be met by the configuration.

Gain accuracy would be maintained within a maximum of 0.1% above that specified for voltage output configuration. Gain nonlinearity would not exceed the voltage output specification by more than the value indicated in Figure 7.

Current output offset and temperature drift are specified as a voltage quantity appearing across R_S. These parameters each contain two terms. The first term is the total offset voltage RTI (referred to input) specification for voltage output mode multiplied by the input gain setting, multiplied by $\frac{R_S}{R_S + R_L}$. The second term is the value found from Figure 8 for the offset voltage and from Figure 9 for the offset voltage drift. Adding these two terms would give the offset voltage and the offset voltage drift values appearing across the scaling resistor R_S. To obtain these parameters in terms of the offset current and the offset current drift, they have to be divided by R_S. In short,

$$\left(\begin{array}{c}\text{Voltage Output Mode}\\ \text{Specification}\end{array}\right)\left(\begin{array}{c}\text{Input}\\ \text{Gain}\end{array}\right)\left(\frac{R_S}{R_S + R_L}\right)+\left(\begin{array}{c}\text{Value from}\\ \text{Fig. 8 or Fig. 9}\end{array}\right)$$
$$=\left(\begin{array}{c}\text{Current Output Mode}\\ \text{Specification}\end{array}\right)$$

To obtain the offset or drift in units of current, divide the above equation by R_S.

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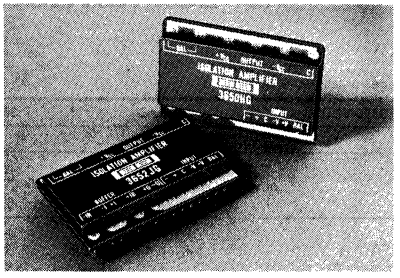


3650
3652

Optically-Coupled Linear ISOLATION AMPLIFIERS

FEATURES

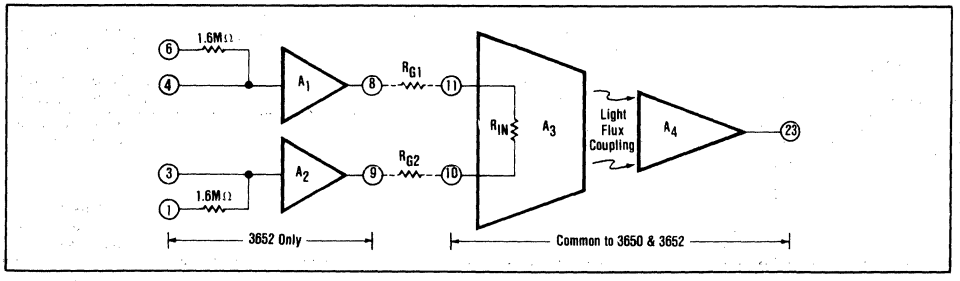
- BALANCED INPUT
- LARGE COMMON-MODE VOLTAGES
  ±2000V Continuous
  140dB Rejection
- ULTRA LOW LEAKAGE
  0.35μA max at 240V/60Hz
  1.8pF Leakage Capacitance
- EXCELLENT GAIN ACCURACY
  0.05% Linearity
  0.05%/1000Hours Stability
- WIDE BANDWIDTH
  15kHz ±3dB
  1.2V/μsec Slew Rate

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- DATA ACQUISITION
- INTERFACE ELEMENT
- BIOMEDICAL MEASUREMENTS
- PATIENT MONITORING
- TEST EQUIPMENT
- CURRENT SHUNT MEASUREMENT
- GROUND-LOOP ELIMINATION
- SCR CONTROLS

DESCRIPTION

The 3650 and 3652 are optically coupled integrated circuit isolation amplifiers. Prior to their introduction commercially available isolation amplifiers had been modular or rack mounted devices using transformer coupled modulation demodulation techniques. Compared to these earlier isolation amplifiers the 3650 and 3652 have the advantage of smaller size, lower cost, wider bandwidth and integrated circuit reliability. Also, because they use a DC analog modulation technique as opposed to a carrier type technique, they avoid the problems of electromagnetic interference (both transmitted and received) that most of the modular isolation amplifiers exhibit.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and ±15VDC supply voltages unless otherwise noted.

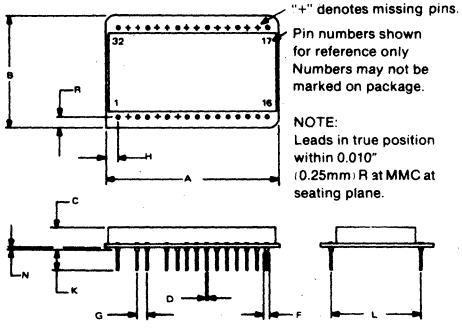
MODEL	3650MG/HG[1]	3650JG	3650KG	3652MG/HG[1]	3652JG
ISOLATION					
Isolation Voltage					
Rated Continuous, (min)			2000Vp or VDC		
Test Voltage, (min) 10sec duration			5000Vp		
Isolation-Mode Rejection, G = 10					
DC			140dB		
60Hz, 5000Ω source unbalance			120dB		
Leakage Current, 240V/60Hz			0.35μA, max		
Isolation Impedance					
Capacitance			1.8pF		
Resistance			$10^{12}\Omega$		
GAIN					
Gain Equation					
for current sources			$G_I = 10^6$ Volt/Amp	$G_I = 1.0057 \times 10^6$ Volt/Amp[2]	
for voltage sources			$G_V = \frac{10^6}{R_{G1} + R_{G2} + R_{IN}}$ V/V	$\frac{10^6}{R_{G1} + R_{G2} + R_{IN} + R_O}$ V/V	
Input Resistance, R_{IN}, max		25Ω		25Ω	
Buffer Output Impedance, R_O		Not applicable		90Ω ±30Ω	
Gain Equation Error, max[3]	1.5%	0.5%	0.5%	1.5%[4]	0.5%[4]
Gain Nonlinearity	±0.05% typ. ±0.2% max	±0.03% typ. ±0.1% max	±0.02% typ. ±0.05% max	±0.05% typ. ±0.2% max	±0.05% typ. ±0.1% max
Gain vs Temperature	300ppm/°C	100ppm/°C	50ppm/°C	300ppm/°C[4]	200ppm/°C[4]
Gain vs Time		±0.05%/1000hrs.		±0.05%/1000hrs.	
Frequency Response					
Slew Rate			0.7V/μsec min, 1.2V/μsec typ.		
±3dB Frequency			15kHz		
Settling Time					
to ±0.01%			400μsec		
to ±0.1%			200μsec		
INPUT STAGE[5]					
Input Offset Voltage					
at 25°C, max[3]	±5mV	±1mV	±0.5mV	±5mV	±2mV
vs Temperature, max	±25μV/°C	±10μV/°C	±5μV/°C	±50μV/°C	±25μV/°C
vs Supply		100μV/V		100μV/V	
vs Time		50μV/1000 hrs.		100μV/1000 hrs.	
Input Bias Current					
at 25°C		10nA typ, 40nA max		10pA typ, 50pA max	
vs Temperature		0.3nA/°C		doubles every +10°C	
vs Supply		0.2nA/V		1pA/V	
Input Offset Current					
vs Temperature		effects included		10pA	
vs Supply		in output offset		doubles every 10°C	
				1pA/V	
Input Impedance					
Differential		"R_{IN}" = 25Ω max		$10^{11}\Omega$	
Common-mode		$10^9\Omega$		$10^{11}\Omega$	
Input Noise					
Voltage, 0.05Hz to 100Hz		8μV, p-p		4μ, p-p	
10Hz to 10kHz		4μV, rms		5μV, rms	
Input Voltage Range					
Common-mode, linear operation,		±(|V| -5)V		±(|V| -5)	
w/o damage, at +,-		±V		±V	
at +I, -I		Not applicable[6]		±300V for 10msec[7]	
at +IR, -IR		Not applicable[6]		±3000V for 10msec[7]	
Differential, w/o damage, at +, -		±V		±V	
Differential, w/o damage, at +I, -I		Not applicable		±600V for 10msec[7]	
Differential, w/o damage, at +IR, -IR		Not applicable		±6000V for 10msec[7]	
Common-mode Rejection, 60Hz		90dB at 60Hz, 5kΩ imbalance		80dB at 60Hz, 5kΩ imbalance	
Power Supply (Input Stage Only)					
Voltage (at "+V" and "-V"		±8V to±18V		±8V to ±18V	
Current					
Quiescent		±1.2mA[8]		±3mA[8]	
with ±10V output[7]		+6.5mA or -6.5mA, typ		+8.5mA or -8.5mA, typ	
		+12mA or -12mA, max		+16mA, max	

ELECTRICAL (cont)

MODEL	3650MG/HG[1]	3650JG	3650KG	3652MG/HG[1]	3652JG
OUTPUT STAGE					
Output Voltage, min	±10V			±10V	
Output Current, min	±5mA			±5mA	
Output Offset Voltage					
at 25°C max[3]	±25mV	±10mV	±10mV	±25mV	±10mV
vs Temperature, max	±900μV/°C	±450μV/°C	±300μV/°C	±900μV/°C	±450μV/°C
vs Supply		±500μV/V		±500μV/V	
vs Time		±1mV/1000hrs		±1mV/1000hrs	
Output Noise Voltage					
0.05Hz to 100Hz		50μV, p-p		50μV, p-p	
10Hz to 1kHz		65μV, rms		65μV, rms	
Power Supply (Output Stage Only)					
Voltage ("+V_{CC}" and "-V_{CC}")			±8V to ±18V		
Current					
Quiescent			±2.3mA typ, ±6mA max		
with ±5mA output, max			±11mA		
TEMPERATURE[8]					
Specification			0°C to 85°C		
Operating			-40°C to +100°C		
Storage			-55°C to +125°C		

1. All electrical and mechanical specifications of the 3650MG and 3652MG are identical to the 3650HG and 3652HG, respectively, except that the following specifications apply to the 3650MG and 3652MG: (a) Isolation test voltage duration incrased from 10sec minimum to 60sec minimum; (b) Input offset voltage at 25°C max: ±10mV; vs temp. max: ±100μV/°C; (c) Output offset voltage at 25°C max: ±50mV; vs temp. max: ±1.8mV/°C.
2. If used as 3650, see Installation and Operating Instructions.
3. Trimmable to zero.
4. Gain error terms specified for inputs applied through buffer amplifiers (i.e., ±1 or ±IR pins).
5. Input stage specifications at +1 and −1 inputs for 3652 unless otherwise noted.
6. Maximum safe input current at either input is 10mA.
7. Continuous rating is 1/3 pulse rating.
8. Load current is drawn from one supply lead at a time; other supply current at quiescent level. For 3652 add 0.2mA/V of positive CMV.
9. dT/dt > 1°C/minute below 0°C, and long-term storage above 100°C is not recommended. Also limit the repeated thermal cycles to be within the 0°C to +85°C temperature range.

MECHANICAL

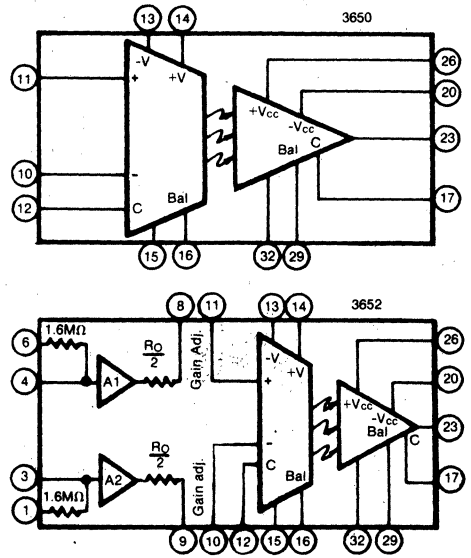


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

ORDER NUMBER:
3650MG 3652MG
3650HG 3652HG
3650JG 3652JG
3650KG

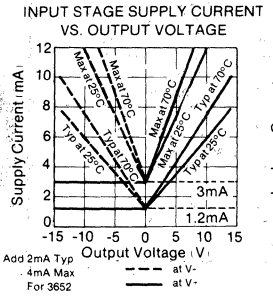
MATERIAL: Alumina (ceramic)
WEIGHT: 14 grams (0.5 oz)
MATING CONNECTOR: 2302MC (set of two, 16-pin strips)

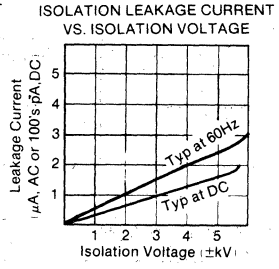
PIN CONNECTIONS

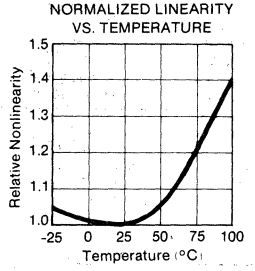


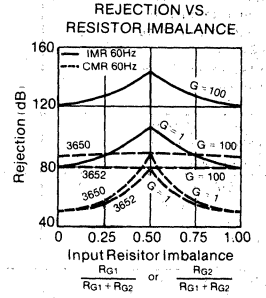
TYPICAL PERFORMANCE CURVES

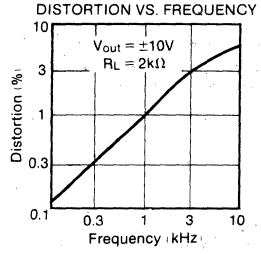
Typical at 25°C and ±15VDC power supplies unless otherwise noted.

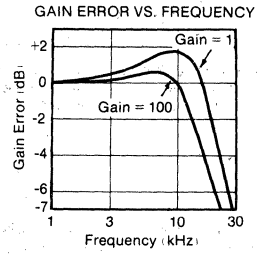


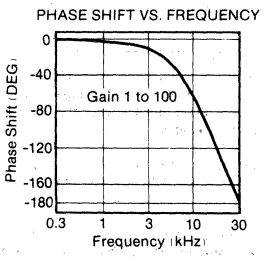


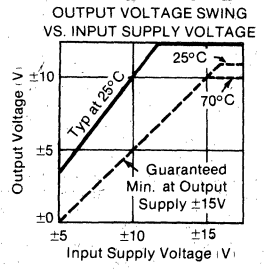


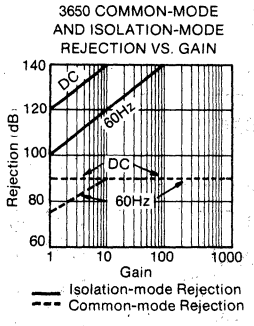


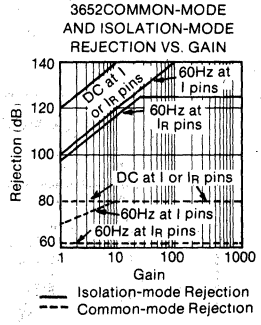


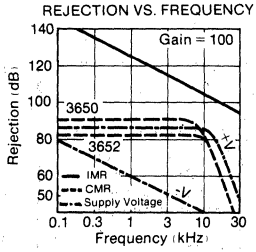


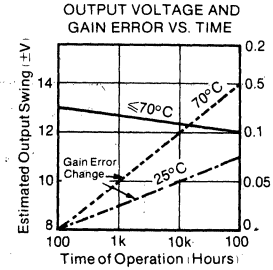












DEFINITIONS

ISOLATION-MODE VOLTAGE, V_{ISO}

The isolation-mode voltage is the voltage which appears across the isolation barrier, i.e., between the input common and the output common. (See Figure 1.)

Two isolation voltages are given in the electrical specifications; "rated continuous" and "test voltage". Since it is impractical on a production basis to test a "continuous" voltage (infinite test time is implied), it is generally accepted practice to test at a significantly higher voltage for some reasonable length of time. For the 3650 and the 3652 the "test voltage" is equal to 1000V plus two times the "rated continuous" voltage. Thus, for a continuous rating of 2000V each unit is tested at 5000V.

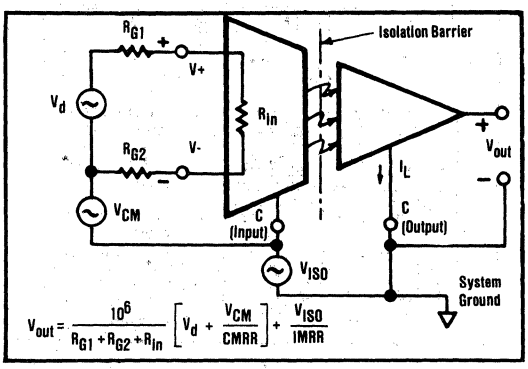


FIGURE 1. Illustration of Isolation-mode and Common-mode Specifications.

COMMON-MODE VOLTAGE, V_{CM}

The common-mode voltage is the voltage midway between the two inputs of the amplifier measured with respect to input common. It is the algebraic average of the voltage applied at the amplifiers' input terminals. In the circuit in Figure 5, $(V_+ + V_-)/2 = V_{CM}$. (Note: Many applications involve a large system "common-mode voltage." Usually in such cases the term defined here as "V_{CM}" is negligible and the system "common-mode voltage" is applied to the amplifier as "V_{ISO}" in Figure 1.)

ISOLATION-MODE REJECTION

The isolation-mode rejection is defined by the equation in Figure 1. The isolation-mode rejection is not infinite because there is some leakage across the isolation barrier due to the isolation resistance and capacitance.

NONLINEARITY

Nonlinearity is specified to be the peak deviation from a best straightline, expressed as a percent of peak-to-peak full scale output (i.e., ±10mV at 20V p-p ≈ 0.05%).

THEORY OF OPERATION

Prior to the introduction of the 3650 family optical isolation had not been practical in linear circuits. A single LED and photodiode combination, while useful in a wide range of digital isolation applications, has fundamental limitations - primarily nonlinearity and instability as a function of time and temperature.

The 3650 and 3652 use a unique technique to overcome the limitations of the single LED and photodiode isolator. Figure 2 is an elementary equivalent circuit for the 3650 which can be used to understand the basic operation without consideration the cluttering details of offset adjustment and biasing for bipolar operation.

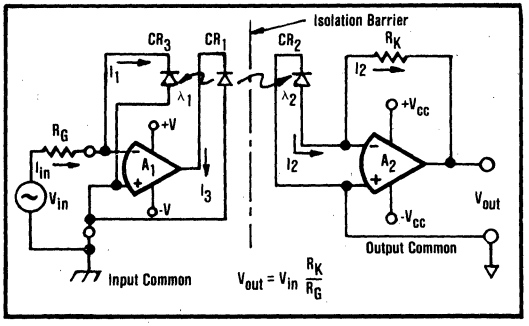


FIGURE 2. Simplified Equivalent Circuit of Linear Isolator.

Two matched photodiodes are used--one in the input (CR_3) and one in the output stage (CR_2) - - to greatly reduce nonlinearities and time - temperature instabilities. Amplifier A_1, LED CR_1, and photodiode CR_3 are used in a negative feedback configuration such that $I_1 = I_{in} R_G$ (where R_G is the user supplied gain setting resistor). Since CR_2 and CR_3 are closely matched and since they receive equal amounts of light from the LED CR_1 (i.e., $\lambda_1 = \lambda_2$), $I_2 = I_1 = I_{in}$. Amplifier A_2 is connected as a current-to-voltage converter with $V_{out} = I_2 R_K$ where R_K is an internal 1MΩ scaling resistor. Thus the overall transfer function is:

$$V_{out} = V_{in} \frac{10^6}{R_G}, \quad (R_G \text{ in ohms})$$

This improved isolator circuit overcomes the primary limitations of the single LED and photodiode combination. The transfer function is now virtually independent of any degradation in the LED output as long as the two photodiodes and optics are closely matched*. Linearity is now a function of the accuracy of the matching and is further enhanced by the use of negative feedback in the input stage. Advanced laser trimming techniques are used to further compensate for residual matching errors.

*The only effect of decreased LED output is a slight decrease in full scale swing capability. See Typical Performance Curves.

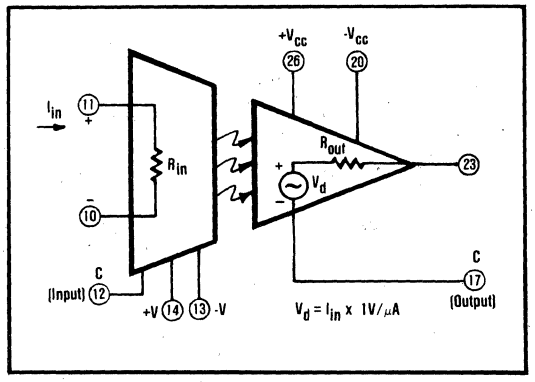


FIGURE 3. Simple Model of 3650.

A model of the 3650 suitable for simple circuit analysis is shown in Figure 3. The output is a current dependent voltage source, V_d, whose value depends on the input current. Thus, the 3650 is a transconductance amplifier with a gain of one volt per microamp. When voltage sources are used the input current is derived by using gain setting resistors in series with the voltage source (see Installation and Operating Instructions for details). R_{in} is the differential input impedance. The common-mode and isolation impedances are very high and are assumed to be infinite for this model.

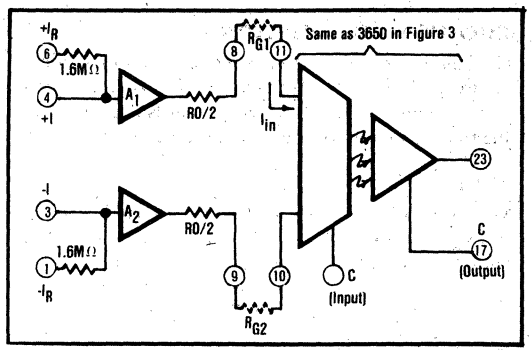


FIGURE 4. Simple Model of 3652.

A simplified model of the 3652 is shown in Figure 4. The isolation and output stages are identical to the 3650. Additional input circuitry consisting of FET buffer amplifiers and input protection resistors have been added to give higher differential and common-mode input impedance ($10^{11}\Omega$), lower bias currents (50pA) and overvoltage protection. The +IR and -IR inputs have a 10msec pulse rating of 6000V differential and 3000V common-mode (see Definitions for a discussion of common-mode and isolation-mode voltages.) The addition of the buffer amplifiers also creates a voltage-in voltage-out transfer function with the gain set by R_{G1} and R_{G2}.

INSTALLATION & OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

The power supply connections for the 3650 and 3652 are shown in Figure 5. When a DC DC converter is used for isolated power it is placed in a parallel with the isolation barrier of the amplifier. This can lower the isolation impedance and degrade the isolation-mode rejection of the overall circuit. Therefore, a high quality, low leakage DC DC converter such as the Burr-Brown Model 722 should be used.

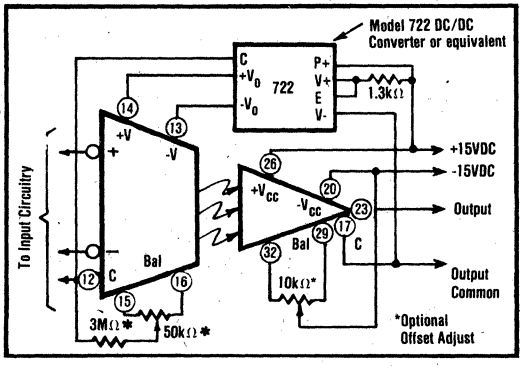


FIGURE 5. Power and Offset Adjust Connections.

OFFSET VOLTAGE ADJUSTMENTS

The offset nulling circuits are identical for the 3650 and 3652 and are shown in Figure 5. The offset adjust circuitry is optional and the units will meet the stated specifications with the BAL terminals unconnected. Provisions are available to null both the input and output stage offsets. If the amplifier is operated at a fixed gain, normally only one adjustment will be used; the output stage (10kΩ adjustment) for low gains and the input stage (50kΩ adjustment) for high gains.(>10).

Use the following procedure if it is desired to null both input and output components (for example, if the gain of the amplifier is to be switched). The input stage offset is first nulled (50kΩ adjustment) with the appropriate input signal pins connected to input common and the amplifier set at its maximum gain. The gain is then set to its minimum value and the output offset is nulled (10kΩ adjustment).

INPUT CONFIGURATIONS

Some possible input configurations for the 3650 and 3652 are shown in Figures 6a, 6b, 6c. Differential input sources are used in these examples. For situations with non-differential inputs the appropriate source term should be set to zero in the gain equations and replaced with a short in the diagrams.

Figure 6a shows the 3650 connected as a transconductance amplifier with input current sources. Voltage sources are shown in Figure 6b. In this case the voltages are converted to currents by R_{G1} and R_{G2}. As shown by the equations, they perform as gain setting resistors in the voltage transfer function. When a single voltage source is used it is recommended (but not essential) that the gain setting resistor remain split into two equal halves in order to minimize errors due to bias currents and common-mode rejection (see Typical Performance Curves).

Figure 6c illustrates the connections for the 3652 when the FET buffer amplifiers A_1 and A_2 are used. This configuration provides an isolation amplifier with high input impedance (both common-mode and differential) and good common-mode and isolation-mode rejection. It is a true isolated instrumentation amplifier which has many benefits for noise rejection when source impedance imbalances are present.

In the 3652 the voltage gain of the buffer amplifiers is slightly less than unity, but the gain of the output stage has been raised to compensate for this so that the overall transfer function from the ±I or ±IR inputs to the output is correct. It should be noted that A_1 and A_2 are buffer amplifiers. No summing can be done at the ±I or ±IR inputs. Figure 6c shows the +I and -I inputs used. If more input voltage protection is desired, then the +IR and −IR inputs should be used. This will increase the input noise due to the contribution from the 1.6MΩ resistors, but will provide additional differential and common-mode protection (10msec rating of 3kV).

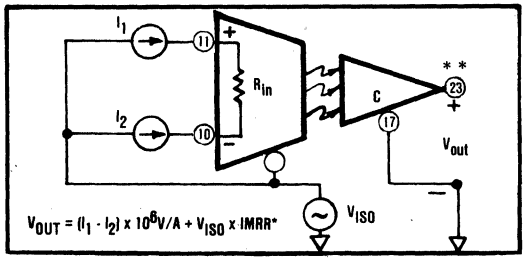


FIGURE 6a. 3650 With Differential Current Sources.

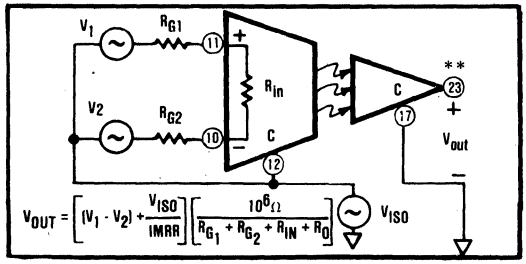


FIGURE 6b. 3650 With Differential Voltage Source.

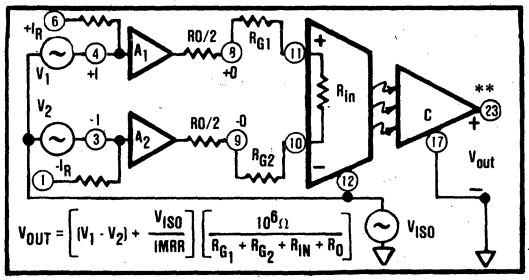


FIGURE 6c. 3652 with Differential Voltage Source.

*IMRR here is in pA V, typically 5pA V at 60Hz and 1pA V at DC.
**The offset adjustment circuitry and power supply connections have been omitted for simplicity. Refer to Figure 5 for details.

ERROR ANALYSIS

A model of the 3650 suitable for DC error analysis of offset voltage, voltage drift versus temperature, bias current, etc., is shown in Figure 7.

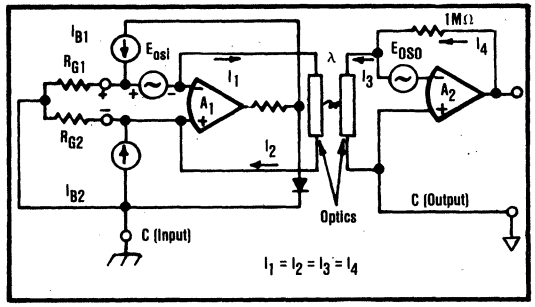


FIGURE 7. DC Error Analysis Model for 3650.

A_1 and A_2, the input and output stage amplifiers, are considered to be ideal. Separate external generators are used to model the offset voltages and bias currents. R_{in} is assumed to be small relative to R_{G1} and R_{G2} and is therefore omitted from the gain equation. The feedback configuration, optics and component matching are such that $I_1 = I_2 = I_3 = I_4$. A simple circuit analysis gives the following expression for the total output error voltage due to offset voltages and bias currents.

$$V_{out-total} = \frac{10^6}{R_{G1} + R_{G2}}\left[E_{osi} + (I_{B1} R_{G1} - I_{B2} R_{G2})\right] + E_{oso} \quad (1)$$

Offset current is defined as the difference between the two bias currents I_{B1} and I_{B2}. If $I_{B1} = I_B$ and $I_{B2} = I_B + I_{os}$, then, for $R_{G1} = R_{G2}$, $V_{out} - I_B = \frac{10^6 \cdot I_{os}}{2}$.

This component of error is not a function of gain and is therefore included as a part of E_{oso} specifications. The output errors due to the output stage bias current are also included in E_{oso}. This results in a very simple equation for the total error:

$$V_{out-total} = \frac{10^6 E_{osi}}{2R_{G1}} + E_{oso} \text{ (for } R_{G1} = R_{G2}) \quad (2)$$

In summary it should be noted that equation (2) should be used only when $R_{G1} = R_{G2}$. When $R_{G1} \neq R_{G2}$, equation (1) applies.

The effects of temperature may be analyzed by replacing the offset terms with their corresponding temperature gradient terms:

$V_{out} \rightarrow \Delta V_{out}$ ΔT, $E_{osi} \rightarrow \Delta E_{osi}$ ΔT, etc.

For a complete analysis of the effects of temperature, gain variations must also be considered.

OUTPUT NOISE

The total output noise is given by

$$E_n\,(RMS) = \sqrt{(E_{ni}\,G)^2 + (E_{nO})^2}$$

where E_n (RMS) = total output noise
E_{ni} = RMS noise of the input stage
E_{nO} = RMS noise of the output stage
$G = 10^6\ (R_{G1} + R_{G2})$

E_{nO} includes the noise contribution due to the optics and the noise currents of the output stage. Errors created by the noise current of the input stage are insignificant compared to other noise sources and are therefore omitted.

COMMON-MODE and ISOLATION-MODE REJECTION

The expression for the output error due to common-mode and isolation mode voltage is:

$$V_{out} = G\left[\frac{V_{cm}}{CMRR} + \frac{V_{iso}}{IMRR}\right]$$

GUARDING & PROTECTION

To preserve the excellent inherent isolation characteristics of these amplifiers, the following recommended practice should be noted:

1. Use shielded, twisted pair of cable at the input as with any instrumentation amplifier;
2. Care sould be taken to minimize external capacitance. A symmetrical layout of external components to achieve balanced capacitance from the input terminals to output common will preserve high IMR;
3. External components and conductor patterns should be at a distance equal to or greater than the distance between the input and output terminals, to prevent HV breakdown.
4. Though not an absolute requirement, the use of laminated or conformally coated printed circuit boards is recommended.

APPLICATIONS

Figure 8 shows a system where isolation amplifiers (3650) are used to measure the armature current and the armature voltage of a motor.

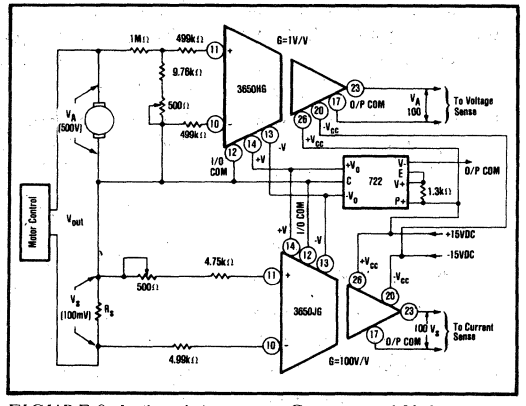


FIGURE 8. Isolated Armature Current and Voltage Sensor.

The armature current of the motor is converted to a voltage by the calibrated shunt R, and then amplifier (adjustable gain) and isolated by the 3650.

The armature voltage is sensed by the voltage divider (adjustable) shown and then amplified and isolated by the 3650.

The 3650 provides the advantage of accurate current measurement in the presence of high common-mode voltage. Both 3650's provide the advantage of isolating the motor ground from the control system ground. Isolated power is provided by an isolated DC/DC converter (BB Model 722 or equivalent).

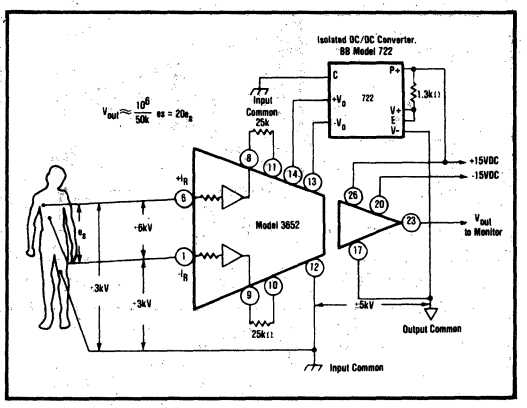


FIGURE 9. 3652 Used in Patient Monitoring Application (ECG, VCG, EMG Amplifier).

The 3652 is ideally suited for patient monitoring applications as shown in Figure 9. The fact that it is a true balanced input instrumentation amplifier with very high differential and common-mode inpedance means that it can greatly reduce the common-mode noise pick up due to imbalance in lead impedances that often appear in patient monitoring situations. The 3kV and 6kV shown in Figure 9 are the 10msec pulse ratings of the +IR and -IR inputs for the common-mode and differential input voltages with respect to input common. The rating of the isolation barrier is 2000V, pk continuous. The non-recurrent pulse rating of the isolation barrier is 5000V, pk since each unit is factory tested at 5000V, pk. If the isolation barrier is to be subjected to higher voltages a gas filled surge voltage protection device can be used. For multichannel operation, two 3562's can be powered by one Model 722 isolated DC/DC converter. The total leakage current for both channels at 240V/60Hz would still be less than 2μA.

The block diagram in Figure 10 shows the use of isolation amplifiers in SCR control application.

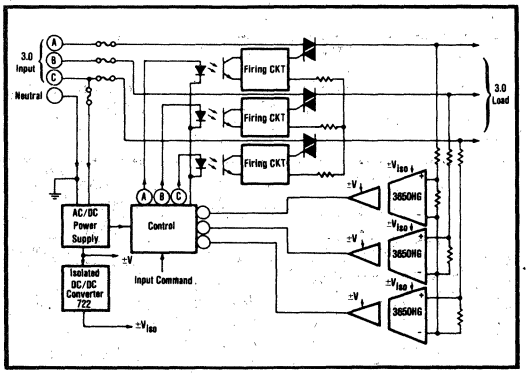
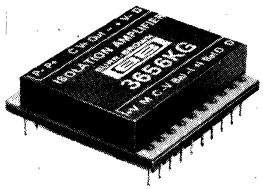


FIGURE 10. 3-Phase Bidirectional SCR Control with Voltage Feedback.

BURR-BROWN®

3656



Integrated Circuit - Transformer Coupled ISOLATION AMPLIFIER

FEATURES

- INTERNAL ISOLATED POWER
- 8000V ISOLATION TEST VOLTAGE
- 0.5μA MAX LEAKAGE AT 120V, 60Hz
- 3-PORT ISOLATION
- 125dB REJECTION AT 60Hz
- 1" x 1" x 0.25" CERAMIC PACKAGE

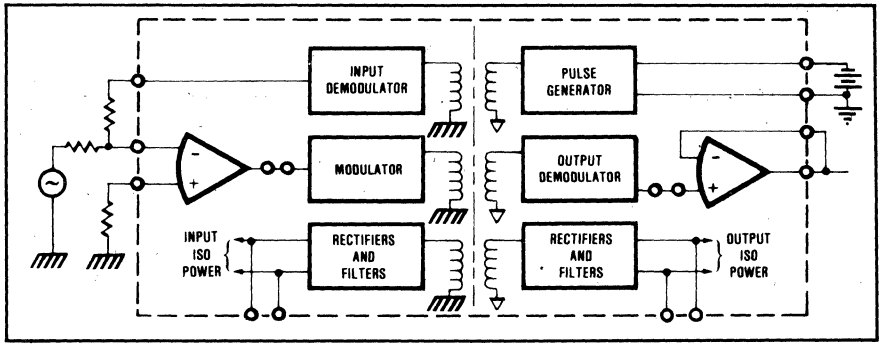
APPLICATIONS

- MEDICAL
  Patient monitoring and diagnostic instrumentation
- INDUSTRIAL
  Ground loop elimination and off-ground signal measurement
- NUCLEAR
  Input/output/power isolation

DESCRIPTION

The 3656 is the first amplifier to provide a total isolation function ... both signal and power isolation ... in integrated circuit form. This remarkable advancement in analog signal processing capability is accomplished by use of a patented modulation technique and minature hybrid transformer.

Versatility and performance are outstanding features of the 3656. It is capable of operating with three completely independent grounds (three-port isolation). In addition, the isolated power generated is available to power external circuitry at either the input or output. The uncommitted op amps at the input and the output allow a wide variety of closed-loop configurations to match the requirements of many different types of isolation applications.



This product is covered by the following United States patents: 4,066,974; 4,103,267; 4, 082,908. Other patents pending may also apply upon the allowance and issuance of patents thereon. The product may also be covered in other countries by one or more international patents corresponding to the above-identified U.S. patents.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

THEORY OF OPERATION

Details of the 3656 are shown in Figure 1. The external connections shown, place it in its simplest gain configuration - unity gain, noninverting. Several other amplifier gain configurations and power isolation configurations are possible. See Installation and Operating Instructions and Applications sections for details.

Isolation of both signal and power is accomplished with a single miniature toroid transformer with multiple windings. A pulse generator operating at approximately 750kHz provides a two-part voltage waveform to transformer T_1. One part of the waveform is rectified by diodes D_1 through D_4 to provide the isolated power to the input and output stages (+V, -V and V+, V-). The other part of the waveform is modulated with input signal information by the modulator operating into the V_2 winding of the transformer.

The modulated signal is coupled by windings W_6 and W_7 to two matched demodulators - one in the input stage and one in the output stage - which generate identical voltages at their outputs, pins 10 and 11 (voltages identical with respect to their respective commons, pins 3 and 17). In the input stage the input amplifier A_1, the modulator and the input demodulator are connected in a negative feedback loop. This forces the voltage at pin 6 (connect as shown in Figure 1) to equal the input signal voltage applied at pin 7. Since the input and the output demodulators are matched and produce identical output voltages, the voltage at pin 11 (referenced to pin 17, the output common) is equal to the voltage at pin 10 (referenced to pin 3, the input common). In the output stage, output amplifier A_2 is connected as a unity gain buffer, thus the output voltage at pin 15 equals the output demodulator voltage at pin 11. The end result is an isolated output voltage at pin 15 equal to the input voltage at pin 7 with no galvanic connection between them.

Several amplifier and power connection variations are possible:

1. The input stage may be connected in various operational amplifier gain configurations.
2. The output stage may be operated at gains above unity.
3. The internally generated isolated voltages which provide power to A_1 and A_2 may be overridden and external supply voltages used instead.

Versatility and its three independent isolated grounds allow simple solutions to demanding analog signal conditioning problems. See the Installation and Operating Instructions and Applications sections for details.

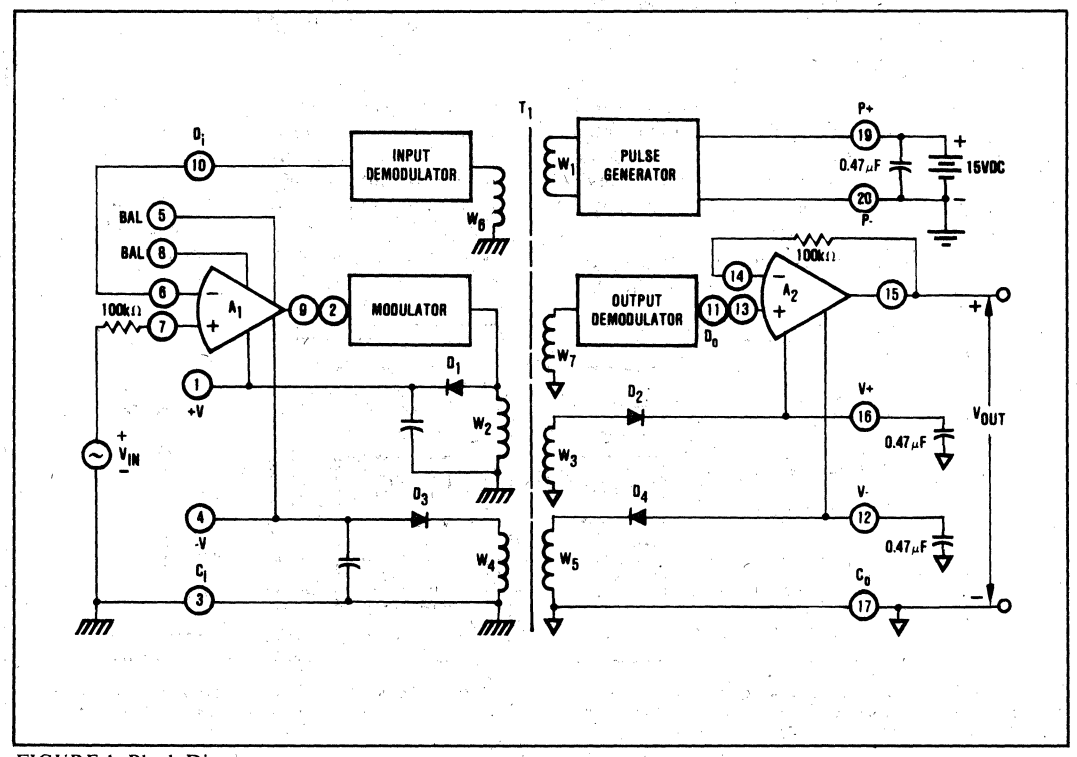


FIGURE 1. Block Diagram.

SPECIFICATIONS

ELECTRICAL

At +25°C, V± = 15VDC and 15VDC between P+ and P-, unless otherwise noted.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG			UNITS
		MIN	TYP	MAX	
ISOLATION					
Voltage					
Rated Continuous(1), DC		3500 (1000)			VDC
Rate Continuous(2), AC		2000 (700)			V, rms
Test, 10sec(1)		8000 (3000)			VDC
Rejection	G_1 = 10V/V				
DC			160		dB
60Hz, < 100Ω in I/P Com(2)			125		dB
60Hz, 5kΩ in I/P Com(2)					
3656HG		108			dB
3656AG, BG, JG, KG		112			dB
Capacitance(1)			6.0 (6.3)		pF
Resistance(1)			10^{12} (10^{12})		Ω
Leakage Current	120V, 60Hz		0.28	0.5	μA
GAIN					
Equations	See Text				
Accuracy of Equations					
Initial(3) 3656HG	G < 100V/V			1.5	%
3656AG, JG, KG				1.0	%
3656BG				0.3	%
vs. Temperature 3656HG				480	ppm/°C
3656AG, JG				120	ppm/°C
3656BG, KG				60	ppm/°C
vs. Time			0.02 (1 + log khrs.)		%
Nonlinearity	$R_A + R_F = R_B \geq 2M\Omega$				
External Supplies used at					
pins 12 and 16, 3656HG	Unipolar or Bipolar Output			±0.15	%
3656AG, JG, KG				±0.1	%
3656BG				±0.05	%
Internal Supplies used for	Bipolar Output Voltage				
Output Stage	Swing, Full Load(4)		±0.15		%
OFFSET VOLTAGE(5)	RTI				
Initial(3), 3656HG	15V_P between P+ and P-			±|4 + 40/G_1|	mV
3656AG, JG				±|2 + 20/G_1|	mV
3656BG, KG				±|1 + 10/G_1|	mV
vs. Temperature, 3656HG				±|200 + 1000/G_1|	μV/°C
3656JG				±|50 + 750/G_1|	μV/°C
3656AG				±|25 + (500/G_1)|	μV/°C
3656KG				±|10 + 350/G_1|	μV/°C
3656BG				±|5 + 350/G_1|	μV/°C
vs. Supply Voltage	Supply between P+ and P-				
3656HG				±|0.6 + 3.5/G_1|	mV/V
3656AG, BG, JG, KG				±|0.3 + 2.1/G_1|	mV/V
vs. Current(6)			±|0.1 + 10/G_1|	±|0.2 + (20/G_1)|	mV/mA
vs. Time			±|10 + 100/G_1| x (1 + log khrs.)		μV
AMPLIFIER PARAMETERS	Apply to A1 and A2				
Bias Current(7)					
Initial				100	nA
vs. Temperature			0.5		nA/°C
vs. Supply			0.2		nA/V
Offset Current(7)			5	20	nA
Impedance	Common-mode		100 || 5		MΩ || pF
Input Noise Voltage	f_B = 0.05Hz to 100Hz		5		μV, p-p
	f_B = 10Hz to 10kHz		5		μV, rms
Input Voltage Range(8)					
Linear Operation	Internal Supply			±5	V
	External Supply			Supply -5V	V
Without Damage	Internal Supply			±8	V
	External Supply			Supply	V
Output Current	V_{OUT} = ±5V				
	±15V External Supply	±5			mA
	Internal Supply	±2.5			mA
	V_{OUT} = ±10V				
	±15V External Supply	±2.5			mA
	V_{OUT} = ±2V, V_{P+}, P_{-} = 8.5V				
	Internal Supply		±1		mA
Quiescent Current			150	450	μA

ELECTRICAL (CONT)

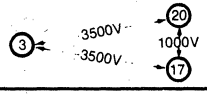
At +25°C, V± = 15VDC and 15VDC between P+ and P-, unless otherwise noted.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG			UNITS
		MIN	TYP	MAX	
FREQUENCY RESPONSE					
±3dB Response	Small Signal		30		kHz
Full Power			1.3		kHz
Slew Rate	Direction measured at output	+0.1, -0.04			V/μsec
Settling Time	to 0.05%		500		μsec
OUTPUT					
Noise Voltage (RTI)	f_B = 0.05Hz to 100Hz		$\sqrt{(5)^2 + (22/G_1)^2}$		μV, p-p
	f_B = 10Hz to 10kHz		$\sqrt{(5)^2 + (11/G_1)^2}$		μV, rms
Residual Ripple[9]			5		mV, p-p
POWER SUPPLY IN	at P+, P-				
Rated Performance			15		VDC
Voltage Range[10]	Derated Performance	8.5		16	VDC
Ripple Current[9]			10	25	mA, p-p
Quiescent Current[11]	Average		14	18	mA, DC
Current vs. Load Current[12]	vs. Currents from +V, -V, V+, V-		0.7		mA/mA
ISOLATED POWER OUT	at +V, -V, V+, V- pins[13]				
Voltage, no load	15V between P+ and P-	8.5	9.0	9.5	V
Voltage, full load	±5mA (10mA sum) load[12]	7.0	8.0	9.0	V
Voltage vs. Power Supply	vs. Supply between P+ and P-		0.66		V/V
Ripple Voltage[9]					
No load			40		mV, p-p
Full load	±5mA load		80	200	mV, p-p
TEMPERATURE RANGE					
Specification 3656AG, BG		-25		+85	°C
3656HG, JG, KG		0		+70	°C
Operation[10]		-55		+100	°C
Storage[14]		-65		+125	°C

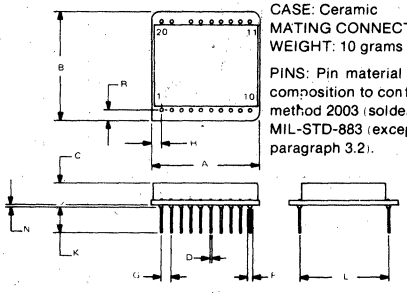
NOTES:

1. Ratings in parenthesis and between P- (pin 20) and O/P Com (pin 17). Other isolation ratings are between I/P Com and O/P Com or I/P Com and P-.

An example of the ratings for 3-port continuous isolation.



MECHANICAL



CASE: Ceramic
MATING CONNECTOR: None
WEIGHT: 10 grams (0.35 oz.)

PINS: Pin material and plating composition to conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.080	1.120	27.43	28.45
B	1.080	1.120	27.43	28.45
C	.235	.300	5.97	7.62
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.100 BASIC		2.54 BASIC	

2. May be improved with proper shielding. See Performance Curves.
3. May be trimmed to zero.
4. If output swing is unipolar, or if the output is not loaded, specification same as if external supply were used.
5. Includes effects of A_1 and A_2 offset voltages and bias currents if recommended resistors used.
6. Versus the sum of all external currents drawn from V+, V-, +V, -V (= ISO).
7. Effects of A_1 and A_2 bias currents and offset currents are included in Offset Voltage specifications.
8. With respect to I/P Com (pin 3) for A_1 and with respect to O/P Com (pin 17) for A_2. CMR for A_1 and A_2 is 100dB, typical.
9. In configuration of Figure 3. Ripple frequency approximately 750kHz. Measurement bandwidth is 30kHz.
10. Decreases linearly from 16VDC at 85°C to 12VDC at 100°C.
11. Instantaneous peak current required from pins 19 and 20 at turn-on is 100mA for slow rising voltages (50msec) and 300mA for fast rises (50μsec).
12. Load current is sum drawn from +V, -V, V+, V- (= I_{ISO}).
13. Maximum voltage rating at pins 1 and 4 is ±18VDC; maximum voltage rating at pins 12 and 16 is ±18VDC.
14. Isolation ratings may degrade if exposed to 125°C for more than 1000 hours or 90°C for more than 50,000 hours.

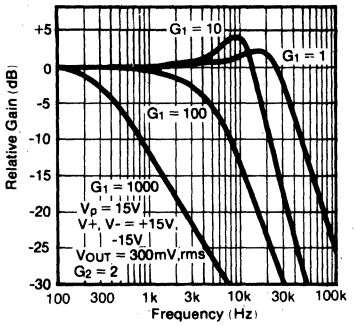
PIN DESIGNATIONS

1.	+V	11.	OUTPUT DEMOD
2.	MOD INPUT	12.	V-
3.	INPUT DEMOD COM	13.	A_2 NONINVERTING INPUT
4.	-V	14.	A_2 INVERTING INPUT
5.	BALANCE	15.	A_2 OUTPUT
6.	A_1 INVERTING INPUT	16.	V+
7.	A_1 NONINVERTING INPUT	17.	OUTPUT DEMOD COM
8.	BALANCE	18.	NO PIN
9.	A_1 OUTPUT	19.	P+
10.	INPUT DEMOD	20.	P-

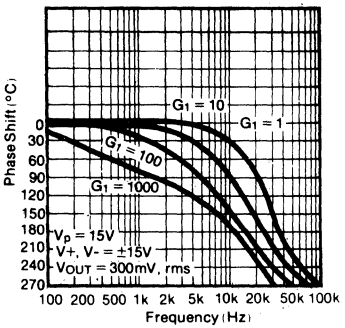
TYPICAL PERFORMANCE CURVES

All specifications typical at +25°C unless otherwise noted.

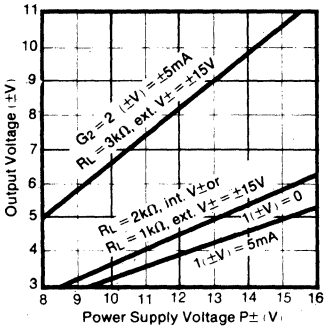
SMALL SIGNAL FREQUENCY RESPONSE



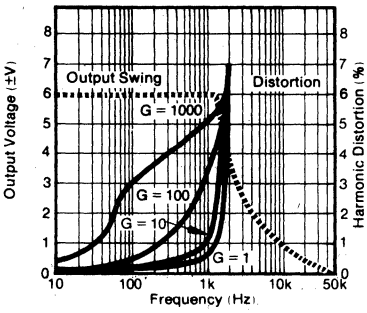
PHASE RESPONSE



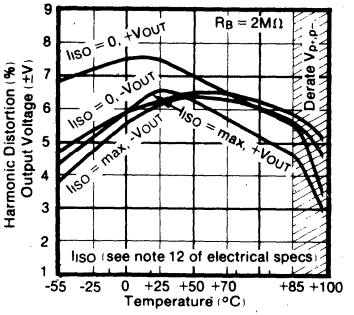
OUTPUT SWING VS SUPPLY VOLTAGE



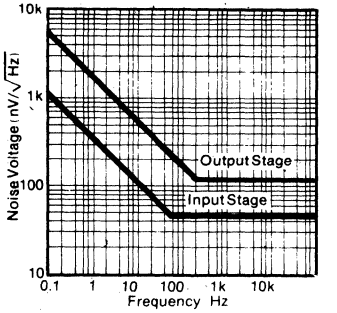
OUTPUT SWING AND DISTORTION VS FREQUENCY



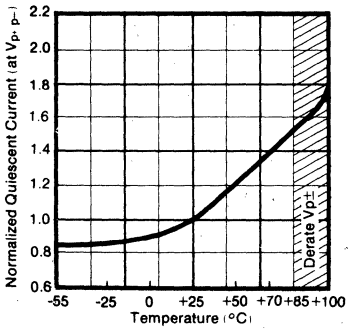
OUTPUT VOLTAGE SWING VS TEMPERATURE AND ISOLATED SUPPLY LOAD



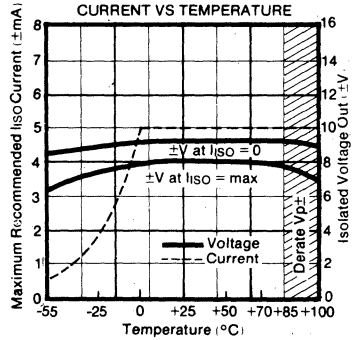
NOISE VOLTAGE VS FREQUENCY



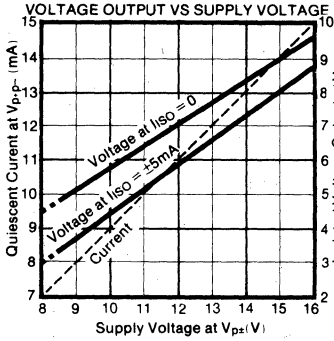
QUIESCENT CURRENT VS TEMPERATURE



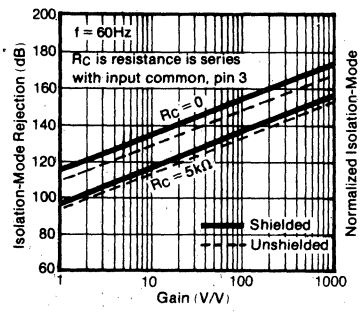
ISOLATED OUTPUT VOLTAGE AND CURRENT VS TEMPERATURE



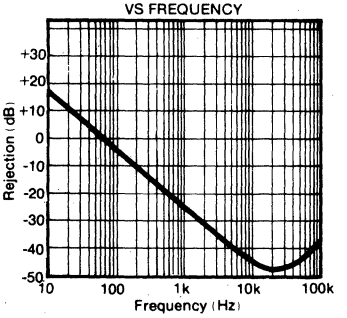
QUIESCENT CURRENT AND ISOLATED VOLTAGE OUTPUT VS SUPPLY VOLTAGE



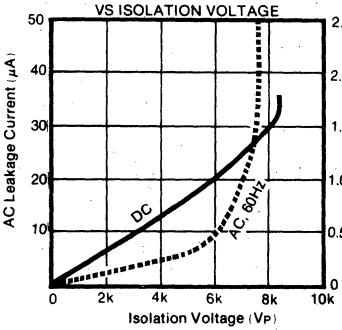
ISOLATION-MODE REJECTION VS GAIN



ISOLATION-MODE REJECTION VS FREQUENCY



AC AND DC LEAKAGE CURRENT VS ISOLATION VOLTAGE



INSTALLATION AND OPERATING INSTRUCTIONS

The 3656 is a very versatile device capable of being used in a variety of isolation and amplification configurations. There are several fundamental considerations that determine configuration and component value constraints:

1. Consideration must be given to the load placed on the resistance (pin 10 and pin 11) by external circuitry. Their output resistance is 100kΩ and a load resistor of 2MΩ or greater is recommended to prevent a voltage divider loading effect in excess of 5%.
2. Demodulator loadings should be closely matched so their output voltages will be equal. (Unequal demodulator output voltages will produce a gain error.) At the 2MΩ level, a matching error of 5% will cause an additional gain error of 0.25%.
3. Voltage swings at demodulator outputs should be limited to 5V. The output may be distorted if this limit is exceeded. This constrains the maximum allowed gains of the input and output stages. Note that the voltage swings at demodulator outputs are tested with 2MΩ load for a minimum of 5V.
4. Total current drawn from the internal isolated supplies must be limited to less than ±5mA per supply and limited to t total of 10mA. In other words, the combination of external and internal current drawn from the internal circuitry which feeds the +V, -V, V+ and V- pins should be limited to 5mA per supply (total current to +V, -V, V+ and V- limited to 10mA). The internal filter capacitors for ±V are 0.01μF. If more than 0.1mA is drawn to provide isolated power for external circuitry (see Figure 12), additional capacitors are required to provide adequate filtering. A minimum of 0.1μF/mA is recommended.
5. The input voltage at pin 7 (noninverting input to A_1) must not exceed the voltage at pin 4 (negative supply voltage for A_1) in order to prevent a possible lockup condition. A low leakage diode connected between pins 7 and 4, as shown in Figure 2, can be used to limit this input voltage swing.
6. Impedances seen by each amplifier's + and - input terminals should be matched to minimize offset voltages caused by amplifier input bias currents. Since the demodulators have a 100kΩ output resistance, the amplifier input not connected to the demodulator should also see 100kΩ.
7. All external filter capacitors should be mounted as close to the respective supply pins as is possible in order to prevent excessive ripple voltages on the supplies or at the output. (Optimum spacing is less than 0.5". Ceramic capacitors recommended.)

POWER AND SIGNAL CONFIGURATIONS

NOTE: Figures 2, 3 and 4 are used to illustrate both signal and power connection configurations. In the circuits shown, the power and signal configurations are independent so that any power configuration could be used with any signal configuration.

ISOLATED POWER CONFIGURATIONS

The 3656 is designed with isolation between the input, the output, and the power connections. The internally generated isolated voltages supplied to A_1 and A_2 may be overridden with external voltages greater than the internal supply voltages. These two features of 3656 provide a great deal of versatility in possible isolation and power supply hook-ups. When external supplies are applied, the rectifying diodes (D_1 through D_4) are reverse biased and the internal voltage sources are decoupled from the amplifiers (see Figure 1). Note that when external supplies are used, they must never be lower than the internal supply voltage.

Three-Port

The power supply connections in Figure 2 show the full three-port isolation configuration. The system has three separate grounds with no galvanic connections between them. The two external 0.47μF capacitors at pins 12 and 16 filter the rectified isolated voltage at the output stage. Filtering on the input stage is provided by internal capacitors. In this configuration continuous isolation voltage ratings are: 3500V between pins 3 and 17; 3500V between pins 3 and 19; 1000V between pins 17 and 19.

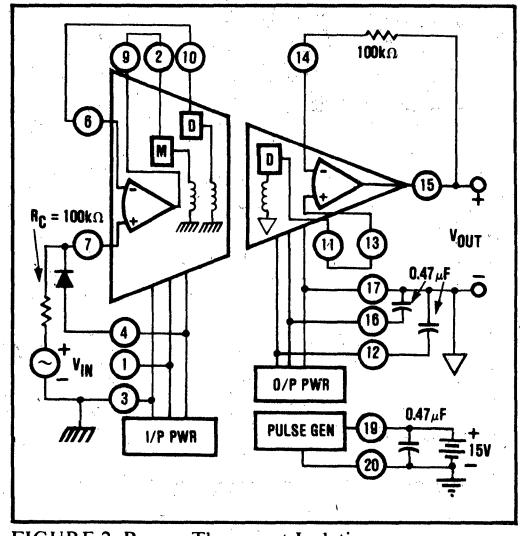


FIGURE 2. Power: Three-port Isolation; Signal: Unity-gain Noninverting.

Two-Port - Bipolar Supply

Figure 3 shows two-port isolation which uses an external bipolar supply with its common connected to the output stage ground (pin 17). One of the supplies (either + or - could be used) provides power to the pulse generator (pins 19 and 20). The same sort of configuration is possible with the external supplies connected to the input stage. With the connection shown, filtering at pins 12 and 16 is not required. In this configuration continuous isolation voltage rating is: 3500VDC between pins 3 and 17; not applicable between pins 17 and 19; 3500VDC between pins 3 and 19.

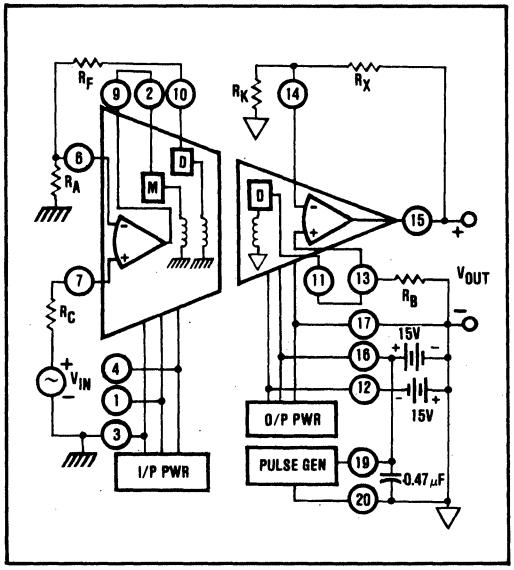


FIGURE 3. Power: Two-port, Dual Supply; Signal: Noninverting Gain.

Two-Port Single Supply

Figure 4 demonstrates two-port isolation using a single polarity supply connected to the output common (pin 17). The other polarity of supply for A_2 is internally generated (thus the filtering at pin 12). This isolated power configuration could be used at the input stage as well and either polarity of supply could be employed. In this configuration continuous isolation voltage rating is: 3500V between pins 3 and 17; 3500V between pins 3 and 19; not applicable between pins 17 and 19.

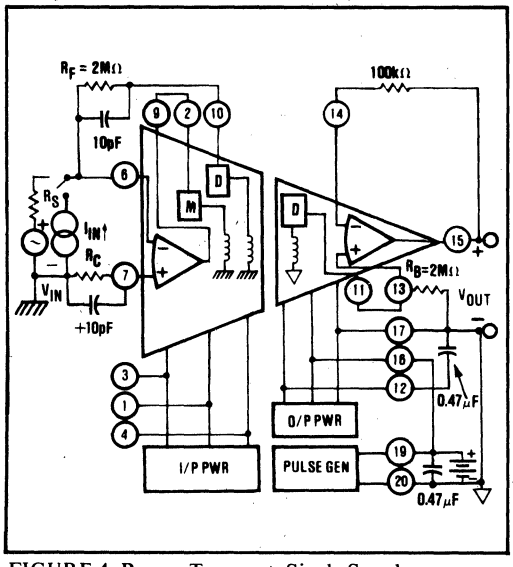


FIGURE 4. Power: Two-port, Single Supply; Signal: Inverting Gains.

SIGNAL CONFIGURATIONS

Unity Gain Noninverting

The signal path portion of Figure 2 shows the 3656 in its simplest gain configuration: unity gain noninverting. The two 100kΩ resistors provide balanced resistances to the inverting and noninverting inputs of the amplifiers. The diode prevents latch up in case the input voltage goes more negative than the voltage at pin 4.

Noninverting With Gain

The signal path portion of Figure 3 demonstrates two additional gain configurations: gain in the otuput stage and noninverting gain in the input stage. The following equations apply:

Total amplifier gain:

$G = G_1 \bullet G_2 = V_{OUT}/V_{IN}$ (1)

Input Stage:

$G_1 = 1 + (R_F/R_A)$ (Select G_1 to be less than 5V/full scale V_{In} to limit demodulator output to 5V) (2)

$R_A + R_F \geq 2M\Omega$ (Select to load input demodulator with at least 2MΩ) (3)

$R_C = R_A \parallel (R_F + 100k\Omega) =$

$$\frac{R_A (R_F + 100k\Omega)}{R_A + R_F + 100k\Omega}$$

(Balance impedances seen by the + and - inputs of A_1 to reduce input offset caused by bias current) (4)

Output Stage:

$G_2 = 1 + (R_X/R_K)$ (Select ratio to obtain V_{OUT} between 5V and 10V full scale with V_{IN} at its maximum) (5)

$R_X \parallel R_K = 100k\Omega$ (Balance impedances seen by the + and - inputs of A_2 to reduce effect of bias current on the output offset) (6)

$R_B = R_A + R_F$ (Load output demodulator equal to input demodulator) (7)

Inverting Gain, Voltage or Current Input

The signal portion of Figure 4 shows two possible inverting input stage configurations: current and input and voltage input.

Input Stage:

For the voltage input case:

$G_1 = -R_F/R_S$ (Select G_1 to be less than 5V/full scale V_{IN} to limit the demodulator output voltage to 5V) (8)

$R_F = 2M\Omega$ (Select to load the demodulator with at least 2MΩ) (9)

$$R_C = R_S \parallel (R_F + 100k\Omega) = \frac{R_S (R_F + 100k\Omega)}{R_S + R_F + 100k\Omega}$$

(Balance the impedances seen by the + and - inputs of A_1). (10)

For the current input case:

$$V_{OUT} = -I_{IN} R_F \bullet G_2 \quad (11)$$

$$R_C = R_F \quad (12)$$

R_F may be made larger than 2MΩ if desired. The 10pF capacitors are used to compensate for the input capacitance of A_1 and to insure frequency stability.

Output Stage:

The output stage is the same as shown in equations (5), (6), and (7).

Illustrative Calculations:

The maximum input voltage is 100mV. It is desired to amplify the input signal for maximum accuracy. Non-inverting output is desired.

Input Stage:

Step 1

G_1 max = 5V/Max Input Signal = 5V/0.1V = 50V/V

With the above gain of 50V/V, if the input ever exceeds 100mV, it would drive the output to saturation. Therefore, it is good practice to allow reasonable input overrange.

So, to allow for 25% input overrange without saturation at the output, select:

$$G_1 = 40V/V$$

$$G_1 = 1 + (R_F + R_A) = 40$$

$$\therefore R_F/R_A = 39 \quad (13)$$

Step 2

$R_A + R_F$ forms a voltage divider with the 100kΩ output resistance of the demodulator. To limit the voltage divider loading effect to no more than 5%, $R_A + R_F$ should be chosen to be at least 2MΩ. For most applications, the 2MΩ should be sufficiently large for $R_A + R_F$. Resistances greater than 2MΩ may help decrease the loading effect, but would increase the offset voltage drift.

The voltage divider with $R_A + R_F = 2M\Omega$ is 2MΩ/(2MΩ + 100kΩ) = 2/(2 + 0.1) = 95.2%, i.e., the percent loading is 4.8%.

Choose $R_A + R_F = 2M\Omega \quad (14)$

Step 3

Solving equations (13) and (14)

$R_A = 50k\Omega$ and $R_F = 1.95M\Omega$

Step 4

The resistances seen by the + and - input terminals of the input amplifier A_1 should be closely matched in order to minimize offset voltage due to bias currents.

$$\therefore R_C = R_A \parallel (R_F + 100k\Omega)$$
$$= 50k\Omega \parallel (1.95M\Omega + 100k\Omega)$$
$$\approx 49k\Omega$$

Output Stage:

Step 5

$$V_{OUT} = V_{IN\ MAX} \bullet G_1 \bullet G_2$$

As discussed in Step 1, it is good practice to provide 25% input overrange.

So we will calculate G_2 for 10V output and 125% of the maximum input voltage.

$$\therefore V_{OUT} = (1.25 \times 0.1)(G_1)(G_2)$$

i.e., $10V = 0.125 \times 40 \times G_2$

$$\therefore G_2 = 10V/5V = 2V/V$$

Step 6

$$G_2 = 1 + (R_X/R_K) = 2.0$$

$$\therefore R_X/R_K = 1.0$$

$$\therefore R_X = R_K \quad (15)$$

Step 7

The resistance seen by the + input terminal of the output stage amplifier A_2 (pin 13) is the output resistance 100kΩ of the output demodulator. The resistance seen by the (-) input terminal of A_2(pin14)should be matched to the resistance seen by the + input terminal.

The resistance seen by pin 14 is the parallel combination of R_X and R_K.

$$\therefore R_X \parallel R_K = 100k\Omega$$

i.e., $(R_X \bullet R_K/(R_X + R_K) = 100k\Omega$

i.e., $R_K/[1 + (R_K/R_X)] = 100k\Omega \quad (16)$

Step 8

Solving equations (15) and (16) $R_K = 20k\Omega$ and $R_X = 200k\Omega$.

Step 9

The otuput demodulator must be loaded equal to the input demodulator.

$$\therefore R_B = R_A + R_F = 2M\Omega$$

(See equation (14) above in Step 2)

Use the resistor values obtained in Steps 3, 4, 8 and 9, and connect the 3656 as shown in Figure 3.

OFFSET TRIMMING

Figure 5 shows an optional offset voltage trim circuit. It is important that $R_A + R_F = R_B$.

CASE 1: Input and output stages in low gain, use output potentiometer (R_2) only. Input potentiometer (R_1) may be disconnected. For example, unity gain could be obtained by setting $R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_F = 0$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 2: Input stage in high gain and output stage in low gain, use input potentiometer (R_1) only. Output potentiometer (R_2) may be disconnected. For example, $G_T = 100$ could be obtained by setting $R_F = 2M\Omega$, $R_B = 2M\Omega$ returned to pin 17, $R_A = 20k\Omega$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 3: When it is necessary to perform a two-stage precision trim (to maintain a very small offset change under conditions of changing temperature and changing gain in A_1 and A_2), use step 1 to adjust the input stage and step 2 for the output stage. Carbon composition resistors are acceptable but potentiometers should be stable.

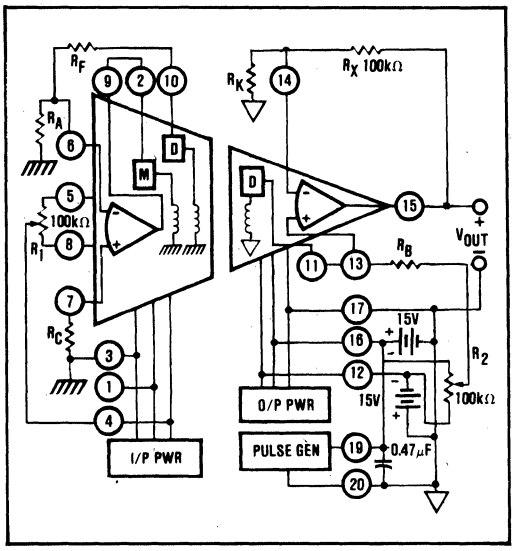


FIGURE 5. Optional Offset Voltage Trim.

Step 1: Input stage trim ($R_A = R_C = 20k\Omega$, $R_F = R_B = 20M\Omega$, $R_X = 100k\Omega$, $R_K = \infty$, R_2 disconnected); A_1 high, A_2 low gain. Adjust R_1 for 0V ±5mV or desired setting at V_{OUT}, pin 15.

Step 2: Output stage trim ($R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_F = 0$, $R_X = 100k\Omega$, $R_K = \infty$, R_1 and R_2 connected); A_1 low, A_2 low gain. Adjust R_2 for 0V ±1mV or desired setting at V_{OUT}, pin 15 (±110mV approximate total range).

Note: Other circuit component values can be used with valid results.

APPLICATIONS

ECG AMPLIFIER

Although the features of the circuit shown in Figure 6 are important in patient monitoring applications, they may also be useful in other applications. The input circuitry uses an external, low quiescent current op amp (OPA21 type) powered by the isolated power of the input stage to form a high impedance instrumentation amplifier input (true three-wire input). R_3 and R_4 give the input stage amplifier of the 3656 a noninverting gain of 10 and an inverting gain of -9. R_1 and R_2 give the external amplifier a noninverting gain of 1 + 1/9. The inputs are applied to the noninverting inputs of the two amplifiers and the composite input stage amplifier has a gain of 10.

The 330kΩ, 1W, carbon resistors and diodes D_1 - D_4 provide protection for the input amplifiers from defibrillation pulses.

The output stage in Figure 6 is configured to provide a bandpass filter with a gain of 22.7 (68MΩ/3MΩ). The high-pass section (0.05Hz cutoff) is formed by the 1μF capacitor and 2MΩ resistor which are connected in series between the output demodulator and the inverting input of the output stage amplifier. The low-pass section (100Hz cutoff) is formed by the 68MΩ resistor and 22pF capacitor located in the feedback loop of the output stage. The diodes provide for quick recovery of the high-pass filter to overvoltages at the input. The 100kΩ pot and the 100MΩ resistor allow the output voltage to be trimmed to compensate for increased offset voltage caused by unbalanced impedances seen by the inputs of the output stage amplifier.

In many modern electrocardiographic systems, the

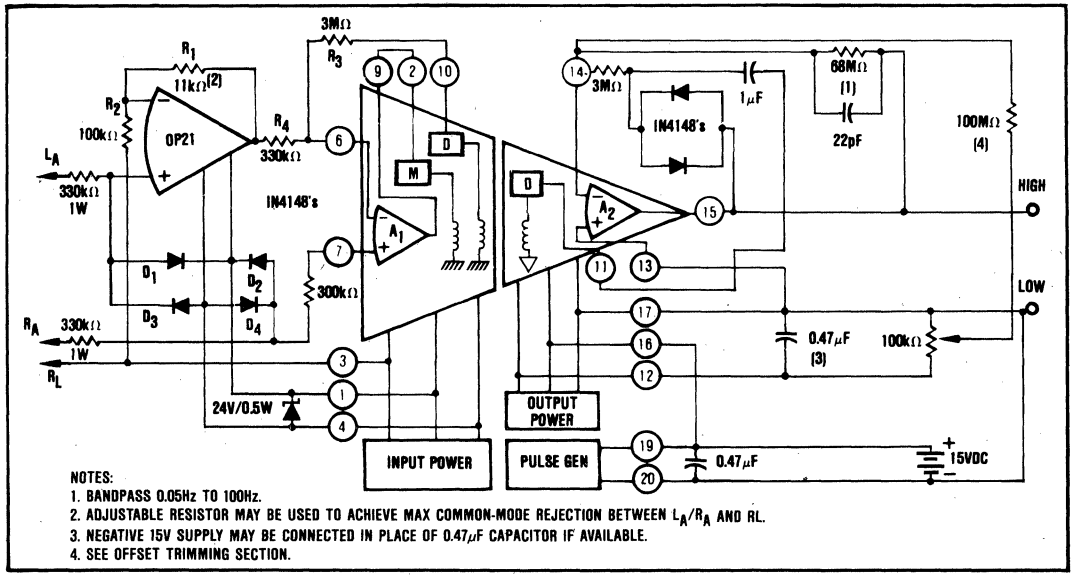


FIGURE 6. ECG Amplifier.

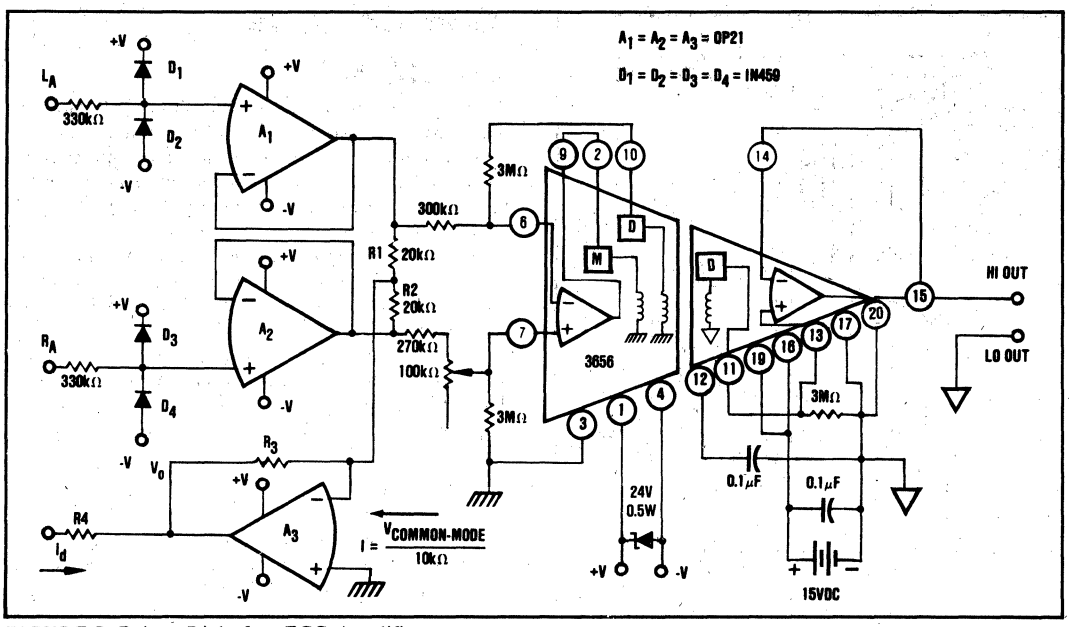


FIGURE 7. Driven Right-Leg ECG Amplifier.

patient is not grounded. Instead, the right-leg electrode is connected to the output of an auxiliary operational amplifier as shown in Figure 7. In this circuit, the common-mode voltage on the body is sensed by the two averaging resistors R_1 and R_2, inverted, amplified, and fed back to the right-leg through resistor R_4. This negative feedback drives the common-mode voltage to a low value. The body's displacement current i_d does not flow to ground, but rather to the output circuit of A_3. This reduces the pickup as far as the ECG amplifier is concerned and effectively grounds the patient.

The value of R_4 should be as large as practical to isolate the patient from ground. The resistors R_3 and R_4 may be selected by these equations:

$$R_3 = (R_1/2)\,(V_o/V_{CM}) \text{ and } R_4 = (V_{CM} - V_o)/i_d$$

$$(-10V \leq V_o \leq +10V \text{ and } -10V \leq V_{CM} \leq +10V)$$

where V_o is the output voltage of A_3 and V_{CM} is the common-mode voltage between the inputs L_A and R_A and the input common at pin 3 of the 3656.

This circuit has the added benefit of having higher common-mode rejection than the circuit in Figure 6 (approximately 10dB improvement).

BIPOLAR CURRENT OUTPUT

The three-port capability of the 3656 can be used to implement a current output isolation amplifier function, usually difficult to implement when grounded loads are involved. The circuit is shown in Figure 8 and the following equations apply:

$$G = I_{OUT}/V_{IN} = 1 + \frac{R_F}{R_A} \times \frac{R_2}{(R_1 + R_2) \cdot R_S}$$

$$I_{OUT} \leq \pm 2.5mA$$

$$V_L \leq \pm 4V \text{ (compliance)}$$

$$R_L \leq 1.6k\Omega$$

$$R_F + R_A = R_1 + R_2 \leq 2M\Omega$$

CURRENT OUTPUT - LARGER UNIPOLAR CURRENTS

A more practical version of the current output function is shown in Figure 9. If the circuit is powered from a source greater than 15V as shown,a three-terminal regulator should be used to provide 15V for the pulse generator (pins 19 and 20). The input stage is configured as a unity gain buffer, although other configurations such as current input could be used. The circuit uses the isolation feature between the output stage and the primary power supply to generate the output current configuration that can work into a grounded load. Note that the output transistors can only drive positive current into the load. Bipolar current output would require a second transistor and dual supply.

ISOLATED 4mA TO 20mA OUTPUT

Figure 10 shows the circuit of an expanded version of the isolated current output function. It allows any input voltage range to generate the 4mA to 20mA output excursion and is also capable of zero suppression. The "span" (gain) is adjusted by R_2 and the "zero" (4mA output for minimum input) is set by the 200kΩ pot in the output stage. A three-terminal 5V reference is used to provide a stable 4mA operating point. The reference is

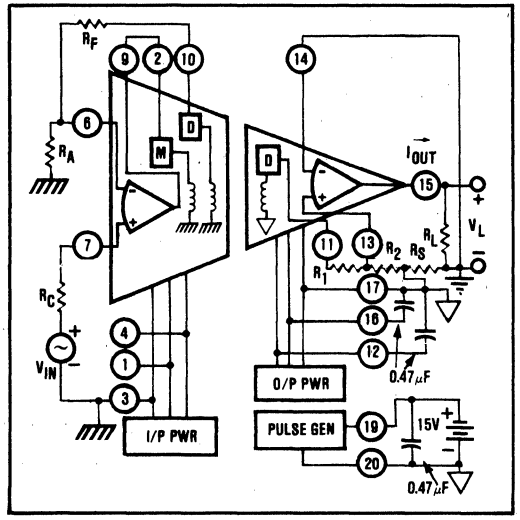


FIGURE 8. Bipolar Current Output.

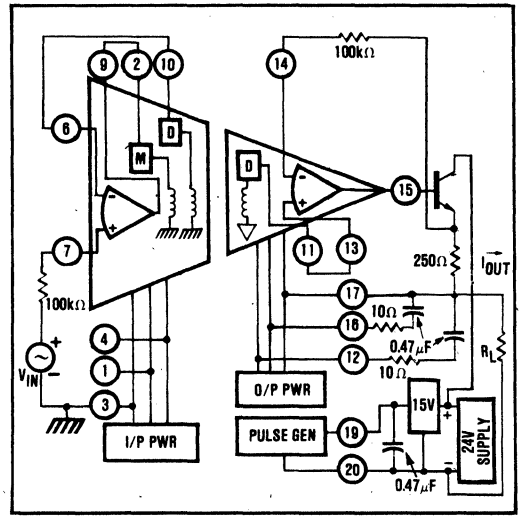


FIGURE 9. Isolated 1 to $5V_{IN}/4$ to 20mA I_{OUT}.

connected to insert an adjustable bias between the demodulator output and the noninverting input of the output stage.

DIFFERENTIAL INPUT

Figure 11 shows the proper connections for differential input configuration. The 3656 is capable of operating in this input configuration only for floating loads (i.e., the source V_{IN} has no connection to the ground reference established at pin 3). For this configuration the usual 2MΩ resistor used in the input stage is split into two halves, R_F and R_{F-}. The demodulator load (seen by pin 10 with respect to pin 3) is still 2MΩ for the floating load as shown. Notice pin 19 is common in Figure 11 whereas pin 20 is common in previous figures.

SERIES STRING SOURCE

Figure 12 shows a situation where a small voltage, which is part of a series string of other voltages, must be measured. The basic problem is that the small voltage to be measured is 500V above the system ground (i.e., a system common-mode voltage of 500V exists). The circuit converts this system CMV to an amplifier isolation mode voltage. Thus, the isolation voltage ratings and isolation-mode rejection specifications apply.

IMPROVED INPUT CHARACTERISTICS

In situations where it is desired to have better DC input amplifier characteristics than the 3656 normally provides it is possible to add a precision operational amplifier as shown in Figure 13. Here the instrumentation grade Burr-Brown 3510 is supplied from the isolated power of the input stage. The 3656 is configured as a unity-gain buffer. The gain of the 3510 stage must be chosen to limit its full scale output voltage to 5V and avoid overdriving the 3656's demodulators. Since the 3656 draws a

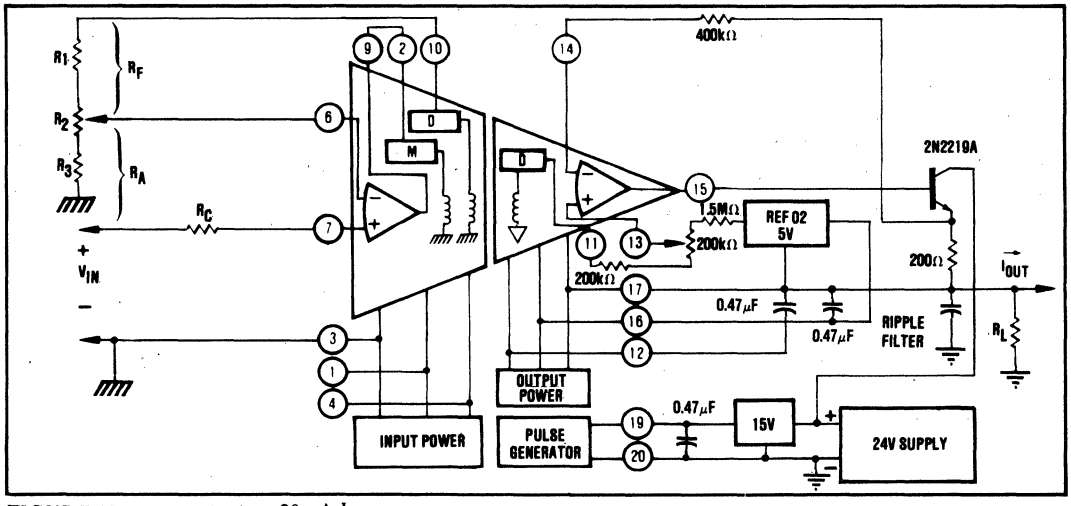


FIGURE 10. Isolated 4mA to 20mA I_{OUT}.

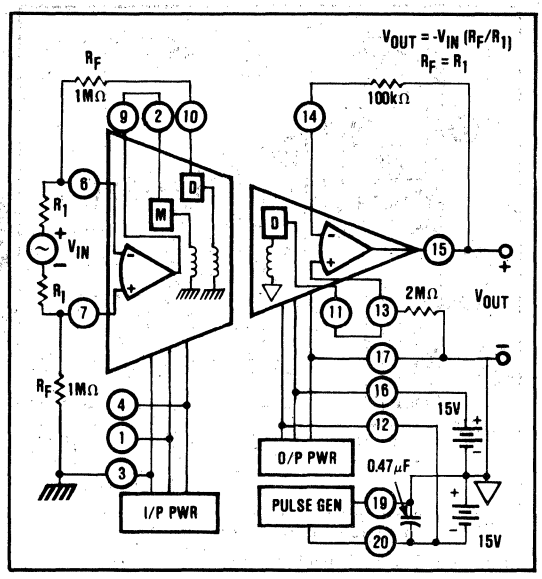


FIGURE 11. Differential Input, Floating Source.

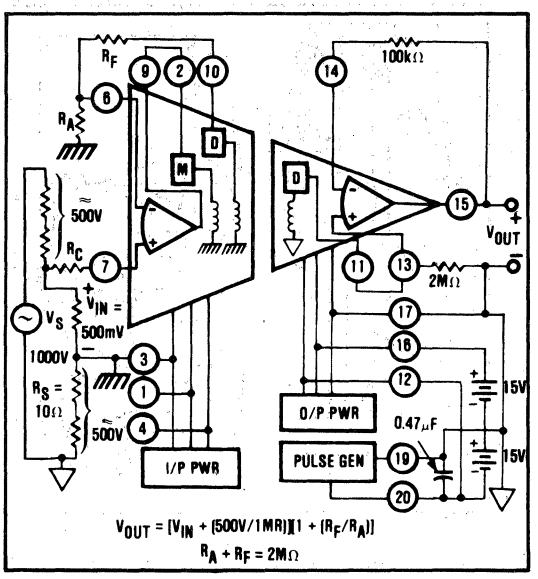


FIGURE 12. Series Source.

significant amount of supply current, extra filtering for the input supply is required as shown (2 x 0.47μF).

ELECTROMAGNETIC RADIATION

The transformer coupling used in the 3656 for isolation makes the 3656 a source of electromagnetic radiation unless it is properly shielded. Physical separation between the 3656 and sensitive components may not give sufficient attenuation by itself. In these applications the use of an electromagnetic shield is a must. A shield, Burr-Brown 100MS, is specially designed for use with the 3656 package. Note that the offset voltage appearing at pin 15 may change by 4mV to 12mV with use of the shield; however, this can be trimmed (see Offset Trimming section).

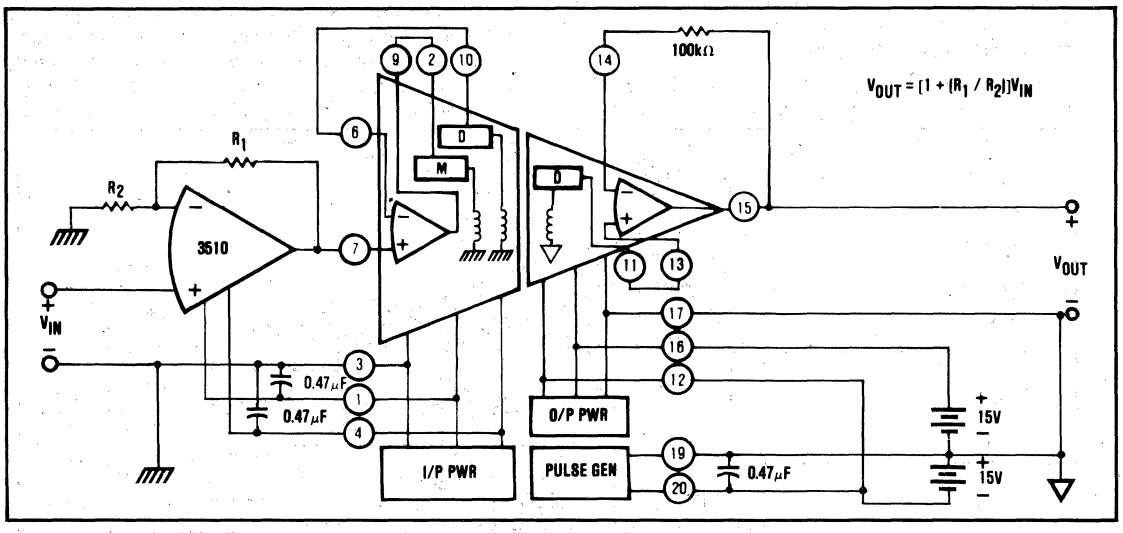
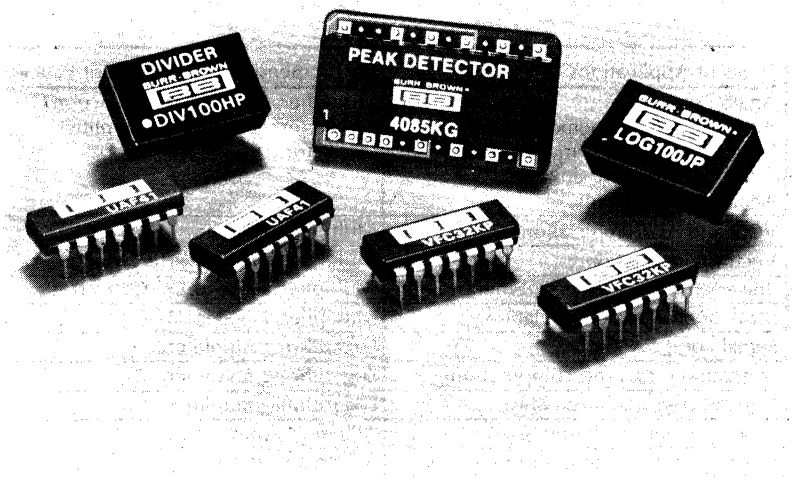


FIGURE 13. Isolator for Low-Level Signals.

ANALOG CIRCUIT FUNCTIONS



Analog circuits act as building blocks with which to perform a variety of instrumentation, computation, and control functions. They provide a broad range of versatile, proven, and ready to use computational function circuits for the designer to use in developing simple or complex systems. The analog circuit functions include multiplers, dividers, multifunction converters, true rms-to-DC converters, logarithmic amplifiers, voltage and window comparators, peak detectors, precision oscillators, and filters. The multifunction converter also provide multiply, divide, square root, exponentiate, roots, sine, cosine, arctangent, vector magnitude RMS-to-DC and logarithmic amplifier functions.

The availability of these relatively complex functions as precise, versatile, easy-to-use, low-cost building blocks has broadened the scope of practical analog circuit systems and greatly simplified analog circuit designs. The names of most analog circuit functions are self-explanatory and describe the main functions they perform.

The functions are used mostly for processing (handing) and/or conditioning of analog signals, and usually (though not always) for simulation of algebraic and/or trigonometrically expressed analog computations. The variety of applications these functions are effectively used for, are limited only by the designer's creative imagination. Some of the interesting applications where analog circuit functions have found wide acceptance are listed in the table on the following page.

Types of Applications	Recommended Analog Circuit Function
Analog simulation. Algebraic and trigonometric computations. Power series approximation, function fitting and linearizing Analog wave shaping.	Multiplier, Divider, Multifunction Converter, Logarithmic Amplifier, Oscillator.
VCO and AGC applications.	Multiplier, Divider.
Vector computation.	Multifunction Converter, Multiplier.
Power and energy measurements.	Multiplier, RMS-to-DC Converter.
Moduation and demodulation.	Multiplier, Divider.
Signal compression.	Logarithmic Amplifier.
Log-antilog-log ratio computations.	Logarithmic Amplifier.
Light-related measurements.	Logarithmic Amplifier.
Analog signal conditioning.	All circuit functions.
Instrumentation and control systems.	All circuit functions.
Variety of test equipment.	All circuit functions.
Transducer excitation	Oscillator.
Signal reference.	Oscillator.
Alarm circuits.	Voltage and Window Comparators.
Bang-bang control applications.	Voltage and Window Comparators.
Control of limit stops.	Voltage and Window Comparators.
Analog memory and peak detection.	Peak Detection.

SELECTION GUIDE

MULTIPLIERS/DIVIDERS

You can select accuracy from 0.25% to 2% max from this complete line of integrated circuit multipliers. Most provide full four-quadrant multiplication. All are laser-trimmed for accuracy—no trim pots are needed to meet specified performance. These compact models bring the cost of high performance down to acceptable levels.

MULTIPLIERS/DIVIDERS									
Model[1]	Transfer Function	Error max at 25°C %, max	Temperature Coefficient %/°C	Feed-through mV	Offset Voltage mV	1% Band-width kHz	Temp Range [2]	Package	Page
4203J	XY/10	2	0.04	50	20	40	Com	TO-100	4-89
4203K	*	1	0.04	50	20	40	Com	TO-100	4-89
4203S, (Q)	*	1	0.04	50	20	40	MIL	TO-100	4-89
4204J	XY/10	0.5	0.01	10	15	32	Ind	DIP	4-91
4204K	*	0.5	0.01	5	5	33	Ind	DIP	4-91
4204S, (Q)	*	0.25	0.02	5	5	33	MIL	DIP	4-91
4205J	$(X_1 - X_2)(Y_1 - Y_2)/10$	2	0.04	50	20	40	Com	TO-100	4-89
4205K	*	1	0.04	50	20	40	Com	TO-100	4-89
4205S, (Q)	*	1	0.04	50	20	40	MIL	TO-100	4-89
4206J	XY/10	0.5	0.01	10	15	33	Com	DIP	4-97
4206K	*	0.25	0.01	5	5	33	Com	DIP	4-97
4213AM, (Q)	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z$	1	0.008	30	10	70	Ind	TO-100	4-103
4213BM	*	0.5	0.008	30	7	70	Ind	TO-100	4-103
4213SM	*	0.5	0.008	30	7	70	MIL	TO-100	4-103
4213/MIL Series			See Military Products						
MPY100A	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$	±2	0.017	100	50	70	Ind	TO-100	4-22
MPY100B	*	±1	0.008	30	10	70	Ind	TO-100	4-22
MPY100C	*	±0.5	0.008	30	7	70	Ind	TO-100	4-22
MPY100S	*	±0.5	0.025	30	7	70	MIL	TO-100	4-22
4214AP	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z$	1	0.02	30	10	70	Ind	DIP	4-110
4214BP	*	0.5	0.02	30	7	70	Ind	DIP	4-110
4214RM	*	1	0.02	30	10	70	Ind	DIP	4-110
4214SM	*	0.5	0.02	30	7	70	Ind	DIP	4-110

*Same as model above.

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0°C to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

SPECIAL FUNCTIONS

This group of models offers many different functions that are the quick, easy way to solve a wide variety of analog computational problems. Most are in integrated circuit packages and are laser-trimmed for excellent accuracy.

SPECIAL FUNCTIONS						
Function	Model	Description	Comments	Temp Range [1]	Package	Page
Multifunction Converter	4301 4302	$Y(Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	4301 is hermetically sealed and shielded in a metal package. 4302 is in a plastic package. Both units are pin-for-pin compatible.	Ind Ind	DIP DIP	4-114 4-116
	LOG100JP	K Log (I_1/I_2)	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.	Com	DIP	4-114
Logarithmic Amplifier	4127JG 4127KP	K Log (I_1/I_{REF})	A more versatile part which contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com Com	DIP DIP	4-82 4-82
$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)dt}$	4340	True rms-to-DC conversion based on a log-antilog computational approach.	Laser-trimmed, requires no external trimming for rated accuracy. Hermetically sealed in a metal package.	Ind	DIP	4-122

SPECIAL FUNCTIONS						
Function	Model	Description	Comments	Temp Range (1)	Package	Page
$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)dt}$	4341	True rms-to-DC conversion based on a log-antilog computational approach.	Some external trimming required. Lower cost in plastic package. Pin compatible with 4340.	Ind	DIP	4-126
Peak Detector	4085BM 4085KG 4085SM	These are analog memory circuits which hold and provide read-out of a DC voltage equal to peak value of a complex input waveform.	Digital mode control provides reset capability and allows selection of peaks within a desired time interval. May be used to make peak-to-peak detector.	Com Ind MIL	DIP DIP DIP	4-74 4-74 4-74
Window Comparator	4115/04	Provides a window or dual limit for comparison. Unit has 3 inputs: one for a voltage that sets upper limit, one for a voltage that sets lower limit, and one for a signal input.	The 3 outputs are capable of sinking up to 200mA of current, indicating if the input voltage is above, below, or in the window.	Com	Module	4-80

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

DIVIDERS

The use of a special log/antilog committed divider design overcomes the major problem encountered when trying to use a multiplier in a divider circuit. Outstanding accuracy is maintained even at very low denominator voltages.

DIVIDERS									
Model	Transfer Function	Input Range	Accuracy, max D = 250mV %	Temperature Coefficient %/°C	0.5% Bandwidth kHz	Rated Output, min	Temp Range(1)	Package	Page
DIV100HP	N/D 10	250mV	1.0	0.2	15	±10V, ±5mA	Ind	DIP	4-6
DIV100JP	N/D 10	to	0.5	0.2	15	±10V, ±5mA	Ind	DIP	4-6
DIV100KP	N/D 10	10V	0.25	0.2	15	±10V, ±5mA	Ind	DIP	4-6

NOTES: (1) Ind = −25°C to +85°C.

FREQUENCY PRODUCTS

This group of products consists of precision oscillators and active filters for both signal generation and attenuation. Both fixed frequency and user selected frequency units are available.

FREQUENCY PRODUCTS						
Function	Model	Description	Comments	Temp Range(1)	Package	Page
Oscillator	4023/25	Fixed-frequency (customer-specified, 10Hz to 20kHz) provides a low distortion, stable amplitude sine wave output.	Frequency stability vs temperature: 0.04%/°C max. Amplitude stability vs temperature: 0.02%/°C max.	Ind	Module	4-72
	4423	Very-low cost in plastic package. Provides resistor programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP	4-130
Universal Active Filter	UAF41 UAF31 UAF21 UAF21H UAF11 UAF11H	These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass and bandpass outputs are available.	Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.	Ind Ind Ind Ind Ind Ind	DIP DIP DIP DIP DIP DIP	4-60 4-52 4-44 4-44 4-44 4-44

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C.

VOLTAGE REFERENCE

This product is a precision voltage reference which provides a +10V output. The output can be adjusted with minimal effect on drift or stability.

VOLTAGE REFERENCE								
				Power Supply				
Model	Output (V)	Minimum Output (mA)	Maximum Drift (ppm/°C)	(V)	(mA)	Temp Range(1)	Package	Page
REF10JM	+10.000 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	4-30
REF10KM	+10.000 ±0.005	10	2	+13.5/35	4.5	Com	TO-99	4-30
REF10RM	+10.000 ±0.005	10	3	+13.5/35	4.5	MIL	TO-99	4-30
REF10SM	+10.000 ±0.005	10	6	+13.5/35	4.5	MIL	TO-99	4-30
REF101JM	+10.000 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	4-36
REF101KM	+10.000 ±0.005	10	2	+13.5/35	4.5	Com	TO-99	4-36
REF101RM	+10.000 ±0.005	10	3	+13.5/35	4.5	MIL	TO-99	4-36
REF101SM	+10.000 ±0.005	10	6	+13.5/35	4.5	MIL	TO-99	4-36

NOTES: (1) Com = 0 to +70°C; MIL = −55°C to +125°C.

GLOSSARY OF TERMS & DEFINITIONS
Analog Circuit Functions

ABSOLUTE-VALUE CIRCUIT
A circuit that produces a unipolar output signal equal to the magnitude or absolute value of a bipolar input signal.

ACCURACY
The deviation from the ideal output voltage defined as a percent of full scale output voltage.

COMPARATOR
A device with two stable output states which signal if an input current or voltage has crossed a threshold. The threshold may be set by one or more other currents or voltages, either fixed or variable.

CREST FACTOR
The ratio of the peak value of a time-varying signal to its rms value.

CURRENT LIMITING
Limiting the output current supplied by a circuit for protection purposes.

FEEDBACK
The return of a portion of the output signal from a device to the input of the device.

FEEDTHROUGH
The input offset parameter applicable to multipliers. It is the output voltage when voltage is applied to one input of the multiplier and the other input is at zero.

FULL POWER FREQUENCY RESPONSE
The maximum frequency at which the output will swing full scale peak-to-peak voltage into a rated load without significant distortion of the output.

HYSTERESIS
The transfer response lag of comparators controlled by positive feedback and resulting in different trip points for the two directions of output transition.

LOGARITHMIC AMPLIFIER
An amplifier which develops an output voltage that is proportional to the logarithm of the input signal.

OUTPUT OFFSET
The output voltage when the inputs are grounded.

RMS
The root-mean-square value of a time-varying signal E(t) over a time period of T is

$$E_{rms} = \sqrt{1/T \int_0^T [E(t)]^2 \, dt}$$

RMS CONVERTER
A circuit that develops a DC output voltage equal in rms value to an input signal of arbitrary waveform.

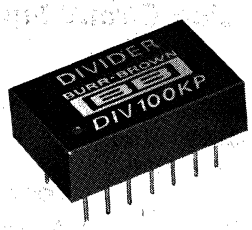
SETTLING TIME
The time required for the output to respond to a step input and to settle within some specified error band around the output final value.

SLEW RATE
The maximum rate of change of an output voltage when supplying the rated output.

SMALL SCALE FREQUENCY RESPONSE
The -3dB output frequency for a small AC signal (normally 1V, p-p) input. For multipliers, one input may be held at +10VDC or -10VDC and the other input held at small AC signal.

WINDOW COMPARATOR
A compartor that detects levels within a set range or window rather than simply distinguishing between levels above and below a set point.

BURR-BROWN®



DIV100

ANALOG DIVIDER

FEATURES

- HIGH ACCURACY
  0.25% maximum error, 40:1 denominator range
- TWO-QUADRANT OPERATION
  Dedicated log-antilog technique
- EASY TO USE
  Laser-trimmed to specified accuracy - no external resistors needed
- LOW COST
- DIP PACKAGE

APPLICATIONS

- DIVISION
- SQUARE ROOT
- RATIOMETRIC MEASUREMENT
- PERCENTAGE COMPUTATION
- TRANSDUCER AND BRIDGE LINEARIZATION
- AUTOMATIC LEVEL - AND GAIN - CONTROL
- VOLTAGE CONTROLLED AMPLIFIERS
- ANALOG SIMULATION

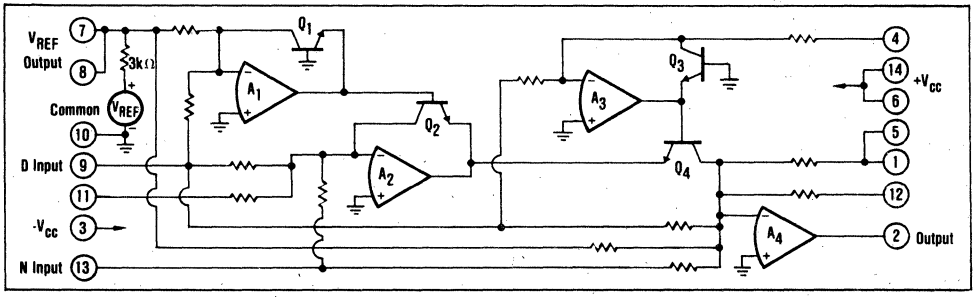
DESCRIPTION

The DIV100 is a precision two-quadrant analog divider offering superior performance over a wide range of denominator input. Its accuracy is nearly two orders of magnitude better than multipliers used for division. It consists of four operational amplifiers and logging transistors integrated into a single monolithic circuit and a laser-trimmed, thin-film resistor network. The electrical characteristics of these devices offer the user guaranteed accuracy without the need for external adjustment - the DIV100 is a complete, single package analog divider.

For those applications requiring higher accuracy than the DIV100 specifies the capability for optional adjustment is provided. These adjustments allow the user to set scale factor, feedthrough, and output-referred offsets for the lowest total divider error.

The DIV100 also gives the user a precision, temperature-compensated reference voltage for external use.

Designers of industrial process control systems, analytical instruments, or biomedical instrumentation will find the DIV100 easy to use and also a low cost, but highly accurate solution to their analog divider applications.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL		DIV100HP			DIV100JP			DIV100KP			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSFER FUNCTION			V_O = 10N/D			*			*		
ACCURACY	$R_L \geq 10k\Omega$										
Total Error											
Initial	$0.25V \leq D \leq 10V$, $N \leq \lvert D \rvert$		0.7	1.0		0.3	0.5		0.2	0.25	% FSO(1)
vs. Temperature	$1V \leq D \leq 10V$, $N \leq \lvert D \rvert$		0.02	0.05(2)		*	*		*	*	% FSO/°C
	$0.25V \leq D \leq 1V$, $N \leq \lvert D \rvert$		0.06	0.2(2)		*	*		*	*	% FSO/°C
vs. Supply	$0.25V \leq D \leq 10V$, $N \leq \lvert D \rvert$		0.15			*			*		% FSO/%
Warm-up time to rated performance			5			*			*		Minutes
AC PERFORMANCE	D = +10V										
Small-Signal Bandwidth	-3dB		350			*			*		kHz
0.5% Amplitude Error	Small-Signal		15			*			*		kHz
0.57° Vector Error	Small-Signal		1000			*			*		Hz
Full-Power Bandwidth	$V_O = \pm 10V$, $I_O = \pm 5mA$		30			*			*		kHz
Slew Rate	$V_D = \pm 10V$, $I_O = \pm 5mA$		2			*			*		V/µsec
Settling Time	ϵ = 1%, ΔV_O = 20V		15			*			*		µsec
Overload Recovery	50% Output Overload		4			*			*		µsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Numerator	$N \leq \lvert D \rvert$	±10			*			*			V
Denominator	$D \geq +250mV$	+10			*			*			V
Input Resistance	Either Input		25			*			*		kΩ
OUTPUT CHARACTERISTICS											
Full-Scale Output (FSO)		±10			*			*			V
Rated Output											
Voltage	$I_O = \pm 5mA$	±10			*			*			V
Current	$V_O = \pm 10V$	±5			*			*			mA
Current Limit											
Positive			15	20(2)		*			*		mA
Negative			19	23(2)		*			*		mA
OUTPUT NOISE VOLTAGE	N = 0V										
f_B = 10Hz to 10kHz											
D = +10V			370			*			*		µV, rms
D = +250mV			1			*			*		mV, rms
REFERENCE VOLTAGE CHARACTERISTICS	$R_L \geq 10M\Omega$										
Output Voltage											
Initial	At +25°C	6.3(2)	6.6	6.9(2)	*	*	*	*	*	*	V
vs. Supply			±25			*			*		µV/V
Temperature Coefficient			±50			*			*		ppm/°C
Output Resistance			3			*			*		kΩ
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*			*		VDC
Operating Range	Derated Performance	±12		±20	*		*	*		*	VDC
Quiescent Current											
Positive Supply			5	7(2)		*	*		*	*	mA
Negative Supply			8	10(2)		*	*		*	*	mA
AMBIENT TEMPERATURE RANGE											
Specification		0		+70	*		*	*		*	°C
Operating Range	Derated Performance	-25		+85	*		*	*		*	°C
Storage		−40		+85	*		*	*		*	°C

*Same as DIV100H.

ABSOLUTE MAXIMUM RATINGS

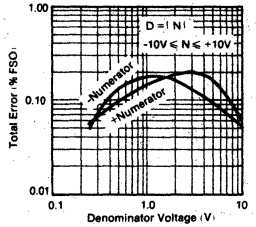
Supply	±20VDC
Internal Power Dissipation(3)	600mW
Input Voltage Range(4)	±20VDC
Storage Temperature Range	-55°C to +125°C
Operating Temperature Range	-25°C to +85°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration(3)(5)	Continuous
Junction Temperature	175°C

NOTES:
1. FSO is the abbreviation for Full Scale Output.
2. This parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
3. See General Information section for discussion.
4. For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage.
5. Short-circuit may be to ground only. Rating applies to an ambient temperature of +38°C at rated supply voltage.

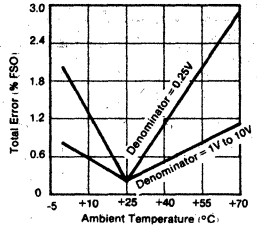
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.)

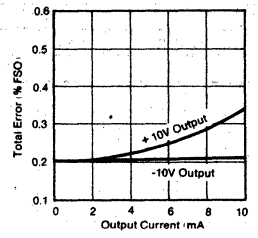
TOTAL ERROR VS DENOMINATOR VOLTAGE



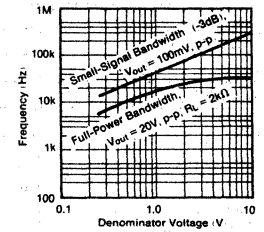
TOTAL ERROR VS AMBIENT TEMPERATURE



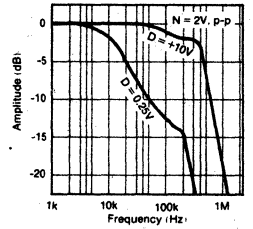
TOTAL ERROR VS OUTPUT CURRENT



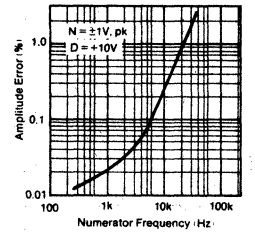
FREQUENCY RESPONSE VS DENOMINATOR VOLTAGE



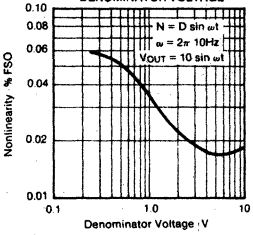
SMALL-SIGNAL FREQUENCY RESPONSE



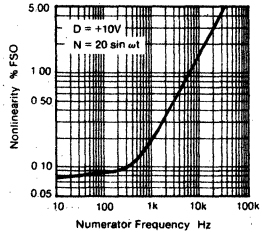
AMPLITUDE ERROR VS NUMERATOR FREQUENCY



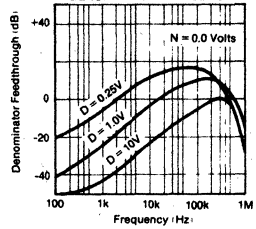
NONLINEARITY VS DENOMINATOR VOLTAGE



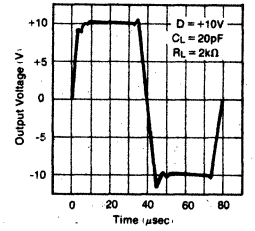
NONLINEARITY VS NUMERATOR FREQUENCY



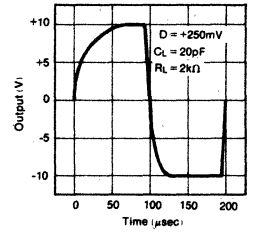
DENOMINATOR FEEDTHROUGH VS DENOMINATOR FREQUENCY



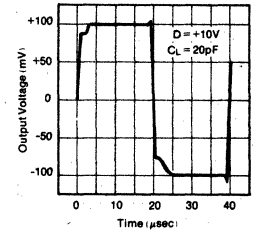
LARGE SIGNAL STEP RESPONSE



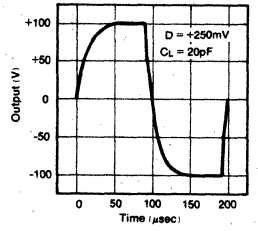
LARGE SIGNAL STEP RESPONSE



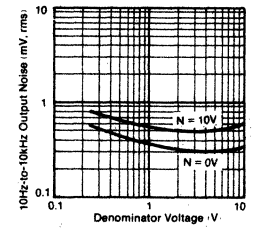
TRANSIENT RESPONSE



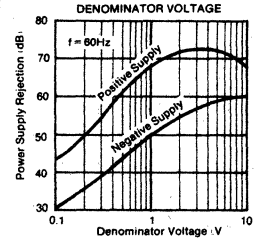
TRANSIENT RESPONSE



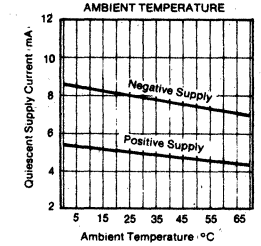
OUTPUT NOISE VS DENOMINATOR VOLTAGE



POWER SUPPLY REJECTION VS DENOMINATOR VOLTAGE

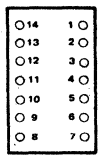


QUIESCENT CURRENT VS AMBIENT TEMPERATURE



PIN CONFIGURATION

1. Gain Error Adjust
2. Output
3. -Vcc
4. D Input Offset Adjust
5. Internally Connected to Pin 1
6. Internally Connected to Pin 14
7. Internally Connected to Pin 8
8. Reference Voltage
9. Denominator (D) Input
10. Common
11. N Input Offset Adjust
12. Output Offset Adjust
13. Numerator (N) Input
14. +Vcc



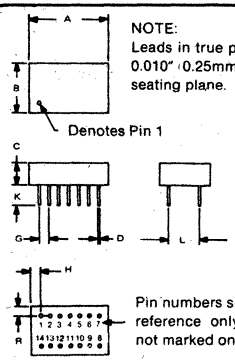
(Bottom View)

MECHANICAL

ORDER NUMBER: DIV100HP, DIV100JP, DIV100KP

CASE: Epoxy
WEIGHT: 2.7 Grams
CONNECTOR: 0145MC

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Denotes Pin 1

Pin numbers shown for reference only. Numbers are not marked on package.

DEFINITIONS

TRANSFER FUNCTION

The ideal transfer function for the DIV100 is:

$V_{out} = 10\ N/D$

where: N = Numerator input voltage
D = Denominator input voltage
10 = Internal scale factor

Figure 1 shows the operating region over the specified numerator and denominator ranges. Note that below the minimum denominator voltage (250mV) operation is undefined.

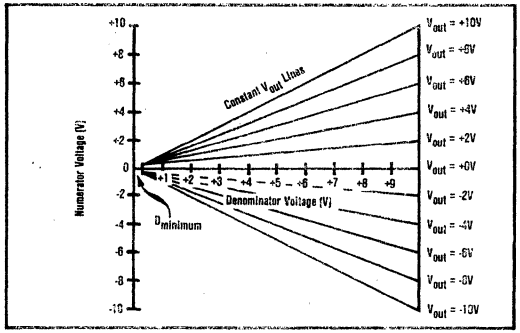


FIGURE 1. Operating Region.

ACCURACY

Accuracy is specified as a percentage of full-scale output (FSO). It is derived from the total error specification.

TOTAL ERROR

Total error is the deviation of the actual output from the ideal quotient 10N/D expressed in percent of FSO(10V); e.g., for the DIV100K:

$V_{out\ (actual)} = V_{out\ (ideal)} \pm$ total error,

where: Total error = 0.25% FSO = 25mV.

It represents the sum of all error terms normally associated with a divider: numerator nonlinearity, denominator nonlinearity, scale-factor error, output-referred numerator and denominator offsets, and the offset due to the output amplifier. Individual errors are not specified because it is their sum that affects the user's application.

SMALL-SIGNAL BANDWIDTH

Small-signal bandwidth is the frequency the output drops to 70% (-3dB) of its DC value. The input signal must be low enough in amplitude to keep the divider's output from becoming slew-rate limited. A rule-of-thumb is to make the output voltage 100mV, p-p, when testing this parameter. Small-signal bandwidth is directly proportional to denominator magnitude as described in the Typical Performance Curves.

0.5% AMPLITUDE ERROR

At high frequencies the input-to-output relationship is a complex function that produces both a magnitude and vector error. The 0.5% amplitude error is the frequency at which the magnitude of the output drops 0.5% from its DC value.

0.57° VECTOR ERROR

The 0.57° vector error is the frequency at which a phase error of 0.01 radians occurs. This is the most sensitive measure of dynamic error of a divider.

LINEARITY

Defining linearity for a nonlinear device may seem unnecessary; however, by keeping one input constant the output becomes a linear function of the remaining input. The denominator is the input that is held fixed with a divider. Nonlinearities in a divider add harmonic distortion to the output in the amount of:

$$\text{Percent Distortion} \approx \frac{\text{Percent Nonlinearity}}{\sqrt{2}}$$

FEEDTHROUGH

Feedthrough is the signal at the output for any value of denominator within its rated range, when the numerator input is zero. Ideally the output should be zero under this condition.

GENERAL INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the DIV100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 1000pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the DIV100's output.

OVERLOAD PROTECTION

The DIV100 can be protected against accidental power supply reversal by putting a diode (1N4001, type) in series with each power supply line as shown in Figure 2. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off.

If this protection circuit is used, the accuracy of the DIV100 will be degraded by the power supply sensitivity specification. No other overload protection circuit is necessary. Inputs are internally protected against overvoltages and they are current-limited by at least a 10kΩ series resistor. The output is protected against short circuits to power supply common only.

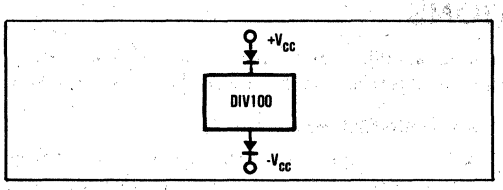


FIGURE 2. Overload Protection Circuit.

STATIC SENSITIVITY

No special handling is required. The DIV100 does not use MOS-type transistors. Furthermore, all external leads are protected by resistors against low energy electrostatic discharge (ESD).

INTERNAL POWER DISSIPATION

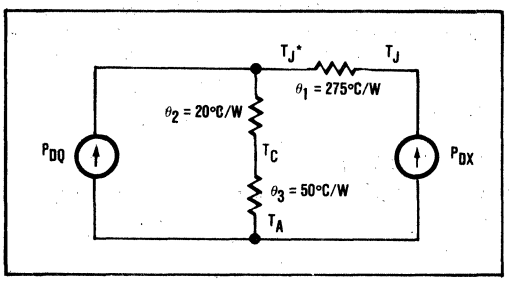


FIGURE 3. DIV100 Thermal Model.

Figure 3 is the thermal model for the DIV100 where:

P_{DQ} = Quiescent Power Dissipation
$= |+V_{CC}| I_{+QUIESCENT} + |-V_{CC}| I_{-QUIESCENT}$

P_{DX} = Worst case power dissipation in the output transistor
$= V_{CC}^2 / 4R_{LOAD}$ (for normal operation)
$= V_{CC} I_{(output\ limit)}$ (for short-circuit)

T_J = Junction Temperature (output loaded)
T_J* = Junction Temperature (no load)
T_C = Case Temperature
T_A = Ambient Temperature
θ = Thermal Resistance

This model is obviously not the simple one power source model that most linear device manufacturers give. It is, however, a more accurate model for a multidevice monolithic or hybrid integrated circuit.

The model in Figure 3 must be used in conjunction with the DIV100's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem:

Determine the highest ambient temperature at which the DIV100 may be operated with a continuous short circuit to ground. $V_{CC} = \pm 15VDC$.

$P_{D(max)} = 600mW$. $T_{J(max)} = +175°C$.

$T_A = T_{J(max)} - P_{DQ}(\theta_2 + \theta_3) - P_{DX(short=circuit)}(\theta_1+\theta_2+\theta_3)$
$= 175°C - 18°C - 119°C = 38°C$

$P_{D(actual)} = P_{DQ} + P_{DX(short=circuit)} \leq P_{D(max)}$
$= 255mW + 345mW = 600mW$

The conclusion is that the device will withstand a short-circuit up to $T_A = +38°C$ without exceeding either the 175°C or 600mW absolute maximum limits.

LIMITING OUTPUT VOLTAGE SWING

The negative output voltage swing should be limited to ±11V, maximum, to prevent polarity inversion and possible system instability. This should be done by limiting the input voltage range.

THEORY OF OPERATION

The DIV100 is a log-antilog divider consisting of four operational amplifiers and four logging transistors integrated into a single monolithic circuit. Its basic principal of operation can be seen by an analysis of the circuit in Figure 4.

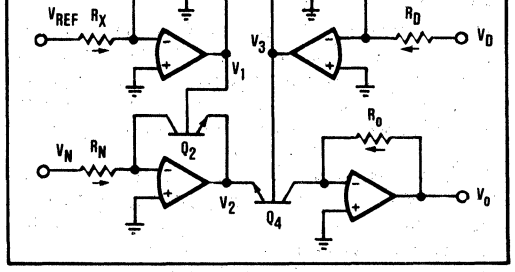


FIGURE 4. One-Quadrant Log-Antilog Divider

The logarithmic equation for a biopolar transistor is:

$$V_{BE} = V_T \ln (I_c / I_s), \quad (1)$$

where: $V_T = kT/q$
k = Boltzmann's constant = 1.381×10^{-23}
T = Absolute temperature in degrees Kelvin
q = Electron charge = 1.602×10^{-19}
I_c = Collector current
I_s = Reverse saturation current

Applying equation (1) to the four logging transistors gives:

For Q_1:
$V_{BE} = V_B - V_E = V_T[\ln(V_{REF}/R_X - \ln I_s]$

This leads to:
$V_1 = -V_T[\ln(V_{REF}/R_X - \ln I_s]$

For Q_2:
$V_1 - V_2 = V_T[\ln(V_N/R_N) - \ln I_S]$

For Q_3:
$V_3 = -V_T[\ln (V_D/R_D) - \ln I_S]$

We have now taken the logarithms of the input voltage V_{REF}, V_N, and V_D. Applying equation (1) to Q_4 gives:
$V_3 - V_2 = V_T [\ln (V_o/R_o) - \ln I_s]$.

Assume V_T and I_s are the same for all four transistors (a reasonable assumption with a monolithic IC). Solving

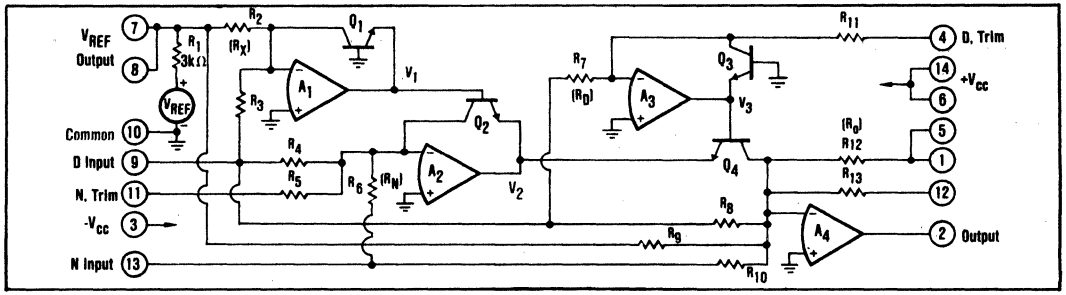


FIGURE 5. DIV100 Two-Quadrant Log-Antilog Circuit.

this last equation in terms of the previously defined variables and taking the antilogarithm of the result yields:

$$V_o = \frac{V_{REF}\, V_N\, R_o\, R_D}{V_D\, R_X\, R_N} \qquad (2)$$

In the DIV100 $V_{REF} = 6.6V$, $R_o = R_N = R_D$, and R_X is such that the transfer function is:

$$V_o = 10\ N\ D \qquad (3)$$

where: N = Numerator Voltage
D = Denominator Voltage

Figure 5 is a more detailed circuit diagram for the DIV100. In addition to the circuitry included in Figure 3, it also shows the resistors (R_3, R_4, R_8, R_9, and R_{10}) used for level-shifting. This converts the DIV100 to a two-quadrant divider.

The implementation of the transfer function is equation (3) is done using devices with real limitations. For example, the value of the D input must always be positive. If it isn't, Q_3 will no longer conduct, A_3 will become open loop, and its output and the DIV100 output will saturate. This limitation is further restricted in that if the D input is less than +250mV the errors will become substantial. It will still function, but its accuracy will be less.

Still another limitation is the value of the N input must always be equal to or less than the absolute value of the D input. From equation (3) it can be seen that if this limitation is not met V_o will try to be greater than the 10V output voltage limit of A_4.

A limitation that may not be obvious is the effect of source resistance. If the numerator or denominator inputs are driven from a source with more than 10Ω of output resistance, the resultant voltage divider will cause a significant output error. This voltage divider is formed by the source resistance and the DIV100 input resistance. With $R_{SOURCE} = 10\Omega$ and $R_{INPUT\ (DIV100)} = 25k\Omega$ an error of 0.04% results. This means that the best performance of the DIV100 is obtained by driving its inputs from operational amplifiers.

Note that the reference voltage is brought out to pins 7 and 8. This gives the user a precision, temperature-compensated reference for external use. Its open-circuit voltage is +6.6VDC, ±0.075V, typically. Its Thevenin equivalent resistance is 3kΩ. Since the output resistance is a relatively high value, an operational amplifier is necessary to buffer this source as shown in Figure 6. The external amplifier is necessary because current drawn through the 3kΩ resistor will effect the DIV100 scale factor.

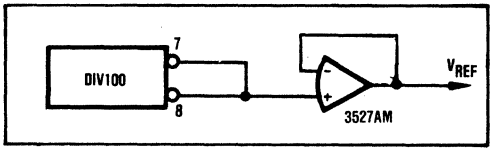


FIGURE 6. Buffered Precision Voltage Reference.

OPTIONAL ADJUSTMENTS

Figure 7 shows the connections to make to adjust the DIV100 for significantly better accuracy over its 40-to-1 denominator range.

The adjustment procedure is:

1. **Begin with R_1, R_2, and R_3 set to their mid-position.**
2. **With |N| = D = 10.000V, ±1mV, adjust R_1 for V_o = +10.000V, ±1mV. This sets the scale factor.**
3. **Set D to the minimum expected denominator voltage. With N = D, adjust R_2 for V_o = −10.000V. This adjusts the output referred offset errors.**
4. **With D still at its minimum expected value, make N = D. Adjust R_3 for V_o = 10.000V. This adjusts the output referred offset errors.**
5. **Repeat steps 2-4 until the best accuracy is obtained.**

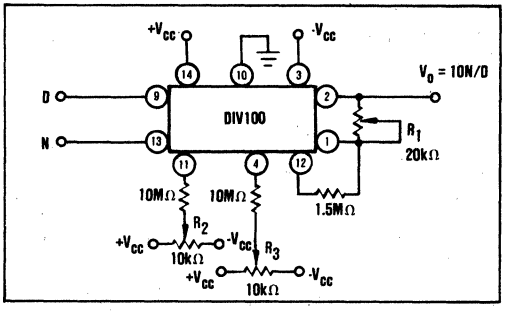


FIGURE 7. Connection Diagram for Optional Adjustments.

TYPICAL APPLICATIONS

CONNECTION DIAGRAM

Figure 8 is applicable to each application discussed in this section, except the square root mode.

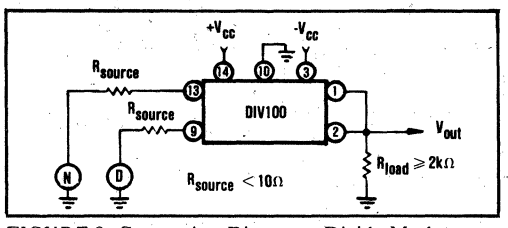


FIGURE 8. Connection Diagram - Divide Mode.

RATIOMETRIC MEASUREMENT

The DIV100 is useful for ratiometric measurements such as efficiency, elasticity, stress, strain, percent distortion, impedance magnitude, and fractional loss or gain. These ratios may be made for instantaneous, average, RMS, or peak values.

The advantage of using the DIV100 can be illustrated from the example shown in Figure 9.

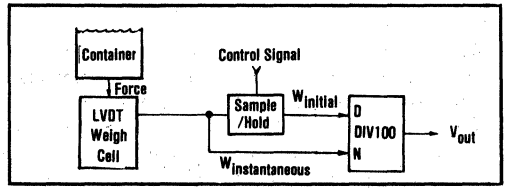


FIGURE 9. Weighing System - Fractional Loss.

The LVDT (Linear Variable Differential Transformer) weigh cell measures the force exerted on it by the weight of the material in the container. Its output is a voltage proportional to:

$$W = \frac{Fg}{a}$$

where: W = Weight of material
F = Force
g = Acceleration due to gravity
a = Acceleration (acting on body of weight W)

In a fractional loss weighing system the initial value of the material can be determined by the volume of the container and the density of the material. If this value is then held on the D-input to the DIV100 for some time interval, the DIV100 output will be a measure of the instantaneous fractional loss:

$$\text{Loss (L)} = W_{INSTANTANEOUS} / W_{INITIAL}$$

Note that by using the DIV100 in this application the common physical parameters of g and a have been eliminated from the measurement, thus eliminating the need for precise system calibration.

The output from a ratiometric measuring system may also be used as a feedback signal in an adaptive process control system. A common application in the chemical industry is in the ratio control of a gas and liquid flow as illustrated in Figure 10.

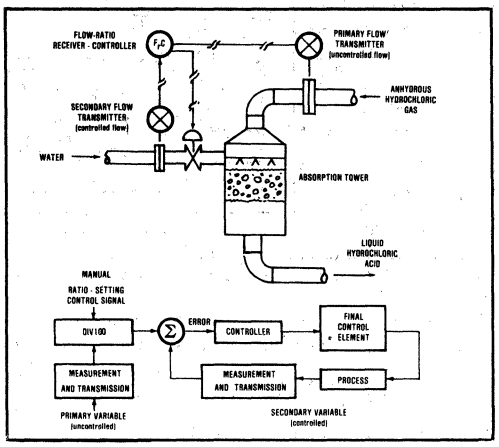


FIGURE 10. Ratio Control of Water to Hydrochloric Gas

PERCENTAGE COMPUTATION

A variation of the direct ratiometric measurements previously discussed is the need for percentage computation. In Figure 11 the DIV100 output varies as the percent deviation of the measured variable to the standard.

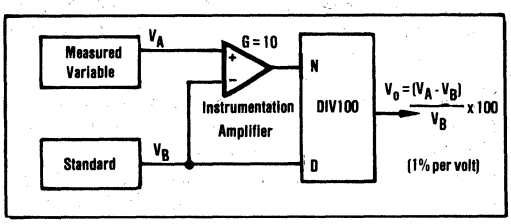


FIGURE 11. Percentage Computation.

TIME AVERAGING

The circuit in Figure 12 overcomes the fixed averaging interval and crude approximation of more conventional time averaging schemes.

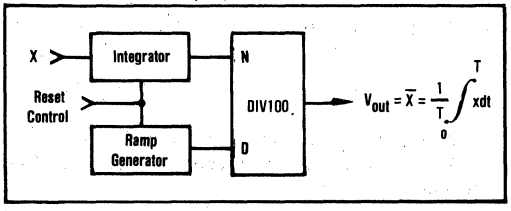


FIGURE 12. Time Averaging Computation Circuit.

BRIDGE LINEARIZATION

The bridge circuit in Figure 13 is fundamental to pressure, force, strain and electrical measurements. It can have one or more active arms whose resistance is a function of the physical quantity, property, or condition that is being measured; e.g., force of compression. For the sake of explanation the bridge in Figure 13 has only one active arm.

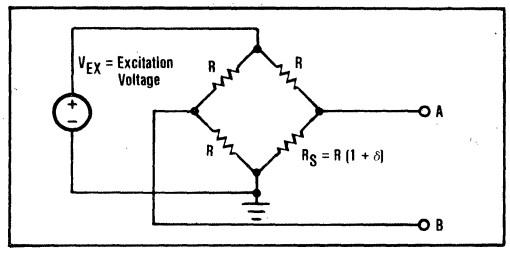


FIGURE 13. Bridge Circuit.

The differential output voltage V_{BA} is:

$$V_{BA} = V_B - V_A = \frac{-V_{EX}\delta}{2(2+\delta)},$$

a nonlinear function of the resistance change in the active arm. This nonlinearity limits the useful span of the bridge to perhaps ±10% variation in the measured parameter.

Bridge linearization is accomplished using the circuit in Figure 14. The instrumentation amplifier converts the differential output to a single-ended voltage needed to drive the divider. The voltage-divider string makes the numerator and denominator voltages:

$$N = \frac{-V_{EX}\delta R_{IN}}{(2R_1 + 3R_{in})(2+\delta)}, \text{ and,}$$

$$D = \frac{2 V_{EX} R_{ID}}{(2R_1 + 3R_{ID})(2+\delta)}, \text{ respectively,}$$

where: R_{IN} = DIV100 numerator input resistance
R_{ID} = DIV100 denominator input resistance

Applying these voltages to the DIV100 transfer function gives:

$$V_o = 10N \div D = \frac{(2R_1 + 3R_{ID})(R_{IN}\delta)\,10}{(2R_1 + 3R_{IN})(2R_{ID})},$$

which reduces to:

$V_o = -5\delta$

if the divider's input resistances are equal.

The nonlinearity of the bridge has been eliminated and the circuit output is independent of variations in the excitation voltage.

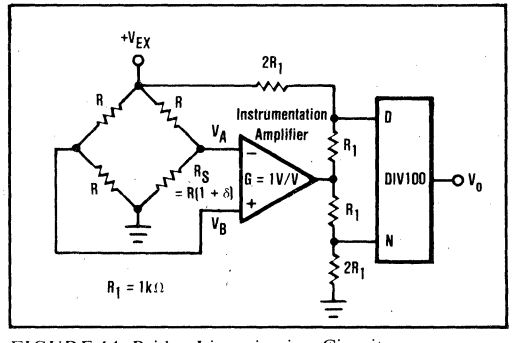


FIGURE 14. Bridge Linearization Circuit.

AUTOMATIC GAIN CONTROL

A simple AGC circuit using the DIV100 is shown in Figure 15. The numerator voltage may vary both positive and negative. The divider's output is half-wave rectified and filtered by D_1, R_3, and C_2. It is then compared to the DC reference voltage. If a difference exists the integrator sends a control signal to the denominator input to maintain a constant output, thus compensating for input voltage changes.

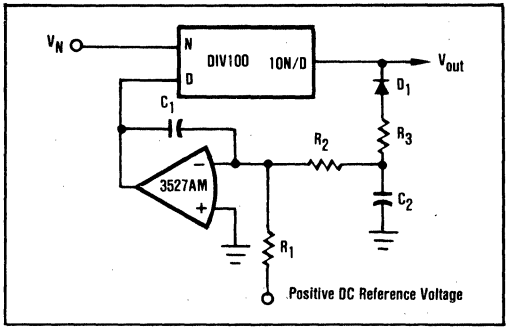


FIGURE 15. Automatic Gain Control Circuit.

VOLTAGE-CONTROLLED FILTER

Figure 16 shows how to use the DIV100 in the feedback loop of an integrator to form a voltage-controlled filter. The transfer function is:

$$\frac{V_{out(S)}}{V_{in(S)}} = \frac{K}{\tau S + 1}$$

where: $K = -R_2 / R_1$

$$\tau = \frac{10\, R_2\, C}{V_{CONTROL}}$$

This circuit may be used as a single-pole low-pass active filter whose cutoff frequency is linearily proportional to the circuit's control voltage.

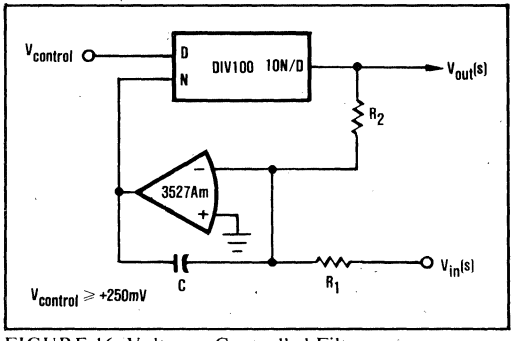


FIGURE 16. Voltage - Controlled Filter.

SQUARE ROOT

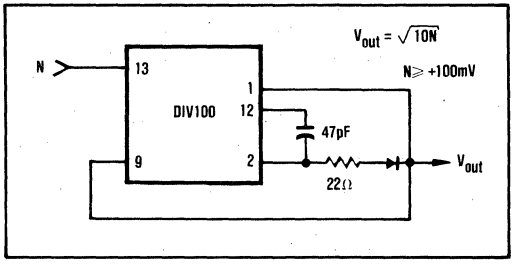


FIGURE 17. Connection Diagram for Square Root Mode.

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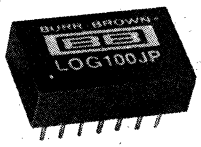


LOG100

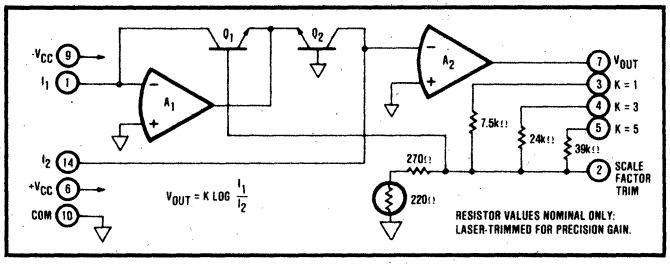
Precision LOGARITHMIC AND LOG RATIO AMPLIFIER

FEATURES

- HIGH ACCURACY
  0.37% FSO max Total Error over 5 decades
- GOOD LINEARITY
  0.1% max Log Conformity over 5 decades
- EASY TO USE
  Pin-selectable Gains
  Internal Laser-trimmed Resistors
- WIDE INPUT DYNAMIC RANGE
  6 Decades, 1nA to 1mA

APPLICATIONS

- LOG, LOG RATIO AND ANTILOG COMPUTATIONS
- ABSORBANCE MEASUREMENTS
- DATA COMPRESSION
- OPTICAL DENSITY MEASUREMENTS
- DATA LINEARIZATION
- CURRENT AND VOLTAGE INPUTS



DESCRIPTION

The LOG100 uses advanced integrated circuit technologies to achieve high accuracy, ease of use, low cost, and small size. It is the logical choice for your logarithmic-type computations. The amplifier has guaranteed maximum error specifications over the full six-decade input range (1nA to 1mA) and for all possible combinations of I_1 and I_2. Total error is guaranteed so that involved error computations are not necessary.

The circuit uses a specially designed compatible thin-film monolithic integrated circuit which contains amplifiers, logging transistors, and low drift thin-film resistors. The resistors are laser-trimmed for maximum precision. FET input transistors are used for the amplifiers whose low bias currents (1pA typical) permit signal currents as low as 1nA while maintaining guaranteed total errors of 0.37% FSO maximum.

Because scaling resistors are self-contained, scale factors of 1V, 3V or 5V per decade are obtained simply by pin selections. No other resistors are required for log ratio applications. The LOG100 will meet its guaranteed accuracy with no user trimming. Provisions are made for simple adjustments of scale factor, offset voltage, and bias current if enhanced performance is desired.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

ELECTRICAL SPECIFICATIONS

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	LOG100JP MIN	LOG100JP TYP	LOG100JP MAX	UNITS
TRANSFER FUNCTION			V_{OUT} = K Log (I_1/I_2)		
Log Conformity Error[1]	Either I_1 or I_2				
Initial	1nA to 100µA (5 decades)		0.04	0.1	%
	1nA to 1mA (6 decades)		0.15	0.25	%
Over Temperature	1nA to 100µA (5 decades)		0.002		%/°C
	1nA to 1mA (6 decades)		0.001		%/°C
K Range[2]			1, 3, 5		V/decade
Accuracy			0.3		%
Temperature Coefficient			0.03		%/°C
ACCURACY					
Total Error[3]	K = 1,[4] Current Input Operation				
Initial	I_1, I_2 = 1mA			±55	mV
	I_1, I_2 = 100µA			±30	mV
	I_1, I_2 = 10µA			±25	mV
	I_1, I_2 = 1µA			±20	mV
	I_1, I_2 = 100nA			±25	mV
	I_1, I_2 = 10nA			±30	mV
	I_1, I_2 = 1nA			±37	mV
vs Temperature	I_1, I_2 = 1mA		±0.20		mV/°C
	I_1, I_2 = 100µA		±0.37		mV/°C
	I_1, I_2 = 10µA		±0.28		mV/°C
	I_1, I_2 = 1µA		±0.033		mV/°C
	I_1, I_2 = 100nA		±0.28		mV/°C
	I_1, I_2 = 10nA		±0.51		mV/°C
	I_1, I_2 = 1nA		±1.26		mV/°C
vs Supply	I_1, I_2 = 1mA		±4.3		mV/V
	I_1, I_2 = 100µA		±1.5		mV/V
	I_1, I_2 = 10µA		±0.37		mV/V
	I_1, I_2 = 1µA		±0.11		mV/V
	I_1, I_2 = 100nA		±0.61		mV/V
	I_1, I_2 = 10nA		±0.91		mV/V
	I_1, I_2 = 1nA		±2.6		mV/V
INPUT CHARACTERISTICS (of amplifiers A_1 and A_2)					
Offset Voltage					
Initial			±0.7	±5	mV
vs Temperature			±80		µV/°C
Bias Current					
Initial			1	5[5]	pA
vs Temperature			doubles every 10°C		
Voltage Noise	10Hz to 10kHz, RTI		3		µV, rms
Current Noise	10Hz to 10kHz, RTI		0.5		pA, rms
AC PERFORMANCE					
3dB Response[6], I_2 = 10µA					
1nA	C_C = 4500pF		0.11		kHz
1µA	C_C = 150pF		38		kHz
10µA	C_C = 150pF		27		kHz
1mA	C_C = 50pF		45		kHz
Step Response[6]					
Increasing	C_C = 150pF				
1µA to 1mA			11		µsec
100nA to 1µA			7		µsec
10nA to 100nA			110		µsec
Decreasing	C_C = 150pF				
1mA to 1µA			45		µsec
1µA to 100nA			20		µsec
100nA to 10nA			550		µsec
OUTPUT CHARACTERISTICS					
Full Scale Output (FSO)		±10			V
Rated Output					
Voltage	I_{OUT} = ±5mA	±10			V
Current	V_{OUT} = ±10V	±5			mA
Current Limit					
Positive			12.5		mA
Negative			15		mA
Impedance			0.05		Ω
POWER SUPPLY REQUIREMENTS					
Rated Voltage			±15		VDC
Operating Range	Derated Performance	±12		±18	VDC
Quiescent Current			±7	±9	mA

ELECTRICAL (CONT'D)

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AMBIENT TEMPERATURE RANGE					
Specification		0		+70	°C
Operating Range	Derated Performance	−40		+85	°C
Storage		−40		+85	°C

NOTES:
1. Log Conformity Error is the peak deviation from the best-fit straight line of the V_{OUT} vs log I_{IN} curve expressed as a percent of peak-to-peak full scale output.
2. May be trimmed to other values. See Applications section.
3. The worst-case Total Error for any ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately.
4. Total Error at other values of K is K times Total Error for K = 1.
5. Guaranteed by design. Not directly measurable due to amplifier's committed configuration.
6. **3dB and transient response are a function of both the compensation capacitor and the level of input current. See Performance Curves.**

ABSOLUTE MAXIMUM RATINGS

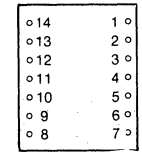
Supply	±18V
Internal Power Dissipation	600mV
Input Current	10mA
Input Voltage Range	±18V
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

SCALE FACTOR PIN CONNECTIONS

K, V/decade	Connections
5	5 to 7
3	4 to 7
1.9	4 and 5 to 7
1	3 to 7
0.85	3 and 5 to 7
0.77	3 and 4 to 7
0.68	3 and 4 and 5 to 7

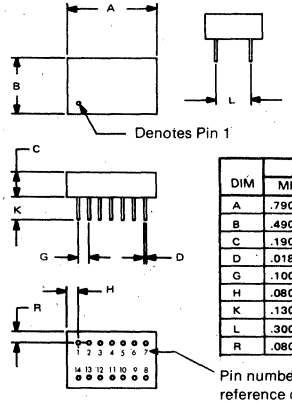
PIN CONFIGURATION

1. I_1 INPUT
2. SCALE FACTOR TRIM
3. K = 1
4. K = 3
5. K = 5
6. +V_{CC}
7. OUTPUT
8. NO INTERNAL CONNECTION
9. -V_{CC}
10. COMMON
11. NO INTERNAL CONNECTION
12. NO INTERNAL CONNECTION
13. NO INTERNAL CONNECTION
14. I_2 INPUT



(Bottom View)

MECHANICAL



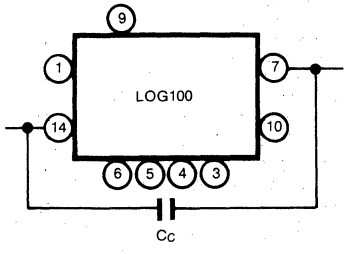
ORDER NUMBER: LOG100JP
CASE: Epoxy
WEIGHT: 2.7 grams
CONNECTOR: 0145MC

NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

Pin numbers shown for reference only. Numbers are not marked on package.

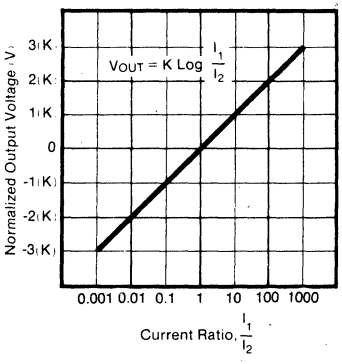
FREQUENCY COMPENSATION



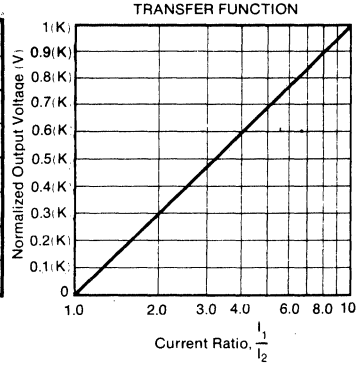
PERFORMANCE CURVES

(Typical at T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.)

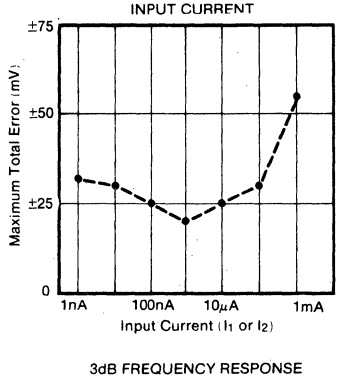
NORMALIZED TRANSFER FUNCTION



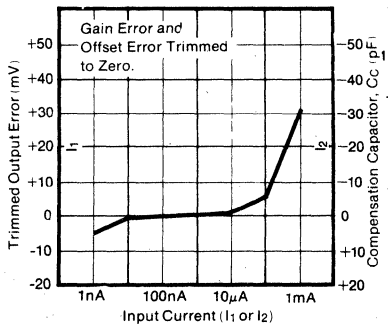
ONE CYCLE OF NORMALIZED TRANSFER FUNCTION



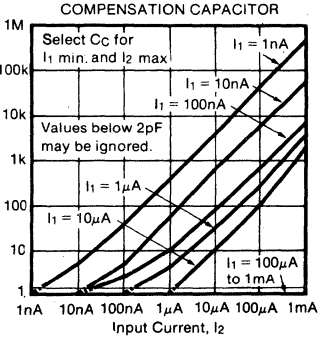
TOTAL ERROR VS INPUT CURRENT



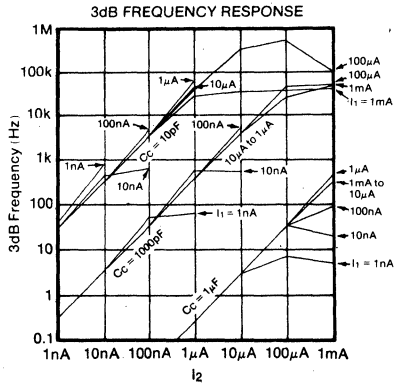
TRIMMED OUTPUT ERROR VS INPUT CURRENT



MINIMUM VALUE OF COMPENSATION CAPACITOR



3dB FREQUENCY RESPONSE



THEORY OF OPERATION

The base-emitter voltage of a bipolar transistor is

$$V_{BE} = V_T \ln \frac{I_c}{I_s} \quad \text{where:} \quad V_T = \frac{KT}{q} \tag{1}$$

K = Boltzman's constant = 1.381 x 10^{-23}

T = Absolute temperature in degrees Kelvin

q = Electron charge = 1.602 x 10^{-19} Coulombs

I_c = Collector current

I_s = Reverse saturation current

From the circuit in Figure 1, we see that

$$V_{OUT}' = V_{BE_1} - V_{BE_2} \tag{2}$$

Substituting (1) into (2) yields

$$V_{OUT}' = V_{T_1} \ln \frac{I_1}{I_{S_1}} - V_{T_2} \ln \frac{I_1}{I_{S_2}} \tag{3}$$

If the transistors are matched and isothermal and $V_{T_1} = V_{T_2}$, then (3) becomes

$$V_{OUT}' = V_T \left[\ln \frac{I_1}{I_s} - \ln \frac{I_2}{I_s} \right] \tag{4}$$

$$V_{OUT}' = V_T \ln \frac{I_1}{I_2} \quad \text{and since} \tag{5}$$

$$\ln X = 2.3 \log_{10} X \tag{6}$$

$$V_{OUT}' = n\, V_T \log \frac{I_1}{I_2} \tag{7}$$

where $n = 2.3$ (8)

also

$$V_{OUT} = V_{OUT}' \frac{R_1 + R_2}{R_1} \tag{9}$$

$$= \frac{R_1 + R_2}{R_1} n\, V_T \log \frac{I_1}{I_2} \tag{10}$$

or

$$V_{OUT} = K \log \frac{I_1}{I_2} \tag{11}$$

It should be noted that the temperature dependance associated with $V_T = KT/q$ is compensated by making R_1 a temperature sensitive resistor with the required positive temperature coefficient.

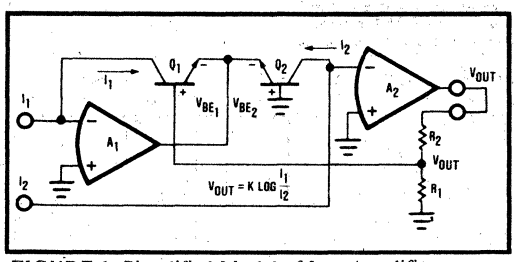


FIGURE 1. Simplified Model of Log Amplifier.

DEFINITION OF TERMS

TRANSFER FUNCTION

The ideal transfer function is $V_{OUT} = K \log \frac{I_1}{I_2}$

where

K = the scale factor with units of volts/decade

I_1 = numerator input current

I_2 = denominator input current.

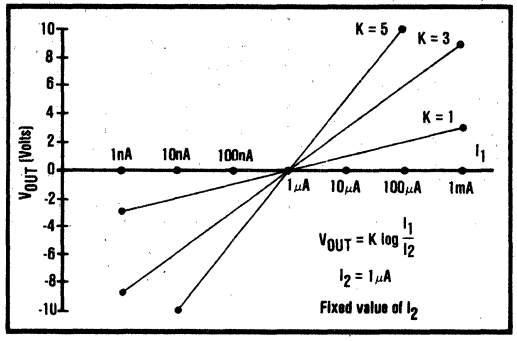


FIGURE 2. Transfer Function with Varying K and I_1.

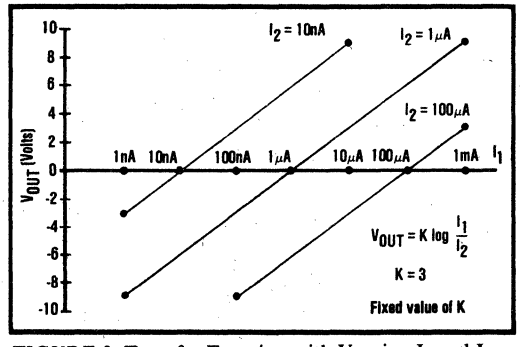


FIGURE 3. Transfer Function with Varying I_2 and I_1.

ACCURACY

Accuracy considerations for a log ratio amplifier are somewhat more complicated than for other amplifiers. The reason is that the transfer function is nonlinear and has two inputs, each of which can vary over a wide dynamic range. The accuracy for any combination of inputs is determined from the total error specification.

TOTAL ERROR

The total error is the deviation (expressed in mV) of the actual output from the ideal output of $V_{OUT} = K \log (I_1/I_2)$. Thus,

$V_{OUT\ (ACTUAL)} = V_{OUT\ (IDEAL)} \pm$ Total Error.

It represents the sum of all the individual components of error normally associated with the log amp when operated in the current input mode. The worst-case error for any given ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately.

Example

I_1 varies over a range of 10nA to 1μA and I_2 varies from 100nA to 10μA. What is the maximum error?

Table I shows the maximum errors for each decade combination of I_1 and I_2.

TABLE I. I_1/I_2 and Maximum Errors.

I_2 (max error)* \ I_1 (max error)*	10nA (30mV)	100nA (25mV)	1μA (20mV)
100nA (25mV)	0.1 (30mV)	1 (25mV)	10 (25mV)
1μA (20mV)	0.01 (30mV)	0.1 (25mV)	1 (20mV)
10μA (25mV)	0.001 (30mV)	0.01 (25mV)	0.1 (25mV)

*Maximum errors are in parenthesis.

Since the largest value of I_1/I_2 is 10 and the smallest is 0.001, K is set at 3V per decade so the output will range from +3V to -9V. The maximum total error occurs when I_1 = 10nA and is equal to K x 30mV. This represents a 0.75% of peak-to-peak FSO error $\frac{(3 \times 0.030)}{12} \times 100\% =$ 0.75% where the full scale output is 12V (from +3V to -9V).

ERRORS RTO AND RTI

As with any transfer function, errors generated by the function itself may be Referred-to-Output (RTO) or Referred-to-Input (RTI). In this respect log amps have a unique property:

Given some error voltage at the log amp's output, that error corresponds to a constant percent of the input regardless of the actual input level.

Refer to: Yu Jen Wong and William E. Ott, "Function Circuits: Design & Applications", McGraw-Hill Book, 1976.

LOG CONFORMITY

Log conformity corresponds to linearity when V_{OUT} is plotted versus I_1/I_2 on a semilog scale. In many applications log conformity is the most important specification. This is true because bias current errors are negligible (1pA compared to input currents of 1nA and above) and the scale factor and offset errors may be trimmed to zero or removed by system calibration. This leaves log conformity as the major source of error.

Log conformity error is defined as the peak deviation from the best-fit straight line of the V_{OUT} versus log (I_1/I_2) curve. This is expressed as a percent of peak-to-peak full scale output. Thus, the nonlinearity error expressed in volts over m decades is

$$V_{OUT\ (NONLIN.)} = K\ 2Nm \text{ volts} \quad (12)$$

where N is the log conformity error, in percent.

INDIVIDUAL ERROR COMPONENTS

The ideal transfer function with current input is

$$V_{OUT} = K \text{ Log } \frac{I_1}{I_2} \quad (13)$$

The actual transfer function with the major components of error is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{I_1 - I_{B_1}}{I_2 - I_{B_2}} \pm K\ 2Nm \pm V_{OS\ OUT} \quad (14)$$

The individual component of error is

ΔK = scale factor error (0.3%, typ)

I_{B_1} = bias current of A_1 (1pA, typ)

I_{B_2} = bias current of A_2 (1pA, typ)

N = log conformity error (0.05%, 0.1%, typ)

$V_{OS\ OUT}$ = output offset voltage (1mV, typ)

m = no. of decades over which N is specified: 0.05% for m = 5, 0.1% for m = 6

Example: what is the error with K = 3 when

$I_1 = 1\mu A$ and $I_2 = 100nA$

$$V_{OUT} = 3(1 \pm 0.003) \log \frac{10^{-6} - 10^{-12}}{10^{-7} - 10^{-12}} \pm 3(2)(0.0005)\ 5 \pm 1mV \quad (15)$$

$$\approx 3.009 \log \frac{10^{-6}}{10^{-7}} + 0.015 + 0.001 \quad (16)$$

$$= 3.009\ (1) + 0.015 + 0.001 \quad (17)$$

$$= 3.025 \text{ volts} \quad (18)$$

Since the ideal output is 3.000V the error as a percent of reading is

$$\%\ \text{error} = \frac{0.025}{3} \times 100\% = 0.83\% \quad (19)$$

For the case of voltage inputs, the actual transfer function is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{\frac{V_1}{R_1} - I_{B_1} \pm \frac{E_{OS_1}}{R_1}}{\frac{V_2}{R_2} - I_{B_2} \pm \frac{E_{OS_2}}{R_2}} \pm K\ 2Nm \pm V_{OS\ OUT} \quad (20)$$

FREQUENCY RESPONSE

The 3dB frequency response of the LOG100 is a function of the magnitude of the input current levels and of the value of the frequency compensation capacitor. See Performance Curves for details.

The frequency response curves are shown for constant DC I_1 and I_2 with a small signal AC current on one of them.

The transient response of the LOG100 is different for increasing and decreasing signals. This is due to the fact that a log amp is a nonlinear gain element and has different gains at different levels of input signals. Frequency response decreases as the gain increases.

GENERAL INFORMATION

INPUT CURRENT RANGE

The stated input range of 1nA to 1mA is the range for specified accuracy. Smaller or larger input currents may be applied with decreased accuracy. Currents larger than 1mA result in increased nonlinearity. The 10mA absolute maximum is a conservative value to limit the power dissipation in the output stage of A_1 and the logging transistor. Currents below 1nA will result in increased errors due to the input bias currents of A_1 and A_2 (1pA typical). These errors may be nulled. See Optional Adjustments section.

FREQUENCY COMPENSATION

Frequency compensation for the LOG100 is obtained by connecting a capacitor between pins 7 and 14. The size of the capacitor is a function of the input currents as shown in the Performance Curves. For any given application the smallest value of the capacitor which may be used is determined by the maximum value at I_2 and the minimum value of I_1. Larger values of C_C will make the LOG100 more stable, but will reduce the frequency response.

SETTING THE REFERENCE CURRENT

When the LOG100 is used as a straight log amplifier I_2 is constant and becomes the reference current in the expression

$$V_{OUT} = K \log \frac{I_1}{I_{REF}} \quad (21)$$

I_{REF} can be derived from an external current source (such as shown in Figure 4) or it may be derived from a voltage source with one or more resistors.

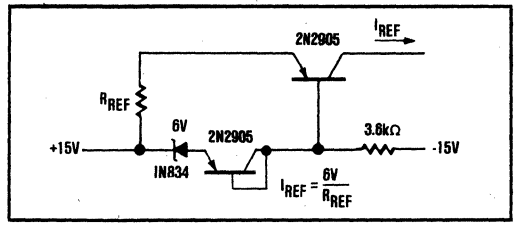


FIGURE 4. Temperature-Compensated Current Reference.

When a single resistor is used the value may be quite large when I_{REF} is small. If I_{REF} is 10nA and +15V is used

$$R_{REF} = \frac{15V}{10\,nA} = 1500M\Omega.$$

A voltage divider may be used to reduce the value of the resistor. When this is done one must be aware of possible errors caused by the amplifier's input offset voltage. This is shown in Figure 5.

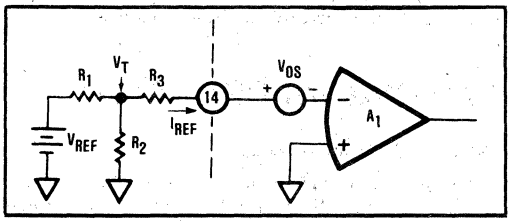


FIGURE 5. "T" Network for Reference Current.

In this case the voltage at pin 14 is not exactly zero, but is equal to the value of the input offset voltage of A_1 which ranges from zero to ±5mV. V_T must be kept much larger than 5mV in order to make this effect negligible. This concept also applies to pin 1.

OPTIONAL ADJUSTMENTS

The LOG100 will meet its specified accuracy with no user adjustments. If improved performance is desired the following optional adjustments may be made.

INPUT BIAS CURRENT

The circuit in Figure 6 may be used to compensate for the input bias currents of A_1 and A_2. Since the amplifiers have FET inputs with the characteristic bias current doubling every 10°C this nulling technique is practical only where the temperature is fairly stable.

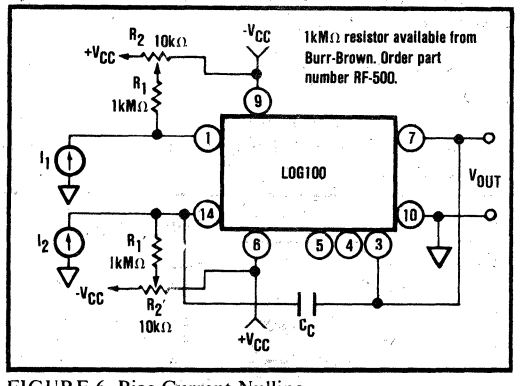


FIGURE 6. Bias Current Nulling.

OUTPUT OFFSET

The output offset may be nulled with the circuit in Figure 7. I_1 and I_2 are set equal at some convenient value in the range of 100nA to 100μA. R_1 is then adjusted for zero output voltage.

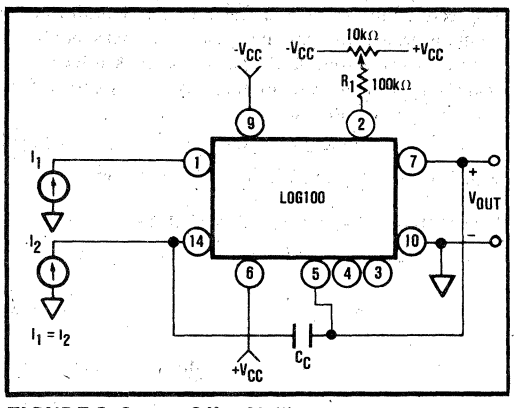


FIGURE 7. Output Offset Nulling.

ADJUSTMENTS OF SCALE FACTOR K

The value of K may be changed by increasing or decreasing the voltage divider resistor normally connected to the output, pin 7. To increase K put resistance in series between pin 7 and the appropriate scaling resistor pin (3, 4 or 5). To decrease K place a parallel resistor between pin 2 and either pin 3, 4 or 5.

APPLICATION INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the LOG100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 100pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the LOG100's output. This resistor will, of course, form a voltage divider with other resistive loads.

CIRCUIT PROTECTION

The LOG100 can be protected against accidental power supply reversal by putting a diode (1N4001 type) in series with each power supply line as shown in Figure 8. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off. If this protection circuit is used, the accuracy of the LOG100 will be degraded slightly by the voltage drops across the diodes as determined by the power supply sensitivity specification.

The LOG100 uses small geometry FET transistors to achieve the low input bias currents. Normal FET handling techniques should be used to avoid damage caused by low energy electrostatic discharge (ESD).

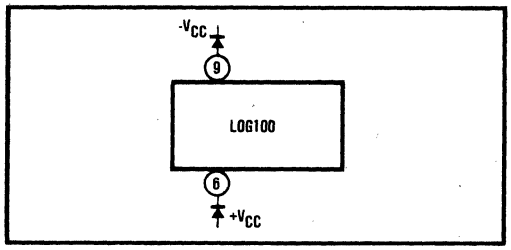


FIGURE 8. Reverse Polarity Protection.

LOG RATIO

One of the more common uses of log ratio amplifiers is to measure absorbance. A typical application is shown in Figure 9.

Absorbance of the sample is: $A = \log \frac{\lambda_1'}{\lambda_1}$ (22)

If $\lambda_2 = \lambda_1$ and D_1 and D_2 are matched $A \propto K \log \frac{I_1}{I_2}$. (23)

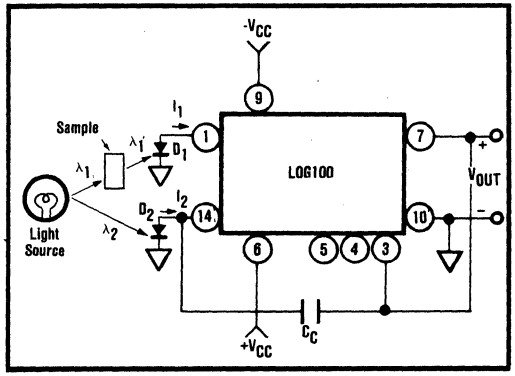


FIGURE 9. Absorbance Measurement.

DATA COMPRESSION

In many applications the compressive effects of the logarithmic transfer function is useful. For example, a LOG100 preceding an 8-bit analog-to-digital converter can replace a more expensive 20-bit converter.

SELECTING OPTIMUM VALUES OF I_2 AND K

In straight log applications (as opposed to log ratio) both K and I_2 are selected by the designer. In order to minimize errors due to output offset and noise it is normally best to scale the log amp to use as much of the ±10V output range as possible. Thus, with the range of I_1 from $I_{1\,MIN}$ to $I_{1\,MAX}$;

For $I_{1\,MAX}$ $+10V = K \log I_{1\,MAX}/I_2$ (24)

For $I_{1\,MIN}$ $-10V = K \log I_{1\,MIN}/I_2$ (25)

Addition of these two equations and solving for I_2 shows that its optimum value, $I_{2\,OPT}$, is the geometric mean of $I_{1\,MAX}$ and $I_{1\,MIN}$.

$$I_{2\,OPT} = \sqrt{I_{1\,MAX} \times I_{1\,MIN}} \quad (26)$$

$$K_{OPT} = \frac{10}{\log \frac{I_{1\,MAX}}{I_{2\,OPT}}} \quad (27)$$

Since K is selectable in discrete steps, use the largest value of K available which does not exceed K_{OPT}.

NEGATIVE INPUT CURRENTS

The LOG100 will function only with positive input currents (conventional current flow into pins 1 and 14). Some current sources (such as photomultiplier tubes) provide negative input currents. In such situations the circuit in Figure 10 may be used.

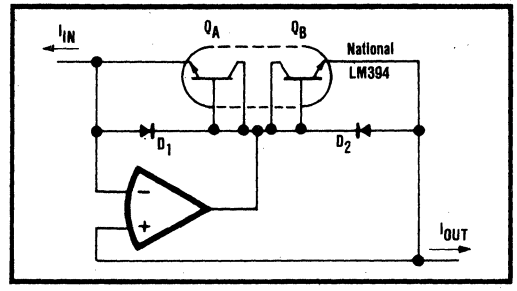


FIGURE 10. Current Inverter.

VOLTAGE INPUTS

The LOG100 gives the best performance with current inputs. Voltage inputs may be handled directly with series resistors, but the dynamic input range is limited to approximately three decades of input voltage by voltage noise and offsets. The transfer function of equation (20) applies to this configuration.

ANTILOG CONFIGURATION (an implicit technique)

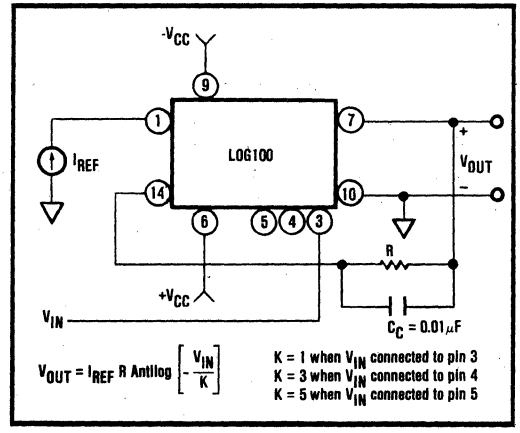
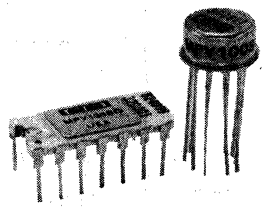


FIGURE 11. Connections for Antilog Function.

BURR-BROWN®



MPY100

MULTIPLIER-DIVIDER

FEATURES

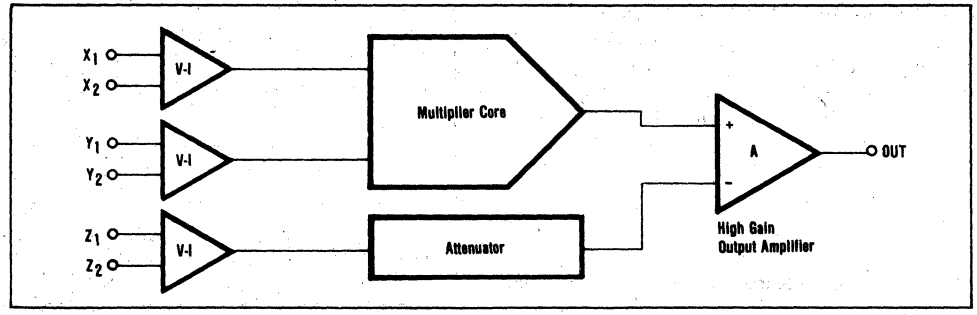
- LOW COST
- DIFFERENTIAL INPUT
- ACCURACY 100% TESTED AND GUARANTEED
- NO EXTERNAL TRIMMING REQUIRED
- LOW NOISE
  90μV, rms, 10Hz to 10kHz
- HIGHLY RELIABLE ONE-CHIP DESIGN
- DIP OR TO-100 TYPE PACKAGE
- WIDE TEMPERATURE OPERATION

APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOT
- LINEARIZATION
- POWER COMPUTATION
- ANALOG SIGNAL PROCESSING
- ALGEBRAIC COMPUTATION
- TRUE RMS-TO-DC CONVERSION

DESCRIPTION

The MPY100 multiplier-divider is a low cost precision device designed for general purpose application. In addition to four-quadrant multiplication, it also performs analog square root and division without the bother of external amplifiers or potentiometers. Laser-trimmed one-chip design offers the most in highly reliable operation with guaranteed accuracies. Because of the internal reference and pretrimmed accuracies the MPY100 does not have the restrictions of other low cost multipliers. It is available in both TO-100 and DIP ceramic packages.



MPY100 FUNCTIONAL BLOCK DIAGRAM

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_S$ = 15VDC unless otherwise noted.

MODEL		MPY100A			MPY100B/C			MPY100S			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
MULTIPLIER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$			*/*			*		
Total Error	-10V ≤ X, Y ≤ 10V										
Initial	T_A = +25°C			±2.0			±1.0/0.5			±0.5	% FSR
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.017	±0.05		±0.008/0.008	±0.02/0.02				% FSR/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.025	±0.05	% FSR/°C
vs. Supply[1]			±0.05			*/*			*		% FSR/%
Individual Errors											
Output Offset											
Initial	T_A = +25°C		±50	±100		±10/7	±50/25		±7	±50mV	mV
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.7	±2.0		±0.7/0.3	±2.0/±0.7				mV/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.3	±0.7	mV/°C
vs. Supply[1]			±0.25			*/*			*		mV/%
Scale Factor Error											
Initial	T_A = +25°C		±0.12			*/*			*		% FSR
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.008			*/*					% FSR/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.008		% FSR/°C
vs. Supply[1]			±0.05			*/*			*		% FSR/%
Nonlinearity											
X Input	X = 20V, p-p; Y = ±10VDC		±0.08			*/*			*		% FSR
Y Input	Y = 20V, p-p; X = ±10VDC		±0.08			*/*			*		% FSR
Feedthrough	f = 50Hz										
X Input	X = 20V, p-p; Y = 0		100			30/30			30		mV, p-p
Y Input	Y = 20V, p-p; X = 0		6			*/*			*		mV, p-p
vs. Temperature	-25°C ≤ T_A ≤ +85°C		0.1			*/*					mV, p-p/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								0.1		mV, p-p/°C
vs. Supply[1]			0.15			*/*			*		mV, p-p/%
DIVIDER PERFORMANCE											
Transfer Function	$X_1 > X_2$		$\frac{10(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			*/*			*		
Total Error with	X = 10V										
external adjustments	-10V ≤ Z ≤+10V		±1.5			±0.75/0.35			±0.35		% FSR
	X = 1V										
	-1V ≤ Z ≤ +1V		±4.0			±2.0/1.0			±1.0		% FSR
	+0.2V ≤ X ≤ +10V										
	-10V ≤ Z ≤ +10V		±5.0			±2.5/1.0			±1.0		% FSR
SQUARER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)^2}{10} + Z_2$			*/*			*		
Total Error	-10V ≤ X ≤ +10V		±1.2			±0.6/0.3			±0.3		% FSR
SQUARE-ROOTER PERFORMANCE											
Transfer Function	$Z_1 < Z_2$		$+\sqrt{10(Z_2 - Z_1)} + X_2$			*/*			*		
Total Error	1V ≤ Z ≤ 10V		±2			±1/0.5			±0.5		% FSR
AC PERFORMANCE											
Small-Signal Bandwidth			550			*/*			*		kHz
1% Amplitude Error	Small-Signal		70			*/*			*		kHz
1% 0.57° Vector Error	Small-Signal		5			*/*			*		kHz
Full Power Bandwidth	$\|V_O\|$ = 10V, R_L = 2kΩ		320			*/*			*		kHz
Slew Rate	$\|V_O\|$ = 10V, R_L = 2kΩ		20			*/*			*		V/μsec
Settling Time	ε = ±1%, ΔV_O = 20V		2			*/*			*		μsec
Overload Recovery	50% Output Overload		0.2			*/*			*		μsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Rated Operation		±10			*/*			*			V
Absolute Maximum				±V_{CC}			*/*			*	V
Input Resistance	X, Y, Z[2]		10			*/*			*		MΩ
Input Bias Current	X, Y, Z		1.4			*/*			*		μA
OUTPUT CHARACTERISTICS											
Rated Output											
Voltage	I_O = ±5mA	±10			*/*			*			V
Current	V_O = ±10V	±5			*/*			*			mA
Output Resistance	f = DC		1.5			*/*			*		Ω
OUTPUT NOISE VOLTAGE	X = Y = 0										
f_O = 1Hz			6.2			*/*			*		μV/√Hz
f_O = 1kHz			0.6			*/*			*		μV/√Hz
1/f Corner Frequency			110			*/*			*		Hz
f_B = 5Hz to 10kHz			60			*/*			*		μV, rms
f_B = 5Hz to 5MHz			1.3			*/*			*		mV, rms
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*/*			*		VDC
Operating Range	Derated Performance	±8.5		±20	*/*		*/*	*		*	VDC
Quiescent Current			±5.5			*/*			*/*		mA

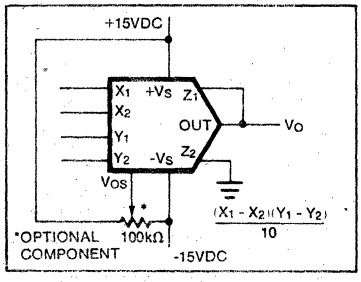
ELECTRICAL SPECIFICATIONS (CONT)

MODEL		MPY100A			MPY100B/C			MPY100S			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE (Ambient)											
Specification	Derated Performance	-25		+85	*/*		*/*	-55		+125	°C
Operating Range		-55		+125	*/*		*/*	*		*	°C
Storage		-65		+150	*/*		*/*	*		*	°C

NOTES:
1. Includes effects of recommended null pots.
2. Z_2 input resistance is 10MΩ, typical, with Vos pin open.
   If Vos pin is grounded or used for optional offset adjustment,
   the Z_2 input resistance may be as low as 25kΩ.

*Same as MPY100A specification. */* means B/C grades same as MPY100A specification.

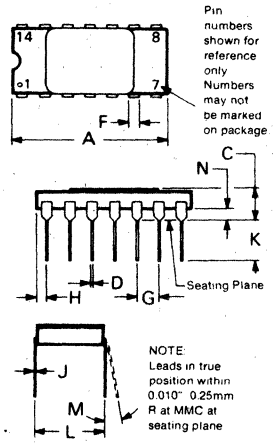
CONNECTION DIAGRAM



MECHANICAL

CERAMIC DUAL-IN-LINE PACKAGE

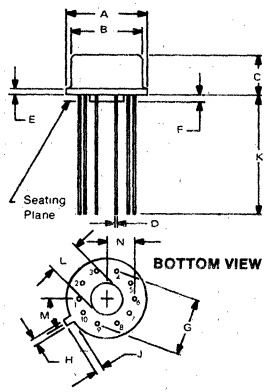
Order Number:
MPY100AG, MPY100BG
MPY100CG, MPY100SG



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M		10°		10°
N	.009	.060	0.23	1.52

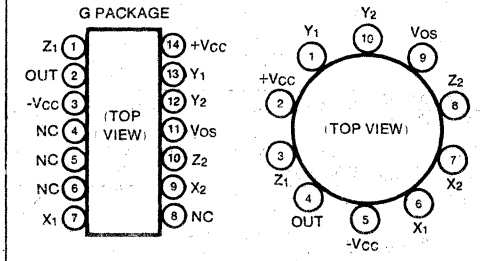
METAL CAN PACKAGE

Order Number:
MPY100AM, MPY100BM
MPY100CM, MPY100SM



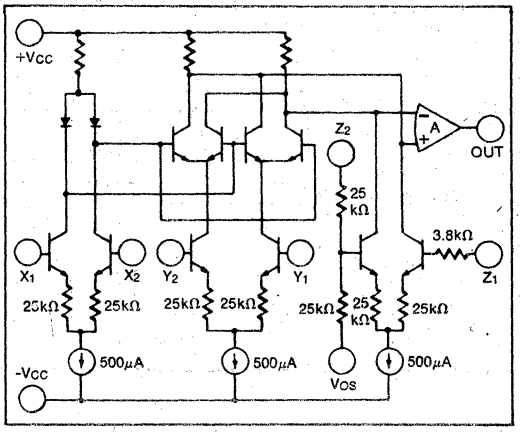
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

PIN CONFIGURATION

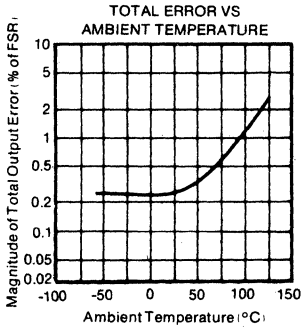


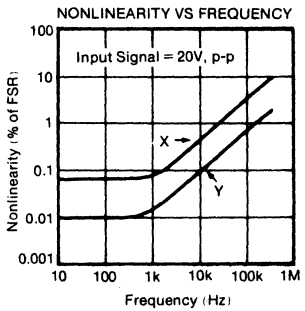
NOTES:
1. Vos adjustment optional not normally recommended. Vos pin may be left open or grounded.
2. All unused input pins should be grounded.

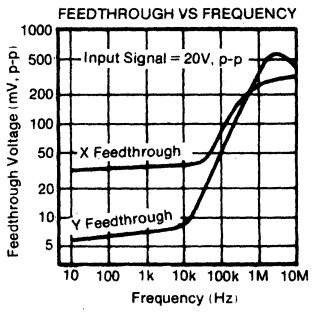
SIMPLIFIED SCHEMATIC

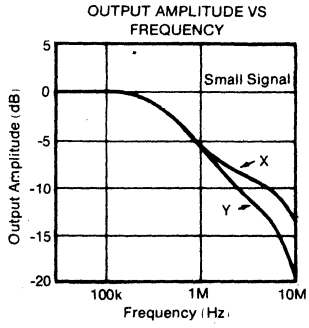


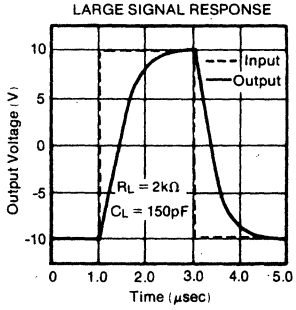
TYPICAL PERFORMANCE CURVES

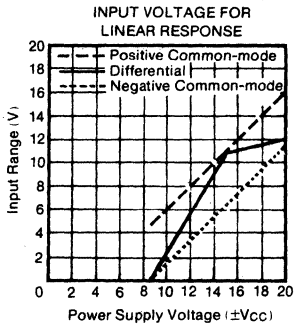


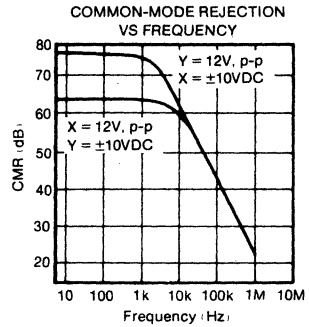


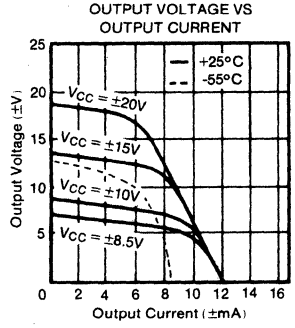


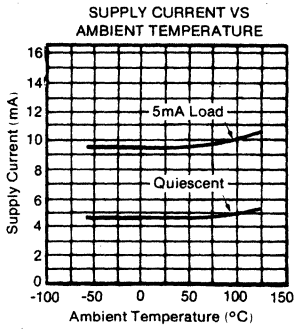












ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-circuit Duration(3)	Continuous
Junction Temperature	+150°C

NOTES:
1. Package must be derated on θ_{JC} = 15°C/W and θ_{JA} = 165°C/W for the metal package and θ_{JC} = 35°C/W and θ_{JA} = 220°C/W for the ceramic package.
2. For supply voltages less than ±20VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground only. Rating applies to +85°C ambient for the metal package and +65°C for the ceramic package.

APPLICATIONS INFORMATION

THEORY OF OPERATION

The MPY100 is a variable transconductance multiplier consisting of three differential voltage-to-current converters, a multiplier core and an output differential amplifier as illustrated in Figure 1.

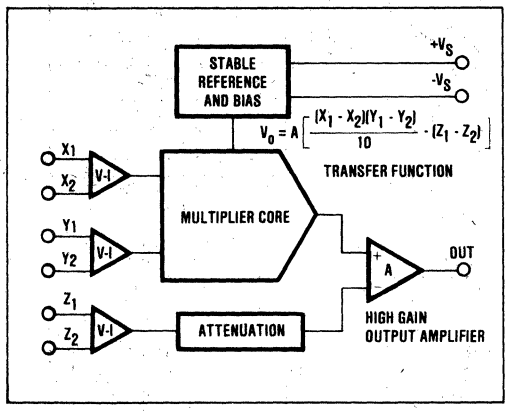


FIGURE 1. MPY100 Functional Block Diagram.

The basic principle of the transconductance multiplier can be demonstrated by the differential stage in Figure 2.

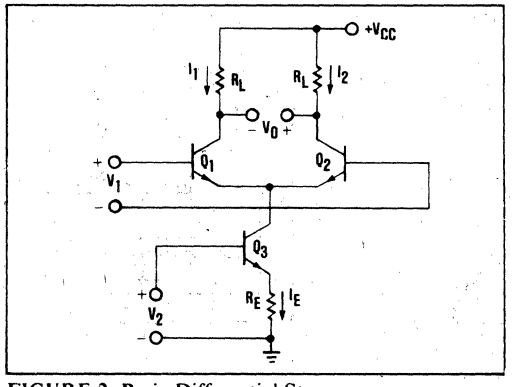


FIGURE 2. Basic Differential Stage as a Transconductance Multiplier.

For small values of the input voltage V_1 that are much smaller than V_T, the transistor's thermal voltage, the differential output voltage V_o is

$$V_o = g_m R_L V_1.$$

The transconductance g_m of the stage is given by:

$$g_m = I_E / V_T,$$

and is modulated by the voltage V_2 to give

$$g_m \approx V_2 / V_T R_E.$$

Substituting this into the original equation yields the overall transfer function

$$V_o = g_m R_L V_1 = V_1 V_2 (R_L / V_T R_E)$$

which shows the output voltage to be the product of the two input voltages, V_1 and V_2.

Variations in I_E due to V_2 cause a large common-mode voltage swing in the circuit. The errors associated with this common-mode voltage can be eliminated by using two differential stages in parallel and cross-coupling their outputs as shown in Figure 3.

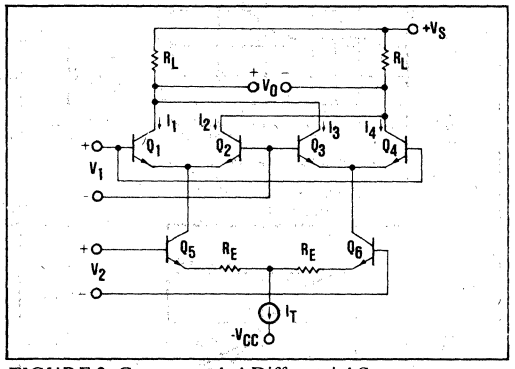


FIGURE 3. Cross-coupled Differential Stages as a Variable-transconductance Multiplier.

An analysis of the circuit in Figure 3 shows it to have the same overall transfer function as before:

$$V_o = V_1 V_2 (R_L / V_T R_E).$$

For input voltages larger than V_T the voltage-to-current transfer characteristics of the differential pair Q_1, Q_2 or Q_3 and Q_4 are no longer linear. Instead, their collector currents are related to the applied voltage V_1 as

$$\frac{I_1}{I_2} = \frac{I_3}{I_4} = e^{\frac{V_1}{V_T}}$$

The resultant nonlinearity can be overcome by developing V_1 logarithmically to exactly cancel the exponential relationship just derived. This is done by diodes D_1 and D_2 in Figure 4.

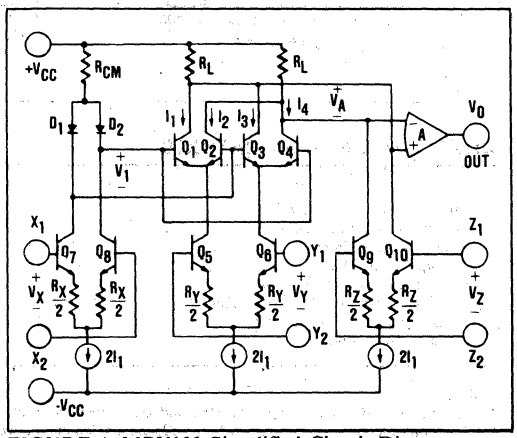


FIGURE 4. MPY100 Simplified Circuit Diagram.

The emitter degeneration resistors R_X and R_Y, in Figure 4, provide a linear conversion of the input voltages to differential current I_X and I_Y, where

$$I_X = V_X / R_X \text{ and } I_Y = V_Y / R_Y.$$

Analysis of Figure 4 shows the voltage V_A to be

$$V_A = (2R_L / I_1)(I_X I_Y).$$

Since I_X and I_Y are linearly related to the input voltages V_X and V_Y, V_A may also be written

$$V_A = KV_XV_Y$$

where K is a scale factor. In the MPY100, K is chosen to be 0.1.

The addition of the Z input alters the voltage V_A to

$$V_A = KV_XV_Y - V_Z.$$

Therefore, the output of the MPY100 is

$$V_o = A[KV_XV_Y - V_Z]$$

where A is the open-loop gain of the output amplifier. Writing this last equation in terms of the separate inputs to the MPY100 gives

$$V_o = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2)\right],$$

the transfer function of the MPY100.

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins of the MPY100 to the power supply common. The connection of these capacitors should be as close to the MPY100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root mode for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the MPY100's output.

DEFINITIONS

TOTAL ERROR (Accuracy)

Total error is the actual departure of the multiplier output voltage from the ideal product of its input voltages. It includes the sum of the effects of input and output DC offsets, gain error and nonlinearity.

OUTPUT OFFSET

Output offset is the output voltage when both inputs V_X and V_Y are zero volts.

SCALE FACTOR ERROR

Scale factor error is the difference between the actual scale factor and the ideal scale factor.

NONLINEARITY

Nonlinearity is the maximum deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

FEEDTHROUGH

Feedthrough is the signal at the output for any value of V_X or V_Y within the rated range, when the other input is zero.

SMALL SIGNAL BANDWIDTH

Small signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value for a nominal output amplitude of 10% of full scale.

1% AMPLITUDE ERROR

The 1% amplitude error is the frequency the output amplitude is in error by 1%, measured with an output amplitude of 10% of full scale.

1% VECTOR ERROR

The 1% vector error is the frequency at which a phase error of 0.01 radians (0.57°) occurs. This is the most sensitive measure of dynamic error of a multiplier.

TYPICAL APPLICATIONS

MULTIPLICATION

Figure 5 shows the basic connection for four-quadrant multiplication.

The MPY100 meets all of its specifications without trimming. Accuracy can, however, be improved over a limited range by nulling the output offset voltage using the 100kΩ optional balance potentiometer shown in Figure 5.

AC feedthrough may be reduced to a minimum by applying an external voltage to the X or Y input as shown in Figure 6.

Z_2, the optional summing input, may be used to sum a voltage into the output of the MPY100. If not used, this

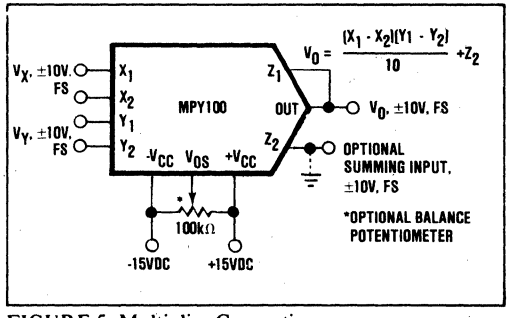


FIGURE 5. Multiplier Connection.

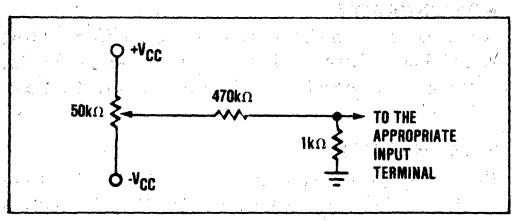


FIGURE 6. Optional Trimming Configuration.

terminal, as well as the X and Y input terminals, should be grounded. All inputs should be referenced to power supply common.

Figure 7 shows how to achieve a scale factor larger than the nominal 1/10. In this case, the scale factor is unity which makes the transfer function

$$V_o = KV_XV_Y = K(X_1 - X_2)(Y_1 - Y_2).$$

$$K = \frac{1 + (R_1/R_2)}{10}$$

$$0.1 \leq K \leq 1$$

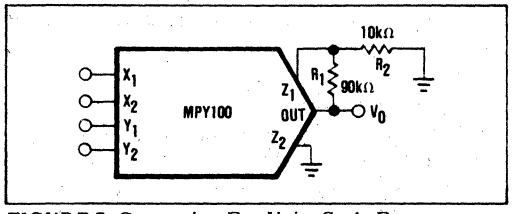


FIGURE 7. Connection For Unity Scale Factor.

This circuit has the disadvantage of increasing the output offset voltage by a factor of 10 which may require the use of the optional balance control as in Figure 1 for some applications. In addition, this connection reduces the small signal bandwidth to about 50kHz.

DIVISION

Figure 8 shows the basic connection for two-quadrant division. This configuration is a multiplier-inverted analog divider, i.e., a multiplier connected in the feedback loop of an operational amplifier. In the case of the MPY100 this operational amplifier is the output amplifier shown in Figure 1.

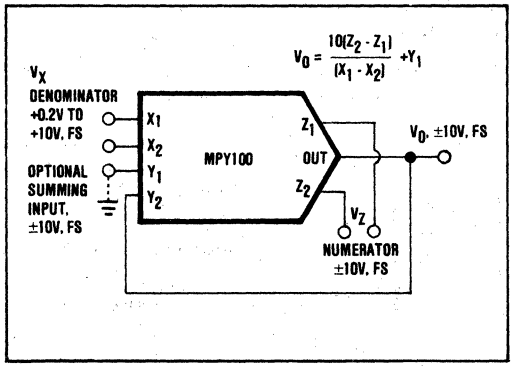


FIGURE 8. Divider Connection.

The divider error with a multiplier-inverted analog divider is approximately

$$\epsilon_{divider} = 10\ \epsilon_{multiplier}/(X_1 - X_2)$$

It is obvious from this error equation that divider error becomes excessively large for small values of $X_1 - X_2$. A 10-to-1 denominator range is usually the practical limit. If more accurate division is required over a wide range of denominator voltages, an externally generated voltage may be applied to the unused X-input (see Optional Trim Configuration). To trim, apply a ramp of +100mV to +1V at 100Hz to both X_1 and Z_1 if X_2 is used for offset adjustment, otherwise reverse the signal polarity, and adjust the trim voltage to minimize the variation in the output. An alternative to this procedure would be to use the Burr-Brown DIV100, a precision log-antilog divider.

SQUARING

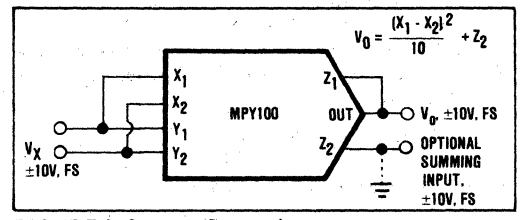


FIGURE 9. Squarer Connection.

SQUARE ROOT

Figure 10 shows the connection for taking the square root of the voltage V_Z. The diode prevents a latching condition which could occur if the input momentarily changed polarity. This latching condition is not a design flaw in the MPY100, but occurs when a multiplier is connected in the feedback loop of an operational amplifier to perform square root functions.

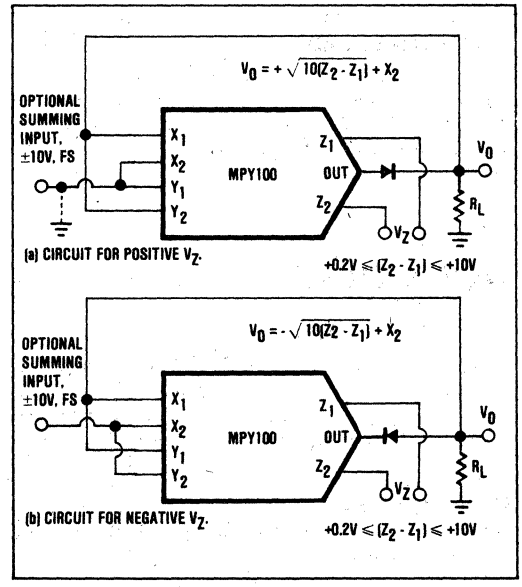


FIGURE 10. Square Root Connection.

The load resistance R_L must be in the range of $10k\Omega \leq R_L \leq 1M\Omega$. This resistance must be in the circuit as it provides the current necessary to operate the diode.

BRIDGE LINEARIZATION

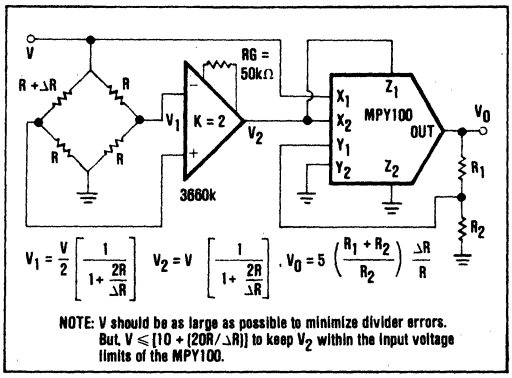


FIGURE 11. Bridge Linearization.

The use of the MPY100 to linearize the output from a bridge circuit makes the output V_o independent of the bridge supply voltage.

TRUE RMS-TO-DC CONVERSION

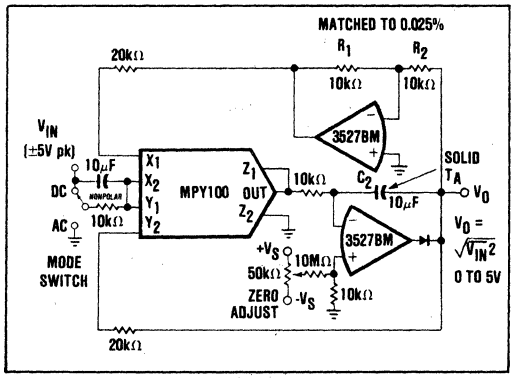


FIGURE 12. True RMS-to-DC Conversion.

The rms-to-DC conversion circuit of Figure 12 gives greater accuracy and bandwidth but with less dynamic range than most rms-to-DC converters.

PERCENTAGE COMPUTATION

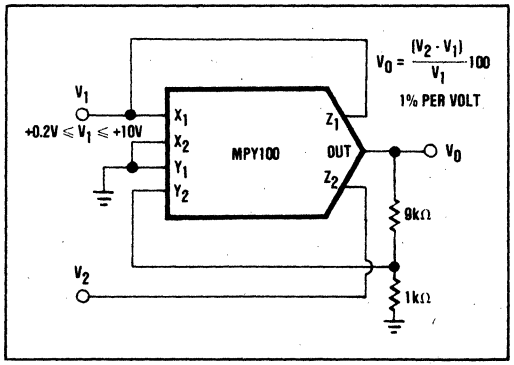


Figure 13. Percentage Computation.

The circuit of Figure 13 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2/R_1.

SINE FUNCTION GENERATOR

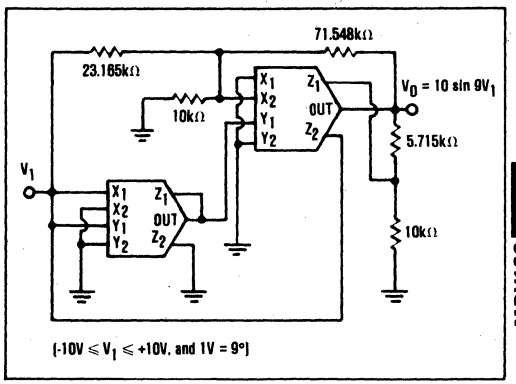


FIGURE 14. Sine Function Generator.

The circuit in Figure 14 uses implicit feedback to implement the following sine function approximation:

$$V_o = (1.5715V_i - 0.004317V_i^5)(1 + 0.001398V_i^2)$$
$$= 10 \sin(9V_i).$$

SINGLE-PHASE POWER MEASUREMENT

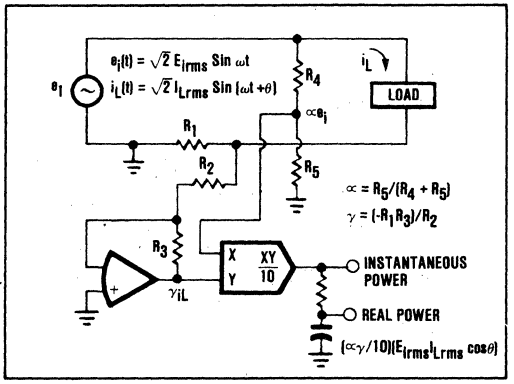
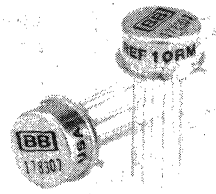


FIGURE 15. Single-Phase Instantaneous and Real Power Measurement.

MORE CIRCUITS

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the Burr-Brown McGraw Hill book "FUNCTION CIRCUITS - Design and Applications."

BURR-BROWN®



REF10

Precision VOLTAGE REFERENCE

FEATURES

- +10.00V OUTPUT
- HIGH ACCURACY, ±0.005V
- VERY-LOW DRIFT, 1ppm/°C max
- EXCELLENT STABILITY, 25ppm/1000hrs.
- LOW NOISE, 6μV p-p, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE, up to 35V

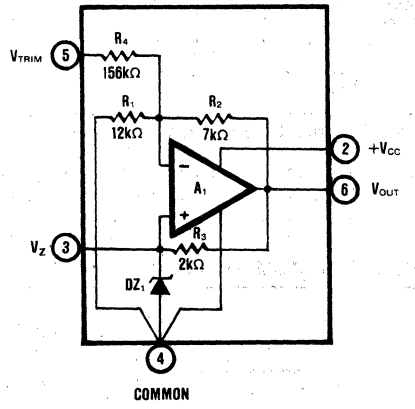
APPLICATIONS

- PRECISION CALIBRATED VOLTAGE STANDARD
- TRANSDUCER EXCITATION
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT

DESCRIPTION

The REF10 is a precision voltage reference which provides a +10.00V output. The drift is laser-trimmed to 1ppm/°C max (KM grade) over the full specification range. This is in contrast to some references which guarantee drift over a limited portion of their specification temperature range. The REF10 achieves its precision without a heater. This results in low quiescent current, fast warm-up, excellent stability, and low noise.

The output can be adjusted with minimal effect on drift or stability. Single supply operation over 13.5V to 35V supply range and excellent overall specifications make the REF10 an ideal choice for the most demanding applications such as precision system standards, D/A and A/D references, transducer excitation, etc.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

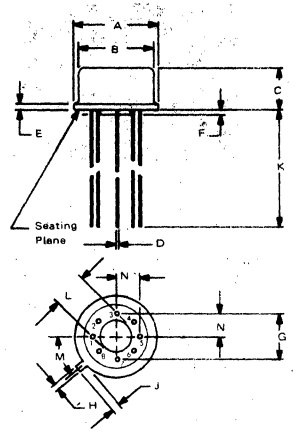
At T_A = +25°C and +15VDC power supply unless otherwise noted.

PARAMETER	CONDITION	REF10JM/KM/RM/SM MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE					
Initial	T_A = +25°C	9.995	10.000	10.005	V
Trim Range[1]		−0.100		+0.250	V
vs Temperature[2]: KM	0°C to +70°C			1	ppm/°C
JM	0°C to +70°C			3	ppm/°C
SM	−55°C to +125°C			3	ppm/°C
RM	−55°C to +125°C			6	ppm/°C
vs Supply (line regulation)	V_{CC} = 13.5 to 35V		0.001	0.002	%/V
vs Output Current (load regulation)	I_L = 0 to ±10mA		0.001	0.002	%/mA
vs Time	T_A = +25°C		50		ppm/1000 hrs
NOISE	0.1Hz to 10Hz		6	25	μV p-p
OUTPUT CURRENT	Source or Sink	±10			mA
INPUT VOLTAGE RANGE		13.5		35	V
QUIESCENT CURRENT	I_{OUT} = 0		4.5	6	mA
WARM-UP TIME	To 0.1%		10		μsec
TEMPERATURE RANGE					
Specification: JM, KM		0		+70	°C
RM, SM		−55		+125	°C
Operating: JM, KM		−25		+85	°C
RM, SM		−55		+125	°C
Storage		−65		+125	°C

NOTES:
1. Trimming the offset voltage will affect the drift slightly. See Installation and Operating Instructions for details.
2. The "box method" is used to specify output voltage drift vs temperature. See the Discussion of Performance section.

MECHANICAL

TO-99 PACKAGE



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers not marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

WEIGHT: 1 gram

ORDERING INFORMATION

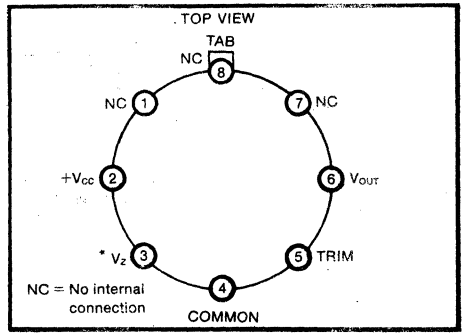
REF10 X M

Basic Model Number
Performance Grade Code
J, K: 0°C to +70°C
R, S: −55°C to +125°C
Package Code
TO-99

ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Power Dissipation at +25°C 200mW
Operating Temperature Range
REF10JM/KM ..... −25°C to +85°C
REF10RM/SM ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +125°C
Lead Temperature (soldering, 10sec) ..... +300°C
Short-Circuit Protection at +25°C to Common or +15VDC ..... Continuous

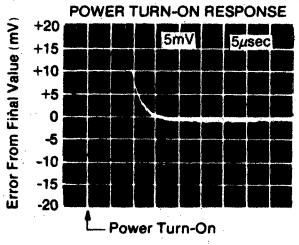
PIN CONFIGURATION



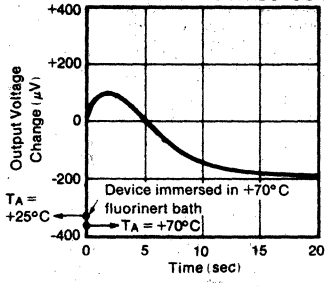
*Pin 3 is an unbuffered 6.3V output. Any load will affect the output voltage and drift. A load of 1μA on pin 3 will typically change the output voltage by 50μV and the drift by 0.1ppm/°C.

TYPICAL PERFORMANCE CURVES

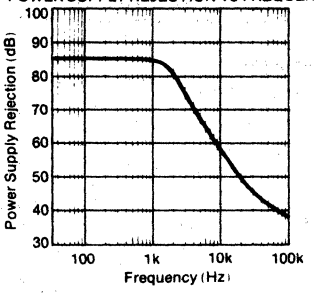
POWER TURN-ON RESPONSE



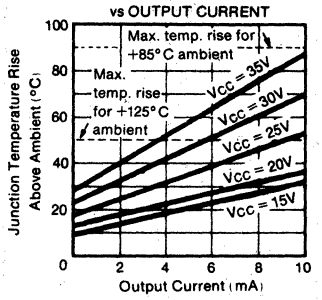
RESPONSE TO THERMAL SHOCK



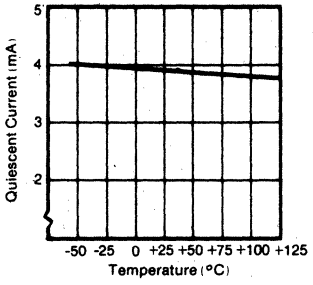
POWER SUPPLY REJECTION VS FREQUENCY



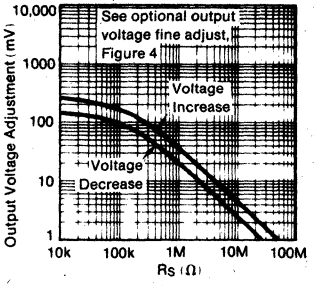
JUNCTION TEMPERATURE RISE vs OUTPUT CURRENT



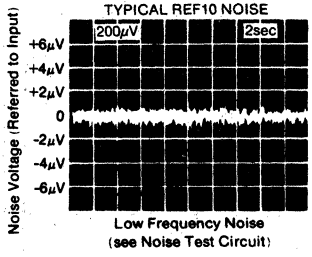
QUIESCENT CURRENT VS TEMPERATURE



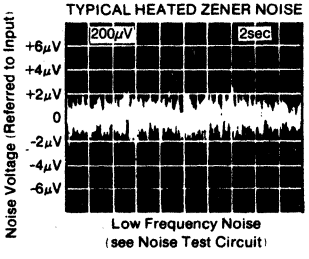
OUTPUT VOLTAGE ADJUSTMENT vs RS



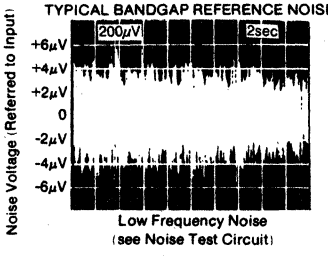
TYPICAL REF10 NOISE

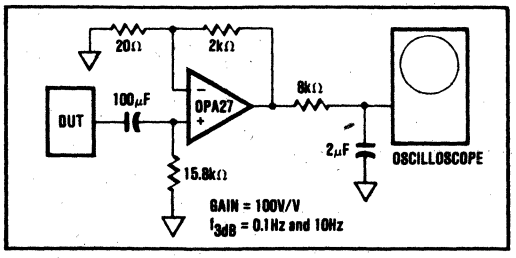


TYPICAL HEATED ZENER NOISE



TYPICAL BANDGAP REFERENCE NOISE





NOISE TEST CIRCUIT

THEORY OF OPERATION

The following discussion refers to the diagram on the first page.

In operation, approximately 6.3V is applied to the noninverting input of op amp A_1 by zener diode DZ_1. This voltage is amplified by A_1 to produce the 10.00V output. The gain is determined by R_1 and R_2: $G = (R_1 + R_2)/R_1$. R_1 and R_2 are actively laser-trimmed to produce an exact 10.00V output. The zener operating current is derived from the regulated output voltage through R_3. This feedback arrangement provides closely regulated zener current. R_3 is actively laser-trimmed to set the zener current to a level which results in low drift at the output of A_1. R_4 allows user-trimming of the output voltage by providing for a small external adjustment of amplifier gain. Since the TCR of R_4 closely matches the TCR of the gain setting resistors, the voltage trim has minimal effect on the drift of the reference.

DISCUSSION OF PERFORMANCE

The REF10 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the "butterfly method" and the "box method." The REF10 is specified with the more commonly used box method. The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

For the REF10 each J and K unit is tested at temperatures of 0°C, +25°C, +50°C, and +70°C and each R and S unit is tested at −55°C, −25°C, 0°C, +25°C, +50°C, +75°C, +100°C and +125°C. The minimum and maximum test voltages must meet this condition:

$$\left[\frac{(V_{OUT\ max} - V_{OUT\ min})/10V}{T_{high} - T_{low}}\right] \times 10^6 \leq \text{drift specification}$$

This assures the user that the variations of output voltage that occur as the temperature changes within the specification range T_{low} to T_{high} will be contained within a box whose diagonal has a slope equal to the maximum specified drift. Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{Upper\ Bound}$ and $V_{Lower\ Bound}$ (see Figure 1).

Figure 1 uses the REF10KM as an example. It has a drift specification of 1ppm/°C maximum and a specification temperature range of 0°C to +70°C. The "box" height (V_1 to V_2) is 700μV and upper bound and lower bound voltages are a maximum of 700μV away from the voltage at +25°C.

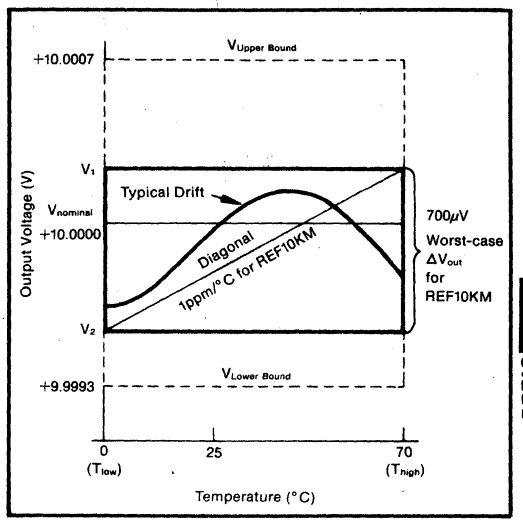


FIGURE 1. REF10KM Output Voltage Drift.

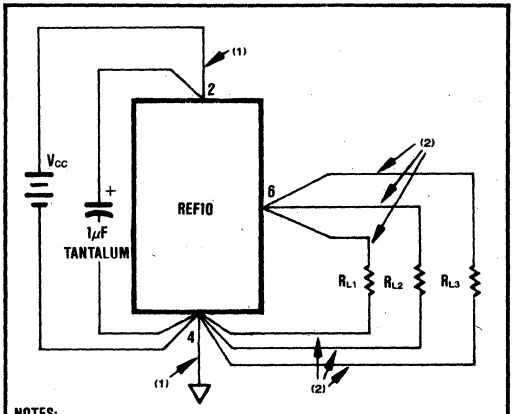
INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF10. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figure 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.01ppm/°C



NOTES:
1. Lead resistances here of up to a few ohms have negligible effect on performance.
2. A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF10 Installation.

per mV of trimmed voltage. In the circuit in Figure 3 any mismatch in TCR between the two sections of the potentiometer will also affect drift but the effect of the ΔTCR is reduced by a factor of 40 by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a range of approximately +250mV to −100mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 156kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

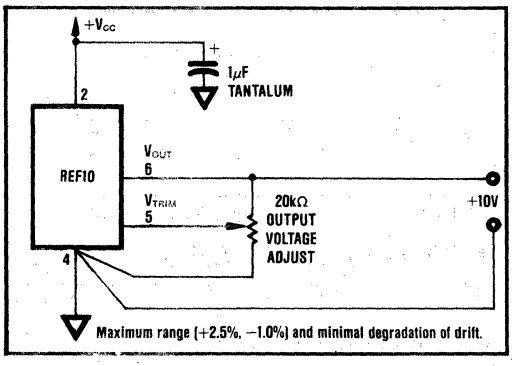


FIGURE 3. REF10 Optional Output Voltage Adjust.

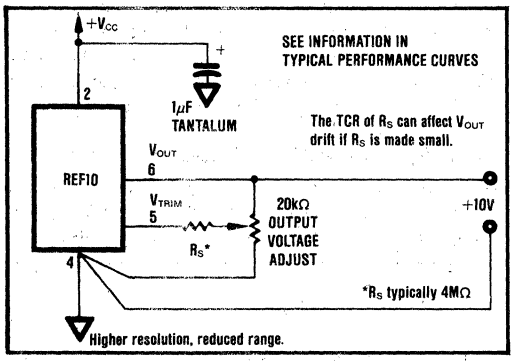


FIGURE 4. REF10 Optional Output Voltage Fine Adjust.

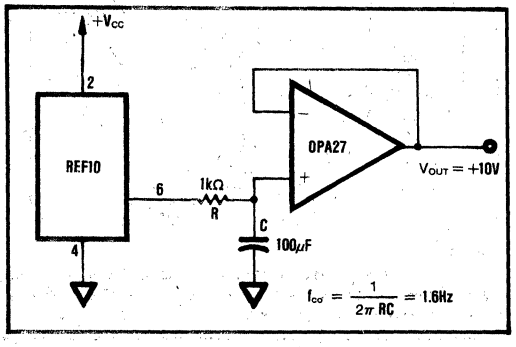


FIGURE 5. Precision Reference with Filtering.

APPLICATION INFORMATION

High accuracy, extremely-low drift, and small size make the REF10 ideal for demanding instrumentation and system voltage reference applications. Since no heater is required, low power supply current designs are readily achievable. Also the REF10 has lower output noise and much faster warm-up times than heated references, permitting high precision without extra power or additional supplies. It should be considered that operating any integrated circuit at an elevated temperature will reduce its MTTF.

A variety of application circuits are shown in Figures 5 through 11.

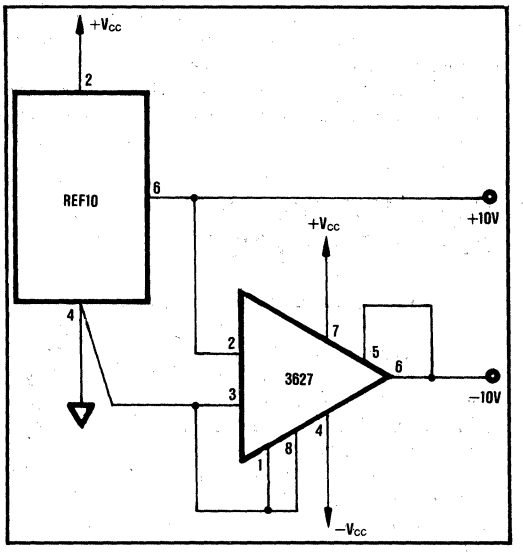


FIGURE 6. ±10V Reference.

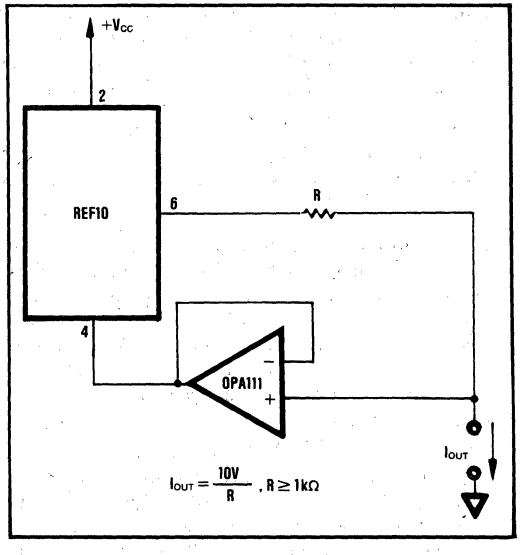


FIGURE 7. Positive Precision Current Source.

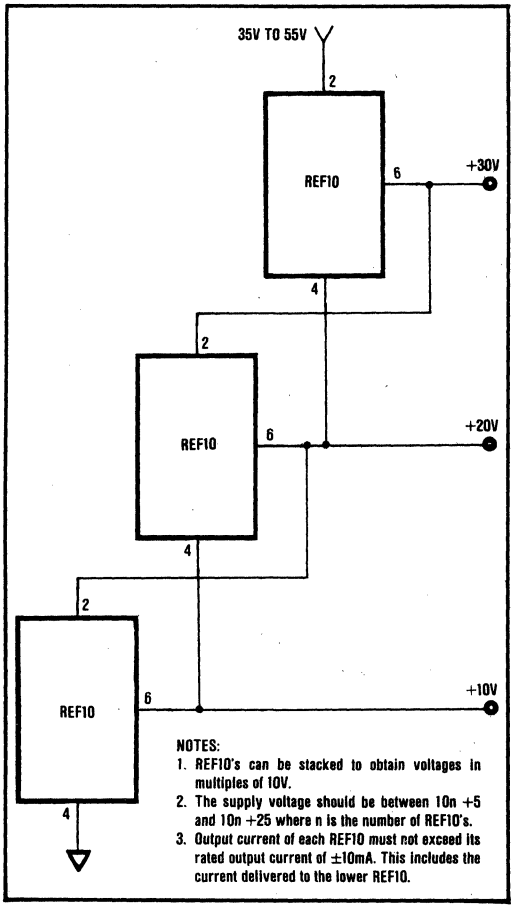


FIGURE 8. Stacked References.

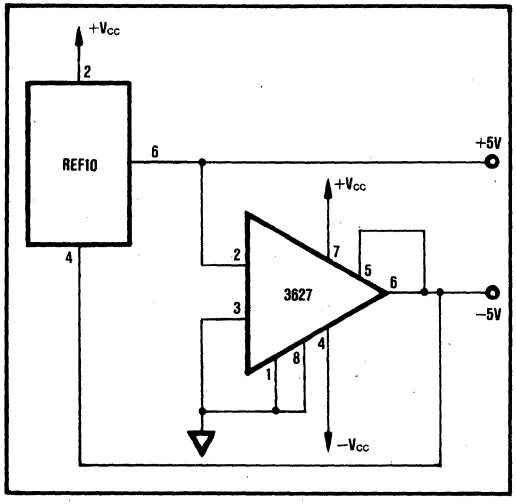


FIGURE 9. ±5V Reference.

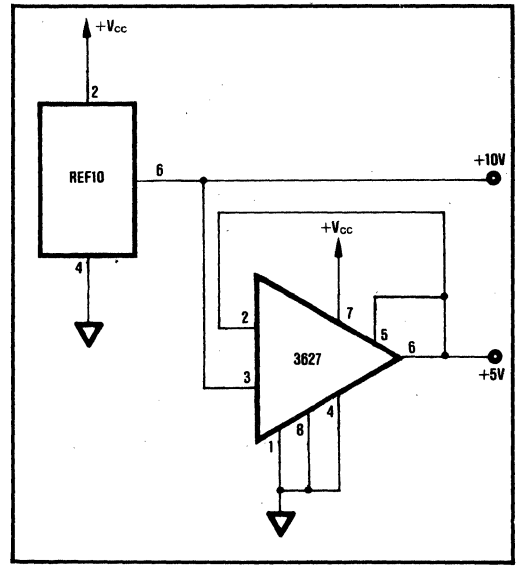


FIGURE 10. +5V and +10V Reference.

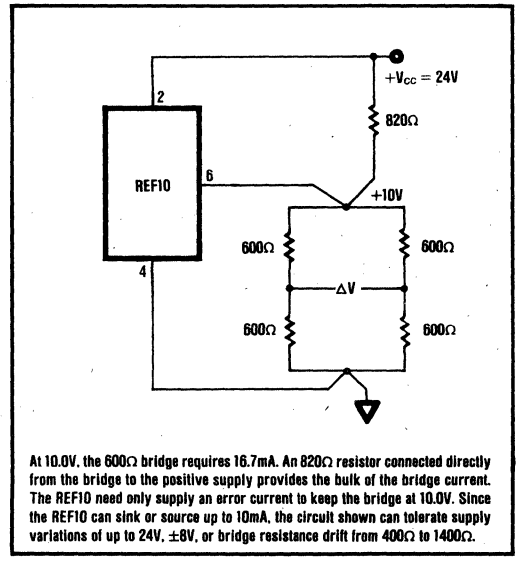
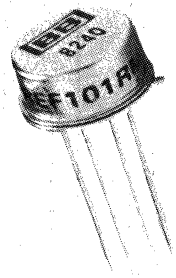


FIGURE 11. +10V Reference with Output Current Boost Using a Resistor to Drive a 600Ω Bridge.

BURR-BROWN®



REF101

Precision VOLTAGE REFERENCE

FEATURES

- +10.00V OUTPUT
- HIGH ACCURACY, ±0.005V
- VERY LOW DRIFT, 1ppm/°C max
- EXCELLENT STABILITY, 25ppm/1000hrs.
- LOW NOISE, 6μV, p-p typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE, up to 35V
- LOW QUIESCENT CURRENT, 6mA max
- USEFUL MATCHED RESISTOR PAIR INCLUDED

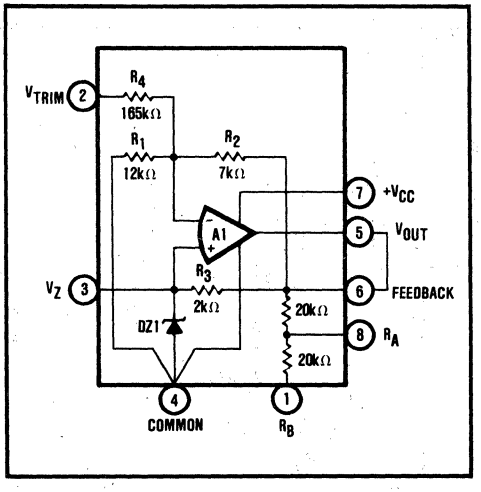
APPLICATIONS

- PRECISION CALIBRATED VOLTAGE STANDARD
- TRANSDUCER EXCITATION
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT

DESCRIPTION

The REF101 is a precision voltage reference which provides a +10.00V output. The drift is laser-trimmed to 1ppm/°C max (KM grade) over the full specification range. This is in contrast to some references which guarantee drift over a limited portion of their specification temperature range. The REF101 achieves its precision without a heater. This results in low quiescent current (4.5mA typ), fast warm-up (1msec to 0.1%), excellent stability (25ppm/1000hrs typ), and low noise (25μV, p-p max, 0.1Hz to 10Hz).

The output can be adjusted with minimal effect on drift or stability. Additionally, the REF101 contains a matched pair of user-accessible precision 20kΩ resistors which are useful in a variety of applications. Single supply operation over 13.5V to 35V supply range and excellent overall specifications make the REF101 an ideal choice for the most demanding applications such as precision system standards, D/A and A/D references, transducer excitation etc.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

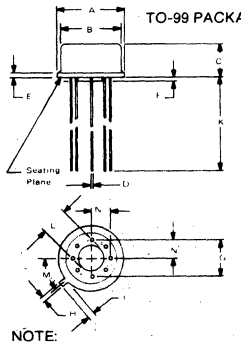
ELECTRICAL

At T_A = +25°C and +15VDC power supply unless otherwise noted.

PARAMETER	CONDITION	REF101JM/KM/RM/SM MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE					
Initial	T_A = +25°C	9.995	10.000	10.005	V
Trim Range(1)		-0.100		+0.250	V
vs Temperature(2)					
KM	0°C to +70°C			1	ppm/°C
JM	0°C to +70°C			2	ppm/°C
SM	-55°C to +125°C			3	ppm/°C
RM	-55°C to +125°C			6	ppm/°C
vs Supply (line regulation)	V_{CC} = 13.5 to 35V		0.00025	0.002	%/V
vs Output Current					
(load regulation)	I_L = 0 to ±10mA		0.00025(3)		%/mA
			0.001(4)	0.002(4)	%/mA
vs Time	T_A = +25°C		25		ppm/1000 hrs
NOISE	0.1Hz to 10Hz		6	25	µV p-p
OUTPUT CURRENT	Source or Sink	±10			mA
INPUT VOLTAGE RANGE		13.5		35	V
QUIESCENT CURRENT	I_{OUT} = 0		4.5	6	mA
WARM-UP TIME	To 0.1%		10		µsec
UNCOMMITTED RESISTORS					
Resistance			20		kΩ
Match			±0.01	±0.05	%
TCR			50		ppm/°C
TCR Tracking			2		ppm/°C
TEMPERATURE RANGE					
Specification					
JM, KM		0		+70	°C
RM, SM		-55		+125	°C
Operating					
JM, KM		-25		+85	°C
RM, SM		-55		+125	°C
Storage		-65		+125	°C

NOTES: (1) Trimming the offset voltage will affect the drift slightly. See Installation and Operating Instructions for details. (2) The "box method" is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (3) Sourcing current. (4) Sinking current.

MECHANICAL



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers not marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
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D	.016	.021	0.41	0.53
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F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

WEIGHT: 1 gram
ORDER: REF101JM, REF101KM
REF101RM, REF101SM

ORDERING INFORMATION

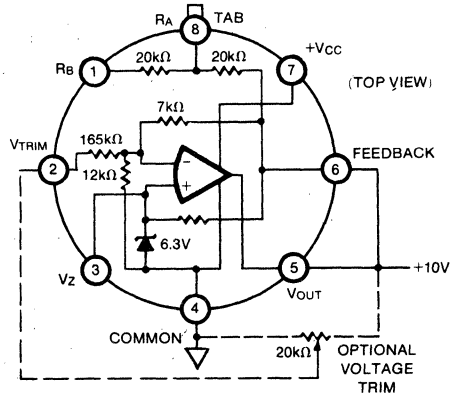
REF101 X M

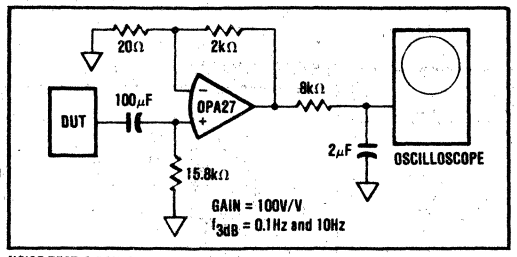
Basic Model Number
Performance Grade Code
J, K -25°C to +85°C
R, S -55°C to +125°C
Package Code
TO-99

ABSOLUTE MAXIMUM RATINGS

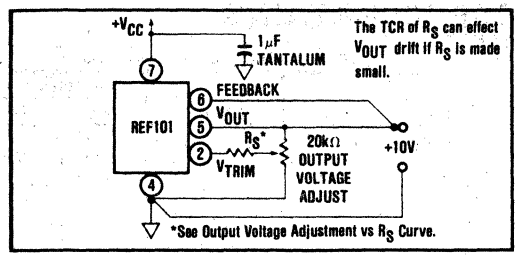
Input Voltage 40V
Power Dissipation at +25°C 200mW
Operating Temperature Range
REF101JM/KM ..... -25°C to +85°C
REF101RM/SM ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +125°C
Lead Temperature (soldering, 10sec) ..... +300°C
Short-Circuit Protection at +25°C
To Common or +15VDC ..... Continuous

PIN CONFIGURATION



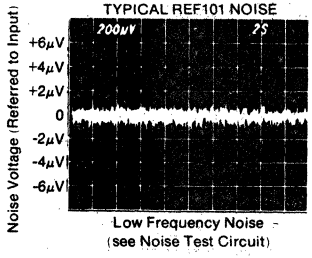


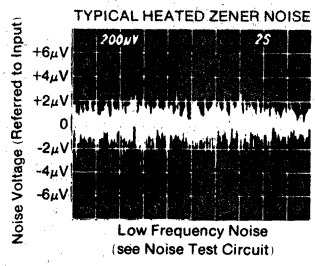
NOISE TEST CIRCUIT

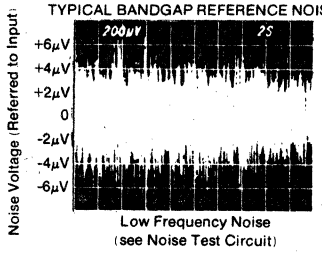


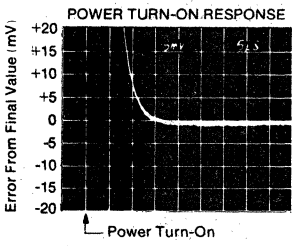
OPTIONAL OUTPUT VOLTAGE FINE ADJUSTMENT CIRCUIT.

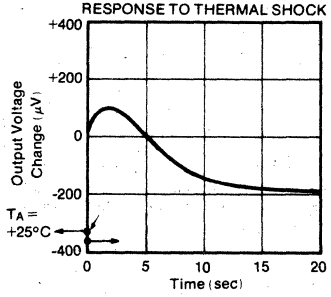
TYPICAL PERFORMANCE CURVES

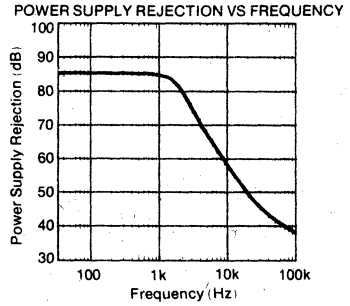


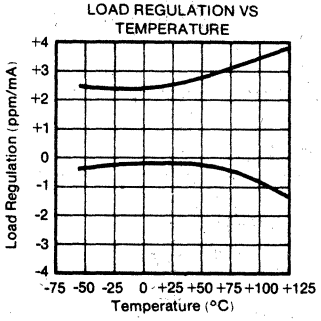


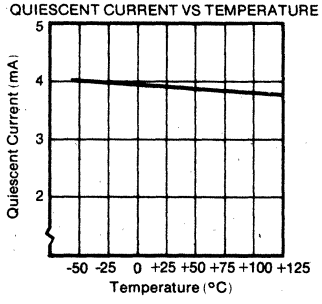


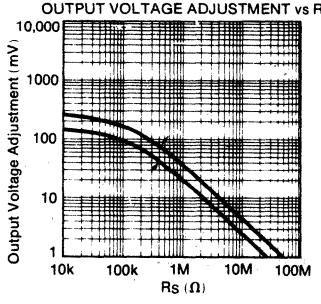


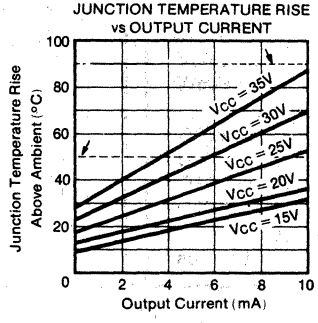












THEORY OF OPERATION

The following discussion refers to the diagram on the first page.

In operation, approximately 6.3V is applied to the noninverting input of op amp A_1 by zener diode DZ_1. This voltage is amplified by A_1 to produce the 10.00V output. The gain is determined by R_1 and R_2: $G = (R_1 + R_2)/R_1$. R_1 and R_2 are actively laser-trimmed to produce an exact 10.00V output. The zener operating current is derived from the regulated output voltage through R_3. This feedback arrangement provides closely regulated zener current. R_3 is actively laser-trimmed to set the zener current to a level which results in low drift at the output of A_1. The adjustment of output voltage and zener current is interactive and several iterations may be used to achieve the desired results. R_4 allows user-trimming of the output voltage by providing for a small external adjustment of amplifier gain. Since the TCR of R_4 closely matches the TCR of the gain setting resistors, the voltage trim has minimal effect on the drift of the reference.

DISCUSSION OF PERFORMANCE

The REF101 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry — the "butterfly method" and the "box method". Neither of these methods is entirely satisfactory in cases where the drift versus temperature is relatively nonlinear as is the case with most voltage references. The REF101 is specified with the more commonly used box method. The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

For the REF101 each J and K unit is tested at temperatures of 0°C, +25°C, +50°C, and +70°C and each R and S unit is tested at -55°C, -25°C, 0°C, +25°C, +50°C, +75°C, +100°C and +125°C. The minimum and maximum test voltages must meet this condition.

$$\left[\frac{(V_{OUT\ max} - V_{OUT\ min}) / 10V}{T_{high} - T_{low}}\right] \times 10^6 \leq \text{drift specification}$$

This assures the user that the variations of output voltage that occur as the temperature changes within the specification range T_{low} to T_{high} will be contained within a box whose diagonal has a slope equal to the maximum specified drift. Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{Upper\ Bound}$ and $V_{Lower\ Bound}$ (see Figure 1).

Figure 1 uses the REF101KM as an example. It has a drift specification of 1ppm/°C maximum and a specification temperature range of 0°C to +70°C. The "box" height (V_1 to V_2) is 700μV and upper bound and lower bound voltages are a maximum of 700μV away from the voltage at +25°C.

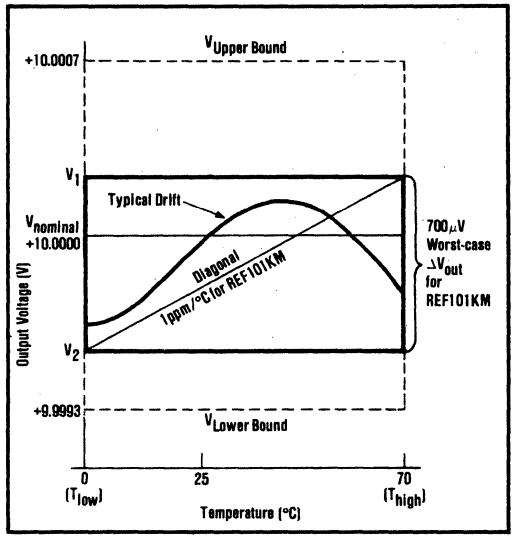
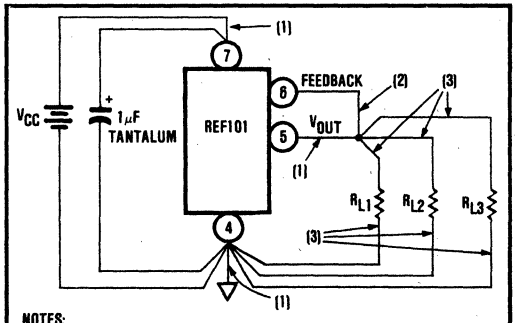


FIGURE 1. REF101KM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF101. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.



NOTES:
1. Lead resistances here of up to a few ohms have negligible effect on performance.
2. A relatively constant current of approx. 2mA at 50ppm/°C flows in this lead. 1Ω in this lead would introduce about 2mV error (adjustable to zero) with about 0.1ppm/°C drift at the output.
3. A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF101 Basic Circuit Connection.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.01ppm/°C per mV of trimmed voltage. In the circuit in Figure 3 any mismatch in TCR between the two sections of the potentiometer will also affect drift but the effect of the ΔTCR is reduced by a factor of 40 by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a range of approximately +250mV to -100mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 165kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

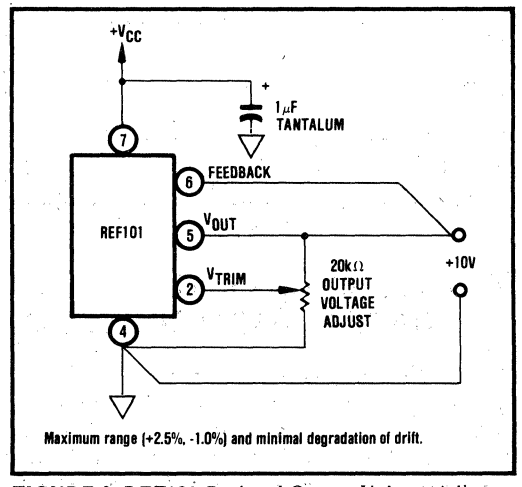


FIGURE 3. REF101 Optional Output Voltage Adjust.

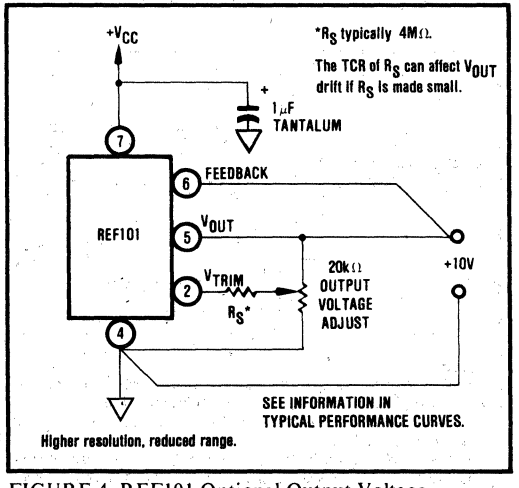


FIGURE 4. REF101 Optional Output Voltage Fine Adjust.

APPLICATION INFORMATION

High accuracy, extremely-low drift, and small size make the REF101 ideal for demanding instrumentation and system voltage reference applications. Since no heater is required, low power supply current designs are readily achievable. Also the REF101 has lower output noise and much faster warm-up times (1msec to 0.1%) than heated references, permitting high precision without extra power from additional supplies. It should be considered that operating any integrated circuit at an elevated temperature will reduce its MTTF.

A variety of application circuits are shown in Figures 5 through 19.

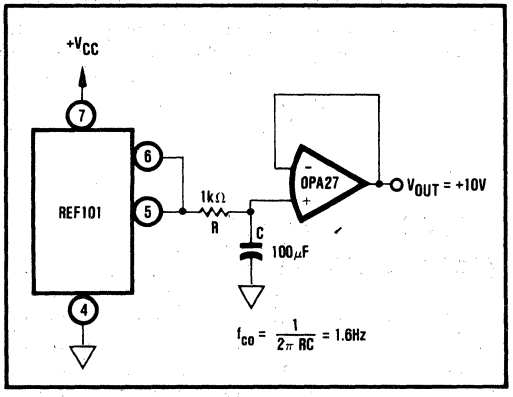


FIGURE 5. Precision Reference with Filtering.

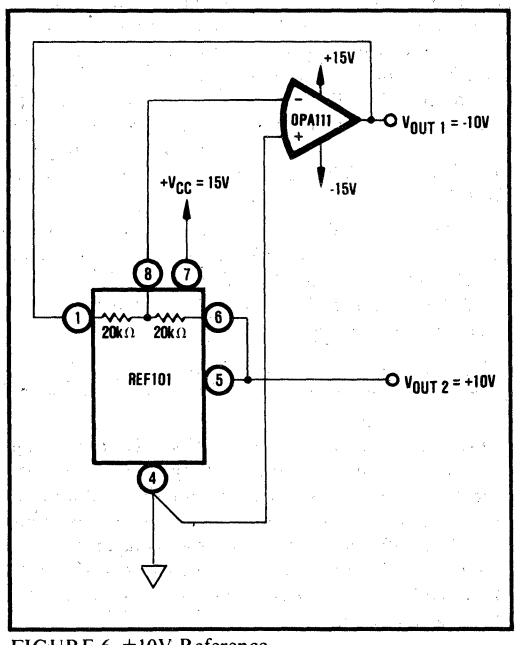


FIGURE 6. ±10V Reference.

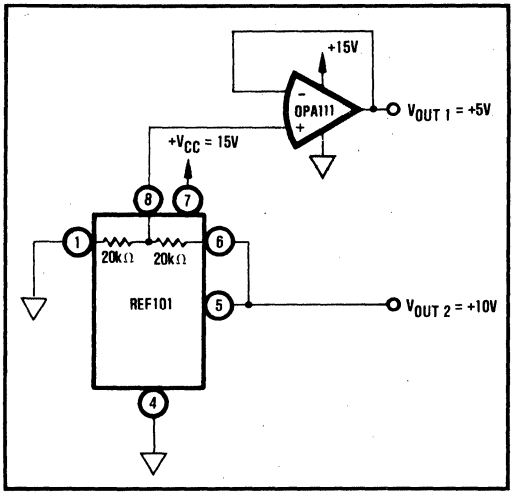


FIGURE 7. +10V and +5V Reference.

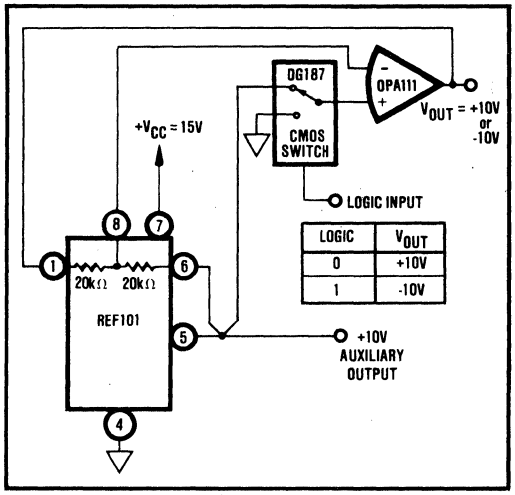


FIGURE 9. Digitally-Controlled Bipolar Precision Reference.

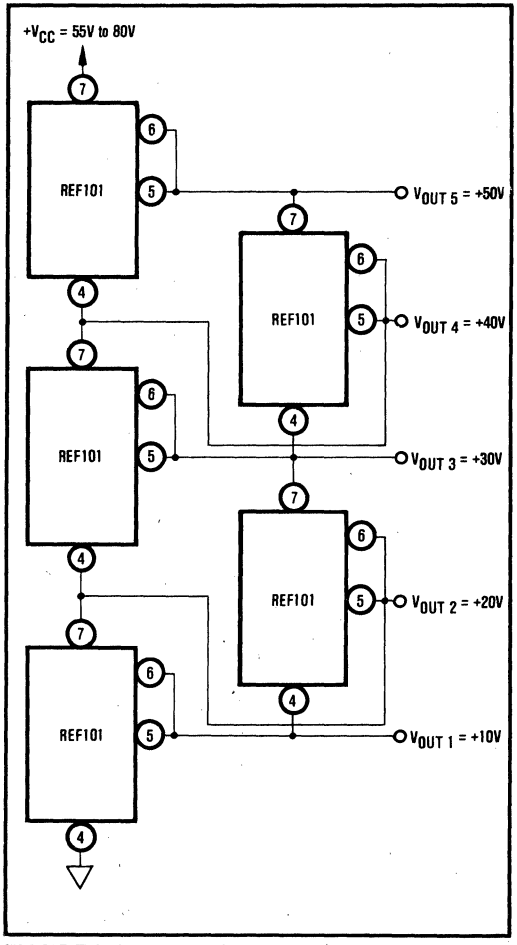


FIGURE 8. Stacked References.

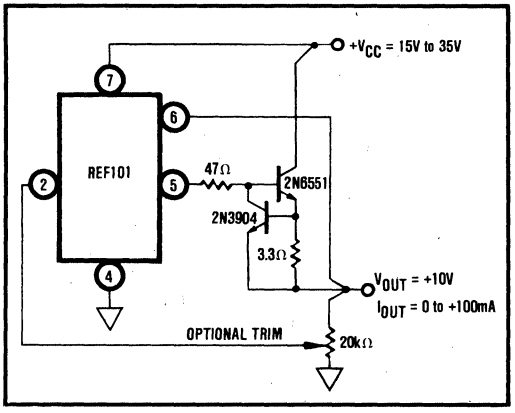


FIGURE 10. +10V Reference with Boosted Output Current to 100mA.

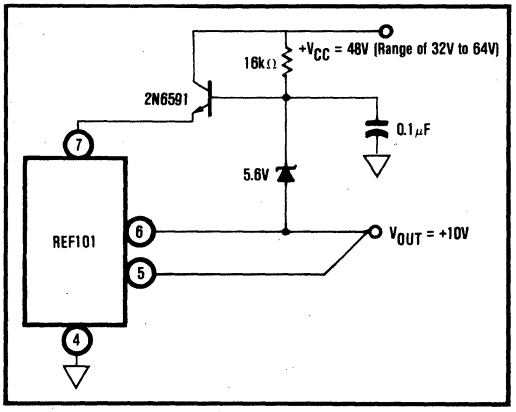


FIGURE 11. +10V Reference with Input Voltage Boost for 48V Operation.

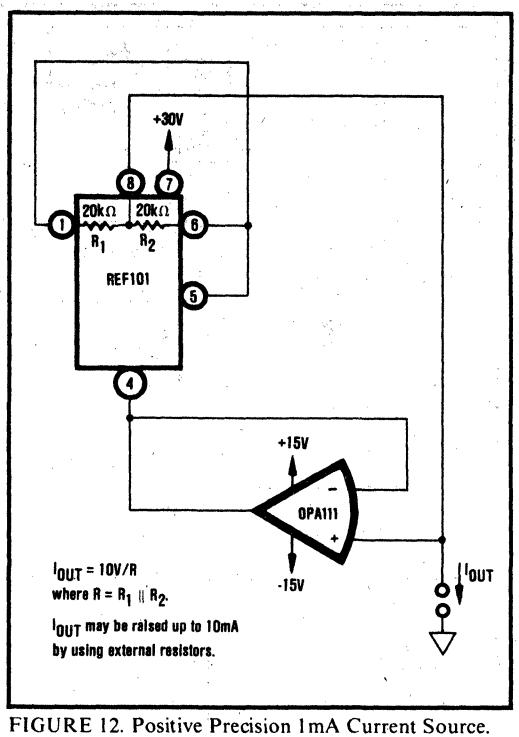


FIGURE 12. Positive Precision 1mA Current Source.

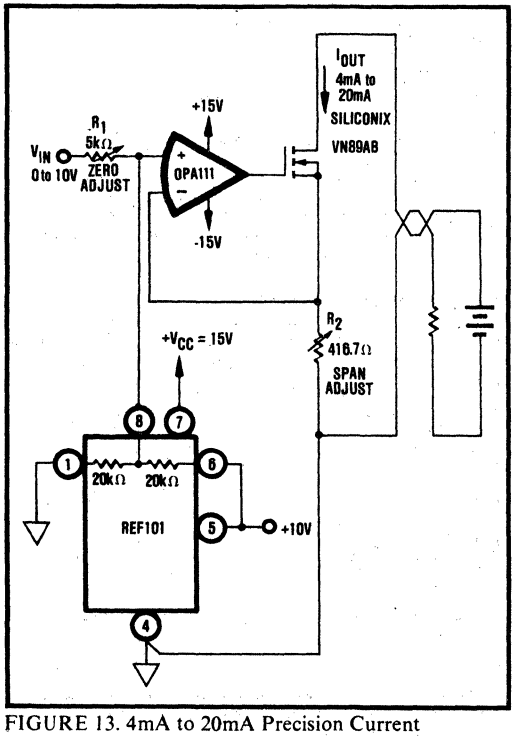


FIGURE 13. 4mA to 20mA Precision Current Transmitter.

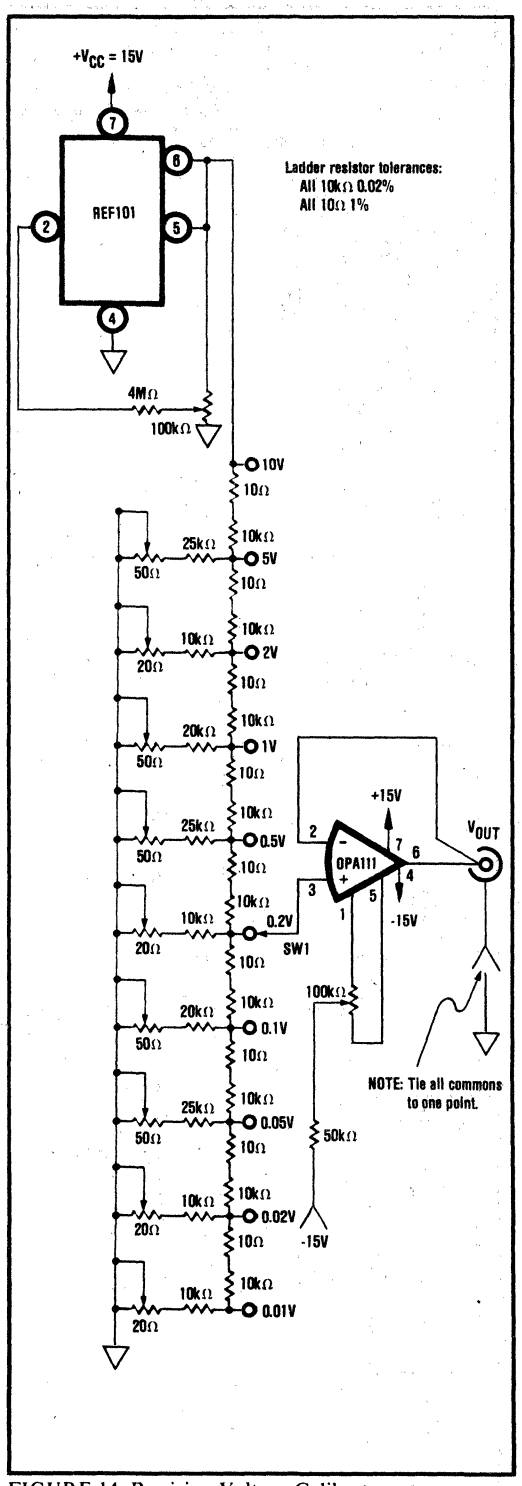


FIGURE 14. Precision Voltage Calibrator.

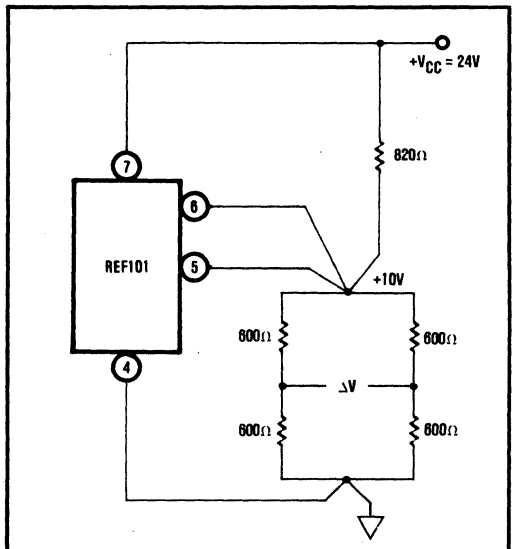


FIGURE 15. +10V Reference with Output Current Boost Using a Resistor to Drive a 600Ω Bridge.

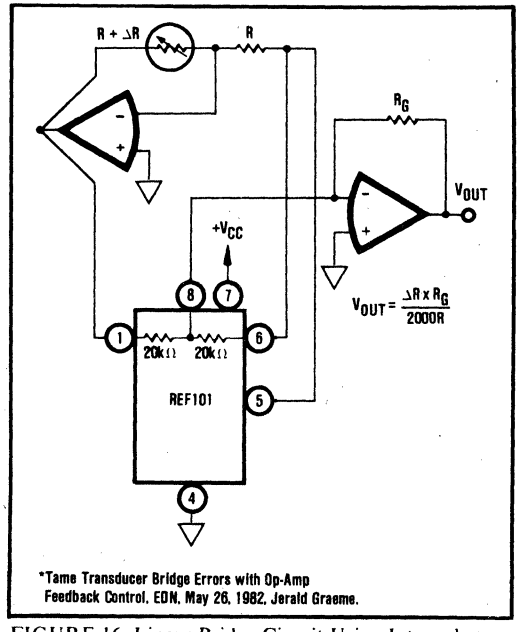


FIGURE 16. Linear Bridge Circuit Using Internal Precision Resistors of the REF101 as the Bridge Completion Network.

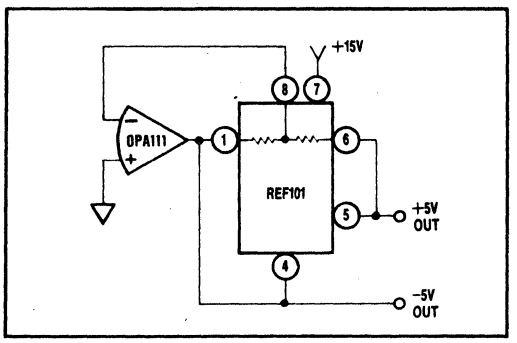


FIGURE 17. ±5V Reference.

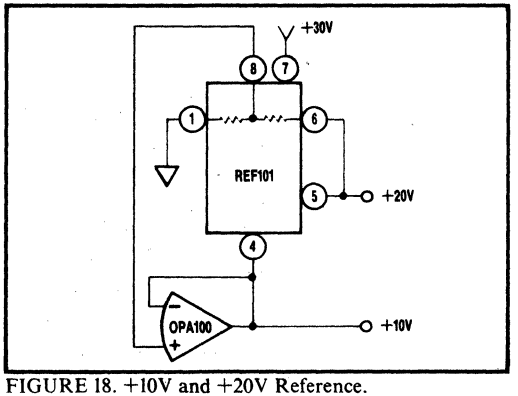


FIGURE 18. +10V and +20V Reference.

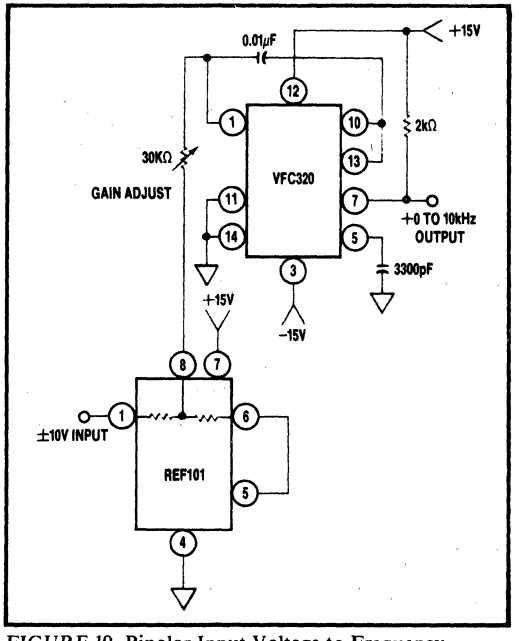
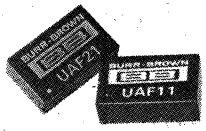


FIGURE 19. Bipolar Input Voltage to Frequency Converter.

BURR-BROWN®



UAF11
UAF21

UNIVERSAL ACTIVE FILTERS

FEATURES

- **SAVES DESIGN TIME**
  - User-tuneable frequency, Q-factor, gain
  - Calculate only three resistance values
  - Design directly from this data sheet
  - Completely characterized parameters
- **IMPROVED PERFORMANCE**
  - Wide frequency ranges
  - UAF11 - 0.001Hz to 20kHz
  - UAF21 - 0.001Hz to 200kHz
  - 1% frequency accuracy
  - Q range of 0.5 to 500
  - Reliable hybrid construction
  - NPO capacitors and thin-film resistors

APPLICATIONS

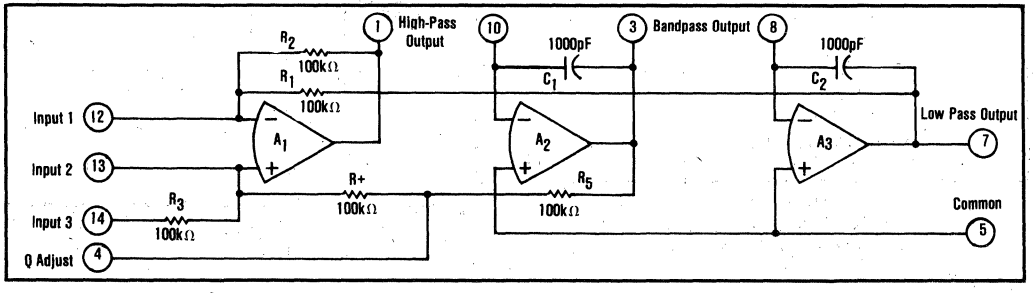
- **FILTER CONFIGURATIONS**
  - Butterworth
  - Bessel
  - Chebyschev
- **FILTER FUNCTIONS**
  - Low pass
  - High pass
  - Bandpass
  - Band reject

DESCRIPTION

The UAF11's and UAF21's are low cost universal active filters. These versatile units can easily be tailored to any active filter application using the extensive information provided in this data sheet. UAF's are excellent choices for use in communications equipment, test equipment (engine analyzers, aircraft and automotive test, medical test, etc.), servo systems, process control equipment, sonar and many others.

The UAF11's and UAF21's are complete two-pole active filters with the addition of four external resistors that provide the user easy control of the Q-factor, resonant frequency and gain. Any complex filter response can be obtained by cascading these units. Three separate outputs provide low-pass, high-pass, and bandpass transfer functions. A band-reject (notch) transfer function may be realized simply by summing the high-pass and low-pass outputs.

Since these UAF's are so versatile and flexible, they can be stocked by the user in quantity for use as building blocks whenever the requirement arises. This means instant availability and the UAF purchases may be made in volume to take advantage of quantity price discounts.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

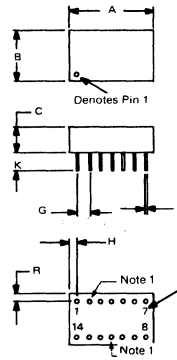
Typical at +25°C and with rated supply unless otherwise noted.

MODEL	UAF11	UAF21(1)	UNITS
INPUT			
Input Bias Current	±100	±15	nA
Input Voltage Range	±10	±10	V
Input Resistance	100k	100k	Ω
TRANSFER CHARACTERISTICS			
Frequency Range (f_o)	0.001 to 20k	0.001 to 200k	Hz
f_o Accuracy(2)	±1	±1	%
f_o Stability(3) (over temp. range)	±0.005	±0.005	%/°C
Q Range(4)	0.5 to 500	0.5 to 500	--
Q Stability(5)			
at f_o Q ≤ 10^4	±0.025	±0.01	%/°C
at f_o Q ≤ 10^5	±0.1	±0.025	%/°C
Gain Range	0.1 to 50	0.1 to 50	--
OUTPUT			
Slew Rate	0.6	6.0	V/μsec
Peak-to-Peak Output Swing(6)			
f_o ≤ 10kHz	20	20	V
f_o ≤ 20kHz	10	20	V
f_o ≤ 100kHz	2	20	V
Output Offset (at low-pass output with unity gain)	±10	±10	mV
Output Impedance	2	10	Ω
Noise(7)	200	200	μV, rms
Output Current(8)	10	10	mA
POWER SUPPLIES			
Rated Power Supplies	±15	±15	V
Power Supply Range(9)	±5 to ±18	±5 to ±18	V
Supply Current at ±15V (Quiescent)	±12, max	±12, max	mA
TEMPERATURE RANGE			
Specification: Epoxy	−25 to +85	−25 to +85	°C
Storage: Epoxy	−40 to +85	−40 to +85	°C

MECHANICAL

EPOXY PACKAGE

NOTE:
Leads in true position within 0.10" 0.25mm R at MMC at seating plane.



ORDER NUMBER:
UAF11
UAF21
WEIGHT: 3.4 Grams
CONNECTOR:
0145MC

Pin numbers shown for reference only. Numbers may not be marked on package.

Note 1: Pin presence optional

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

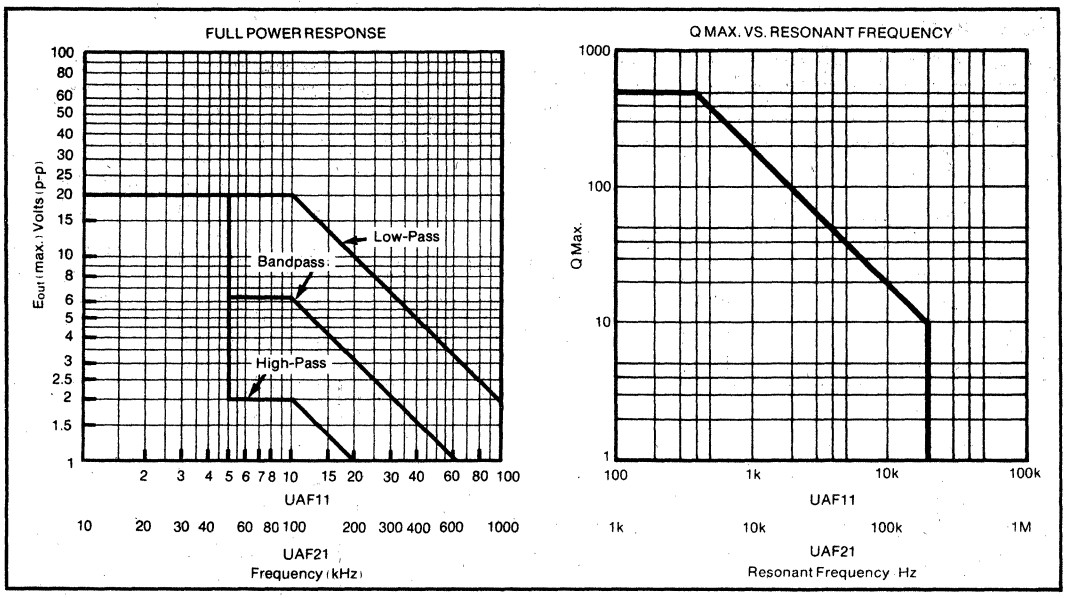
NOTES

1. The UAF21 includes two internal 0.002μF power supply capacitors.
2. Repeatibility of f_o using 0.1% frequency determining resistors.
3. T.C.R. of external frequency determining resistors must be added to this figure.
4. Derated 50% from maximum - see Typical Performance Curves.
5. Q stability varies with both the value of Q and the resonant frequency f_o.
6. Low-pass output - see Typical Performance Curves.
7. Measured at the bandpass output with Q = 50 over DC to 50kHz.
8. The current required to drive R_{F1} and R_{F2} (external) as well as C_1 and C_2 must come from this current.
9. For supplies below ±10V, Q max will decrease slightly; filters will operate below ±5V.

PIN CONNECTIONS

Pin 1. High-Pass Output
Pin 2. Optional Pin
Pin 3. Bandpass Output
Pin 4. Q Adjust Point
Pin 5. Common
Pin 6. +Supply
Pin 7. Low-Pass Output
Pin 8. Frequency Adjust
Pin 9. -Supply
Pin 10. Frequency Adjust
Pin 11. Optional Pin
Pin 12. Input 1
Pin 13. Input 2
Pin 14. Input 3

TYPICAL PERFORMANCE CURVES



APPLICATIONS INFORMATION

TRANSFER FUNCTION

The UAF21 uses the state variable technique to produce a basic second order transfer function. The equation describing the three outputs available are:

$$T(\text{Low-Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{Bandpass}) = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{High-Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $\omega_o = 2\pi f_o$.

To obtain band reject characteristics the low-pass and high-pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band-Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $A_{LP} = A_{HP} = A$.

The state variable approach uses two op amp integrators and a summing amplifier to provide simultaneous low-pass, bandpass and high-pass responses. One UAF is required for each two poles of low-pass or high-pass filters and for each pole-pair of bandpass or band-reject filters.

DESIGN PROCEDURE SUMMARY

These procedures give the design steps for the proper application of a UAF and for the selection of the external components. More detailed information on filter theory pertinent to some of the steps can be found in the reference sources listed in Table I.

TABLE I. Useful References.

1. Tobey, Gene, et al, Operational Amplifiers: Design and Applications, Chapter 8, McGraw-Hill Book Company, 1971.
2. Wong, Yu Jen, and William Ott: Function Circuits: Design and Applications, Chapter 6, McGraw-Hill Book Company, 1976.
3. Daniels, Richard W.: Approximation Methods for Electronic Filter Design, McGraw-Hill Book Company, 1974.
4. Zyerev, Anatol I.: Handbook of Filter Synthesis, John Wiley and Sons, 1967.
5. Temes, Gabor C., and Sanjit K. Mitra: Modern Filter Theory and Design, John Wiley and Sons, 1973.

Burr-Brown also manufactures a line of completely self-contained active filters called the ATF76 series. These are available in most popular transfer functions with from 2- to 8-pole responses. They contain all necessary components and do not require any user design effort.

DESIGN STEPS

1. Choose the type of function (low-pass, bandpass, etc.), type of response (Butterworth, Bessel, etc.), number of poles, and cutoff frequency based on the particular application.

   If the transfer function is band-reject see Band-Reject Transfer Function before proceeding to step 2.
2. Determine the normalized low-pass filter parameters (f_n and Q) based on the type of response and number of poles selected in step 1. See Normalized Low-Pass Parameters.
3. If the actual response desired is low-pass go to step 4. For other responses a transformation of variables must be made (low-pass to bandpass or low-pass to high-pass). See Low-Pass Transformation.

4. Determine the actual (denormalized) cutoff frequency, f_o, by multiplying f_n by the actual desired cutoff frequency. See Denormalization of Parameters.
5. Pick the desired UAF configuration (noninverting, inverting or bi-quad). See Configuration Selection Guide and UAF Configurations and Design Equations.
6. Decide whether to use design equations "A" or "B". See Design Equations "A" and "B".
7. Calculate R_{F1} and R_{F2}. See Natural Frequency and UAF Configurations and Design Equations.
8. Determine Q_P. See Q_P Procedure.
9. Select the desired gain for each UAF and calculate the corresponding R_G and R_Q. See Gain (A) and UAF Configurations and Design Equations.

BAND-REJECT TRANSFER FUNCTION

The band-reject is achieved by summing the high-pass and low-pass UAF outputs. Either of the configurations in Figures 2 and 3 can be used to provide the band-reject function if they are used as shown in Figure 1.

The 15kΩ resistor is adjusted for maximum rejection. The circuit in Figure 3 is applicable when using design equations "A" ($A_{LP} = A_{HP}$). When design equations "B" are used ($A_{LP} = 10A_{HP}$), the resistor at pin 7 must be 10 times the resistor at pin 1 to obtain equal pass-band gains above and below f_n.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_o and Q of the band-reject filter desired and for A_{LP} to equal the desired pass-band gain. An input constraint is that the input voltage times A_{BP} must not exceed the rated peak-to-peak voltage of the bandpass output, or clipping will result.

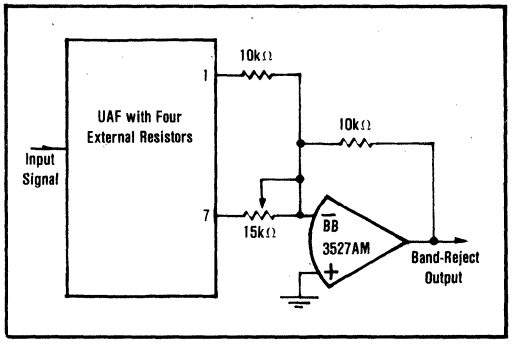


FIGURE 1. Band-Reject Configuration.

NORMALIZED LOW-PASS PARAMETERS

Usual active filter design procedure involves using normalized low-pass parameters. Table II is provided to assist in this step for the more common filter responses. Table III is a FORTRAN program which allows f_n and Q to be calculated for any desired ripple and number of poles for the Chebyschev response. Program inputs are the number of poles (N) and the peak-to-peak ripple (R). Program outputs are f_n and Q, which are used exactly as the values taken from Table II.

TABLE II. Low-Pass Filter Parameters.

Number	Butterworth		Bessel		Chebysev			
					0.5 dB Ripple		2 dB Ripple	
of Poles	f_n(1)	Q	f_n(1)	Q	f_n(2)	Q	f_n(2)	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	--	1.32475	--	0.626456	--	0.368911	--
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	--	1.50470	--	0.362320	--	0.218308	--
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982628	10.4616
7	1.0	--	1.68713	--	0.256170	--	0.155410	--
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67658	0.237699	0.89236
	1.0	0.60134	1.85314	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5308	0.990142	18.6873

1. -3dB frequency.
2. Frequency at which amplitude response passes through the ripple band.

TABLE III. Low-Pass Chebyschev Program.

```
      PI=3.1415926536
      COMPLEX P(10)
      READ 5, N, R
    5 FORMAT (I2,F8.6)
      A=SQRT(EXP(R/4.3429448))+1.)
      B=1./A
      AN=ALOG(B+SQRT(B**2-1.))
      AN=AN/FLOAT(N)
      J=MOD(N, 2)+N/2
      DO 10 K=1, J
      RP=-SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT(2*N))
      XIP=COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
      WN=SQRT(RP**2+XIP**2)
      Q=-WN/(2*RP)
      P(K)=CMPLX(WN,Q)
      IF(MOD(N,2).NE.0.AND.K.EQ.J)GO TO 15
      PRINT 20, P(K)
      GO TO 10
   15 F=REAL(P(K))
      PRINT 30, F
   10 CONTINUE
   20 FORMAT (2X"FN="E20.8"Q="E20.8)
   30 FORMAT (2X"FN = "E20.8)
      STOP
      END
```

NOTE: Language variations between computers may require modification of this program.

Note that for bandpass and high-pass filters complex conjugate pole pairs in the actual filter correspond to single poles in the normalized low-pass model. Thus four poles in Table II would correspond to four-pole pairs in a bandpass or high-pass filter.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents a simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. An external op amp and RC network can be used for this purpose.

The cutoff frequency determined by the Table II filter parameters is (1) the -3dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band (to enter the stop band).

LOW-PASS TRANSFORMATION

Low-Pass to High-Pass

The following simple transformation may be used for high-pass filters:

$$f_n \text{ (high-pass)} = \frac{1}{f_n \text{ (low-pass)}}$$

$$Q \text{ (high-pass)} = Q \text{ (low-pass)}$$

Low-Pass to Bandpass

The low-pass to bandpass transformation to generate f_n (bandpass) and Q (bandpass) is much more complicated. It is tedious to do by hand but can be accomplished with the FORTRAN program given in Table IV. This program automates the tranformation

$$s = p/2 \pm \sqrt{(p/2)^2 - 1}.$$

TABLE IV. Low-Pass to Bandpass Transformation Program.

```
      COMPLEX P,S,U
      READ 5, FN, Q, QBP
    5 FORMAT (3F12.5)
      Y=FN*SQRT(1.-1(./(Q*2.))**2)
      X=-FN/Q*2.)
      P=CMPLX(X,Y)
      U=CONJG(P)
      DO 30 I=1,2
      S=P/(2*QBP)
      P=S**2-1.
      T=ATAN2(AIMAG(P),REAL(P))
      IF (T.GE.0.)GO TO 10
      T=2.*3.14159+T
   10 T=T/2.
      A=SQRT(CABS(P))*COS(T)
      B=SQRT(CABS(P))*SIN(T)
      S=S+CMPLX(A,B)
      FN=CABS(S)
      Q=-FN/(2.*REAL(S))
      PRINT 20,FN,Q
   20 FORMAT (2X"FN="F12.5"Q="F12.5)
      IF(AIMAG(U).EQ.0.)GO TO 40
   30 P=U
   40 STOP
      END
```

NOTE: Language variations between computers may require modification of this program.

Program Inputs

1. f_n - From Table II for the low-pass filter of interest
2. Q - From Table II
3. Q_{BP} - Desired Q of the bandpass filter

For filters with an odd number of poles a Q of 0.5 should be used where Q is not given in Table II. Enter 10^5 for Q when transforming zeros on the imaginary axis.

The program transforms each low-pass pole into a bandpass pole pair. Thus a three-pole low-pass input, would result in the pole positions for a three-pole pair bandpass filter requiring three UAF stages.

DENORMALIZATION OF PARAMETERS

Table II shows filter parameters for many 2- to 8-pole normalized low-pass filters. The Q and the normalized undamped natural frequency, f_n for each two-pole section are shown. The Q values do not have to be denormalized and may be used directly as described in the Design Procedure Summary. f_n must be denormalized by multiplying it by the desired cutoff frequency of the actual overall filter to obtain the required frequency, f_o for the design formulas. As an example, consider a 4-pole low-pass Bessel filter with a cutoff frequency of 1000Hz. The first stage would be designed to an f_o of 1432.41Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94Hz and Q of 0.80554. To combine the two stages into the composite filter the low-pass output of the first stage (pin 9) would be connected to the input resistors (R_G) of the second stage.

CONFIGURATION SELECTION GUIDE

It is possible to configure the UAF three different ways. Each configuration produces features that may or may not be desirable for a specific application. The selection guide in Table V is given to assist in determining the most advantageous configuration for a particular application.

UAF CONFIGURATIONS AND DESIGN EQUATIONS

Noninverting Configuration

For applications requiring a bandpass gain of 1V/V, the internal resistor R_F may be used (input at pin 14) as the gain resistor R_G; thus, only three external resistors are needed to configure the filter.

To use equations "B" connect an 11kΩ resistor between pins 12 and 1. Use equations "B" for frequencies above 8kHz or when R_Q from equations "A" becomes a negative value.

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 10^4\ \omega_o = 1.59 \times 10^8\ f_o$
2. $A_{BP} = QA_{LP} = QA_{HP}$
3. $R_Q = 10^5\ (2Q_P - A_{BP} - 1)$
4. $R_G = (2Q_P - A_{BP} + 1)\ 10^5\ A_{BP}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^8\ \omega_o = 5.03 \times 10^7\ f_o$
2. $A_{BP} = Q\ 3.16\ A_{LP} = 3.16Q\ A_{HP}$
3. $R_Q = 10^5\ (3.48Q_P - A_{BP} - 1)$
4. $R_G = (3.48Q_P - A_{BP} + 1)\ 10^5\ A_{BP}$

Inverting Configuration

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 10^4\ \omega_o = 1.59 \times 10^8\ f_o$
2. $A_{BP} = Q\ A_{LP} = Q\ A_{HP}$
3. $R_G = 10^4\ Q_P\ A_{BP}$
4. $R_Q = 2 \times 10^5\ (2Q_P + A_{BP} - 1)$

	NONINVERTING INPUT	INVERTING INPUT	BI-QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Inverted Outputs	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant bandwidth
Other Advantages	May be used with only three external resistors (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies
Parameter Limitations	$2Q_P - A_{BP} > 1$ ($f_o < 8kHz$) $3.48Q_P - A_{BP} > 1$ ($f_o > 8kHz$)	$2Q_P + A_{BP} > 1$ ($f_o < 8kHz$) $3.48Q_P + A_{BP} > 1$ ($f_o > 8kHz$)	None

Summary: The Bi-Quad filter is particularly useful as a bandpass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a bandpass or maintaining constant response of a low-pass or high-pass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than R_G and R_Q of the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 100k\Omega$; therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q).

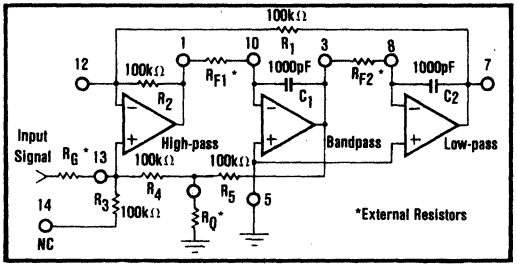


FIGURE 2. Noninverting Configuration.

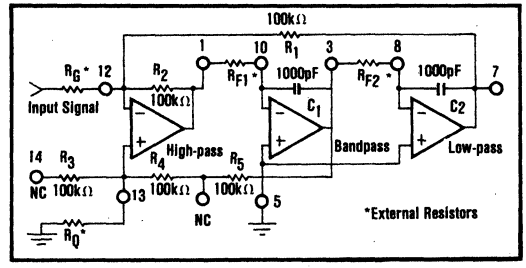


FIGURE 3. Inverting Configuration.

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or $50kHz$ (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^4\ \omega_o = 5.03 \times 10^7\ f_o$
2. $A_{BP} = Q_P/3.16 = 3.16Q_P A_{HP}$
3. $R_G = 3.16 \times 10^4\ Q_P\ A_{BP}$
4. $R_Q = 2 \times 10^5\ (3.48Q_P + A_{BP} - 1)$

Bi-QUAD Configuration

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5kHz$ (UAF11) or $50kHz$ (UAF21)

1. $R_{F1} = R_{F2} = 10^4\ \omega_o = 1.59 \times 10^4\ f_o$
2. $Q\ A_{LP} = A_{BP}$
3. $R_Q = Q_P R_{F1}$
4. $R_G = R_Q\ A_{BP}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or $50kHz$ (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^4\ \omega_o = 5.03 \times 10^7\ f_o$
2. $Q\ A_{LP} = A_{BP}$
3. $R_Q = 3.16\ Q_P\ R_{F1}$
4. $R_G = R_Q\ A_{BP}$

Design Equations "A" and "B"

1. For f_o below 8kHz, either of equations "A" or "B" may be used.
2. For f_o above 8kHz, equations "B" must be used. If equations "A" were used above 8kHz, the filter could become unstable.
3. Equations "A" are for the UAF as it is supplied. When using equations "B", a 11kΩ resistor must be placed in parallel with R_2 (between pins 12 and 1).

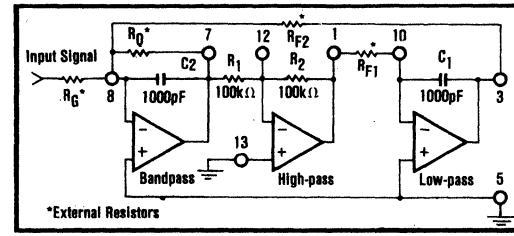


FIGURE 4. Bi-Quad Configuration.

4. The values of R_{F1} and R_{F2} calculated with equations "B" are approximately one-third of those calculated with equations "A". Thus there may be an advantage in using equations "B" at low frequencies. Using equations "B" would require use of one more resistor, but that would not alter or affect filter performance in any manner.
5. Using the negative gain values for A_{LP} or A_{HP} or A_{BP} could result in the negative values for resistors R_G and R_Q. So the absolute value of the gain should always be used in the equations.
6. Under some circumstances the value of R_Q using equations "A" will be negative. If this occurs, use design equations "B".

Natural Frequency (f_o)

1. f_o for each one pole-pair bandpass filter is the center frequency (f_C). f_C is defined as $f_C = \sqrt{f_1 f_2}$ where f_1 is the lower -3dB point and f_2 is the upper -3dB point of the pole-pair response.

2. To obtain f_o below 100Hz using practical resistor values, capacitors may be paralleled with C1 and C2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}\ (new) = R_{F2}\ (new) = R_{F1}\ (old)\ \frac{1000pF}{C + 1000pF}$$

where R_F (new) is the new lower value frequency resistor, C is the value of the two external capacitors placed across C1 and C2 (between pins 10 and 3 and pins 8 and 7 and R_{F1} (old) is the value calculated in the simplified design equations.

Q-Factor

$$\frac{f_o}{3dB\ bandwidth}$$

1. For bandpass filters Q =
2. When designing low-pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.

Qp Procedure

1. If the "f_o times Q" product is greater than 10^4 (or 10^5 for the UAF21), it is possible for the measured filter Q to be different from the calculated value of Q. This effect is the result of nonideal characteristics of operational amplifiers. It can be compensated for by introducing the parameter Q_P into the design equations.
2. Calculate the f_o Q product for the filter. If the product is above 10^4Hz (or 10^5 for the UAF21), locate the corresponding f_oQ_P product on the curve in Figure 5. Divide f_oQ_P by f_o to obtain Q_P. Use Q_P as indicated in the design equations. For f_oQ products below 10^4Hz (or 10^5 for the UAF21), $Q_P = Q$.

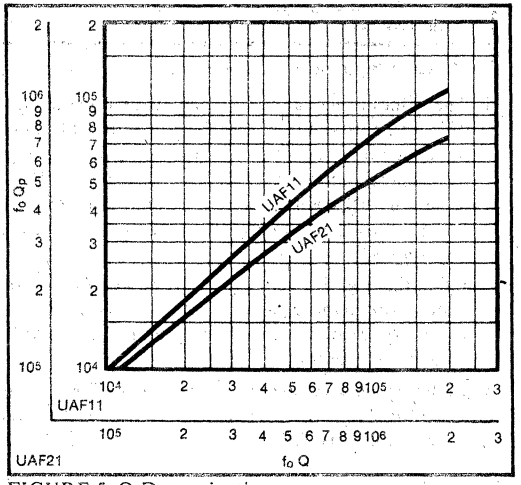


FIGURE 5. Q_P Determination.

Gain (A)

1. The gain (V/V) of each filter section is:
   A_{LP} - for low-pass output - gain at DC
   A_{BP} - for bandpass output - gain at f_o
   A_{HP} - for high-pass output - gain at high frequencies.
2. Refer to the Typical Performance Curves for full power response. When selecting the gain, insure the limits of the curve are not exceeded for the desired voltage range.

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF filter components. They are not required for the regular design procedure but could be used if a detailed analysis is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = R_2 / (R_1 R_{11} C_1 R_{12} C_2)$
2. $Q = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{R_1 \| R_3}{R_1 + R_3}\right) (1 + 10^5 R_O) \sqrt{\frac{R_2 R_{11} C_1}{R_1 R_{11} C}}$
3. $R_1 = 10^5 + 10^5 R_O / (10^5 + R_O)$
4. $Q\ A_{LP} = Q\ A_{HP}\ R_1 / R_2 = A_{BP} \sqrt{R_1 R_{11} C_1 / (R_2 R_{11} C_1)}$
5. $A_{HP} = 10^5 / (2 + 10^5 R_O)\ R_G$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = R_2 / (R_1 R_{11} C_1 R_{12} C_2)$
2. $Q = R_P (1 + 2 \times 10^5 R_O) \sqrt{R_{11} C_1 / (R_1 R_2 R_{12} C_2)}$
3. $Q\ A_{LP} = Q\ R_1\ A_{HP} / R_2 = A_{BP} \sqrt{R_1 R_{11} C_1 / (R_2 R_{12} C_2)}$
4. $A_{HP} = \sqrt{R_1 R_2 R_{12} C_2 / (R_{11} C_1)}\ Q\ R_G$
5. $1 / R_P = 1 / R_1 + 1 / R_2 + 1 / R_G$

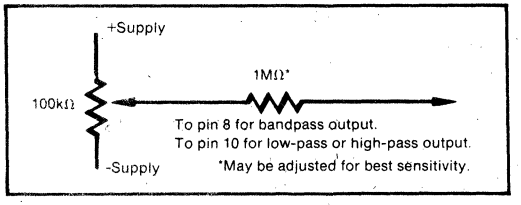
BI-QUAD CONFIGURATION

1. $\omega_o^2 = R_2 / (R_1 R_{11} C_1 R_{12} C_2)$
2. $Q = R_Q C_2\ \omega_o$
3. $Q\ A_{LP} / (\omega_o R_1 C_2) = A_{HP} = R_Q / R_G$

Offset Error Adjustment

DC offset errors will be minimized by grounding pin 5 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}. The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.



Design Example

It is desired to design a 5-pole Bessel, Low-Pass Filter with $f_o = 3.3$kHz and $A_{LP} = 1$. We will use the UAF11 to implement this filter.

From Table II the following values of f_n and Q are obtained.

Complex Poles:
$f_n = 1.55876$
$Q = 0.56354$
$f_n = 1.75812$
$Q = 0.91652$

Simple Pole:
$f_n = 1.50470$

Using the above shown values of f_n and Q, we now will proceed to design the three stages of filter separately.

Any one of the three configurations can be used. We will select inverting configuration.

For Stage 1.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.55876 = 5144Hz$

Since $f_o > 5kHz$, equations "B" would be used, thus an 11kΩ resistor must be connected between pins 12 and 1.

$$R_{F1} = R_{F2} = \frac{5.03 \times 10^7}{5144} = 9778\Omega$$

$$f_oQ = 5144 \times 0.56354 = 2.9 \times 10^3$$

$f_oQ < 10^4$, $\therefore Q_P = Q = 0.56354$

$$A_{BP} = \frac{Q_P}{3.16} \quad A_{LP} = \frac{0.56354}{3.16} \times 1 = 0.17834$$

$$R_G = \frac{3.16 \times 10^4 Q_P}{A_{BP}} = \frac{3.16 \times 10^4 \times 0.56354}{0.17834} = 99.85k\Omega$$

$$R_Q = \frac{2 \times 10^5}{3.48Q_P + A_{BP}\text{-}1} = \frac{2 \times 10^5}{3.48 \times 0.56354 + 0.17834 - 1} = 175.52k\Omega$$

For Stage 2.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.75812 = 5802Hz$

Since $f_o > 5kHz$, equations "B" would again be used, and an 11kΩ resistor would be connected between pins 12 and 1 of the second UAF stage.

$$R_{F1} = R_{F2} = \frac{5.03 \times 10^7}{5802} = 8669\Omega$$

$$f_oQ = 5802 \times 0.91652 = 5.32 \times 10^3$$

$f_oQ < 10^4$, $\therefore Q_P = Q = 0.91652$

$$A_{BP} = \frac{Q_P}{3.16} \quad A_{LP} = \frac{0.91652}{3.16} \times 1 = 0.29004$$

$$R_G = \frac{3.16 \times 10^4 Q_P}{A_{BP}} = \frac{3.16 \times 10^4 \times 0.91652}{0.29004} = 99.86k\Omega$$

$$R_Q = \frac{2 \times 10^5}{(3.48 Q_P + A_{BP}\text{-}1)} = \frac{2 \times 10^5}{(3.48 \times 0.91652 + 0.29004 - 1)} = 80.66k\Omega$$

For Stage 3.

$f = 3.3kHz \times f_n = 3.3kHz \times 1.50470 = 4966Hz$

For the simple pole,

$$RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 4966} = 3.2049 \times 10^{-5}$$

3300pF (or any convenient value)

$$R = \frac{3.2049 \times 10^{-5}}{3300 \times 10^{-12}} = 9.71k\Omega$$

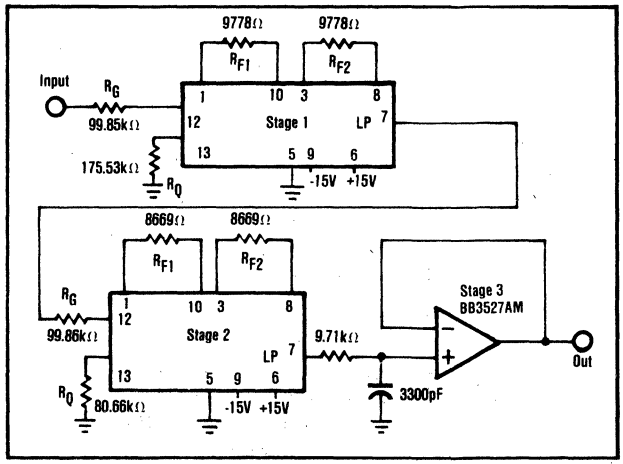


FIGURE 6. Overall Circuit.

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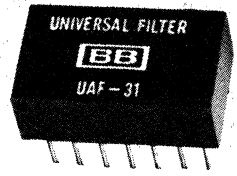
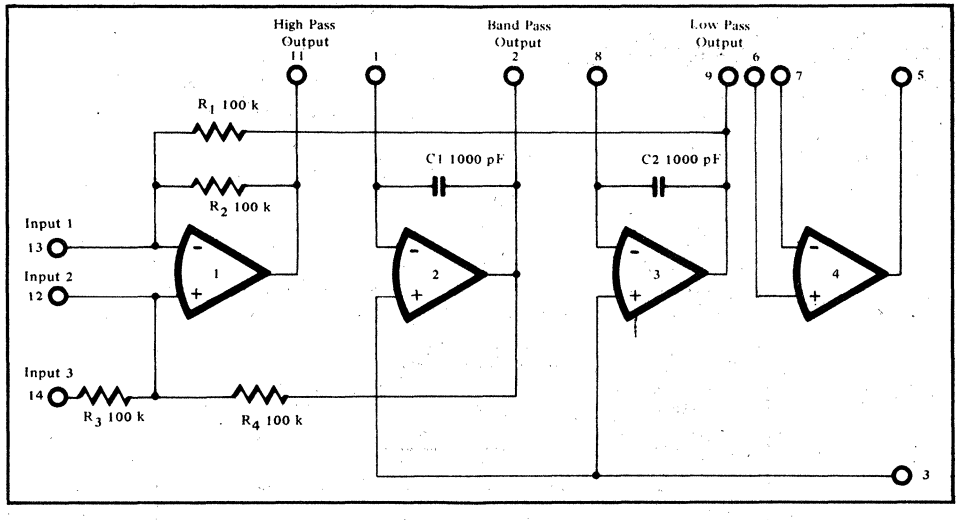


UAF31

UNIVERSAL ACTIVE FILTER



FEATURES

- **LOW COST**
- **SAVES DESIGN TIME**
  - **Calculate only three resistance values**
  - **Design directly from this data sheet**
  - **Completely characterized parameters**
- **IMPROVED PERFORMANCE**
  - **1% frequency accuracy**
  - **Uncommitted op amp included**
  - **Q range of 0.5 to 500**
  - **Reliable hybrid construction**
  - **NPO capacitors and thin-film resistors**

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

The UAF31 is a versatile 2-pole active filter which, with the addition of three or four external resistors, provides the user easy control of the Q-factor, resonant frequency and gain. Any complex filter response can be obtained by cascading units. The UAF31 is an ideal building block that can be purchased and stocked in quantity to be used whenever the requirement for a filter arises. In this way filters are available immediately and may be purchased in volume to take advantage of quantity price discounts.

Three separate outputs provide low pass, high pass, and band pass transfer functions. A band reject (notch) transfer function may be realized simply by summing the high pass and low pass outputs. The UAF31 also includes an uncommitted op amp that may be used as an input or output buffer or to add an additional one-pole response to the filter.

TRANSFER FUNCTION

The UAF31 uses the state variable technique to produce a basic second order transfer function. The equations describing the three outputs available are:

$$T(\text{Low Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\, s + \omega_o^2}$$

$$T(\text{Band Pass}) = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/Q)\, s + \omega_o^2}$$

$$T(\text{High Pass}) = \frac{A_{HP}\, s^2}{s^2 + (\omega_o/Q)\, s + \omega_o^2}$$

To obtain band reject characteristics the low pass and high pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2 + (\omega_o/Q)\, s + \omega_o^2} \text{ where } A_{LP}=A_{HP}=A.$$

The state variable approach uses two op amp integrators (#2 and #3 in the simplified schematic below) and a summing amplifier (#1) to provide simultaneous low pass, band pass and high pass responses. One UAF31 is required for each two poles of low pass or high pass filters and for each pole-pair of band pass or band reject filters.

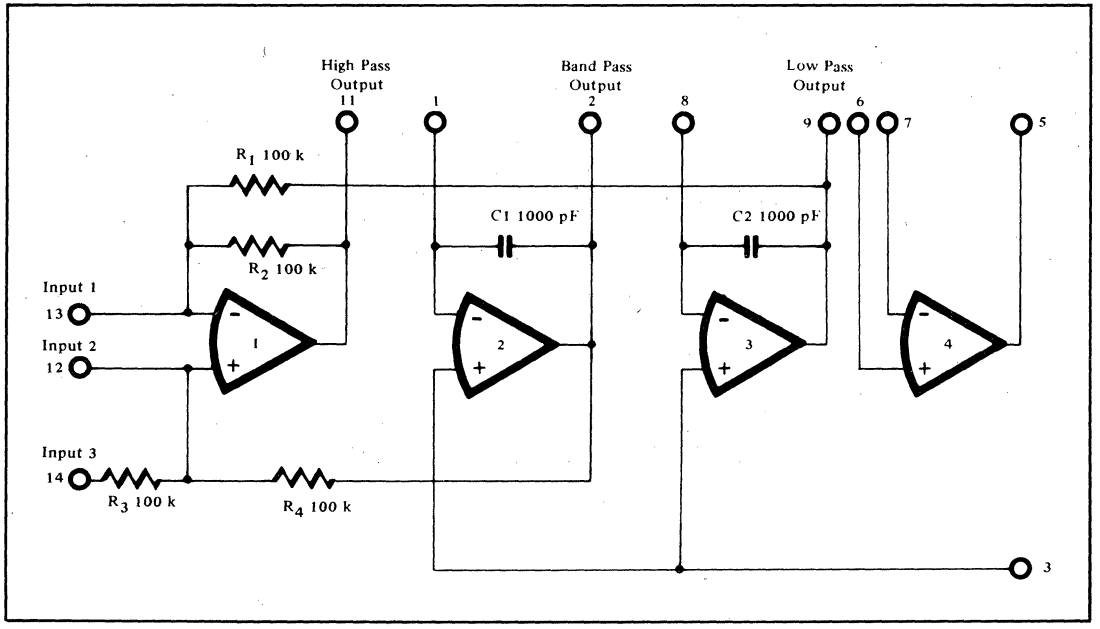


FIGURE 1. UAF31 Schematic.

SPECIFICATIONS

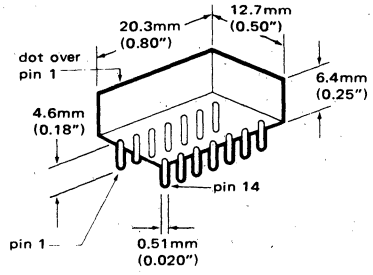
ELECTRICAL

Typical at 25°C and with rated supply unless otherwise noted.

MODEL	UAF31
INPUT	
Input Bias Current	±40 nA
Input Voltage Range	±10 V
Input Resistance	100 kΩ
TRANSFER CHARACTERISTICS	
Frequency Range (f_o)	0.001 to 25 kHz
f_o Accuracy(1), max	±1%
f_o Stability(2)	±0.002%/°C
Q Range(3)	0.5-500
Q Stability(4)	
@f_o Q ≤ 10^4	±0.01%/°C
@f_o Q ≤ 10^5	±0.025%/°C
Q Repeatability	±10%
Gain Range	0.1 to 50V/V
OUTPUT	
Peak to Peak Output Swing(5)	20 V
Output Offset (at L.P. output with unity gain)	±20 mV
Output Impedance	1 Ω
Noise(6)	200 μV (rms)
Output Current(7)	5 mA
UNCOMMITTED AMP CHARACTERISTICS	
Input Offset Voltage	5 mV
Input Bias Current	40 nA
Input Impedance	1 MΩ
Large Signal Voltage Gain	85 dB
Output Current	5 mA
POWER SUPPLIES	
Rated Power Supplies	±15 V
Power Supply Range(8)	±5 to ±18 V
Supply Current @ ±15 V(Quiescent), max	12 mA
TEMPERATURE RANGE	
Specification	−25°C to +85°C
Storage	−40°C to +85°C

(1) The tolerance of external frequency determining resistors must be added to this figure.
(2) T.C.R. of external frequency determining resistors must be added to this figure.
(3) See figure 3 for Q vs. F curve.
(4) Q stability varies with both the value of Q and the resonant frequency f_o.
(5) See figure 2 for full power response curve.
(6) Measured at the band pass output with Q @ 50 over DC to 50 kHz.
(7) The current required to drive R_{F1} and C_1 and C_2 must come from this current.
(8) For supplies below ±10 V, Q max will decrease slightly; filters will operate below ±5 V.

MECHANICAL



ROW SPACING—7.6 (0.300")
WEIGHT—.12 oz. (3.4)
CONNECTOR—14 pin DIP connector

Pin material and plating composition conform to method 208 (solderability) of MIL-STD-202.

PIN CONNECTIONS

Pin 1—Frequency Adjust
Pin 2—Band pass Output
Pin 3—Common
Pin 4—Positive Supply
Pin 5—Auxiliary Amp. Output
Pin 6—Auxiliary Amp + Input
Pin 7—Auxiliary Amp - Input
Pin 8—Frequency Adjust
Pin 9—Low Pass Output
Pin 10—Negative Supply
Pin 11—High Pass Output
Pin 12—Filter Input 2
Pin 13—Filter Input 1
Pin 14—Filter Input 3

TYPICAL PERFORMANCE CURVES

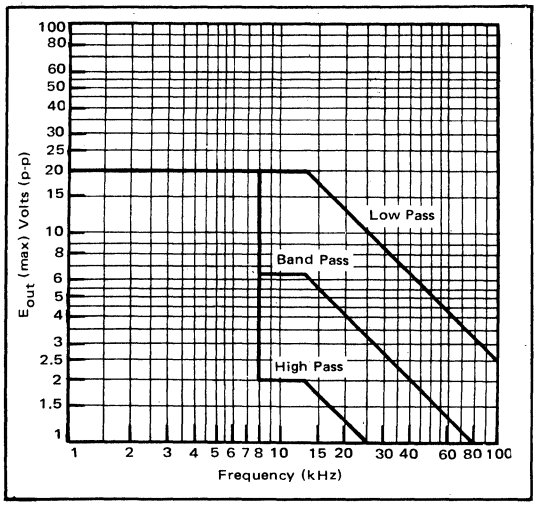


FIGURE 2. Full Power Response

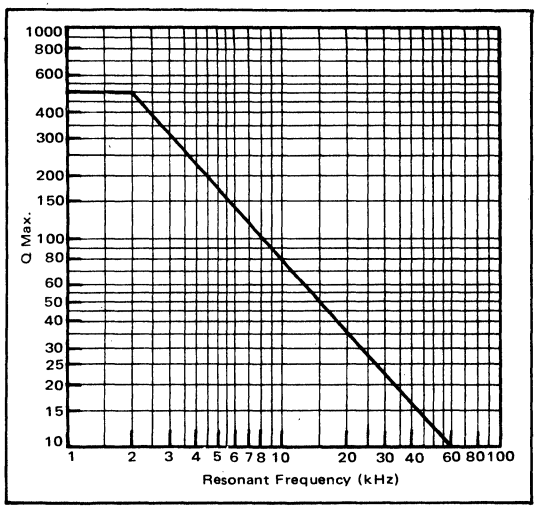


FIGURE 3. Q Max. vs. Resonant Frequency

ACTIVE FILTER DESIGN PROCEDURE

To design filters using the circuits shown on the following pages, these six design steps should be followed:

1. Determine f_0, the natural frequency of the pole pair.
2. Determine A, the gain of the filter section (V/V).
3. Determine the Q factor.
4. Calculate Q_p as shown in the Q factor design notes to compensate for amplifier phase shift errors.
5. Determine the filter configuration that will be used (see configuration selection guide on the opposite page for recommendations).
6. Calculate the resistance values required using the design equations for the filter configuration selected.

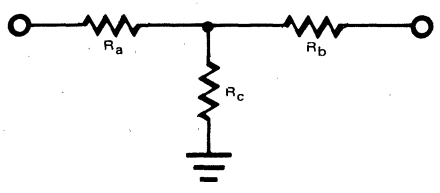
NATURAL FREQUENCY (f_0) DESIGN NOTES

f_0 values for many low pass and high pass filters are given in the filter parameter table on page 5-107.

f_0 for each one pole-pair band pass filter is the center frequency (f_c). f_c is defined as $f_c = \sqrt{f_1 f_2}$ when f_1 is the lower 3 dB point and f_2 is the upper 3 dB point of the filter.

To use the UAF31 with f_0 above 8 kHz, an 11 kΩ resistor must be placed in parallel with R_2 (between pins 13 and 11). For the higher frequencies where an 11 kΩ resistor is required, use simplified design equations "B". For operation below these frequencies; use simplified design equations "A" or "B".

To obtain f_0 below 100 Hz using practical resistor values, T-networks may be used for the frequency determining resistors (R_{F1} and R_{F2}).



The equivalent resistance if inserted between pins 1 and 11 or pins 2 and 8 is

$$R = \frac{R_a R_b}{R_c} + R_a + R_b$$

Capacitors may also be paralleled with C_1 and C_2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}(\text{new}) = R_{F2}(\text{new}) = R_{F1}(\text{old}) \frac{1000\ \text{pF}}{C + 1000\ \text{pF}}$$

where R_F(new) are the new lower value frequency resistors, C is the value of the two external capacitors placed across C_1 and C_2 (between pins 1 and 2 and pins 8 and 9), R_{F1} (old) is the value calculated in the simplified design equations.

GAIN (A) DESIGN NOTES

The gain (V/V) of the filter section is:

A_{LP} - for low pass output - gain at DC.

A_{BP} - for band pass output - gain at f_0.

A_{HP} - for high pass output - gain at high frequencies.

Q FACTOR DESIGN NOTES

For band pass filters $Q = \frac{f_o}{3\text{ dB bandwidth}}$

Q values for many low pass and high pass filters are given in the pole position table on page 5-107.

A FORTRAN computer program to transform low pass pole positions to band pass pole positions is given on page 5-108.

When designing low pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.

Q repeatability (Q change from unit-to-unit) is typically ±5% at f_oQ products less than 10^4. The Q repeatability error increases as the f_oQ product increases, to approximately ±20% for f_oQ products near 10^6.

Calculate the f_o times Q product of the filter. If the product is above 10^4 Hz, locate the corresponding f_oQ_p product in Figure 4. Divide f_oQ_p by f_o to obtain Q_p. Use Q_p as indicated in the equations on page 5-106 to correct for amplifier phase shift errors. For f_oQ products below 10^4 Hz, simply use Q. As can be seen in Figure 4, the amplifier phase shift errors cause Q to rise with increasing f_oQ products.

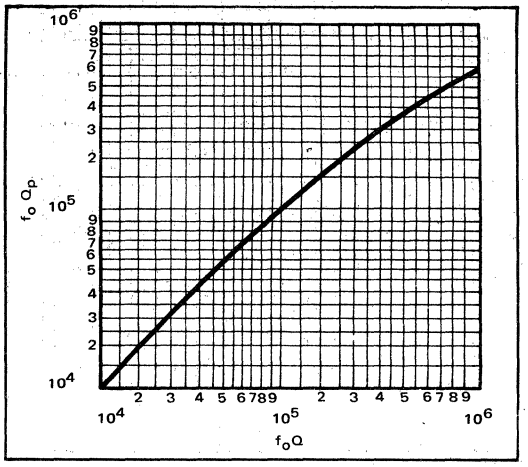


FIGURE 4. Qp Determination

NOTE: For more comprehensive detailed design procedure and illustrated examples of filter design using the Universal Active Filters, please refer to PDS-359, product data sheet for Burr-Brown model No. UAF41.

CONFIGURATION SELECTION GUIDE

	NONINVERTING INPUT	INVERTING INPUT	BI-QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Inverted Outputs	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant bandwidth
Other Advantages	May be used with only three external resistors (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies
Parameter Limitations	$2Q_p - A_{BP} > 1$ ($f_o < 8$ kHz) $3.48Q_p - A_{BP} > 1$ ($f_o > 8$ kHz)	$2Q_p + A_{BP} > 1$ ($f_o < 8$ kHz) $3.48Q_p + A_{BP} > 1$ ($f_o > 8$ kHz)	NONE

Summary: The Bi-Quad filter is particularly useful as a bandpass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a band pass or maintaining a constant response of a lowpass or highpass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than R_G and R_Q of the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 100$ k therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q).

NONINVERTING INPUT CONFIGURATION

For applications requiring a band pass gain of 1 (V/V), the internal resistor R_3 may be used (input at pin 14) as the gain resistor R_G. Thus only three external resistors are needed to configure the filter.

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 8$ kHz

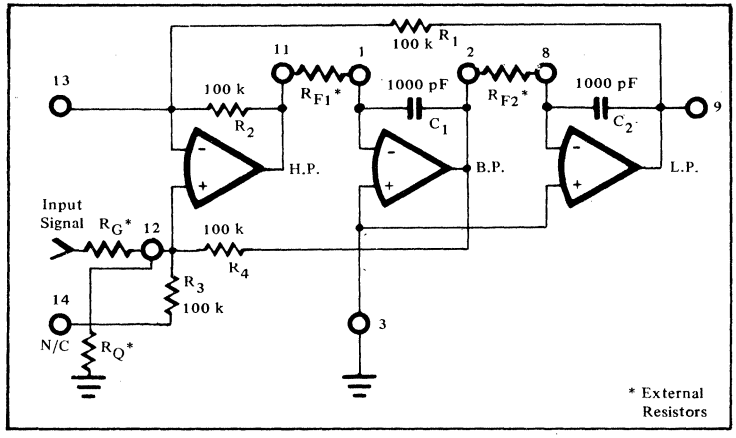
1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q\,A_{LP} = Q\,A_{HP}$
3. $R_G = \frac{10^5\ Q}{A_{BP}\ Q_P}$
4. $R_Q = \frac{10^5}{2Q_P - \frac{A_{BP}\,Q_P}{Q} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = \frac{Q}{3.16}\,A_{LP} = 3.16\,Q\,A_{HP}$
3. $R_G = \frac{10^5\ Q}{A_{BP}\ Q_P}$
4. $R_Q = \frac{10^5}{3.48\,Q_P - A_{BP}\,Q_P/Q - 1}$

* To use equations "B" connect an 11 k resistor between pins 11 and 13. Equations "B" are also valid for frequencies below 8 kHz.



INVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

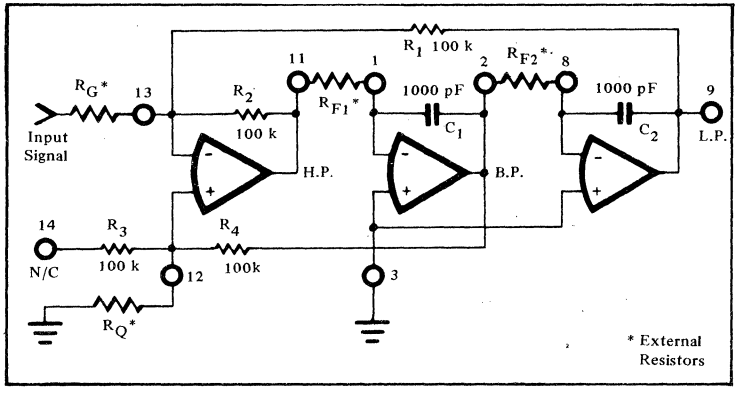
$f_o < 8$ kHz

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q_P\,A_{LP} = Q_P\,A_{HP}$
3. $R_G = \frac{10^5\ Q_P}{A_{BP}}$
4. $R_Q = \frac{10^5}{2Q_P + A_{BP} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = \frac{Q_P}{3.16}\,A_{LP} = 3.16\,Q_P\,A_{HP}$
3. $R_G = \frac{3.16 \times 10^4\ Q_P}{A_{BP}}$
4. $R_Q = \frac{10^5}{3.48\,Q_P + A_{BP} - 1}$



BI-QUAD CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

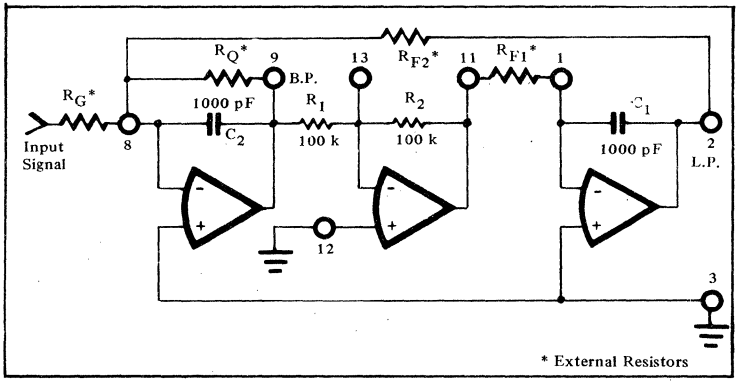
$f_o < 8$ kHz

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q\,A_{LP}$
3. $R_Q = Q_P\,R_{F1}$
4. $R_G = \frac{R_Q}{A_{BP}}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = 3.16\,Q\,A_{LP}$
3. $R_Q = 3.16\,Q_P\,R_{F1}$
4. $R_G = \frac{R_Q}{A_{BP}}$



UAF31

BAND REJECT

The band reject configuration is achieved by summing the high pass and low pass UAF outputs. The circuits shown in Figures 5 and 6 can be used to provide the band reject function if they are connected as shown in Figure 8. The Figure 8 circuit is applicable when using simplified design equations "A" ($A_{LP} = A_{HP}$), but when operating with an 11 kΩ resistor between pins 13 and 11 ($A_{LP} = 10\ A_{HP}$), the resistor at pin 9 must be 10 times the resistor at pin 11 to obtain equal passband gains above and below f_O.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_O and Q of the band reject filter desired and for A_{LP} to equal the desired passband gain. An input constraint: the input voltage times A_{BP} must not exceed the rated peak-to-peak output voltage of the band pass output, or clipping and distortion will result.

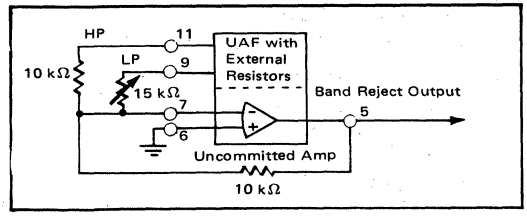


FIGURE 8. Band Reject Output

FILTER PARAMETERS

LOW PASS AND HIGH PASS

Table 1 shows filter parameters for many 2 to 8 pole low pass filters. The Q and the normalized undamped natural frequency, f_n, for each two-pole section are shown. The Q values should be used with Figure 4 and in the design formulas on page 5-106 and f_n must be multiplied by the desired cutoff frequency of the overall filter to obtain the required frequency, f_o, for the design formulas. As an example, consider a 4-pole low pass Bessel filter with a cutoff frequency of 1000Hz. The first stage would be designed to an f_o of 1432.41Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94Hz and a Q of 0.80554. The low pass output of the first stage (pin 9) should be connected to the input resistor (R_G) of the second stage.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents the simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. The uncommitted internal op amp should be used as a buffer to isolate the RC network so that the UAF input resistor will not affect the cutoff frequency of the RC network.

The cutoff frequency determined by the Table 1 filter parameters is (1) the 3 dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band and enters the stop band.

To obtain high pass pole positions, the low pass to high pass transformation may be used:

$$f_n\ (\text{high pass}) = \frac{1}{f_n\ (\text{low pass})}$$

$$Q\ (\text{high pass}) = Q\ (\text{low pass})$$

The low pass to band pass transformation is much more complicated, but it can be done using the low pass to band pass conversion program (Table III).

NUMBER OF POLES	BUTTERWORTH		BESSEL		CHEBYSCHEV 0.5 dB RIPPLE		CHEBYSCHEV 2 dB RIPPLE	
	f_n	Q	f_n	Q	f_n	Q	f_n	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	----------	1.32475	----------	0.626456	----------	0.368911	----------
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	----------	1.50470	----------	0.362320	----------	0.218308	----------
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	----------	1.68713	----------	0.256170	----------	0.155410	----------
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67657	0.237699	0.89236
	1.0	0.60134	1.83514	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5305	0.990142	18.6873

TABLE 1. Low Pass Filter Parameters

LOW PASS CHEBYSCHEV

Table II details a FORTRAN program to determine f_n and Q for a Chebyschev low pass filter. The only inputs required are the number of poles and the peak to peak ripple (dB) of the desired filter. The program outputs are treated exactly as the values on the pole position table (Table 1).

BAND PASS

Table III details a FORTRAN program that may be used to transform low pass pole positions into the equivalent band pass pole positions.

Program Inputs:

1. f_n—From Table I for the low pass filter of interest.
2. Q From Table I.
3. Q_{BP}—Desired Q of the band pass filter.

For filters with an odd number of poles a Q of .5 should be used where Q is not given in Table I. The program transforms each low pass pole into a band pass pole pair. That is, using the two-pole low pass pole positions would result in the pole positions for a two pole pair, band pass filter, requiring two UAF stages. Enter 10^6 for Q when transforming zeros on the imaginary axis. This program automates the transformation $s = p/2 \pm (p/2)^2 - 1$.

```
   PI=3.1415926536
   COMPLEX P(10)
   READ 5,N,R
5 FORMAT(I2,F8.6)
   A=SQRT(EXP(R/4.3429448)-1.)
   B=1./A
   AN=ALOG(B+SQRT(B**2+1.))
   AN=AN/FLOAT(N)
   J=MOD(N,2)+N/2
   DO 10 K=1,J
   RP=SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT(2*N))
   XIP=COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
   WN=SQRT(RP**2+XIP**2)
   Q=-WN/(2.*RP)
   P(K)=CMPLX(WN,Q)
   IF(MOD(N,2).NE.0.AND.K.EQ.J) GO TO 15
   PRINT 20,P(K)
   GO TO 10
15 F=REAL(P(K))
   PRINT 30,F
10 CONTINUE
20 FORMAT(2X"FN="E20.8" Q = "E20.8)
30 FORMAT(2X"FN="E20.8)
   STOP
   END
```

OFFSET ERROR ADJUSTMENT

DC offset errors will be minimized by grounding pin 3 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}.

The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.

```
   COMPLEX P,S,U
   READ 5, FN, Q, QBP
5  FORMAT (3F12.5)
   Y=FN*SQRT(1.-(1./(Q*2.))**2)
   X=-FN/(Q*2.)
   P=CMPLX(X,Y)
   U=CONJG(P)
   DO 30 I=1,2
   S=P/(2.*QBP)
   P=S**2-1.
   T=ATAN2(AIMAG(P),REAL(P))
   IF(T.GE.0.) GO TO 10
      T=2.*3.14159+T
10 T=T/2.
   A=SQRT(CABS(P))*COS(T)
   B=SQRT(CABS(P))*SIN(T)
   S=S+CMPLX(A,B)
   FN=CABS(S)
   Q=-FN/(2.*REAL(S))
   PRINT 20,FN,Q
20 FORMAT (2X"FN = "F12.5" Q = "F12.5)
   IF(AIMAG(U).EQ.0.) GO TO 40
30 P=U
40 STOP
   END
```

TABLE III. Low Pass to Band Pass Transformation Program

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF31 filter components. They should be used if a detailed analysis, not covered in the simplified equations, is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \dfrac{1 + \frac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \frac{R_2}{R_1}} \left(\dfrac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{1 + \frac{R_1}{R_2}}{R_G\left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$

5. $A_{HP} = \dfrac{R_2}{R_1} A_{LP} = \dfrac{1 + \frac{R_2}{R_1}}{R_G\left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$

6. $A_{BP} = \dfrac{R_4}{R_G}$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \left(1 + \dfrac{R_4}{R_Q}\right) \left(\dfrac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}}\right) \left(\dfrac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{R_1}{R_G}$

5. $A_{HP} = \dfrac{R_2}{R_1} A_{LP} = \dfrac{R_2}{R_G}$

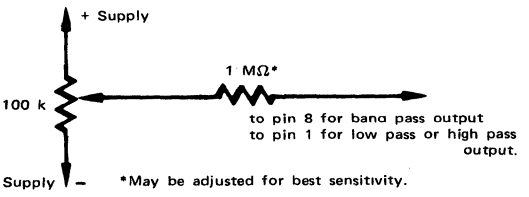
6. $A_{BP} = \left(1 + \dfrac{R_4}{R_Q}\right) \dfrac{1}{R_G\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)}$

BI-QUAD CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} C_1 R_{F2} C_2}$

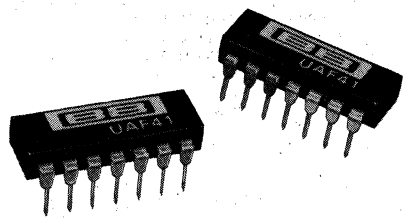
2. $Q = R_Q C_2 \omega_o$

3. $A_{BP} = \dfrac{Q A_{LP}}{\omega_o R_{F2} C_2} = \dfrac{R_Q}{R_G}$



BURR-BROWN®

UAF41



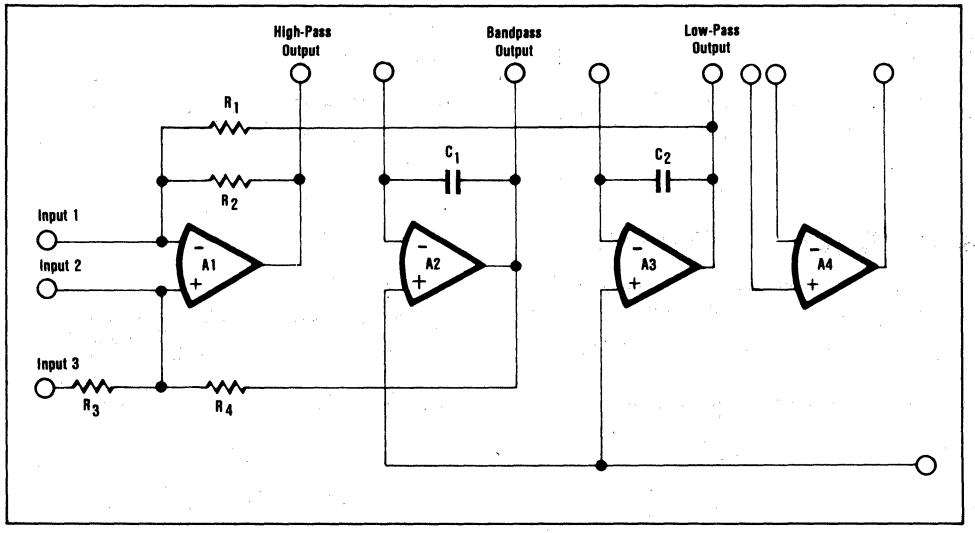
UNIVERSAL ACTIVE FILTER

FEATURES

- LOW COST
- SMALL SIZE
  - Single wide DIP package
- FULLY CHARACTERIZED PARAMETERS
- HYBRID CONSTRUCTION
- IMPROVED PERFORMANCE
  - 1% frequency accuracy
  - Q range of 0.5 to 500
  - NPO capacitors and thin-film resistors
  - Uncommitted op amp included

BENEFITS

- SAVES PRINTED CIRCUIT BOARD SPACE
- SAVES DESIGN TIME
  - Calculate only four resistance values
  - Design directly from this data sheet
  - Versatile building block for filter design
- HIGH RELIABILITY
- HIGH STABILITY



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DESCRIPTION

The UAF41 is a versatile two-pole active filter. It uses a three operational amplifier double integrator feedback loop to generate a complex pole pair (two conjugate poles). The location of the poles in the complex plane (and thus the natural frequency and Q) are determined by external, user supplied resistors. Either three or four resistors are used depending on the particular configuration chosen.

The UAF41 produces three transfer functions simultaneously - low-pass, high-pass, and bandpass - which are available at three separate outputs. The fourth basic transfer function - the band-reject or notch - can be obtained simply by summing the high-pass and low-pass outputs using the uncommitted amplifier (A4) contained in the UAF41. The uncommitted op amp can also be used to add a single-pole response for complex filters requiring an odd number of poles.

More complex higher-order filters can readily be obtained by cascading UAF's. This is easily done with the UAF41 since the high input impedance and low output impedance associated with the operational amplifiers used prevents the series connected stages from interacting (e.g., no frequency pull due to following stage loading). This data sheet contains the design procedures for an easy selection of resistor values for the stagger tuning of cascaded stages.

The versatility of the UAF41 makes it a general purpose building block for a wide variety of active filter applications. Its universal nature, ease of use, small size, and low cost allows the user the convenience of keeping units on hand for immediate use whenever a filter requirement arises.

TRANSFER FUNCTION

The UAF41 uses the state variable technique to produce a basic second order transfer function. The equations describing the three outputs available are:

$$T(\text{Low-Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{Bandpass}) = \frac{A_{BP}\,(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{High-Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

To obtain band-reject characteristics the low-pass and high-pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band-Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $A_{LP} = A_{HP} = A$.

The state variable approach uses two op amp integrators (A2 and A3 in the simplified schematic below) and a summing amplifier (A1) to provide simultaneous low-pass, bandpass, and high-pass responses. One UAF41 is required for each two poles of low-pass or high-pass filters and for each pole-pair of bandpass or band-reject filters.

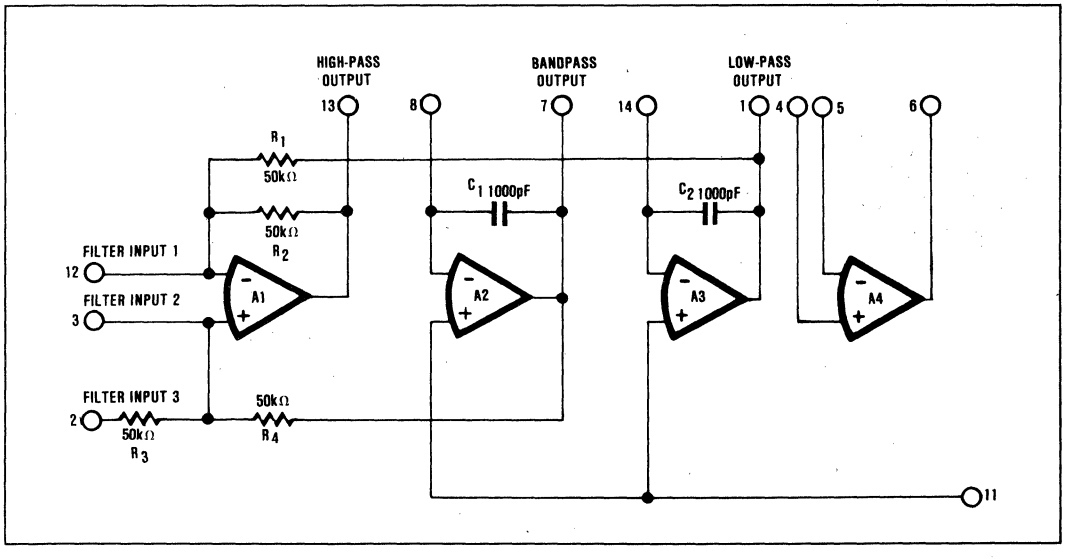


FIGURE 1. UAF41 Schematic.

SPECIFICATIONS

ELECTRICAL

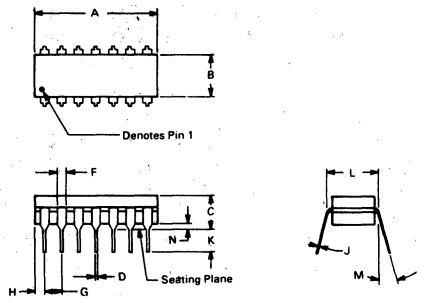
Typical at 25°C and with rated supply unless otherwise noted.

MODEL	UAF41
INPUT	
Input Bias Current	±40nA
Input Voltage Range	±10V
Input Resistance(1)	50kΩ
TRANSFER CHARACTERISTICS	
Frequency Range (f_0)	0.001Hz to 25kHz
f_0 Accuracy(2), max	±1%
f_0 Stability(3)	±0.002%/°C
Q Range(4)	0.5 to 500
Q Stability(5)	
@ f_0 Q ≤ 10^4	±0.01%/°C
@ f_0 Q ≤ 10^5	±0.025%/°C
Q Repeatability at f_0 Q ≤ 10^5	±10%
Gain Range	0.1V/V to 50V/V
OUTPUT	
Peak-to-Peak Output Swing(6)	20V
Output Offset(7)	
(at L.P. output with unity gain)	±20mV
Output Impedance	1Ω
Noise(8)	200μV, rms
Output Current(9)	5mA
UNCOMMITTED AMP CHARACTERISTICS	
Input Offset Voltage	5mV
Input Bias Current	40nA
Input Impedance	1MΩ
Large Signal Voltage Gain	85dB
Output Current	5mA
POWER SUPPLIES	
Rated Power Supplies	±15VDC
Power Supply Range(10)	±5VDC to ±18VDC
Supply Current @ ±15V (Quiescent), max	7mA
TEMPERATURE RANGE	
Specification Temperature Range	-25°C to +85°C
Storage Temperature Range	-25°C to +85°C

NOTES:

1. For noninverting input configuration with A_{BP} * 1.
2. The tolerance of external frequency determining resistors must be added to this figure.
3. T.C.R. of external frequency determining resistors must be added to this figure.
4. See Performance Curves for Q_{max} vs F curve.
5. Q stability varies with both the value of Q and the resonant frequency f_0.
6. See Performance Curves for full power response curve.
7. $R_{F1} = R_{F2} < 100k\Omega$ at low-pass output with unity gain.
8. Measured at the bandpass output with Q @ 50 over DC to 50kHz.
9. The current required to drive R_{F1} and R_{F2} (external) as well as C1 and C2 must come from this current.
10. For supplies below ±10V, Q_{max} will decrease slightly; filters will operate below ±5V.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.660	.785	16.76	19.94
B	.220	.280	5.59	7.11
C	–	.200	–	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095		
J	.008	.015	0.20	0.38
K	.100	–	2.54	–
L	.300 BASIC		7.62 BASIC	
M	–	15°	–	15°
N	.020	.050	0.51	1.27

ROW SPACING: 7.63mm (0.300")
WEIGHT: 1.1 grams max
CONNECTOR: 14-pin DIP connector (145MC @ $3.90)

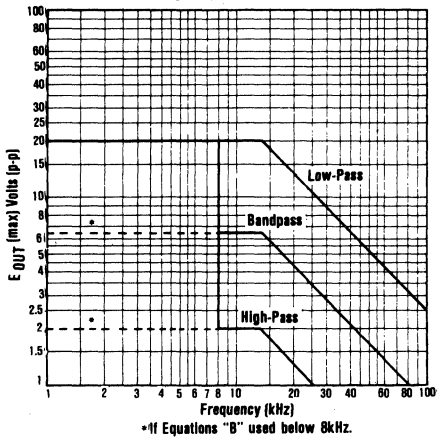
Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

PIN CONNECTIONS

Pin 1 - LOW-PASS OUTPUT
Pin 2 - FILTER INPUT 3
Pin 3 - FILTER INPUT 2
Pin 4 - AUXILIARY AMP + INPUT
Pin 5 - AUXILIARY AMP - INPUT
Pin 6 - AUXILIARY AMP OUTPUT
Pin 7 - BANDPASS OUTPUT
Pin 8 - FREQUENCY ADJUST
Pin 9 - NEGATIVE SUPPLY
Pin 10 - POSITIVE SUPPLY
Pin 11 - COMMON
Pin 12 - FILTER INPUT 1
Pin 13 - HIGH-PASS OUTPUT
Pin 14 - FREQUENCY ADJUST

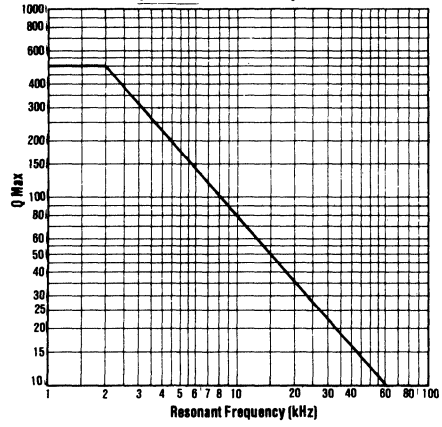
TYPICAL PERFORMANCE CURVES

FULL POWER RESPONSE

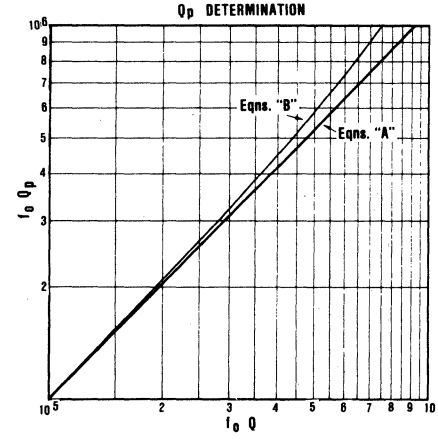


*If Equations "B" used below 8kHz.

Q MAX VS RESONANT FREQUENCY



Qp DETERMINATION



DESIGN PROCEDURE SUMMARY

This summary gives the design steps for the proper application of UAF41s and for the selection of the external components. More detailed information on filter theory pertinent to some of the steps can be found in the reference sources listed on last page.

Burr-Brown also manufactures a line of completely self-contained active filters called the ATF76 series. These are available in most popular transfer functions with from 2- to 8-pole responses. They contain all necessary components and do not require any user design effort.

DESIGN STEPS:

1. Choose the type of function (low-pass, bandpass, etc.), type of response (Butterworth, Bessel, etc.), number of poles, and cutoff frequency based on the particular application.

   If the transfer function is band-reject see Band-Reject Transfer Function before proceeding to step 2.
2. Determine the normalized low-pass filter parameters (f_n and Q) based on the type of response and number of poles selected in step 1. See Normalized Low-Pass Parameters.
3. If the actual response desired is low-pass go to step 4. For other responses a transformation of variables must be made (low-pass to bandpass or low-pass to high-pass). See Low-Pass Transformation.
4. Determine the actual (denormalized) cutoff frequency, f_o, by multiplying f_n by the actual desired cutoff frequency. See Denormalization of Parameters.
5. Pick the desired UAF configuration (noninverting, inverting or bi-quad) see Configuration Selection Guide and UAF41 Configuration and Design Equations.
6. Decide whether to use design equations "A" or "B". See Design Equations "A" and "B".
7. Calculate R_{F1} and R_{F2}. See Natural Frequency and UAF Configurations and Design Equations.
8. Determine Q_P. See Q_P Procedure.
9. Select the desired gain for each UAF and calculate the corresponding R_G and R_Q. See Gain (A) and UAF41 Configurations and Design Equations.

NORMALIZED LOW-PASS PARAMETERS

Usual active filter design procedure involves using normalized low-pass parameters. Table I is provided to assist in this step for the more common filter responses. Table II is a FORTRAN program which allow f_n and Q to be calculated for any desired ripple and number of poles for the Chebyschev response. Consult the references on last page for other information.

Note that for bandpass and high-pass filters complex conjugate pole pairs in the actual filter correspond to single poles in the normalized low-pass model. Thus four poles in Table I would correspond to four-pole pairs in a bandpass or high-pass filter.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents a simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. The uncommitted internal op amp with an external RC network can be used for this purpose.

The cutoff frequency determined by the Table I filter parameters is (1) the -3dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band (to enter the stop band).

TABLE I. Low-Pass Filter Parameters.

NUMBER OF POLES	BUTTERWORTH		CHEBYSCHEV					
			BESSEL		0.5dB RIPPLE		2dB RIPPLE	
	f_n(1)	Q	f_n(1)	Q	f_n(2)	Q	f_n(2)	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	----	1.32475	----	0.626456	----	0.368911	----
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	----	1.50470	----	0.362320	----	0.218308	----
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	----	1.68713	----	0.256170	----	0.155410	----
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67657	0.237699	0.89236
	1.0	0.60134	1.83514	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5305	0.990142	18.6873

(1) -3 dB Frequency.
(2) Frequency at which amplitude response passes through the ripple band.

NORMALIZED LOW-PASS CHEBYSCHEV

Table II gives a FORTRAN program for the determination of f_n and Q for a general normalized Chebyschev low-pass filter of any ripple and number of poles. Program inputs are the number of poles (N) and the peak-to-peak ripple (R). Program outputs are f_n and Q, which are used exactly as the values taken from Table I.

BAND-REJECT TRANSFER FUNCTION

The band-reject is achieved by summing the high-pass and low-pass UAF outputs. Either of the configurations in Figures 3 and 4 can be used to provide the band-reject function if they are used as shown in Figure 2.

The 15kΩ resistor is adjusted for maximum rejection. The circuit in Figure 2 is applicable when using design equations "A" ($A_{LP} = A_{HP}$). When design equations "B" are used ($A_{LP} = 10A_{HP}$), the resistor at pin 1 must be 10 times the resistor at pin 13 to obtain equal pass-band gains above and below f_n.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_o and Q of the

band-reject filter desired and for A_{LP} to equal the desired pass-band gain. An input constraint is that the input voltage times A_{BP} must not exceed the rated peak-to-peak voltage of the bandpass output, or clipping will result.

TABLE II. Low-Pass Chebyschev Program.

```
      PI = 3.1415926536
      COMPLEX P(10)
      READ 5, N, R
    5 FORMAT (12, F8, 6)
      A = SQRT (EXP(R/4.3429448)-1)
      B = 1./A
      AN = ALOG(B+SQRT(B**2+1.))
      AN = AN/FLOAT(N)
      J = MOD(N,2)+N/2
      DO 10 K = 1, J
      RP=SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT(2*N))
      XIP = COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
      WN= SQRT(RP**2+XIP**2)
      Q = -WN/(2.*RP)
      P(K) = CMPLX(WN,Q)
      IF(MOD(N,2).NE.0 AND.K.E.Q.J.)GO TO 15
      PRINT 20, P(K)
      GO TO 10
   15 F = REAL(P(K))
      PRINT 30, F
   10 CONTINUE
   20 FORMAT(2X"FN="E20.8"E20.8)
   30 FORMAT(2X"FN="E20.8)
      STOP
      END
```

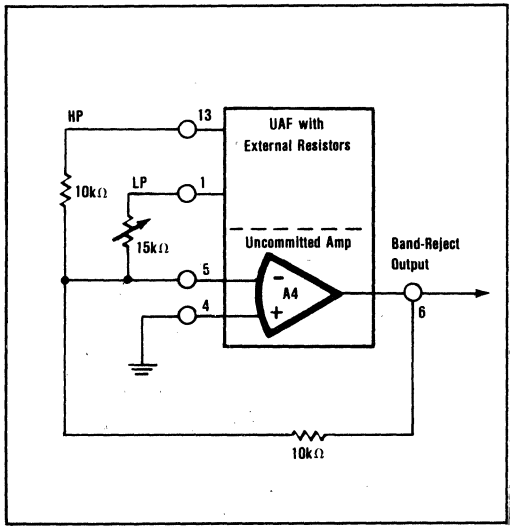
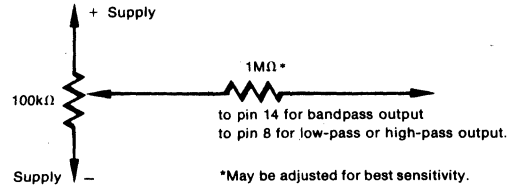


FIGURE 2. Band-Reject Configuration.

OFFSET ERROR ADJUSTMENT

DC offset errors will be minimized by grounding pin 3 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}. The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.



LOW-PASS TRANSFORMATION

LOW-PASS TO HIGH-PASS

The following simple transformation may be used for high-pass filters:

$$f_n \text{ (high-pass)} = \frac{1}{f_n \text{ (low-pass)}}$$

$$Q \text{ (high-pass)} = Q \text{ (low-pass)}$$

LOW-PASS TO BANDPASS

The low-pass to bandpass transformation to generate f_n (bandpass) and Q (bandpass) is much more complicated. It is tedious to do by hand but can be accomplished with the FORTRAN program given in Table III. This

TABLE III. Low-Pass to Bandpass Transformation Program.

```
      COMPLEX P, S, U
      READ 5, FN, Q, QBP
    5 FORMAT (3F12.5)
      Y=FN*SQRT(1.-(1./(Q*2.))**2)
      X=-FN/(Q*2)
      P=CMPLX(X,Y)
      U=CONJG(P)
      DO 30 I=1, 2
      S=P/(2.*QBP)
      P=S**2-1.
      T=ATAN2(AIMAG(P),REAL(P))
      IF(T.GE.0) GO TO 10
      T=2.*3.1459+T
   10 T=T/2
      A=SQRT(CABS(P))*COS(T)
      B=SQRT(CABS(P))*SIN(T)
      S=S+CMPLX(A,B)
      FN=CABS(S)
      Q=-FN/(2.*REAL(S))
      PRINT 20, FN, Q
   20 FORMAT (2X"FN ="F12.5"Q ="2.5)
      IF(AIMAG(U).EQ.0) GO TO 40
   30 P=U
   40 STOP
      END
```

program automates the tranformation
$s = p/2 \pm \sqrt{(p/2)^2 - 1}$.

PROGRAM INPUTS:

1. f_n - From Table I for the low-pass filter of interest
2. Q - From Table I
3. Q_{BP} - Desired Q of the bandpass filter

For filters with an odd number of poles a Q of 0.5 should be used where Q is not given in Table I. Enter 10^5 for Q when transforming zeros on the imaginary axis.

The program transforms each low-pass pole into a bandpass pole pair. Thus a three-pole low-pass input, would result in the pole positions for a three-pole pair bandpass filter requiring three UAF stages.

DENORMALIZATION OF PARAMETERS

Table I shows filter parameters for many 2- to 8-pole normalized low-pass filters. The Q and the normalized undamped natural frequency, f_n for each two-pole section are shown. The Q values do not have to be denormalized and may be used directly as described in the Design Procedure Summary. f_n must be denormalized by multiplying it by the desired cutoff frequency of the actual overall filter to obtain the required frequency, f_o for the design formulas. As an example, consider a 4-pole low-pass Bessel filter with a cutoff frequency of 1000Hz. The first stage would be designed to an f_o of 1432.41Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94Hz and a Q of 0.80554. To combine the two stages into the composite filter the low-pass output of the first stage (pin 1) would be connected to the input resistors (R_G) of the second stage.

DESIGN EQUATIONS "A" AND "B"

1. For f_o below 8kHz, either of equations "A" or "B" may be used.
2. For f_o above 8kHz, equations "B" must be used. If equations "A" were used above 8kHz, the filter could become unstable.
3. Equations "A" are for the UAF as it is supplied. When using equations "B", a 5.49kΩ resistor must be placed in parallel with R_2 (between pins 12 and 13).
4. The values of R_{F1} and R_{F2} calculated with equations "B" are approximately one-third of those calculated with equations "A". Thus there may be an advantage in using equation "B" at low frequencies. Using equation "B" would require use of one more resistor, but that would not alter or affect filter performance in any manner.
5. Using the negative gain values for A_{LP} or A_{HP} or A_{BP} could result in the negative values for resistors R_G and R_Q. So the absolute value of the gain should always be used in the equations.

GAIN (A)

1. The gain (V/V) of each filter section is:
   A_{LP} - for low-pass output - gain at DC
   A_{BP} - for bandpass output - gain at f_o
   A_{HP} - for high-pass output - gain at high frequencies.
2. Refer to Performance Curves for full power response. When selecting the gain, insure that the limits of the curve are not exceeded for the desired voltage range.

NATURAL FREQUENCY (f_o)

1. f_o for each one pole-pair bandpass filter is the center frequency (f_C). f_C is defined as $f_C = \sqrt{f_1 f_2}$ where f_1 is the lower -3dB point and f_2 is the upper -3dB point of the pole pair response.
2. To obtain f_o below 100Hz using practical resistor values, capacitors may be paralleled with C1 and C2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}\text{ (new)} = R_{F2}\text{ (new)} = R_{F1}\text{ (old)}\ \frac{1000\text{pF}}{C + 1000\text{pF}}$$

where R_F (new) is the new lower value frequency resistor, C is the value of the two external capacitors placed across C1 and C2 (between pins 7 and 8 and pins 1 and 14 and R_{F1} (old) is the value calculated in the simplified design equations.

Q-FACTOR

1. For bandpass filters $Q = \dfrac{f_o}{3\text{dB bandwidth}}$
2. When designing low-pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.
3. Q repeatability (Q change from unit-to-unit) is typically ±5% for f_oQ products less than 10^4. The Q repeatability error increases as the f_oQ product increases to approximately ±10% for f_oQ products near 10^5.

Q_P PROCEDURE

1. If the "f_o times Q" product is greater than 10^5, it is possible for the measured filter Q to be different from the calculated value of Q. This effect is the result of non-ideal characteristics of operational amplifiers. It can be compensated for by introducing the parameter Q_P into the design equations.
2. Calculate the f_oQ product for the filter. If the product is above 10^5Hz, locate the corresponding f_oQ_P product in the Performance Curves. Divide f_oQ_P by f_o to obtain Q_P. Use Q_P as indicated in the design equations. For f_oQ products below 10^5Hz, $Q_P = Q$.

CONFIGURATION SELECTION GUIDE

It is possible to configure the UAF41 three different ways. Each configuration produces features that may or may not be desirable for a specific application. This selection guide is given to assist in determining the most advantageous configuration for a particular application.

	NONINVERTING INPUT	INVERTING INPUT	BI QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Outputs Inverted with respect to the Input	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant Bandwidth
Other Advantages	May eliminate one external resistor (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies
Parameter Limitations	$2\,Q_p - A_{BP} > 1$ (Eqns. "A") $3.48\,Q_p - A_{BP} > 1$ (Eqns. "B")	$2\,Q_p + A_{BP} > 1$ (Eqns. "A") $3.48\,Q_p + A_{BP} > 1$ (Eqns. "B")	No HP Output

Summary: The Bi-Quad filter is particularly useful as a bandpass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a bandpass or maintaining a constant response of a low-pass or high-pass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than with the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 50k\Omega$; therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q).

UAF41 CONFIGURATIONS AND DESIGN EQUATIONS

NONINVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q\,A_{LP} = Q\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\,Q}{A_{BP}\,Q_P}$

4. $R_Q = \frac{5.0 \times 10^4}{2Q_P - \frac{A_{BP}\,Q_P}{Q} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o > 8kHz$

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = \frac{Q}{3.16}\,A_{LP} = 3.16\,Q\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\,Q}{A_{BP}\,Q_P}$

4. $R_Q = \frac{5.0 \times 10^4}{3.48Q_p - \frac{A_{BP}\,Q_P}{Q} - 1}$

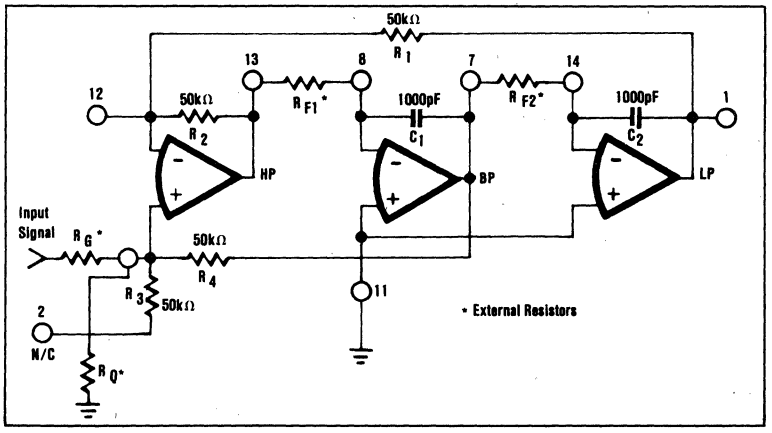


FIGURE 3. Noninverting Input Configuration.

INVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q_P A_{LP} = Q_P A_{HP}$

3. $R_G = \frac{5.0 \times 10^4 Q_P}{A_{BP}}$

4. $R_Q = \frac{5.0 \times 10^4}{2Q_P + A_{BP} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o > 8$kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = \frac{Q_P}{3.16} A_{LP} = 3.16\, Q_P A_{HP}$

3. $R_G = \frac{1.58 \times 10^4 Q_P}{A_{BP}}$

4. $R_Q = \frac{5.0 \times 10^4}{3.48 Q_P + A_{BP} - 1}$

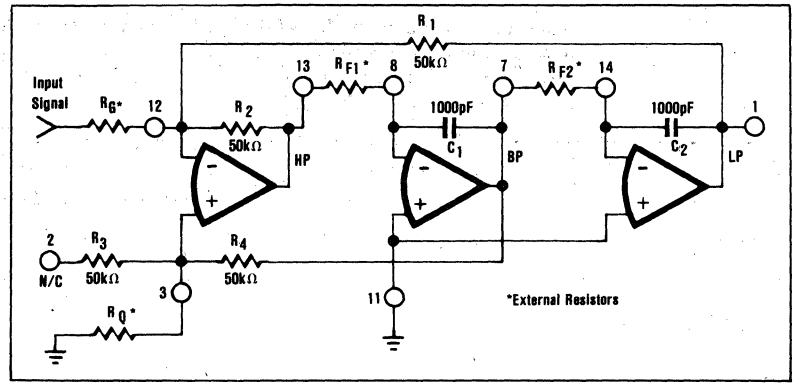


FIGURE 4. Inverting Input Configuration.

BI-QUAD CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q A_{LP}$

3. $R_Q = Q_P R_{F1}$

4. $R_G = \frac{R_Q}{A_{BP}}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o > 8$kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = 3.16\, Q A_{LP}$

3. $R_Q = 3.16\, Q_P R_{F1}$

4. $R_G = \frac{R_Q}{A_{BP}}$

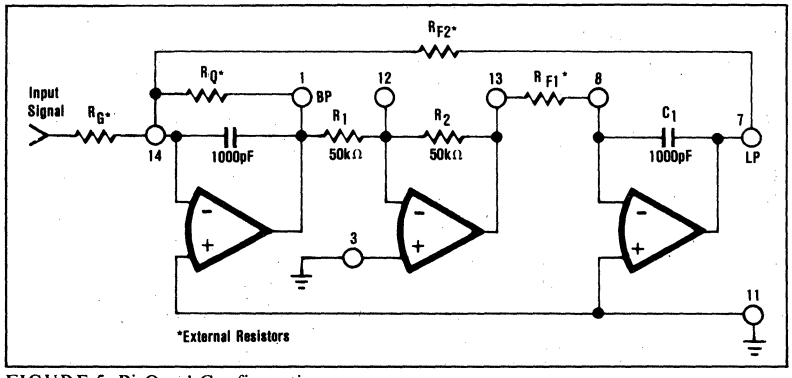


FIGURE 5. Bi-Quad Configuration.

† To use equations "B" connect a 5.49kΩ resistor between pins 12 and 13. Equations "B" are also valid for frequencies below 8kHz.

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF41 filter components. They are not required for the regular design procedure but could be used if a detailed analysis is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \frac{1 + \frac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \frac{R_2}{R_1}} \cdot \left(\frac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\frac{R_1}{R_2}\right) = A_{BP} \left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \frac{1 + \frac{R_1}{R_2}}{R_G \left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$

5. $A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{1 + \frac{R_2}{R_1}}{R_G \left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$

6. $A_{BP} = \frac{R_4}{R_G}$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \left(1 + \frac{R_4}{R_Q}\right) \left(\frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}}\right) \left(\frac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\frac{R_1}{R_2}\right) = A_{BP} \left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \frac{R_1}{R_G}$

5. $A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{R_2}{R_G}$

6. $A_{BP} = \left(1 + \frac{R_4}{R_Q}\right) \frac{1}{R_G \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)}$

BI-QUAD CONFIGURATION

1. $\omega_o^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = R_Q C_2 \omega_o$

3. $A_{BP} = \frac{Q A_{LP}}{\omega_o R_{F2} C_2} = \frac{R_Q}{}$

ACTIVE FILTER DESIGN EXAMPLES USING THE DESIGN PROCEDURE OUTLINED IN DESIGN STEPS SECTION.

Example 1.

It is desired to design a three-pole, 0.5dB ripple, Chebyschev High-Pass Filter; the cutoff frequency f_c = 2kHz, Gain $A_{HP} = +1$.

Step 1.
The type of transfer function (high-pass), the type of response (Chebyschev), number of poles (3), and the cut off frequency (f_c) are chosen depending upon the particular application and are stated in the example.

Step 2.
Normalized low-pass filter parameters f_n and Q are obtained from Table I (or from program shown in Table II).

Complex Poles:
$f_n = 1.068853$
$Q = 1.7062$
Simple Pole:
$f_n = 0.626456$

Step 3.
Now, since the actual response desired is high-pass, the low-pass to high-pass transformation must be made as previously discussed in Low-Pass Transformation.

$$f_n \text{ (high-pass)} = \frac{1}{f_n \text{ (low-pass)}}, \quad Q_{HP} = Q_{LP}$$

∴ For Complex Poles:

$$f_n = \frac{1}{1.068853} = 0.935582$$

and Q = 1.7062
For Simple Pole: $f_n = \frac{1}{0.626456} = 1.596281$

Step 4.
Now, determine the actual (denormalized) frequency.
$f_o = f_c \times f_n = 2\text{kHz} \times 0.935582 = 1871.2\text{Hz}$

Step 5.
Refer to the Configuration Selection Guide. Since the gain required is positive, the HP output is not inverted with respect to the input. Therefore, the noninverting input configuration must be selected. Note that the HP output is not available with the Bi-Quad configuration.

Step 6.
Since $f_o < 8\text{kHz}$, Equations "A" would be used.

Step 7.
For the Complex Poles Stage of the filter, using the equations "A".

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{1871.2} = 85.08\text{k}\Omega$$

Step 8.
$f_o Q = 1871.2 \times 1.7062 = 3.19 \times 10^3$
$\therefore f_o Q < 10^5$
$\therefore Q_P = Q = 1.7062$

Step 9.
$A_{BP} = Q_P \times A_{HP} = 1.7062 \times 1 = 1.7062$

$$R_G = \frac{5.0 \times 10^4 \times 1.7062}{1.7062 \times 1.7062} = 29.3\text{k}\Omega$$

$$R_Q = \frac{5.0 \times 10^4}{2 \times 1.7062 - 1.7062 - 1} = 70.8\text{k}\Omega$$

The above obtained resistor values are for the complex pole pair of the first stage of the required active filter. The simple pole obtained as outlined below, using the uncommitted op amp in the UAF41 makes the second stage of the required filter.

For the simple pole f_n was obtained in step 3.
$f_n = 1.596281$
The actual (denormalized) frequency = $f_c \times f_n$
$= 2\text{kHz} \times 1.596281 = 3192.6\text{Hz}$

Now, $f = \frac{1}{2\pi RC}$

$$\therefore RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 3192.6} = 4.9851 \times 10^{-5}$$

Choosing C = 2200pF (or any convenient value),

$$R = \frac{4.9851 \times 10^{-5}}{2200 \times 10^{-12}} = 22.66\text{k}\Omega$$

Note:
R and/or C may be chosen in any convenient manner to obtain the desired RC product.

The overall circuit for the required filter is shown below:

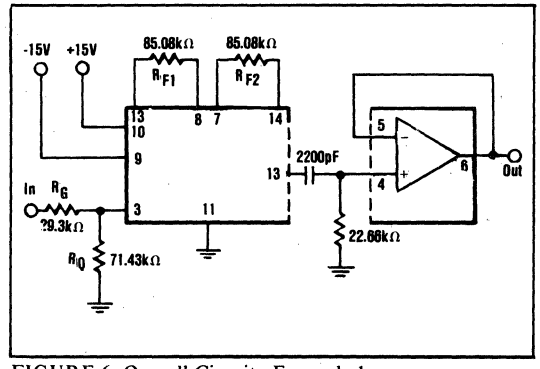


FIGURE 6. Overall Circuit - Example 1.

Example 2.

It is desired to design a 4-pole Butterworth, Bandpass Filter, with Q = 25, f_c = 19kHz and A_{BP} = 1.

Using the computer program shown in Table III, the following values of f_n and Q are obtained.

$$f_n = 1.0142435,\ Q = 35.36541$$

and

$$f_n = 0.9859565,\ Q = 35.35886$$

Using the above shown values of Q and f_n, we now will proceed to design the two stages of filter separately.

Any one of the three configurations shown in the Configuration Selection Guide can be used. We will select the noninverting input configuration.

For Stage 1.

f_o = 19kHz x f_n = 19kHz x 1.0142435 = 19270.6Hz

Since $f_o > 8$kHz, equations "B" would be used.

$$R_{F1} = R_{F2} = \frac{5.033 \times 10^7}{19270.6} = 2.6118k\Omega$$

$$f_oQ = 19270.6 \times 35.36541 = 6.815136 \times 10^5$$

Since $f_o > 10^5$, locate the corresponding f_oQ_P from the Performance Curves.

Divide f_oQ_P by f_o to obtain Q_P.

Thus Q_P = 48.78

$$R_G = \frac{5.0 \times 10^4 \times 35.36541}{1 \times 48.78} = 36.25k\Omega$$

$$R_Q = \frac{5.0 \times 10^4}{3.48 \times 47.78 - \frac{48.78}{35.37} - 1} = 298.7\Omega$$

For Stage 2.

Following the same procedure as shown for Stage 1 above, the values shown below are obtained.

$f_oQ = 6.624 \times 10^5$, using the Performance Curves,

Q_P = 48.04

$R_{F1} = R_{F2}$ = 2.6867kΩ

R_G = 36.8kΩ

and R_Q = 303.4Ω

The overall circuit for the required filter is shown below.

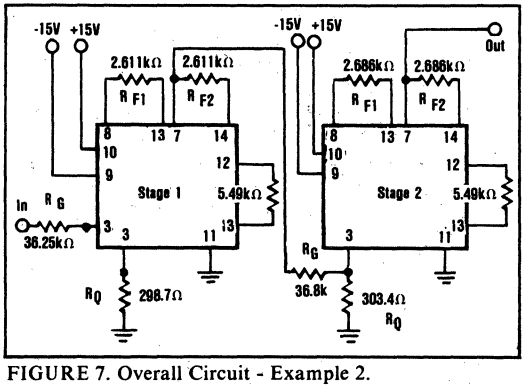


FIGURE 7. Overall Circuit - Example 2.

Example 3.

It is desired to design a 5-pole Bessel, Low-Pass Filter with f_c = 3.3kHz and A_{LP} = 1.

From Table I the following values of f_o and Q are obtained.

Complex Poles:

f_n = 1.55876
Q = 0.56354

f_n = 1.75812
Q = 0.91652

Simple Pole:

f_n = 1.50470

Using the above shown values of f_n and Q, we now will proceed to design the three stages of filter separately.

Any one of the three configurations can be used. We will select inverting configuration.

For Stage 1.

f_o = 3.3kHz x f_n = 3.3kHz x 1.55876 = 5144Hz

Since $f_o > 8$kHz, equations "A" would be used.

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{5144} = 30.95k\Omega$$

$$f_oQ = 5144 \times 0.56354 = 2.9 \times 10^3$$

$f_oQ > 10^5$, $\therefore Q_P = Q = 0.56354$

$A_{BP} = Q_P A_{LP} = 0.56354 \times 1 = 0.56354$

$$R_G = \frac{5 \times 10^4 \times 0.56354}{0.56354} = 50k\Omega$$

$$R_Q = \frac{5 \times 10^4}{2 \times 0.56354 + 0.56354 - 1} = 72.4k\Omega$$

For Stage 2.

f_o = 3.3kHz x f_n = 3.3kHz x 1.75812 = 5802Hz

Since $f_o > 8$kHz, equations "A" would be used.

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{5802} = 27.44k\Omega$$

$$f_oQ = 5802 \times 0.91652 = 5.32 \times 10^3$$

$f_oQ > 10^5$, $\therefore Q_P = Q = 0.91652$

$A_{BP} = Q_P A_{LP} = 0.91652 \times 1 = 0.91652$

$$R_G = \frac{5 \times 10^4 \times 0.91652}{0.91652} = 50k\Omega$$

$$R_Q = \frac{5 \times 10^4}{2 \times 0.91652 + 0.91652 - 1} = 28.58k\Omega$$

For Stage 3.

f = 3.3kHz x f_n = 3.3kHz x 1.50470 = 4966Hz

For the simple pole,

$$RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 4966} = 3.2049 \times 10^{-5}$$

3300pF (or any convenient value)

$$R = \frac{3.2049 \times 10^{-5}}{3300 \times 10^{-12}} = 9.71k\Omega$$

The overall circuit is shown below.

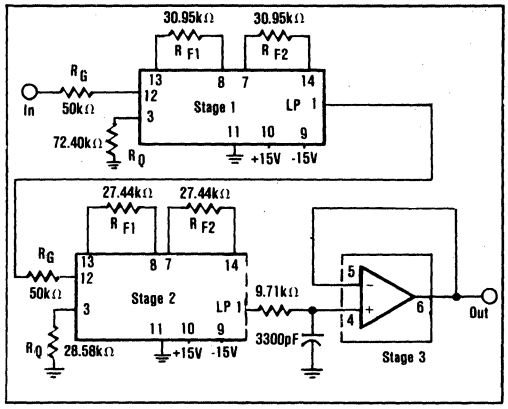


FIGURE 8. Overall Circuit - Example 3.

USEFUL REFERENCES

1. G.E. Tobey, J.G. Graeme and L.P. Huelsman, Operational Amplifiers: Design and Applications, (Chapter 8) McGraw Hill Book Co., 1971.
2. Yu Jen Wong, William E. Ott, Function Circuits: Design and Applications, (Chapter 6) McGraw Hill Book Co., 1976.
3. Richard W. Daniels, Approximation Methods for Electronic Filter Design, McGraw Hill Book Co., 1974.
4. Anatol I. Zverev, Handbook of Filter Synthesis, John Wiley and Sons Inc., New York, N.Y., 1967
5. Gabor C. Temes, Sanjit K. Mitra, Modern Filter Theory and Design, John Wiley and Sons, New York, N.Y., 1973

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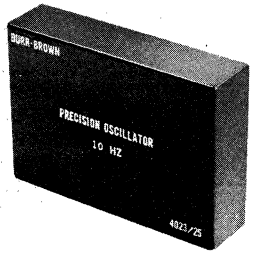


4023/25

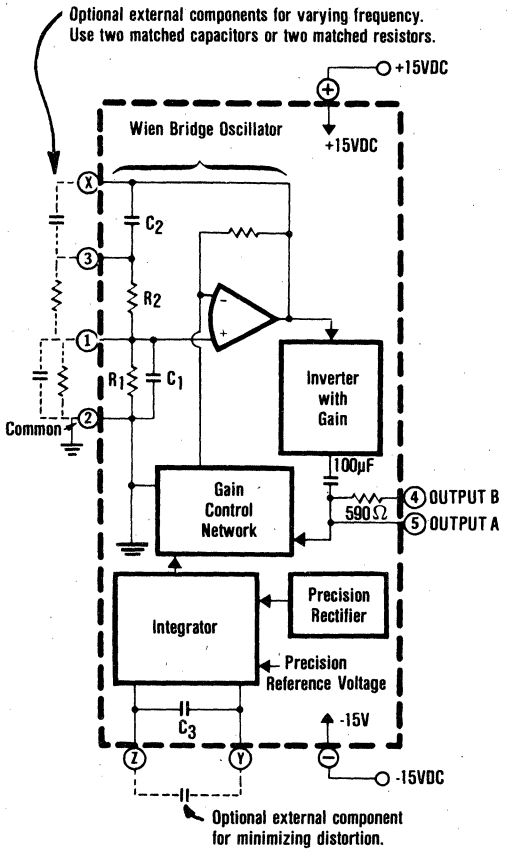
PRECISION OSCILLATOR

FEATURES

- FIXED FREQUENCY - 10Hz to 20kHz
- STABLE AMPLITUDE
- SINE WAVE OUTPUT
- LOW DISTORTION

DESCRIPTION

Model 4023/25 is an all solid-state, ultra-stable sine-wave oscillator. Both output amplitude and frequency are constant, and the stability of both with time and temperature variations is excellent. Internal high-performance Burr-Brown IC operational amplifiers are used to form a Wien bridge oscillator circuit and to regulate the output amplitude. The frequency of oscillation is within ±1% of the customer-specified value. If desired, external components may be added to trim the frequency to an exact value. Adding two external resistors will raise the output frequency and adding two external capacitors will lower the output frequency. With its small size, low distortion, and excellent frequency and amplitude stability, the Model 4023/25 is ideal for use as a reference oscillator in airborne or mobile equipment, special-purpose test equipment, and in telemetry systems. To order, specify Model 4023/25 and frequency.



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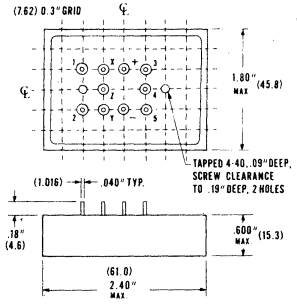
ELECTRICAL SPECIFICATIONS

Typical performance at 25°C and with rated supply unless otherwise noted.

FREQUENCY	
Range (1)	Customer specified, may be any value from 10 Hz to 20 kHz.
Accuracy	±1%, (May be trimmed by the user to less than ±1%)
Stability vs. Temperature	0.04%/°C (max.)
OUTPUT (3)	
Amplitude - Output A	6 Vrms
- Output B	3 Vrms (with 600 Ω load)
Amplitude Accuracy	±2%
Impedance - Output A	1 Ω
- Output B	600 Ω
Rated Load - Output A	1.2 kΩ
- Output B	600 Ω
Distortion (max.)	0.1%
AMPLITUDE STABILITY	
vs. Temperature (max.)	0.02%/°C
Noise and Jitter (max.)	0.02%
Long Term (max.)	0.1%
TEMPERATURE RANGE	
Operating, Rated Specifications	-25°C to +85°C
Storage	-55°C to +100°C
POWER REQUIREMENTS	
Rated Supply	±15 Vdc
Voltage Range at 25°C (2)	±12 Vdc to ±18 Vdc
Supply Drain (max.)	±40 mA

(1) To order, specify Model 4023/25 and frequency.
(2) The positive and negative supplies must be balanced within 2% of each other.
(3) The output may be taken from either Output A or Output B (not both).

MECHANICAL SPECIFICATIONS



Dimensions in millimeters are shown in parentheses.

Weight: 4 oz. maximum (120 grams)

Mating Connector: 1500MC (Optional)

OPERATING INSTRUCTIONS

With $R_1 = R_2$ and $C_1 = C_2$, the Wien-Bridge oscillator will provide a sine-wave oscillation of frequency:

$f_o = 1/2\pi RC$, where $R = R_1 = R_2$ and $C = C_1 = C_2$.

The frequency of oscillation, f_o, will be within ±1% of the nominal value specified by the customer. The frequency may be lowered by externally paralleling the internal capacitors C_1 and C_2; and the frequency may be raised by paralleling the internal resistors R_1 and R_2. The nominal values of C_1 and C_2 will be as follows:

Frequency f_o	C_1 and C_2
10Hz to 100Hz	0.1μF
101Hz to 1000Hz	0.01μF
1001Hz to 20kHz	0.001μF

It is important to pad both R_1 and R_2 or C_1 and C_2 by an equal amount to keep distortion within specifications.

If the frequency is lowered by a significant amount, it may be necessary to externally parallel the integrator capacitor C_3 to lower distortion of the output.

The range of frequency adjustment is approximately 2 decades (within 10kHz and 20kHz). For example, a 10Hz unit may be trimmed for a frequency of up to 1kHz or a 10kHz unit may be varied down to 100Hz. However, the distortion and amplitude stability specifications are guaranteed and tested only for the nominal frequency of oscillation. In general, the degradation in distortion and amplitude stability as the frequency is varied over a wide range is very small.

INSTALLATION

The Model 4023/25 is designed for installation on a flat mounting surface such as a chassis or printed circuit board. The gold-flashed pins may be hand or dip soldered; for plug-in installation, the Model 1500MC mating connector may be installed on the chassis. The unit may be secured to the mounting surface by means of two 4-40 machine screws inserted through the mounting surface not more than 3/16" into the tapped holes in the bottom.

Pin 1 and pin 3 must be shielded from external sources of electrical noise. The module is particularly sensitive to periodic noise near the resonant frequency. Also, if external bridge components are added to the Wien bridge terminals they must be physically near the 4023/25 module.

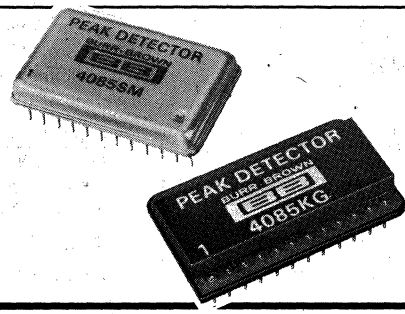
EXTERNAL CONNECTIONS

External connections are made to the gold-flashed pins on the unit. These connections include the Wien bridge, integrator feedback, output, and power supply termination and are made as follows:

Pin 1	Wien Bridge Terminals
Pin 2 Common	Wien Bridge Terminals
Pin 3	Wien Bridge Terminals
Pin X	Wien Bridge Terminals
Pin 4	Output B
Pin 5	Output A
Pin Y	Integrator Feedback Terminals
Pin Z	Integrator Feedback Terminals
(+)	Positive Power, +15VDC
(-)	Negative Power, -15VDC

BURR-BROWN®

4085



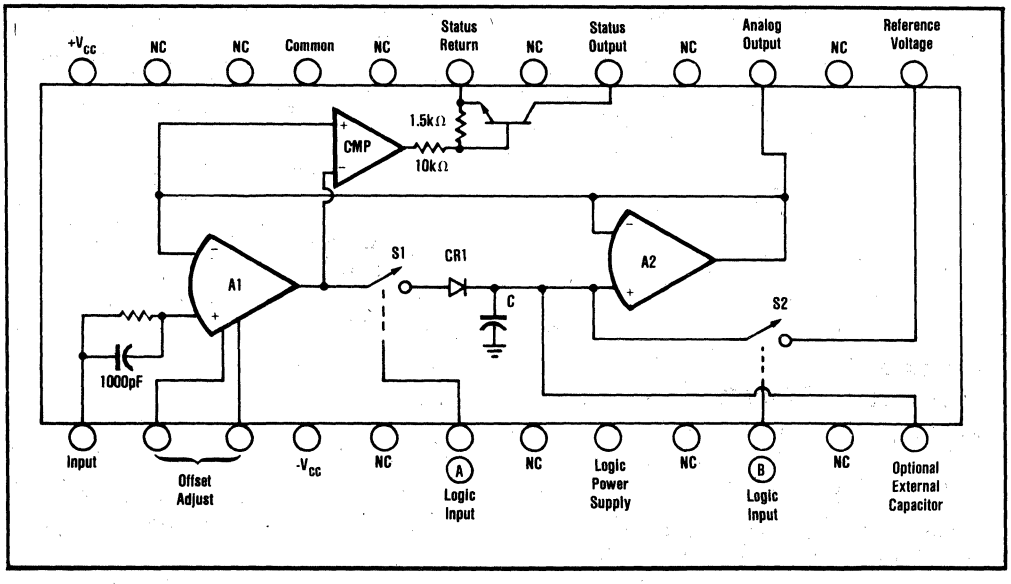
HYBRID MICROCIRCUIT PEAK DETECTOR

FEATURES:

- STORES TRANSIENT VOLTAGES
- COMPLETELY SELF-CONTAINED
- ACCURATE TO ±0.01%
- LOW DROOP ERRORS
- SMALL DIP PACKAGE

DESCRIPTION

The 4085 is a specialized sample/hold amplifier that tracks an input signal until a maximum amplitude is reached. That maximum value is held at the analog output, and the digital Status output indicates that a peak has been detected. The unit can then be commanded to hold that value, ignoring additional peaks, or reset to a user-specified reference voltage. The 4085 detects positive-going peaks from -10V to +10V and is available in a hermetic metal package and a low-cost ceramic package. Three models are available, specified for temperature ranges 0 to +70°C (4085KG), -25°C to +85°C (4085BM), and -55°C to +125°C (4085SM).



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SPECIFICATIONS

ELECTRICAL

Specification at T_A = +25°C and ±15VDC and +5VDC power supplies unless otherwise noted.

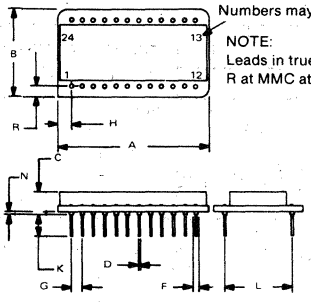
MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG INPUT				
Signal Inputs				
Operating Range	±10	|Vcc|-3		V
Absolute Maximum Range			±Vcc	V
Input Offset Voltage				
adjustable to zero			2	mV
Input Offset Voltage Drift		15	50	µV/°C
Input Bias Current		15	50	pA
Input Resistance		1		GΩ
Input Capacitance		8		pF
DIGITAL INPUT				
Logic Levels				
Logic "1"	+2.4 at 50nA, max			V
Logic "0"			+0.8 at 100µA, max	V
Truth Table	Logic Input A		Logic Input B	
Peak Detect Mode	1		0	
Hold Mode	0		0	
Reset	0		1	
TRANSFER CHARACTERISTICS				
Voltage Gain		1.0		V/V
ACCURACY				
DC Voltage Gain Error			±0.01	% of FSR(1)
Dynamic Accuracy to 300Hz		±0.01	±0.02	% of FSR
Dynamic Accuracy to 100Hz			±0.01	% of FSR
Temperature Coefficient of Gain Error		±3		ppm/°C
Feedthrough			±0.05	% of Step
Droop all units at T_A = +25°C (2)			±0.06	mV/msec
T_A = +70°C, 4085KG			±0.5	mV/msec
T_A = +85°C, 4085BM			±1.2	mV/msec
T_A = +125°C, 4085SM			±12.0	mV/msec
Power Supply Sensitivity, ±Vcc			±0.005	%/% Supply Variation
Logic Supply			±0.005	%/% Supply Variation
DYNAMIC PERFORMANCE				
Acquisition Time BM, SM			500	µsec
Acquisition Time KG			800	µsec
Slew Rate		0.5		V/µsec
Charge Offset(3)		0.5	1	mV
Status Delay at 500Hz		0.7	1	msec
Status Delay at 100Hz		1.2	2	msec

MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG OUTPUT				
Voltage Range	±10	|Vcc|-3		V
Output Current	5			mA
Output Resistance		0.2	0.5	Ω
Output Noise 10Hz to 100kHz		30		µV, rms
Output Load Capacitance	50	100		pF
STATUS OUTPUT				
Collector-emitter Voltage			+30	V
Collector Current			20	mA
DC Current Gain	50	100		mA/mA
V_{BE}		0.65		V
REFERENCE VOLTAGE				
Operating Range	±10	|Vcc|-3		V
Absolute Maximum Range			±Supply	V
Discharge Current(4)	5		30	mA
POWER SUPPLY REQUIREMENTS				
Rated Voltage		±15		V
Operating Range	±8		±18	V
Current Drain (I_{OUT} = 0)			±20	mA
Rated Logic Supply Voltage(5)		+5.0 ±0.5		V
Logic Supply Current				
(Logic A & B high)		3.0 ±0.3		mA
(Logic A & B = 0V)		4.4 ±0.5		mA
TEMPERATURE RANGE				
Specification				
4085KG	0		+70	°C
4085BM	-25		+85	°C
4085SM	-55		+125	°C
Operating				
4085KG	-25		+85	°C
4085BM	-55		+90	°C
4085SM	-55		+125	°C
Storage				
4085KG	-30		+90	°C
4085BM	-60		+100	°C
4085SM	-60		+150	°C

NOTES:

1. FSR = Full Scale Range, 20V for the 4085.
2. Equation for droop: $\text{Droop (mV/msec)} = \dfrac{100\text{pA} \times 2^{\left(\frac{T - 25°C}{11}\right)}}{3300\text{pF} + C_{EXT}\text{ (pF)}}$
3. Charge Offset is the charge transferred from the holding capacitor when the 4085 is switched to the hold mode.
4. Any circuitry connected to the reference pin should be capable of sinking the desired discharge current of the internal 3300pF holding capacitor plus any external capacitor. The discharge current range is the current limit imposed by an internal FET switch. It does not imply that the I_{DSS} of external circuitry must be designed to limit current to this range.
5. Logic Supply, pin 8, may be connected to higher supply voltages for operation with MOS or CMOS logic. Refer to "Operating Instructions".

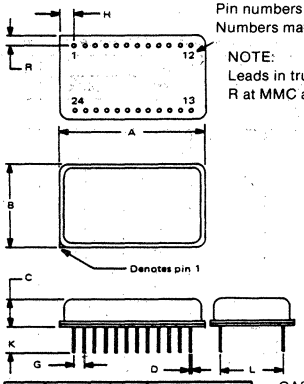
MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

ORDER NUMBER:
4085KG

CASE: Black Ceramic (alumina)
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz)

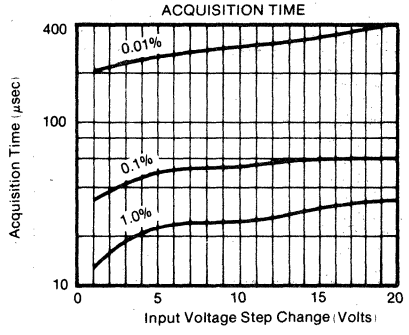


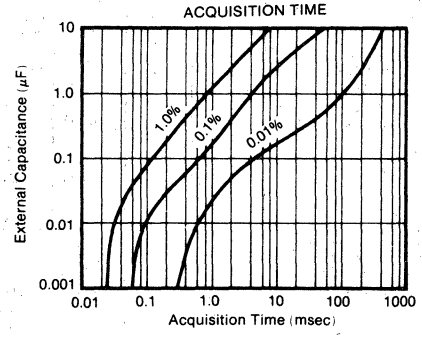
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

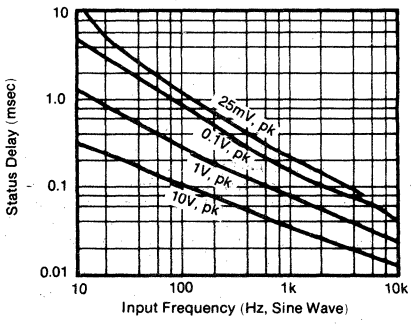
ORDER NUMBER:
4085BM
4085SM

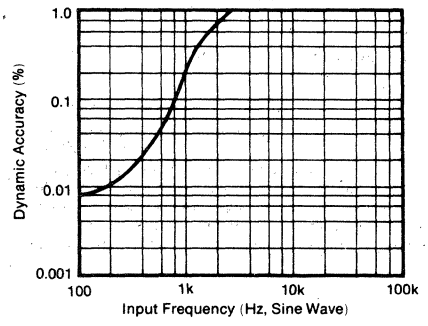
CASE: Kovar, Gold or Nickel plated
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz)

TYPICAL PERFORMANCE CURVES



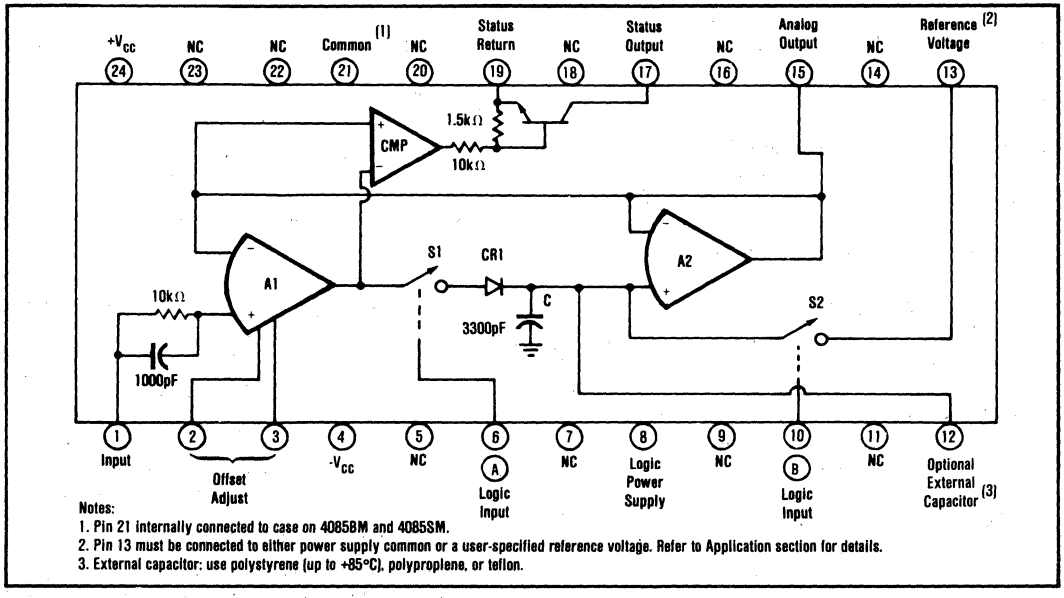






THEORY OF OPERATION

In the Peak Detect Mode (S1 closed, S2 open), the analog output tracks the analog input until a peak value is reached. When the input voltage falls below the magnitude of the peak voltage, CR1 becomes reversed biased, and the feedback loop between A1 and A2 is broken. At this point, the status output transistor turns on and the magnitude of the peak voltage is held on the analog output. In the Hold Mode (S1 open, S2 open), the current charging path from the output of A1 to the capacitor is opened. The output voltage is equal to the voltage stored in the capacitor even though the input voltage may become larger than the peak voltage. In the Reset Mode (S1 open, S2 open), the voltage on the capacitor will charge to whatever voltage is applied to the reference voltage input. If both S1 and S2 are closed at the same time, the output of A1 will be connected to the reference voltage input through a low impedance. This represents an illegal mode of operation, but will cause no damage to the unit.



Notes:
1. Pin 21 internally connected to case on 4085BM and 4085SM.
2. Pin 13 must be connected to either power supply common or a user-specified reference voltage. Refer to Application section for details.
3. External capacitor: use polystyrene (up to +85°C), polypropiene, or teflon.

FIGURE 1. 4085 Functional Diagram and Pin Configuration.

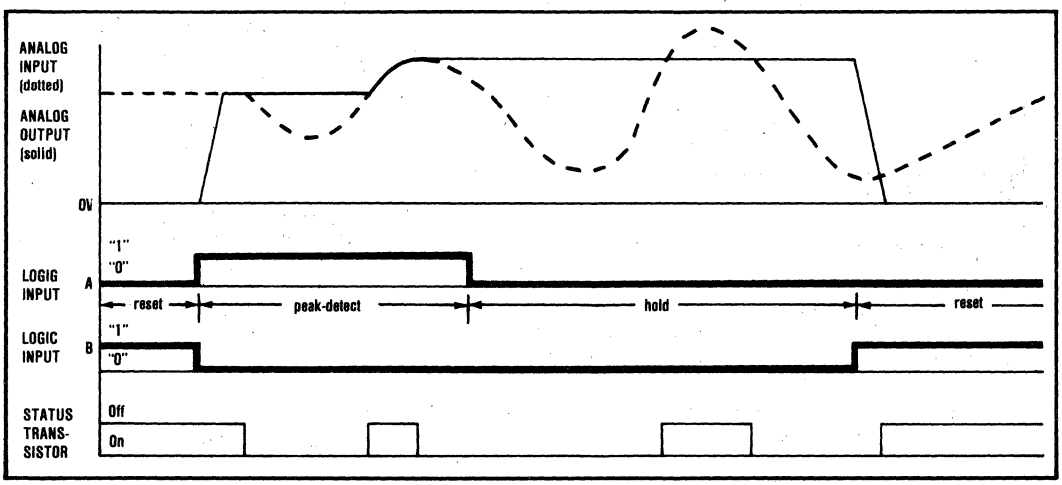


FIGURE 2. Timing Diagram For Peak-Detect Operation.

OPERATING INSTRUCTIONS

OFFSET VOLTAGE ADJUSTMENT

The ±2mV input offset voltage of the 4085 may be nulled to zero by using the circuit shown in Figure 3. With the 4085 in the Peak Detect Mode (logic input A = "1", logic input B = "0") apply zero volts to pin 1. Adjust the potentiometer until the output voltage is zero volts. Disconnect pin 12 after adjustment is made.

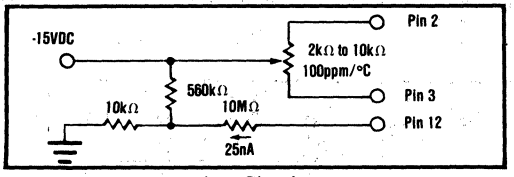


FIGURE 3. Offset Adjust Circuit.

POWER SUPPLY CONSIDERATIONS

The 4085 will operate as specified with power supplies from ±8VDC to ±18VDC. To minimize noise pickup, the supply inputs should be decoupled with 1μF tantalum capacitors located physically close to the unit.

DIGITAL INPUTS AND LOGIC SUPPLY

The digital inputs may be driven with TTL or CMOS logic. Pin 8 should be tied to the logic supply. The logic supply voltage (V_L) may also be provided by connecting pin 8 through a resistor of value R (kΩ) = 1.67 (V_{CC} - V_L)/V_L to the +V_{CC} ($V_{CC} \geq V_L$). The logic threshold voltage is equal to 0.4V_L - 0.7V.

INPUT FREQUENCY BANDWIDTH LIMITING

It is recommended that the input bandwidth be limited as much as possible by an RC section such as that shown in Figure 4. This is to limit noise spikes at the input that may cause erroneous readings. If detecting large pulse heights, a 5μsec time constant should be used. This will not degrade acquisition time or tracking accuracy for frequencies up to 500Hz. For input frequencies greater than 500Hz, a smaller time constant may be used.

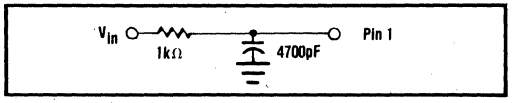


FIGURE 4. Input Bandwidth Limiting.

STATUS OUTPUT CHARACTERISTICS

The open-collector, open-emitter output transistor is a small signal, medium speed switching transistor similar to a 2N2222. To facilitate driving a variety of devices, the configuration of the status output has been left to the user's discretion.

The internal comparator shown in the block diagram (Figure 1) has an output characteristic as follows. Input signal track: $Z_{out} \approx \infty$; peak hold: V_{out} = +V_{CC} - 0.5V.

Several configurations are illustrated in Figures 5, 6, and 7. "Inverting" means logic "0" = peak has been detected. "Noninverting" means logic "1" = peak has been detected.

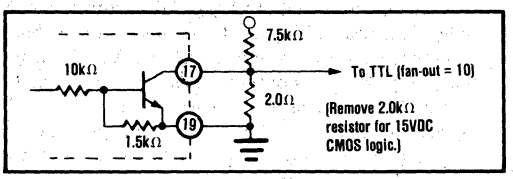


FIGURE 5. Inverting TTL (CMOS) Status Output.

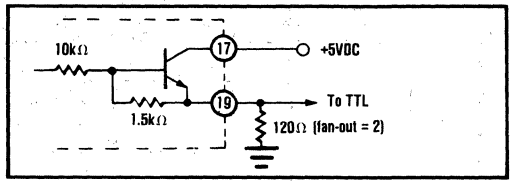


FIGURE 6. Noninverting TTL Status Output.

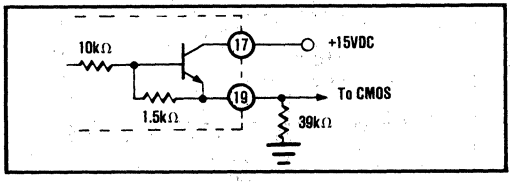


FIGURE 7. Noninverting CMOS Status Output.

DESIGNING IN HYSTERESIS

It may be desirable in some situations to have hysteresis in the circuit such that small peaks will not be detected, eliminating jitter in the Status output. This is possible through external components connected as shown in Figure 8. After a peak is detected, the input voltage must be slightly greater (determined by R1/R2) than the previous peak to cause the output to resume tracking the input. This hysteresis voltage is expressed by:

$$V_H = \frac{(V_{in} - V_E - 0.9V)\,R1}{R1 + R2}$$

The emitter voltage of the status transistor should be tied to a voltage sufficiently lower than the lowest expected peak to allow proper operation.

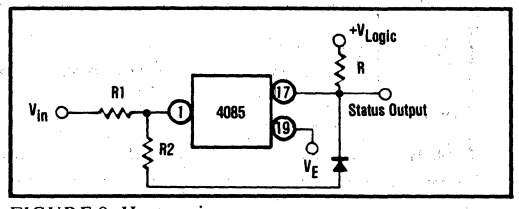


FIGURE 8. Hysteresis.

APPLICATIONS

PEAK CATCHER

This circuit detects and holds the first peak it encounters. After the first peak is detected, it automatically is switched to the Hold Mode. To reset the circuit for catching another peak, a 10μsec or longer positive logic pulse should occur at the Release Input. This will reset the peak detector to the desired voltage and put it in the peak-detect mode.

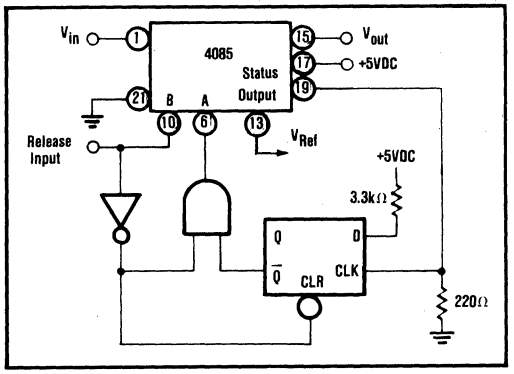


FIGURE 9. Peak Catcher.

NO-RIPPLE, FAST-SETTLING RMS-DC CONVERTER

If a waveform is known, the rms value of the signal may be computed from the peak value. In this circuit, the rms value is computed by the output amplifier from the peak value held by the 4085. The output in the circuit shown is updated manually. It may be updated automatically by replacing the switch circuit with an oscillator plus timing logic.

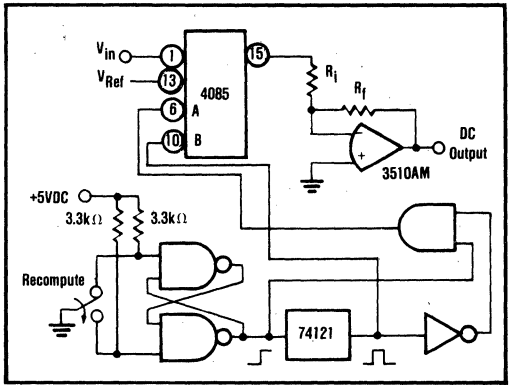


FIGURE 10. RMS-DC Converter.

INTERFACING TO A/D CONVERTER

Interfacing to an A/D converter is straightforward. The gating of the A/D converter command allows a conversion only if a peak has been detected and permits completion of each conversion. If a peak occurs while the A/D is converting, it will not be detected.

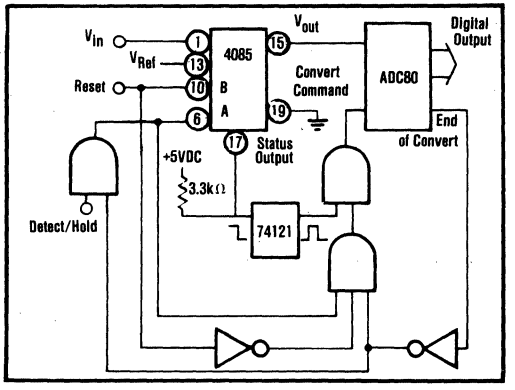


FIGURE 11. A/D Converter Interface.

PEAK-TO-PEAK DETECTOR

Figure 12 shows a circuit that will display the peak-to-peak voltage of an input waveform. The Status Output indicates that both positive and negative peaks have been detected and that the output is valid. The resistors around A3 should be matched to insure good common-mode rejection.

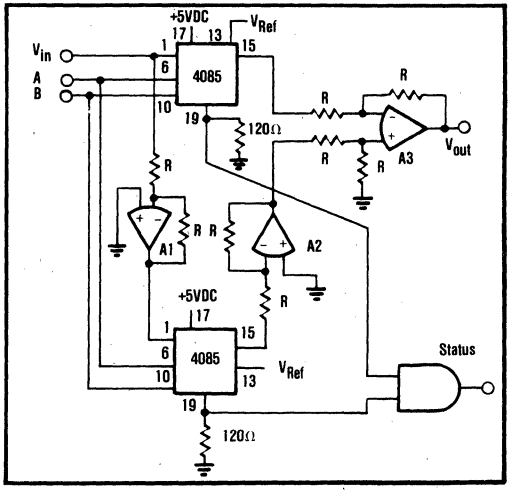


FIGURE 12. Peak-to-Peak Detector.

REFERENCE VOLTAGE

In the Reset Mode the voltage applied to pin 13 places an initial charge on the holding capacitor at the input to A2 (see Figure 1). This threshold voltage may be any value between positive and negative 10 volts. For most applications pin 13 will be tied to power supply common. This sets V_{Ref} to 0 volts. The 4085 will then capture peaks greater than 0 volts.

Pin 13 must be connected to either power supply common or to a user-specified reference voltage. If this connection is not made the 4085 will appear to have excessive droop.

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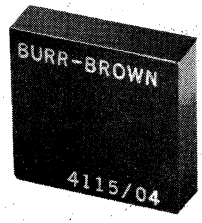


4115/04

WINDOW COMPARATOR

FEATURES

- ADJUSTABLE LIMITS FOR "HIGH", "LOW", AND "GO"
- UP TO 200mA LOAD CAPABILITY (each output)
- INPUT PROTECTION

APPLICATIONS

- PRODUCTION LINE TESTING
- TEMPERATURE CONTROLS
- INDUSTRIAL ALARMS
- LEVEL DETECTORS/CONTROLS

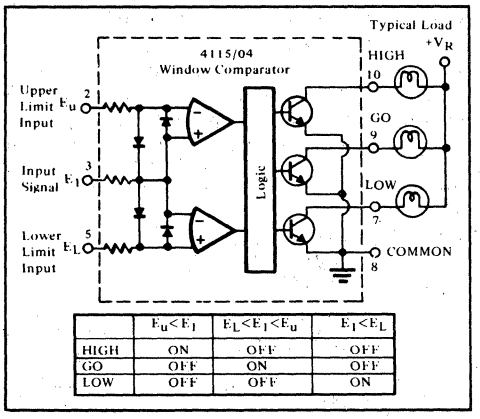
DESCRIPTION

Model 4115/04 is a hybrid IC window comparator in a double width DIP. The unit has three inputs - one for a voltage that sets the upper limit, another for a voltage that sets the lower limit, and a signal input. There are three mutually exclusive outputs - HIGH, LOW and GO. When an output is ON it will sink up to 200mA of current. This input diode protected device is designed to work with input voltages of up to ±10V, and will not be harmed by voltages to ±15V. The 4115/04 will drive a variety of loads including lamps, relays, MOS circuitry, and high noise immunity logic as well as DTL and TTL devices.

INSTALLATION

Separate connections should be made from each power supply common (+15VDC, -15VDC and V_R) to the 4115/04 common (pin 8).

To avoid unwanted pickup or chattering it may be necessary to include bypass capacitors from the ±15V supply pins (13 and 14) to the module common pin (8).



	$E_U<E_I$	$E_L<E_I<E_U$	$E_I<E_L$
HIGH	ON	OFF	OFF
GO	OFF	ON	OFF
LOW	OFF	OFF	ON

Model 4115/04 Transfer Characteristics.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

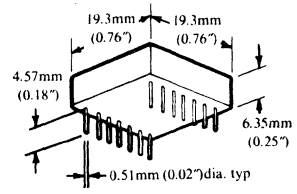
ELECTRICAL SPECIFICATIONS

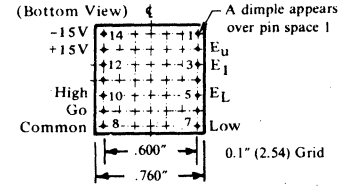
Typical performance at 25°C and with rated supply unless otherwise noted.

MODEL	4115 04	Units
INPUT		
All Inputs	±10V into 6kΩ (min)	
Maximum Safe Input	±15	V
ACCURACY		
D.C. Resolution (min)	±0.2	mV
Voltage Offset (referred to input)		
at 25°C (max)	±2	mV
vs Temperature (max)	±30	μV °C
Over Temperature Range (max)	±7	mV
vs Power Supply	±50	μV V
Switching Speed		
Total Switching Time at 30mV		
Overdrive	300	μsec
OUTPUT		
Impedance to COMMON from all Outputs		
OFF state	> 1	MΩ
ON state	3	Ω
Load Supply Voltage (V_R)	0 to +30	V
Load Current		
Steady State	+200	mA
Transient (absolute maximum)		
1 Second Duration	+400	mA
Saturation Voltage (V_{C1}) (max)		
at 200mA	0.7	V
TEMPERATURE RANGE		
Rated Specifications	-25 to +85	°C
Derated Performance	-40 to +85	°C
Storage	-55 to +100	°C
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltage	±15	VDC
Derated Performance	-12 to ±18	VDC
Quiescent Drain (max)	±15	mA

To achieve best results use stable quiet reference sources and drive signal input from low impedance source. Noise and drift in input sources readily masks the inherently high resolution of the device.

MECHANICAL SPECIFICATIONS





WEIGHT: 0.24 oz. (6.80 grams)
MATERIAL: Black Exoxy
PIN: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
CONNECTOR: Fits any commercial dual-in-line connector.

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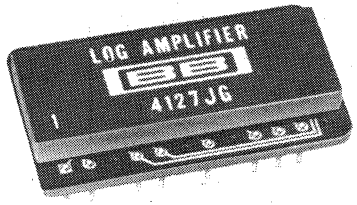


4127

LOGARITHMIC AMPLIFIER

FEATURES

- **ACCEPTS INPUT VOLTAGES OR CURRENTS OF EITHER POLARITY**
- **WIDE INPUT DYNAMIC RANGE**
  6 Decades of current
  4 Decades of voltage
- **VERSATILE**
  Log, antilog, and log ratio capability
- **SMALL SIZE**
  Double wide DIP
- **LOW COST**

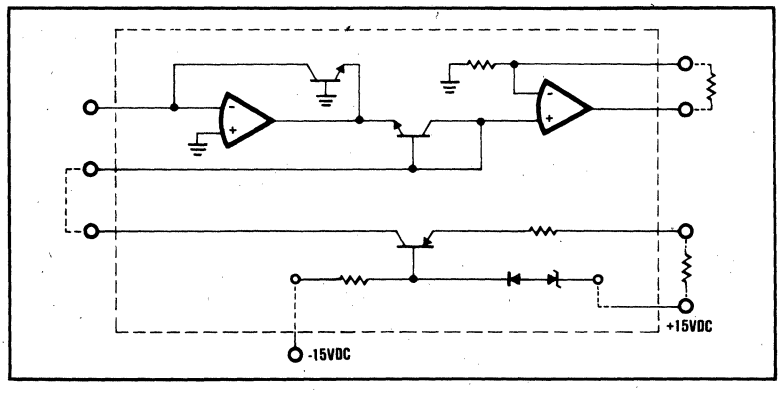
DESCRIPTION

Packaged in a ceramic double wide DIP, the 4127 is the first hybrid logarithmic amplifier that accepts signals of either polarity from current or voltage sources. A special purpose monolithic chip, developed specifically for logarithmic conversions, functions accurately for up to six decades of input current and four decades of input voltage. In addition, a newly developed current inverter and a precise internal reference allow pin programming of the 4127 as a logarithmic, log ratio, or antilog amplifier.

To further increase its versatility and reduce your system cost, the 4127 has an uncommitted operational amplifier in its package that can be used as a buffer, inverter, filter, or gain element.

The 4127 is available with initial accuracies (log conformity) of 0.5% and 1.0%, and operates over an ambient temperature range of -10°C to +70°C.

With its versatility and high performance, the 4127 has many applications in signal compression, transducer linearization, and phototube buffering. Manufacturers of medical equipment, analytical instruments, and process control instrumentation will find the 4127 a low cost solution to many signal processing problems.



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SPECIFICATIONS

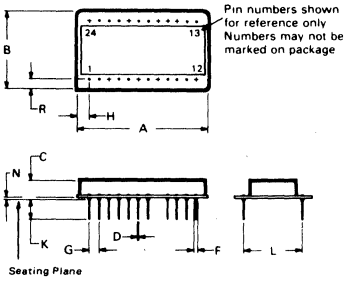
ELECTRICAL

Typical specifications at +25°C with rated supplies unless otherwise noted.

MODEL	4127KG	4127JG
ACCURACY(1), % of FSR		
Current Source Input: 1nA to 1mA	0.5% max	1% max
Voltage Input: 1mV to 10V	0.5% max	1% max
INPUT		
Current Source Input, Pin 4	+1nA to +1mA	
Current Source Input, Pin 7	-1nA to -1mA	
Reference Current Input, Pin 2	+1μA to +1mA	
Absolute Maximum Inputs	±10mA or ±Supply Volts	
OUTPUT		
Voltage	±10V	
Current	±5mA	
Impedance	10Ω	
FREQUENCY RESPONSE		
-3dB Small Signal at Current Input		
of 100μA	90kHz	
of 10μA	50kHz	
of 1μA	5kHz	
of 100nA	250Hz	
of 10nA	80Hz	
Step Response to within ±1% of Final Value (I_R = 1μA, A = 5)	10msec	
STABILITY		
Scale Factor Drift (ΔA/°C)	±0.0005A/°C	
Reference Current Drift (ΔI_R/°C)	±0.001 I_R/°C for $I_R \geq 1\mu A$ ±0.003 I_R/°C for 400nA < I_R < 1μA	
Input Offset Current Drift (ΔI_S/°C)	10pA at +25°C, Doubles Every 10°C	
Input Offset Voltage Drift	±10μV/°C	
Accuracy vs. Supply Variation		
Reference Current	±0.001I_R/V	
Input Offset Voltage	±300μV/V	
Input Noise - Current Input	1pA, rms, 10Hz to 10kHz	
Input Noise - Voltage Input	10μV, rms, 10Hz to 10kHz	
UNCOMMITTED OP AMP CHARACTERISTICS		
Input Offset Voltage	5mV	
Input Bias Current	40nA	
Input Impedance	1MΩ	
Large Signal Voltage Gain	85dB	
Output Current	5mA	
TEMPERATURE RANGE		
Specification	0°C to +60°C	
Operating	-10°C to +70°C	
Storage	-55°C to +125°C	
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltages	±15VDC	
Supply Voltage Range	±14VDC to ±16VDC	
Supply Current Drain		
at Quiescent, max	±20mA	
at Full Load, max	±26mA	

NOTE:
1. Log conformity at 25°C.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

CASE: Ceramic
MATING CONNECTOR: 245MC
WEIGHT: 56 grams (2 oz.)
ORDER NUMBER: 4127KG
4127JG

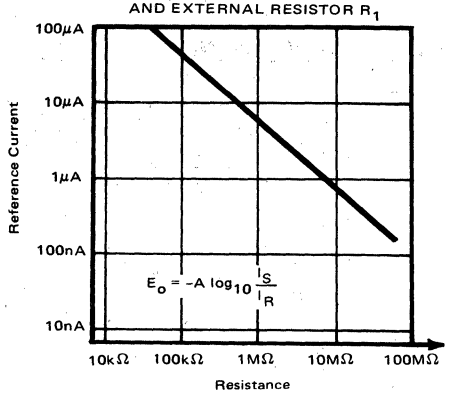
PIN CONNECTIONS

1. I_{REF} OUTPUT
2. I_{REF} INPUT
3. NO PIN PRESENT
4. +I INPUT *
5. CURRENT INVERTER OUTPUT*
6. NO PIN PRESENT
7. CURRENT INVERTER INPUT
8. NO PIN PRESENT
9. OP AMP +INPUT
10. OP AMP -INPUT
11. OP AMP OUTPUT
12. NO PIN PRESENT
13. MAKE NO CONNECTION
14. NEGATIVE SUPPLY
15. NO PIN PRESENT
16. NO PIN PRESENT
17. NO PIN PRESENT
18. LOG OUTPUT
19. GAIN ADJUST
20. NO PIN PRESENT
21. COMMON
22. POSITIVE SUPPLY
23. I_{REF} BIAS
24. NO PIN PRESENT

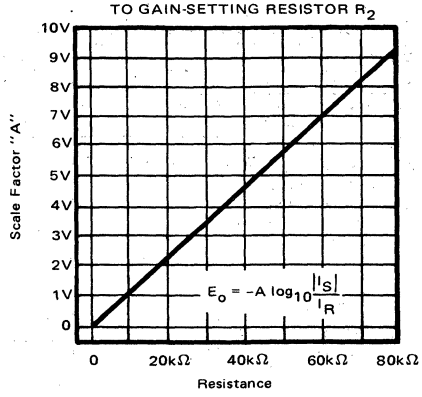
*Pins 4 and 5 are internally connected.

TYPICAL PERFORMANCE CURVES

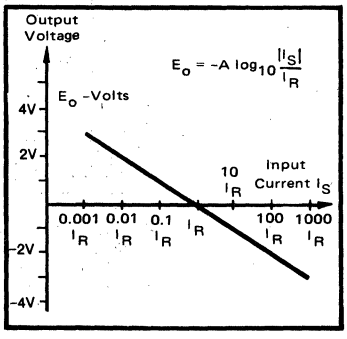
RELATIONSHIP OF REFERENCE CURRENT I_R AND EXTERNAL RESISTOR R_1



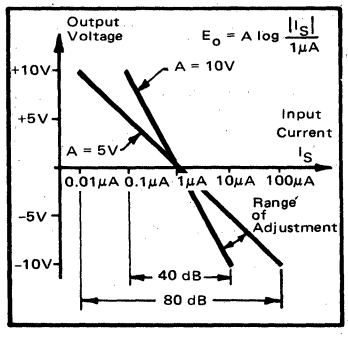
RELATIONSHIP OF SCALE FACTOR "A" TO GAIN-SETTING RESISTOR R_2



LOG RELATIONSHIP OF $\frac{|I_S|}{I_R}$ AND OUTPUT VOLTAGE IN TERMS OF "A"



RELATIONSHIP OF $\frac{|I_S|}{I_R}$ TO OUTPUT VOLTAGE FOR I_R = 1μA AND A = 5V AND 10V



DISCUSSION OF SPECIFICATIONS

ACCURACY

The deviation from the ideal output voltage defined as a percent of the full scale output voltage.

INPUT/OUTPUT RANGE

The log relationships of $-A \log \frac{I_S}{I_R}$ and $-A \log \frac{E_S}{I_R R}$ are subject to the constraints specified. The 4127 can be operated with inputs lower than those given, but the accuracy will be degraded.

FREQUENCY RESPONSE

The small-signal frequency response varies considerably with signal level and scaling, so the frequency response is specified under several different operating conditions.

STABILITY

The use of a monolithic transistor quad and low-drift op amps minimizes drift, but some drift remains in the scale-factor, reference current, and input offset. Input offset consists of a bias current plus the op amp input voltage offset divided by the signal source resistance. Also, there is some slight drift in conformity to the log function and in output amplifier offset, but this is generally negligible.

THEORY OF OPERATION

The 4127 is a complete logarithmic amplifier that can be pin-programmed to accept input currents or voltages of either polarity. By making use of the internal current inverter, reference current generator, log ratio element, and uncommitted op amp, you can generate a variety of logarithmic functions, including the log ratio of two signals, the logarithm of an input signal, or the antilog of an input signal. The unique FET-input current-inverting element removes the polarity limitations present in most conventional log amplifiers.

Utilizing the inherent exponential characteristics of transistor functions, the 4127 calculates accurate log functions for input currents from 1nA to 1mA, or input voltages from 1mV to 10V. Carefully matched monolithic quad transistors and temperature sensitive gain elements are used to produce a log amplifier with excellent temperature characteristics.

A functional diagram of the 4127 circuit is shown in Figure 1. In addition to the basic log amplifier, the 4127 contains a separate internal current source, a current inverter, and an uncommitted operational amplifier. The current inverter accurately converts negative input current to a positive current of equal magnitude.

The 4127 is capable of accurately logging input current over a 120dB range but to use this full range, good shielding practice must be followed. A current source input is, by definition, a high impedance source and is therefore subject to electrostatic pickups.

The input op amps A_1 and A_3 have FET input stages for low noise and very-low input bias current. The op amp A_1 will make the collector current of Q_1 equal to the signal input current I_S, and the collector current of Q_2 will be the reference input current I_R.

From the semiconductor junction characteristics, the base-to-emitter voltage will be

$$V_{BE} \approx \frac{m\,K\,T}{q} \ln \frac{I_C}{I_L}$$, where I_C = Collector current
I_L = Reverse saturation current
q, m, K = Constants
T = Absolute temperature

$$\text{So } E_1 = -\frac{m\,K\,T_1}{q} \ln \frac{I_S}{I_{L1}} \quad \text{and } E_2 - E_1 = \frac{m\,K\,T_2}{q} \ln \frac{I_R}{I_{L2}}$$

If the transistors Q_1 and Q_2 are at the same temperature and have matched characteristics then

$$E_2 = \frac{m\,K\,T}{q}\left[\ln \frac{I_R}{I_L} - \ln \frac{I_S}{I_L}\right]$$

$$E_2 = \frac{-m\,K\,T}{q} \ln \frac{I_S}{I_R}$$

The output op amp A_2 provides a voltage gain of approximately $(R_T + R_2)/R_T$, and the value of $(mKT)/q$ is about 26mV at room temperature. Since resistor R_T varies with temperature to compensate for gain drift, the output voltage E_o expressed as a log will be

$$E_o = -A \log_{10} \frac{I_S}{I_R}$$

$$\text{where } A \approx \frac{R_T + R_2}{R_T}\,(26\text{ mV})\frac{1}{0.434},\ R_T \approx 520\Omega$$

The external resistor R_1 sets the reference current I_R and resistor R_2 sets the scale-factor "A". R_1 and R_2 must be trimmed to the desired values, but the approximate relationships are shown in Typical Performance Curves.

The relationship between the input current I_S and the output voltage E_o in terms of the externally adjusted parameters I_R and "A" is illustrated in Typical Performance Curves. This relationship is, of course, restricted to values of I_S between 1nA and 1mA and output voltages of less than ±10V.

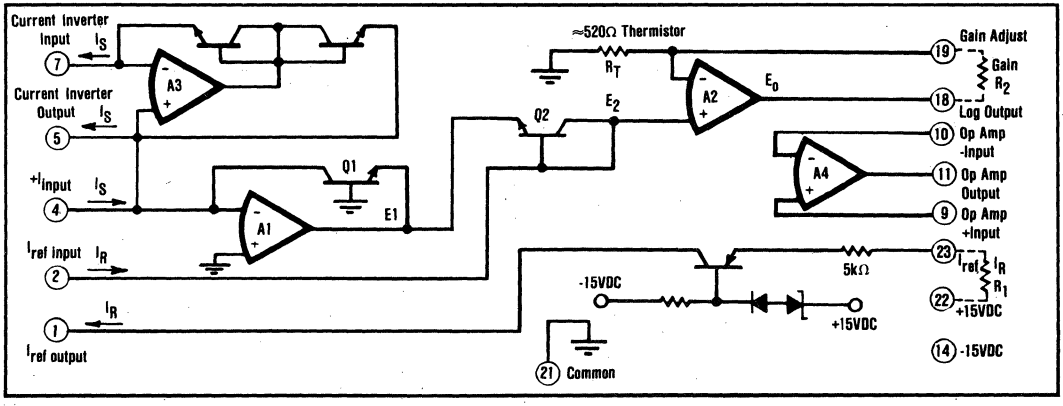


FIGURE 1. Functional Diagram.

CHOOSING THE OPTIMUM SCALE FACTOR AND REFERENCE CURRENT

To minimize the effects of output offset and noise, it is usually best to use the full ±10V output range. Once an output range of ±10V has been chosen, then "A" and I_R can be determined from the min/max of the input current I_S.

$$E_o = -A \log \frac{I_S}{I_R}, \text{ where } I_{min} < I_S < I_{max}$$

The output range of ±10V for an input range of I_{min} to I_{max} means that

$$+10 = -A \log \frac{I_{min}}{I_R} \text{ and } -10 = -A \log \frac{I_{max}}{I_R}$$

Adding these two equations together

$$\log \frac{I_{max} I_{min}}{I_R^2} = 0, \text{ or } I_R = \sqrt{I_{max} I_{min}}$$

The value for A can be found from:

$$10 = A \log \frac{I_{max}}{\sqrt{I_{max} I_{min}}}$$

In terms of the input current range for I_S, the values for I_R and A that will provide a full ±10V output swing are:

$$I_R = \sqrt{I_{max} I_{min}} \text{ and } A = \frac{10}{\log \frac{I_{max}}{I_R}}$$

Example: Assume that I_{min} is +10nA and I_{max} is +100μA.

This is an 80dB range.

$$I_R = \sqrt{I_{max} I_{min}} = \sqrt{(10^{-4})\ (10^{-8})} = 10^{-6}, \text{ or } 1\mu A.$$

$$\frac{I_{max}}{I_R} = \frac{10^{-4}}{10^{-6}} = 100$$

$$\log \frac{I_{max}}{I_R} = 2 \quad \text{So } A = 5$$

For an I_R of 1μA and A of 5,

$$E_o = -5 \log \frac{I_S}{1\mu A}$$

CONNECTION DIAGRAMS

Transfer function is $E_o = -A \log \frac{I_1}{I_R}$ where I_1 is a positive input current and I_R is the resistor-programmed internal reference current (see Figure 2).

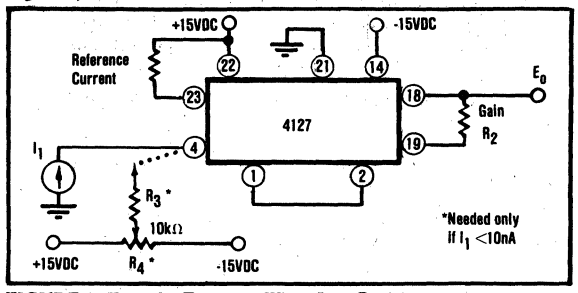


FIGURE 2. Transfer Function When I_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $I_1 = I_R$, adjust R_1 such that $E_o = 0$.
3. Apply $I_1 = I_{max}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $I_{1min} \geq 10nA$. Otherwise, apply $I_1 = 1nA$, make $R_3 = 1k\Omega$* and adjust R_4 for the proper output voltage.

Transfer function is $E_o = -A \log \frac{|I_1|}{I_R}$ where I_1 is a negative input current and I_R is the resistor-programmed internal reference current (see Figure 3).

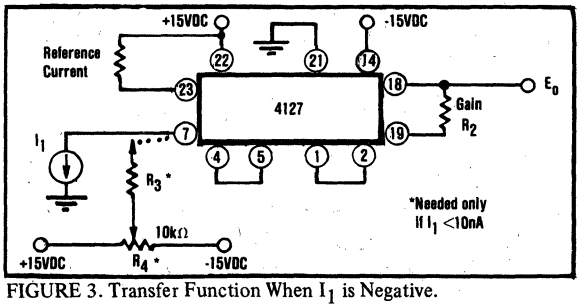


FIGURE 3. Transfer Function When I_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $|I_1| = I_R$ adjust R_1 such that $E_o = 0$.
3. Apply $|I_1| = I_{max}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{1min}| \geq 10nA$. Otherwise, apply $|I_1| = 1nA$, make $R_3 = 1k\Omega$* and adjust R_4 for the proper output voltage.

* Single resistor recommended. Voltage divider network difficult to use due to amplifier offset voltage. RF500-108, 1GΩ resistor available from Burr-Brown.

CONNECTION DIAGRAMS [CONT]

Transfer function is $E_0 = -A \log \frac{E_1}{R_4 I_R}$, where E_1 is a positive input voltage and I_R is the resistor-programmed internal reference current (see Figure 4).

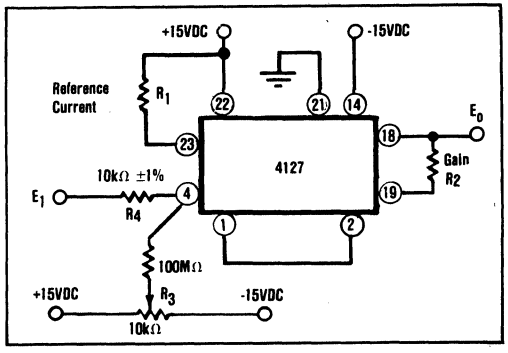


FIGURE 4. Transfer Function When E_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $E_1 = I_R$ (10kΩ), adjust R_1 such that $E_0 = 0$.
3. Apply $E_1 = E_{max}$, adjust R_2 for the proper output voltage.
4. Apply $E_1 = E_{min}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_0 = -A \log \frac{|E_1|}{R_4 I_R}$, where E_1 is a negative input voltage and I_R is the resistor-programmed internal reference current (see Figure 5).

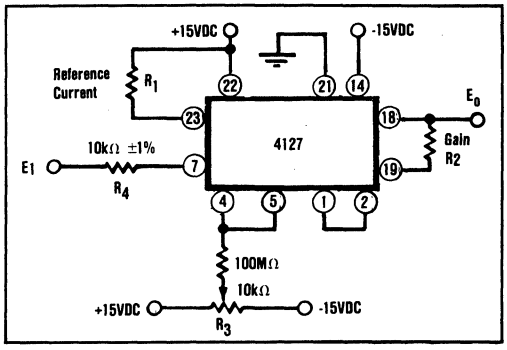


FIGURE 5. Transfer Function When E_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $|E_1| = I_R$ (10kΩ), adjust R_1 such that $E_0 = 0$.
3. Apply $|E_1| = E_{max}$, adjust R_2 for the proper output voltage.
4. Apply $|E_1| = E_{min}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_0 = -A \log \frac{|I_1|}{|I_2|}$ with I_1 and I_2 negative; $|I_1| \geq 1nA, |I_2| \geq 1\mu A$ (see Figure 6).

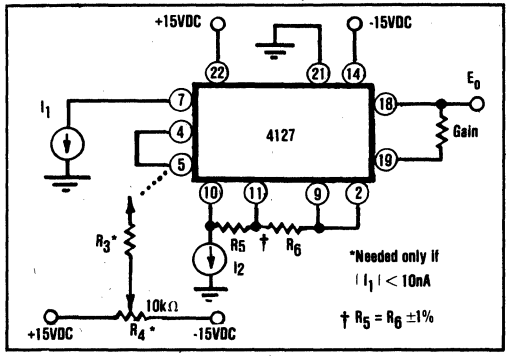


FIGURE 6. Transfer Function When I_1 and I_2 are Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if I_1 min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with R_4 =10kΩ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of ±5mV, it is not practical to use a T - network to replace R_3.

Transfer function is $E_0 = -A \log \frac{|I_1|}{I_2}$ with I_1 negative, I_2 positive; $|I_1| \geq 1nA$, $I_2 \geq 1\mu A$ (see Figure 7).

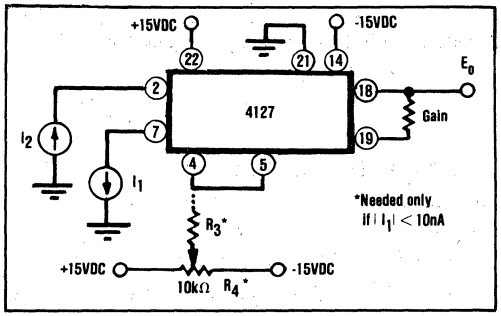


FIGURE 7. Transfer Function When I_1 is Negative, I_2 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $|I_1|$min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with $R_4 = 10k\Omega$ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm$5mV, it is not practical to use a T - network to replace R_3.

Transfer function is $E_0 = -A \log \frac{I_1}{I_2}$ with I_1 and I_2 positive; $I_1 \geq 1nA$, $I_2 \geq 1\mu A$ (see Figure 8).

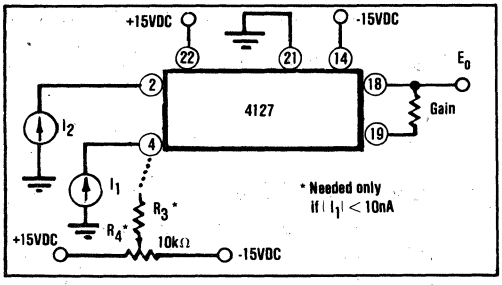


FIGURE 8. Transfer Function When I_1 and I_2 are Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if I_1 min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with $R_4 = 10k\Omega$ and $R_3 = 10^9\Omega$. Adjust R4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm$5mV, it is not practical to use a T - network to replace R_3.

ANTILOG OPERATION

The 4127 can also perform the antilog function. The output is connected through a resistor R_0 into the current input, pin 4. The input signal is connected through a gain resistor to pin 19 as shown in Figure 9.

These connections form an implicit loop for computing the antilog function. From the block diagram of Figure 1, the voltage at the inverting input of the output amplifier A2 must equal E_2, so

$$E_2 \approx \frac{R_T}{R_T + R_2} E_S, \quad R_T \approx 520\Omega$$

Since the output is connected through R_0 to pin 4, the current I_S will equal E_0/R_0 and E_2 will be

$$E_2 = -\frac{m K T}{q} \ln \frac{E_0}{R_0 I_R}$$

Combining expressions for E_2 gives the relationship

$$\frac{R_T}{R_T + R_2} E_S = -\frac{m K T}{q} \ln \frac{E_0}{R_0 I_R}$$

$$-\frac{E_S}{A} = \log \frac{E_0}{R_0 I_R}$$

where

$$A \approx \frac{R_T + R_2}{R_T} (26mV) \frac{1}{0.434}$$

$$E_0 = R_0 I_R \text{ Antilog} - \frac{E_S}{A}$$

Setting R_0 and I_R will set the scale factor. For example, an R_0 of 1MΩ and I_R of 1μA will give a scale factor of unity and

$$E_0 = \text{Antilog} - \frac{E_S}{A}$$

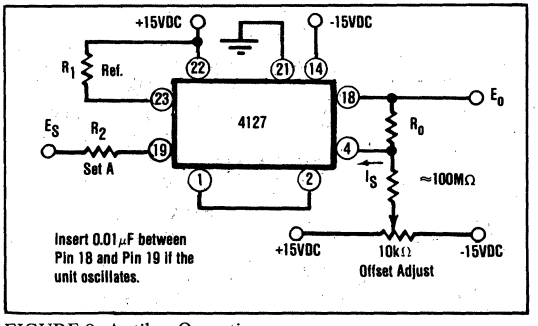


FIGURE 9. Antilog Operation.

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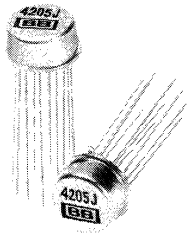

4203
4205

Integrated Circuit MULTIPLIER-DIVIDERS

FEATURES

- LASER-TRIMMED
  Requires No Adjustment
- GUARANTEED ACCURACY - 1% or 2%
- SELF-CONTAINED
  No Additional Amplifiers
- FAST SLEWING - 25V/μsec
- SMALL PACKAGE - TO-100

APPLICATIONS

- MULTIPLICATION, DIVISION, SQUARING, SQUARE ROOTS
- RMS MEASUREMENTS
- FREQUENCY DOUBLER
- BALANCED MODULATOR AND DEMODULATOR
- ELECTRONIC GAIN CONTROL
- FUNCTION GENERATOR AND LINEARIZING CIRCUITS
- PROCESS CONTROL SYSTEMS

DESCRIPTION

Burr-Brown Models 4203 and 4205 are integrated circuit multipliers designed for general purpose usage. In addition to four-quadrant multiplication they also perform division and square rooting of analog signals, requiring no additional amplifiers in performing the above functions. They are laser-trimmed prior to final packaging and are guaranteed to their rated accuracy with no external components. This is a distinct advantage from the standpoints of cost and reliability.

These multipliers contain their own zener-regulated references and, as a result, are much less sensitive to supply voltage variation than were earlier IC multipliers. The fast (25V/μsec) slew rate and 1MHz bandwidth are key performance factors for applications where delay phase shift must be minimized. Harmonic distortion of the 4203 and 4205 remain low for frequencies well above 100kHz, an important asset in modulation applications.

Other desirable features are hermetic TO-100 package (10-pin version of TO-99) and wide temperature range of operation. The 4203S and 4205S are specified for operation over the full MIL temperature range.

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SPECIFICATIONS

ELECTRICAL

Typical at +25°C with rated power supplies unless otherwise noted.
Percent specifications refer to % of full scale (10V).

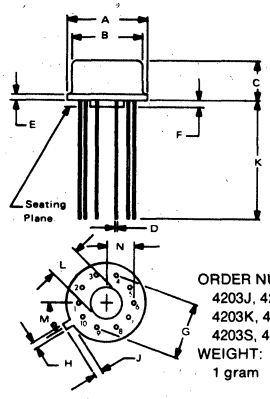
MODEL	4203J/4205J	4203K/4205K	4203S/4205S
OUTPUT FUNCTION 4203	XY/10		
4205	$(X_1 - X_2)(Y_1 - Y_2)/10$		
TOTAL ERROR*			
Internal Trim	2%, max	1%, max	1%, max
External Trim	1%	0.6%	0.6%
vs Temperature		0.04%/°C	
vs Supply		0.2%/%	
INDIVIDUAL ERRORS			
Output Offset at +25°C (X = Y = 0)	20mV	20mV	20mV, max
vs Temperature (Operating Range)		0.4mV/°C	
vs Supply		10mV/%	
Scale Factor Error	1%	0.6%	0.6%
vs Temperature (Operating Range)		0.04%/°C	
vs Supply		0.1%/%	
Nonlinearity			
X(X = 20V, p-p; Y = ±10VDC)	0.8%	0.5%	0.5%
Y(Y = 20V, p-p; X = ±10VDC)		0.2%	
Feedthrough at 50Hz			
X = 0, Y = 20V, p-p (Internal Trim)		50mV, p-p	
(External Trim)		20mV, p-p	
vs Temperature		1mV, p-p/°C	
Y = 0, X = 20V, p-p (Internal Trim)		50mV, p-p	
(External Trim)		20mV, p-p	
vs Temperature		2mV, p-p/°C	
AC PERFORMANCE			
Slew Rate		25V/μsec	
-3dB Small Signal Bandwidth		1MHz	
1% Amplitude Error		40kHz	
1% Vector Error (0.57° phase shift)		10kHz	
Settling Time (2% of final value, 20V, step)		1μsec	
Overload Recovery Time		3μsec	
OUTPUT NOISE (X = Y = 0)			
10kHz to 10MHz		3mV, rms	
10Hz to 10kHz		600μV, rms	
INPUT CHARACTERISTICS			
Input Voltage Range			
Rated Operation		±10V	
Absolute Max		±15V	
Input Impedance, X		10MΩ	
Y		10MΩ	
Z		36kΩ	
OUTPUT CHARACTERISTICS			
Rated Output		±10V at ±5mA	
Output Impedance		1Ω	
POWER SUPPLY REQUIREMENTS			
Rated Voltage		±15VDC	
Operating Range		±12VDC to ±18VDC	
Quiescent Current		±4.5mA	
TEMPERATURE RANGE			
Operating, Rated Performance	0°C to +70°C		-55°C to +125°C
Storage	-65°C to +150°C		

*Total error is a tested maximum at .25°C and represents the maximum allowed value for the sum of the individual errors.

MECHANICAL

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

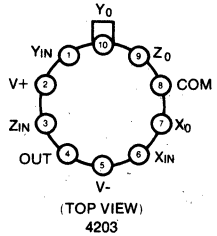
Pin numbers shown for reference only.
Numbers may not be marked on package.



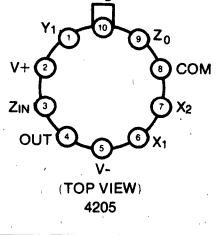
ORDER NUMBER:
4203J, 4205J
4203K, 4205K
4203S, 4205S
WEIGHT:
1 gram

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

CONNECTION DIAGRAM



(TOP VIEW)
4203



(TOP VIEW)
4205

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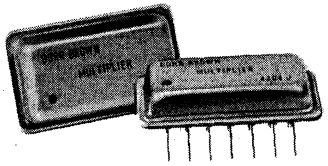
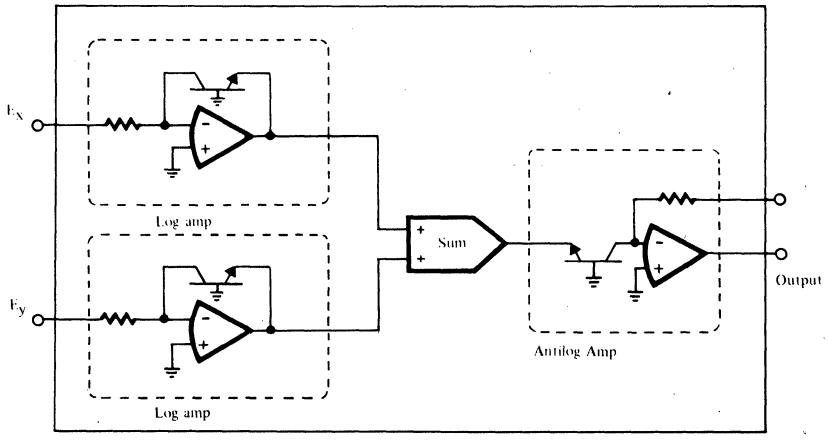


4204

ANALOG MULTIPLER-DIVIDER

FEATURES

- **IMPROVE SYSTEM ACCURACY**
  ±0.25% and ±0.5% units
- **LOW COST**
  0.5% accuracy
- **IMPROVE ACCURACY**
  OVER TEMPERATURE - ±0.02%/°C max
- **SIMPLIFY ASSEMBLY**
  Laser-trimmed at the factory
  No external components required



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DESCRIPTION

The 4204 is an internally trimmed four quadrant analog multiplier/divider using the log/antilog technique. This method yields excellent accuracy, low noise and moderate bandwidth–at low cost. No external components or amplifiers are required with the 4204. Accuracy specifications are guaranteed without external adjustments and are verified at Burr-Brown by an automatic tester which scans the X-Y plane. Maximum error at any point in the plane is required to be less than the specified values.

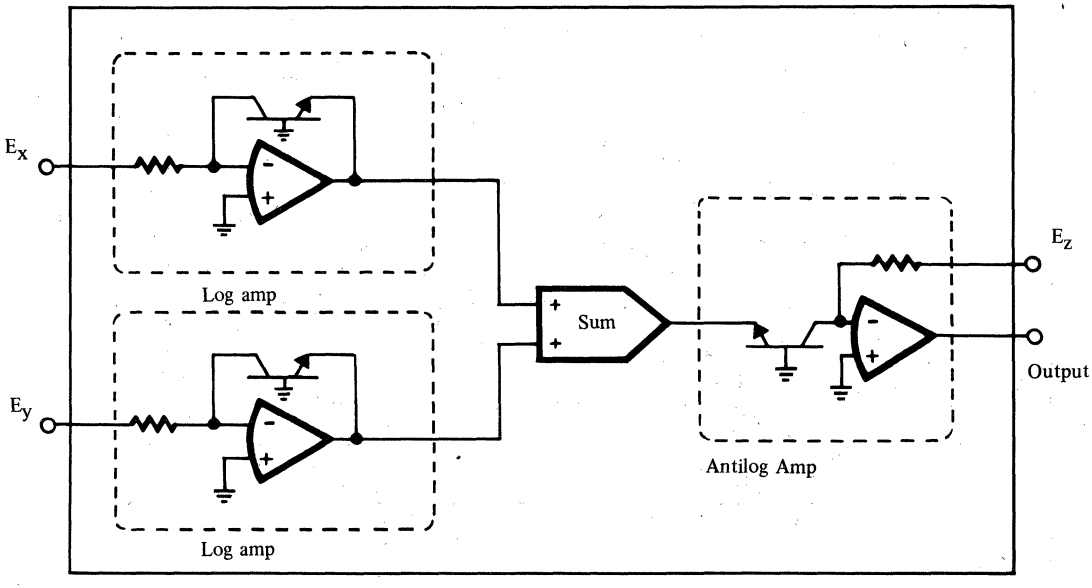
The laser trimmed 4204 is the first high accuracy hybrid IC multiplier/divider ever offered. Just as Burr-Brown was first to offer internally laser trimmed IC multipliers with accuracies of 1% and 2% (Model 4203), we have now extended this money saving technology into the accuracy areas where only higher priced modules were previously available. The excellent tracking characteristics of adjacent monolithic transistors is a key element in maintaining the 4204's high accuracy performance over the temperature range. By variation of external pin connections, the 4204 may be used as a divider or square rooter. No external amplifiers are required for either operation.

THEORY OF OPERATION

The 4204's log-antilog multiplication technique is based upon the logarithmic voltage-current relationship in a semiconductor junction. This action is shown by this simplified equation: $V_{be} = (\frac{KT}{q})(\ln I_c - \ln I_s)$

where V_{be} is the transistor's emitter base voltage, I_c is the transistor collector current, I_s is the collector saturation current, K is Boltzmann's constant, q is the charge of one electron and T is the absolute temperature in degrees Kelvin. As can be seen from the equation, the logarithmic function is extremely temperature sensitive. The 4204, however, has excellent temperature characteristics because the log and antilog circuitry have equal and opposite temperature drifts which cancel to a first order approximation. The log and antilog circuits will compensate each other to the extent that the various logging transistors are matched to each other. In the 4204 these transistors are placed adjacently on a monolithic chip to obtain the best possible matching and so the best possible performance.

BLOCK DIAGRAM



Functional Diagram of Model 4204.

SPECIFICATIONS

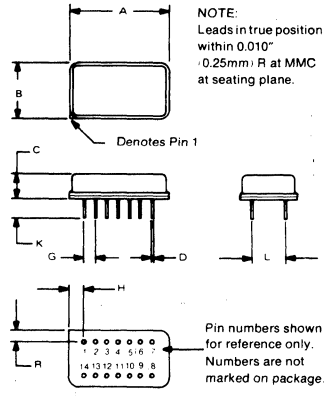
Typical performance at +25°C with rated power supplies unless otherwise noted.
Per cent specifications refer to % of full scale (10V).

ELECTRICAL

MODEL	4204J	4204K	4204S
OUTPUT FUNCTION	$\frac{E_x E_y}{10}$	*	*
TOTAL ERROR**			
Internal trim †	0.5% max	0.25% max	0.25%,max
External trim, typ	0.2%	0.1%	0.1%
vs. Temperature	0.01%/°C	*	0.02%/°C,max
vs. Supply	0.02%/%	*	*
INDIVIDUAL ERRORS			
Output Offset X=Y=0	15 mV	5 mV	5 mV
Scale Factor Error	0.2%	0.1%	0.1%
Non-Linearity			
X = 20 V, p-p Y = −10 VDC Y = 20 V, p-p X = −10 VDC	0.005%	*	*
X = 20 V, p-p Y = +10 VDC Y = 20 V, p-p X = +10 VDC	0.05%	*	*
Feedthrough @ 50 Hz			
X = 20 V, p-p Y = 0	10 mV p-p	5 mV p-p	5 mV p-p
Y = 20 V, p-p X = 0	10 mV p-p	5 mV p-p	5 mV p-p
AC PERFORMANCE		*	*
Slew Rate	1 V/μsec		
−3 dB Small Signal Bandwidth	250 kHz		
1% Amplitude Error	33 kHz		
1% Vector Error (0.57° phase shift)	2.5 kHz		
Full Power Response	20 kHz		
OUTPUT NOISE X = Y = 0.0V		*	*
DC to 10 kHz	300 μV rms		
INPUT CHARACTERISTICS		*	*
Input Voltage			
Maximum for Rated Specifications X,Y,Z	±10 V		
Maximum Safe Level X,Y,Z	±Supply		
Input Impedance X/Y/Z	25kΩ/25kΩ/100kΩ		
OUTPUT CHARACTERISTICS		*	*
Rated Output			
Voltage, min	±10 V		
Current, min	±5 mA		
Output Impedance	1 Ω		
POWER SUPPLY REQUIREMENTS		*	*
Rated Supply	±15 VDC		
Operating Range	±14 to ±16 V		
Quiescent Current	+15 mA, −8.5 mA		
TEMPERATURE RANGE		*	
Specification	-25°C to +85°C		-55°C to +125°C
Operating	-55°C to +125°C		*
Storage	-65°C to +125°C		*

*Same as for 4204J.
** Total error is a tested maximum and does not represent a sum of the maximum individual errors as the maximum individual errors do not occur at the same X, Y operating point.
† With output loading of 10 kΩ or less.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

PIN CONNECTIONS

1 E_z
2 Output
3 $-V_s$
4 Feedthrough Adj.
5 Make No Connection
6 Make No Connection
7 E_x
8 Internal Reference
9 Make No Connection
10 Ground
11 Feedthrough Adj.
12 Offset Adj.
13 E_y
14 $+V_s$

TYPICAL PERFORMANCE CURVES

Typical Performance @25°C and ±15 VDC

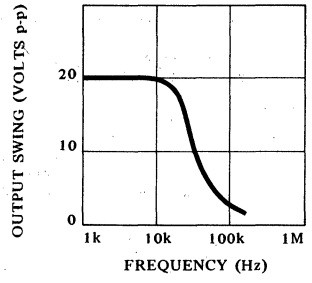


FIGURE 1. Large Signal Frequency Response

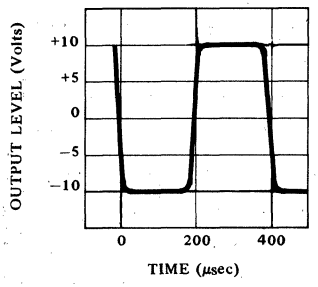


FIGURE 2. Step Response

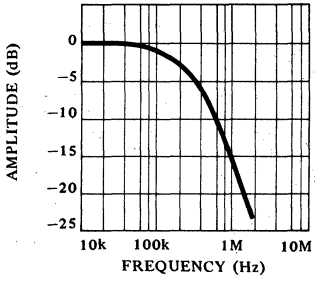


FIGURE 3. Small Signal Frequency Response

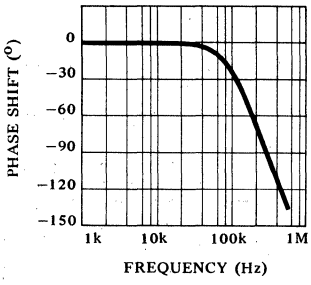


FIGURE 4. Small Signal Frequency Response

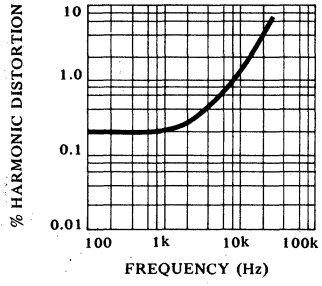


FIGURE 5. Output Distortion vs. Frequency

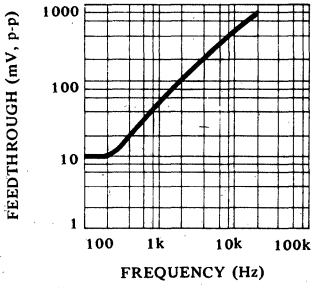


FIGURE 6. AC Feedthrough vs. Frequency

DISCUSSION OF PERFORMANCE CURVES

LARGE SIGNAL FREQUENCY RESPONSE

This response curve describes the output voltage capability of the 4204 as a function of frequency. The measurement is made with one input at +10 or −10 VDC, and with a sine wave applied at the other input. An output distortion of 0.5% is allowed.

STEP RESPONSE

Step response is measured with one input at +10 or −10VDC and with a 20 volt p-p square wave applied at the other input.

SMALL SIGNAL FREQUENCY RESPONSE

These curves are the amplitude and phase response of the 4204's transfer function, when one input is held at +10 or −10 VDC. A sine wave signal is applied to the other input. Small signal response requires that the amplitude of the input sine wave be adjusted so that the output signal does not reach the slew rate limitation.

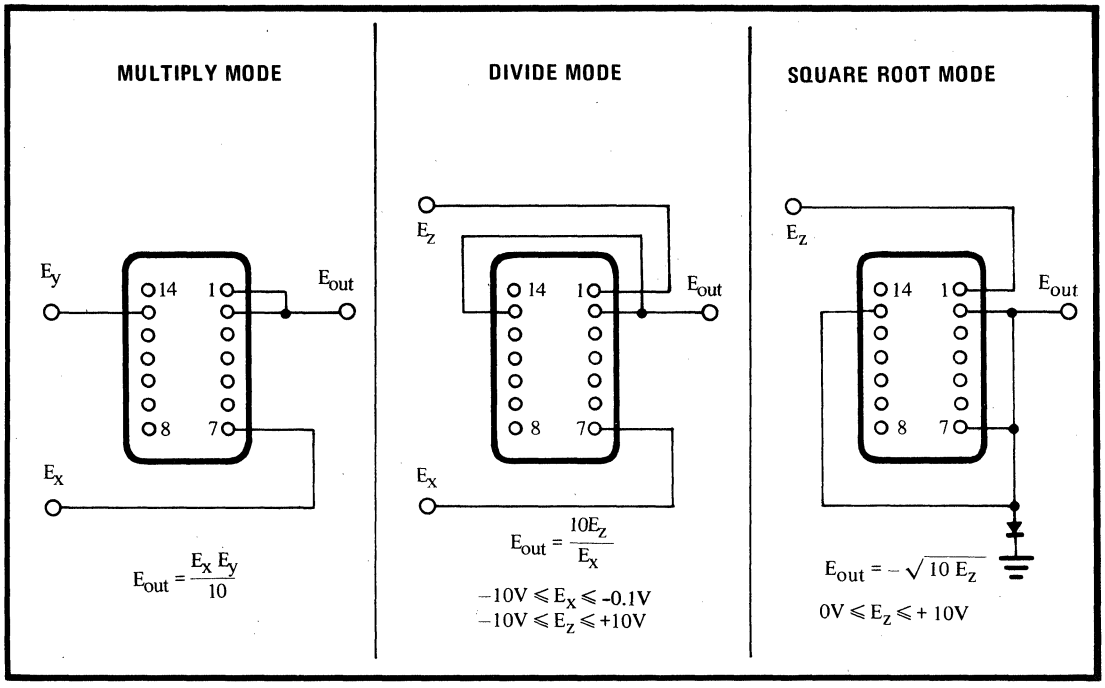
OUTPUT DISTORTION

The output distortion of the 4204 is of most interest in modulator applications. The curve of Figure 5 characterizes this distortion with one input of the 4204 held at +10 or −10 VDC. A sine wave is applied to the other input. The sine wave amplitude is held constant at 20 volts p-p while frequency is varied.

AC FEEDTHROUGH

The variation of feedthrough as a function of frequency is illustrated by Figure 6. One of the inputs is a zero while a 20 volt p-p sine wave is applied at the other input. The output feedthrough generally has substantial harmonic content and is measured in millivolts, peak-to-peak.

OPERATING MODES



ADJUSTMENTS

Although the 4204 will achieve specified performance in the multiply mode with no external trimming, optimized performance can be achieved with external adjustments. The proper connections and the trim procedures are explained below.

The 4204 will operate within specification with any combination of input signals. The best performance, however, will be obtained in the 2nd, 3rd and 4th quadrants. That is if four quadrant operations are not needed, the performance of the 4204 can be optimized by constraining operation to quadrants 2, 3 and 4 rather than 1.

MULTIPLICATION

MULTIPLICATION TRIM PROCEDURE (FIG. 7)

1) Set E_x = 0 and apply a 10 volt peak-peak sine wave (50 Hz) to E_y: Adjust R_1 for minimum output.
2) Set E_y = 0 and apply a 10 volt peak-to-peak sine wave (50 Hz) to E_x: Adjust $R_2$for minimum output.
3) Set $E_x = E_y$ = 0: Adjust R_3 for E_{out} = 0.000 V.
4) Set $E_x = E_y$ = +10.000 V ±1 mV: Adjust R_4 for E_{out} = +10.000 V ±2 mV.

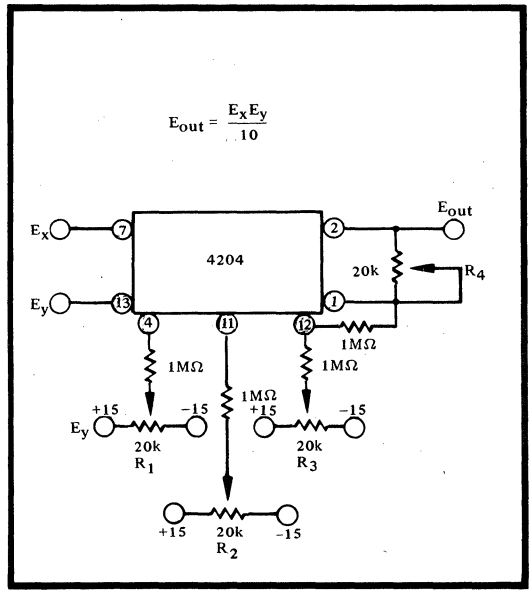


FIGURE 7. Multiplication Trim Procedure.

DIVISION

The 4204 may be used as a two-quadrant divider without the need for an external operational amplifier. It should, however, be noted that the maximum output error is approximately given by:

$$\text{divider error} \approx \frac{10\epsilon_m}{E_X}$$

where ϵ_m is the total error specification for the multiply mode. Obviously, divider error becomes excessively large for small values of E_X. A 10:1 denominator range is usually the practical limit. IF accurate division is required over a wide dynamic range of denominator voltage, the Burr-Brown DIV100 is recommended (0.25%, max over a 40:1 range).

DIVISION TRIM PROCEDURE (FIG. 8)

1) Set all potentiometers at about mid-scale.
2) Set E_Z = 0 volt, $E_X \approx$ -10V, adjust R_2 such that E_O = 0.000V ±2mV.
3) Set $E_X = E_Z \mp$ -10.000VDC ±2mV, adjust R_3 such that E_O = +10.000VDC ±2mV.
4) Set $E_X = E_Z \approx$ minimum value required by application, adjust R_1 such that E_O = +10.000VDC ±5mV.
5) Repeat steps (2) through (4) if necessary.

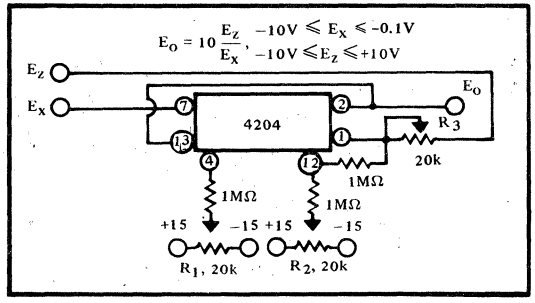


FIGURE 8. Division Trim Procedure.

SQUARE ROOT

The pin connections for the Square Root mode of operation are similar to those for division, except that the denominator input is connected to the output node. Errors in the Square Root mode of operation become troublesome for small values of E_Z. However, the output error does not increase so rapidly as in the divide mode. The actual output for small values of E_Z is given approximately by:

$$E_{OUT} \approx \sqrt{10E_Z + 10\epsilon_m}$$

where ϵ^m is the total error specified for Multiply mode. This equation can be used to determine the feasibility of using the 4204 as a square rooter for a given application. For operation over a much wider dynamic range, with improved accuracy, the Model 4302 multifunction converter is recommended.

SQUARE ROOT TRIM PROCEDURE (FIG. 9)

1) Set E_Z = +10.000VDC ±2mV, adjust R_2 such that E_O = -10.000VDC ±2mV.
2) Set $E_Z \approx$ minimum value required by application (E_{ZM}) adjust R_1 such $E_O \mp -\sqrt{10E_{ZM}}$ ±2mV.
3) Repeat steps (1) and (2) if necessary.

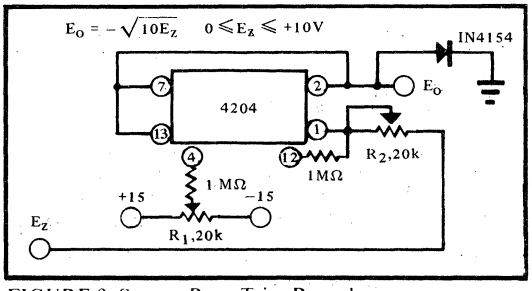
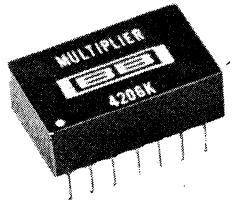


FIGURE 9. Square Root Trim Procedure.

BURR-BROWN®

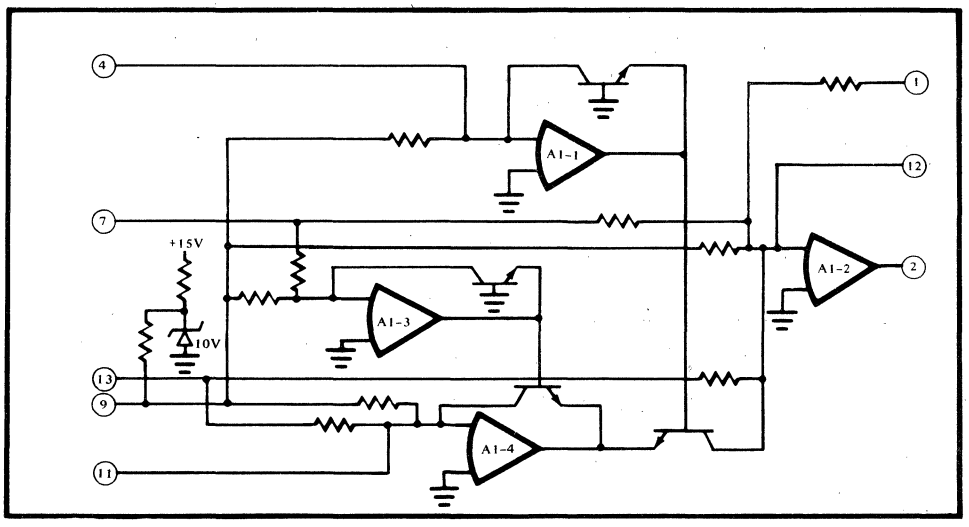
4206



ANALOG MULTIPLIER-DIVIDER

FEATURES

- HIGH TOTAL ACCURACY
  0.25% and 0.5% max, no external trims
  0.1% and 0.2% typ. with external trims
- LOW TEMPERATURE DRIFT
  100ppm/°C from 0°C to +70°C
- SMALL PACKAGE
  Dual-in-line saves board space
- LOW COST



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

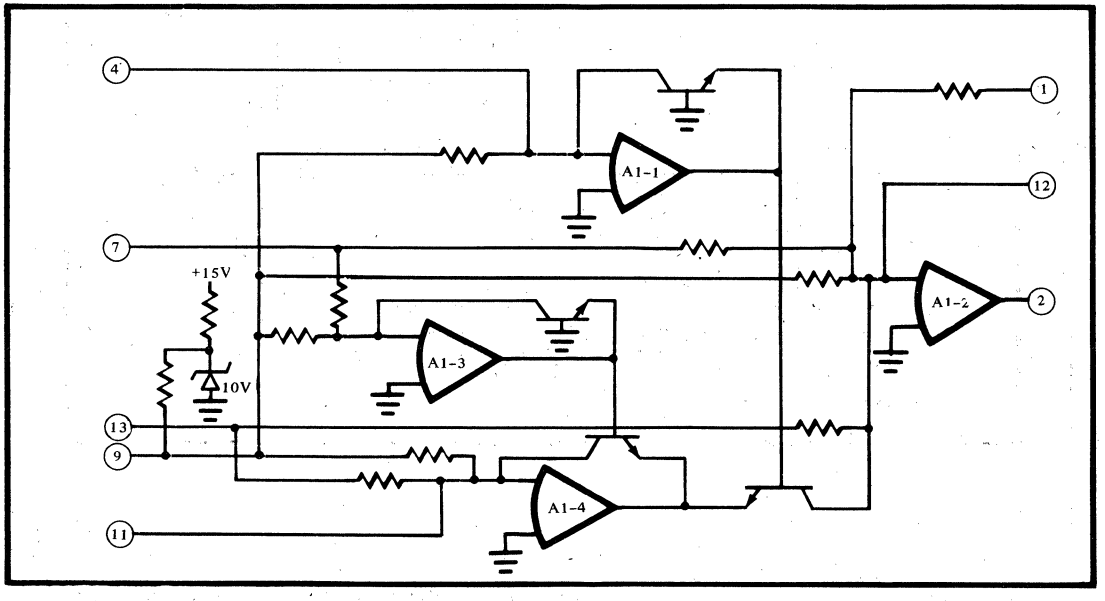
The 4206 is a four-quadrant analog multiplier offering high accuracy, low noise, and moderate bandwidth at low cost. It uses the log/antilog technique and is internally laser-trimmed and multiply mode accuracies of 0.25% and 0.5% max, are guaranteed with no external components. By following the external trim procedure described in Multiplication section, accuracies can be improved to 0.1% and 0.2% typ. Accuracy specifications are verified at Burr-Brown by an automatic tester which scans the X-Y plane. Maximum error at any points in the plane is required to be less than the specified values.

The 4206 also performs the divide function in two quadrants and the square root function in one quadrant with no external components required. Detailed instructions for these operations are given on the last page.

THEORY OF OPERATION

The 4206's log-antilog multiplication technique is based upon the logarithmic voltage-current relationship in a semiconductor junction. This action is shown by the simplified equation: $V_{be} = (\frac{KT}{q})(\ln I_c - \ln I_s)$

where V_{be} is the transistor's emitter-base voltage, I_c is the transistor collector current, I_s is the collector saturation current, K is Bolzmann's constant, q is the charge of one electron and T is the absolute temperature in degrees Kelvin. As can be seen from the equation, the logarithmic function is extremely temperature sensitive. The 4206, however, has excellent temperature characteristics because the log and antilog circuitry have equal and opposite temperature drifts which cancel to a first order approximation. The log and antilog circuits will compensate each other to the extent that the various logging transistors are matched to each other. In the 4206 these transistors are placed adjacently on a monolithic chip to obtain the best possible matching and so the best possible performance.



SPECIFICATIONS

Typical performance at +25°C with rated power supplies unless otherwise noted.
Per cent specifications refer to % of full scale (10V).

ELECTRICAL

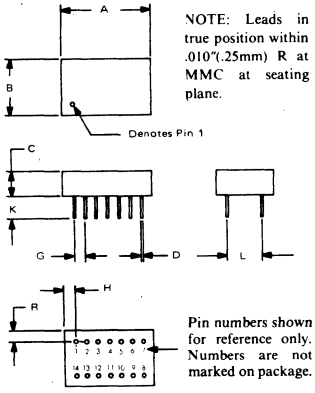
MODEL	4206J	4206K
OUTPUT FUNCTION	$\frac{E_X E_Y}{10}$	*
TOTAL ERROR (Multiply Mode)**		
Internal trim, max †	0.5% max	0.25% max
External trim, typ	0.2%	0.1%
vs. Temperature	0.01%/°C	*
vs. Supply	0.02%/%	*
INDIVIDUAL ERRORS (Multiply Mode)		
Output Offset X=Y=0	15 mV	5 mV
Scale Factor Error	0.2%	0.1%
Non-Linearity		
X = 20 V, p-p Y = −10 VDC Y = 20 V, p-p X = −10 VDC	0.005%	*
X = 20 V, p-p Y = +10 VDC Y = 20 V, p-p X = +10 VDC	0.05%	*
Feedthrough @ 50 Hz		
X = 20 V, p-p Y = 0	10 mV p-p	5 mV p-p
Y = 20 V, p-p X = 0	10 mV p-p	5 mV p-p
AC PERFORMANCE		*
Slew Rate	1 V/μsec	
−3 dB Small Signal Bandwidth	250 kHz	
1% Amplitude Error	33 kHz	
1% Vector Error (0.57° phase shift)	2.5 kHz	
Full Power Response	20 kHz	
OUTPUT NOISE X = Y = 0.0V		*
DC to 10 kHz	300 μV rms	
INPUT CHARACTERISTICS		*
Input Voltage		
Maximum for Rated Specifications X,Y,Z	±10 V	
Maximum Safe Level X,Y,Z	±Supply	
Input Impedance X/Y/Z	25kΩ/25kΩ/100kΩ	
OUTPUT CHARACTERISTICS		*
Rated Output		
Voltage, min	±10 V	
Current, min	±5 mA	
Output Impedance	1 Ω	
POWER SUPPLY REQUIREMENTS		*
Rated Supply	±15 VDC	
Operating Range	±14 to ±16 V	
Quiescent Current	+15 mA, −8.5 mA	
TEMPERATURE RANGE		*
Specification	0°C to +70°C	
Operating	−25°C to +85°C	
Storage	−40°C to +85°C	

* Same as for 4206J

** Total error is a tested maximum and does not represent a sum of the maximum individual errors as the maximum individual errors do not occur at the same X, Y operating point.

† With output loading of 10kΩ or less.

MECHANICAL



NOTE: Leads in true position within .010"(.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

PIN SPACING: 2.5mm (0.1") ROW SPACING: 7.6mm (0.300") WEIGHT: 3.4 grams (0.12 oz.) CONNECTOR: 14-pin DIP 0145MC Price: $3.75 ea.

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

PIN CONNECTIONS

1 E_Z
2 Output
3 $-V_S$
4 Feedthrough Adj.
5 Make No Connection
6 Make No Connection
7 E_X
8 Internal Reference
9 Make No Connection
10 Ground
11 Feedthrough Adj.
12 Offset Adj.
13 E_Y
14 $+V_S$

TYPICAL PERFORMANCE CURVES

Typical Performance @25°C and ±15 VDC

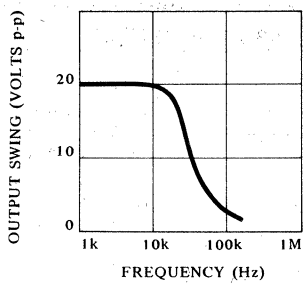


FIGURE 1. Large Signal Frequency Response

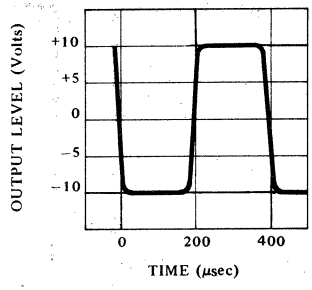


FIGURE 2. Step Response

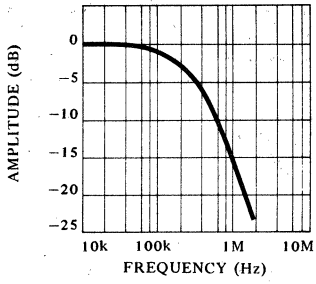


FIGURE 3. Small Signal Frequency Response

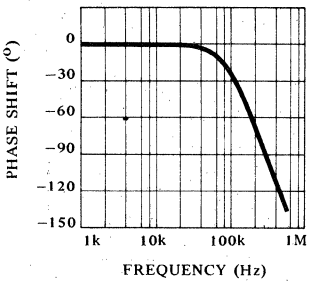


FIGURE 4. Small Signal Frequency Response

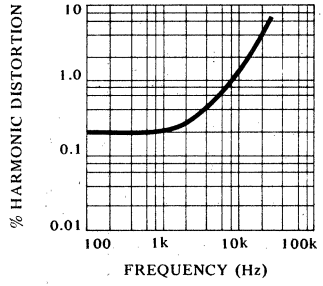


FIGURE 5. Output Distortion vs. Frequency

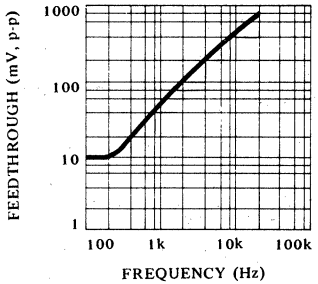


FIGURE 6. AC Feedthrough vs. Frequency

DISCUSSION OF PERFORMANCE CURVES

LARGE SIGNAL FREQUENCY RESPONSE

This response curve describes the output voltage capability of the 4206 as a function of frequency. The measurement is made with one input at +10 or −10 VDC, and with a sine wave applied at the other input. An output distortion of 0.5% is allowed.

STEP RESPONSE

Step response is measured with one input at +10 or −10VDC and with a 20 volt p-p square wave applied at the other input.

SMALL SIGNAL FREQUENCY RESPONSE

These curves are the amplitude and phase response of the 4206's transfer function, when one input is held at +10 or −10 VDC. A sine wave signal is applied to the other input. Small signal response requires that the amplitude of the input sine wave be adjusted so that the output signal does not reach the slew rate limitation.

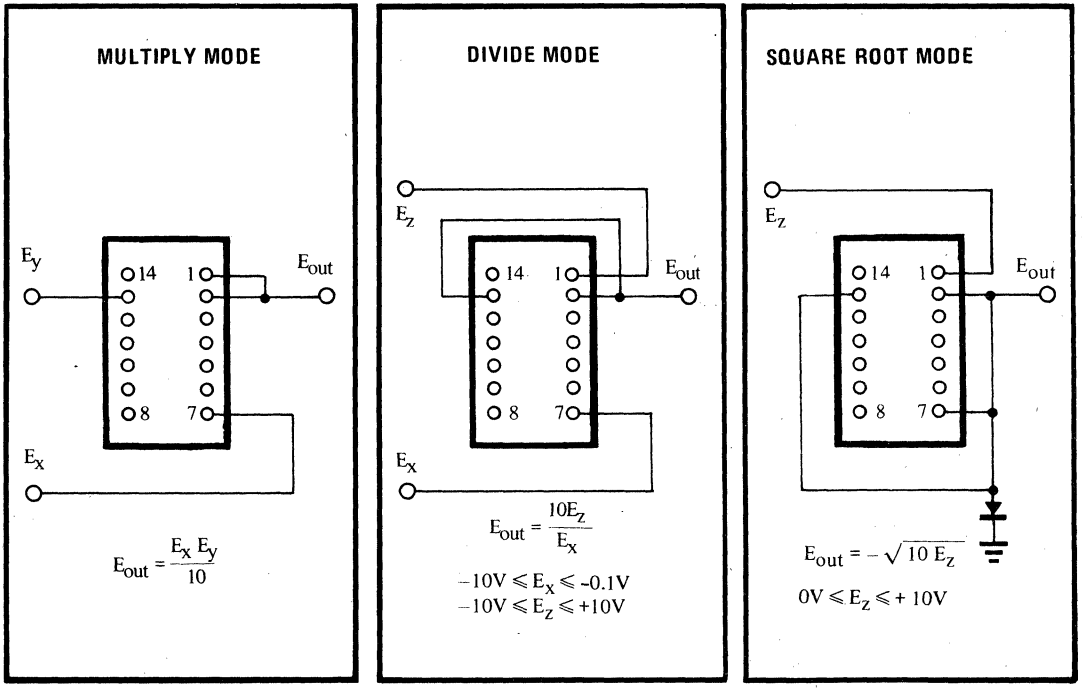
OUTPUT DISTORTION

The output distortion of the 4206 is of most interest in modulator applications. The curve of Figure 5 characterizes this distortion with one input of the 4206 held at +10 or −10 VDC. A sine wave is applied to the other input. The sine wave amplitude is held constant at 20 volts p-p while frequency is varied.

AC FEEDTHROUGH

The variation of feedthrough as a function of frequency is illustrated by Figure 6. One of the inputs is a zero while a 20 volt p-p sine wave is applied at the other input. The output feedthrough generally has substantial harmonic content and is measured in millivolts, peak-to-peak.

OPERATING MODES



4206

ADJUSTMENTS

Although the 4206 will achieve specified performance in the multiply mode with no external trimming, optimized performance can be achieved with external adjustments. The proper connections and the trim procedures are explained below.

The 4206 will operate within specification with any combination of input signals. The best performance, however, will be obtained in the 2nd, 3rd and 4th quadrants. That is if four quadrant operations are not needed, the performance of the 4206 can be optimized by constraining operation to quadrants 2, 3 and 4 rather than 1.

MULTIPLICATION

MULTIPLICATION TRIM PROCEDURE (FIG. 7)

1) Set E_x = 0 and apply a 10 volt peak-peak sine wave (50 Hz) to E_y: Adjust R_1 for minimum output.
2) Set E_y = 0 and apply a 10 volt peak-to-peak sine wave (50 Hz) to E_x: Adjust R_2 for minimum output.
3) Set $E_x = E_y$ = 0: Adjust R_3 for E_{out} = 0.000 V.
4) Set $E_x = E_y$ = +10.000 V ±1 mV: Adjust R_4 for E_{out} = +10.000 V ±2 mV.

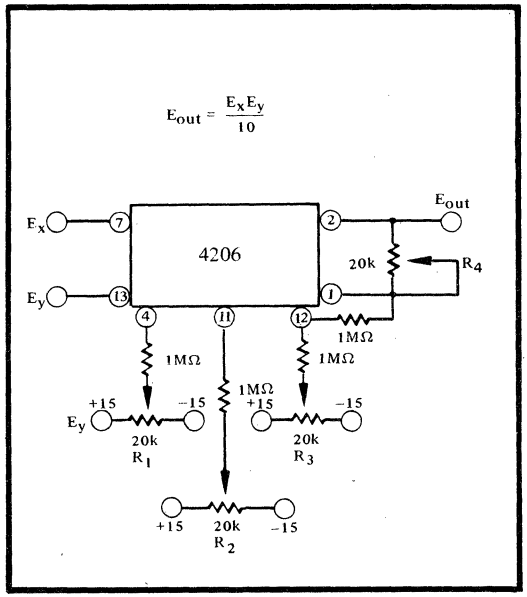


FIGURE 7 Multiplication Trim Procedure

DIVISION

The 4206 may be used as a two-quadrant divider without the need for an external operational amplifier. It should, however, be noted that the maximum output error is approximately given by

$$\text{divider error} \approx \frac{10\epsilon_m}{Ex}$$

where ϵ_m is the total error specification for the multiply mode. Obviously, divider error becomes excessively large for small values of E_X. A 10:1 denominator range is usually the practical limit. If accurate division is required over a wide dynamic range of denominator voltage, the Burr-Brown Model 4291 is recommended (0.5%, max., over a 100:1 range).

DIVISION TRIM PROCEDURE (FIG. 8)

1) Set all potentiometers near mid-scale.
2) Set E_Z = 0 volt, $E_X \approx -10$ V, adjust R_2 such that E_O = 0.000 V ±2 mV.
3) Set $E_X = E_Z$ = -10.000VDC ±2 mV, adjust R_3 such that E_O = +10.000VDC ±2 mV.
4) Set $E_X = E_Z \approx$ minimum value required by application, adjust R_1 such that E_O = +10.000 VDC ±5 mV.
5) Repeat steps (2) through (4) if necessary.

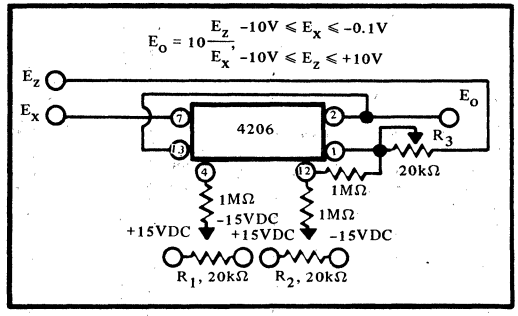


FIGURE 8 Division Trim Procedure

SQUARE ROOT TRIM PROCEDURE (FIG. 9)

1) Set E_Z = +10.000VDC ±2 mV, adjust R_2 such that E_O = +10.000VDC ±2 mV.
2) Set $E_Z \approx$ minimum value required by application (E_{Zm}) adjust R_1 such that $E_O = -\sqrt{10\,E_{Zm}}$ ±2 mV.
3) Repeat steps (1) and (2) if necessary.

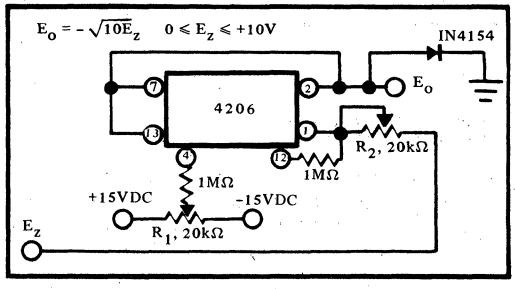


FIGURE 9 Square Root Trim Procedure

SQUARE ROOT

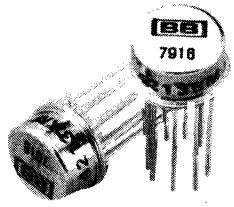
The pin connections for the Square Root mode of operation are similar to those for division, except that the denominator input is connected to the output node. Errors in the Square Root mode of operation become troublesome for small values of E_Z. However, the output error does not increase so rapidly as in the divide mode. The actual output for small values of E_Z is given approximately by

$$E_{out} \approx -\sqrt{10E_Z + 10\epsilon_m}$$

where ϵ_m is the total error specified for Multiply mode. This equation can be used to determine the feasibility of using the 4206 as a square rooter for a given application. For operation over a much wider dynamic range, with improved accuracy, the Model 4302 multifunction converter is recommended.

BURR-BROWN®

4213



MULTIPLIER-DIVIDER

FEATURES

- LOW COST
- DIFFERENTIAL INPUT
- ACCURACY 100% TESTED AND GUARANTEED
- LOW NOISE
  120μV, rms, 10Hz to 10kHz
- SELF-CONTAINED
  No additional amplifiers
- SMALL SIZE
  Hermetic TO-100 package
- WIDE TEMPERATURE OPERATION

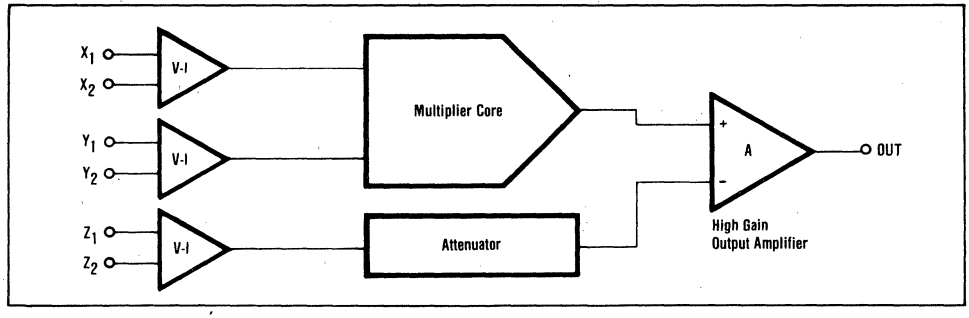
APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOT
- LINEARIZATION
- POWER COMPUTATION
- ANALOG SIGNAL PROCESSING
- ALGEBRAIC COMPUTATION
- TRUE RMS-TO-DC CONVERSION

DESCRIPTION

The 4213 multiplier-divider is a low cost precision device designed for general purpose application. In addition to four-quadrant multiplication, it also performs analog square root and division without the bother of external amplifiers. The 4213 is laser-trimmed to guarantee its rated accuracy with no external components. The internal zener regulated references make the 4213 much less sensitive to supply variation than earlier IC multipliers. Hermetic TO-100 package, wide operating temperature range, low output noise, and low cost are some of the desirable features of this versatile device.

4213 FUNCTIONAL DIAGRAM



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL		4213AM			4213BM			4213SM			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
MULTIPLIER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$			•			•		
Total Error	-10V ≤ X, Y ≤ 10V										
Initial	T_A = +25°C			±1.0			±0.5			±0.5	% FSR
vs Temperature	-25°C ≤ T_A ≤ +85°C		±0.008	±0.02		•	•		--	--	% FSR/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--	--		--	--		±0.025	±0.05	% FSR/°C
vs Supply			±0.05			•			•		% FSR/%
Individual Errors											
Output Offset											
Initial	T_A = +25°C		±10	±50		±7	±25		±7	±25	mV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±0.7	±2.0		±0.3	±0.7		--	--	mV/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--	--		--	--		±0.3	±0.7	mV/°C
vs Supply			±0.25			•			•		mV/%
Scale Factor Error											
Initial	T_A = +25°C		±0.12			•			•		% FSR
vs Temperature	-25°C ≤ T_A ≤ +85°C		±0.008			•			--		% FSR/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--			--			±0.008		% FSR/°C
vs Supply			±0.05			•			•		% FSR/%
Nonlinearity											
X Input	X = 20V, p-p; Y = ±10VDC		±0.08			•			•		% FSR
Y Input	Y = 20V, p-p; X = ±10VDC		±0.01			•			•		% FSR
Feedthrough	f = 50Hz										
X Input	X = 20V, p-p; Y = 0		30			•			•		mV, p-p
Y Input	Y = 20V, p-p; X = 0		6			•			•		mV, p-p
vs Temperature	-25°C ≤ T_A ≤ +85°C		0.1			•			--		mV, p-p/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--			--			0.1		mV, p-p/°C
vs Supply			0.15			•			•		mV, p-p/%
DIVIDER PERFORMANCE											
Transfer Function	$X_1 > X_2$		$\frac{10(Z_1 - Z_2)}{X_1 - X_2} + Y_2$			•			•		
Total Error with	X = -10V										
external adjustments	-10V ≤ Z ≤+10V		±0.75			±0.35			±0.35		% FSR
	X = -1V										
	-1V ≤ Z ≤ +1V		±2.0			±1.0			±1.0		% FSR
	-10V ≤ X ≤ -0.2V										
	-10V ≤ Z ≤ +10V		±5.0			±1.0			±1.0		% FSR
SQUARER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)^2}{10} + Z_2$			•			•		
Total Error	-10V ≤ X ≤ +10V		±0.6			±0.3			±0.3		% FSR
SQUARE-ROOTER PERFORMANCE											
Transfer Function	$Z_1 < Z_2$		$+\sqrt{10(Z_2 - Z_1)}$			•			•		
Total Error	1V ≤ Z ≤ 10V		±1			±0.5			±0.5		% FSR
AC PERFORMANCE											
Small-Signal Bandwidth	±3dB		550			•			•		kHz
1% Amplitude Error	Small Signal		70			•			•		kHz
1% 0.57° Vector Error	Small Signal		5			•			•		kHz
Full Power Bandwidth	$\|V_o\|$ = 10V, R_L = 2kΩ		320			•			•		kHz
Slew Rate	$\|V_o\|$ = 10V, R_L = 2kΩ		20			•			•		V/μsec
Settling Time	ε = ±1%, ΔV_o = 20V		2			•			•		μsec
Overload Recovery	50% Output Overload		0.2			•			•		μsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Rated Operation		±10			•			•			V
Absolute Maximum				±V_{CC}			•			•	V
Input Resistance	X, Y, Z[1]		10			•			•		MΩ
Input Bias Current	X, Y, Z		1.4			•			•		μA
OUTPUT CHARACTERISTICS											
Rated Output											
Voltage	I_o = ±5mA	±10			•			•			V
Current	V_o = ±10V	±5			•			•			mA
Output Resistance	f = DC		1.5			•			•		Ω
OUTPUT NOISE VOLTAGE	X = Y = 0										
f_o = 1Hz			40			•			•		μV/√Hz
f_o = 10kHz			1.0			•			•		μV/√Hz
1/f Corner Frequency			1060			•			•		Hz
f_B = 10Hz to 10kHz			125			•			•		μV, rms
f_B = 10Hz to 10MHz			3			•			•		mV, rms
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			•			•		VDC
Operating Range	Derated Performance	±8.5		±20	•		•	•		•	VDC
Quiescent Current			±5.5			•			•		mA

ELECTRICAL (CONT)

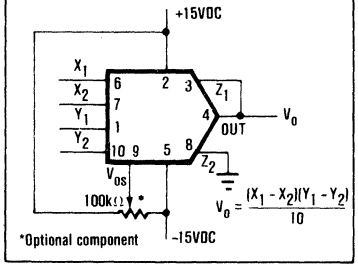
MODEL		4213AM			4213BM			4213SM			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE (Ambient)											
Specification	Derated Performance	-25		+85	·		·	-55		+125	°C
Operating Range		-55		+125	·		·	·		·	°C
Storage		-65		+150	·		·	·		·	°C

NOTES:
1. Z_2 input resistance is 10MΩ, typical, with Pin 9 open. If Pin 9 is grounded or used for optional offset adjustment, the Z_2 input resistance may be as low as 25kΩ.

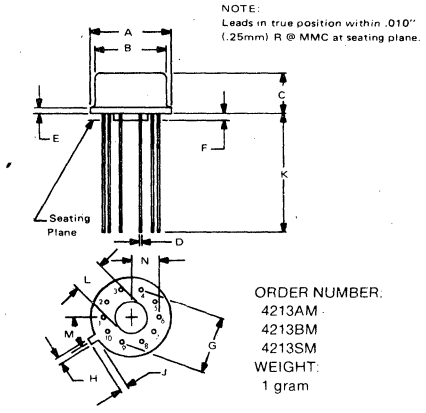
*Same as 4213AM specification.

4213

CONNECTION DIAGRAM



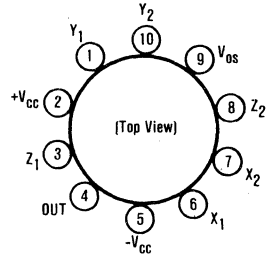
MECHANICAL



ORDER NUMBER:
4213AM
4213BM
4213SM
WEIGHT:
1 gram

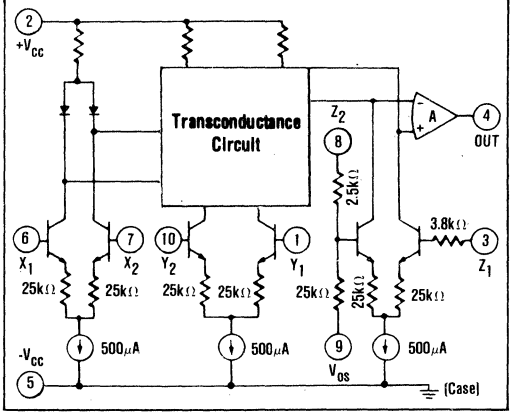
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	---	12.70	---
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

PIN CONFIGURATION



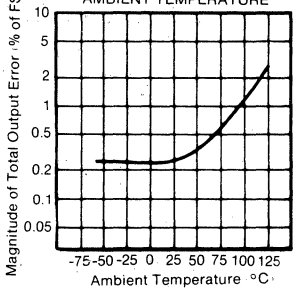
NOTES:
1. V_{OS} adjustment optional not normally recommended. V_{OS} pin may be left open or grounded.
2. All unused input pins should be grounded.
3. Pin 5 is connected to the case.

SIMPLIFIED SCHEMATIC

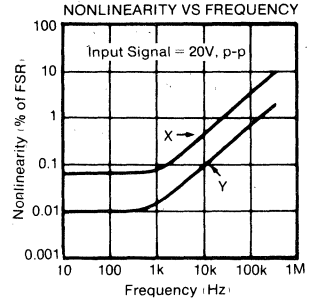


TYPICAL PERFORMANCE CURVES

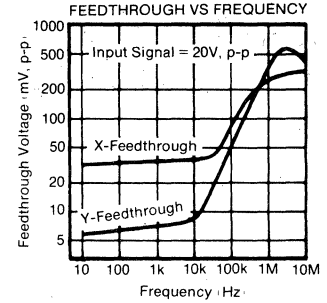
TOTAL ERROR VS AMBIENT TEMPERATURE



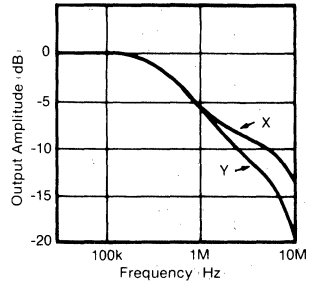
NONLINEARITY VS FREQUENCY



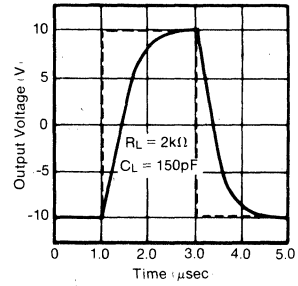
FEEDTHROUGH VS FREQUENCY



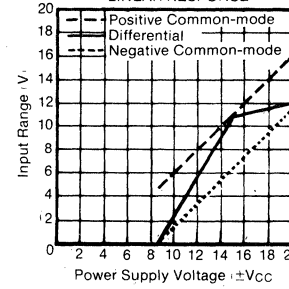
OUTPUT AMPLITUDE VS FREQUENCY



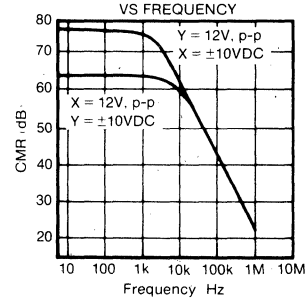
LARGE SIGNAL RESPONSE



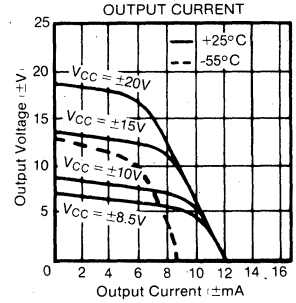
INPUT VOLTAGE FOR LINEAR RESPONSE



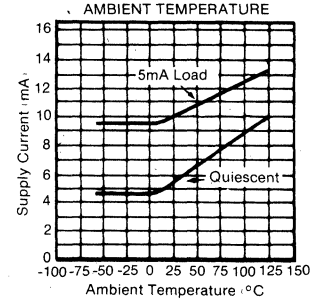
COMMON-MODE REJECTION VS FREQUENCY



OUTPUT VOLTAGE VS OUTPUT CURRENT



SUPPLY CURRENT VS AMBIENT TEMPERATURE



ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-circuit Duration(3)	Continuous
Junction Temperature	+150°C

NOTES:
1. Package must be derated based on: θ_{JC} = 55°C/W and θ_{JA} = 165°C/W.
2. For supply voltages less than ±20VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground only. Rating applies to +85°C ambient.

DEFINITIONS

TOTAL ERROR (Accuracy)

Total error is the actual departure of the multiplier output voltage from the ideal product of its input voltages. It includes the sum of the effects of input and output DC offsets, gain error and nonlinearity.

OUTPUT OFFSET

Output offset is the output voltage when both inputs V_X and Y_Y are zero volts.

SCALE FACTOR ERROR

Scale factor error is the difference between the actual scale factor and the ideal scale factor.

NONLINEARITY

Nonlinearity is the maximum deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

FEEDTHROUGH

Feedthrough is the signal at the output for any value of V_X or V_Y within the rated range, when the other input is zero.

SMALL SIGNAL BANDWIDTH

Small signal bandwidth is the frequency at which the output is down 3dB from its low frequency value for a nominal output amplitude of 10% of full scale.

1% AMPLITUDE ERROR

The 1% amplitude error is the frequency the output amplitude is in error by 1%, measured with an output amplitude of 10% of full scale.

1% VECTOR ERROR

The 1% vector error is the frequency at which a phase error of 0.01 radians (0.57°) occurs. This is the most sensitive measure of dynamic error of a multiplier.

APPLICATIONS INFORMATION

MULTIPLICATION

Figure 1 shows the basic connection for four-quadrant multiplication.

The 4213 meets all of its specifications without trimming. Accuracy can, however, be improved over a limited range by nulling the output offset voltage using the 100kΩ optional balance potentiometer shown in Figure 1.

AC feedthrough may be reduced to a minimum by applying an external voltage to the X or Y input as shown in Figure 2.

Z_2, the optional summing input, may be used to sum a voltage into the output of the 4213. If not used, this terminal, as well as the X and Y input terminals, should be grounded. All inputs should be referenced to power supply common.

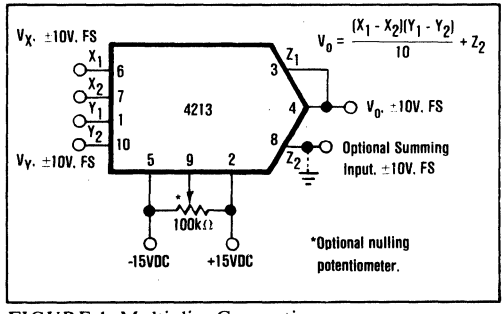


FIGURE 1. Multiplier Connection.

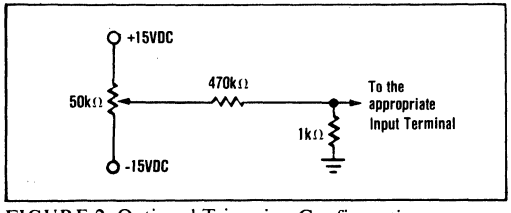


FIGURE 2. Optional Trimming Configuration.

Figure 3 shows how to achieve a scale factor larger than the nominal 0.1. In this case, the scale factor is unity which makes the transfer function

$$V_o = KV_XV_Y = K(X_1 - X_2)(Y_1 - Y_2)$$
$$K = [1 + (R_1/R_2)]\ 10$$
$$0.1 \leq K \leq 1$$

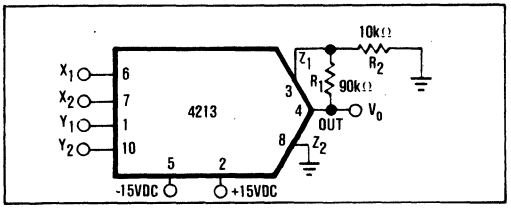


FIGURE 3. Connection For Unity Scale Factor.

This circuit has the disadvantage of increasing the output offset voltage by a factor of 10 which may require the use of the optional balance control for some applications. In addition, this connection reduces the small signal bandwidth to about 50kHz.

DIVISION

Figure 4 shows the basic connection for two-quadrant division. This configuration is a multiplier-inverted analog divider, i.e., a multiplier connected in the feedback loop of an operational amplifier. In the case of the 4213 this operational amplifier is the output amplifier of the multiplier itself.

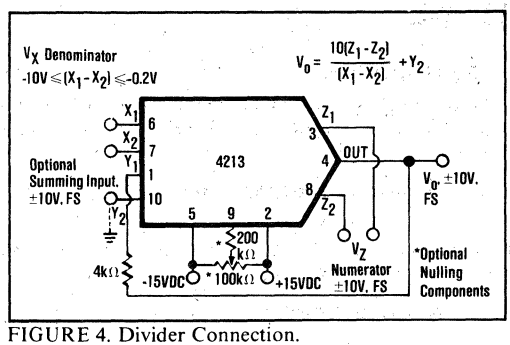


FIGURE 4. Divider Connection.

The divider error with a multiplier-inverted analog divider is approximately

$$\epsilon_{divider} = 10\ \epsilon_{multiplier}\ (X_1 - X_2).$$

It is obvious from this error equation that divider error becomes excessively large for small values of $X_1 - X_2$. A 10-to-1 denominator range is usually the practical limit. If more accurate division is required over a wide range of denominator voltages, an externally generated voltage may be applied to the unused X-input (see Optional Trim Configuration). To trim, apply a ramp of +100mV to +1V at 100Hz to both X_1 and Z_1 if X_2 is used for offset adjustment, otherwise reverse the signal polarity, and adjust the trim voltage to minimize the variation in the output. An alternative to this procedure would be to use the Burr-Brown DIV100, a precision log-antilog divider.

SQUARING

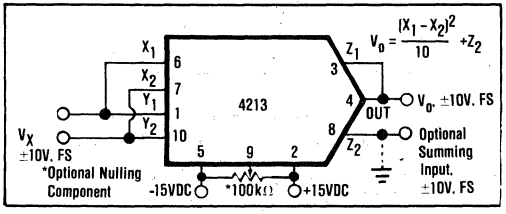


FIGURE 5. Squarer Connection.

SQUARE ROOT

Figure 6 shows the connection for taking the square root of the voltage V_Z. The diode prevents a latching condition which could occur if the input momentarily changed polarity. This latching condition is not a design flaw in the 4213, but occurs when a multiplier is connected in the feedback loop of an operational amplifier to perform square root functions.

The load resistance R_1 must be in the range of $10k\Omega \leq R_1 \leq 1M\Omega$. This resistance must be in the circuit as it provides the current necessary to operate the diode.

The output offset should be nulled for optimum performance by allowing the input to be its smallest expected value and adjusting R_1 for the proper output voltage.

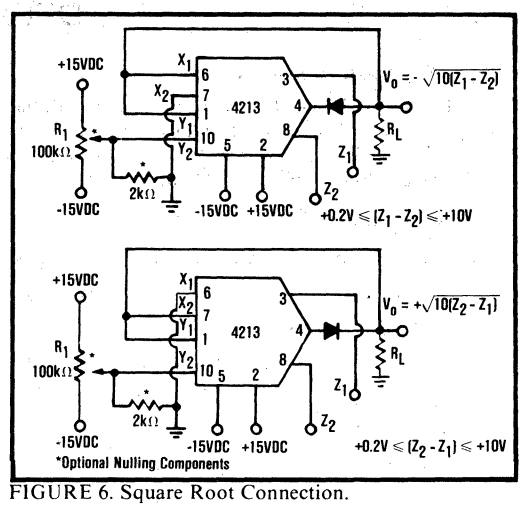


FIGURE 6. Square Root Connection.

This will improve the square root mode accuracy to about that of the multiply mode.

BRIDGE LINEARIZATION

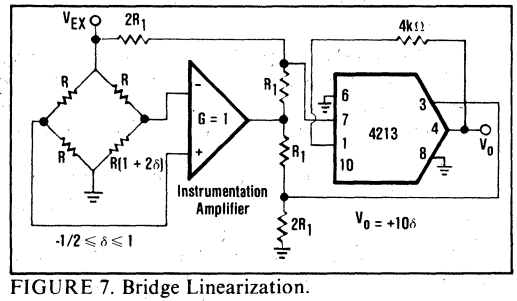


FIGURE 7. Bridge Linearization.

The use of the 4213 and the instrumentation amplifier to linearize the output from a bridge circuit makes the output V_0 independent of the bridge supply voltage.

TRUE RMS-TO-DC CONVERSION

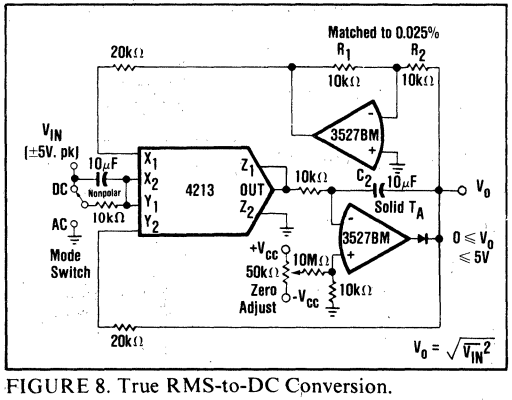


FIGURE 8. True RMS-to-DC Conversion.

The RMS-to-DC conversion circuit of Figure 8 gives greater accuracy and bandwidth but with less dynamic range than most rms-to-DC converters.

PERCENTAGE COMPUTATION

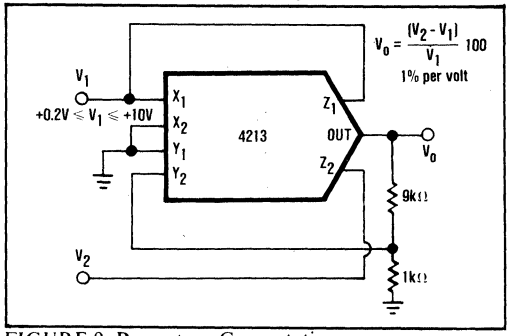


FIGURE 9. Percentage Computation.

The circuit of Figure 9 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2: R_1.

SINE FUNCTION GENERATOR

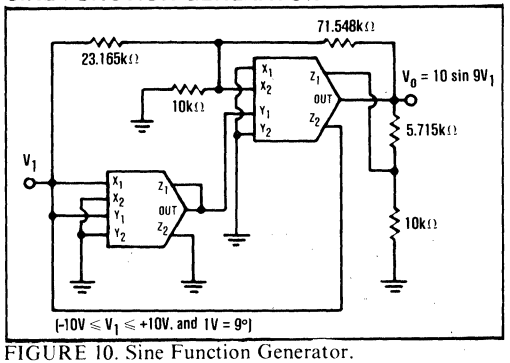


FIGURE 10. Sine Function Generator.

The circuit in Figure 10 uses implicit feedback to implement the following sine function approximation:

$$V_o = (1.5715V_1 - 0.004317V_1^3)(1 + 0.001398V_1^2)$$
$$= 10 \sin(9V_1).$$

SINGLE-PHASE POWER MEASUREMENT

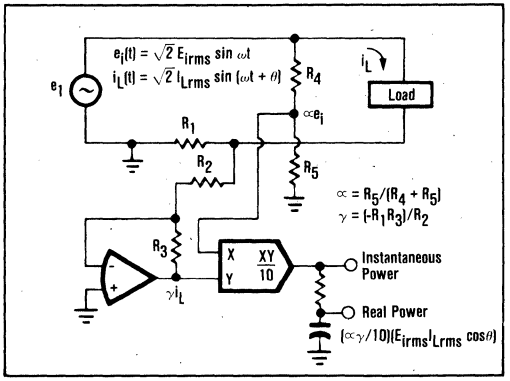


FIGURE 11. Single-Phase Instantaneous and Real Power Measurement.

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{cc}$ and $-V_{cc}$ pins of the 4213 to the power supply common. The connection of these capacitors should be as close to the 4213 as practical.

CAPACITIVE LOADS

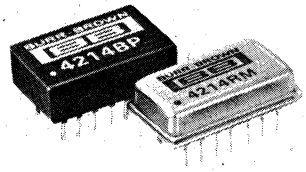
Stable operation is maintained with capacitive loads to 1000pF in all modes typically, except the square root mode for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the 4213's output.

MORE CIRCUITS

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the Burr-Brown McGraw Hill book "FUNCTION CIRCUITS - Design and Applications."

BURR-BROWN®

4214



MULTIPLIER - DIVIDER

FEATURES

- DIFFERENTIAL INPUTS
- LASER-TRIMMED
- GUARANTEED ACCURACY
  0.5% and 1%
- SELF-CONTAINED
  No additional parts required
- LOW NOISE
  120μV rms, 10Hz - 10kHz
- DIP PACKAGES

APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOTING
- ADAPTIVE CONTROL
- ALGEBRAIC COMPUTATION
- POWER COMPUTATION

DESCRIPTION

The 4214 family of multipliers are low cost integrated circuit multiplier/dividers designed for general purpose usage. In addition to four quadrant multiplication, they also perform division and square rooting of analog signals. They do not require use of additional amplifiers to perform these functions. The 4214 is laser-trimmed prior to final packaging and is guaranteed to its rated accuracy with no external components - a distinct advantage from standpoints of cost and reliability.

4214 contains its own zener regulated references and, as a result is much less sensitive to supply voltage variation than were earlier IC multipliers. The multipliers' output noise is only 120μV rms in a 10Hz to 10kHz bandwidth.

The unit is available in two 14 pin DIP packages. The plastic version ("P" package) is offered for minimum cost as is specified over the -25°C to +85°C range. The hermetic metal package ("M" package option) provides operation over the full -55°C to +125°C temperature range.

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ELECTRICAL SPECIFICATIONS

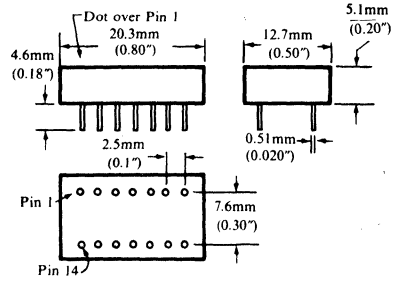
Typical performance at +25°C with rated power supplies unless otherwise noted.

MODEL	4214AP/RM	4214BP/SM
OUTPUT FUNCTION	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$	
TOTAL ERROR[1]		
Without Trimming	1% max	0.5% max
Error vs Temperature (-25°C to +85°C), (AP and BP)	0.008%/°C typ., 0.02%/°C max	
(-55°C to +125°C), (RM and SM)	0.025%/°C typ., 0.05%/°C max	
Error vs Supply	0.05%/%	
INDIVIDUAL ERRORS		
Output Offset	10mV typ	7mV typ
	50mV max	25mV max
vs Temperature	0.7mV/°C typ	0.3mV/°C typ
	2mV/°C max	0.7mV/°C max
vs Supply	0.25mV/%	
Scale Factor Error	0.12%	
vs Temperature	0.008%/°C	
vs Supply	0.05%/%	
Nonlinearity		
X(X = 20V p-p, Y = ±10VDC)	±0.08%	
Y(Y = 20V p-p, X = ±10VDC)	±0.01%	
Feedthrough at 50 Hz		
X = 20V p-p, Y = 0	30mV p-p	
Y = 20V p-p, X = 0	6mV p-p	
vs Temperature	0.1mV p-p/°C	
vs Supply	0.15mV p-p/%	
AC PERFORMANCE		
Small Signal ±3dB Flatness	610 kHz	
Small Signal ±1% Flatness	90 kHz	
Small Signal ±1% Vector Error (0.57° Phase Shift)	7.5 kHz	
Full Power Bandwidth	330 kHz	
Slew Rate	23V/μs	
Settling Time to 1% (20V step)	1.7μs	
OUTPUT NOISE (X = Y = 0)		
10 Hz to 10 kHz	120μV rms	
10 Hz to 10 MHz	700μV rms	
INPUT CHARACTERISTICS		
Input Voltage Range		
Rated Operation, min.	±10V	
Absolute max	±V_s	
Input Impedance, X, Y, Z[2]	10 MΩ	
Input Bias Current, X, Y, Z	1.4μA	
OUTPUT CHARACTERISTICS		
Rated Output	±10V at ±5mA min	
Output Impedance	1.5Ω	
POWER SUPPLY REQUIREMENTS		
Rated Voltage	±15V	
Operating Range	±8.5VDC to ±20VDC	
Quiescent Current	±5.5mA	
TEMPERATURE RANGE		
Rated Performance (specification)	AP and BP	−25°C to +85°C
	RM and SM	−55°C to +125°C
Operation		−55°C to +125°C
Storage	AP and BP	−40°C to +85°C
	RM and SM	−65°C to +150°C

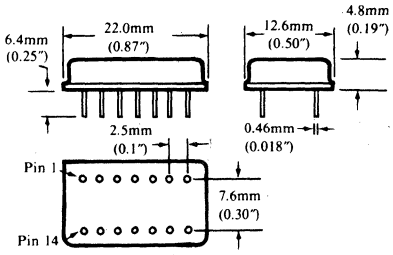
1. Total error is the maximum allowed value of the sum of the individual errors.
2. Z_2 input impedance is 10 MΩ typ with Pin 11 open circuit. If Pin 11 is grounded or used for optional offset adjustment the Z_2 input impedance may become as low as 25kΩ.

MECHANICAL

4214AP, 4214BP
Weight: 2.9 grams (0.10 oz.)

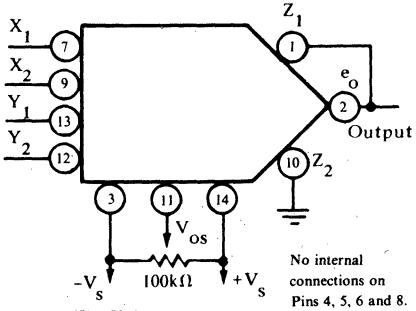


4214RM, 4214SM
Weight: 3.9 grams (0.13 oz.)



Connector: 0145MC (14-pin DIP)
Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

CONNECTION DIAGRAM



No internal connections on Pins 4, 5, 6 and 8.

$$e_o = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$$

NOTE: V_{os} adjustment optional, not normally recommended. Pin 11 may be left open or grounded.

4214

TYPICAL PERFORMANCE CURVES

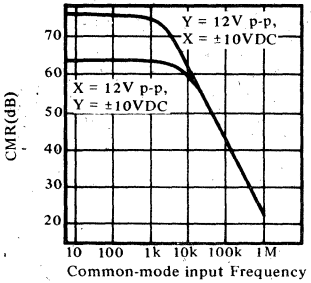


FIGURE 1. Common-mode Rejection vs. Frequency.

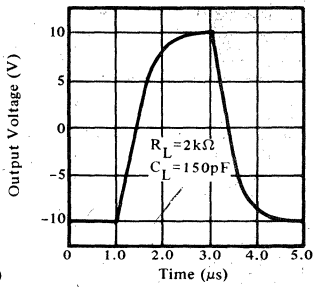


FIGURE 2. Step Response.

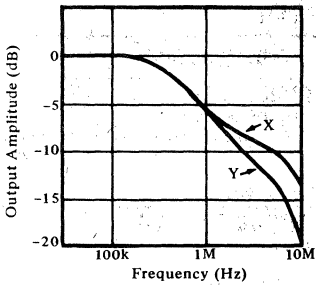


FIGURE 3. Small-signal Frequency Response.

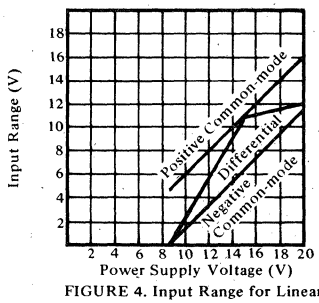


FIGURE 4. Input Range for Linear Response.

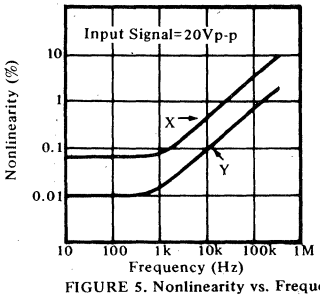


FIGURE 5. Nonlinearity vs. Frequency.

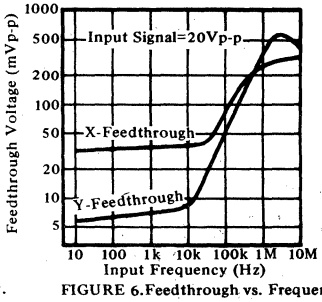


FIGURE 6.Feedthrough vs. Frequency.

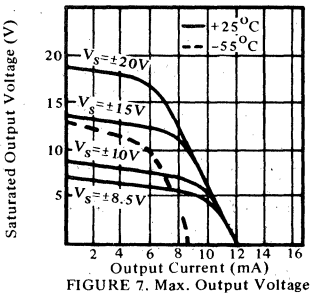


FIGURE 7. Max. Output Voltage vs. Output Current.

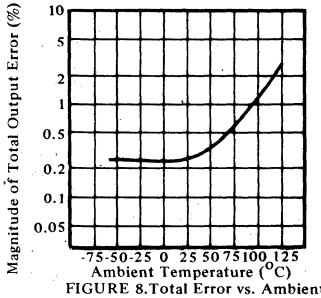


FIGURE 8.Total Error vs. Ambient Temperature.

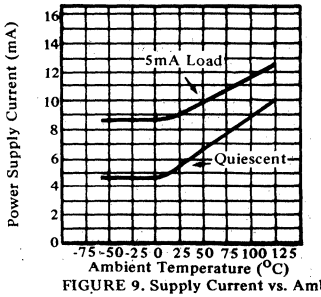


FIGURE 9. Supply Current vs. Ambient Temperature.

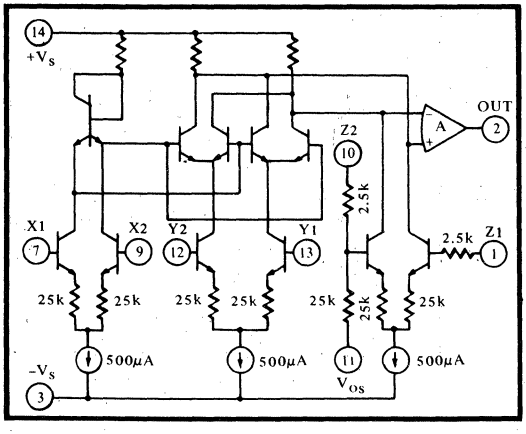


FIGURE 10. Simplified Equivalent Circuit.

OPERATING MODES MULTIPLICATION

The 4214 is a general purpose multiplier/divider with three sets of differential inputs viz. X, Y, and Z. Its open-loop transfer function is

$$e_O = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2)\right]$$

where, A is the open-loop gain of the internal output amplifier (see the simplified equivalent circuit, Figure 10). Due to very high gain ($A \rightarrow \infty$) of the output amplifier the feedback from the output to any of the inputs will establish the relationship

$$Z_1 - Z_2 = (X_1 - X_2)(Y_1 - Y_2)/10$$

Taking output at Z_1 the multiplication mode transfer function is obtained and is expressed as

$$e_O = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2.$$

This connection of 4214 is shown on page 2.

DIVISION

The 4214 may be used as a two quadrant divider, without the need for an external op amp. Note that the maximum output error in the divide mode is given approximately by,

$$\text{Divider error} \simeq \frac{10 \in m}{X_1 - X_2}, \text{ where } \in m \text{ is}$$

the total error specified for the multiply mode. The divider error, as shown above, becomes excessively large for small values of $(X_1 - X_2)$. A 10:1 denominator range is usually the practical limit. This is true for all such units, where a multiplier is used in voltage feedback mode to generate "divide" function.

If more accurate division is required over wide range of denominator voltages, the Burr-Brown model 4291 is recommended (0.25% max error over 100:1 range).

For optimum performance, the Z offset should be nulled by letting the input be zero and adjusting R_1 for zero output. This offset adjustment will improve the divider error to about $\frac{3 \in m}{(X_1 - X_2)}$ for $(X_1 - X_2)$ much less than 10V.

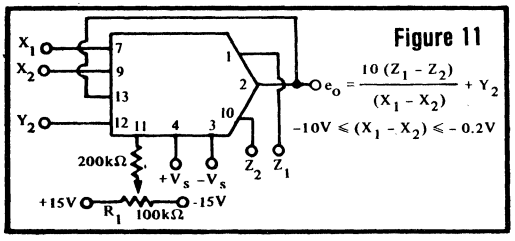


FIGURE 11. Divide Mode Connections - 4214.

SQUARE ROOT

By applying feedback from the output to both the X and Y inputs, the square root function can be obtained. The errors in the square root mode become large for small values of Z input. The actual output is approximately

$$\text{Square root output } e_o \simeq \sqrt{10(Z_1 - Z_2) + 10 \in m}$$

where $\in m$ is the total error for the multiply mode.

Burr-Brown's multifunction converter model 4302 is recommended for applications requiring more accuracy over wider dynamic range.

The output offset should be nulled for optimum performance by allowing the input to be its smallest expected value and adjusting R_1 for the proper output voltage.

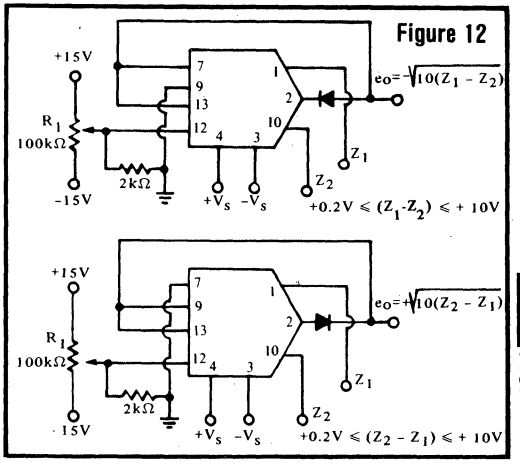


FIGURE 12. Square Root Mode Connections - 4214.

SINE FUNCTION GENERATOR

Two 4214's can be connected with implicit feedback as shown in Figure 13 to implement the following sine function approximation.

$$e_o = \frac{1.5715\, e_i - 0.004317\, e_i^3}{1 + 0.001398\, e_i^2} = 10 \text{ Sin } 9\, e_i$$

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the new Burr-Brown/McGraw Hill book "FUNCTION CIRCUIT - Design and Applications."

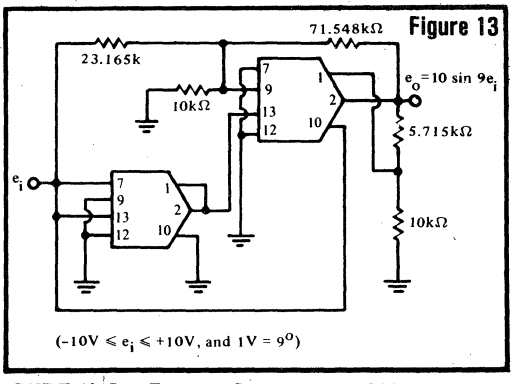


FIGURE 13. Sine Function Connections - 4214.

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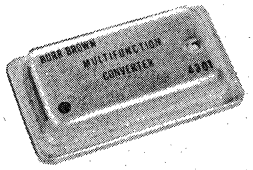
4301



Low Cost MULTIFUNCTION CONVERTER

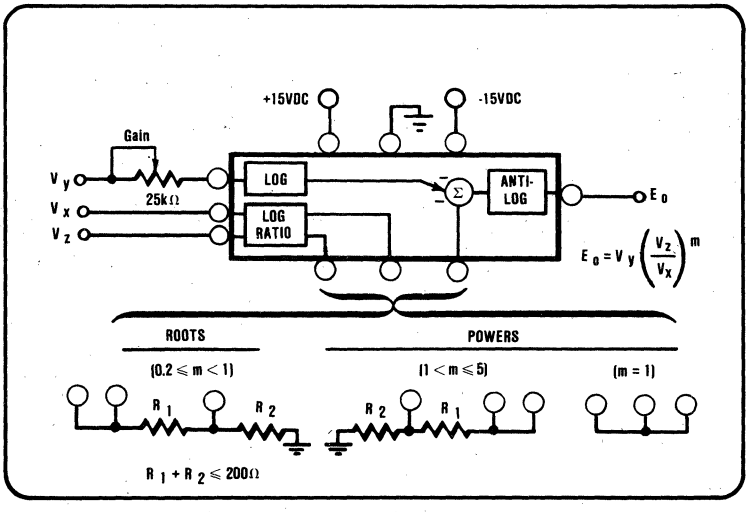
FEATURES

- LOW COST
- SMALL PACKAGE - Dual-in-line
- HERMETIC, SHIELDED PACKAGE
- UNIVERSAL CONVERTER

FUNCTIONS	ACCURACY
MULTIPLY	±0.25%
DIVIDE	±0.25%
SQUARE	±0.03%
SQUARE ROOT	±0.07%
EXPONENTIATE	±0.15% (m = 5)
ROOTS	±0.2% (m = 0.2)
SINE θ	±0.5%
COSINE θ	±0.8%
TAN^{-1} (Y/X)	±0.6%
$\sqrt{X^2 + Y^2}$	±0.07%

DESCRIPTION

Burr-Brown's multifunction converter model 4301 is a low-cost solution to many analog conversion needs. Much more than just another multiplier divider, the 4301 out performs many analog circuit functions with a very-high degree of accuracy at a very-low total cost to the user.



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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and with rated supply unless otherwise noted.

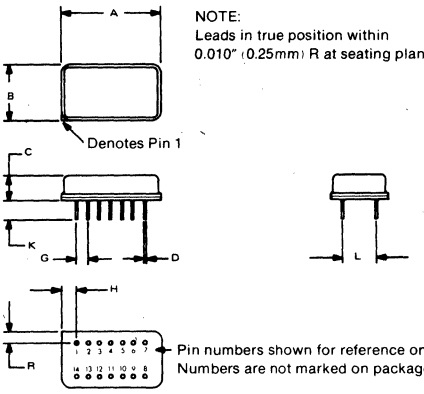
MODEL	4301
TRANSFER FUNCTION	$E_o = V_Y (V_Z/V_X)^m$
RATED OUTPUT	
Voltage	+10.0V
Current	5mA
INPUT	
Signal Range	$0 \leq (V_X, V_Y, V_Z) \leq +10V$
Absolute Maximum	$(V_X, V_Y, V_Z) \leq \pm 18V$
Impedance (X/Y/Z)	100kΩ/90kΩ/100kΩ
EXPONENT RANGE(1)	
Roots ($0.2 \leq m < 1$)	$m = [R_2/(R_1 + R_2)]$
Powers ($1 < m \leq 5$)	$m = [(R_1 + R_2)/R_2]$
Powers ($m = 1$)	$R_1 = 0\Omega$, R_2 not used
POWER REQUIREMENTS	
Rated Supply	±15VDC
Range	±12VDC to ±18VDC
Quiescent Current	±10mA
TEMPERATURE RANGE	
Operating	−25°C to +85°C
Storage	−55°C to +125°C

NOTE: 1. Refer to Figure 1.

General specifications for the Model 4301 Multifunction Converter are shown above; Figure 1 is a functional diagram. These specifications characterize the 4301 as a versatile three input multifunction converter.

Applications information to help you apply the 4301 to your particular need is shown in the product data sheet for model 4302. The dedicated circuit configurations needed to produce the multiplication, division, exponentiation, square rooting, squaring, sine, cosine, arctangent, and vector algebraic functions are shown along with information for model 4302.

MECHANICAL



NOTE:
Leads in true position within 0.010" (0.25mm) R at seating plane.

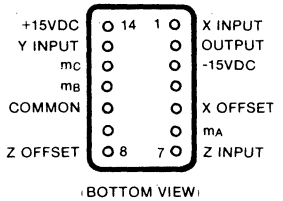
Pin numbers shown for reference only.
Numbers are not marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

CASE: Kovar or equiv.
WEIGHT: 0.15 oz. (3.4 grams)
CONNECTOR: 14-pin DIP connector
Burr-Brown Model No. 0145MC

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

PIN CONNECTIONS



(BOTTOM VIEW)

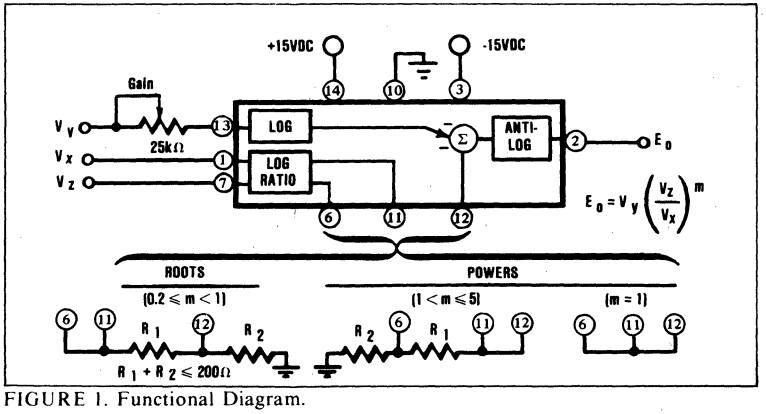


FIGURE 1. Functional Diagram.

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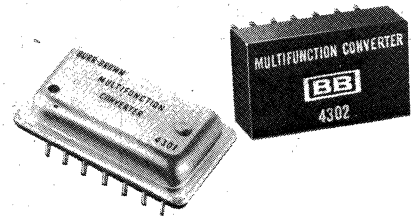

4302

Low Cost MULTIFUNCTION CONVERTER

FEATURES

- LOW COST
- SMALL PACKAGE - Dual-in-line
- RELIABLE HYBRID CONSTRUCTION
- VERSATILE

FUNCTIONS	ACCURACY
MULTIPLY	±0.25%
DIVIDE	±0.25%
SQUARE	±0.03%
SQUARE ROOT	±0.07%
EXPONENTIATE	±0.15% (m = 5)
ROOTS	±0.2% (m = .2)
SINE θ	±0.5%
COSINE θ	±0.8%
TAN $^{-1}$ (Y/X)	±0.6%
$\sqrt{X^2 + Y^2}$	±0.07%

Typical accuracies expressed as a % of output full scale (+10VDC) at 25°C

DESCRIPTION

Burr-Brown's multifunction converter model 4302 is a low cost solution to many analog conversion needs. Much more than just another multiplier/divider, the 4302 out performs many analog circuit functions with a very high degree of accuracy at a very low total cost to the user.

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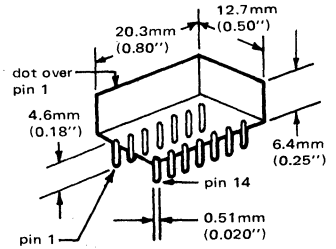
SPECIFICATIONS

Performance typical at 25°C and with rated supply unless otherwise noted.

ELECTRICAL

MODEL	4302
TRANSFER FUNCTION	$E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$
RATED OUTPUT	
Voltage	+10.0 V
Current	5 mA
INPUT	
Signal Range	$0 \leq (V_X, V_Y, V_Z) \leq +10$ V
Absolute Maximum	$(V_X, V_Y, V_Z) \leq \pm 18$ V
Impedance (X/Y/Z)	100 kΩ/90 kΩ/100 kΩ
EXPONENT RANGE	
Roots ($0.2 \leq m < 1$)	$m = \frac{R_2}{R_1 + R_2}$ Refer to Functional Diagram below
Powers ($1 < m \leq 5$)	$m = \frac{R_1 + R_2}{R_2}$
($m = 1$)	$R_1 = 0\ \Omega$, R_2 not used
POWER REQUIREMENTS	
Rated Supply	±15 VDC
Range	±12 to ±18 VDC
Quiescent Current	±10 mA
TEMPERATURE RANGE	
Operating	−25°C to +85°C
Storage	−25°C to +85°C

MECHANICAL

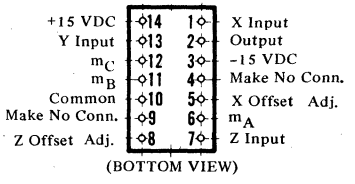


Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-pin DIP

0145MC Price: $3.75 ea.

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

PIN CONNECTIONS



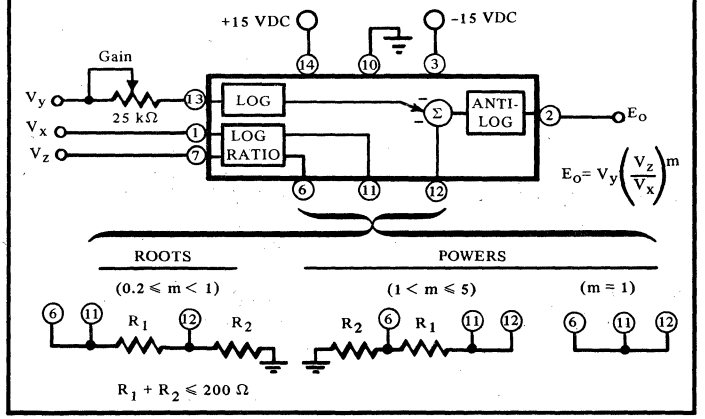
(BOTTOM VIEW)

General specifications for the Model 4302 Multifunction Converter are presented on this page. These specifications characterize the 4302 as a versatile three input multifunction converter.

The following pages are applications oriented to help you apply the 4302 to your particular circuit function need. These pages contain dedicated circuit configurations in order to produce the functions of: multiplication, division, exponentiation, square rooting, squaring, sine, cosine, arctangent, and vector algebra.

It is the purpose of this product data sheet to enable you to apply the 4302 to your analog conversion needs quickly and efficiently.

4302 FUNCTIONAL DIAGRAM



Many of the following circuit configurations using the 4302 require a reference voltage for scaling purposes. The reference voltage is shown to be +15 VDC (+15 VDC REF.) since in most cases the +15 VDC power source for the 4302 has sufficient time and temperature related stability to achieve the specified typical accuracies.

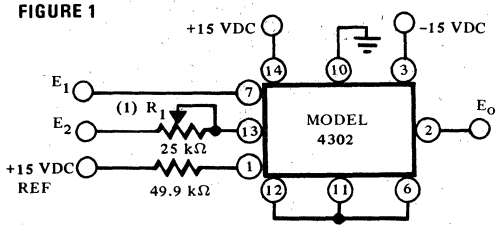
If the particular supplies which are available for powering the 4302 do not have the necessary stability for the required conversion accuracy, an additional +15 VDC precision supply may be required.

MULTIPLIER/DIVIDER FUNCTIONS

MULTIPLIER

In multiplier applications the 4302 provides high accuracy at a low cost. The 4302 accepts inputs up to +10 VDC and provides a typical accuracy of ±0.25% of full scale.

FIGURE 1



(1) Set R_1 so that with $E_1 = E_2 = +10.00$ VDC, $E_o = +10.00$ VDC.

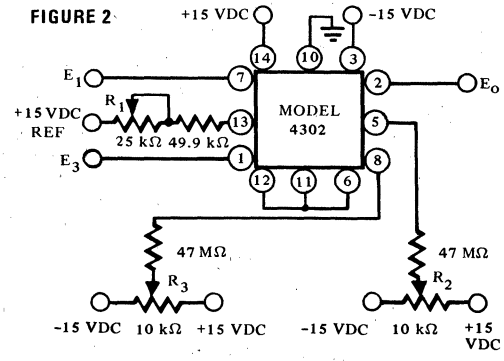
Transfer Function	$E_o = +\frac{E_1 E_2}{10}$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for input range)	$\begin{cases} 0.03V \leq E_1 \overset{*}{\leq} 10\ V \\ 0.01\ V \leq E_2 \leq 10\ V \end{cases}$
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = E_2 = 0$)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±0.2 mV/°C
NOISE (10 Hz to 1 kHz)	100 μV rms
BANDWIDTH (E_1, E_2)	
Small Signal (-3 dB)	500 kHz
Full Output	60 kHz

DIVIDER

As a divider, the 4302 outperforms many of the multiplier/dividers on the market at a much lower cost. In the divider configuration the 4302 boasts a typical conversion accuracy of ±0.25% of full scale.

Transfer Function	$E_o = +10\ (E_1/E_3)$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for $E_1 \leq E_3$ and input range)	$\begin{cases} 0.03V \leq E_1 \overset{*}{\leq} 10\ V \\ 0.1\ V \leq E_3 \leq 10\ V \end{cases}$
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = 0$, $E_3 = +10$ V)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±1 mV/°C
NOISE (10 Hz to 1 kHz)	
$E_3 = +10$ V	100 μV rms
$E_3 = +0.1$ V	300 μV rms
BANDWIDTH (E_1, E_3)	
Small Signal (-3 dB)	500 kHz
Full Output ($E_3 = +10$ V)	60 kHz

FIGURE 2



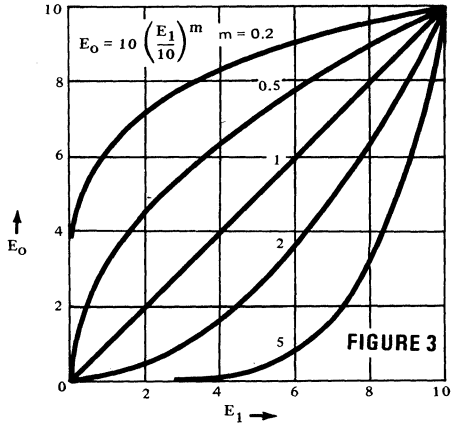
NOTES:
(1) Set R_1 so that with $E_1 = E_3 = +10.00$ VDC, $E_o = +10.00$ VDC.
(2) Set R_2 so that with $E_1 = E_3 = +0.10$ VDC, $E_o = +10.00$ VDC.
(3) Set R_3 so that with $E_1 = +0.01$ VDC and with $E_3 = +0.10$ VDC, $E_o = +1.00$ VDC.
(4) Repeat steps 1 through 3 as necessary to achieve the specified output voltages.

* The input voltage may be extended below 0.03V by connecting a 0.047 μF capacitor between pins 11 and 5, causing a slight reduction in bandwidth. (Multiply and Divide Modes).

EXPONENTIAL FUNCTIONS

Model 4302 may be used as exponentiator over a range of exponents from 0.2 to 5. The exponents 0.5 and 2, square rooting and squaring respectively, are often used functions and are treated below. Other values of exponents (m) may be useful in terms of linearization of nonlinear functions or simply for producing the mathematical conversions. Characteristics of m = 0.2 and m = 5 are presented on the right. For other values of m the curves presented in Figure 3 may be used to interpolate the error for a nonspecified value of m.

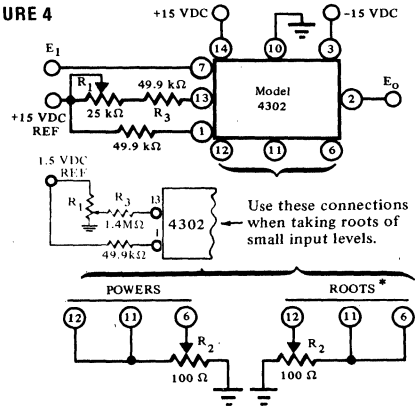
Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^m$
Total Conversion Error (typical)	
m = 0.2	
0.5 VDC < $E_1 \leq$ 10 VDC	±2 m VDC
0.1 VDC < $E_1 \leq$ 0.5 VDC	±25 m VDC
m = 5	
1.0 VDC < $E_1 \leq$ 10 VDC	±15 m VDC
Exponent Range (continuous)	$0.2 \leq m \leq 5$
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC



Exponentiator Transfer Characteristics

NOTES:
(1) Connect a 100 Ω potentiometer as shown in Figure 4 for either roots ($0.2 \leq m < 1$) or powers ($1 < m \leq 5$).
(2) Set R_1 so that with E_1 = +10.00 VDC, E_o = +10.00 VDC.
(3) Select a + DC voltage level (E_1) such that the output voltage (E_o), as acted upon by the desired exponent, will not exceed +10.00 VDC. A level which is mid-range for input values of interest is an appropriate one to use. Set R_2 so that the output voltage (E_o) is the value expected for the chosen values of input (E_1) and exponent (m).

FIGURE 4



(4) Repeat steps (2) through (4) as necessary.

* When taking roots of smaller input levels, a modified transfer equation $[E_o = (10E_1)^m]$ will provide improved conversion accuracy. To achieve this transfer function: 1) apply a +1.5 VDC REF in place of the +15 VDC REF shown in Figure 4., 2) make R_3 a 1.40 MΩ resistor, and rearrange R_1 and R_3 as 1.5VDC REF and 3) follow all notes except in note (2) apply +0.10VDC to pin 7 to set R_1 to E_o = +1.00VDC.

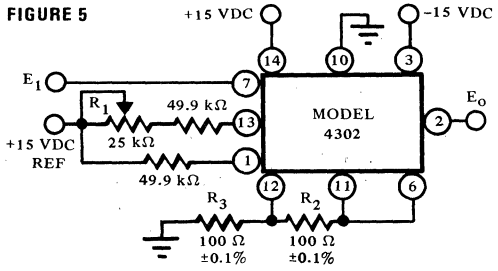
SQUARE ROOT

As a Square Rooter (m = 0.5), the 4302 provides a typical total conversion accuracy of ±0.07%. Refer to Figure 5 and notes for connections and adjustments respectively.

Transfer Function	$E_o = 10\sqrt{\frac{E_1}{10}}$
Total Conversion Error (Typical)	
0.5 VDC < E_1 ≤ 10 VDC	±7 mV
0.02 VDC < E_1 ≤ 0.5 VDC	±55 mV
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC

NOTES:
(1) Connect pins 12, 11, and 6 together. Set R_1 such that with E_1 = +10.00 VDC; E_o = +10.00 VDC.
(2) Connect 100 Ω resistors as shown in Figure 5.
(3) For greater conversion accuracy, R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

FIGURE 5



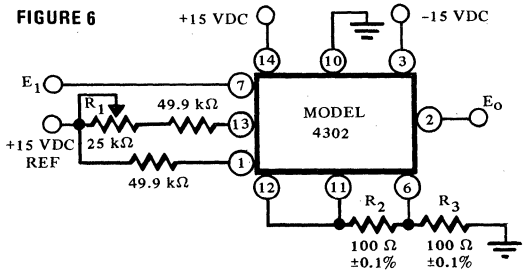
SQUARE

Configured as a Square Function Converter (m = 2), the 4302 produces high conversion accuracies of typically 0.03%. Please refer to Figure 6 and accompanying notes.

Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^2$
Total Conversion Error (typical)	
0.1 VDC ≤ E_1 ≤ 10 VDC	±3 mV
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC

NOTES:
(1) Set R_1 such that with E_1 = +10.00 VDC, E_o = +10.00 VDC.
(2) Connect 100 Ω resistors as shown in Figure 6.
(3) For greater conversion accuracy R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

FIGURE 6



TRIGONOMETRIC FUNCTIONS

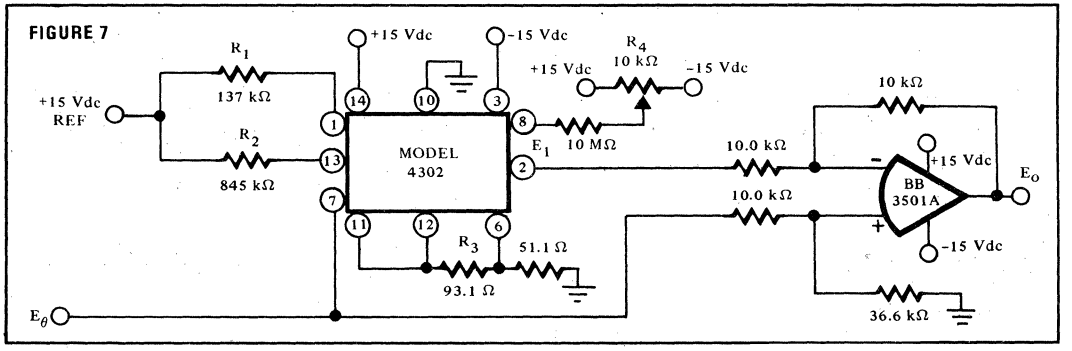
SINE

Sine functions can be accurately generated from input voltage levels representing angular displacement from 0 to 90°. Model 4302 configured as in Figure 7 will produce the sine power series approximations with modified coefficients to typically better than ±0.5% of full scale. In this circuit, the 4302 is scaled so that when $\theta = 0$, $E_O = 0$ VDC, and when $\theta = 90$, $E_O = 10$ VDC.

NOTES:
(1) Adjust R_4 if needed so that $E_1 < 1$ m VDC when $E_\theta = 0$.
(2) Adjust R_2 so that $E_1 = +0.8045$ VDC when $E_\theta = +5.00$ VDC.
(3) Adjust R_3 so that $E_1 = +5.709$ VDC when $E_\theta = +10.00$ VDC.
(4) Repeat steps (2) and (3) as necessary.

Transfer Function	$E_O = 10 \text{ Sin } 9E_\theta$
Power Series Approximation $E_O = 1.5708E_\theta - 1.5924\left(\frac{E_\theta}{6.366}\right)^{2.827}$	
Total Conversion Error (typical)	±50 mV
Input Voltage Range ($0 \leq \theta \leq 90^o$)	0 to +10 VDC
Output Voltage Range ($0 \leq \sin\theta \leq 1$)	0 to +10 VDC

FIGURE 7



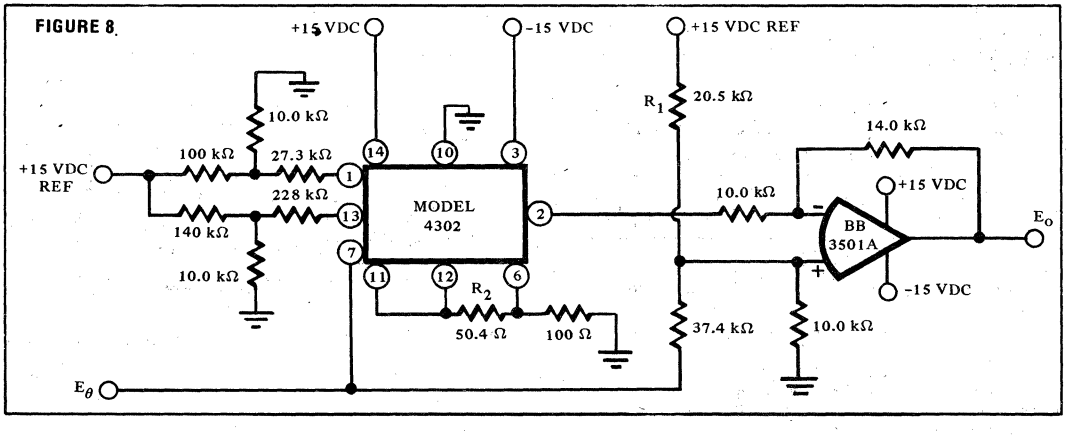
COSINE

Connected as in Figure 2, the Model 4302 will generate a cosine function of the input voltage. Typical accuracies of ±0.8% can be expected from this configuration.

NOTES:
(1) Adjust R_1 so that $E_O = +10.00$ VDC when $E_\theta = 0$.
(2) Adjust R_2 so that $E_O = 0$ when $E_\theta = +10.00$ VDC.

Transfer Function	$E_O = 10 \cos 9E_\theta$
Power Series Approximation $E_O = 10 + 0.3652\,E_\theta - 0.4276E^{1.504}$	
Total Conversion Error (typical)	±80 mV
Input Voltage Range ($0 \leq \theta \leq 90^o$)	0 VDC to +10 VDC
Output Voltage Range ($1 \leq \cos\theta \leq 0$)	+10 VDC to 0 VDC

FIGURE 8



ARCTANGENT

Model 4302 and the associated circuitry shown below will produce the inverse tangent of a ratio. This application is particularly well suited to conversion from rectangular coordinates to polar coordinates where

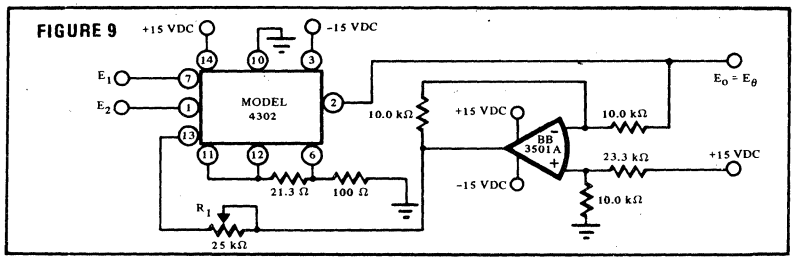
$$E_\theta = \tan^{-1}\frac{E_Y}{E_X}$$

The accuracy of conversion depends upon the levels of the input signals. Please refer to table at right.

NOTE:
(1) Set R_1 so that with $E_1 = E_2 = +10.00$ VDC, $E_o = +4.500$ VDC ±1 mVDC.

Transfer Function	$E_o = \tan^{-1}\left(\frac{[E_1]}{[E_2]}\right)$
Power Series Approximation	$E_o = \frac{\left(\frac{[E_1]}{[E_2]}\right)^{1.2125}}{1+\left(\frac{[E_1]}{[E_2]}\right)^{1.2125}}(90^o)$
Total Conversion Error $2 < E_1, E_2 \leq 10$ VDC $0.1 < E_1, E_2 \leq 2$ VDC $0.03 < E_1, E_2 \leq 0.1$ VDC Input Voltage Range (E_1, E_2) Output Voltage Range $0 \leq E_\theta \leq 90^o$	 ±55 m VDC ±65 m VDC ±340 m VDC +0.01 VDC to +10 VDC 0 VDC to +9 VDC

FIGURE 9



VECTOR MAGNITUDE FUNCTION

The model 4302 will produce the square root of the sum of the squares of two inputs. This function is companion to the arctangent of a ratio for the conversion of rectangular to polar coordinates.

Transfer Function	$E_o = \sqrt{E_1^2 + E_2^2}$
Input Voltage Range E_1 E_2	0 to +10VDC -10VDC to +10VDC
(refer to notes 1 and 2)	
Output Voltage Range	0 to +10VDC
Conversion Error	±7m VDC

NOTES:
1. Figure 10 shows one practical way to implement the transfer function $E_o=\sqrt{E_1^2+E_2^2}$ using 4302. It shows use of model 3501A op amp. Model 3501's rated output is ±10V. This limits the range of E_1 and E_2, such that the conditions $E_1 \leq \sqrt{100 - E_2}$ and $|E_2| \leq (5 - E_1^2/20)$ and $\sqrt{E_1^2 + E_2^2} \leq 10$ are always satisfied.
(a) The above conditions imply, $0V \leq E_1 \leq 10V$ and $-5V \leq E_2 \leq 5V$.
(b) The above conditions also imply that for applications where $E_1 = |E_2|$ the range would be limited to 4.142V max.
2. Use of model 3627 as shown in Figure 11 would directly substitute the eight 10kΩ resistors and the two model 3501A op amps. This would reduce the number of components needed to implement vector magnitude function and reduce overall cost.

FIGURE 10

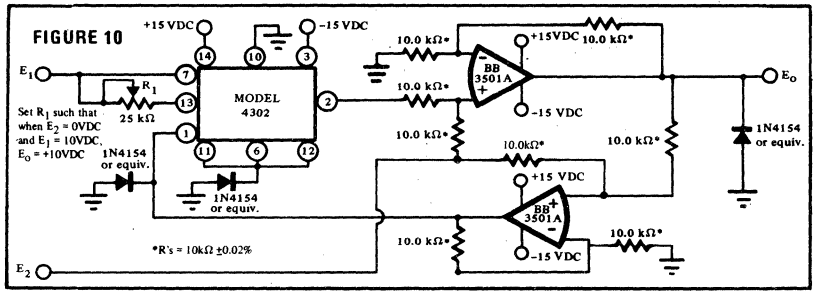
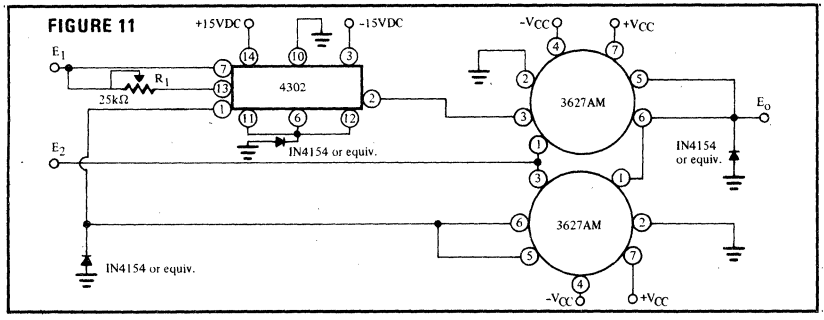
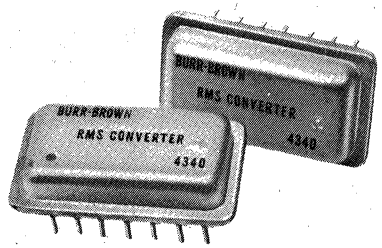


FIGURE 11



BURR-BROWN®

4340



TRUE RMS-TO-DC CONVERTER

FEATURES

- LOW COST
- HIGH ACCURACY
  ±0.3mV ±0.1% Reading
- HIGH INPUT IMPEDANCE - 5kΩ
- HERMETIC METAL PACKAGE

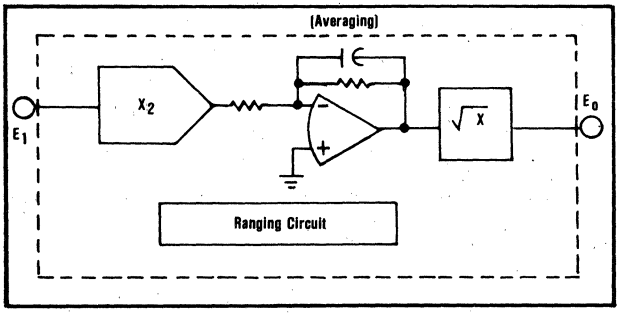
DESCRIPTION

The Burr-Brown Model 4340 is a true rms-to-DC converter featuring high performance, low cost, and a small hermetic package. The 4340 will compute the true rms value of a variety of signals applied to the input. The input signal may consist of complex AC waveforms as well as a DC voltage level. The output of the 4340 is a DC voltage, the amplitude of which is equal to the rms value of the input voltage.

The 4340 will accept input voltages from 0 to ±10V over a wide input frequency range. The conversion accuracy of the 4340 is specified in terms of error in millivolts plus a percent of reading, as a function of input signal level over an input frequency range.

The 4340 has an input impedance of 5kΩ and an output impedance of 1Ω. This product will supply up to 5mA of output current at a voltage of +10VDC. The input is fully protected for conditions of overvoltage up to the supply voltage. The output will withstand short-circuit to power supply common for an indefinite period of time.

The specified unadjusted performance characteristics of the 4340 are shown in the Electrical Specifications. Provision for the external adjustment of gain, voltage offset, DC reversal error, and frequency response performance allow the user to improve upon the specified conversion accuracies to the degree required by the user's application.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Typical at 25°C with rated power supplies unless otherwise noted.

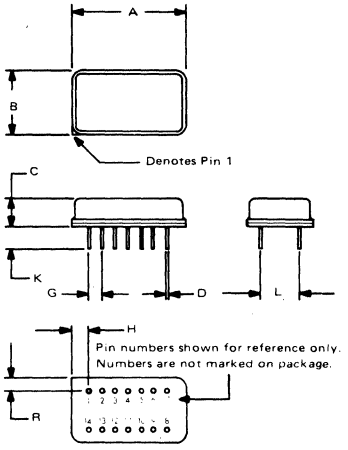
MODEL	4340
TRANSFER FUNCTION	E_o (DC) = $\sqrt{\overline{E_{IN}2}}$
INPUT	
Peak Voltage	±10VDC
Absolute Maximum Voltage	±Supply
Impedance	5kΩ
OUTPUT	
Voltage	0 to +10VDC
Current, min	+5mA
Impedance	1Ω
CONVERSION ACCURACY	
Total Unadjusted Error, max	
Input: 10mV, rms to 7V, rms	±2mV ±0.2% Reading
Input: 100Hz to 10kHz sine wave*	
Total Adjusted Error**	
Input: 10mV, rms to 7V, rms	±0.3mV ±0.1% Reading
Input: 50Hz to 20kHz*	
STABILITY	
Accuracy vs Temperature	±0.001% of FSR plus ±0.01% of reading per °C
Accuracy vs Supply	±0.001% of FSR plus ±0.01% of reading per %ΔV
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +125°C
POWER REQUIREMENTS	
Rated Voltage	±15VDC
Voltage Range	±14VDC to ±16VDC
Quiescent Current	±12mA

*Model 4340 will convert DC inputs. Lower frequency AC input signals will require the addition of external capacitors to preserve the accuracy.

**Performance with external trims and $C_L \geq 3\mu F$ and $20pF \leq C_H \leq 100pF$.

MECHANICAL

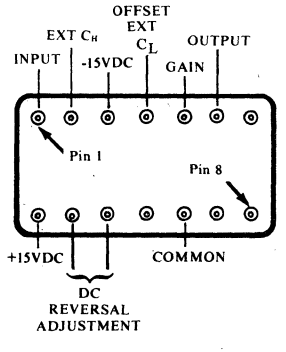
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Pin material and plating composition meet method 2003 (solderability) of MIL-STD-883 (except for paragraph 3.2.1).

PIN CONNECTIONS



(BOTTOM VIEW)

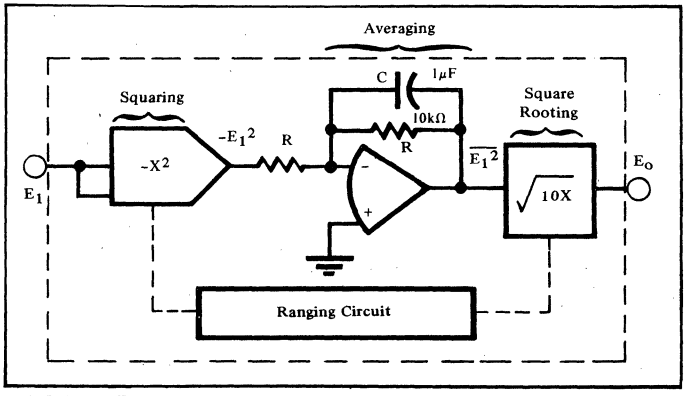


FIGURE 1. Functional Block Diagram of Model 4340.

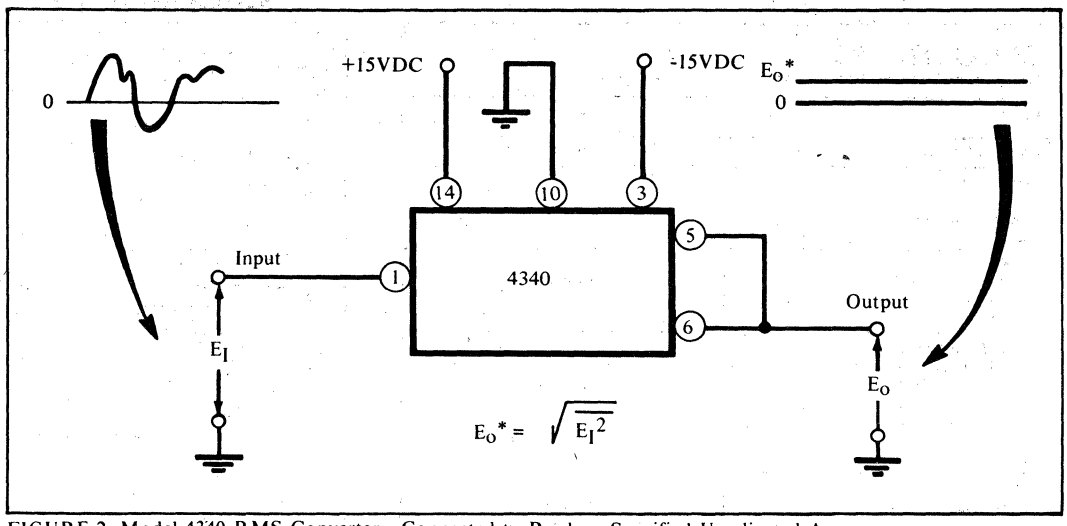


FIGURE 2. Model 4340 RMS Converter - Connected to Produce Specified Unadjusted Accuracy.

OPTIONAL EXTERNAL ADJUSTMENTS

Although the unadjusted performance of the 4340 is quite high for most applications, optimized performance can be achieved with external adjustments. The following paragraphs and figures will demonstrate the techniques for external adjustments of gain, voltage offset, DC reversal error, and frequency response. The unity gain adjustment should be made first, then the offset voltage adjustment. The unity gain adjustment should then be repeated for best results.

UNITY GAIN

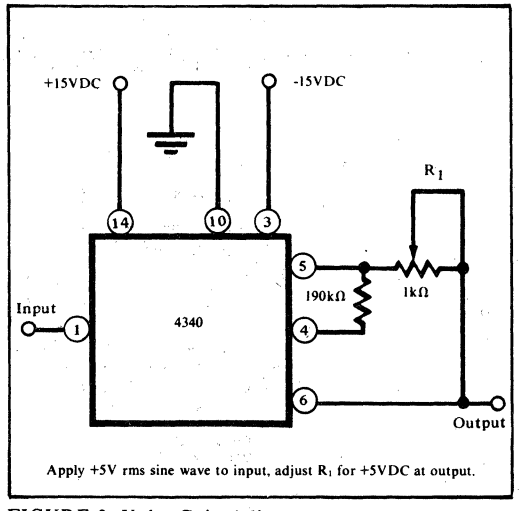


FIGURE 3. Unity Gain Adjustment.

OFFSET VOLTAGE

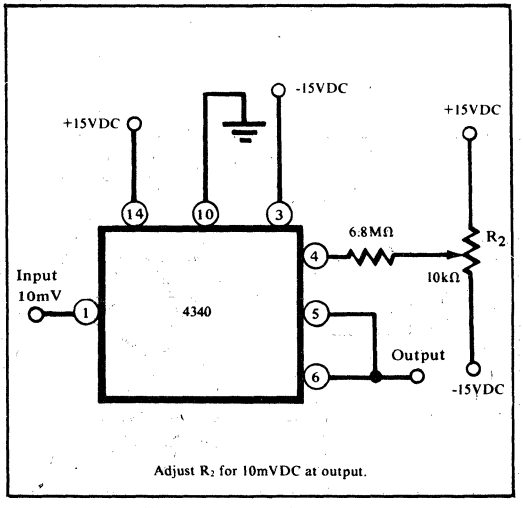
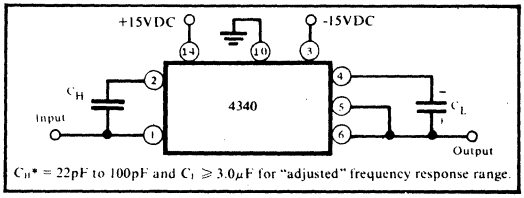


FIGURE 4. Offset Voltage Adjustment.

FREQUENCY RESPONSE

The conversion accuracy of the 4340 over a broad range of input frequencies can be enhanced by the addition of one or more externally connected capacitors. Referring to Figure 5, C_H will improve the high frequency performance and C_L will extend the low frequency response.



C_H* = 22pF to 100pF and $C_L \geq 3.0\mu F$ for "adjusted" frequency response range.

FIGURE 5. Frequency Response Adjustments.

HIGH FREQUENCY RESPONSE COMPENSATION

The upper limit of frequency response of the 4340 may be extended to meet the adjusted conversion accuracy specification by the proper selection of C_H.

Sweep a 1.0V rms signal from 10kHz to 20kHz, measure the output voltage change from 1.0VDC. Select a value for C_H that minimizes the change in output voltage over 10kHz to 20kHz frequency range.

*C_H may be selected from 22pF, 33pF, 47pF, or 100pF.

LOW FREQUENCY RESPONSE EXTENSION

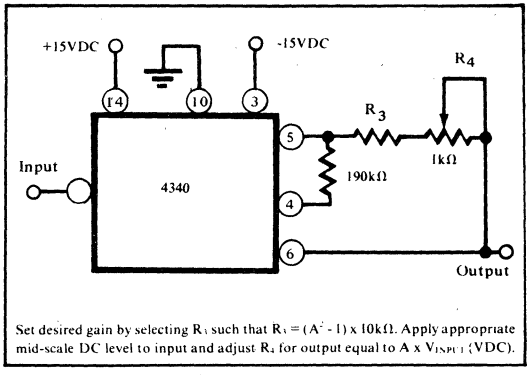
In the 4340, a single-pole, low-pass filter provides the averaging function. The time constant of this filter is selected to be 0.005 seconds. Larger time constants should be selected in order to achieve the conversion accuracy at frequencies lower than 100Hz.

The external capacitor can be 100's of microfarads, but the shunt resistance of the capacitor must be very large in order to maintain gain accuracy. The best value of C_L is inherently a compromise - the larger the capacitor the lower the ripple, but the response time is increased. Calculating the proper C_L for a given waveform can be done, but is tedious. The fastest method of choosing C_L is to apply a representative input signal, and observe the ripple at the output. Select various values of C_L until the ripple is attenuated sufficiently. The amount of allowable output ripple depends upon the application. For example, if the output is being read by an integrating digital voltmeter, the output ripple won't be critical.

ADDITIONAL ADJUSTMENTS

NON-UNITY GAIN

The 4340 may be adjusted to achieve a non-unity gain transfer function: $E_o = \sqrt{E_{IN}^2}$ for $1 < A \leq 10$. Figure 6 illustrates the technique to achieve this gain change.

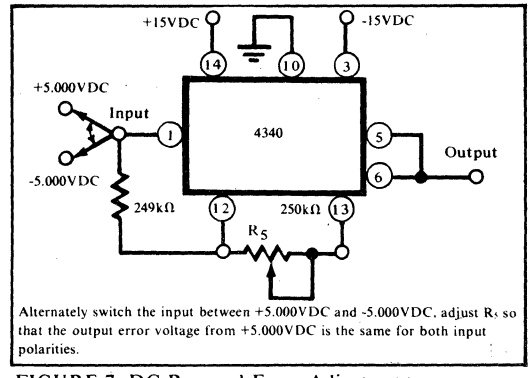


Set desired gain by selecting R_3 such that $R_3 = (A^2 - 1) \times 10k\Omega$. Apply appropriate mid-scale DC level to input and adjust R_4 for output equal to A x V_{INPUT} (VDC).

FIGURE 6. Non-Unity Gain Adjustment.

DC REVERSAL ERROR

When the 4340 is utilized with DC inputs and a high degree of conversion accuracy is required, a correction for DC reversal error may be required. Figure 7 illustrates the method to accomplish this adjustment.

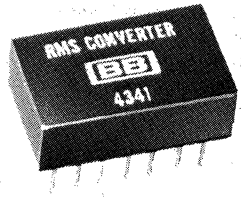


Alternately switch the input between +5.000VDC and -5.000VDC, adjust R_5 so that the output error voltage from +5.000VDC is the same for both input polarities.

FIGURE 7. DC Reversal Error Adjustment.

BURR-BROWN®

4341



Low Cost
TRUE RMS-TO-DC CONVERTER

FEATURES

- **LOW COST**
- **HIGH ACCURACY**
  ±0.2% ±2mV
- **HIGH RELIABILITY**
  Hybrid construction

DESCRIPTION

The Burr-Brown Model 4341 RMS-to-DC Converter features low cost without sacrificing performance. The 4341 computes a DC voltage proportional to the true rms value of signals which may be complex waveforms, DC levels, or a combination of both.

The input and output are fully protected against overvoltages and short circuits. Provisions for the external adjustment of gain, offset voltage, DC-reversal error, and frequency response make the 4341 versatile enough to fill the majority of your applications.

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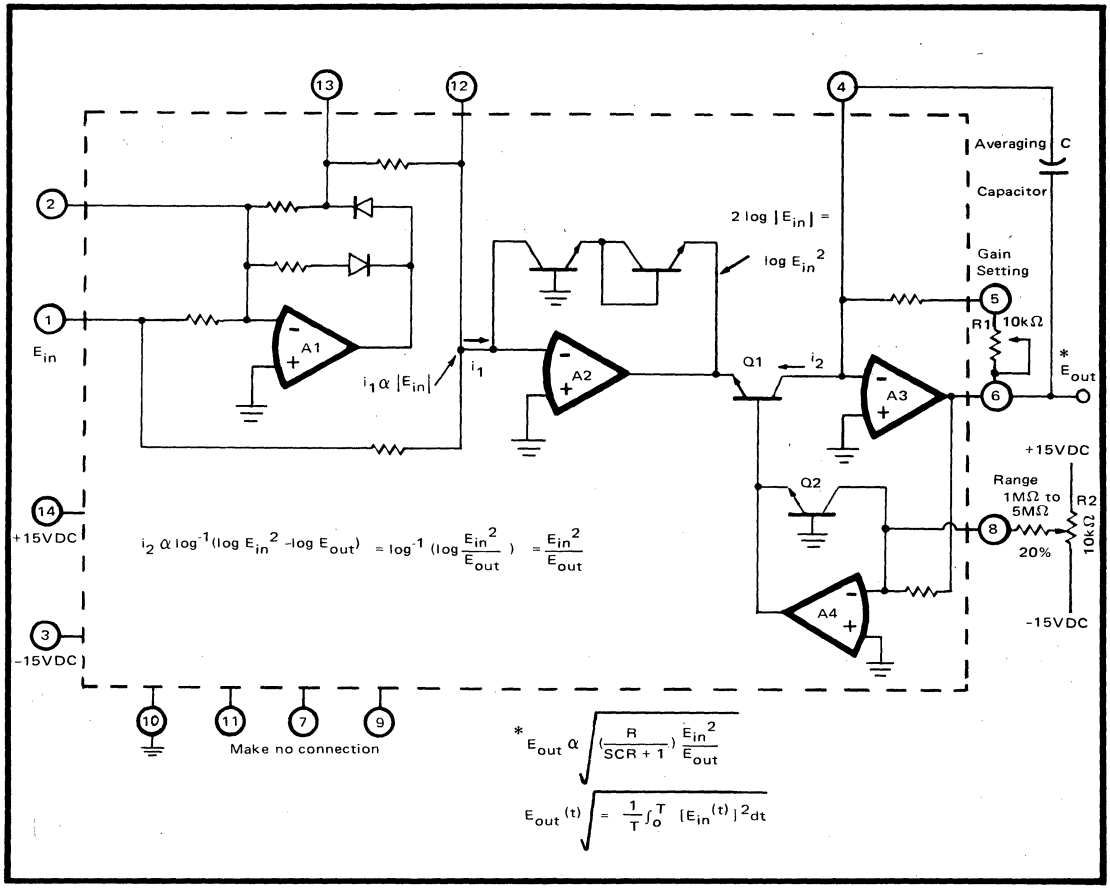


FIGURE 1. Simplified Schematic.

THEORY OF OPERATION

The true rms value of a time-varying signal E (t) over a time period T is

$$E_{rms} = \sqrt{1/T \int T/o\,[E(t)]^2\,dt}$$

The required operations are squaring, averaging and square rooting. A simplified schematic diagram of the 4341 is shown in Figure 1. The A1 circuit produces a current i_1 which is proportional to the rectified input voltage. The A2 circuit is a logarithmic amplifier which produces a voltage proportional to 2 log E_{in} or log E_{in}^2. The logarithmic gain of the A2 circuit is derived from the inherent exponential characteristics of transistor junctions. By using proprietary monolithic components, the circuit provides an accurate log function over many decades which is relatively insensitive to temperature variations. Amplifier A4 uses the same techniques as A2 to generate log E_{out}.

Transistor Q1 produces a collector current i_2 proportional to the antilog of its base-emitter voltage such that

$$i_2 \alpha \log^{-1} (\log E_{in}^2 - \log E_{out})$$
$$= \log^{-1} (\log E_{in}^2/E_{out}) = E_{in}^2/E_{out}$$

The A3 circuit which contains the external capacitor takes the time average of the i_2 signal and produces E_{out} which is directly proportional to the rms value of E_{in}.

Figures 2 and 3 show the effects of the external filter capacitor on ripple magnitude and response time. As the frequency of the input approaches DC, the 4341 begins to act like a full wave rectifier such that the output is the absolute value of the input. While the 4341 will accurately convert DC input voltages, the averaging capacitor must be made very large to minimize ripple at low frequencies.

ELECTRICAL SPECIFICATIONS

Typical at 25°C with rated supply voltages, unless otherwise noted.

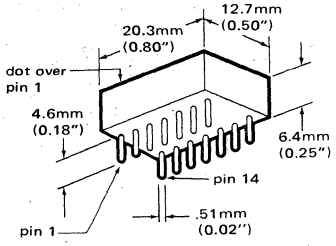
MODEL	4341
TRANSFER FUNCTION	$I_{out}(DC) = \frac{1}{T}\int_0^T E_{in}^2(t)\,dt$
INPUT	
Peak Operating Voltage	±10V
Absolute Maximum Voltage	±Supply
Impedance	5kΩ
OUTPUT	
Voltage	0 to +10V
Current	+5mA, min
Resistance	1Ω, max
BANDWIDTH	
±1% of Theoretical Output	80kHz
-3dB	450kHz
CONVERSION ACCURACY[2]	
Input: 500mV, rms to 5.0V, rms Input: DC to 10kHz Sine Wave Input: 10mV, rms to 7V, rms Input: DC to 20kHz	±0.5% of Reading, max[1] ±2mV ±0.2% Reading
STABILITY	
Accuracy vs. Temperature	±0.1mV ±0.01% of Reading/°C
Accuracy vs. Supply Voltage	±0.1mV ±0.01% of Reading/% of Supply Voltage Change
TEMPERATURE RANGE	
Operating	−25°C to +85°C
Storage	−40°C to +85°C
POWER REQUIREMENTS	
Rated Voltage	±15VDC
Voltage Range	±14VDC to ±16VDC
Quiescent Current	±12mA, typ., ±24mA, max

NOTES:
1. After standard trim procedure (see below).
2. Model 4341 will convert DC inputs. Lower frequency AC inputs require a large value of averaging capacitor to minimize ripple at output. (see Figure 2).
3. After expanded trim procedure, see page 4.

Row Spacing: 7.6mm (0.30")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-Pin DIP 0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

MECHANICAL



Row Spacing: 7.6mm (0.30")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-Pin DIP
0145MC Price: $3.90 ea.

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

STANDARD TRIM PROCEDURE

If the 4341 is used to measure sine waves or distorted sine waves, only two trims are needed to achieve an accuracy of ±0.5% of reading from 500mV, rms to 5V, rms up to 10kHz. Refer to Figure 1.

1. Set E_{in} = 5.000V, rms ±0.02% and adjust R1 such that E_o = 5.000VDC ±2mV.
2. Set E_{in} = 500mV, rms ±0.02% and adjust R2 such that E_o = 500mVDC ±0.2mV.
3. Repeat Step 1.

CHOOSING THE AVERAGING CAPACITOR

A single-pole low-pass RC filter provides the averaging function. The time constant is 1/2 RC where R is 10kΩ when the 4341 is adjusted for unity gain. To select the best value of C, make a tradeoff between output ripple and response time. Figure 2 shows the ripple magnitude vs. frequency for several typical values of capacitor. Response time vs. capacitor value is shown in Figure 3. (Note that rise times and fall times are different for the same value of capacitor).

While the ripple magnitude for signals other than sine waves can be analytically determined, it is tedious. The fastest method of choosing C is to apply a representative input signal and observe the output for various value of C. C can be 100's of microfarads, but should have a leakage current less than 0.1μA to minimize gain errors. With very large values of C, the input signals with frequencies approaching DC level could be averaged. Since the output is always a positive voltage, C can be polar capacitor.

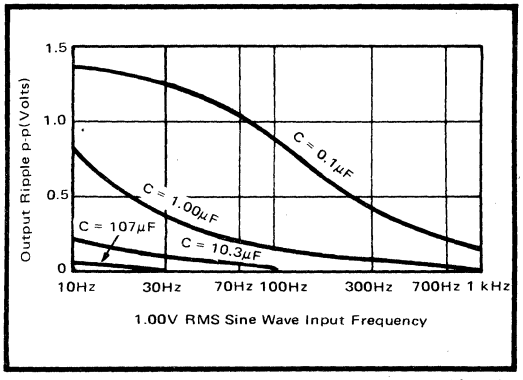


FIGURE 2. Output Ripple Magnitude vs. Input Signal Frequency.

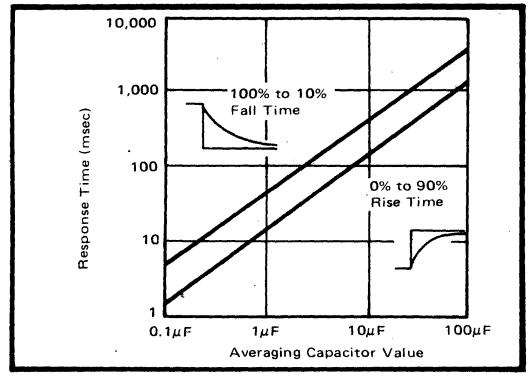


FIGURE 3. Response Time vs. Value of Averaging Capacitor.

EXPANDED TRIM PROCEDURE FOR GREATER ACCURACY

If the 4341 is used in applications to measure complex waveforms, the following expanded trim procedure is recommended. (Refer to Figure 4).

First set all potentiometers at mid turn position.

1. DC Reversal Error - Apply +10.000V ±1mV and -10.000V ±1mV to E_{in} alternatively, adjust R5 such that E_o readings are the same ±2mV.
2. Gain Adjustment - Apply E_{in} = +10.000VDC ±1mV, adjust R1 such that E_o = +10.000VDC ±1mV.
3. Input Offset - Apply +10.0mV ±0.1mV and -10.0mV ±0.1mV to E_{in}, adjust R4 such that E_o readings are the same ±0.1mV.
4. Offset - Ground E_{in}, adjust R3 such that E_o = 0 ±0.1mV. Repeat Step (3).
5. Low Level Accuracy - Apply E_{in} = +10.0mV ±0.1mV, adjust R2 such that E_o = +10.0mV ±0.1mV.

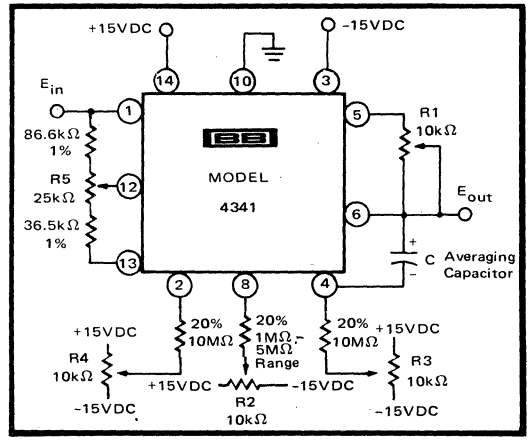


FIGURE 4. Expanded Trim Procedure (High Accuracy Applications).

NONUNITY GAINS

Gain values greater than unity can be achieved by inserting resistor R_x between pin 5 and pin 6. $R_x \simeq (A^2 - 1) \times 10k + 2k$ where A is the desired value of gain ($1 < A \leq 10$). (R_x is in ohms).

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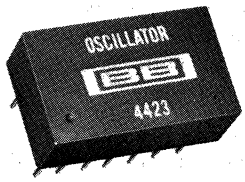

4423

PRECISION QUADRATURE OSCILLATOR

FEATURES

- SINE AND COSINE OUTPUTS
- RESISTOR-PROGRAMMABLE FREQUENCY
- WIDE FREQUENCY RANGE: 0.002Hz to 20kHz
- LOW DISTORTION: 0.2% max up to 5kHz
- EASY ADJUSTMENTS
- SMALL SIZE
- LOW COST

DESCRIPTION

The Model 4423 is a precision quadrature oscillator. It has two outputs 90 degrees out of phase with each other, thus providing sine and cosine wave outputs available at the same time. The 4423 is resistor programmable and is easy to use. It has low distortion (0.2% max up to 5kHz) and excellent frequency and amplitude stability.

The Model 4423 also includes an uncommitted operational amplifier which may be used as a buffer, a level shifter, or as an independent operational amplifier. The 4423 is packaged in a versatile, small, low-cost DIP package.

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SPECIFICATIONS

Prices and Specifications subject to change without notice

Specifications typical at 25°C and ±15VDC Power Supply Unless Otherwise Noted.

ELECTRICAL

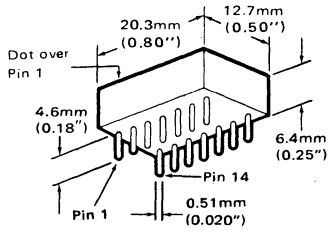
	MIN	TYP	MAX	UNITS
FREQUENCY				
Initial Frequency (no adjustments)	20.0k	20.5	21.0k	Hz
Frequency Range (using 2 R's only)	2k		20k	Hz
Frequency Range (using 2 R's and 2 C's)	.0.002		20k	Hz
Accuracy of Frequency Equation*		±1	±5	%
Stability vs Temperature		±50	±100	ppm/°C
Quadrature Phase Error		±0.1		degree
DISTORTION				
Sine Output (pin 1)				
0.002Hz to 5kHz			0.2	%
5kHz to 20kHz			0.5	%
Cosine Output (pin 7)				
0.002Hz to 5kHz		0.2		%
5kHz to 20kHz		0.8		%
Distortion vs Temperature		0.015		%/°C
OUTPUT				
Amplitude (Sine)				
At 20 kHz	6.5	7	7.5	V rms
vs Temperature		0.05		%/°C
vs Supply		0.4		V/V
Output Current	1.5	5		mA
Output impedance			1	Ω
UNCOMMITTED OP AMP				
Input Offset Voltage		1.5		mV
Input Bias Current		275		nA
Input Impedance		1		MΩ
Open Loop Gain		90		dB
Output Current	5			mA
POWER SUPPLY				
Rated Supply Voltage		±15		VDC
Supply Voltage Range	±12		±18	VDC
Quiescent Current		±9	±18	mA
TEMPERATURE RANGE				
Specifications	0		+70	°C
Operation	-25		+85	°C
Storage	-55		+125	°C

* May be trimmed for better accuracy.

PIN CONNECTIONS

1. E_1, Sine Output
2. Frequency Adjustment
3. Frequency Adjustment
4. +In, Uncommitted Op Amp
5. -In, Uncommitted Op Amp
6. Output, Uncommitted Op Amp
7. E_2, Cosine Output
8. Frequency Adjustment
9. $-V_{CC}$, -15VDC
10. $+V_{CC}$, +15VDC
11. Common
12. Frequency Adjustment
13. Frequency Adjustment
14. Frequency Adjustment

MECHANICAL



ROW SPACING - 7.6 (0.300")
WEIGHT - 3.4 gms (0.12 oz)
CONNECTOR - 14 pin DIP connector

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

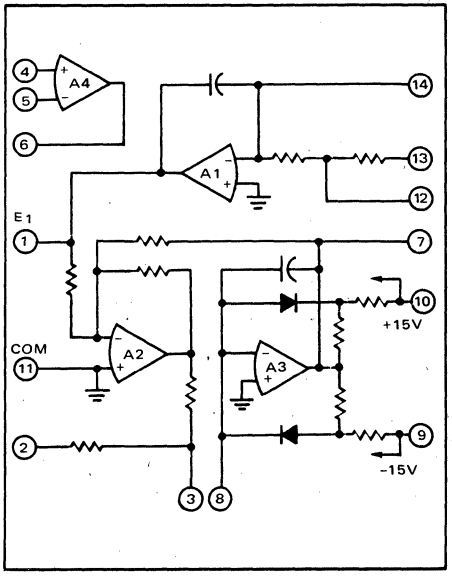


FIGURE 1. Equivalent Circuit.

TYPICAL PERFORMANCE CURVES

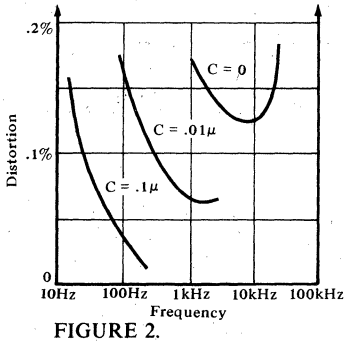


FIGURE 2.

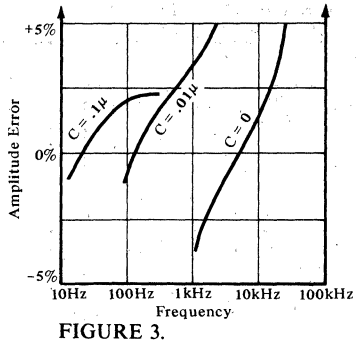


FIGURE 3.

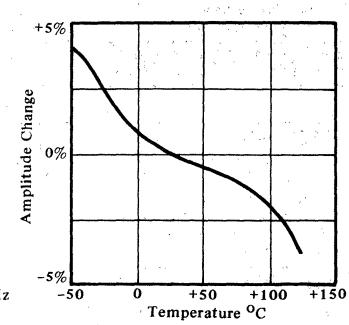


FIGURE 4.

EXTERNAL CONNECTIONS

1. 20 kHz Quadrature Oscillator

The 4423 does not require any external component to obtain a 20 kHz quadrature oscillator. The connection diagram is as shown in Figure 5.

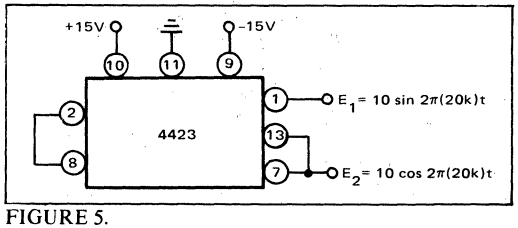


FIGURE 5.

2. Resistor Programmable Quadrature Oscillator

For resistor programmable frequencies in the 2 kHz to 20 kHz frequency range, the connection diagram is shown in Figure 6. Note that only two resistors of equal value are required. The resistor R can be expressed by,

$$R = \frac{3.785f}{42.05 - 2f}$$, R in kΩ, f in kHz

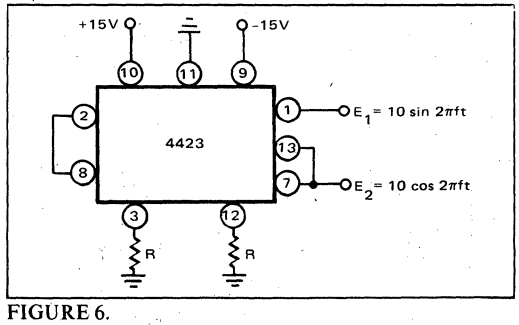


FIGURE 6.

3. Quadrature Oscillator Programmable to 0.002 Hz

For oscillator frequencies below 2000 Hz, use of two capacitors of equal value and two resistors of equal value as shown in Figure 7 is recommended. Connections shown in Figure 7 can be used to get oscillator frequency in the 0.002 Hz to 20 kHz range.

The frequency f can be expressed by:

$$f = \frac{42.05\ R}{(C + 0.001)\ (3.785 + 2R)}$$

where, f is in Hz
C is in μF
and R is in kΩ

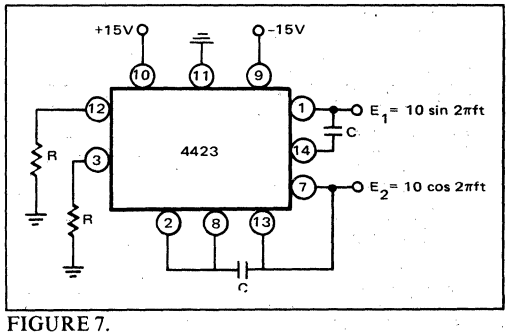


FIGURE 7.

For best results, the capacitor values shown in Table I should be selected with respect to their frequency ranges.

f	20 kHz to 2 kHz	2 kHz to 200 Hz	200 Hz to 20 Hz
C	0	0.01μF	0.1μF
20 Hz to 2 Hz	2 Hz to 0.2 Hz	0.2 Hz to 0.02 Hz	0.02 Hz to 0.002 Hz
1μF	10μF	100μF	1000μF

TABLE I.

After selecting the capacitor for a particular frequency the value of the required resistor can be obtained by using the resistor selection curve shown in Figure 8 or by the expression:

$$R = \frac{3.785f\ (C + 0.001)}{42.05 - 2f\ (C + 0.001)}$$

where,
R is in kΩ
f is in Hz
and C is in μF

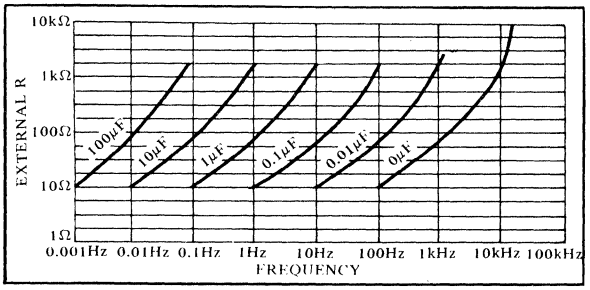


FIGURE 8.

The curves shown in Figure 8 are provided only as a nomographic design aid. The selection of capacitor values is not limited to the values shown in Figure 8. Any suitable combination of R and C values which satisfies the expression relating R, F and C as shown above, would work satisfactorily with the 4423.

NOTES ON TYPES OF CAPACITORS TO USE:

There are various kinds of capacitors available for use. There are polarized, also known as DC capacitors and non-polarized, also known as AC capacitors available. Of these two types, the polarized capacitors cannot be used with 4423 to set the frequencies.

Commonly available non-polarized capacitors include NPO ceramic, silver mica, teflon, polystyrene, polycarbonate, mylar, ceramic disc etc. A comparison is shown in Table II.

	Capacitance Range (μF)	Temperature Coefficients ppm/°C	Dissipation Factor (%)
NPO Ceramic	5pF - 0.1 μF	30	0.05
Silver Mica	5pF - 0.047 μF	60	0.05
Teflon	0.001 - 100 μF	200	0.01
Polystyrene	0.001 - 500 μF	100	0.03
Polycarbonate	0.001 - 1000 μF	90	0.08
Metalized Teflon	0.001 - 100 μF	60	0.1
Metalized Polycarbonate	0.001 - 1000 μF	10	0.4
Mylar	0.001 - 1000 μF	700	0.7
Metalized Mylar	0.001 - 2000 μF	700	1
Ceramic Disc	5pF - 0.5 μF	10,000	3

TABLE II.

For use with the 4423 oscillator, the choice of capacitors depends mainly on the user's application, error budget and cost budget. Note that the specifications of 4423 do not include the error contribution of the external components. The errors sourced by external components normally have to be added to the 4423 specifications.

As a general selection criteria we recommend the use of the above table. Start from the top of the list in the above table. If the capacitor is found unsuitable due to it being too large in size, too expensive, or is not easily available, then move down in the list for the next best selection. In any case do not choose or use any capacitors with dissipation factors greater than 1%. Such a capacitor would stop 4423 oscillation.

DISSIPATION FACTOR (DF)

A capacitor can be modeled by an ideal capacitor in parallel with an internal resistor whose value depends on its dissipation factor (DF). Mathematically, the internal resistor R is given by,

$$R = \frac{1}{2\pi f\, C(DF)}$$

where R is in Ω, f is the Hz, and C is in farads.

For example, the DF of ceramic disc capacitors is of the order of 3%, which for a 0.01 μF capacitor would look like having an internal resistor of 530kΩ at 1 kHz. The 530 kΩ value resistor is small enough to stop the 4423 oscillator from oscillating.

Some capacitor manufacturers use the terms "Power Factor" (PF) or "Q Factor" (Q) instead of the term "Dissipation Factor". These terms are similar in meaning and are mathematically related by,

$$(PF) = \frac{(DF)}{\sqrt{1 + (DF)^2}} \quad ; \quad Q = \frac{1}{(DF)}$$

OSCILLATION AMPLITUDE

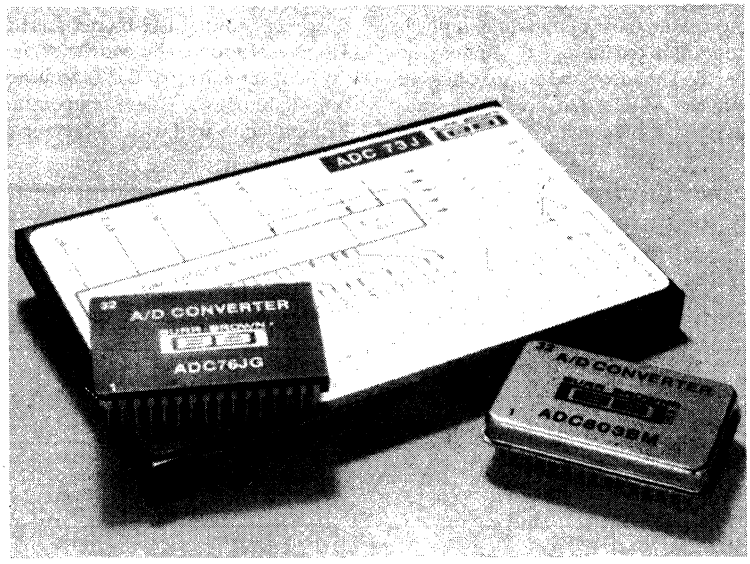
It takes a finite time to build up the amplitude of the oscillation to its final full scale value. There is a relationship between the amplitude build-up time and the frequency. The lower the frequency, the longer the amplitude build-up time. For example, typically it takes 250 seconds at 1 Hz, 30 seconds at 10 Hz, 4 seconds at 100 Hz, 400 milliseconds at 1 kHz, and 40 milliseconds at 10 kHz oscillator frequencies.

There are two methods available to shorten this normal amplitude build-up time. But there is also a relationship between the amplitude build-up time and distortion at final amplitude value. When the amplitude build-up time is shortened, the distortion can get worse.

One method to shorten the amplitude build-up time is to connect a resistor between pin 3 and pin 14. The lower this resistor is the shorter will be the time to build up amplitude of the oscillation, and worse will be the distortion of the output waveform. For example, a 100kΩ resistor would shorten the amplitude build up time from 15 seconds to 1 second at 20 Hz frequency, but the distortion could be degraded from tpically 0.05% to 0.5%.

The other method is to momentarily insert a 1kΩ resistor via a reset switch betwen pin 3 and pin 14. The amplitude of oscillation is built up instantaneously when the reset switch is pushed. There will be no degradation of distortion with this method since the 1kΩ resistor does not remain in the circuit continuously.

ANALOG-TO-DIGITAL CONVERTERS



The Burr-Brown analog-to-digital converter product line has a broad range of devices that enable the user to select the performance and price range ideally suited for the application. The high-performance 12-bit ADC80, which converts to 12-bit accuracy in 25μsec, was originated by Burr-Brown in 1975 and has become an industry standard. The recently introduced ADC803 is a 12-bit, 1.5μsec conversion time A/D converter that multiplies your system's throughput capabilities at the best price/performance ratio available. A high-resolution converter, the ADC76, converts 16 bits to $\pm$0.003% absolute accuracy in only 15μsec and is packaged in a 32-pin triple-wide dual-in-line package. Other performance categories are high-temperature (up to +200°C), and total harmonic distortion for digital recording of audio.

All devices are totally complete and fully specified, and have a track record of high reliability proven both in the field as well as in internal qualification testing.

SELECTION GUIDE

ANALOG-TO-DIGITAL CONVERTERS

These designs will meet your most demanding applications. We employ monolithic technology to support the high performance offered. The successive-approximation design approach produces ADC's that give 12-bit conversion in as low as 1.5μsec, 8-bit conversion in less than 3μsec, and low cost 12-bit designs that convert in 25μsec. High resolution 16-bit converters in small DIL packages give conversions to 0.003% accuracy in 15μsec at a very reasonable price. Harsh temperature environments can be handled as well with 12-bit converters that operate to +200°C.

ANALOG-TO-DIGITAL CONVERTERS									
Description	Model[1]	Resolution (Bits)	Linearity Error max (% of FSR)	Conversion Time, max (μsec)	Accy. Drift Bipolar, max (ppm FSR/°C)	Input Range (V)	Temp Range[2]	Package	Page
Low Cost	ADC80AG-10[3] ADC80AG-12[3]	10 12	±0.048 ±0.012	21 25	±23 ±23	±2.5, ±5, ±10, +5, +10	Ind Ind	Ceramic 32-pin DIP	5-54 5-54
Low Cost, High Speed	ADC82AG-10 ADC82AM, (Q)	8 8	±0.2 ±0.2	2.8 2.8	±60 ±60	±2.5, ±5, ±10, +5, +10, +20	Ind Ind	24-pin DIP	5-62 5-62
	ADC84KG-10 ADC84KG-12	10 12	±0.048 ±0.012	6 10	±21 ±21	±2.5, ±5, ±10, +5, +10	Com Com	32-pin DIP	5-70 5-70
Low Drift, High Speed	AD85C-10 ADC85-10 ADC85C-12, (Q) ADC85-12, (Q)	10 10 12 12	±0.048 ±0.048 ±0.012 ±0.012	6 6 10 10	±26 ±16 ±19 ±13	±2.5, ±5, ±10, +5, +10	Com Ind Com Ind	Metal Hermetic 32-pin DIP	5-70 5-70 5-70 5-70
Very High Speed	ADC803BM ADC803CM	12 12	±0.020 ±0.015	1.5 1.5	±23 ±23	±5, ±10, −10 ±5, ±10, −10	Ind Ind	Metal Hermetic 32-pin DIP	5-86 5-86
High Resolution, High Accuracy	ADC73J ADC73K ADC731J ADC731K	16 16 16 16	±0.0015 ±0.00075 ±0.0015 ±0.00075	170 170 170 170	±9 ±9 ±9 ±9	±5, ±10, +10, +20	Com Com Com Com	Module Module Module Module	5-35 5-35 5-35 5-35
High Resolution	ADC71JG ADC71KG	16 16	±0.006 ±0.003	50 50	±15 ±15	±2.5, ±5, ±10, 0 to +5, 0 to +10, 0 to +20	Com Com	Ceramic 32-pin DIP	5-19 5-19
	ADC72AM ADC72BM ADC72JM ADC72KM	16 16 16 16	±0.006 ±0.003 ±0.006 ±0.003	50 50 50 50	±12 ±12 ±17 ±17	±2.5, ±5, ±10, 0 to +5, 0 to +10, 0 to +20	Ind Ind Com Com	Metal Hermetic 32-pin DIP	5-27 5-27 5-27 5-27
	ADC76JG ADC76KG	16 16	±0.006 ±0.003	15 15	±15 ±15	±2.5, ±5, ±10, 0 to +5, 0 to +10, 0 to +20	Com Com	Ceramic 32-pin DIP	5-46 5-46
Very-Wide Temp Range	ADC10HT ADC10HT-1	12 12	±0.012 ±0.048	50 50	±34 ±63	±5, ±10 ±5, ±10	−55°C to +200°C	Ceramic 28-pin DIP	5-3 5-3
High Speed	ADC60-08 ADC60-10 ADC60-12	8 10 12	±0.195 ±0.0488 ±0.0244	0.88 1.88 3.50	±20 ±20 ±15	±2.5, ±5 ±10, +5 +10, +20	Com Com Com	Module Module Module	5-13 5-13 5-13
Military	ADC87/MIL Series				See Military Products				
High Resolution	ADC100-SMD	4 digit + sign	±0.005	30msec	±5	±10	Com	Module	5-78

NOTES: (1) "Q" indicates product also available with screening for increased reliability. See Q Program. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) "Z" models operate from ±12VDC supply.

PCM ANALOG-TO-DIGITAL CONVERTERS FOR AUDIO								
Description	Model	Resolution (Bits)	Total Harmonic Distortion (max)	Conversion Time (max)	Input Range (V)	Temp Range[1]	Dynamic Range	Page
PCM-Audio A/D Converter[3]	PCM75KG PCM75JG	16 14[4]	0.02% at −15dB 0.05% at −15dB	17μsec[2] 15μsec[2]	±2.5, ±5, ±10 ±2.5, ±5, ±10	Com Com	90dB 90dB	5-98 5-98

NOTES: (1) Com = 0 to +70°C. (2) Can be reduced to 8μsec. (3) Internal 16-bit DAC available to user. (4) Can be operated at 16 bits.

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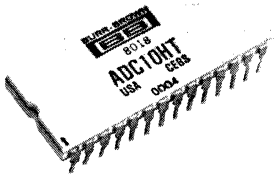


ADC10HT

Wide Temperature Range General Purpose 12-Bit ANALOG-TO-DIGITAL CONVERTER

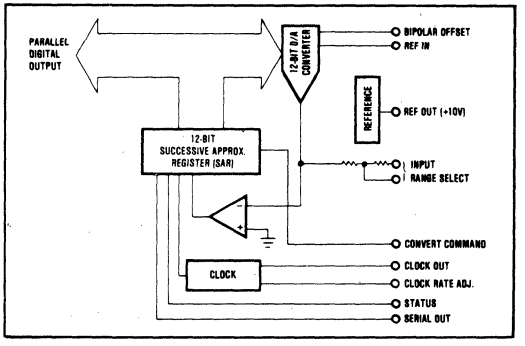
FEATURES

- -55°C to +200°C SPECIFICATIONS
- FULL 12-BIT RESOLUTION
- 50μsec MAX CONVERSION TIME
- NO MISSING CODES OVER FULL TEMPERATURE RANGE
- COMPLETE WITH INTERNAL CLOCK AND REFERENCE VOLTAGE
- SERIAL OUTPUT DATA AVAILABLE
- TTL AND +5V CMOS COMPATIBLE
- DUAL-WIDTH HERMETIC CERAMIC PACKAGE
- LOW POWER OPERATION WITH EXTERNAL REFERENCE (250mW)

DESCRIPTION

You'll find this general purpose, 12-bit, successive approximation A/D converter ideally qualified for circuits that must operate over wide temperature ranges. The ADC10HT incorporates state-of-the-art IC and laser-trimmed thin-film components. It is complete with an internal clock and reference voltage. Internal scaling resistors allow bipolar input voltage ranges of ±5V and ±10V. A pin is provided for serial output data. The ADC10HT is contained in a compact, dual width, 28-pin ceramic DIL package.

To assure consistent performance, 100% screening procedures are conducted on the ADC10HT at key points during its manufacture. Burn-in and temperature cycling are examples. A clean-room environment is maintained for assembly operations.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at rated power supply voltages and T_A = +25°C unless otherwise noted.

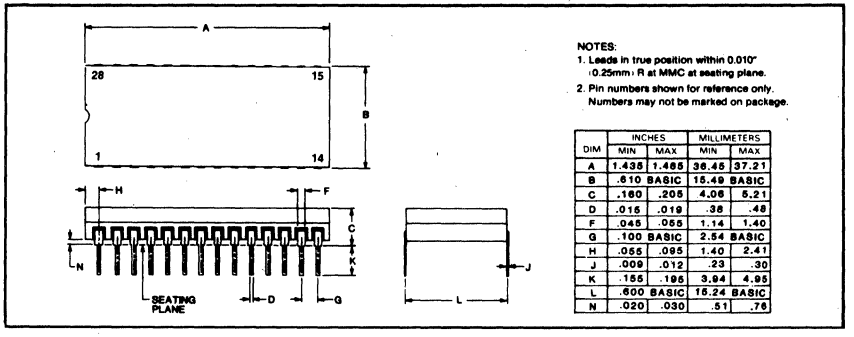
MODEL	ADC10HT			ADC10HT-1			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION	12			12			Bits
INPUT							
ANALOG							
Voltage Ranges							
Unipolar		0 to +10, 0 to +20			0 to +10, 0 to +20		V
Bipolar		±5, ±10			±5, ±10,		V
Impedance (direct input)							
0 to +10V, ±5V		2			2		kΩ
0 to +20V, ±10V		4			4		kΩ
DIGITAL(1)							
Convert Command Logic Loading		1			1		CMOS Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(2)		±0.05	±0.2		±0.05	±0.2	%
Offset Error(2)							
Unipolar		±0.05	±0.2		±0.05	±0.2	% of FSR(3)
Bipolar		±0.05	±0.2		±0.05	±0.2	% of FSR
Linearity Error			±0.012			±0.048	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.012	±0.024		±0.048	±0.096	% of FSR
Total Unadjusted Error(4)							
+25°C		±0.10	±0.40		±0.15	±0.40	% of FSR
-55°C to +200°C		±0.30	±1.00		±0.80	±1.50	% of FSR
Total Adjusted Error(5)							
+25°C		±0.006	±0.012		±0.024	±0.048	% of FSR
-55°C to +200°C		±0.20	±0.60		±0.50	±1.10	% of FSR
Total Unadjusted Error(6)							
Exclusive of Reference							
+25°C		±0.10	±0.40		±0.15	±0.45	% of FSR
-55°C to +200°C		±0.20	±0.80		±0.50	±1.10	% of FSR
Total Adjusted Error(7)							
Exclusive of Reference							
+25°C		±0.006	±0.012		±0.024	±0.048	% of FSR
-55°C to +200°C		±0.15	±0.40		±0.40	±0.75	% of FSR
CONVERSION TIME		30	50		30	50	μsec
DRIFT (-55°C ≤ T_A ≤ +200°C)							
Gain							
With Internal Reference		±15	±35		±25	±100	ppm/°C
Exclusive of Reference		±5	±10		±10	±20	ppm/°C
Offset							
Unipolar		±1	±2		±2	±10	ppm of FSR/°C
Bipolar							
With Internal Reference		±10	±35		±25	±100	ppm of FSR/°C
Exclusive of Reference		±4	±10		±8	±20	ppm of FSR/°C
Linearity		±0.5	±1		±1	±3	ppm of FSR/°C
No Missing Codes (Temp. Range							
-55°C to +200°C	12			10			Bits
OUTPUT							
DIGITAL DATA							
Parallel							
Output Codes(8)							
Unipolar		SB			SB		
Bipolar(9)		OB, TC			OB, TC		
Output Drive	1			1			LSTTL Loads
Serial Data Code (NRZ) - SB, OB		SB, OB			SB, OB		
Output Drive	1			1			LSTTL Loads
Status		Logic "1" During Conversion			Logic "1" During Conversion		
Status Output Drive	1			1			LSTTL Loads
Internal Clock							
Output Drive	1			1			LSTTL Loads
Frequency		400			400		kHz

SPECIFICATIONS

MODEL	ADC10HT			ADC10HT-1			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLIES AND REFERENCE							
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain, +15VDC(10)		+15			+15		mA
-15VDC(10)		-30			-30		mA
+5VDC		+16			+16		mA
Power Supply Sensitivity							
±15VDC		0.01			0.01		% of FSR/%Vs
+5VDC		0.01			0.01		% of FSR/%Vs
Internal Reference Voltage	9.990	10.0	10.010	9.990	10.0	10.010	V
Max External Current with							
no Degradation of Specs		2			2		mA
Temperature Coefficient		±10			±10		ppm/°C
TEMPERATURE RANGE							
Specification	-55		+200	-55		+200	°C
Operating	-55		+200	-55		+200	°C
Storage	-65		+210	-65		+210	°C

NOTES:
1. +5V CMOS compatible. Input current (low to high state) = 1μA max. Use pull-up resistor when driving convert command from TTL.
2. Adjustable to zero (see Table II and Figures 5 and 6).
3. FSR means Full Scale Range. For example, unit connected for ±10V has a 20V FSR.
4. Includes Gain, Offset, and Linearity Errors (Bipolar Mode).
5. Gain and Offset Errors removed at +25°C (Bipolar Mode).
6. Includes Gain, Offset, and Linearity Errors with external +10.0V ±1mV reference, does not include Reference Drift (Bipolar Mode).
7. Gain and Offset Errors removed at +25°C with external +10.0V ±1mV reference, does not include Reference Drift (Bipolar Mode).
8. See Table I. SB - Straight Binary, OB - Offset Binary, TC - Two's Complement.
9. TC coding obtained by using $\overline{MSB}$ (pin 13) instead of MSB (pin 12).
10. May be reduced. See Low Power Operation, pages 5-11 and 5-12.

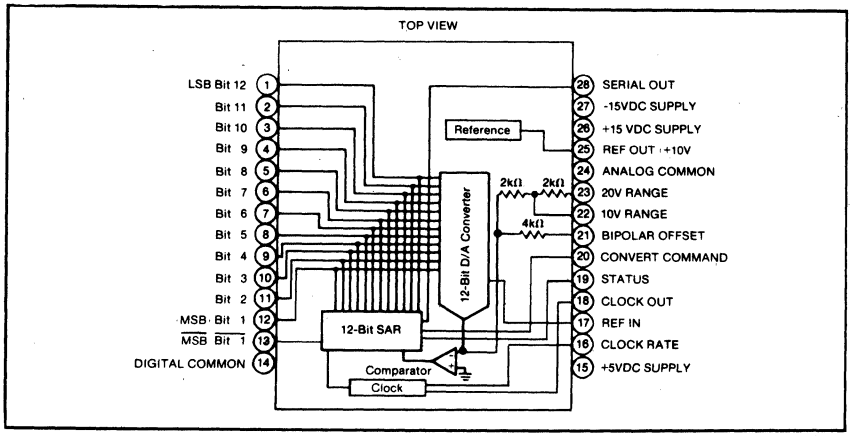
MECHANICAL



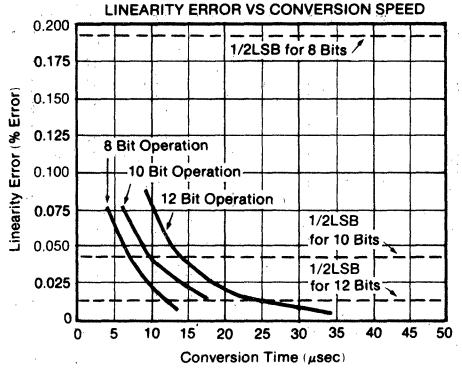
NOTES:
1. Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
2. Pin numbers shown for reference only. Numbers may not be marked on package.

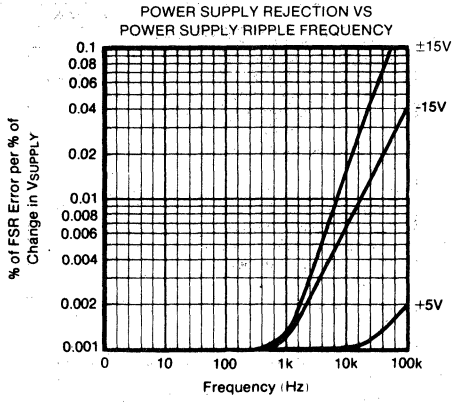
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.438	1.468	36.48	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	.38	.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	.23	.30
K	.155	.195	3.94	4.95
L	.600 BASIC		15.24 BASIC	
N	.020	.030	.51	.76

CONNECTION DIAGRAM



TYPICAL PERFORMANCE CURVES





DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over range of the A/D converter is 1LSB, ±1/2LSB.

The ADC10HT is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also specifies that this converter will have no missing codes over the full operating temperature range.

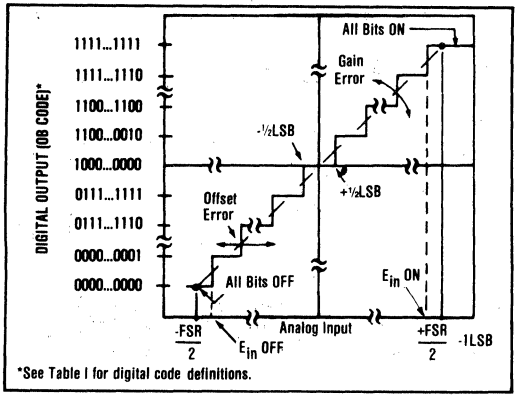


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 0110 0111 0110 exists.

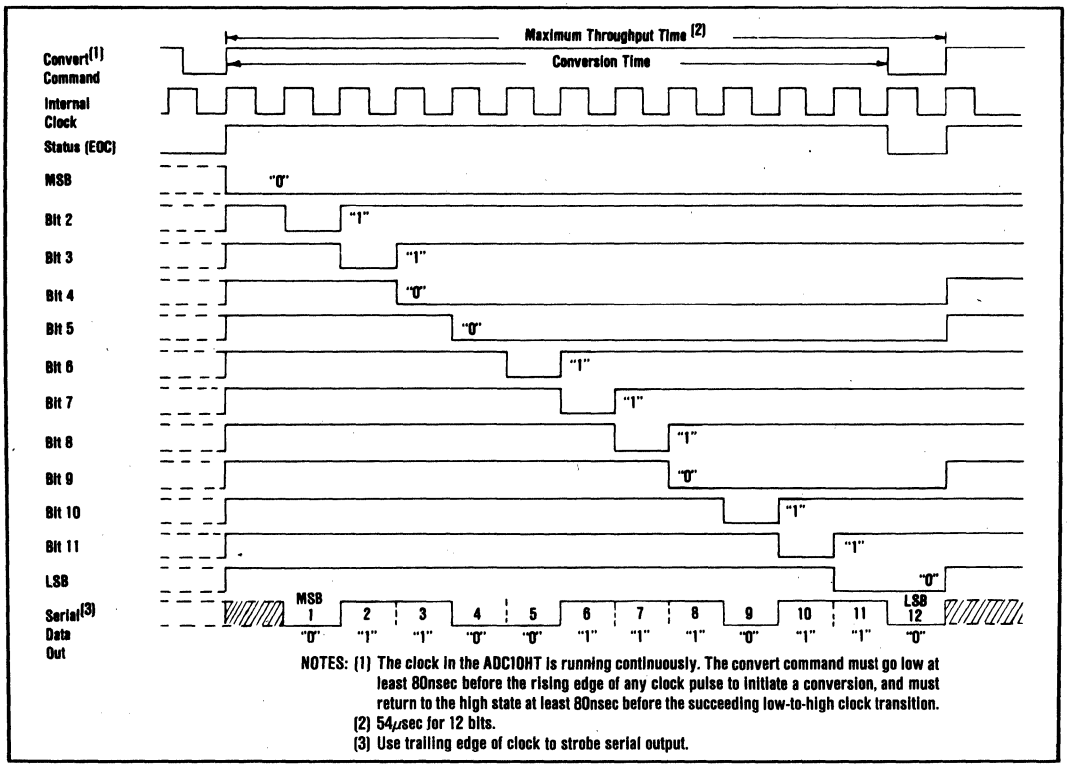


FIGURE 2. ADC10HT Timing Diagram.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Two binary codes are available on the ADC10HT parallel output; they are straight binary (SB) for unipolar input signal ranges and offset binary (OB) for bipolar input signal ranges. Two's complement (TC) may be obtained by using $\overline{\text{MSB}}$ (pin 13).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 8-, 10- and 12-bit resolutions. Figure 3 shows the connections for 12-bit resolution, parallel data output, with ±10V input.

SERIAL DATA

Two straight binary codes are available on the serial output line; they are SB and OB. The serial data is available only during conversion and appears with the MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the TC code.

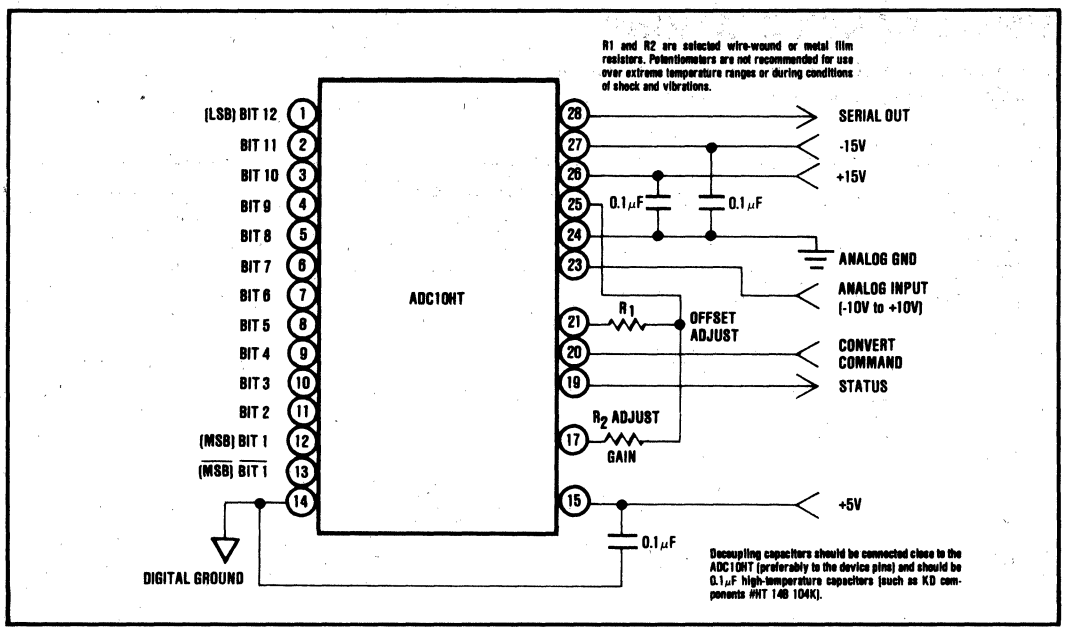


FIGURE 3. ADC10HT Connections for ±10V Analog Input, 12-Bit Resolution, and Serial or Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined As:	±10V	±5V	0 to +10V	0 to +20V
Code Designation		OB(1) or TC(2)	OB(1) or TC(2)	SB(3)	SB(3)
One Least Significant Bit (LSB)	FSR/2^n	20V/2^n	10V/2^n	10V/2^n	20V/2^n
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n = 10	19.53mV	9.77mV	9.77mV	19.53mV
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
Transition Values					
MSB LSB					
111...111(4)	+Full Scale	+10V - 3/2LSB	+5V - 3/2LSB	+10V - 3/2LSB	+20V - 3/2LSB
100...000	Mid Scale	0	0	+5V	+10V
000...001	-Full Scale	-10V + 1/2LSB	-5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

NOTES:
(1)OB = Offset Binary
(2)TC = Two's Complement - obtained by inverting the most significant bit. $\overline{MSB}$ (pin 13)
(3)SB = Straight Binary
(4)Voltages given are the nominal value for transition to the code specified

DISCUSSION OF SPECIFICATIONS

The ADC10HT is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion-speed effects on accuracy. This ADC is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.05% of FSR at 25°C. These errors may be trimmed to zero as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC10HT power supply sensitivity is specified for ±0.01% of FSR / %V_S for ±15V supplies and ±0.01% of FSR / %V_S for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC10HT but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with high temperature mica or teflon capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC.

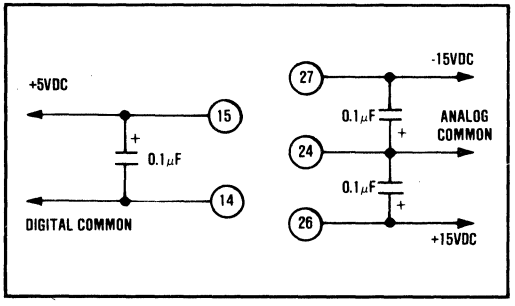


FIGURE 4. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

TABLE II. ADC10HT Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 21 To Pin	Connect Pin 23 To	Connect Input Signal To Pin
±10V	OB or TC*	25**	Input Sig.	23
±5V	OB or TC*	25**	Open	22
0 to +10V	SB	Open	Open	22
0 to +20V	SB	Open	Input Sig.	23

*Obtained by using $\overline{MSB}$ pin 13

** If optional offset adjustment is not used connect a 25Ω ±0.1% resistor from pin 21 to pin 25 to obtain specified gain and offset errors.

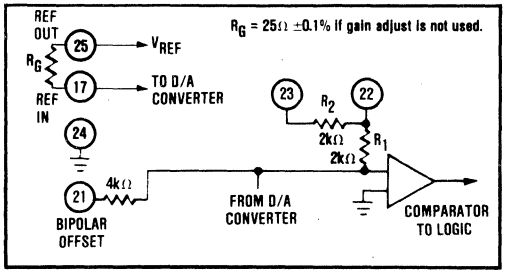


FIGURE 5. ADC10HT Input Scaling Circuit.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

A connection diagram for the ADC10HT in the ±10V input bipolar mode of operation is shown in Figure 3. The gain and offset adjustment resistors (R1 and R2) should be selected discrete metal-film or wirewound resistors and not potentiometers if optimum performance is required under high shock and vibration levels. The internal gain and offset errors are laser trimmed to within a maximum error of ±0.2% with 25Ω, 0.1% resistors in place of R1 and R2. Another possible approach in many applications is to simply remove the offset and gain errors with digital techniques after the A/D conversion has taken place. This approach can virtually eliminate the need for initial gain and offset adjustment and even the effects of gain and offset drift with time and temperature can often be removed. In some cases it may be desirable to use potentiometers.

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer or resistance substitution boxes as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits off E_{IN}^{OFF}.

Adjust the Offset potentiometer or resistor substitution boxes until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

GAIN - Connect the Gain adjust potentiometer or resistor substitution boxes as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

It is also possible to make the adjustments just described with potentiometers and then replace the resistive arms with discrete metal film or wire-wound resistors in order to make a system more rugged before subjecting it to harsh environments.

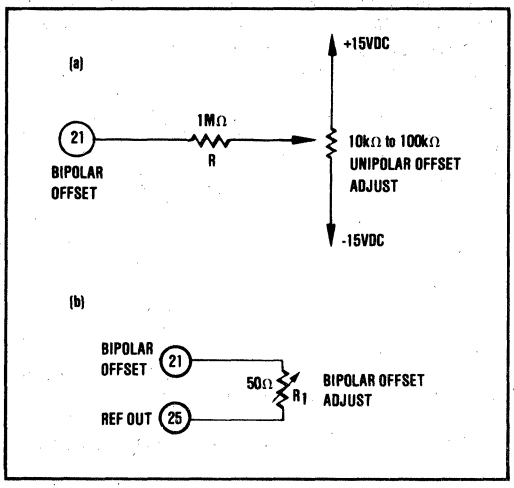


FIGURE 6. Optional Unipolar and Bipolar Offset Adjust Circuitry with ±0.4% of FSR Range of Adjustment.

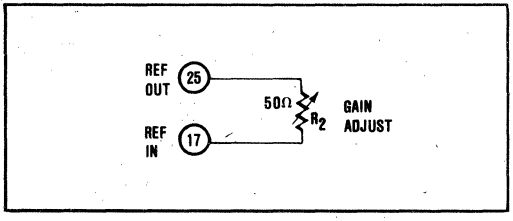


FIGURE 7. Optional Gain Adjust with ±0.4% Range of Adjustment.

CLOCK RATE CONTROL (OPTIONAL)

Faster Conversion

If adjustment of the clock rate is desired for faster conversion times, a resistor may be connected between Clock Rate (pin 16) and Clock Out (pin 18) as shown in Figure 8.

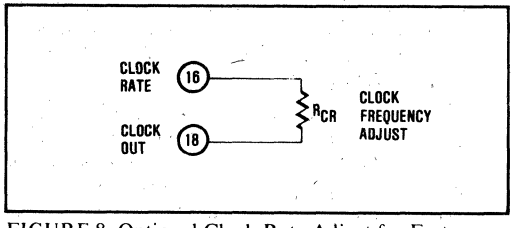


FIGURE 8. Optional Clock Rate Adjust for Faster Conversion Times.

Figure 9 shows the effect of clock rate control resistor (R_{CR}) on clock frequency. Figure 9 is based on a typical initial clock frequency of about 400kHz (conversion time of 30μsec for 12 bits). To determine the required clock frequency:

$$f_{clock} = \frac{\text{Bit Resolution}}{\text{Conversion Time}}$$

For example, if the ADC10HT is short cycled to 10-bit operation and a conversion time of 20μsec is required, then

$$f_{clock} = \frac{10}{20\mu sec} = 500kHz$$

from Figure 9 a clock rate resistor (R_{CR}) of about 40kΩ is required.

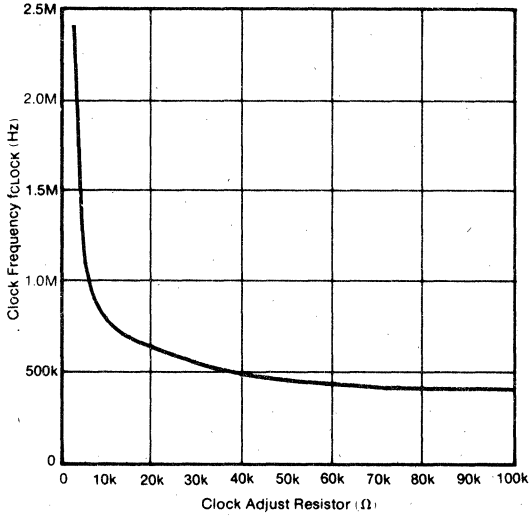


FIGURE 9. Clock Frequency vs Clock Rate Control Resistor (R_{CR}).

Slower Conversion

The conversion time can be decreased by connecting a capacitor from the Clock Rate pin to Digital Common (see Figure 10).

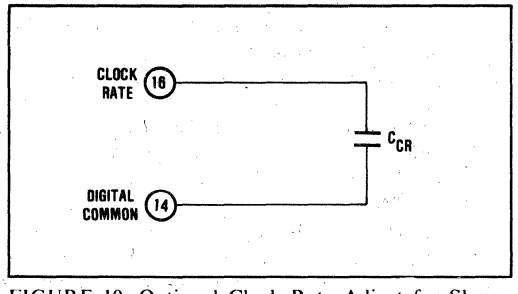


FIGURE 10. Optional Clock Rate Adjust for Slower Conversion Times.

Figure 11 shows the effect of the clock rate control capacitor on the clock frequency.

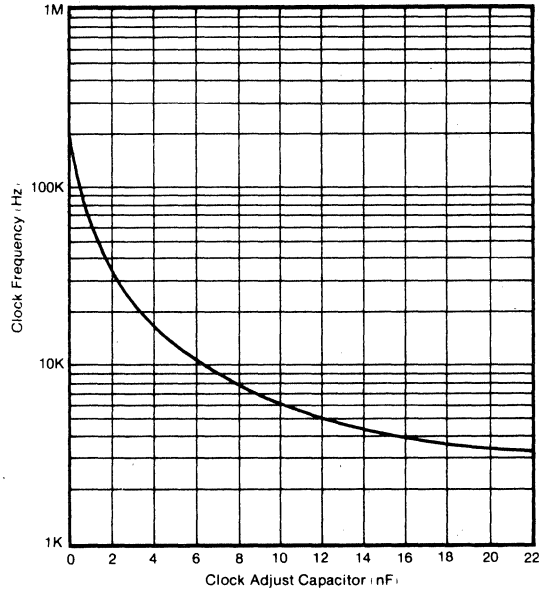


FIGURE 11. Clock Frequency vs. Clock Rate Control Capacitor (C_{CR}).

The serial output data (pin 28) is synchronous with the internal clock. In some applications the clock frequency must be lowered to 3kHz or 4kHz so that the data can be transmitted over long distances. If 12-bit resolution is required, the conversion time for 4kHz is

$$\text{conversion time} = \frac{12 \text{ bits}}{4\text{kHz}} = 3\text{msec}$$

From Figure 11, a clock rate control capacitor, C_{CR}, of approximately 16nF is required.

In applications requiring such a slow conversion time, a low-pass filter should be used at the analog input to the ADC10HT.

SHORT-CYCLE AND CONTINUOUS CONVERSION OPERATION.

The ADC10HT may be operated at faster speeds for resolutions less than 12 bits by using the clock rate control feature. The conversion time can be further increased by using the short cycle circuit shown in Figure 12. Without this circuit, the status signal (pin 19) will always remain high for 13 clock pulses even if only 8 bits are being used. By connecting the short cycle input of the NAND gate to the n + 1 bit (connect to bit 9 for 8-bit operation, for example) the conversion will be completed and the status signal will go low after n + 1 clock pulses (9 pulses for 8-bit operation). It should be noted that with the circuit shown in Figure 12, the ADC10HT will operate in a continuous conversion mode, i.e., a new conversion will start on the n + 2 clock pulse without the need for an external convert command.

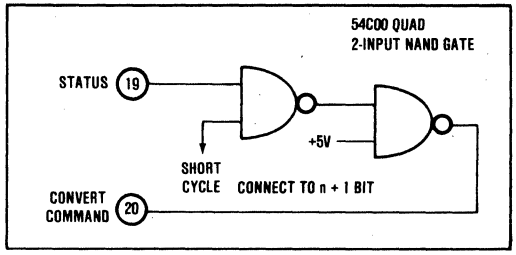


FIGURE 12. Short-Cycle Circuit which Provides for Lower Resolutions than 12 Bits with Faster Conversion Times and Continuous Conversions.

Table III indicates where to connect the short cycle input for 8-bit and 10-bit resolution and gives possible conversion time(s) obtainable by using this feature along with the clock rate pin.

TABLE III. Short Cycle Connections and Specifications for 8 to 12 Bit Resolutions.

Resolution (Bits)		12	10	8
Connect SHORT CYCLE to:		N/A	Pin 2	Pin 4
Conversion Time (μsec)(1)		24	10	6
Nonlinearity at +25°C (% of FSR)	ADC10HT	±0.012	±0.048	±0.1
	ADC10HT-1	±0.048	±0.048	±0.1

NOTE: (1) Adjust Conversion Time with Clock Rate Control resistor as shown in Figures 8 and 9.

For 12-bit operation and continuous conversion, simply connect status (pin 19) directly to convert command (pin 20).

OUTPUT DRIVE

Normally the ADC10HT logic outputs will drive two low power TTL loads or one LSTTL load. If long digital lines must be driven, external logic buffers are recommended. The digital outputs are connected directly to the internal CMOS successive-approximation-register and can drive +5V CMOS without the need for pull-up resistors.

HEAT DISSIPATION

The ADC10HT dissipastes approximately 750mW and the package has a case-to-case ambient thermal resistance (θ_{CA}) of 35°C W. For optimum performance at +200°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the package can be achieved by using a silicone heat-sink compound.

LOW POWER OPERATION

The typical supply currents required by the ADC10HT under normal operating conditions are 15mA (+15V), 30mA (-15V), and 16mA (+5V). The average power required (P_D) is therefore

$P_D = |15\text{mA} \times 15\text{V}| + |30\text{mA} \times -15\text{V}| + |16\text{mA} \times 5\text{V}| = 755\text{mW}$.

Under certain operating conditions this power consumption can be reduced to as little as 250mW.

The ADC10HT is completely self-contained with an internal +10V reference voltage. The +15V supply is used only to supply power for the op amp current source and zener diode used in this reference. If an external reference is available, the +15V supply is not required and it can be removed. This reduces the P_D by 15mA x 15V = 225mW. The average P_D for the ADC10HT is therefore reduced to 530mW.

The major contributor to the power consumption is the -15V supply. As long as a +10V reference is used, the V- supply voltage must be between -13V and -16V. If, however, a lower voltage reference is used, this V- supply voltage can be reduced considerably which greatly reduces the power consumption. Lowering the reference voltage will, of course, lower the full scale input voltage by a proportional amount. For example, if the reference voltage is +5V, the full scale input voltage for the 10V range input (pin 22) will be +5V, instead of +10V with a +10V reference, in the unipolar mode of operation. Table IV indicates the minimum supply voltages and the typical power consumption obtained when using these supply voltages for various values of V_{REF}.

TABLE IV. Minimum Power Supply Voltages and Typical Power Consumption for Operation with External V_{REF}. (Note: +15V is not required if internal V_{REF} is not used.)

External V_{REF}	+V_{LOGIC} (Pin 15)	-V_S (Pin 27) (Minimum)	Total Power Consumption (Typical)
+10V	+5V	-13V	470mW
+6.3V	+5V	-10V	300mW
+5V	+5V	-8V	250mW

LOW-POWER EXTERNAL REFERENCE

A simple external reference voltage can be made with a single resistor and a zener diode as shown in Figure 13. The power consumed by the reference is only about 75mW with $+V_S = +10V$. The power supply sensitivity of this reference is approximately ±0.02% of FSR/%V_S.

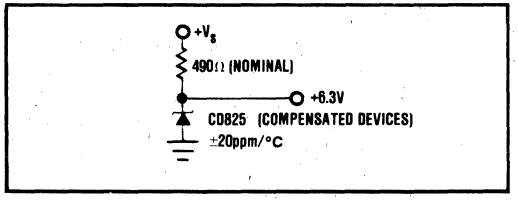


FIGURE 13. Simple +6.3V External Reference That Requires Only 75mW.

A very simple procedure can be used to obtain the lowest possible drift with this reference. First, vary the zener current from about 4mA to 11mA by changing either the bias voltage, +V_S, or bias resistor, R_B, and plot V_Z versus I_Z as shown in Figure 14. Next, heat the zener (the exact temperature is not important, but it should be near the desired operating temperature), and repeat the procedure. The point where the two curves cross is the zero-temperature-coefficient bias current. +V_S and/or R_B should then be adjusted accordingly for this optimum operating current.

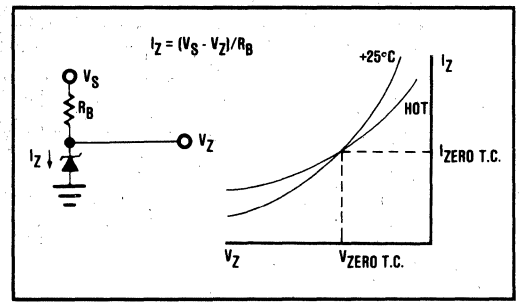


FIGURE 14. Simple Techniques for Obtaining a Low Drift Reference Voltage.

This procedure is also discussed in a Burr-Brown Application Note: "Squeeze High Performance out of Low-Cost Hybrid Data Converters, AN-86.

Other Application Notes

Burr-Brown also has other Application Notes of interest to the converter user. In particular:

"What Designers Should Know About Data Converter Drift," AN-89.

"Correcting Errors Digitally in Data Acquisition and Control," AN-101.

OPERATION WITH EXTERNAL CLOCK

Figure 15 shows the internal clock circuit of the ADC10HT. To operate with an external clock, first connect the Clock Rate Control (pin 16) to ground. This will shut off the internal clock and also turn off the open collector output transistor of the LM119 comparator. The Clock Out (pin 18) will then be in a "high" state (+5V) because of the 2kΩ pull-up resistor to +5V. Now simply use the Clock Out pin for the external clock input. Note that the external clock must have the capability of sinking 2.5mA when it is in the low state due to the 2kΩ pull-up resistor.

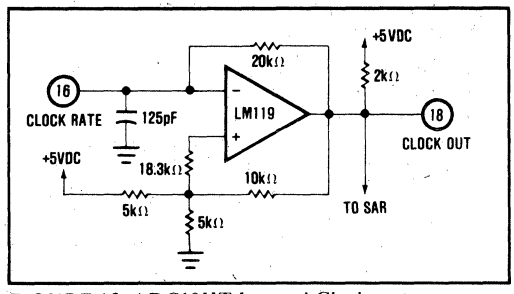


FIGURE 15. ADC10HT Internal Clock.

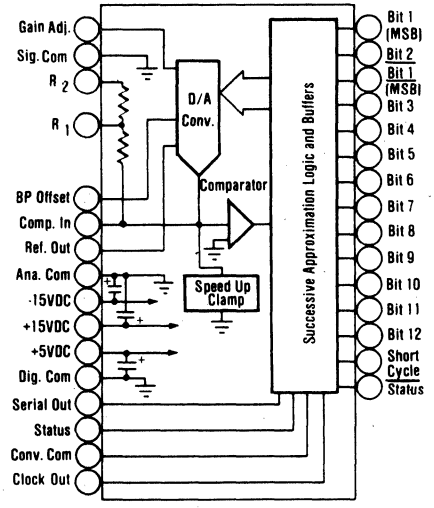
BURR-BROWN®

ADC60

High Speed ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **FAST CONVERSION SPEED:**
  12-bits - 3.5μsec, max
  10-bits - 1.88μsec, max
  8-bits - 0.88μsec, max
  Throughput sampling rates from 250kHz (12-bits) to 1MHz (8-bits) can be attained
- **PIN-PROGRAMMABLE UNIPOLAR OR BIPOLAR**
- **ANALOG SIGNALS**
- **SERIAL AND PARALLEL DATA OUTPUTS**
- **SELF-CONTAINED WITH INTERNAL CLOCK & REFERENCE**
  Simplifies system design and reduces cost
- **±1/2LSB LINEARITY**
  Provides accurate conversion
- **NO MISSING CODES**



DESCRIPTION

The Model ADC60 is a very high speed, successive approximation A/D converter than is designed for applications requiring system throughput sampling rates from 250kHz to 1MHz. The fast conversion speed is accomplished with proprietary fast settling circuits which preserve linearity and drift while permitting conversion speeds up to 100nsec/bit.

Available in 8-, 10-, and 12-bit resolutions the ADC60 contains an internal reference and clock. Internal components are provided for pin-programmable analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Digital data is available in both serial and parallel, binary form with corresponding timing signals. All digital input and output signals are DTL/TTL-compatible.

The ADC60 operates from ±15VDC and +5VDC power, and is housed in a 2" x 4" x 0.75" module with screened-on pin function identification.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

THEORY OF OPERATION

Upon receipt of an external Convert Command, the previous data sample is cleared from the output register. Each bit is then successively compared against the amplitude of the input signal, and is either held as a "0" or turned on as a "1" until all bits have been tried. The parallel data output is not available for transfer to external devices until the Status output changes from logic "1" to logic "0".

Serial data is only available during conversion, and must be transferred to external devices with the Clock and Status signals beginning with the first clock pulse following a change in Status from logic "0" to logic "1".

TIMING CONSIDERATIONS

Data is available in both serial and parallel form. Timing signals are available for the transfer of data to external devices. For parallel data transfer, Status and its compliment Status indicate when the conversion is complete. For serial data transfer, the Clock Out signal starts on the trailing edge of the Convert Command; and serial data is valid before the positive going edge of the Clock Out signal. The Clock ceases operation when the conversion is complete. There will be one more clock pulse than the number of bits converted (resolution). Figure 1 shows the timing details of the ADC60.

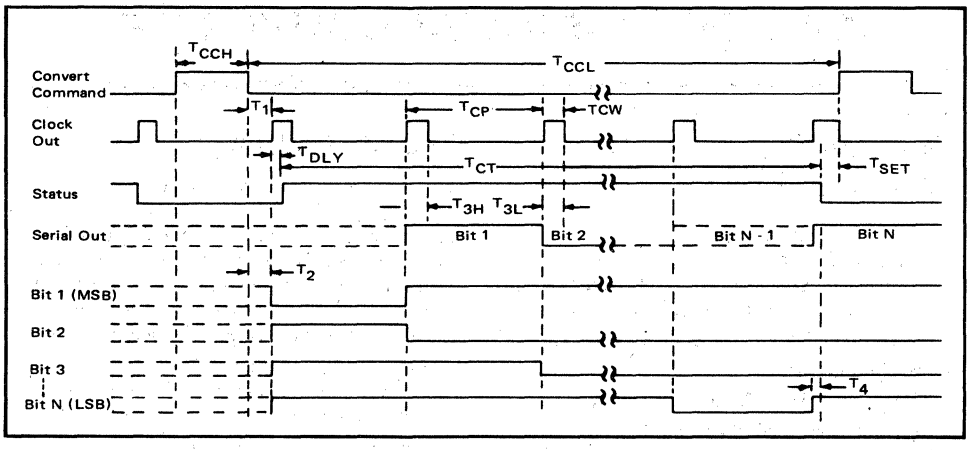


FIGURE 1. ADC60 Timing Diagram.

TABLE I. Switching Characteristics.

SYMBOL	PARAMETER DESCRIPTION	MIN.	TYP.	MAX.	UNITS
T_{CT}	Conversion Time - 12 Bit	2.50	3.45	3.50	μsec
	10 Bit	1.20	1.83	1.88	μsec
	8 Bit	0.80	0.84	0.88	μsec
T_{CCH}	Width of Convert Command Pulse	30	---	---	nsec
T_{CCL}	Internal Between Convert Command Pulses – $(T_{CT} + T_1 + T_{DLY})$		(1)		
T_1	Delay From Trailing Edge of Conv. Command To Leading Edge of Clock Out	30	41	60	nsec
T_2	Delay from Conv. Command To Reset	26	40	68	nsec
T_{3H}	Delay From Valid High Output To Trailing Edge of Clock Out	22	43	70	nsec
T_{3L}	Delay From Valid Low Output To Trailing Edge of Clock Out	30	51	72	nsec
T_4	Delay From Valid Data to STATUS LOW	12	18	37	nsec
T_{DLY}	Delay From Clock Out to STATUS HIGH	22	44	60	nsec
T_{SET}	Setup Time from Status to Conv. Command - (2)	0	---	---	nsec
T_{CW}	Clock Out Width	40	50	60	nsec
T_{CP}	Clock Out Period - (3) 12 Bit	192	265	270	nsec
	10 Bit	104	165	171	nsec
	8 Bit	88	95	98	nsec

NOTES: 1. ADC60 internal clock may be inhibited by returning the convert command to "1". By this technique, the converter may be cycled through an entire conversion one clock pulse at a time. This technique allows the conversion time to be extended to virtually any conversion time.

2. The convert command may rise as soon as the last clock out pulse rises.
3. The clock period for ADC60 is not necessarily constant throughout the conversion time.

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

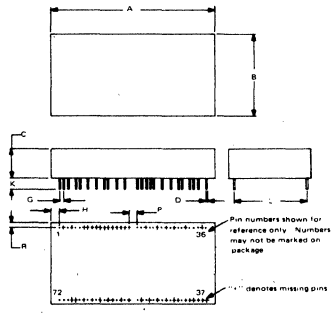
MODEL	ADC60-08	ADC60-10	ADC60-12	UNITS
RESOLUTION	8	10	12	Bits
INPUT				
ANALOG INPUTS				
Voltage Ranges, Bipolar		±2.5, ±5, ±10		V
Voltage Ranges, Unipolar		0 to +5, 0 to +10, 0 to +20		V
Impedance		0.2		kΩ/V FSR
DIGITAL INPUTS(1)				
Convert Command		Positive Pulse 30nsec wide min. Trailing edge "1" to "0" initiates conversion.		
Logic Loading		2		TTL Loads
TRANSFER CHARACTERISTICS				
ERROR(2)				
Gain Error	±0.2	±0.1	±0.1	% of FSR(3)
Offset Error	±0.2	±0.1	±0.1	% of FSR
Linearity Error, max	±0.195	±0.0488	±0.0244	% of FSR
Inherent Quantization Error	±0.19	±0.048	±0.012	% of FSR
Differential Linearity Error, max	±0.27	±0.068	+0.024, -0.019	% of FSR
Monotonicity	•	Guaranteed	•	
No Missing Codes	•	Guaranteed	•	
Power Supply Sensitivity	•	±0.002	•	% of FSR/%
DRIFT				
0°C to +70°C, max	±20	±20	±15	ppm/°C
-25°C to +85°C, max	±40	±40	±30	ppm/°C
CONVERSION SPEED, max	0.88	1.88	3.5	µsec
OUTPUT(4)				
DIGITAL DATA				
Parallel				
Output Codes, Unipolar		USB (straight binary		
Output Codes, Bipolar		BOB (offset binary) and BTC (Two's Complement)		
Output Drive		6		TTL Loads
Serial Data Output Drive		6		TTL Loads
Status		"1" During Conversion		
$\overline{\text{Status}}$		"0" During Conversion		
Output Drive of Status and $\overline{\text{Status}}$		6		TTL Loads
Clock		A Positive Pulse Train Used for Strobing Serial Data into an External Register.		
Clock Output Drive		9		TTL Loads
INTERNAL REF. VOLTAGE		6.3		V
Max External Current with no degradation of Specifications		200		µA
POWER REQUIREMENTS				
Rated Voltages		±15 and +5		V
Range for Rated Accuracy		±14.5 to ±15.5 and +4.75 to +5.25		V
Supply Drain +15V		+50		mA
Supply Drain -15V (max)		-50		mA
Supply Drain +5V		+270		mA
PACKAGE		2" x 4" x 0.75"		
TEMPERATURE RANGE				
Specification		0 to +70		°C
Operating (reduced drift specs - see above)		-25 to +85		°C
Storage		-55 to +100		°C

NOTES:
1. All digital inputs in the ADC60 are TTL compatible (i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V, min.).
2. Gain and Offset Errors may be adjusted to zero with external trimming.
3. FSR means Full Scale Range.
4. TTL compatible, Logic "0" = +0.4V, max, Logic "1" = +2.4V, min.

*Specifications same for all models.

MECHANICAL

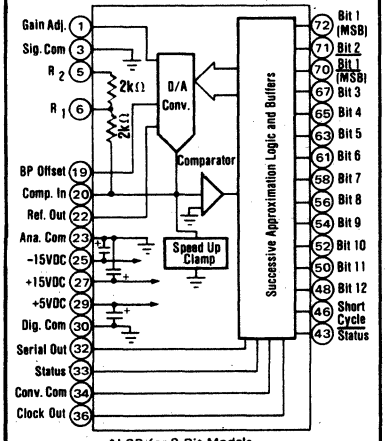
NOTE:
Leads in true position within .015" (.38mm) R @ MMC at seating plane.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.950	2.010	49.53	51.05
B	1.950	2.010	49.53	51.05
C	.350	4.10	8.89	10.41
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.300	6.35	7.62
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	.050	.150	1.27	3.81

Material: Case - Diallyl Phthalate Shell.
Weight: 5 oz.
Mating Connector: 2400MC - PC Card & Terminals
2401MC - Set of four 18-pin connector strips.
Pin spacing located on 2.54mm (0.10") grid. Allow 5.08mm (0.20") between pins 18-19 and 54-55. Pin material and plating composition meet method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CONNECTION DIAGRAM



*LSB for 8 Bit Models.
**LSB for 10 Bit Models.
***LSB for 12 Bit Models.

DISCUSSION OF PERFORMANCE

ACCURACY

A/D converter error contributors are Quantization Error, Linearity Error, Drift, Gain and Offset errors. Figure 2 shows the transfer function of an ideal bipolar A/D converter, and describes the quantization and linearity error bands at a single temperature. Initial gain and offset errors are trimmed to zero. Gain drift rotates the line about the minus full scale point (or around zero for a unipolar A D converter). Offset drift contributes an offset shift to the transfer function over the operating temperature range.

LINEARITY ERROR

Linearity Error is measured as the difference, in LSB, between the actual input voltage signal and the ideal transition voltage as shown in Figure 2. This measurement is made with Gain and Offset errors adjusted to zero. Thus, the Linearity Error, neglecting Quantizing Error, expresses the true accuracy of an A D converter relative to the reading.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error is defined as the difference between actual adjacent transition values and an ideal 1LSB step. A Differential Linearity Error of 1 2LSB means that the size of a horizontal step can range from 1 2LSB to 3 2LSB. The size of the smallest step must be greater than 0.2LSB to guarantee no missing codes in an A/D converter. Expressed mathematically, Differential Linearity (D.L.)

$$\triangleq[(V_{i+1} - V_i) - \text{LSB LSB}] \text{ where LSB} \triangleq V_{i+1} - V_i.$$

MONOTONICITY

An A/D converter is monotonic when the digital output code increases or remains the same for increasing analog input signals. The ADC60 is monotonic over the full scale range.

DIGITAL OUTPUT CODES

Three binary digital codes may be derived from the ADC60. They are Unipolar Straight Binary (USB) for unipolar analog input signals, and Bipolar Offset Binary (BOB) and Bipolar Two's Complement (BTC) for bipolar analog input signals. These codes are defined below in Table II.

A more detailed discussion of these and other A/D converters specifications is given in a separate Burr-Brown Application Note - AN53.

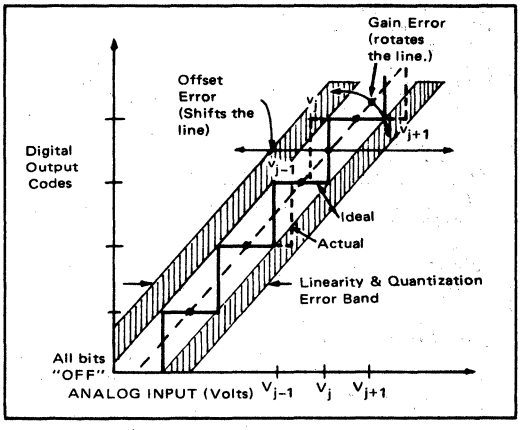


FIGURE 2. A/D Converter Definition of Specifications.

DEFINITION OF DIGITAL CODES

Three binary codes are available on the ADC60 parallel output; these are USB for unipolar input signals, and BOB or BTC for bipolar input signals. The LSB values and code definitions for each analog input signal range are shown below.

TABLE II. Input Voltages, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Signal Range	Defined As:	±10V	±5V	±2.5V	0 to +20V	0 to +10V	0 to +5V
Code Designation		BOB or BTC*	BOB or BTC*	BOB or BTC*	USB**	USB**	USB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	78.13mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	19.53mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	4.88mV	2.44mV	1.22mV
MSB LSB							
111....111***	+Full Scale	+10V -½LSB	+5V -½LSB	+2.5V -½LSB	+20V -½LSB	+10V -½LSB	+5V -½LSB
100....000	Mid Scale	0	0	0	+10V	+5V	+2.5V
000....001	-Full Scale	-10V +½LSB	-5V +½LSB	-2.5V +½LSB	0 +½LSB	0 +½LSB	0 +½LSB

*BOB = Bipolar Offset Binary
**USB = Unipolar Straight Binary
BTC = Bipolar Two's complement - obtained by using the complement of the most significant bit (MSB). MSB is available on pin 70 of the module.
*** Voltages given are the nominal value for transition to the code specified.

INSTALLATION AND OPERATING INSTRUCTIONS

The ADC60 is available with binary code resolutions of 8, 10 and 12 bits. Six input signal ranges are pin-programmable over the following ranges: 0 to +5V, +20V, +10V, ±2.5V, ±5V and ±10V.

Single polarity binary ranges are designated USB and dual polarity binary ranges are designated BOB or BTC. Connections for specific codes are detailed in Table III.

OPTIONAL GAIN AND OFFSET ADJUST

Although Gain and Offset are factory trimmed to ±0.1%, these parameters may be trimmed to zero error using external trim adjustments as shown in Figure 3. Due to component aging, these external adjustments may be required later on to recalibrate the ADC60 after 3 to 6 months.

To avoid interaction between adjustments, the offset should be adjusted first. Use multiturn potentiometers with TCR of 150ppm °C or better.

Offset is adjusted by sweeping the input through the end point transition voltage that causes an output transition to "all bits Off". Adjust the Offset potentiometers until the actual end point transition voltage occurs at the value shown in Table II.

Gain is adjusted by sweeping the input voltage through the end point transition that causes an output digital code of "all bits On". See Table I for end point transition values.

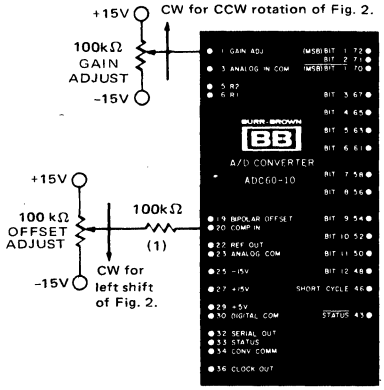


FIGURE 3. ADC60 Installation Diagram.

NOTE:
1. If Gain and/or Offset trim adjustments are not used simply leave pin 1 and/or pin 20 open. The minimum range of adjustment for OFFSET is ±0.25% of full scale range; for GAIN it is ±0.3% of full scale range. Locate the 100kΩ resistor as close as possible to pin 20..

GENERAL NOTES:
- If an input buffer amplifier is required, the BB3550 is recommended.
- Use BB SHM60 Sample/Hold if a Sample/Hold is required (1μsec acquisition time).

INPUT SCALING

To utilize the maximum resolution of the ADC60, the input FSR must be selected to match the expected full scale range of the input signal. Figure 4 and TableIII show the connections required for input scaling.

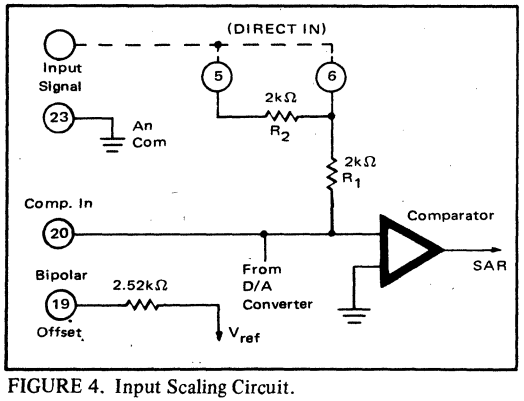


FIGURE 4. Input Scaling Circuit.

TABLE III. ADC60 Input Scaling Connections.

INPUT SIGNAL RANGE	DIGITAL OUTPUT CODE	CONNECT PIN 19 TO	CONNECT PIN 5 TO	CONNECT INPUT SIGNAL TO
±2.5V	BOB or BTC	PIN 20	PIN 20	PIN 6
0 to +5V	USB	PIN 23	PIN 20	PIN 6
±5V	BOB or BTC	PIN 20	OPEN	PIN 6
0 to +10V	USB	PIN 23	OPEN	PIN 6
0 to +20V	USB	PIN 23	INPUT	PIN 5
±10V	BOB or BTC	PIN 20	INPUT	PIN 5

INSTALLATION AND OPERATING INSTRUCTIONS (CONT)

SYSTEM TIMING

The basic system timing diagram is shown in Figure 1.

CONVERT COMMAND

A pulse of at least 30nsec duration (positive going) is required at pin 34 to start each conversion. Conversion starts after the Negative Going edge of the Convert Command.

STATUS

The Status output switches to a logical "1" on the Negative Edge of the Convert Command pulse. It returns to a logical "0" at the end of the conversion. The $\overline{\text{Status}}$ output leads Status by one normal gate delay (10nsec).

SHORT CYCLE

The ADC60 may be short-cycled for obtaining lower resolutions and corresponding faster conversion speeds. Connect "Short Cycle" (pin 46) of the ADC60 to bit N + 1 as shown in Table IV.

The Short Cycle feature must be used for the 8- and 10-bit models as outlined in Table IV. For 12-bit models, the Short Cycle is not used and may be left open; however, in a high noise environment, the Short Cycle input, pin 46, should be tied to +5V (pin 29) through a 1000Ω resistor.

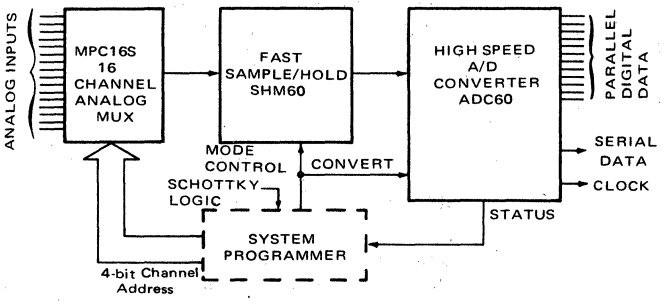
TABLE IV. Short Cycle Connections for ADC60 and Corresponding Conversion Speeds.

RESOLUTION (BITS)	CONNECT PIN 46 TO PIN	MAXIMUM CONVERSION TIME (μSEC)		
		MODEL		
		8	10	12
12	N/A	–	–	3.50
11	48	–	–	3.29
10	50	–	1.88	3.08
9	52	–	1.71	2.87
8	54	0.88	1.53	2.66
7	56	0.79	1.37	2.45
6	58	0.69	1.20	2.24
5	61	0.59	1.03	2.03
4	63	0.49	0.85	1.69

APPLICATION NOTE

HIGH SPEED DATA ACQUISITION SYSTEM

A high speed 16-channel data acquisition system with up to 625kHz system sampling rate is shown below. (If the ADC60 is used without a multiplexer or sample/hold for single channel applications, sampling rates up to 1MHz are possible.)



The system shown uses an overlapped mode programmer to eliminate or reduce the settling effects of the multiplexer and sample/hold and maximizes system throughput speed.

Typical system sampling speeds for the input signal ranges using these components are shown in Table V.

TABLE V. Typical System Characteristics.

RESOLUTION (BITS)	INPUT SIGNAL RANGE (volts)	SYSTEM THROUGHPUT SAMPLING RATE (max)	TYPICAL SYSTEM ACCURACY *RSS
12	±10	200kHz	±0.04%
12	0 to +10	220kHz	±0.04%
10	±10	325kHz	±0.125%
10	0 to +10	370kHz	±0.125%
8	±10	530kHz	±0.25%
8	0 to +10	625kHz	±0.25%

*RSS = Root Sum Squared.

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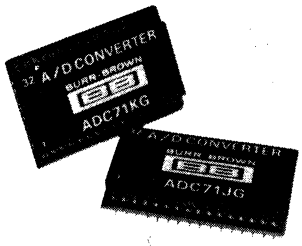


ADC71

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES:

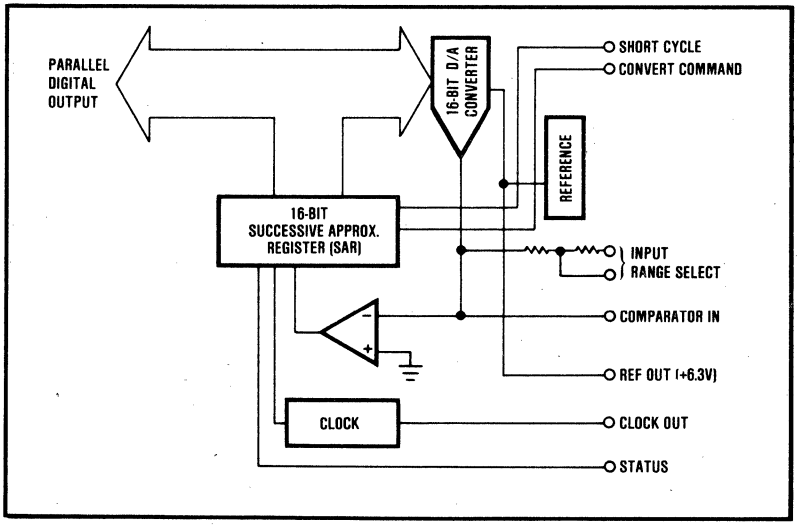
- 16-BIT RESOLUTION
- LINEARITY ERROR ±0.003%
- COMPACT DESIGN
  32-Pin Ceramic Package
- FAST CONVERSION SPEED
- LOW COST

DESCRIPTION

The ADC71 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The ADC71 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a convenient 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, and thin-film scaling resistors, which allows selection of analog input ranges of ±2.5V, ±5.0V, ±10.0V, 0 to +5.0V, 0 to +10V and 0 to +20V.

Data is available in parallel form with corresponding clock and status output. All digital input and outputs are DTL/TTL compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

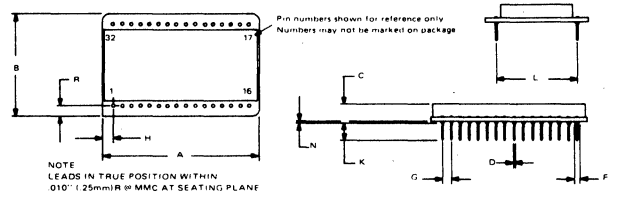
Typical at +25°C and rated power supplies unless otherwise noted.

MODEL	ADC71KG			ADC71JG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
ANALOG INPUTS							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL INPUTS(1)							
Convert Command	Positive pulse 50nsec wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading			1			1	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±0.1(2)	±0.2		±0.1(2)	±0.2	%
Offset							
Unipolar		±0.05(2)	±0.1		±0.05(2)	±0.1	% of FSR(3)
Bipolar		±0.1(2)	±0.2		±0.1(2)	±0.2	% of FSR
Linearity Error			±0.003			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0.003		% of FSR/%V_{CC}
+5VDC		0.001			0.001		% of FSR/%V_{CC}
CONVERSION TIME(4) 14 Bits			50			50	µsec
WARM-UP TIME	5			5			min
DRIFT							
Gain			±15			±15	ppm/°C
Offset							
Unipolar		±2	±4		±2	±4	ppm of FSR/°C
Bipolar			±10			±10	ppm of FSR/°C
Linearity		±2	±3		±2	±3	ppm of FSR/°C
No Missing Codes Temp Range							
KG 14-bit	+10		+40				°C
JG 13-bit				0		50	°C
OUTPUT							
DIGITAL DATA							
All codes complementary							
Parallel							
Output Codes(5)							
Unipolar			CSB				
Bipolar			COB, CTC(6)				
Output Drive			2				TTL Loads
Status			Logic "1" during conversion				
Status Output Drive			2			2	TTL Loads
Internal Clock							
Clock Output Drive			2			2	TTL Loads
Frequency		280			280		kHz
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Max External Current with No Degradation of Specs			±200			±200	µA
Temp Coefficient			±10			±10	ppm/°C
POWER SUPPLY REQUIREMENTS							
Power Consumption		1.55			1.55		W
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+45			+45		mA
Supply Drain -15VDC		-35			-35		mA
Supply Drain +5VDC		+70			+70		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (derated specs)	-25		+85	-25		+85	°C
Storage	-55		+125	-55		+125	°C

NOTES:
1. DTL/TTL compatible, i.e., Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V, max. Logic "1" = 2.4V, min.
2. Adjustable to zero.
3. FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR.
4. Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section.
5. See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.
6. CTC coding obtained by inverting MSB (Pin 1).

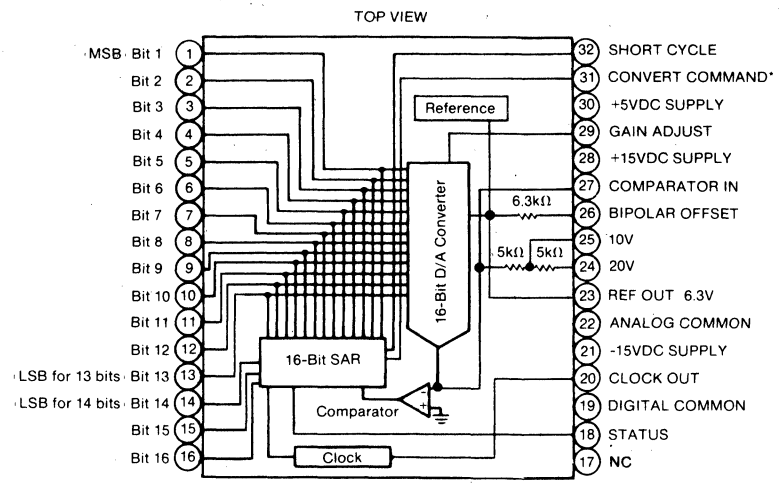
MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30



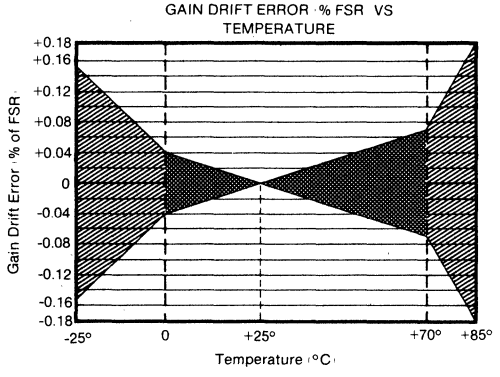
CASE: Ceramic
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams 0.46 oz.

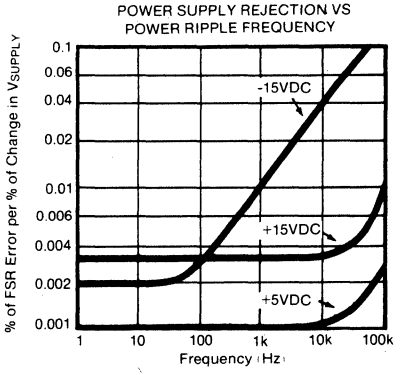
CONNECTION DIAGRAM



*If an external clock is used, connect the clock to pin 31 CONVERT COMMAND.

TYPICAL PERFORMANCE CURVES





DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2 LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1 2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC71 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that this converter will have no missing codes over a specified temperature range when short cycled for 14-bit operation.

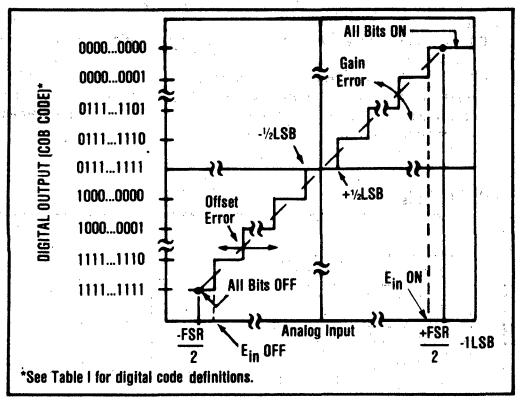


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output).

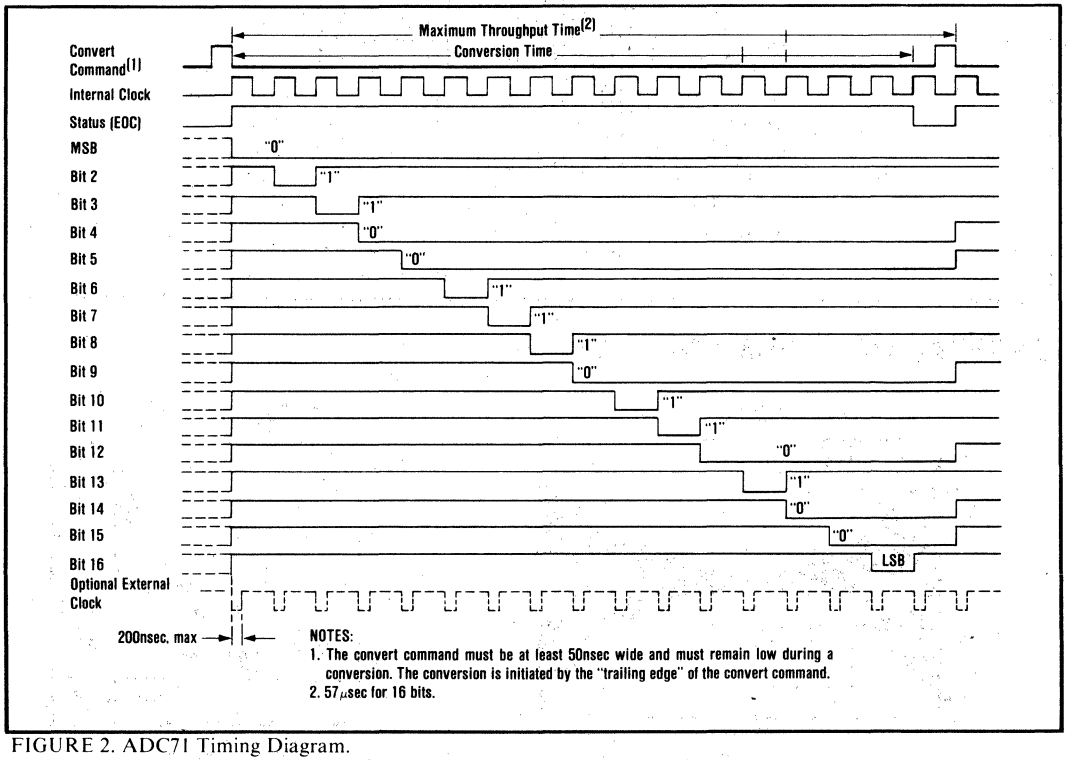


FIGURE 2. ADC71 Timing Diagram.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Two binary codes are available on the ADC71 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (Pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

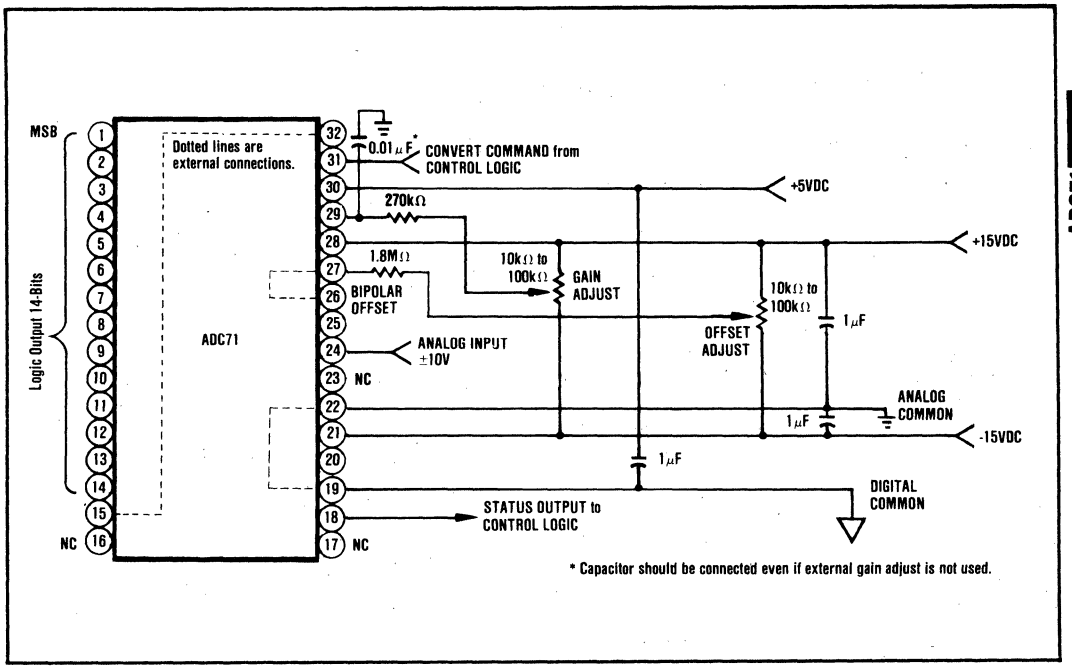


FIGURE 3. ADC71 Connections For: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
n = 12		4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
n = 13		2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
n = 14		1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary
**CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB (Pin 1)
***CSB = Complementary Straight Binary
****Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC71 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC71 power supply sensitivity is specified for ±0.003% of FSR/%V_{CC}, for ±15V supplies and ±0.0015% of FSR/%V_{CC} for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC71 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (Pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC.

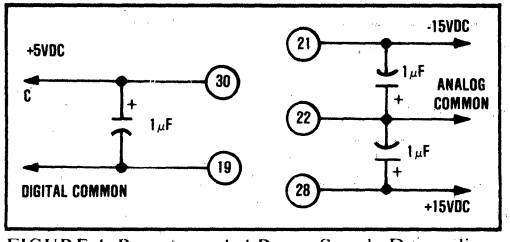


FIGURE 4. Recommended Power Supply Decoupling.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

TABLE II. ADC71 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB Pin 1.

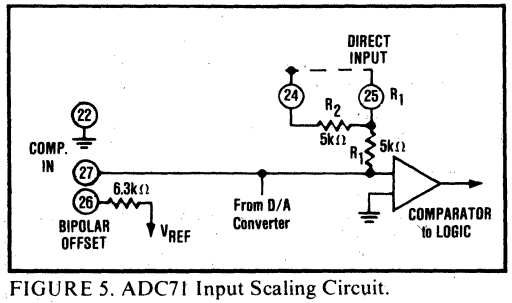


FIGURE 5. ADC71 Input Scaling Circuit.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm °C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and Pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 6. Sweep the input through the end point transition voltage

that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

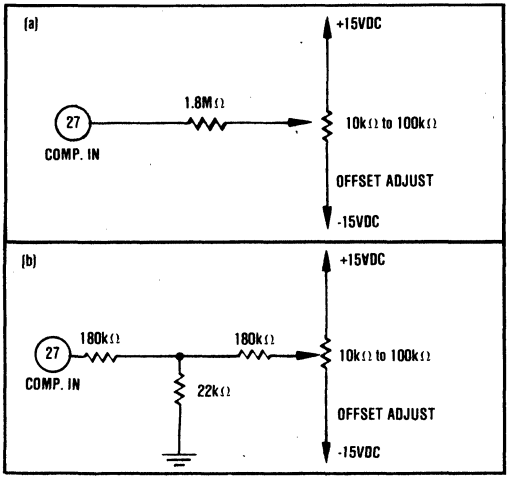


FIGURE 6. Two Methods of Connecting Optional Offset Adjust.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

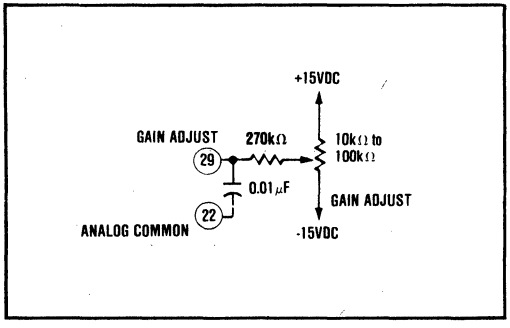


FIGURE 7. Connecting Optional Gain Adjust.

EXTERNAL CLOCK

If an external clock is used, connect the external clock to convert command, pin 31. The convert command shown in Figure 2 is not used. After each conversion is completed, a new conversion cycle will automatically start on the first falling edge of the external clock following the completion of conversion. The clock out signal will remain as shown in Figure 2 even if an external clock is used. The external clock pulse must be a negative going pulse with a width between 100nsec and 200nsec as shown in Figure 2, and must be at a lower frequency than the internal clock.

ADDITIONAL CONNECTIONS REQUIRED

The ADC71 may be operated at faster speeds for resolutions less than 14 or 13 bits, depending on the model selected, by connecting the Short Cycle Input, pin 32, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

TABLE III. Short Cycle Connections and Specifications for 12- to 14-Bit Resolutions.

Resolution (Bits)	16	14	13	12
Connect Pin 32 to	Open	Pin 15	Pin 14	Pin 13
Maximum Conversion Speed (μsec)(1)	57	50	46.5	43
Maximum Nonlinearity at 25°C (% of FSR)	0.003(2)	0.003(2)	0.006(3)	0.006(3)

NOTES:
1. Max. conversion time to maintain specified nonlinearity error.
2. ADC71KG only.
3. ADC71KG or ADC71JG.

OUTPUT DRIVE

Normally all ADC71 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC71 dissipates approximately 1.55 watts (typical) and the packages have a case-to-ambient thermal resistance (θ_{CA}) of 25°C W. For operation above 70°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 8 for θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square inch (min.) area, this technique will allow operation to 85°C.

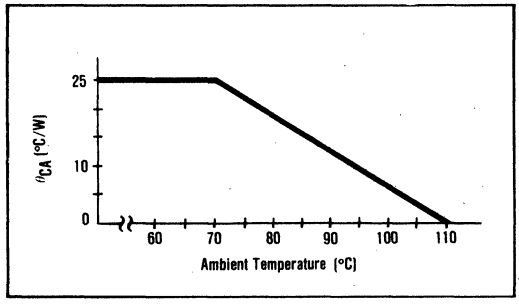


FIGURE 8. θ_{CA} Requirement Above 70°C.

ORDERING INFORMATION

MODEL	TEMPERATURE	PACKAGE
ADC71KG	0°C to +70°C	Ceramic
ADC71JG	0°C to +70°C	Ceramic

BURR-BROWN®

ADC72

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES:

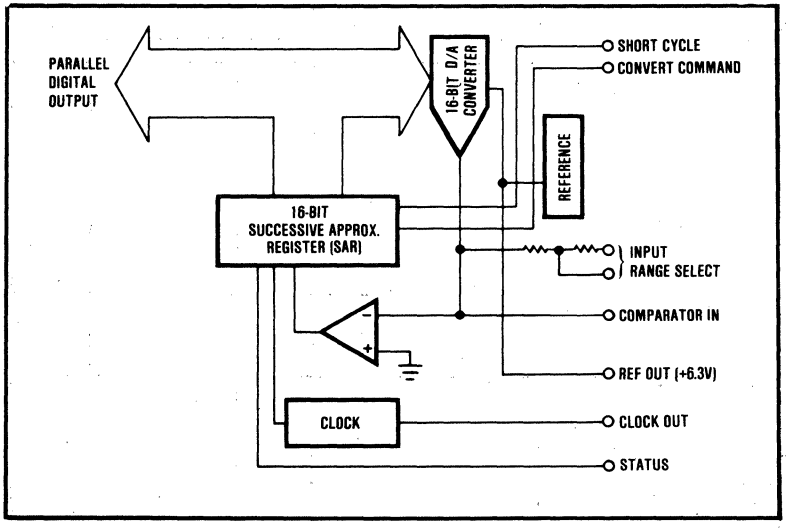
- 16-BIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- COMPACT DESIGN
  32-Pin Hermetic Metal Package
- FAST CONVERSION SPEED
  50μsec Maximum
- LOW COST

DESCRIPTION

The ADC72 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. It uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a compact 32-pin metal dual-in-line package. The converter is complete with internal reference, clock, comparator, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel form with corresponding click and status output. All digital input and outputs are DTL/TTL compatible.

Power suply voltages are ±15VDC and +5VDC.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

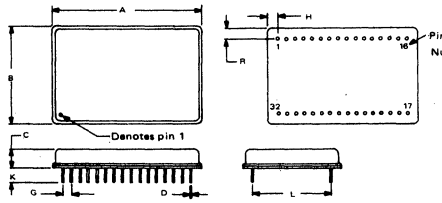
Typical at +25°C and rated power supplies unless otherwise noted.

MODEL	ADC72JM, KM			ADC72AM, BM			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
INPUT							
ANALOG							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Impedance, Direct Input							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL(1)							
Convert Command	Positive pulse 50nsec wide, min. trailing edge, "1" to "0" initiates conversion						
Logic Loading		1				1	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(2)		±0.1	±0.2		±0.1	±0.2	%
Offset Gain(2)							
Unipolar		±0.05	±0.1		±0.05	±0.1	% of FSR(3)
Bipolar		±0.1	±0.2		±0.1	±0.2	% of FSR
Linearity Error KM, BM			±0.003			±0.003	% of FSR
JM, AM			±0.006			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		±0.003			±0.003		% of FSR/%ΔVs
+5VDC		±0.001			±0.001		% of FSR/%ΔVs
CONVERSION TIME(4), 14 Bits			50			50	μsec
WARM-UP TIME	10			10			min
DRIFT							
Gain		±10	±20		±7	±15	ppm/°C
Offset							
Unipolar		±2	±4			±2	ppm of FSR/°C
Bipolar		±8	±10		±5	±10	ppm of FSR/°C
Linearity		±2	±3			±2	ppm of FSR/°C
No Missing Codes Temp Range							
JM, AM (13 bits)	0		+50	0		+50	°C
KM, BM (14 bits)	+10		+40	+10		+40	°C
OUTPUT							
DIGITAL DATA							
All codes complementary							
Parallel							
Output Codes(5)							
Unipolar	CSB						
Bipolar	COB, CTC(6)						
Output Drive	2						TTL Loads
Status	Logic "1" during conversion						
Status Output Drive			2			2	TTL Loads
Internal Clock							
Clock Output Drive			2			2	TTL Loads
Frequency		280			280		kHz
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Max External Current with No Degradation of Specs			±200			±200	μA
Temp Coefficient			±10			±5	ppm/°C
POWER SUPPLY REQUIREMENTS							
Power Consumption		1.3			1.3		W
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+45			+45		mA
Supply Drain -15VDC		-35			-35		mA
Supply Drain +5VDC		+70			+70		mA
TEMPERATURE RANGE							
Specification	0		+70	-25		+85	°C
Operating, derated specs	-25		+85	-55		+85	°C
Storage	-55		+125	-55		+125	°C

NOTES:
1. DTL/TTL compatible, i.e., Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V, max. Logic "1" = 2.4V, min.
2. Adjustable to zero.
3. FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR.
4. Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section.
5. See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.
6. CTC coding obtained by inverting MSB (Pin 1).

MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56



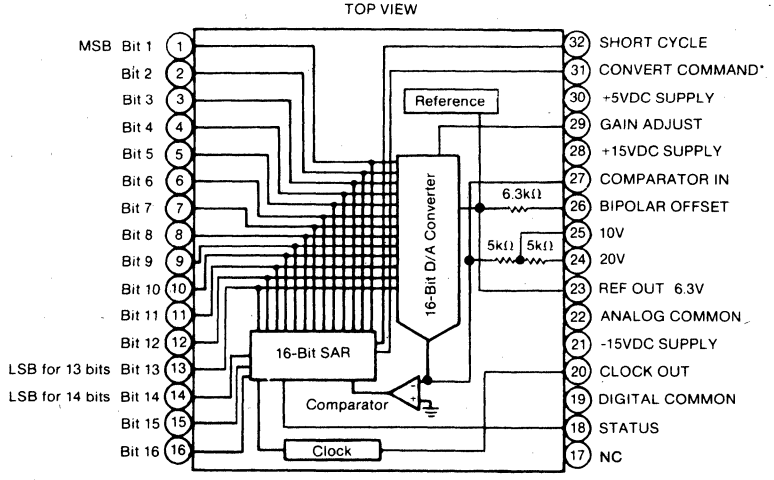
NOTE:
Leads in true position within .010" .255mm R at MMC at seating plane.

Pin numbers shown for reference only.
Numbers may not be marked on package.

CASE: Nickel-plated kovar
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams (0.46 oz.)

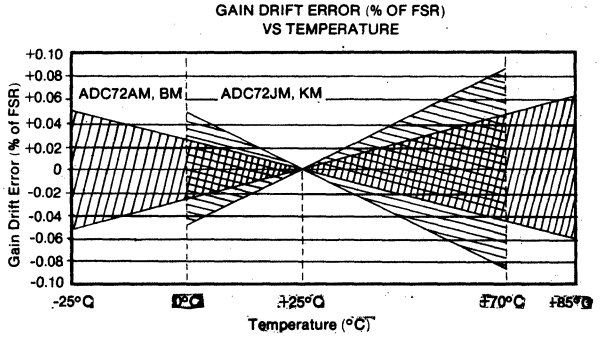
Contrasting glass seal or square corner denotes pin 1.

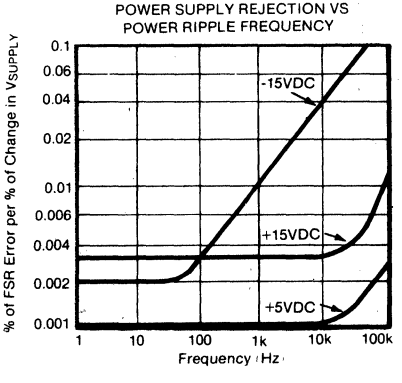
CONNECTION DIAGRAM



*If an external clock is used, connect the clock to pin 31 CONVERT COMMAND.

TYPICAL PERFORMANCE CURVES





DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2 LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC72 is also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperature range when short-cycled for 14-bit operation.

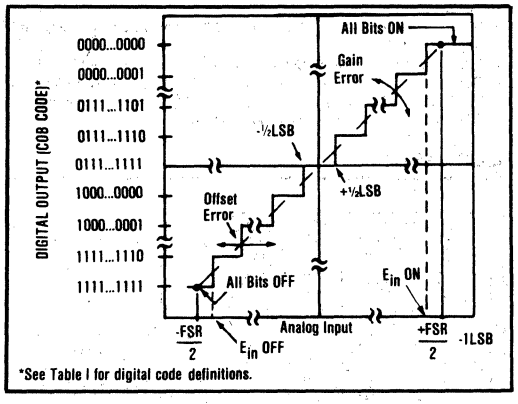


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output).

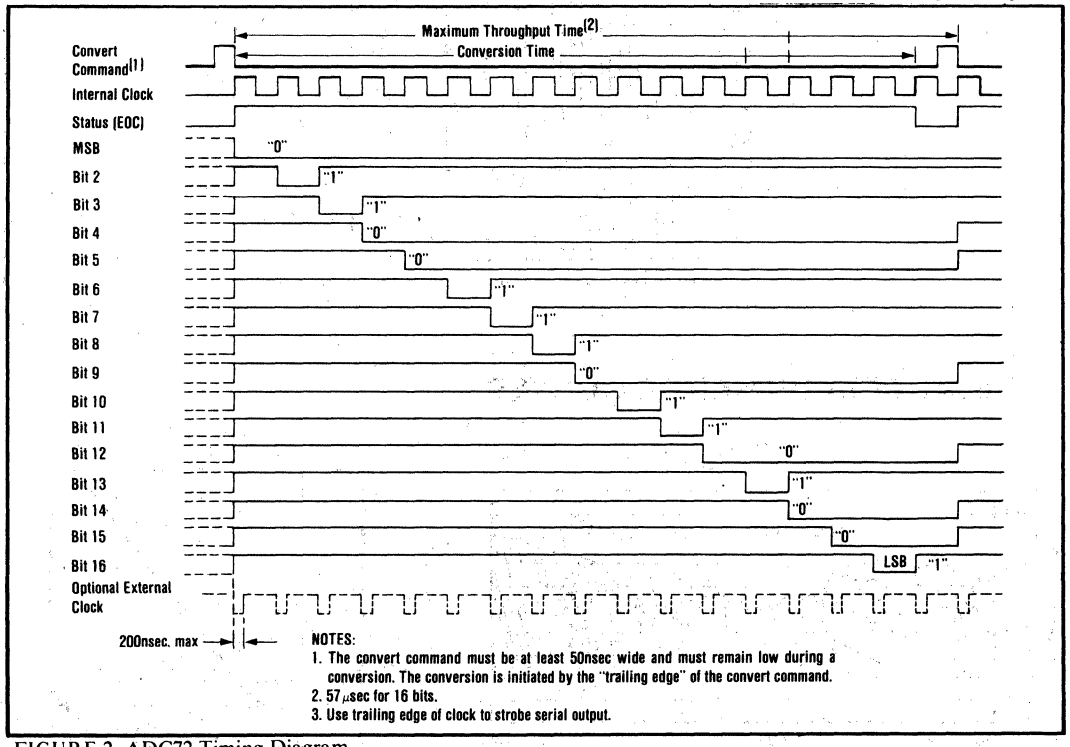


FIGURE 2. ADC72 Timing Diagram.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Two binary codes are available on the ADC72 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (Pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±10V output.

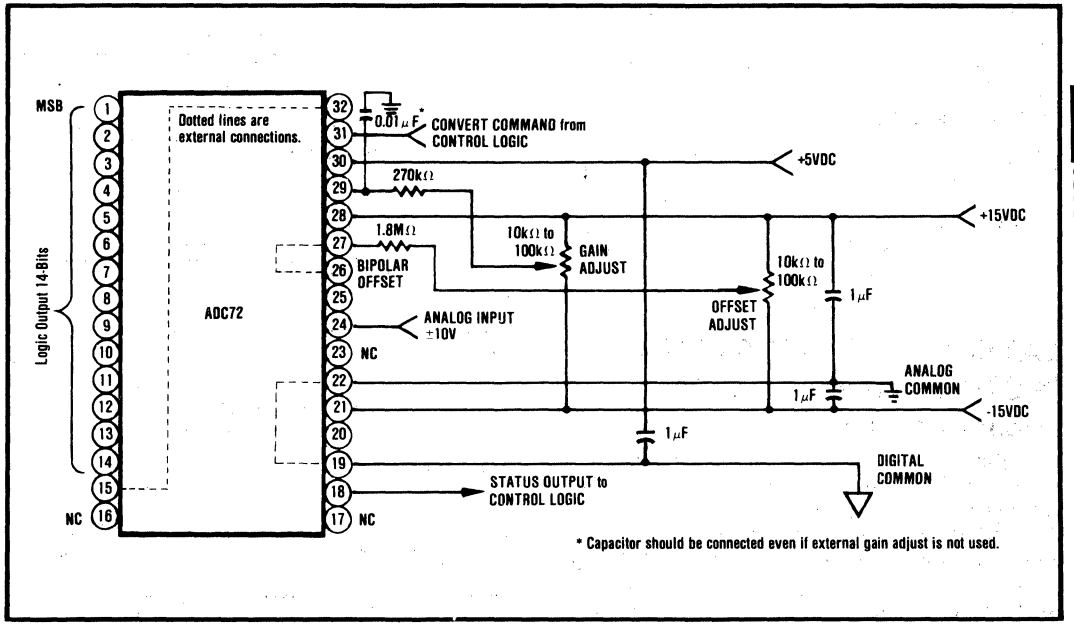


FIGURE 3. ADC72 Connections For: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

(1) COB = Complementary Offset Binary
(2) CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB (Pin 1)
(3) CSB = Complementary Straight Binary
(4) Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC72 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC72 power supply sensitivity is specified for ±0.003% of FSR/%ΔV_S for ±15V supplies and ±0.001% of FSR/%ΔV_S for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC72 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF non-polarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (Pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC.

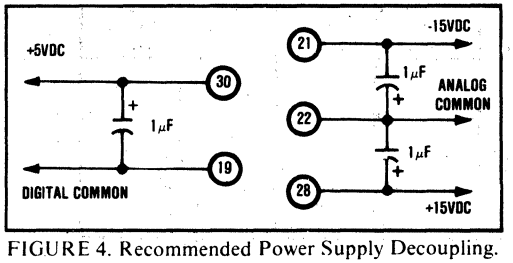


FIGURE 4. Recommended Power Supply Decoupling.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

TABLE II. ADC72 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB - Pin 1

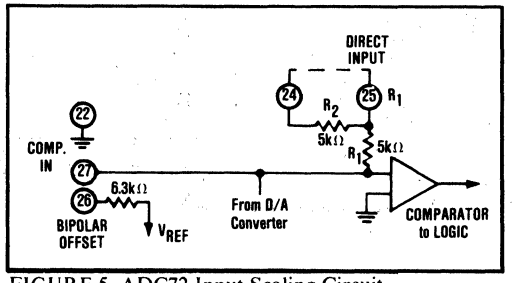


FIGURE 5. ADC72 Input Scaling Circuit.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and Pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits Off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

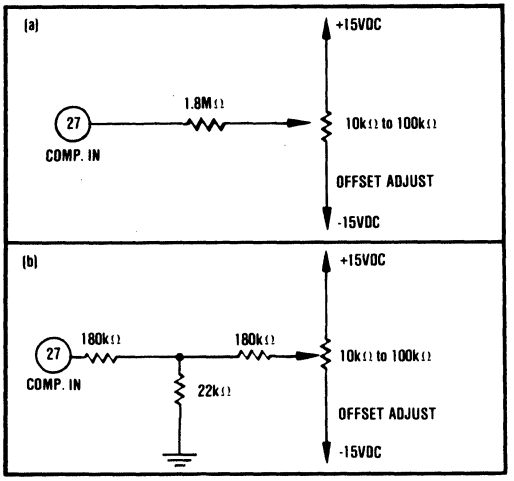


FIGURE 6. Two Methods of Connecting Optional Offset Adjust.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

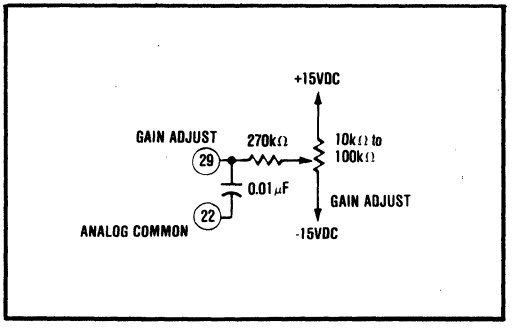


FIGURE 7. Connecting Optional Gain Adjust.

EXTERNAL CLOCK

If an external clock is used, connect the external clock to convert command, pin 31. The convert command shown in Figure 2 is not used. After each conversion is completed, a new conversion cycle will automatically start on the first falling edge of the external clock following the completion of conversion. The clock out signal will remain as shown in Figure 2 even if an external clock is used.

The external clock pulse must be a negative-going pulse with a width between 100nsec and 200nsec as shown in Figure 2, and must be at a lower frequency than the internal clock.

ADDITIONAL CONNECTIONS REQUIRED

The ADC72 may be operated at faster speeds for resolutions less than 14 or 13 bits, depending on the model selected, by connecting the Short-Cycle Input, pin 32, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

TABLE III. Short-Cycle Connections and Specifications for 12- to 14-Bit Resolutions.

Resolution (Bits)	16	14	13	12
Connect Pin 32 to	Open	Pin 15	Pin 14	Pin 13
Maximum Conversion Speed (μsec)(1)	57	50	46.5	43
Maximum Nonlinearity at 25°C (% of FSR)	0.003(2)	0.003(2)	0.006	0.006

NOTES:
1. Max. conversion time to maintain specified nonlinearity error.
2. BM and KM models only.

OUTPUT DRIVE

Normally all ADC72 logic outputs will drive 2 standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC72 dissipates approximately 1.3 watts (typical) and the packages have a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above 70°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 8 for θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square inch (min.) area, this technique will allow operation to 85°C.

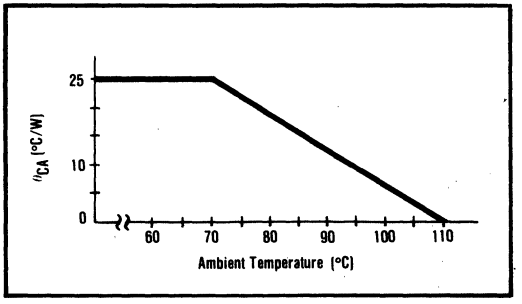
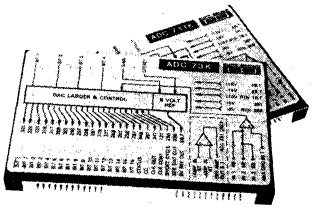


FIGURE 8. θ_{CA} Requirement Above 70°C.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	NONLINEARITY
ADC72JM	0°C to +70°C	±0.006% FSR
ADC72KM	0°C to +70°C	±0.003% FSR
ADC72AM	-25°C to +85°C	±0.006% FSR
ADC72BM	-25°C to +85°C	±0.003% FSR

BURR-BROWN®



ADC73
ADC731

True 16-Bit
ANALOG-TO-DIGITAL CONVERTER

FEATURES

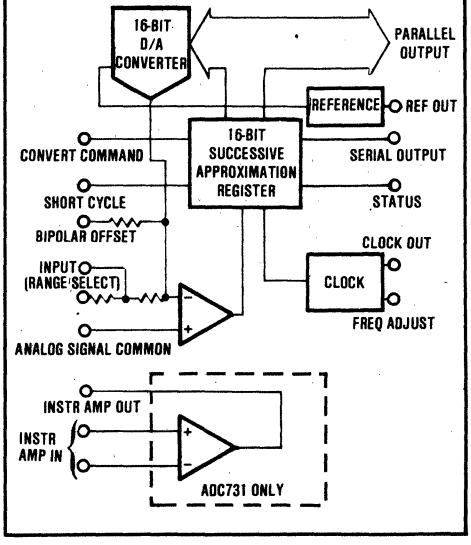
- 16-BIT RESOLUTION WITH TRUE 16-BIT ACCURACY
- LINEARITY ERROR OF LESS THAN ±0.00075% max (K model)
- OPTIONAL UNITY-GAIN INSTRUMENTATION AMPLIFIER INPUT (ADC731)
- FAST CONVERSION TIME - 170μsec max to ±0.00075% accuracy (K models)
- USER-SELECTED INPUT RANGES
- VERY-HIGH PERFORMANCE/PRICE RATIO

DESCRIPTION

The ADC73 and ADC731 are high quality, 16-bit successive approximation analog-to-digital converters that are linear to within ±0.0015% of full scale range (J models) or ±0.00075% of full scale range (K models). They combine state-of-the-art monolithic, hybrid, and discrete technologies to establish a new standard in value for true 16-bit A D converters. Complete with precision internal reference and comparator, ultra-stable clock, and unity-gain instrumentation amplifier input (ADC731), the ADC73 and ADC731 are ready to use. The user-selectable input ranges of ±5V, ±10V, 0 to +10V, and 0 to +20V, short-cycle capability for faster throughput rates, optional instrumentation amplifier input, binary or two's complement codes, parallel and serial outputs, and low price make this versatile converter suitable for a wide range of demanding applications.

Control signals and output data lines are TTL-compatible over the entire operating temperature range. Output data is available as a parallel word or a serial bit stream (MSB first) with corresponding clock and status outputs.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and rated power supplies unless otherwise noted.

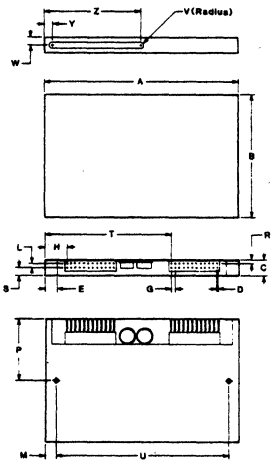
MODEL	ADC73J, ADC731J			ADC73K, ADC731K			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
INPUT CHARACTERISTICS							
ANALOG							
Voltage Ranges							
Bipolar		±5, ±10			*		V
Unipolar(1)		0 to +10, 0 to +20			*		V
Input Impedance, Direct Input							
0 to +10, ±5V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
Differential Amplifier - ADC731 only							
Input Impedance, Differential		10^{10} ‖ 3			*		Ω ‖ pF
Common-mode		5 x 10^9 ‖ 3			*		Ω ‖ pF
Common-mode Voltage(2)		±(|Vcc|-3)			*		V
CMRR ±10V input (3)		76			*		dB
DIGITAL (Convert Command)							
Pulse Width	200			*			nsec
Logic "1" Voltage	2.0			*			V
Current			20			*	μA
Logic "0" Voltage			0.8			*	V
Current			0.4			*	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(4)		±0.001			*		%
Offset Error(4), Unipolar		±0.001			*		% of FSR
Bipolar		±0.001			*		% of FSR
Linearity Error(5)			±0.0015			±0.00075	% of FSR
Differential Linearity Error(5)		±0.0015	±0.003		±0.00075	±0.0015	% of FSR
Quantization Error			±0.00075			±0.00075	% of FSR
No Missing Codes Temperature Range	+15		+35	*		*	°C
Differential Ground Potential Error(6)							
Gain		0.01			*		LSB/mV
Offset		0.02			*		LSB/mV
Linearity		0.01			*		LSB/mV
Differential Linearity		0.02			*		LSB/mV
3σ Noise - Full Scale (7)		150	300		*	*	μV, p-p
POWER SUPPLY SENSITIVITY							
Offset, +15VDC			±0.0005			*	% of FSR/%ΔV
-15VDC			±0.0001			*	% of FSR/%ΔV
+5VDC			±0.0007			*	% of FSR/%ΔV
Gain, +15VDC			±0.00035			*	% of FSR/%ΔV
-15VDC			±0.0012			*	% of FSR/%ΔV
+5VDC			±0.0004			*	% of FSR/%ΔV
CONVERSION TIME(8)		150	170		*	*	μsec
WARM-UP TIME (To rated accuracy)		15			*		minutes
TEMPERATURE DRIFT (Including Internal Reference)							
Gain			±10			*	ppm/°C
Offset, Unipolar			±2			*	ppm of FSR/°C
Bipolar			±5			*	ppm of FSR/°C
Linearity		±0.5	±2		*	*	ppm of FSR/°C
Differential Linearity		±0.5	±2		*	*	ppm of FSR/°C
LONG TERM STABILITY							
Gain - Exclusive of Reference		±30			*		ppm/10^3 hr
Offset, - Exclusive of Reference - Bipolar		±30			*		ppm of FSR/ 10^3 hr
Unipolar		±5			*		ppm of FSR/ 10^3 hr
Linearity		±3.7	±7.5		*	*	ppm of FSR/ 10^3 hr
Reference		±50			*		ppm/10^3 hr

ELECTRICAL (CONT)

MODEL	ADC73J, ADC731J			ADC73K, ADC731K			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS							
DIGITAL							
Data Codes (Positive True Logic)							
Parallel(9)		USB, BOB, BTC			•		
Serial (NRZ)(9)		USB, BOB			•		
Status		Logic "1" During Conversion			•		
Internal Clock							
Frequency		113			•		kHz
Clock Adjust Range		±20			•		%
Logic Levels							
Logic "1" Voltage	2.4			•			V
Current			0.4			•	mA
Logic "0" Voltage			0.4			•	V
Current			3.2			•	mA
INTERNAL REFERENCE							
Voltage	+5.9988	+6.0000	+6.0012	•	•	•	V
Source Current Available for External Loads	4.0			•			mA
Temperature Drift			±5			•	ppm/°C
POWER SUPPLY REQUIREMENTS							
Voltage, +15VDC	+14.5	+15	+15.5	•	•	•	V
-15VDC	-14.5	-15	-15.5	•	•	•	V
+5VDC	+4.75	+5	+5.25	•	•	•	V
Current, +15VDC		---	60		•	•	mA
-15VDC		---	65		•	•	mA
+5VDC		---	130		•	•	mA
POWER DISSIPATION		---	2.5		•	•	W
TEMPERATURE RANGE							
Specification	0		+70	•		•	°C
Storage	-55		+100	•		•	°C

NOTES:
1. Maximum input voltage of ADC731 differential buffer input is ±10V.
2. V_{CC} is value of supply voltage connected to +15V and -15V power supply pins.
3. See CMRR versus frequency performance curve.
4. Adjustable to zero with internal potentiometers. FSR = Full Scale Range.
5. As adjusted at the factory. Periodic recalibration is performed by following the adjustment procedure in the Installation and Operating Instructions.
6. Effect on output of DC voltage differential being present between analog and digital grounds. Measured with 10V Full Scale Range input and up to 175mVDC between grounds.
7. For 20V FSR input voltage. Noise is directly proportional to user-selected FSR.
8. Conversion time can be reduced to 120μsec. See Typical Performance Curves for accuracy versus conversion time. Conversion time and resolution may also be reduced by "short-cycling". See Installation and Operating Instructions.
9. BOB = Bipolar Offset Binary, USB = Unipolar Straight Binary, BTC = Bipolar Two's Complement.

MECHANICAL



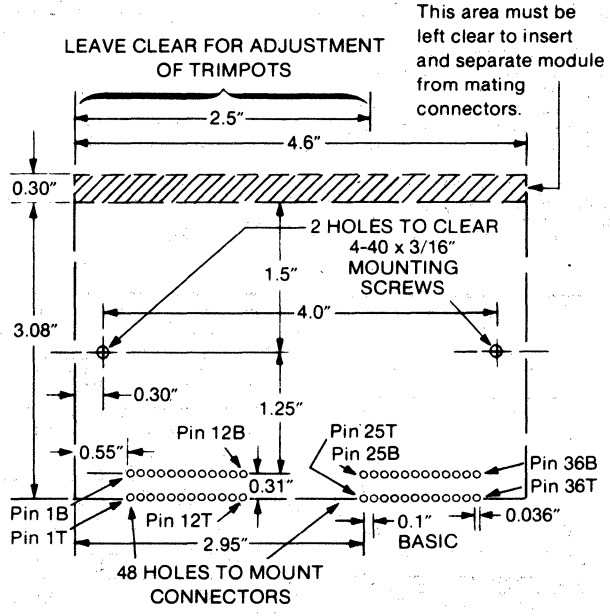
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.590	4.810	116.59	117.09
B	2.990	3.010	75.95	76.45
C	.380	.400	9.65	10.16
D	.022	.028	0.56	0.71
E	.290	.310	7.37	7.87
G	100 BASIC		2.54 BASIC	
H	.540	.560	13.72	14.22
L	100 BASIC		2.54 BASIC	
M	.290	.310	7.37	7.87
P	1.46	1.54	37.08	39.11
R	.180	.200	4.57	5.08
S	.090	.110	2.29	2.79
T	2.95	2.97	74.93	75.44
U	3.990	4.010	101.35	101.85
V	.065	.085	1.65	2.16
W	.140	.160	3.56	4.06
Y	.235	.255	5.97	6.48
Z	2.285	2.305	58.04	58.55

PIN DESIGNATIONS

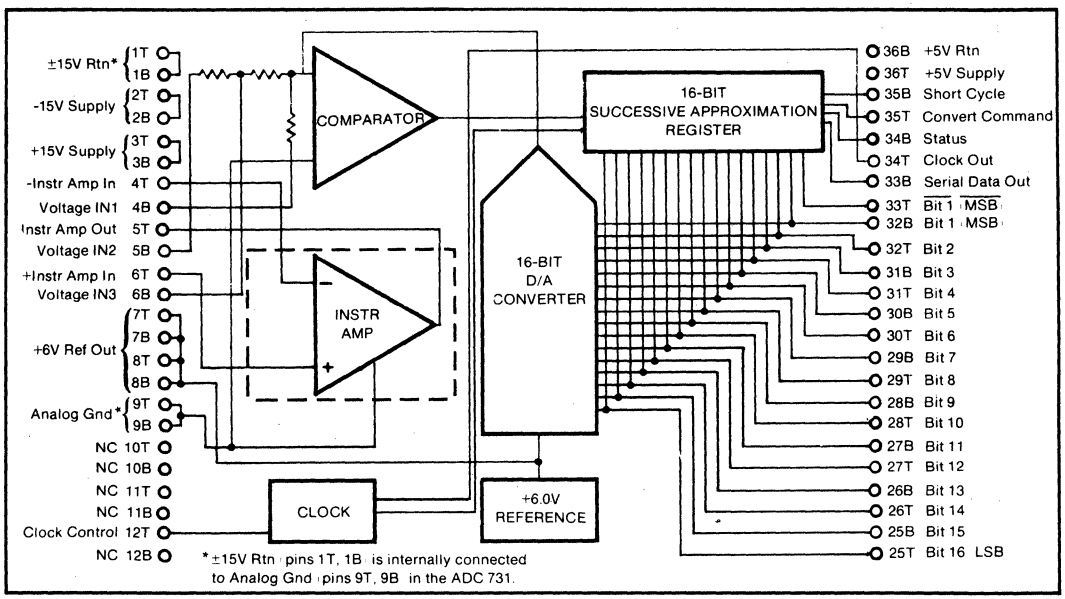
±15V Return(1)	1B	1T	±15V Return(1)	Bit 15	25B	25T	Bit 16 (LSB)
-15V Supply	2B	2T	-15V Supply	Bit 13	26B	26T	Bit 14
+15V Supply	3B	3T	+15V Supply	Bit 11	27B	27T	Bit 12
IN1	4B	4T	-Instr Amp Input	Bit 9	28B	28T	Bit 10
IN2	5B	5T	Instr Amp Output (ADC731 only(3))	Bit 7	29B	29T	Bit 8
IN3	6B	6T	+Instr Amp Input	Bit 5	30B	30T	Bit 6
NC(2)	7B	7T	NC(2)	Bit 3	31B	31T	Bit 4
+6V Ref Out	8B	8T	+6V Ref Out	Bit 1 (MSB)	32B	32T	Bit 2
Analog Gnd(1)	9B	9T	Analog Gnd(1)	Serial Out	33B	33T	Bit 1 (MSB)
NC	10B	10T	NC	Status Out	34B	34T	Clock Out
NC	11B	11T	NC	Short Cycle	35B	35T	Convert Command
NC	12B	12T	Clock Control	+5V Return	36B	36T	+5V Supply

NOTES:
1. ±15V Return (Pins 1T, 1B) is internally connected to Analog Gnd (Pins 9T, 9B) in ADC731.
2. Internally connected to Pins 8T, 8B.
3. Not internally connected on ADC73 models.

PC BOARD MOUNTING DETAILS (component side)



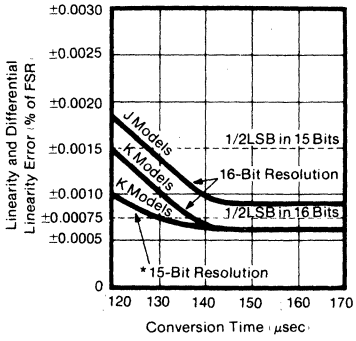
CONNECTION DIAGRAM



*±15V Rtn (pins 1T, 1B) is internally connected to Analog Gnd (pins 9T, 9B) in the ADC 731.

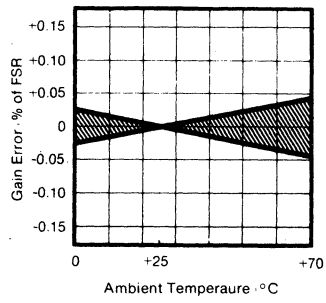
TYPICAL PERFORMANCE CURVES

LINEARITY AND DIFFERENTIAL LINEARITY ERROR VS CONVERSION TIME

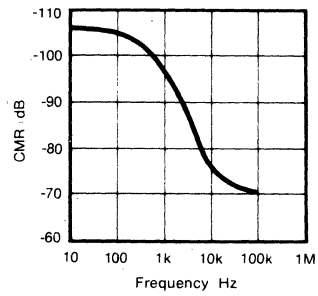


*Short-cycled to 15 Bits

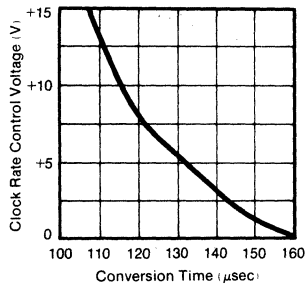
GAIN DRIFT VS AMBIENT TEMPERATURE



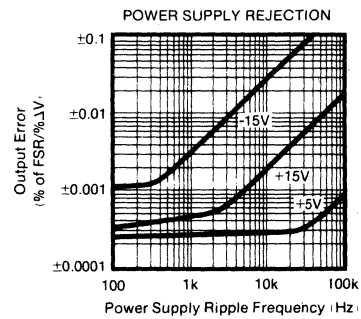
COMMON-MODE REJECTION OF DIFFERENTIAL INPUT BUFFER VS FREQUENCY



CLOCK RATE CONTROL VOLTAGE VS CONVERSION TIME



POWER SUPPLY REJECTION



DISCUSSION OF SPECIFICATIONS AND PERFORMANCE

ACCURACY

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent quantization error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and the scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including gain, offset, linearity, differential linearity, and power supply sensitivity. Initial gain and offset errors are adjusted to zero at the factory prior to shipment. Periodic recalibration may be performed by the user as needed. Gain drift over temperature rotates the transfer characteristic (Figure 1) about the zero or -FS point (all bits OFF) and offset drift shifts the transfer characteristic left or right. The linearity error has also been adjusted to within ±1/2LSB at the factory and, like gain and offset error, is user adjustable. Linearity error is the deviation of an actual bit transition from ideal transition value at any level over the range of the A/D converter. A differential linearity error of ±1/2LSB means that the width of each bit step over the input range of the A/D converter is 1LSB±1/2LSB. The ADC73 and ADC731 are also guaranteed to have no missing codes from +15°C to +35°C.

TIMING CONSIDERATIONS

The timing diagram shown in Figure 2 illustrates by a specific example the timing of the A/D logic. It shows how an analog input voltage is converted to the output digital word 0110 0111 0110 1001.

DEFINITION OF DIGITAL CODES

The user may select one of three available codes for the ADC73 or ADC731 parallel output. They are unipolar straight binary (USB) for unipolar input ranges, bipolar offset binary (BOB), and bipolar two's complement (BTC) for bipolar input voltage ranges. Table I shows the LSB voltage, transition voltages and code definitions for each possible analog input signal range for 14-, 15-, and 16-bit resolutions.

Two serial data output codes are available, USB and BOB. The serial data is available as each bit is being converted with the MSB being output first. The serial data is synchronized with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition voltages shown in Table I also apply to the serial data output except for the BTC code.

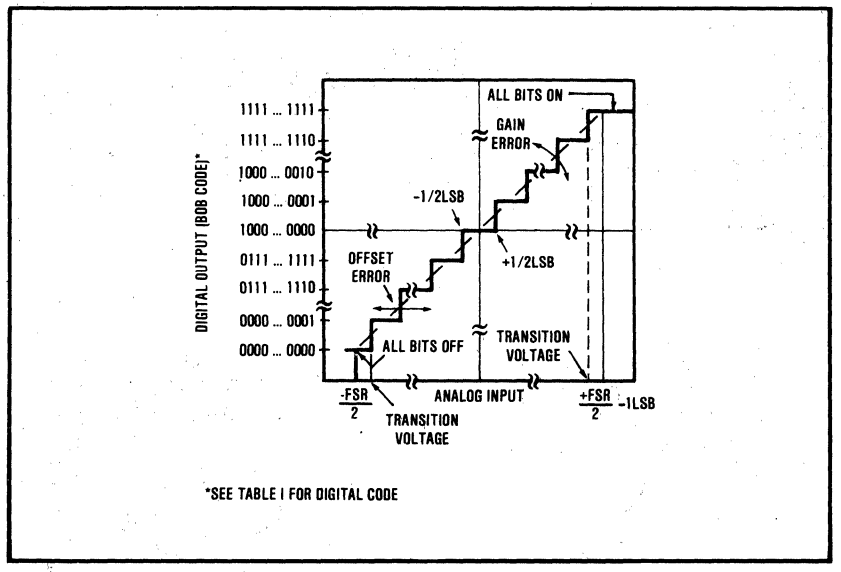
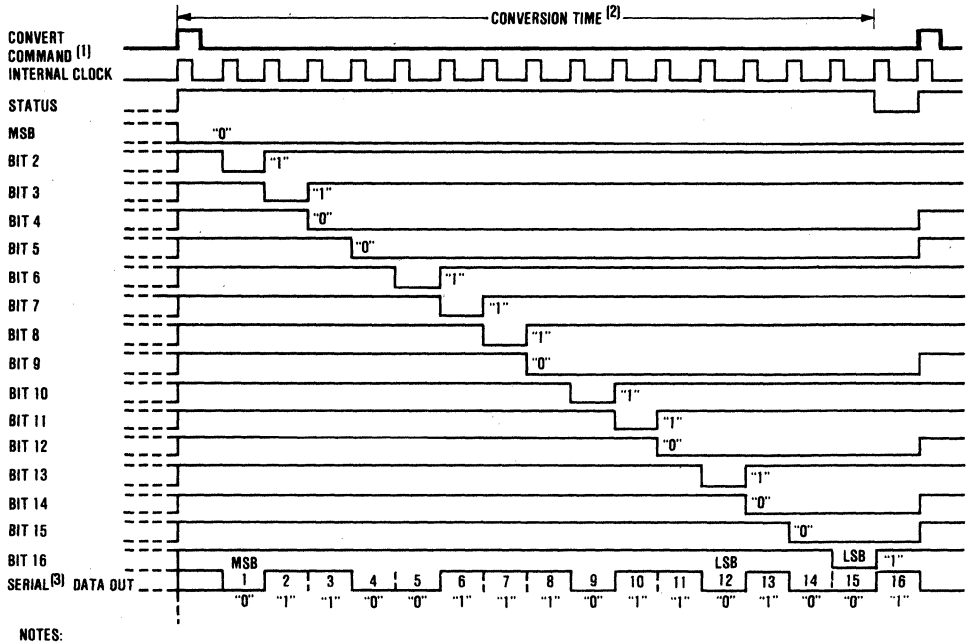


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.



NOTES:
1. The convert command must be at least 200nsec wide. The conversion is initiated by the "leading edge" of the convert command.
2. 170μsec maximum for 16 bits.
3. Use trailing (high to low) edge of clock to strobe each serial output bit.

FIGURE 2. ADC73 731 Timing Diagram.

TABLE I. Input Voltages, Transition Values, LSB Value and Code Definitions.

INPUT VOLTAGE - RANGE AND LSB VALUES					
Analog Input Voltage Range		±10V	±5V	0 to +10V	0 to +20V
Code Designation		BOB(1) or BTC(2)	BOB(1) or BTC(2)	USB(3)	USB(3)
One Least Significant Bit LSB	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 14	1.22mV	610μV	610μV	1.22mV
	n = 15	610μV	305μV	305μV	610μV
	n = 16	305μV	153μV	153μV	305μV
Transition Values(4) MSB LSB					
1111 ... 1111	+Full Scale	+10V-3/2LSB	+5V-3/2LSB	+10V-3/2LSB	+20-3/2LSB
1000 ... 0000	Mid Scale	0±1/2LSB	0±1/2LSB	+5V±1/2LSB	+10±1/2LSB
0000 ... 0000	-Full Scale	-10V+1/2LSB	-5V+1/2LSB	0+1/2LSB	0+1/2LSB

1. BOB = Bipolar Offset Binary
2. BTC = Binary Two's Complement
3. USB = Unipolar Straight Binary
4. Nominal voltages for transition to code specified.

INSTALLATION AND OPERATING INSTRUCTIONS

MOUNTING

Mounting on a printed circuit board is accomplished using the female printed circuit connectors supplied with each A D converter. Mount the A D converter with two #4 external tooth lockwashers and two #4-40 machine screws. Refer to the mounting instructions. Be sure to leave clearance for screwdriver adjustment of the trim potentiometers.

PC LAYOUT CONSIDERATIONS

The metal case (ADC73 and ADC731) is connected internally to the ±15V Rtn pins (1B and 1T). Care must be taken to prevent other printed circuit conductors from making electrical contact with the case. In order to avoid ground loop paths, the case itself should not be connected to any other local power supply returns.

Coupling between digital signal paths and the analog inputs, IN1, IN2, IN3 and +Amp In and -Amp In (ADC731) should be minimized by careful layout separation and or ground plane shielding.

In addition to the power supply connections, other connections to the A D converter should be limited to digital inputs and outputs with a single digital common return path and the analog input.

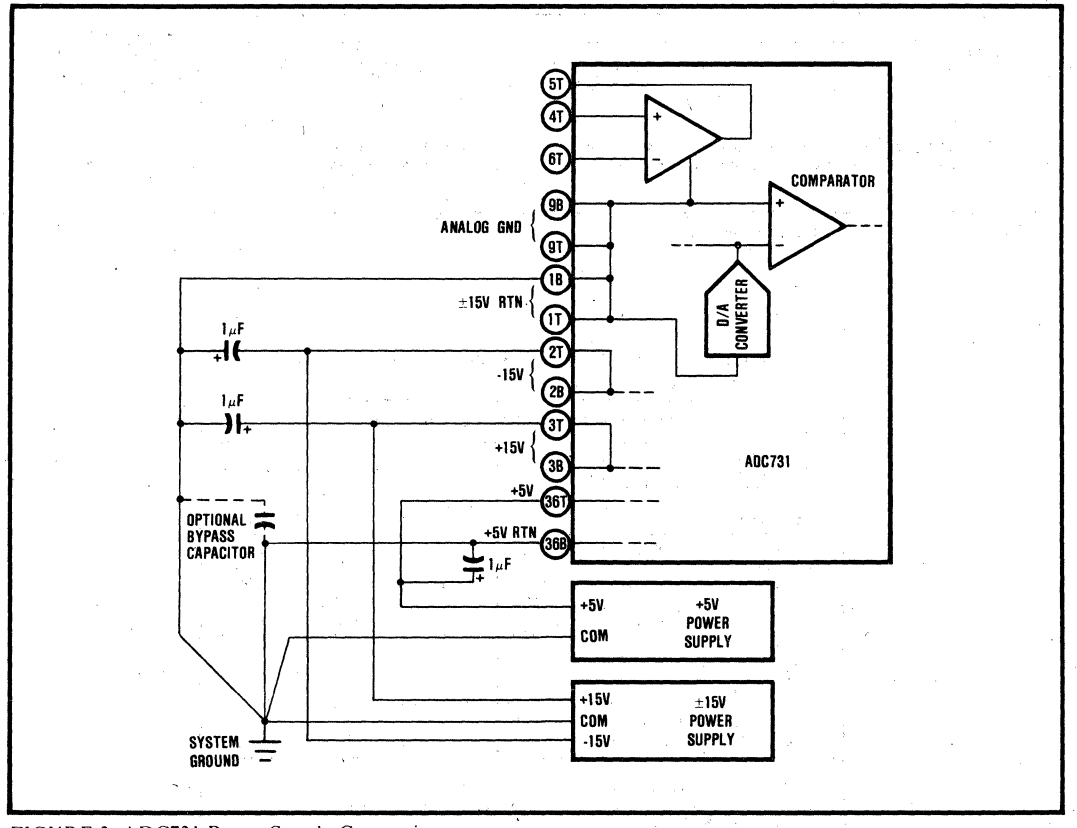


FIGURE 3. ADC731 Power Supply Connections.

POWER SUPPLY CONNECTIONS

ADC731

Analog Gnd (pins 9B, 9T) and ±15V Rtn (pins 1B, 1T) are connected together internally. ±15V Rtn and +5V Rtn (pin 36B) are not connected internally. These supply return lines should be connected together as close to the unit as possible. If ±15V Rtn and +5V Rtn are connected together at a system common point a significant distance from the pins, use a 0.01μF to 0.1μF nonpolarized bypass capacitor between these pins as close to the pins as possible. Refer to Differential Ground Potential Error in Electrical Specification table.

Power supply decoupling capacitors should be used as shown in Figure 3 and located as close as possible to the pins. Use 1μF tantalum or electrolytic capacitors. Parallel electrolytic capacitors with 0.01μF ceramic capacitors for best high frequency decoupling.

ADC73

Analog Gnd and ±15V Rtn pins are not connected internally on this model to permit a separate analog input signal return sense connection. Input signal connections are described in a following section.

Comments made for ADC731 power supply connections also apply to the ADC73. Refer to Figure 4.

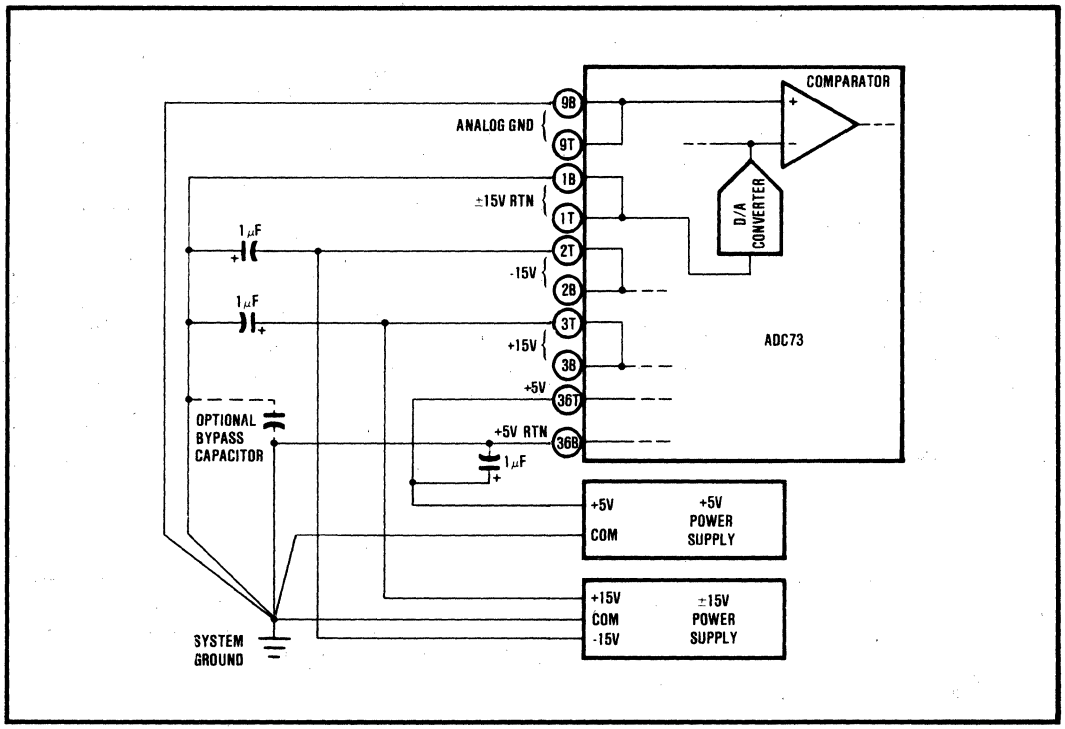


FIGURE 4. ADC73 Power Supply Connections.

SEPARATE POWER SUPPLIES

Because the effectiveness of high resolution A/D converters can be reduced by small amounts of noise, separate floating supplies may be needed for applications in environments with high electrical noise. These supplies and their return paths should be connected to the A/D converter only. Some experimentation with extra shielding and alternative return configurations may be necessary in extreme circumstances.

INPUT CONNECTIONS

ADC73

Analog input signals to ADC73 are connected directly to low impedance inputs (5kΩ and 10kΩ). The user may select unipolar or bipolar, 10V or 20V full scale ranges as illustrated in Figure 5.

ADC731

ADC731 has a precision high impedance differential input buffer. The user may select a unipolar range of 0 to +10V or bipolar ranges of ±5V or ±10V as illustrated in Figure 6. Note that signal input voltage V_{IN} plus the common-mode voltage is limited to ±10V for the bipolar connection and +10V for the unipolar connections.

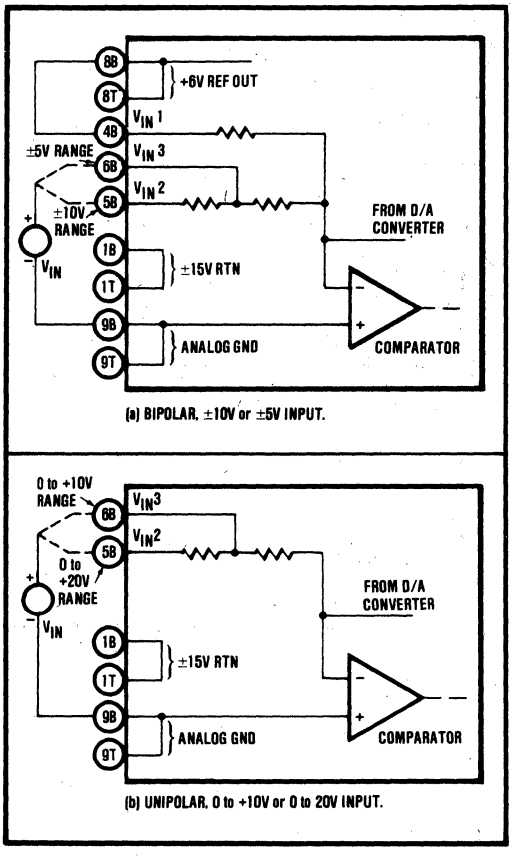


FIGURE 5. Signal Input Connections for ADC73.

CALIBRATION

The relative accuracy of ADC73 and ADC731 is adjusted to within specification at the factory. Offset and Gain may need to be adjusted after the A/D converter is installed and, after extended periods of time, recalibration will be necessary.

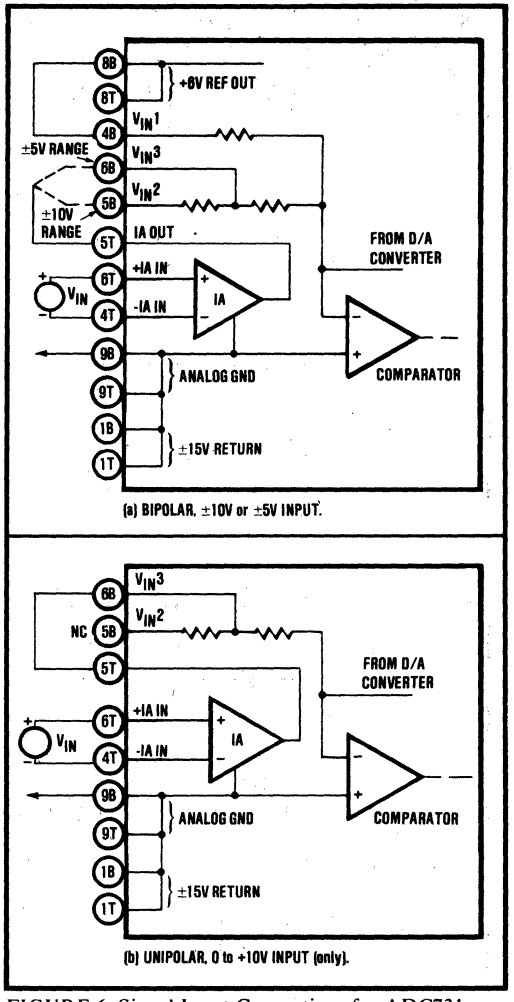


FIGURE 6. Signal Input Connections for ADC731.

Six potentiometers are built into the ADC73 and ADC731 for adjusting Offset (1 potentiometer), Gain (1 potentiometer), and Linearity (4 potentiometers). Linearity is adjusted in the first 4MSB's by adjusting the currents in bits 1(MSB), 2, 3, and 4. Refer to Table II for the transition voltages to be applied to the input appropriate to the input range being used. All input voltages should be set within ±10μV of the ideal voltage.

Procedure for full calibration (Offset, Linearity, and Gain):

1. Set the input voltage to the transition voltage for offset calibration. Adjust the Offset potentiometer until the transition to 0001_{16} from 0000_{16} occurs 50% of the time with repeated conversions.
2. Set the input to the transition voltage for the Gain Cal adjustment listed in Table II. Adjust the Gain potentiometer until the transition to $0FFF_{16}$ from $0FFE_{16}$ occurs 50% of the time with repeated conversions. If bit 4 should turn on such that the codes $1FFF_{16}$ and $1FFE_{16}$ occur, adjust potentiometer labeled bit 4 so that bit 4 (pin 31T) does not turn on.
3. Set the input to the bit 4 transition voltage of Table II. Adjust the potentiometer labeled bit 4 until the transition to 1001_{16} from 1000_{16} occurs 50% of the time with repeated conversions.
4. Set the input to the transition voltage for bit 3. Adjust potentiometer labeled bit 3 until the transition to 2001_{16} from 2000_{16} occurs 50% of the time with repeated conversions.
5. Set the input to the transition voltage for bit 2. Adjust the potentiometer labeled bit 2 until the transition to 4001_{16} from 4000_{16} occurs 50% of the time with repeated conversions.
6. Set the input to the transition voltage for bit 1. Adjust the potentiometer labeled bit 1 until the transition to 8001_{16} from 8000_{16} occurs 50% of the time with repeated conversions.
7. Set the input to the transition voltage for Gain calibration. Adjust the potentiometer labeled Gain until transition to $FFFF_{16}$ from $FFFE_{16}$ occurs 50% of the time with repeated conversions.

If adjusting only Offset and Gain, perform only steps 1 and 7, in that order.

TABLE II. Calibration Values for ADC73 and ADC731.

Input Voltage Range	0 to +10V	0 to +20V	±5V	±10V
POTENTIOMETER ADJUST Transition Codes(1)	**Transition voltages for 16-bit resolution(2)**			
Offset to 0001_{16} from 0000_{16}	0.000076V	0.000153V	-4.99924V	-9.999847V
Gain Cal(3) to $0FFF_{16}$ from $0FFE_{16}$	0.624771V	1.249542V	-4.375229V	-8.750458V
Bit 4 to 1001_{16} from 1000_{16}	0.625076V	1.250153V	-4.374924V	-8.7498747V
Bit 3 to 2001_{16} from 2000_{16}	1.250076V	2.500153V	-3.749924V	-7.499847V
Bit 2 to 4001_{16} from 4000_{16}	2.500076V	5.000153V	-2.499924V	-4.999847V
Bit 1 to 8001_{16} from 8000_{16}	5.000076V	10.000153V	0.000076V	0.000153V
Gain to $FFFF_{16}$ from $FFFE_{16}$	9.999771V	19.999542V	4.999771V	9.999542V

1. Positive true codes, Bipolar Offset Binary or Unipolar Straight Binary.
2. Voltages given are the nominal value for transition to the code shown.
3. This transition code used only prior to linearity error adjustment.

OPTIONAL CONVERSION TIME ADJUSTMENT

ADC73 and ADC731 may be operated at faster or slower conversion rates by connecting the Clock Control pin (12T) to a positive voltage between 0 and +15V as shown in Figure 7. The conversion time range is typically from 120μsec (12T at +15V) to 190μsec (12T tied to +15V Rtn), see Typical Performance Curves. If pin 12T is left open, the conversion time is typically 150μsec. Figure 7 illustrates the circuit used for conversion rate control. The potentiometer is a non-critical component.

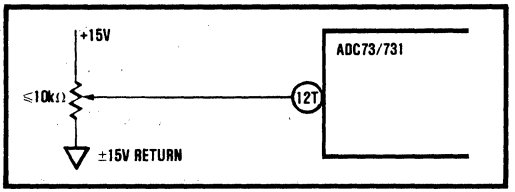


FIGURE 7. Clock Rate Control.

CHANGING RESOLUTION BY SHORT CYCLING

The ADC73 and ADC731 may be short cycled to lower resolutions and higher conversion rates by connecting the Short Cycle pin (35B) to the appropriate bit output as listed in Table III.

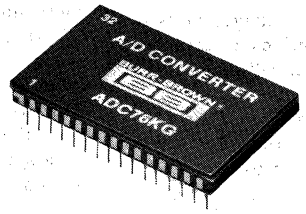
TABLE III. Connections for Short-Cycling Resolution Conversions.

Resolution (bits)	16	15	14	13	12
Connect pin 35B* to	Open	25T	25B	26T	26B
Connect pin 12T to	Open	Open	Open	Open	Open
Typical Conversion Time with pin 12T open · μsec	150	141	132	123	114

*For resolutions less than 16 bits also connect pin 35B through a 2kΩ resistor to +5V.

BURR-BROWN®

ADC76



16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES

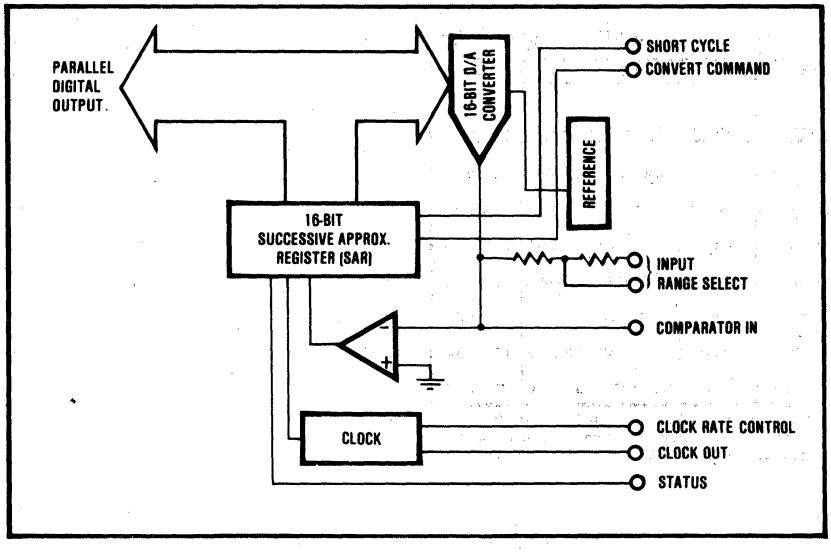
- 16-BIT RESOLUTION
- LINEARITY ERROR ±0.003% MAX (KG)
- COMPACT DESIGN
  32-Pin Ceramic Package
- LOW COST
- 15μsec CONVERSION TIME (14-BIT)

DESCRIPTION

The ADC76 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a convenient 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, and thin-film scaling resistors, which allows selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel form with corresponding clock and status output. All digital inputs and outputs are DTL/TTL compatible.

Power supply voltages are ±15VDC and +5VDC.



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THEORY OF OPERATION

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC76 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that this converter will have no missing codes over a specified temperature range when short cycled for 14-bit operation.

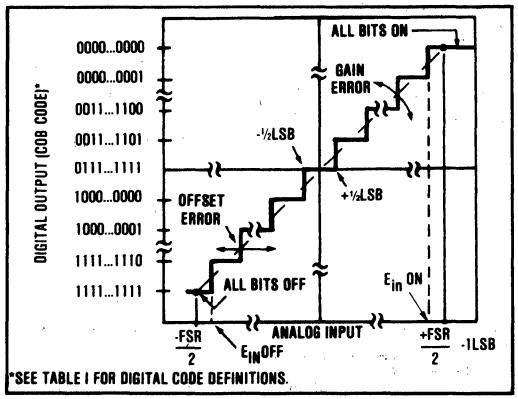


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output).

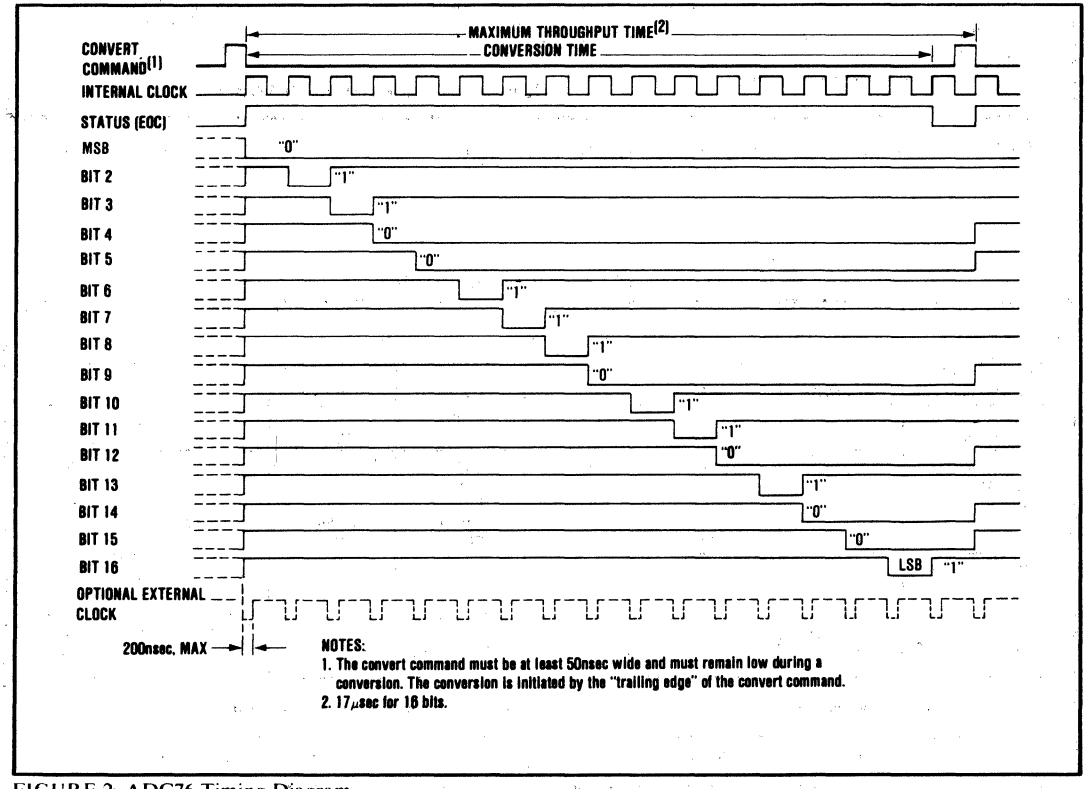


FIGURE 2. ADC76 Timing Diagram.

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC76 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

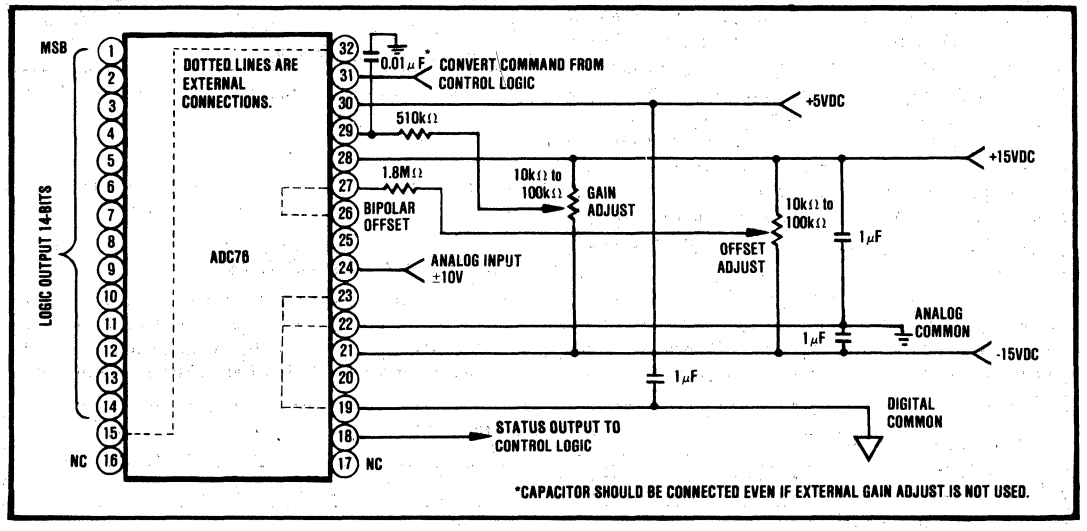


FIGURE 3. ADC76 Connections For: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

(1)COB = Complementary Offset Binary

(2)CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB (pin 1).

(3)CSB = Complementary Straight Binary

(4)Voltages given are the nominal value for transition to the code specified.

SPECIFICATIONS

ELECTRICAL

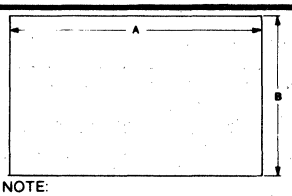
At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC76KG			ADC76JG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
ANALOG INPUTS							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL INPUTS(1)							
Convert Command	Positive pulse 50nsec wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading		1				1	TTL Load
External Clock	Negative pulse 100-200nsec wide. Frequency < internal clock(2)						
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(3)		±0.1	±0.2		±0.1	±0.2	%
Offset Error							
Unipolar(3)		±0.05	±0.1		±0.05	±0.1	% of FSR(4)
Bipolar(3)		±0.1	±0.2		±0.1	±0.2	% of FSR
Linearity Error			±0.003			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
Noise (3σ, p-p)		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0.003		% of FSR/%Vs
+5VDC		0.001			0.001		% of FSR/%Vs
CONVERSION TIME(5) (14 Bits)			15			15	μsec
WARM-UP TIME	5			5			min
DRIFT							
Gain			±15			±15	ppm/°C
Offset							
Unipolar		±2	±4		±2	±4	ppm of FSR/°C
Bipolar			±10			±10	ppm of FSR/°C
Linearity		±2	±3		±2	±3	ppm of FSR/°C
No Missing Codes Temp Range							
KG (14-bit)	+10		+40				°C
JG (13-bit)				0		50	°C
OUTPUT							
DIGITAL DATA							
(All codes complementary)							
Output Codes(6)							
Unipolar		CSB			CSB		
Bipolar		COB, CTC(7)			COB, CTC(7)		
Output Drive			2			2	TTL Loads
Status	Logic "1" during conversion			Logic "1" during conversion			
Status Output Drive			2			2	TTL Loads
Internal Clock							
Clock Output Drive			2			2	TTL Loads
Frequency(8)	933		1400	933		1400	kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		1.55			1.55		W
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+45			+45		mA
Supply Drain -15VDC		-35			-35		mA
Supply Drain +5VDC		+70			+70		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (derated specs)	-25		+85	-25		+85	°C
Storage	-55		+125	-55		+125	°C

NOTES:
1. DTL/TTL compatible, i.e., Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V, max, Logic "1" = 2.4V, min.
2. See External Clock operating instructions.
3. Adjustment to zero. See "Optional External Gain and Offset Adjustment" section.
4. FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR.
5. Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15 (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor.
6. See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.
7. CTC coding obtained by inverting MSB (pin 1).
8. Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 12 and 13 and Table III.

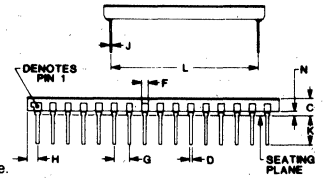
MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89



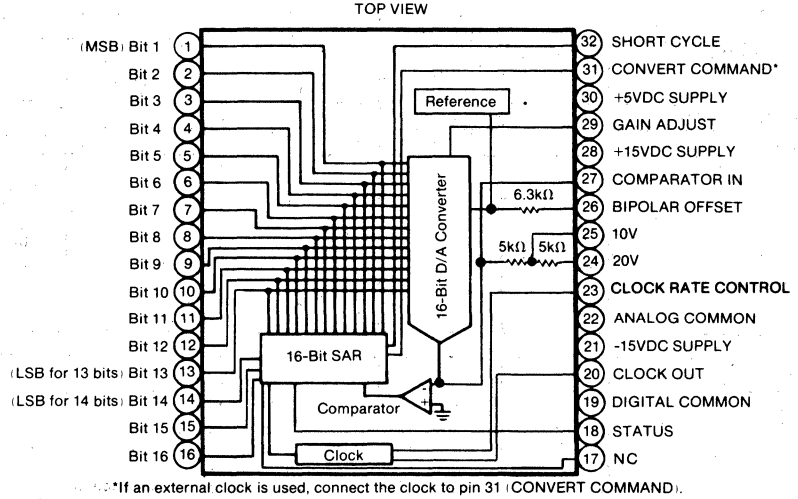
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



CASE: Ceramic
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams (0.46 oz.)
HERMETICITY: Conforms to method 1014 condition C step 1 fluorocarbon of MIL-STD-883 gross leak.

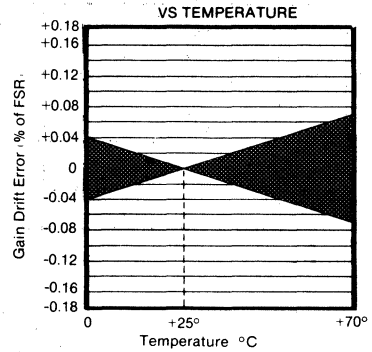
CONNECTION DIAGRAM



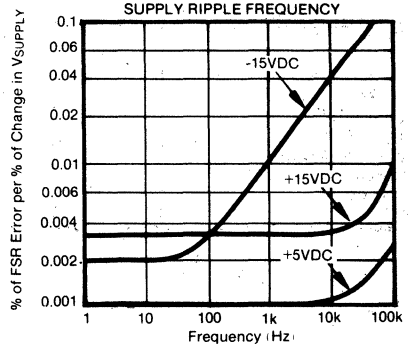
*If an external clock is used, connect the clock to pin 31 (CONVERT COMMAND).

TYPICAL PERFORMANCE CURVES

GAIN DRIFT ERROR (% OF FSR) VS TEMPERATURE



POWER SUPPLY REJECTION VS SUPPLY RIPPLE FREQUENCY



DISCUSSION OF SPECIFICATIONS

The ADC76 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 7 and 8.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. The ADC76 power supply sensitivity is specified at ±0.003% of FSR/%V_S for the ±15V supplies and ±0.0015% of FSR/%V_S for the +5V supply. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 5.

LINEARITY ERROR

Linearity error is not adjustable and is the most meaningful indicator of A/D converter accuracy. Linearity is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential linearity describes the step size between transition values. A differential linearity error of ±0.003% of FSR indicates that the size of any step may not vary from the ideal step size by more than 0.003% of Full Scale Range.

ACCURACY VERSUS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC76 are shown in Figure 4.

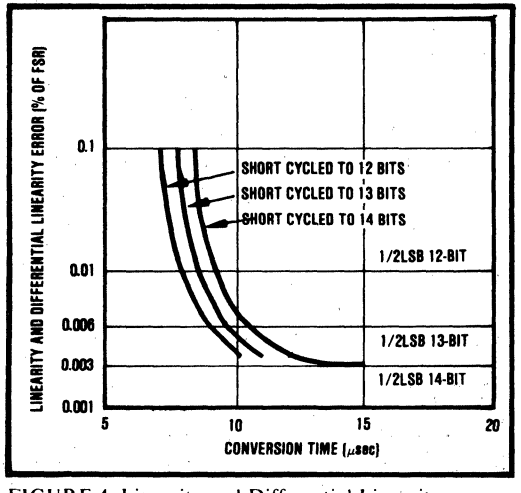


FIGURE 4. Linearity and Differential Linearity Versus Conversion Time.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC76, but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 5 to obtain noise free operation. These capacitors should be located close to the ADC.

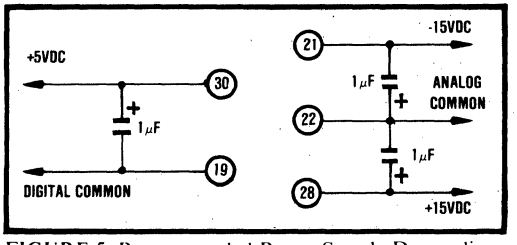


FIGURE 5. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 6 for circuit details.

TABLE II. ADC76 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB (pin 1).

OUTPUT DRIVE

Normally all ADC76 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

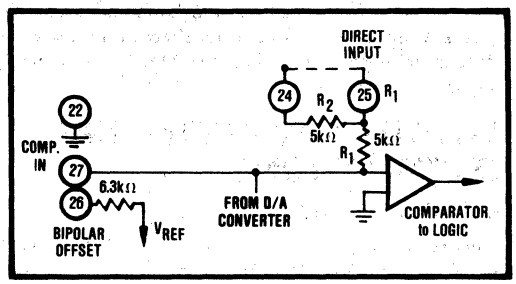


FIGURE 6. ADC76 Input Scaling Circuit.

INPUT IMPEDANCE

The input signal to the ADC76 should be a low impedance, such as the output of an op amp to avoid any errors due to the relatively low input impedance of the ADC76.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the ADC76 as shown in Figure 7.

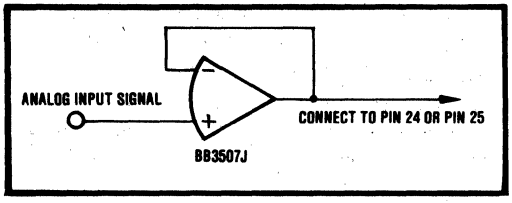


FIGURE 7. Source Impedance Buffering.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 8 and 9. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

Offset - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 8. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

Gain - Connect the Gain adjust potentiometer as shown in Figure 9. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

Table I details the transition voltage levels required.

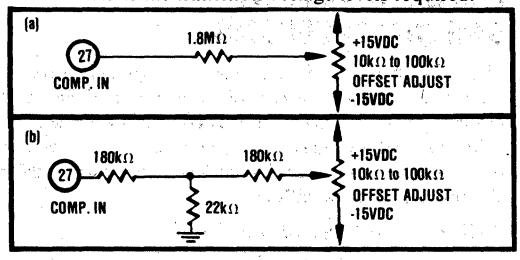


FIGURE 8. Two Methods of Connecting Optional Offset Adjust.

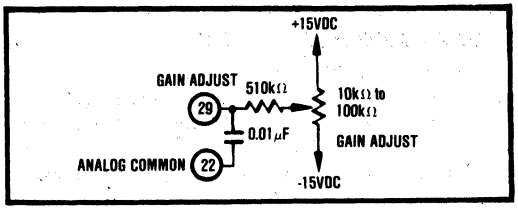


FIGURE 9. Connecting Optional Gain Adjust.

EXTERNAL CLOCK

If an external clock is used, connect the external clock to Convert Command, pin 31. The convert command shown in Figure 2 is not used. After each conversion is completed, a new conversion cycle will automatically start on the first falling edge of the external clock following the completion of conversion. The clock out signal will remain as shown in Figure 2 even if an external clock is used. The external clock pulse must be a negative going pulse with a width between 100nsec and 200nsec as shown in Figure 2, and must be at a lower frequency than the internal clock. The circuit in Figure 10 shows a simple technique for generating a clock signal with the required duty cycle from an external clock with an arbitrary duty cycle. The external clock must operate at a lower frequency than the internal clock for proper operation. This should not present a problem since the frequency of the internal clock can be increased to any desired value by using the Clock Rate Control, pin 23. Figure 11 shows a conversion using a continuous external clock.

OPTIONAL CONVERSION TIME ADJUSTMENT

The ADC76 may be operated with faster conversion times for resolutions less than 14 bits by connecting the Clock Rate Control (pin 23) and the Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

TABLE III. Short Cycle and Clock Rate Control Connections for 12- to 16-Bit Resolutions.

Resolution (Bits)	16	15	14	13	12
Connect Pin 32* to	Open	Pin 16	Pin 15	Pin 14	Pin 13
Connect Pin 23 to	Pin 19	Pin 19	Pin 19	Pin 30	Pin 30
Typical Conversion Time	17μsec	16μsec	15μsec	10μsec	8μsec

*For resolutions less than 16 bits also connect a 2kΩ resistor from +5V to pin 32.

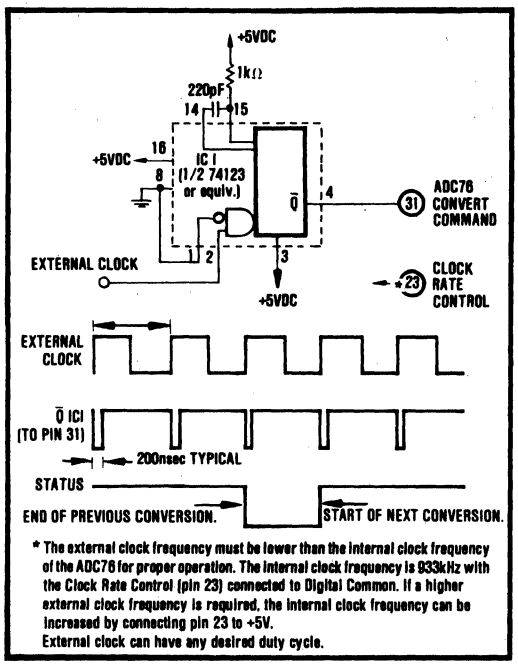


FIGURE 10. Continuous Conversion Using External Clock With Arbitrary Duty Cycle.

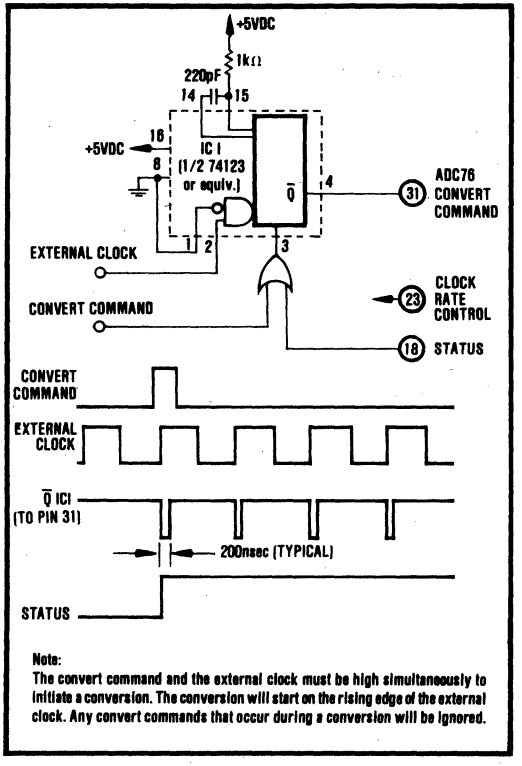


FIGURE 11. Conversion Initiated by Convert Command Using Continuous External Clock.

If a more precise adjustment of conversion time is desired than can be obtained by simply connecting the Clock Rate Control (pin 23) to Digital Common or +5V, as indicated in Table III, the Clock Rate Control may be connected to an external multiturn trim potentiometer with a TCR of ±100ppm/°C or less as shown in Figure 12. The typical conversion time versus the Clock Rate Control voltage is shown in Figure 13. The effect of

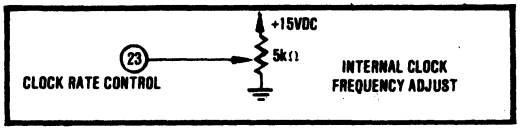


FIGURE 12. Clock Rate Control, Optional Fine Adjust.

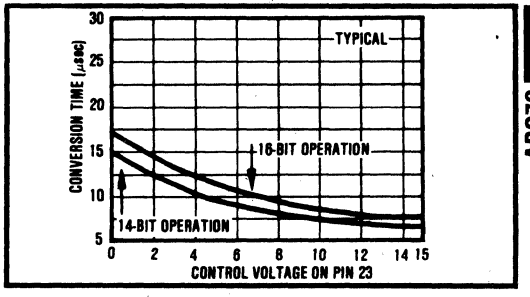


FIGURE 13. Conversion Time vs Clock Rate Control Voltage.

varying the conversion time and the resolution on Linearity Error and Differential Linearity Error is shown in Figure 4.

HEAT DISSIPATION

The ADC76 dissipates approximately 1.8 watts (typical) and the packages have a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above 70°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 14 for θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square inch (minimum) area, this technique will allow operation to +85°C.

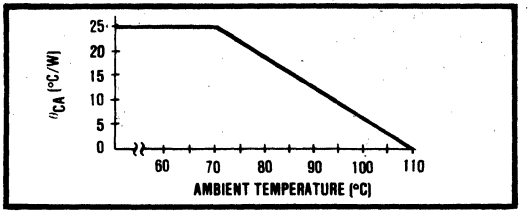


FIGURE 14. θ_{CA} Requirement Above 70°C.

BURR-BROWN®

ADC80

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **COMPACT DESIGN - Self-contained with internal clock, comparator, and reference**

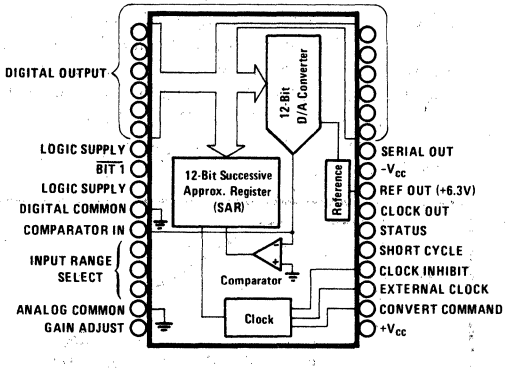
  32-pin ceramic package

- **FAST CONVERSION SPEEDS**
  Provide fast signal sampling rates
  12-bits - 25μsec, 10-bits - 21μsec
  Faster conversion speeds obtainable with "Short-Cycling" and optional external clock

- **LOW COST**

- **WIDE SUPPLY RANGE - Will operate with ±11.4V to ±16V supplies (Z models)**

FUNCTIONAL DIAGRAM



DESCRIPTION

The Model ADC80AG-10 and ADC80AG-12 are 10-and 12-bit successive approximation A D converters. They utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a compact 32-pin ceramic package.

Complete with internal reference, the ADC80 offers versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V.

Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.0122% (±1 2LSB). The model ADC80 is specified for -25°C to +85°C operation.

Th fast conversion speeds of 25μsec for 12-bit and 21μsec for 10-bit resolution make the ADC80 excellent for a wide range of applications where system throughput sampling rates from 40kHz to 47kHz are required. In addition, the ADC80 may be short-cycled and an external clock may be used to obtain faster.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Two power supply ranges are available: ±15V and ±12V (Z models). A +5V logic supply is also required.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A D converter are combinations of analog errors due to the linear circuitry, matching, and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC80 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. A monotonic converter

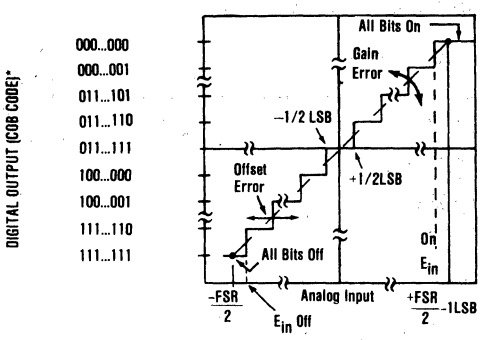


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

*See Table I for digital code definitions.

can have missing codes; therefore, Burr-Brown specifies no missing codes over a temperature range.

TIMING CONSIDERATIONS

The timing diagram of the ADC80 (Figure 2) assumes an analog input such that the positive true digital word 1001-1000 1001 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110) is the digital output.

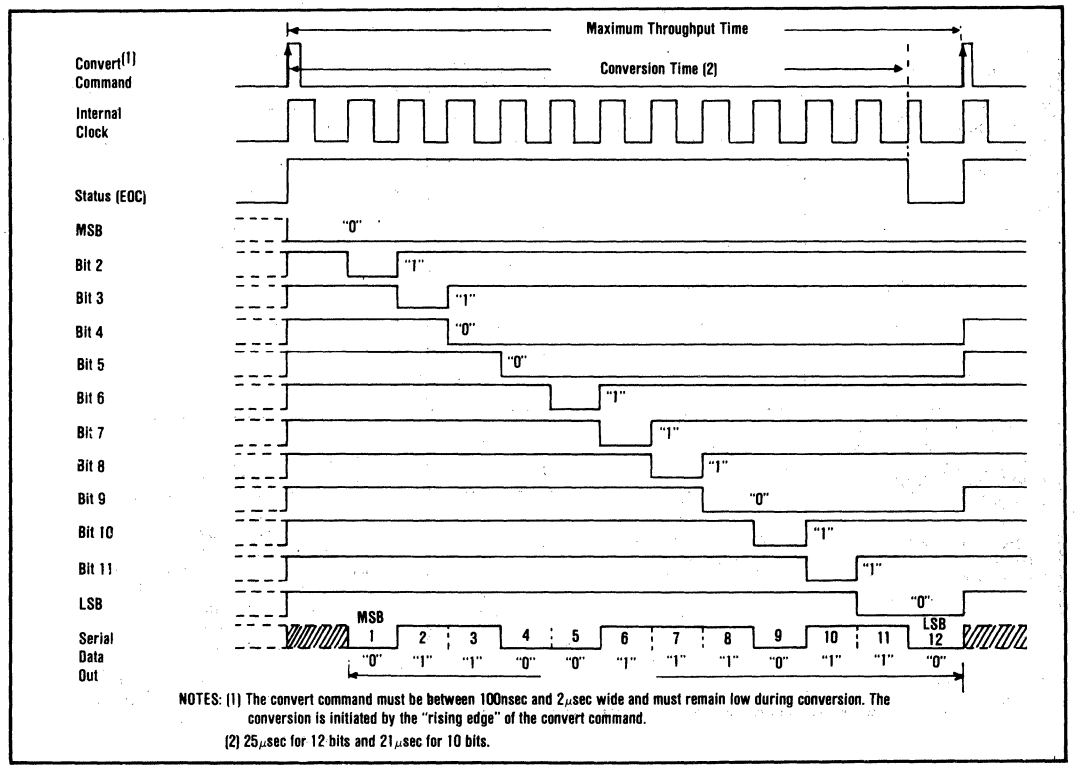


FIGURE 2. ADC80 Timing Diagram.

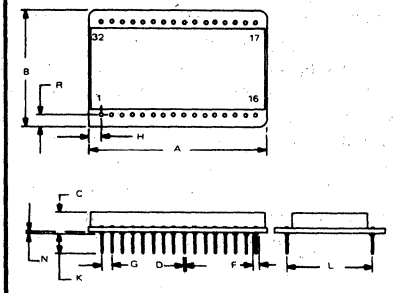
SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated power supplies unless otherwise noted.

MODEL	ADC80AGZ-12 ADC80AG-12	ADC80AGZ-10 ADC80AG-10	UNITS
RESOLUTION	12	10	Bits
INPUT			
ANALOG INPUTS			
Voltage Ranges - Bipolar	±2.5, ±5, ±10		V
- Unipolar	0 to +5, 0 to +10		V
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5		kΩ
0 to +10V, ±5V	5		kΩ
±10V	10		kΩ
DIGITAL INPUTS(1)			
Convert Command	Positive Pulse 100nsec Wide (min) 2μsec Wide (max).		
Logic Loading	1		TTL Load
External Clock	1		TTL Load
TRANSFER CHARACTERISTICS			
ERROR			
Gain Error(2)	±0.1		%
Offset Error(2) - Unipolar	±0.05		% of FSR(3)
- Bipolar	±0.1		% of FSR
Linearity Error, max(4)	±0.012	±0.048	% of FSR
Inherent Quantization Error	±1/2		LSB
Differential Linearity Error	±1/2		LSB
No Missing Codes Temp. Range	0 to +70	0 to +70	°C
Power Supply Sensitivity			
±15V	±0.0030		% of FSR/%V_S
+5V	±0.0015		% of FSR/%V_S
DRIFT			
Specification Temperature Range	-25 to +85		°C
Total Accuracy, Bipolar, max(5)	±23		ppm/°C
Gain, max	±30		ppm/°C
Offset - Unipolar	±3		ppm of FSR/°C
Bipolar, max	±15		ppm of FSR/°C
Linearity, max	±3		ppm of FSR/°C
Monotonicity	GUARANTEED		
CONVERSION SPEED (max)(6)	25	22	μsec
OUTPUT			
DIGITAL DATA			
(all codes complementary)			
Parallel			
Output Codes(7) - Unipolar	CSB		
- Bipolar	COB, CTC		
Output Drive	2		TTL Loads
Serial Data Codes (NRZ)	CSB, COB		
Output Drive	2		TTL Loads
Status	Logic "1" during conversion		
Status Output Drive	2		TTL Loads
Internal Clock			
Clock Output Drive	2		TTL Loads
Frequency(8)	500		kHz
INTERNAL REF. VOLTAGE	6.3		V
Max. External Current (with no degradation of specifications)	200		μA
Tempco of Drift, max	±20		ppm/°C
POWER REQUIREMENTS			
Rated Voltages	±15, +5		V
Z models	±12, +5		V
Range for Rated Accuracy	4.75 to 5.25 and ±14.0 to ±16.0		V
Z models	4.75 to 5.25 and ±11.4 to ±16.0		V
Supply Drain +15V or +12V	+20		mA
-15V or -12V	-20		mA
+5V	+70		mA
TEMPERATURE RANGE			
Specification	-25 to +85		°C
Operating (derated spec)	-55 to +100		°C
Storage	-55 to +125		°C

MECHANICAL



NOTE: LEADS IN TRUE POSITION WITHIN .010" (.25mm)R @ MMC AT SEATING PLANE.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

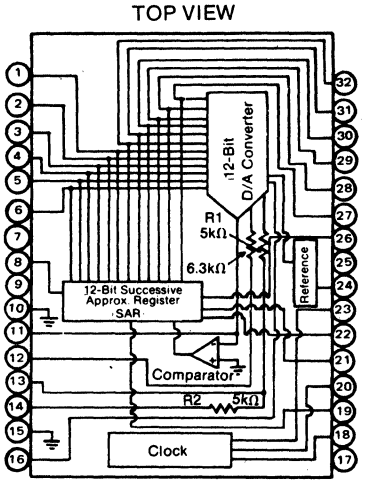
CASE: Ceramic
MATING CONNECTOR: 2302MC - Set of two 16-pin strips $9.40 per set.
WEIGHT: 13 grams 0.46oz.

1. DTL/TTL compatible, i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for inputs and for digital outputs, Logic "0" = +0.4V max and "1" = 2.4V min.
2. Adjustable to zero with external trimpots.
3. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
4. Error shown is the same as ±1/2LSB max for resolution of A/D converter.
5. Includes drift due to linearity, gain, and offset drifts.
6. Conversion time with internal clock.
7. See Table I. CSB - Complementary Straight Binary.
   COB - Complementary Offset Binary.
   CTC - Complementary Two's Complement.
8. For conversion speeds specified.

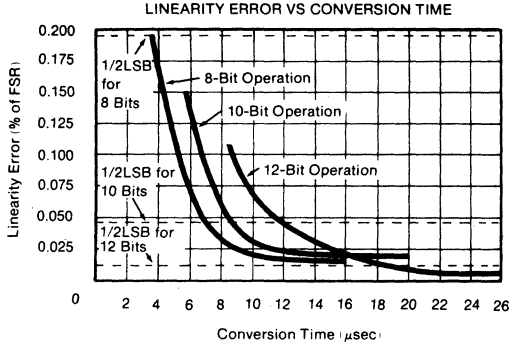
CONNECTION DIAGRAM

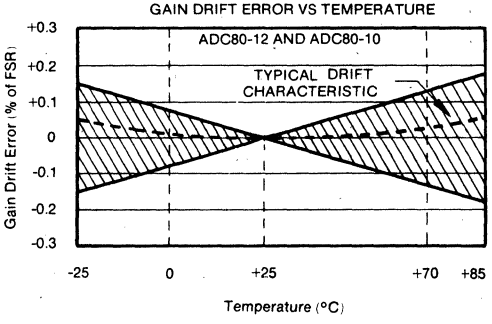
Pin 1 - BIT 6
Pin 2 - BIT 5
Pin 3 - BIT 4
Pin 4 - BIT 3
Pin 5 - BIT 2
Pin 6 - BIT 1 (MSB)
Pin 7 - +5V ANALOG SUPPLY
Pin 8 - $\overline{\text{BIT 1}}$ ($\overline{\text{MSB}}$)
Pin 9 - +5V DIGITAL SUPPLY
Pin 10 - DIGITAL COMMON
Pin 11 - COMPARATOR IN
Pin 12 - BIPOLAR OFFSET
Pin 13 - R1 10V RANGE
Pin 14 - R2 20V RANGE
Pin 15 - ANALOG COMMON
Pin 16 - GAIN ADJUST

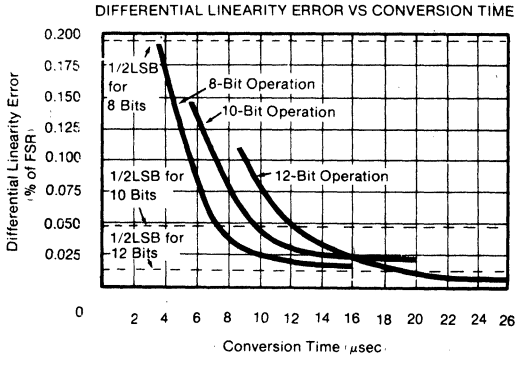
Pin 32 - BIT 7
Pin 31 - BIT 8
Pin 30 - BIT 9
Pin 29 - BIT 10 (LSB-10 BITS)
Pin 28 - BIT 11
Pin 27 - BIT 12 (LSB-12 BITS)
Pin 26 - SERIAL OUT
Pin 25 - -15V OR -12V (Z MODELS)
Pin 24 - REF. OUT (+6.3V)
Pin 23 - CLOCK OUT
Pin 22 - STATUS
Pin 21 - SHORT CYCLE
Pin 20 - CLOCK INHIBIT
Pin 19 - EXTERNAL CLOCK
Pin 18 - CONVERT COMMAND
Pin 17 - +15V or +12V (Z MODELS)

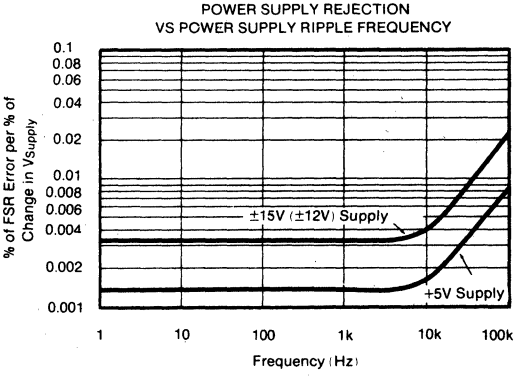


TYPICAL PERFORMANCE CURVES









DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC80 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible ADC80 analog input signal range.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line of the ADC80; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES					
Analog Input Voltage Range	Defined As	±10V	+5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB or CTC*	COB or CTC*	COB or CTC*	CSB**	CSB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000...000***	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V
111...110	-Full Scale	-10V +½LSB	-5V +½LSB	-2.5V +½LSB	0 + ½LSB	0 +½LSB

* COB = Complementary Offset Binary
** CSB = Complementary Straight Binary
*CTC = Complementary Two's Complement - obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
*** Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC80 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A D converter are linearity, drift, gain and offset errors and conversion speed effects on accuracy. The ADC80 is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown on next page.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A D converter accuracy over temperature; they are gain, offset and linearity drift. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1δ errors as follows:

$$RSS = \sqrt{\epsilon g^2 + \epsilon o^2 + \epsilon e^2}$$

where ϵg = gain drift error (ppm °C)
ϵo = offset drift error (ppm of FSR °C)
ϵe = linearity error (ppm of FSR °C)

For unipolar operation, the total RSS drift is ±30.3ppm °C.

ACCURACY VS SPEED

In successive approximation A D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC80 are shown in Typical Performance Curves.

The ADC80 conversion speeds are specified for a maximum linearity error of ±1 2LSB and a differential linearity error of±1 2LSB with the internal clock. Faster conversion speeds up to 23μsec for 12 bits, 12μsec for 10 bits and 6μsec for 8 bits are possible with an external clock.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect the accuracy of the ADC80. The ADC80 power supply sensitivity is specified for ±0.003% of FSR %V_S for ±15V (±12V) supplied for ±0.0015% of FSR/%V_S for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the ADC80. See layout precautions and power supply decoupling on next page.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC80 but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC80. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input and digital lines should be minimized by careful layout. Analog and digital +5V supplies are also not connected internally; they should be connected together at the unit as shown below in Figure 3 (Pins 7 and 9).

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 3 to obtain noise free operation. These capacitors should be located close to the ADC80. 1μF electrolytic type capacitors should be bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

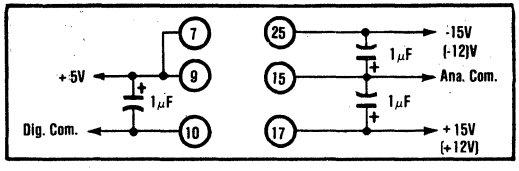


FIGURE 3. Recommended Power Supply Decoupling.

INPUT SCALING

The ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 4 for circuit details.

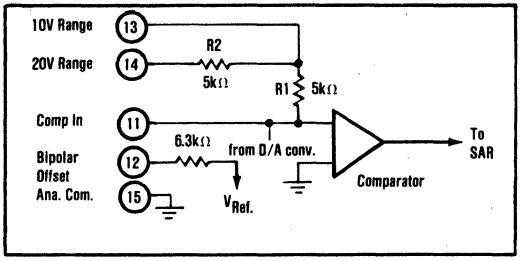


FIGURE 4. ADC80 Input Scaling Circuit.

TABLE II. ADC80 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC80 as shown in Figures 5 and 6. Multiturn potentiometers with 100ppm °C or better TCR's are recommended for maximum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 16 (Gain Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer as shown in Figure 5. Sweep the input through the end point transition voltage that should cause an output transition to all ones.

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all zeros.

Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

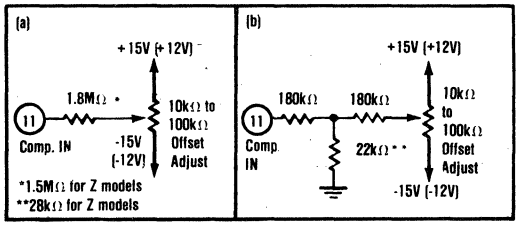


FIGURE 5. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range Adjustment.

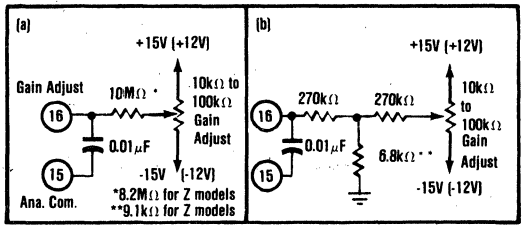


FIGURE 6. Two Methods of Connecting Optional Gain Adjust with a 0.6% Range of Adjustment.

CLOCK OPTIONS

The ADC80 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with nothing more than an inexpensive quad 2-input NAND gate (7400) as shown in Figures 7 through 10.

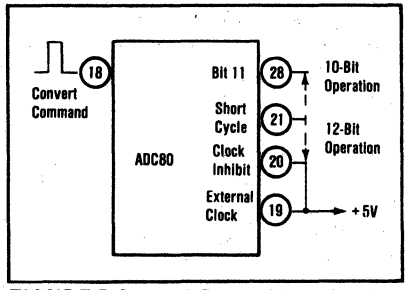


FIGURE 7. Internal Clock - Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

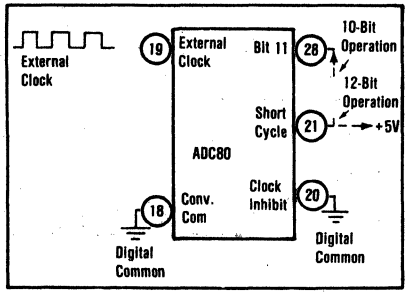


FIGURE 8. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

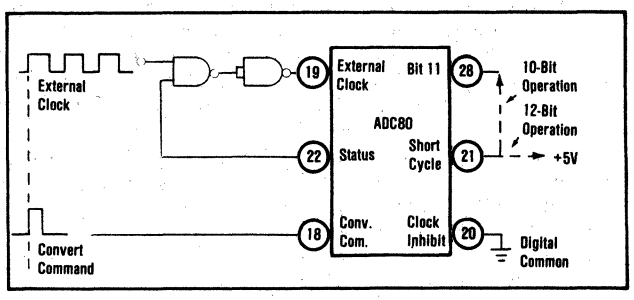


FIGURE 9. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

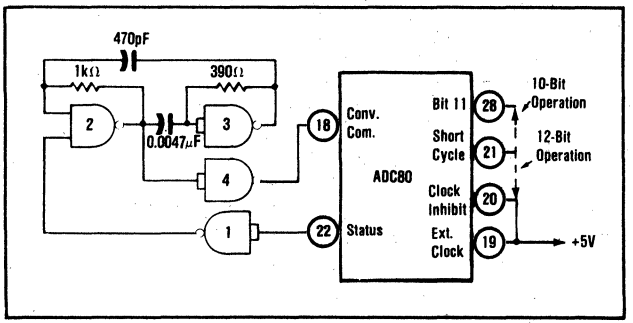


FIGURE 10. Continuous Conversion with Internal Clock. (Conversion is initiated by the 14th clock pulse. Clock runs continuously. The oscillator formed by gates 2 and 3 insures that the conversion process will start when logic power is first turned on.)

SHORT CYCLE FEATURE

The ADC80 may be operated at faster speeds for resolutions less than 10 or 12 bits, depending on the model selected, by connecting the short cycle pin, pin 21, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

TABLE III. Short Cycle Connections and Resolutions for 8- to 12-bit Resolutions - ADC80.

RESOLUTION (BITS)	12	10	8
Connect Pin 21 to	Pin 9	Pin 28	Pin 30
Maximum Conversion Time[1] Internal Clock (μsec) External Clock (μsec)	 25 23	 22 12	 18 6
Maximum Nonlinearity At +25°C (% of FSR)	0.012[2]	0.048[3]	0.20[3]

NOTES: (1) Max conversion time to maintain ±½LSB Nonlinearity error.
(2) 12 Bit Models only.
(3) 10 or 12 Bit Models.

OUTPUT DRIVE

Normally all ADC80 logic outputs will drive 2 standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

APPLICATIONS

LOW COST DATA ACQUISITION SYSTEM

When combined with a sample hold, multiplexer and simplified logic, a 16-channel 12-bit, 25kHz data acquisition system can be built for less than $125.00 parts cost.

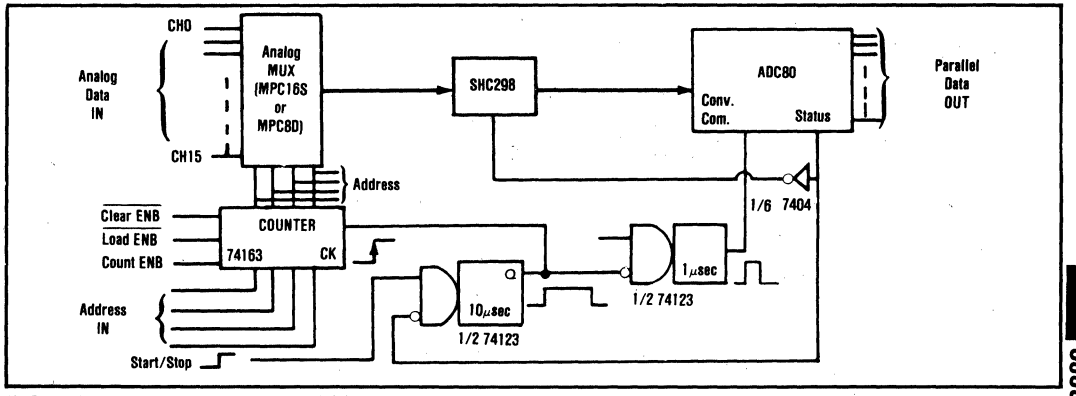


FIGURE 11. Low Cost Data Acquisition System.

ZERO DROOP SAMPLE/HOLD

A zero droop - infinite hold sample hold can be constructed with the ADC80 with the circuit shown in Figure 12. A sample command will cause the relay to switch the analog input to the ADC80 input and also generate a convert command to the ADC80. The sample pulse width (T_A) should be greater than the combined switching and settling time of the relay and driver circuit and the ADC80 conversion time.

In the Hold mode, the analog value can be held indefinitely with zero droop. The period of the first one-shot multivibrator must be equal to or greater than T_R, the switching time of the relay.

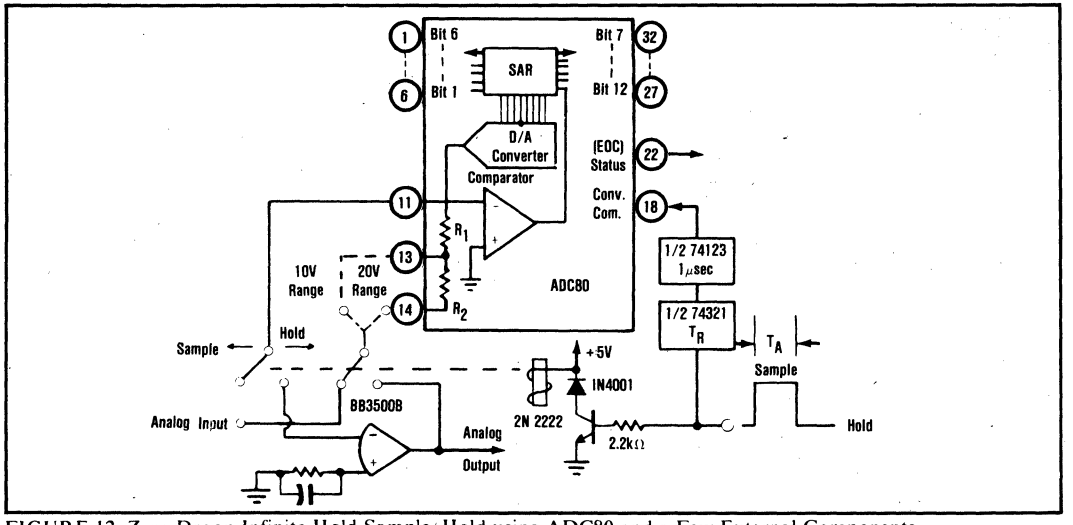


FIGURE 12. Zero Droop Infinite Hold Sample/Hold using ADC80 and a Few External Components.

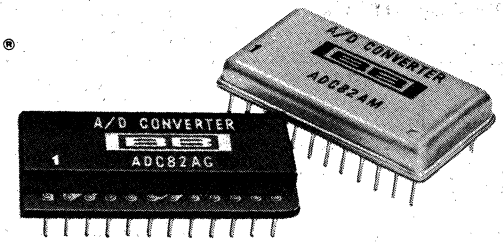
ORDERING INFORMATION

ADC80AG - XX

A D Converter family	Blank - ±14.0V to ±16.0V Supply range	Resolution (No. of Bits)
A = -25°C to +85°C	Z - ±11.4V to ±16.0V supply range	10 = 10 Bits
G = Ceramic Package		12 = 12 Bits

BURR-BROWN®

ADC82



IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **ABSOLUTE ACCURACY - No external gain or offset adjustments are required for 0 to +10V or ±10V signal ranges**
- **PRECISION - ±1/2LSB maximum nonlinearity error**
- **COMPACT DESIGN - 24-pin ceramic or metal dual-in-line package**
- **LOW COST - Ceramic packaged ADC82AG**
- **FAST CONVERSION SPEED - 2.8μsec, max Throughput sampling rates of over 300kHz Faster conversion speeds obtainable with optional external clock**
- **COMPLETELY SELF-CONTAINED - Internal clock, comparator, and reference**

DESCRIPTION

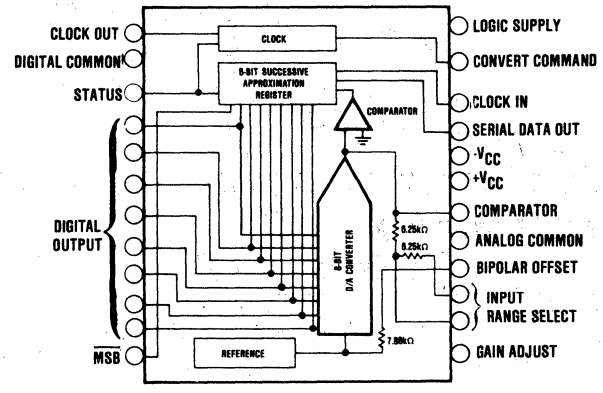
The model ADC82AG and ADC82AG are high-speed, 8-bit successive-approximation A/D converters designed for applications requiring system throughput sampling rates of over 300kHz. They utilize state-of-the-art IC and laser-trimmed thin-film components and are packaged in a 24-pin ceramic (ADC82AG) or metal (ADC82AM) package.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.25V, ±5V, ±10V, 0 to +5, 0 to +10V, or 0 to +20V.

No external adjustments are required to obtain initial absolute accuracies of better than ±1LSB for the 0 to +10V or ±10V signal ranges. Gain and offset errors may be externally trimmed to zero to obtain even greater accuracy.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Power supply voltages are ±15VDC and +5VDC.

FUNCTIONAL DIAGRAM



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DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors, including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC82 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. A monotonic converter can have missing codes; therefore, Burr-Brown specifies no missing codes over a temperature range.

TIMING CONSIDERATIONS

The timing diagram of the ADC82 (see Figure 2) assumes an analog input such that the positive true digital word 10011000 exists. The output will be complementary as shown in Figure 2 (01100111 is the digital output).

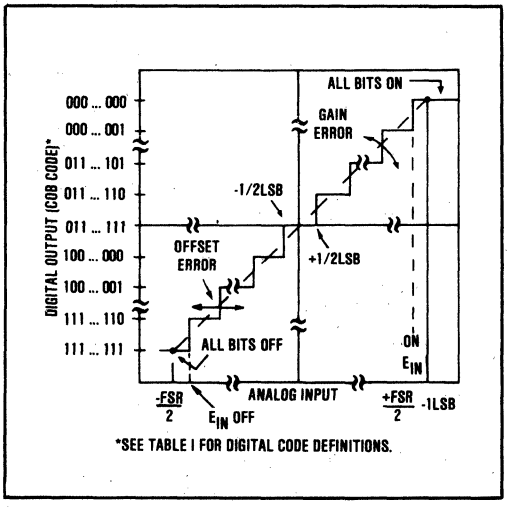


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

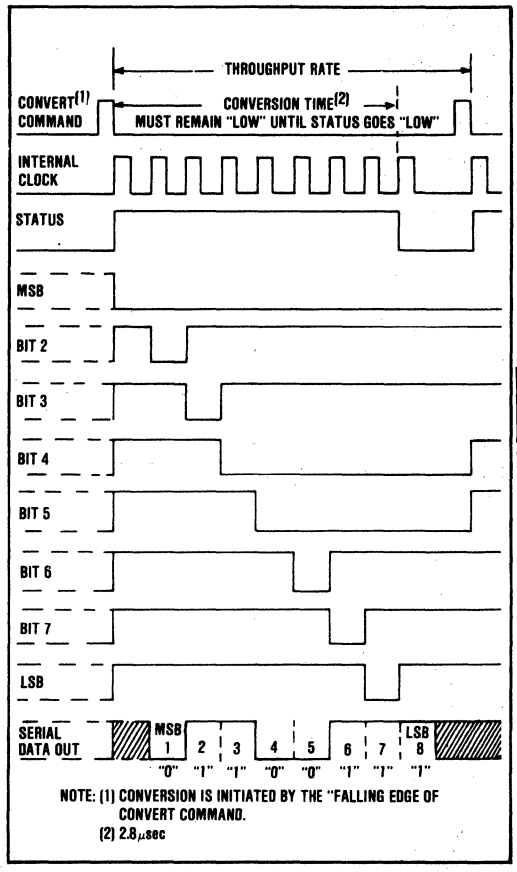


FIGURE 2. ADC82 Timing Diagram.

SPECIFICATIONS

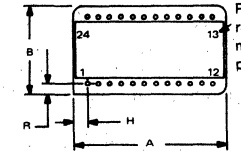
ELECTRICAL

Typical at +25°C and rated power supplies unless otherwise noted.

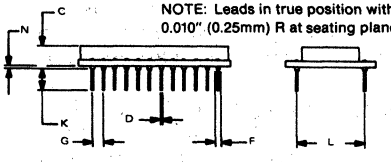
MODEL	ADC82AG ADC82AM	UNITS
RESOLUTION	8	Bits
INPUT		
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5, ±5, ±10	V
Unipolar	0 to +5, 0 to +10, 0 to +20	V
Impedance (Direct Inputs)		
0 to +5V, ±2.5V	3.125	kΩ
0 to +10V, ±5V	6.25	kΩ
0 to +20V, ±10V	12.50	kΩ
DIGITAL INPUTS(1)		
Convert Command	Positive pulse 50nsec wide (min) trailing edge ("1" to "0") initiates conversion	
Logic Loading	1	TTL Load
External Clock	1	TTL Load
TRANSFER CHARACTERISTICS		
ERROR		
Total Accuracy Error, max	±1	LSB
Gain Error(2)	±0.1	%
Offset Error(2)		
Unipolar	±0.05	% of FSR(3)
Bipolar	±0.05	% of FSR
Linearity Error, max(4)	±0.2	% of FSR
Inherent Quantization Error	±1/2	LSB
Differential Linearity Error	±1/2	LSB
No Missing Codes Temp. Range	0 to 70	°C
Power Supply Sensitivity		
+15V	±0.02	% of FSR/%Vs
+5V and -15V	±0.006	% of FSR/%Vs
DRIFT		
Specification Temp. Range	-25 to +85	°C
Gain, max	±40	ppm/°C
Offset		
Unipolar	±20	ppm of FSR°C
Bipolar, max	±35	ppm of FSR°C
Linearity, max	±20	ppm of FSR/°C
Monotonicity	Guaranteed	
CONVERSION SPEED, max(5)	2.8	µsec
OUTPUT		
DIGITAL DATA (All codes complementary)		
Parallel		
Output Codes(6)		
Unipolar	CSB	
Bipolar	COB, CTC	
Output Drive	5	TTL Loads
Serial Data Codes (NRZ)	CSB, COB	
Output Drive	5	TTL Loads
Status	Logic "1" during conversion	
Status Output Drive	5	TTL Loads
Internal Clock		
Clock Output Drive	4	TTL Loads
Frequency(7)	2.85	MHz
POWER REQUIREMENTS		
Rated Voltages	±15, +5	VDC
Range for Rated Accuracy(8)	+4.75 to +5.25, ±14.5 to ±15.5	VDC
Supply Drain, +15VDC	+20	mA
-15VDC	-20	mA
+5VDC	+80	mA
TEMPERATURE RANGE		
Specification	-25 to +85	°C
Storage	-55 to +125	°C

MECHANICAL

ADC82AG



Pin numbers shown for reference only. Numbers may not be marked on package.

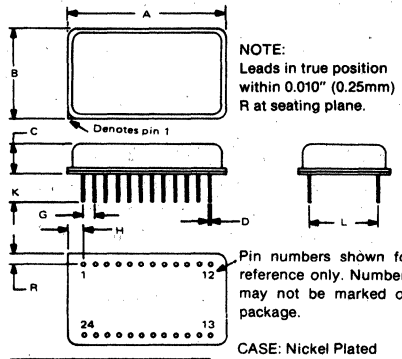


NOTE: Leads in true position within 0.010" (0.25mm) R at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	0.85	.105	2.16	2.67

CASE: Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 7 grams, (0.25 oz).

ADC82AM



NOTE:
Leads in true position within 0.010" (0.25mm) R at seating plane.

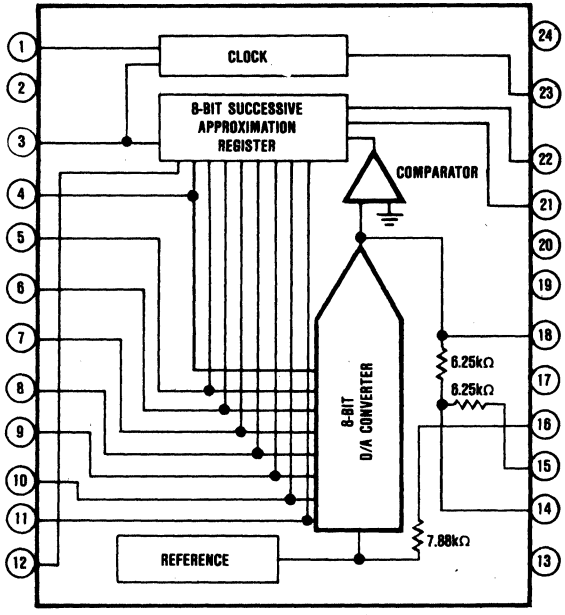
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

CASE: Nickel Plated
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 7 grams, (0.25 oz).

NOTES:
1. DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min.
2. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
3. Adjustable to zero with external trimpots.
4. Error shown is the same as ±1/2LSB max for resolution of A/D converter.
5. Conversion time with internal clock.
6. See Table I. CSB - Complementary Binary.
   COB - Complementary Offset Binary.
   CTC - Complementary Two's Complement.
7. For conversion speeds specified.
8. ±14.0V to ±16.0V for ±1-1/4LSB total accuracy error.

CONNECTION DIAGRAM

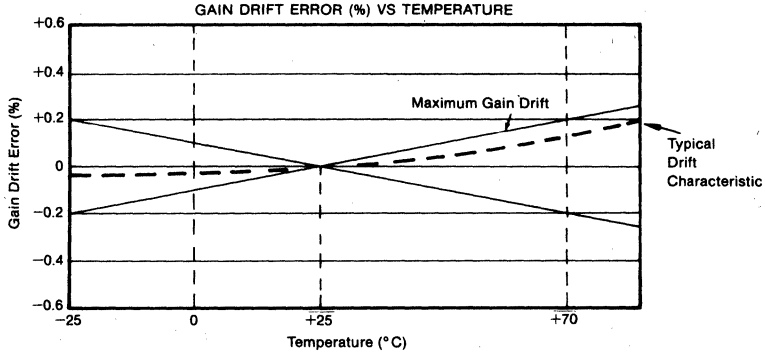


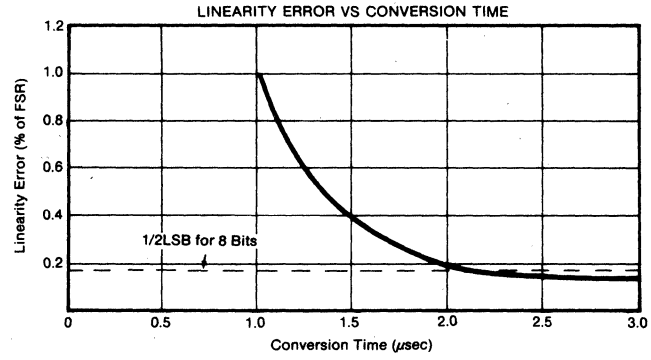
PIN ASSIGNMENTS

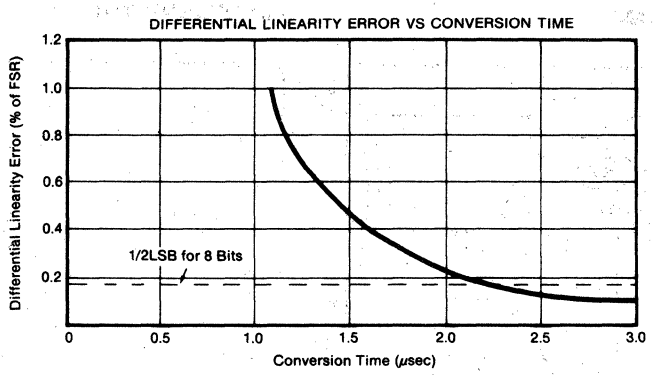
1. Clock Out
2. Digital Common*
3. Status
4. Bit 8 (LSB)
5. Bit 7
6. Bit 6
7. Bit 5
8. Bit 4
9. Bit 3
10. Bit 2
11. Bit 1 (MSB)
12. $\overline{\text{Bit 1}}$ ($\overline{\text{MSB}}$)
13. Gain Adjust
14. R_1 (10V Range)
15. R_2 (20V Range)
16. Bipolar Offset
17. Analog Common
18. Comparator Input
19. +15
20. -15V
21. Serial Out
22. Clock In
23. Convert Command
24. +5V

*Internally connected to case on ADC82AM.

TYPICAL PERFORMANCE CURVES







DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC82 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible ADC82 analog input signal range.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line of the ADC82; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTD code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Ranges	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB or CTC*	COB or CTC*	COB or CTC*	CSB**	CSB**	CSB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV	78.13mV
Transition Values							
MSB LSB							
000 ... 00Ø***	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5 -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 11Ø	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

* COB = Complementary Offset Binary
** CSB = Complementary Straight Binary
*CTC = Complementary Two's complement - obtained by using the complement of the most-significant bit ($\overline{MSB}$). $\overline{MSB}$ is avaliable on pin-12.
***Ø is the Transition Bit. Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC82 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. The ADC82 is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial gain and offset errors are factory trimmed to ±0.05% of FSR at +25°C for both the 0 to +10 and ±10V ranges. No external adjustment is required to obtain initial absolute accuracies of ±1LSB. When using one of the other input signal ranges or when even greater initial accuracy is desired these errors may be trimmed to zero by connecting external potentiometers as shown in Figures 9 and 10.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst-case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\epsilon_g^2 + \epsilon_o^2 + \epsilon_e^2}$$

Where ϵ_g = gain drift error (ppm/°C)
ϵ_o = offset drift error (ppm of FSR/°C)
ϵ_e = Linearity error (ppm of FSR/°C)

For unipolar operation, the total RSS drift is ±49.0ppm/°C and for bipolar operation, the total RSS drift is ±56.8 ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC82 are shown in Typical Performance Curves.

The ADC82 conversion speeds are specified for a maximum linearity error of ±1/2LSB and a differential linearity error of ±1/2LSB with the internal clock. Faster conversion speeds are possible with an external clock (see Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect the accuracy of the ADC82. The ADC82 power supply sensitivity is specified for ±0.006% of FSR/%V_S for -15V and +5V supplies and ±0.02% of FSR/%V_S for +15V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the ADC82. See layout precautions and power supply decoupling below.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC82 but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC82. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 3 to obtain noise free operation. These capacitors should be located close to the ADC82. 1μF electrolytic type capacitors should by bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

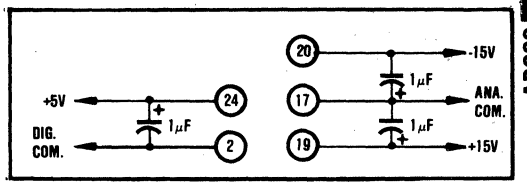


FIGURE 3. Recommended Power Supply Decoupling.

INPUT SCALING

The ADC82 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 4 for circuit details.

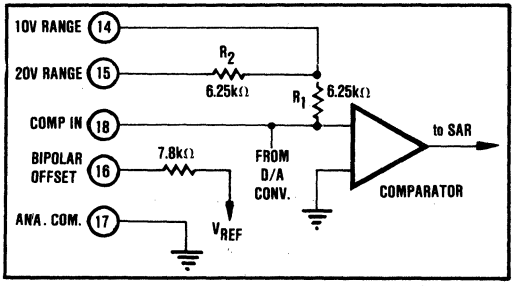


FIGURE 4. ADC82 Input Scaling Circuit.

TABLE II. ADC82 Input Scaling Connection.

Input Signal Range	Output Code	Connect Pin 16 To Pin	Connect Pin 15 To	Connect Input Signal To
±10V	COB or CTC	18	Input Signal	15
±5V	COB or CTC	18	Open	14
±2.5V	COB or CTC	18	Pin 18	14
0 to +5V	CSB	17	Pin 18	14
0 to +10V	CSB	17	Open	14
0 to +20V	CSB	17	Input Signal	15

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

CLOCK OPTIONS

The ADC82 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with nothing more than an inexpensive quad 2-input NAND Gate (7400) as shown in Figure 5 through 8.

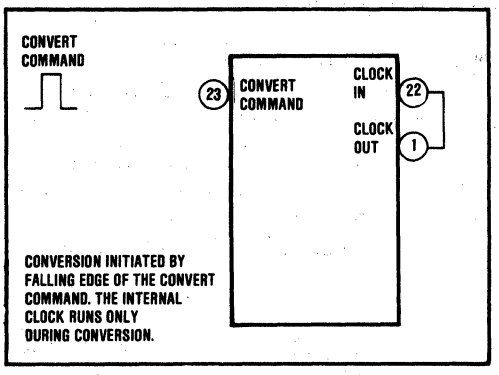


FIGURE 5. Internal Clock-Normal Operating Mode.

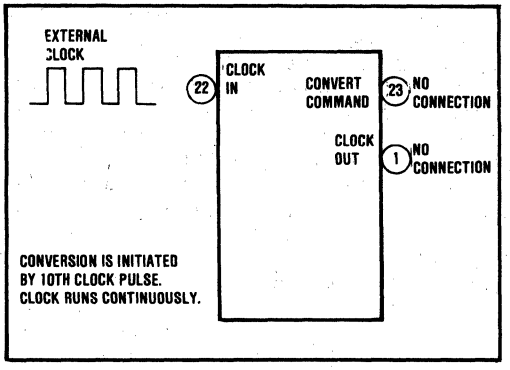


FIGURE 6. Continuous Conversion with External Clock.

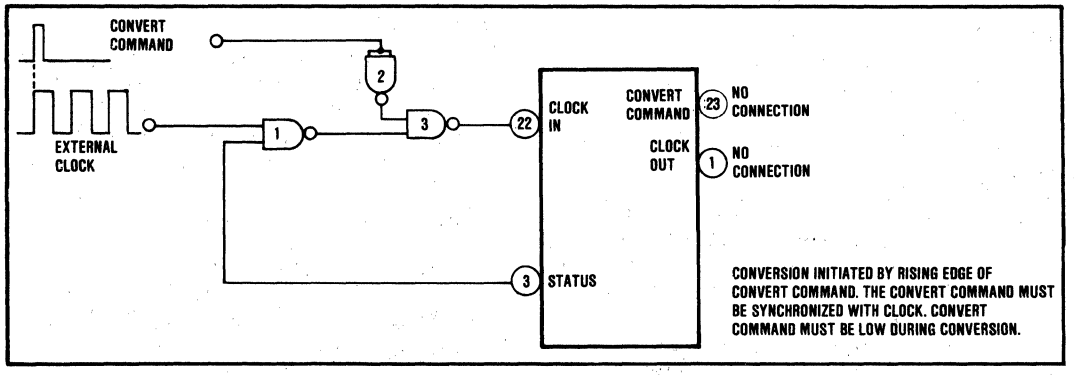


FIGURE 7. Continuous External Clock.

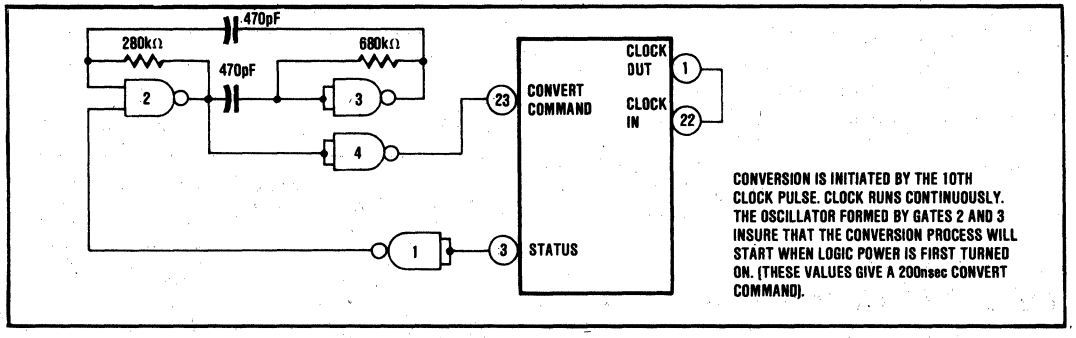


FIGURE 8. Continuous Conversion with Internal Clock.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC82 as shown in Figures 9 and 10. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 13 (Gain Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

Offset - Connect the Offset potentiometer as shown in Figure 9. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

Gain - Connect the Gain adjust potentiometer as shown in Figure 10. Sweep the input through the end point transition voltage that should cause output transitions to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

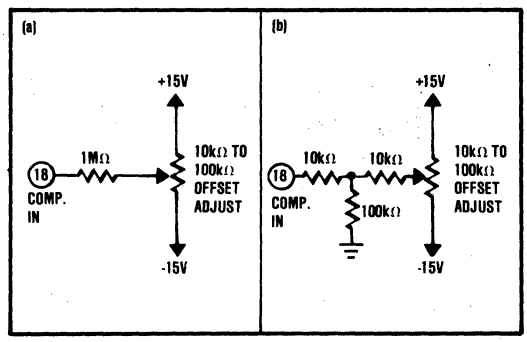


FIGURE 9. Two methods of Connecting Optional Offset Adjust with a ±1.0% of FSR Range of Adjustment.

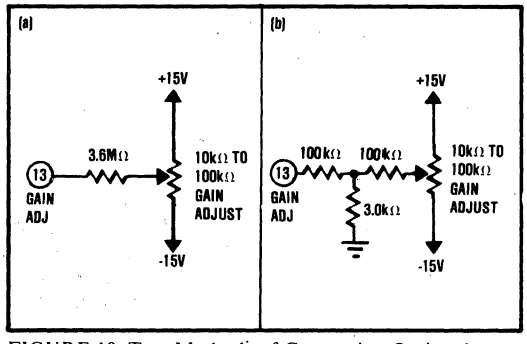
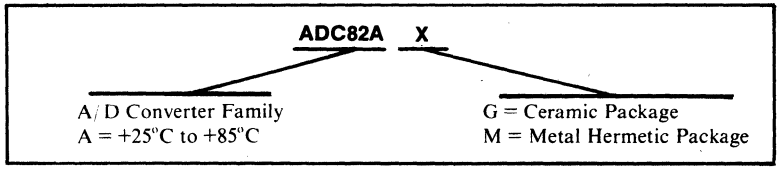


FIGURE 10. Two Methods of Connecting Optional Gain Adjust with a ±10% Range of Adjustment.

ORDERING INFORMATION



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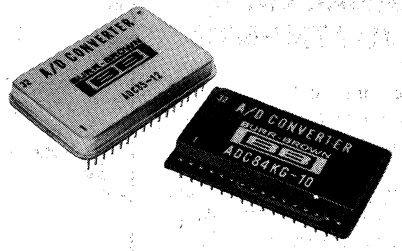

ADC84
ADC85

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **COMPACT DESIGN - Self-contained with internal clock, comparator, reference, and input buffer amplifier 32-pin ceramic or hermetic metal package**
- **FAST CONVERSION SPEEDS**
  Provide Fast Signal Sampling Rates
  12-bits - 10μsec, 10-bits - 6μsec
  Faster conversion speeds obtainable with "Short-Cycling" and adjustable clock rate
- **LOW COST - ADC84KG-12**

DESCRIPTION

The ADC84 and ADC85 families of 10- and 12-bit analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a compact 32-pin dual-in-line packages.

Complete with internal reference and input buffer amplifier, they offer versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.012% (±1/2LSB).

The fast conversion speeds of 10μsec for 12-bit and 6μsec for 10-bit resolution make these ADC's excellent for a wide range of applications where system throughput sampling rates from 100kHz to 120kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at low resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Power supply voltages are ±15VDC and +5VDC.

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DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC84 and ADC85 are also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperture range.

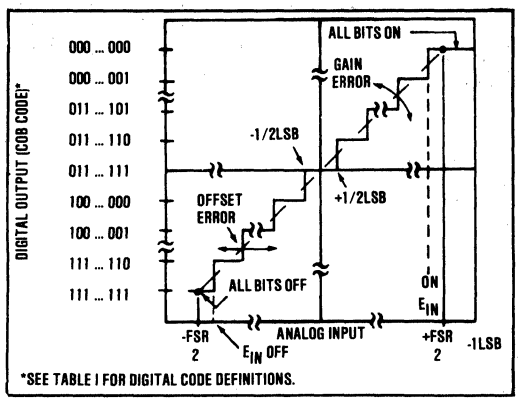


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram of the ADC's (see Figure 2) assumes an analog input such that the positive true digital word 100110001001 exists. The output will be complementary as shown in Figure 2 (011001110110 is the digital output).

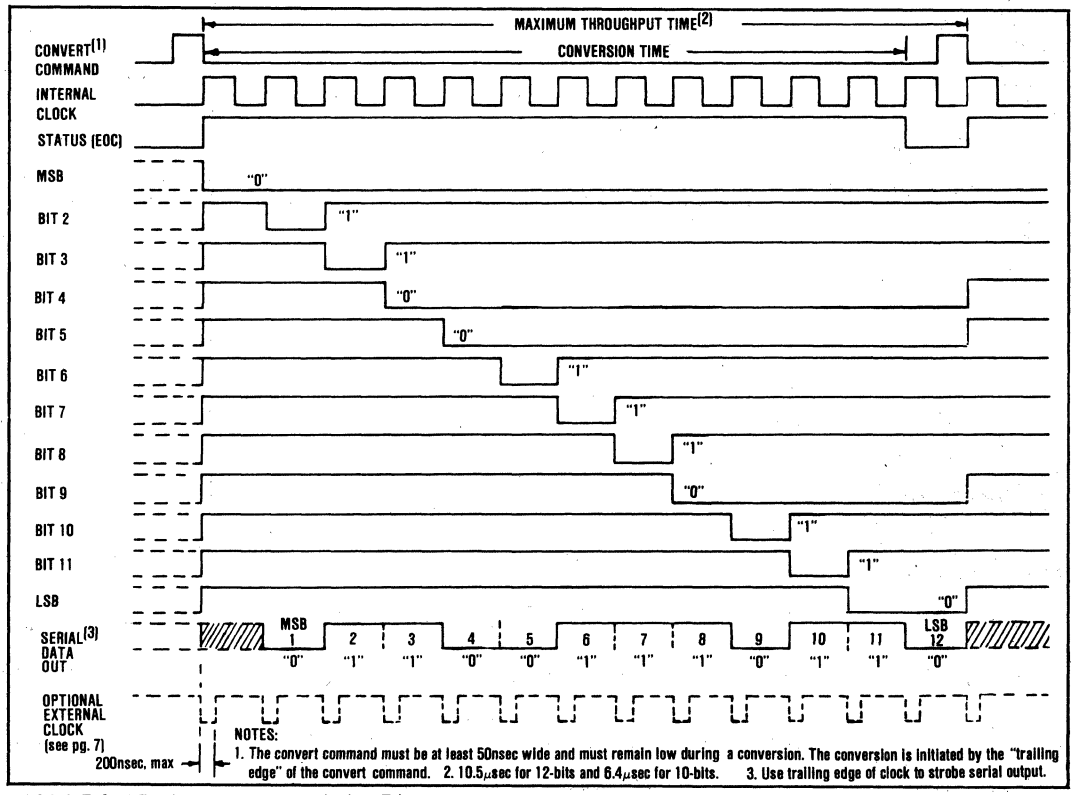


FIGURE 2. ADC84 and ADC85 Timing Diagram.

SPECIFICATIONS

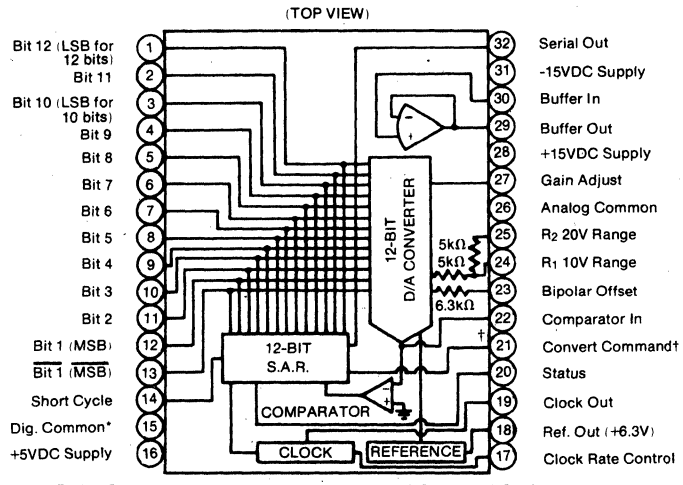
ELECTRICAL

Typical at +25°C and rated power supplies otherwise noted.

MODEL	ADC85		ADC85C		ADC84KG		UNITS
RESOLUTION	10	12	10	12	10	12	**BITS**
INPUT							
ANALOG INPUTS							
Voltages Ranges							
Bipolar			±2.5, ±5, ±10				V
Unipolar			0 to +5, 0 to +10				V
Impedance (Direct Input)							
0 to +5V, ±2.5V			2.5				kΩ
0 to +10V, ±5V			5				kΩ
±10V			10				kΩ
Buffer Amplifier							
Impedance, min			100				MΩ
Bias Current			50				nA
Settling Time							
to 0.01% for 20V step(1)			2				µsec
DIGITAL INPUTS(2)							
Convert Command			Positive pulse 50nsec wide, min. Trailing Edge "1" to "0" initiates conversion				
Logic Loading			1				TTL Load
External Clock			See External Clock paragraph				
TRANSFER CHARACTERISTICS							
ERROR							%
Gain Error			±0.1 (Adjustable to zero)				
Offset Error			Adjustable to zero				% of FSR(3)
Unipolar			±0.05				% of FSR
Bipolar			±0.1				% of FSR
Linearity Error, max(4)	±0.048	±0.012	±0.048	±0.012	±0.048	±0.012	% of FSR
Inherent Quantization Error			±1/2				LSB
Differential Linearity Error			±1/2				LSB
No Missing Codes	-25 to +85	0 to +70	0 to +70	0 to +70	0 to +70	0 to +70	°C
Power Supply Sensitivity							
±15VDC			±0.004				% of FSR/%Vs
+5VDC			±0.001				% of FSR/%Vs
DRIFT							
Specification Temperature Range	-25 to +85		0 to +70		0 to +70		°C
Gain, max	±20	±15	±40	±25		±30	ppm/°C
Offset							
Unipolar	±3	±3	±3	±3	±3	±3	ppm of FSR/°C
Bipolar	±10	±7	±20	±12	±15	±15	ppm of FSR/°C
Linearity, max	±3	±2	±3	±3	±3	±3	ppm of FSR/°C
Monotonicity			Guaranteed				
CONVERSION SPEED (max)(5)(6)	6	10	6	10	6	10	µsec
OUTPUT							
DIGITAL DATA							
All codes complementary							
Parallel							
Output Codes(7)							
Unipolar			CSB				
Bipolar			COB, CTC				
Output Drive			2				TTL Loads
Serial Data Codes (NRZ)			CSB, COB				
Output Drive			2				TTL Loads
Status			Logic "1" during conversion				
Status Output Drive			2				TTL Loads
Internal Clock							
Clock Output Drive			2				TTL Loads
Frequency(6)	1.9	1.35	1.9	1.35	1.9	1.35	MHz
INTERNAL REF. VOLTAGE			6.3				V
Max External Current With no degradation of Specifications			200				µA
Tempco of Drift, max	±5	±5	±10	±10	±20	±20	ppm/°C
POWER REQUIREMENTS							
Rated Voltages			±15, +5				V
Range for Rated Accuracy			4.75 to 5.25 and ±14.5 to ±15.5				V
Supply Drain +15VDC			+45		+45		mA
-15VDC			-35		-35		mA
+5VDC			+120		+70		mA
TEMPERATURE RANGE							
Specification	-25 to +85		0 to +70		0 to +70		°C
Operating (derated specs)			-55 to +85 (110°C case Temp.				°C
Storage	-55 to +125		-55 to +125		-55 to +125		°C
PACKAGE (see Mechanical Specifications)	Metal (Hermetic)				Ceramic		

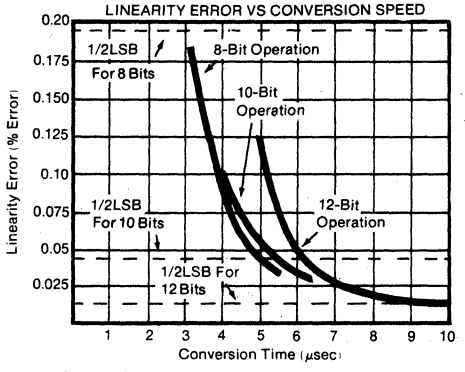
NOTES:
1. This settling time adds to conversion speed when buffer is connected to input.
2. DTL/TTL compatible; i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V, min for inputs. For digital outputs, Logic "0" = +0.4V max, Logic "1" = 2.4V, min.
3. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
4. Error shown is the same as ±1/2LSB max linearity error in % of FSR.
5. Conversion time may be shortened with "short cycle" set for lower resolution. See Table III.
6. Internal Clock is externally adjustable.
7. See Table II. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.

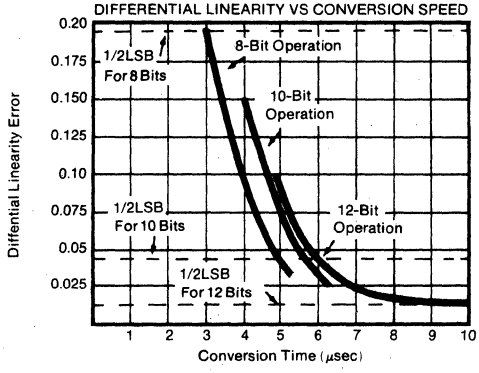
CONNECTION DIAGRAM

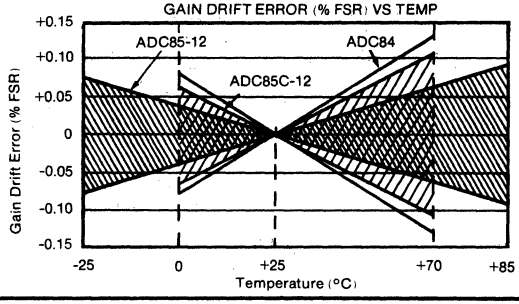


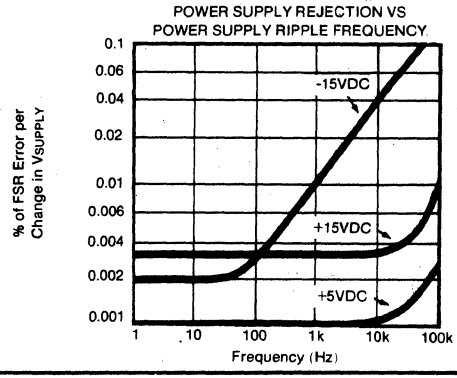
*Digital Common is internally connected to case. (ADC85 and ADC85C only)
† If an external clock is used, connect the clock to Pin-21 (conv. command). (See Figure 2 and External Clock paragraph).

TYPICAL PERFORMANCE CURVES









DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC84 and ADC85 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input singal ranges.

Table I describes the LSB, transition values and code definitions for each possible analog input signal range for 8-, 10-, and 12-bit resolutions.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES					
Analog Input Voltage Ranges	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB* or CTC***	COB* or CTC***	COB* or CTC***	CSB**	CSB**
One Least Significant Bit (LSB)	FSR 2^n	20V 2^n	10V 2^n	5V 2^n	10V 2^n	5V 2^n
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 ... 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5 -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 ... 111	MIL Scale	0	0	0	+5V	+2.5V
111 ... 110	-Full Scale	-10V +1/2LSB	-5V + 1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary
**CSB = Complementary Straight Binary
***CTC = Complementary Two's complement - obtained by using the complement of the most-significant bit (MSB). MSB is available on pin-13.
****Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC84 and ADC85 are specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors and conversion speed effects on accuracy. These ADC's are factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown on next page.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst-case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\epsilon g^2 + \epsilon o^2 + \epsilon e^2}$$

where ϵg = gain drift error (ppm/°C)
ϵo = offset drift error (ppm of FSR/°C)
ϵe = linearity error (ppm of FSR/°C)

For the ADC85-12 operating in the unipolar mode the total RSS drift is ±15.42ppm/°C and for bipolar operation the total RSS drift is ±16.7ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC84 and ADC85 are shown in Typical Performance Curves.

The conversion speeds are specified for a maximum linearity error of ±1/2LSB with the internal clock. Faster conversion speeds are possible (see Clock Rate Control Alternate Connections).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC84 and the ADC85 power supply sensitivity is specified for ±0.003% of FSR/%Vs for ±15VDC supplies and ±0.0015% of FSR/%Vs for +5VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with these ADC's. See Layout Precautions and Power Supply Decoupling on next page.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC84 and ADC85, but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 3 to obtain noise free operation. These capacitors should be located close to the ADC. 1μF electrolytic type capacitors should be bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

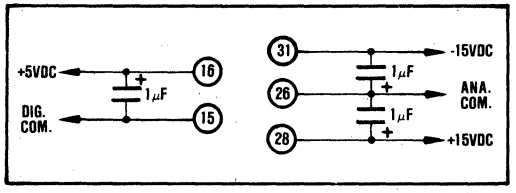


FIGURE 3. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 4 for circuit details.

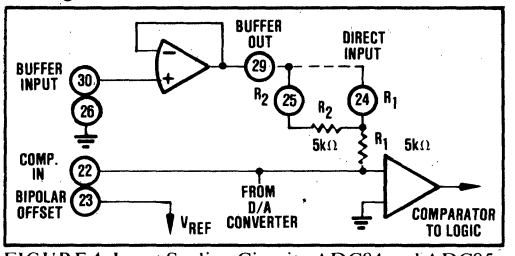


FIGURE 4. Input Scaling Circuit - ADC84 and ADC85.

TABLE II. ADC84 and ADC85 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Buffered Input* Connect Pin 29 To Pin	For Direct Input (see note) Connect Input Signal To Pin
			Input		
±10V	COB or CTC	22	Signal**	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0 to +5V	CSB	26	Pin 22	24	24
0 to +10V	CSB	26	Open	24	24

*Connect to Pin 29 or input signal as shown in next two columns.
**The input signal is connected to Pin 30 if the buffer amplifier is used.
NOTE: If the buffer amplifier is not used, the input Pin 30 must be grounded (Pin 26).

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 5 and 6. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 27 (Gain Adjust) and Pin 22 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

Offset - Connect the Offset potentiometer as shown in Figure 5. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

Gain - Connect the Gain adjust potentiometer as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition voltage to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

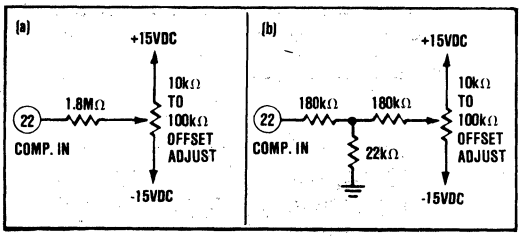


FIGURE 5. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment.

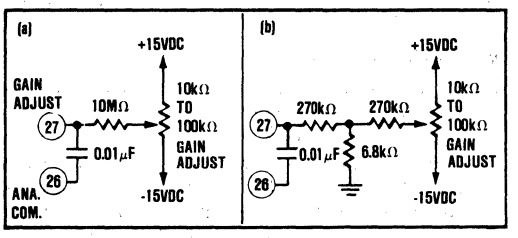


FIGURE 6. Two Methods of Connecting Optional Gain Adjust with a 0.6% Range of Adjustment.

CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the Clock Rate is desired for faster conversion speeds, the Clock Rate Control may be connected to an external multiturn trim potentiometer with TCR of ±100ppm/°C or less as shown in Figures 7A and 7B. If the potentiometer is connected to -15VDC, conversion time can be increased as shown in Figure 8. If these adjustments are used, delete the connections shown in Table III for pin 17. See Typical Performance Curves for nonlinearity error vs. clock frequency, and Figure 8 for the effect of the control voltage on clock speed.

Operation with Clock Rate Control voltage of less than −1VDC is not recommended.

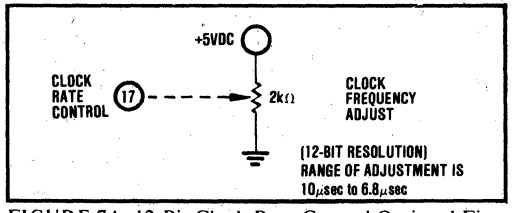


FIGURE 7A. 12-Bit Clock Rate Control Optional Fine Adjust.

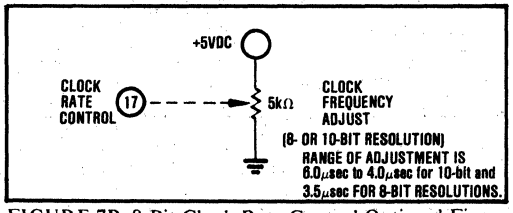


FIGURE 7B. 8-Bit Clock Rate Control Optional Fine Adjust.

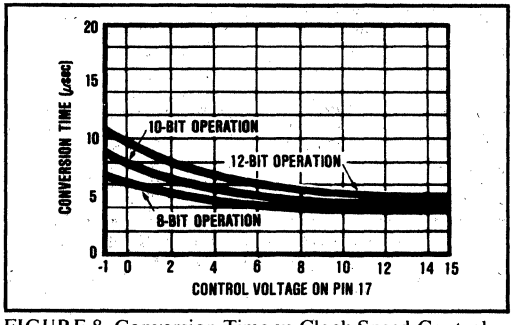


FIGURE 8. Conversion Time vs Clock Speed Control Voltage.

EXTERNAL CLOCK

If an external clock is used, connect the external clock to convert command, pin 21. The convert command shown in Figure 2 is not used. After each conversion is completed, a new conversion cycle will automatically start of the first falling edge of the external clock following the completion of conversion. The clock-out signal will remain as shown in Figure 2 even if an external clock is used. The external clock pulse must be a negative going pulse with a width between 100nsec and 200nsec as shown in Figure 2.

ADDITIONAL CONNECTIONS REQUIRED

The ADC84 and ADC85 may be operated at faster speeds for resolutions less than 12 bits by connecting the Short Cycle input, pin 14, as shown in Table III. Conversion speeds, linearity and resolution are shown for reference. Specifications for 10-bit units assume connections as shown below.

TABLE III. Short Cycle Connections and Specifications for 8- to 12-Bit Resolution.

RESOLUTION (Bits)	12	10	8
Connect Pin 17 to (1)	Pin 15	Pin 16	Pin 28
Connect Pin 14 to	Pin 16	Pin 2	Pin 4
Maximum Conversion Speed (μsec)(2)	10	6	4
Manimum Nonlinearity at 25°C (% of FSR)	0.012(3)	0.048(4)	0.20(4)

NOTES:
1. Connect only if clock rate control is not used.
2. Max. conversion speeds to maintain ±1/2LSB nonlinearity error.
3. 12-bit models only.
4. 10- or 12-bit models.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

OUTPUT DRIVE

Normally all ADC84 and ADC85 logic outputs will drive 2 standard TTL-loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC84 and ADC85 dissipate approximately 1.2W and the packages have a case-to-ambient thermal resistance (Θ_{CA} should be lowered by a heat-sink or by forced air over the surface of the package). See Figure 9 for Θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat-sink compound. On a 0.062-inch thick PC card with 16 square-inch minimum area, this technique will allow operation to 85°C.

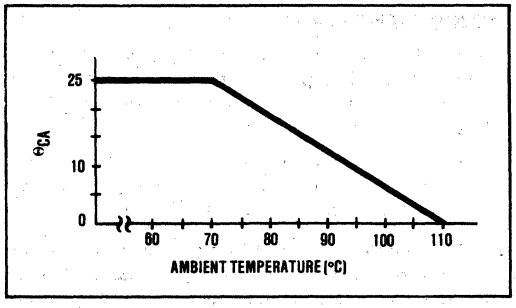


FIGURE 9. θ_{CA} Requirement Above 70°C.

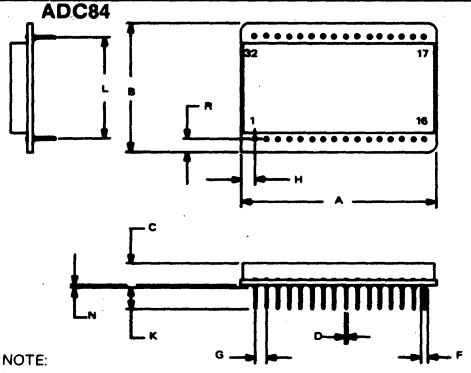
HIGH RELIABILITY A/D CONVERTERS

Each of the ADC85 models are available screened to the requirements of the Burr-Brown Q-Program, which consists of a sequence of thermal and mechanical stress procedures, plus a verification of package hermeticity. The diagram below illustrates the screening sequence which is applied to 100% of the Q-Screened A/D converters.

High Temp. Storage (MIL-STD-883)	Temperature Cycling (MIL-STD-883)	Hermeticity Gross Leak (MIL-STD-883)	Hermiticity Fine Leak (MIL-STD-883)	Burn-In (MIL-STD-883)	Centrifuge (MIL-STD-883)
Method 1008 Condition B +125°C 24 Hours	Method 1010 Condition B -55 to +25°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-7}cc/sec	Method 1015 Condition D 168 Hours +70°C (ADC85C) +85°C (ADC85)	Method 2001 2,000 G Y_1 Axis

MECHANICAL

ADC84

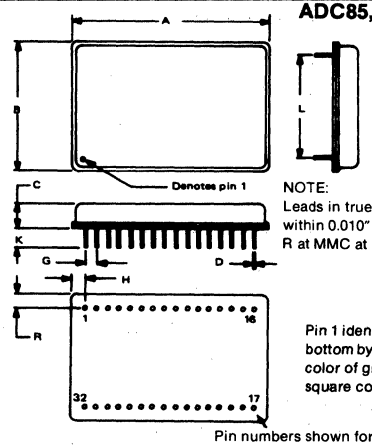


NOTE:
Leads in true position within 0.010" (0.255mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
CASE: Ceramic
MATING CONNECTOR: 2302MC
Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz.)

ADC85, ADC85C



NOTE:
Leads in true position within 0.010" (0.255mm) R at MMC at seating plane.

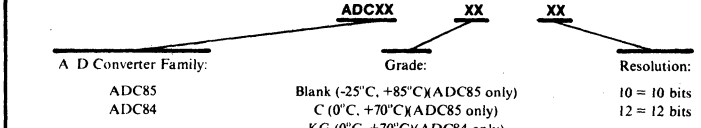
Pin 1 identified on bottom by contrasting color of glass or square corner.

Pin numbers shown for reference only. Numbers may not be marked on package.

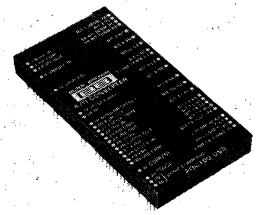
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
CASE: Kovar, Nickel plated
MATING CONNECTOR: 2302MC
Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz.)

ORDERING INFORMATION



BURR-BROWN®



ADC100

High Resolution - Integrating ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 16-BIT RESOLUTION
- SELF-CONTAINED MODULAR PACKAGE
- LOW DRIFT
- USER-ADJUSTABLE LINEARITY
- EXPANDABLE TO 5-DIGIT BCD RESOLUTION

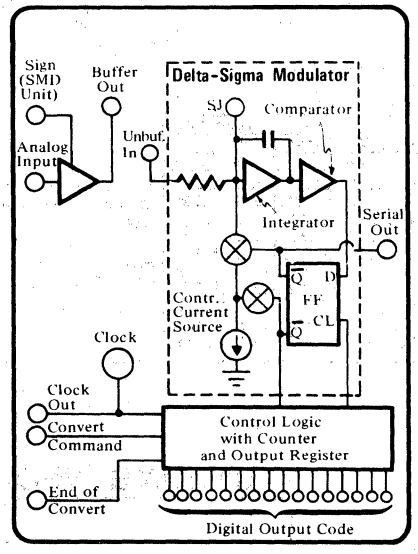
DESCRIPTION

The Burr-Brown Model ADC100 A/D Converter is an integrating A/D Converter that utilizes the delta sigma modulation principle. The digital equivalent of analog signals is developed by counting a number of pulses whose average repetition rate is proportional to the amplitude of the input signal over a fixed integration period. The internal clock is externally-adjustable to provide integration periods which are integral multiples of 50Hz or 60Hz periods for maximum powerline noise rejection. The closed conversion loop assures linear performance of ±0.005% ±1 count that is independent of clock frequency deviations over the specified temperature range of 0°C to ±70°C.

The ADC100 is housed in a 2" x 4" x 0.4" module and operates from ±15VDC and +5VDC power. All digital input and output signals are TTL-compatible.

Four basic models are offered: Unipolar 4-digit BCD, 4-digit plus sign BCD, unipolar and bipolar 16-bit binary. The binary units are pin-programmable for 12-, 14-, or 16-bit resolution.

The ADC100 is excellent for applications which require good accuracy and high resolution, but where speed is not too important. Conversion speeds range from 12msec for 12-bit binary to 30msec for 4-digit plus sign BCD codes.



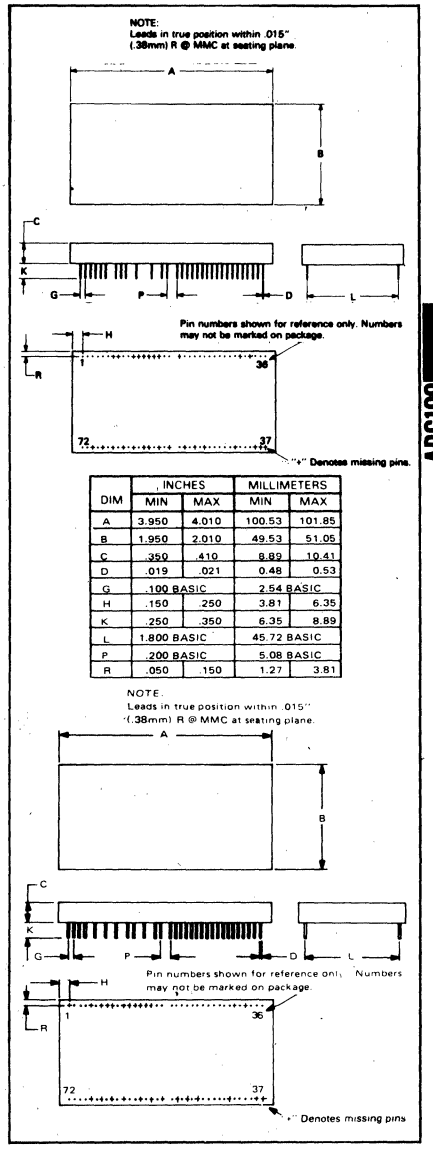
International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

Typical at 25°C and rated power supply unless otherwise noted.

ELECTRICAL

MODEL ADC100	DECIMAL BCD	DECIMAL SMD	BINARY Unipolar USB	BINARY Bipolar BOB	UNITS
RESOLUTION	4 digits	4 digits + sign	14 or 16 bits	14 or 16 bits	
INPUT					
ANALOG INPUT					
Voltage Range	0 to +10	±10	0 to +10	±10	V
Maximum Safe Input Signal	±25V or supply voltage, whichever is less				
Input Bias Current typ max	20		200		nA
Impedance	200				nA
Buffered	200	200	200	200	MΩ
Unbuffered	10	10(1)	10	25	kΩ
Settling Time (to 0.003%) FSR(2) step					
Buffered, max	25	50	25	50	μsec
Unbuffered, max	1	1	1	1	μsec
DIGITAL INPUT					
Convert Command	TTL/DTL Compatible Logical "1" for at least one clock period @ 2 TTL Loads (Approximately 3μsec with internal clock)				
External Clock	See "Clock Operation"				
TRANSFER CHARACTERISTICS					
ACCURACY(3)					
Gain Error	.05	.05	.05	.05	% of FSR
Offset Error	.02	.02	.02	.05	% of FSR
Linearity Error, max(4)	±0.005	±0.005	±0.005	±0.005	% of FSR(2)
Quantizing Error	±1 count				
ACCURACY DRIFT					
Temperature Coefficient (max)	±10	±5	±10	±10	ppm of FSR/°C
POWER SUPPLY SENSITIVITY					
Power Supply Sensitivity, max					
±15VDC	±0.007	±0.004	±0.0002	±0.0002	% of FSR/% of P.S. Voltage(15V)
+5VDC	±0.002	±0.001	±0.002	±0.001	% of FSR/% of P.S. Voltage(5V)
CONVERSION TIME					
(maximum with Internal Clock)	30	30	For 12 bits - 12.5 14 bits - 50 16 bits - 200		msec
OUTPUT					
DIGITAL OUTPUTS	TTL/DTL Compatible				
	All digital outputs will drive 6 TTL loads except the sign bit (for SMD units) which will drive 4 TTL loads				
End of Conversion	"0" during conversion				
TEMPERATURE					
Specification	0 to +70				°C
Operating (reduced specs)	-25 to +85				°C
Storage	-55 to +100				°C
POWER SUPPLY					
Rated Voltage	±15 and +5				V
Range (max)	±14.5 to ±15.5 and +4.75 to +5.25				V
Supply Drain					
+15VDC	25	25	25	25	mA
-15VDC	20	20	15	15	mA
+5VDC	300	300	300	300	mA



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	3.950	4.010	100.53	101.85
B	1.950	2.010	49.53	51.05
C	.350	.410	8.89	10.41
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.350	6.35	8.89
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	.050	.150	1.27	3.81

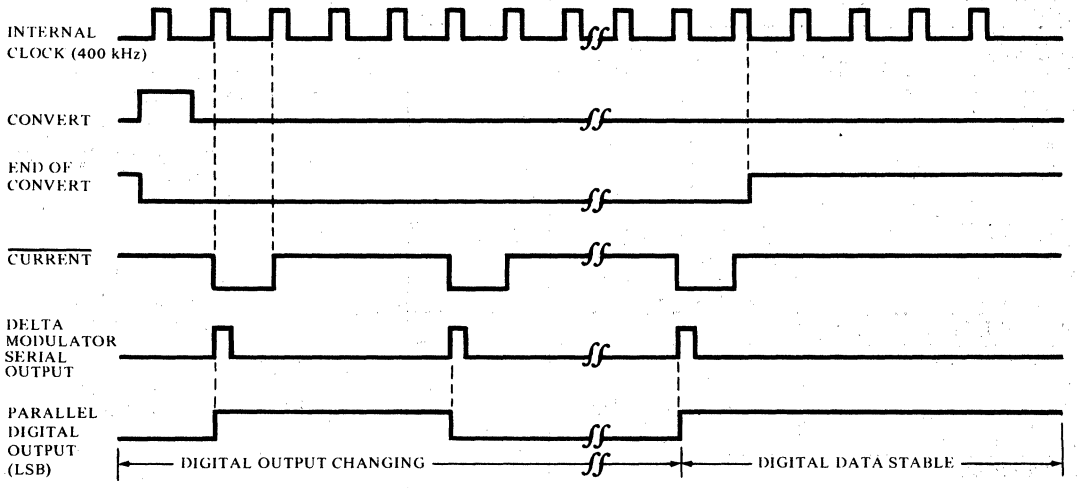
1) The internal buffer may be bypassed by connecting the input directly to unbuffered inputs. For SMD units this connection bypasses the sign magnitude circuitry and results in a unipolar BCD unit.
2) F S R is Full Scale Range; 10V for unipolar, 20V for bipolar converters.
3) Gain and Offset Error may be externally adjusted to zero.
4) Linearity is factory adjusted for 4 digit or 14 bit operation and is user adjustable to typically 0.002%.

Case: Diallyl Phthalate shell
Pins: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].
Weight: 4 oz (114 grams)
Actual pin assignments not shown on this diagram.
Mating Connectors: 2400MC - P.C. Card with solder terminals or 2401MC - Set of 4 - 18 pin connector strips

Method of Conversion

DELTA-SIGMA MODULATION

The Burr-Brown Model ADC100 A/D Converter utilizes the delta-sigma conversion technique which produces a train of pulses whose rate is proportional to the amplitude of the input analog signal. For a given internal clock frequency (400 kHz) the delta-sigma modulator output is a train of pulses whose average frequency varies from zero to 400 kHz. The width of these pulses are constant, but the number of pulses varies in relation to input signal amplitude. These pulses are counted in a binary (or BCD) counter over the integration interval resulting in a direct digital output that is equivalent to the analog input. The ADC100 timing diagram is shown in Figure 1.



DISCUSSION OF SPECIFICATIONS

ANALOG INPUT SETTLING TIME is the time required after a F.S.R. input step for the converter's input circuitry to settle to specified accuracy. The CONVERT COMMAND should be delayed by this period of time after any large input voltage change to preserve the converter's accuracy.

ACCURACY - The basic accuracy of the ADC100 is defined by linearity and quantizing errors. When gain and offset errors are adjusted as shown in Figures 3 and 4 and Table I, the accuracy of the ADC100 is 0.005% ±1 count.

LINEARITY ERROR is a measure of the deviation of the converter's actual transfer characteristic from the ideal. It is defined as the maximum deviation of the actual converter transfer function from the best fit straight line through it. If the linearity error is also adjusted, the accuracy will typically be 0.002% ±1 count.

QUANTIZING ERROR is inherent in any A/D converter simply because a converter's analog input is continuous while its digital output must be discrete codes. The ADC 100 is designed such that increased resolution may be obtained by interpolation of several successive conversions of the same input voltage. For example, if the output code is zero for three conversions and one LSB for one conversion, the actual input voltage is one quarter of an LSB.

ACCURACY DRIFT is the maximum change with temperature of any point on the converter's transfer characteristic.

OFFSET ERROR is the deviation from the ideal input required to produce an output of all logical zeroes (all bits OFF). GAIN ERROR is the deviation from the ideal input required to produce an output of all logical ones (all bits ON) with the offset error adjusted to zero.

SERIAL OUTPUT

The serial output of the ADC100 may be used to transmit data remotely over a single line. Details for implementing this method of data transmission are discussed in "Applications."

DIGITAL OUTPUT CODES

For unipolar analog input signals, 4-digit BCD or 16-bit straight binary (USB) digital output codes are offered; for bipolar analog input signals, 4-digit plus sign BCD (SMD) or 16-bit offset binary (BOB) digital output codes are offered. The LSB & full scale analog values and equivalent digital codes are shown in Table I.

ORDERING INFORMATION

The ADC 100 may be ordered by using the ordering code below.

ADC100 – XXX –

ADC100 – Converter Family

XXX – OUTPUT CODE
BCD - Binary Coded Decimal
SMD - Sign Magnitude BCD
USB - Unipolar Straight Binary
BOB - Bipolar Offset Binary

INSTALLATION and OPERATING INSTRUCTIONS

CLOCK OPERATION

The ADC100 may be operated from the internal clock, or from a user supplied external clock.

A clock period faster than 2.5 μseconds or slower than 25μseconds will degrade the performance of the ADC100. 50 Hz or 60 Hz rejection may be achieved by adjusting the clock frequency such that the CONVERT COMPLETE pulse is an integral number of 50 or 60 Hz periods (i.e., a multiple of 16.67 ms for 60 Hz rejection or 20.00 ms for 50 Hz rejection). For example, SMD or BCD units convert in 30 millisec with a clock period of 3 μsec. The closest multiple for 60 Hz rejection is 33.33 ms integration time.

EXTERNAL CLOCK

An external clock may be used by leaving CLOCK OUT, pin 26, open and connecting the external clock to CLOCK IN, pin 28. The duty cycle of the external clock should be 80% to 90% as shown in Figure 3.

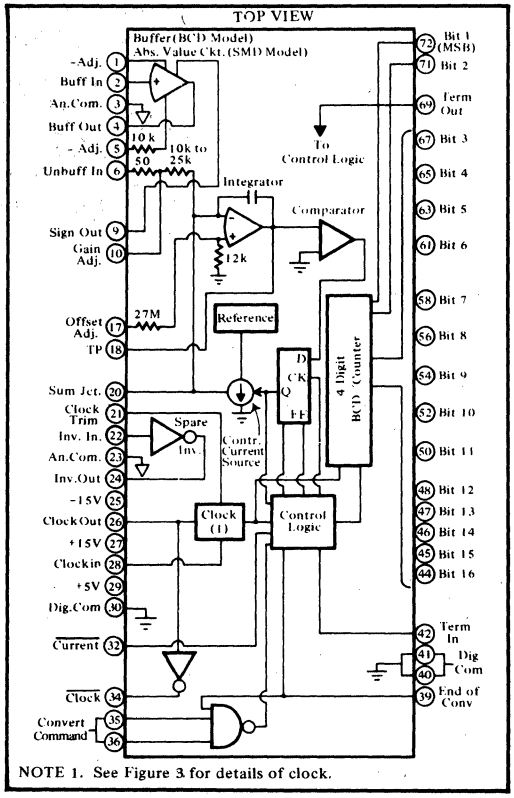
INTERNAL CLOCK

If the internal clock is used, CLOCK OUT, pin 26, and CLOCK IN, pin 28, must be connected together.

The approximate period of the internal clock is 3 μseconds.

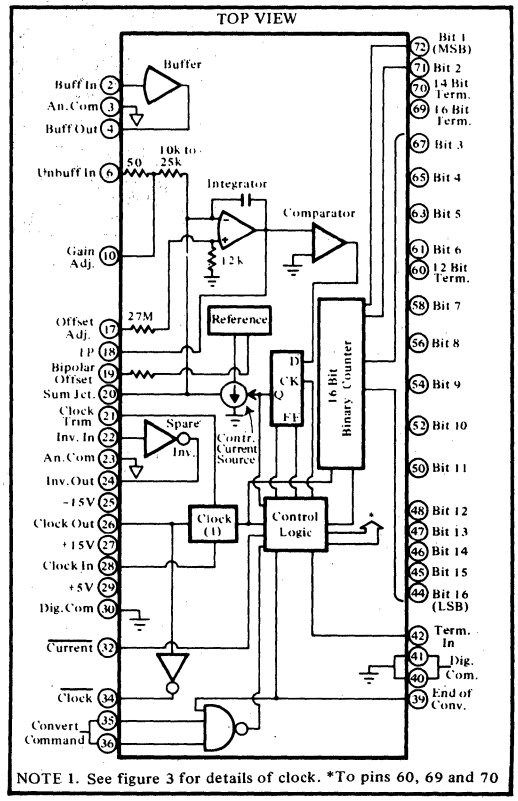
The internal clock frequency may be adjusted using the circuit shown in Figure 5 over a range of approximately 2.5 μsec to 25 μsec. If the clock frequency is not adjusted, pin 21 should simply be left open.

CONNECTION DIAGRAMS



NOTE 1. See Figure 3 for details of clock.

FIGURE 2a. BCD and SMD Models.



NOTE 1. See figure 3 for details of clock. *To pins 60, 69 and 70

FIGURE 2b. USB and BOB Models.

ANALOG COMMON, pins 3 and 23, are connected together internally as are DIGITAL COMMON, pins 30, 40 and 41. Digital and Analog Common are not connected internally; but they should be tied together at some point in the system as close as possible to the ADC100 to prevent any difference voltage between them.

All units have available a spare inverter (SN7404) whose input is pin 22 and output is pin 24.

USB and BOB units are marked as shown in Figure 3; the BOB units only will have a connection for BIPOLAR OFFSET, pin 19. The BOB units must have pin 19 externally connected by the user to SUMMING JUNCTION, pin 20.

For USB and BOB units, either 16-BIT TERMINATE, pin 69, 14-BIT TERMINATE, pin 70, or 12-BIT TERMINATE, pin 60, must be connected to TERMINATE IN, pin 42. The LSB will always be on pin 44, the MSB for 16 bits is on pin 72, for 14 bits is on pin 67, for 12 bits is on pin 63.

BCD and SMD units are marked as shown in Figure 4, the SMD units only will have connections for ADJ, pin 1 and pin 5, and SIGN OUT, pin 9.

For BCD and SMD units, TERMINATE OUT, pin 69, should be connected to TERMINATE IN, pin 42, for 4-digit operation (see "Applications" for increased resolution).

NOTE:
For SMD units, the output sign bit operates continuously. That is, the sign bit output will change with the input voltage polarity even though the end of conversion output is "high". Therefore an output flip flop (such as the 7474 IC shown on next page) may be used to store the sign bit at the end of conversion. (The PC mount option includes this flip-flop).

CONNECTIONS FOR INPUT SIGNAL, EXTERNAL GAIN and OFFSET TRIM

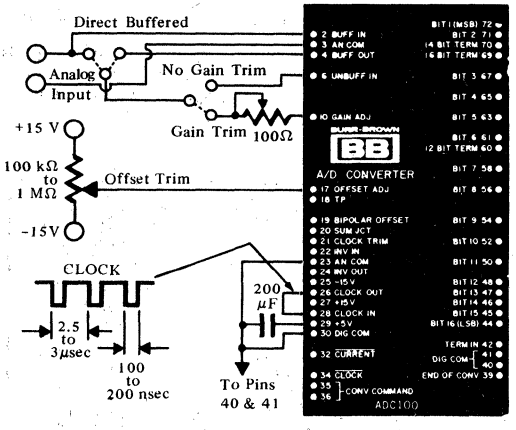


FIGURE 3. GAIN and OFFSET Adjustments for all Converters.

The connections shown in Figure 3 illustrate various input and trim connection options; it is not necessary to include switches or jumpers as indicated unless that level of flexibility is desired. If linearity is not externally adjusted, the transfer characteristic of the ADC100 can be adjusted for minimum errors using only the GAIN and OFFSET adjustments. Table I shows the input voltage and respective output codes for these adjustments.

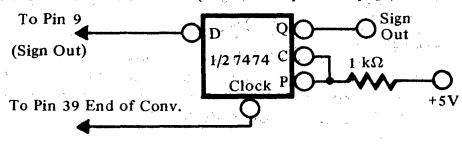
BCD and USB MODELS

Adjust to the proper output code with an input of +2.5000 volts using the OFFSET adjustment; then adjust to the proper output code with +7.5000 volts input using the GAIN adjustment (see Figure 3 for circuitry and Table I for input/output values). Repeat until both are optimum.

SMD MODELS

Adjust to the proper output codes as described above for BCD and USB models at 2.500 and +7.500 volts; then use the negative OFFSET adjustment (as shown in Figure 4) to provide the proper output code with -10 mV input and the negative GAIN adjustment (also in Figure 4) to provide the proper output code with -9.9900 volts input (see Table I).

SMD SIGN BIT STORAGE (see note on previous page)



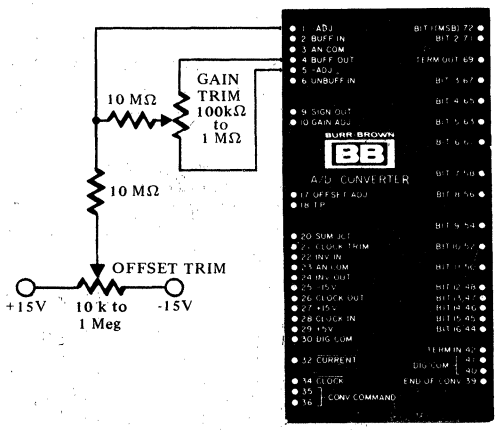


FIGURE 4. Additional NEGATIVE GAIN and OFFSET Adjustments required for SMD Converters.

BOB MODELS

Using the OFFSET adjustment, adjust to the output code of 0100 . . . . 00 with an input of -5.0000 volts; then find the input voltage, (near +5.00 volts), that causes an output code of 1100 . . 000. Set the input voltage to a point halfway between e and 5.0000 volts. Use the GAIN adjustment to provide an output of 1100 . . . 000. Repeat the OFFSET adjustment at -5.0000 volts and check to see that an input of +5.00000 volts produces an output code of 1100 . . . 000. (See Table I). Repeat until both are optimum.

WIRING PRECAUTIONS

All connections between the ADC100 and external components should be as short as possible to minimize coupling effects and noise pickup. The +5V logic supply must be bypassed with a 100 to 200 μF tantalum capacitor to digital common to preserve ADC100 linearity, particularly near mid-scale. Experimenting by setting full scale and zero exactly correct and checking at or near mid-scale while varying the power supply decoupling will demonstrate the quality of the bypassing. This should be done first without any of the clock and/or linearity adjust circuitry, and then with the circuitry if it is to be used.

UNUSED ADJUSTMENTS

All unused adjustments should be left open except OFFSET adjust which should be grounded.

TABLE I. GAIN and OFFSET Adjustments without LINEARITY TRIM.

CODE		One LSB (mV)	1/4 Scale OFFSET Adjust		3/4 Scale GAIN Adjust	
			Input Voltage	OUTPUT CODE	Input Voltage	OUTPUT CODE
	BCD 4 digit	1.00	+2.5000	MSB LSB 0010 0101 0000 0000	+7.5000	MSB LSB 0111 0101 0000 0000
USB	12 bits	2.44	+2.5000	010000000000	+7.5000	110000000000
	14 bits	0.61	+2.5000	01000000000000	+7.5000	11000000000000
	16 bits	0.15	+2.5000	0100000000000000	+7.50000	1100000000000000
SMD	Positive	1.00	+2.5000	1 0010 0101 0000 0000	+7.5000	1 0111 0101 0000 0000
	Negative		-0.0100	0 0000 0000 0001 0000	-9.9900	0 1001 1001 1001 0000
BOB	12 bits	4.88	-5.0000	010000000000	+5.0000	110000000000
	14 bits	1.22	-5.0000	01000000000000	+5.0000	11000000000000
	16 bits	0.31	-5.00000	0100000000000000	+5.00000	1100000000000000

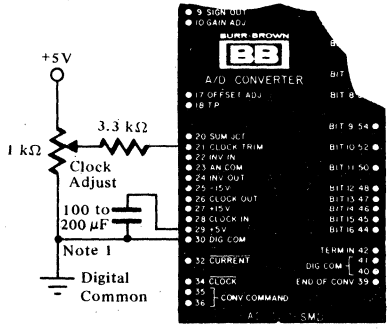
NOTE: Negative full scale is 0.000V for unipolar and -10.000V for bipolar models. Positive full scale is +10.000V -1 LSB.

CLOCK and LINEARITY ADJUSTMENTS

CLOCK ADJUST

It may be necessary to adjust the clock frequency if optimum noise rejection to 50 or 60 Hz power line frequency is desired, or else a specific conversion period is desired. Otherwise, an external clock adjustment is not required. The CLOCK ADJUST trim circuitry shown in Figure 5 may affect linearity, particularly where there is already a bypassing problem with the 5 volt logic supply. If clock trim is employed, it may also be necessary to perform the linearity adjustment described below. The external wiring at pin 21 should be as short as possible to minimize this problem.

NOTE: The 400 kHz clock frequency will vary up to 1% per degree Centigrade. This will have a very small affect on the accuracy of the ADC100, but it can cause problems in some systems applications since the total conversion time will vary inversely with this frequency.



NOTE 1. Use tantalum capacitor.

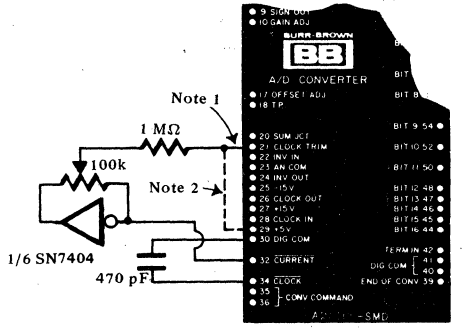
FIGURE 5. CLOCK ADJUST Circuit.

LINEARITY ADJUSTMENT

Linearity errors can typically be adjusted to less than 0.002% with the circuitry shown in Figure 6. This adjustment can be done only when the internal clock is used.

If the LINEARITY adjust circuitry is used, the OFFSET adjustment should be made near negative full scale, the GAIN adjustment should be made near positive full scale, and linearity adjusted near mid-scale. See Table II for the proper input voltages and output codes.

With GAIN and OFFSET adjusted per above, the linearity error should be adjusted to zero near mid-scale. Supply the ADC100 input with the mid-scale voltage shown in Table II and adjust the linearity potentiometer to obtain the output code also specified in Table II.



NOTES:
1. This wire should be as short as possible
2. This connection required only when external clock is used.

FIGURE 6. LINEARITY Adjustment Circuit.

TABLE II. GAIN and OFFSET Adjustments with LINEARITY Trim.

CODE	OFFSET Adjustment		GAIN Adjustment		Mid-Scale LINEARITY Adjust	
	Input Voltage	Output Code	Input Voltage	Output Code	Input Voltage	Output Code
BCD 4 digit	+0.0100	MSB LSB 0000 0000 0001 0000	+9.9900	1001 1001 1001 0000	+5.010	MSB LSB 0101 0000 0001 0000
USB 12 bits	+0.00976	000000000100	+9.9878	111111111011	+5.00488	100000000010
14 bits	+0.00976	00000000010000	+9.9896	11111111101111	+5.00488	10000000001000
16 bits	+0.00976	0000000001000000	+9.9901	1111111110111111	+5.00488	1000000000100000
SMD Positve	+0.0100	1 0000 0000 0001 0000	+9.9900	1 1001 1001 1001 0000	+5.010	1 0101 0000 0001 0000
Negative	-0.0100	0 0000 0000 0001 0000	-9.9900	0 1001 1001 1001 0000	– –	– –
BOB 12 bits	-9.99024	000000000010	+9.9854	111111111101	+0.00976	100000000010
14 bits	-9.99024	00000000001000	+9.9890	11111111110111	+0.00976	10000000001000
16 bits	-9.99024	000000000010000	+9.9898	1111111111011111	+0.00976	1000000000100000

APPLICATIONS

VOLTAGE TO FREQUENCY CONVERTER

The $\overline{\text{CURRENT}}$ output, pin 32, and the $\overline{\text{CLOCK}}$ output, pin 34, may be used to provide a continuous serial output pulse train whose average repetition rate is proportional to the analog input voltage. This circuitry is shown in solid lines in Figure 8. The END OF CONVERSION output, pin 39, can be gated with the serial output using the additional circuitry shown with dotted lines. The gated output pulse train is available only during conversion and the number of pulses in that period is proportional to the input voltage, as shown in Figure 7.

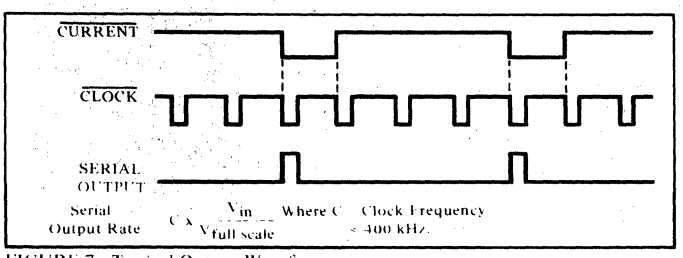


FIGURE 7. Typical Output Waveforms.

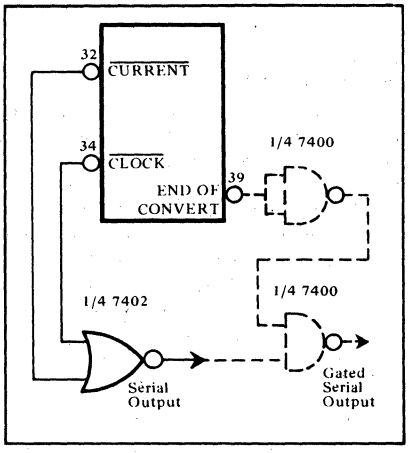


FIGURE 8. Voltage to Frequency Converter.

5 DIGIT ADC100

The resolution of BCD and SMD models may be expanded to 4-1/2 or 5 digits with a minimum of external circuitry. Expansion to 4-1/2 digits will double the conversion time to about 60 milliseconds while 5 digit conversion will require 300 milliseconds. Figure 9 shows the application of two SN 7490 decade counters to provide an extra digit output.

If the ADC100 is used for five digit operation, it is recommended that the linearity adjustment circuitry shown in Figure 6 be used to provide accuracy consistent with the resolution. With five digit operation, the positive full scale input voltage is +9.99990 volts while the negative full scale input is 0.00000 volts (BCD) or -9.99990 (SMD). A good mid-scale input voltage to use for the linearity adjustment is 5.00500 volts (output code 0101 0000 0000 0101 0000). The ADC100 may be used as the heat of a 5 digit DPM with accuracy much better than that of any moderately priced digital panel meters at a lower cost.

The components required in addition to the ADC100 are:

(1) Two decade counters (such as TI's SN7490)

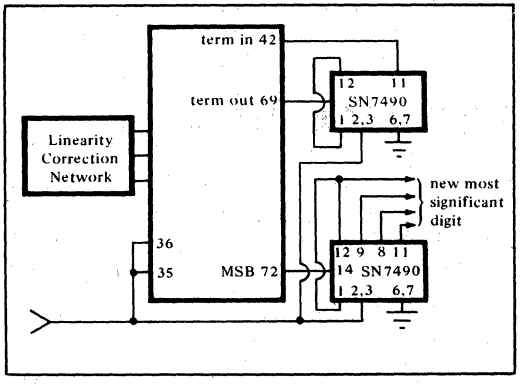


FIGURE 9. Extending ADC100 to 5 Digits.

(2) Five BCD to seven segment decoders (such at TI's SN7447A)

(3) A display (such as RCA's DR2100 Numitron series)

(4) Power Supplies, ±15 volts and +5 volts (such as Burr-Brown's Model 551 and Model 562).

ADC100 PREAMPLIFIER

An instrumentation amplifier may be used as the input to the ADC100. An input instrumentation amplifier such as Burr-Brown's 3625 will provide differential inputs with common mode rejection as well as gain. The circuitry shown below will provide a gain of 10 (i.e., 1 volt instead of 10 volt input range) and 74 dB CMR.

The offset adjustment of the ADC100 has enough range to compensate for the small output offset of the 3625 and its' gain adjustment can compensate for the gain errors of the 3625

The 3625B will add no more than 10 ppm/°C gain drift and 1 ppm/°C offset drift while contributing only 0.002% linearity errors.

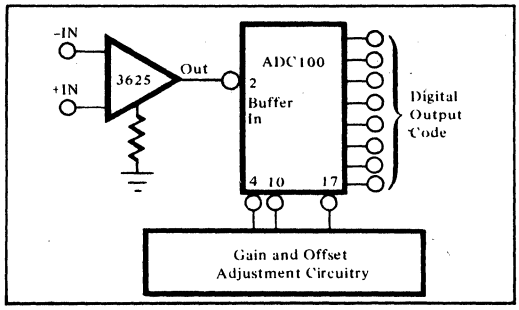
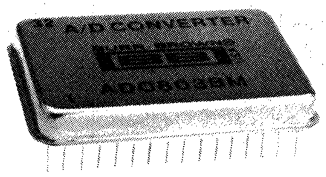


FIGURE 10. Differential Input ADC100.

BURR-BROWN®



ADC803

High-Speed ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 12-BIT RESOLUTION
- ±0.012% LINEARITY AND DIFFERENTIAL LINEARITY ERROR MAXIMUM (C GRADE)
- NO MISSING CODES –25°C TO +85°C
- 32-PIN METAL PACKAGE
- CONVERSION TIME: 500nsec, 8 bits
  670nsec, 10 bits
  1.5μsec, 12 bits

DESCRIPTION

The ADC803 is a high speed successive approximation analog-to-digital converter utilizing state-of-the-art IC and laser-trimmed thin film components.

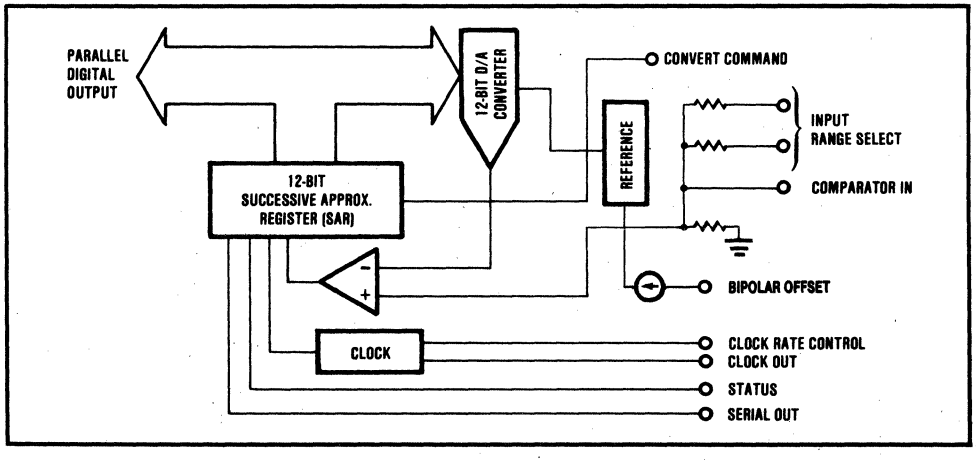
It is complete with internal reference, clock, and comparator and is packaged in a 32-pin metal package. Conversion time is set at the factory to 1.5μsec.

With user-adjusted conversion time set at 1μsec, ±1LSB accuracy can be achieved. The gain and offset errors may be externally-trimmed to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of 0V to -10V, ±5V, and ±10V.

Output data is available in a serial or parallel format. Output codes available are complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, 1.5μsec conversion time, and after 6-minute warm-up unless otherwise noted.

MODEL	ADC803CM			ADC803BM			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			12	Bits
INPUTS							
ANALOG							
Voltage Ranges							
Bipolar		±5, ±10			*		V
Unipolar		0 to -10			*		V
Impedance							
-10V to 0V, ±5V		1.4			*		kΩ
±10V		2.4			*		kΩ
DIGITAL							
Convert Command	Negative pulse 50nsec wide (min) trailing edge (0 to 1) initiates conversion						
Logic Loading			4			*	TTL Loads
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(1)		±0.04	±0.1		±0.08	±0.2	%
Offset Error(1)							
Unipolar		±0.05	±0.2		±0.07	±0.3	% of FSR(2)
Bipolar		±0.02	±0.1		*	±0.2	% of FSR
Linearity Error							
1.5μsec Conversion Time		±0.009	±0.012			±0.020	% of FSR
1.0μsec Conversion Time		±0.015	±0.020		±0.020		% of FSR
Differential Linearity Error							
1.5μsec Conversion Time		±0.012	±0.015			±0.020	% of FSR
1.0μsec Conversion Time			±0.024		±0.024		% of FSR
Inherent Quantization Error		1/2			*		LSB
POWER SUPPLY SENSITIVITY							
Gain and Offset							
+15VDC		±0.0036			*		% of FSR/%V_{CC}
-1 VDC		±0.0005			*		% of FSR/%V_{CC}
+5VDC		±0.001			*		% of FSR/%V_{DD}
Conversion Time							
+15VDC		±0.7			*		%/%V_{CC}
-15VDC		None			*		%/%V_{CC}
+5VDC		±0.8			*		%/%V_{DD}
CONVERSION TIME							
Factory Set	1.3		1.5			*	μsec
Range of Adjustment(3)	0.8		2.2	*		*	μsec
DRIFT							
Gain		±10	±30		±15	*	ppm of FSR/°C
Offset							
Unipolar		±2	±7		±3	*	ppm of FSR/°C
Bipolar		±3	±10		±5	*	ppm of FSR/°C
Linearity Error, -25°C to +85°C							
1.5μsec Conversion Time		±0.012	±0.018			±0.024	% of FSR
1.0μsec Conversion Time		±0.015			±0.020		% of FSR
Differential Linearity Error, -25°C to +85°C							
1.5μsec Conversion Time		±0.012	±0.018			±0.024	% of FSR
1.0μsec Conversion Time		±0.015			±0.024		% of FSR
Conversion Time		±0.1			*		%/°C
No Missing Code Temp. Range							
1.5μsec Conversion Time	-25		+85	*		*	°C
OUTPUT							
DIGITAL DATA							
Parallel							
Output Codes							
Unipolar			Complementary Straight Binary				
Bipolar			Bipolar Offset Binary				
Output Drive	6		*				TTL Loads
Serial Data Codes (NRZ)			Same as Parallel (MSB first)				
Output Drive	6		*				TTL Loads
Status			Logic "1" during Conversion				
Status Output Drive	6		*				TTL Loads
Internal Clock							
Clock Output Drive	3		*				TTL Loads
Frequency (without external clock adjustment)		8			*		MHz

ELECTRICAL (CONT)

MODEL	ADC803CM			ADC803BM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Power Consumption							
Rated voltage, Analog ($\pm V_{CC}$)	±14.25	±15.0	±15.75	*	*	*	VDC
Digital (V_{DD})	+4.75	+5.0	+5.25	*	*	*	VDC
Supply Drain, +15V		+27	+32		*	*	mA
-15V		-38	-55		*	*	mA
+5V		+180	+210		*	*	mA
TEMPERATURE RANGE (AMBIENT)							
Specification	-25		+85	*		*	°C
Storage	-55		+125	*		*	°C

*Specification same as for ADC803CM

NOTES:
1. Adjustable to zero. See Optional Gain and Offset Adjustment section.
2. FSR means Full Scale Range. For example, unit connected for ±10V has 20V FSR.
3. See Optional Clock Rate Control section. For faster conversion time at less resolution, see section on External Short Cycle.

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage To Analog Common. . . ±18V

Digital Supply Voltage To Digital Common. . . . +7V

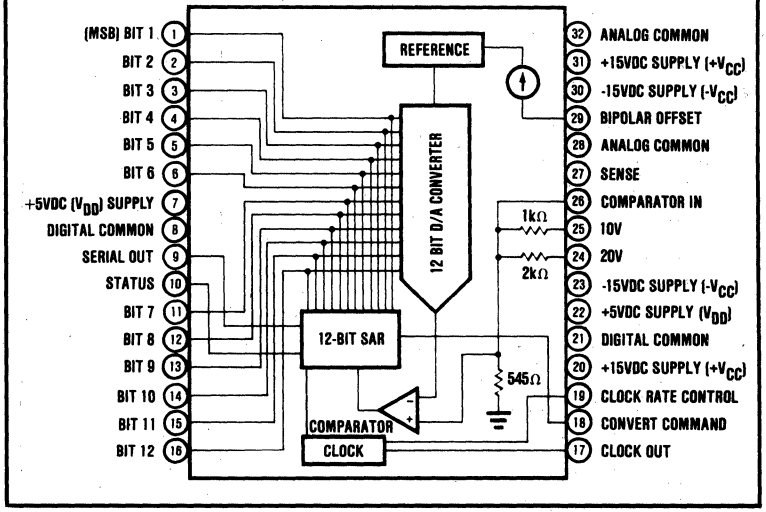
Digital Controls Inputs . . . . . +5.5V

Analog Inputs . . . . . ±15V

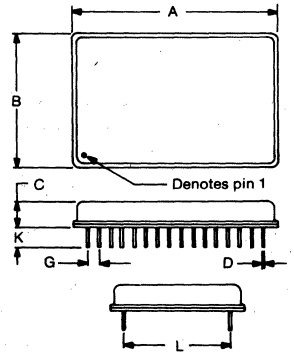
Operating Temperature
- Ambient . . . . . +85°C
- Case . . . . . +125°C

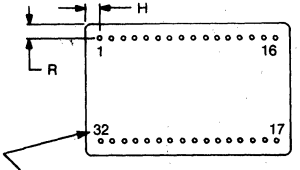
Storage Temperature. . . . +125°C

CONNECTION DIAGRAM



MECHANICAL





Pin numbers shown for reference only. Numbers may not be marked on package.

Pin 1 can be identified from bottom of unit by either a contrasting color of glass seal or a square corner. Case is tied to Digital Common.

NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane. Pin 8 connected to case.

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
CASE: Kovar, Nickel plated
HERMETICITY: Gross Leak Test
MATING CONNECTOR: 2302MC Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

THEORY OF OPERATION

The accuracy of a successive approximation analog-to-digital converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry matching and tracking properties of the ladder and scaling networks, power supply rejection, reference errors and the dynamic errors of the DAC and comparator. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the transfer function (Figure 1) about the zero point and Offset drift shifts the transfer function left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB. The ADC803 is guaranteed to have no missing codes over the specified temperature range.

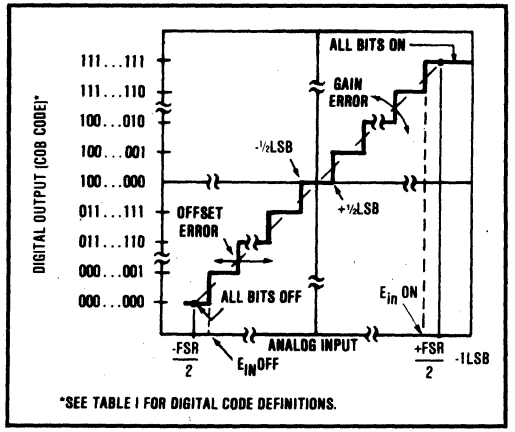


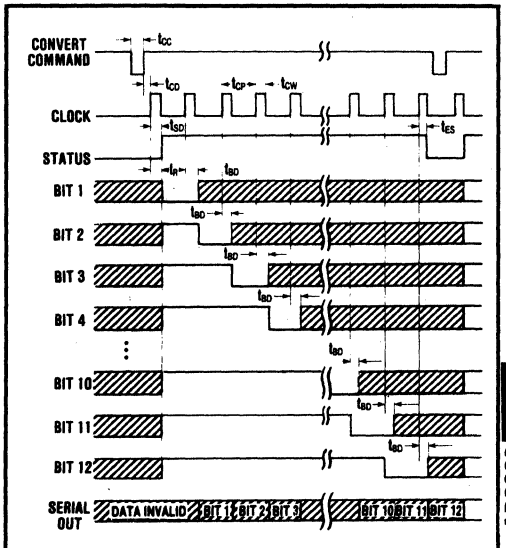
FIGURE 1. Input versus Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) shows the relationship between the convert command, clock and outputs. The digital output word is positive true logic for bipolar operation and complementary logic for unipolar operation.

The following are some important notes on the ADC803 timing. The times given are typical unless otherwise noted. Nominal maximum and minimum times are also given in Figure 2.

1. When power is first applied, the status of the ADC803 will be undetermined. A CONVERT COMMAND must be applied to initialize the ADC803.



Time Period	Min* (nsec)	Max* (nsec)
t_{CC}	50	—
t_{CD}	15	40
t_{CP}**	100	125
t_{CW}	17	25
t_{SD}	10	38
t_R	10	38
t_{BD}	10	38
t_{ES}	10	38

*Nominal
**Without external adjustment

FIGURE 2. ADC803 Timing Diagram.

2. The CONVERT COMMAND must be low at least 50nsec prior to the "0" to "1" edge that starts a conversion.
3. The clock runs continuously when the initial CONVERT COMMAND goes high and whenever the CONVERT COMMAND is high thereafter. It does not run when CONVERT COMMAND is low. It may be beneficial to keep CONVERT COMMAND low except during conversions to limit the digital noise induced in the ground and power supply lines.
4. The clock starts 25nsec after the "0" to "1" transition of the CONVERT COMMAND.
5. **Parallel Output Data:** The Successive Approximation Register (SAR) is reset 26nsec after the leading edge of the first clock period in the conversion cycle. The MSB is set to logic "0" and all other bits are set to logic "1". The bits are determined in succession starting with the MSB, Bit 1, as shown in Figure 2. Each bit will be valid 26nsec after its corresponding clock pulse.

   The falling edge of the STATUS signal should not be used to strobe parallel data out of the ADC803

directly. The table in Figure 2 indicates that the falling edge of STATUS may occur prior to bit 12 data becoming valid.

6. **Serial Output Data:** The serial output is indeterminate until Bit 1 is valid, which occurs 26nsec after the leading edge of the second clock pulse. The remaining bits (Bits 2 through 12) are valid in succession for one clock period each beginning 26nsec after the leading edge of each clock pulse.
7. STATUS goes high 26nsec after the leading edge of the first clock pulse and goes low 18nsec after the leading edge of the last clock pulse.
8. Bit 12 will become valid at about the same time STATUS goes low and a new conversion can be initiated at anytime after the output data has been read.
9. The converter may be restarted during a conversion. When CONVERT COMMAND makes a "0" to "1" transition after the minimum set-up time, the SAR will be reset and a new conversion will start regardless of the state of the converter prior to the CONVERT COMMAND being received.

Figures 3, 4, and 5 are photographs of the actual pulse shapes and relationships.

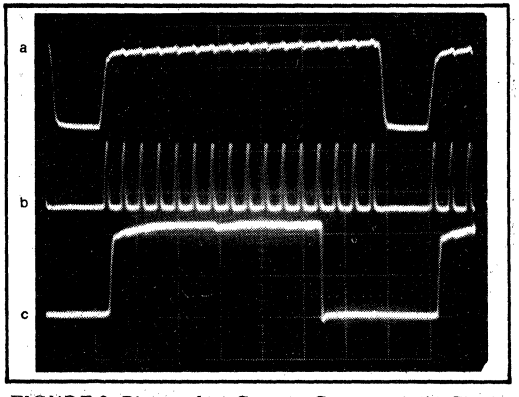


FIGURE 3. Photo of (a) Convert Command, (b) Clock, and (c) Status (200nsec/div).

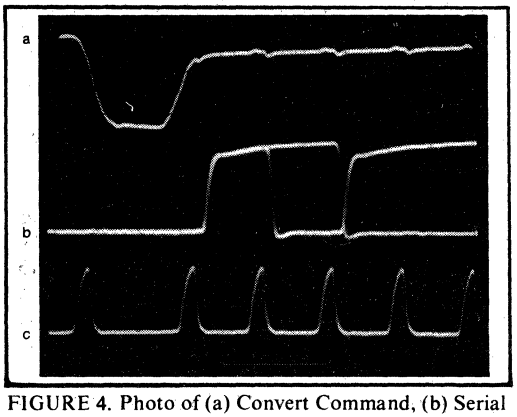


FIGURE 4. Photo of (a) Convert Command, (b) Serial Out, and (c) Clock (50nsec/div).

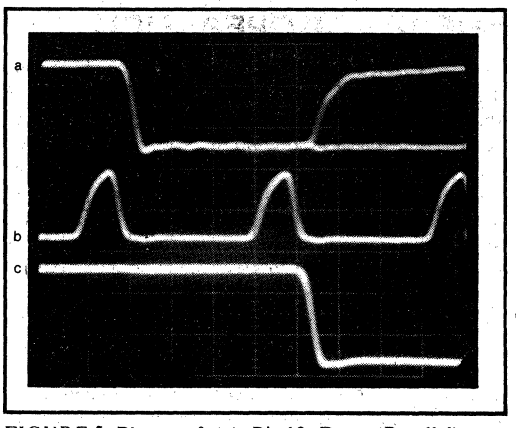


FIGURE 5. Photo of (a) Bit-12 Data (Parallel), (b) Clock, and (c) Status (20nsec/div).

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC803 parallel output; they are complementary straight binary (Logic "0" true) for unipolar input signal ranges and bipolar offset binary (Logic "1" true) for bipolar input signal ranges. Binary two's complement may be obtained for bipolar input ranges by inverting the MSB. It should be noted that for unipolar input ranges -10 volts is full scale.

Table I shows the LSB, transition values, and code definitions for each possible analog signal range.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Analog Input Voltage Range	±10V	±5V	0 to -10V
Code Designation	BOB(1) or BTC(2)	BOB or BTC	CSB(3)
One Least Significant Bit (LSB)	4.88mV	2.44mV	2.44mV
Transition Values MSB LSB(4)			
000...000 ↔ 000...001	-10V + 1/2LSB	-5V + 1/2LSB	-10V + 3/2LSB
011...111 ↔ 100...000	-1/2LSB	-1/2LSB	-5V + 1/2LSB
111...110 ↔ 111...111	+10V - 3/2LSB	+5V - 3/2LSB	−1/2LSB

NOTES: 1. BOB = Bipolar Offset Binary.
2. BTC = Binary Two's Complement (obtained by inverting the most significant bit (pin 1).
3. CSB = Complementary Straight Binary.
4. Voltages given are the nominal value for the transition from the next lower code.

Serial Data (NRZ)

Two binary codes are available on the serial output line; they are complementary straight binary (CSB) for unipolar input ranges and bipolar offset binary (BOB) for bipolar input signal ranges. The serial data is available

only during conversion and appears with the MSB first. See the timing diagram and discussion under "timing considerations" for more detailed information.

The LSB and transition values shown in Table I. also apply to the serial data output, except serial output does not have a BTC code.

DISCUSSION OF SPECIFICATIONS

The ADC803 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are Linearity, Drift, Gain and Offset errors, and Conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.05% of FSR at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10, 11, and 12.

ACCURACY VERSUS CONVERSION TIME

In successive approximation A/D converters, the conversion time affects Linearity and Differential Linearity errors. Conversion time and its effect on Linearity and Differential Linearity errors for the ADC803 are shown in Figure 6.

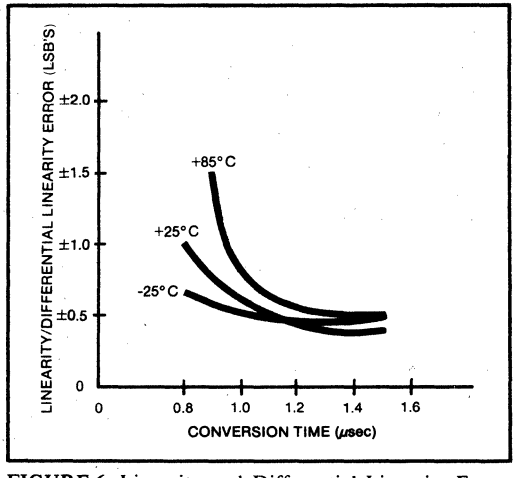


FIGURE 6. Linearity and Differential Linearity Error versus Conversion Time.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

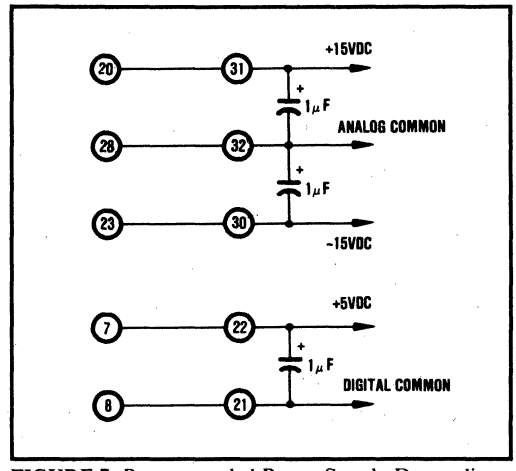


FIGURE 7. Recommended Power Supply Decoupling.

LINEARITY ERROR

Linearity error is not adjustable by the user and is the most meaningful indicator of A/D converter accuracy. Linearity is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity describes the step size between transition values. A Differential Linearity error of ±1/2LSB indicates that the size of any step may not vary from 1LSB by more than ±1/2LSB.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

The ADC803 is a high speed analog-to-digital converter which requires more layout precautions than general purpose products.

The ADC803 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins must be connected together externally. The connection between the digital supply pins and the connection between the digital common pins must be as short as possible. The analog and digital commons are not connected together internally in the ADC803, but should be connected together externally to a ground plane.

Connecting all commons to a ground plane at the ADC803 is the best method to minimize noise and dissipate heat. Pin 8 (Digital Common) is internally connected to the case.

The ADC803 also has an analog common Sense input (pin 27) for the analog input. This sense pin must be

connected to analog common as close to the input signal source as possible or connected to the ground plane. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. Special attention should be taken to ensure that the clock noise on the +5V supply line does not couple into the analog inputs.

The Comparator input (pin 26) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by analog common or ±15VDC supply patterns. The Clock Output (pin 17) is sensitive to stray capacitance; capacitance on this pin could alter the clock wave shape.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF tantalum capacitors as shown in Figure 8 to obtain noise-free operation. These capacitors should be located close to the ADC.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signals as shown in Table II. See Figure 8 for circuit details.

TABLE II. ADC803 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 29 To	With Gain Adjust	Connect Pin 24 To	Connect Pin 25 To
±10V	BOB or BTC*	26	Yes	40Ω resistor in series with input signal	Gain Adjust Potentiometer
			No	Input Signal	Analog Common
±5V	BOB or BTC*	26	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal
0 to −10V	CSB	Analog Common	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal

*Obtained by inverting MSB (pin 1) externally.

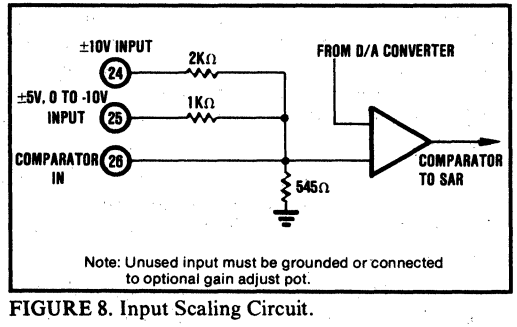


FIGURE 8. Input Scaling Circuit.

OUTPUT DRIVE

All ADC803 outputs except the clock will drive six TTL loads; the clock will drive three TTL loads. If long digital lines must be driven, external logic buffers are required particularly for the clock which is sensitive to capacitive loading.

INPUT IMPEDANCE

The source impedance to the ADC803 should be low, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the ADC803.

If this impedance is not low, a buffer amplifier should be added between the input signal and the ADC803 input as shown in Figure 9.

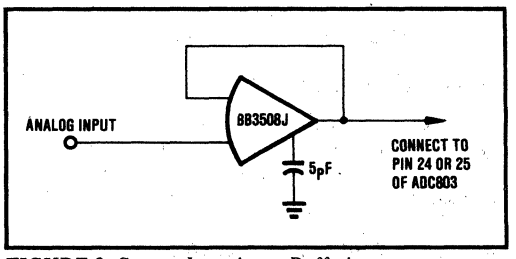


FIGURE 9. Source Impedance Buffering.

A common problem with successive approximation A/D converters is the transients in input current caused by the comparator input being switched back and forth. This requires a fast settling amplifier to drive the input.

The ADC803 comparator is connected in a differential mode (see Figure 8), greatly reducing the size of the input transients. The user, therefore, may use a low cost wideband monolithic amplifier to drive the ADC803. The small signal settling time of the amplifier should be less than 100nsec.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external trim potentiometers connected to the ADC as shown in Figures 10, 11, and 12. For proper gain adjust range a series resistor must be connected to the analog input pin as specified in Table II and shown in Figures 11 and 12. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. All resistors should be ±1% metal film or better. If the Offset adjust is not used, pin 26 should be left open except for bipolar operation when it is connected to pin 29. If the Gain adjust is not used, the unused input (pin 24 or 25) must be grounded to meet specified gain accuracy.

Adjustment Procedure

Refer to Table I for LSB voltages and transition values.

Unipolar offset - connect the offset potentiometer and resistors as shown in Figure 11, sweep the input through

the end point transition voltage, from 111...110 to 111...111. Adjust the Offset potentiometer until the actual end point transition voltage occurs at -1/2LSB.

Bipolar offset - connect the offset potentiometer and resistors as shown in Figure 10. Sweep the input through zero and adjust the offset potentiometer until the transition from 0111 1111 1111 to 1000 0000 0000 occurs at −1/2LSB.

Gain - connect the Gain potentiometer as shown in Figure 11 or 12. Sweep the input through the end point transition voltage that should cause an output transition from 000...000 to 000...001. Adjust the Gain potentiometer until this transition occurs at the correct end point transition voltage as given in Table I.

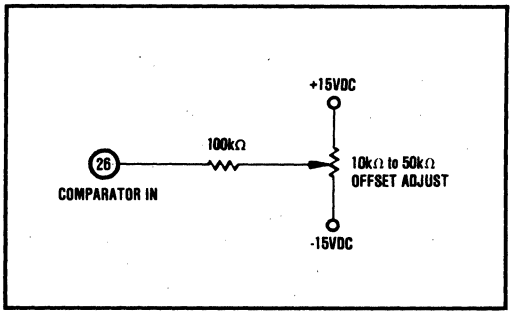


FIGURE 10. Optional Offset Adjust

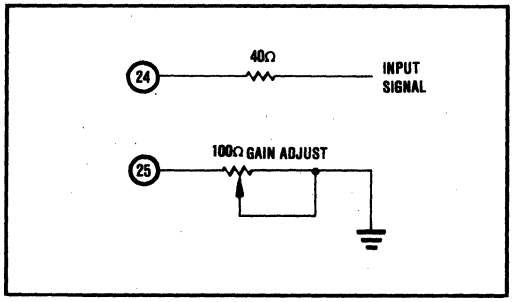


FIGURE 11. Optional Gain Adjust for ±10V Bipolar Operation.

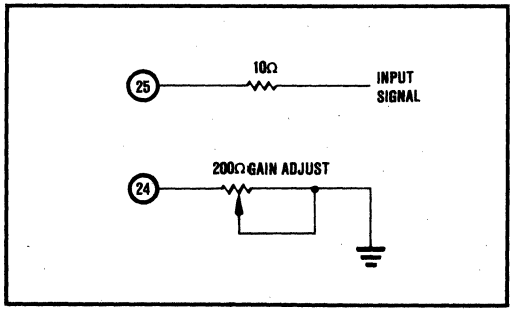


FIGURE 12. Optional Gain Adjust for ±5V Bipolar or 0 to -10V Unipolar Operation.

OPTIONAL CLOCK RATE CONTROL

The clock is factory-set for a conversion time between 1.3μsec and 1.5μsec. By use of the optional Clock Rate Control as shown in Figure 13, the Conversion time can be adjusted down to 0.8μsec for 12-bit resolution. If the optional Clock Rate Control is not used, pin 19 should be left open. Figure 14 shows Conversion Time versus Clock Rate Control voltage and Figure 6 shows Differential Linearity error versus Conversion time.

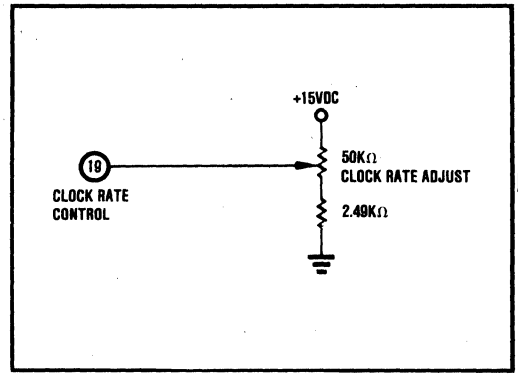


FIGURE 13. Optional Clock Rate Control.

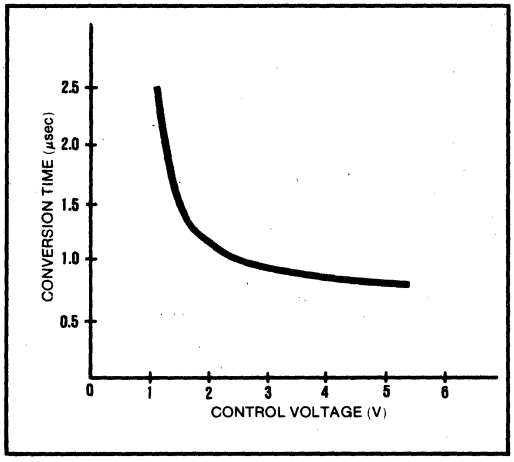


FIGURE 14. Conversion Time versus Clock Rate Control Voltage.

POWER DISSIPATION

The ADC803 dissipates approximately 1.9 watts (typical) and the package has a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above +85°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 15 for θ_{CA} requirements above +85°C. Improved thermal contact with the PC card copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16-square inch (minimum) area, this technique will allow operation to +100°C.

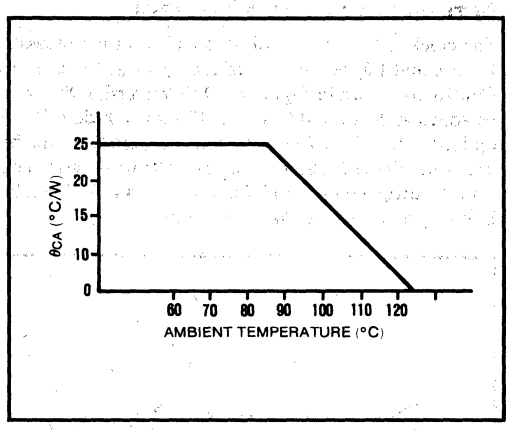


FIGURE 15. θ_{CA} Requirement Above +85°C.

EXTERNAL SHORT CYCLE

If less than 12 bits of resolution is required, the cycle time of the ADC803 can be shortened with the addition of two external components as shown in Figure 16. This circuit will create a shortened status signal directly proportional to the reduction of resolution. For n bits of resolution, the n+1 bit is used to create the falling edge of the shortened status signal. It is possible to obtain the equivalent of a 10-bit converter with 670nsec conversion time and an 8-bit converter with 500nsec conversion time using this short cycle technique and the external clock rate control shown in Figure 13. To begin a new conversion, simply give the converter a new convert command pulse. The SAR will reset and a new conversion will begin.

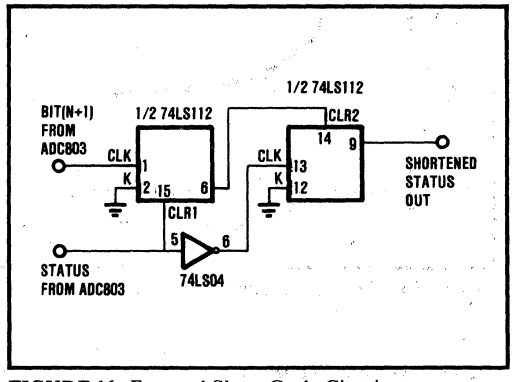


FIGURE 16. External Short Cycle Circuit.

TESTING OF THE ADC803

In order to validate the test results of the ADC803 obtained during final test, the customer must take extreme care in the design and layout of his test fixtures. Proper grounding, correct routing of analog and digital signals and power supply bypassing are crucial in achieving successful results.

ANALOG GROUND, DIGITAL GROUND, SENSE

Figure 17 shows a simplified model of the ADC depicting proper analog and digital grounding. Several analog and digital ground pins have been provided to allow for optimizing the internal layout of the ADC. As will be explained in more detail later, analog and digital grounds should be connected together only at one point by an extremely low resistive and inductive connection (a ground plane is ideal). A special analog ground called "sense" has been provided to eliminate the voltage drop that would otherwise be in the ground return of the R-2R ladder. Measuring the input signal with respect to the sense terminal makes the measurement independent of the impedance that is developed in the connection between the sense terminal and the analog ground, pin 28.

ANALOG-TO-DIGITAL CONVERTER TEST TECHNIQUE

A very effective way of determining the DC performance of an ADC is by using the "servo loop method." The block diagram of this technique is shown in Figure 18. This measurement system automatically locates the analog voltage that causes the digital output to alternate between the desired code and the adjacent code. The computer is programmed to place the desired code on the I/O bus which is one set of inputs to the digital comparator. The other set of inputs to this comparator is the digital output of the ADC. Depending upon the result of this comparison, the integrator is directed to change its output until an equilibrium state is achieved. Once in equilibrium, the DVM measures the analog input to the ADC and transmits the information to the computer via the IEEE-488 bus. The test program checks all the desired code combinations, verifying the performance of the ADC. Test time will range from 10 seconds to several minutes depending on the speed of the test program, settling time of the DVM, and number of codes to be checked.

GROUND LOOPS

Figure 19 illustrates the interaction that occurs between the analog and digital grounds when an ADC is connected into a test circuit. This interaction is created by ground loops. The circuit in Figure 19 shows how ground loops are created when the ADC tester combines digital and analog portions of the circuit together—in this case, the test signal generator (analog) and the digital circuitry that detects the ADC code which corresponds to the analog signal (digital). The ground loop exists when the digital ground connection between the ADC and the tester is in parallel with the analog grounds that connect the tester with the ADC. When the connection is made in this manner some of the digital current is diverted into the analog signal return, which creates a code-dependent error signal due to the resistance in the analog signal return. This error distorts the linearity measurement and induces hysterisis. The error can be substantially reduced if the analog and digital grounds are isolated from each other in the ADC tester.

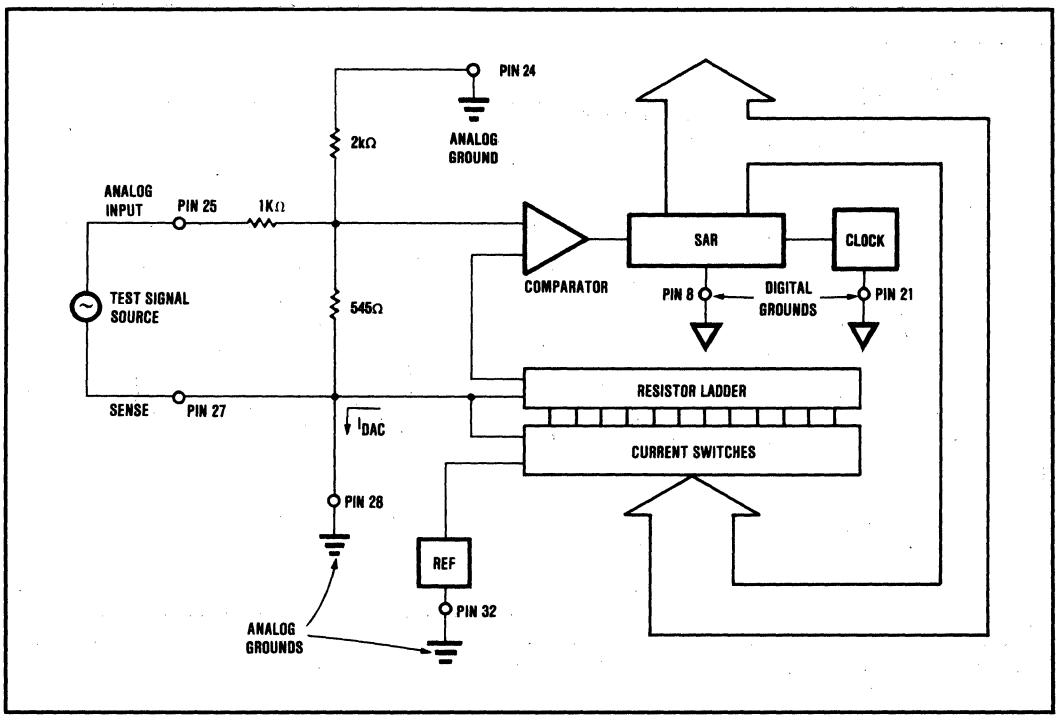


FIGURE 17. Simplified Model of ADC803 Depicting Proper Analog and Digital Ground.

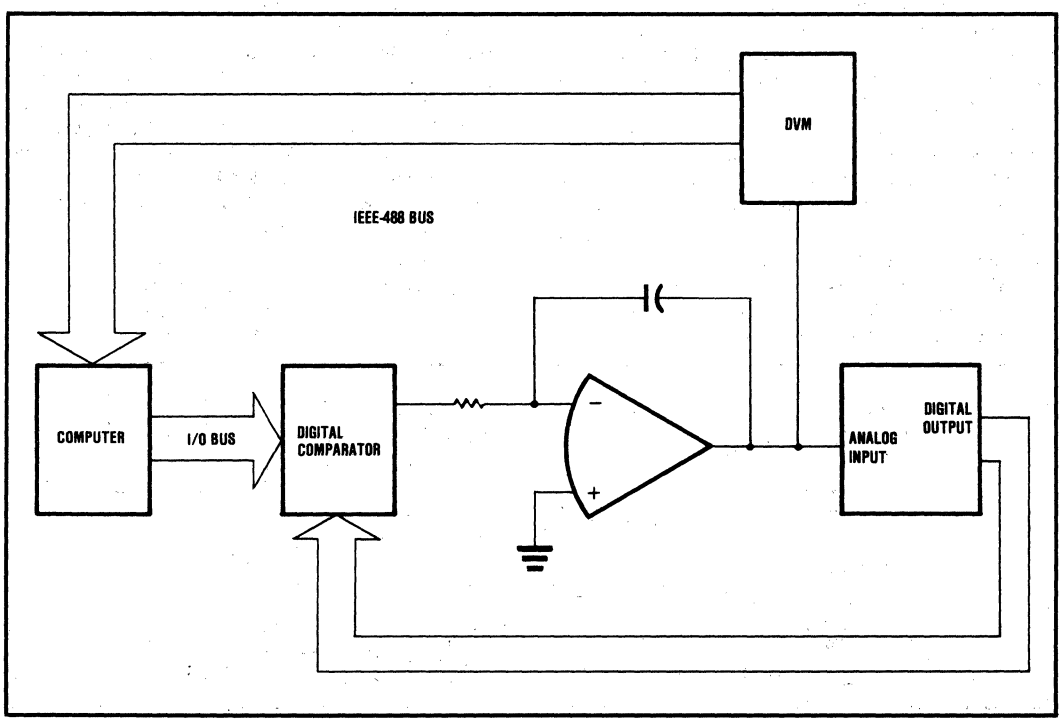


FIGURE 18. Servo Loop Analog-to-Digital Tester.

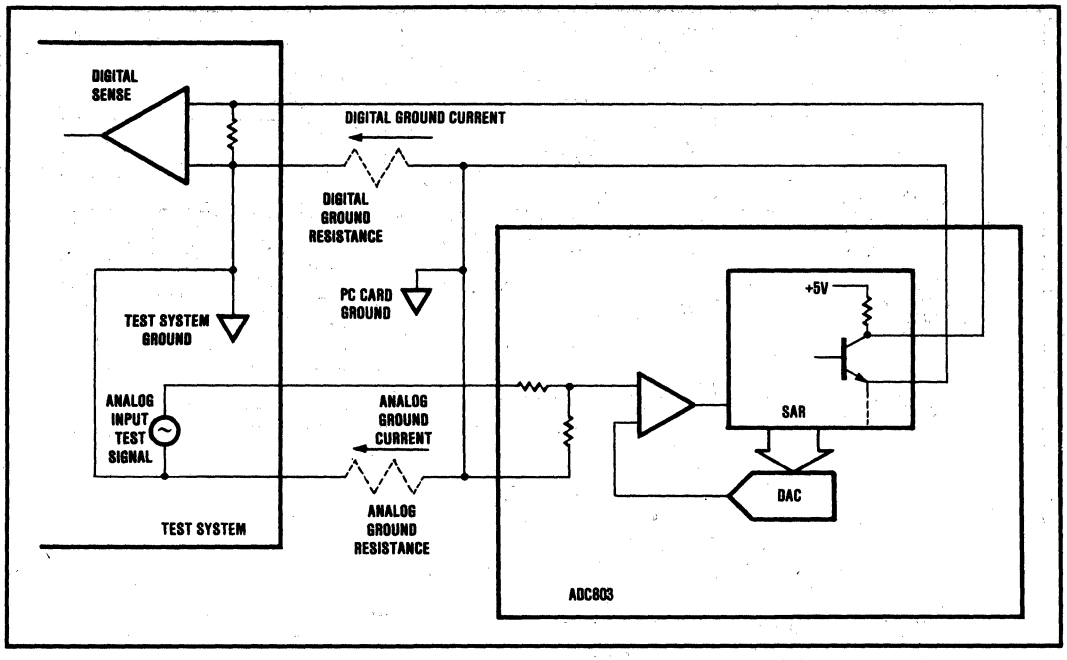


FIGURE 19. Ground Loop Interaction Between Analog and Digital Grounds When ADC Is Connected Into Test Circuit.

BEAT FREQUENCY TEST

A "beat frequency test" applied to an ADC803 with a companion sample/hold illustrates both an effective means of testing the high frequency performance of such a system and demonstrating that the ADC803 with its associated sample/hold is capable of digitizing high frequency signals cleanly. A sample/hold must be used when performing this test to hold the input of the ADC803 constant during the conversion time. Figure 20 is a block diagram of the beat frequency test set up.

The beat frequency test is useful for being able to rapidly determine whether there are any serious problems with the ADC. In this test the input frequency is set at slightly less than one-half the sampling rate. The slight difference is selected to allow the sample point to vary by 1LSB, or less, on successive samples. The data is clocked into a low frequency reconstruction DAC at one-half the sampling rate to enable viewing on an oscilloscope. Figure 21 is a photograph of the response to a full scale input sine wave centered around the MSB and Figure 22 is a photograph of the response of a small signal sine wave centered around the MSB. For comparison, a photograph (Figure 23) is included which shows the response of the ADC803 to a 125Hz input signal which is the same as the beat frequency.

Figure 24 is the PC card layout that was used for the beat frequency test. This layout demonstrates some of the layout practices that must be followed when using a high speed ADC like the ADC803.

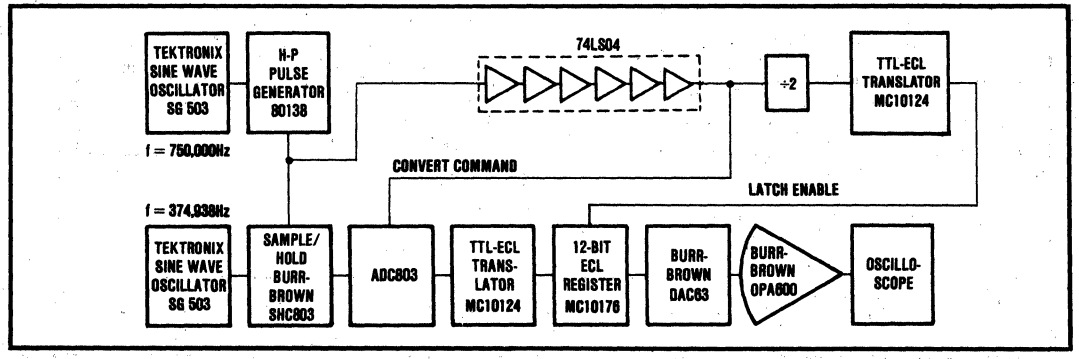


FIGURE 20. Block Diagram of Beat Frequency Test Circuit.

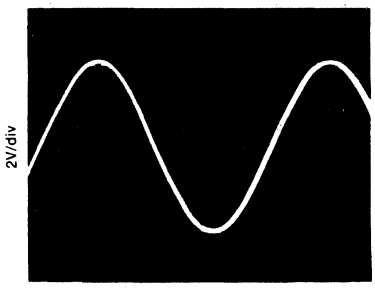


FIGURE 21. Beat Frequency Test Response of Full Scale Sine Wave Input.

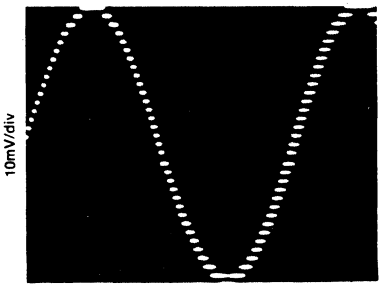


FIGURE 22. Beat Frequency Test Response of Small Signal Sine Wave Input.

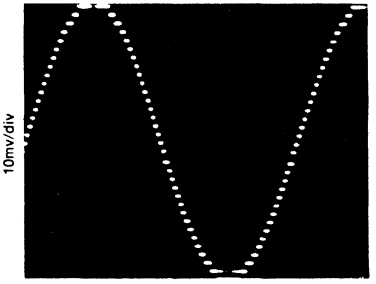
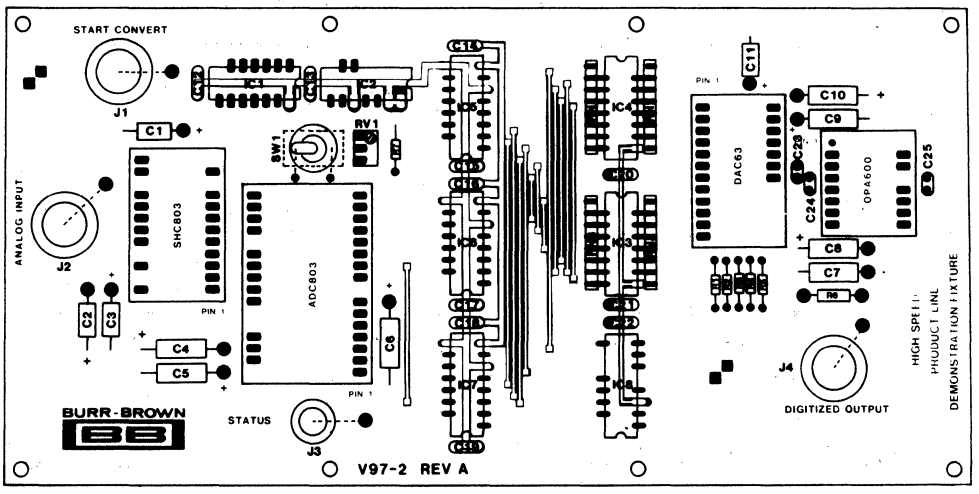
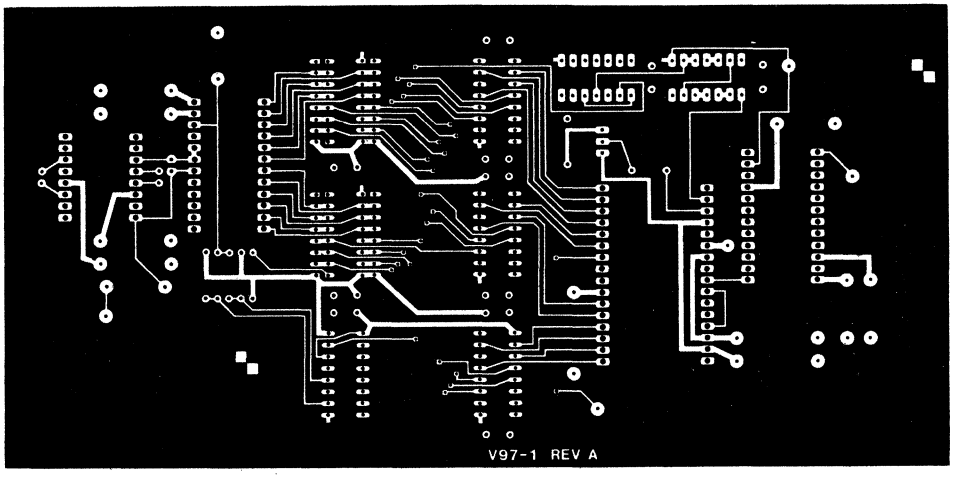


FIGURE 23. Response of Small Signal 125Hz Sine Wave Input.



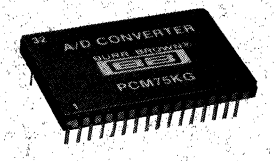
(a) Top View



(b) Bottom View

FIGURE 24. PC Board Layout for Beat Frequency Test Fixture.

BURR-BROWN®



PCM75
DESIGNED FOR AUDIO

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

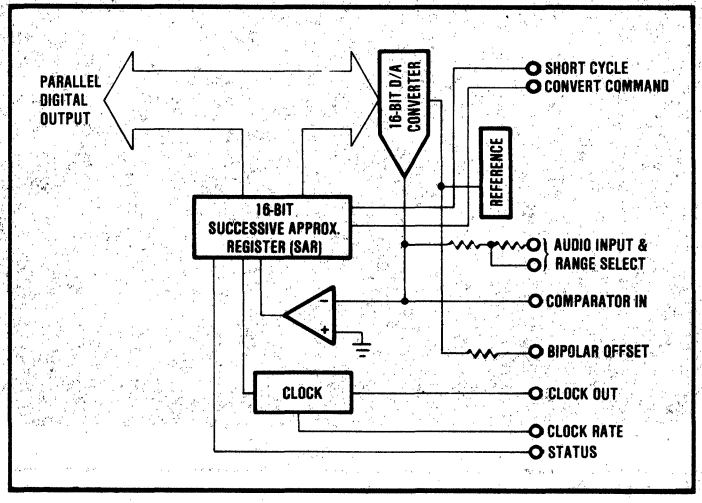
FEATURES

- 16-BIT RESOLUTION
- 90dB DYNAMIC RANGE
- 0.004% THD (FS Input, 16 Bits)
- 0.02% MAX THD (-15dB, 16 Bits)
- 17μsec MAX CONVERSION TIME (16 Bits)
- 15μsec MAX CONVERSION TIME (14 Bits)
- 8μsec CONVERSION (Reduced Specs)
- EIAJ STC-007-COMPATIBLE
- INTERNAL 16-BIT DAC AVAILABLE TO USER

DESCRIPTION

The PCM75 is designed for PCM Audio applications and is compatible with EIAJ STC-007 specifications. The internal 16-bit digital-to-analog converter is available for the designer to utilize in the playback mode, thus saving the cost of an additional DAC. The conversion time can be reduced from 15μsec to 8μsec with some increase in distortion. Distortion is specified on the data sheet to assure performance in critical audio applications.

The PCM75 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The PCM75 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a bottom-brazed ceramic 32-pin dual-in-line package. The converter is complete with internal reference and clock.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

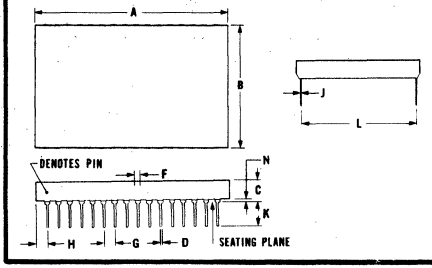
ELECTRICAL

At 25°C and rated power supplies unless otherwise noted.

MODEL	PCM75KG			PCM75JG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
DYNAMIC RANGE(1)		90			90		dB
INPUT							
ANALOG							
Voltage Ranges, Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL(2)							
Convert Command		Positive pulse 50nsec wide (min) trailing edge ("1" to "0" initiates conversion)					
Logic Loading			1			1	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±0.1(3)			±0.1(3)		%
Offset Error, Bipolar		±0.1(3)			±0.1(3)		% of FSR(4)
Differential Linearity Error (major carry)		±0.0015			±0.003		% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
TOTAL HARMONIC DISTORTION (THD)(1)							
V_{IN} = ±FS at f = 400Hz							
14-Bit Resolution		0.006			0.008		%
16-Bit Resolution		0.004			0.006		%
V_{IN} = -15dB at f = 400Hz							
14-Bit Resolution		0.025			0.03	0.05	%
16-Bit Resolution		0.015	0.02		0.021		%
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0.003		% of FSR/%V_S
+5VDC		0.001			0.001		% of FSR/%V_S
CONVERSION TIME(5) (14 Bits)			15			15	µsec
(16 Bits)			17				µsec
WARM-UP TIME	5			5			min
DRIFT							
Gain			±20			±20	ppm/°C
Offset, Bipolar			±15			±15	ppm of FSR/°C
OUTPUT							
DIGITAL							
All codes complementary							
Parallel							
Output Codes(6)							
Bipolar		COB, CTC(7)			COB, CTC(7)		
Output Drive	2			2			TTL Loads
Status		Logic "1" during conversion			Logic "1" during conversion		
Status Output Drive	2			2			TTL Loads
Internal Clock							
Clock Output Drive	2			2			TTL Loads
Frequency(8)		933			933		kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		1.55			1.55		W
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+45			+45		mA
Supply Drain -15VDC		-35			-35		mA
Supply Drain +5VDC		+70			+70		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (derated specs)	-25		+85	-25		+85	°C
Storage	-55		+100	-55		+100	°C

NOTES:
1. The measurement of total harmonic distortion (THD) and Dynamic Range is highly dependent on the characteristics of the sample/hold amplifier, the digital-to-analog converter, the deglitcher, and the low-pass filter. To accurately measure THD and Dynamic Range, the accuracy of each device should be better than 16-bit accuracy. A block diagram showing the measurement technique Burr-Brown uses is shown in Figure 4.
2. DTL/TTL compatible, i.e., Logic "0" = 0.8V max. Logic "1" = 2.0V min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.
3. Adjustable to zero. (See "Optional External Gain and Offset Adjustment.")
4. FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR.
5. Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Additional Optional Connections" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified max conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to bit 15 (pin 15) for 14-bit resolution.
6. See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.
7. CTC coding obtained by inverting MSB (pin 1).
8. Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 12 and 13 and Table III.

MECHANICAL



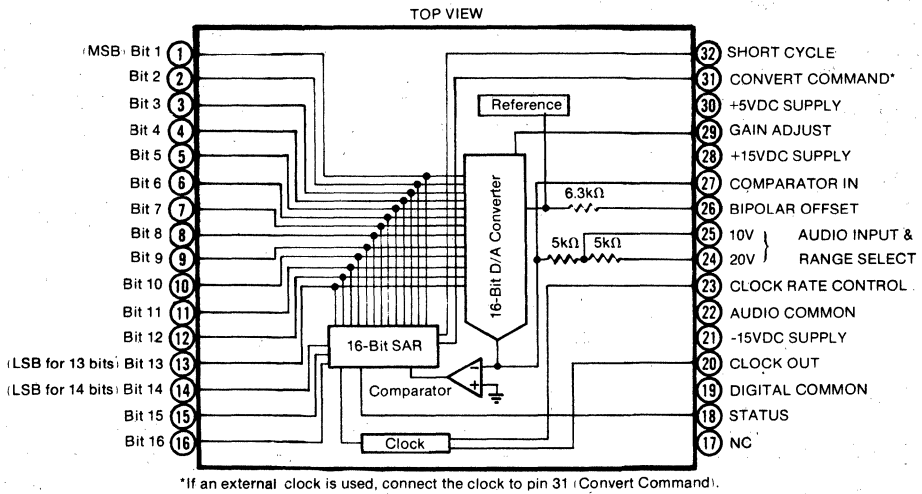
Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Ceramic
MATING CONNECTOR:
2302MC
WEIGHT: 13 grams (0.46oz.)
HERMETICITY:
Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

LEADS IN TRUE POSITION WITHIN .010" (.25 MM) R @ MMC AT SEATING PLANE

CONNECTION DIAGRAM



*If an external clock is used, connect the clock to pin 31 (Convert Command).

THEORY OF OPERATION

The accuracy of a successive-approximation A/D converter is described by the transfer function shown in Figure 1. All successive-approximation A/D converters have an inherent Quantization Error ±1/2LSB. The remaining errors in the A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off), and Offset drift shifts the line left or right over the operating temperature range. Total Harmonic Distortion (THD) is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error, that is useful in Audio Applications. To be useful, THD should be specified for both high level and low level input

signals. This error is unadjustable and is the most meaningful indicator of A/D converter accuracy for Audio Applications. The resolution of an A/D converter can be expressed in terms of Dynamic Range. The Dynamic Range is a measure of the ratio of the smallest signals the converter can resolve to the full scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution, or 96dB for a 16-bit converter. The actual or useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

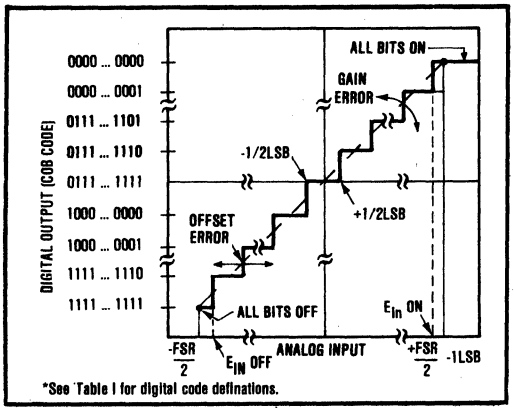


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exits. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output).

DEFINITION OF DIGITAL CODES

Parallel Data

Two binary codes are available on the PCM75 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (pin1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 14-, 15-, and 16-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±5V input.

DISCUSSION OF SPECIFICATIONS

The PCM75 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter in audio applications are total harmonic distortion, drift, gain and offset errors, and conversion time effects on accuracy. The ADC is factory-trimmed and tested for all critical key specifications.

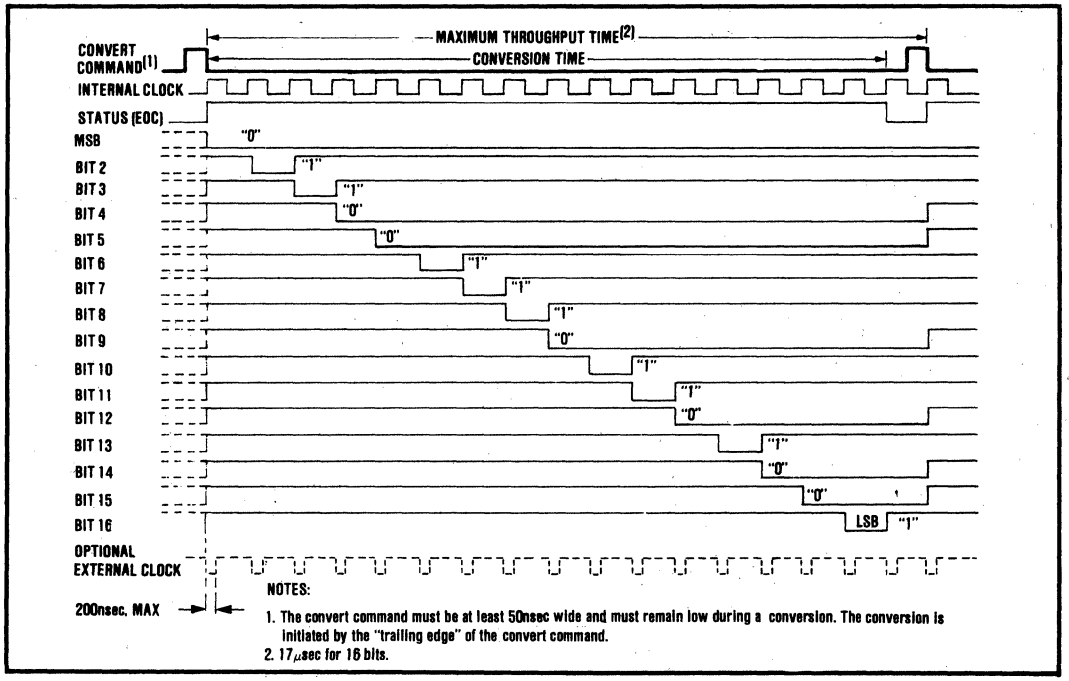


FIGURE 2. Timing Diagram.

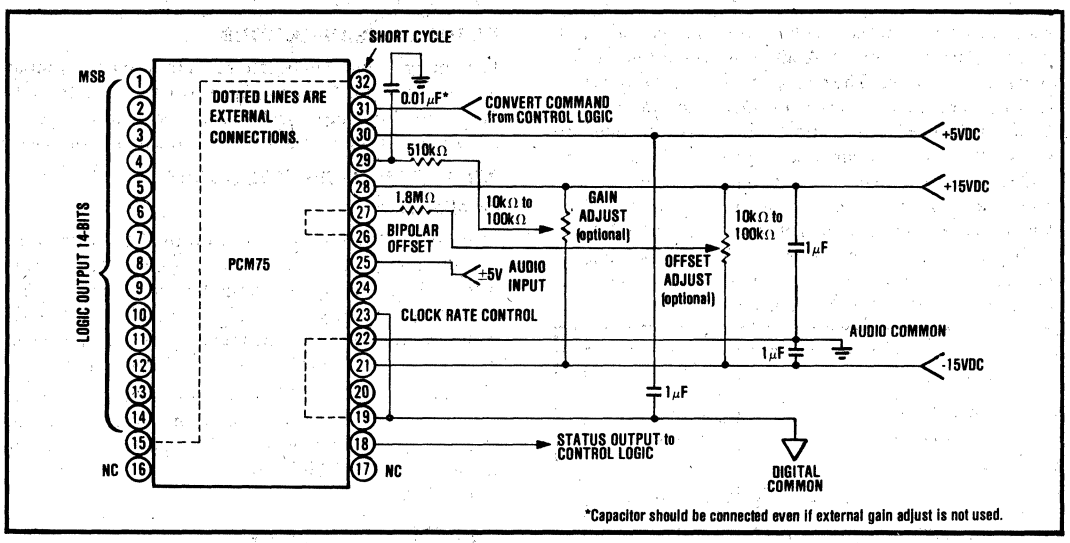


FIGURE 3. PCM75 Connections For: ±5V Audio Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Audio Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 16	305μV	153μV	77μV	153μV	77μV	305μV
	n = 15	610μV	305μV	153μV	305μV	153μV	610μV
	n = 14	1.22mV	610μV	305μV	6.0μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

(1) COB = Complementary Offset Binary
(2) CTC = Complementary Two's Complement - obtained by inverting the most significant bit, MSB (pin 1).
(3) CSB = Complementary Straight Binary
(4) Voltages given are the nominal value for transition to the code specified.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10 and 11.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM75 power supply sensitivity is specified for ±0.003% of FSR/%V, for ±15VDC supplies and ±0.0015% of FSR/%V, for +5VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics to the value of the rms fundamental and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM75 is shown in Figure 4 along with a timing diagram for the control logic. If we assume that the error due to the test circuit is negligible, then the rms value of the PCM75 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2}$$

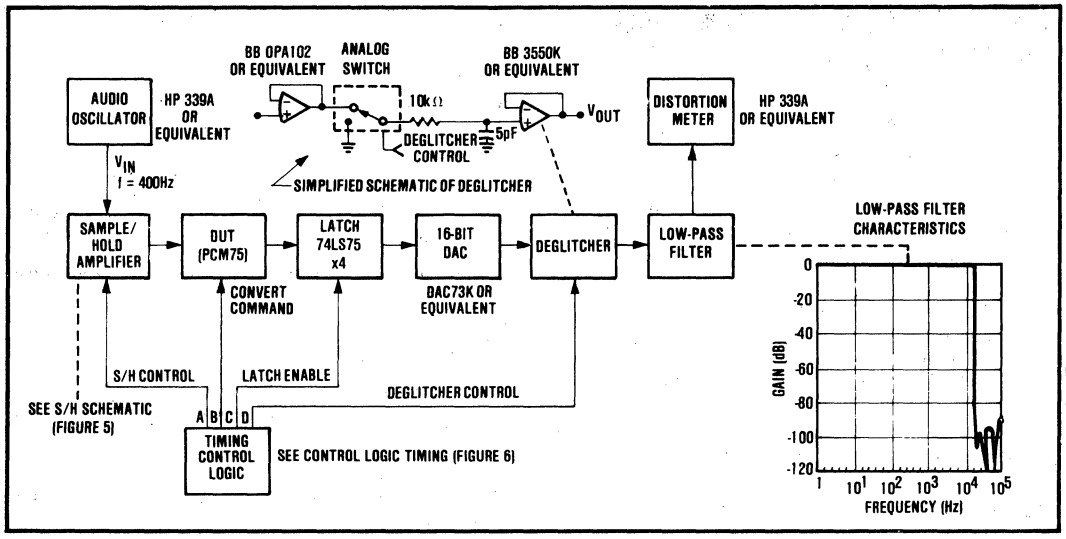


FIGURE 4. Block Diagram of Distortion Test Circuit.

where N is the number of samples, $E_L(i)$ is the linearity error of the PCM75 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\%$$

This expression indicates that there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the A D is directly correlated to the THD because the digital output words from the A D vary according to the amplitude and frequency of the sine wave input as well as the sampling frequency.

For the PCM75 the test sampling period was chosen to be 22.7μsec which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 400Hz and the amplitude of the input signal is 0dB (full scale) and -15dB.

ACCURACY VS CONVERSION TIME

Figures 14 and 15 show the relationship of THD vs input voltage level for the PCM75 with both 14-bit and 16-bit resolution and conversion times of 8μsec and 15μsec. Notice that the distortion level is reduced by increasing the resolution from 14 to 16 bits due to the reduced quantization error. Conversely, decreasing the conversion time of the PCM75 from 15μsec to 8μsec increases the distortion level due to dynamic linearity errors resulting from insufficient settling time for the internal D A converter and comparator.

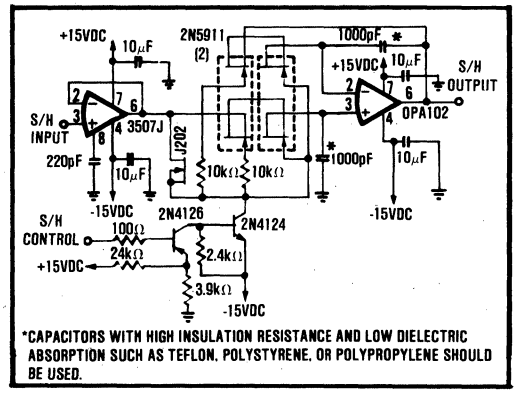


FIGURE 5. Schematic of Sample/ Hold Amplifier.

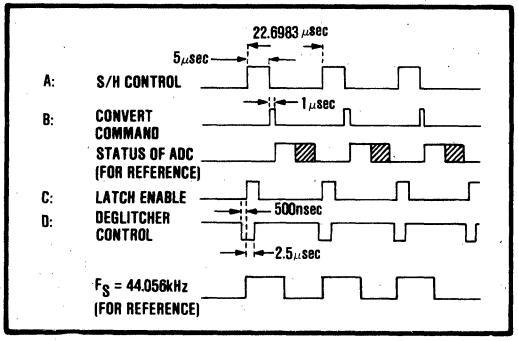


FIGURE 6. Control Logic Timing for PCM75 Distortion Test Circuit.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and Digital Common are not connected internally in the PCM75 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC. Bypass the 1μF electrolytic type capacitors with 0.01μF ceramic capacitors for improved high frequency performance.

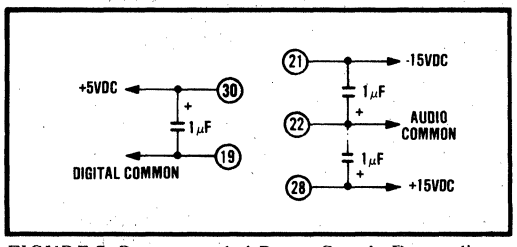


FIGURE 7. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

TABLE II. PCM75 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB (pin 1).

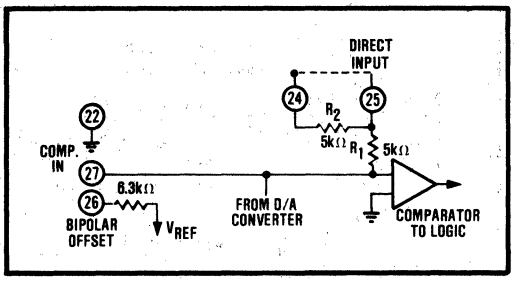


FIGURE 8. PCM75 Input Scaling Circuit.

INPUT IMPEDANCE

The input signal to the PCM75 should come from a low impedance source, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the PCM75.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the PCM75 as shown in Figure 9.

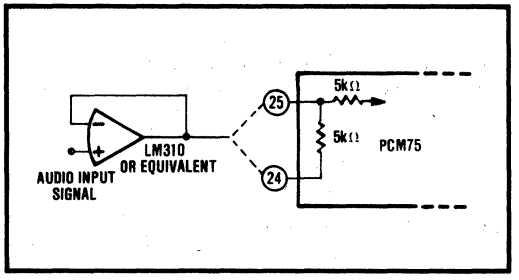


FIGURE 9. Buffer Amplifier for PCM75 Input.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 10 and 11. Multiturn potentiometers with 100ppm °C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 10. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

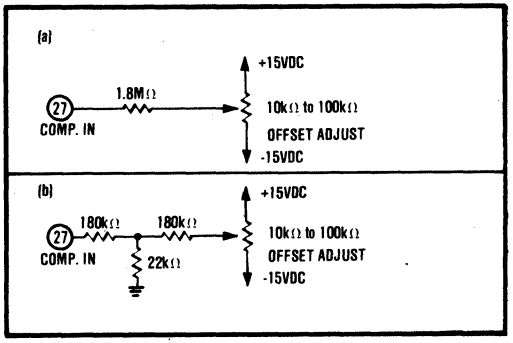


FIGURE 10. Two Methods of Connecting Optional Offset Adjust.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 11. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}. Table I details the transition voltage levels required.

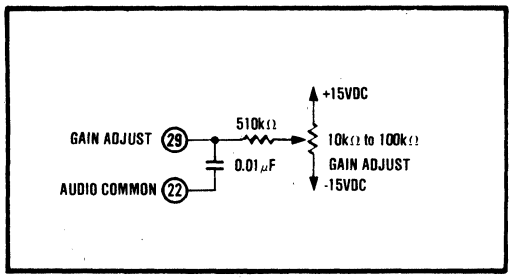


FIGURE 11. Connecting Optional Gain Adjust.

OUTPUT DRIVE

Normally all PCM75 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

ADDITIONAL OPTIONAL CONNECTIONS

The PCM75 may be operated with faster conversion times for resolutions less than 14 bits, if a higher THD is acceptable, by connecting the Clock Rate (pin 23) and the Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

TABLE III. Short Cycle and Clock Rate Control Connections for 12- to 16-Bit Resolutions.

Resolution Bits	16	15	14	13	12
Connect Pin 32 to	Open	Pin 16	Pin 15	Pin 14	Pin 13
Connect Pin 23 to	Pin 19	Pin 19	Pin 19	Pin 30	Pin 30
Conversion Time (Typical) μsec	17	16	15	10	8

If a more precise adjustment of conversion time is desired than can be obtained by simply connecting the Clock Rate (pin 23) to Digital Common or +5V, as indicated in Table III, the Clock Rate pin may be connected to an external multiturn trim potentiometer with a TCR of ±100ppm °C or less as shown in Figure 12. The typical conversion time vs the Clock Rate Control voltage is shown in Figure 13. The effect of varying the conversion time and the resolution on the total harmonic distortion is shown in Figures 14 and 15.

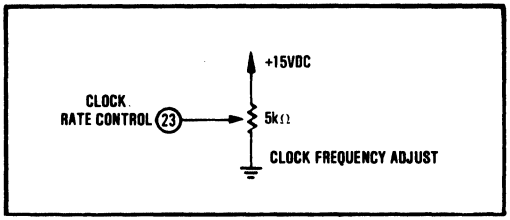


FIGURE 12. Clock Rate Control, Optional Fine Adjust.

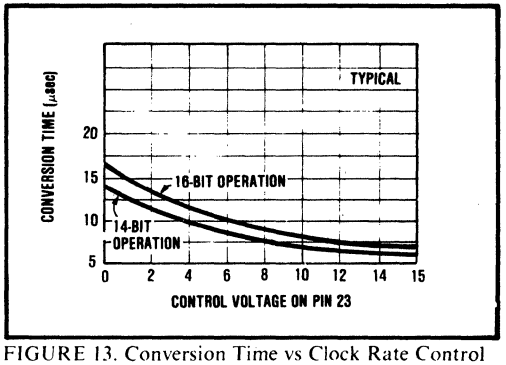


FIGURE 13. Conversion Time vs Clock Rate Control Voltage.

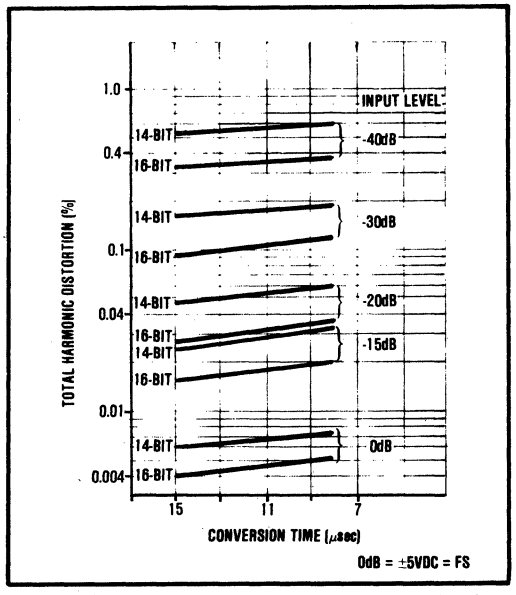


FIGURE 14. Total Harmonic Distortion vs Conversion Time.

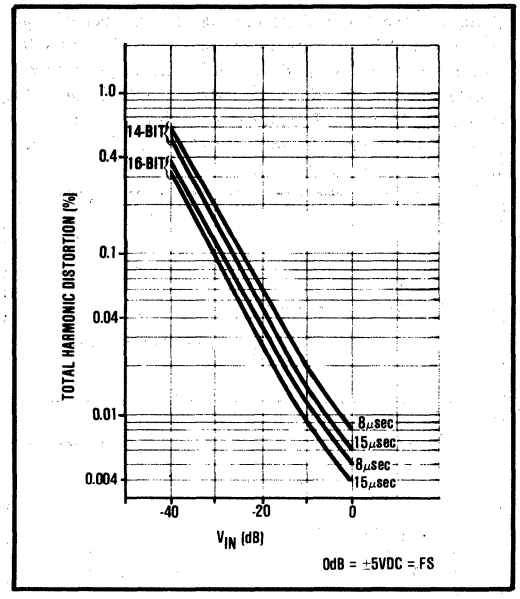


FIGURE 15. Total Harmonic Distortion vs Input Voltage Level.

EXTERNAL CLOCK

If an external clock is used, connect it to the Convert Command, pin 31. The convert command waveform as shown in Figure 2 is then not used on pin 31. The internal clock signal will still appear on pin 20 and its waveform can vary from that shown in Figure 2. The external clock pulse, as applied to pin 31, must be a negative-going pulse with a width between 100nsec and 200nsec as shown in Figure 2 and in Figures 16, 17, and 18.

Figure 16 shows continuous conversion using an external clock waveform, with the correct duty cycle applied directly to pin 31. A new conversion will automatically be initiated by the (n + 2) clock pulse where n is the resolution of the PCM75.

Figure 17 shows how to shape the waveform to apply to pin 31 when using an external clock that has an arbitrary duty cycle.

Figure 18 shows how to obtain continuous external clock conversion initiated by the rising edge of an external clock pulse only when an additional convert command pulse is high.

In all cases when using an external clock, the frequency of the external clock must be lower than the frequency of the internal clock. The internal clock normally runs at 933kHz when the Clock Rate Control, pin 23, is connected to digital common. Higher internal clock frequencies can be obtained by connecting the Clock Rate Control, pin 23, to positive voltages; +5V is often convenient to use. See Figure 13 for relative increases.

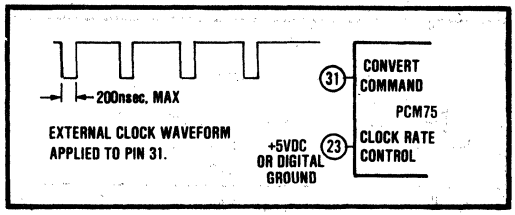


FIGURE 16. Continuous Conversion Using an External Clock.

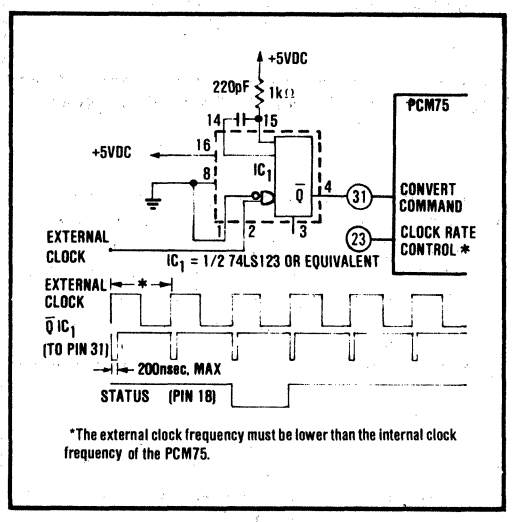


FIGURE 17. Continuous Conversion Using an External Clock That Has an Arbitrary Duty Cycle.

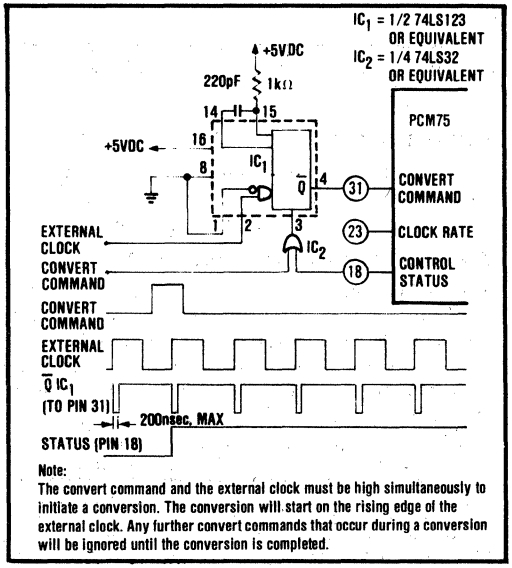


FIGURE 18. Continuous Conversion Initiated by the Rising Edge of an External Clock Pulse, Only When an Additional Convert Command Signal is High.

DESCRIPTION OF A/D - D/A OPERATION

The PCM75 was designed so that the internal D/A converter can be made available to the user as shown in Figure 19. The D A converter portion of the PCM75 requires only ±15VDC supplies and analog common for operation. Therefore, floating the +5VDC supply pin (pin 30) turns off the internal clock, successive approximation register (SAR), and comparator without affecting the operation of the DAC. Note that the +5VDC line must appear as a high impedance to the PCM75 or damage may result to the SAR digital outputs when they are used as digital inputs for operation of the D/A converter.

This circuit provides a low cost alternative to using a separate A/D and D/A converter in applications where the operation of only one device is required at any given time. The current settling time of the D/A portion of the PCM75 is about 1μsec to within ±0.003% of the final value. The voltage settling time is dependent upon the characteristics of the output amplifier (A_1).

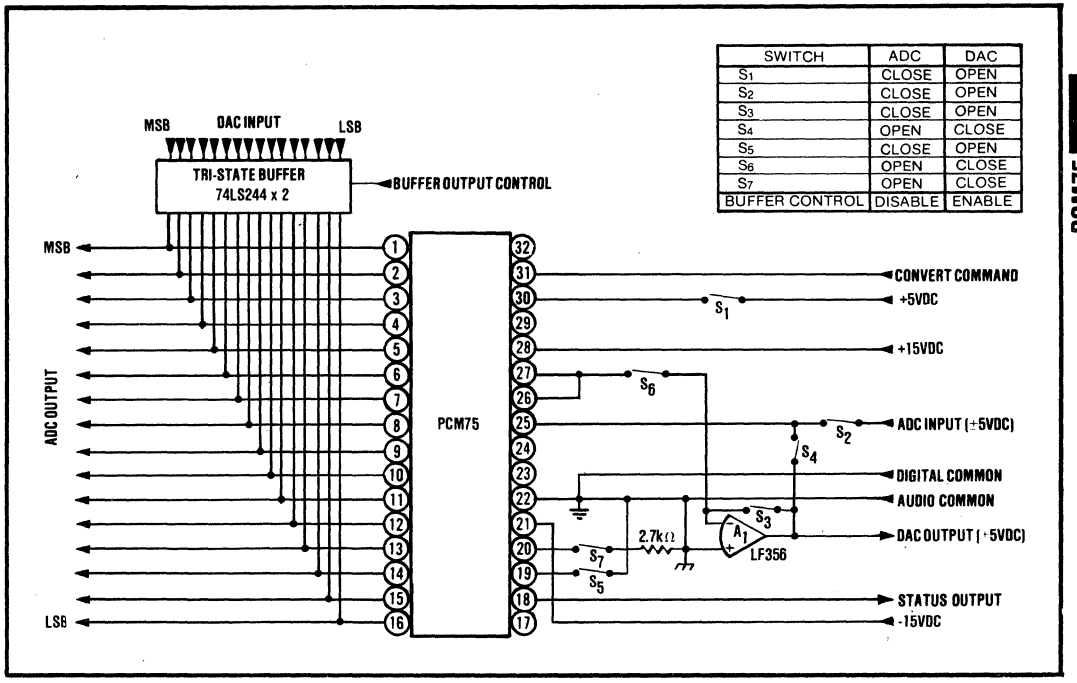
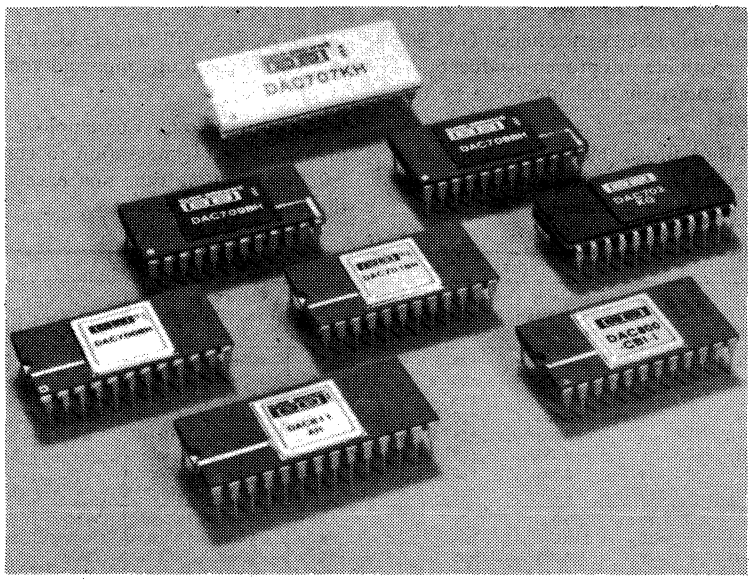


FIGURE 19. PCM75 Used Both as an A D Converter and as a D A Converter.

DIGITAL-TO-ANALOG CONVERTERS



The Burr-Brown digital-to-analog converter product line contains a broad variety of products designed to simplify your task of converting digital information to analog form. The available products provide resolutions ranging from 8 bits to 16 bits, and encompass a variety of performance features and package types engineered to meet your needs for accuracy and reliability at low cost.

These products are designed to ease the task of application. Most units are complete, requiring no external components to achieve the desired function. All the D/A converters listed in this section include an internal reference and most have an output voltage amplifier, although the line also includes current output versions carefully designed for applications requiring current outputs, such as driving displays.

For low-cost general-purpose applications, consider the pin-compatible DAC800 and DAC80. If you require high resolution and accuracy, such as in test equipment and high performance instrumentation, the DAC700 and DAC70 families provide a variety of alternatives. Need high speed? Try the ECL-compatible DAC63 or TTL-compatible DAC812. The PCM52 and PCM53 have been optimized to provide 16-bit resolution with very low total harmonic distortion, required in audio and acoustic applications. Recent additions to the line include DAC708/709 and DAC811, designed for complete microprocessor compatibility. Refer to the Selection Guide in this section for a complete listing of available products.

Whether your system requires low cost, high resolution, high speed, wide temperature range, or low drift, consider Burr-Brown—a world leader in D/A converters.

SELECTION GUIDE

DIGITAL-TO-ANALOG CONVERTERS

Our DAC80 is a standard in 12-bit performance. DAC800 —a monolithic IC—continues this proven product offering the same pinout, functions and improved performance at a lower price.

16-bit designs from Burr-Brown have also set industry standards: DAC71 is the industry standard low-cost 16-bit D/A; DAC701 and DAC703 are complete 16-bit monolithics with op amps and voltage reference on the chip.

ECL-compatible DAC63 employs new technology and higher levels of integration to achieve 35nsec (typ to ±0.012%) settling time and excellent temperature and time stability at low cost.

DIGITAL-TO-ANALOG CONVERTERS									
Description	Model[1]	Resolution (Bits)	Linearity Error max (% of FSR)	Accy. Drift Bipolar, max (ppm FSR/°C)	Output Ranges	Settling Time (FSR, ±1/2LSB)	Temp Range [2]	Package	Page
High Resolution Monolithic	DAC700KH	16	±0.003	±28	0 to −2mA	350nsec	Com		6-107
	DAC700BH	16	±0.003	±28	0 to −2mA	350nsec	Ind		6-107
	DAC701KH	16	±0.003	±28	0 to +10V	4µsec	Com	Ceramic	6-107
	DAC701BH	16	±0.003	±28[3]	0 to +10V	4µsec	Ind	24-pin	6-107
	DAC702KH	16	±0.003	±25[3]	±1mA	350nsec	Com	DIP	6-107
	DAC702BH	16	±0.003	±25	±1mA	350nsec	Ind		6-107
	DAC703KH	16	±0.003	±25	±10V	4µsec	Com		6-107
	DAC703BH	16	±0.003	±25	±10V	4µsec	Ind		6-107
High Resolution Microprocessor Compatible	DAC706KH	16	±0.003	±25	0 to −2mA	4µsec	Com	Ceramic	6-115
	DAC706BH	16	±0.003	±25	±1mA	4µsec	Ind	Hermetic	6-115
	DAC707KH	16	±0.003	±25	±5V, ±10V	4µsec	Com	28-pin	6-115
	DAC707BH	16	±0.003	±25	0 to +10V	4µsec	Ind	DIP	6-115
	DAC708KH	16	±0.003	±25	0 to −2mA	4µsec	Com	Ceramic	6-115
	DAC708BH	16	±0.003	±25	±1mA	4µsec	Ind	Hermetic	6-115
	DAC709KH	16	±0.003	±25	0 to +10V	4µsec	Com	24-pin	6-115
	DAC709BH	16	±0.003	±25	0 to +10V	4µsec	Ind	DIP	6-115
Monolithic[4] 12-Bit	DAC800-CBI-I	12	±0.012	±25[4]	±1, −2mA	300nsec	Com	Ceramic	6-126
	DAC800-CBI-V	12	±0.012	±25	±2.5, ±5, ±10, +5, +10V	3µsec	Com	24-pin DIP	6-126
	DAC800P-CBI-V	12	±0.012	±25	±2.5, ±5, ±10, +5, +10V	3µsec	Com	Plastic	6-126
	DAC850-CBI-I	12	±0.012	±17[4]	±1, −2mA	300nsec	Ind	Ceramic	6-147
	DAC850-CBI-V	12	±0.012	±17	±2.5, ±5, ±10, +5, +10V	3µsec	Ind	Hermetic 24-pin DIP	6-147
	DAC851-CBI-I	12	±0.012	±30[4]	±1, −2mA	300nsec	MIL	Ceramic	6-147
	DAC851-CBI-V	12	±0.012	±30	±2.5, ±5, ±10, +5, +10V	3µsec	MIL	Hermetic 24-pin DIP	6-147
Microprocessor Compatible	DAC811AH	12	±0.012	±30	±5, ±10, +10V	4µsec	Ind	Ceramic	6-133
	DAC811BH	12	±0.006	±20	±5, ±10, +10V	4µsec	Ind	24-pin	6-133
	DAC811KH	12	±0.012	±30	±5, ±10, +10V	4µsec	Ind	DIP	6-133
	DAC811SH	12	±0.006	±20	±5, ±10, +10V	4µsec	Ind		6-133
Low Cost	DAC80-CBI-I[5]	12	±0.012	±25[6]	±1.0, −2mA	300nsec	Com		6-77
	DAC80-CBI-V[5]	12	±0.012	±25	±2.5, ±5, ±10, +5, +10V	3µsec	Com	Ceramic 24-pin	6-77
	DAC80-CCD-I[5]	3 digits	±0.025	±25[6]	0 to −2mA	300nsec	Com	DIP	6-77
	DAC80-CCD-V[5]	3 digits	±0.025	±25	0 to +10V	3µsec	Com		6-77
Low Drift	DAC85-CBI-I, (Q)	12	±0.012	±20[6]	±1.0, −2mA	300nsec	Ind		6-94
	DAC85-CBI-V, (Q)	12	±0.012	±20	±2.5, ±5, ±10, +5, +10V	3µsec	Ind		6-94
	DAC85C-CBI-I, (Q)	12	±0.012	±30[6]	±1.0, −2mA	300nsec	Com	Metal Hermetic 24-pin	6-94
	DAC85C-CBI-V, (Q)	12	±0.012	±30	±2.5, ±5, ±10, +5, +10V	3µsec	Com	DIP	6-94
	DAC85LD-CBI-V	12	±0.012	±5	±2.5, ±5, ±10, +5, +10V	3µsec	Ind		6-94

DIGITAL-TO-ANALOG CONVERTERS									
Description	Model[1]	Resolution (Bits)	Linearity Error max (% of FSR)	Accy. Drift Bipolar, max (ppm FSR/°C)	Output Ranges	Settling Time (FSR, ±1/2LSB)	Temp Range[2]	Package	Page
High Resolution	DAC70-CSB-I	16	±0.003	±7[6]	0 to −2mA	50µsec	Ind	Metal Hermetic 24-pin DIP	6-26
	DAC70-COB-I, (Q)	16	±0.003	±7[6]	±1mA	50µsec	Ind		6-26
	DAC71-CSB-I	16	±0.003	±15[6]	0 to −2mA	1µsec	Com	Ceramic 24-pin DIP	6-34
	DAC71-COB-I	16	±0.003	±15[6]	±1mA	1µsec	Com		6-34
	DAC71-CCD-I	4 digits	±0.005	±15[6]	0 to −2mA	1µsec	Com		6-34
	DAC71-CSB-V	16	±0.003	±15	0 to +10V	10µsec	Com		6-34
	DAC71-COB-V	16	±0.003	±15	±10V	10µsec	Com		6-34
	DAC71-CCD-V	4 digits	±0.005	±15	0 to +10V	10µsec	Com		6-34
	DAC72-CSB-I	16	±0.003	±19[6]	0 to −2mA	1µsec	Ind	Metal Hermetic 24-pin DIP	6-44
	DAC72-COB-I	16	±0.003	±19[6]	±1mA	1µsec	Ind		6-44
	DAC72-CCD-I	4 digits	±0.005	±19[6]	0 to −2mA	1µsec	Ind		6-44
	DAC72-CSB-V	16	±0.003	±19	0 to +10V	10µsec	Ind		6-44
	DAC72-COB-V	16	±0.003	±19	±10V	10µsec	Ind		6-44
	DAC72-CCD-V	4 digits	±0.005	±19	0 to +10V	10µsec	Ind		6-44
High-Resolution Highly Accurate	DAC73J	16	±0.015	±22	0 to −2, ±1mA, ±2.5, ±5, ±10, +5, +10V	50µsec	Com	Module	6-54
	DAC73K	16	±0.00075	±22		50µsec	Com	Module	6-54
	DAC736J	16	±0.0015	±22		50µsec	Com	Module	6-54
	DAC736K	16	±0.00075	±22		50µsec	Com	Module	6-54
Very-Wide Temperature Range	DAC10HT	12	±0.012	±20	±2.5, ±5, ±10, +5, +10V	200nsec	−55°C to +200°C	Ceramic 24-pin DIP	6-5
	DAC10HT-1	12	±0.048	±50		200nsec			6-5
Very-High Speed	DAC60-10	10	±0.048	±15[6]	0 to −5, ±2.5mA	40nsec	Com	Module	6-13
	DAC60-12	12	±0.012	±15[6]		150nsec	Com	Module	6-13
Ultra-High Speed	DAC63BG	12	±0.012	±21	±5, −10mA	35nsec	Ind	Ceramic 24-pin DIP	6-18
	DAC63CG	12	±0.012	±16	±5, −10mA	35nsec	Ind		6-18
	DAC63BM	12	±0.012	±21	±5, −10mA	35nsec	Ind	Metal Hermetic 24-pin DIP	6-18
	DAC63CM	12	±0.012	±16	±5, −10mA	40nsec	Ind		6-18
	DAC63SM	12	±0.018	±21	±5, −10mA	40nsec	MIL		6-18
	DAC63TM	12	±0.018	±16	±5, −10mA	40nsec	MIL		6-18
	DAC812BM	12	±0.018	±47	±5, −10mA	65nsec	Ind	Metal Hermetic 24-pin DIP	6-141
	DAC812CM	12	±0.012	±25	±5, −10mA	80nsec	Ind		6-141
Military	DAC87/MIL Series	See Military Products							
Low Cost	DAC82KG	8	±0.16	±50	±2.5, ±5, ±10 +5, +10, ±0.8, 0 to −1.6mA	2.5µsec	Com	Ceramic 18 pin DIP	6-87
Monolithic 8-Bit	DAC90BG, (Q)	8	±0.2	±75[4]	±1, −2mA	200nsec	Ind	Ceramic Hermetic 16-pin DIP	6-102
	DAC90SG, (Q)	8	±0.2	±75[6]	±1, −2mA	200nsec	MIL		6-102

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See Q Program. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (3) Connected internally for unipolar operation. (4) In -V models the output op amp is on a second chip. (5) "Z" models operate from ±12VDC supply. (6) When used with an external op amp which uses the internal feedback resistor.

PCM DIGITAL-TO-ANALOG CONVERTERS FOR AUDIO								
Description	Model	Resolution (Bits)	Total Harmonic Distortion (max)	Settling Time	Output Range	Temp Range[1]	Dynamic Range	Page
PCM-Audio D/A Converter	PCM51JG	16	0.04% at −15dB	5µsec	±10, ±5V	Com	96dB	6-154
	PCM52JG-V	16	0.002% at F.S.	3µsec	±5V	Com	96dB	6-162
	PCM53JG-V	16	0.002% at F.S.	3µsec	±10V	Com	96dB	6-162
	PCM53JG-I	16	0.002% at F.S.	350nsec	±1mA	Com	96dB	6-162
	PCM53JP-V	16	0.002% at F.S.	3µsec	±10V	Com	96dB	6-162

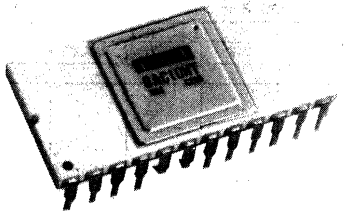
NOTES: (1) Com = 0 to +70°C.

SELF-CALIBRATING, HIGH PRECISION D/A CONVERTER

This unique 16-bit D/A converter is actually an instrument. The heart is a highly accurate 16-bit D/A converter with a heated, temperature compensated precision reference. Wrapped around this D/A are microcomputer-controlled measurement and calibration circuits that automatically null out gain, offset and linearity errors caused by shifts with time and temperature when initiated by one negative-going TTL-pulse provided by the user.

SELF-CALIBRATING D/A CONVERTER							
Description	Model	Resolution	Total Error +15 to +45°C	Output Ranges	Calibration Time	Package	Page
Precision, High-Resolution	DAC74	16 bits	±0.0015%, max	0 to +10V ±10V	2.5sec, initiated by 15μsec negative TTL pulse	7" x 5" x 0.600" metal	6-62

BURR-BROWN®



DAC10HT

Wide Temperature Range General Purpose 12-Bit DIGITAL-TO-ANALOG CONVERTER

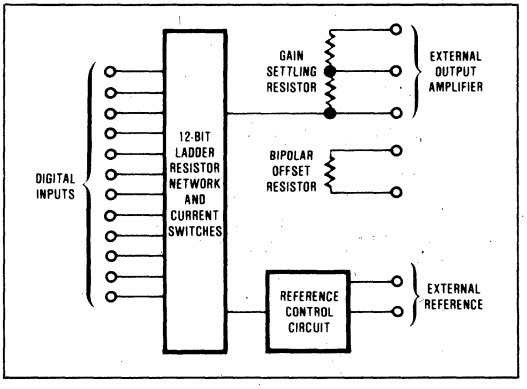
FEATURES

- -55°C to +200°C SPECIFICATIONS
- FULL 12-BIT RESOLUTION
- 200nsec SETTLING TIME, TYPICAL
- MONOTONIC OVER FULL TEMPERATURE RANGE
- TTL AND CMOS COMPATIBLE
- HERMETIC DUAL-WIDTH CERAMIC PACKAGE

DESCRIPTION

Designed for use in circuits that operate over a wide temperature range, DAC10HT is a general purpose, 12-bit D/A converter. The design uses state-of-the-art integrated circuit and laser-trimmed thin-film techniques for maximum accuracy. Compatible with TTL and CMOS logic, DAC10HT is monotonic over the full -55°C to +200°C temperture range. Special design techniques minimize output glitches. The package is compact, dual-width, 24-pin ceramic DIL.

100% screening operations are conducted at key manufacturing steps. Burn-in and temperature cycling are examples, and the product is assembled in a clean-room environment.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at V_{CC} = +15VDC, V_{EE} = -15VDC, Reference = +10VDC, and T_A = +25°C unless otherwise noted.

MODEL	DAC10HT			DAC10HT-1			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT							
DIGITAL INPUTS							
Resolution	12			12			Bits
TTL-Logic "1" at 100na, max	2.0			2.0			V
Logic "0" at −100μA, max			0.8			0.8	V
Logic "0" at −100μA, max at +200°C			0.6			0.6	
CMOS(1)-Logic "1" at 100nA, max	70% Vcc			70% Vcc			V
Logic "0" at -100μA, max			30% Vcc			30% Vcc	V
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error at +25°C							
12-Bit		±1/4	±1/2				LSB
10-Bit					±1/4	±1/2	LSB
at -55°C to +200°C							
12-Bit			±2				LSB
10-Bit						±2	LSB
Gain Error(2)		0.05	0.2		0.05	0.2	%
Bipolar Offset Error (input all 0's)(2)		0.05	0.2		0.05	0.2	% of FSR
Unipolar Offset Error (input all 0's)(2)			0.2			0.2	% of FSR
Monotonic Temperature Range							
12-Bit	-55		+200				°C
10-Bit				-55		+200	°C
Differential Linearity Error							
12-Bit		±1/2	±1				LSB
10-Bit					±1/2	±1	LSB
Total Unadjusted Error(3)							
+25°C		±0.1	±0.4		±0.15	±0.45	% of FSR
-55°C to +200°C		±0.3	±0.8		±0.90	±1.30	% of FSR
Total Adjusted Error(4)							
+25°C		±0.006	±0.012		0.024	±0.048	% of FSR
-55°C to +200°C		±0.015	±0.40		±0.40	±0.90	% of FSR
CONVERSION SPEED							
Settling Time to 1/2LSB (+FS change)(5)		200			200		nsec
Major Carry Glitch Duration (to 90% complete)		35			35		nsec
DRIFT (-55°C to +200°C)							
Gain (exclusive of reference drift)		±2	±10		±5	±25	ppm/°C
Bipolar Offset		±2	±10		±5	±25	ppm of FSR/°C
Unipolar Offset		±0.5	±1		±2	±5	ppm of FSR/°C
Differential Linearity		±2	±3		±3	±4	ppm of FSR/°C
OUTPUT							
Current - Unipolar (±10%)		0 to 5			0 to 5		mA
Current - Bipolar (±10%)		-2.5 to +2.5			-2.5 to +2.5		mA
Selectable Ranges(6)		0 to +5, 0 to +10, -2.5 to +2.5, -5 to +5, -10 to +10			0 to +5, 0 to +10, -2.5 to +2.5 -5 to +5, -10 to +10		V
Resistance		1.0			1.0		kΩ
Capacitance		20			20		pF
Compliance Voltage	-3		+10	-3		+10	V
EXTERNAL ADJUSTMENTS							
Gain Adjust Range		±0.25			±0.25		% of FSR
Bipolar Offset Adjust Range		±0.25			±0.25		% of FSR
Unipolar Offset Adjust Range		±0.25			±0.25		% of FSR
NOISE (0.1Hz to 10Hz, all "1"s)		30			30		μV, p-p
MULTIPLYING MODE PERFORMANCE							
Number of Quadrants(7)			2			2	
Reference Voltage Range	0		+10.24	0		+10.24	V
Accuracy(8)	±0.05			±0.05			% of FSR
Feedthrough(9)		±0.02			±0.02		% of FSR
Output Slew Rate(10)		6			6		mA/μsec
Output Settling Time (to 0.01% of FS)(10)		3			3		μsec
Control Amplifier BW (small-signal, closed-loop)		10			10		MHz
POWER SUPPLIES AND REFERENCE							
Reference Input Impedance		8 ±10%			8 ±10%		kΩ
Reference Voltage Range	0		+10.24	0		+10.24	V
Power Supply, Voltage - Vcc	+4.75		+15.0	+4.75		+15.0	VDC
Voltage - VEE	-13.5	-15	-16.5	-13.5	-15	-16.5	VDC
Current - Vcc		+9	+15.0		+9		mA
Current - VEE		-28	-40.0		-28		mA
Power Supply Sensitivity							
Vcc at +5VDC		1	5		1	5	ppm/%ΔV
VEE at -15VDC		3	10		3	10	ppm/%ΔV

SPECIFICATIONS

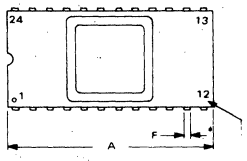
MODEL	DAC10HT			DAC10HT-1			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE							
Specification	-55		+200	-55		+200	°C
Operating	-55		+200	-55		+200	°C
Storage	-65		+210	-65		+210	°C

NOTES:
1. +4.75V < V_{CC} < +15.0V and pin 2 tied to pin 1.
2. Adjustable to zero (see Figures 4 and 5).
3. Includes Gain, Offset, and Linearity Errors with external +10.0V ±1mV reference. Does not include Reference Drift.
4. Gain and Offset Errors removed at +25°C with external +10.0V ±1mV reference. Does not include Reference Drift.
5. Current settling into short circuit.
6. Using internal scaling resistors and OPA11HT output op amp.
7. Bipolar operation at digital inputs only.
8. For 1VDC reference voltage (see Figure 2). Full Scale Range = 1V.
9. Voltage at reference input: 0 to +10V. 2kHz sine wave (see Figure 3).
10. All "1"s. 10V step on reference input.

PIN DESIGNATIONS

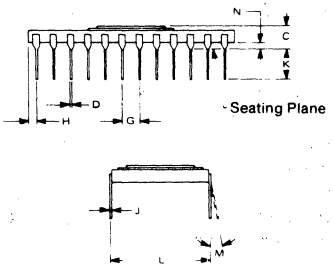
$+V_{CC}$	1	24	BIT 1 (MSB)
LOGIC THRESHOLD	2	23	BIT 2
V_{REF} INPUT (LO)	3	22	BIT 3
N/C	4	21	BIT 4
V_{REF} INPUT (HI)	5	20	BIT 5
$-V_{EE}$	6	19	BIT 6
BIPOLAR OFFSET	7	18	BIT 7
BIPOLAR OFFSET	8	17	BIT 8
CURRENT OUTPUT	9	16	BIT 9
10V RANGE	10	15	BIT 10
20V RANGE	11	14	BIT 11
COMMON	12	13	BIT 12 (LSB)

MECHANICAL



Pin numbers shown for reference only.
Numbers may not be marked on package.

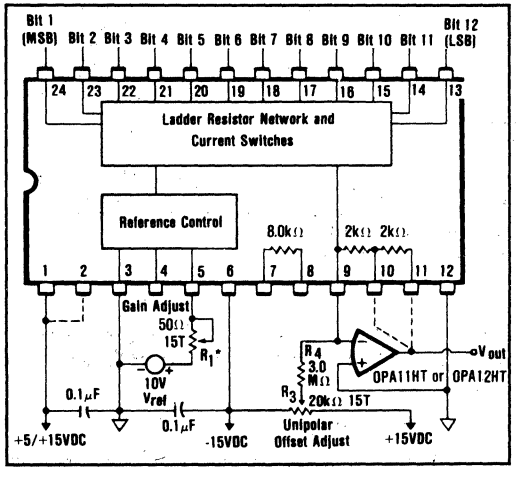
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



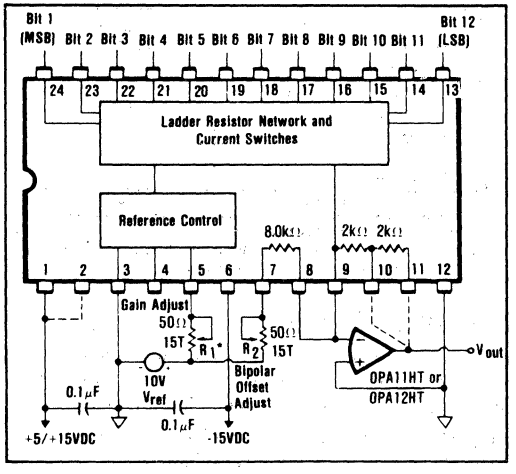
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°		10°
N	.025	.060	0.64	1.52

CASE: Ceramic with hermetic seal

CONNECTION DIAGRAM - UNIPOLAR



CONNECTION DIAGRAM - BIPOLAR



*In high temperature environments with high levels of shock and vibration it is recommended that discrete wirewound or metal film resistors be used instead of potentiometers.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

DAC10HT accepts a positive-true straight binary (BIN) input code. Offset-binary code is created by offsetting the output amplifier with the DAC reference. Two's complement code is obtained from offset binary by inverting bit 1 (the most significant bit) externally. See Table I.

ACCURACY

Linearity of the DAC10HT is guaranteed to be within the specification over its temperature range. This is the measure of the deviation of the actual transfer curve from the ideal transfer curve expressed graphically as a straight line drawn between the end-point values. For the DAC10HT the maximum deviation is ±1/2LSB at 25°C and ±1LSB over the full specification temperature range from -55°C to +200°C.

Differential Linearity error is the deviation from an ideal 1LSB output voltage change from one adjacent state to the next. An error specification of ±1/2LSB indicates that output voltage step size can range from 1/2LSB to 3/2LSB between adjacent states.

Monotonicity is an important property for a D/A converter, especially one used in a closed control loop. A converter is monotonic if the output signal increases or remains the same for an increase in digital input. A converter's differential linearity determines whether or not it is monotonic. If differential linearity is <±1LSB, the converter will be monotonic. Monotonicity is guaranteed over the entire specified temperature range for the DAC10HT.

Leakage Current is measured at the converter output with logic 0 on all digital inputs. It appears as part of offset error, both at room temperature and over the specified temperature range. In the unipolar configuration, virtually all offset error is due to leakage current.

DRIFT

Gain Drift is a measure of the change in the full scale range output due to a change in temperature and is expressed in parts per million per °C (ppm/°C). It is calculated by determining the full scale range value at high temperature, then at low temperature. The difference in the two values is divided by the difference in the two temperatures.

Offset Drift is a measure of the actual change in output over the specified temperature range with logic 0 on all digital inputs. It is calculated by measuring offset voltage at the temperature extremes. The maximum change referred to the offset voltage at +25°C is divided by the temperature excursion from +25°C. Offset drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

Differential Linearity Drift (the change in differential linearity over the specified temperature range) is calculated in a manner similar to offset drift and is expressed in ppm of FSR/°C.

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES				
	ANALOG OUTPUT			
LOGIC INPUTS	VOLTAGE*		CURRENT	
Binary	0 to +10V	-10V to +10V	0 to -2mA	-1mA to +1mA
111111111111	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
100000000000	+5.0000V	0.0000V	-1.0000mA	0.0000mA
011111111111	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
000000000000	0.0000V	-10.0000V	0.0000mA	+1.0000mA
Binary Two's Complement**				
011111111111		+9.9951V		-0.9995mA
000000000000		0.0000V		0.0000mA
111111111111		-0.0049V		+0.0005mA
100000000000		-10.000V		+1.0000mA
1LSB (BIN)	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.
**MSB must be inverted externally for this code.

CONVERSION SPEED

Settling Time is the time required for the output to enter and remain within an error band of the final value measured from the time the digital input is changed.

The settling time for a 1LSB change at the input is naturally less than for a full scale change. It is greatest at the major carry point (the point at which all of the bits change states) due to nonuniform switching times of the internal current switches. For a 1LSB change at the major carry point, settling time to within 0.01% will typically be 200nsec.

COMPLIANCE VOLTAGE

This is the maximum voltage which can be impressed on the current output node and still remain within the specified accuracy. These voltages are -3.0V and +10V.

POWER SUPPLY SENSITIVITY

This measure of the effect of a power supply voltage change on the D/A converter output is defined as a percent of FSR/percent of change in either the +5V, +15V or -15V power supplies about the nominal supply voltages. Figure 1 shows power supply rejection vs frequency.

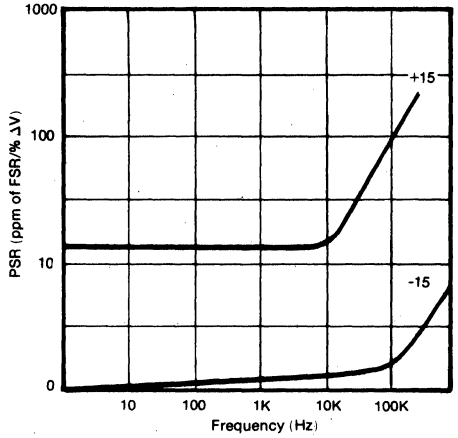


FIGURE 1. Power-Supply Rejection vs Power-Supply Ripple Frequency.

MULTIPLYING MODE PERFORMANCE

The output of the DAC10HT is the product of the reference input and digital input values. The reference may be an AC signal and can vary from 0 to +10 volts. This is useful in applications where digitally programmed attenuation of a signal is desired. Bcause the reference voltage input must be positive, the DAC10HT multiplies in two quadrants only. For highest accuracy the input reference voltage should be as high as possible (see Figure 2).

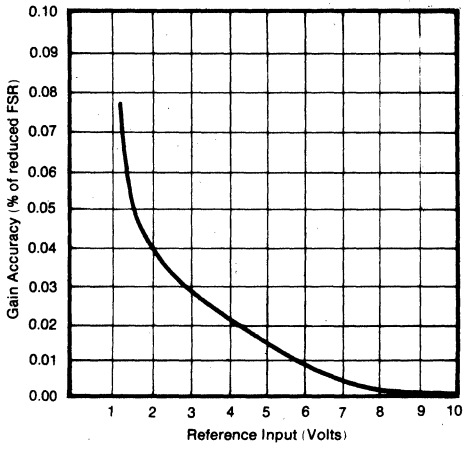


FIGURE 2. Gain Accuracy vs Reference Voltage.

Feedthrough of the DAC10HT is the amount of reference signal that appears at the output when all digital inputs are logic 0. Expressed in % of FSR, it increases with increasing reference frequency (see Figure 3).

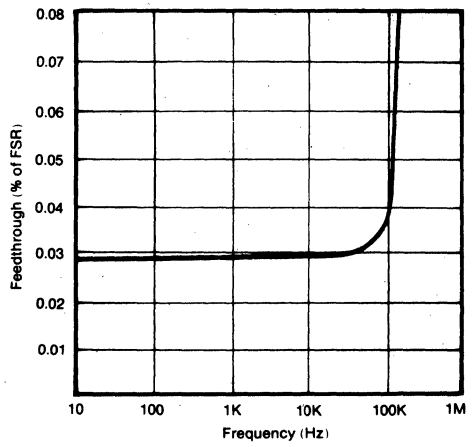


FIGURE 3. Feedthrough Voltage vs Power-Supply Ripple Frequency (Unipolar Mode).

OPERATING INSTRUCTIONS

INPUT LOGIC LEVELS

Inputs of the DAC10HT are either TTL or CMOS logic compatible. For TTL, connect +5V to pin 1 (pin 2 open). For +5V CMOS, connect +5V to pins 1 and 2. For +15V CMOS compatibility, connect +15V to pins 1 and 2.

In circuits where pin 2 is used to determine the digital threshold level, the following application tip may be helpful. If the analog system ground (to which the DAC10HT is referred) is separate from the digital driving logic ground, the threshold voltage input (at pin 2) may be driven from an external voltage source to keep the threshold at proper value. Threshold voltage will always be at one-half the voltage applied to pin 2 (+1.4V < pin 2 < +15V).

POWER SUPPLIES

Each power supply should be bypassed to ground with a 0.1μF capacitor as shown in the Connection Diagrams. Locate the capacitors as close as possible to the DAC10HT.

GAIN AND OFFSET ADJUSTMENTS

(Voltage Output Configuration)

Initial gain and offset errors of the DAC10HT circuit may be trimmed out using the following procedures.

Unipolar configuration - input all 0's and null offset error by adjusting R_3 until output voltage equals zero. Input all 1's and adjust R_1 until the output voltage is +FS -1LSB (see Table I and Connection Diagram).

Bipolar configuration - input all 0's and null offset error by adjusting R_2 until output voltage equals -FS. Input all 1's and adjust R_1 until the output voltage is +FS - 1LSB (see Table I and Connection Diagram).

To obtain specified gain and offset errors, replace the 50Ω potentiometers (R_1 and R_2) shown in the Connection Diagrams with 25Ω 0.1% fixed resistors.

SELECTING AN EXTERNAL REFERENCE

DAC10HT is configured to use a +10V reference. An internal 8kΩ resistor in series with an external 50Ω adjust potentiometer sets the current into the reference input at 1.25mA (see Figure 4).

Temperature drift of the reference increases drift of the entire circuit. In unipolar configurations the drift specification adds directly to the total circuit drift. In the bipolar configuration some drift cancelling effects take place. One-half of the reference drift added to the total DAC drift will give total circuit drift.

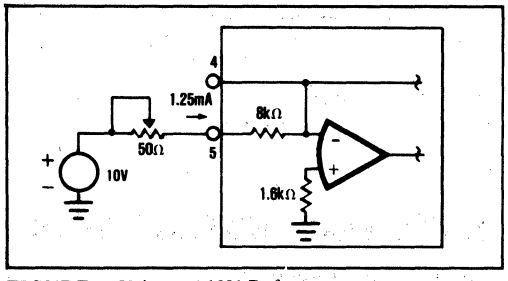


FIGURE 4. Using a +10V Reference.

SELECTING AN EXTERNAL REFERENCE

Building An External +10V 200°C Reference

The DAC10HT requires an external +10V reference for normal operation. A circuit for obtaining this reference voltage that will operate at +200°C is shown in Figure 5. The value of R_1 or R_2 should be adjusted to provide a reference voltage of 10V ±1mV due to the tolerance of the zener voltage. With no adjustment to the zener current for optimum zero T.C. point (see page 10), this reference will have an average temperature coefficient of about ±20ppm/°C over −55°C to +200°C.

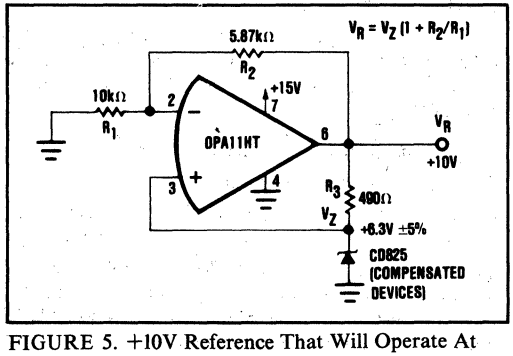


FIGURE 5. +10V Reference That Will Operate At +200°C.

LOW POWER OPERATION

The typical supply currents required by the DAC10HT under normal operating conditions are 9mA (V_{CC}) and 28mA (V_{EE}). The average power required (P_D) is therefore

$$P_D = |V_{CC} \times 9mA| + |V_{EE} \times 28mA|$$
$$= 555mW \ (+V_S = 15V, -V_S = 15V), \text{ or}$$
$$= 465mW \ (+V_S = 5V, -V_S = 15V).$$

Under certain operating conditions this power consumption can be reduced to as little as 245mW.

The major contributor to the power consumption is the -15V supply. As long as a +10V reference is used, V_{EE} must be between -13.5V and -16.5V. If, however, a lower reference voltage is used, V_{EE} can be reduced considerably and this greatly reduces the power consumption. Lowering the reference voltage will, of course, lower the full scale output voltage by a proportional amount. For example, if the reference voltage is +5V, the full scale output voltage when using the 10V range pin (pin 10) will be +5V instead of +10V with a +10V reference in the unipolar mode of operation. Table II indicates the minimum supply voltages and the power consumption obtained when using these supply voltages for various values of V_{REF}. See also page 10 for a discussion of how to build a low power voltage reference circuit.

TABLE II. Minimum Power Supply Voltages and Typical Power Consumption for Operation with Various Values of V_{REF}.

External V_{REF}	+V_{CC} (Pin 1)	-V_{EE} (Pin 6)	Total Power Consumption (Typical)
+10V	+5V	-13V	409mW
+6.3V	+5V	-10V	275mW
+5V	+5V	-8V	235mW

SELECTING AN OUTPUT AMPLIFIER

The most important characteristics of the output amplifier are input offset voltage drift, input bias (or difference) current drift, and settling time. Specifications over the full operating temperature range are very important. Initial input offset voltage and bias current effects will be trimmed out, but bias errors will be introduced as these parameters drift with temperature changes. Errors introduced will appear as offset in the D/A circuit output.

Table III provides the equations used to convert these amplifier errors to D/A output errors.

TABLE III. Computing DAC Error Contributed by External Amplifier.

PARAMETER	UNIPOLAR CONFIGURATION	BIPOLAR CONFIGURATION
I_{Bias}	$\frac{I_B \times R_F}{FSR} \times 100$	$\frac{I_B \times R_F}{FSR} \times 100$
V_{os}	$\frac{V_{os}\left(1 + \frac{R_F}{1k\Omega}\right)}{FSR} \times 100$	$\frac{V_{os}\left(1 + \frac{R_F}{0.8k\Omega}\right)}{FSR} \times 100$

FSR = Full scale range (-2.5V to +2.5V is a 5V FSR, etc.). Results are in % of FSR; to get ppm of FSR, multiply by 10^4.
R_F is the value of the feedback resistor.
R_{F_1} and R_{F_2} are options shown in Figure 7.

Example:
If V_{os} drift and I_{bias} drift of the output amplifier are $10\mu V/°C$ and $0.5nA/°C$, respectively, in a D A converter with -10V to +10V output, the output drift due to these effects would be computed in this manner.

$$V_{os}: \frac{(10 \times 10^{-6})\left(1 + \frac{10k\Omega}{4.0k\Omega}\right)}{20} \times 100 = 0.00018\% \text{ of FSR } °C$$

or 1.8ppm of FSR/°C

$$I_{Bias}: \frac{0.5 \times 10^{-9} \times (10k\Omega)}{20} \times 100 = 0.00003\% \text{ of FSR } °C$$

or 0.3ppm of FSR/°C

Total error contribution of amplifier = 1.8 + 0.3 = 2.1ppm of FSR °C

Effects of input bias current drift may be reduced approximately by a factor of 5 by placing a resistor in series with the positive input lead of the amplifier as shown in Figure 6.

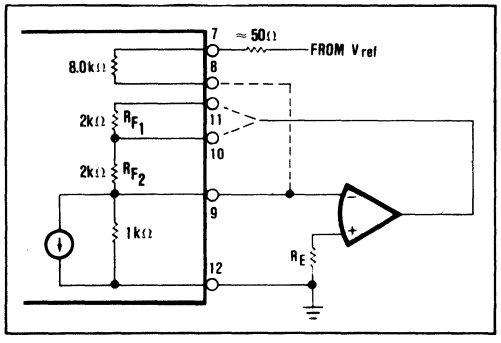


FIGURE 6. Equivalent Output Circuit.

This balances the offset created by bias currents and the error is reduced to the difference in bias currents in the positive and negative inputs. (Substitute I_{offset} in equations in Table III).

The value of this resistor is shown in Table IV for different output ranges.

TABLE IV. R_E Values.

Output Range	±2.5V	±5V	±10V	0 to +5V	0 to +10V
R_E Value	470Ω	615Ω	727Ω	500Ω	800Ω

Settling time of the DAC10HT is less than 400nsec for an FSR change to within 0.01% of final value. The output amplifier's dynamic characteristics should be compatible with this performance. Burr-Brown's OPA12HT fast-settling amplifier is recommended for use up to 175°C. The OPA11HT is recommended for operation at +200°C.

CURRENT OUTPUT OPERATION

DAC10HT can be connected to produce a bipolar voltage output without the use of external components by connecting the internal resistors as shown in Figure 7. Output voltage range of this circuit is approximately ±2.25V.

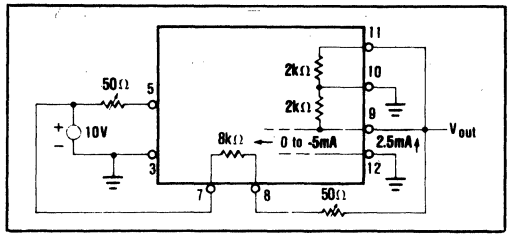


FIGURE 7. Bipolar Current Output Operation Utilizing Internal Resistors.

Gain and offset adjustments are made as described previously except the "+FS" and "-FS" are interchanged and "-FS + 1LSB substituted for +FS -1LSB.

Unipolar and other bipolar ranges may be selected by using an external load resistor as long as the compliance voltage limits, −3.0V to +10V, are observed. To minimize temperature drift when using an external load resistor, (R_2 in Figure 8), an external reference-current-setting resistor should also be used. These two resistors should track over temperature as explained in the section on selecting an external reference on the previous page.

MULTIPLYING MODE OPERATION

DAC10HT can be used as a two-quadrant multiplying D A converter by applying the analog signal to be processed through a 100Ω potentiometer to the reference voltage input, pin 5. The analog signal must be between 0 and +10V. The output will be an analog signal equal to the product of the input analog signal and the input digital code. DC error of the output signal is less than

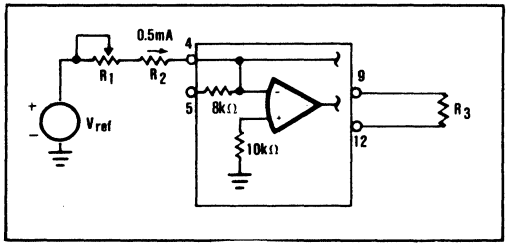


FIGURE 8. Using an External Load Resistor.

0.05% for a reference voltage range of +1V to +10V. For voltages near zero, the error can be quite large (see Figure 2).

HEAT DISSIPATION

The DAC10HT dissipates approximately 430mW (with +5V and -15V power supplies) and the package has a case-to-ambient thermal resistance (θ_{CA}) of 34°C/W. For optimum performance at +200°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the package can be achieved by using a silicone heat-sink compound.

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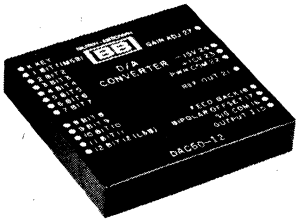

DAC60

Ultra-high Speed DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 40nsec SETTLING TIME
- 10- AND 12-BITS
- LOW COST
- MONOTONIC
- 1/2LSB DIFFERENTIAL LINEARITY

DESCRIPTION

The DAC60 is a high speed digital-to-analog converter designed for high speed display applications, for use in high speed A/D converters, and for use as a high speed, precision waveform generator. The DAC60 is available in 10- and 12-bit accuracy. The extremely high speed of the DAC60 is accomplished with low impedance current switching techniques. The typical settling time to 0.05% for an LSB step is 25nsec. The maximum settling time for the major carry or for a full scale transition is only 40nsec to 0.05%. (The major carry is the LSB transition from 011 ... 11 to 100 ... 00).

The DAC60 produces a current output proportional to the digital input. The most significant bit (MSB) produces an output of -2.5mA. The DAC60 is pin-programmable to obtain unipolar or bipolar output signals. The current output may be fed directly into the summing junction of an external high speed operational amplifier, or onto an external summing resistor. An internal 2kΩ feedback resistor is included in the DAC60 for use with an external operational amplifier. This resistor provides voltage output ranges of 0 to +10V or ±5V and compensates for temperature drift of the DAC60.

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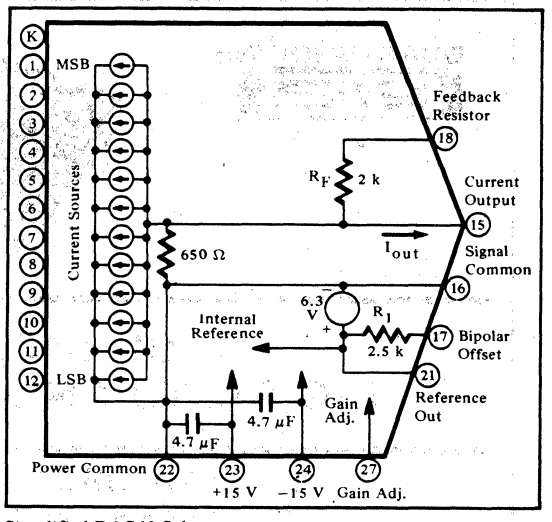
SPECIFICATIONS

Specifications typical at 25°C and with rated supply unless otherwise noted.

ELECTRICAL

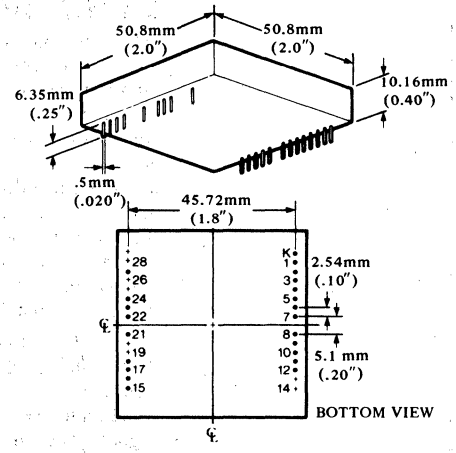
MODEL	DAC60
DIGITAL INPUTS	**10 Bits and 12 Bits**
Data Input Codes	TTL/DTL Compatible Complementary Logic
TRANSFER CHARACTERISTICS	
ACCURACY	
Linearity Error	±1/2 LSB
Differential Linearity Error (max)	±1/2 LSB
Gain Error	
(adjustable to zero)	±0.05% of FSR (3)
Offset Error	
(adjustable to zero)	
Unipolar	±0.001% of FSR
Bipolar	±0.05% of FSR
ACCURACY DRIFT	
Voltage Output (1)	±15 ppm/°C
Current Output	±30 ppm/°C
Differential Linearity Error	
(0° to +70°C)	
10 bits	±1/2 LSB
12 bits	±1 LSB
Monotonicity (0° to +70°C)	Guaranteed
CONVERSION SPEED	
Settling Time for 1 LSB Change (2)	
to 0.05%	25 ns
to 0.0125%	40 ns
for full scale change or major carry change	
to 0.05% (max)	40 ns
to 0.0125%	150 ns
POWER SUPPLY SENSITIVITY (4)	
±15 Volt Supply	±0.002 %/% P.S. Change
OUTPUT	
Unipolar Output Range (5)	0 to -5 mA
Compliance	3.2 V
Output Impedance	650 Ω
Bipolar Output Range (5)	±2.5 mA
Compliance	0.70 V
Output Impedance	516 Ω
POWER SUPPLY REQUIREMENTS	
Rated Power Supplies	±15 V
Power Supply Range	±14.5 to ±15.5 V
Supply Drain (max)	+45 mA, -35 mA
TEMPERATURE RANGE	
Specification	0° to +70°C
Operating (reduced specs)	-25°C to +85°C
Storage	-55°C to +100°C



Simplified DAC60 Schematic.

MECHANICAL

Dimensions in parentheses are in inches.



Material
Case - Diallyl Phtalate Shell
"Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)."
Connector - 2301MC
or - 2302MC

(1) When in the voltage output mode using an external op amp and the internal feedback resistor as shown in figure 1.
(2) For any data change not involving the four most significant bits.
(3) FSR is Full Scale Range (5 mA).
(4) The percent change in the output level with a one percent change in power supply voltage.
(5) The unipolar output may be fed into a resistive load providing a 3.2 volt or less swing. It is recommended that the bipolar output be fed into the summing junction of an op amp or a resistive load low enough to limit the swing to less than 100 mV.

DEFINITION OF SPECIFICATIONS

DIFFERENTIAL LINEARITY ERROR

The differential linearity of the DAC60 is ±1/2 LSB. This means that any 1 LSB digital input change will produce an output change of 1 LSB ±1/2 LSB (1/2 LSB to 3/2 LSB). This specification is especially important in CRT display systems because the eye is sensitive to differential linearity errors greater than ±1/2 LSB.

LINEARITY ERROR

Linearity error is the deviation of any output state from an ideal straight line drawn between the end points (all bits ON and all bits OFF)

MONOTONICITY

The DAC60 is guaranteed to be monotonic over 0 to 70°C. This means that the output will never decrease for an increase in the digital input.

COMPLIANCE

The compliance voltage of the DAC60 is the maximum voltage swing allowed on the current output node in order to maintain the specified accuracy; it is 0.70 volts for the bipolar current range of ±2.5 mA and is 3.6 volts for the unipolar current range of 0 to -5 mA. The maximum safe voltage swing allowed with no damage to the DAC60 output is ±5 volts.

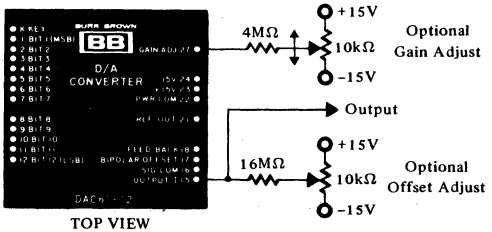
DEFINITION OF DIGITAL INPUT CODES

The DAC60 is available with complementary binary coding. The user may pin strap the output for bipolar complementary offset binary or unipolar complementary straight binary.

INPUT		OUTPUT CURRENT(1)		OUTPUT VOLTAGE(2)		OUTPUT VOLTAGE(3) when driving 50 Ω
MSB	LSB	BIPOLAR	UNIPOLAR	BIPOLAR	UNIPOLAR	UNIPOLAR
111 ...	111	+2.5 mA	0 mA	-5.0 V	0.0 V	0.00 mV
011 ...	111	0 mA	-2.5 mA	0.0 V	+5.0 V	-116.07 mV
000 ...	000	-(2.5 mA -1 LSB)	-(5 mA -1 LSB)	+5.0V -1 LSB	+10.0V -1 LSB	-(232.14 mV -1 LSB)
One LSB						
10 bits		4.88 μA	4.88 μA	9.76 mV	9.76 mV	0.227 mV
12 bits		1.22 μA	1.22 μA	2.44 mV	2.44 mV	0.057 mV

(1) Short circuit current
(2) Op-Amp output when driving summing junction and using the internal R_F (see Figure 1)
(3) See Figures 2 and 3.

INSTALLATION AND OPERATING INSTRUCTIONS



TOP VIEW
Optional GAIN and OFFSET Adjustments

- BIPOLAR OFFSET, pin 17, should be connected to I OUTPUT, pin 15, for bipolar operation or to POWER COMMON, pin 22, for unipolar operation.
- GAIN Adjustment Range: ±0.15% of FSR
- Offset Adjustment Range: ±0.15% of FSR
- If the GAIN ADJUST is not used, leave pin 27 open.
- REF OUT, pin 21 may be used to provide a low drift (5 ppm/°C) reference for external circuitry as long as less than ±100 μA is drawn from it.
- Internal 4.7 μF bypass capacitors between the ±15 Vdc power inputs and ground are included so that the DAC60 does not require external bypass capacitors.
- Both the DAC60-10 and DAC60-12 provide 12 digital inputs. Digital inputs that are not used should be tied to "1" (+5 volts). (Bits 11 and 12 on the DAC60-10 should be tied to +5 V if not used.)

INTERNAL FEEDBACK RESISTOR

Burr-Brown includes a 2 kΩ feedback resistor in the high speed resistor network (pin 18). The feedback resistor's temperature coefficient of resistance (TCR) is matched with that of the resistor network. Since the TCR of the resistor network contributes much of the current output drift of the DAC60, use of the feedback resistor with an external op amp reduces the effective drift of the voltage output. This is why the voltage output drift in the electrical specifications table is significantly better than the current output drift.

OPTIONAL OPERATING CONFIGURATIONS

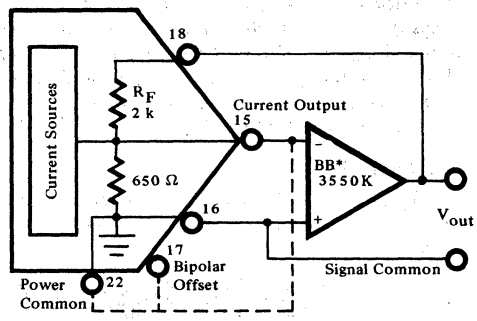
DRIVING AN OP AMP SUMMING JUNCTION

The DAC60 will drive the summing junction of an op amp (op amp being used as a current to voltage converter) to produce an output voltage:

$$V_{OUT} = -(I_{OUT})(R_F)$$

where I_{OUT} is the DAC60 short circuit output current and R_F is the op amp feedback resistor. Use of the internal feedback resistor (pin 18) will result in a 0 to +10 volt or ±5 volt output range. A 16 kΩ feedback resistor would produce output ranges of 0 to +50 volts or ±25 volts.

Use of the internal 2 kΩ feedback resistor will result in output voltage drifts as indicated in the specification table because the internal R_F drift is matched to that of the current sources. When using external feedback resistors, their temperature coefficient of resistance (TCR) should be directly added to the current output drift of the DAC60 to obtain the drift of the voltage output.



* Burr-Brown's 3400, 3401 and 3402 may also be used.

FIGURE 1. Driving an op amp summing junction.

DRIVING A RESISTIVE LOAD

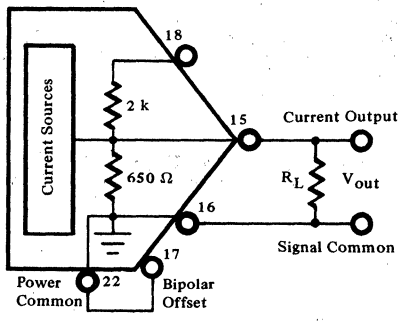


FIGURE 2. Driving a resistive load.

When driving a resistive load, the voltage output of the DAC60 is the short circuit output current times the equivalent load resistance. The DAC60 output impedance is approximately 650 ohms (in parallel with the load resistance, R_L). The output voltage is:

$$V_{OUT} = (I_{OUT})\left(\frac{R_L \times 650\ \Omega}{R_L + 650\ \Omega}\right)$$

With an R_L of 100 kΩ or higher, the full scale output voltage will be approximately 3.2 volts. An R_L of 300 ohms will provide a full scale output voltage of approximately 1 volt.

NOTE: For bipolar use, the output voltage should be less than 700 mV for acceptable output accuracy.

DRIVING A CABLE

The DAC60 can drive long lengths of cable with a circuit as shown in Figure 3. With just the 93 ohm terminating resistor used, the full scale output will be approximately 500 mV. The 120 ohm resistor across pins 15 and 16 will minimize output re-reflections due to mismatches between the characteristic impedance of the cable and the output impedance of the DAC60. The reflection factor of a cable is $\frac{Z_o - Z_t}{Z_o + Z_t}$ where Z_o is the characteristic impedance of the cable and Z_t is the termination resistance. A 1% mismatch between Z_o and Z_t will reflect back 1% of the output voltage to the cable input where the termination resistance normally seen is the 650 ohm output impedance of the DAC60. The reflection factor at the cable input would then be .75.. The 120 ohm resistor reduces this reflection factor to 0.06 and significantly reduces glitches caused by reflections. Of course the 120 ohm resistor will reduce the full scale output voltage to about 250 mV.

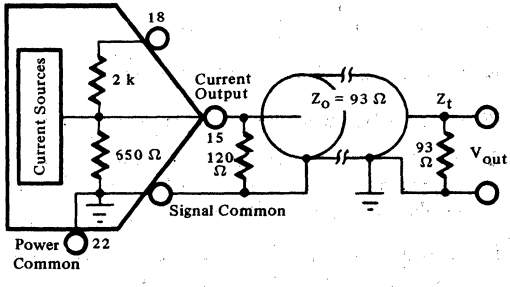


FIGURE 3. Driving a cable.

APPLICATIONS

DEGLITCHED VOLTAGE OUTPUT

Output transients when switching from one state to another are always a problem with high speed D/A converters. These transients, sometimes called glitches, are the result of unequal turn on and turn off times of the digital and analog components. A major contributor to glitch amplitude for the DAC 60 is the data skew of the digital inputs. Data skew is the time difference between the time one bit input changes state to the time other bit inputs change state. With data skew of less than 2 nanoseconds the DAC60 glitch area will typically be 25 picoamp seconds.

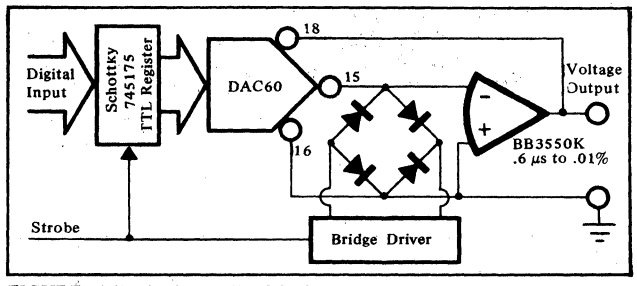


FIGURE 4. Deglitcher on DAC60 Output.

If a high speed amplifier, such as BB Model 3550 is used on the DAC60 output, a bridge clamping circuit on the summing junction will reduce the glitch amplitude. The deglitching bridge and bridge driver should be connected as shown in Figure 4. A high speed Schottky digital storage buffer should be used to reduce skew to 2 nanoseconds or less.

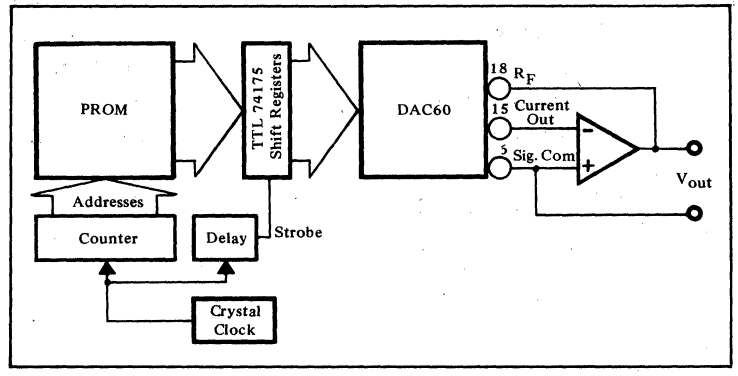
The deglitcher performance depends on the switching speed and matching of the bridge diodes. The bridge essentially clamps the summing junction near ground, preventing voltage glitches from appearing at the amplifier output. This technique can essentially eliminate or significantly reduce glitch amplitudes to 5 LSB or less at the output.

DAC60

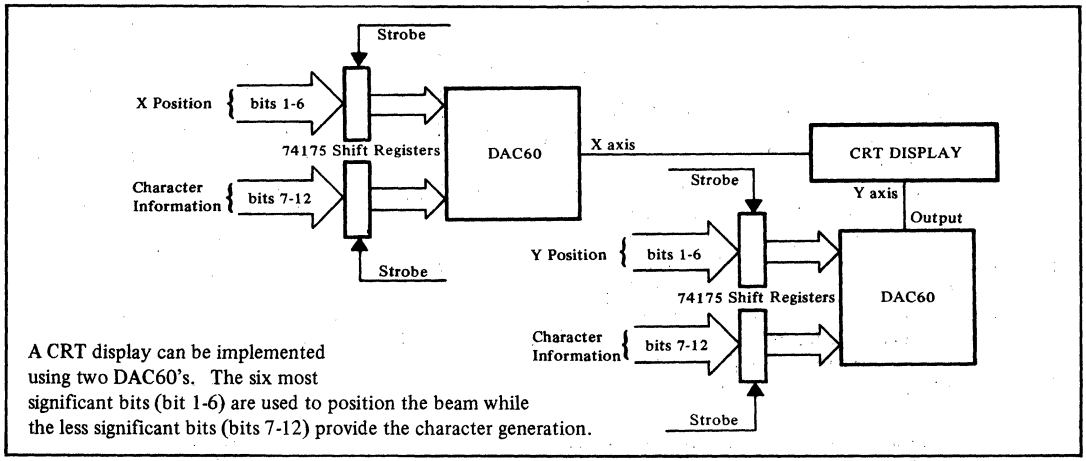
WAVEFORM GENERATORS

The DAC60 may be used as a high speed, precision signal generator with the help of a programmable read-only memory.

The counter updates the PROM addresses once each clock cycle. The delay provides a strobe pulse for the shift register when the PROM outputs have settled to a new word. This circuitry may be programmed to provide almost any complex, high speed waveform with up to 0.01% accuracy.



CRT DISPLAY CHARACTER GENERATOR



A CRT display can be implemented using two DAC60's. The six most significant bits (bit 1-6) are used to position the beam while the less significant bits (bits 7-12) provide the character generation.

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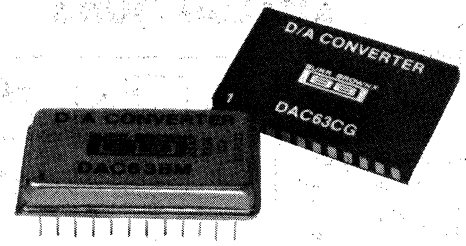


DAC63

Ultra-High Speed DIGITAL-TO-ANALOG CONVERTER

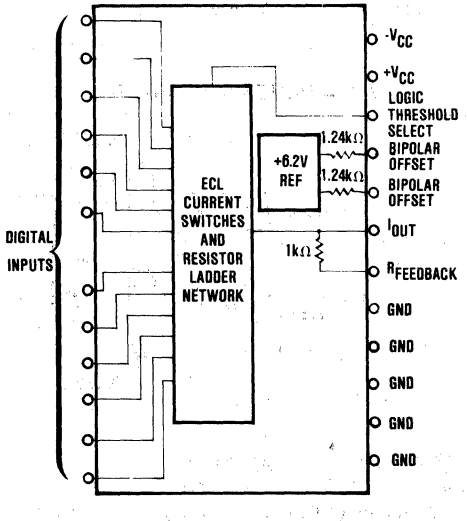
FEATURES

- 12-BIT RESOLUTION AND ACCURACY
- 30nsec SETTLING TIME (MAJOR CARRY)
- ECL-COMPATIBLE INPUTS
- LOW GLITCH ENERGY
- ±30ppm/°C MAX GAIN DRIFT
- LINEARITY ERROR LESS THAN ±1/2LSB OVER SPECIFIED TEMP RANGE
- ADJUSTABLE LOGIC THRESHOLD FOR IDEAL SWITCHING
- INTERNALLY-BYPASSED SUPPLY LINES TO MINIMIZE SETTLING TIME
- INTERNAL FEEDBACK RESISTOR FOR EXCELLENT THERMAL TRACKING
- INDUSTRIAL AND MILITARY GRADES
- HIGH RELIABILITY SCREENING AVAILABLE

DESCRIPTION

The DAC63 is an ultra-fast-settling 12-bit current output D/A converter in a 24-pin dual-in-line package. The inputs are ECL-compatible and the output settles in 30nsec, typ (40nsec, max for C and T grades) to within ±0.012% of Full Scale Range for an MSB change. The DAC63 utilizes a monolithic 12-bit switch chip and a stable thin-film-on-sapphire resistor network to achieve fast settling time and excellent stability over temperature and time. Because of the close thermal tracking of the current-switching transistors (all on one monolithic chip), the possibility of thermal-tail settling time problems are eliminated. An internal applications resistor for use with an external output op amp is included to convert the output current to insure excellent tracking and therefore lower drift. The linearity is guaranteed to be within ±1/2LSB over the specified temperature range of −25°C to +85°C for the CG, CM, BG, and BM grades and −55°C to +125°C for SM and TM grades. Gain drift is ±30ppm/°C max and bipolar offset drift is ±10ppm of FSR/°C max (high grades). Also included internally is a +6.2V reference. An output voltage compliance range of +2.0V to −0.5V allows the generation of an output voltage without using an external output amplifier. The device is available in both metal and ceramic bottom-brazed packages.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

ELECTRICAL

At +25°C and rated supplies unless otherwise specified.

MODEL	DAC63CG/CM/TM			DAC63BG/BM/SM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT							
DIGITAL INPUT							
Resolution			12			•	Bits
Logic Inputs[1]		ECL-compatible			•		
Logic "1": Voltage	−0.78	−0.90	−0.96	•	•	•	V
Current	6.0		33.0			•	μA
Logic "0": Voltage	−1.62	−1.75	−1.85	•	•	•	V
Current		10.0			•		nA
Logic Threshold: Voltage	−1.20	−1.33	−1.40	•	•	•	V
Current			0.25			•	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±0.012			•	% of FSR[3]
Differential Linearity Error			±0.012			•	% of FSR
Gain Error[2]		±0.02	±0.1		•	•	%
Offset Error[2]: Unipolar		±0.01	±0.04		•	•	% of FSR
Bipolar		±0.02	±0.1		•	•	% of FSR
Monotonicity Temp. Range (min)							
CG, CM, BG, BM	−25		+85	•		•	°C
TM, SM	−55		+125	•		•	°C
SETTLING TIME (into 150Ω)							
1LSB Change							
Settling to ±0.012% of FSR							
CM/TM, BM/SM		30	40		40	50	nsec
CG, BG		30	40		35	45	nsec
Full Scale Change							
Settling to ±1% of FSR		17			20		nsec
±0.1% of FSR		30			•		nsec
±0.024% of FSR							
CM/TM, BM/SM		55	65		65	75	nsec
CG, BG		35	50		40	55	nsec
±0.012% of FSR							
CM/TM, BM, SM		70			80		nsec
CG, BG		40			•		nsec
Glitch Energy[4]		250			•		LSB/nsec
DRIFT (over specified temp. range)							
Gain		±15	±30		±20	±40	ppm/°C
Offset: Unipolar		±0.3	±0.6		±0.5	±1	ppm/°C
Bipolar			±10			±15	ppm/°C
Linearity Error							
(over specified temp. range)			±0.012			±0.025	% of FSR
Differential Linearity Error							
(over specified temp. range)			±0.025			±0.05	% of FSR
OUTPUT							
ANALOG OUTPUT							
Output Current		0 to −10, ±5			•		mA
Output Voltage Ranges							
with External Op Amp		0 to +10, ±5			•		V
without External Op Amp[5]		0 to +1.5, ±0.5			•		V
Output Impedance without							
External Op Amp							
Unipolar: Positive		150			•		Ω
Negative		200			•		Ω
Bipolar		170			•		Ω
Compliance Voltage	−0.5		+2.0	•		•	V
POWER SUPPLIES AND REFERENCE							
Internal Reference Voltage		+6.2			•		V
Internal Reference Drift		±15			•		ppm/°C
Power Supply Voltages	±13	±15	±18	•	•	•	V
Power Supply Current: +15V		26	31		•	•	mA
−15V		38	46		•	•	mA
Power Supply Sensitivity: +15V		±0.0035			•		%/%ΔV
−15V		±0.0004			•		%/%ΔV
Power Dissipation		960	1160		•	•	mW

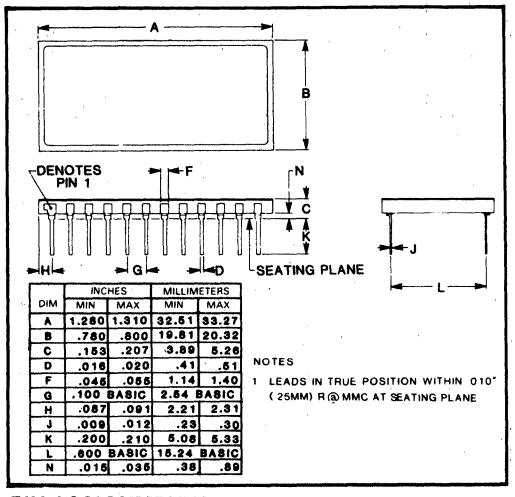
ELECTRICAL (CONT)

MODEL	DAC63CG/CM/TM			DAC63BG/BM/SM			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification: CG, CM, BG, BM	−25		+85	*		*	°C
TM, SM	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C
PACKAGE							
CG, BG	24-pin DIP bottom-brazed ceramic						
CM, TM, BM, SM	24-pin DIP metal						

*Specification same as for DAC63CG/CM/TM.

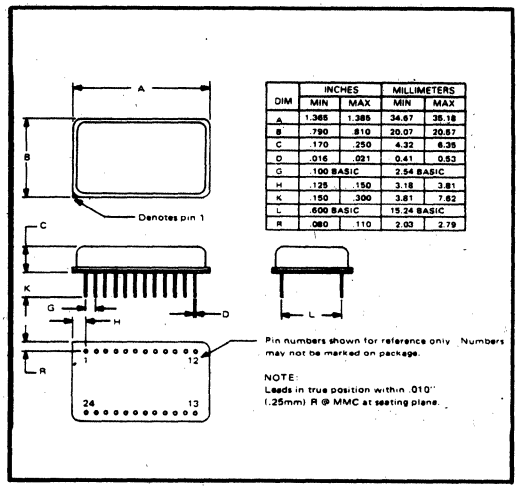
NOTES: (1) Logic Input voltages and currents are dependent on the logic threshold voltage. The logic input values given in each column are correct for the logic threshold voltage given in that column. (2) When used with an external output op amp or when the internal impedances/resistors are used as the load. (3) FSR is Full Scale Range, which is 10mA for both the DAC63BG and DAC63CG. (4) Refer to Output Glitch section. (5) Refer to Figures 8 and 9.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.280	1.310	32.51	33.27
B	.780	.800	19.81	20.32
C	.153	.207	3.89	5.26
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.087	.091	2.21	2.31
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.600 BASIC		15.24 BASIC	
N	.015	.035	.38	.89

NOTES
1 LEADS IN TRUE POSITION WITHIN .010" (.25MM) R @ MMC AT SEATING PLANE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.385	1.395	34.67	35.18
B	.790	.810	20.07	20.67
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

PIN ASSIGNMENTS

Pin No.	Function
1	Bit 1 (MSB)
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7
8	Bit 8
9	Bit 9
10	Bit 10
11	Bit 11
12	Bit 12 (LSB)
13	GND
14	GND
15	GND
16	GND
17	GND
18	Feedback Resistor Connection
19	Current Output
20	Bipolar Offset
21	Bipolar Offset
22	Logic Threshold
23	+15VDC
24	-15VDC

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a D/A converter is one of the true measures of its performance. The linearity error of the DAC63 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specified temperature range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for the DAC63 at t_{min}, +25°C, and t_{max}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications (includes internal reference).

Offset Drift is a measure of the actual change in output around zero over the specified temperature range. The offset is measured at t_{min}, +25°C, and t_{max}. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of the DAC63 is +2.0V and −0.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltage. To insure precision operation, each supply lead should be bypassed to ground as close to the unit as possible with a 1μF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC63 (pins 13, 14, 15, 16, and 17). In order to preserve the stated linearity and accuracy specifications it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these five pins and the actual ground reference point will degrade the performance of the DAC63. To achieve fast settling performance it is recommended that pins 13 through 17 be returned directly to a ground plane (see Figure 1). The analog ground should be located as close to the DAC63 as possible. Otherwise, the accuracy will be degraded by the voltage drop in the ground lines.

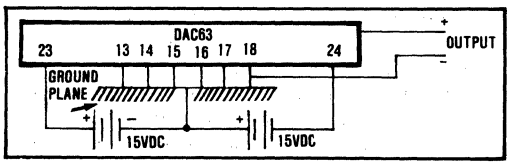


FIGURE 1. DAC63 Grounding.

DIGITAL INTERFACE, LOGIC THRESHOLD, AND NOISE IMMUNITY

The DAC63 is compatible with conventional ECL logic families such as ECL 10,000. The circuit diagram shows that the equivalent circuit of each DAC63 digital input is the base of one side of a differential amplifier. The logic 1 input voltage is −0.85V with a typical input current of 8μA. The logic 0 input voltage is −1.75V with an input current of less than 8nA.

The Logic Threshold function of the DAC63 is very important in dealing with noise in the ECL input-driving circuitry. The ECL 10,000 logic family has a noise immunity of 125mV maximum. It has a temperature coefficient of −1.4mV/°C and a power supply sensitivity of 16mV/%ΔV. With a realistic condition of a 5% power supply variation and a 25°C temperature change, the noise immunity would be degraded to 10mV. In addition, a precision D/A converter is more susceptible to noise than is the ECL logic. Noise at levels acceptable to the logic can couple through the D/A, resulting in an unacceptably noisy output.

Through the logic threshold input, the threshold voltage of the DAC63 is dynamically adjusted as the temperature and power supplies vary to give maximum noise immunity at the analog output over a wide range of conditions.

If an MC10115 line receiver (or similar logic function) is used to drive the DAC63 input, the logic threshold pin can be driven by the V_{BB} output of the ECL gate. Refer to an ECL 10,000 data book for more detail. Figure 2 shows alternate methods for generating the drive signal for logic threshold, pin 22.

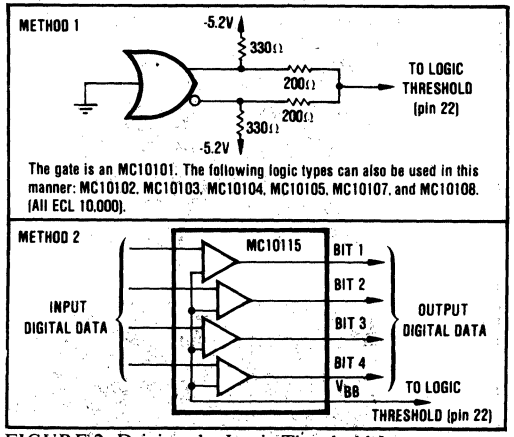


FIGURE 2. Driving the Logic Threshold Input.

SETTLING TIME

Settling time for the DAC63 is the total time required for the output to settle within an error band around its final value after a digital input change. This time includes the digital delay of the internal switches.

The settling time of the DAC63 is determined by digitizing the output waveform produced by toggling the inputs between 011111111111 and 100000000000 continuously and verifying the output settles to within ±1/2LSB in the specified time. The testing technique used is described in detail in Application Note AN-115 which can be obtained from the factory.

Figure 3 shows a typical settling time curve of the DAC63 versus output error. This curve is for full-scale digital code changes. Figure 4 is a photograph showing typical output response characteristics of the DAC63.

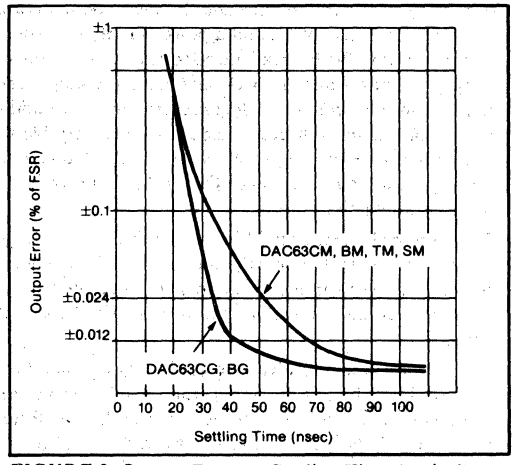


FIGURE 3. Output Error vs Settling Time (typical).

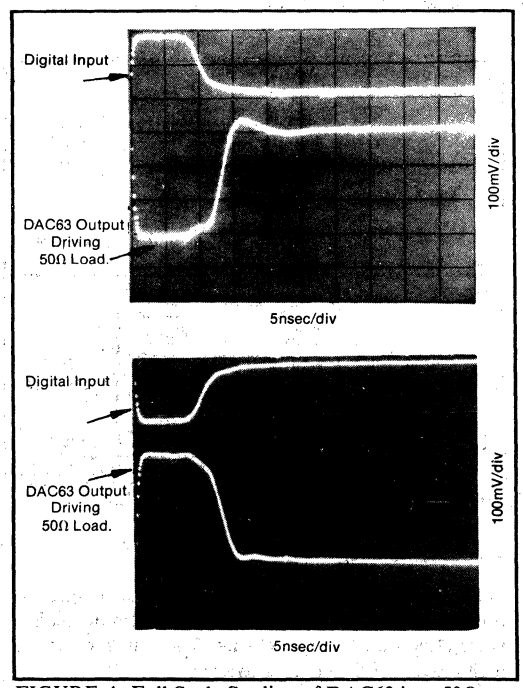


FIGURE 4. Full Scale Settling of DAC63 into 50Ω Load.

In order to achieve minimum settling time it is necessary to observe the following good high frequency construction techniques:

1. The power supplies, including the logic threshold input (pin 22), should be bypassed by 1μF CS-type tantalum capacitors.
2. Use a ground plane to connect common ground points.
3. Remove the ground plane from underneath signal lines where it would add capacitance.
4. Separate analog and digital signal leads to avoid coupling of the digital signal into the analog paths.
5. Bring the source of the digital driving signal as close to the inputs of the DAC63 as possible. If the digital inputs are not clean it will be necessary to reshape them using registers or line drivers. Figure 6 shows how to interface the DAC63 to an input register. It is recommended that the logic power line be bypassed near the digital logic circuitry as a further measure to achieve clean signals.
6. If possible, the DAC63 should be soldered directly into the printed circuit board since connector lead length will cause ringing in the output.

OUTPUT GLITCH

"Glitch" is defined as the difference in the waveforms at the output of the DAC if there is data skew and if there is not. The measurement of glitch is accomplished by measuring the area between these two waveforms.

An output glitch of less than 250LSB-nsec is achievable with the DAC63 because it employs ECL circuitry with current switches that have virtually identical delay times for logic signals making either positive or negative transitions. A glitch results when the digital data changes from one code to the next and the bits do not all switch at the same time. The delay time between the earliest and latest switching bits is called skew time. Typically during the skew time of the digital data, which includes the DAC switching, the digital code is undefined and the DAC output can go to any voltage between the full scale extremes. The glitch creates a noisy output which can be troublesome in some applications such as precision displays and complex waveform generation. Figure 5 is a photograph of a scope trace of the DAC output with a glitch occurring at the major carry transition.

The DAC63 design has been optimized for low glitch energy. However, a further reduction in the output glitch can be achieved by adjusting the skew of the higher order bits of the driving circuitry and by adjusting the logic threshold. This can be done by connecting a variable capacitor from the data lines to ground on each of the first three significant bits (more than three lines may be adjusted if desired). Refer to Figure 6. It will be necessary to create a driving digital code pattern that causes a major carry transition around these bits. It is convenient to use a digital ramp from a counter for this purpose. Initially set the logic threshold exactly half-way between logic 1 and a logic 0. This will be about −1.3V. Then

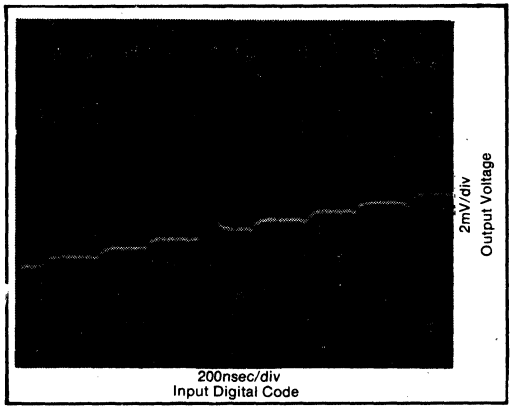


FIGURE 5. Typical Glitch Repsonse of DAC63 at Major Carry Transition with a 1.6V Full Scale Range.

examine the major carry transition associated with bit 3 and adjust the capacitor for minimum glitch. Make the same adjustment to bit 2 and then to bit 1. If done in this order, interactions will be minimized. Finally, fine tune the response by adjusting the logic threshold voltage (pin 22) for minimum glitch. It may be necessary to repeat this procedure once or twice for complete optimization.

OUTPUT CONFIGURATIONS AND APPLICATIONS INFORMATION

The DAC63 contains two 1.24kΩ resistors for generating the bipolar offset current and a 1kΩ resistor which is primarily used as the feedback resistor when used with an external op amp. This thin-film network is constructed on sapphire to provide excellent temperature tracking capability inherent in thin-film networks. These internal resistors along with other internal resistors cause the DAC63 output, in any mode, to be a ratiometric product of the reference. The feedback resistor has very low power sensitivity so that linearity is maintained independent of digital code changes. Because this resistor is constructed on a sapphire network, it is possible to have both superior tracking and low capacitance. Figure 7 shows the DAC63 connected to an external op amp in unipolar and bipolar modes. With the Burr-Brown model OPA600 it is possible to achieve settling times to ±0.01% accuracy in 150nsec. Many of the output accuracy and linearity specifications are given when connected to an external op amp.

For highest speed operation, the DAC63 should be used without an external op amp. Figures 8 and 9 show how to connect the DAC63 for bipolar and positive unipolar

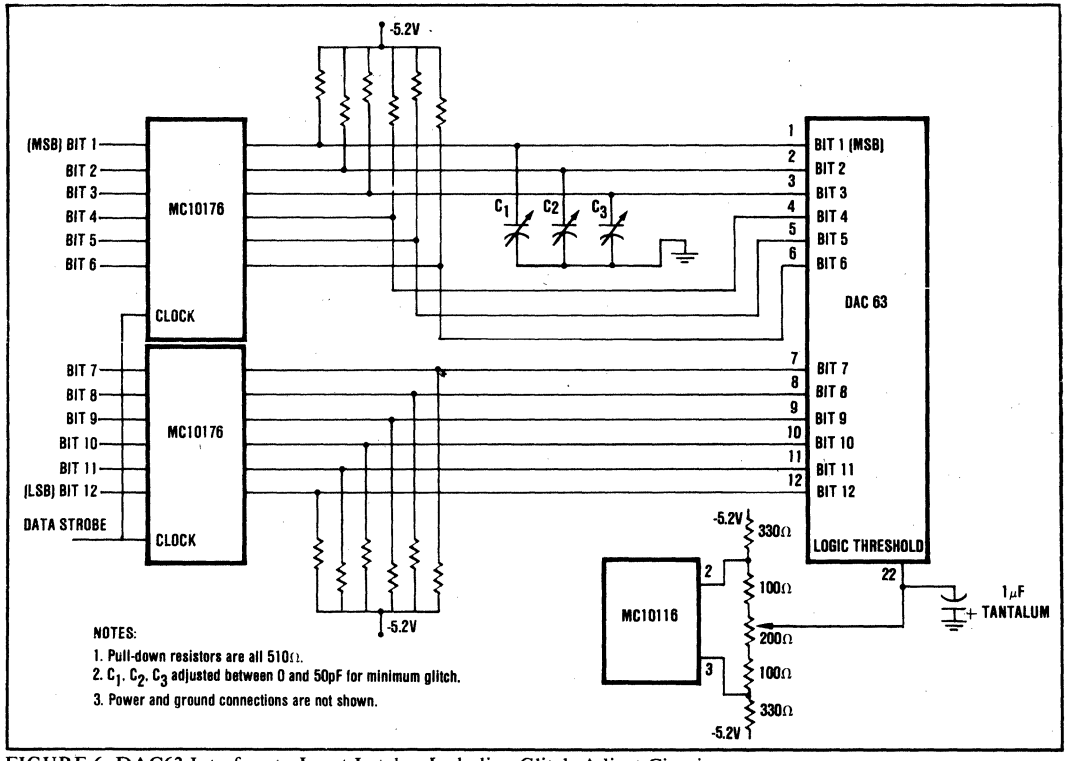
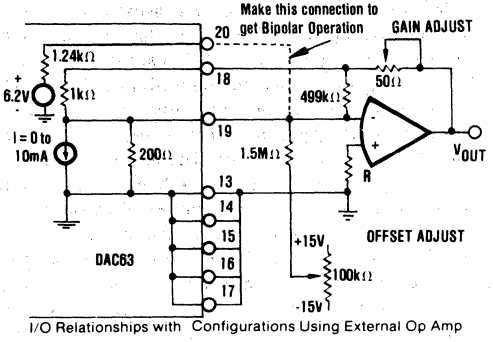


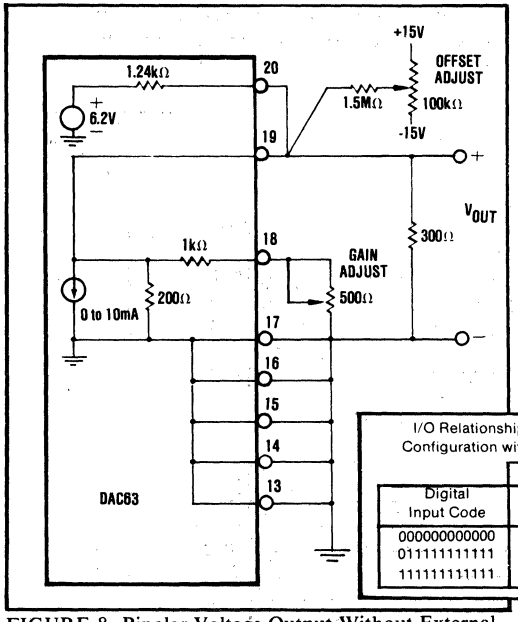
FIGURE 6. DAC63 Interface to Input Latches Including Glitch-Adjust Circuitry.

operation. Figure 10 illustrates how to connect the DAC63 to construct a fast A/D converter. The ADC attempts to create a null at the DAC output, so it is possible to clamp the output voltage with a pair of diodes, thereby avoiding the negative compliance limit.



		Unipolar	Bipolar
Digital Codes vs Output Voltage	111111111111	0.0000V	-5.0000V
	011111111111	5.0000V	0.0000V
	000000000000	9.9976V	4.9976V
R Value	R	169Ω	147Ω
Pin 20 Connection		Open	Connect to Pin 19

FIGURE 7. Bipolar and Unipolar Output Connections when Used with External Op Amp.



I/O Relationships for Voltage Output Configuration without External Op Amp

Digital Input Code	Output Voltage: Positive Unipolar	Output Voltage: Bipolar
000000000000	0.0000V	-0.500V
011111111111	0.7500V	0.000V
111111111111	1.4996V	0.500V

FIGURE 8. Bipolar Voltage Output Without External Op Amp.

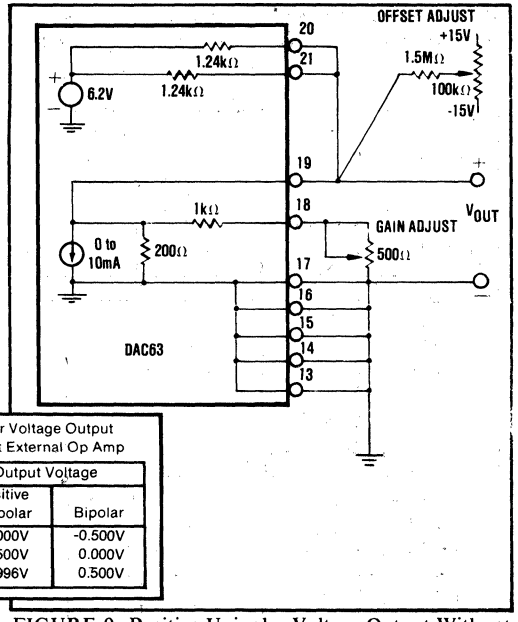


FIGURE 9. Positive Unipolar Voltage Output Without External Op Amp.

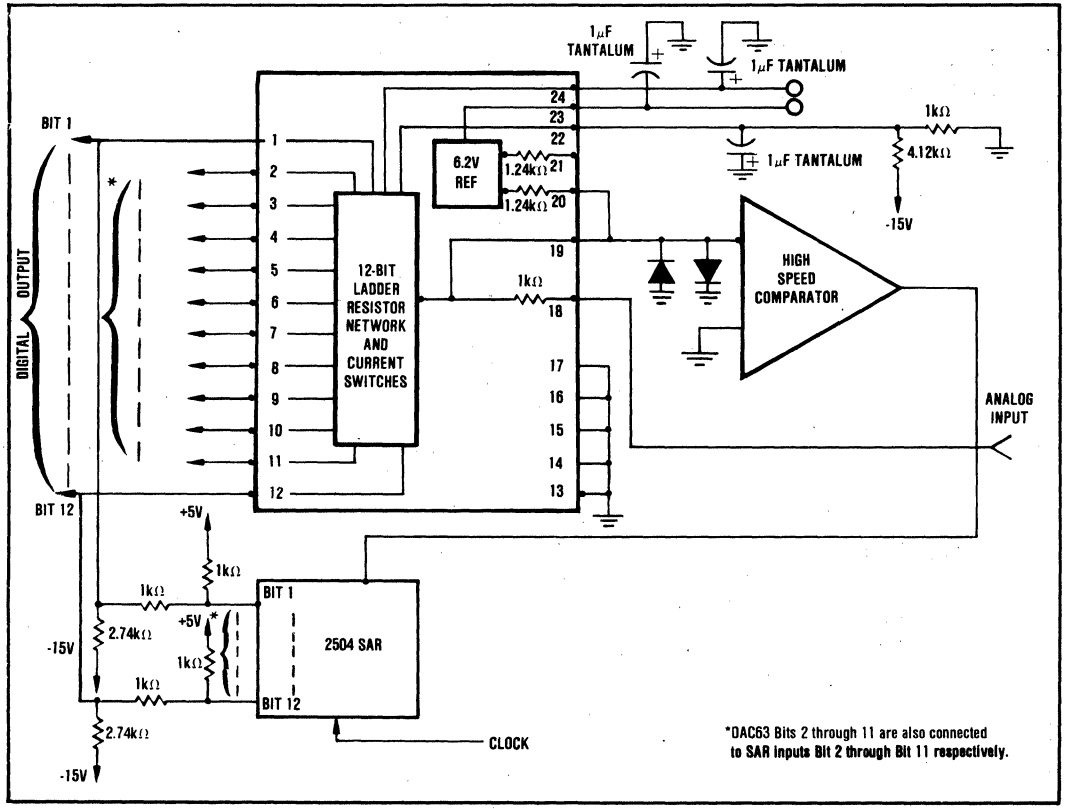
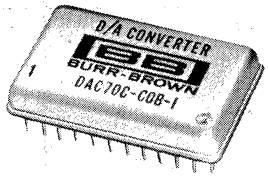


FIGURE 10. DAC63 Used in a Fast A/D Converter.

BURR-BROWN®

DAC70



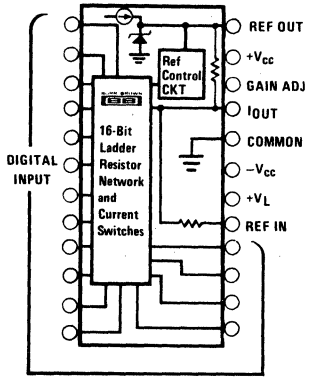
High Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

PROVIDES ACCURATE ANALOG SIGNALS
EXCELLENT FOR CALIBRATION STANDARD AND HIGH RESOLUTION APPLICATIONS
- **16-bit resolution**
- **Laser-trimmed to ±0.003% maximum nonlinearity**
- **Ultra-low drift - ±4ppm/°C, max**

SMALL SIZE SAVES SPACE AND WEIGHT
- **Hermetic Dual-in-line Package**
- **Low Cost**

FUNCTIONAL DIAGRAM



DESCRIPTION

The DAC70 is a high quality 16-bit hybrid IC D/A converter in a 24-pin DIP-compatible hermetic metal package. Constructed with laser-trimmed and drift-matched thin-film resistor network and fast-settling bipolar IC current switches, the DAC70 settles in 50μsec to a maximum nonlinearity of ±0.003% of full scale range (FSR) and has a very low maximum gain drift of ±4ppm/°C over 15°C to 50°C. Three basic models accept complementary unipolar or bipolar 16-bit binary or complementary 4-digit BCD TTL-compatible input codes. Each model is available in two grades of drift, linearity and operating temperature range. The Model DAC 70 (-25°C to +85°C) offers ±0.003% of FSR maximum nonlinearity and ±7ppm/°C maximum gain drift. The Model DAC70C (0°C to +70°C) offers ±0.005% of FSR maximum nonlinearity and ±14ppm/°C maximum gain drift.

These units provide output current signals of ±1mA or 0 to -2mA, and contain the scaling resistors for connecting an external amplifier to provide 0 to +10V (CSB, CCD) or ±10V (COB) output voltage ranges. Input power is ±15VDC and +5VDC.

Excellent stability, long life and quality product performance is assured because each DAC70 is burned-in for 96 hours at +100°C. Calibration equipment used to test the DAC70 is traceable to the National Bureau of Standards.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

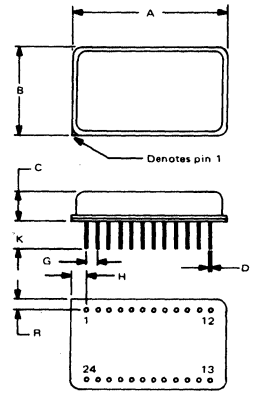
ELECTRICAL

(Typical at 25°C with rated power supplies unless otherwise noted.)

MODEL	DAC70	DAC70C	UNITS
INPUT			
DIGITAL INPUTS	TTL Compatible		
Data Input Codes	Complementary: 16 bit Binary/ 4 digit BCD		
Logic Levels (1)			
Logic "1"	$+2.4 < e_d < 5.5$ at 40μA Source		V
Logic "0"	$0 < e_d < +0.4$ max at 1.6mA sink		V
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Linearity Error (max)	±0.003	±0.005	% of FSR(2)
Gain Error, (max)(3)	±0.05		%
Offset Error, (max)(3)	±0.05		% of FSR
Monotonicity Guaranteed (10°C to 40°C)	14	13	bits
DRIFT(4)			
Gain (max) (0°C to +70°C)	— — —	±14	ppm/°C
(max) (−25°C to +85°C)	±7	— —	ppm/°C
(max) (+15°C to 50°C)	±4	±8	ppm/°C
Offset			
Unipolar	±1		ppm of FSR/°C
Bipolar (max)	±5	±10	ppm of FSR/°C
Linearity (max)	±2	± 2	ppm of FSR/°C
SETTLING TIME(4)			
(to 0.003% FSR)			
Voltage Output(5) (max) 20 V step	100		μsec
.6 mV step	50		μsec
Current Output 2 mA step	50		μsec
Output Switching Transient	500		mV
Slew Rate	1		V/μsec
POWER SUPPLY SENSITIVITY			
Unipolar Offset			
±15 V	±1		ppm of FSR/%
+5 V	±0.1		ppm of FSR/%
Bipolar Offset			
±15 V	±4		ppm of FSR/%
+5 V	±1		ppm of FSR/%
Gain			
±15 V	±10		ppm/%
+5 V	±5		ppm/%
OUTPUT			
ANALOG OUTPUT			
Voltage Mode(5)			
CSB and CCD Models	0 to +10		V
COB Model	±10		V
Output Current (min)	5		mA
Output Impedance (DC)	0.05		Ω
RMS Noise (10 Hz to 10 kHz)	0.003		% FSR
Current Mode			
CSB and CCD Models	0 to −2		mA
COB Model	±1		mA
Compliance(6)	±2.5		V
Output Impedance (DC)			
Bipolar	4.4		kΩ
Unipolar	15		kΩ
INTERNAL REFERENCE VOLTAGE (V_r)	6.3		V
Maximum External Current(7)	200		μA
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15 and +5		V
Range	±14.5 to ±15.5 & +4.75 to +5.25		V
Supply Drain			
±15 V (including 5 mA load)	30		mA
+5 V	25		mA
TEMPERATURE RANGE			
Specification	−25 to +85	0 to +70	°C
Operating (Double above drift specs)	−55 to +100	−25 to +85	°C
Storage	−55 to +125		°C

(1) It is recommended that the digital input lines to the DAC70 be drawn from TTL devices (inverters or registers) that drive only the DAC to obtain the specified accuracy.
(2) FSR means full scale range and is 20V for ±10V range, 10V for 0 to +10V range, etc.
(3) Gain and offset are externally adjustable to zero (see Figures 4 and 5).
(4) Worse case conditions measured at the worst case major carry (mid-scale).
(5) With external Burr-Brown Model 3500C op amp or equivalent, using internal feedback resistors.
(6) The current output should be connected to the virtual ground of an amplifier summing junction to obtain specified accuracy.
(7) With no degredation of specifications.

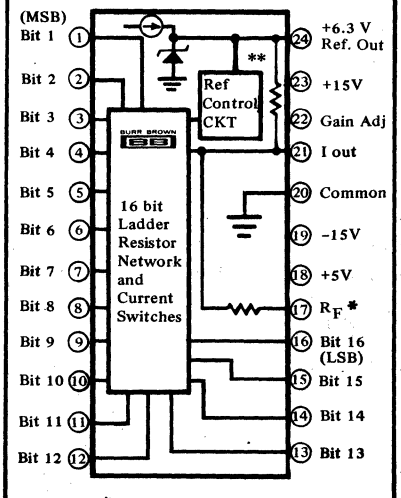
MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

CASE: Kovar
Mating Connector 245MC.
PIN: Pin material and plating composition conform to method 2003 (solderabiltiy) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 9 grams (.32 oz)

CONNECTION DIAGRAM



* R_F = 5k (CSB) 10k (COB) 8k (CCD)
** 6.3k Bipolar Offset Resistor (COB only)

DAC70

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC70 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The COB model may be user connected for either complementary offset binary (COB) or complementary two's complement (CTC) codes as shown in Table I.

DIGITAL INPUT CODES					
	Logic Inputs		CSB	COB	CTC*
	MSB	LSB	Compl. Straight Binary	Compl. Offset Binary	Compl. Two's Complement
CBI Models	All bits OFF	0000 ... 000	+Full Scale	+Full Scale	-1 LSB
	Mid Scale	0111 ... 111	+½Full Scale	Zero	-Full Scale
	All bits ON	1111 ... 111	Zero	-Full Scale	Zero
		1000 ... 000	Mid Scale -1 LSB	-1 LSB	+Full Scale
			CCD (Complementary Coded Decimal) 3 Digits		*Invert the MSB of the COB code with an external inverter to obtain CTC code.
CCD Models	F.S. bits OFF	0110 ... 0110	+Full Scale		
	All bits ON	1111 ... 1111	Zero		

TABLE I. Digital Input Codes.

ACCURACY†

LINEARITY

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.003% of FSR max (DAC 70) or ±0.005% of FSR max (DAC70C) from a straight line drawn through the end points (all bits ON and all bits OFF) at 25°C.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage step sizes can be anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

MONOTONICITY

Monotonicity over 10 to +40°C is guaranteed in the DAC70. This insures that the analog output will increase or remain the same for increasing 14 bit input digital codes. It is 13 bits over the same temperature range for the DAC70C.

DRIFT†

GAIN DRIFT is a measure of the change in the full scale range analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at -25°C or 0°C, +25°C and +70°C or +85°C for each model and calculating the GAIN ERROR with respect to the 25°C value and dividing by the temperature change. This specification is expressed in ppm/°C and is shown in Figure 1.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in the output with all bits OFF $\left(V_{OUT}^{OFF}\right)$ over the specified temperature range. V_{OUT}^{OFF} is measured at -25°C or 0°C, +25°C and +70°C or +85°C. The maximum charge in OFFSET is referenced to the OFFSET at 25°C divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME†

The settling time for each model DAC70 is the total time (including slew time) for the output to settle to within an error band about its final value after a change in the input. Two settling times are specified to ±0.003% of full scale range (FSR); one for a maximum full scale range change of 20V and also for a 1 LSB change. The 1 LSB change is measured at the major carry (0111 ... 11 to 1000 ... 00) since this is the point where the worst case settling time occurs. This measurement is made with an external BB3500C op amp. (See Figure 3.)

OUTPUT SIGNAL RANGES

For optimum operation and performance to specification, an external operational amplifier (BB Model 3500C) should be used with the DAC70. A laser trimmed low-drift thin film feedback resistor (R_F) is provided in each DAC70 to provide an output voltage range of ±10V for the COB model or 0 to +10V for the CSB or CCD models. The internal feedback resistor must be used to obtain low gain drift. (see Applications).

COMPLIANCE

The compliance voltage of the DAC70 is the maximum voltage swing allowed on the current output mode in order to maintain the specified accuracy; it is ±2.5V and is compatible with an external op amp summing junction. The maximum safe voltage swing allowed with no damage to the DAC70 output is ±5 volts.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of power supply voltage change on the D/A converter output. It is defined as ppm of FSR per percent of change in either the +15 volt or - 15 volt and +5 power supplies about the nominal power supply voltages. Figure 2 shows Power Supply rejection vs. Frequency.

[† All specifications are tested with a BB3500C operational amplifier connected to the DAC70 output.]

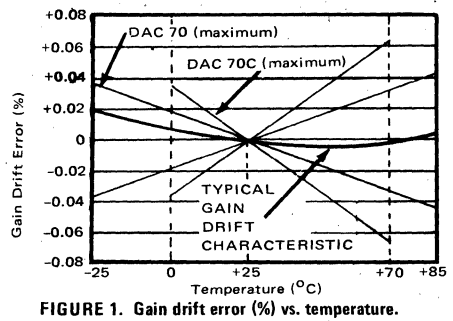


FIGURE 1. Gain drift error (%) vs. temperature.

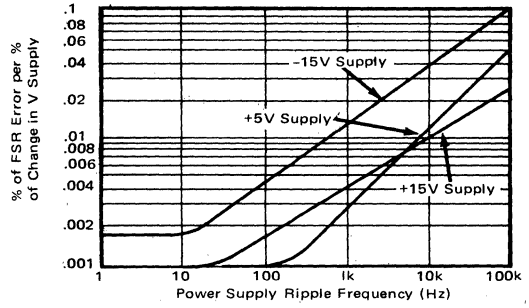


FIGURE 2. Power supply rejection vs. power supply ripple frequency.

TYPICAL PERFORMANCE CURVES

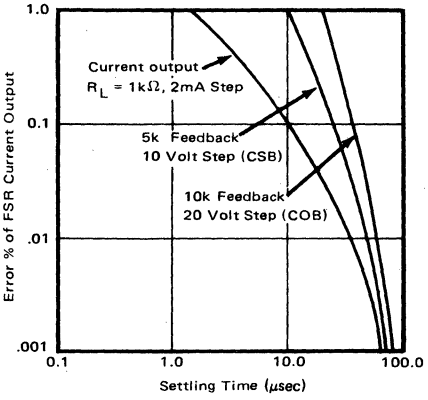


FIGURE 3. Full scale range settling time vs. accuracy.

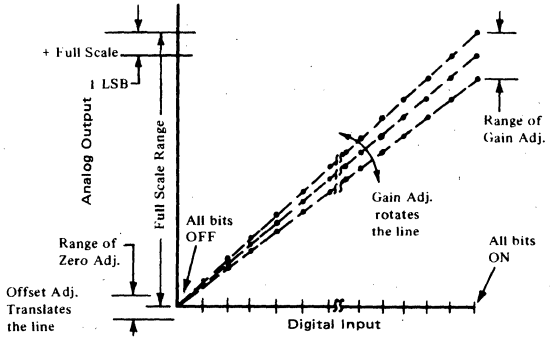


FIGURE 4. Relationship of OFFSET and GAIN adjustments for a UNIPOLAR D/A converter.

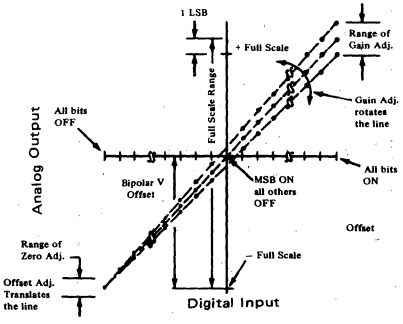


FIGURE 5. Relationship of OFFSET and GAIN adjustments for a BIPOLAR D/A converter.

DIGITAL INPUT AND ANALOG OUTPUT RELATIONSHIPS

DIGITAL INPUT CODE	OUTPUT CODE			
	VOLTAGE		CURRENT	
	16 Bit Resolution	14 Bit Resolution	16 Bit Resolution	14 Bit Resolution
Complementary Unipolar Straight Binary (CSB) 0 to +10V or 0 to -2mA				
One LSB	+153μV	+610μV	0.031mA	0.122μA
All Bits Off	+9.99985V	+9.99939	-1.99997mA	-1.99988mA
All Bits On	Zero	Zero	Zero	Zero
Complementary Bipolar Offset Binary (COB) ±10V or ±1mA				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits Off	+9.99969V	+9.99878V	-0.99997mA	-0.99988mA
All Bits On	-10.0000V	-10.0000V	+1.0000mA	+1.0000mA
Complementary Binary Coded Decimal (CCD) 0 to +10V or 0 to -1.25mA	4 Digit Resolution	N/A	4 Digit Resolution	N/A
One LSB	+1.0mV		0.125μA	
F.S. Bits off	+9.999V		-1.24987mA	
All Bits on	Zero		Zero	

TABLE II. Ideal output voltage and current.

INSTALLATION CONSIDERATIONS

The DAC70 is laser trimmed to 14 bit linearity. The design of the device makes the 16 bit resolution available on binary units. If 16 bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5 V through a single 1 k Ω resistor.

Due to the extremely high resolution and linearity of the DAC70, system design problems such as grounding and contact resistance become very important. For a 16 bit converter with a +10 volt full scale range, one LSB is 153μV. With a load current of 5 mA and series wiring and connector resistance of only 30 mΩ, the output will be in error by 1 LSB. To understand what this means in terms of a system layout, the impedance of #18 wire is about 0.064 Ω/ft. Neglecting contact resistance, less than 6 inches of wire will produce a 1 LSB error in the analog output voltage! Although the problems involved seem enormous, care in the installation planning can minimize the potential causes of error.

The output can be made essentially independent of lead resistance by sensing the output at the load itself as shown in Figure 6. The lead and contact resistance, Z_i, is reduced by the loop gain to acceptable values.

The DAC70 and the wiring to its connector should be located so as to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pick-up is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pick-up in the circuit. The metal case of the unit is internally connected to the common pin to further minimize pick-up. The DAC70 case is made of gold plated Kovar which also provides some electromagnetic shielding.

NOTE:

It is recommended that the digital input lines of the DAC70 be driven from inverters of TTL input registers to obtain specified accuracy.

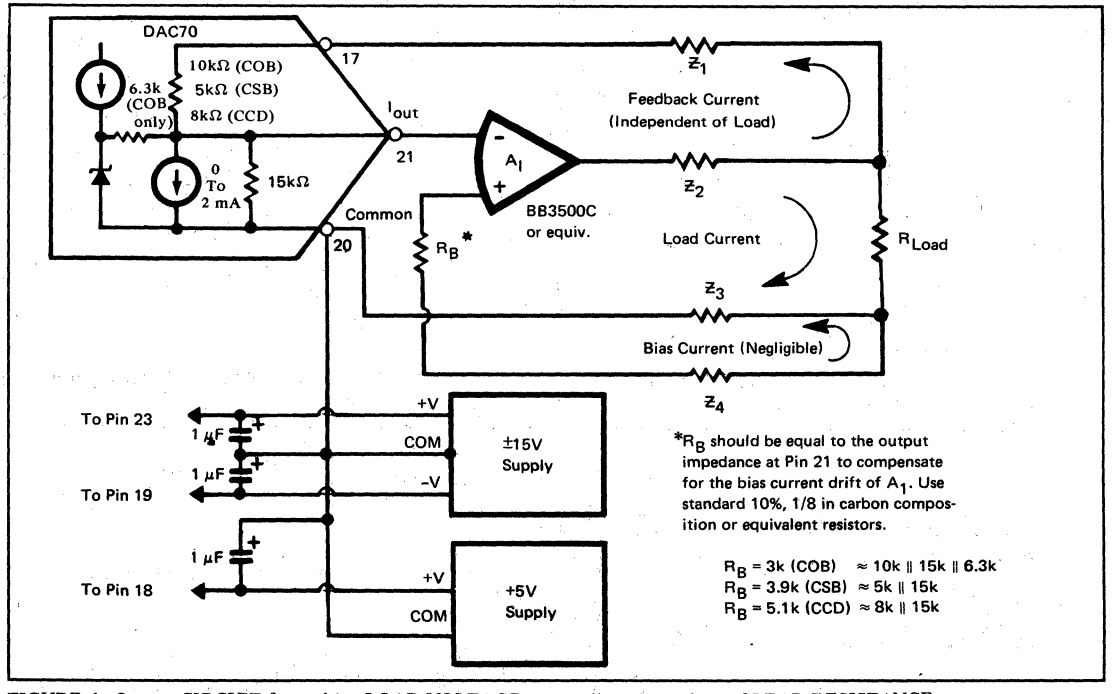


FIGURE 6. Output CIRCUIT for making LOAD VOLTAGE essentially independent of LEAD RESISTANCE.

SUPPLY DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 6. These capacitors should be located close to the DAC70.

EXTERNAL OFFSET AND GAIN ADJ.

Offset and gain may be trimmed by the user with externally connected offset and gain potentiometers. Connection of these potentiometers and the method of adjustment is outlined below. In each case a simplified schematic of the DAC 70 as seen from the adjustment point is given to assist the user in designing his own adjustment networks. Adjust offset first and then gain to avoid interaction (see Figures 4 and 5).

OFFSET ADJUSTMENT

For unipolar (CSB, CCD) D/A converters, apply the digital input code that should give zero volts output and adjust the offset potentiometer for zero volts output. For bipolar (COB) D/A converters, apply the digital input code that should give minus full scale (-10 volts) and adjust the offset potentiometer for an output voltage of -10 volts. Two methods of offset adjustment are shown in Figures 7 & 8.

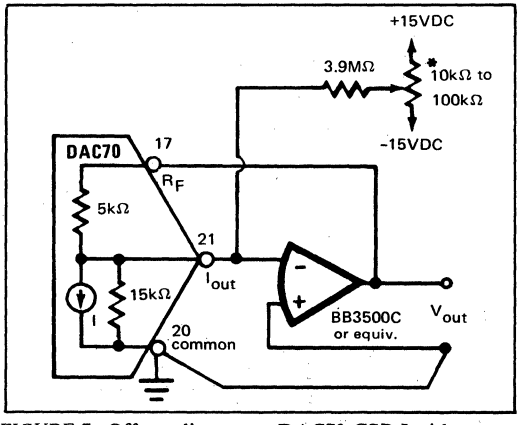


FIGURE 7. Offset adjustment, DAC70-CSB-I with external op amp.

In some applications the use of such a large offset adjustment resistor might be undesirable. An alternative method of offset adjustment is shown in Figure 8:

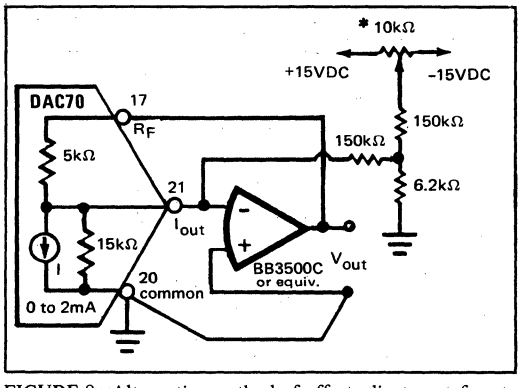


FIGURE 8. Alternative method of offset adjustment for DAC70-CSB-I with external op amp.

GAIN ADJUSTMENT

For either unipolar (CSB, CCD) or bipolar (COB) models, apply the digital input that should give the maximum positive current or voltage output. Adjust the gain potentiometer for this full scale value. The positive full scale voltage and currents for the DAC70 are given in Table II.

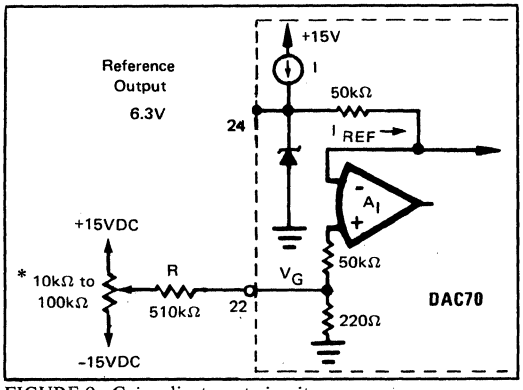


FIGURE 9. Gain adjustment circuit.

Figure 9 shows how the gain adjust works on the DAC70. The gain of the DAC70 is determined by the reference current I_{ref}. Due to the high gain and low bias current of A_1, the voltage at the positive input of A_1 is approximately equal to the voltage at the gain adjust pin V_G. Therefore, the reference current is

$$I_{REF} = \frac{6.3\ V - V_G}{50\ k}$$

Since V_G is approximately equal to zero initially, a simple formula for determining the voltage range necessary at the gain adjust pin for a given percentage change in gain is

$$\Delta V_G = \frac{\%\ Gain\ Change}{100} \times 6.3\ volts$$

The full scale output voltage of the DAC70 with an external output amplifier and internal feedback resistor is laser trimmed to less than ±0.05% of FSR.

REFERENCE SUPPLY

All DAC70 and DAC70C models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5% and is connected internally for specified operation. The zener is selected for a gain drift of typically ±3 ppm/°C and is burned in for a total of 160 hours for guaranteed reliability.

This reference may also be used externally but the current drain is limited to 200 μA. An external buffer amplifier is recommended if the DAC70 internal reference will be used externally in order to supply a constant load to the reference supply output.

NOTE: An external reference cannot be used. The DAC70 internal reference must be used.

* High quality multi-turn (10 turns if possible) potentiometers with less than 100 ppm/°C, T.C.R. should be used.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP

The DAC70 is a current output device and will drive the summing junction of an op amp to produce an output voltage (see Figure 10). The op amp output voltage is:

$$V_{out} = -I_{out} R_f$$

Where I_{out} is the DAC70 output current and R_f is the feedback resistor. Use of the internal feedback resistor (Pin 17) is required to obtain specified gain accuracy and low gain drift.

The DAC70 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±25 ppm/°C. The resistors in the DAC70 are chosen for ratio tracking of ±1 ppm/°C and not absolute T.C.R. (which may be as high as ±25 ppm/°C).

An alternative method of scaling the output voltage of the DAC70 and preserving the low gain drift is shown in Figure 11.

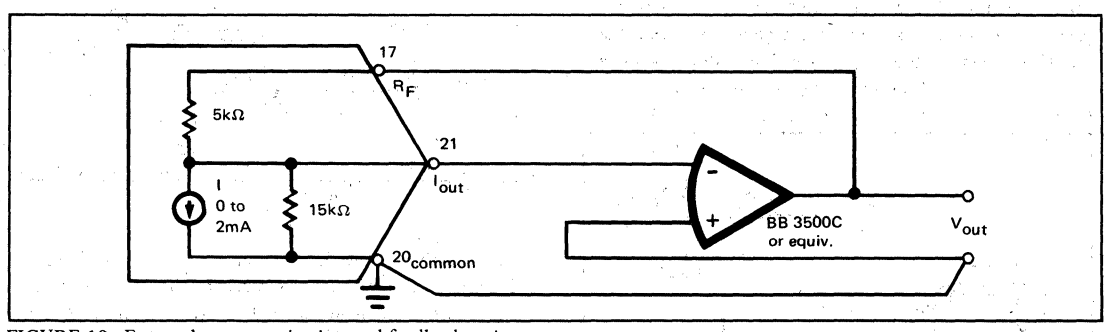


FIGURE 10. External op amp using internal feedback resistors.

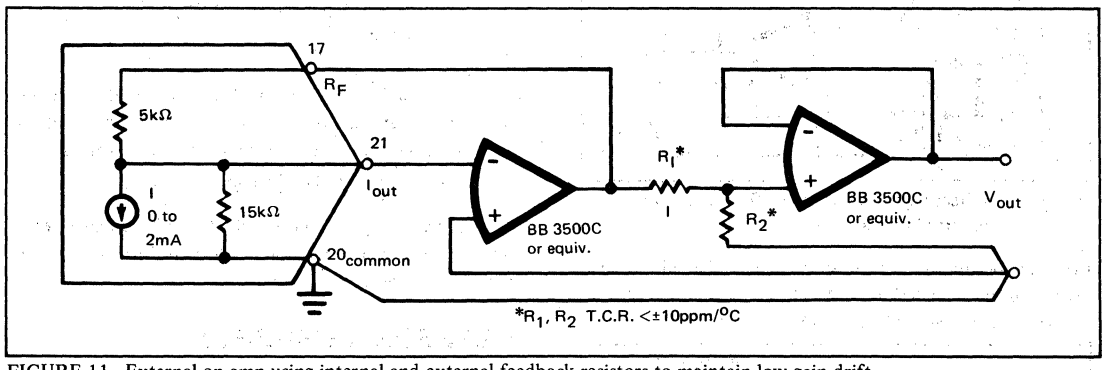


FIGURE 11. External op amp using internal and external feedback resistors to maintain low gain drift.

OUTPUTS LARGER THAN 20 VOLT RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{out} values of ±1 mA for bipolar voltage ranges and -2 mA for unipolar voltage ranges (see Figure 12). Use protection diodes when a high voltage op amp is used.

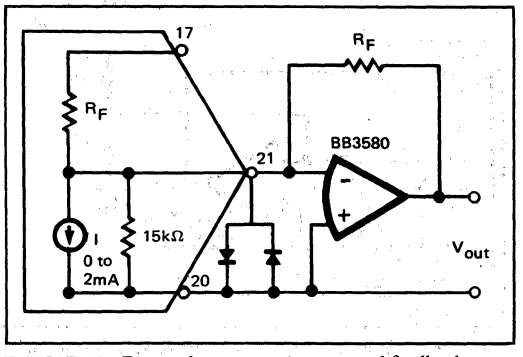
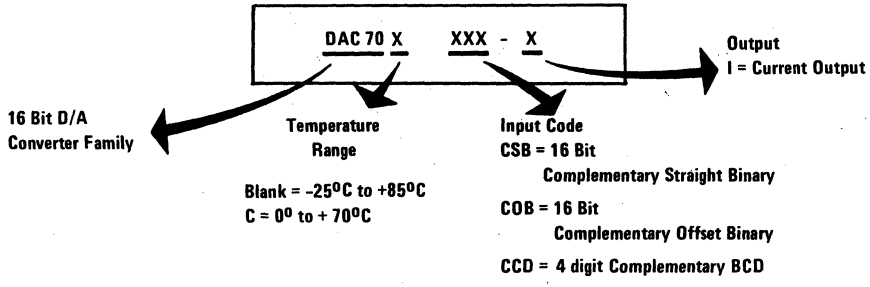
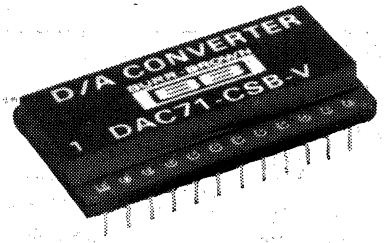


FIGURE 12. External op amp using external feedback resistors.

ORDER INFORMATION



BURR-BROWN®

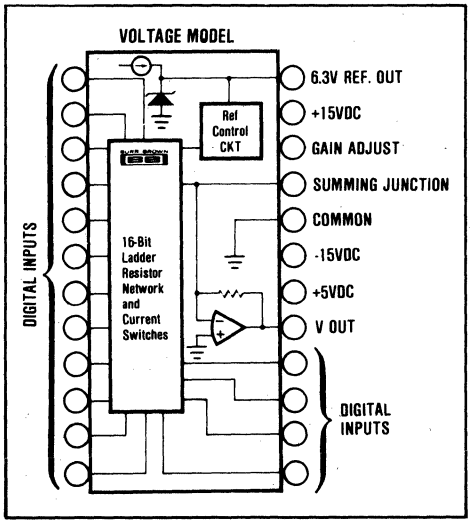


DAC71

High Resolution
16-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT, 4-DIGIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- LOW DRIFT ±7ppm/°C, (TYPICAL)
- CURRENT AND VOLTAGE MODELS
- LOW COST



DESCRIPTION

The DAC71 is a high quality 16-bit hybrid IC D/A converter available in a 24-pin dual-in-line ceramic package.

The DAC71 with internal reference and optional output amplifier offers a maximum linearity error of ±0.003% of FSR at room temperature and a maximum gain drift of ±20ppm/°C over a temperature range of 0°C to +70°C.

Three basic models accept complementary 16-bit binary or complementary 4-digit BCD TTL-compatible input codes.

Packaged within the DAC71 are fast-settling switches and stable laser-trimmed thin-film resistors that let you select output voltages 0 to +10V (CSB and CCD) or ±10V (COB) and output currents of ±1mA or 0 to -2mA. Input power is ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

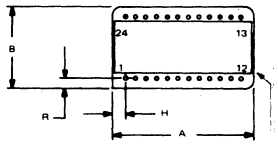
SPECIFICATIONS

ELECTRICAL

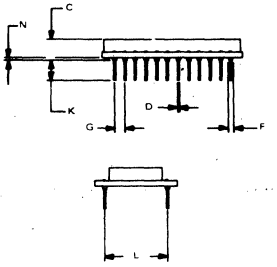
Typical at T_A = 25°C and rated power supplies unless otherwise noted.

MODEL	DAC71			UNITS
	MIN	TYP	MAX	
INPUT				
DIGITAL INPUT				
Resolution, CCD		4		Digits
CSB, COB		16		Bits
Logic Levels (TTL-Compatible)(1)				
Logical "1" (at +40µA)	+2.4		+5.5	VDC
Logical "0" (at -1.6mA)	0		+0.4	VDC
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error at 25°C, CCD			±0.005	% of FSR(2)
COB, CSB			±0.003	% of FSR
Gain Error,(3) Voltage		±0.01	±0.1	%
Current		±0.05	±0.25	%
Offset Error,(3) Voltage, Unipolar		±0.1	±2	mV
Voltage, Bipolar			±5	mV
Current, Unipolar			±1	µA
Current, Bipolar			±5	µA
Monotonicity Temperature Range (14 bits)	0		+50	°C
DRIFT (Over specified temp. range)				
Total Bipolar Drift (includes gain,				
offset, and linearity drift) (4) Voltage		±7	±15	ppm of FSR/°C
Current		±15	±50	ppm of FSR/°C
Total Error over Temperature Range(5)				
Voltage, Unipolar			±0.083	% of FSR
Bipolar			±0.071	% of FSR
Current, Unipolar			±0.23	% of FSR
Bipolar			±0.23	% of FSR
Gain, Voltage			±20	ppm/°C
Current			±60	ppm/°C
Offset				
Voltage, Unipolar		±1	±2	ppm of FSR/°C
Bipolar			±10	ppm of FSR/°C
Current, Unipolar			±1	ppm of FSR/°C
Bipolar			±40	ppm of FSR/°C
Differential Linearity over Temperature			±2	ppm of FSR/°C
Linearity Error over Temperature			±2	ppm of FSR/°C
SETTLING TIME				
Voltage Models (to ±0.003% of FSR)				
Output: 20V Step		5	10	µsec
1LSB Step(6)		3	5	µsec
Slew Rate		20		V/µsec
Current Models (to ±0.003% of FSR)				
Output: 2mA step 10Ω to 100Ω Load			1	µsec
1kΩ Load			3	µsec
Switching Transient		500		mV
OUTPUT				
ANALOG OUTPUT				
Voltage Models				
Ranges - CSB, CCD		0 to +10		V
COB		±10		V
Output Current	±5			mA
Output Impedance (DC		0.05		Ω
Short Circuit Duration		Indefinite to Common		
Current Models				
Ranges - CSB, CCD		0 to -2		mA
COB		±1		mA
Output Impedance - Unipolar		15		kΩ
Bipolar		4.4		kΩ
Compliance		±2.5		V
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	V
Maximum External Current(7)			±200	µA
Temperature Coefficient of Drift			±10	ppm/°C

MECHANICAL



NOTE: Leads in true position within 0.10" 0.25mm R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	0.85	.105	2.16	2.67

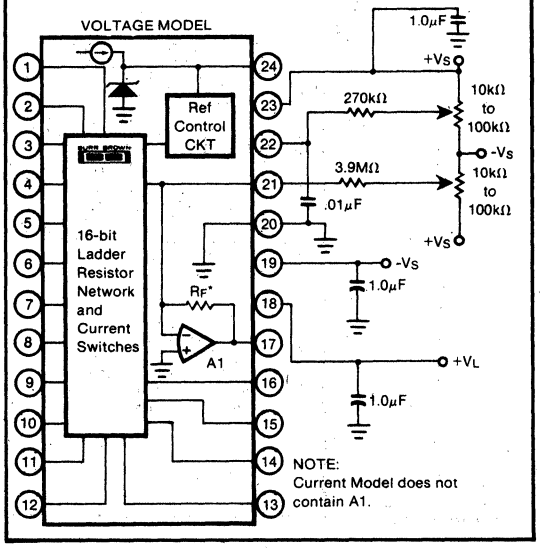
CASE: Ceramic
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 condition C step 1 (fluorocarbon of MIL-STD-883 (gross leak).

MODEL	DAC71			UNITS
	MIN	TYP	MAX	
POWER SUPPLY SENSITIVITY				
Unipolar Offset				
±15VDC		±0.0001		% of FSR/%V_S
+15VDC		±0.0001		% of FSR/%V_S
Bipolar Offset				
±15VDC		±0.0004		% of FSR/%V_S
+5VDC		±0.0001		% of FSR/%V_S
Gain				
±15VDC		±0.001		% of FSR/%V_S
+5VDC		±0.0005		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS				
Voltage	±14.5, +4.75	±15, +5	±15.5, +5.25	VDC
Supply Drain, ±15VDC (no load)		±25	±35	mA
+5VDC (logic supply)		+20	+35	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating (double above Drift Specs)	-25		+85	°C
Storage	-55		+100	°C

NOTES:

1. Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility. The percent change in output (ΔV_O) as logic 0 varies from 0.0V to +0.4V and logic 1 changes from +2.4V to +5.0V on all inputs is less than 0.006% of FSR.
2. FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc.
3. Adjustable to zero with external trim potentiometer.
4. See "Computing Total Accuracy over Temperature".
5. With gain and offset errors adjusted to zero at 25°C.
6. LSB is for 14-bit resolution.
7. Maximum with no degradation of specifications.

CONNECTION DIAGRAM



*R_F = 5kΩ (CSB), 10kΩ (COB), 8kΩ (CCD).

PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
R_F	17	V_{OUT}
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
I_{OUT}	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6.3V REF. OUT	24	6.3V REF. OUT

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC71 accepts complementary digital input codes in either binary (CSB, COB) or decimal (CCD) format. The COB model may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES					
			CSB	COB	CTC*
CSB, COB MODELS		MSB LSB	Compl. Straight Binary	Compl. Offset Binary	Compl. Two's Complement
	All bits ON	0000...000	+Full Scale	+Full Scale	-1LSB
	Mid Scale	0111...111	+1/2 Full Scale	Zero	-Full Scale
	All bits OFF	1111...111	Zero	-Full Scale	Zero
		1000...000	Mid Scale -1LSB	-1LSB	+Full Scale
CCD MODELS			CCD Complementary Coded Decimal 4 Digits		*Invert the MSB of the COB code with an external inverter to obtain CTC code.
	F.S. bits ON	0110...0110	+Full Scale		
	All Bits OFF	1111...1111	Zero		

ACCURACY

LINEARITY

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.003% max (CSB, COB) or ±0.005% max (CCD) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can be anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent input stage to the next.

MONOTONICITY

Monotonicity over 0°C to +50°C is guaranteed. This insures that the analog output will increase or remain the same for increasing 14-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (see Figure 1). Gain Drift is established by: 1) testing the end point differences for each DAC71 model at +25°C and the appropriate specification temperature extremes; 2) calculating the gain error with respect to the +25°C value; and 3) dividing by the temperature change. This is expressed in ppm/°C.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range.

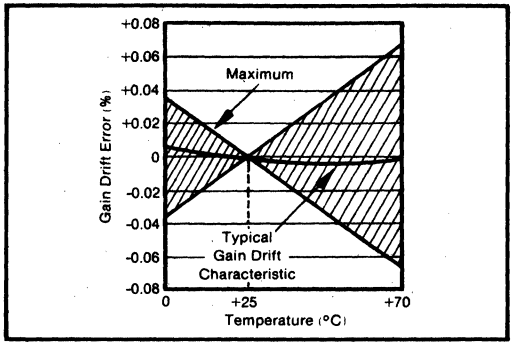


FIGURE 1. Gain Drift Error (%) vs Temperature.

The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC71 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 2).

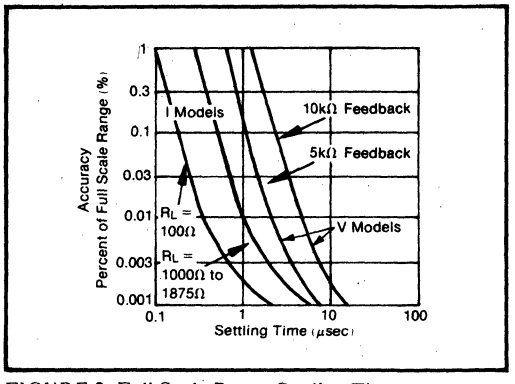


FIGURE 2. Full Scale Range Settling Time vs Accuracy.

VOLTAGE OUTPUT MODELS

Settling times are specified to ±0.003% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

CURRENT OUTPUT MODELS

Two settling time are specified to ±0.003% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω.

COMPLIANCE

Compliance voltage is the maximum voltage swing

allowed on the output of the current models while maintaining specified accuracy. The typical compliance voltage of all current output models is ±2.5V and maximum safe voltage swing permitted without damage is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 3).

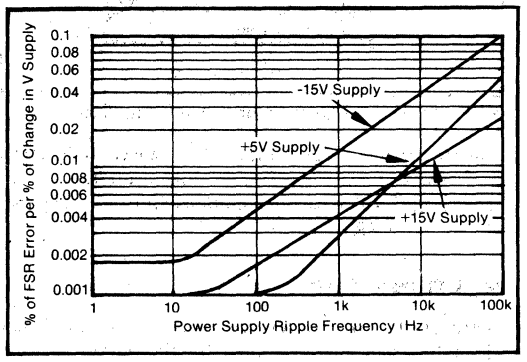


FIGURE 3. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All DAC71 models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5% and is connected internally for specified operation. The zener is selected for a Gain Drift of typically ±3ppm °C and is burned-in for a total of 168 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 200μA. An external buffer amplifier is recommended if the DAC71 internal reference is used externally in order to provide a constant load to the reference supply output.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC71. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (20% carbon or better) should be located close to the DAC71 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to Figures 5 and 6 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

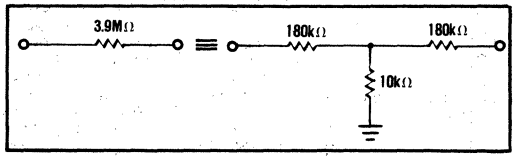


FIGURE 4. Equivalent Resistances.

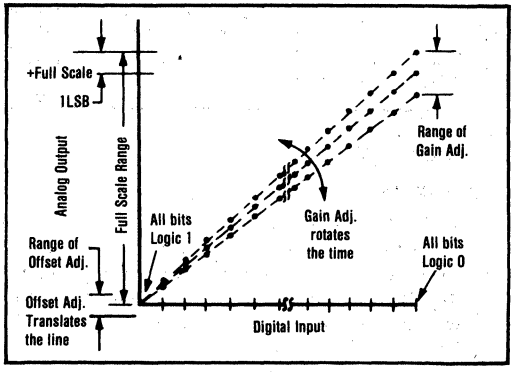


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

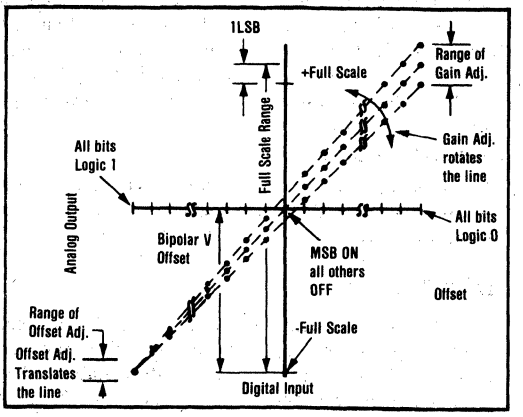


FIGURE 6. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential

output and adjust the offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. The COB model is internally connected for a 20V FSR range where the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

TABLE II. Digital Input and Analog Output Relationships.

DIGITAL INPUT CODE	OUTPUT CODE			
	VOLTAGE		CURRENT	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Unipolar Straight Binary CSB 0 to +10V or 0 to -2mA*				
One LSB	+153μV	+610μV	0.031μA	0.122μA
All Bits ON 00...00	+9.99985V	+9.99939V	-1.99997mA	-1.99988mA
All Bits OFF 11...11	Zero	Zero	Zero	Zero
Complementary Bipolar Offset Binary COB ±10V or ±1mA*				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits ON 00...00	+9.99969V	+9.99878V	-0.99997mA	-0.99988mA
All Bits OFF 11...11	-10.0000V	-10.0000V	-1.0000mA	-1.0000mA
Complementary Binary Coded Decimal CCD 0 to +10V or 0 to -1.25mA	4-Digit Resolution	N/A	4-Digit Resolution	N/A
One LSB	+1.0mV		0.125μA	
Full Scale 0110...0110	+9.999V		-1.24987mA	
All Bits OFF 1111...1111	Zero		Zero	

* To obtain values for other binary CBI ranges 0 to -5V range, divide 0 to +10V range by 2; ±5V range, divide ±10V range by 2, ±2.5V range, divide ±10V range by 4.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

The DAC71 is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available on binary units. If 16-bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5VDC through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the DAC71, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ, the output will be in error by 1LSB. To understand what this means in terms of a system layout, the impedance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 6 inches of wire will produce a 1LSB error in the analog output voltage! Although the problems involved seem enormous, care in the installation planning can minimize the potential causes of error.

Figure 7 shows the connection diagram for a voltage output DAC71. Lead and contact resistances are represented by R_1 through R_5. As long as the load resistance (R_L) is constant, R_2 simply introduces a gain error than can be removed during initial calibration. R_3 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable then R_2 should be less than $R_{L\min}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if $R_{L\min}$ is 5kΩ then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the DAC71 for optimum performance.

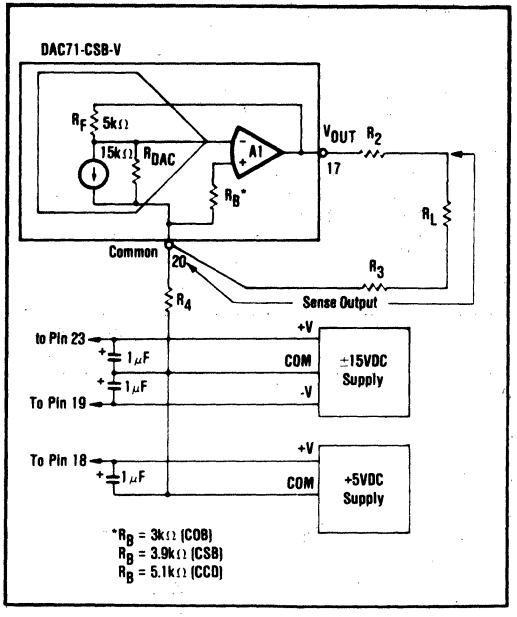


FIGURE 7. Output Circuit for Voltage Models.

Figures 8 and 9 show two methods of connecting current model DAC71's with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A1 at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated during initial calibration. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain. If the output cannot be sensed at Common (pin 20), then the differential output circuit shown in Figure 9 is recommended. In this circuit the output voltage is sensed at the load common and not at the DAC common as in the previous circuits. The value of R_6 and R_5 must be adjusted for maximum common-mode rejection at R_L. Note that if R_5 is negligible the circuit of Figure 9 can be reduced to the one shown in Figure 8 because $R_B = (R_5 + R_6) \parallel R_6$. In all three circuits the effect of R_4 is negligible.

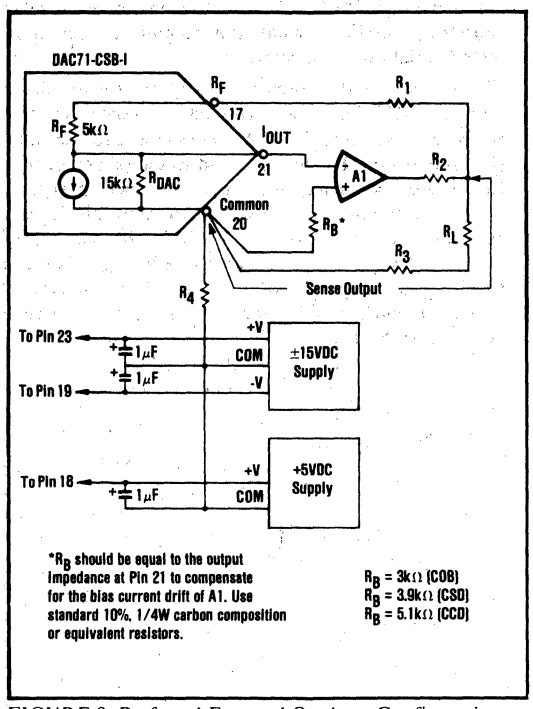


FIGURE 8. Preferred External Op Amp Configuration.

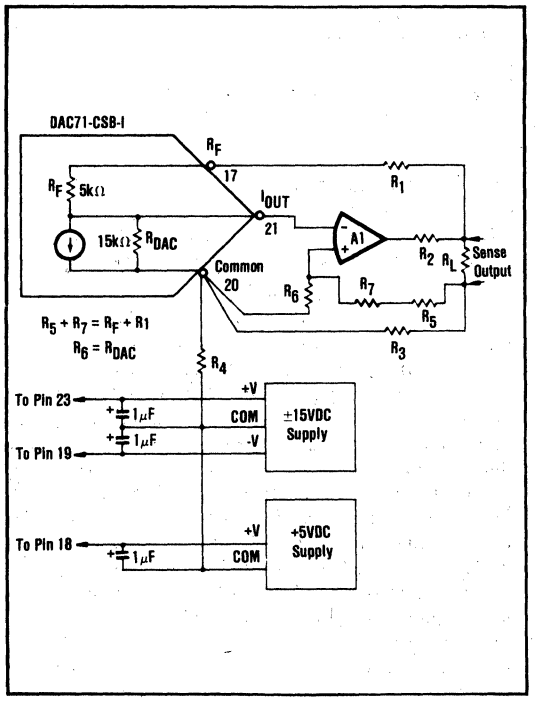


FIGURE 9. Differential Sensing Output Op Amp Configuration.

The DAC71 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

NOTE: It is recommended that the digital input lines of the DAC71 be driven from inverters or buffers of TTL input registers to obtain specified accuracy.

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, R_L, with the current output model connected as shown in Figure 10, will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA[(15k\Omega \times R_L)/(15k\Omega + R_L)]$$

Where R_L max = 1.36kΩ

and V_{OUT} max = -2.5V

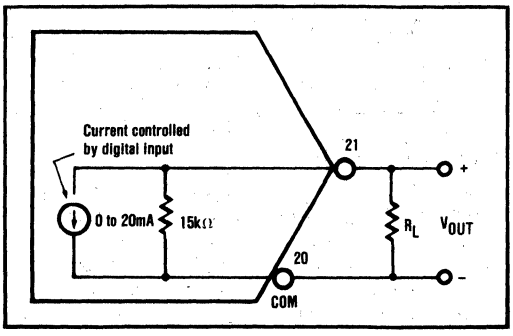


FIGURE 10. Equivalent Circuit DAC71-CSB-I Connected for Unipolar Voltage Output with Resistive Load.

Add an external low T.C. (<10ppm °C) resistor (R_L) as shown in Figure 11 to obtain a 0 to -2V full scale output voltage range for CCD input codes.

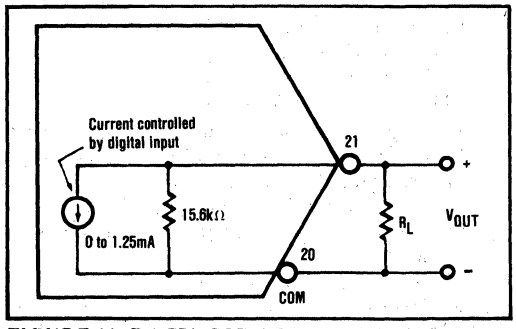


FIGURE 11. DAC71-CCD-I Connected for Voltage Output with Resistive Load.

$V_{OUT} = -1.25mA[(15.6k\Omega \times R_L)/(15.6k\Omega + R_L)]$
Where R_L max = 1.79kΩ
and V_{OUT} max = -2.01V

DRIVING A RESISTIVE LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12. V_{OUT} is determined by:

$V_{OUT} = \pm 1mA[(4.44k\Omega \times R_L)/(4.44k\Omega + R_L)]$
Where R_L max = 5.72kΩ
and V_{OUT} max = ±2.5V

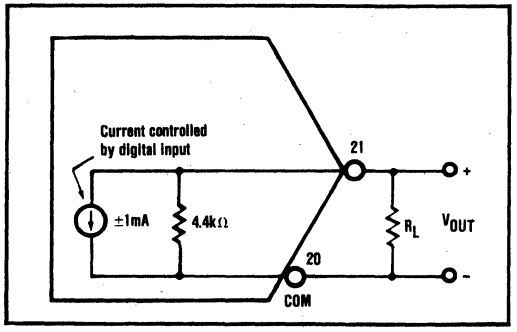


FIGURE 12. DAC71-COB-I Connected for Bipolar Output Voltage with Resistive Load.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DAC

The DAC71-(CSB, COB, CCD)-I are current output devices and will drive the summing junction of an op amp to produce an output voltage (see Figure 13). The op amp output voltage is:

$$V_{OUT} = -I_{OUT} R_F$$

where I_{OUT} is the DAC71 output current and R_F is the feedback resistor. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

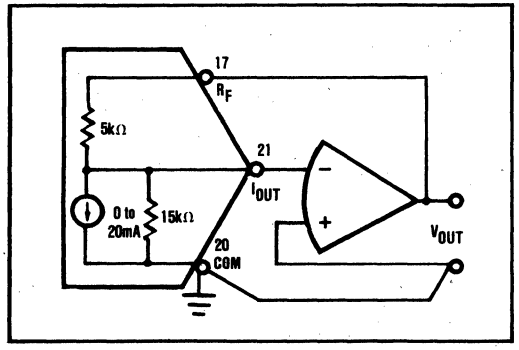


FIGURE 13. External Op Amp Using Internal Feedback Resistors.

The DAC71 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±25ppm/°C. The resistors in the DAC71 are chosen for ratio tracking of ±1ppm/°C and not absolute TCR (which may be as high at ±25ppm/°C.)

An alternative method of scaling the output voltage of the DAC71 and preserving the low gain drift is shown in Figure 14.

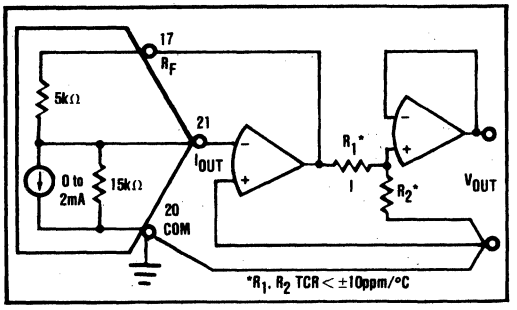


FIGURE 14. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

OUTPUTS LARGER THAN 20-VOLT RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges (see Figure 15). Use protection diodes when a high voltage op amp is used.

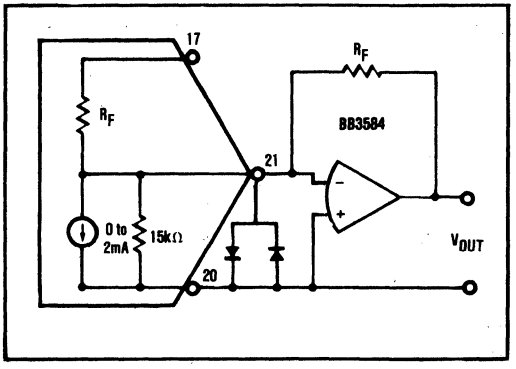


FIGURE 15. External Op Amp Using External Feedback Resistors.

COMPUTING TOTAL ACCURACY OVER TEMPERATURE

The accuracy drift with temperature of a DAC71 consists of three primary components: gain drift, unipolar or bipolar offset drift, and linearity drift. To obtain the

worst-case accuracy drift, most users would assume that all drift errors are random and would simply add them algebraically. However, the worst-case accuracy drift for a DAC71 operating in the bipolar mode is about one-half of the algebraic sum of the individual drift errors.

To explain this fact, it is necessary to consider the unipolar and bipolar modes of operation separately.

In the unipolar mode of operation, offset drift (±1ppm/°C) is due primarily to voltage offset drift of the output op amp and, to a lesser extent, to the leakage current through the quad current switches. Gain drift consists of several components: 1) ±5ppm/°C due to ratio drift of current switch V_{BE} to the reference transistor, 2)±10ppm/°C due to the zener reference and, 3) ±2ppm/°C linearity drift due to ratio drift of current weighting resistors and V_{BE} of the quad current switches. The sum of these three components, ±17ppm/°C, is the maximum gain drift.

Because the parameters described could all drift in the same direction, the worst-case accuracy drift in the unipolar mode is simply the sum of the components, or ±18ppm/°C.

In the bipolar mode the major portion of gain drift is due to the zener reference. The gain and offset drifts caused by reference drift are always in opposite directions. Therefore, the accuracy drift will be the difference rather than the sum of these drifts.

First, consider the effect of reference variations on offset drift. Figure 16 shows a simplified circuit diagram of a DAC71-COB-V with all bits off. The current switch leakage current is negligible, so

$$V_{-FULL\ SCALE} = (-R_F/R_{BPO}) \cdot V_{REF}$$
$$= (-10k\Omega/6.3k\Omega) \cdot 6.3V = -10V$$

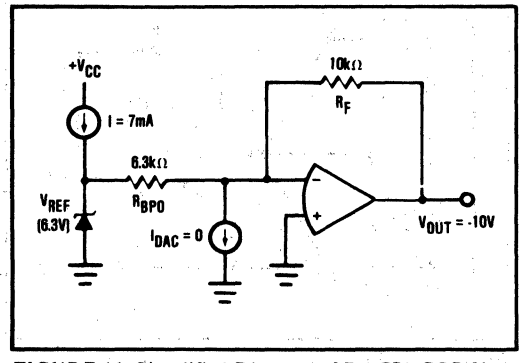


FIGURE 16. Simplified Diagram of DAC71-COB-V with "All Bits Off" (±10V Range).

This equation shows that if V_{REF} increases, the output voltage will decrease and vice versa. If the V_{REF} drift is +10ppm/°C, this equivalent to (+10ppm/°C) x (+6.3V) = +63μV/°C. This will result in a voltage drift at the amplifier output of

$$\Delta V_{-FS}/\Delta T = -(R_F/R_{BPO}) \cdot (\Delta V_{REF}/\Delta T)$$
$$= -(10k\Omega/6.3k\Omega) \cdot (63\mu V/°C) = -100\mu V/°C.$$

Since the DAC71-COB-V is operating in the ±10V range this equivalent to (-100μV/°C) ÷ (20V range) = -5ppm of FSR/°C.

Now consider the effect of reference changes on gain drift. When all of the bits are turned on it can be shown that:

$$\Delta V_{+FULL\ SCALE}/\Delta T = +(R_F/R_{BPO}) \cdot (\Delta V_{REF}/\Delta T)$$
$$= +(10k\Omega/6.3k\Omega) \cdot (63\mu V/°C) = +100\mu V/°C.$$

and (+100μV/°C) 20V Range = +5ppm/°C of FSR.

This result indicates that the drift of the minus full scale voltage will be equal in magnitude to, and in the opposite direction of, the drift of the plus full scale voltage and that zener reference variations have virtually no effect on the zero point (see Figure 17). This equation also indicates that the gain drift is equal to the V_{REF} drift in ppm/°C, and the magnitude of the minus full scale drift and plus full scale drift is equal to one-half of the V_{REF} drift.

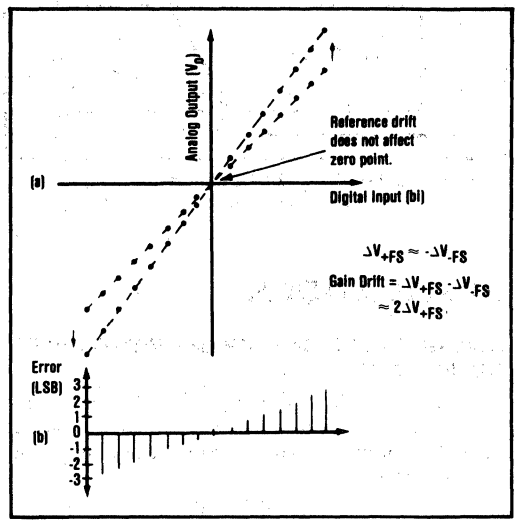


FIGURE 17. (a) Effect of a Positive Reference Drift on the Ideal D. A Transfer Function; (b) Error Distribution Due to Reference Voltage Drift in a DAC71.

Using this relationship, the worst-case accuracy drift for a DAC71-COB-V can be computed. The maximum TCR of the zener reference is ±10ppm °C. The gain drift due to the reference then is also ±10ppm °C. The full scale drift and bipolar offset drift are each half that amount or ±5ppm °C. The maximum gain and offset drifts of the DAC71, exclusive of the reference, are ±5 and ±3ppm °C respectively. Adding this to the full scale drift due to the reference plus the linearity drift of ±2ppm °C gives a worst-case total accuracy drift of ±15ppm °C. (Random drifts, which these are, can be in the same direction so they add directly.) This is much less than the total drift obtained by simply adding the maximum gain, bipolar offset, and linearity drifts (±27ppm °C). The maximum

zero point drift is equal to one-half of the gain drift exclusive of the reference plus the offset drift exclusive of the reference, or ±5.5ppm of FSR/°C.

The DAC71 is specified over a 0°C to +70°C temperature range giving a maximum excursion from room temperature (+25°C) of 45°C. Assuming that gain and offset errors have been adjusted to zero at room temperature,

total worst-case accuracy error
= Linearity error + Accuracy drift x ΔT
= ±0.003% + ±15ppm/°C (45°) (100)
= ±0.07%

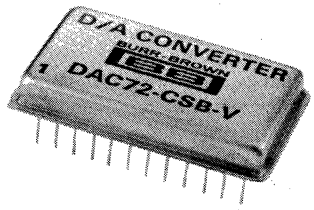
total worst-case bipolar zero point error
= Bipolar zero drift x ΔT
= ±5.5ppm of FSR% (45°C) (100)
= ±0.025%

ORDERING INFORMATION

MODEL	INPUT CODE
CURRENT MODELS	
DAC71-COB-I	Complementary Offset Binary
DAC71-CSB-I	Complementary Straight Binary
DAC71-CCD-I	Complementary Coded Decimal
VOLTAGE MODELS	
DAC71-COB-V	Complementary Offset Binary
DAC71-CSB-V	Complementary Straight Binary
DAC71-CCD-V	Complementary Coded Decimal

BURR-BROWN®

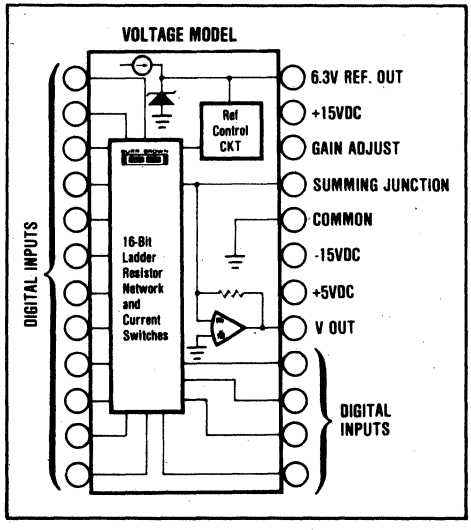
DAC72



High Resolution
16-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT, 4-DIGIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- LOW DRIFT ±5ppm/°C, TYPICAL
- AVAILABLE IN TWO TEMPERATURE RANGES:
  0°C to +70°C
  -25°C to +85°C
- CURRENT AND VOLTAGE MODELS
- LOW COST
- METAL HERMETIC PACKAGE



DESCRIPTION

The DAC72 is a high quality 16-bit hybrid IC D/A converter in a 24-pin dual-in-line metal package.

DAC72 with internal reference and optional output amplifier offers a maximum linearity error of ±0.003% of FSR at room temperature and a maximum gain drift of ±20ppm/°C over a temperature range of 0°C to +70°C. DAC72 offers a maximum linearity error of ±0.003% of FSR at room temperature and a gain drift of ±20ppm/°C from −25°C to +85°C.

Three basic models accept complementary 16-bit binary or complementary 4-digit BCD TTL-compatible input codes.

Packaged within the DAC72 are fast-settling switches and stable laser-trimmed thin-film resistors that let you select output voltages 0 to +10V (CSB and CCD) or ±10V (COB) and output currents of ±1mA or 0 to -2mA. Input power is ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

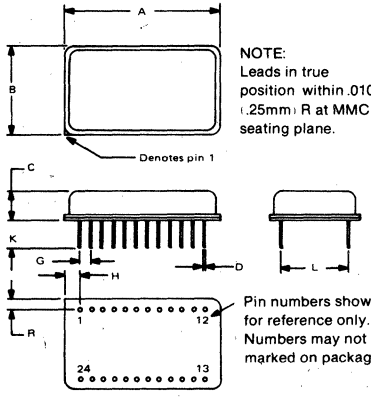
MODEL	DAC72C			DAC72			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution, CCD		4			4		Digits
CSB, COB		16			16		Bits
Logic Levels TTL-Compatible(1)							
Logical "1" at +40µA	+2.4		+5.5	+2.4		+5.5	VDC
Logical "0" at -1.6mA	0		+0.4	0		+0.4	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error at 25°C, CCD			±0.005			±0.005	% of FSR(2)
COB, CSB			±0.003			±0.003	% of FSR
Gain Error(3), Voltage		±0.05	±0.15		±0.05	±0.15	%
Current		±0.05	±0.25		±0.05	±0.25	%
Offset Error(3), Voltage, Unipolar		±0.1	±2		±0.1	±2	mV
Voltage, Bipolar			±10			±10	mV
Current, Unipolar			±1			±1	µA
Current, Bipolar			±5			±5	µA
Monotonicity Temp. Range 14-bits	0		+50	0		+70	°C
DRIFT Over specified temp. range							
Total Bipolar Drift includes gain, offset,							
and linearity drift(4), Voltage hot/cold(5)		±7	±15		±5	±11/±19	ppm of FSR/°C
Current		±15	±50		±10	±40	ppm of FSR/°C
Total Error over Temp. Range(6)							
Voltage, Unipolar hot/cold(5)			±0.083			±0.072/±0.10	% of FSR
Bipolar hot/cold(5)			±0.071			±0.072/±0.10	% of FSR
Current, Unipolar			±0.23			±0.24	% of FSR
Bipolar			±0.23			±0.24	% of FSR
Gain, Voltage hot/cold(5)			±20		±5	±20	ppm/°C
Current			±60			±47	ppm/°C
Offset							
Voltage, Unipolar		±1	±2		±1	±2	ppm of FSR/°C
Bipolar			±10			±8	ppm of FSR/°C
Current, Unipolar			±1			±1	ppm of FSR/°C
Bipolar			±40			±35	ppm of FSR/°C
Differential Linearity over Temperature			±2			±1	ppm of FSR/°C
Linearity Error over Temperature			±2			±1	ppm of FSR/°C
SETTLING TIME							
Voltage Models to ±0.003% of FSR							
Output: 20V Step		5	10		5	10	µsec
1LSB Step(7)		3	5		3	5	µsec
Slew Rate		20			20		V/µsec
Current Models to ±0.003% of FSR							
Output: 2mA step 10Ω to 100Ω Load			1			1	µsec
1kΩ Load			3			3	µsec
Switching Transient		500			500		mV
OUTPUT							
ANALOG OUTPUT							
Voltage Models							
Ranges - CSB, CCD		0 to +10			0 to +10		V
COB		±10			±10		V
Output Current	±5			±5			mA
Output Impedance DC		0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
Current Models							
Ranges - CSB, CCD		0 to -2			0 to -2		mA
COB		±1			±1		mA
Output Impedance - Unipolar		15			15		kΩ
Bipolar		4.4			4.4		kΩ
Compliance		±2.5			±2.5		V
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Maximum External Current(8)			±200			±200	µA
Temp. Coeff. of Drift			±10			±5	ppm/°C

MODEL	DAC72C			DAC72			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY SENSITIVITY							
Unipolar Offset							
±15VDC		±0.0001			±0.0001		% of FSR/% V_S
+15VDC		±0.0001			±0.0001		% of FSR/% V_S
Bipolar Offset							
±15VDC		±0.0004			±0.0004		% of FSR/% V_S
+5VDC		±0.0001			±0.0001		% of FSR/% V_S
Gain							
±15VDC		±0.001			±0.001		% of FSR/% V_S
+5VDC		±0.0005			±0.0005		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS							
Voltage	±14.5, +4.75	±15, +5	±15.5, +5.25	±14.5, +4.75	±15, +5	±15.5, +5.25	VDC
Supply Drain, ±15VDC (no load)		±25	±35		±25	±35	mA
+5VDC (logic supply)		+20	+35		±20	+35	mA
TEMPERATURE RANGE							
Specification	0		+70	-25		+85	°C
Operating (double above Drift Specs)	-25		+85	-55		+100	°C
Storage	-55		+100	-55		+110	°C

NOTES:

1. Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility. The percent change in output (ΔV_O) as logic 0 varies from 0.0V to 0.4V and logic 1 changes from +2.4V to +5.0V on all inputs is less than 0.006% of FSR.
2. FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc.
3. Adjustable to zero with external trim potentiometer.
4. See "Computing Total Accuracy over Temperature".
5. Hot ≡ +25°C to +85°C; Cold ≡ -25°C to +25°C for DAC72.
6. With gain and offset errors adjusted to zero at 25°C.
7. LSB is for 14-bit resolution.
8. Maximum with no degradation of specifications.

MECHANICAL



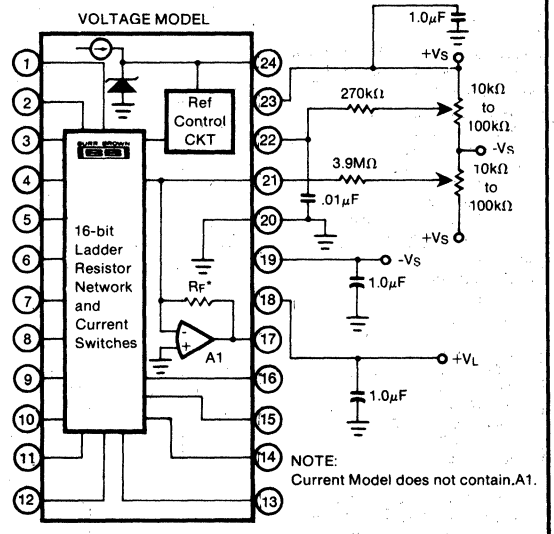
NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

CASE: Nickel Plated Steel
MATING CONNECTOR:245MC
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

CONNECTION DIAGRAM



NOTE:
Current Model does not contain A1.

*R_F = 5kΩ (CSB), 10kΩ (COB), 8kΩ (CCD).

PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
R_F	17	V_{OUT}
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
I_{OUT}	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6.3V REF. OUT	24	6.3V REF. OUT

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC72 accepts complementary digital input codes in either binary (CSB, COB) or decimal (CCD) format. The COB model may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

			DIGITAL INPUT CODES		
			CSB	COB	CTC*
CSB, COB MODELS		MSB LSB	Compl. Straight Binary	Compl. Offset Binary	Compl. Two's Complement
	All bits ON	0000...000	+Full Scale	+Full Scale	-1LSB
	Mid Scale	0111...111	+1/2 Full Scale	Zero	-Full Scale
	All bits OFF	1111...111	Zero	-Full Scale	Zero
		1000...000	Mid Scale -1LSB	-1LSB	+Full Scale
CCD MODELS			CCD		*Invert the MSB of the COB code with an external inverter to obtain CTC code.
			Complementary Coded Decimal 4 Digits		
	F.S. bits ON	0110...0110	+Full Scale		
	All Bits OFF	1111...1111	Zero		

ACCURACY

LINEARITY

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.003% max (CSB, COB) or ±0.005% max (CCD) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can be anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent input stage to the next.

MONOTONICITY

Monotonicity over 0°C to +50°C (DAC72C) and 0°C to +70°C (DAC72) is guaranteed. This insures that the analog output will increase or remain the same for increasing 14-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (see Figure 1). Gain Drift is established by: 1) testing the end point differences for each DAC72 model at +25°C and the appropriate specification temperature extremes; 2) calculating the gain error with respect to the +25°C value; and 3) dividing by the temperature change. This is expressed in ppm/°C.

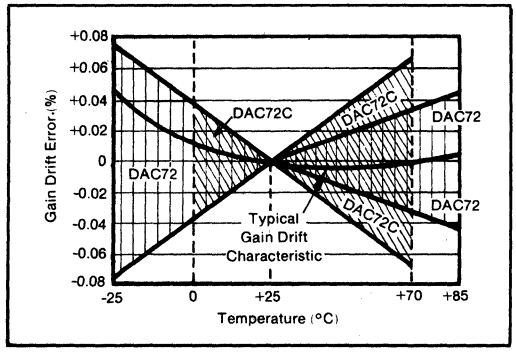


FIGURE 1. Gain Drift Error (%) vs Temperature.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range.

The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC72 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 2).

VOLTAGE OUTPUT MODELS

Settling times are specified to ±0.003% of FSR; one for maximum full scale range changes of 20V and one for a

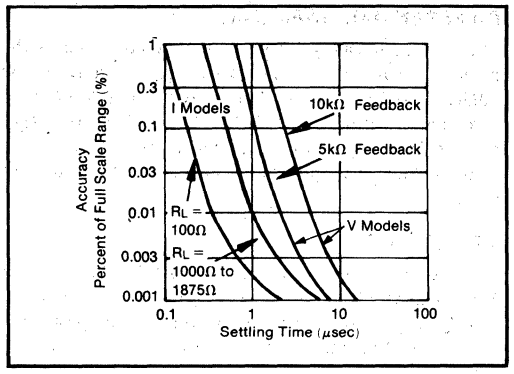


FIGURE 2. Full Scale Range Settling Time vs Accuracy.

1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

CURRENT OUTPUT MODELS

Two settling times are specified to ±0.003% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the output of the current models while maintaining specified accuracy. The typical compliance voltage of all current output models is ±2.5V and maximum safe voltage swing permitted without damage is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 3).

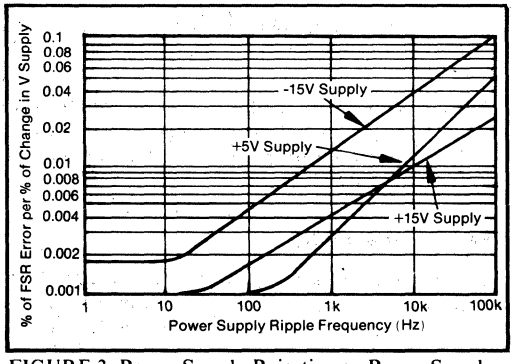


FIGURE 3. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All DAC72 models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5% and is connected internally for specified operation. The zener is selected for a Gain Drift of typically ±3ppm/°C and is burned-in for a total of 168 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 200μA. An external buffer amplifier is recommended if the DAC72 internal reference is used externally in order to provide a constant load to the reference supply output.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC72. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers **should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (20% carbon or better) should be located close to** the DAC72 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic

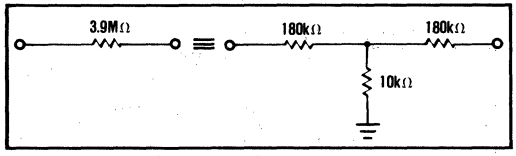


FIGURE 4. Equivalent Resistances.

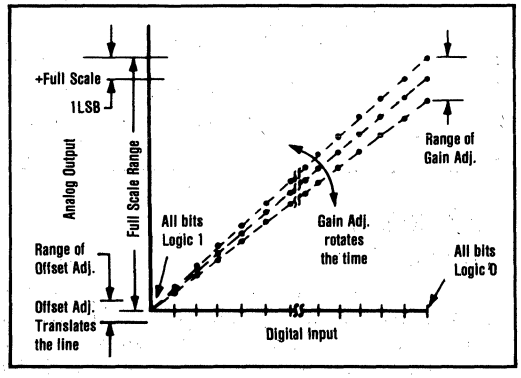


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to Figures 5 and 6 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

If the full (absolute) accuracy capability of the DAC72 is required, recalibration of gain and offset every 2 months is recommended.

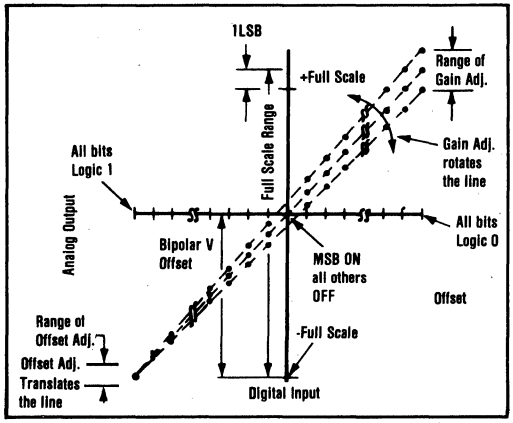


FIGURE 6. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. The COB model is internally connected for a 20V FSR range where the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

TABLE II. Digital Input and Analog Output Relationships.

DIGITAL INPUT CODE	OUTPUT CODE			
	VOLTAGE		CURRENT	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Unipolar Straight Binary (CSB) 0 to +10V or 0 to -2mA*				
One LSB	+153μV	+610μV	0.031μA	0.122μA
All Bits ON (00...00	+9.99985V	+9.99939V	-1.99997mA	-1.99988mA
All Bits OFF (11...11	Zero	Zero	Zero	Zero
Complementary Bipolar Offset Binary (COB ±10V or ±1mA*				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits ON (00...00	+9.99969V	+9.99878V	-0.99997mA	-0.99988mA
All Bits OFF (11...11)	-10.0000V	-10.0000V	+1.0000mA	+1.0000mA
Complementary Binary Coded Decimal (CCD 0 to +10V or 0 to -1.25mA	4-Digit Resolution	N/A	4-Digit Resolution	N/A
One LSB	+1.0mV		0.125μA	
Full Scale (0110...0110	+9.999V		-1.24987mA	
All Bits OFF (1111...1111	Zero		Zero	

* To obtain values for other binary (CBI) ranges: 0 to +5V range, divide 0 to +10V range by 2; ±5V range, divide ±10V range by 2; ±2.5V range, divide ±10V range by 4.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

The DAC72 is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available on binary units. If 16-bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5VDC through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the DAC72, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ, the output will be in error by 1LSB. To understand what this means in terms of a system layout, the impedance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 6 inches of wire will produce a 1LSB error in the analog output voltage! Although the problems involved seem enormous, care in the installation planning can minimize the potential causes of error.

Figure 7 shows the connection diagram for a voltage output DAC72. Lead and contact resistances are represented by

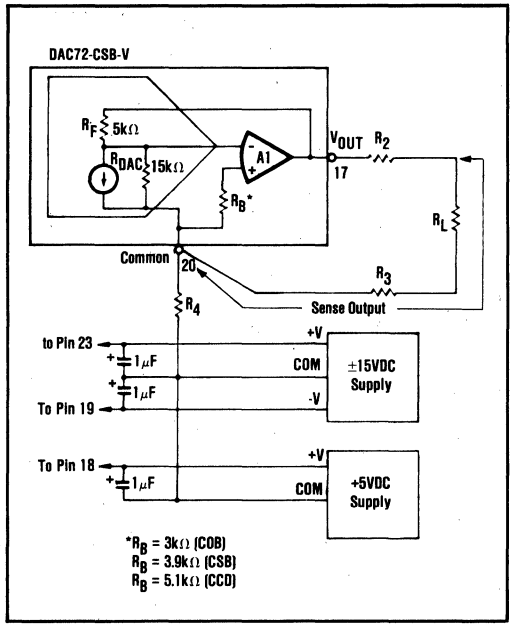


FIGURE 7. Output Circuit for Voltage Models.

R_1 through R_5. As long as the load resistance (R_L) is constant, R_2 simply introduces a gain error that can be removed during initial calibration. R_3 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable then R_2 should be less than 1LSB. For example, if $R_{L,min}$ is 5kΩ then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the DAC72 for optimum performance.

Figures 8 and 9 show two methods of connecting current model DAC72's with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A1 at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but it is independent of the value of R_L and can be eliminated during initial calibration. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain. If the output cannot be sensed at Common (pin 20), then the differential output circuit shown in Figure 9 is recommended. In this circuit the output voltage is sensed at the load common and not at the DAC common as in the previous curcuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible the circuit of Figure 9 can be reduced to the one shown in Figure 8 because $R_B = (R_7 + R_5) \parallel R_6$. In all three circuits the effect of R_4 is negligible.

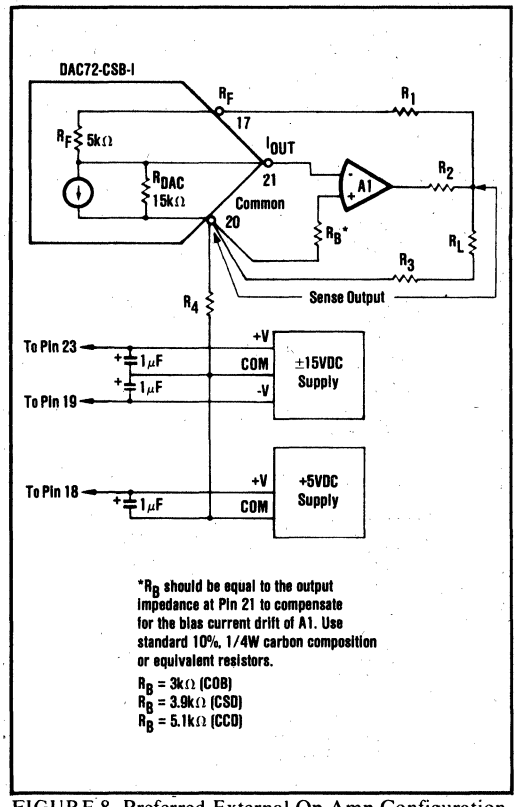


FIGURE 8. Preferred External Op Amp Configuration.

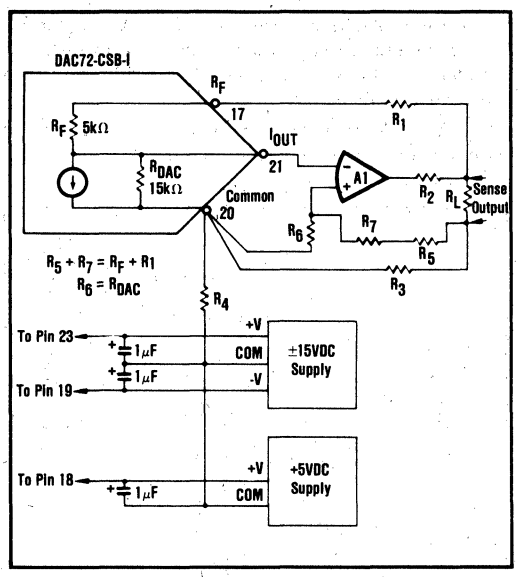


FIGURE 9. Differential Sensing Output Op Amp Configuration.

The DAC72 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit. The metal case of the DAC72 is internally connected to the common pin to further minimize pickup. The DAC72 is made of nickel plated steel which also provides some electromagnetic shielding.

NOTE: It is recommended that the digital input lines of the DAC72 be driven from inverters or buffers of TTL input registers to obtain specified accuracy.

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, R_L, with the current output model connect as shown in Figure 10, will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA[(15k\Omega \times R_L)/(15k\Omega + R_L)]$$

Where R_L max = 1.36kΩ

and V_{OUT} max = -2.5V

Add an external low T.C. (<10ppm/°C) resistor (R_L) as shown in Figure 11 to obtain a 0 to -2V full scale output voltage range for CCD input codes.

$$V_{OUT} = 1.25mA\ [(15.6k\Omega \times R_L)/(15.6k\Omega + R_L)]$$

Where R_L max = 1.79kΩ

and V_{OUT} max = -2.01V

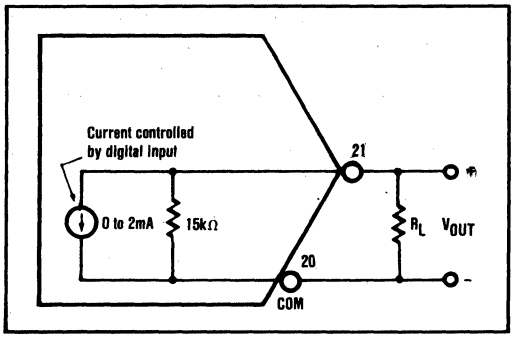


FIGURE 10. Equivalent Circuit DAC72-CSB-I Connected for Unipolar Voltage Output with Resistive Load.

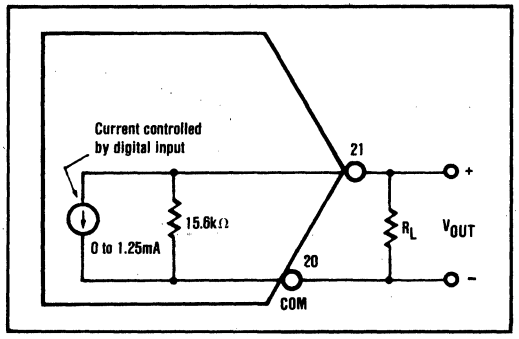


FIGURE 11. DAC72-CCD-I Connected for Voltage Output with Resistive Load.

DRIVING A RESISTIVE LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA\ [(4.44k\Omega \times R_L)/(4.44k\Omega + R_L)]$$

Where R_L max = 5.72kΩ
and V_{OUT} max = ±2.5V

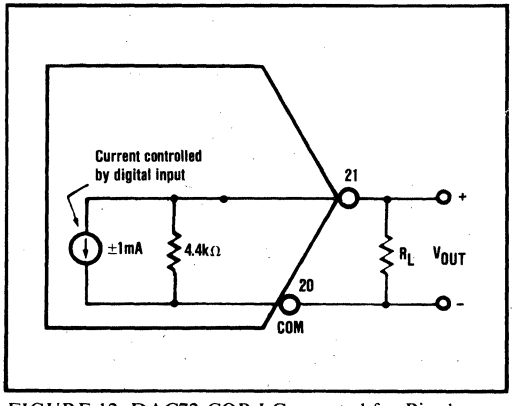


FIGURE 12. DAC72-COB-I Connected for Bipolar Output Voltage with Resistive Load.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DAC

The DAC72-(CSB, COB, CCD)-I are current output devices and will drive the summing junction of an op amp to produce an output voltage (see Figure 13). The op amp output voltage is:

$$V_{OUT} = -I_{OUT}\ R_F$$

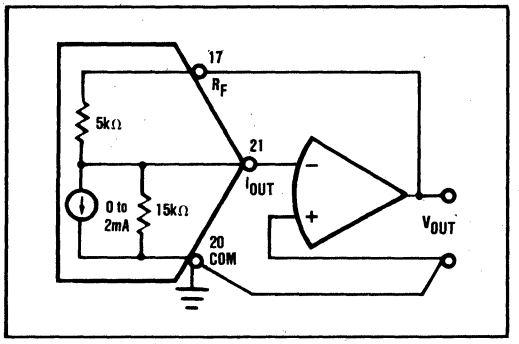


FIGURE 13. External Op Amp Using Internal Feedback Resistors.

Where I_{OUT} is the DAC72 output current and R_F is the feedback resistor. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

The DAC72 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±25ppm/°C. The resistors in the DAC72 are chosen for ratio tracking of ±1ppm/°C and not absolute TCR (which may be as high at ±25ppm/°C.)

An alternative method of scaling the output voltage of the DAC72 and preserving the low gain drift is shown in Figure 14.

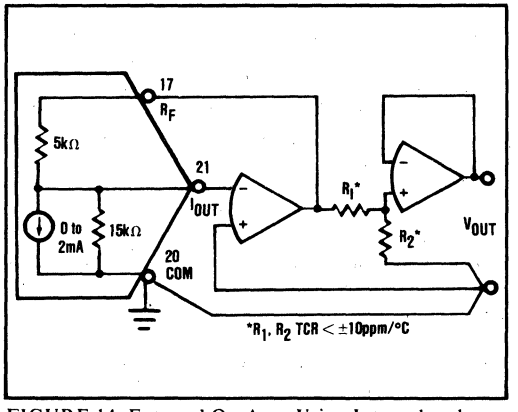


FIGURE 14. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

OUTPUTS LARGER THAN 20-VOLT RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges (see Figure 15). Use protection diodes when a high voltage op amp is used.

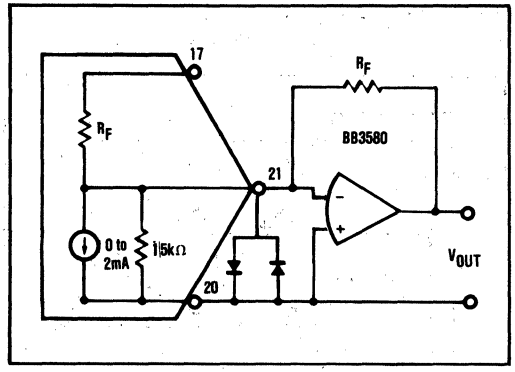


FIGURE 15. External Op Amp Using External Feedback Resistors.

COMPUTING TOTAL ACCURACY OVER TEMPERATURE

The accuracy drift with temperature of a DAC72 consists of three primary components: gain drift, unipolar or bipolar offset drift, and linearity drift. To obtain the worst-case accuracy drift, most users would assume that all drift errors are random and would simply add them algebraically. However, the worst-case accuracy drift for a DAC72 operating in the bipolar mode is about one-half of the algebraic sum of the individual drift errors.

To explain this fact, it is necessary to consider the unipolar and bipolar modes of operation separately. The following analysis is for the DAC72C although it applies to both models by simply substituting the proper temperature coefficients from the electrical specifications.

In the unipolar mode of operation, offset drift (±1ppm °C) is due primarily to voltage offset drift of the output op amp and, to a lesser extent, to the leakage current through the quad current switches. Gain drift consists of several components: 1) ±5ppm/°C due to ratio drift of current switch V_{BE} to the reference transistor, 2) ±10ppm/°C due to the zener reference and, 3) ±2ppm/°C linearity drift due to ratio drift of current weighting resistors and V_{BE} of the quad current switches. The sum of these three components, ±17ppm/°C, is the maximum gain drift.

Because the parameters described could all drift in the same direction, the worst-case accuracy drift in the unipolar mode is simply the sum of the components, or ±18ppm/°C.

In the bipolar mode the major portion of gain drift is due to the zener reference. The gain and offset drifts caused by reference drift are always in opposite directions. Therefore, the accuracy drift will be the difference rather than the sum of these drifts.

First, consider the effect of reference variations on offset drift. Figure 16 shows a simplified circuit diagram of a DAC72C-COB-V with all bits off. The current switch leakage current is negligible, so

$$V_{-FULL\ SCALE} = (-R_F / R_{BPR}) \cdot V_{REF}$$
$$= (-10k\Omega / 6.3k\Omega) \cdot 6.3V = -10V$$

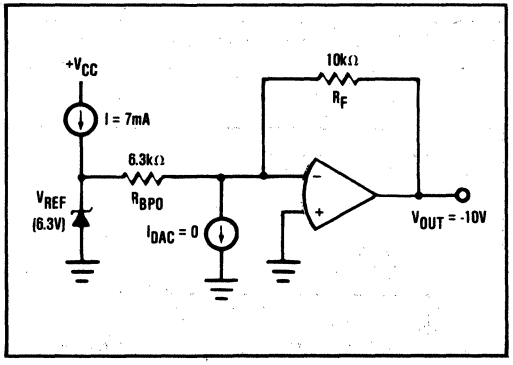


FIGURE 16. Simplified Diagram of DAC72C-COB-V with "All Bits Off" (±10V Range).

This equation shows that if V_{REF} increases, the output voltage will decrease and vice versa. If the V_{REF} drift is +10ppm °C, this is equivalent to (+10ppm °C) x (+6.3V) = +63V °C. This will result in a voltage drift at the amplifier output of

$$\Delta V_{-FS} / \Delta T = -(R_F / R_{BPO}) \cdot (\Delta V_{REF} / \Delta T)$$
$$= -(10k\Omega / 6.3k\Omega) \cdot (63\mu V / °C) = -100\mu V / °C.$$

Since the DAC72C-COB-V is operating in the ±10V range this is equivalent to (-100μV °C) ÷ (20V range) = -5ppm of FSR °C.

Now consider the effect of reference changes on gain drift. When all of the bits are turned on it can be shown that:

$$\Delta V_{+FULL\ SCALE} / \Delta T = +(R_F / R_{BPO}) \cdot (\Delta V_{REF} / \Delta T)$$
$$= +(10k\Omega / 6.3k\Omega) \cdot (63\mu V / °C) = +100\mu V / °C$$

and (+100μV °C) 20V Range = +5ppm °C of FSR.

This result indicates that the drift of the minus full scale voltage will be equal in magnitude to, and in the oppposite direction of, the drift of the plus full scale voltage and that zener reference variations have virtually no effect on the zero point (see Figure 17). This equation also indicates that the gain drift is equal to the V_{REF} drift in ppm °C, and the magnitude of the minus full scale drift and plus full scale drift is equal to one-half of the V_{REF} drift.

Using this relationship, the worst-case accuracy drift for a DAC72C-COB-V can be computed. The maximum TCR of the zener reference is ±10ppm °C. The gain drift due to the reference then is also ±10ppm °C. The full scale drift and bipolar offset drift are each half that amount or

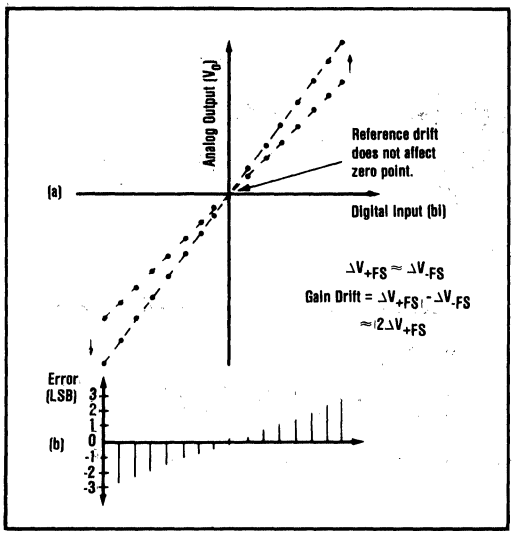


FIGURE 17. (a) Effect of a Positive Reference Drift on the Ideal D/A Transfer Function; (b) Error Distribution Due to Reference Voltage Drift in a DAC72.

±5ppm/°C. The maximum gain and offset drifts of the DAC72C, exclusive of the reference, are ±5 and ±3ppm/°C respectively. Adding this to the full scale drift due to the reference plus the linearity drift of ±2ppm/°C gives a worst-case total accuracy drift of ±15ppm/°C. (Random drifts, which these are can be in the same direction, so they add directly.) This is much less than the total drift obtained by simply adding the maximum gain, bipolar offset, and linearity drifts (±27ppm/°C). The maximum zero point drift is equal to one-half of the gain drift exclusive of the reference plus the offset drift exclusive of the reference, or ±5.5ppm of FSR/°C.

The DAC72C is specified over a 0°C to +70°C temperature range giving a maximum excursion from room temperature (+25°C) of 45°C. Assuming that gain and offset errors have been adjusted to zero at room temperature,

total worst-case accuracy error
= Linearity error + Accuracy drift x ΔT
= ±0.003% + ±15ppm °C (45°) (100)
= ±0.07%

total worst-case bipolar zero point error
Bipolar zero drift x ΔT
= ±5ppm of FSR% (45°C) (100)
= ±0.025%

ORDERING INFORMATION

MODEL	TEMP RANGES	PKG	INPUT CODE			
CURRENT MODELS						
DAC72C-COB-I	0°C to +70°C	Metal	Compl. Offset Binary			
DAC72C-CSB-I	0°C to +70°C	Metal	Compl Straight Binary			
DAC72C-CCD-I	0°C to +70°C	Metal	Compl. Coded Decimal			
DAC72-COB-I	-25°C to +85°C	Metal	Compl. Offset Binary			
DAC72-CSB-I	-25°C to +85°C	Metal	Compl. Straight Binary			
DAC72-CCD-I	-25°C to +85°C	Metal	Compl. Coded Decimal			
VOLTAGE MODELS						
DAC72C-COB-V	0°C to +70°C	Metal	Compl. Offset Binary			
DAC72C-CSB-V	0°C to +70°C	Metal	Compl. Straight Binary			
DAC72C-CCD-V	0°C to +70°C	Metal	Compl. Coded Decimal			
DAC72-COB-V	-25°C to +85°C	Metal	Compl. Offset Binary			
DAC72-CSB-V	-25°C to +85°C	Metal	Compl. Straight Binary			
DAC72-CCD-V	-25°C to +85°C	Metal	Compl. Coded Decimal			

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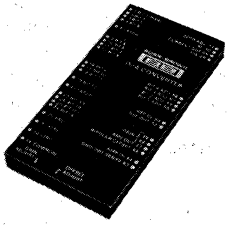
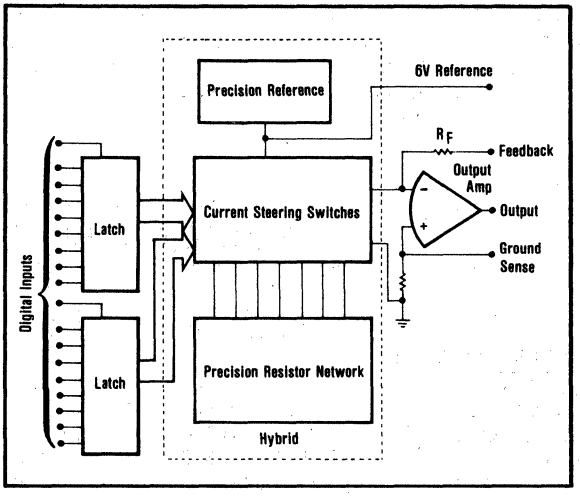


DAC73
DAC736

High Resolution 16-Bit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY
- LOW DRIFT
- CURRENT OR VOLTAGE OUTPUT
- INTERNAL GAIN, OFFSET, AND LINEARITY ADJUSTMENT
- LATCHED INPUTS (DAC73)
- LOW COST



DESCRIPTION

The DAC73 is a 16-bit modular high performance digital-to-analog converter in a 2" x 4" x 0.4" (50.8mm x 101.6mm x 10.2mm) package. The low drift and ultra-high linearity of the DAC73 provide voltage or current output signals that are accurate to ±0.00075% of full scale input range at 25°C ambient.

The critical components including the current steering switches, the temperature-compensated zener reference, and the precision laser-trimmed bit resistor network are contained in a single ceramic hybrid package.

The feedback and reference resistors are laid out for maximum stability with low current density and ±10ppm/°C maximum temperature coefficient with ±1ppm °C tracking. This insures very-low superposition errors and low temperature coefficient of gain.

The inputs are TTL-compatible CMOS and contain level triggered latches in an 8-bit format for microprocessor data bus compatibility. No external components are required to achieve full 16-bit accuracy. Gain and offset potentiometers are also included in the DAC73.

The DAC736 has electrical specifications identical to the DAC73, but it is pin-compatible with the AD1136. The input latches, bit adjust pins, ground sense pin, and internal offset adjust pot are not included.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC73J/DAC736J MIN	DAC73J/DAC736J TYP	DAC73J/DAC736J MAX	DAC73K/DAC736K MIN	DAC73K/DAC736K TYP	DAC73K/DAC736K MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution - CSB, COB			16			16	Bits
Logic Levels (TTL-Compatible CMOS)							
Logical "1" (at +1.0μA)	+3.5		+5.5	+3.5		+5.5	VDC
Logical "0" (at -0.5mA)	-0.5		+1.5	-0.5		+1.5	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error at 25°C			±0.0015			±0.00075	% of FSR(1)
Gain Error,(2) Voltage CSB		±0.005	±0.02		±0.005	±0.02	%
COB		±0.01	±0.05		±0.01	±0.05	%
Current		±0.05	±0.25		±0.05	±0.25	%
Offset Error,(2) Voltage, Unipolar			±0.8			±0.8	mV
Bipolar			±10			±10	mV
Current, Unipolar			±1			±1	μA
Bipolar			±5			±5	μA
Monotonicity Temp. Range 16 Bits for K, 15 Bits for J		±15			+5	+35	°C
DRIFT (Over specified temp. range)							
Total Drift (includes gain, offset, and linearity drift)							
CSB		±9.5	±24		±9.5	±24	ppm of FSR/°C
COB		±9	±22		±9	±22	ppm of FSR/°C
Total Error over Temp. Range(3)							
Voltage, Unipolar 0°C to 70°C		±0.043	±0.108		±0.043	±0.108	% of FSR
Bipolar		±0.040	±0.099		±0.040	±0.099	% of FSR
Voltage, Unipolar 15°C to 35°C		±0.010	±0.024		±0.010	±0.024	% of FSR
Bipolar		±0.009	±0.022		±0.009	±0.022	% of FSR
Gain (Exclusive of reference drift		±4	±10		±4	±10	ppm/°C
Offset (Exclusive of reference drift)							
Unipolar		±0.5	±2		±0.5	±2	ppm of FSR/°C
Bipolar		±2	±5		±2	±5	ppm of FSR/°C
Differential Linearity over Temperature		±1	±2		±1	±2	ppm of FSR/°C
Linearity Error over Temperature		±1	±2		±1	±2	ppm of FSR/°C
SETTLING TIME							
Voltage (to ±0.00075% of FSR)							
Output: 20V Step			50			50	μsec
1LSB Step(4)		6	10		6	10	μsec
Slew Rate		18			18		V/μsec
Current (to ±0.00075% of FSR)							
Output: 2mA Step		6			6		μsec
COB Switching Transient Magnitude		600			600		mV
COB Switching Transient Energy		0.45			0.45		V-μsec
OUTPUT							
ANALOG OUTPUT							
Voltage Output							
Ranges - CSB		0 to +5			0 to +5		V
		0 to +10			0 to +10		V
COB		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Output Current - Unipolar			+4			+4	mA
Bipolar			±2			±2	mA
Output Impedance (DC		0.03	0.05		0.03	0.05	Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
Current Output							
Ranges - CSB		0 to -2			0 to -2		mA
COB		±1			±1		mA
Output Impedance - Unipolar		15			15		kΩ
Bipolar		4.4			4.4		kΩ
Compliance		-1.5 to +10			-1.5 to +10		V
INTERNAL REFERENCE VOLTAGE	5.990	6.000	6.010	5.990	6.000	6.010	V
Maximum External Current(5)			+4			+4	mA
Temp. Coeff.		±4	±10		±4	±10	ppm/°C
OUTPUT NOISE							
Current, COB							
0.1Hz to 10Hz		1			1		nA, p-p
10Hz to 100kHz		4			4		nA, rms
Voltage, COB, ±10V Range							
0.1Hz to 10Hz		10			10		μV, p-p
10Hz to 100kHz		70			70		μV, rms

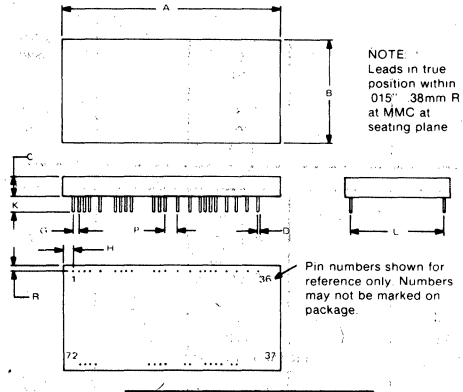
ELECTRICAL (CONT)

MODEL	DAC73J/DAC736J MIN	DAC73J/DAC736J TYP	DAC73J/DAC736J MAX	DAC73K/DAC736K MIN	DAC73K/DAC736K TYP	DAC73K/DAC736K MAX	UNITS
STABILITY, LONG TERM							
Gain (Exclusive of reference)		±30			±30		ppm/10³hr
Offset COB (Exclusive of reference)		±30			±30		ppm of FSR/10³hr
CSB		±5			±5		ppm of FSR/10³hr
Linearity		±0.25			±0.25		LSB/10³hr
Reference		±10			±10	±20	ppm/10³hr
POWER SUPPLY SENSITIVITY							
Unipolar Offset							
±15VDC		±0.0001			±0.0001		% of FSR/% Vs
+5VDC		±0.0001			±0.0001		% of FSR/% Vs
Bipolar Offset							
±15VDC		±0.0004			±0.0004		% of FSR/% Vs
+5VDC		±0.0001			±0.0001		% of FSR/% Vs
Gain							
±15VDC		±0.001			±0.001		% of FSR/% Vs
+5VDC		±0.0005			±0.0005		% of FSR/% Vs
POWER SUPPLY REQUIREMENTS							
Rated Voltage		±15, +5			±15, +5		VDC
Range	±14.5, +4.75	±15, +5	±15.5, +5.25	±14.5, +4.75	±15, +5	±15.5, +5.25	VDC
Supply Drain, ±15VDC no load		+35, -45	+50, -60		+35, -45	+50, -60	mA
+5VDC logic supply		9			9		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Storage	-55		100	-55		100	C

NOTES:
1. FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc.
2. Adjustable to zero with internal trim potentiometer, offset adjustment external on DAC736.
3. With gain and offset errors adjusted to zero at +25°C.
4. LSB is for 16-bit resolution.
5. Maximum with no degradation of specifications.

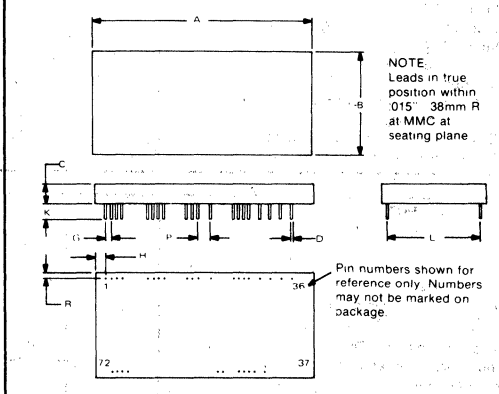
MECHANICAL

DAC73



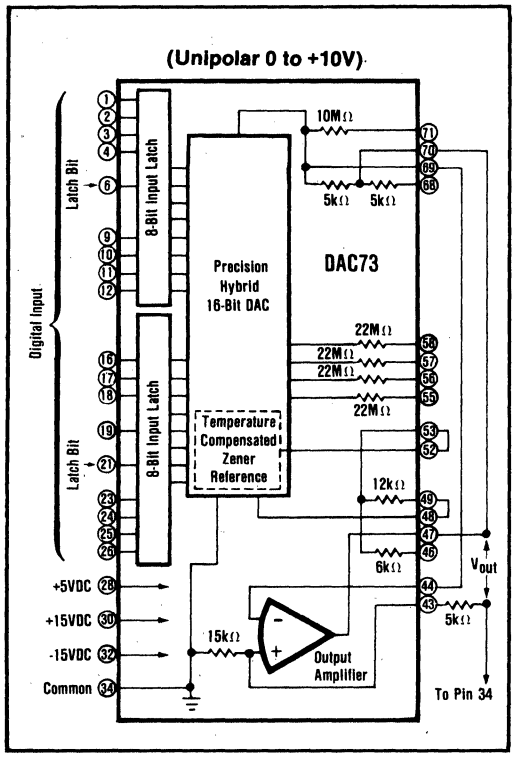
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	3.950	4.010	100.33	101.85
B	1.950	2.010	49.53	51.05
C	.350	.410	8.89	10.41
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.350	6.35	8.89
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	0.50	.150	1.27	3.81

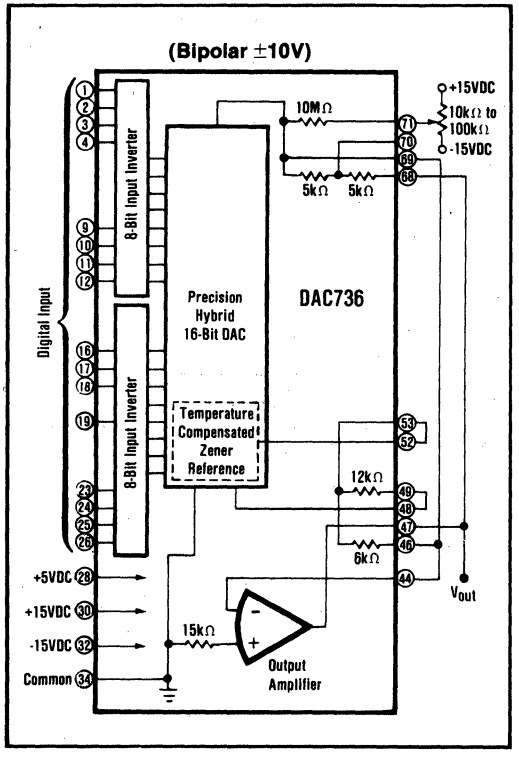
DAC736



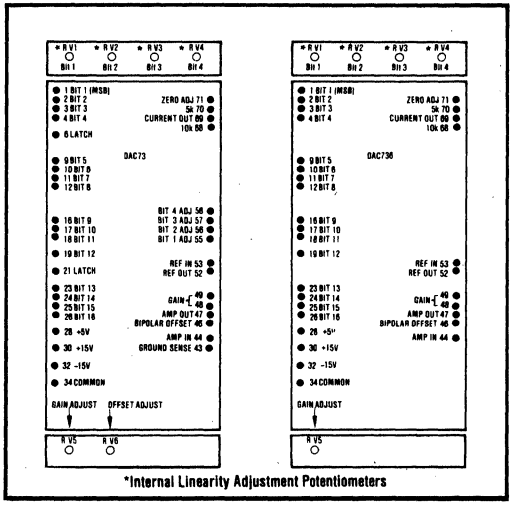
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	3.950	4.010	100.33	101.85
B	1.950	2.010	49.53	51.05
C	.350	.410	8.89	10.41
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.350	6.35	8.89
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	0.50	.150	1.27	3.81

CONNECTION DIAGRAMS





PIN ASSIGNMENTS



DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC73 736 accepts complementary digital input codes in CSB or COB format. The COB model may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

	DIGITAL INPUT CODES			
CSB, COB MODELS	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Comple-ment
All bits ON	0000...000	+Full Scale	+Full Scale	-1LSB
Mid Scale	0111...111	+1/2 Full Scale	Zero	-Full Scale
All Bits OFF	1111...111	Zero	-Full Scale	Zero
	1000...000	Mid Scale-1LSB	-1LSB	+Full Scale

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

INPUTS

Each bit input of the DAC73 consists of a buffered CMOS D type latch (see Figure 1). Bits 1 (MSB) through 8 are latched by a low level on pin 6. Bits 9 through 16 (LSB) are latched by a low level on pin 21. The latch inputs may be left open for transparent transfer of data.

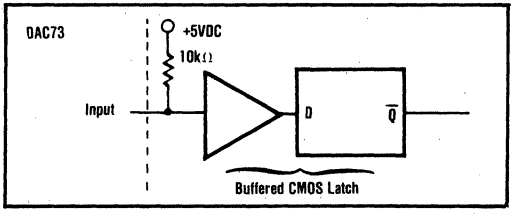


FIGURE 1. DAC73 Input.

The DAC736 inputs are CMOS inverters with 10kΩ pull-up resistors (see Figure 2).

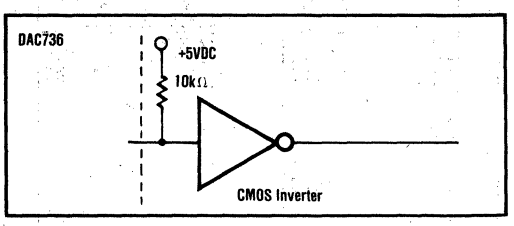


FIGURE 2. DAC736 Input.

The DAC73 and DAC736 can be driven directly by open collector or totem pole TTL logic.

ACCURACY

Linearity

This specification describes one of the truest measures of D A converter accuracy. As defined it means that the analog output will not vary by more than ±0.00075% max (CSB, COB) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C (see Figure 3).

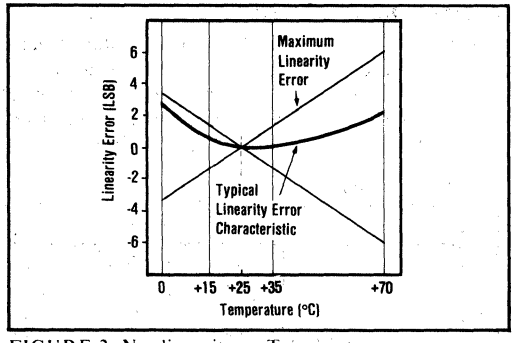


FIGURE 3. Nonlinearity vs Temperature.

Differential Linearity

Differential linearity error of a D A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1 2LSB means than the output voltage step sizes can be anywhere from 1 2LSB to 3 2LSB when the input changes from one adjacent input stage to the next.

Monotonicity

Monotonicity over a ±5°C range for the DAC73 and DAC736 is guaranteed when ambient linearity is calibrated. This insures that the analog output will increase or remain the same for increasing 16-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in LSB's per °C (see Figure 4). Gain Drift is established by: 1) testing the end point differences for each DAC73 model at +25°C and the appropriate specification temperature extremes; 2) calculating the gain error with respect to the +25°C value; and 3) dividing by the temperature change. This is expressed in ppm/°C.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range.

The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

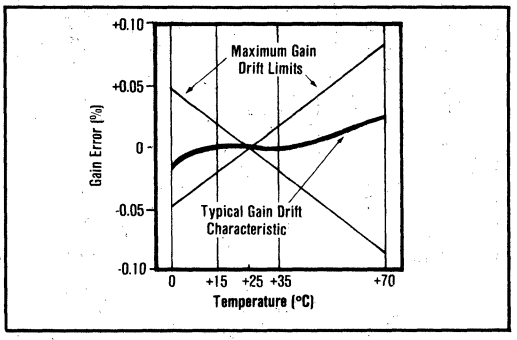


FIGURE 4. Gain Drift Error (%) vs Temperature.

SETTLING TIME

Settling time for each DAC73/736 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 5).

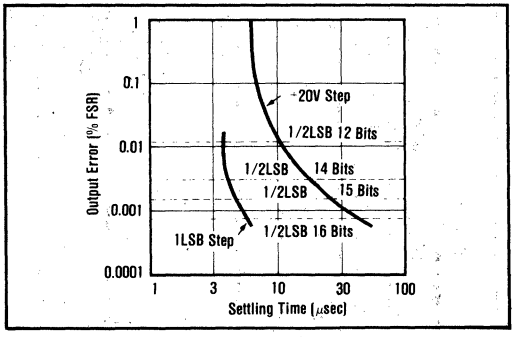


FIGURE 5. Full Scale Range Settling Time vs Accuracy.

Settling times are specified to ±0.00075% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output while maintaining

specified accuracy. The maximum compliance voltage is -1.5V to +10V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 6).

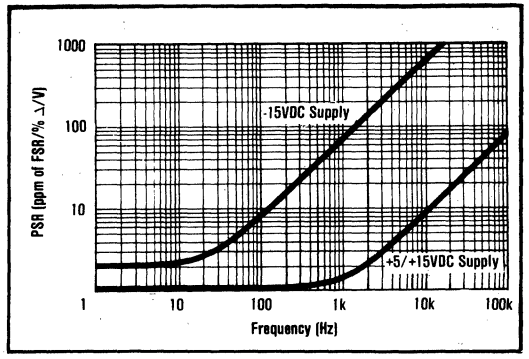


FIGURE 6. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All models are supplied with an internal +6V reference voltage supply. This reference voltage (pin 52) has a tolerance of ±0.05% and is connected internally for specified operation. The zener is selected for a Gain Drift of typically ±4ppm °C and is burned-in for a total of 48 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 4mA and constant load conditions.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection the DAC73 736 decoupling capacitors are included internally. Refer to Figure 13 for correct grounding connections.

OFFSET AND GAIN ADJUSTMENT

Before taking measurements or making adjustments, the DAC73 736 should be warmed up for at least 25 minutes. The DAC73 has internal gain and offset potentiometers that are connected to an internal regulated supply. In most applications no external adjustment will be required.

External offset and gain adjustment of the DAC736, or DAC73 if the application requires, maybe accomplished as shown in Figures 7 and 8. These external circuits could be used in an application using both unipolar and bipolar modes. Refer to Figures 9 and 10 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters. The internal potentiometers could be used to null the unipolar gain and offset, and the external null could be switched in by relays to null bipolar gain and offset. An alternate offset adjustment is shown on the DAC736 connection diagram.

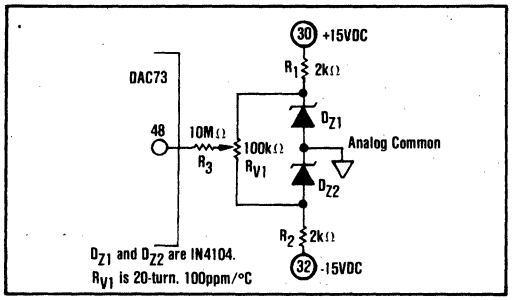


FIGURE 7. External Gain Adjustment.

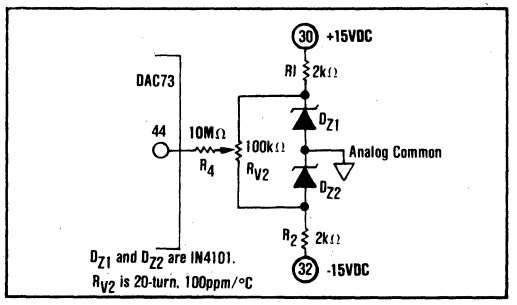


FIGURE 8. External Offset Adjustment.

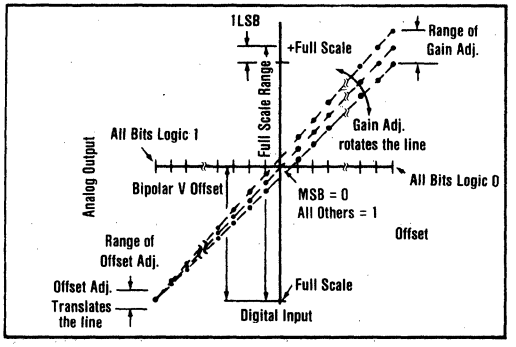


FIGURE 9. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

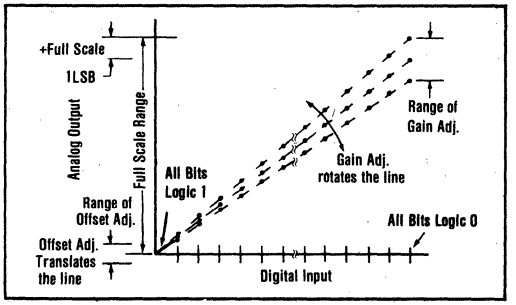


FIGURE 10. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors in the DAC73/736 provide a wide range of output voltage range connections. These internal resistors may be connected to provide three bipolar output voltage ranges of ±10V, ±5V, or ±2.5V or two unipolar voltage ranges of 0 to +5V or 0 to +10V. Since the internal scaling resistors are an integral part of the DAC73/736, gain and offset drift are minimized by their use. Connections for DAC73/736 are shown in Table II. Figure 11 is a connection diagram.

TABLE II. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 47 to	Connect Pin 46 to	Connect Pin 44 to	Connect Pin 68 to
±10V	COB	68	44	69	47
±5V	COB	70	44	69	NC
±2.5V	COB	70	44	69	69
0 to +10V	CSB	70	NC	69	NC
0 to +5V	CSB	70	NC	69	69

In all cases pins 52 and 53 and pins 48 and 49 should be shorted together with low resistance capacitance connections.

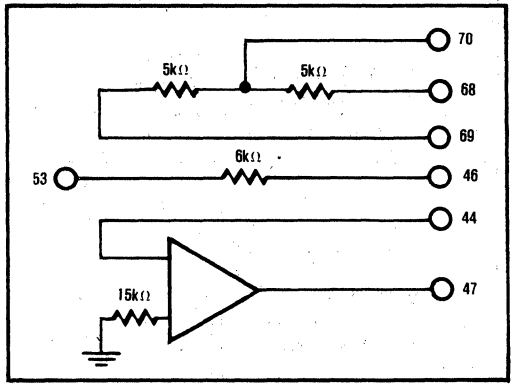


FIGURE 11. Output Amplifier Voltage Range Scaling Circuit.

LINEARITY ADJUSTMENT

Internal

If it becomes necessary to adjust the linearity of the DAC73 or DAC736 after an extended time period or for operation under temperature extremes, the 4MSB's may be user-adjusted. For optimum operation the unit should be calibrated in its operating environment. Calibration is performed by a differential linearity adjustment at the first four major carries. This method of calibration is possible since the DAC73 and DAC736 have almost no superposition error. The calibration procedure including gain, offset, and linearity adjustment is outlined in Table III. Steps 1 and 10 may be omitted for linearity adjustment only.

External (DAC73 only)

The linearity adjustment of the first 4MSB's of the DAC73 may be accomplished externally either with potentiometers or with D/A converters. Using a DAC to adjust linearity will allow computer controlled accuracy adjustments of the DAC thus giving the capability of maintaining 16-bit accuracy over all environmental variations. Gain and offset may also be adjusted in this manner.

Eight-bit bipolar voltage output DAC's can be used for all of the adjustments. Each circuit is shown in Figure 12.

INSTALLATION CONSIDERATIONS

To maintain the extremely-high accuracy of the DAC73 and DAC736 when installed in a system environment, careful attention must be paid to grounding and to connection resistances. Figures 13 and 14 are examples of correct connection configurations to yield maximum accuracy. The effects of various wiring and contact resistances R_1, R_2, R_3, and R_4 are reduced or eliminated as follows.

R_1 appears in series with the feedback resistance and therefore introduces only a gain error that can be nulled during calibration.

R_2 is inside the output amplifier feedback loop and its effect will be reduced by the loop gain.

In Figure 13 for the DAC736, R_3 is in series with the load

TABLE III. Calibration Procedure.

STEP	HEX INPUT CODE	ADJUST POTENTIOMETER(1)	DVM READING: UNIPOLAR MODE	DVM READING: ±10 VOLT BIPOLAR MODE	DESCRIPTION
1	FFFF	R_{V6}(2)	0.0V	-10.0000V	Null Offset
2	F000	N/A	V_4	V_4	Read Output Voltage
3	EFFF	R_{V4}	V_4 + 153μV	V_4 + 305μV	Adjust R_{V4} until DVM reads V_4 + 1LSB
4	E000	N/A	V_3	V_3	Read Output Voltage
5	DFFF	R_{V3}	V_3 + 153μV	V_3 + 305μV	Adjust R_{V3} until DVM reads V_3 + 1LSB
6	C000	N/A	V_2	V_2	Read Output Voltage
7	BFFF	R_{V2}	V_2 + 153μV	V_2 + 305μV	Adjust R_{V2} until DVM reads V_2 + 1LSB
8	8000	N/A	V_1	V_1	Read Output Voltage
9	7FFF	R_{V1}	V_1 + 153μV	V_1 + 305μV	Adjust R_{V1} until DVM reads V_1 + 1LSB
10	0000	R_{V5}	+9.999847V	+9.999695V	Adjust Gain

NOTES: 1. For potentiometer location see Pin Assignments. 2. External offset adjustment on DAC736.

resistor and will cause an error in the voltage across R_L. One-half LSB error would result at full load for $R_3 = 0.02\Omega$. Therefore, if possible, sense the output voltage to include R_3.

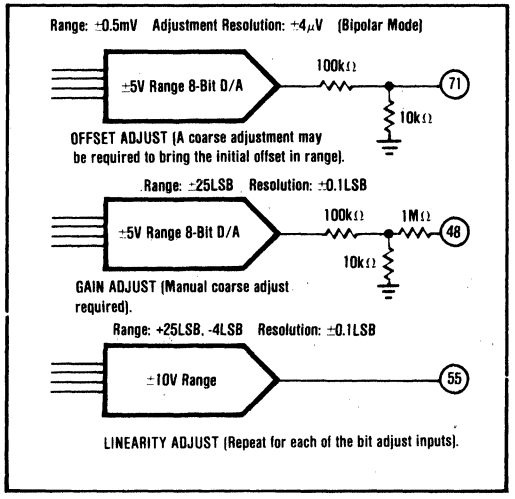


FIGURE 12. External Accuracy Adjustment.

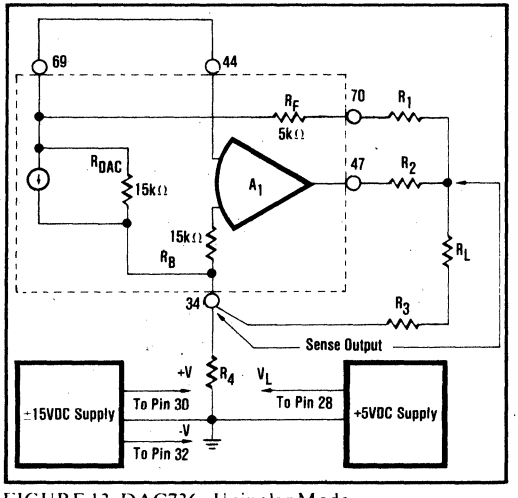


FIGURE 13. DAC736 - Unipolar Mode.

Figure 14 illustrates the optimum connection made possible by the ground sense pin on the DAC73. In the configuration shown $R'_F = R_F$ and $R'_B \parallel R_B = R_{DAC} \parallel R_{BPO}$. This causes any signal developed across R_3 to be rejected as a common-mode input, and R_3 will not affect the voltage across R_L. This configuration will also reject noise present on the system common.

R_4 is negligible in both circuits when ground connections are made as shown.

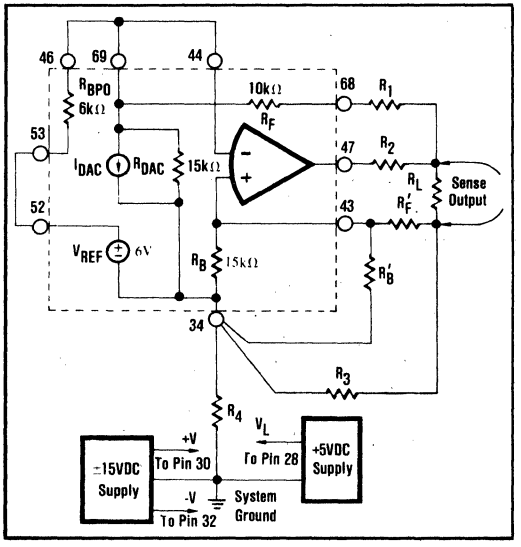


FIGURE 14. DAC73 - ±10V Bipolar Mode.

The DAC73/736 and the wiring to their connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field.

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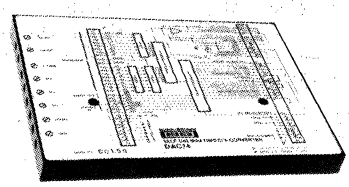


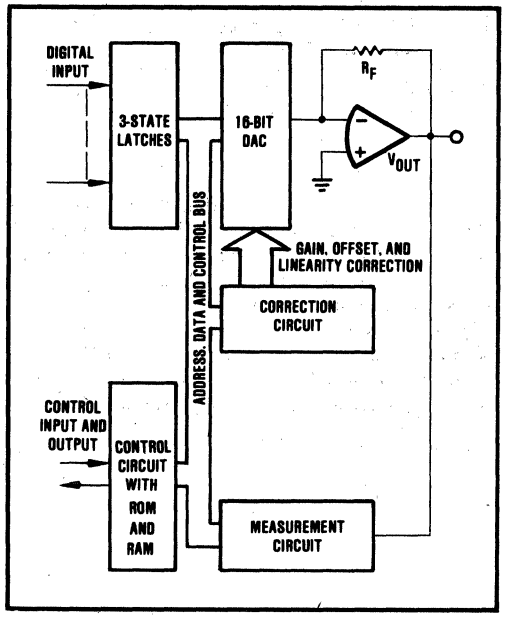
DAC74

Self-Calibrating High Resolution True 16-Bit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT RESOLUTION
- SELF-CALIBRATION MAINTAINS ACCURACY OF
  - ±1/2LSB NONLINEARITY
  - ±0.00035% GAIN ERROR
  - ±40μV OFFSET

  } +15°C TO +45°C
- UNIPOLAR OR BIPOLAR VOLTAGE OUTPUT
- DOUBLE BUFFERED FOR AN 8- OR 16-BIT BUS



DESCRIPTION

The DAC74 is a self-contained true 16-bit Digital-to-Analog converter designed for applications requiring high resolution and accuracy such as displays, frequency synthesizers, automated test equipment, analytical instruments, and high resolution controllers. Furthermore, in applications where equipment is inaccessible or frequent calibration is impractical the DAC74 is ideal because the self-calibration accuracy depends only on the long term stability of a heated zener reference diode.

Using self-calibration circuits, the DAC74 maintains typically ±1LSB total error over +15°C to +45°C! Compare this with other high resolution converters which can only maintain this accuracy over a ±2°C or ±3°C range. A patented microprocessor-controlled differential measurement technique is the key contributor to the DAC74's drift performance. This technique allows use of low cost hybrid and monolithic circuits to remove linearity, gain, and offset errors resulting from ambient temperature variations, component aging, and varying load conditions.

This product is covered by United States patents 4,222,107 and 4,272,760. Other patents pending may also apply upon the allowance and issuance of patents thereon. The product may also be covered in other countries by one or more international patents corresponding to the above identified U.S. patents.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SYSTEM DESCRIPTION

The DAC74 is a self-calibrating, 16-bit digital-to-analog converter in a 5" x 7" x 0.6" (127mm x 178mm x 15.2mm) package. This D/A converter provides either a unipolar or a bipolar voltage output that is linear to within ±1/2LSB of the Full Scale Range (FSR). The FSR in the unipolar mode is set by the internal +10V reference. The FSR in the bipolar mode is set by the difference between the +10V and the -10V references. With respect to the internal references, the offset and gain errors are also less than ±1/2LSB. The settling time to ±1/2LSB is typically 6μsec for a 1LSB step.

A microprocessor-controlled calibration circuit retrims the D/A converter to this accuracy in the face of drift over temperature and time. The absolute accuracy of the calibration is dependent upon the accuracy of the internal voltage references. The drift of the reference is typically ±0.5ppm/°C.

The linearity and accuracy of the DAC74 versus temperature is illustrated in Figures 1 and 2. The calibration was performed at 5°C intervals. It can be seen that the calibration greatly increases the useful temperature range of the D/A converter.

The DAC74 (see Figure 3) consists of (1) a 16-bit, latched input main D/A converter, which performs the digital-to-analog conversion, (2) a stable, temperature-compensated voltage reference, (3) an error-measuring circuit which compares the D/A converter output to known references, and (4) a microcomputer-based controller that stores the output of the error measuring circuit and calculates correction factors for offset, gain, and linearity. The controller stores these correction factors in RAM and these are used to adjust errors when an input data word selected by the user is presented at the input to the main D/A converter.

The critical components, including the current steering switches and the laser-trimmed resistor network, are contained in a single ceramic hybrid package for improved thermal tracking. The zener reference is maintained at a constant temperature to reduce drift due to ambient temperature fluctuations.

The DAC74 is housed in a steel package which provides excellent electromagnetic shielding. The package can be mounted from either side for socket mounting or for use of ribbon cable connectors.

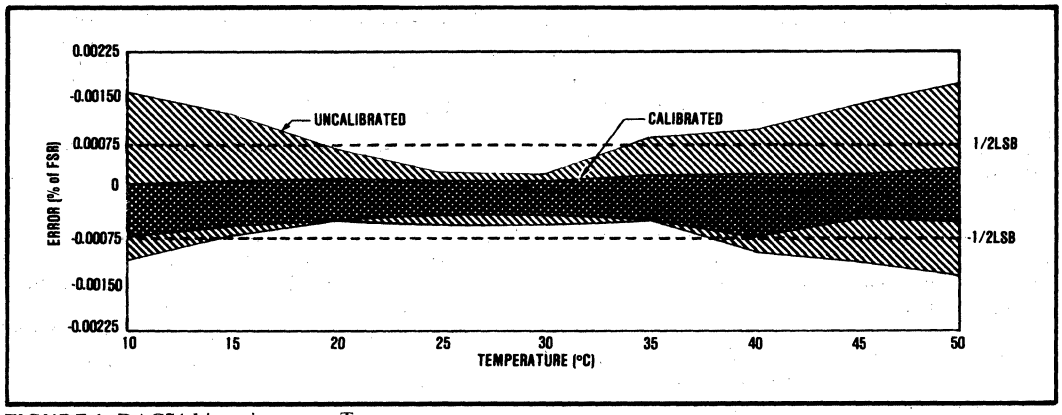


FIGURE 1. DAC74 Linearity versus Temperature.

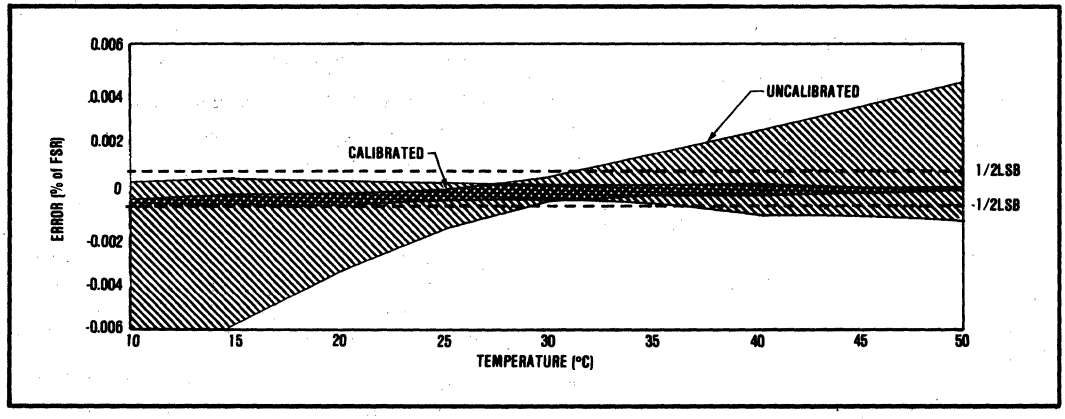


FIGURE 2. DAC74 Accuracy versus Temperature.

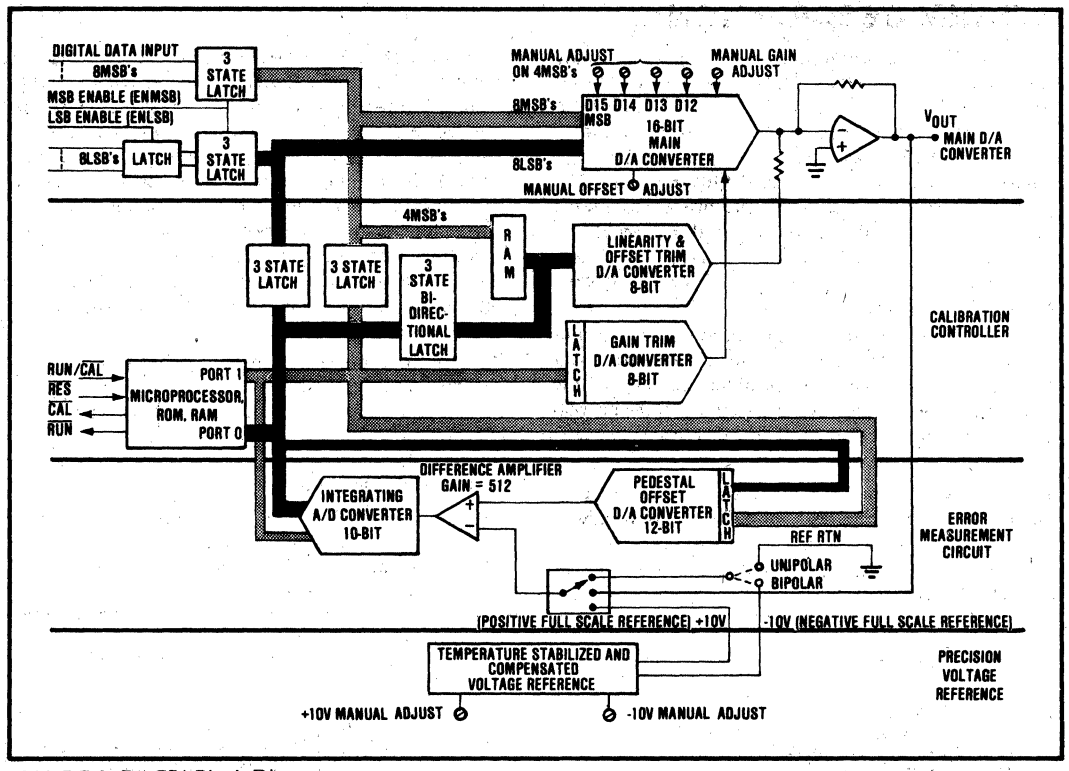


FIGURE 3. DAC74 Block Diagram.

A user initiates a calibration by applying a negative pulse to the reset input $\overline{RES}$ with the RUN $\overline{CAL}$ input held low. After an initial system check, the $\overline{CAL}$ status goes low and a 2.5 second calibration cycle is started. During calibration, the external inputs are disabled and the $\overline{RUN}$ status is high. The D/A converter returns to the RUN mode at the end of the calibration cycle. $\overline{CAL}$ remains low in the RUN mode if the calibration was successful. The $\overline{RUN}$ status output is low during normal D/A converter operation; in this state, the external digital data inputs are routed to the main D/A converter.

THE MAIN D/A CONVERTER

The 16 data inputs to the main D/A converter are buffered by two octal latches that are enabled by a high input to ENMSB. In addition, the 8LSB's are double buffered by a latch with an enable input labeled ENLSB. This arrangement allows transparent operation, a 16-bit interface, or an 8-bit interface. The data inputs are positive true. The MSB is labeled D15 and the LSB is labeled D0. Both latches transfer their inputs to the output when the enable is high. The input data is held in the latch when the enable is low.

Four potentiometers adjust the bit currents for the 4MSB's. Two more potentiometers allow the Offset and Gain to be adjusted manually. After a calibration period of 1 year, these potentiommeter adjustments may be required to trim the D/A converter to within the error range which can be trimmed by the self-calibration circuits. The procedure is given in the Manual Calibration section.

The output operational amplifier converts the 0 to 2mA current from the bit switches into a voltage output. A 5-wire output connection to the main D/A converter is described in the Installation section. All five wires MUST be installed to the load as indicated to obtain the full specified accuracy.

The output connection diagrams for 0 to +10V unipolar operation or ±10V bipolar operation are shown in the Installation section. Jumpers must be installed to configure the main D/A converter and the calibration circuits for each of these output configurations.

PRECISION VOLTAGE REFERENCES

The +10V and -10V references, shown in Figure 3, supply the voltage standards for calibrating the main D/A converter. The -10V reference is required only for bipolar operation. The ±10V references derive their outputs from a heated zener reference diode. In addition, both reference circuits are temperature compensated to cancel variations caused by drift in the other components of the reference. The accuracy of these references over temperature and time determine the accuracy of the D/A converter after calibration. These reference voltages are available for external use but the load must remain constant. Alternatively, external +10V and -10V references may be used with the DAC74.

ERROR MEASUREMENT CIRCUIT

The error measurement circuit of the DAC74 includes an analog switch, differential instrumentation amplifier, pedestal offset D/A converter, and an analog-to-digital converter. The circuit measures a sequence of voltage pairs. The error of the main D/A converter trim is derived from the differences in each pair of voltages. For instance, the Offset error is the difference between the minus full scale D/A converter output and the minus full scale reference (RTN for unipolar and -10V for bipolar). The Gain error is the difference between the plus full scale D/A converter output and the +10V reference less 1LSB.

The analog switch selects one of three sources as the input to the instrumentation amplifier. These sources are the main D/A converter output, minus full scale reference, and the plus full scale reference. The analog switch is controlled by the calibration controller.

The difference amplifier derives one of its inputs from a pedestal offset D/A converter which provides a voltage roughly comparable to the other input. The other input comes from the analog switch. During any pair of measurements, the pedestal offset D/A converter output remains the same. Since the gain of the instrumentation amplifier is 512, small differences (20μV) in the voltage pair are detected by the analog-to-digital converter connected to the output of the difference amplifier. The input to the pedestal offset D/A converter is set to the same value as that sent to the main D/A converter so that the high gain difference amplifier will stay within its linear range. The accuracy of the pedestal offset D/A converter does not affect the calibration accuracy.

The 10-bit analog-to-digital converter translates the output of the difference amplifier into a digital code for the microcomputer-based controller. Only the difference in the readings between a pair of measurements is used by the controller. The Gain and Offset of this 10-bit analog-to-digital converter are preset at the factory. The control signals to the A/D converter are generated by the controller during a calibration cycle.

CALIBRATION CONTROLLER

The Calibration Controller consists of a microcomputer which has three functions; (1) interpret commands from the control inputs and terminal interface, (2) conduct measurements by sending control signals to the error measurement subsystem, and (3) calculate the trims to be sent to the trim D/A converters. In the RUN mode, the microcomputer is idle; in fact, it can be turned off to reduce noise by asserting the MPUOFF control input high or leaving it open. The user may initiate a calibration cycle with a negative pulse to the $\overline{\text{RES}}$ control input with the MPUOFF and the RUN/$\overline{\text{CAL}}$ control inputs both low. At the end of the pulse to $\overline{\text{RES}}$, the $\overline{\text{RUN}}$ status output goes high indicating the main D/A converter is no longer under user control. As discussed in the Manual Calibration section, the $\overline{\text{CAL}}$ output goes low indicating that the calibration process is underway. At the end of the calibation, the $\overline{\text{RUN}}$ status will return low. If and only if the calibration succeeds, the $\overline{\text{CAL}}$ status will remain low.

The two status outputs $\overline{\text{RUN}}$ and $\overline{\text{CAL}}$ are open-collector TTL outputs (7406) which can drive an LED indicator directly. At the end of the calibration, the controller automatically returns to the RUN mode and control of the main D/A converter inputs is returned to the user.

The Offset is first adjusted with respect to the minus full scale reference. Then a sequence of four differential linearity measurements are conducted on the four MSB's of the D/A converter. Starting with the LSB of these four bits, each bit is trimmed to be linear with respect to all the lesser significant bits. After the linearity is established, a final gain correction is made with respect to the full scale reference. If the calibration fails, either a component has failed, or the internal drift of the system has exceeded the range of the trim circuit. If calibration under normal operating conditions fails, adjustments of eight potentiometers must be made to restore the D/A converter to its original accuracy. A detailed description of the calibration procedure is contained in the Manual Calibration section.

The trim circuits of the DAC74 consist of 16 RAM locations, Linearity/Offset trim D/A converter, and a Gain trim D/A converter. As shown in the block diagram, the RAM address inputs are taken from either a latch connected to the controller bus or from the four MSB's of the data input to the main D/A converter. In the RUN mode, the four inputs from the main D/A converter select one of 16 digital codes. The 8-bit code selected by the address inputs constitutes the sum of the corrections for the Offset error and the sum of the bit errors for those bits of the upper four which are logic ones. For instance, the RAM location 0 contains the digital code for just the Offset correction since none of the upper four bits are turned on. The RAM location 8 contains the digital code for the sum of the Offset correction and the correction for the MSB error. During calibration, the controller addresses the RAM. It first zeros the RAM and then adds the correction for the Offset error to all the RAM locations. Then the corrections for the bit errors are added to those locations which have that bit turned on. For instance, the correction for the MSB is added to all locations whose address starts with one (1XXX). The 8-bit digital code from the RAM is the input to the Offset/Linearity trim D/A converter. The output of the trim D/A converter makes a slight adjustment in the total current of the main D/A converter (one part in 2048). The maximum trim in the unipolar mode is ±2.441mV. With an 8-bit resolution trim D/A converter, the minimum possible trim is 1/8LSB or 0.019mV at the main D/A converter output.

A final Gain trim is made by sending a separate 8-bit trim word to the Gain D/A converter. The Gain error is the deviation of the full scale output from the full scale reference (+10V -1LSB). The maximum and minimum correction range in the full scale output are the same as the linearity/offset maximum and minimum, 2.441mV.

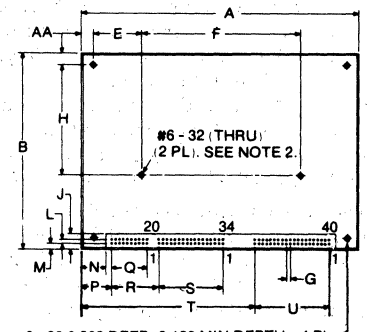
SPECIFICATIONS

ELECTRICAL

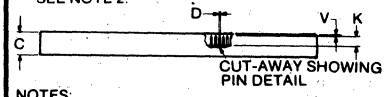
T_A = 25°C, rated power supplies and after 30 minute warm-up unless otherwise noted.

MODEL	DAC74			
	MIN	TYP	MAX	UNITS
DIGITAL INPUT				
Resolution			16	Bits
Voltage Levels				
Logic 1, V_{IH}	+2		+5.5	VDC
Logic 0, V_{IL}	0		+0.8	VDC
Current				
D0-D15, ENLSB, ENMSB (SN74LS373)				
I_{IH}, V_I = 2.7V			20	µA
I_{IL}, V_I = 0.4V			-0.4	mA
$\overline{RES}$, RUN/$\overline{CAL}$, UNIPOLAR $\overline{CAL}$				
I_{IH}, V_I = 2.4V			40	µA
I_{IL}, V_I = 0.4V			-1.6	mA
MPUOFF (inc. 10kΩ pullup)				
I_{IH}, V_I = 2.4V			-0.3	mA
I_{IL}, V_I = 0.4V			-2.1	mA
ANALOG OUTPUT				
Ranges, Unipolar		0 to +10		V
Bipolar		±10		V
Output Impedance (DC)		0.03	0.05	Ω
Short Circuit to Common (Duration)		Indefinite		
Load Current	±5			mA
Settling Time (to ±1/2LSB)				
20V Step		20	50	µsec
1LSB Step(1)			10	µsec
Slew Rate		18		V/µsec
Noise				
Voltage, Bipolar				
0.1Hz to 10Hz		10		µV, p-p
10Hz to 100Hz		70		µV, rms
DIGITAL OUTPUT				
Open Collector (SN7406) (with 10kΩ Pullup)				
Voltage Levels				
Logic 1	+2.4			V
Logic 0			+0.4	V
Current (with 10kΩ Pullup)				
$\overline{CAL}$, $\overline{RUN}$				
I_{OH}			1	mA
I_{OL}			-15	mA
TRANSFER CHARACTERISTICS AFTER SELF-CALIBRATION CYCLE				
Accuracy(2)				
Total Error				
Unipolar			±0.0015	% of FSR(3)
Bipolar			±0.0015	% of FSR
Linearity Error			±1/2	LSB
Gain, Error, Unipolar			±0.00035	% of output
Bipolar			±0.00035	% of output
Offset Error, Unipolar			±40	µV
Bipolar			±80	µV
Monotonicity after Calibration, 16 bits		Guaranteed		
DRIFT				
Total Error Drift (includes gain, offset and linearity drift(4))				
Unipolar		±4	±9	ppm of FSR/°C
Bipolar		±5	±11	ppm of FSR/°C
Total Error over Temp Range				
Voltage, Unipolar (0°C to 70°C)			±0.06	% of FSR
Bipolar			±0.06	% of FSR
Voltage, Unipolar (+15°C to +45°C)			±0.013	% of FSR
Bipolar			±0.013	% of FSR
Gain (exclusive of reference drift)		±2	±5	ppm/°C
Offset (exclusive of reference drift)				
Unipolar		±0.5	±1	ppm of FSR/°C
Bipolar		±2	±3	ppm of FSR/°C
Differential Linearity over Temperature		±1	±2	ppm of FSR/°C
Linearity Error over Temperature		±1	±2	ppm of FSR/°C
PRECISION 10V REFERENCES				
Voltage(5)	±9.9995	±10.00	±10.0005	V
Drift vs Temperature		±0.5	±1	ppm/°C
External Current(6)			±4	mA

MECHANICAL



#6 - 32 0.263 DEEP (0.188 MIN DEPTH) (4 PL) SEE NOTE 2.

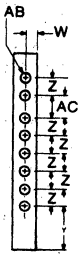


CUT-AWAY SHOWING PIN DETAIL

NOTES:
1. Leads in true position within 0.015" (0.38mm) R at MMC at seating plane.
2. Holes in true position within 0.015" (0.38mm) R at MMC.

CASE MATERIAL: Epoxy coated steel
LABEL: Metal foil
WEIGHT: 20oz. (257gm.) max.
PIN: Gold Flashed
Mating Connectors shipped with DAC74:

AMP86418-1	20 pin, P1 Test Interface
AMP1-86418-8	34 pin, P2 Digital
AMP86418-2	40 pin, P3 Analog

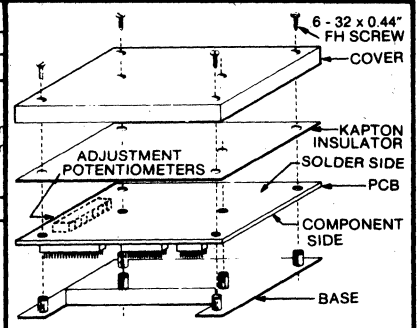


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	6.980	7.020	177.29	178.31
B	4.980	5.020	126.49	127.51
C	.550	.600	13.97	15.24
D	.022	.028	.56	.71
E	1.112 BASIC		28.24 BASIC	
F	4.150 BASIC		105.41 BASIC	
G	.100 BASIC		2.54 BASIC	
H	2.837 BASIC		71.98 BASIC	
J	.353	.373	8.97	9.47
K	.308	.328	7.82	8.33
L	.100 BASIC		2.54 BASIC	
M	.143	.183	3.63	4.65
N	.573	.613	14.55	15.57
P	.730	.770	18.54	19.56
Q	.900 BASIC		22.86 BASIC	
R	1.200 BASIC		30.48 BASIC	
S	1.600 BASIC		40.64 BASIC	
T	3.600 BASIC		91.44 BASIC	
U	1.900 BASIC		48.26 BASIC	
V	.020	.040	.51	1.02
W	.267	.287	6.78	7.29
Y	.831	.851	21.11	21.62
Z	.430	.470	10.92	11.94
AA	.293	.333	7.44	8.46
AB	.240	.260	6.10	6.60
AC	.565	.585	14.35	14.86

ELECTRICAL (CONT)

MODEL	DAC74			
	MIN	TYP	MAX	UNITS
STABILITY, LONG TERM				
Gain (exclusive of reference)		±30		ppm/10³ hr
Offset (exlusive of reference)				
Unipolar		±5		ppm of FSR/10³ hr
Bipolar		±30		ppm of FSR/10³ hr
Linearity		±0.25	±0.5	LSB/10³ hr
Precision 10V References		±20		ppm/10³ hr
POWER SUPPLY SENSITIVITY				
Unipolar Offset				
+15V and -15V Supplies		±0.0001		% of FSR/%Vs
+5V Supply		±0.0001		% of FSR/%Vs
Bipolar Offset				
+15V and -15V Supplies		±0.0004		% of FSR/%Vs
+5V Supply		±0.0001		% of FSR/%Vs
Gain				
+15V and -15V Supplies		±0.001		% of FSR/%Vs
+5V Supply		±0.0005		% of FSR/%Vs
POWER SUPPLY REQUIREMENTS				
Range	±14.5, +4.75	±15, +5	±15.5, +5.25	V V
Supply Drain, ±15VDC (not including output load)			200	mA
Current Surge, +15V Supply(7)			400	mA
+5VDC Supply			800	mA
TEMPERATURE RANGE				
Self-calibration Operation	+15		±45	°C
Drift Specification	0		+70	°C
Storage	-55		+100	°C
TIMING SPECIFICATIONS				
Control and Status Timing(8)				
t_{on}	50			msec
t_{RES}	14			µsec
t_{IN}			500	µsec
td_0		100		µsec
td_1		100		µsec
t_{RUN} (self-cal mode)		2.5	3	sec
t_{RUN} (service mode)		300	350	msec
Data Input Timing				
$t_{ENLSB, ENMSB}$ (pulse width t_w)	15			nsec
t_{su} (data input setup time)	20			nsec
t_h (data input hold time)	10			nsec

MECHANICAL (CONT)



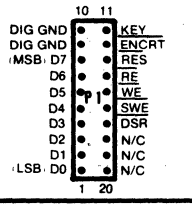
Screws holding the package together are covered by the top label (not shown). If the package must be opened, the top label must be peeled back at the corners. The package is mounted through inserts in the corners when the connectors are mounted pins-down or through the two holes in the center of the package when the connectors are mounted pins-up.

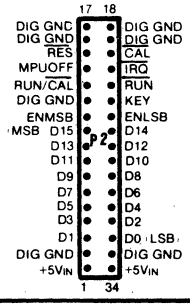
Manual calibration potentiometers are located on one end of the package. The potentiometers are accessed by peeling off the label on the edge of the package.

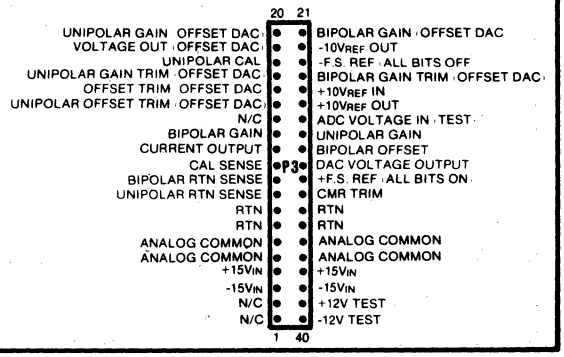
NOTES:
1. 1LSB at 16 bits = 0.00152% of FSR, = 15.2ppm of FSR, 152µV unipolar, 304µV bipolar.
2. Self-calibration can operate over +15°C to +45°C. DAC74 meets these specifications after the calibration cycle. These assume that the ±10V references have been adjusted to ±10.0000V ±10µV after 30-minute warm-up.
3. FSR means Full Scale Range and is 20V for bipolar and 10V for unipolar.
4. DAC74 will operate as a D/A converter over 0°C to +70°C. Self-calibration feature may be out of correctable range over a temperature range wider than +15°C to +45°C.
5. Manually adjustable to +10.00000 and -10.00000 after 30-minute warm-up.
6. Maximum with constant load for no degradation of specifications.
7. The heater current of the heated zener reference momentarily causes the initial power-up current of the +15V supply to approach 400mA. The +15V supply current then tapers to less than 200mA within 3 seconds.
8. See Operation section for timing diagrams.

PIN CONFIGURATION

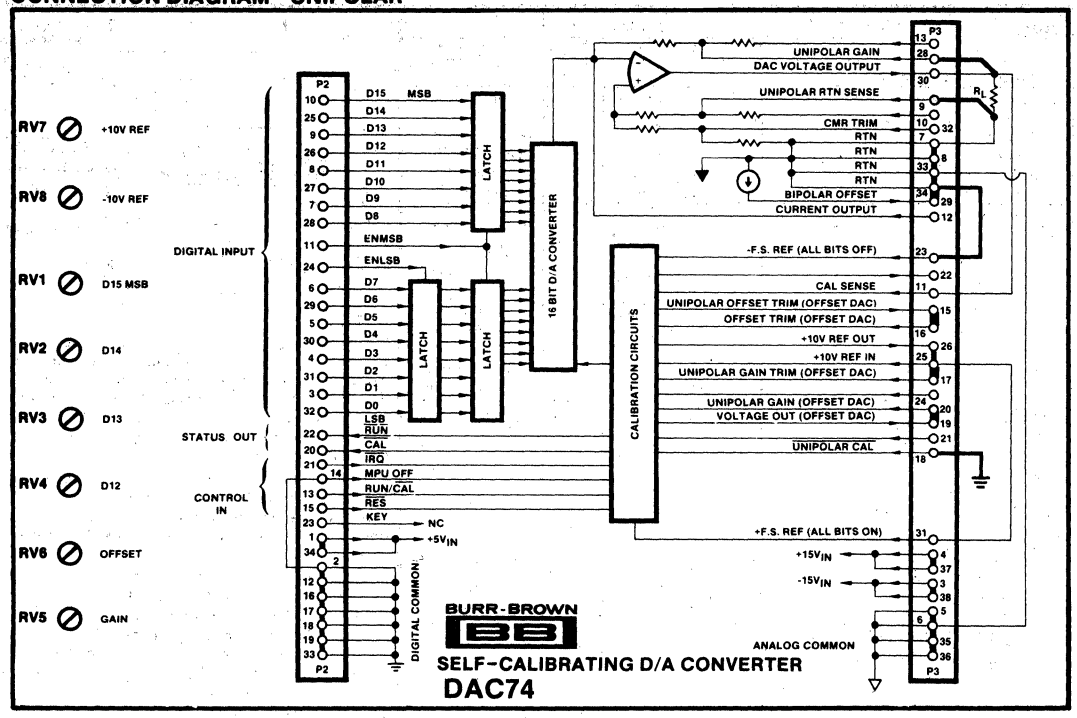
Connector P1 is a special service and test connector used by the factory. P2 is the Digital I/O connector containing the 16 input lines to the D/A converter, the control and status signals, and the +5V supply pins. Connector P3 contains all analog function pins for output, output sense, references, options, analog test points, and ±15V power supply input.
The DAC74 is delivered complete with mating connectors for printed circuit mounting.



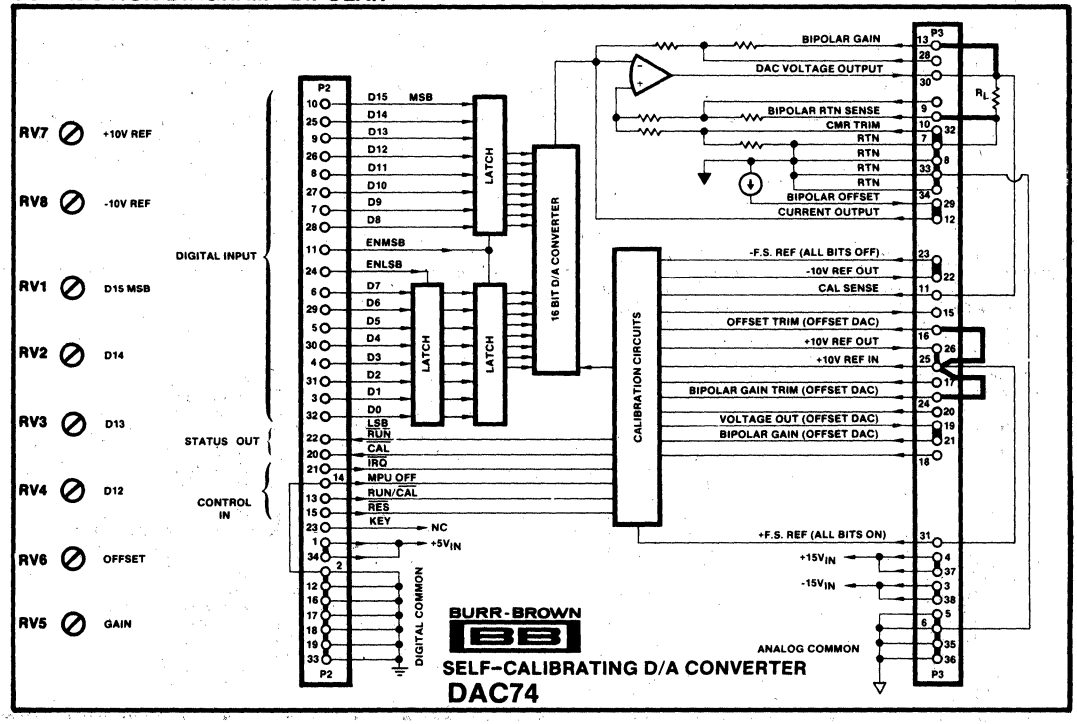




CONNECTION DIAGRAM - UNIPOLAR



CONNECTION DIAGRAM - BIPOLAR



DESCRIPTION OF PIN FUNCTIONS

CONNECTOR P1

Connector P1 is a test connector used by the factory. It is not described in this data sheet.

CONNECTOR P2 (Digital Signal Connector)

Pin No.	Designation	Function
1	$+5V_{IN}$	+5V supply input. Connected internally to pin 34.
2	DIGITAL COMMON	+5V supply return. Connected internally to pins 12, 16, 17, 18, 19, 33.
3 through 10	D1, D3, D5, D7, D9, D11, D13, D15	Data input to the Main D/A. D15 is the MSB. Logic 1 is a high input logic level.
11	ENMSB	Enable for the data input latches. Controls the MSB byte latch and the 2nd latch in the double-buffered LSB byte. Level triggered on high level.
12	DIGITAL COMMON	+5V supply return.
13	RUN/$\overline{CAL}$	Control input. Low input for SELF-CALIBRATION mode. High input for SERVICE, the manual calibration mode.
14	MPU OFF	Controls microprocessor oscillator. Low - ON, High - OFF. Must be low for 50msec before $\overline{RES}$ is asserted.
15	$\overline{RES}$	Control input. Resets the DAC74 controller and subsequently causes the RAM to be cleared and "calibration" or "service" to begin. Input is a logic 0 (low) pulse with 14μsec minimum width.
16, 17, 18, 19	DIGITAL COMMON	+5V supply return.
20	$\overline{CAL}$	Status Output. Informs the user if calibration failed. Logic low means calibration successful.
21	$\overline{IRQ}$	An internal microprocessor control input. Not used by user.
22	$\overline{RUN}$	Status Output. This is high during the time the calibration controller has control of the main D/A converter.
23	KEY	This pin may be used to key the module to protect against incorrect plug-in alignment.
24	ENLSB	Enable input for LSB byte latch. Level triggered on high level.
25 through 32	D14, D12, D10, D8, D6, D4, D2, D0	Data input to the main D/A. D0 is the LSB. Logic 1 is high logic level.
33	DIGITAL COMMON	+5V supply return.
34	$+5V_{IN}$	+5V supply input.

CONNECTOR P3 (Analog Connector)

Pin No.	Designation	Function
1, 2	NC	No connection.
3	$-15V_{IN}$	-15V supply input. Connected internally to pin 38.
4	$+15V_{IN}$	+15V supply input. Connected internally to pin 37.
5, 6	ANALOG COMMON	Return for ±15V supply. Connected internally to pins 35 and 36.
7, 8	RTN	Analog return for the analog output. Connected internally to pins 33 and 34.
9	UNIPOLAR RTN SENSE	Unipolar Return Sense. Analog load sense for unipolar output configuration.
10	BIPOLAR RTN SENSE	Bipolar Return Sense. Analog load sense for bipolar output configuration.
11	CAL SENSE	Calibration Sense. A connection to sense the D/A output at the load and provide an input to the error measurement circuit.
12	CURRENT OUTPUT	A connection to the current output of the bit switches. Used to connect Bipolar Offset, pin 29.
13	BIPOLAR GAIN	Connection to scale the output amplifier for bipolar output range (-10 to +10V) and to provide a sense input from the load.
14	NC	No connection.
15	UNIPOLAR OFFSET TRIM (OFFSET DAC)	Connects an internal trim network to pin 16 for unipolar operation. This network is factory set.
16	OFFSET TRIM (OFFSET DAC)	Offset trim input connection to the pedestal offset D/A converter.
17	UNIPOLAR GAIN TRIM (OFFSET DAC)	Gain trim input connection to the pedestal offset D/A converter for unipolar operation.
18	$\overline{UNIPOLAR\ CAL}$	A digital option line selecting the software routine calibrating the main D/A converter for the bipolar or unipolar configuration.
19	VOLTAGE OUT (OFFSET DAC)	Analog output of the pedestal offset D/A converter.
20	UNIPOLAR GAIN (OFFSET DAC)	Connects the pedestal offset D/A converter for 0 to +10V output range. Connect to pin 19.
21	BIPOLAR GAIN (OFFSET DAC)	Connects the pedestal offset D/A converter for -10V to +10V output range. Connect to pin 19.
22	$-10V_{REF}$ OUT	-10V precision reference output.
23	-F.S. REF (ALL BITS OFF)	Minus Full Scale input to analog switch of error measurement circuit. Connect to pins 7, 8, 33, 34 for unipolar. Connect to pin 22 for bipolar.
24	BIPOLAR GAIN	Gain trim input connection to the pedestal offset D/A converter for bipolar operation. Connect to pin 25.

25	$+10V_{REF}$ IN	Connection to provide precision +10V reference to the D/A converter circuits. Connect to pin 26.
26	$+10V_{REF}$ OUT	+10V precision reference output.
27	ADC VOLTAGE IN (TEST)	The analog output of the difference amplifier in the error measurement circuit.
28	UNIPOLAR GAIN	Connection to scale the output amplifier for unipolar output range (0 to +10V) and to provide a sense input from the load.
29	BIPOLAR OFFSET	Connects the bipolar offset current source to the current output of the main D/A converter to provide bipolar offset. Connect to pins 7, 8, 33, 34 for unipolar. Connect to pin 12 for bipolar.
30	DAC VOLTAGE OUTPUT	Analog voltage output of the main D/A converter.
31	+F.S. REF (ALL BITS ON)	Plus Full Scale input to analog switches of the error measurement circuit. Connect to pin 25.
32	CRM TRIM	Common-mode rejection trim for the output amplifier for bipolar operation only. Connect to pins 7, 8, 33, 34 for unipolar. Connect to pin 12 for bipolar.
33, 34	RTN	Analog return for the analog output. Also connected internally to pins 7 and 8.
35, 36	ANALOG COMMON	Return for ±15V supplies. Connected internally to pins 5 and 6.
37	$+15V_{IN}$	+15V supply input. Connected internally to pin 4.
38	$-15V_{IN}$	-15V supply input. Connected internally to pin 3.
39	+12V TEST	Test pin for internal +12VDC.
40	-12V TEST	Test pin for internal -12VDC.

INSTALLATION

The three connectors described in the previous section have three separate functions; analog interface, digital interface, and the terminal interface. The terminal interface is used only for factory test. Connection to a printed circuit board can be made using female printed-circuit-mounted connectors supplied with the DAC74. They should be positioned relative to the four internally-threaded mounting holes at the corners of the DAC74 as shown in Figure 4. Mount the DAC74 with four #6 external tooth lockwashers and four #6-32 screws using 0.156" diameter holes. Be sure to leave clearance for screwdriver adjustment of the trim potentiometers.

Alternatively, the DAC74 can be mounted on a chassis with the connectors facing upward using two #6 lockwashers and two #6-32 screws by means of the two internally-threaded holes near the center of the DAC74 as shown in Figure 4. In this orientation, connection to ribbon cable can be made with mass terminated, female, flat cable connectors (3M, 3421-0000, 3414-0000, 3417-0000). Individual wires may also be connected to the DAC74 in this orientation using female wire-applied connectors (AMP 1-87456-6, 3-87456-0, 3-87456-6 housings plus appropriate crimp snap-in pins). In either case, the jumpers for the unipolar or the bipolar configuration should be made right at the analog connector P2 as described in the following paragraph. The potential drops due to long jumpers cause a degradation in the accuracy of the calibration circuit.

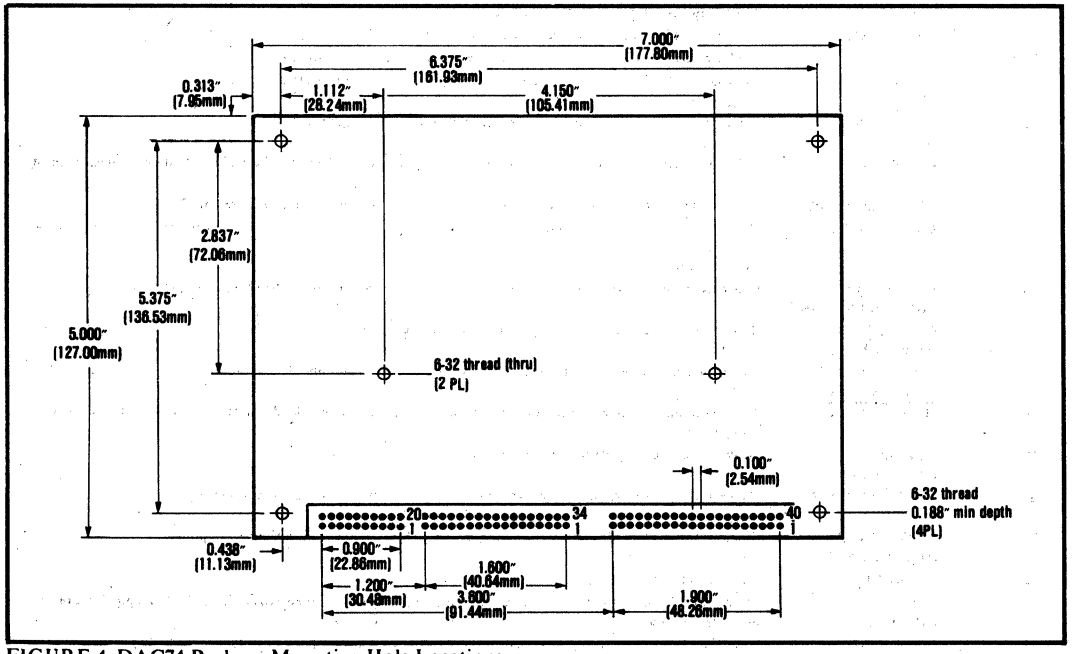


FIGURE 4. DAC74 Package Mounting Hole Locations.

POWER SUPPLY CONNECTIONS

A typical configuration is shown in Figure 5. Regardless of the local grounding, bring two separate return lines from the common near the power supplies to the DAC74. Connect one to Digital Common and the other to Analog Common. The load return line should be connected only to RTN (pins 7, 8, 33, 34) on P3 as shown in the unipolar and bipolar Connection Diagrams. Other connections to local grounds should be made with caution as they may cause ground loops which induce undesirable voltages at the common return points. The case is tied internally to Analog Common. Normally it should not be connected to any local grounds. Besides the power supply connections, other connections to the DAC74 should be limited to the digital inputs with a single digital current return and the 5-wire connection to the load. The external connections should be made so as to minimize the conduction paths to external noise sources. Internal bypass capacitors are included in the DAC74; no other bypass is needed nor recommended.

The power supply voltages may be sequenced on or off in any order provided that the power supply inputs have no transient voltages of polarity opposite to the normal DC input with respect to Analog or Digital Common.

The power supply requirements are listed below. During power-up, an initial surge of 400mA is required by the +15V supply input.

Input Voltage	+5V	+15V	-15V
Current, max	800mA	200mA	200mA
typ	500mA	150mA	150mA

Precautions

1. Provide all three grounds before applying voltage to either the power supply inputs or the signal inputs.
2. Avoid static discharge during handling and installation. Store the DAC74 in a conductive package.
3. Use short pairs of wire close together to minimize electromagnetic pickup.

In very noisy environments, separate floating supplies may be needed to power the DAC74. These supplies and their common returns should be connected only to the DAC74. Some experimentation with extra shielding and alternative return configurations may be necessary in extreme circumstances.

OUTPUT CONNECTION

The output connection for unipolar and bipolar operation are shown in the Connection Diagrams. For either unipolar or bipolar, it is very important to provide both a current-carrying wire and a sense wire to both sides of the load in order to minimize the errors caused by induced potentials and losses in the wiring to the load. The fifth wire, CAL SENSE, returns the output voltage at the load to the error measurement circuit. In a noisy environment these wires should be enclosed in a shield that is connected only to the RTN pins of the DAC74. The return line from the load to the RTN pin of the DAC74 must be separate from other grounds in order to avoid potential drops due to shared current paths. The resistance of this path must be low so that the voltage drop is less than 20μV. For example, at 5mA one foot of 16-guage copper wire (4Ω/1000ft.) produces a 20μV drop.

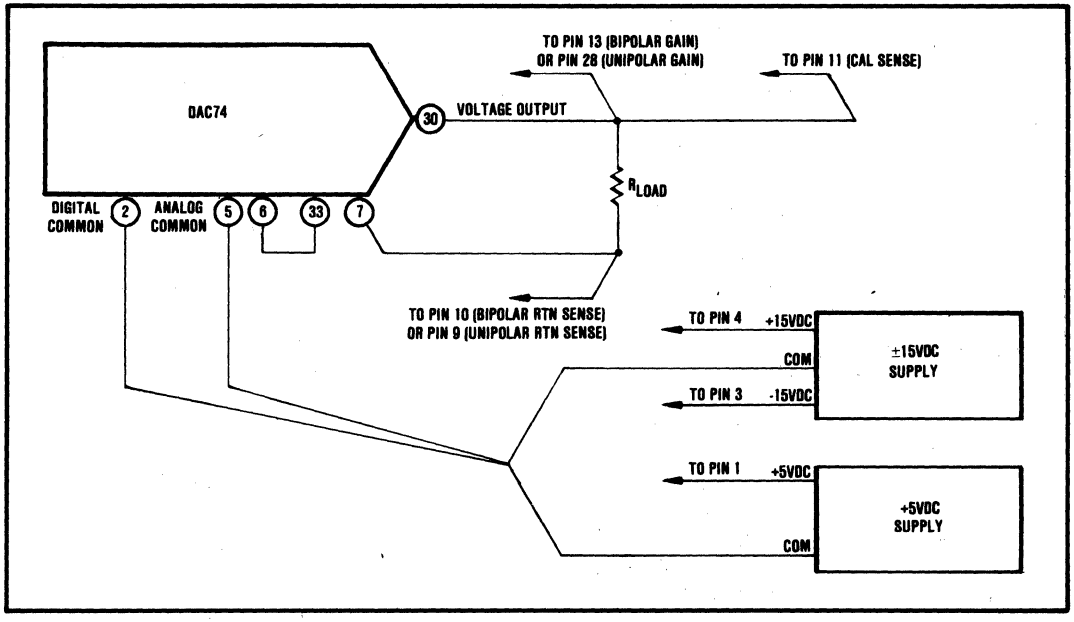


FIGURE 5. Power Supply and Common Connections.

Unipolar Connection. The output connections and jumpers are listed below. The pin numbers refer to the analog connector P3. The first five connections constitute the 5-wire connection to the load.

Connection	Purpose
30 to load (top)	DAC VOLTAGE OUTPUT Output connection to the load.
28 to load (top)	UNIPOLAR GAIN Output sense to the inverting input of the output amplifier. Sets unipolar range.
7 to load (bottom)	RTN Current return from the load. This return impedance must be low - equivalent of 16-gauge wire.
9 to load (bottom)	UNIPOLAR RETURN SENSE Return sense to the noninverting input of the output amplifier.
11 to load (top)	CAL SENSE Input to the error measurement circuit from the load.
33 to 6	RTN TO ANALOG COMMON Connect common returns. This jumper is essential to prevent damage to the internal reference.
23 to 34	-F.S. REF (ALL BITS OFF) Set minus full scale to 0 volts. Keep as short as possible.
29 to 34	BIPOLAR OFFSET TO RTN Maintain the same current drain on the +10 volt reference as bipolar connection.
26 to 25	+10V REF OUT TO +10V REF IN Keep as short as possible.
15 to 16	UNIPOLAR OFFSET TRIM TO OFFSET TRIM Connect offset trim to offset adjust input of the pedestal offset D A converter.
17 to 25	UNIPOLAR GAIN TRIM (OFFSET DAC) to +10 VOLT REF Connect the full scale gain reference of pedestal offset D A converter.
19 to 20	VOLTAGE OUT (OFFSET DAC) output to UNIPOLAR GAIN (OFFSET DAC) Return sense to inverting input of the pedestal offset D A converter.
18 to digital common	UNIPOLAR CAL to DIGITAL COMMON Set software to unipolar mode.
31 to 25	+F.S. REF to +10V REF IN.

Bipolar Connection. The output connections and jumpers for bipolar operation are listed below. The pin numbers refer to the analog connector P3. The first five connections constitute the 5-wire connection to the load.

Connection	Purpose
30 to load (top)	DAC VOLTAGE OUTPUT Output connection to the load.
13 to load (top)	BIPOLAR GAIN Sense to the inverting input of the output amplifier. Sets bipolar range.
7 to load (bottom)	RTN Current return from the load. This return impedance must be low - equivalent of 1 foot 16-guage wire for 5mA output.
10 to load (bottom)	BIPOLAR RETURN SENSE Return sense to the noninverting input of the output amplifier.
11 to load (top)	CAL SENSE Input to the error measuring circuit from the load.
32 to 7	CMR to RTN Match the equivalent impedance to RTN for both inputs of output amplifier for the bipolar configuration.
7, 8, 33, 34	RTN Tied together internally.
33 to 6	RTN to ANALOG COMMON Connect common returns. This jumper is essential to prevent damage to the internal references

Connection	Purpose
23 to 22	-F.S. REF (ALL BITS OFF) to -10V REF OUT Set minus Full Scale to -10 volts. Keep as short as possible.
29 to 12	BIPOLAR OFFSET to CURRENT OUTPUT Bipolar offset for output amplifier.
26 to 25	+10V REF OUT to +10V REF IN Keep as short as possible.
16 to 25	OFFSET TRIM (OFFSET DAC) to +10V REFERENCE IN Connect bipolar offset of the pedestal offset D/A converter to +10V REF.
24 to 25	BIPOLAR GAIN TRIM (OFFSET DAC) to +10V REF Connect the Full Scale gain reference of the pedestal offset D/A converter.
19 to 21	VOLTAGE OUTPUT (OFFSET DAC) to BIPOLAR GAIN (OFFSET DAC) Return sense to inverting input of the pedestal offset D/A converter.
31 to 25	+F.S. REF to +10V REF IN.

Internally Connected Pins. The following pins are connected internally:

Function	Pin No.
DIGITAL COMMON	2, 12, 16, 17, 18, 19, 33
$+5V_{IN}$	1, 34
ANALOG COMMON	5, 6, 35, 36
$+15V_{IN}$	4, 37
$-15V_{IN}$	3, 38
RTN	7, 8, 33, 34

DIGITAL INPUTS

Data inputs D0 - D15 and enable inputs, ENMSB and ENLSB, are low power Schottky (74LS373). Control inputs $\overline{RES}$, RUN/$\overline{CAL}$ and $\overline{UNIPOLAR\ CAL}$ are standard TTL inputs. MPUOFF is a standard TTL input with a 10kΩ pullup resistor connected to +5V volts.

Timing specifications on the digital inputs are listed in the Specifications table and discussed in the Operation section.

OPERATION

DAC74 data inputs, control signals, and status lines are shown in Figure 6. MPUOFF will usually be tied to DIGITAL COMMON permitting the internal crystal ocsillator to run continuously. However, one may wish to control the oscillator to remove all possible sources of noise during D/A converter operation. MPUOFF must be asserted low 50msec before the $\overline{RES}$ pulse is asserted.

The $\overline{RES}$ line resets the calibration controller and starts controller operation when it returns high after being asserted low for at least 14μsec.

RUN/$\overline{CAL}$ is a mode control line. When high, RUN/$\overline{CAL}$ enables the controller to set up the SERVICE mode. In this mode, the user performs a coarse manual adjustment of the D/A converter. When RUN/$\overline{CAL}$ is low, the controller is informed to set up the SELF-CALIBRATION mode, the normal mode of operation.

Data input latches are level-triggered by ENSMB and ENLSB. These are used to strobe-in data from an 8-bit bus with D0 through D7 connected to D8 through D15 respectively. For 16-bit bus operation ENLSB can be permanently connected to +5V. Since all three latches are octal transparent latches (74LS373), their inputs may be transferred directly to their outputs by setting their respective enable inputs high. The table below indicates four common interfaces. A high input refers to a logic 1 input (2V to 3.5V) and a low input refers to a logic 0 input (0V to 0.8V).

Mode	ENMSB	ENLSB	Description
Transparent	High	High	Inputs are transferred directly to the MAIN D/A converter.
16-bit interface	Positive Pulse	High	All 16 bits are latched at the end of the ENMSB pulse.
8-bit interface	Low	Positive Pulse	Capture 8LSB's from the data bus in low byte buffer.
8-bit interface	Positive Pulse		Transfer 8MSB's from the data bus and transfer latched 8LSB's to the MAIN D/A converer at the end of the pulse.

The three-state output in the second rank of latches is disabled by $\overline{RUN}$, a status output signal, during the time the calibration controller has control of the main D/A converter.

INITIAL SETUP

It is necessary to trim the +10V and -10V reference as close to 10V as possible using the potentiometers located at the edge of the module. The procedure is described in Manual Calibration section.

It should not be necessary to manually adjust OFFSET, GAIN, and LINEARITY on units received from the factory. However, after a year or more of operation it may be necessary to adjust these parameters to within the range which can be trimmed by the self-calibration circuits. The manual adjustment procedure is described in the Manual Calibration section. It is important that either the load be connected or that a dummy load be switched in during calibration or adjustment.

Self-Calibration Mode

After power-up, a 1/2-hour warm-up period must be allowed. This permits the heated zener reference and other critical circuits to stabilize.

The next step is to initiate the SELF-CALIBRATION routine. Self-calibration is initiated by providing a pulse (low, 14μsec min) from the host equipment to the $\overline{\text{RES}}$ line. Self-calibration typically takes 2-1/2 seconds. $\overline{\text{CAL}}$ and $\overline{\text{RUN}}$ inform the user on the internal status of the calibration controller. The operation of these is best explained by a timing diagram, Figure 7.

Upon application of the reset pulse, $\overline{\text{CAL}}$ goes (or remains) low and goes high about 100μsec after $\overline{\text{RES}}$ is returned high. $\overline{\text{CAL}}$ remains high for 500μsec maximum. If it remains high, self-calibration has failed. If it goes low, self-calibration will be successful. The fact that calibration has failed means that either a noise transient has interferred with system operation or that the maximum correction factors have been used and that the main D/A converter connot be corrected to within specification. However, the converter will still operate. It will be necessary to perform manual adjustments described in the Manual Calibration section.

$\overline{\text{RUN}}$ goes high about 100μsec after the $\overline{\text{RES}}$ pulse returns high and remains high until all calibration controller operations are complete and control of the main D/A converter is returned to the digital data inputs. It is important to be aware of two facts during self-calibration: (1) the main D/A converter is being exercised, its output is moving and changing the voltage on the load; and (2) the three-state output enable of the main D/A converter input latches is held high by $\overline{\text{RUN}}$ thereby disconnecting the data inputs from the main D/A converter.

Service Mode

Before one can manually adjust the GAIN, OFFSET and LINEARITY of the DAC74, it must be put in a mode called the SERVICE mode. This is accomplished by switching RUN/$\overline{\text{CAL}}$ high and asserting a pulse on the $\overline{\text{RES}}$ line. The result of going into this mode is that all corrections in the RAM are set to zero before control is returned to the user data input lines.

The timing is illustrated in Figure 7. $\overline{\text{CAL}}$ does not return low as it did in the SELF-CALIBRATION mode but remains high. $\overline{\text{RUN}}$ returns low indicating that control has been returned to the data inputs. $\overline{\text{RUN}}$ time is about 300msec. Manual calibration may proceed as described in the Manual Calibration section.

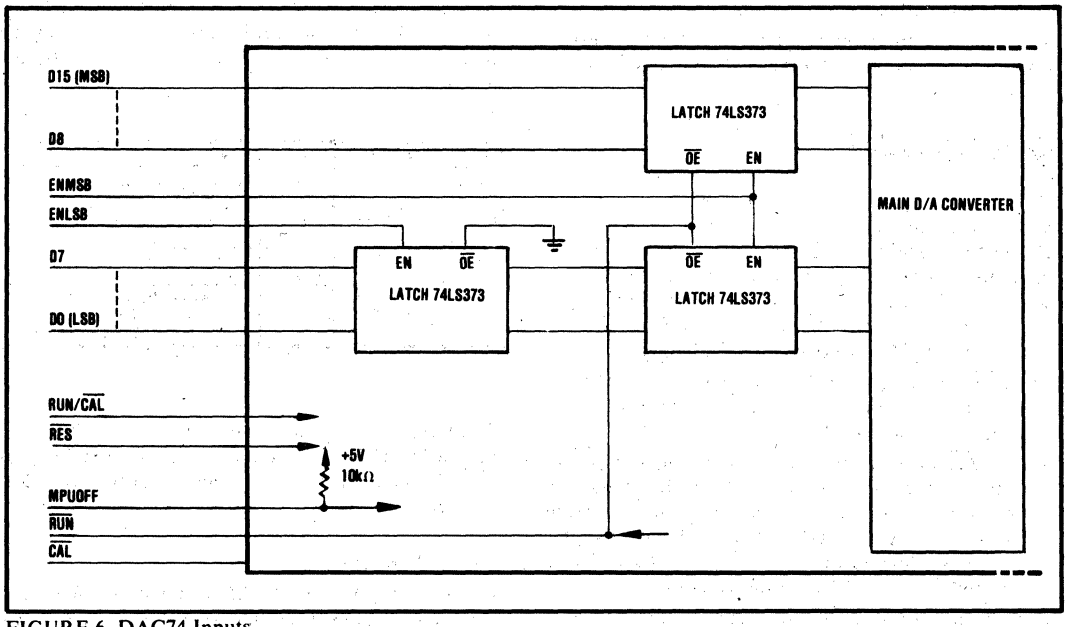


FIGURE 6. DAC74 Inputs.

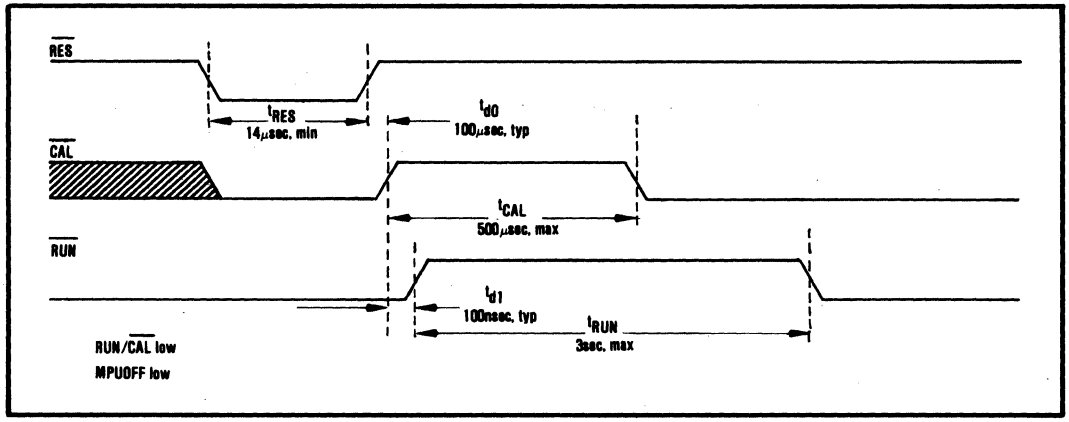


FIGURE 7. Self-Calibration Mode Timing.

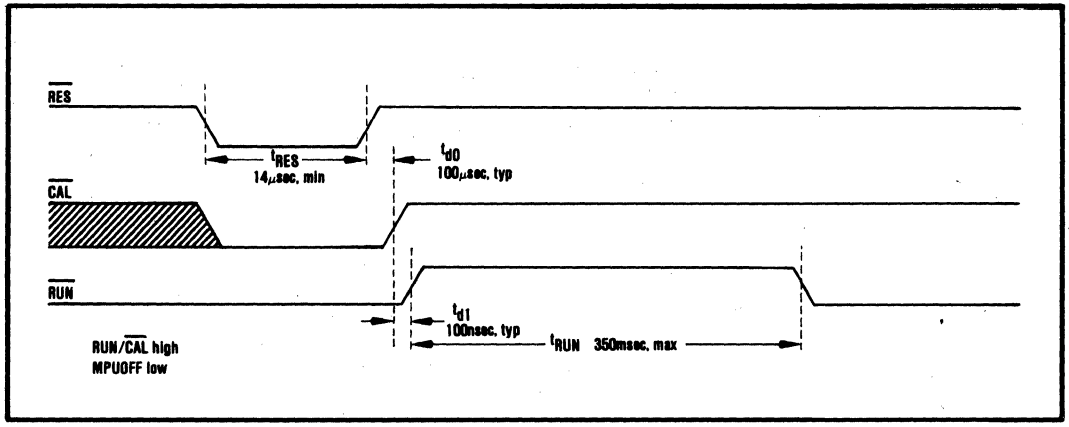


FIGURE 8. Service Mode Timing.

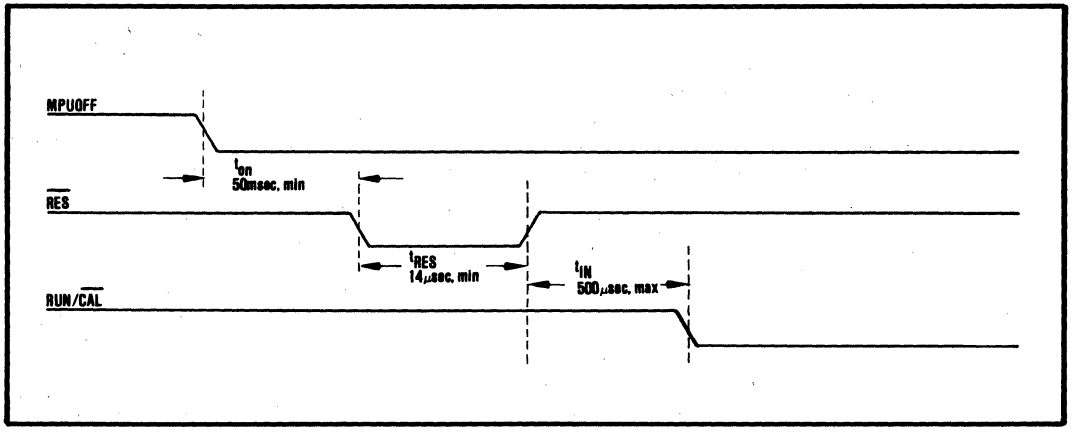


FIGURE 9. Control Timing Diagram.

Full Automatic Control

If the user wishes to automatically control the total operation of the DAC74 including the SERVICE mode as well as the SELF-CALIBRATION mode, additional timing considerations apply. An additional timing diagram is shown in Figure 8. Note that the MPUOFF must be asserted low 50msec before $\overline{RES}$ is asserted and the RUN/$\overline{CAL}$ must be asserted within 500μsec of the time that the $\overline{RES}$ pulse returns high.

MANUAL CALIBRATION

Manual adjustment of the DAC74 is accomplished by eight potentiometers located at one end of the package. Space for screwdriver access must be provided on the mounting surface. A label marked "REFER TO MANUAL BEFORE REMOVING LABEL" must be removed from the end of the package to access the potentiometers.

10V Reference Adjustment

After the DAC74 has been installed, the load connected, and a 1/2-hour warm-up period has elapsed, the references may be adjusted. The reference voltages should be set to 10V, ±10μV.

A 6-1/2 digit voltmeter, which has been calibrated as accurately as possible may be used to adjust the reference and coarse calibrate the D/A converter.

ADJUSTMENT PROCEDURE

1. Connect the voltmeter between the +10V REF OUT pin (26) and an ANALOG COMMON pin (5, 6, 35, 36). Adjust the +10V REF potentiometer to obtain a reading of 10.00000V, ±10μV.
2. Connect the voltmeter to the -10V REF OUT pin (22) and adjust the -10V REF potentiometer to read -10.00000V, ±10μV. Needed for bipolar only.

Note: If these reference voltages are to be used to provide references to other circuits, those loads must be connected before the above adjustments are made. External reference loads must remain constant for accurate operation of the DAC74.

Coarse Calibration of the Main D/A Converter.

The self-calibration controller can correct main D/A errors within a limited range. If the gain, offset or linearity shift due to initial installation environment, such as load return wire voltage drops, power supply voltage line regulation, or component aging, a manual coarse adjustment will be necessary. These six adjustments are made using potentiometers at the edge of the DAC74 package.

Coarse adjustments bring the errors of the DAC74 to within the operating range of the self-calibration circuit. It is sufficient to adjust the DAC74 output to within norminal values.

ADJUSTMENT PROCEDURE

After the DAC74 had been installed, the load connected, a 1/2-hour warm-up period has elapsed, and the reference voltages have been set, manual calibration may proceed.

Put the DAC74 into the SERVICE mode as described in the Service Mode section.

Adjustments will be made in the following order: OFFSET, preliminary GAIN, 4MSB's (LINEARITY), and final GAIN. Output voltage readings will be different for bipolar and unipolar configurations. Table I shows the data word to be strobed into DAC74, the potentiometer to be adjusted, and the output reading to be attained for unipolar and bipolar configurations.

After these adjustments are made, put the DAC74 in the SELF-CALIBRATION mode as described in the Self-Calibration Mode section. The DAC74 is now ready for normal operation.

TABLE I. Calibration Voltages.

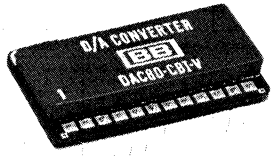
Step	Data Input Word (hex)	Adjust Potentiometer	D/A Output Reading	
			Unipolar	Bipolar
1	0000	OFFSET	0.0000V,±50μV	-10.0000V,±100μV
2	0800	GAIN	0.3125V,±50μV	-9.3750V,±100μV
3	1000	D12	0.6250V,±50μV	-8.7500V,±100μV
4	2000	D13	1.2500V,±50μV	-7.5000V,±100μV
5	4000	D14	2.5000V,±50μV	-5.0000V,±100μV
6	8000	D15	5.0000V,±50μV	0.0000V,±100μV
7	FFFF	GAIN	9.99985V,±50μV	-9.9997V,±100μV

OPERATIONAL CHECKLIST

1. Be sure that all pins and jumpers are connected properly as discussed and illustrated in the Installation section. Careful layout and shielding is necessary to keep digital noise out of the analog circuits.
2. The load return line from the load to RTN (pin 7, P3) must have less than 20μV voltage drop across its length for proper operation. See Installation section.
3. Be sure and wait about 1 2-hour for warm-up.
4. Check power supply voltages at the module pins.
   +15V and -15V, ±0.5V
   +5V, ±0.25V
5. Check +12V and -12V voltages generated internally.
   +12V, ±0.6V pin 39, P3
   -12V, ±0.6V pin 40, P3
6. Check +10V and -10V references. The D A converter accuracy is directly dependent on these voltages. See Adjustment Procedure in the Manual Calibration section.
   +10.00000V, ±10μV pin 26, P3
   -10.00000V, ±10μV pin 22, P3
7. Check MPUOFF (pin 14, P3) to be sure it is low. It must be low for at least 50msec before attempting self-calibration.
8. Be sure $\overline{UNIPOLAR\ CAL}$ (pin 18, P3) is high for bipolar operation or low for unipolar operation.
9. $\overline{RES}$ pulse must be at least 14μsec wide.
10. If $\overline{CAL}$ status does not return low during an automatic self-calibration, the D/A converter may be out of tolerance. Adjust it using the procedure in the Manual Calibration section. An unsuccessful self-calibration can result from a voltage or current transient in the D/A converter system. Attempt a second self-calibration.

BURR-BROWN®

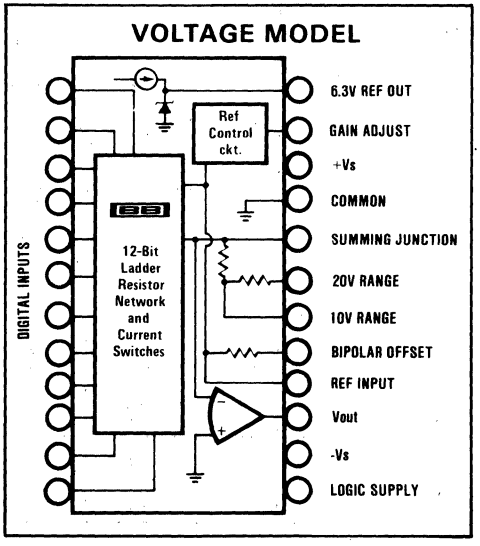
DAC80



Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES:

- WIDE POWER SUPPLY RANGE MODELS AVAILABLE (Z MODELS)
- 12-BIT, 3-DIGIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY
- COMPLETE WITH INTERNAL REFERENCE AND OUTPUT AMPLIFIER (V MODELS)
- FAST SETTLING - 300nsec to ±0.01% (I MODELS)
- CERAMIC DUAL-IN-LINE PACKAGE
- LOW COST



DESCRIPTION

Use this popular 12-bit digital-to-analog converter for low cost precision performance applications.

DAC80, with internal reference and optional output amplifier, offers a maximum nonlinearity error of ±0.012%, ±30ppm/°C maximum gain drift, and monotonicity - all over a 0°C to 70°C operating range. In the bipolar configuration, total accuracy drift is guaranteed to be less than ±25ppm/°C. Select TTL compatible complementary 12-bit binary (CBI) or 3-digit BCD (CCD) input codes.

Packaged within DAC80's 24-pin dual-in-line ceramic case are fast-settling switches and stable, laser-trimmed thin-film resistors that let you select output voltage ranges of ±2.5, ±5, ±10, 0 to +5, 0 to +10 volts (V models) or output current ranges of ±1mA or 0 to -2mA (I models). Voltage output models settle to ±0.01% of FSR in 3μsec for a 10V step change.

By specifying the DAC80Z model with a supply range of ±11.4V to ±16.0V, you can use this proven D/A converter in microprocessor and semiconductor memory systems.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

ELECTRICAL

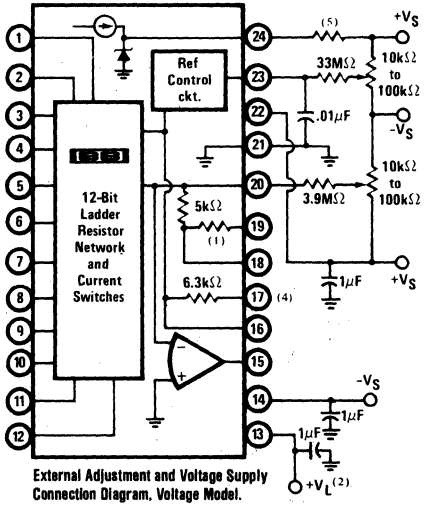
MODEL	DAC80CBI			DAC80CCD			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DIGITAL INPUT							
Resolution			12				Bits
						3	Digits
Logic Levels (TTL/Compatible)(1)							
Logic "1" (+40μA max at +5.0V)	+2.4		+5.0	+2.4		+5.0	VDC
Logic "0" (1.6mA max at +0.4V)	0		+0.4	0		+0.4	VDC
ACCURACY							
Linearity Error at 25°C		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	+1, -3/4		±1/4	±1/2	LSB
Gain Error(2)		±0.1	±0.3		±0.1	±0.3	%
Offset Error(2)		±0.05	±0.15		±0.05	±0.15	% of FSR(3)
Monotonicity Temp. Range, min	0		+70	0		+70	°C
DRIFT(4) (0°C to +70°C)							
Total bipolar drift, max (includes gain, offset, and linearity drifts)(5)			±25			±25	ppm of FSR/°C
Total error over 0°C to +70°C(6)							
Unipolar		±0.08	±0.15		±0.08	±0.15	% of FSR
Bipolar		±0.06	±0.12		±0.06	±0.12	% of FSR
Gain		±15	±30		±15	±30	ppm/°C
Exclusive of internal reference			±10			±10	ppm/°C
Unipolar Offset		±1	±3		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, -7/8		±1/2	+1, -7/8	LSB
Linearity Error 0°C to +70°C			±1/2			±1/2	LSB
CONVERSION SPEED/V models							
Settling Time to ±0.01% of FSR							
For FSR Change							
with 10kΩ Feedback		5			5		μsec
with 5kΩ Feedback		3			3		μsec
For 1LSB Change		1.5			1.5		μsec
Slew Rate	10	20		10	20		V/μsec
CONVERSION SPEED/I models - of FSR							
Settling Time to ±0.01%							
For FSR Change							
10Ω to 100Ω Load		300			300		nsec
1kΩ Load		1			1		μsec
ANALOG OUTPUT/V models							
Ranges(7)	±2.5, ±5, ±10, 0 to +5, 0 to +10				0 to +10		Volts
Output Current	±5			±5			mV
Output Impedance (DC)		0.05			0.05		ohms
Short Circuit Duration	Indefinite to Common						
ANALOG OUTPUT/I models							
Ranges		±1, 0 to -2			0 to -2		mA
Output Impedance - Bipolar		4.4			4.4		kΩ
Output Impedance - Unipolar		15			15		kΩ
Compliance			±2.5			±2.5	Volts
INTERNAL REFERENCE VOLTAGE		+6.3			+6.3		Volts
Maximum External Current(8)			±200			±200	μA
Tempco of Drift, max		±10	±20		±10	±20	ppm/°C
POWER SUPPLY SENSITIVITY							
+15V Supply		±0.02			±0.02		% of FSR/% Vs
-15V and +5V Supplies		±0.002			±0.002		% of FSR/% Vs
POWER SUPPLY REQUIREMENTS							
DAC80	±14, +4.75	±15, +5	±16, +16	±14, +4.75	±15, +5	±16, +16	VDC
DAC80Z(7)	±11.4, +4.75	±12, +5	±16, +16	±11.4, +4.75	±12, +5	±16, +16	VDC
Supply Drain							
±15V/±12V (including 5mA load)		±25	±35		±25	±35	mA
+5V (logic supply)		+20	±30		+20	±30	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (double above specs)	-25		+85	-25		+85	°C
Storage	-55		+100	-55		+100	°C

NOTES:

1. Adding external CMOS hex buffers CD 4009A will provide CMOS input compatibility.
2. Adjustable to zero with external trim potentiometer.
3. FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
4. To maintain drift spec internal feedback resistors must be used for current output models.
5. See "Computing Total Accuracy Over Temperature."
6. With gain and offset errors adjusted to zero at 25°C. See discussion on last page.
7. DAC80Z supply range is ±12.0V min to ±16.0V max for 0 to +10V and ±10V outputs.
8. Maximum with no degradation of specifications.

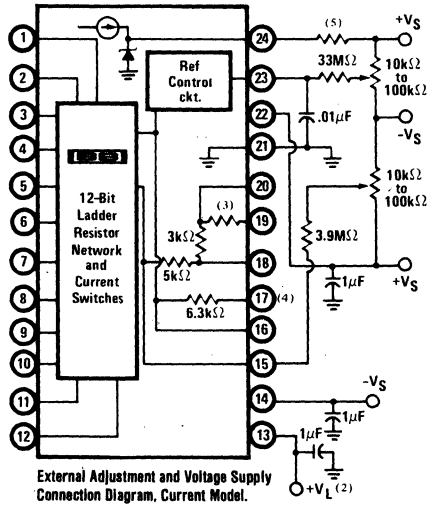
CONNECTION DIAGRAMS

VOLTAGE MODEL



External Adjustment and Voltage Supply Connection Diagram, Voltage Model.

CURRENT MODEL



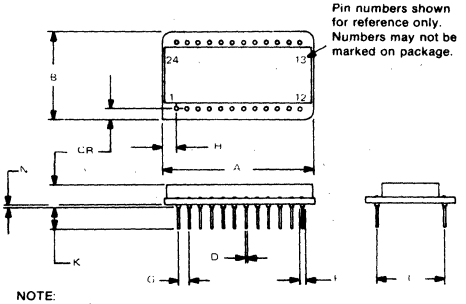
External Adjustment and Voltage Supply Connection Diagram, Current Model.

NOTES:
1. 3kΩ for CCD models, 5kΩ for CBI models.
2. If connected to+Vs, which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model, 0Ω and pin 20 has no internal connection.
4. 6.3kΩ resistor internally grounded on CCD models.
5. Resistor required only for Z models, see "Operating Instructions". Make no connection to power supply on non-Z models.

PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
LOGIC SUPPLY	13	LOGIC SUPPLY
-Vs	14	-Vs
IOUT	15	VOUT
REF. INPUT	16	REF. INPUT
BIPOLAR OFFSET	17	BIPOLAR OFFSET
SCALING NETWORK	18	10V RANGE
SCALING NETWORK	19	20V RANGE
SCALING NETWORK	20	SUMMING JUNCTION
COMMON	21	COMMON
+Vs	22	+Vs
GAIN ADJUST	23	GAIN ADJUST
6.3V REF. OUT	24	6.3V REF. OUT

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm)R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	085	.105	2.16	2.67

CASE: Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DISCUSSION

DIGITAL INPUT CODES

The DAC80 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, CTC or COB.

TABLE I. Digital Input Codes.

DIGITAL INPUT		ANALOG OUTOUT		
	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+1/2 Full Scale	Zero	-Full Scale
	100000000000	Mid-scale -1LSB	-1LSB	-Full Scale
	111111111111	Zero	-Full Scale	Zero
	MSB LSB	CCD		
CCD Models		Complementary Coded Decimal - 3 Digits		
	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C and +70°C; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

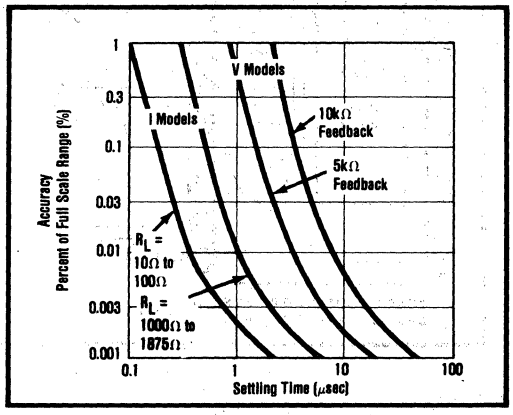


FIGURE 1. Full Scale Range Settling Time vs Accuracy

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to -2V. See Table IV.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage swing permitted without damage to the DAC80 is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in

either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

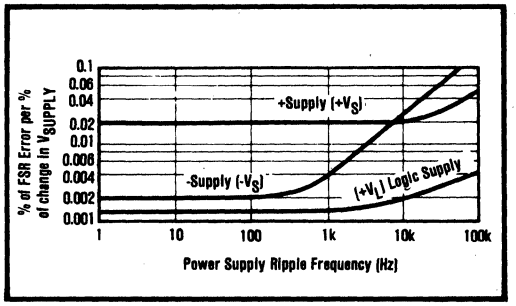


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) has a tolerance of ±5% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 200μA. An external buffer amplifier is recommended if this reference will be used to drive other system components.

OPERATING INSTRUCTIONS

±12 VOLT SUPPLY OPERATION

The Z models will operate with supply voltages as low as ±11.4V. For operation with supplies less than ±14V an external resistor must be connected between the positive supply and pin 24. This provides additional current required by the internal reference. The required resistor value for supply voltages of ±11.4V to ±12.6V is 2.0kΩ and for supplies of ±12.6V to ±14V is 3.9kΩ.

It is recommended that output voltage ranges -10V to +10V and 0 to +10V not be used with the Z model if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{supply}| - |V_{out}\ max| < 2.0V$. This applies to units with both CBI and CCD input codes. Except for operation at lower supply voltages, the DAC80Z and DAC80 operation is identical.

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 33MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. The Gain Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figures 4 and 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A converters.

Offset Adjustment: For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

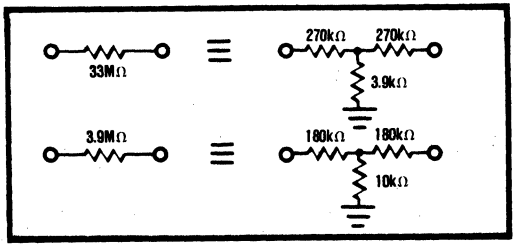


FIGURE 3. Equivalent Resistance.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections.

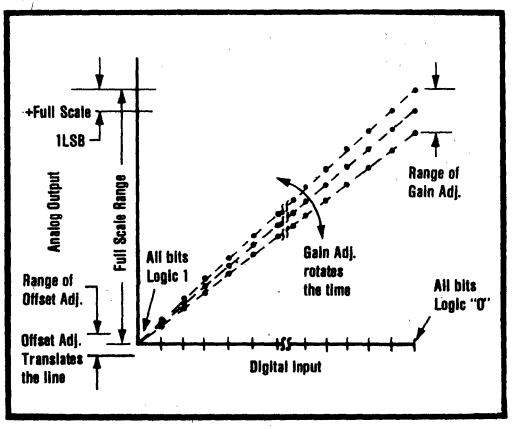


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

TABLE II. Digital Input/Analog Output.

	DIGITAL INPUT	ANALOG OUTPUT			
		VOLTAGE*		CURRENT	
		0 to +10V	±10V	0 to -2mA	±1mA
CBI Models	12-Bit Resolution MSB LSB				
	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
	011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
	100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
	111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
	One LSB	2.44mV	4.88mV	0.488μA	0.488μA
CCD Models	3-Digital Resolution MSB LSB				
	0110 0110 0110	+9.990V**	N/A	-1.249mA	N/A
	0110 0110 1111	+9.900V	N/A	-1.238mA	N/A
	0110 1111 1111	+9.000V	N/A	-1.125mA	N/A
	1111 1111 1111	0.000V	N/A	0.000mA	N/A
	One LSB	10.00mV	N/A	1.25μA	N/A

*To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

**Normal Full Scale Range with correct codes; output can go higher if illegal codes are applied.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

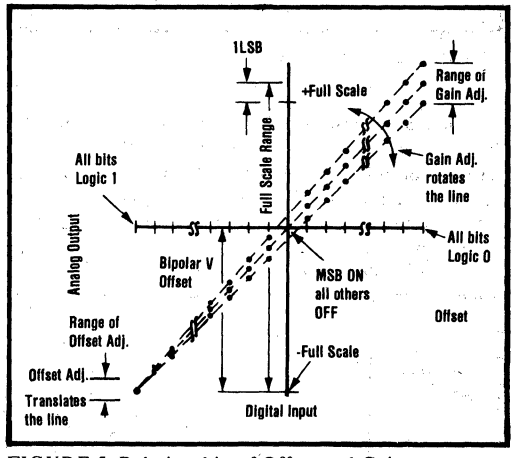


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

VOLTAGE OUTPUT MODELS

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10V*, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V*. See Figure 6.

*Refer to ±12V Supply Operation discussion.

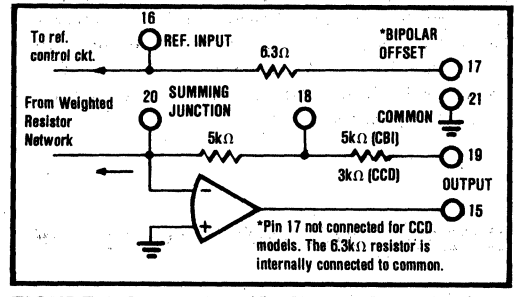


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized in the DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

TABLE III. Output Voltage Range Connections - Voltage Model DAC80.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

CURRENT OUTPUT MODELS

The equivalent output circuit and resistive scaling network of the current model differ from the voltage model and are shown in Figures 7 and 8. Instructions for using the DAC80-XXX-I with a resistor or an external op amp follow. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25 ppm/°C or less to minimize drift. This will typically add ±50 ppm/°C + the TCR of R_L (or R_F) to the total drift.

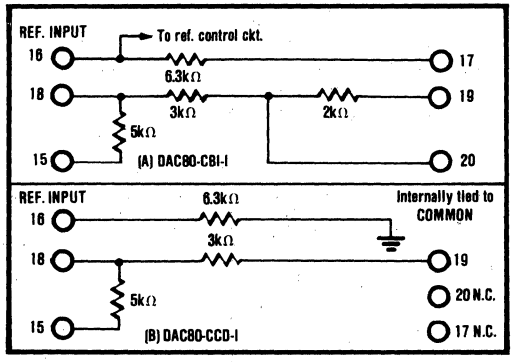


FIGURE 7. Internal Scaling Resistors.

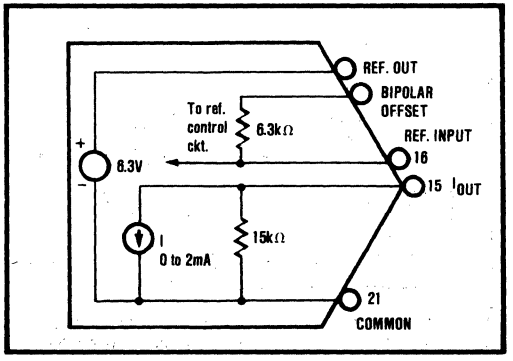


FIGURE 8. DAC80 Current Model Equivalent Output Circuit.

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{15k\Omega \times R_L}{15k\Omega + R_L} \right)$$

Where R_L max = 1.36kΩ
and V_{OUT} max = -2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With $R_{LS} = 0$, V_{OUT} = -1.82V.

CCD Input Code: Connect the internal scaling resistors as shown in Table IV and add an external metal film

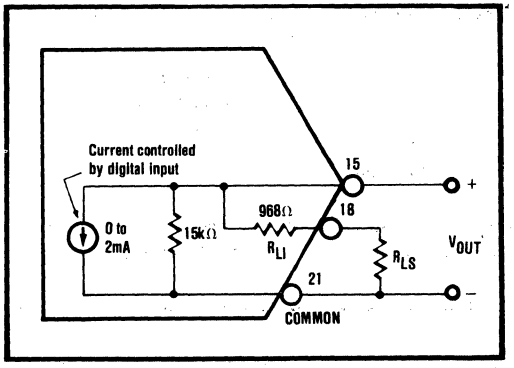


FIGURE 9. Equivalent Circuit DAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load.

TABLE IV. DAC80-XXX-I Resistive Load Connections.

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance		R_{LI} Connections			Reference	Bipolar Offset		
			R_{LS}	R_{LP}	Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Connect Pin 16 to	Connect Pin 17 to	R_{LS}	R_{LP}
CSB	0 to -2V	0.968kΩ	105Ω	N/A	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)	N/A
CCD	0 to -2V	1.875kΩ	N/A	36.5kΩ	19	Com (21)	N.C.	24	N.C	N/A	Between Pin 15 & 21
COB or CTC	±1V	1.2kΩ	90.9Ω	N/A	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)	N/A

resistor (R_{LP}) in parallel as shown in Figure 10 to obtain a 0 to -2V full scale output voltage range for CCD input codes:

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}}$$

$$V_{OUT} = -1.25mA \left(\frac{15.6k\Omega \times R_L}{15.6k\Omega + R_L} \right)$$

If $R_{LP} = \infty$, $V_{OUT} = -2.08V$

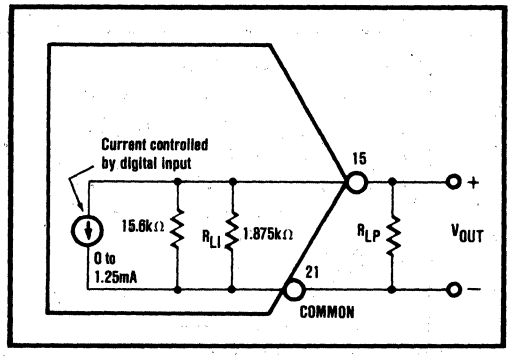


FIGURE 10. DAC80-CCD-I Connected for Voltage Output with Resistive Load.

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent ouptut circuit for a bipolar output voltage range is shown in Figure 11, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 4.44k\Omega}{R_L + 4.44k\Omega} \right)$$

Where R_L max = 5.72kΩ

V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V.

$$\text{With } R_{LS} = 0,\ V_{OUT} = \pm 0.944V.$$

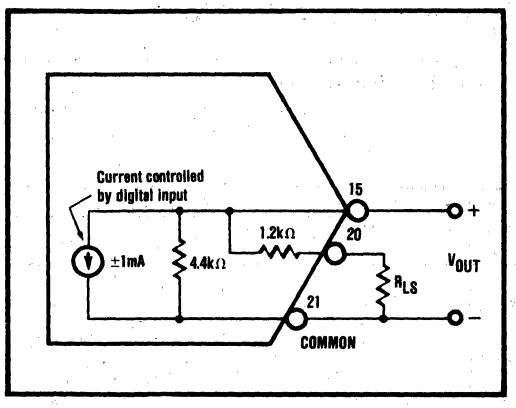


FIGURE 11. DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load.

DRIVING AN EXTERNAL OP AMP

The current model DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 12.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V.

TABLE V. Voltage Range of Current Output DAC80.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	Ⓐ	24

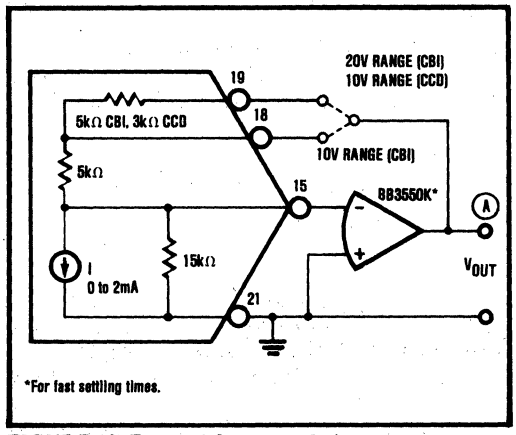


FIGURE 12. External Op Amp - Using Internal Feedback Resistors.

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges. See Figure 13. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the

lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

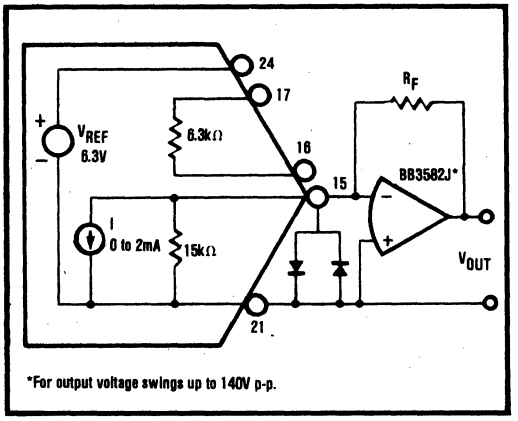


FIGURE 13. External Op Amp - Using External Feedback Resistors.

COMPUTING TOTAL ACCURACY OVER TEMPERATURE

The accuracy drift with temperature of a DAC80 consists of three primary components: Gain drift, unipolar or bipolar offset drift, and linearity drift. To obtain the worst case accuracy drift, most users would assume that all drift errors are random and would simply add them algebraically. However, the worst case accuracy drift for a DAC80 operating in the bipolar mode is about one-half of the algebraic sum of the individual drift errors.

To explain this fact, it is necessary to consider the unipolar and bipolar modes of operation separately. Note that the linearity drift of both modes is negligible. (Total linearity error is less than ±1/2LSB over 0°C to +70°C.)

In the unipolar mode of operation, offset drift (±1 ppm/°C) is due primarily to voltage offset drift of the output op amp and, to a lesser extent, to the leakage current through the quad current switches. Gain drift consists of several components: 1) ±10 ppm/°C due to ratio drift of current weighting resistors to the reference resistor and current switch V_{BE} to the reference transistor (refer to Model 4550 data sheet); and 2) ±20 ppm/°C due to the zener reference. The sum of these two components, ±30 ppm/°C, is the maximum gain drift.

Because the parameters described could all drift in the same direction, the worst case accuracy drift in the unipolar mode is simply the sum of the components, or ±31 ppm/°C.

In the bipolar mode the major portion (67%) of gain drift is due to the zener reference. The gain and offset drifts caused by reference drift are always in opposite directions. Therefore, the accuracy drift will be the difference rather than the sum of these drifts.

First, consider the effect of reference variations on offset drift. Figure 14 shows a simplified circuit diagram of a DAC80 operating in the bipolar mode with all bits off. The current switch leakage current is negligible, so

$$V_{\text{-FULL SCALE}} = -\frac{R_F}{R_{BPO}} \times V_{REF}$$

$$= -\frac{10k\Omega}{6.3k\Omega} \bullet 6.3V = -10V$$

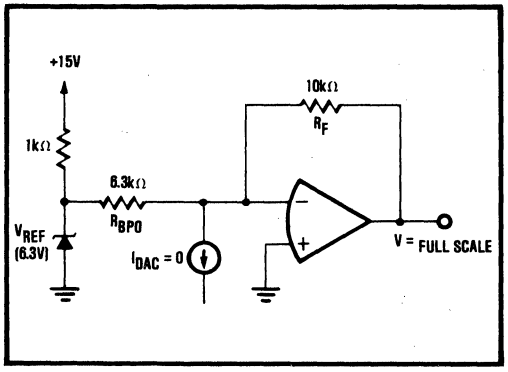


FIGURE 14. Simplified Diagram of DAC80 with "All Bits Off" Operating in Bipolar ±10V Range.

This equation shows that if V_{REF} increases, the output voltage will decrease and vice versa. If the V_{REF} drift is +20 ppm/°C, this is equivalent to (+20 ppm/°C) x (+6.3V) = +126μV/°C. This will result in a voltage drift at the amplifier output of

$$\frac{\Delta V_{\text{-FS}}}{\Delta T} = -\frac{R_F}{R_{BPO}} \bullet \frac{\Delta V_{REF}}{\Delta T}$$

$$= -\frac{10k\Omega}{6.3k\Omega} \bullet 126\mu V/°C = -200\mu V/°C.$$

Since the DAC80 is operating in the ±10V range this is equivalent to (-200μV/°C) ÷ (20V range) = -10 ppm of FSR/°C.

Now consider the effect of reference changes on gain drift. When all the bits are turned on it can be shown that:

$$\frac{\Delta V_{\text{+FULL SCALE}}}{\Delta T} = +\frac{R_F}{R_{BPO}} \bullet \frac{V_{REF}}{\Delta T}$$

$$= +\frac{10k\Omega}{6.3k\Omega} \bullet 126\mu V/°C = +200\mu V/°C$$

and $\frac{+200\mu V/°C}{20V \text{ Range}} = +10 \text{ppm/°C of FSR.}$

This result indicates that the drift of the minus full scale voltage will be equal in magnitude to, and in the opposite direction of, the drift of the plus full scale voltage and that zener reference variations have virtually no effect on the zero point (see Figure 15). This equation also indicates that the gain drift is equal to the V_{REF} drift in ppm/°C, and the magnitude of the minus full scale drift and plus full scale drift is equal to one-half of the V_{REF} drift.

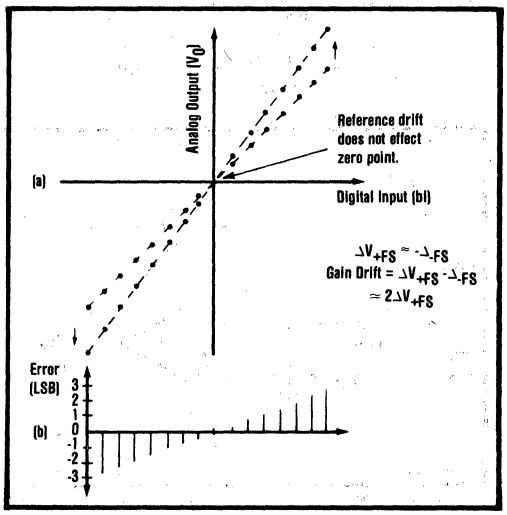


FIGURE 15. (a) Effect of a Positive Reference Drift on the Ideal D/A Transfer Function; (b) Error Distribution Due to Reference Voltage Drift in a DAC80.

Using this relationship, the worst case accuracy drift for a bipolar DAC80 can be computed. The maximum TCR of the zener reference is ±20ppm/°C. The gain drift due to the reference then is also ±20ppm/°C. The full scale drift and bipolar offset drift are each half that amount or ±10ppm/°C. The maximum gain and offset drifts of the DAC80, exclusive of the reference, are ±10ppm/°C and ±5ppm/°C respectively. Adding this to the full scale drift due to the reference gives a worst case total accuracy drift of ±25ppm/°C. (Random drifts, which these are, can be in the same direction, so they add directly.) This is much less than the total drift obtained by simply adding the maximum gain and bipolar offset drifts (±45ppm/°C). The maximum zero point drift is equal to one-half of the gain drift exclusive of the reference plus the offset drift exclusive of the reference, or ±10ppm of FSR/°C.

The DAC80 is specified over a 0°C to +70°C temperature range giving a maximum excursion from room temperature (+25°C) of 45°C. Assuming that gain and offset errors have been adjusted to zero at room temperature,

total worst case accuracy error
= Linearity error + Accuracy drift x ΔT
= ±0.01% + ±25ppm/°C (45°C)(100)
= ±0.12%;

total worst case bipolar zero point error
= Bipolar zero drift x ΔT
= ±10ppm of FSR% (45°C)(100)
= ±0.045%.

ORDERING INFORMATION

DAC80	X –	XXX –	X
Low Cost 12-Bit D/A Converter Family Example: DAC80-CBI-V Binary DAC80 with voltage output	Z = Wide Supply Range Blank = Standard	INPUT CODE CBI = Complementary 12-bit binary CCD = Complementary 3-digit BCD	OUTPUT V = Voltage I = Current

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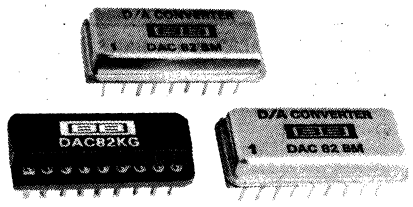


DAC82

8-BIT DIGITAL-TO-ANALOG CONVERTER

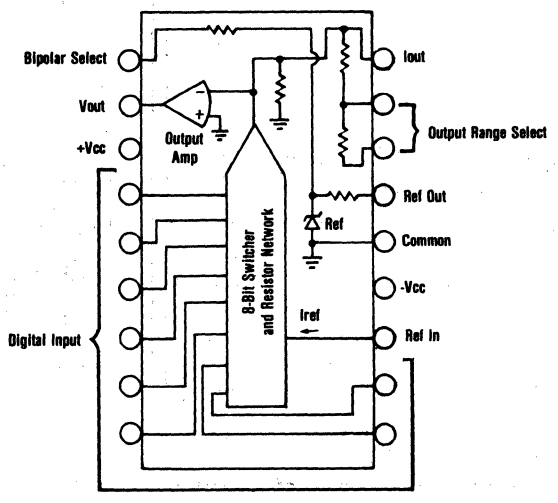
FEATURES

- 8-BIT RESOLUTION/LINEARITY
- NO EXTERNAL ADJUSTMENTS REQUIRED FOR ±1LSB ACCURACY
- INTERNAL REFERENCE AND SCALING RESISTORS
- 2-QUADRANT MULTIPLYING WITH EXTERNAL REFERENCE
- HERMETIC, DUAL-IN-LINE PACKAGE
- OPERATION OVER −55°C TO +125°C

DESCRIPTION

The DAC82 is an 8-bit digital-to-analog converter with voltage and current outputs. Packaged in an 18-pin metal DIP, it is complete with its own internal reference and scaling resistors. When used with a variable, external reference, the DAC82 will multiply in two quadrants. Two versions are available: the DAC82BM (-25°C to +85°C) and the DAC82SM (-55°C to +125°C). Both offer ±1LSB absolute accuracy at room temperature with no external adjustments required and nonlineaity is guaranteed to be within ±1/2LSB over the specified temperature ranges. The small size of the DAC82 makes it an ideal choice for applications where space or weight is at a premium such as aircraft instrumentation, portable instruments, or CRT displays.

FUNCTIONAL DIAGRAM



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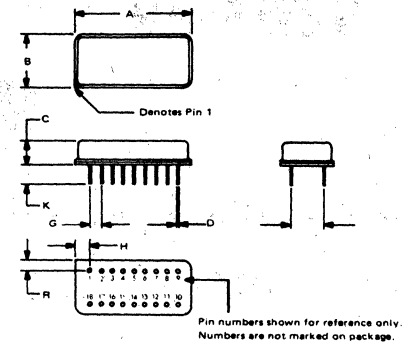
ELECTRICAL SPECIFICATIONS

MODEL	DAC82KG DAC82BM	DAC82SM	UNITS
DIGITAL INPUT			
Resolution	8	8	Bits
Logic Levels (TTL compatible)			
Logic "1"	+2 < e_d < +5.5 at +40μA		V
Logic "0"	0 < e_d < +0.8 at -1.0mA		V
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error at 25°C (max)	±0.16	±0.16	% of FSR
-25°C to +85°C (max)	±0.2		% of FSR
-55°C to +125°C (max)		±0.2	% of FSR
Differential Linearity Error	±0.5	±0.5	LSB
Gain Error	±0.1	±0.1	%
Offset Error	±0.05	±0.05	% of FSR
Total Accuracy Error (max)	±1	±1	LSB
Monotonicity Temp Range	-25 to +85	-55 to +125	°C
DRIFT			
Gain (max)			
-25°C to +85°C	±50		ppm/°C
-55°C to +125°C		±35	ppm/°C
Offset			
Unipolar			
-25°C to +85°C	±1		ppm of FSR/°C
-55°C to +125°C		±1	ppm of FSR/°C
Bipolar (max)			
-25°C to +85°C	±20		ppm of FSR/°C
-55°C to +125°C		±15	ppm of FSR/°C
CONVERSION SPEED			
Voltage Output			
Settling time to ±0.2% of FSR			
For FSR change			
20V Range	2.5		μsec
10V Range	2.0		μsec
For 1 LSB change	0.5		μsec
Slew Rate	20		V/μsec
Current Output			
Settling time to ±0.2%			
For FSR change			
10 to 100Ω load	250		nsec
1kΩ load	350		nsec
OUTPUT			
ANALOG OUTPUT			
Voltage Output			
Ranges	±2.5, ±5, ±10, +5, +10		Volts
Output Current, min	±5		mA
Output Impedance (DC)	0.05		Ω
Current Output			
Ranges	±0.8, 0 to -1.6		mA
Output Impedance - Bipolar	1.8		kΩ
Unipolar	2.0		kΩ
Compliance	±4.0V		Volts
INTERNAL REFERENCE VOLTAGE			
Magnitude	+6.3		Volts
Tempco of Drift, max	±20		ppm/°C
POWER SUPPLY SENSITIVITY			
+15VDC Supply	±0.02		% of FSR/%Vs
-15VDC Supply	±0.002		% of FSR/%Vs
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15		Volts
Range	±14.0 to ±16.0		Volts
Supply Drain (No load)			
+15VDC	15		mA
-15VDC	10		mA
TEMPERATURE RANGE			
Specification	-25 to +85	-55 to +125	°C
Operating (double above drift specs)	-55 to +125	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C

MECHANICAL

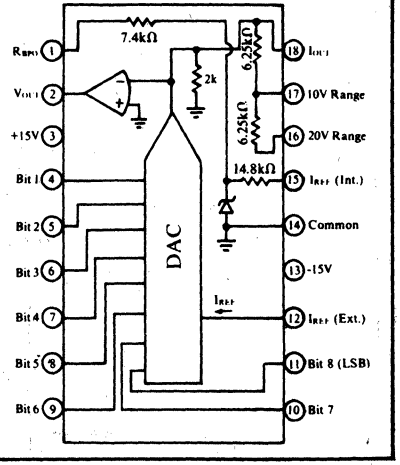
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.



CONNECTOR: None
CASE: Metal (BM, SM) Ceramic (KG)
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
HERMETICITY: Gross Leak (fluorocarbon) Fine Leak (helium, 5 x 10^{-7}cc/sec) (BM, SM only)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.060	1.080	26.92	27.43
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

CONNECTION DIAGRAM



DIGITAL INPUT CODES

The DAC82 accepts digital inputs in complementary binary (CBI) format and may be connected for complementary straight binary (CSB) or complementary offset binary (COB) operation. By using one external inverter, the user can operate the DAC82 in the complementary two's complement (CTC) mode.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
	0 to +10V	±10V	0 to 1.6mA	±0.8mA
MSB LSB				
0 0 0 0 0 0 0 0	+9.961V	+9.922V	-1.594mA	-0.794mA
0 1 1 1 1 1 1 1	+5.000V	0.000V	-0.800mA	0.000mA
1 0 0 0 0 0 0 0	+4.961V	-78.12mV	-0.792mA	+6.248μA
1 1 1 1 1 1 1 1	0.000V	-10.000V	0.000mA	+0.800mA
one LSB	39.06mV	78.12mV	6.248μA	6.248μA

* To obtain values for other binary (CBI) ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE I. Digital Input and Analog Output Relationship.

ACCURACY

LINEARITY

The LINEARITY of a D/A converter is the true measure of its performance. The DAC82 analog output will not vary by more than ±1/2 LSB from an ideal straight line drawn between the end points (all 1's and all 0's) over the specified temperature range.

DIFFERENTIAL LINEARITY

The DIFFERENTIAL LINEARITY error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A DIFFERENTIAL LINEARITY error specification of ±1/2 LSB means that the output voltage can change anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent digital state to the next.

DRIFT

GAIN DRIFT

GAIN DRIFT is a measure of the change in the analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at the high and low temperature extremes and at 25°C for each model, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in output voltage at zero volts output over the specified temperature range. The offset voltage is measured at the temperature extremes, and the maximum change referenced to 25°C is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the time required for the output to enter and remain in an error band equal to ±0.2% of full scale range measured from the time the digital input is changed. Typical settling time values for full scale changes are a function of the load resistor and are shown in the figure below.

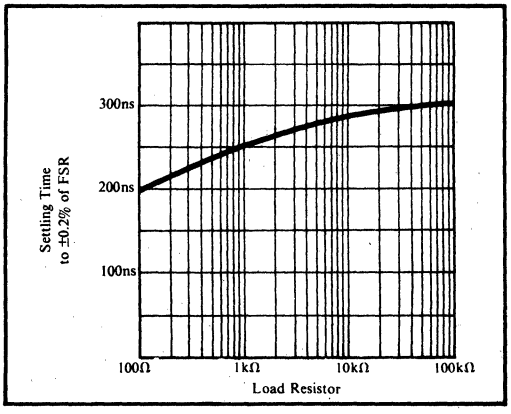


FIGURE 1. Settling Time for FSR Change vs Load.

COMPLIANCE

The COMPLIANCE VOLTAGE of the DAC82 is the maximum voltage swing allowed on the current output in order to maintain the specified accuracy. It is -4.0 to +4.0 volts for the unipolar and bipolar current ranges.

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D/A converter output. It is defined as a percent of FSR/percent of change in either the +15 volt or -15 volt power supplies about the nominal power supply voltages. Figure 2 shows Power Supply Rejection vs Frequency.

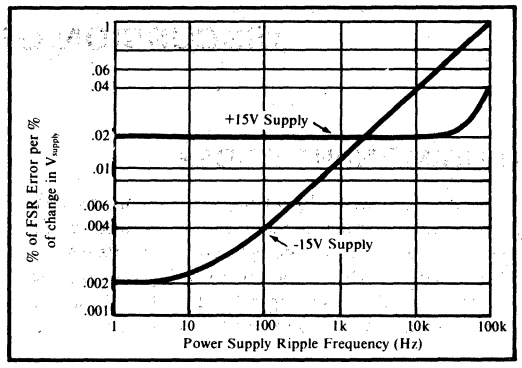


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC82 and should be tantalum or electrolytic types bypassed with a 0.01 μF ceramic capacitor for best high frequency performance.

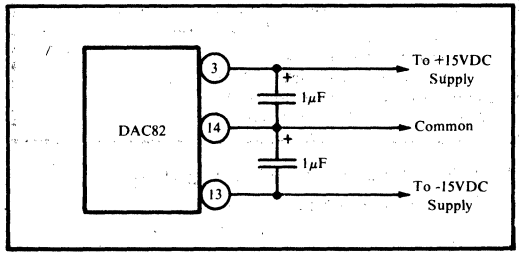


FIGURE 3. Recommended Power Supply Decoupling.

OPERATION IN THE CURRENT OUTPUT MODE

On the current output pin, the DAC82 provides a unipolar output current of 0 to -1.6mA and a bipolar output current of ±0.8mA. Refer to Figure 4 and Table II for proper connections. In applications requiring the use of the DAC82 in the current output mode, such as an A/D converter, the internal scaling resistors should be used to generate currents corresponding to analog input voltages.

OUTPUT RANGE	CONNECT PIN 1 TO:
0 to -1.6mA	N.C.
±0.8mA	Pin 18

TABLE II. Connections for Current Output Mode.

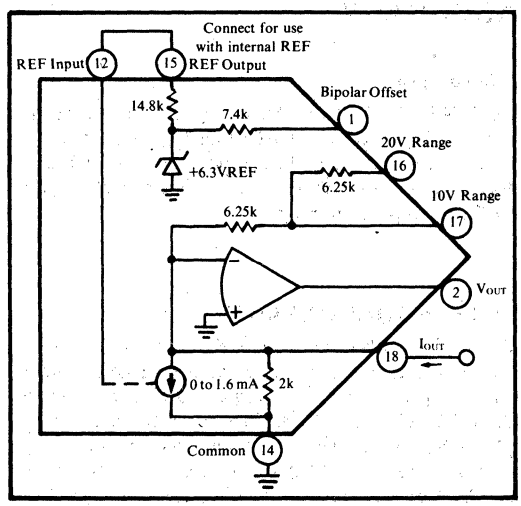


FIGURE 4. Current Output Mode Connection Diagram.

DRIVING AN EXTERNAL OP AMP

UNIPOLAR OR BIPOLAR - UP TO 20V OUTPUT RANGE

The DAC82 will drive the summing junction of an op amp (the op amp being used as a current to voltage converter) to produce an output voltage (see Figure 5).

$$V_{OUT} = -I_{OUT} \times R_F$$

where I_{OUT} is the DAC82 output current and R_F is the feedback resistor. The internal feedback resistors should be used to maintain the temperature drift specification. Refer to Table III and Figure 5 for proper connections.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT (A) TO	CONNECT PIN 1 TO	CONNECT PIN 16 TO
±10V	COB or CTC	16	18	(A)
±5V	COB or CTC	17	18	N.C.
±2.5V	COB or CTC	17	18	18
0 to +10V	CSB	17	Common	N.C.
0 to +5V	CSB	17	Common	18

TABLE III. Voltage Ranges of Current Output DAC82 with External Op Amp.

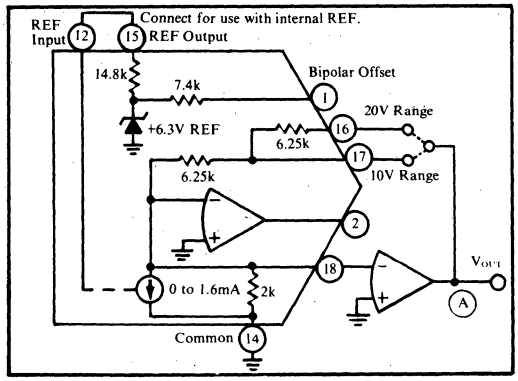


FIGURE 5. External Op Amp - Using Internal Feedback Resistors.

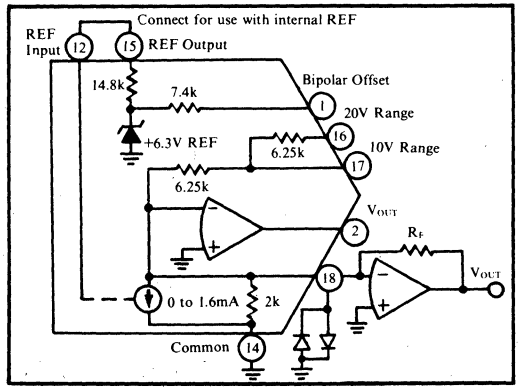


FIGURE 6. External Op Amp - Using External Feedback Resistors.

OUTPUTS LARGER THAN 20 VOLT RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±0.8mA for bipolar voltage ranges, and 0 to -1.6mA for unipolar voltage ranges (see Figure 6). Use protection diodes when a high voltage op amp is used.

VOLTAGE OUTPUT OPERATION USING INTERNAL AMPLIFIER

The DAC82 contains internal scaling resistors to provide a wide range of output voltage ranges. These resistors may be connected to provide 3 bipolar output ranges of ±10, ±5, or ±2.5 volts or two unipolar output voltage ranges of 0 to +5 or 0 to +10 volts. Gain and offset drift errors are minimized since these scaling resistors are an integral part of the DAC. Connections for DAC82 output voltage ranges are shown in Table IV and Figure 7 below.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 2 TO	CONNECT PIN 1 TO	CONNECT PIN 16 TO
±10V	COB or CTC	16	18	2
±5V	COB or CTC	17	18	N.C.
±2.5V	COB or CTC	17	18	18
0 to +10V	CSB	17	Common	N.C.
0 to +5V	CSB	17	Common	18

TABLE IV. Voltage Ranges of Current Output DAC82 with External Op Amp.

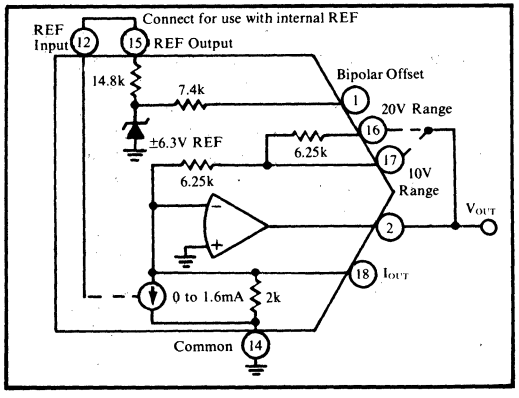


FIGURE 7. Voltage Output Using Internal Amplifier.

OPERATION AS MULTIPLYING DAC

By using an external voltage reference, the DAC82 can be connected as a multiplying DAC, such that the analog output represents the product of the digital input and the analog reference input. To operate the DAC82 as a two quadrant MDAC, connect the unit as shown in Figure 8. If R2, the bipolar offset resistor, is replaced with an open circuit, the DAC will operate in one quadrant. Table V below shows the digital input and analog output relationships for one quadrant and two quadrant multiplication and Figure 8 shows the connection for output voltage or output current. Since the absolute temperature coefficient of the internal feedback resistors (6.25k) is typically 30 ppm/°C, improved temperature stability can be achieved by using an external 13.5k resistor connected between pins 2 and pins 18, making no connection to pins 16 or 17.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -1.6mA	±0.8mA
00000000	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.9961)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.9922)$	$\frac{(4\ V_R)}{(R_1)}(0.9961)$	$\frac{(4\ V_R)}{(R_1)}(0.9922)$
0111111	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.5000)$	0.0000	$\frac{(4\ V_R)}{(R_1)}(0.5000)$	0.0000
10000000	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.4961)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(-0.0078)$	$\frac{(4\ V_R)}{(R_1)}(0.4961)$	$\frac{(4\ V_R)}{(R_1)}(-0.0078)$
1111111	0.0000	$\frac{(4\ V_R)(R_F)}{(R_1)}(-1)$	0.0000	$\frac{(4\ V_R)}{(R_1)}(-1)$
1 LSB	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.0039)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.0078)$	$\frac{(4\ V_R)}{(R_1)}(0.0039)$	$\frac{(4\ V_R)}{(R_1)}(0.0078)$

TABLE V. Digital Input and Analog Output Relationship for Multiplying Configuration.

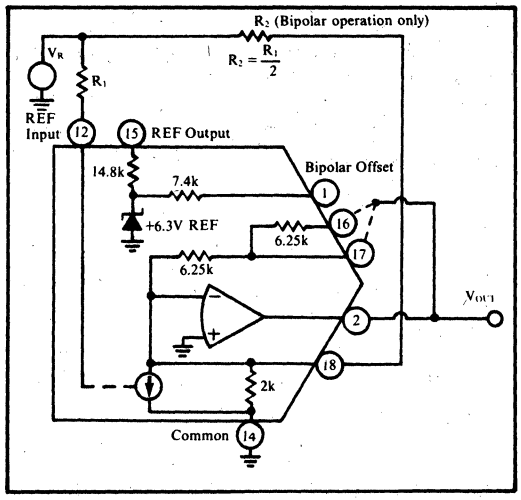


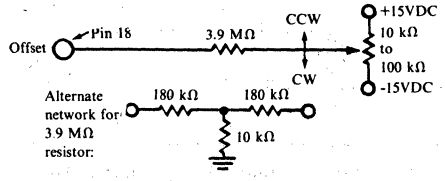
FIGURE 8. Connection for Multiplying Mode.

OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS

The DAC82 has been laser trimmed at the factory to insure absolute accuracy of 1 LSB at +25°C. However, externally connected offset and gain potentiometers may be used to null these error components to zero. If these adjustments are not used, simply leave the pins open. Adjustment networks should be located physically closed to the DAC82 to minimize signal pickup.

OFFSET ADJUSTMENT

For unipolar operation, apply the digital input code that should give zero volts output and adjust the OFFSET potentiometer for zero volts output. For bipolar operation, apply the digital input code that should give the maximum negative voltage output. Example: If the FULL SCALE RANGE is connected for 20 volts, then the maximum negative voltage output is -10 volts. See Table I for corresponding codes.



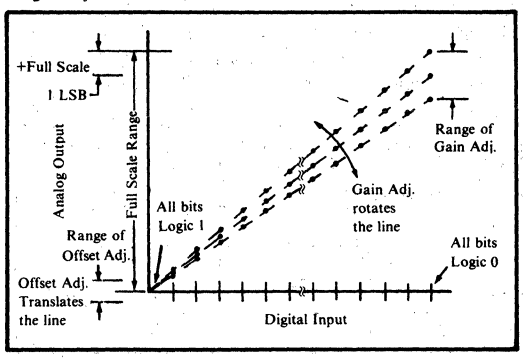
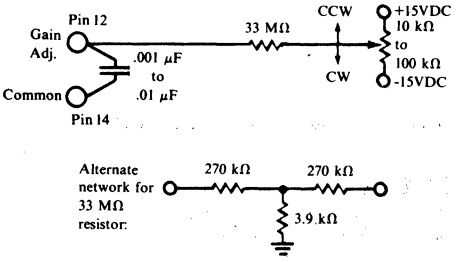


FIGURE 9. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter.

GAIN ADJUSTMENT

For either unipolar or bipolar D/A converters, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. The positive full scale voltages for the DAC82 are given in Table V.



Range of Offset Adjustment: ±0.2% of FSR

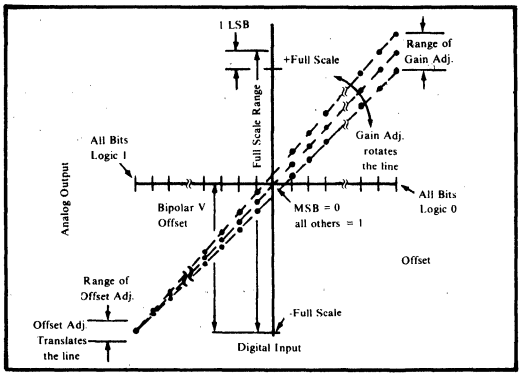


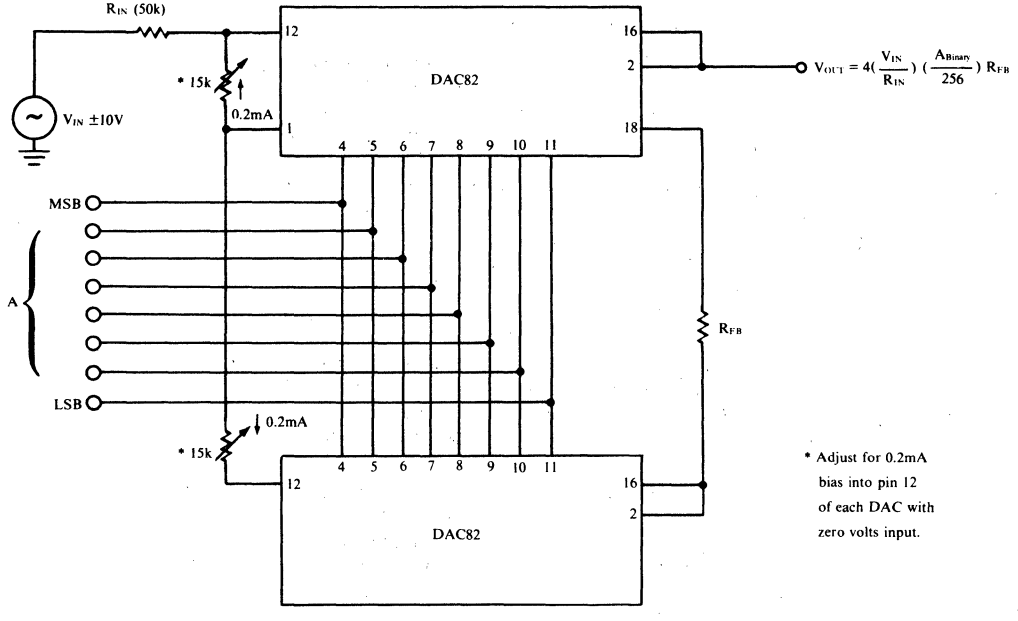
FIGURE 10. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter.

APPLICATIONS

Two DAC82's can be connected as shown to construct a digitally-controlled attenuator which will accept bipolar input voltages. Since the input to the DAC is a summing junction (pin 12), input voltages greater than ±10V can be used if R_{IN} is increased proportionately. The transfer function is:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{4\,R_{FB}}{R_{IN}}\right)\left(\frac{A_{BINARY}}{256}\right)$$

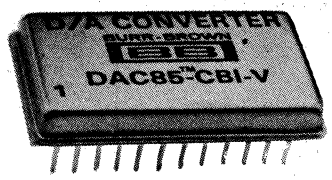
To remove initial gain errors, the two 15k resistors should be adjusted such that 0.2 mA flows into pin 12 of each DAC82 when $V_{IN} = 0$.



DIGITALLY CONTROLLED ATTENUATOR WITH BIPOLAR INPUT

BURR-BROWN®

DAC85



Hybrid Microcircuit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION
- LASER-TRIMMED TO ±1/2LSB LINEARITY
- CURRENT OR VOLTAGE OUTPUT
- FAST SETTLING - 300nsec to ±.01% (Current Output Model)
- HERMETIC DUAL-IN-LINE PACKAGE
- LOW COST

DESCRIPTION

The DAC85 12-bit D/A converter offers quality performance usually found in larger modular units. Housed in a 24-pin dual-in-line metal case, this D/A converter is complete with internal reference and output amplifier and is engineered to preserve the performance normally found only in much larger, higher cost modular units, while providing sealed protection from rugged environments.

Highly stable laser-trimmed thin-film resistors and our Model 4550 quad current switches provide low nonlinearities of ±0.012% over 0°C to 70°C (DAC85C) and ±0.012% over -25°C to +85°C (DAC85 and DAC85LD) operating temperature ranges. Current output models settle to ±0.01% in 300nsec while voltage output models settle to ±0.01% in 5μsec, permitting throughput rates as high as 3MHz for full scale range changes.

The small size of the DAC85 makes it an ideal choice as the heart of your A/D converter design or for applications where space or weight is at a premium, such as CRT displays, aircraft instrumentation and portable instruments. The wide choice of performance models allows you to choose the right unit for your application and budget.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

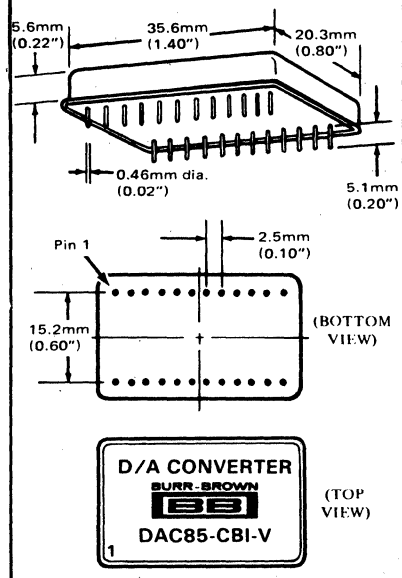
SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	DAC85C		DAC85		DAC85LD	Units
Binary	CBI		CBI		CBI	
Decimal		CCD		CCD		
INPUT						
DIGITAL INPUT						
Resolution	12	3	12	3	12	Bits Digits
Logic Levels (TTL compatible)						
Logic "1"(1)	$+2.4 < e_d < +5.0$ at $+40\mu A$					V
Logic "0"(2)	$0 < e_d < +0.4$ at $-1.6mA$					V
TRANSFER CHARACTERISTICS						
ACCURACY						
Linearity Error @ 25°C (max)	±1/2	±1/4	±1/2	±1/4	±1/2	LSB
0°C to +70°C (max)	±1/2	±1/2				LSB
-25°C to +85°C (max)			±1/2	±1/2	±1/2	LSB
Differential Linearity Error	±1/2					LSB
Gain Error(3)	±0.1					%
Offset Error(3)	±0.05					% of FSR(4)
Minimum Temperature Range for Guaranteed Monotonicity	0 to +70		-25 to +85			°C
DRIFT(5)						
Gain						
0°C to +70°C (max)	±20		±20		±10	ppm/°C
-25°C to +85°C (max)	—		±20		±10	ppm/°C
Offset						
Unipolar 0°C to +70°C	±1					ppm of FSR/°C
-25°C to +85°C			±1		±1	ppm of FSR/°C
Bipolar 0°C to +70°C (max)	±10					ppm of FSR/°C
-25°C to +85°C(max)			±10		±5	ppm of FSR/°C
CONVERSION SPEED						
Voltage Models						
Settling time to ±0.01% of FSR for FSR change						
with 10 kΩ Feedback	5					µsec
with 5 kΩ Feedback	3					µsec
for 1 LSB change	1.5					µsec
Slew Rate	20					V/µsec
Current Models						
Settling time to ±0.01% of FSR for FSR change						
10 to 100 Ω load	300					nsec
1 kΩ load	1					µsec
OUTPUT						
ANALOG OUTPUT						
Voltage Models						
Ranges – CBI Units	±2.5, ±5, ±10, +5, +10					V
CCD Units	+10					V
Output Current (min)	±5					mA
Output Impedance (dc)	0.05					Ω
Current Models						
Ranges	±1, -2					mA
Output Impedance - Bipolar	4.4					kΩ
Unipolar	15					kΩ
Compliance	±2.5					V
Internal Reference Voltage (V_r)	6.3					V
Max. External Current(6)	200					µA
Tempco of Drift (max)	±10	±10	±10	±10	±5	ppm of V_r/°C
POWER SUPPLY SENSITIVITY						
+15V Supply	±0.02					% of FSR/%Vs
-15 and +5V Supplies	±0.002					% of FSR/%Vs
POWER SUPPLY REQUIREMENTS						
Rated Voltage	±15 and +5					V
Range	±14.5 to ±15.5 and +4.75 to +15.5(7)					V
Supply Drain						
±15 V (including 5 mA load)	±25					mA
+5 V	+20					mA
TEMPERATURE RANGE						
Specification	0 to +70		-25 to +85			°C
Operating(double above drift specs)	-25 to +85		-25 to +85			°C
Storage	-55 to +100		-55 to +100			°C

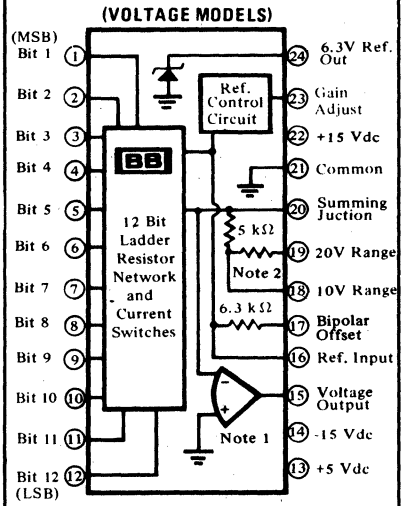
1. Logic "1" current = 40µA max at V_{IN} = +5.0V
2. Logic "0" current = -1.6mA max at V_{IN} = +0.4V
3. Adjustable to zero with external trim potentiometer.
4. FSR means "full scale range" and is 20V for ±10V range. 10V for ±5V range etc.
5. To maintain drift spec internal feedback resistors must be used for current output models.
6. With no degradation of specifications.
7. Operating logic supply at +15.5V increases power dissipation 200mW.

MECHANICAL



CASE: Kovar, Gold or Nickel Plated
MATING CONNECTOR 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
WEIGHT: 8.4 grams (0.3 oz.)

CONNECTION DIAGRAM



Note 1: Amplifier not included in current output models.
Note 2: 3 kΩ for CCD models
5 kΩ for CBI models

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC85 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be user connected for any one of three complementary binary codes: CSB, CTC, or COB.

	DIGITAL INPUT	ANALOG OUTPUT		
	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+1/2 Full Scale	Zero	-Full Scale
	100000000000	Mid Scale -1 LSB	-1 LSB	+Full Scale
	111111111111	Zero	-Full Scale	Zero
CCD Models	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE 1. Digital Input Codes.

ACCURACY

LINEARITY

The linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC85 and DAC-85C is specified over the entire specification temperature ranges. The definition of this specification means that the analog output will not vary by more than ±1/2LSB from an ideal straight line drawn between the end points (all bits ON and all bits OFF) over the specified operating temperature range.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage can change anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

DRIFT

GAIN DRIFT

GAIN DRIFT is a measure of the change in the full scale range analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at -25°C or 0°C, +25°C and +70°C or +85°C for each model and calculating the GAIN ERROR with respect to the 25°C value and dividing by the temperature change. This specification is expressed in ppm/°C.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in the output with all bits OFF (V_{OUT}^{OFF}) over the specified temperature range. V_{OUT}^{OFF} is measured at -25°C or 0°C, +25°C and +70°C or +85°C. The maximum change in OFFSET is referenced to the OFFSET at 25°C divided by the temperature range. This drift is expressed in parts per million of full scale range per °C. (ppm of FSR/°C).

SETTLING TIME

The settling time for each model DAC85 is the total time (including slew time) for the output to settle to within an error band about its final value after a change in the input.

VOLTAGE OUTPUT MODELS

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V and 10V and also for a 1 LSB change. The 1 LSB change is measured at the major carry (0111 ... 11 to 1000 ... 00) since this is the point where the worst case settling time occurs.

CURRENT OUTPUT MODELS

Two settling times are specified for current output models; each specified settling time to ±0.01% of FSR is given for the DAC85 current models connected with two different resistive loads – i.e., 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 ohms to 1800 ohms for output voltage ranges of ±1 volt and 0 to -2 volts. (See Table 4)

COMPLIANCE

The compliance voltage of the DAC85 is the maximum voltage swing allowed on the current output mode in order to maintain the specified accuracy; it is ±2.5 volts for the bipolar current range of ±1.0 mA and is -2.5 volts for the unipolar current range of 0 to -2 mA. The maximum safe voltage swing allowed with no damage to the DAC85 output is ±5 volts for current output models.

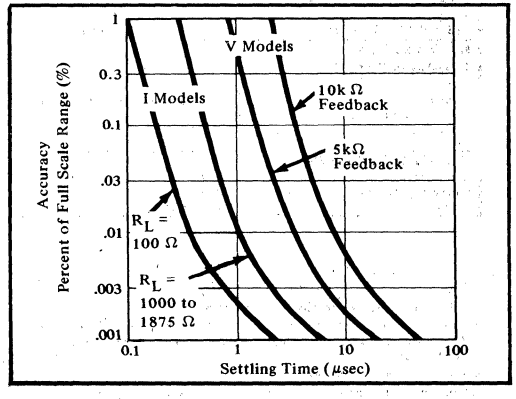


FIGURE 1. Full Scale Range Settling Time vs. Accuracy.

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the +15 volt or -15 volt and +5 power supplies about the nominal power supply voltages. Figure 2 shows Power Supply rejection vs. frequency.

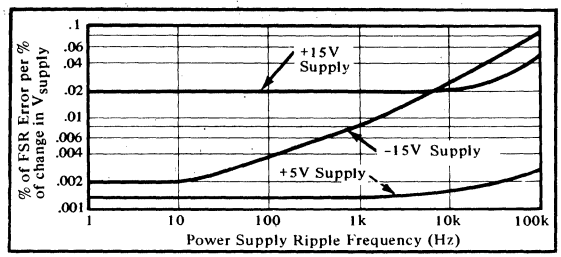


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

REFERENCE SUPPLY

All DAC85 models are supplied with an internal 6.3 volt reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5%, and must be connected to the Reference Input (pin 16) for specified operation.

This reference may also be used externally, but the current drain is limited to 200 μA. An external buffer amplifier is recommended if the DAC85 internal reference will be externally used in order to provide a constant load to the reference supply output.

DAC85

ORDERING INFORMATION

DAC85 XX – XXX – X

- DAC85 XX: 12-Bit D/A Converter Family
  - Example: DAC85-CBI-V DAC85 with voltage output, Binary code and -25°C to +85°C temp. range.
- XX: C = 0 to +70°C Model; LD = Low drift -25°C to +85°C Model; Leave blank for -25°C to +85°C Model
- XXX: INPUT CODE
  - CBI = Complementary 12-bit binary
  - CCD = Complementary 3-digit BCD (not available for DAC85LD
- X: OUTPUT
  - V = Voltage
  - I = Current (not available for LD model)

OPERATING INSTRUCTIONS

DIGITAL INPUT AND ANALOG OUTPUT RELATIONSHIP

Digital Input Codes	Output Range			
	Voltage *		Current	
	0 to +10V	±10V	0 to -2mA	±1mA
Binary (CBI)				
12 bit resolution				
One LSB	+2.44mV	4.88mV	0.488μA	0.488μA
All bits ON	+9.9976V	+9.9951V	−1.9995mA	-0.9995mA
All bits OFF	Zero	−10.000V	Zero	+1.0000mA
Decimal (CCD)				
3 digit resolution				
One LSB	10 mV		1.25μA	
+ FS bits ON	+9.99V†	N/A	−1.249mA	N/A
All bits OFF	Zero		Zero	

TABLF 2. Ideal Output Voltage and Current.

†Normal full scale range with correct codes; output can go to +12 volts if illegal codes are applied.

*To obtain values for other binary (CBI) ranges:

0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

POWER SUPPLY CONNECTIONS

DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC85 and should be tantalum or electrolytic types bypassed with a 0.01 μF ceramic capacitor for best high frequency performance.

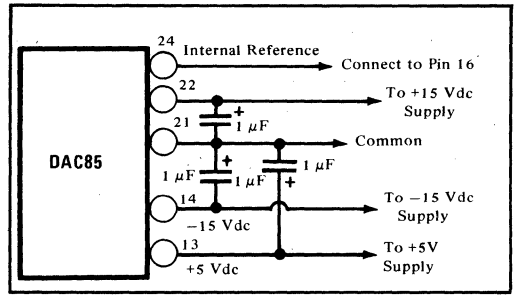


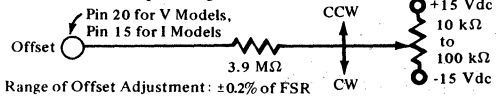
FIGURE 3. Recommended Power Supply Decoupling.

EXTERNAL OFFSET and GAIN ADJUSTMENT

Offset and gain may be trimmed externally by the user with externally connected OFFSET and GAIN potentiometers. If gain and offset adjust circuits are not used, pins 15, 20, and 23 should be connected as described in other sections herein. (Do not ground.) Connection of the potentiometers and the methods of adjutments is as outlined below. Potentiometer resistance values indicated are range of values. Potentiometers should have TCR of 100ppm/°C or less. The 3.9MΩ and 18MΩ resistors can be 20% carbon composition or better. These two resistors should be located close to the DAC85 to prevent signal pickup.

OFFSET ADJUSTMENT

For unipolar (CSB, CCD) D/A converters, apply the digital input code that should give zero volts output and adjust the OFFSET potentiometer for zero volts output. For bipolar (COB, CTC) D/A converters, apply the digital input code that should give the maximum negative voltage output. Example: If the FULL SCALE RANGE is connected for 20 volts, then the maximum negative voltage output is -10 volts. See Table 2 for corresponding codes.



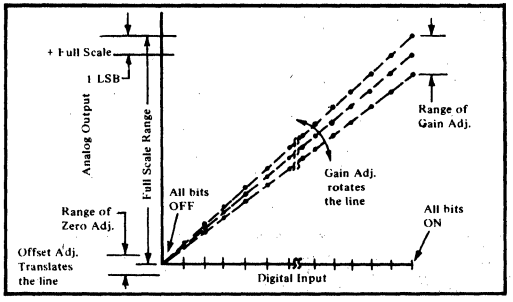
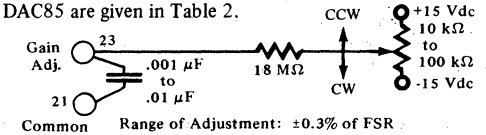


FIGURE 4. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter.

GAIN ADJUSTMENT

For either unipolar or bipolar D/A converters, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. The positive full scale voltages for the DAC85 are given in Table 2.



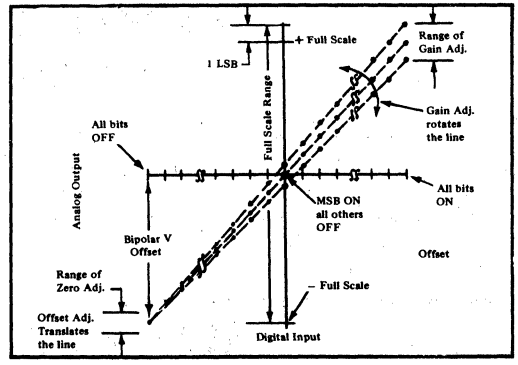


FIGURE 5. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter.

VOLTAGE OUTPUT MODELS

OUTPUT RANGE CONNECTIONS

Internal scaling resistors are provided in the DAC85 to provide a wide range of output voltage range connections. These internal resistors may be connected to provide three bipolar output voltage ranges of ±10, ±5 or ±2.5 volts or two unipolar output voltage ranges of 0 to +5 or 0 to +10 volts. Since these internal scaling resistors are an integral part of the DAC85, gain and offset drift is minimized. Connections for DAC85 output voltage ranges are shown in Table 3.

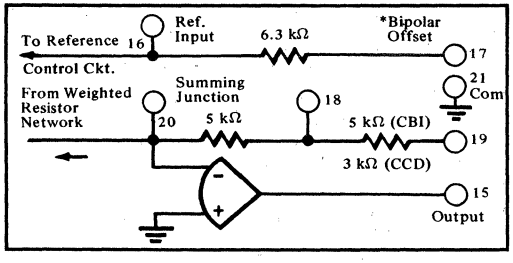


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

*pin 17 not connected for CCD models. The 6.3 kΩ resistor is internally connected to common.

Settling time for these voltage ranges is specified for a full scale range change, and is 5 microseconds for 8 kΩ or 10 kΩ and 3 microseconds for a 5 kΩ feedback resistor.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

TABLE 3. Output Voltage Range Connections – Voltage Model DAC85.

CURRENT OUTPUT MODELS

Internal resistors are provided either for scaling an external op amp to the same voltage ranges as the voltage model DAC85 or for configuring a resistive load to provide two output voltage ranges of ±1 volt or 0 to -2 volts. These internal resistors (R_{LI}) are an integral part of the DAC85 design, and are required to maintain the gain and bipolar offset drift specifications of the DAC85. If the internal resistors are not used, external R_L or R_F resistors should have ±25 ppm/°C or less temperature coefficient to minimize drift.

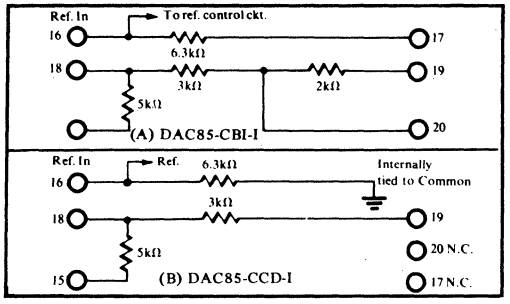


FIGURE 7. Internal Scaling Resistors.

The current model DAC85 equivalent output circuit and resistive scaling network is different from the voltage model DAC85, and is shown in Figure 7 and 8 for reference.

Instructions for using the DAC85-xxx-I with either a resistive load or an external op amp are on the following pages. External R_{LS} or R_{LP} resistors are required to give exactly 0 to -2V or ±1V output range. These resistors should have a TCR of ±100 ppm/°C or less. If these exact output ranges are not required, R_{LS} (or R_{LP}) need not be used as discussed below.

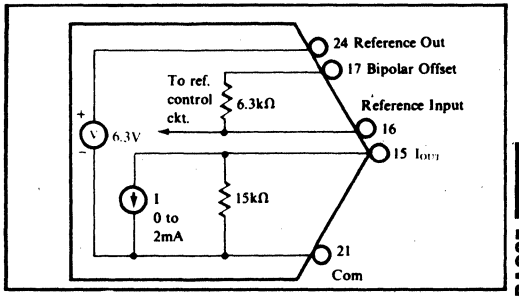


FIGURE 8. DAC85 Current Model Equivalent Output Circuit.

Voltage Output Using Resistive Load

UNIPOLAR

BINARY INPUT CODE (CSB)

A load resistance R_L connected to the output as shown in Figure 9, will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2\text{ mA}\left(\frac{15\text{ k} \times R_L}{15\text{ k} + R_L}\right)$$

where R_L max = 1.36 kΩ
and V_{OUT} max = -2.5 volts

For minimum drift as specified, the internal scaling resistor (R_{LI}) should be connected as shown in Table 4 for the CSB code with a series connected external metal film full scale trim resistor (R_{LS}) to provide a full scale output voltage range of 0 to -2 volts. With R_{LS} = 0, V_{OUT} = -1.82V.

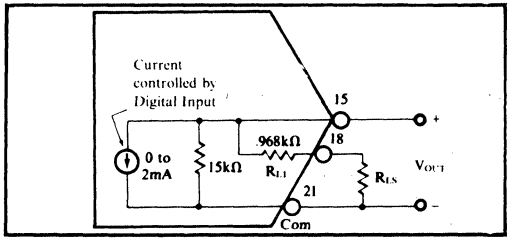


FIGURE 9. Equivalent Circuit DAC85-CBI-I connected for Unipolar Voltage Output with Resistive Load.

BCD INPUT CODE (CCD)

Connect the internal scaling resistors as shown in Table 4, and add an external parallel connected metal film resistor (R_{LP}) as shown in Figure 10 to obtain a 0 to -2 volt full scale output voltage range for CCD input codes. With R_{LP} = ∞, V_{OUT} = -2.08V.

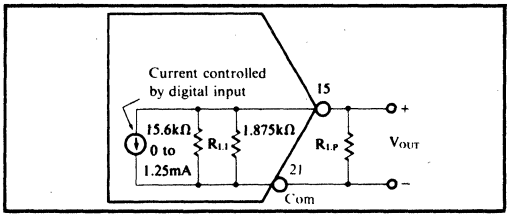


FIGURE 10. DAC85-CCD-I Connected for Voltage Output with Resistive Load.

Input Code	Output Voltage Range	Internal Resistance R_{LI}	1% Metal Film External Resistor R_{LS}	1% Metal Film External Resistor R_{LP}	R_{LI} Connections: Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Reference: Connect Pin 16 to	Bipolar Offset: Connect Pin 17 to	Bipolar Offset R_{LS}	Bipolar Offset R_{LP}
CSB	0 to -2V	0.968 kΩ	105 Ω	N/A	20	19 & R_{LS}	15	24	21 (Com)	Between pin 18 & 21	N/A
CCD	0 to -2V	1.875 kΩ	N/A	36.5 kΩ	19	21 (Com)	N.C.	24	N.C.	N/A	Between pin 15 & 21
COB or CTC	±1V	1.2 kΩ	90.9 Ω	N/A	18	19	R_{LS}	24	15	Between pin 20 & 21	N/A

TABLE 4. DAC85X - XXX - I Resistive Load Connections.

BIPOLAR

COB and CTC INPUT CODES

The equivalent output circuit for a bipolar output voltage range is shown in Figure 11. V_{OUT} is determined by:

$$V_{OUT} = \pm 1 \text{ mA} \times \left(\frac{R_L \times 4.44\text{ k}}{R_L + 4.44\text{ k}} \right)$$

where R_L max = 5.72 kΩ
V_{OUT} max = ±2.5 volts

For minimum drifts (as specified) the internal scaling resistors (R_{LI}) are connected as shown in Table 4 for the COB or CTC codes and an external series connected metal film resistor (R_{LS}) is added to obtain a full scale output voltage range of ±1 volt. With $R_{LS} = 0$, $V_{OUT} = \pm 0.944$V.

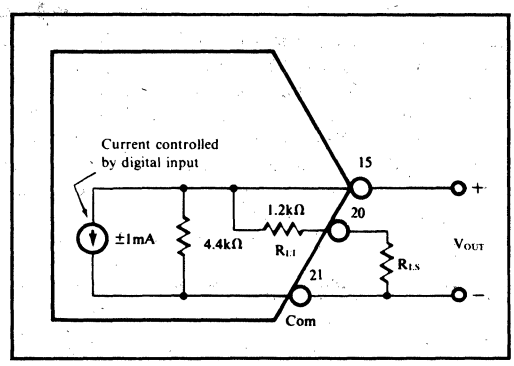


FIGURE 11. DAC85-CBI-I Connected for Bipolar Output Voltage with Resistive Load.

SETTLING TIME

The current output DAC85 models have a specified settling time of 300 nanoseconds with a 100 ohm load. Settling time increases as the load resistance increases due to the RC time constant of R_L and the summing junction capacitance.

Driving an External Op Amp

UNIPOLAR or BIPOLAR – Up to 20V Output Range

The current model DAC85 will drive the summing junction of an op amp (the op amp being used as a current to voltage converter) to produce an output voltage (see Figure 12):

$$V_{OUT} = -I \times R_F$$

where I_{OUT} is the DAC85 output current and R_F is the feedback resistor. Use of the internal feedback resistors of the DAC85 will provide the same output voltage ranges as the voltage model DAC85. Table 5 must be used for connecting the external op amp to obtain the desired output voltage range.

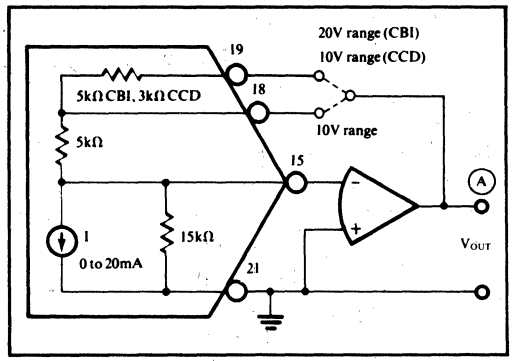


FIGURE 12. External Op Amp - Using Internal Feedback Resistors.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	Ⓐ	24

TABLE 5. Voltage Ranges of Current Output DAC85 with External Op Amp.

OUTPUTS LARGER THAN 20 VOLT RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1 mA for bipolar voltage ranges, and -2 mA for unipolar voltage ranges (see Figure 13). Use protection diodes when a high voltage op amp is used.

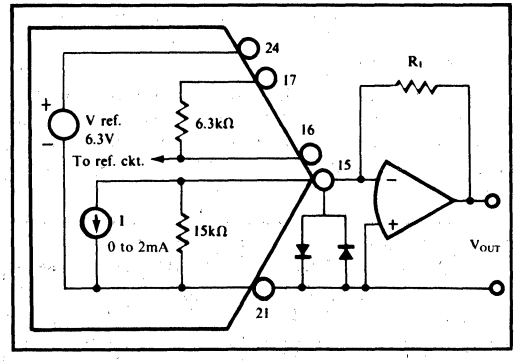


FIGURE 13. External Op Amp - Using External Feedback Resistors.

BUILDING AN A/D CONVERTER

The small size and good performance of the DAC85 makes it an excellent component for building A/D converters. The most popular medium speed (1 μsec/bit to 10 μsec/bit) A/D converter is the successive approximations type, in which the digital output equivalent of the analog input is formed by comparing a programmed D/A converter output with the analog input. The digital output is successively compared one bit at a time until the final comparison is within ± 1/2 bit of the resolution of the D/A converter.

The conversion speed of a successive approximation A/D converter constructed around a DAC85 is determined by the settling speed to ±1/2 LSB, the speed of the comparator, and the switching speed of the successive approximations logic. The A/D converter shown in Figure 14 will convert at speeds in excess of 60 kHz for 12 bits and near 80 kHz for 10 bits.

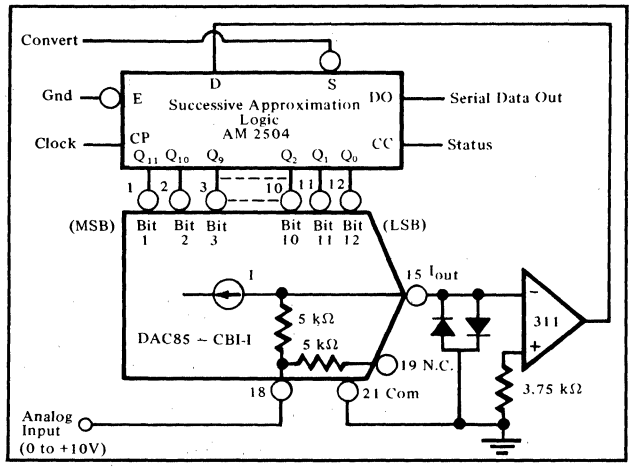
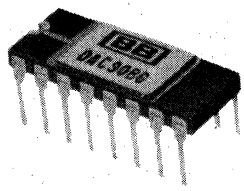


FIGURE 14. 12-Bit Successive Approximation A/D Converter.

BURR-BROWN®

DAC90

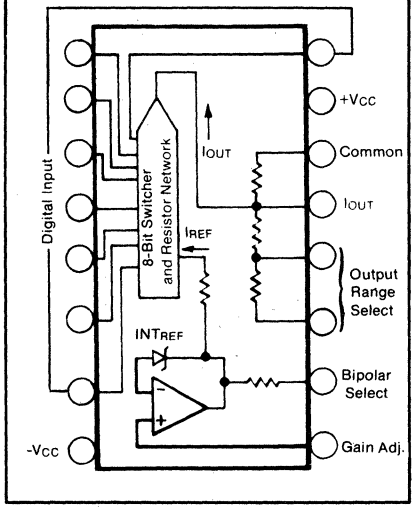


Monolithic Microcircuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 8-BIT RESOLUTION
- CURRENT OUTPUT
- FAST SETTLING
  200nsec to ±0.2%
- HERMETIC DUAL-IN-LINE PACKAGE
- LOW COST
- INTERNAL REFERENCE AND SCALING RESISTORS

FUNCTIONAL DIAGRAM



DESCRIPTION

The DAC90 is an 8-bit D/A Converter that offers performance usually found only in larger, modular units. Housed in a 16-pin ceramic dual-in-line package, the DAC90 is complete with its own internal reference and scaling resistors.

Two versions are available: the DAC90BG (-25°C to +85°C) and DAC90SG (-55°C to +125°C) both offer ±0.2% nonlinearity over their respective temperature ranges. Settling time to ±0.2% is typically 200nsec.

The small size of the DAC90 makes it an ideal choice as the heart of your A/D converter design or for applications where space or weight is at premium, such as CRT displays, aircraft instrumentation, and portable instruments.

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SPECIFICATIONS

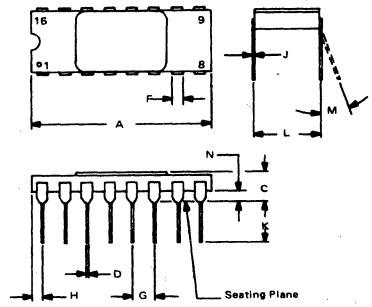
ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	DAC90BG	DAC90SG	UNITS
DIGITAL INPUT			
Resolution	8	8	Bits
Logic Levels (TTL-compatible)			
Logic "1"	+2< e_d < +5.5 at +40μA		V
Logic "0"	0< e_d < +0.8 at -1.0mA		V
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error at 25°C, max	±1/2	±1/2	LSB
-25°C to +85°C, max	±1/2		LSB
-55°C to +125°C, max		±1/2	LSB
Differential Linearity Error	±1/2	±1/2	LSB
Gain Error(1)	5	5	%
Offset Error(1)	1	1	% of FSR(2)
Minimum Temperature Range for Guaranteed Monotonicity	-25 to +85	-55 to +125	°C
DRIFT(3)			
Gain			
-25°C to +85°C	±50		ppm/°C
-55°C to +125°C		±50	ppm/°C
Offset			
Unipolar			
-25°C to +85°C	±1		ppm of FSR/°C
-55°C to +125°C		±1	ppm of FSR/°C
Bipolar			
-25°C to +85°C	±50		ppm of FSR/°C
-55°C to +125°C		±50	ppm of FSR/°C
CONVERSION SPEED			
Settling time to ±0.2% of FSR for FSR change			
10Ω to 100Ω load	200		nsec
1kΩ load	300		nsec
ANALOG OUTPUT			
Ranges	±1, 0 to -2		mA
Output Impedance - Bipolar	1.8		kΩ
Unipolar	2		kΩ
Compliance	-4 to +4		V
Internal Reference Voltage (V_r)	7.6		V
Tempco of Drift	±50	±50	ppm of V_r/°C
POWER SUPPLY SENSITIVITY			
+15VDC	±0.02%		% of FSR/%V_S
-15VDC	±0.002		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15		VDC
Range	±14.5 to ±15.5		VDC
Supply Drain ±15VDC	7		mA
TEMPERATURE RANGE			
Specification	-25 to +85	-55 to +125	°C
Operating	-55 to +125	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C

NOTES:
1. Adjustable to zero with external trim potentiometer.
2. FSR means "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.
3. To maintain drift spec internal feedback resistors must be used.

MECHANICAL

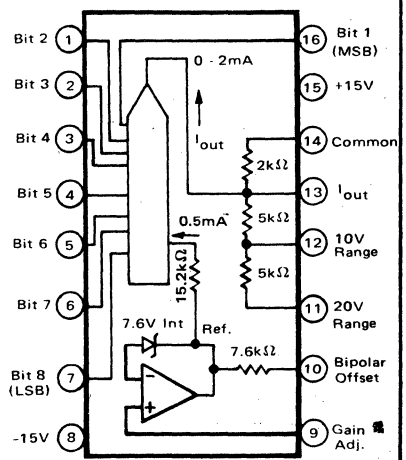


NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

CASE: Ceramic, with hermetic seal
HERMETICITY: Conforms to MIL-STD-883 Method 1014, Condition C, Step 1 Fluorocarbon Gross leak and Condition A Helium), 5 x 10-7 cc/sec (fine leak).

CONNECTION DIAGRAM



4. Connect to ground if gain adjust circuit is not used.

DAC90

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC90 accepts digital inputs in complementary binary (CBI) format and may be connected for complementary straight binary (CSB) or complementary offset binary (COB) operation (see Table I). By using one external inverter, the user can operate the DAC90 in the complementary two's complement (CTC) mode.

TABLE I. Digital Input and Analog Output Relationship.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
	0 to +10V	±10V	0 to -2mA	±1mA
MSB LSB				
00000000	+9.961V	+9.922V	-1.992mA	-0.992mA
01111111	+5.000V	0.000V	-1.000mA	0.0000mA
10000000	+4.961V	-78.12mV	-0.99mA	+7.81μA
11111111	0.000V	-10.000V	0.000mA	+1.000mA
one LSB	39.06mV	78.12mV	7.81μA	7.81μA

* Requires external amplifier. To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

ACCURACY

Linearity

The LINEARITY of a D/A converter is the true measure of its performance. The DAC90 analog output will not vary by more than ±1/2LSB from an ideal straight line drawn between the end points (all 1's and all 0's) over the specified temperature range.

Differential Linearity

DIFFERENTIAL LINEARITY error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A DIFFERENTIAL LINEARITY error specification of ±1/2LSB means that the output voltage can change anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent digital state to the next.

DRIFT

Gain Drift

GAIN DRIFT is a measure of the change in the analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at the high and low temperature extremes and at 25°C for each model, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change.

Offset Drift

OFFSET DRIFT is a measure of the actual change in output voltage (using an external amplifier) at zero volts output over the specified temperature range. The offset voltage is measured at the temperature extremes, and the maximum change referenced to 25°C is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

SETTLING TIME is the time required for the output to enter and remain in an error band equal to ±0.2% of full scale range measured from the time the digital input is changed. Typical settling time values for full scale changes are a function of the load resistor and are shown in the figure below.

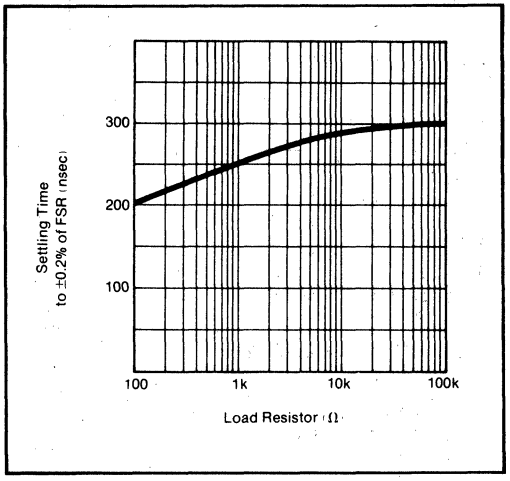


FIGURE 1. Settling Time for FSR Change vs Load.

Compliance

The COMPLIANCE VOLTAGE of the DAC90 is the maximum voltage swing allowed on the current output in order to maintain the specified accuracy; it is -4.0V to +4.0V for the unipolar and bipolar current ranges. The maximum safe voltage swing allowed with no damage to the DAC90 output is -4.0B to +15.0V

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D A converter output. It is defined as a percent of FSR/ percent of change in either the +15VDC or -15VDC power supplies about the nominal power supply voltages. Figure 2 shows power supply rejection vs frequency.

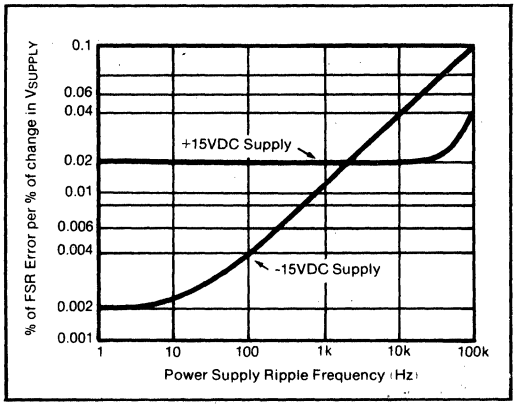


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Decoupling

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC90 and should be tantalum or electrolytic types bypassed with a 0.01μF ceramic capacitor for best high frequency performance.

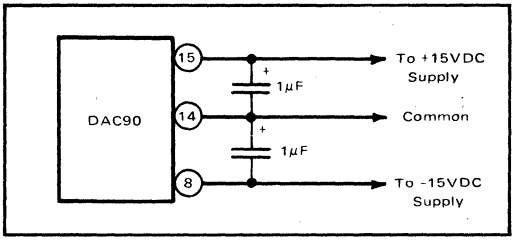


FIGURE 3. Recommended Power Supply Decoupling

OPERATION IN THE CURRENT OUTPUT MODE

In the current output mode, the DAC90 provides a unipolar output current of 0 to -2mA and a bipolar output current of ±1mA. Refer to Figure 4 and Table II for proper connections. In applications requiring the use of the DAC90 in the current output mode, such as an A D converter, the internal scaling resistors should be used to generate currents corresponding to analog input voltages.

TABLE II. Connections for Current Output Mode.

Output Range	Connect Pin (13) to:
0 to -2mA	N.C.
±1mA	Pin 10

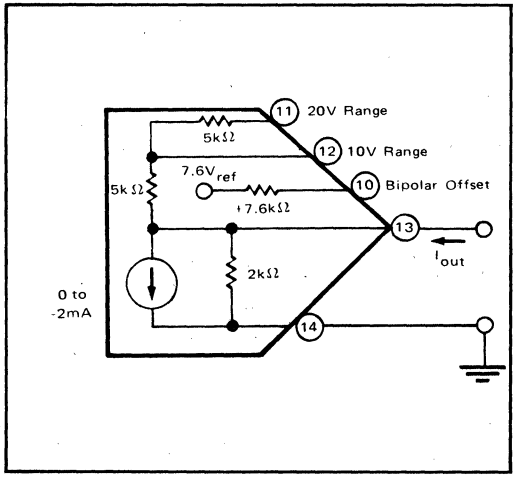


FIGURE 4. Current Output Mode Connection Diagram.

VOLTAGE OUTPUT using an EXTERNAL OP AMP

UNIPOLAR OR BIPOLAR OPERATION

The DAC90 will drive the summing junction of an op amp (the op amp being used as a current-to-voltage converter) to produce and output voltage.

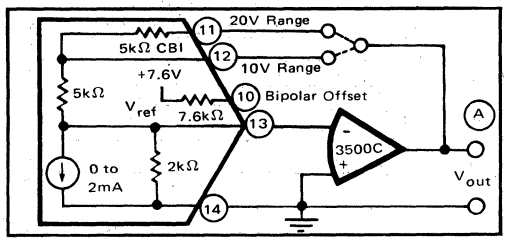


FIGURE 5. External Op Amp Using Internal Feedback Resistors.

$$V_{OUT} = -I \times R_F$$

where I_{OUT} is the DAC90 output current and R_F is the feedback resistor. Refer to Table III and Figure 5.

TABLE III. Voltage Ranges of Current Output DAC90 with External Op Amp.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin (13) to
±10V	COB	11	10
±5V	COB	12	10
±2.5V	COB	12	10,11
0 to +10V	CSB	12	N.C.
0 to +5V	CSB	12	11

EXTERNAL OFFSET and GAIN ADJUSTMENT

Initial offset and gain errors may be trimmed by the user with externally connected OFFSET and GAIN potentiometers and an operational amplifier. Refer to Figures 5 and 6 for proper connections. The adjustment procedures are described below. Potentiometer resistances are shown as a range of values and should have a temperature drift coefficient of 100ppm °C or less. The trimming networks should be located as close to the DAC90 as possible to minimize noise pickup. The ceramic capacitor shown in Figure 6 will further reduce noise pickup at the gain adjust point.

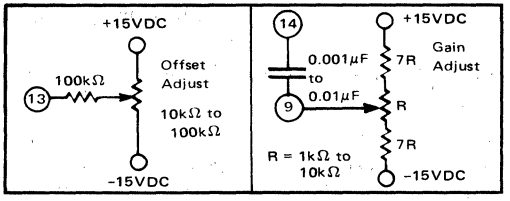


FIGURE 6. Connections for OFFSET and GAIN Adjustment.

OFFSET ADJUSTMENT

Offset adjustment should be made prior to gain adjustment. Connect the unit as shown in Figure 5 for the desired output range and add the offset adjust network shown in Figure 6. Offset adjustment is the same procedure for either bipolar or unipolar operation. Apply the digital input code which should give zero volts output and adjust the offset potentiometer for zero volts output. See Table I for the corresponding codes.

GAIN ADJUSTMENT

The gain adjust procedure is the same for either bipolar or unipolar operation. An external amplifier should be connected as shown in Figure 5. Connect the unit for the desired output range and add the gain adjust network shown in Figure 6. Apply the digital input code which should give the maximum positive output voltage and adjust the gain potentiometer for the correct output. Refer to Table I for the corresponding codes.

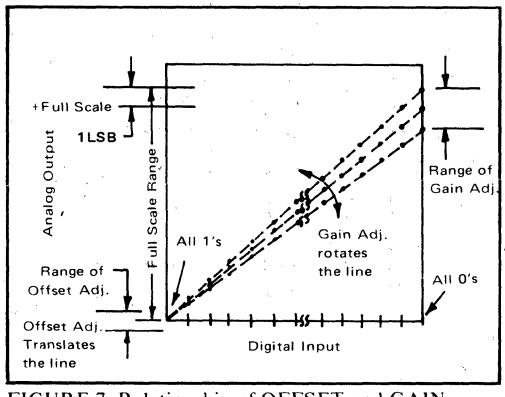


FIGURE 7. Relationship of OFFSET and GAIN Adjustment for a UNIPOLAR D/A Converter.

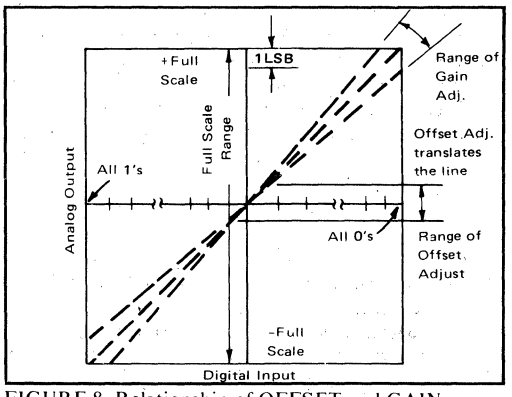


FIGURE 8. Relationship of OFFSET and GAIN Adjustments for BIPOLAR D A Converter.

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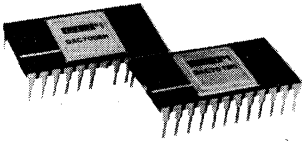


DAC700/702
DAC701/703

Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

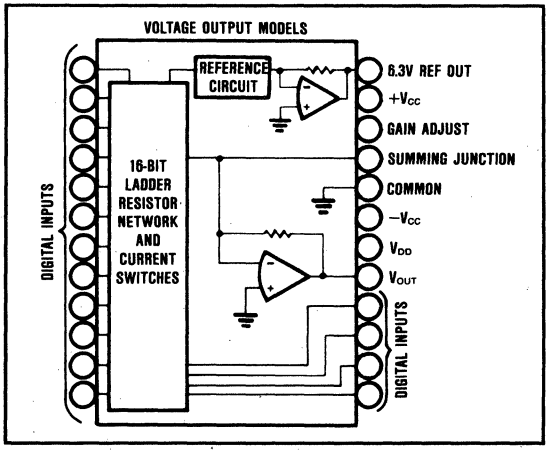
- MONOLITHIC CONSTRUCTION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY:
  Linearity Error: ±0.003% of FSR max (BH, KH models)
  Differential Linearity Error: ±0.006% of FSR max (BH, KH models)
- MONOTONIC (at 14 bits) OVER FULL SPEC TEMPERATURE RANGE (BH, KH models)
- PIN-COMPATIBLE WITH DAC70, DAC71, DAC72
- LOW COST

DESCRIPTION

This is another industry first from Burr-Brown—a complete 16-bit digital-to-analog converter that includes a precision buried-zener voltage reference and a low-noise, fast-settling output operational amplifier (DAC701/703), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range (BH and KH grades) but also a maximum end-point linearity error of ±0.003% of Full Scale Range (BH and KH grades). Total full scale gain drift is limited to ±15ppm/°C maximum (BH grade).

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs are 0 to +10V (DAC701), ±10V (DAC703), 0 to −2mA (DAC700) and ±1mA (DAC702).

This D/A family is pin-compatible with the voltage and current output DAC71 and DAC72 model families. The DAC700 and DAC702 are also pin-compatible with the DAC70 model family. These D/A converters are packaged in 24-pin ceramic side-brazed packages that are hermetically sealed.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC700/701/702/703BH			DAC700/701/702/703KH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT							
DIGITAL INPUT							
Resolution			16			*	Bits
Digital Inputs[1]: V_{IH}	+2.4		$+V_{CC}$	*		*	V
V_{IL}	−1.0		+0.8	*		*	V
I_{IH}, V_I = +2.7V			+40				µA
I_{IL}, V_I = +0.4V		−0.35	−0.5		*	*	mA
TRANSFER CHARACTERISTICS							
ACCURACY[2]							[3]
Linearity Error[4]		±0.0015	±0.003		*	*	% of FSR
Differential Linearity Error[4]		±0.003	±0.006		*	*	% of FSR
Differential Linearity Error[4]							
at Bipolar Zero (DAC702/703)		±0.0015	±0.003		±0.003	±0.006	% of FSR
Gain Error[5]		±0.05	±0.10		±0.07	±0.15	%
Zero Error[5][6]		±0.05	±0.1		*	*	% of FSR
Monotonicity Over Spec. Temp. Range	14			14			Bits
DRIFT[2]							
(over specification temperature range)							
Total Error Over Temp. Range (all models)[7]		±0.05	±0.10		±0.08	±0.15	% of FSR
Total Full Scale Drift: DAC700/701		±8.5	±18		±10	±30	ppm of FSR/°C
DAC702/703		±7	±15		±10	±25	ppm of FSR/°C
Gain Drift (all models)		±7	±15		±10	±25	ppm/°C
Zero Drift: DAC700/701		±1.5	±3		±2.5	±5	ppm of FSR/°C
DAC702/703		±4	±10		±5	±12	ppm of FSR/°C
Differential Linearity Over Temp.[4]			+0.009, −0.006			*	% of FSR
Linearity Error Over Temp.[4]			±0.006			*	% of FSR
SETTLING TIME (to ±0.003% of FSR)[8]							
DAC701/703 (V_{OUT} models)							
Full Scale Step, 2kΩ load		4	8		*	*	µsec
1LSB Step at Worst Case Code[9]		2.5	4		*	*	µsec
Slew Rate		10			*		V/µsec
DAC700/702 (I_{OUT} Models)							
Full Scale Step (2mA), 10Ω to 100Ω load		350			*		nsec
1kΩ load		1			*		µsec
OUTPUT							
VOLTAGE OUTPUT MODELS							
DAC701 (CSB Code)		0 to +10			*		V
DAC703 (COB Code)		±10			*		V
Output Current	±5			*			mA
Output Impedance		0.15			*		Ω
Short Circuit to Common Duration		Indefinite			*		
CURRENT OUTPUT MODELS							
DAC700 (CSB Code)[10]		0 to −2		*	*	*	mA
Output Impedance[10]		4.0			*		kΩ
DAC702 (COB Code)[10]		±1		*	*	*	mA
Output Impedance[10]		2.45			*		kΩ
Compliance Voltage		±2.5		*		*	V
REFERENCE VOLTAGE							
Voltage	+6.24	+6.30	+6.36	+6.0	+6.3	+6.6	V
Source Current Available							
for External Loads	+1.5	+2.5		*	*		mA
Temperature Coefficient		±10	±15		*	±25	ppm/°C
Short Circuit to Common Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	13.5	15	16.5	*	*	*	V
$-V_{CC}$	13.5	15	16.5	*	*	*	V
V_{DD}	+4.5	+5	+16.5	*	*	*	V
Current (no load)							
DAC700/702 (I_{OUT} models): $+V_{CC}$		+10	+25		*	*	mA
$-V_{CC}$		−13	−25		*	*	mA
V_{DD}		+4	+8		*	*	mA
DAC701/703 (V_{OUT} models): $+V_{CC}$		+16	+30		*	*	mA
$-V_{CC}$		−18	−30		*	*	mA
V_{DD}		+4	+8		*	*	mA

ELECTRICAL [CONT]

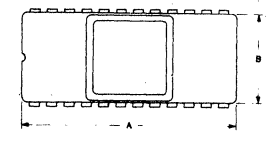
MODEL	DAC700/701/702/703BH			DAC700/701/702/703KH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY REQUIREMENTS [CONT]							
Power Dissipation (V_{DD} = +5.0V)[11]							
DAC700/702		365	630		*	790	mW
DAC701/703		530	780		*	940	mW
Power Supply Rejection: $+V_{CC}$		±0.0015	±0.003		*	±0.006	% of FSR/%V_{CC}
$-V_{CC}$		±0.0015	±0.003		*	±0.006	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*	% of FSR/%V_{DD}
TEMPERATURE RANGE							
Specification	−25		+85	0		+70	°C
Storage	−60		+150	*		*	°C

*Specification same as model to the left.

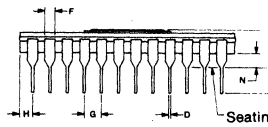
NOTES:

1. Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. As logic "0" and logic "1" inputs vary over 0V to +0.8V and +2.4V to +10V respectively, the change in the D/A converter output voltage will not exceed ±0.003% of FSR for the BH grade and ±0.006% of FSR for the KH grade.
2. DAC700 and DAC702 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time.
3. FSR means Full Scale Range and is 20V for the ±10V range (DAC703), 10V for the 0 to +10V range (DAC701). FSR is 2mA for the ±1mA range (DAC700) and the 0 to +2mA range (DAC702).
4. ±0.0015% of Full Scale Range is equivalent to 1LSB in 16-bit resolution. ±0.003% of Full Scale Range is equivalent to 1LSB in 15-bit resolution. ±0.006% of Full Scale Range is equivalent to 1LSB in 14-bit resolution.
5. Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point.
6. Error at input code $FFFF_H$ for DAC700 and DAC701, $7FFF_H$ for DAC702 and DAC703.
7. With gain and zero errors adjusted to zero at +25°C.
8. Maximum represents the 3σ limit. Not 100% tested for this parameter.
9. At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.
10. Tolerance on output impedance and output current is ±30%.
11. Power dissipation is an additional 40mW when V_{DD} is operated at +15V.

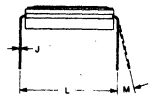
MECHANICAL



NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



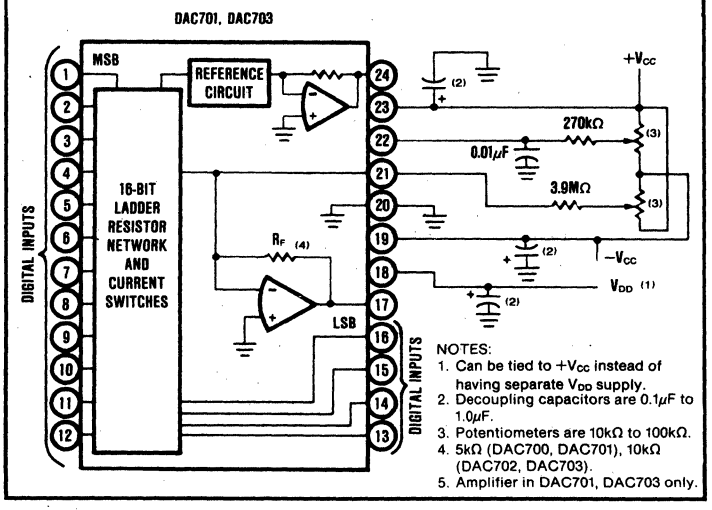
Seating Plane



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.237	1.263	31.42	32.08
B	.514	.526	13.06	13.36
C	.120	.200	3.05	5.08
D	.016	.020	0.41	0.51
F	.050	.070	1.27	1.78
G	.100 BASIC		2.54 BASIC	
H	.065	.085	1.65	2.16
J	.009	.012	0.20	0.30
K	.100	.200	2.54	5.08
L	.600 BASIC		15.24 BASIC	
M	—	15°	—	15°
N	.035	.055	0.89	1.40

CASE: Ceramic, hermetic
MATING CONNECTOR: 0245MC
WEIGHT: 9.2 grams (0.32 oz.)

CONNECTION DIAGRAM



NOTES:
1. Can be tied to $+V_{CC}$ instead of having separate V_{DD} supply.
2. Decoupling capacitors are 0.1μF to 1.0μF.
3. Potentiometers are 10kΩ to 100kΩ.
4. 5kΩ (DAC700, DAC701), 10kΩ (DAC702, DAC703).
5. Amplifier in DAC701, DAC703 only.

PIN ASSIGNMENTS

Pin #	DAC700/702	DAC701/703
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	$R_{FEEDBACK}$	V_{OUT}
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	I_{OUT}	Summing Junction (Zero Adjust)
22	Gain Adjust	Gain Adjust
23	$+V_{CC}$	$+V_{CC}$
24	+6.3V Reference Output	+6.3V Reference Output

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to Common	0V, +18V
$+V_{CC}$ to Common	0V, +18V
$-V_{CC}$ to Common	0V, −18V
Digital Data Inputs (pins 1-16) to Common	−1V, +18V
Reference Out (pin 24) to Common	Indefinite Short to Common
External Voltage Applied to R_F (pin 21, DAC700/702)	±18V
External Voltage Applied to D/A Output (pin 17, DAC701/703)	−5V to +5V
V_{OUT} (pin 17, DAC701/703)	Indefinite Short to Common
Power Dissipation	1000mW
Storage Temperature	−60°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC700/701/702/703 accept complementary digital input codes in either binary format (CSB, Unipolar or COB, Bipolar). The COB models DAC702/703 may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output		
	DAC700/701 Complementary Straight Binary (CSB)	DAC702/703 Complementary Offset Binary (COB)	DAC702/703 Complementary Two's Complement (CTC)*
0000_H	+ Full Scale	+ Full Scale	−1LSB
$7FFF_H$	+1/2 Full Scale	Bipolar Zero	− Full Scale
8000_H	+1/2 Full Scale −1LSB	−1LSB	+ Full Scale
$FFFF_H$	Zero	− Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.006% for 14-bit resolution) ensures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC700/701/702/703 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade. Gain drift is established by: (1) testing the end point differences for each D/A at t_{min}, +25°C and t_{max}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with $FFFF_H$ (DAC700 and DAC701) applied to the digital inputs over the specified temperature range. For the bipolar models, zero is measured at $7FFF_H$ (bipolar zero) applied to the digital inputs. This code corresponds to zero volts (DAC703) or zero milliamps (DAC702) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (DAC703) or 10V (DAC701) and a 1LSB change at the "major carry," the point at which the

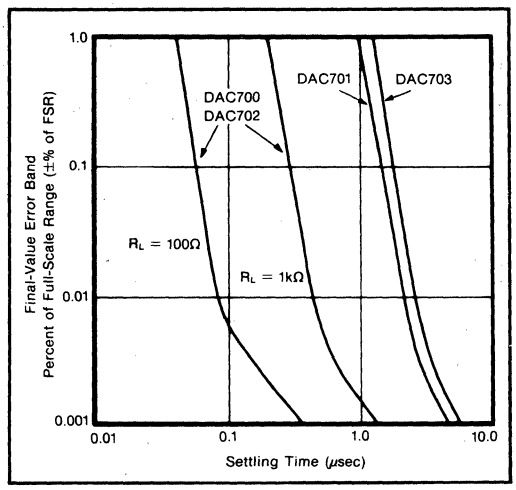


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

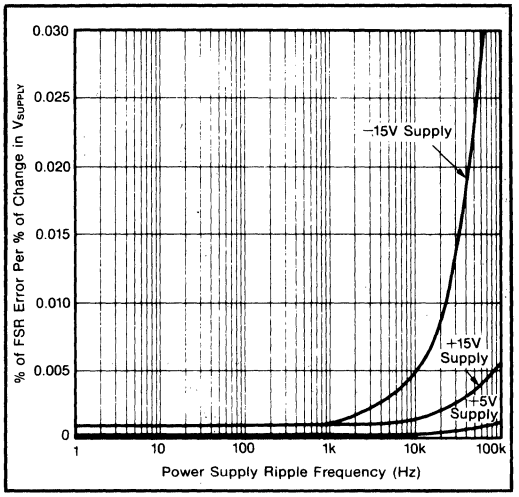


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin with the DAC still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

REFERENCE SUPPLY

All models have an internal low-noise +6.3V reference voltage derived from an on-chip buried zener diode. This reference voltage, available at pin 24, has a tolerance of ±5% (KH models) and ±1% (BH models). A minimum of 1.5mA is available for external loads. Since the output impedance of the reference output is typically 1Ω, the external load should remain constant.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the Bipolar Offset (connected internally to the reference) from load variations.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO GAIN AND ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor should be connected from GAIN ADJUST (pin 22) to COMMON to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

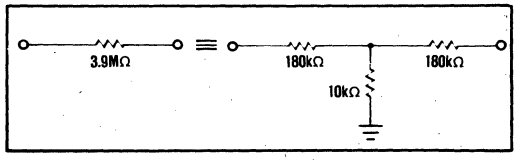


FIGURE 3. Equivalent Resistances.

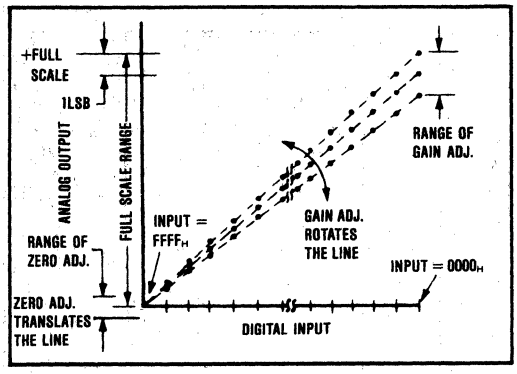


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC700 and DAC701.

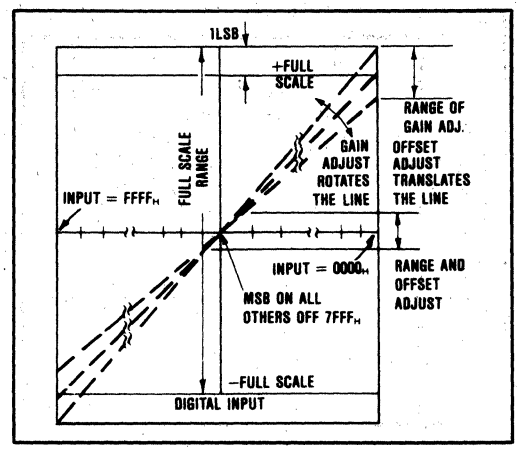


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A converters, DAC702 and DAC703.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at COMMON (pin 20), and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than

TABLE II. Digital Input and Analog Output Relationships.

VOLTAGE OUTPUT MODELS						
	Analog Output					
	DAC701 Unipolar			DAC703 Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μV)	153	305	610	305	610	1224
0000$_H$ (V)	+9.99985	+9.99969	+9.99939	+9.99960	+9.99939	+9.99878
FFFF$_H$ (V)	0	0	0	–10.0000	–10.0000	–10.0000
CURRENT OUTPUT MODELS						
	Analog Output					
	DAC700 Unipolar			DAC702 Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μA)	0.031	0.061	0.122	0.031	0.061	0.122
0000$_H$ (mA)	–1.99997	–1.99994	–1.99988	–0.99997	–0.99994	–0.99988
FFFF$_H$ (mA)	0	0	0	+1.00000	+1.00000	+1.00000

0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at pin 20. Sensing the output voltage at the system ground point is permissible with the DAC700 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from pin 20. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times 2mA$) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.

Figures 7 and 8 show two methods of connecting the current output models (DAC700 or DAC702) with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is

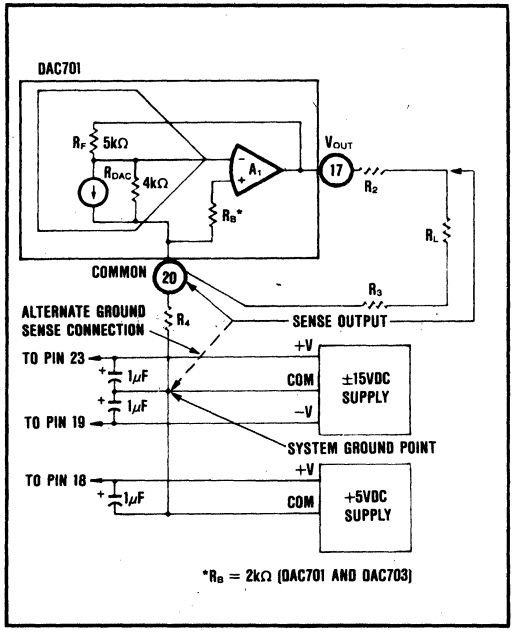
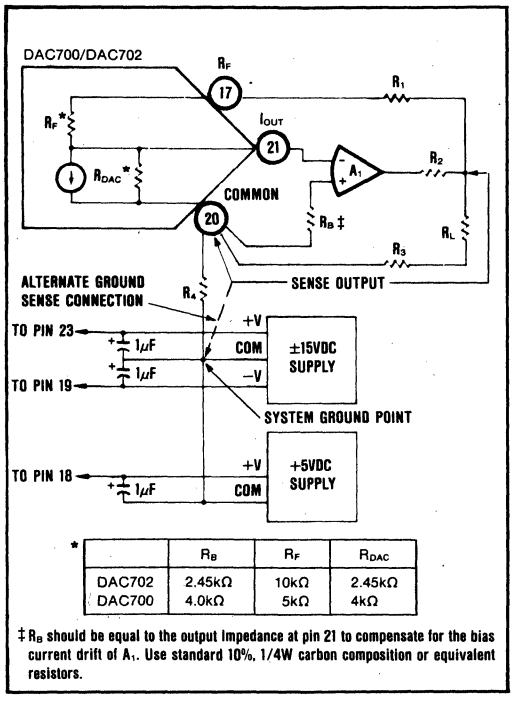


FIGURE 6. Output Circuit for Voltage Models.

independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

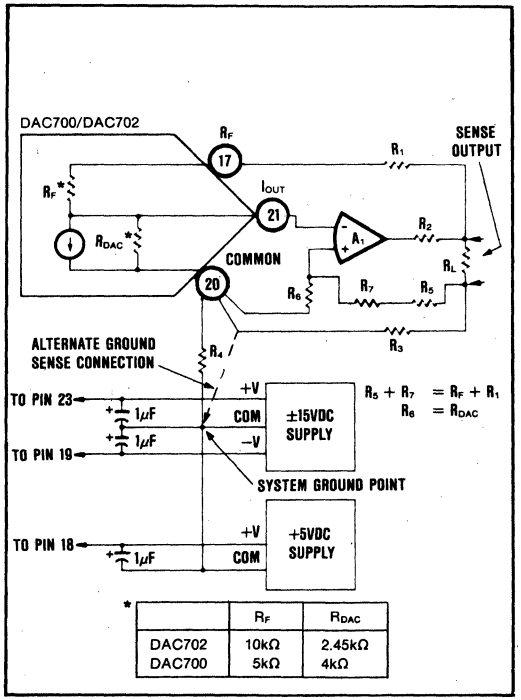
If the output cannot be sensed at COMMON (pin 20), or the system ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be



*	R_B	R_F	R_{DAC}
DAC702	2.45kΩ	10kΩ	2.45kΩ
DAC700	4.0kΩ	5kΩ	4kΩ

‡R_B should be equal to the output impedance at pin 21 to compensate for the bias current drift of A_1. Use standard 10%, 1/4W carbon composition or equivalent resistors.

FIGURE 7. Preferred External Op Amp Configuration.



*	R_F	R_{DAC}
DAC702	10kΩ	2.45kΩ
DAC700	5kΩ	4kΩ

FIGURE 8. Differential Sensing Output Op Amp Configuration.

adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

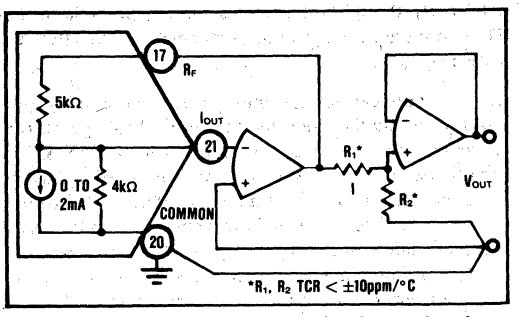


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT D/A's

DAC700 and DAC702 are current output devices and will drive the summing junction of an op amp to produce an output voltage as shown in Figure 9. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

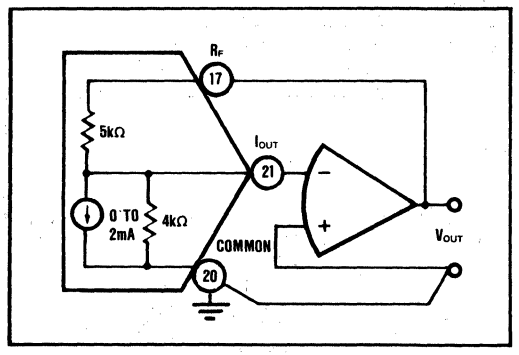


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

DAC700 or DAC702 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±50ppm/°C. The resistors in the DAC700 and DAC702 ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 10.

OUTPUTS LARGER THAN 20-VOLT RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 11). Use protection diodes as shown when a high voltage op amp is used.

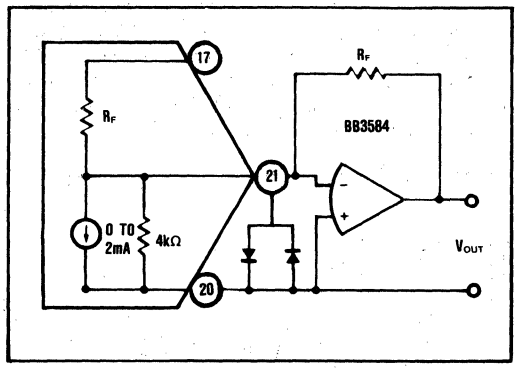
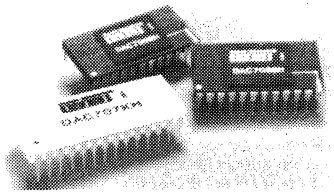


FIGURE 11. External Op Amp Using External Feedback Resistors.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC700KH	Current Output, 0 to −2mA, 0°C to +70°C
DAC700BH	Current Output, 0 to −2mA, −25°C to +85°C
DAC701KH	Voltage Output, 0 to +10V, 0°C to +70°C
DAC701BH	Voltage Output, 0 to +10V, −25°C to +85°C
DAC702KH	Current Output, ±1mA, 0°C to +70°C
DAC702BH	Current Output, ±1mA, −25°C to +85°C
DAC703KH	Voltage Output, ±10V, 0°C to +70°C
DAC703BH	Voltage Output, ±10V, −25°C to +85°C

BURR-BROWN®



DAC706/707
DAC708/709

Microprocessor-Compatible 16-BIT DIGITAL-TO-ANALOG CONVERTERS

FEATURES

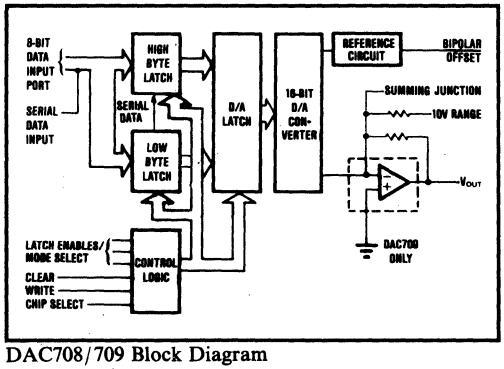
- TWO-CHIP CONSTRUCTION
- HIGH-SPEED 16-BIT PARALLEL, 8-BIT (BYTE) PARALLEL, AND SERIAL INPUT MODES
- DOUBLE-BUFFERED INPUT REGISTER CONFIGURATION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY:
  Linearity Error ±0.003% of FSR max
  Differential Linearity Error ±0.006% of FSR max
- MONOTONIC (TO 14 BITS) OVER SPECIFIED TEMPERATURE RANGE
- HERMETICALLY SEALED

DESCRIPTION

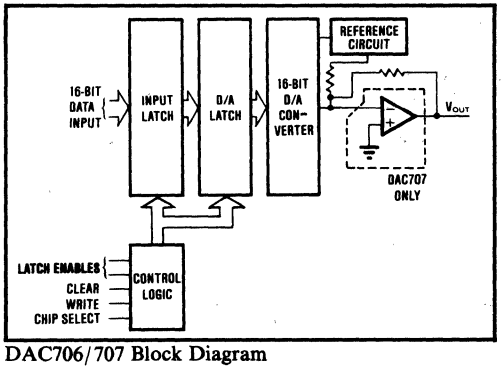
The DAC708 and DAC709 are 16-bit D/A converters designed to interface to an 8-bit microprocessor bus. 16-bit data is loaded in two successive 8-bit bytes into parallel 8-bit latches before being transferred into the D/A latch. The DAC708 and DAC709 have current and voltage outputs respectively and are in 24-pin dual-wide hermetic DIPs. Output coding is Binary Two's Complement (bipolar) or Unipolar Straight Binary (unipolar, when an external logic inverter is used to invert the MSB). In addition, the DAC708/709 can be loaded serially (MSB first).

The DAC706 and DAC707 are designed to interface to a 16-bit bus. Data is written into a 16-bit input latch and subsequently the D/A latch. The DAC706 and DAC707 have current and voltage outputs respectively and are in 28-pin dual-wide hermetic DIPs. Outputs are bipolar only (±1mA and ±10V respectively) and have BTC input coding.

All models have Chip Select, Write and Clear control lines as well as input latch enable lines. In bipolar mode, the Clear input sets the D/A latch to give zero voltage or current output. These converters are 14-bit accurate and are complete with reference and, for the DAC709 and DAC707, a voltage output amplifier.



DAC708/709 Block Diagram



DAC706/707 Block Diagram

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, rated power supplies, and after a 10 minute warm-up unless otherwise noted.

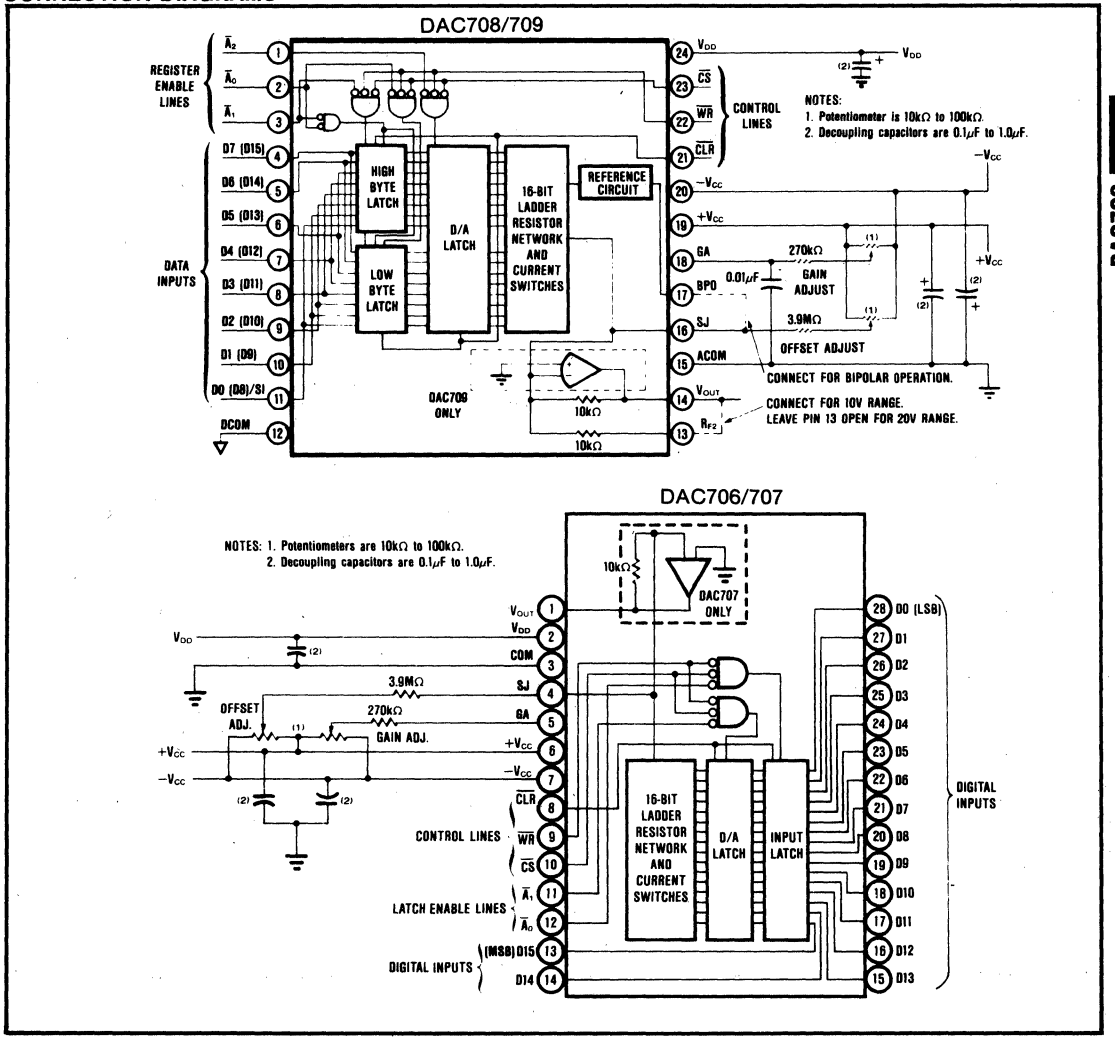
MODEL	DAC706/707/708/709BH			DAC706/707/708/709KH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution			16			*	Bits
Bipolar Input Code		Binary Two's Complement		*			
Unipolar Input Code[1] (DAC708/709 only)		Unipolar Straight Binary		*			
Logic Levels[2]: V_{IH}	+2.0		+5.5	*		*	V
V_{IL}	−1.0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			1			*	μA
I_{IL} (V_I = +0.4V)			1			*	μA
TRANSFER CHARACTERISTICS							
ACCURACY[3]							
Linearity Error		±0.0015	±0.003		*	*	% of FSR[4]
Differential Linearity Error[5]		±0.003	±0.006		*	*	% of FSR
Differential Linearity Error at Bipolar Zero[5,6]		±0.0015	±0.003		±0.003	±0.006	% of FSR
Gain Error[7]		±0.05	±0.10		±0.07	±0.15	%
Zero Error[7]		±0.05	±0.1		*	*	% of FSR
Monotonicity Over Spec Temp. Range	14			*			Bits
Power Supply Sensitivity: +V_{CC}		±0.0015	±0.003		*	±0.006	% of FSR/%V_{CC}
−V_{CC}		±0.0015	±0.003		*	±0.006	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*	% of FSR/%V_{DD}
DRIFT (over specification temperature range[3]							
Gain Drift		±7	±15		±10	±25	ppm/°C
Zero Drift: Unipolar (DAC708/709 only)		±1.5	±3		±2.5	±5	ppm of FSR/°C
Bipolar		±4	±10		±5	±12	ppm of FSR/°C
Differential Linearity Over Temp[5]			+0.009, −0.006			*	% of FSR
Linearity Error Over Temp[5]			±0.006			*	% of FSR
SETTLING TIME (to ±0.003% of FSR)[8]							
Voltage Output Models							
Full Scale Step (2kΩ load)		4	8		*	*	μsec
1LSB Step at Worst Case Code[9]		2.5	4		*	*	μsec
Slew Rate		10			*		V/μsec
Current Output Models							
Full Scale Step (2mA)							
10 to 100Ω load		350			*		nsec
1kΩ load		1			*		μsec
OUTPUT							
VOLTAGE OUTPUT MODELS							
Output Voltage Range							
DAC709 Unipolar (USB Code)		0 to +10			*		V
Bipolar (BTC Code)		±5, ±10			*		V
DAC707 Bipolar (BTC Code)		±10			*		V
Output Current	±5			*			mA
Output Impedance		0.15			*		Ω
Short Circuit to Common Duration		Indefinite			*		
CURRENT OUTPUT MODELS							
Output Current Range							
DAC708 Unipolar (USB Code)[10]		0 to −2			*		mA
Bipolar (BTC Code)[10]		±1			*		mA
DAC706 Bipolar (BTC Code)[10]		±1					mA
Unipolar Output Impedance[10]		4.0			*		kΩ
Bipolar Output Impedance[10]		2.45			*		kΩ
Compliance Voltage		±2.5			*		V
POWER SUPPLY REQUIREMENTS							
Voltage: +V_{CC}	+13.5	+15	+16.5	*	*	*	V
−V_{CC}	−13.5	−15	−16.5	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	V
Current (No Load)							
Current Output Models: +V_{CC}		+10	+25		*	*	mA
−V_{CC}		−13	−25		*	*	mA
V_{DD}		+5	+10		*	*	mA
Voltage Output Models: +V_{CC}		+16	+30		*	*	mA
−V_{CC}		−18	−30		*	*	mA
V_{DD}		+5	+10		*	*	mA
Power Dissipation: Current Output Models		370	640		*	*	mW
Voltage Output Models		535	790		*	*	mW

MODEL	DAC706/707/708/709BH			DAC706/707/708/709KH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TEMPERATURE RANGE							
Specification	−25		+85	0		+70	°C
Storage	−65		+150	*		*	°C

*Specification same as for DAC706/707/708/709BH.

NOTES: (1) MSB must be inverted externally prior to DAC708/709 input. (2) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specified temperature range. (3) DAC706 and DAC708 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all tests. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) ±0.0015% of Full Scale Range is equal to 1 LSB in 16-bit resolution. ±0.003% of Full Scale Range is equal to 1 LSB in 15-bit resolution. ±0.006% of Full Scale Range is equal to 1 LSB in 14-bit resolution. (6) Error at input code 0000_H. (For unipolar connection on DAC708/709 the MSB must be inverted externally prior to D/A input.) (7) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer fucntion around the bipolar zero point. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) The bipolar worst-case code change is $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$. For unipolar (DAC708/709 only) it is $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$. (10) Tolerance on output impedance and output current is ±30%.

CONNECTION DIAGRAMS

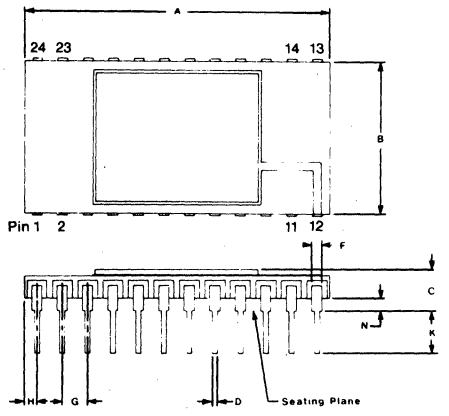


DESCRIPTION OF PIN FUNCTIONS

DAC706/707		Pin #	DAC708/709	
Designator	Description		Designator	Description
V_{OUT} (DAC707) R_F (DAC706)	Voltage output for DAC707 or an internal feedback resistor for use with an external output op amp for the DAC706.	1	$\overline{A_2}$	Latch enable for D/A latch (Active low)
V_{DD}	Logic supply (+5V)	2	$\overline{A_0}$	Latch enable for "low byte" input (Active low). When both $\overline{A_0}$ and $\overline{A_1}$ are logic "0", the serial input mode is selected and the serial input is enabled.
COM	Common	3	$\overline{A_1}$	Latch enable for "high byte" input (Active low). When both $\overline{A_0}$ and $\overline{A_1}$ are logic "0", the serial input mode is selected and the serial input is enabled.
SJ (DAC707) I_{OUT} (DAC706)	Summing Junction of the internal output op amp for the DAC707, or the current output for the DAC706. Offset adjust circuit is connected to the summing junction of the output amplifier. Refer to Connection Diagram.	4	D7 (D15)	Input for data bit 7 if enabling low byte (LB) latch or data bit 15 if enabling the high byte (HB) latch.
GA	Gain Adjust pin. Refer to Connection Diagram for gain adjust circuit.	5	D6 (D14)	Input for data bit 6 if enabling LB latch or data bit 14 if enabling the HB latch.
$+V_{CC}$	Positive supply voltage (+15V)	6	D5 (D13)	Data bit 5 (LB) or data bit 13 (HB)
$-V_{CC}$	Negative supply voltage (−15V)	7	D4 (D12)	Data bit 4 (LB) or data bit 12 (HB)
$\overline{CLR}$	Clear line. Sets the input latch to zero and sets the D/A latch to the input code that gives bipolar zero on the D/A output (Active low)	8	D3 (D11)	Data bit 3 (LB) or data bit 11 (HB)
		9	D2 (D10)	Data bit 2 (LB) or data bit 10 (HB)
$\overline{WR}$	Write control line (Active low)	10	D1 (D9)	Data bit 1 (LB) or data bit 9 (HB)
$\overline{CS}$	Chip select control line (Active low)	11	D0 (D8)/SI	Data bit 0 (LB) or data bit 8 (HB). Serial input when serial mode is selected.
$\overline{A_1}$	Enable for D/A converter latch (Active low)			
$\overline{A_0}$	Enable for input latch (Active low)	12	DCOM	Digital Common
D15 (MSB)	Data bit 15 (Most Significant Bit)	13	R_{F2}	Feedback resistor for internal or external operational amplifier. Connect to pin 14 when a 10V output range is desired. Leave open for a 20V output range.
D14	Data bit 14	14	V_{OUT} R_{F1} (DAC708)	Voltage output for DAC709 or feedback resistor for use with an external output op amp for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D13	Data bit 13	15	ACOM	Analog common
D12	Data bit 12	16	SJ (DAC709) I_{OUT} (DAC708)	Summing junction of the internal output op amp for the DAC709, or the current output for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D11	Data bit 11	17	BPO	Bipolar offset. Connect to pin 16 when operating in the bipolar mode. Leave open for unipolar mode.
D10	Data bit 10	18	GA	Gain Adjust pin
D9	Data bit 9	19	$+V_{CC}$	Positive supply voltage (+15V)
D8	Data bit 8	20	$-V_{CC}$	Negative supply voltage (−15V)
D7	Data bit 7	21	$\overline{CLR}$	Clear line. Sets the high and low byte input registers to zero and, for bipolar operation, sets the D/A register to the input code that gives bipolar zero on the D/A output. (In the unipolar mode, invert the MSB prior to the D/A.)
D6	Data bit 6	22	$\overline{WR}$	Write control line
D5	Data bit 5	23	$\overline{CS}$	Chip select control line
D4	Data bit 4	24	V_{DD}	Logic supply (+5V)
D3	Data bit 3	25	No pin	
D2	Data bit 2	26	No pin	(The DAC708 and DAC709 are in 24-pin packages)
D1	Data bit 1	27	No pin	
D0 (LSB)	Data bit 0 (Least Significant Bit)	28	No pin	

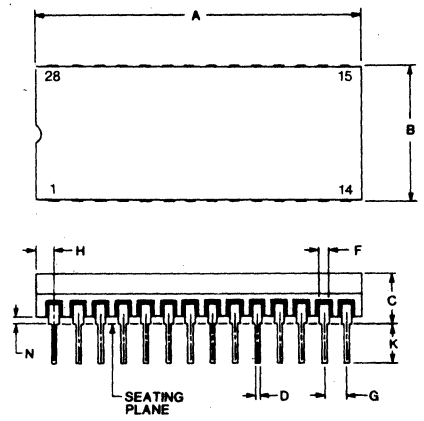
MECHANICAL

DAC708/709



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.190	1.210	30.23	30.73
B	.580	.600	14.73	15.24
C	.140	.185	3.56	4.70
D	.016	.020	0.41	0.51
F	.030	.050	0.76	1.27
G	.100 BASIC		2.54 BASIC	
H	.035	.065	0.89	1.65
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

DAC706/707



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.435	1.465	36.45	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	.38	.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	.23	.30
K	.155	.195	3.94	4.95
L	.600 BASIC		15.24 BASIC	
N	.020	.030	.51	.76

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON ..... 0V, +15V
$+V_{CC}$ to COMMON ..... 0V, +18V
$-V_{CC}$ to COMMON ..... 0V, −18V
Digital Data Inputs to COMMON ..... −0.5V, V_{DD} +0.5
DC Current any Input ..... ±10mA
Reference Out to COMMON ..... Indefinite Short to COMMON
External Voltage Applied to R_F
(pin 1, DAC706; pin 13 or 14, DAC708) ..... ±18V
External Voltage Applied to D/A Output
(pin 1, DAC707; pin 14, DAC709) ..... ±5V
V_{OUT} (DAC707, DAC709) ..... Indefinite Short to COMMON
Power Dissipation 1000mW
Storage Temperature ..... −60°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

For bipolar operation, the DAC706/707/708/709 accept positive-true binary two's complement input code. For unipolar operation (DAC708/709 only) the input code is positive-true straight-binary provided that the MSB input is inverted with an external inverter. See Table I.

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output: Unipolar Straight Binary[1] (DAC708/709 only; connected for Unipolar operation)	Analog Output: Binary Two's Complement (Bipolar operation; all models)
$7FFF_H$	+1/2 Full Scale −1 LSB[2]	+Full Scale
0000_H	Zero	Zero
$FFFF_H$	+Full Scale	−1LSB
8000_H	+1/2 Full Scale	−Full Scale

(1) MSB must be inverted externally. (2) Assumes MSB is inverted externally.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (−Full Scale point and +Full Scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2 LSB when the input changes between

adjacent codes. A negative DLE specification of −1LSB maximum (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC706/707/708/709 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences at t_{min}, +25°C and t_{max}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with 0000_H applied to he D/A converter inputs over the specified temperature range. (For the DAC708/709 in unipolar mode, the MSB must be inverted.) This code corresponds to zero volts (DAC707 and DAC709) or zero milliamps (DAC706 and DAC708) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V for bipolar or 10V for unipolar and a 1LSB change at the "major carry", the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the ouput RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

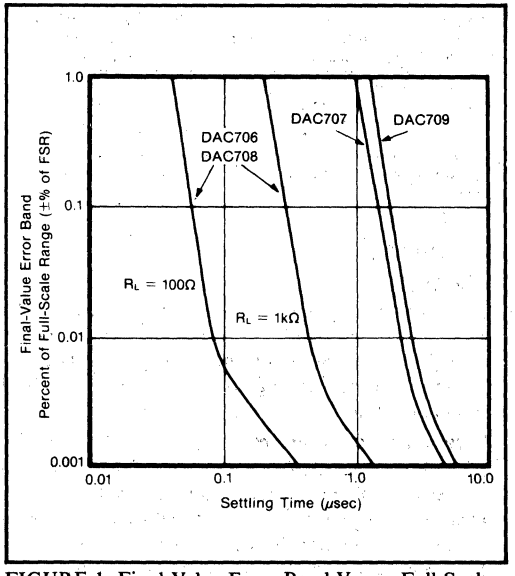


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

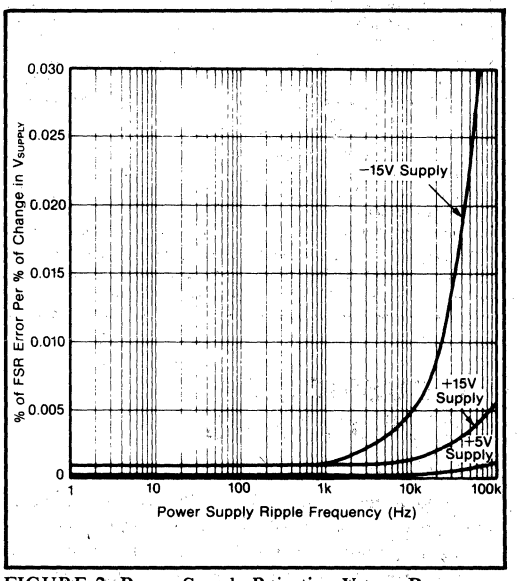


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substitued in place of the 3.9MΩ resistor. A 0.001μF to 0.01μF ceramic capacitor should be connected from GAIN ADJUST (pin 22) to COMMON to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

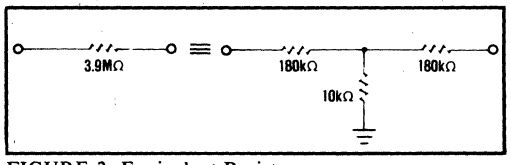


FIGURE 3. Equivalent Resistances.

Zero Adjustment

For unipolar (USB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (BTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and connection diagrams for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

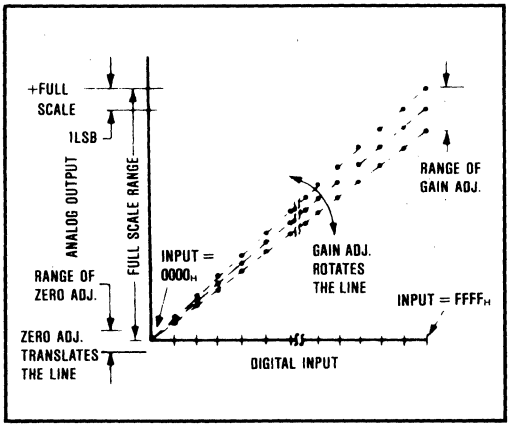


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC708 and DAC709.

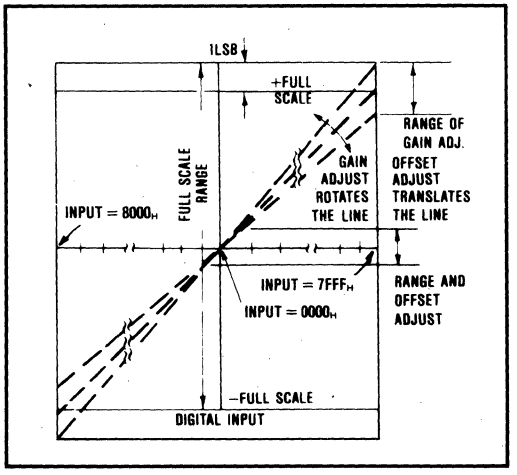


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC706/707 and DAC708/709.

TABLE II. Digital Input And Analog Output Voltage/Current Relationships.

VOLTAGE OUTPUT MODELS									
Digital Input Code	Analog Output *Unipolar (DAC709) 16-Bit	15-Bit	14-Bit	Units	Digital Input Code	Analog Output Bipolar (DAC707 and DAC709) 16-Bit	15-Bit	14-Bit	Units
One LSB	153	305	610	μV	One LSB	305	610	1224	μV
FFFFH	+9.99985	+9.99969	+9.99939	V	7FFFH	+9.99960	+9.99939	+9.99878	V
0000H	0	0	0	V	8000H	−10.0000	−10.0000	−10.0000	V
CURRENT OUTPUT MODELS									
Digital Input Code	Analog Output *Unipolar (DAC708) 16-Bit	15-Bit	14-Bit	Units	Digital Input Code	Analog Output Bipolar (DAC706 and DAC708) 16-Bit	15-Bit	14-Bit	Units
One LSB	0.031	0.061	0.122	μA	One LSB	0.031	0.061	0.122	μA
FFFFH	−1.99997	−1.99994	−1.99988	mA	7FFFH	−0.99997	−0.99994	−0.99988	mA
0000H	0	0	0	mA	8000H	+1.00000	+1.00000	+1.00000	mA

*MSB assumed to be inverted externally.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagram for gain adjustment circuit connections.

INTERFACE LOGIC AND TIMING

DAC708/709

The signals CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), register enables ($\overline{A_0}$, $\overline{A_1}$, and $\overline{A_2}$), and CLEAR ($\overline{CLR}$), provide the control functions for the microprocessor interface. They are all active in the "low" or logic "0" state. $\overline{CS}$ must be low to access any of the registers. $\overline{A_0}$ and $\overline{A_1}$ steer the input 8-bit data byte to the low- or high-byte input latch respectively. $\overline{A_2}$ gates the contents of the two input latches through to the D/A latch in parallel. The contents are then applied to the input of the D/A converter. When $\overline{WR}$ goes low, data is strobed into the latch or latches which have been enabled.

The serial input mode is activated when both $\overline{A_0}$ and $\overline{A_1}$ are logic "0" simultaneously. The D0 (D8)/SI input data line accepts the serial data MSB first. Each bit is clocked in by a $\overline{WR}$ pulse. Data is strobed through to the D/A latch by $\overline{A_2}$ going to logic "0" the same as in the parallel input mode.

Each of the latches can be made "transparent" by maintaining its enable signal at logic "0". However, as stated above, when both $\overline{A_0}$ and $\overline{A_1}$ are logic "0" at the same time, the serial mode is selected.

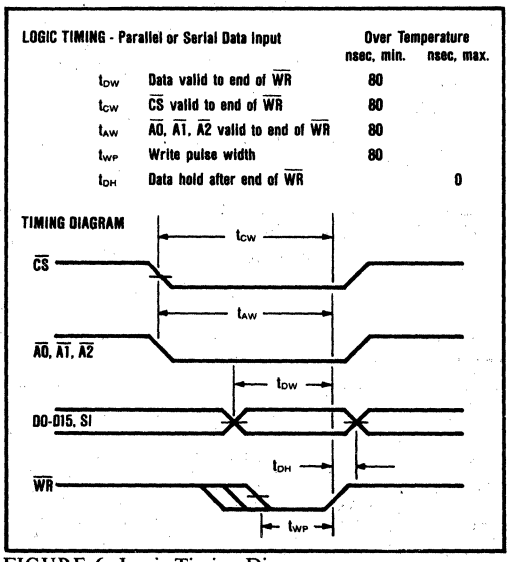


FIGURE 6. Logic Timing Diagram.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the D/A latch to 8000_H. This is the binary code that gives a null, or zero, at the output of the D/A in the bipolar mode. In the unipolar mode, activitating $\overline{CLR}$ will cause the output to go to one-half of full scale.

The maximum clock rate of the latches is 10MHz. The minimum time between write ($\overline{WR}$) pulses for successive enables is 20nsec. In the serial input mode (DAC708 and DAC709), the maximum rate at which data can be clocked into the input shift register is 10MHz.

The timing of the control signals is given in Figure 6.

DAC706/707

The DAC706/707 interface timing is the same as that described above except instead of two 8-bit separately-enabled input latches, it has a single 16-bit input latch enabled by $\overline{A_0}$. The D/A latch is enabled by $\overline{A_1}$. Also, there is no serial-input mode.

INSTALLATION CONSIDERATIONS

DAC708 AND DAC709

Due to the extremely-high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of typical 1 ounce copper-clad printed circuit board material is approximately 1/2mΩ per square. In the example above, a 10 milliinch-wide conductor 60 milliinches long would cause a 1LSB error.

In Figures 7 and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed with gain calibration. R_3 is part of R_L if the output voltage is sensed at COMMON (pin 15).

Figures 8 and 9 show two methods of connecting the current output mdoel (DAC708) with an external precision output op amp. By sensing the output voltage at the load resistor (connecting R_F to the output of the amplifier at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

In many applications it is impractical to sense the output voltage at ANALOG COMMON, pin 15. Sensing the output voltage at the system ground point is permissible with the DAC708 and DAC709 because they have separate analog and digital common lines and the return current is a near-constant 2mA and varies by only 10μA to 20μA over the entire input code range. R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 is constant and appears as a zero error that can be nulled with the zero calibration adjustment.

Another approach senses the output at the load as shown in Figure 9. In this circuit the output voltage is

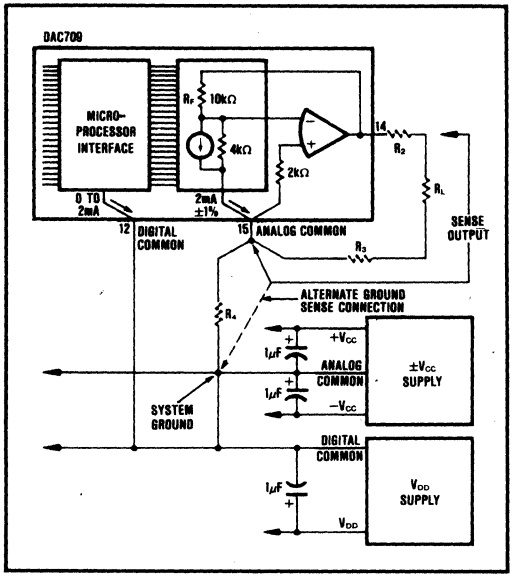


FIGURE 7. DAC709 Bipolar Output Circuit (Voltage Out).

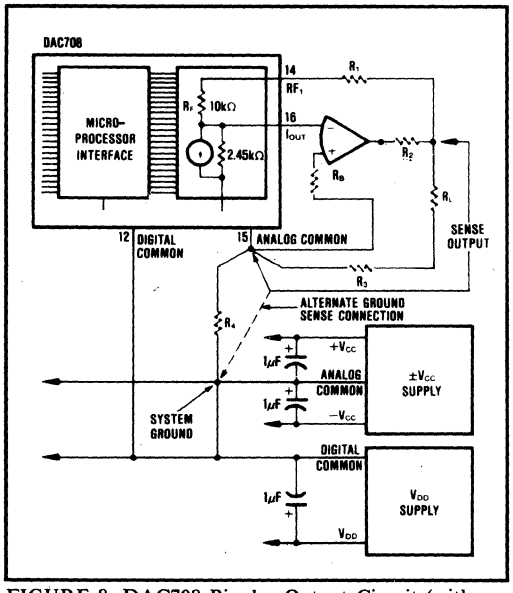


FIGURE 8. DAC708 Bipolar Output Circuit (with External Op Amp).

sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection across R_L. The effect of R_4 is negligible as explained previously.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from

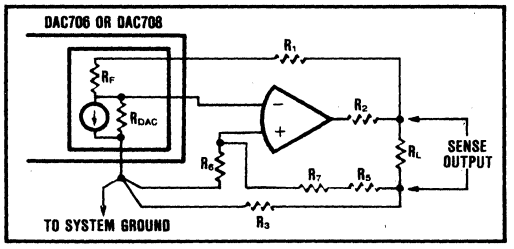


FIGURE 9. Alternate Connection for Ground Sensing at the Load (Current Output Models).

sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small flux-capture cross section for any external field.

DAC706 AND DAC707

The above considerations are all applicable to the DAC706 and DAC707 except there is only one COMMON pin (pin 3). Refer to Figures 9, 10, and 11. The ground currents in the ANALOG COMMON of the

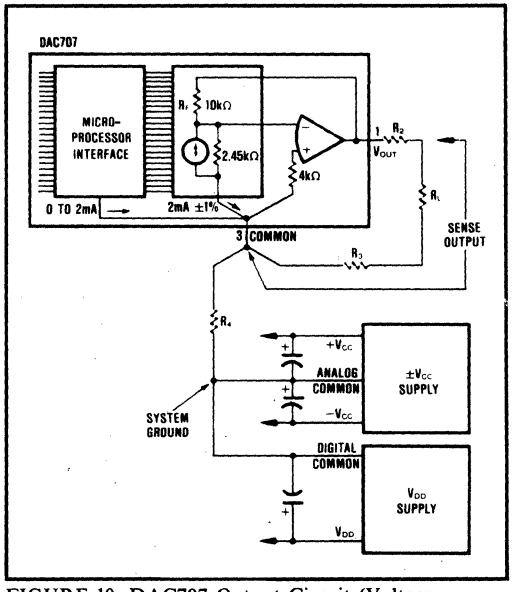


FIGURE 10. DAC707 Output Circuit (Voltage, Bipolar).

DAC708/709 are also present in the COMMON pin of the DAC706/707. There is also an additional code-dependent ground current from the digital interface circuitry that flows through pin 3. Again, the effects of this component of the ground current can be minimized by using pin 3 as the sense point.

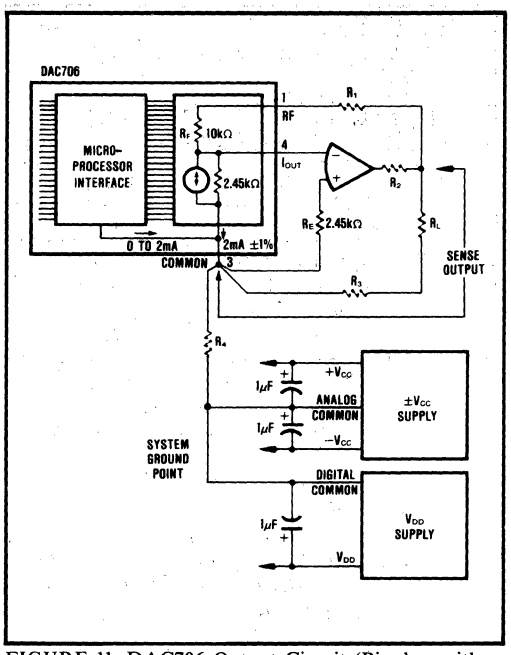


FIGURE 11. DAC706 Output Circuit (Bipolar, with External Op Amp).

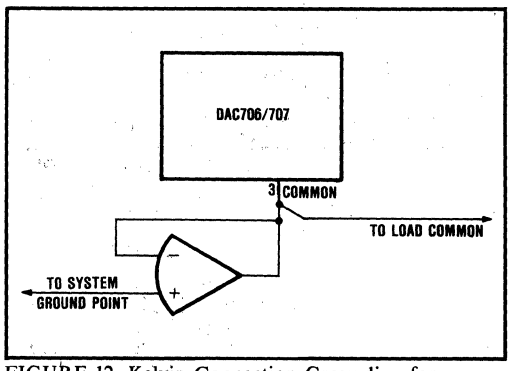


FIGURE 12. Kelvin Connection Grounding for DAC706/707.

In situations where this is not possible, the output signal may be sensed at the system ground point by either maintaining the return lead resistance below 0.04Ω (to keep the error from this source to ±0.003% of FSR max) or by using Kelvin sensing as shown in Figure 12. An operational amplifier connected as a unity-gain follower is used to reference the D/A common to the system ground. In addition, the varying ground current is "soaked up" by the op amp, eliminating the ground drop problems that would result in running the ground current through R_4. The input offset and offset drift of the amplifier will add directly to the zero error and zero drift of the D/A converter.

APPLICATIONS

LOADING THE DAC709 SERIALLY ACROSS AN ISOLATION BARRIER

A very useful application of the DAC709 is in achieving low-cost isolation that preserves high accuracy. Using the serial input feature of the input register pair, only three signal lines need to be isolated. The data is applied to pin 11 in a serial bit stream, MSB first. The $\overline{WR}$ input is used as a data strobe, clocking in each data bit. A RESET signal is provided for system startup and reset. These three signals are each optically isolated. Once the 16 bits of serial data have been strobed into the input register pair, the data is strobed through to the D/A register by the "carry" signal out of a 4-bit binary synchronous counter that has counted the 16 $\overline{WR}$ pulses used to clock in the data. The circuit diagram is given in Figure 13.

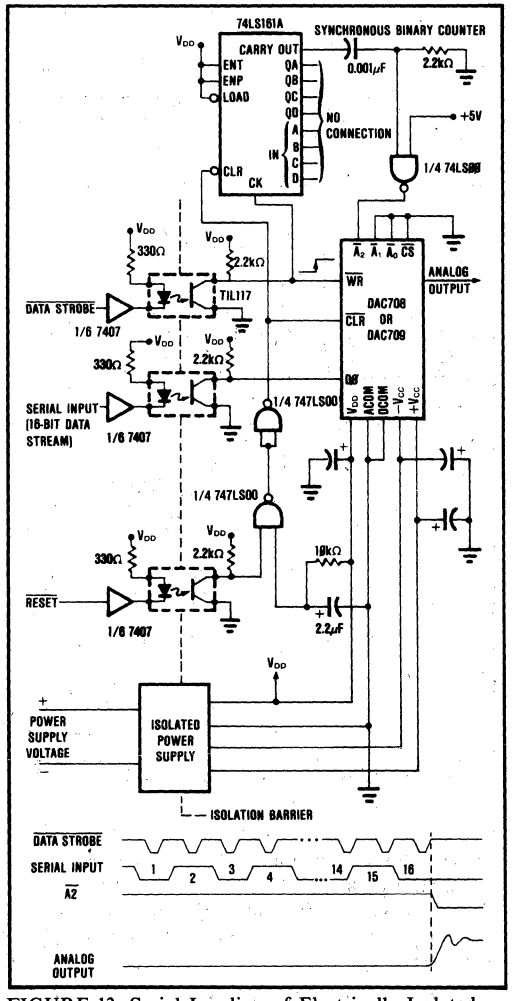


FIGURE 13. Serial Loading of Electrically Isolated DAC708/709.

CONNECTING MULTIPLE DAC707'S TO A 16-BIT MICROPROCESSOR BUS

Figure 14 illustrates the method of connecting multiple DAC707's to a 16-bit microprocessor bus. The circuit shown has two DAC707's and uses only one address line to select either the input register or the D/A register. An external address decoder selects the desired converter.

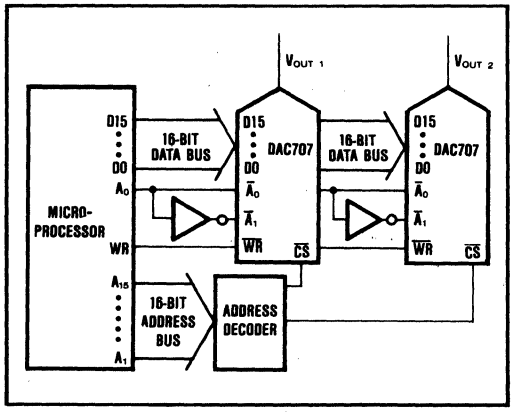


FIGURE 14. Connecting Multiple DAC707's to a 16-Bit Microprocessor.

ORDERING INFORMATION

Model	Temperature Range	Input Configuration	Output Configuration
DAC706BH	−25 to +85°C	16-bit Port	Current Out
DAC706KH	0 to +70°C	16-bit Port	Current Out
DAC707BH	−25 to +85°C	16-bit Port	Voltage Out
DAC707KH	0 to +70°C	16-bit Port	Voltage Out
DAC708BH	−25 to +85°C	8-bit Port/Serial Input	Current Out
DAC708KH	0 to +70°C	8-bit Port/Serial Input	Current Out
DAC709BH	−25 to +85°C	8-bit Port/Serial Input	Voltage Out
DAC709KH	0 to +70°C	8-bit Port/Serial Input	Voltage Out

BURR-BROWN®

DAC800
DAC800P

Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST HIGH RELIABILITY SINGLE-CHIP REPLACEMENT FOR INDUSTRY STANDARD DAC80
- 12-BIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY, 0°C to +70°C
- GUARANTEED MONOTONICITY, 0°C to +70°C
- DUAL-IN-LINE PACKAGE WITH INDUSTRY STANDARD (DAC80) PINOUT
- HERMETIC PACKAGE (optional)
- TWO PACKAGE OPTIONS: hermetic side-brazed and molded plastic
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES

DESCRIPTION

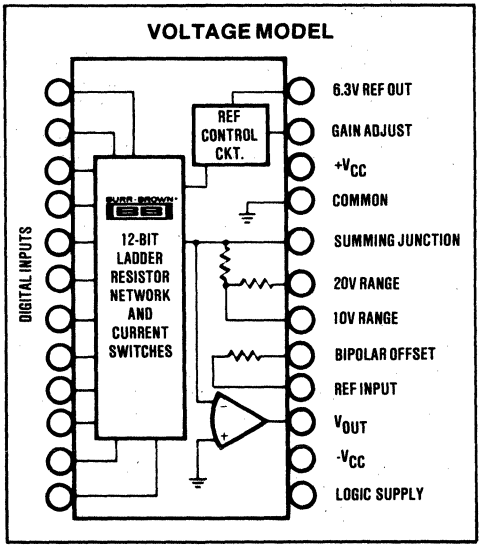
The DAC800 is a third-generation monolithic Integrated Circuit that is a pin-for-pin equivalent to the industry-standard DAC80 first introduced by Burr-Brown. It has all of the functions of its predecessor plus faster settling time and enhanced reliability because of its monolithic construction.

The current output model of the DAC800 is a single-chip integrated circuit containing a subsurface zener reference diode, high speed current switches, and laser-trimmed thin-film resistors. The DAC800 provides output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V (V models) or output current ranges of ±1.175mA or 0 to −2.35mA (I model).

This high accuracy converter offers a maximum nonlinearity error of ±1/2LSB, ±30ppm/°C maximum gain drift and guaranteed monotonicity, all over 0°C to +70°C. In the bipolar configuration, total drift is guaranteed to be less than 25ppm of FSR/°C.

The DAC800 is in a 24-pin dual-in-line package with the popular DAC80 pinout. Two package options are available: a hermetic ceramic side-brazed package and a low-cost molded plastic package (voltage out only).

For designs that require a wide temperature range, see Burr-Brown models DAC850 and DAC851.



Patents pending may apply upon the allowance and issuance of patents thereon. The product may also be covered in other countries by one or more international patents.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

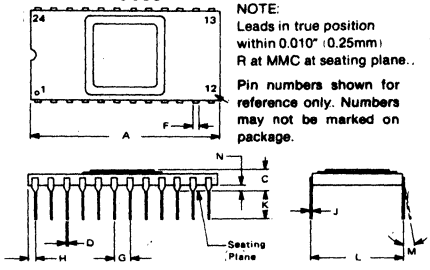
ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

MODEL	DAC800, DAC800P			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT				
Resolution			12	bits
Logic Levels				
(over spec. temp range)[1]				
V_{IH} (Logic "1")	+2		16.5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IN} = +2.4V)			+20	µA
I_{IL} (V_{IN} = +0.4V)			−0.36	mA
ACCURACY				
Linearity Error at 25°C		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	+1, −3/4	LSB
Gain Error[2]		±0.1	±0.3	%
Offset Error[2]		±0.05	±0.15	% of FSR[3]
POWER SUPPLY SENSITIVITY				
+15V and +5V Supplies		±0.0001	±0.001	% of FSR/%V_{CC}
−15V Supply		±0.003	±0.006	% of FSR/%V_{CC}
DRIFT[4] (0°C to +70°C)				
Bipolar Drift (±full scale drift for the bipolar connection)		±10	±25	ppm of FSR/°C
Total error over 0°C to +70°C[5]				
Unipolar		±0.06	±0.15	% of FSR
Bipolar		±0.05	±0.12	% of FSR
Gain		±10	±30	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, −7/8	LSB
Linearity Error 0°C to +70°C			±1/2	LSB
Monotonicity Temp. Range, min	0		+70	°C
CONVERSION SPEED, V models				
Settling Time to ±0.01% of FSR				
For FSR Change				
20V range, 2kΩ load		3	5	µsec
10V range, 2kΩ load		2.5	4	µsec
For 1LSB Change, Major Carry, 2kΩ load		1.5		µsec
Slew Rate, 2kΩ load	10	15	V/µsec	
CONVERSION SPEED, I model (DAC800 only)				
Settling Time to ±0.01% of FSR				
For FSR Change				
10Ω to 100Ω load		300		nsec
1kΩ load		1		µsec
ANALOG OUTPUT, V models				
Ranges ($\pm V_{CC}$ = 15V)[6]	±2.5, ±5, ±10, 0 to +5, 0 to +10			V
Output Current	±5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit to Common, Duration		Indefinite		
ANALOG OUTPUT, I model (DAC800 only)				
Ranges: Bipolar	±0.88	±1.175	±1.47	mA
Unipolar	0 to 1.76	0 to −2.35	0 to −2.94	mA
Output Impedance: Bipolar		3.1		kΩ
Unipolar		7.2		kΩ
Compliance	2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	V
Current (for external loads), Source	1.5	2.5		mA
Tempco of Drift		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
$\pm V_{CC}$	±11.4	±15	±16.5	VDC
V_{DD}[7]	+4.5	+5.0	+16.5	VDC
Supply Drain				
+15V, −15V (no load)		+8, 20	+12, −25	mA
85V (logic supply)		+7	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating[8]	25		+85	°C
Storage	−60		+100	°C

MECHANICAL

DAC800



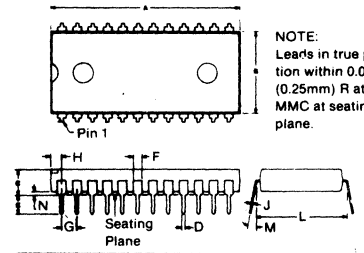
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane..

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

CASE: Ceramic
MATING CONNECTOR: 0245MC
WEIGHT: 4.1 grams (0.15 oz.)

DAC800P



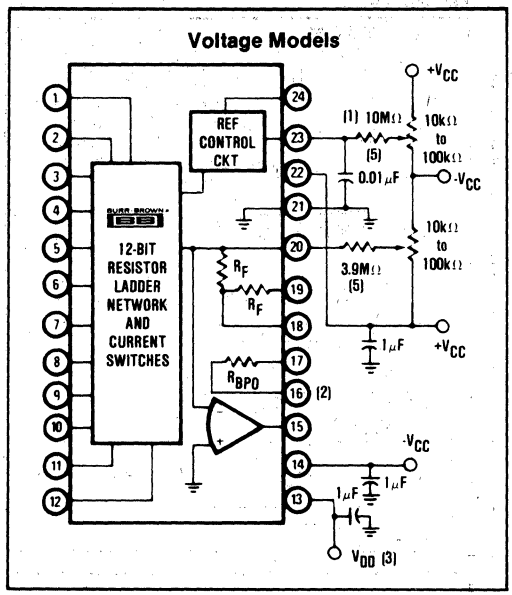
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

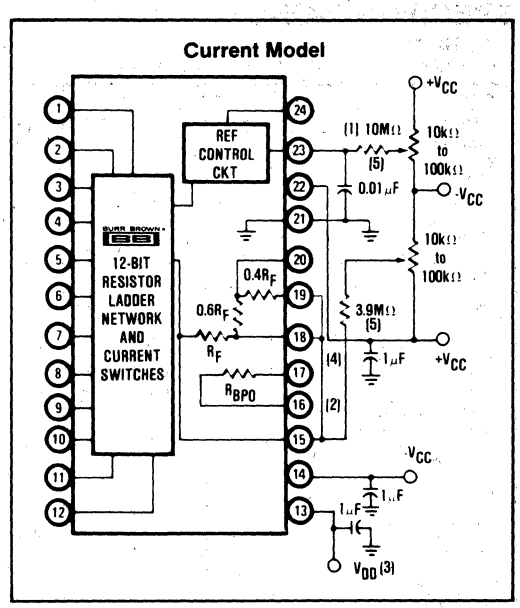
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.233	1.283	31.32	32.59
B	.538	.575	13.67	14.61
C	.169	.224	4.29	5.69
D	.015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

CASE: Plastic
MATING CONNECTOR: 0245MC
WEIGHT: 3.7 grams (0.13 oz.)

NOTES:
(1) Refer to Logic Input Compatibility section.
(2) Adjustable to zero with external trim potentiometer.
(3) FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
(4) To maintain drift spec internal feedback resistors must be used for current output models.
(5) Includes the effects of gain, offset and linearity drift. Gain and offset errors are adjusted to zero at +25°C.
(6) A minimum of ±13V supply is required for ±10V and 0 to 10V ranges. All other ranges accept ±12V supplies.
(7) Power dissipation is an additional 100mW, max, when V_{DD} is operated at +15V.
(8) Max operating temperature for DAC800P-CBI-V is +70°C.

CONNECTION DIAGRAMS





PIN ASSIGNMENTS

I MODEL	PIN NO.	V MODELS
MSB BIT 1	1	BIT 1 MSB
BIT 2	2	BIT 2
BIT 3	3	BIT 3
BIT 4	4	BIT 4
BIT 5	5	BIT 5
BIT 6	6	BIT 6
BIT 7	7	BIT 7
BIT 8	8	BIT 8
BIT 9	9	BIT 9
BIT 10	10	BIT 10
BIT 11	11	BIT 11
LSB BIT 12	12	BIT 12 LSB
LOGIC SUPPLY, V_{DD}	13	LOGIC SUPPLY, V_{DD}
$-V_{CC}$	14	$-V_{CC}$
I_{OUT}	15	V_{OUT}
REF. INPUT	16	REF. INPUT
BIPOLAR OFFSET	17	BIPOLAR OFFSET
SCALING NETWORK	18	10V RANGE
SCALING NETWORK	19	20V RANGE
SCALING NETWORK	20	SUMMING JUNCTION
COMMON	21	COMMON
$+V_{CC}$	22	$+V_{CC}$
GAIN ADJUST	23	GAIN ADJUST
6.3V REF. OUT	24	6.3V REF. OUT

NOTES:

1. DAC80 which may be replaced by DAC800 requires a 33MΩ resistor. DAC800 requires a 10MΩ resistor. DAC80's may also be operated with a 10MΩ resistor resulting in increased trim range.
2. Pin 16 of DAC800 is used only to connect the bipolar offset resistor. An external reference voltage may not be used with DAC800 as is possible with DAC80.
3. If connected to $+V_{CC}$, which is permissible, power dissipation increases 75mW typ, 100mW max.
4. For fastest settling time connect pins 19, 18, and 15 together.
5. Values shown are for ±15V supplies. For supplies below ±13.5V use 2.7MΩ in place of 3.9MΩ and 7.5MΩ in place of 10mΩ.

ORDERING INFORMATION

MODEL	OUTPUT	PACKAGE
DAC800-CBI-I	Current	Side-braze
DAC800-CBI-V	Voltage	Side-braze
DAC800P-CBI-V	Voltage	Molded Plastic

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC800 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes; CSB, CTC, or COB.

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-1LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	1/2 Full Scale -1LSB	-1LSB	+Full Scale
111111111111	Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC800 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC800 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain Drift is established by: 1) testing the end point differences for each DAC800 model at 0°C, +25°C and +70°C; 2) calculating the gain change with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C.

Offset Drift is a measure of the change in output with all "1"s on the inputs over the specified temperature range. The Offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

Bipolar Drift is a measure of the change in plus or minus full scale output over the specification temperature range for the bipolar connection. Because Bipolar Offset Drift and Gain Drift have canceling interactions, Bipolar Drift is not simply the sum of the two. Total bipolar error over temperature is calculated using Bipolar Drift, then adding ±1/2LSB of linearity error.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Model: Two settling times are specified to ±0.01% of FSR. Each is given for the current model connected with two different resistive loads: 10Ω to 100Ω and 1000Ω. Internal resistors are provided for connecting a nominal load resistance of approximately 1000Ω for output voltage ranges of ±1V and 0 to -2V.

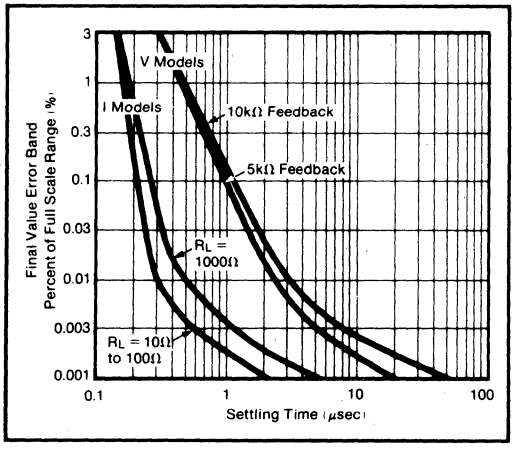


FIGURE 1. Full Scale Range Settling Time vs Final Value Error Band.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is -2.5V to +2.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

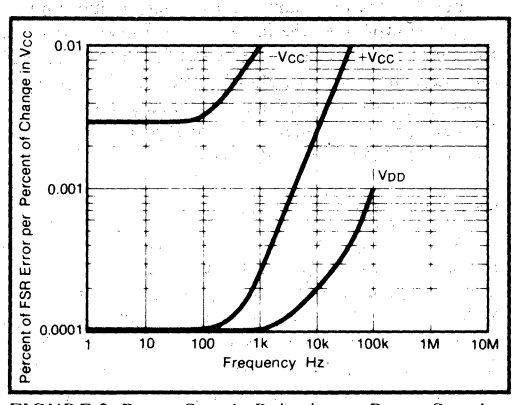


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC800 models have an on-chip +6.3 volt reference. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. Pin 16 is used only to connect the bipolar offset resistor. An external reference may not be used with DAC800. See Connection Diagrams. The reference voltage may be used to supply external circuits with 2.5mA of current (typical) in addition to the 1mA required by the bipolar offset circuit.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC800. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

±12V OPERATION

The DAC800 is fully specified for operation on ±12V power supplies. However, to use the ±10V and 0 to +10V ranges of the voltage output models, the power supplies must be ±13V or greater. All other voltage output ranges and all current output ranges provide satisfactory operation with ±11.4V supplies. The supplies should be balanced to obtain optimum performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC800 to prevent noise pick-up. For operation with supplies of less than ±13.5V, use 2.7MΩ and 7.5MΩ resistors in place of the 3.9MΩ and 10MΩ resistors, respectively. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. The Gain Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to reduce noise pick-up. Figures 4 and 5 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

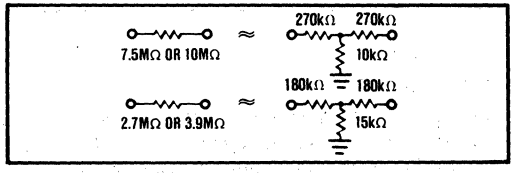


FIGURE 3. Equivalent Resistances.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

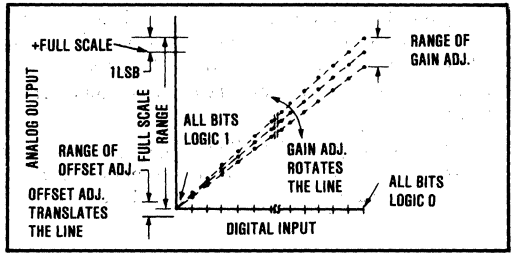


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

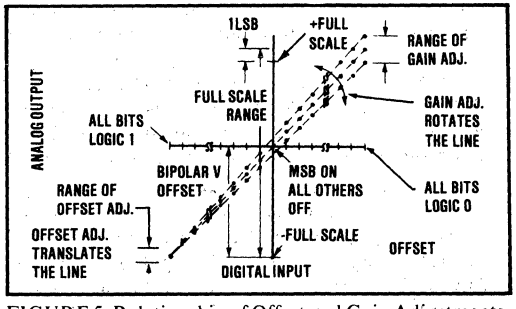


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections. Offset should be adjusted prior to gain.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

TABLE II. Digital Input/Analog Output.

Digital Input	Analog Output			
	Voltage*		Current	
MSB LSB	0 to +10V	±10V	0 to −2mA	±1mA
000000000000	+9.9976V	+9.9951V	−1.9995mA	−0.9995mA
011111111111	+5.0000V	0.0000V	−1.0000mA	0.0000mA
100000000000	+4.9976V	−0.0049V	−0.9995mA	+0.0005mA
111111111111	0.0000V	−10.0000V	0.0000mA	+1.0000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC800 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

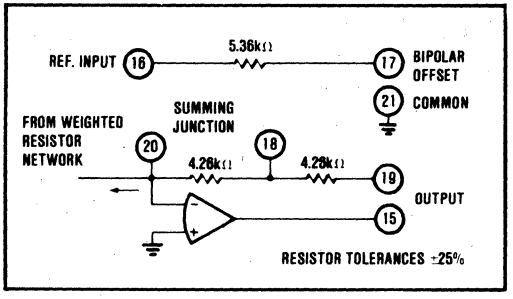


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE III. Output Voltage Range Connections - Voltage Model DAC800.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full scale range change is specified as 3μsec for the 20-volt range and 2.5μsec for the 10-volt range.

CURRENT OUTPUT MODEL

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

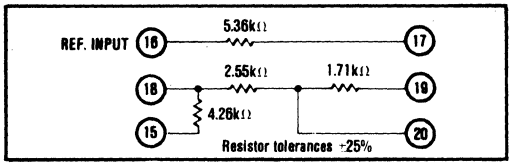


FIGURE 7. Internal Scaling Resistors.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of

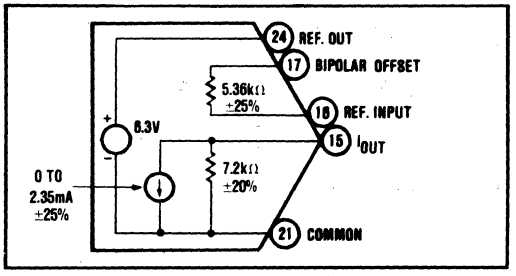


FIGURE 8. Current Output Model Equivalent Output Circuit.

±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2.35mA \left(\frac{R_L \times 7.2k\Omega}{R_L + 7.2k\Omega} \right)$$

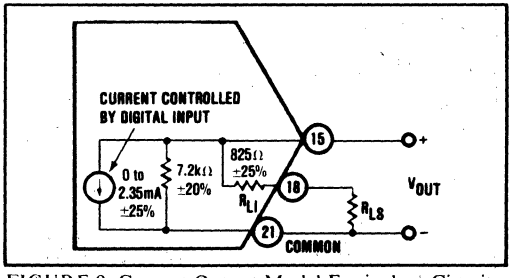


FIGURE 9. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift. Tolerances on internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 10, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1.175mA\left(\frac{R_L \times 3.07k\Omega}{R_L + 3.07k\Omega}\right)$$

To achieve specified drift, connect 1.71kΩ and 2.55kΩ internal scaling resistors in parallel (R_{LI}) and add an external metal film resistor (R_{LS}) in series to obtain a full

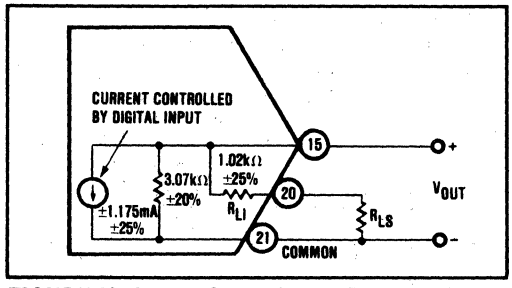


FIGURE 10. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

scale output range of ±1V. The tolerances on the internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving An External Op Amp

The current output model DAC800 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 11.

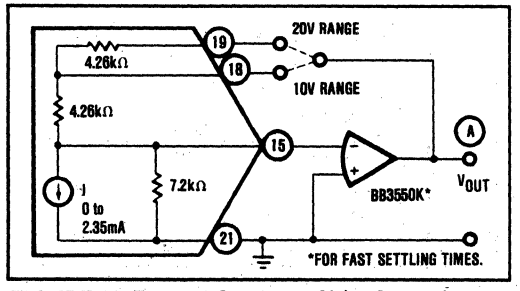


FIGURE 11. External Op Amp - Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC800 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC800 provides output voltage ranges the same as the voltage model DAC800. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output DAC800.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1.175mA ±25% for bipolar voltage ranges and -2.35mA ±25% for unipolar voltage ranges. See Figure 12. Use protection diodes when a high voltage op amp is used.

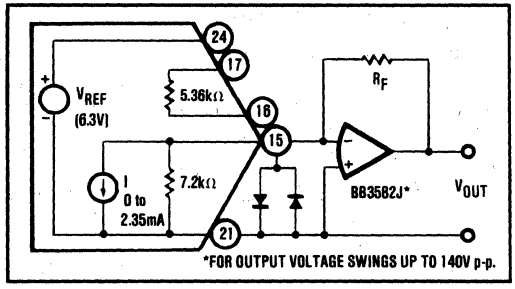


FIGURE 12. External Op Amp - Using External Feedback Resistors.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

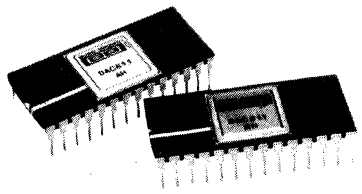
LOGIC INPUT COMPATIBILITY

DAC800 digital inputs are TTL, LSTTL and 54 74HC CMOS compatible over the operating range of V_{DD}, +5 to +15V. The input switching threshold remains at the TTL threshold over supply range of V_{DD}, +5V to +15V.

Logic "0" input current over temperature is low enough to permit driving DAC800 directly from outputs of 4000B and 54/74C CMOS devices over the logic power supply range of +5V to +15V.

BURR-BROWN®

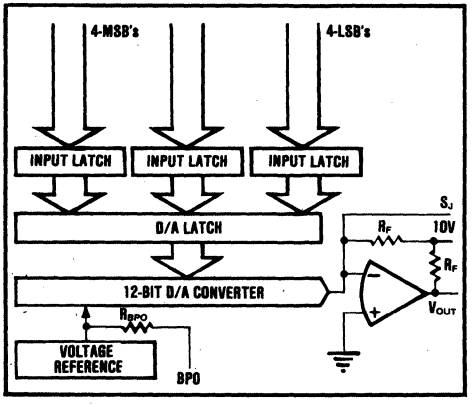
DAC811



Microprocessor-Compatible 12-BIT D/A CONVERTER

FEATURES

- SINGLE INTEGRATED CIRCUIT CHIP
- MICROCOMPUTER INTERFACE: DOUBLE-BUFFERED LATCH
- VOLTAGE OUTPUT: ±10V, ±5V, +10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- ±1/2LSB MAXIMUM NONLINEARITY OVER TEMPERATURE
- GUARANTEED SPECIFICATIONS AT ±12V AND ±15V SUPPLIES
- TTL/5V CMOS-COMPATIBLE LOGIC INPUTS



DESCRIPTION

The DAC811 is a complete single-chip integrated circuit microcomputer-compatible 12-bit digital-to-analog converter. The chip includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nybbles to permit interfacing to 4-, 8-, 12- or 16-bit buses and to handle right- or left-justified data. The 12-bit data in the input latches is transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last nybble or byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions.

The DAC811 is laser trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (B and S grades) at 25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range.

The DAC811 is available in four performance grades. The DAC811AH and BH are specified over the −25°C to +85°C; the DAC811RH and SH are specified over −55°C to +125°C. All models are packaged in a 28-pin 0.6-inch wide dual-in-line hermetically-sealed ceramic side-braze package.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

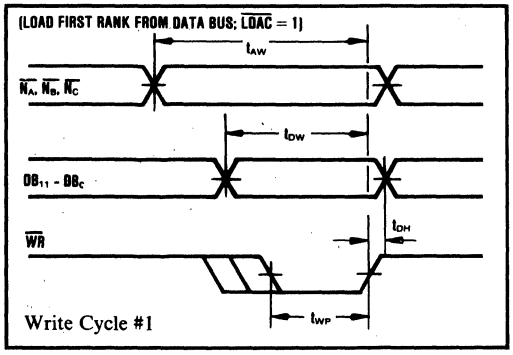
T_A = +25°C ±V_{CC} = 12V or 15V unless otherwise noted.

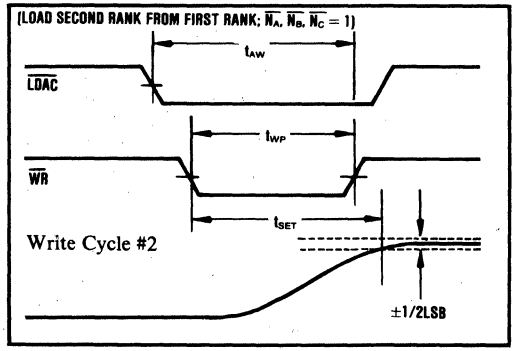
MODEL	DAC811AH			DAC811BH			DAC811RH			DAC811SH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT													
DIGITAL INPUT													
Resolution			12			•			•			•	Bits
Codes[1]		USB, BOB			•			•			•		
Digital Inputs Over Temperature Range[2]													
V_{IH}	+2.0		+15	•		•	•		•	•		•	VDC
V_{IL}	0.0		+0.8	•		•	•		•	•		•	VDC
I_{IH}, V_I = +2.7V			±10			•			•			•	µA
I_{IL}, V_I = +0.4V			±20			•			•			•	µA
Digital Interface Timing Over Temperature Range													
t_{WP}, $\overline{WR}$ pulse width	50			•			•			•			nsec
t_{AW1}, $\overline{N_X}$ and $\overline{LDAC}$ valid to end of $\overline{WR}$	50			•			•			•			nsec
t_{DW}, data valid to end of $\overline{WR}$	80			•			•			•			nsec
t_{DH}, data valid hold time	0			•			+10			•			nsec
TRANSFER CHARACTERISTICS													
ACCURACY													
Linearity Error		±1/4	±1/2		±1/8	±1/4		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[3]		±0.1	±0.2		•	•		•	•		•	•	%
Offset Error[3,4]		±0.05	±0.15		•	•		•	•		•	•	% of FSR[5]
Monotonicity		Guaranteed			•			•			•		
Power Supply Sensitivity, +V_{CC}		±0.001	±0.003		•	•		•	•		•	•	% of FSR/%V_{CC}
−V_{CC}		±0.002	±0.006		•	•		•	•		•	•	% of FSR/%V_{CC}
V_{DD}		±0.0005	±0.0015		•	•		•	•		•	•	% of FSR/%V_{DD}
DRIFT (over specification temperature range)													
Gain		±10	±30		±10	±20		±15	±30		±15	±20	ppm/°C
Unipolar Offset		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Bipolar Zero		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Linearity Error Over Temperature Range		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Monotonicity Over Temperature Range		Guaranteed			•			•			•		
CONVERSION SPEED													
SETTLING TIME[6] (to within ±0.01% of FSR of final value; 2kΩ load)													
For Full Scale Range Change, 20V Range		3	4		•	•		•	•		•	•	µsec
10V Range		2	3		•	•		•	•		•	•	µsec
For 1LSB Change at Major Carry[7]		1			•			•			•		µsec
Slew Rate[8]	8	12		•	•		•	•		•	•		V/µsec
OUTPUT													
ANALOG OUTPUT													
Voltage Range (±V_{CC} = 15V)[9], Unipolar		0 to +10			•			•			•		V
Bipolar		±5, ±10			•			•			•		V
Output Current	±5			•			•			•			mA
Output Impedance (at DC)		0.2			•			•			•		Ω
Short Circuit to Common Duration		Indefinite			•			•			•		
REFERENCE VOLTAGE													
Voltage	+6.0	+6.3	+6.6	•	•	•	•	•	•	•	•	•	V
Source Current Available for External Loads	+2.0			•			•			•			mA
Temperature Coefficient		±10	±30		±10	±20		±10	±30		±10	±20	ppm/°C
Short Circuit to Common Duration		Indefinite			•			•			•		
POWER SUPPLY REQUIREMENTS													
Voltage, +V_{CC}	+11.4	+15	+16.5	•	•	•	•	•	•	•	•	•	VDC
−V_{CC}	−11.4	−15	−16.5	•	•	•	•	•	•	•	•	•	VDC
V_{DD}	+4.5	+5	+5.5	•	•	•	•	•	•	•	•	•	VDC
Current (no load), +V_{CC}		+16	+25		•	•		•	•		•	•	mA
−V_{CC}		−23	−35		•	•		•	•		•	•	mA
V_{DD}		+8	+15		•	•		•	•		•	•	mA
Potential at DCOM with Respect to ACOM[9]			±0.5			•			•			•	V
Power Dissipation		625	800		•	•		•	•		•	•	mW
TEMPERATURE RANGE													
Specification	−25		+85	•		•	−55		+125	•		•	°C
Storage	−65		+150	•		•	•		•	•		•	°C
PACKAGE													
Type	28-pin side braze				•			•			•		
	0.6-inch wide dual-in-line				•			•			•		
Material	Ceramic				•			•			•		
Seal	Hard solder (hermetic)				•			•			•		
Weight			6			•			•			•	Grams

*Same as specification to immediate left.

NOTES: (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) Refer to Logic Input Compatibility section. (3) Adjustable to zero with external trim potentiometer. (4) Error at input code 000_{16} for both unipolar and bipolar ranges. (5) FSR means Full Scale Range and is 20V for the ±10V range. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) At the major carry, $7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$. (8) Minimum supply voltage required for ±10V output swing is ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

TIMING DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

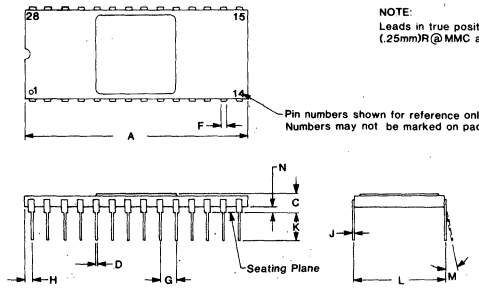
$+V_{CC}$	0 to +18V
$-V_{CC}$ to ACOM	0 to −18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs (pins 2-14, 16-19) to DCOM	−0.4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
REF OUT	Indefinite short to ACOM
External Voltage Applied to DAC Output	−5V to +5V
Power Dissipation	1000mW
Operating Temperature:	
AH, BH	−25°C to +85°C
RH, SH	−55°C to +125°C
Storage Temperature	−65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Model	Package	Temperature Range	Linearity Error, max (+25°C)
DAC811AH	Hermetic Ceramic	−25°C to +85°C	±1/2LSB
DAC811BH	Hermetic Ceramic	−25°C to +85°C	±1/4LSB
DAC811RH	Hermetic Ceramic	−55°C to +125°C	±1/2LSB
DAC811SH	Hermetic Ceramic	−55°C to +125°C	±1/4LSB

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm)R@MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.414	35.20	35.92
C	.108	.166	2.74	4.22
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

PIN NOMENCLATURE

PIN	NAME	FUNCTION
1	V_{DD}	Logic Supply, +5V
2	$\overline{WR}$	WRITE, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	NYBBLE A, enables $\overline{WR}$ to load input latch A (the most significant nybble. Logic low enables.
5	$\overline{N_B}$	NYBBLE B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	NYBBLE C, enables $\overline{WR}$ to load input latch C (the least significant nybble). Logic low enables.
7	D_{11}	DATA, Bit 12, MSB, positive true.
8	D_{10}	DATA, Bit 11
9	D_9	DATA, Bit 10
10	D_8	DATA, Bit 9
11	D_7	DATA, Bit 8
12	D_6	DATA, Bit 7
13	D_5	DATA, Bit 6
14	D_4	DATA, Bit 5
15	DCOM	DIGITAL COMMON, V_{DD} supply return
16	D_0	DATA, Bit 1, LSB
17	D_1	DATA, Bit 2
18	D_2	DATA, Bit 3
19	D_3	DATA, Bit 4
20	$+V_{CC}$	Analog Supply Input, +15V or +12V
21	$-V_{CC}$	Analog Supply Input, −15V or −12V
22	GAIN ADJ	To externally adjust gain
23	ACOM	ANALOG COMMON, $\pm V_{CC}$ supply return
24	V_{out}	D/A converter voltage output
25	10V RANGE	Connect to pin 24 for 10V Range
26	SJ	SUMMING JUNCTION of output amplifier
27	BPO	BIPOLAR OFFSET. Connect to pin 26 for Bipolar Operation
28	REF OUT	6.3V reference output

DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC811 accepts positive true binary input codes. DAC811 may be connected by the user for any one of the following codes: USB (unipolar straight binary), BOB (bipolar offset binary) or, using an external inverter on the MSB line, BTC (binary two's complement). See Table I.

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
111111111111	+Full Scale	+Full Scale	−1 LSB
100000000000	+1/2 Full Scale	Zero	−Full Scale
011111111111	1/2 Full Scale −1 LSB	−1 LSB	+Full Scale
000000000000	Zero	−Full Scale	Zero

*Invert the MSB of the BOB code with external inverter to obtain BTC code.

LINEARITY ERROR

Linearity Error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1's" and all "0's"). The DAC811 linearity error is specified at ±1/4LSB (max) at +25°C for B and S grades and ±1/2LSB (max) for the A and R grades.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC811 are monotonic over their specification temperature range.

DRIFT

Gain drift is a measure of the change in the full scale range output over the specification temperature range. Drift is expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by testing the full scale range value (e.g., +FS minus −FS) at high temperature, +25°C, and low temperature; calculating the error with respect to the +25°C value and dividing by the temperature change.

Unipolar offset drift is a measure of the change in output with all 0's on the input over the specification temperature range. Offset is measured at high temperature, +25°C, and low temperature. The maximum change in offset referred to the +25°C value divided by the temperature change is the offset drift. It is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

Bipolar zero drift is measured at a digital input of 800_{16}, the code that gives zero volts output for bipolar operation.

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of Full Scale Range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC811 contains an on-chip 6.3V reference. This voltage (pin 28) has a tolerance of ±0.3V. The reference output may be used to drive external loads, sourcing at least 2.0mA. This current should be constant for best performance of the D/A converter.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR output change per percent of change in either the positive, negative, or logic supply voltages about the nominal voltages. Figure 1 shows typical power supply rejection versus power supply ripple frequency.

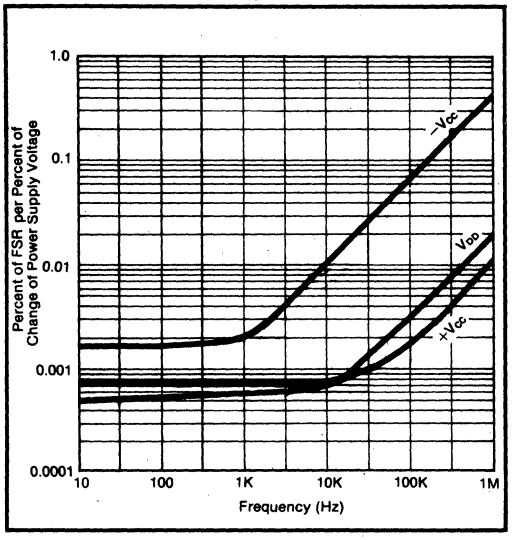


FIGURE 1. Power Supply Rejection versus Power Supply Ripple Frequency.

OPERATION

DAC811 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 2.

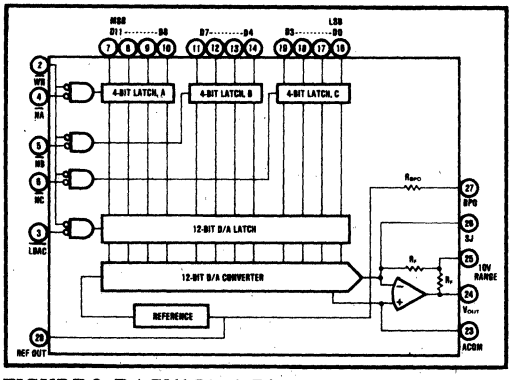


FIGURE 2. DAC811 Block Diagram.

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic "0". When either $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) or $\overline{WR}$ go to logic "1", the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic "0".

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic "0". When either $\overline{LDAC}$ or $\overline{WR}$ are at logic "1", the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic "0".

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for all latches is given in Table II.

TABLE II. DAC811 Interface Logic Truth Table.

$\overline{WR}$	$\overline{N_A}$	$\overline{N_B}$	$\overline{N_C}$	$\overline{LDAC}$	OPERATION
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4MSB's
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4 LSB's
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the Offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table III for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

±12V OPERATION

The DAC811 is fully specified for operation on ±12V power supplies. However, in order for the output to

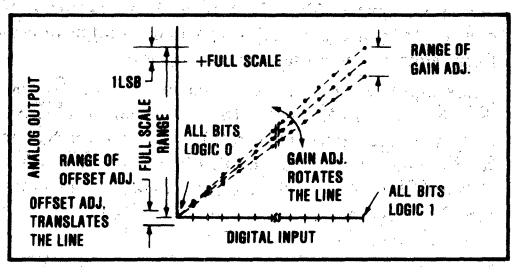


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter

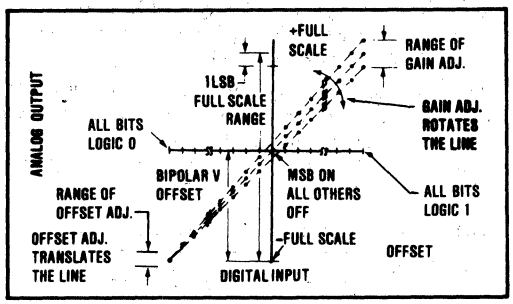


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

TABLE III. Digital Input/Analog Output, $\pm V_{CC} = \pm 15V$.

DIGITAL INPUT	ANALOG OUTPUT VOLTAGE		
	0 to +10V	±5V	±10V
12-Bit Resolution MSB ↓ LSB ↓			
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5.0000V	0.0000V	0.0000V
011111111111	+4.9976V	−0.0024V	−0.0049V
000000000000	0.0000V	−5.0000V	−10.0000V
1LSB	2.44mV	2.44mV	4.88mV

swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12V supplies, the output swing should be restricted to ±8V in order to meet specifications.

LOGIC INPUT COMPATIBILITY

The DAC811 digital inputs are TTL, LSTTL, and 54/74HC CMOS-compatible over the operating range of V_{DD}. The input switching threshold remains at the TTL threshold over the supply range.

The logic input current over temperature is low enough to permit driving the DAC811 directly from the outputs of 4000B and 54/74C CMOS devices.

INSTALLATION

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram, Figure 5. These capacitors (1μF tantalum recommended) should be located close to the DAC811.

The DAC811 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The Analog Common (pin 23) and Digital Common (pin 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output, therefore, some caution is required in applying these common connections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

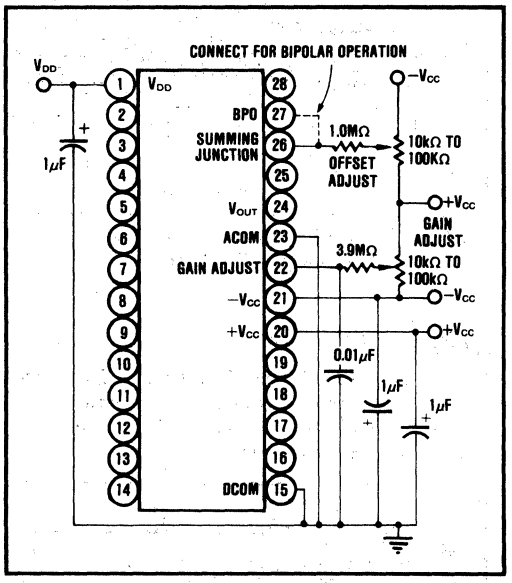


FIGURE 5. Power Supply, Gain, and Offset Potentiometer Connections.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 5. TCR of the potentiometers should be 100 ppm/°C or less. The 1.0MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the DAC811 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pickup in all applications, including those not employing external gain adjustment.

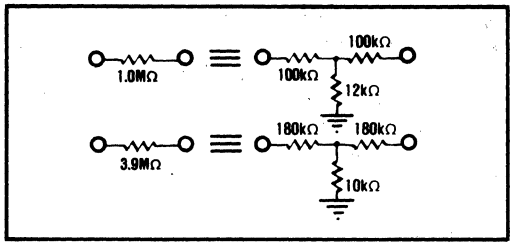


FIGURE 6. Equivalent Resistances.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC811 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 7. Connections for the output ranges are listed in Table IV.

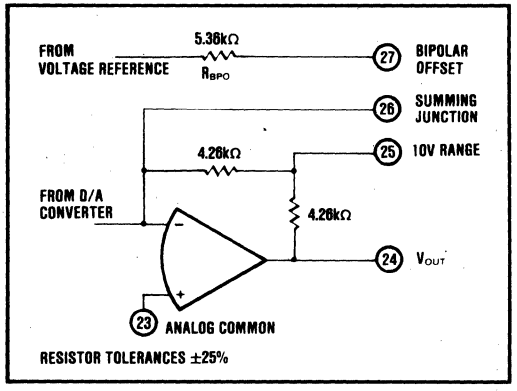


FIGURE 7. Output Amplifier Voltage Range Scaling Circuit.

Table IV. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 25 To	Connect Pin 27 To
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC811 interface logic allows easy interface microcomputer bus structures. The control signal $\overline{WR}$ is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{LDAC}$ determine which of the latches are enabled. It is permissible to enable two or more latches simultaneously as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC811's and later strobed into the D/A latch of all D/A's simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are unused, the base address decoder can be simplified or eliminated altogether. For instance if half the memory space is unused, address line A_{15} of the microcomputer can be used as the chip select control.

4-BIT INTERFACE

An interface to a 4-bit microcomputer is shown in Figure 8. Each DAC811 occupies four address locations. A 74LS139 provides the two to four decoder and selects these with the base address. Memory Write ($\overline{WR}$) of the microcomputer is connected directly to the $\overline{WR}$ pin of the DAC811. A 8205 decoder is an alternative device to use instead of the 74LS139.

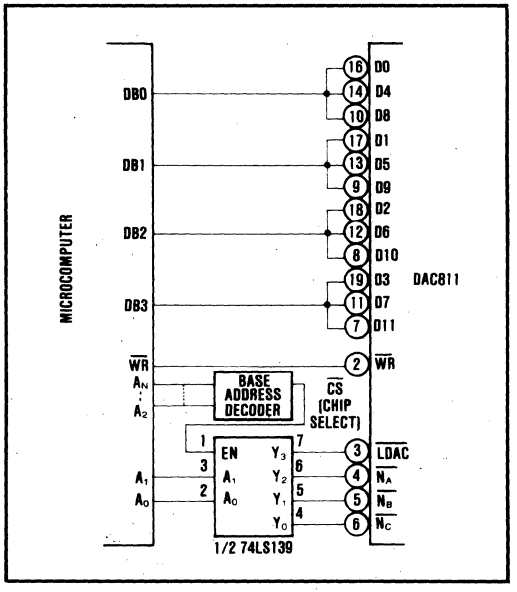


FIGURE 8. Addressing and Control for 4-Bit Microcomputer Interface.

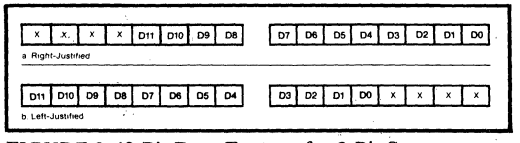


FIGURE 9. 12-Bit Data Formats for 8-Bit Systems.

8-BIT INTERFACE

The control logic of DAC811 permits interfacing to right- or left-justified data formats illustrated in Figure 9. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figures 10 and 11 show an addressing scheme for right-justified and left-justified data respectively. The base address is decoded from the high-order address bits. A_0 and A_1 address the appropriate latches. Note that adjacent addresses are

used. For the right-justified case $X10_{16}$ loads the 8 LSB's and $X01_{16}$ loads the 4MSB's and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{16}$ and $X11_{16}$ are not used.

Left-justified data is handled in a similar manner, shown in Figure 11. The DAC811 still occupies two adjacent locations in the microcomputer's memory map.

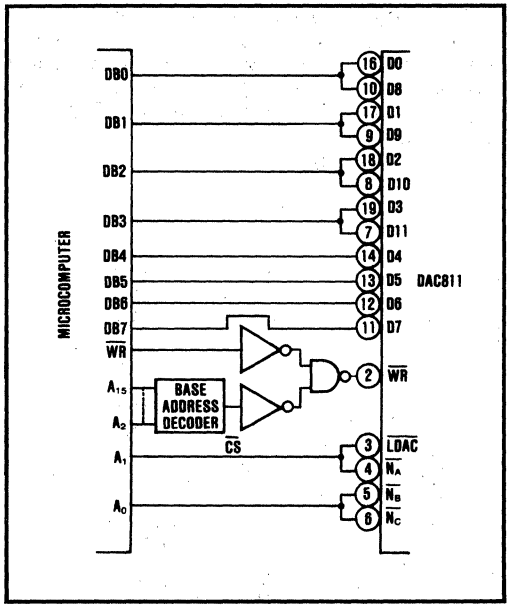


FIGURE 10. Right-Justified Data Bus Interface.

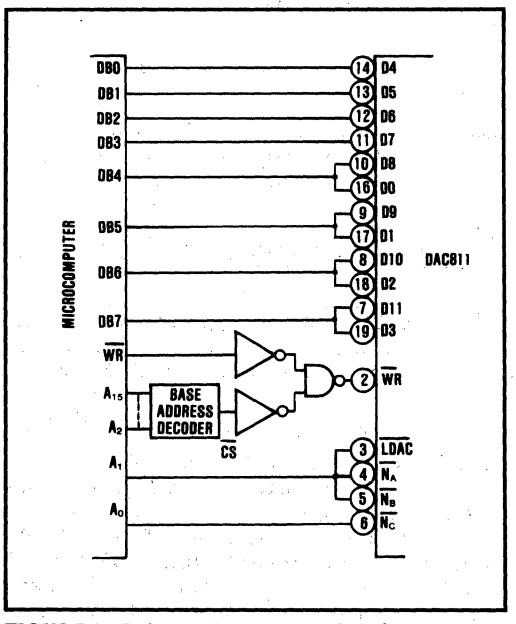
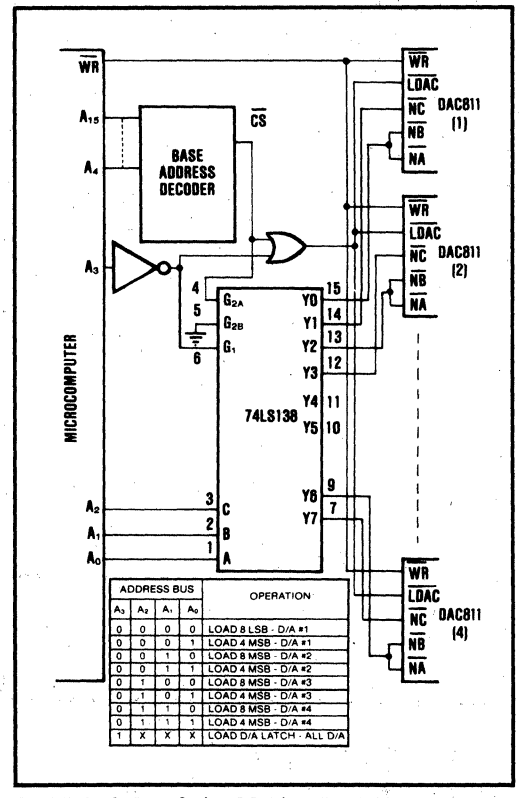


FIGURE 11. Left-Justified Data Bus Interface.

INTERFACING MULTIPLE DAC811's IN 8-BIT SYSTEMS

Many applications require that the outputs of several D/A converters be updated simultaneously such as automatic test systems. The interface shown in Figure 12 uses a 74LS138 decoder to decode a set of eight adjacent addresses to load the input latches of four DAC811's. The example shows a right-justified data format.

A ninth address using A_3 causes all DAC811's to be updated simultaneously. If a particular DAC811 is always loaded last, for instance, D/A #4, A_3 is not needed, thus saving 8 address spaces for other uses. Incorporate A_3 into the Base Address Decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{N_C}$ of D/A #4, and connect G1 of the 74LS138 to +5V.



ADDRESS BUS				OPERATION
A_3	A_2	A_1	A_0	
0	0	0	0	LOAD 8 LSB - D/A #1
0	0	0	1	LOAD 4 MSB - D/A #1
0	0	1	0	LOAD 8 MSB - D/A #2
0	0	1	1	LOAD 4 MSB - D/A #2
0	1	0	0	LOAD 8 MSB - D/A #3
0	1	0	1	LOAD 4 MSB - D/A #3
0	1	1	0	LOAD 8 MSB - D/A #4
0	1	1	1	LOAD 4 MSB - D/A #4
1	X	X	X	LOAD D/A LATCH - ALL D/A

FIGURE 12. Interfacing Multiple DAC 811's to an 8-Bit Bus.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines, $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC 811, is selected by the address decoder and strobed by $\overline{WR}$.

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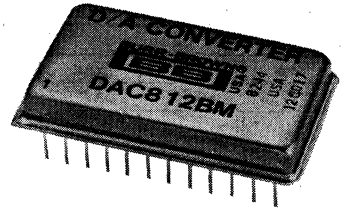
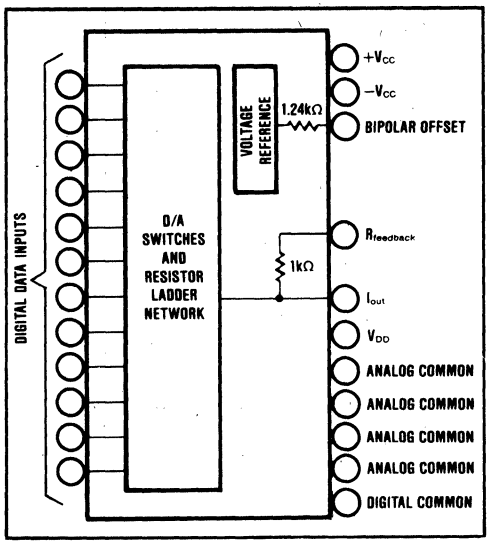


DAC812

Ultra-High Speed DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION AND ACCURACY
- 55nsec CURRENT OUTPUT SETTLING TIME
- TTL-COMPATIBLE INPUTS
- MONOTONIC OVER ENTIRE TEMPERATURE RANGE
- LINEARITY ERROR LESS THAN ±1/2LSB OVER TEMPERATURE RANGE (C GRADE)
- HERMETIC METAL PACKAGE



DESCRIPTION

The DAC812 is an ultra-fast-settling 12-bit current-output D/A converter with TTL-compatible inputs packaged in a 24-pin dual-wide dual-in-line hermetic metal package.

The current output settles to ±0.012% of full scale range in 55nsec, typical (65nsec, max., C grade; 80nsec, max., B grade).

The DAC812 utilizes a monolithic 12-bit switch chip with stable, compatible thin-film resistors to achieve fast settling time and excellent stability over temperature and time. An internal applications resistor for use with an external op amp is included to convert the output current into a voltage for 0V to +10V or −5V to +5V ranges.

An output voltage compliance range of +4V to −4V allows the generation of an output voltage without using an external output amplifier.

The DAC812 comes in two drift grades. The linearity error of the C grade is guaranteed to be within ±1/2LSB over the temperature range of −25°C to +85°C. Gain drift of the C grade is ±20ppm/°C (max) and bipolar offset drift is ±10ppm of FSR/°C (max). The B grade has a linearity error of ±1LSB over the temperature range and a maximum gain drift and bipolar offset drift of ±40ppm/°C and ±15ppm/°C, respectively.

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SPECIFICATIONS

ELECTRICAL

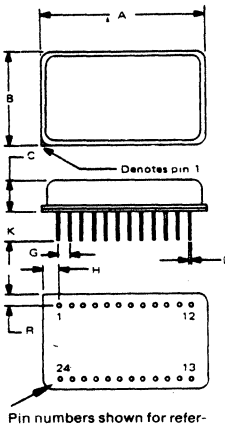
At $T_A = +25°C$, rated power supplies, and after 5-minute warm-up unless otherwise noted.

MODEL	DAC812CM			DAC812BM			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution; CSB, COB			12			*	Bits
Logic Inputs: V_{IH}	+2.0		+5.25	*		*	V
V_{IL}	0.0		+0.8	*		*	V
I_{IH}, $V_I = +2.7V$			+20			*	µA
I_{IL}, $V_I = +0.4V$			−800			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±0.006	±0.012		±0.009	±0.018	% of FSR[1]
Differential Linearity Error			±0.012			±0.018	% of FSR
Gain Error[2]		±0.03	±0.1		*	*	%
Offset Error[2]: Unipolar		±0.02	±0.04		*	*	% of FSR
Bipolar		±0.03	±0.1		*	*	% of FSR
Monotonicity Temp. Range (min)	−25		+85	*		*	°C
CONVERSION SPEED							
Settling Time to ±1/2LSB into 150Ω							
For FSR Change		55	65		*	80	nsec
For 1LSB Change		25			*		nsec
DRIFT							
Gain		±10	±20		±20	±40	ppm/°C
Offset: Unipolar		±0.25	±0.5		±0.5	±1	ppm of FSR/°C
Bipolar			±10			±15	ppm of FSR/°C
Linearity Error	±0.012 over Temp. Range (max)			±0.025 over Temp. Range (max)			% of FSR
Differential Linearity Error	±0.025 over Temp Range (max)			±0.04 over Temp. Range (max)			% of FSR
OUTPUT							
ANALOG OUTPUT							
Output Current: Unipolar		0 to −10			*		mA
Bipolar		−5 to +5			*		mA
Output Voltage Ranges							
with External Op Amp: Unipolar		0 to +10			*		V
Bipolar		−5 to +5			*		V
Output Impedance: Unipolar		170			*		Ω
Bipolar		150			*		Ω
Output Compliance	−4		+4	*		*	V
POWER SUPPLIES							
Power Supply Sensitivity: $+V_{CC}$			±0.004			*	%FSR/%V_{CC}
$-V_{CC}$			±0.001			*	%FSR/%V_{CC}
V_{DD}			±0.0002			*	%FSR/%V_{DD}
Power Supply Voltages: $+V_{CC}$	+14	+15	+18	*	*	*	V
$-V_{CC}$	−18	−15	−14	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	V
Power Supply Current: $+V_{CC}$		+30	+40		*	*	mA
$-V_{CC}$		−40	−50		*	*	mA
V_{DD}		+25	+40		*	*	mA
Power Dissipation		1.2	1.6		*	*	W
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−55		+150	*		*	°C
PACKAGE	24-pin Hermetic Metal 0.6" Pin Row Spacing						

*Specification the same as for DAC812CM.

NOTES: (1) FSR is full scale range. (2) Adjustable to zero with external potentiometer.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

Pin numbers shown for reference only. Numbers may not be marked on package.

PIN ASSIGNMENTS

Pin	Function	Pin	Function
1	Bit 1 (MSB, Data Input)	14	Digital Common (V_{DD} Common)
2	Bit 2	15	Analog Common ($\pm V_{CC}$ Common)
3	Bit 3	16	Analog Common
4	Bit 4	17	Analog Common
5	Bit 5	18	Analog Common
6	Bit 6	19	V_{DD} (Logic Supply)
7	Bit 7	20	I_{OUT} (Current Output)
8	Bit 8	21	R_f (Application Resistor)
9	Bit 9	22	BPO (Bipolar Offset)
10	Bit 10	23	$-V_{CC}$ (Negative Analog Supply)
11	Bit 11	24	$+V_{CC}$ (Positive Analog Supply)
12	Bit 12 (LSB)		
13	No connection		

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a D/A converter is one of the true measures of its performance. The linearity error of the DAC812 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB (±1LSB for the BM model) from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of −25°C to +85°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a −25°C to +85°C range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by 1) testing the end point differences for the DAC812 at t_{min}, +25°C, and t_{max}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications (includes internal reference).

Offset Drift is a measure of the actual change in output around the minus full-scale point over the specified temperature range. The offset is measured at t_{min}, +25°C, and t_{max}. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of the DAC812 is ±4.0V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages. To insure precision operation, each supply lead should be bypassed to ground as close to the unit as possible with a 1μF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC812 (pins 14, 15, 16, 17, and 18). In order to preserve the stated linearity and accuracy specifications it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these five pins and the actual ground reference point will degrade the performance of the DAC812. To achieve fast settling performance it is recommended that pins 14 through 18 be returned directly to a ground plane (see Figure 1). The analog ground should be located as close to the DAC812 as possible. Otherwise, the accuracy will be degraded by the voltage drop in the ground lines.

SETTLING TIME

Settling time for the DAC812 is the total time required for the output to settle within an error band around its

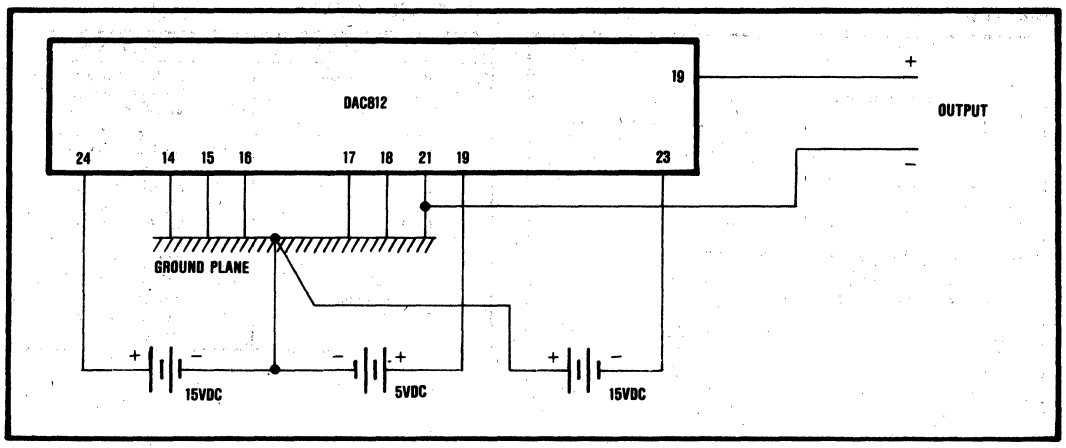


FIGURE 1. DAC812 Grounding Using Feedback Resistor to Generate Output Voltage.

final value after a digital input change. This time includes the digital delay of the internal switches.

Figure 2 shows a typical settling time curve of the DAC812 versus output error. This curve is for full-scale digital code changes. Figures 3 and 4 show typical measured settling time characteristics of the DAC812.

In order to achieve the minimum settling time, it is necessary to observe the following good high frequency construction techniques.

1. The power supplies should be bypassed by 1μF CS-type tantalum capacitors.
2. Use a ground plane to connect common ground points.
3. Remove the ground plane from underneath signal lines where it would add capacitance.
4. Keep analog and digital signal lines physically separated to avoid coupling of the digital signal into the analog paths.

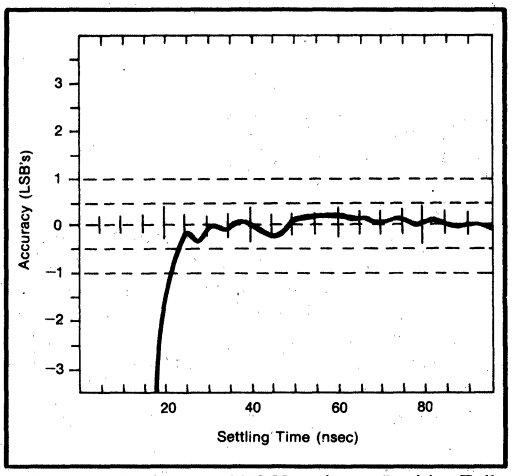


FIGURE 3. Typical DAC812 Negative-to-Positive Full-Scale Output Characteristic.

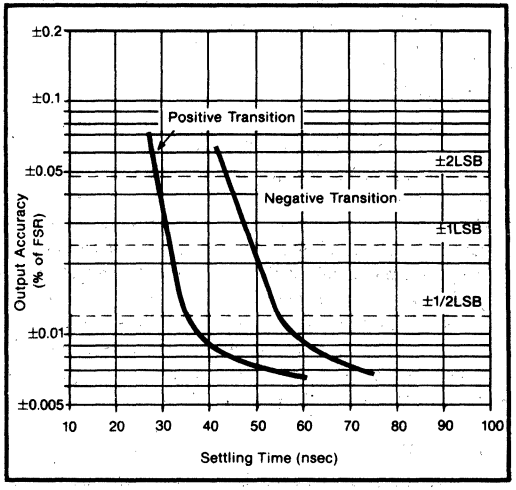


FIGURE 2. DAC812 Typical Settling Time vs. Accuracy

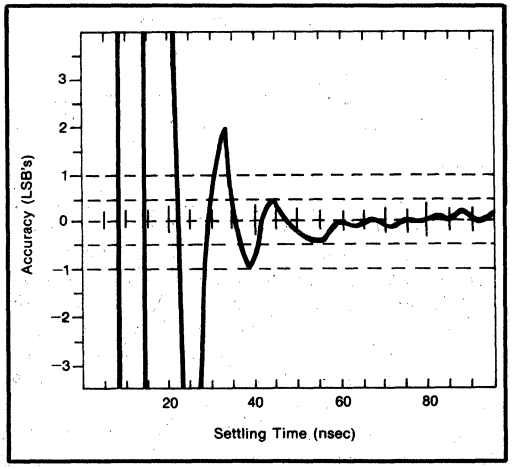


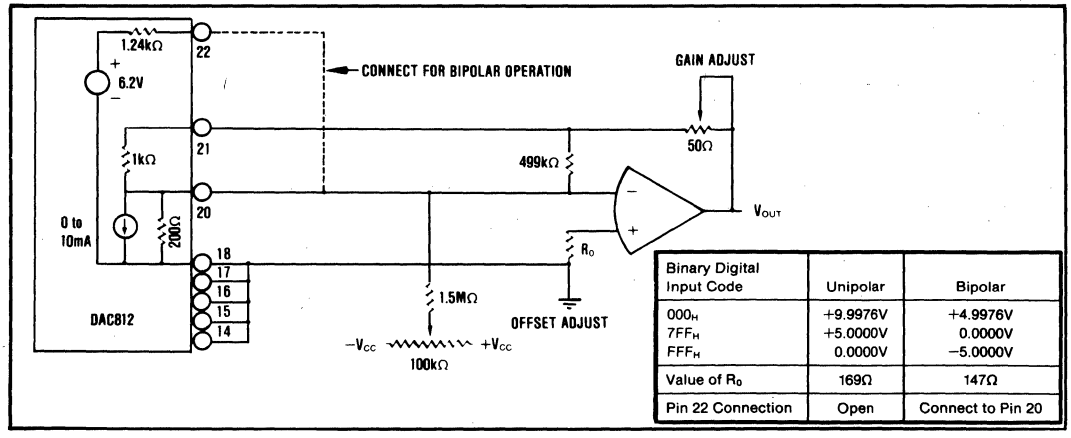
FIGURE 4. Typical Positive-to-Negative Full-Scale Output Characteristic.

5. Bring the source of the digital driving signal as close to the inputs of the DAC812 as possible. If the digital inputs are not clean it will be necessary to reshape them using registers or line drivers. It is recommended that the logic power line be bypassed near the digital logic circuitry as a further measure to achieve clean signals.
6. If possible, the DAC812 should be soldered directly into the printed circuit board since connector lead length will cause ringing in the output.

OUTPUT CONFIGURATIONS AND APPLICATIONS INFORMATION

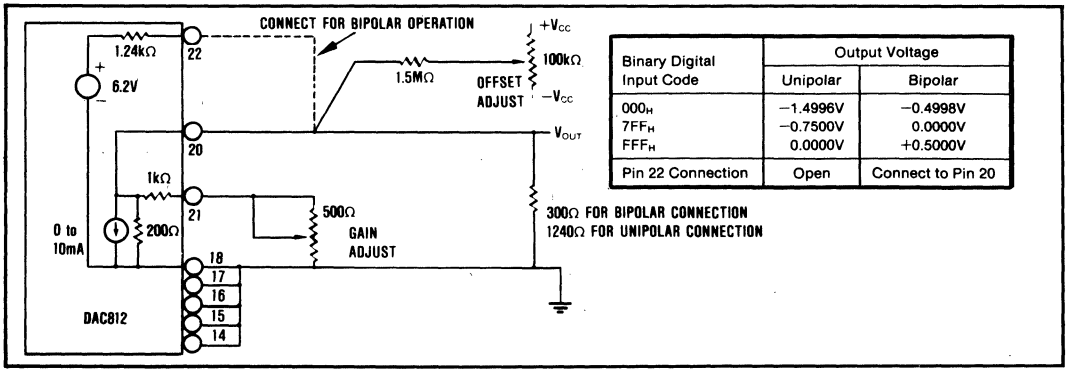
The DAC812 contains a 1.24kΩ resistor for generating the bipolar offset current and a 1kΩ resistor which is primarily used as the feedback resistor when used with an external op amp. This thin-film network is constructed on sapphire to provide excellent temperature tracking capability inherent in thin-film networks. These internal resistors along with other internal resistors cause the DAC812 output, in any mode, to be a ratiometric product of the reference. The feedback resistor has very low power sensitivity so that linearity is maintained independent of digital code changes. Because this resistor is constructed on a sapphire network, it is possible to have both superior tracking and low capacitance. Figure 5 shows the DAC812 connected to an external op amp in unipolar and bipolar modes. When the op amp is a Burr-Brown model OPA600 it is possible to achieve settling times to ±0.1% accuracy in 150nsec. Many of the output accuracy and linearity specifications are given when connected to an external op amp.

For highest speed operation, the DAC812 should be used without an external op amp. Figure 6 shows how to connect the DAC812 for bipolar and unipolar operation. Figure 7 illustrates how to connect the DAC812 to construct a fast A/D converter.



Binary Digital Input Code	Unipolar	Bipolar
000_H	+9.9976V	+4.9976V
$7FF_H$	+5.0000V	0.0000V
FFF_H	0.0000V	−5.0000V
Value of R_o	169Ω	147Ω
Pin 22 Connection	Open	Connect to Pin 20

FIGURE 5. Bipolar and Unipolar Output Connections with External Op Amp.



Binary Digital Input Code	Output Voltage	
	Unipolar	Bipolar
000_H	−1.4996V	−0.4998V
$7FF_H$	−0.7500V	0.0000V
FFF_H	0.0000V	+0.5000V
Pin 22 Connection	Open	Connect to Pin 20

FIGURE 6. Bipolar and Unipolar Output Connection with Resistor Load Only.

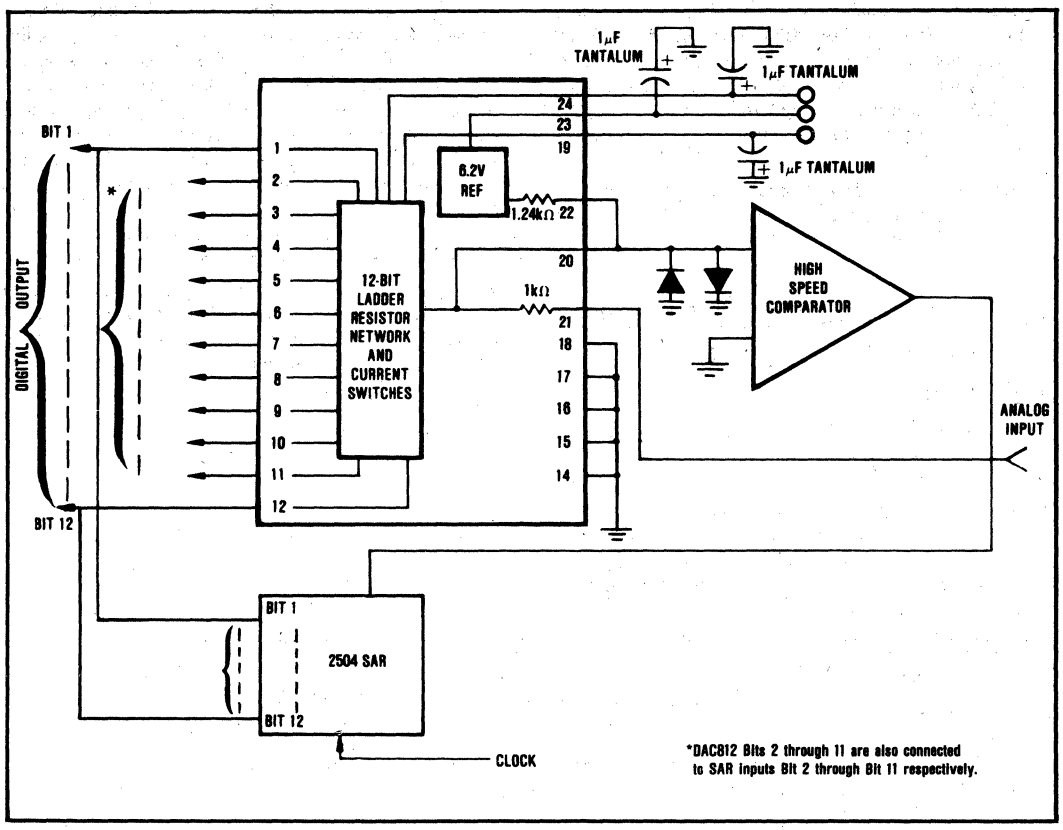


FIGURE 7. DAC812 Used in a Fast A/D Converter.

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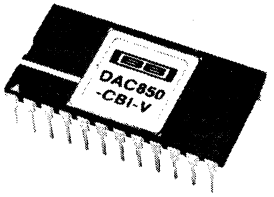
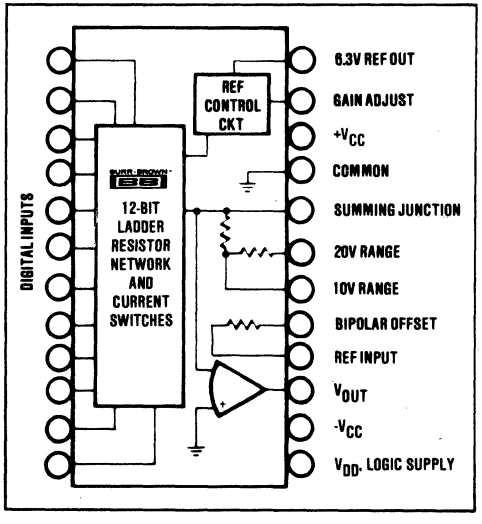


DAC850
DAC851

Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST HIGH RELIABILITY SINGLE-CHIP REPLACEMENT FOR DAC85 AND DAC87
- 12-BIT RESOLUTION
- HIGH ACCURACY: ±1/2LSB max nonlinearity
  −25°C to +85°C (DAC850)
  −55°C to +125°C (DAC851)
- GUARANTEED MONOTONICITY
- DUAL-IN-LINE HERMETIC PACKAGE WITH SIDE-BRAZED PINS
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES



DESCRIPTION

The DAC850 and DAC851 are 12-bit single-chip (current output model) digital-to-analog converters for use in wide temperature high reliability applications.

The DAC850 and DAC851 are packaged in a hermetically-sealed package with side-brazed pins. The DAC850 is specified with a linearity error of ±1/2LSB over -25°C to +85°C and the DAC851 has a linearity error of ±3/4LSB over -55°C to +125°C. Both converters have guaranteed monotonicity over their specification temperature range. The current output configuration of these D/A converters is a single-chip integrated circuit containing a subsurface zener reference diode, high-speed current switches, and laser-trimmed thin-film resistors.

The DAC850 and DAC851 provide output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5 and 0 to +10V (V models) or output current ranges of ±1.175mA or 0 to -2.35mA (I models).

Patents pending may apply upon the allowance and issuance of patents thereon. The product may also be covered in other countries by one or more international patents.

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SPECIFICATIONS

ELECTRICAL

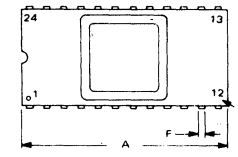
At 25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

MODEL	DAC850-CBI			DAC851-CBI			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT							
DIGITAL INPUT							
Resolution			12			12	Bits
Logic Levels (LSTTL Compatible)[1]							
Logic "1" (at +20μA)	+2		+5.5	+2		+5.5	VDC
Logic "0" (at 0.36mA)	0		+0.8	0		+0.8	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±1/4	±1/2		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	+1, −3/4		±1/2	+1, −3/4	LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	%
Offset Error[2]		±0.05	±0.15		±0.05	±0.15	% of FSR[3]
Power Supply Sensitivity							
+15V and +5V Supplies		±0.0001	±0.001		±0.0001	±0.001	% of FSR/%V_{CC}
−15V Supply		±0.003	±0.006		±0.003	±0.006	% of FSR/%V_{CC}
DRIFT[4] (over spec. temp range)							
Bipolar Drift							
(± full scale drift for the bipolar connection)		±5	±17		±15	±30	ppm of FSR/°C
Total Error[5]: Unipolar		±0.1	±0.20		±0.15	±0.30	% of FSR
Bipolar		±0.06	±0.12		±0.15	±0.30	% of FSR
Gain		±10	±20		±10	±25	ppm/°C
Offset: Unipolar		±1	±3		±1	±3	ppm of FSR/°C
Bipolar		±5	±10		±5	±15	ppm of FSR/°C
Differential Linearity (over spec. temp range)		±1/2	±1		±1/2	±1	LSB
Linearity Error (over spec. temp. range)			±1/2			±1/2	LSB
Monotonicity Temp. Range, min	−25		+85	−55		+125	°C
CONVERSION SPEED							
V Model (settling time to ±0.01% of FSR)							
For FSR Change: 20V Range, 2kΩ Load		3	5		3	5	μsec
10V Range, 2kΩ Load		2.5	4		2.5	4	μsec
For 1LSB Change, Major Carry, 2kΩ Load		1.5			1.5		μsec
Slew Rate, 2kΩ Load	10	15		10	15		V/μsec
I Model (settling time to ±0.01% of FSR)							
For FSR Change: 10Ω to 100Ω Load		300			300		nsec
1kΩ Load		1			1		μsec
OUTPUT							
ANALOG OUTPUT							
V Model							
Ranges (±V_{CC} = 15V)[6]	±2.5, ±5, ±10, 0 to +5, 0 to +10			±2.5, ±5, ±10, 0 to +5, 0 to +10			V
Output Current	±5			±5			mA
Output Impedance (DC)		0.05			0.05		Ω
Short Circuit to Common, Duration		Indefinite			Indefinite		
I Model							
Ranges	±0.88, 0 to −1.76	±1.175, 0 to −2.35	±1.47, 0 to −2.94	±0.88, 0 to −1.76	±1.175, 0 to −2.35	±1.47, 0 to −2.94	mA
Output Impedance: Bipolar	2.5	3.1	3.7	2.5	3.1	3.7	kΩ
Unipolar	5.8	7.2	8.6	5.8	7.2	8.6	kΩ
Compliance	−2.5		+2.5	−2.5		+2.5	V
POWER SUPPLIES AND REFERENCE							
Reference Voltage Output	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	V
Current (for external loads), Source	1.5	2.5		1.5	2.5		mA
Temperature Coefficient of Drift		±10	±20		±10	±25	ppm/°C
Power Supply Requirements: ±V_{CC}	±11.4	±15	±16.5	±11.4	±15	±16.5	VDC
V_{DD}[7]	+4.5	+5	+16.5	+4.5	+5	+16.5	VDC
Power Supply Drain: ±V_{CC} (no load)		+8, −20	+12, −25		+8, −20	+12, −25	mA
V_{DD} (logic supply)		+7	+10		+7	+10	mA
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	°C
PACKAGE	24-pin hermetic DIP side-brazed ceramic						

NOTES:

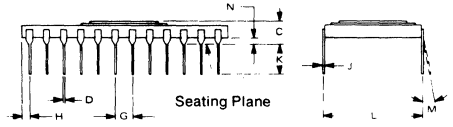
1. Adding external CMOS hex buffers CD 4049A/4050A will provide CMOS input compatibility. Refer to Logic Input Compatibility section.
2. Adjustable to zero with external trim potentiometer.
3. FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
4. To maintain drift spec internal feedback resistors must be used for current output models.
5. Includes the effects of gain, offset and linearity drift. Gain and offset errors are adjusted to zero at +25°C.
6. A minimum of ±13V supplies is required for ±10V and 0 to +10V ranges. All other ranges accept ±12V supplies.
7. Power dissipation is an additional 100mW, max, when V_{DD} is operated at +15V.

MECHANICAL



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	–	10°		10°
N	.025	.060	0.64	1.52

NOTE:
Metal Cap connected to -Vcc internally.

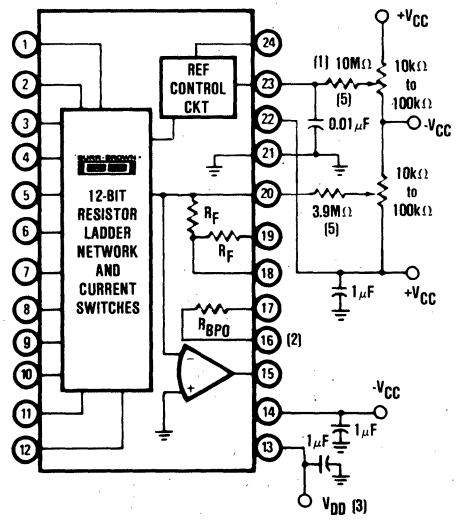
CASE: Ceramic
MATING CONNECTOR: 0245MC
WEIGHT: 8.4 grams (0.3oz.)

PIN ASSIGNMENTS

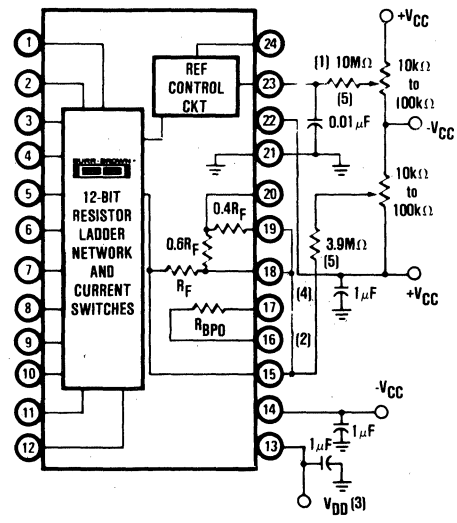
I MODELS	PIN NO.	V MODELS
(MSB) BIT 1	1	BIT 1 (MSB)
BIT 2	2	BIT 2
BIT 3	3	BIT 3
BIT 4	4	BIT 4
BIT 5	5	BIT 5
BIT 6	6	BIT 6
BIT 7	7	BIT 7
BIT 8	8	BIT 8
BIT 9	9	BIT 9
BIT 10	10	BIT 10
BIT 11	11	BIT 11
(LSB) BIT 12	12	BIT 12 (LSB)
LOGIC SUPPLY, V_{DD}	13	LOGIC SUPPLY, V_{DD}
-Vcc	14	-Vcc
Iout	15	Vout
REF. INPUT	16	REF. INPUT
BIPOLAR OFFSET	17	BIPOLAR OFFSET
SCALING NETWORK	18	10V RANGE
SCALING NETWORK	19	20V RANGE
SCALING NETWORK	20	SUMMING JUNCTION
COMMON	21	COMMON
+Vcc	22	+Vcc
GAIN ADJUST	23	GAIN ADJUST
6.3V REF. OUT	24	6.3V REF. OUT

CONNECTION DIAGRAMS

Voltage Model



Current Model



NOTES:

1. **DAC850/851 use a 10MΩ resistor. These models can replace the DAC85 which uses an 18MΩ resistor and the DAC87 which uses a 33MΩ resistor.**
2. **Pin 16 of DAC850/851 is used only to connect the bipolar offset resistor. An external reference voltage may not be used with DAC850/851.**
3. **If connected to +V_{CC}, which is permissible, power dissipation increases 75mW typ., 100mW max.**
4. **For fastest settling time connect pins 19, 18, and 15 together.**
5. **Values shown are for ±15V supplies. For supplies below ±13.5V use 2.7MΩ in place of 3.9MΩ and 7.5MΩ in place of 10MΩ.**

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC850 and DAC851 accept complementary binary digital input codes. They may be connected by the user for any one of three complementary codes; CSB, CTC, or COB (see Table I).

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	Midscale -1LSB	-1LSB	+Full Scale
111111111111	Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specification temperature range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm °C). Gain drift is established by: 1) testing the end point differences at -25°C, +25°C, and +85°C for the DAC850 and at -55°C, +25°C, and +125°C for the DAC851; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This is expressed in ppm °C.

Offset drift is a measure of the actual change in output with all "1"s on the input over the specification temperature range. The offset is measured at -25°C, +25°C, and +85°C for the DAC850 and at -55°C, +25°C, and +125°C for the DAC851. The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per °C (ppm of FSR °C).

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

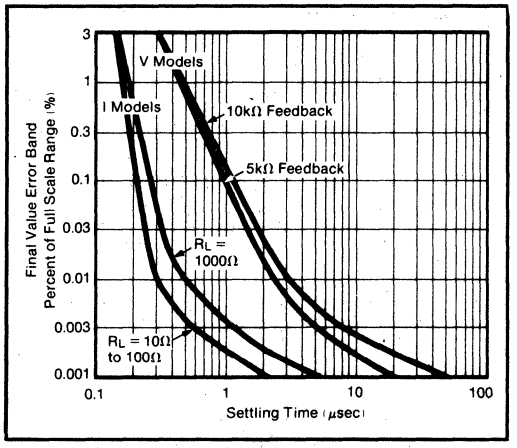


FIGURE 1. Full Scale Range Settling Time vs Final Value Error Band.

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω. Internal resistors are provided for connecting a nominal load resistance of approximately 1000Ω for output voltage ranges of ±1V and 0 to -2V.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is +2.5V to -2.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

REFERENCE SUPPLY

All models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also. The external current drain is limited to sourcing 2.5mA up to +85°C and 1mA up to +125°C not including current required by the bipolar offset circuit.

An external buffer amplifier is recommended if this reference will be used to drive other system components because variations in a load driven from the reference will result in bipolar offset variations of the D/A converter. Gain and bipolar offset adjustments should be made under constant load conditions.

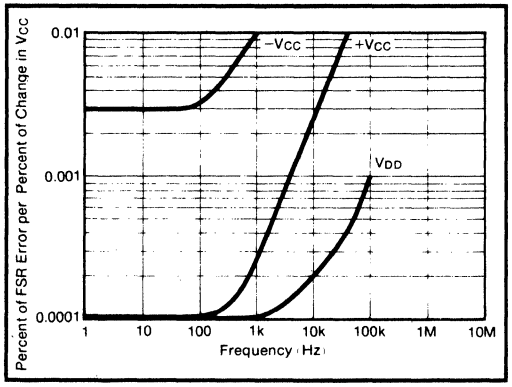


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the case. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance. The metal cap on the top of the package is connected internally to $-V_{CC}$.

±12 VOLT OPERATION

The DAC850 and DAC851 are fully specified for operation on ±12V power supplies; however, to use the ±10V and 0 to +10V ranges of the voltage output models, the power supplies must be ±13V or greater. All other voltage output ranges and all current output ranges provide satisfactory operation with ±11.4V supplies. The supplies should be balanced to obtain optimum performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the case to prevent noise pickup. For operation with supplies of less than ±13.5V, use 2.7MΩ and 7.5MΩ resistors in place of the 3.9MΩ and 10MΩ resistors, respectively. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. Figures 4 and 5 illustrate the relationship of offset and main adjustments to unipolar and bipolar D/A converter output.

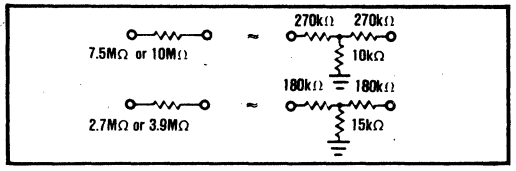


FIGURE 3. Equivalent Resistances.

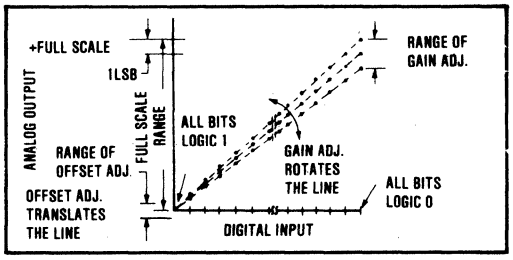


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

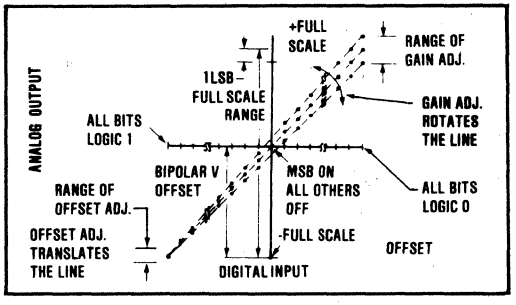


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

TABLE II. Digital Input/Analog Output.

DIGITAL INPUT	ANALOG OUTPUT			
	VOLTAGE*		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC850 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

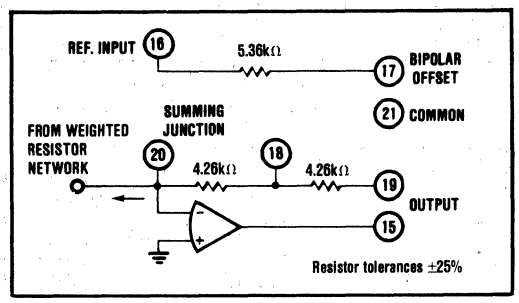


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full scale range change is specified as 3μsec for the 20 volt range and 2.5μsec for the 10 volt range.

TABLE III. Output Voltage Range Connections - Voltage Model.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8. It is important to note that there is a relationship between the tolerances of the current source and the scaling resistors. The magnitude of the tolerance tracks very closely but with opposite sign. The tolerance of the internal resistance of the converter (7.2kΩ unipolar, 3.07kΩ bipolar) tracks the tolerance of the scaling resistors in sign and approximately proportionately in magnitude. That is, if the scaling resistors are high by 10%, the internal impedance is high by about 8%.

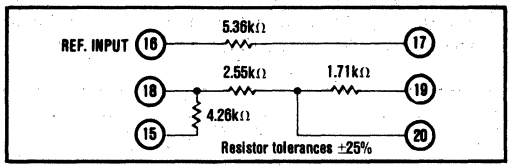


FIGURE 7. Internal Scaling Resistors.

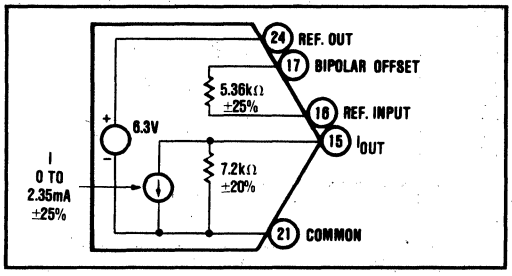


FIGURE 8. Current Output Model Equivalent Output Current.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a low drift direct voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2.35mA \left(\frac{R_L \times 7.2k\Omega}{R_L + 7.2k\Omega} \right)$$

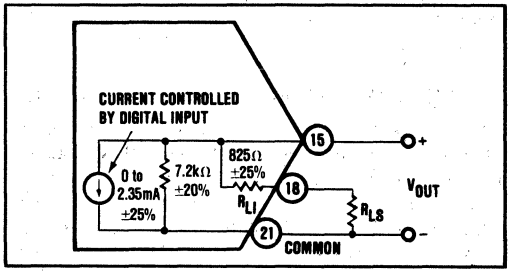


FIGURE 9. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. Tolerances on internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 10, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1.175mA\left(\frac{R_L \times 3.17k\Omega}{R_L + 3.17k\Omega}\right)$$

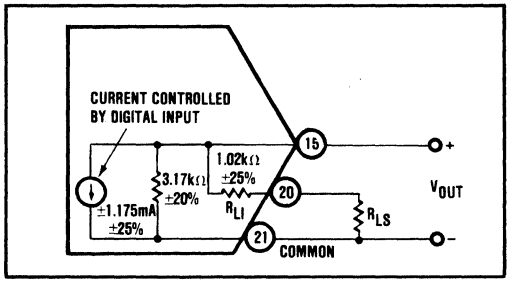


FIGURE 10. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

To achieve specified drift, connect the 1.71kΩ and 2.55kΩ internal scaling resistors in parallel (R_{LI}) and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. The tolerances on the equivalent internal resistors are wide. R_{LS} will have to be selected for each unit.

Driving An External Op Amp

The current output model will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage (see Figure 11).

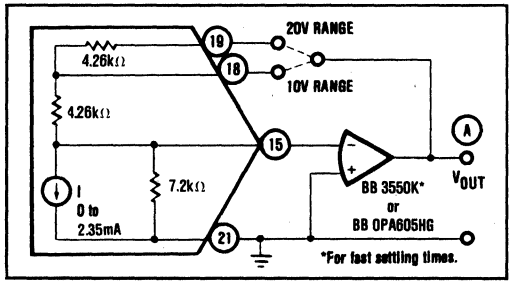


FIGURE 11. External Op Amp - Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model provides output voltage ranges the same as the voltage model. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output D/A Converter.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1.175mA for bipolar voltage ranges and -2.35mA for unipolar voltage ranges (see Figure 12). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.

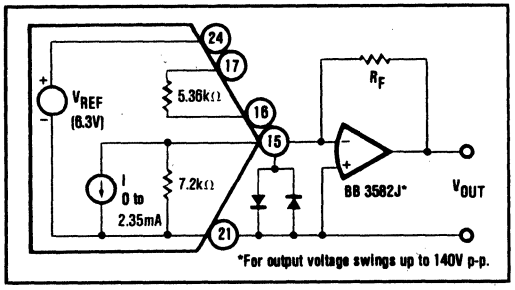


FIGURE 12. External Op Amp - Using External Feedback Resistors.

LOGIC INPUT COMPATIBILITY

DAC850 and DAC851 digital inputs are TTL, LSTTL, 54/74HC CMOS compatible as shown in the specification table when V_{DD} is operated over 4.5 to 16.5 volts.

Figure 13 illustrates using CMOS hex buffers with DAC850 to provide CMOS input compatibility. This combination will operate together over a wide range of logic power supply voltages.

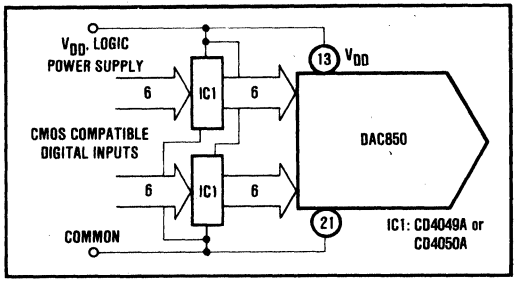
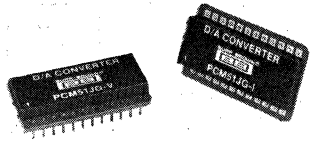


FIGURE 13. Using DAC850/851 with CMOS Hex Buffers Over a Wide Range of Logic Power Supply Voltages.

BURR-BROWN®

PCM51JG
DESIGNED FOR AUDIO



16-Bit
DIGITAL-TO-ANALOG CONVERTER

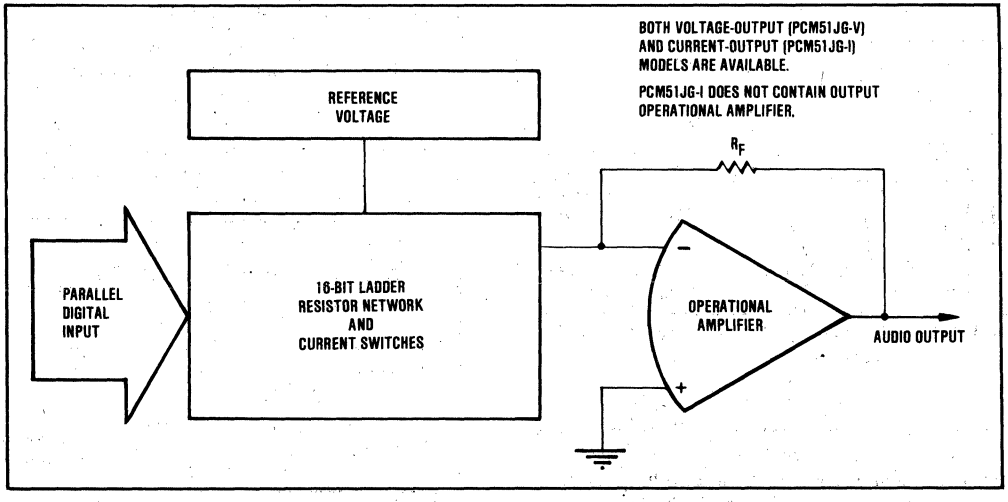
FEATURES

- 16-BIT RESOLUTION
- 350nsec SETTLING TIME, typ (I Model)
- 5μsec SETTLING TIME, typ (V Model)
- 0.006% OF FSR MAX DIFFERENTIAL LINEARITY ERROR (0.0025% typ)
- 0.0025% THD (FS Input, 16 Bits), typ
- 0.012% THD (-15dB, 16 Bits), typ
- 96dB DYNAMIC RANGE
- EIAJ STC-007 COMPATIBLE
- PIN COMPATIBLE - DAC71 & PCM50
- LOW COST

DESCRIPTION

The PCM51 is designed for PCM audio applications and is compatible with EIAJ STC-007 specifications. The PCM51 may be operated as either a 16-bit or a 14-bit converter. It features wide dynamic range, low differential linearity error, low distortion, and has a very-fast settling time.

The PCM51 contains an internal voltage reference. It uses state-of-the-art IC and laser-trimmed thin-film components. The converter combines high quality and high performance with low cost.



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SPECIFICATIONS

ELECTRICAL

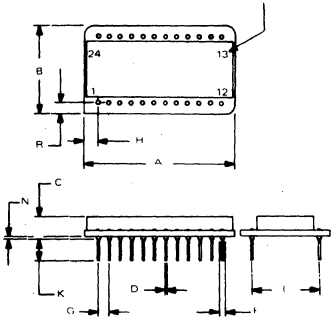
(T_A = +25°C and rated power supplies unless otherwise noted.)

MODEL	PCM51JG			
	MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Dynamic Range		96		dB
Logic Levels (TTL-Compatible)(1)				
Logic "1" at +40µA	+2.4		+5.5	VDC
Logic "0" at -1.6mA	0		+0.4	VDC
TRANSFER CHARACTERISTICS				
Gain Error		±0.1	±0.5	%
Bipolar Zero Error(2)		±10	±100	mV
Differential Linearity Error at Bipolar Zero		0.0025	0.006	% of FSR(3)
TOTAL HARMONIC DISTORTION(4)				
V_O = ±FS at f = 400Hz				
14-Bit Resolution		0.004		%
16-Bit Resolution		0.0025	0.005	%
V_O = -15dB at f = 400Hz				
14-Bit Resolution		0.023	0.06	%
16-Bit Resolution		0.012	0.04	%
V_O = -20dB at f = 400Hz				
14-Bit Resolution		0.04		%
16-Bit Resolution		0.025		%
V_O = -60dB at f = 400Hz				
14-Bit Resolution		4.2		%
16-Bit Resolution		1.9		%
DRIFT (Over Specified Temperature Range)				
Total Bipolar Drift (includes gain, offset, and linearity drift)		±25	±50	ppm of FSR/°C
SETTLING TIME (To ±0.006% of FSR)				
Voltage Model, PCM51JG-V				
Output: 20V Step		5		µsec
1LSB Step(5)		3		µsec
Slew Rate		20		V/µsec
Current Model, PCM51JG-I				
Output: 1mA Step				
10Ω to 100Ω load		350		nsec
1kΩ Load(6)		350		nsec
WARM-UP TIME	1			Min
OUTPUT				
ANALOG OUTPUT				
Voltage Model, PCM51JG-V				
Ranges		±10		V
		±5(7)		V
Output Current		±5		mA
Output Impedance (DC)		0.1		Ω
Short-Circuit Duration		Indefinite To Common		
Current Model, PCM51JG-I				
Range		±1		mA
Output Impedance		3		kΩ
POWER SUPPLY				
SENSITIVITY				
-15VDC		±0.02		% of FSR/% V_S
+15VDC		±0.002		% of FSR/% V_S
POWER SUPPLY REQUIRMENTS				
Voltage, V_S	±14.5,	±15	±15.5	VDC
Supply Drain, +15VDC (no load)		±25		mA
-15VDC		-40		mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating (derated specs)	-25		+85	°C
Storage	-55		+85	°C

MECHANICAL

NOTE: Leads in true position. Within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



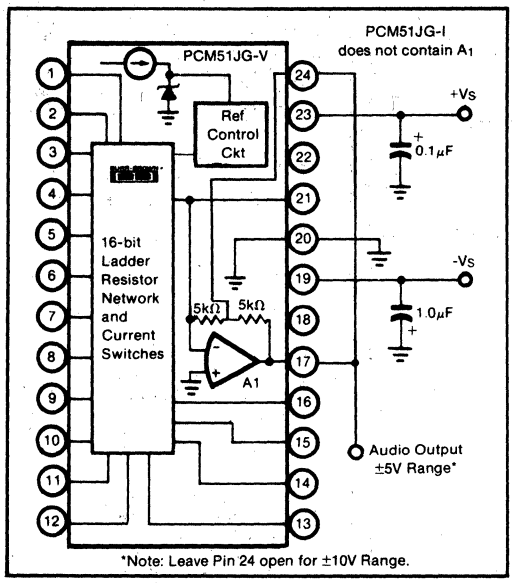
CASE: Black Ceramic
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

NOTES:

1. Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility. The percent change in output (V_O) as logic 0 varies from 0.0V to +0.4V and logic 1 changes from +2.4V to +5.0V on all inputs is less than 0.006% of FSR.
2. Adjustable to zero with external trim potentiometer.
3. FSR means Full Scale Range and is 20V for ±10V range and 10V for ±5V range.
4. The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. A block diagram of a measurement circuit is shown in Figure 3. Burr-Brown calculates THD from the measured linearity errors using equation (2) in the section on "Total Harmonic Distortion", and specifies that the maximum THD measured with the circuit shown in Figure 3 will be less than the limits indicated.
5. LSB is for 14-bit resolution.
6. Measured with an active clamp, as shown in Figure 10, to provide a low impedance for approximately 200nsec.
7. Connect pin 24 to pin 17 to obtain ±5V range.

CONNECTION DIAGRAM



PIN ASSIGNMENTS

Pin No.	PCM51JG-I	Pin No.	PCM51JG-V
1	Bit 1 (MSB)	1	Bit 1 (MSB)
2	Bit 2	2	Bit 2
3	Bit 3	3	Bit 3
4	Bit 4	4	Bit 4
5	Bit 5	5	Bit 5
6	Bit 6	6	Bit 6
7	Bit 7	7	Bit 7
8	Bit 8	8	Bit 8
9	Bit 9	9	Bit 9
10	Bit 10	10	Bit 10
11	Bit 11	11	Bit 11
12	Bit 12	12	Bit 12
13	Bit 13	13	Bit 13
14	Bit 14	14	Bit 14
15	Bit 15	15	Bit 15
16	Bit 16 (LSB)	16	Bit 16 (LSB)
17	±10V RANGE SELECT	17	AUDIO OUT
18	TEST POINT	18	TEST POINT
19	-15VDC	19	-15VDC
20	COMMON	20	COMMON
21	I_{OUT}	21	SUMMING JUNCTION
22	TEST POINT	22	TEST POINT
23	+15VDC	23	+15VDC
24	±5V RANGE SELECT	24	±5V RANGE SELECT

THEORY OF OPERATION

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Offset or Bipolar zero errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the minus full scale point (all bits Off), and Offset drift shifts the line left or right over the operating temperature range. Most of the offset and gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the bipolar zero voltage is virtually unaffected by variations in the reference voltage. Total Harmonic Distortion (THD) is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications. The resolution of a D/A converter can be expressed in terms of Dynamic Range. The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution, or 96dB for a 16-bit converter. The actual or useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

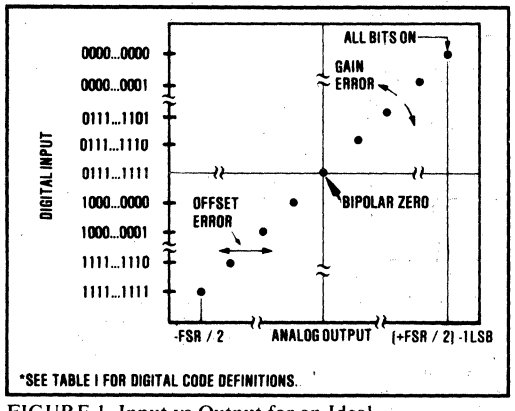


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DIGITAL INPUT CODES

The PCM51 accepts complementary digital input codes in binary format. It may be connected by the user for

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES			
		COB	CTC*
	MSB LSB	Complementary Offset Binary	Complementary Two's Complement
All bits ON	0000...000	+Full Scale	-1LSB
Mid Scale	0111...111	Zero	-Full Scale
All bits OFF	1111...111	-Full Scale	Zero
	1000...000	-1LSB	+Full Scale

*A TTL inverter must be connected between the MSB input signal and bit 1 (pin 1) to obtain CTC input code.

either complementary offset binary (COB) or complementary two's complement (CTC) codes. See Table I.

DISCUSSION OF SPECIFICATIONS

The PCM51 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are total harmonic distortion, differential linearity error, bipolar zero error, parameter shifts with time and temperature, and settling-time effects on accuracy. This DAC is factory-trimmed and tested for all critical key specifications.

BIPOLAR ZERO ERROR

Initial bipolar zero error (Bit 1 "ON" and all other bits "OFF") is factory-trimmed to typically ±10mV (±100mV maximum) at +25°C. This error may be trimmed to zero by connecting the external trim potentiometer shown in Figure 6.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at bipolar zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM51 is factory-trimmed to typically ±0.0025% of FSR (±0.006% of FSR, maximum).

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the offset and gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM51 is designed so that these drifts are in opposite directions so that the bipolar zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon the matching and tracking of V_{BE} and h_{FE} of the current-source transistors. The PCM51 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very-low to further enhance their stability.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM51 power supply sensitivity is specified for ±0.02% of FSR/% V_S, for -15VDC supplies and ±0.002% of FSR/% V_S, for +15VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME (PCM51JG-V)

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 2).

Settling times are specified to ±0.006% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

SETTLING TIME (PCM51JG-I)

Two settling times are specified to a ±0.006% of FSR. Each is given for current model connected with two different resistive loads: 10Ω to 200Ω and 1000Ω. Current-output model settling time is particularly important if the PCM51JG-I is going to be used to build a successive-approximation A/D converter. See Figure 11.

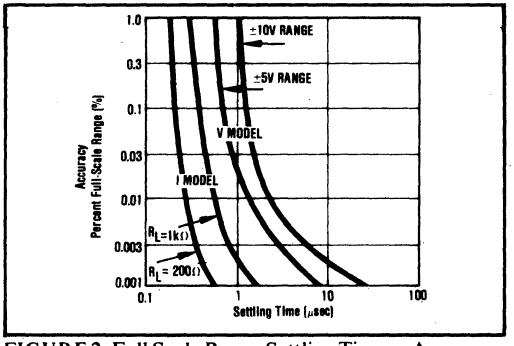


FIGURE 2. Full Scale Range Settling Time vs Accuracy.

TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics to the value of the rms fundamental and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM51 is shown in Figure 3. A timing diagram for the control logic is shown in Figure 4. The digital input code stored in the PROM as well as the output obtained from an ideal PCM51, the value of an ideal sine wave, and the inherent quantization error are given in Tables III and IV. If we assume that the error due to the test circuit is negligible, then the rms value of the PCM51 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{1/N \sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2} \qquad (1)$$

where N is the number of samples, $E_L(i)$ is the linearity error of the PCM51 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \epsilon_{rms}/E_{rms} = \frac{\sqrt{1/N \sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \qquad (2)$$

This expression indicates that, in general, there is a correlation between the THD and the square root of the

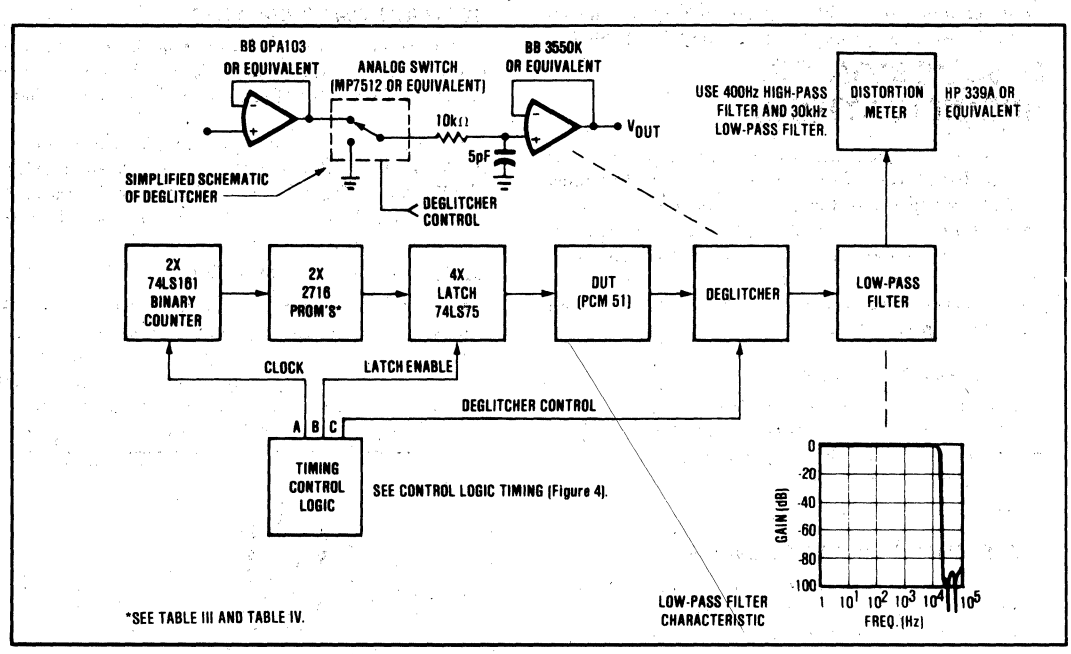


FIGURE 3. Block Diagram of Distortion Test Circuit.

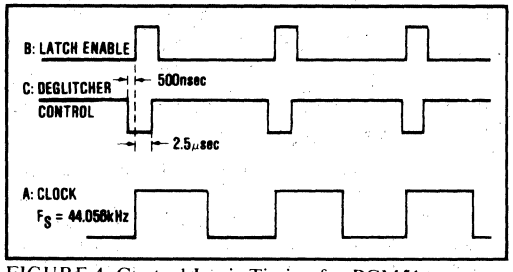


FIGURE 4. Control Logic Timing for PCM51 Distortion Test Circuit.

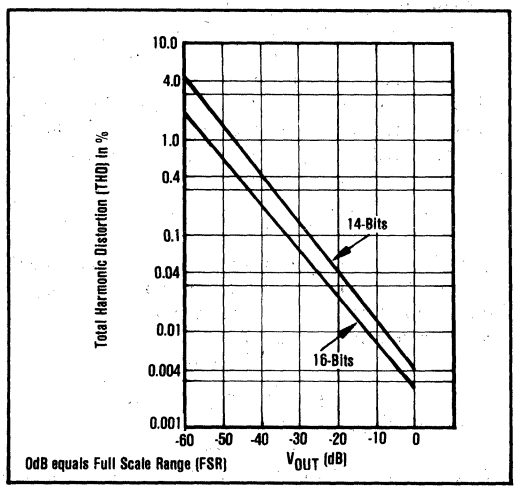


FIGURE 5. Total Harmonic Distortion (THD) vs V_{OUT}.

sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D A is directly correlated to the THD.

For the PCM51 the test period was chosen to be 22.7μsec (44.056kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 400Hz and the amplitude of the input signal is -15dB down from full scale.

Figure 5 shows the typical THD as a function of output voltage.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the PCM51.

EXTERNAL BIPOLAR ZERO ADJUST (OPTIONAL)

In some applications the bipolar zero error may require adjustment. This error may be adjusted to zero by installing an external potentiometer as shown in Figure 6.

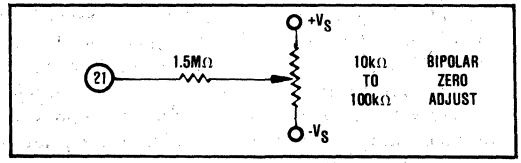


FIGURE 6. Optional External Bipolar Zero Adjust.

The TCR of the potentiometer should be 100ppm/°C or less. The 1.5MΩ resistor (20% carbon or better) should be located close to the PCM51 to prevent noise pickup. Refer to Figure 7 for the relationship of bipolar zero adjust on the D/A converter transfer function.

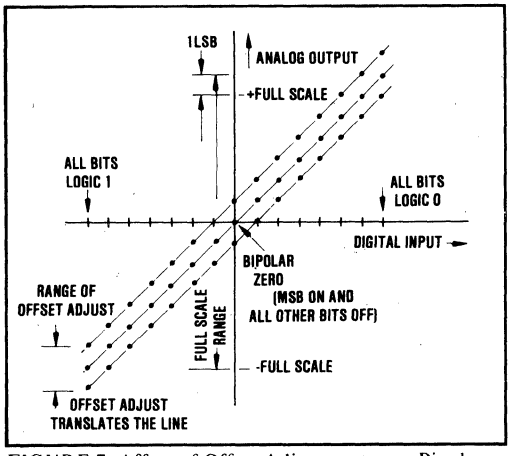


FIGURE 7. Affect of Offset Adjustment on a Bipolar D/A Converter Transfer Function.

ADJUSTMENT PROCEDURE

Apply the digital input code that should produce zero volts output (bit 1 or MSB "ON" and all other bits "OFF"). Adjust the offset potentiometer until zero volts is obtained.

Table II shows the ideal plus and minus full scale voltages and LSB values for both 14- and 16-bit resolution and ±10V, ±5V, and ±1mA output ranges.

TABLE II. Digital Input and Analog Output Relationships.

	OUTPUT CODE			
	VOLTAGE		CURRENT	
DIGITAL INPUT CODE	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Bipolar Offset Binary COB				
±10V or ±1mA				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits On (00..00)	+9.99969V	+9.99878V	-0.99997mA	-0.99988mA
All Bits Off (11..11)	-10.0000V	-10.0000V	+1.0000mA	+1.0000mA
±5V or ±1mA				
One LSB	+152μV	+610μV	0.031μA	0.122μA
All Bits On (00..00)	+4.999848V	+4.99939V	-0.99997mA	-0.99988mA
All Bits Off (11..11)	-5.0000V	-5.0000V	+1.0000mA	+1.0000mA

*Connect pin 24 to pin 17 to obtain ±5V Range.

INSTALLATION CONSIDERATIONS

If 16-bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5VDC through a 1kΩ resistor.

Figure 8 shows the connection diagram for a PCM51. Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance (R_L) is constant, R_1 simply introduces a gain error. R_2 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_1 should be less than 0.08Ω. R_L should be located as close as possible to the PCM51 for optimum performance.

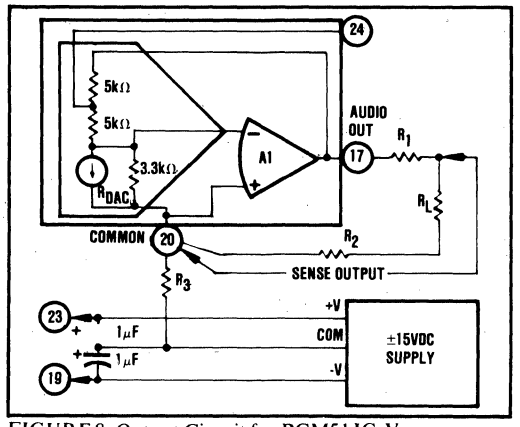


FIGURE 8. Output Circuit for PCM51JG-V.

The PCM51 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

See Figure 9 for the connection diagram of a PCM51JG-I current-to-voltage converter. R_1 through R_4 represent lead and contact resistances.

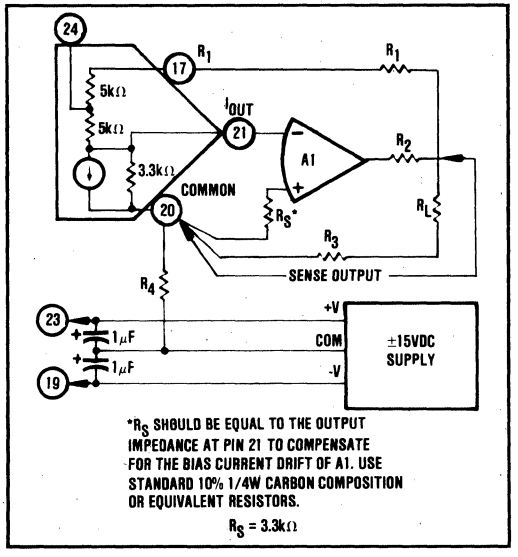


FIGURE 9. Preferred External Op Amp Configuration for PCM51JG-I

APPLICATIONS

A single PCM51 can be used for both the left and right channel as shown in Figure 10. Note that a Sample/Hold is not required.

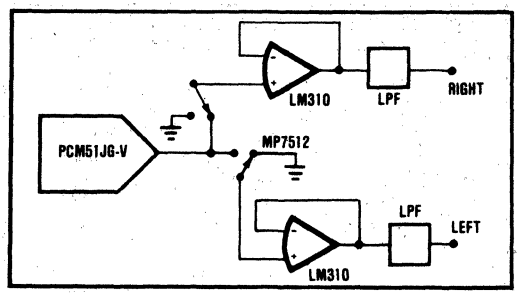


FIGURE 10. PCM51 Used for Stereo.

An A/D converter can be constructed using the PCM51JG-I shown in Figure 11.

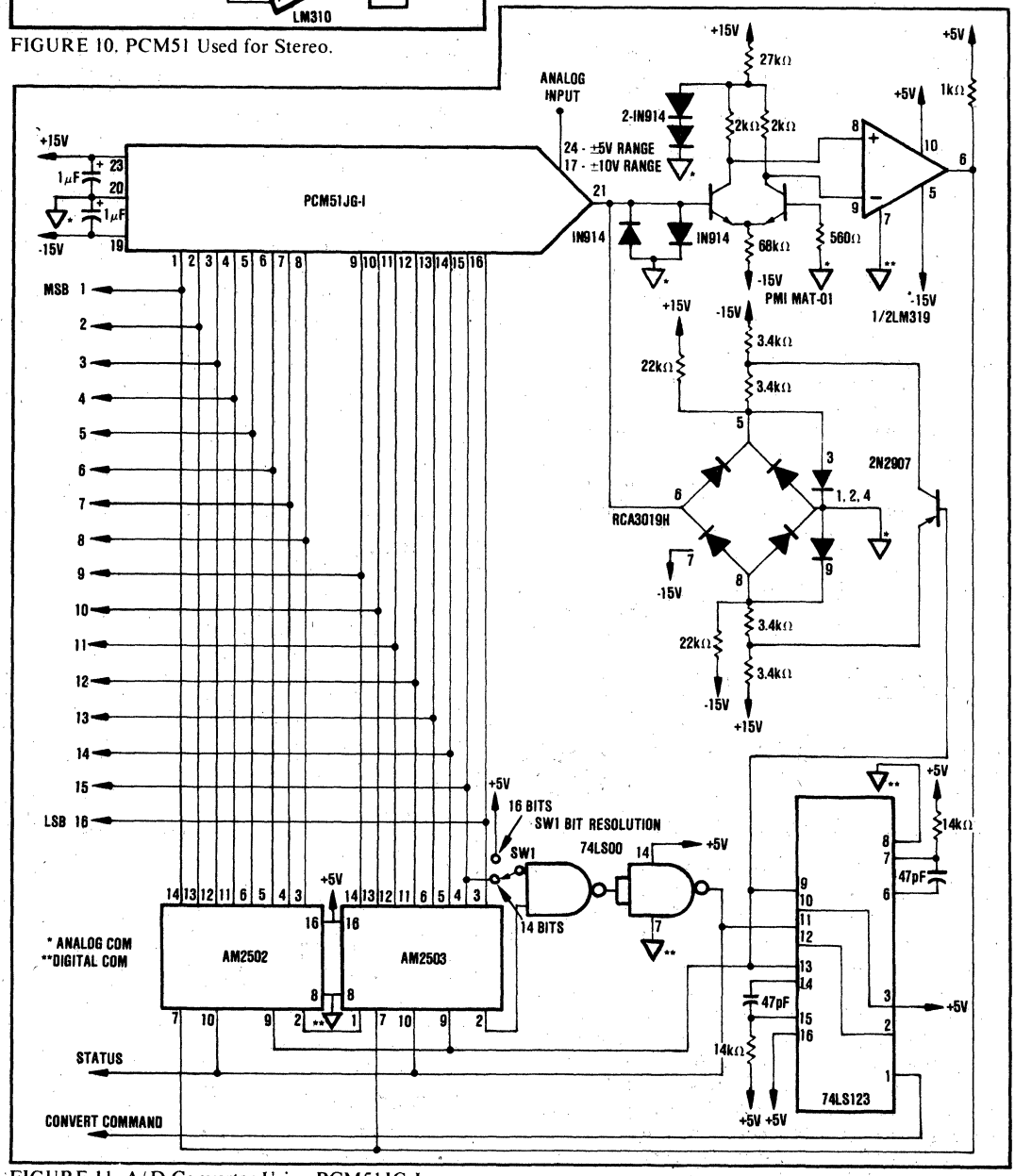


FIGURE 11. A/D Converter Using PCM51JG-I.

Table III shows the hex code loaded into the PROM's of the Distortion Test Circuit, Figure 3, for 14-bit values and Table IV shows the hex code for 16-bit values. Values are for a 400Hz sine wave (-15dB of full scale); all values are in volts.

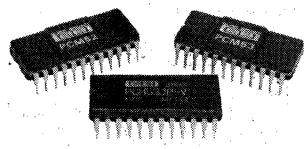
TABLE III. Hex Code for 14-Bit Values (-15dB Output in 20V Full Scale Range).

CODE#	HEX CODE	IDEAL DAC OUT Volts	IDEAL SINE VALUE Volts	QUANTIZING ERROR Volts
1	7FFF	0.000000	0.000000	0.000000
2	7EB3	.101318	.101520	.000201
3	7D67	.202637	.202709	.000072
4	7C1F	.302734	.303236	.000502
5	7AD7	.402832	.402775	-.000057
6	7997	.500488	.500999	.000511
7	7857	.598145	.597590	-.000555
8	7723	.692139	.692231	.000092
9	75F3	.784912	.784614	-.000298
10	74CF	.874023	.874439	.000415
11	73AF	.961914	.961410	-.000504
12	729F	1.044922	1.045246	.000325
13	7197	1.125488	1.125673	.000185
14	709B	1.202393	1.202428	.000035
15	6FAB	1.275635	1.275261	-.000374
16	6ECB	1.343994	1.343934	-.000060
17	6DF7	1.408691	1.408223	-.000468
18	6D33	1.468506	1.467920	-.000586
19	6C7F	1.522828	1.522828	-.000610
20	6BDF	1.572266	1.572769	.000503
21	6B4B	1.617432	1.617580	.000148
22	6AC7	1.657715	1.657115	-.000600
23	6A5B	1.690674	1.691244	.000570
24	69FB	1.719971	1.719857	-.000113
25	69AF	1.743164	1.742861	-.000303
26	6977	1.760254	1.760179	-.000075
27	6953	1.771240	1.771756	.000516
28	693F	1.777344	1.777554	.000210
29	693F	1.777344	1.777554	.000210
30	6953	1.771240	1.771756	.000516
31	6977	1.760254	1.760179	-.000075
32	69AF	1.743164	1.742861	-.000303
33	69FB	1.719971	1.719857	-.000113
34	6A5B	1.690674	1.691244	.000570
35	6AC7	1.657715	1.657115	-.000600
36	6B4B	1.617432	1.617580	.000148
37	6BDF	1.572266	1.572769	.000503
38	6C7F	1.523438	1.522828	-.000610
39	6D33	1.468506	1.467920	-.000586
40	6DF7	1.408691	1.408223	-.000468
41	6ECB	1.343994	1.343934	-.000060
42	6FAB	1.275635	1.275261	-.000374
43	709B	1.202393	1.202428	.000035
44	7197	1.125488	1.125673	.000185
45	729F	1.044922	1.045246	.000325
46	73AF	.961914	.961410	-.000504
47	74CF	.874023	.874439	.000415
48	75F3	.784912	.784614	-.000298
49	7723	.692139	.692231	.000092
50	7857	.598145	.597590	-.000555
51	7997	.500488	.500999	.000511
52	7AD7	.402832	.402775	-.000057
53	7C1F	.302734	.303236	.000502
54	7D67	.202637	.202709	.000072
55	7EB3	.101318	.101520	.000201
56	7FFF	0.000000	0.000000	0.000000
57	814B	-.101318	-.101520	-.000201
58	8297	-.202637	-.202709	-.000072
59	83DF	-.302734	-.303236	-.000502
60	8527	-.402832	-.402775	-.000057
61	8667	-.500488	-.500999	-.000511
62	87A7	-.598145	-.597590	-.000555
63	88DB	-.692139	-.692231	-.000092
64	8A0B	-.784912	-.784614	-.000298
65	8B2F	-.874023	-.874439	-.000415
66	8C4F	-.961914	-.961410	-.000504
67	8D5F	-1.044922	-1.045246	-.000325
68	8E67	-1.125488	-1.125673	-.000185
69	8F63	-1.202393	-1.202428	-.000035
70	9053	-1.275635	-1.275261	.000374
71	9133	-1.343994	-1.343934	.000060
72	9207	-1.408691	-1.408223	.000468
73	92CB	-1.468506	-1.467920	.000586
74	937F	-1.523438	-1.522828	.000610
75	941F	-1.572266	-1.572769	-.000503
76	94B3	-1.617432	-1.617580	-.000148
77	9537	-1.657715	-1.657115	.000600
78	95A3	-1.690674	-1.691244	-.000570
79	9603	-1.719971	-1.719857	.000113
80	964F	-1.743164	-1.742861	.000303
81	9687	-1.760254	-1.760179	.000075
82	96AB	-1.771240	-1.771756	-.000516
83	96BF	-1.777344	-1.777554	-.000210
84	96BF	-1.777344	-1.777554	-.000210
85	96AB	-1.771240	-1.771756	-.000516
86	9687	-1.760254	-1.760179	.000075
87	964F	-1.743164	-1.742861	.000303
88	9603	-1.719971	-1.719857	.000113
89	95A3	-1.690674	-1.691244	-.000570
90	9537	-1.657715	-1.657115	.000600
91	94B3	-1.617432	-1.617580	-.000148
92	941F	-1.572266	-1.572769	-.000503
93	937F	-1.523438	-1.522828	.000610
94	92CB	-1.468506	-1.467920	.000586
95	9207	-1.408691	-1.408223	.000468
96	9133	-1.343994	-1.343934	.000060
97	9053	-1.275635	-1.275261	.000374
98	8F63	-1.202393	-1.202428	-.000035
99	8E67	-1.125488	-1.125673	-.000185
100	8D5F	-1.044922	-1.045246	-.000325
101	8C4F	-.961914	-.961410	-.000504
102	8B2F	-.874023	-.874439	-.000415
103	8A0B	-.784912	-.784614	-.000298
104	88DB	-.692139	-.692231	-.000092
105	87A7	-.598145	-.597590	.000555
106	8667	-.500488	-.500999	-.000511
107	8527	-.402832	-.402775	-.000057
108	83DF	-.302734	-.303236	-.000502
109	8297	-.202637	-.202709	-.000072
110	814B	-.101318	-.101520	-.000201

TABLE IV. Hex Code for 16-Bit Values (-15dB Output in 20V Full Scale Range).

CODE#	HEX CODE	IDEAL DAC OUT Volts	IDEAL SINE VALUE Volts	QUANTIZING ERROR Volts
1	7FFF	0.000000	0.000000	0.000000
2	7EB2	.101624	.101520	-.000104
3	7D67	.202637	.202709	.000072
4	7C1D	.303345	.303236	-.000109
5	7AD7	.402832	.402775	-.000057
6	7995	.501099	.500999	-.000099
7	7859	.597534	.597590	.000056
8	7723	.692139	.692231	.000092
9	75F4	.784607	.784614	.000007
10	74CE	.874329	.874439	.000110
11	73B1	.961304	.961410	.000107
12	729E	1.045227	1.045246	.000019
13	7196	1.125793	1.125673	-.000120
14	709B	1.202393	1.202428	.000035
15	6FAC	1.275330	1.275261	-.000069
16	6ECB	1.343994	1.343934	-.000060
17	6DF9	1.408081	1.408223	.000142
18	6D35	1.467896	1.467920	.000024
19	6C81	1.522827	1.522828	.000001
20	6BDD	1.572876	1.572769	-.000107
21	6B4B	1.617432	1.617580	.000148
22	6AC9	1.657104	1.657115	.000010
23	6A59	1.691284	1.691244	-.000040
24	69FB	1.719971	1.719857	-.000113
25	69B0	1.742859	1.742861	.000002
26	6977	1.760254	1.760179	-.000075
27	6951	1.771851	1.771756	-.000094
28	693E	1.777649	1.777554	-.000095
29	693E	1.777649	1.777554	-.000095
30	6951	1.771851	1.771756	-.000094
31	6977	1.760254	1.760179	-.000075
32	69B0	1.742859	1.742861	.000002
33	69FB	1.719971	1.719857	-.000113
34	6A59	1.691284	1.691244	-.000040
35	6AC9	1.657104	1.657115	.000010
36	6B4B	1.617432	1.617580	.000148
37	6BDD	1.572876	1.572769	-.000107
38	6C81	1.522827	1.522828	.000001
39	6D35	1.467896	1.467920	.000024
40	6DF9	1.408081	1.408223	.000142
41	6ECB	1.343994	1.343934	-.000060
42	6FAC	1.275330	1.275261	-.000069
43	709B	1.202393	1.202428	.000035
44	7196	1.125793	1.125673	-.000120
45	729E	1.045227	1.045246	.000019
46	7381	.961304	.961410	.000107
47	74CE	.874329	.874439	.000110
48	75F4	.784607	.784614	.000007
49	7723	.692139	.692231	.000092
50	7859	.597534	.597590	.000056
51	7995	.501099	.500999	-.000099
52	7AD7	.402832	.402775	-.000057
53	7C1D	.303345	.303236	-.000109
54	7D67	.202637	.202709	.000072
55	7EB2	.101624	.101520	-.000104
56	7FFF	0.000000	0.000000	0.000000
57	814C	-.101624	-.101520	.000104
58	8297	-.202637	-.202709	-.000072
59	83E1	-.303345	-.303236	.000109
60	8527	-.402832	-.402775	.000057
61	8669	-.501099	-.500999	.000099
62	87A5	-.597534	-.597590	-.000056
63	88DB	-.692139	-.692231	-.000092
64	8A0A	-.784607	-.784614	-.000007
65	8B30	-.874329	-.874439	-.000110
66	8C4D	-.961304	-.961410	-.000107
67	8D60	-1.045227	-1.045246	-.000019
68	8E68	-1.125793	-1.125673	.000120
69	8F63	-1.202393	-1.202428	-.000035
70	9052	-1.275330	-1.275261	.000069
71	9133	-1.343994	-1.343934	.000060
72	9205	-1.408081	-1.408223	-.000142
73	92C9	-1.467896	-1.467920	-.000024
74	937D	-1.522827	-1.522828	-.000001
75	9421	-1.572876	-1.572769	.000107
76	94B3	-1.617432	-1.617580	-.000148
77	9535	-1.657104	-1.657115	-.000010
78	95A5	-1.691284	-1.691244	.000040
79	9603	-1.719971	-1.719857	.000113
80	964E	-1.742859	-1.742861	-.000002
81	9687	-1.760254	-1.760179	.000075
82	96AD	-1.771851	-1.771756	.000094
83	96C0	-1.777649	-1.777554	.000095
84	96C0	-1.777649	-1.777554	.000095
85	96AD	-1.771851	-1.771756	.000094
86	9687	-1.760254	-1.760179	.000075
87	964E	-1.742859	-1.742861	-.000002
88	9603	-1.719971	-1.719857	.000113
89	95A5	-1.691284	-1.691244	.000040
90	9535	-1.657104	-1.657115	-.000010
91	94B3	-1.617432	-1.617580	-.000148
92	9421	-1.572876	-1.572769	.000107
93	937D	-1.522827	-1.522828	-.000001
94	92C9	-1.467896	-1.467920	-.000024
95	9205	-1.408081	-1.408223	.000142
96	9133	-1.343994	-1.343934	.000060
97	9052	-1.275330	-1.275261	.000069
98	8F63	-1.202393	-1.202428	-.000035
99	8E68	-1.125793	-1.125673	.000120
100	8D60	-1.045227	-1.045246	-.000019
101	8C4D	-.961304	-.961410	-.000107
102	8B30	-.874329	-.874439	-.000110
103	8A0A	-.784607	-.784614	-.000007
104	88DB	-.692139	-.692231	-.000092
105	87A5	-.597534	-.597590	-.000056
106	8669	-.501099	-.500999	.000099
107	8527	-.402832	-.402775	.000057
108	83E1	-.303345	-.303236	.000109
109	8297	-.202637	-.202709	-.000072
110	814C	-.101624	-.101520	.000104

BURR-BROWN®



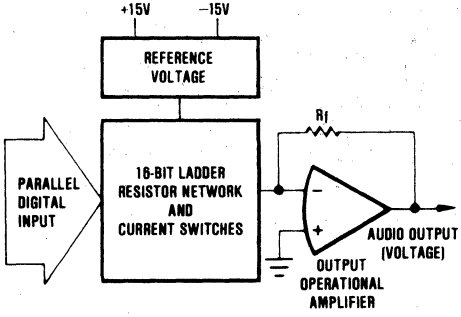
PCM52JG-V
PCM53JG-V
PCM53JP-V
PCM53JG-I

DESIGNED FOR AUDIO

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 16-BIT MONOTONICITY, typ
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.002% THD (FS Input, 16 Bits), typ
- 0.02% THD (-20dB, 16 Bits), typ
- 3μsec SETTLING TIME, typ
- 96dB DYNAMIC RANGE
- ±10V (PCM53) AND ±5V (PCM52) AUDIO OUTPUT AVAILABLE
- EIAJ STC-007 COMPATIBLE
- INDUSTRY-STANDARD PIN OUT
- COMPACT, 24-PIN, DIL PACKAGE



DESCRIPTION

The PCM52 and PCM53 are state-of-the-art, fully monolithic, digital-to-analog converters that are designed and specified for digital audio applications. These devices employ a segmented architecture and ultra-stable, nichrome (NiCr), thin-film, well-matched resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature range.

The PCM52-V and PCM53-V are completely self-contained with stable, low noise, internal, zener voltage reference; high speed current switches; resistor ladder network; and fast-settling, low noise, output operational amplifier all on a single monolithic chip. A special, open-loop reference circuit helps provide the fast-settling time required for critical audio applications. The converters can be operated using two power supplies (±15V) instead of three separate supplies. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps to assure the user of high system reliability and outstanding overall system performance.

The PCM53JG-I is similar to the PCM53JG-V except it provides a current output that settles to within ±0.006% of FSR of its final value in typically 350nsec in response to a full-scale change in the digital input code.

The letters JG and JP after the number (PCM53JG or PCM53JP) refer to the package type: the JG refers to a ceramic DIP package and JP refers to a plastic molded package. The letters -V and -I (PCM53JG-V and PCM53JG-I) refer to the voltage-output and current-output models respectively. These models are currently available: PCM52JG-V, PCM53JG-V, PCM53JP-V, PCM53JG-I. Other family members may become available later.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

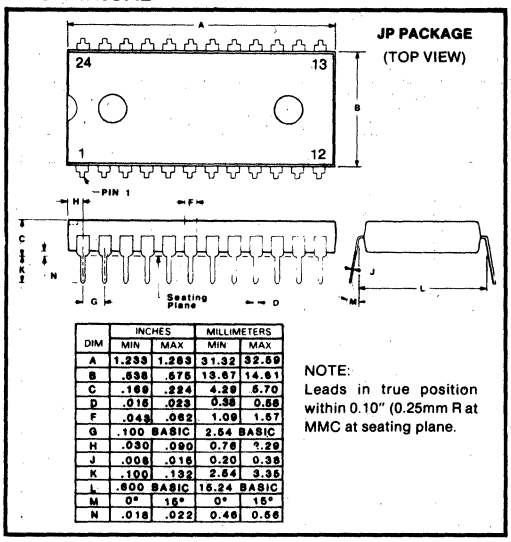
ELECTRICAL

T_A = +25°C rated power supplies unless otherwise noted.

MODEL	PCM52/PCM53			UNITS
	MIN	TYP	MAX	
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Dynamic Range		96		dB
Logic Levels (TTL/CMOS Compatible): Logic "1" at +40µA	+2.4		$+V_{CC}$	VDC
Logic "0" at −0.5mA	0		+0.8	VDC
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error		±0.1	±1.0	%
Bipolar Zero Error[1]		±10	±50	mV
Differential Linearity Error at Bipolar Zero		0.001	0.005	% of FSR[2]
Noise (rms)(20Hz to 20kHz) at Bipolar Zero: PCM52-V[3]		15	30	µV
PCM53-V[3]		30	60	µV
TOTAL HARMONIC DISTORTION[4] (16-Bit Resolution)				
V_O = ±FS at f = 420Hz		0.002	0.004	%
V_O = −20dB at f = 420Hz		0.02	0.04	%
V_O = −60dB at f = 420Hz		1.9	4.0	%
MONOTONICITY		16		Bits
DRIFT (0°C to +70°C)				
Total Bipolar Drift (includes gain, offset, and linearity drift)		±25	±150	ppm of FSR/°C
		±0.1	±0.68	% of FSR
		±0.01	±0.06	dB
Bipolar Zero Drift		±4	±20	ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)				
Voltage Models (PCM52-V, PCM53-V) Output: 10V Step		3		µsec
1LSB Step		1		µsec
Current Model (PCM53-I) Output (1mA Step): 10Ω to 100Ω Load		350		nsec
1kΩ Load[7]		350		nsec
Deglitcher Delay (THD Test)[5]		2.5	4.0	µsec
Slew Rate		10		V/µsec
WARM-UP TIME	1			Min
OUTPUT				
ANALOG OUTPUT				
Voltage Models				
Ranges: PCM53-V	±9.8	±10	±10.2	V
PCM52-V	±4.9	±5	±5.1	V
Output Current	±5			mA
Output Impedance		0.1		Ω
Short-Circuit Duration		Indefinite to Common		
Current Model				
Range, PCM53-I (±30%)		±1		mA
Output Impedance (±30%)		2.4		kΩ
POWER SUPPLY				
SENSITIVITY				
$+V_{CC}$		±0.001		% of FSR/%V_{CC}
$-V_{CC}$		±0.001		% of FSR/%V_{CC}
V_{DD}		±0.001		% of FSR/%V_{CC}
POWER SUPPLY REQUIREMENTS				
Voltage: ±V_{CC}[6]	±14.25	±15	±15.75	VDC
V_{DD}[6]	+4.75	+5	+15.75	VDC
(V_{DD} may be connected to +V_{CC} supply voltage. Result is slightly increased total power dissipation of approximately 40mW).				
Supply Drain (no load): +V_{CC}[6]		+18	+30	mA
−V_{CC}[6]		−18	−30	mA
V_{DD}[6]		+4	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	−25		+85	°C

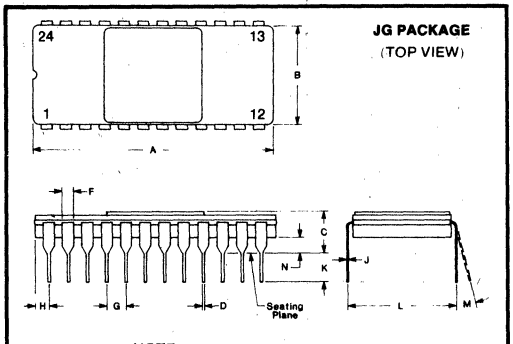
NOTES: 1. Adjustable to zero with external potentiometer. 2. FSR means Full Scale Range and is 20V for ±10V (PCM53-V) and 10V for ±5V range (PCM52-V). 3. Characterization units show at least two sigma units to meet this specification. Not 100% final tested. 4. The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. A block diagram of a measurement circuit is shown in Figure 2. Burr-Brown may calculate THD from the measured linearity errors using equation (2) in the section on "Total Harmonic Distortion," but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. 5. Deglitcher or Sample/Hold delay used in THD measurement test circuit. See Figures 2 and 3. 6. See Connection Diagram and Pin Assignments. 7. Measured with an active clamp to provide a low impedance for approximately 200nsec.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.233	1.263	31.32	32.59
B	.538	.575	13.67	14.61
C	.169	.224	4.29	5.70
D	.016	.023	0.38	0.58
F	.045	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.016	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

NOTE:
Leads in true position within 0.10" (0.25mm R at MMC at seating plane.



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

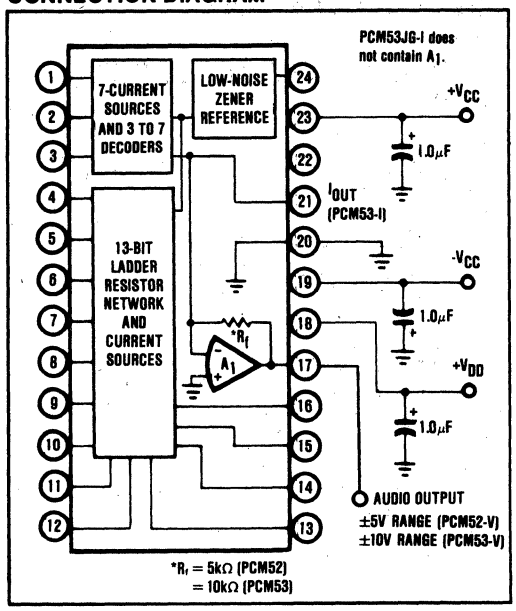
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.237	1.263	31.42	32.08
B	.514	.526	13.06	13.36
C	.178	.230	4.52	5.84
D	.016	.020	0.41	0.51
F	.050	.070	1.27	1.78
G	.100 BASIC		2.54 BASIC	
H	.065	.085	1.65	2.16
J	.008	.012	0.20	0.30
K	.100	.200	2.54	5.08
L	.600 BASIC		15.24 BASIC	
M	—	15°	—	15°
N	.035	.055	0.89	1.40

Actual package, such as cover appearance, may vary slightly from unit to unit. Pin spacing will not change.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±18VDC
Input Logic Voltage	-1V to +Supply Voltage
Storage Temperature	-55°C to +100°C
Lead Temperature During Soldering	10sec at +300°C

CONNECTION DIAGRAM



PIN ASSIGNMENTS

PIN NO.	PCM52/53-V	PIN NO.	PCM53-I
1	Bit 1 (MSB)	1	Bit 1 (MSB)
2	Bit 2	2	Bit 2
3	Bit 3	3	Bit 3
4	Bit 4	4	Bit 4
5	Bit 5	5	Bit 5
6	Bit 6	6	Bit 6
7	Bit 7	7	Bit 7
8	Bit 8	8	Bit 8
9	Bit 9	9	Bit 9
10	Bit 10	10	Bit 10
11	Bit 11	11	Bit 11
12	Bit 12	12	Bit 12
13	Bit 13	13	Bit 13
14	Bit 14	14	Bit 14
15	Bit 15	15	Bit 15
16	Bit 16 (LSB)	16	Bit 16 (LSB)
17	±5V AUDIO OUT (PCM52-V) ±10V AUDIO OUT (PCM53-V)	17	R_f (10kΩ ±30%)
18	V_{DD}	18	V_{DD}
19	$-V_{CC}$	19	$-V_{CC}$
20	COMMON	20	COMMON
21	SUMMING JUNCTION	21	I_{OUT}, ±1mA ±30% (AUDIO OUTPUT)
22	TEST POINT	22	TEST POINT
23	$+V_{CC}$	23	$+V_{CC}$
24	REFERENCE OUT (+6.3V)	24	REFERENCE OUT (+6.3V)

THEORY OF OPERATION AND AUDIO SPECIFICATIONS

The transfer function of an ideal binary D/A converter is a set of discrete output levels that lie on a straight line as shown in Figure 1. The number of possible discrete output levels, or resolution, is equal to 2^n where n is the number of digital inputs or "bits". The PCM52/53 has 2^{16} or 65,536 possible output levels. Another method of expressing resolution that is useful in audio applications is Dynamic Range.

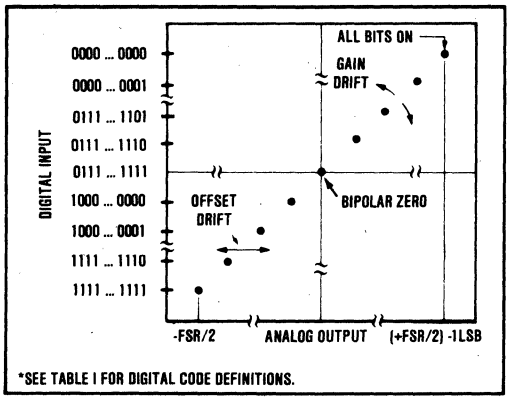


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 × n, or about 96dB for a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion (THD).

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error in unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM52/53 is shown in Figure 2. A timing diagram for the control logic is shown in Figure 3.

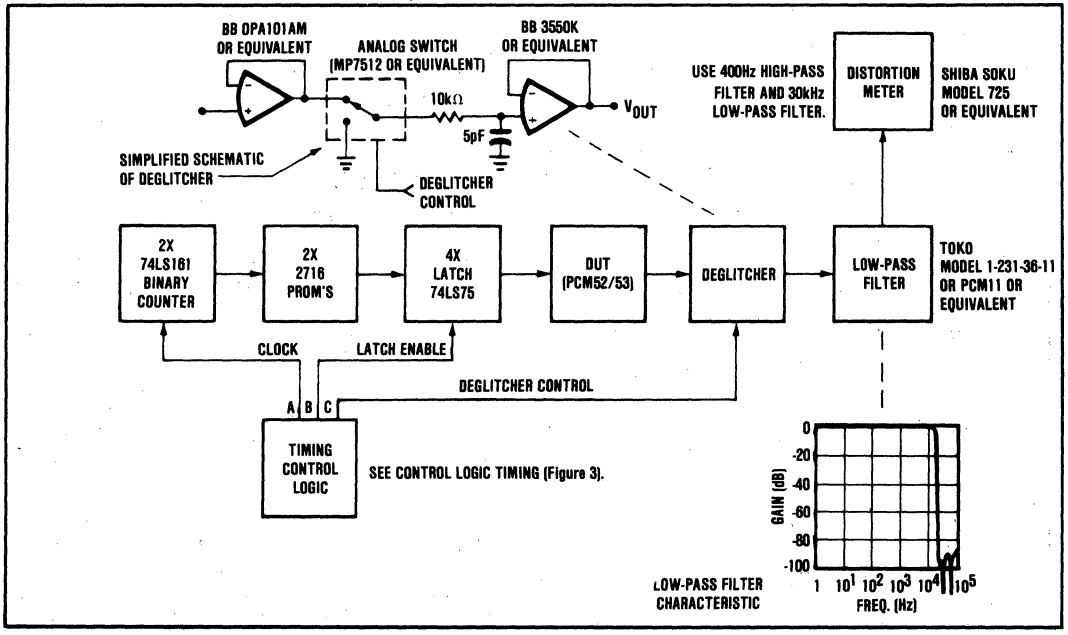


FIGURE 2. Block Diagram of Distortion Test Circuit.

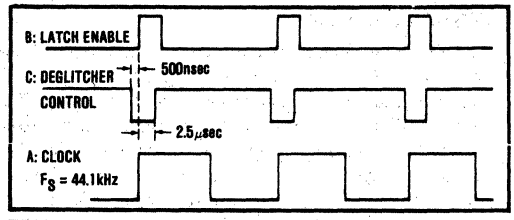


FIGURE 3. Control Logic Timing for PCM52/53 Distortion Test Circuit.

If we assume that the error due to the test circuit is negligible, then the rms value of the PCM52/53 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM52/53 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \qquad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM52/53 the test period was chosen to be 22.7μsec (44.1kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 420Hz and the amplitude of the input signal is 0dB, -20dB, and -60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

Figure 5 shows typical THD as a function of frequency.

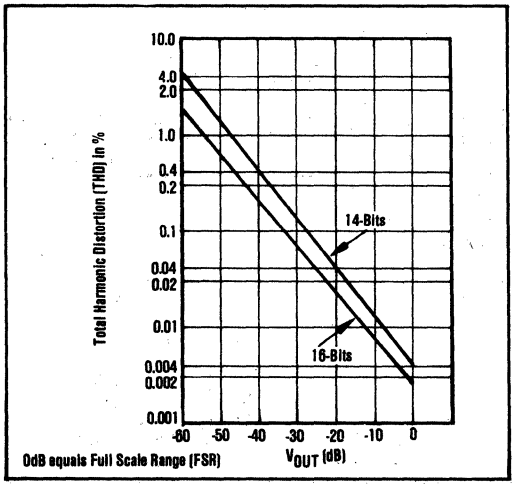


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

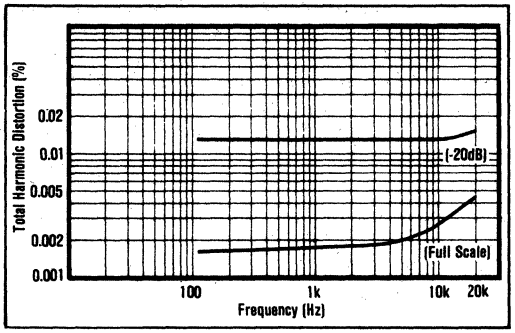


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

DIGITAL INPUT CODES

The PCM52/53 accepts complementary digital input codes in binary format. It may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes. See Table I.

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES			
	MSB LSB	COB	CTC*
	↓ ↓	Complementary Offset Binary	Complementary Two's Complement
All bits ON	0000...000	+Full Scale	-1LSB
Mid Scale	0111...111	Zero	-Full Scale
All bits OFF	1111...111	-Full Scale	Zero
	1000...000	-1LSB	+Full Scale

*A TTL inverter must be connected between the MSB input signal and bit 1 (pin 1) to obtain CTC input code.

DETAILED THEORY OF OPERATION

In the basic design, the three functions represented by the complete D/A converter—the voltage reference, the output amplifier, and the converter—are distributed among six major circuit blocks (Figure 6). Three blocks—the open loop reference, the current-offset circuit, and the reference output amplifier—perform the reference functions. The D/A conversion is performed by two circuits called the upper converter and the lower converter, which are combined into the voltage output by the on-chip output op amp.

The prime requirements for a D/A converter circuit designed for PCM audio applications are that it have low differential linearity error and monotonicity and that it stay that way over a useful temperature range. To obtain this performance at 14 to 16 bits, the converter combines segmentation with multiple R-2R networks.

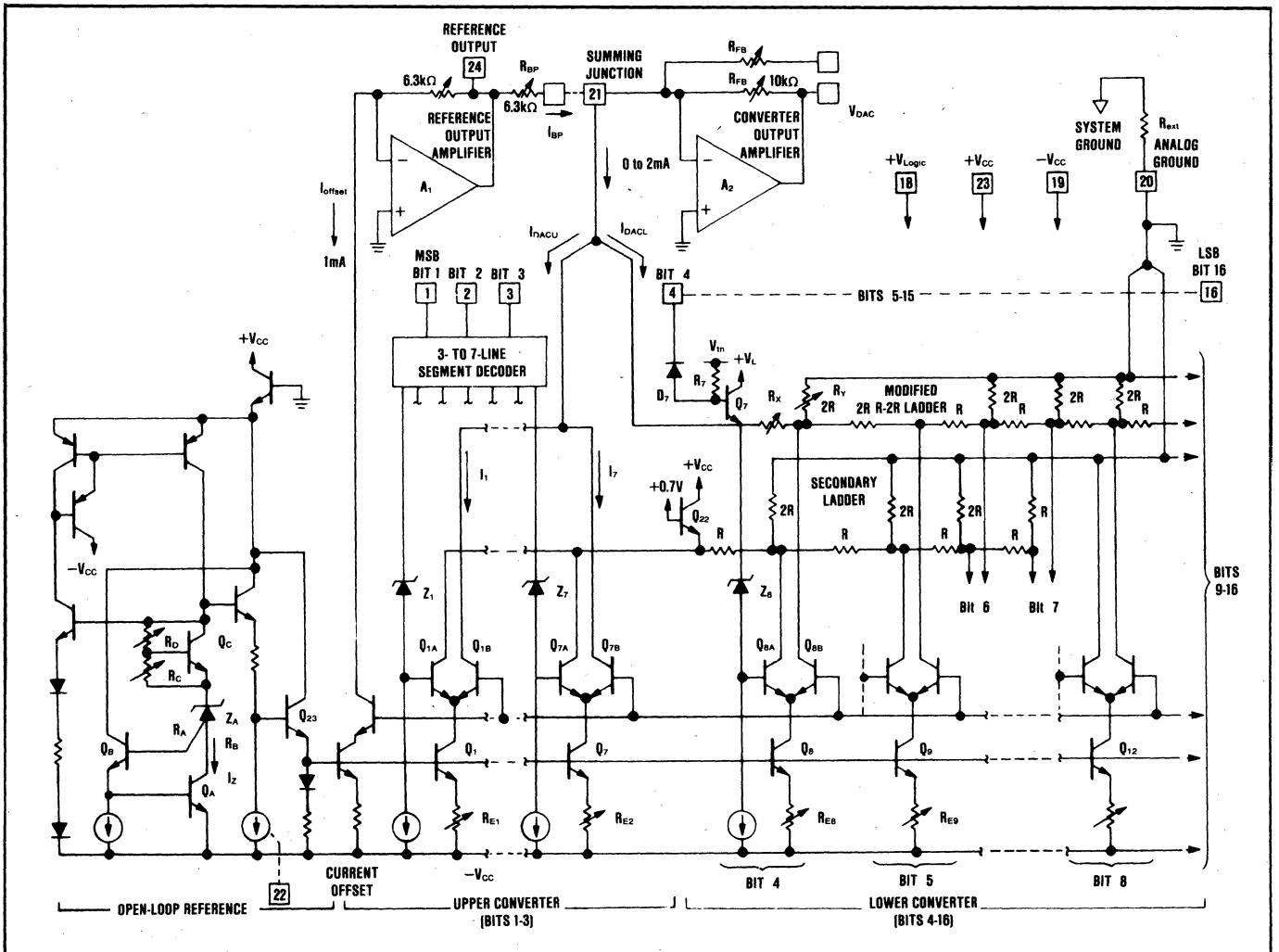


FIGURE 6. Simplified Circuit Diagram of the PCM52/53 16-bit Digital-to-Analog Converter.

The upper converter, which generates the three most significant bits, is made up of seven equal current sources (Q_1 R_{E1} through Q_1 R_{E7}), each providing 0.25mA. Together the sources form the upper converter current, I_{DACU}.

The three binary-coded MSBs (bits 1, 2, and 3) are decoded by a three-to-seven-line circuit, which sequentially selects the equal current sources as the binary code formed by the bits changes through the eight values (000 to 111). Thus, as the code ranges through its values, I_{DACU} changes from 0 to 1.75mA. This scheme ensures monotonicity, reduces initial matching and tracking requirements, and cuts the tracking errors that occur with temperature and time.

Averaging Transistor and Resistor Shifts

To further improve the tolerance of the upper converter to time and temperature change, the seven equal currents are turned on in the following order: Q_4, Q_2, Q_7, Q_5, Q_1, Q_6, Q_3. This sequence, which produces the zero-to-full-scale output, averages the shifts that occur in transistor parameters and in the value of the emitter resistors.

The 13 least significant bits are produced by the lower converter, which uses nine more equal-current sources for the nine middle bits and emitter area rationing for the 4LSBs. However, rather than being summed directly by the current of the upper converter (which would have required $2^{16}-1$ equal current sources) the current sources are further divided binarily by a pair of R-2R networks, called the modified R-2R ladder and the secondary ladder. By diverting the LSB currents through the modified ladder, the lower converter produces I_{DACL}. This current consists of $2^{13}-1$ discrete, 30nA steps for each 0.25mA segment of the upper converter. I_{DACU} and I_{DACL} are added at the summing junction, SJ, to form the I_{DAC}, which has a range that varies between 0 and 1.99997mA.

The modified R-2R ladder is superior to a conventional R-2R ladder because its output can be increased or decreased by laser-trimming of its output resistors (R_X and R_Y). Such trimming does not change the binary current division in the ladder. The gain of the lower converter can then be trimmed relative to the gain of the upper converter without interacting or in any way affecting the linearity of the lower converter.

The initial values of the 16 current sources are determined by the voltage at the output of the reference (the emitter of Q_{23}), but the sources are set to the same value when the emitter resistors (R_1-R_{16}) are laser-trimmed. The sources are turned on and off by a differential switch pair (such as Q_{SA}-Q_{SB}) driven by the low-power Schottky TTL-compatible input circuit (typical of D_8, R_8, Q_8, Z_8). The input circuit provides the level translation.

Constant Power

To maintain 16-bit performance, the on-chip power dissipation—and therefore the chip temperature—must be kept constant during code changes. Therefore the current from both the ON side (Q_{1B}) and the OFF side (Q_{1A}) of each differential switch pair in the upper converter should come from $+V_{CC}$, rather than one from $+V_{CC}$ and one from ground. The ON side currents (when the bits are on) come from $+V_{CC}$ and flow through A_2 and the feedback resistor, R_{fb}, to the summing junction to form I_{DACU}. Transistor Q_{22} is used to provide the OFF side current with a similar path to $+V_{CC}$. In the lower converter, the secondary R-2R ladder, which is connected between the OFF side of the differential switches and Q_{22}, provides the same function by keeping the $+V_{CC}$ current and the analog ground current constant with code changes.

The secondary ladder also significantly reduces linearity errors that would otherwise be caused by external ground wiring. Indeed, the secondary ladder makes possible the use of a single ground pin, which is the only way to make all the connections in a 24-pin package.

Most converters use a closed-loop op amp for precision DC biasing of their current sources. However, switching transients can cause excessive settling time in the op amp. To ensure minimum settling time, the PCM52/53 uses an open-loop reference circuit, which incidentally does not require space-consuming capacitors for frequency compensation or suppression of switching transients.

The reference voltage is generated by a Kelvin-sensed buried zener diode. Kelvin sensing is used because the elements of the buried zener, R_A and R_B, have a large and nonlinear temperature coefficient. The Kelvin-sensed connection removes from the reference path the large voltage drop, $R_B I_Z$, caused by the 1mA zener current I_Z. Instead it substitutes the voltage drop produced across R_A by the base current of Q_B.

Since this base current is only 1μA, the drop is negligible, and the true zener breakdown, V_Z is sensed. In addition great care was taken to ensure that all temperature-sensitive parts of the open-loop reference were laid out along lines of thermal equilibrium, to prevent thermal settling tails.

High-Speed Output Amplifier

The converter's output amplifier, A_2, which sums all of the output currents and converts them into the output voltage, V_{DAC}, must be just as accurate as the reference and current sources and just as fast as the switching circuits.

The amplifier is very fast, and it is well behaved when driving a capacitive load. It slews at 10V/μsec and typically settles to 0.003% of final value in less than 4μsec for a 20V step. For a step of 1LSB at the major carry, it settles in 1.5μsec. The thermal tails caused by temperature gradients and resistor self-heating are less than 0.001% of full scale.

Thermal tails occur when thermal gradients across the chip change as signal levels change. For example, when driving a load the output stage of the amplifier and its feedback resistor generate more heat at the full-scale output voltage than at zero. Therefore the temperature-

sensitive differential input stage, which is close by on the chip, uses cross-coupled transistors and resistors to equalize thermal gradients.

To achieve a ±10V output swing when operating from ±15V, the output stage of the amplifier uses two transistor pairs connected in series. This scheme is necessary because the breakdown voltage of the npn transistors is limited to 20V by the semiconductor process.

In addition, the output stage is biased in a class AB condition, so that current is always flowing. Continuous current flow is essential to ensure that the open-loop gain, A_O, and closed-loop output impedance, R_O, remain constant for both positive and negative full-scale output swings at 103dB and 0.03Ω, respectively. With lesser performance, errors would occur. If, for example, A_O changed from 94dB to 100dB for an output swing of −10V to +10V respectively, the output error would change by 100μV, and the change would be nonlinear. Likewise a nonlinear error approaching 200μV would occur if R_O changed from 0.04Ω to 0.08Ω.

DISCUSSION OF SPECIFICATIONS

The PCM52/53 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature, and settling time effects on accuracy. The PCM52/53 is factory-trimmed and tested for all critical key specifications.

The accuracy ot a D/A converter is described by the transfer function shown in Figure 1. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Offset or Bipolar zero errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

BIPOLAR ZERO ERROR

Initial bipolar zero error (Bit 1 "ON" and all other bits "OFF") is the deviation from zero volts out and is factory-trimmed to typically ±10mV at +25°C. This error may be trimmed to zero by connecting the external trim potentiometer shown in Figure 8.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM52/53 is factory-trimmed to typically ±0.001% of FSR.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM52/53 is designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM52/53 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM52/53 power supply sensitivity is specified for ±0.001% of FSR/%V_{CC} for all supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 7).

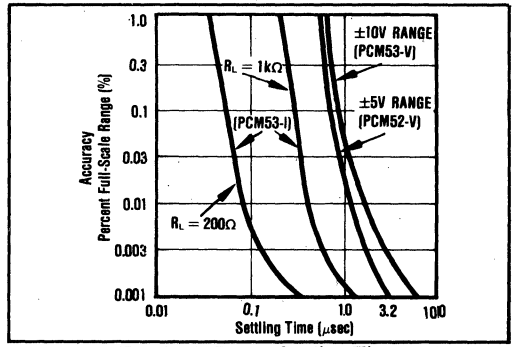


FIGURE 7. Full Scale Range Settling Time vs Accuracy.

Settling times are specified to ±0.006% of FSR; one for a large output voltage change of 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the PCM52/53.

EXTERNAL BIPOLAR ZERO ADJUST (OPTIONAL)

In some applications the Bipolar Zero Error (offset) may require adjustment. This error may be adjusted to zero by installing an external potentiometer as shown in Figure 8.

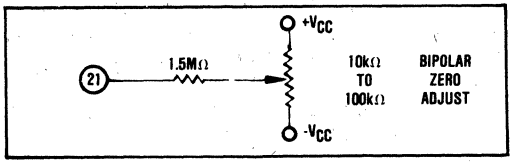


FIGURE 8. Optional External Bipolar Zero Adjust.

The potentiometer should have adequate resolution, at least 10 turns for full-scale resistance.

The TCR of the potentiometer should be 100ppm/°C or less. The 1.5MΩ resistor (20% carbon or better) should be located close to the PCM52/53 to prevent noise pickup. Refer to Figure 9 for the relationship of Bipolar Zero adjust on the D/A converter transfer function.

ADJUSTMENT PROCEDURE

Apply the digital input code that should produce zero volts output (bit 1 or MSB "ON" and all other bits "OFF"). Adjust the bipolar zero potentiometer until zero volts is obtained.

Table II shows the ideal plus and minus full scale voltages and LSB values for both 14- and 16-bit resolution and ±10V and ±5V output ranges.

INSTALLATION CONSIDERATIONS

If 14-bit resolution is desired, bit 15 (pin 15) and bit 16 (pin 16) should be connected to V_{DD} through a 1kΩ resistor to insure that these bits remain off.

Figure 10 shows the connection diagram for a PCM52/53-V. Figures 11 and 12 show connection diagrams for PCM53-I models.

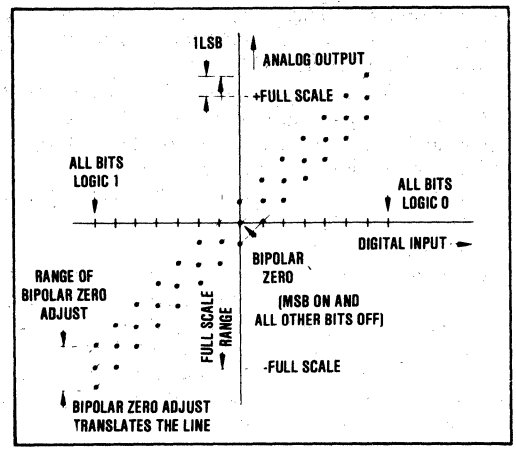


FIGURE 9. Effect of Bipolar Zero Adjustment on a Bipolar D/A Converter Transfer Function.

TABLE II. Digital Input and Analog Output Relationship.

DIGITAL INPUT CODE	OUTPUT			
	Voltage Model		Current Model	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Bipolar Offset Binary (COB)				
±10V (PCM53)				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits On				
00...00	+9.99969V	+9.99878V	−0.99997mA	−0.99988mA
All Bits Off				
11...11	−10.00000V	−10.00000V	−1.00000mA	+1.00000mA
±5V (PCM52)				
One LSB	+152μV	+610μV		
All Bits On				
00...00	+4.999848V	+4.99939V		
All Bits Off				
11...11	−5.00000V	−5.00000V		

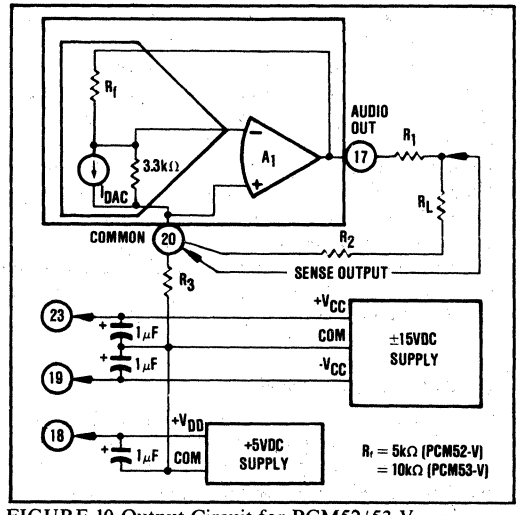


FIGURE 10. Output Circuit for PCM52/53-V.

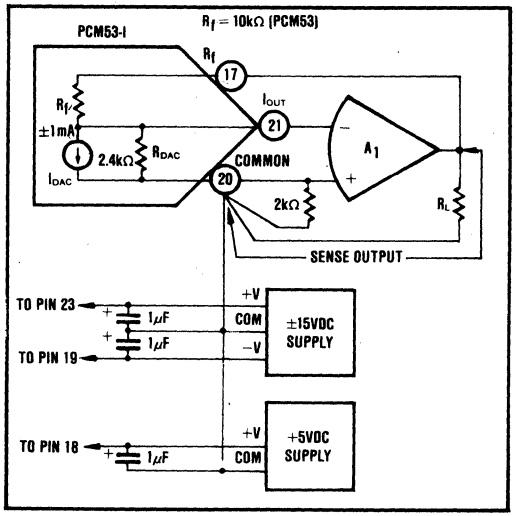


FIGURE 11. Preferred External Op Amp Configuration Using PCM53-I.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance (R_L) is constant, R_1 simply introduces a gain error. R_2 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{L\min}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. R_L should be located as close as possible to the PCM52/53 for optimum performance.

The PCM52/53 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

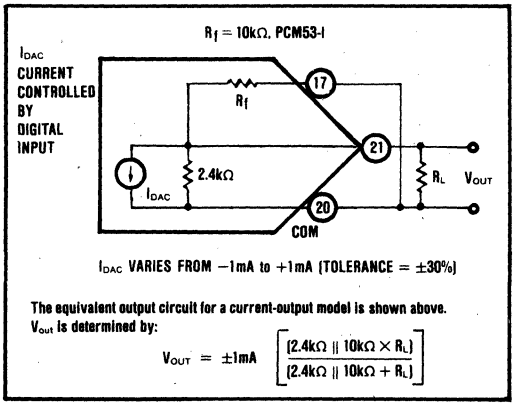


FIGURE 12. Driving a Resistive Load With PCM53-I.

The PCM52/53 is not normally sensitive to electrostatic discharge (ESD). Figures 11 and 12 show connection diagrams for PCM53-I models.

APPLICATIONS

Figures 13 and 14 show a circuit diagram and timing diagram of a single PCM52/53-V used to obtain both left and right channel audio output in a typical digital audio system. The Sony CX-7934 and associated LSI logic contain all of the required circuitry for error detection, correction, and formatting of the digital data obtained from the Compact Disc prior to sending this information to the D/A converter. The CX-7934 is used in a parallel output mode where the left and right channel parallel data are time-shared. Since the digital inputs of the PCM52/53 are TTL-compatible, they can be connected directly to the parallel outputs of the CX-7934. Only a single inverter is required (Bit 1) to convert the two's complement output code of the CX-7934 to offset binary. The audio output of the PCM52/53-V is alternately time-shared between the left and right channels. The design is greatly simplified because the PCM52/53-V is a complete D/A converter.

A sample/hold amplifier, or "deglitcher", is required at the output of the D/A converter for both the left and right channel, as shown in Figure 15. The S/H amplifier for the left channel is composed of A_2, SW_1, and associated circuitry. A_2 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET switch operates at a virtual ground when "C" and "B" are closed in the sample mode, there is no increase in distortion caused by the modulation effect of R_{on} by the audio signal.

Figure 16 shows the deglitcher control signals for both the left and right channels which are produced by the timing control logic. A delay of 2.5μsec ($t\omega$) is provided to eliminate the glitch and allow the output of the PCM52/53-V to settle within a small error band around its final value before connecting it to the channel output.

Due to the fast settling time of the PCM52/53-V, it is possible to minimize the delay between the left channel and right channel outputs when using a single D/A converter for both channels. This is important because the left and right channel data is recorded in phase and use of a slower D/A converter would result in significant phase error at the higher audio frequencies.

A low-pass filter is required at the S/H output to remove all unwanted frequency components caused by the sampling frequency as well as the discrete nature of the D/A converter output. The filter must have a flat amplitude response over the entire audio band (0 to 20kHz) and a very-high attenuation above 20kHz. Most previous digital audio circuits used a high-order (9-13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristics of the transients contained in music.

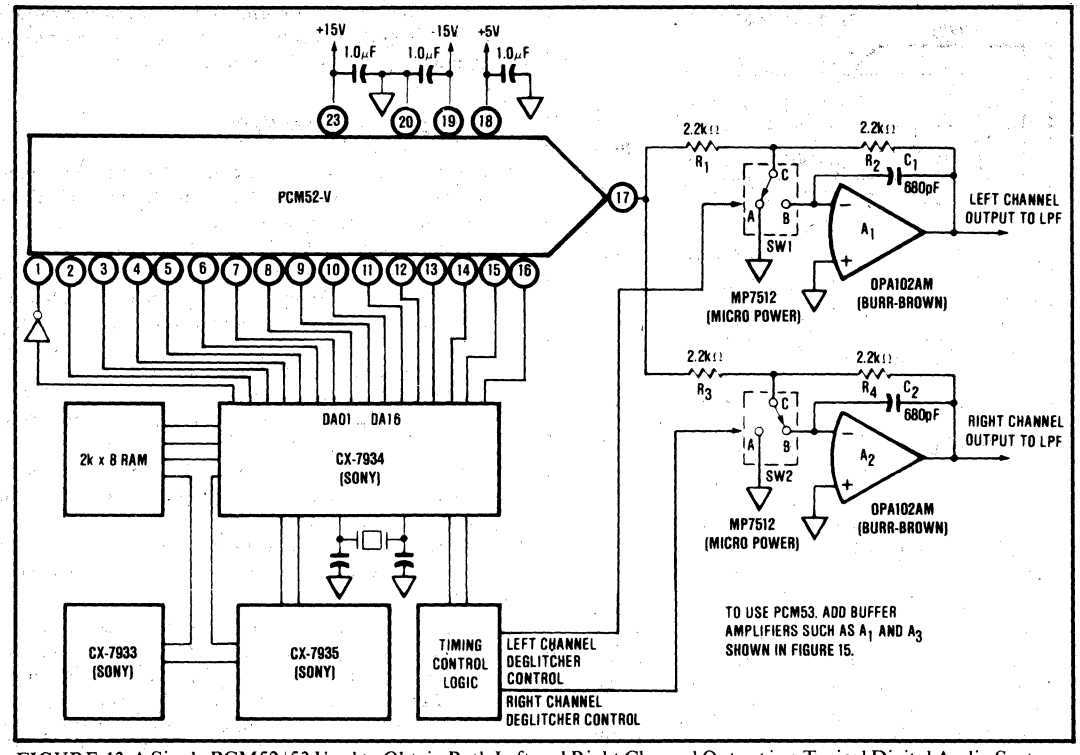


FIGURE 13. A Single PCM52/53 Used to Obtain Both Left and Right Channel Output in a Typical Digital Audio System.

SECOND-GENERATION SYSTEMS

One method of avoiding this problem and obtaining a linear phase response is to use an oversampling digital filter technique as shown in Figure 17. The Yamaha YM-3511 and YM-2201 LSI chips provide all of the functions described for the Sony chip set and, in addition, contain an onboard digital oversampling filter which effectively multiplies the sampling frequency by a factor of two and sends the parallel data at a rate of 88.2kHz to the D/A converter. Since the offset binary parallel data is directly available from the YM-2201, no external inverter is required. Furthermore, since the deglitcher control signal is also available from the YM-2201, no external timing

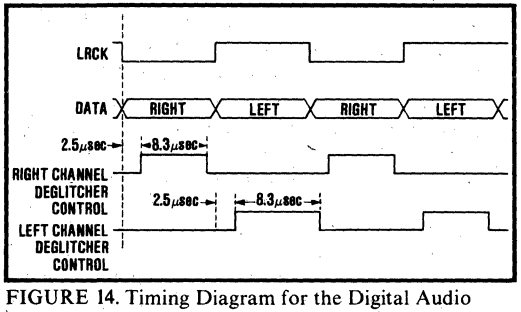


FIGURE 14. Timing Diagram for the Digital Audio System using PCM52/53 and Sony LSI Logic.

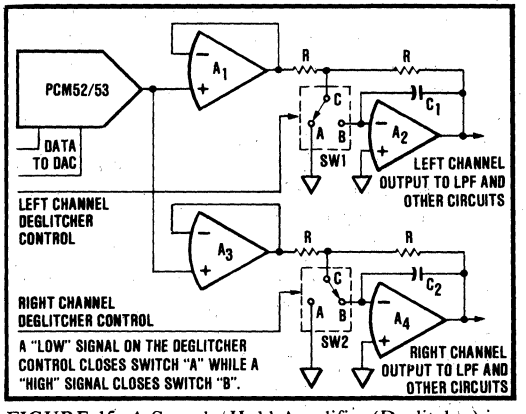


FIGURE 15. A Sample/Hold Amplifier (Deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.

control logic is required for most applications. The timing diagram for this circuit is shown in Figure 18.

This circuit requires a very fast D/A converter since the sampling frequency is multiplied by a factor of two or more. This technique results in intermodulation products being created, by mixing the sampling frequency and components of the audio frequency, that are far outside the audio band of 0 to 20kHz. These unwanted frequencies

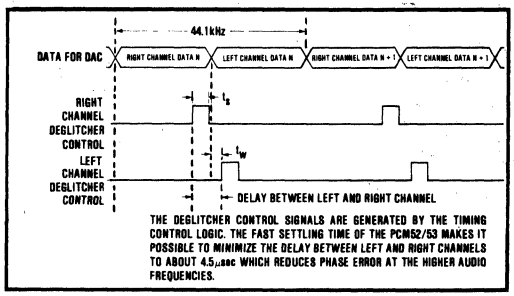


FIGURE 16. Timing Diagram for the Deglitcher Control Signals.

are easily removed by a low-order linear-phase analog filter following the deglitcher circuit since a sharp amplitude response is not required. A single PCM52/53-V can be used for both the left and right channel as long as the oversampling rate of the digital filter is two. An oversampling rate of four can be used if a separate PCM52/53 is used for each channel. This would reduce the complexities of the analog filter required even further (at the expense of an additional D/A converter).

Another factor to consider when choosing a D/A converter for digital audio applications is that the linearity of the total harmonic distortion versus output signal should be good since a change in the background noise level can be audible. The design of the PCM52/53 ensures that the linearity of the total harmonic distortion versus output signal level is very good over the full range of amplitude and frequencies. Also, no special grounding or shielding techniques are required to obtain good signal-to-noise ratio with the PCM52/53. Some converters require a high frequency clock which can couple to the analog output of the D/A converter through the output wiring and ground circuitry.

The PCM52 and PCM53 D/A converters provide a complete solution to one of the most critical portions of a digital audio system. Since the sound of the system can be affected by the D/A converter more than any other single component, the selection of which converter to use should be made with care.

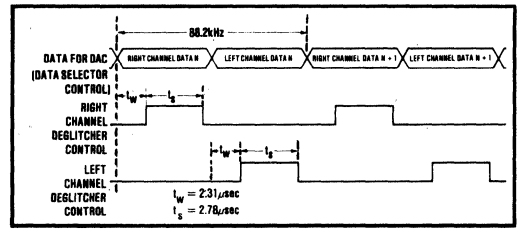


FIGURE 18. Timing Diagram for Digital Oversampling Technique when using Yamaha LSI.

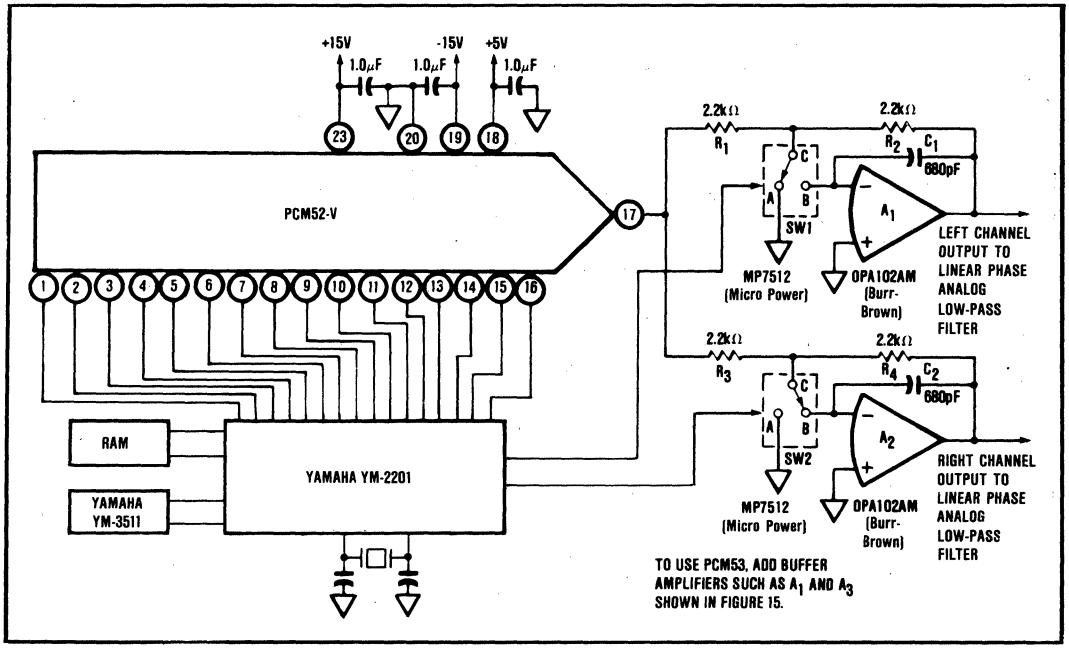


FIGURE 17. Oversampling Digital-Filter Technique Using Yamaha LSI.

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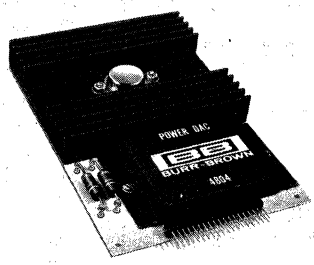


4804

Low Cost 12-BIT POWER DAC

FEATURES

- DIGITALLY PROGRAMMABLE VOLTAGE SOURCE ±30VDC, 1A Continuous Output
- RESISTOR-PROGRAMMED VOLTAGE RANGE AND CURRENT LIMIT
- LOW COST
- INPUT STORAGE REGISTER
- ±1/2LSB MAXIMUM NONLINEARITY

DESCRIPTION

The 4804 Power DAC offers versatility and low cost in automatic test equipment and process control applications. The output range is ±30VDC at 1A with built in current limiting at ±1.2A. By adding one external resistor, you can select any full scale output range less than ±30VDC and still maintain 12-bit resolution. Also, the current limiting can be varied by changing the value of two easily accessible resistors. The package was designed for mounting on a PC card and can dissipate up to 20W internally in free air with no external heat sinking required.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED DESCRIPTION

GENERAL

The 4804 consists of a 12-bit storage register with strobed inputs, a 12-bit digital-to-analog converter, and a power output stage. By changing the input code according to Table I, the output voltage may be varied between ±30V with output currents up to 2A continuous. The maximum internal power dissipation for various output conditions is described in Figure 3 and 5. Care must be taken not to exceed the power dissipation limits for the thermal environments described in the figures.

No external adjustments or components are required to achieve the specified accuracy. If improved performance is required, two adjustments will null the offset and gain errors. The procedures for adjusting these parameters are described on page 6-178.

To minimize noise levels in the 4804 the analog and digital signal returns are not internally connected. For proper operation, these two grounds must be externally connected together.

STORAGE REGISTER

The storage register consists of 12 integrated-circuit, positive-edge-triggered flip-flops utilizing TTL circuitry. The logic levels at the register inputs are transferred to the D/A converter on the positive-going edge of the strobe pulse. Strobing occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the strobe input is at either the high or low level, the inputs to the register have no effect on the D/A converter inputs. The strobe and register are fully compatible with most TTL or DTL circuits.

DIGITAL-TO-ANALOG CONVERTER

The D/A converter stage accepts the digital output from the storage register and converts it into a bipolar analog signal according to Table I.

To reduce gain and offset errors below the specified values, OFFSET ADJUST and GAIN ADJUST trim points are provided. Follow the procedure shown on page 6-178.

POWER AMPLIFIER

The power amp stage buffers the D/A converter signal and provides the power output capability. Connecting the ±30V RANGE pin to the output will preset the full scale range to ±30V, giving the transfer function described in Table I; i.e. 1 LSB = 14.65mV. R_F and R_S were selected for optimum temperature stability to minimize gain drift errors, and the offset of the Power Amplifier has been nulled at the factory. By connecting a resistor between the V_{OUT} RANGE ADJUST pin and the output, a variety of full scale ranges can be selected while maintaining 12-bit resolution.

For optimum stability, the external resistor should have a T.C. which is less than ±10ppm/°C. The ±35V inputs to the power amplifier may be reduced if full scale ranges less than ±30V are desired. To maintain the best accuracy, these supplies should not be reduced below ±15V. Since the 4804 output current is derived from the ±35V power inputs, the current-carrying capability of these power supply connecting leads should be considered.

R_P and R_M determine the output positive and negative current limits, respectively, of the output. They have been preselected for current limiting of ±1.2A, typ. The current limiting can be changed by replacing R_P and R_M with other values according to the following formula:

$$R = \frac{1.2V}{I_{current\ limit}}$$

It is not necessary that R_P and R_M be the same value. Since the output current of the 4804 flows through these resistors, the power dissipation of R_P and R_M should be considered. Both resistors are stud mounted for easy accessibility.

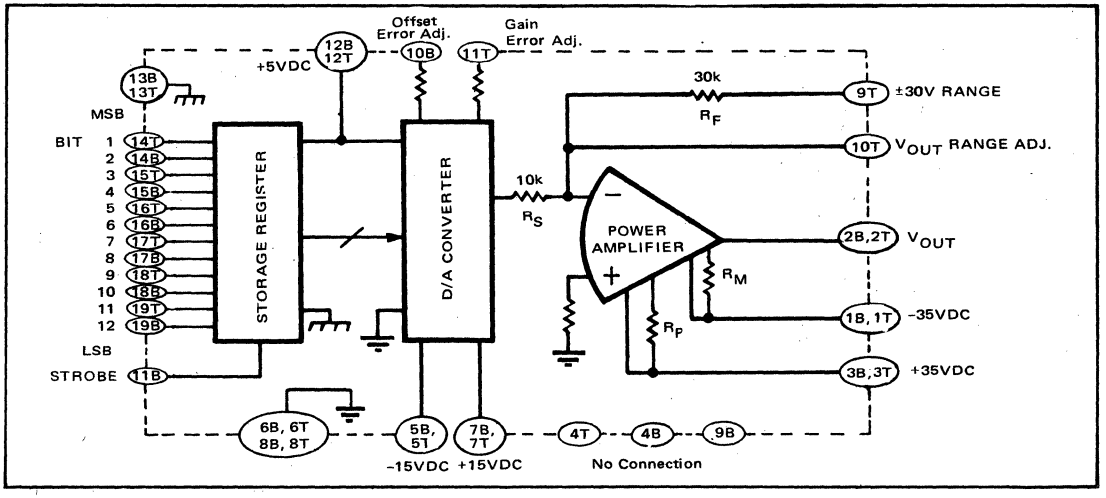


FIGURE 1. Block Diagram

SPECIFICATIONS

Typical at 25°C, rated power supplies, and V_{out} range = ±30 unless otherwise noted.

ELECTRICAL

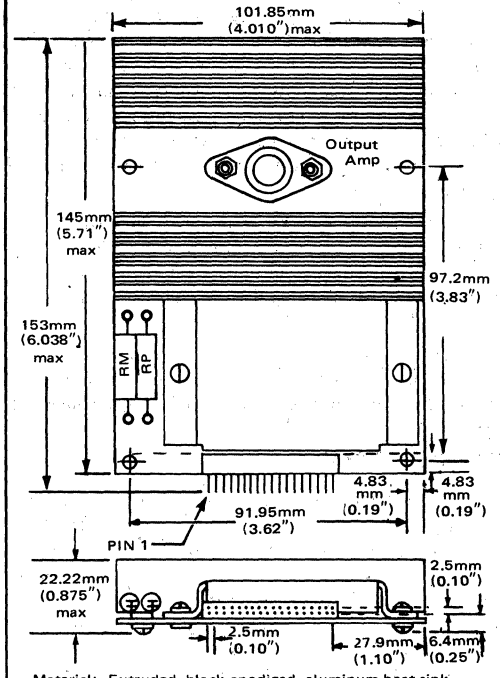
INPUT	
Resolution	12 bits
Logic levels (TTL/CMOS Compatible)	
Logical "1"	$+2V < {}^{e}in < +5.5V$ @ ≤ +0.1mA
Logical "0"	$0V < {}^{e}in < +0.8V$ @ ≤ -0.36mA
Digital Input Coding	offset binary (see Table I.)
TRANSFER CHARACTERISTICS	
TOTAL ACCURACY	
V_{out} Range = ±30V	±0.05% of reading
Individual Error Contributors	
Linearity Error (0°C to +70°C)	±½LSB max
Differential Linearity Error	±½LSB max
Output Offset Voltage	±3mV max
Drift (0°C to +70°C)	
Gain	±50ppm/°C max
Output Offset Voltage	±70μV/°C max
Differential Linearity	±2ppm/°C
Power Supply Sensitivity	
+15V Supply	2mV/V (for V_{out} = ±30V range)
-15V Supply	2mV/V (for V_{out} = ±30V range)
+ 5V Supply	6mV/V (for V_{out} = ±30V range)
±35V Supplies	400μV/V (for V_{out} = ±30V range)
Settling Time (to within 0.01% of final value for any input change)	100μsec max
OUTPUT	
Voltage Range @ I_{out} = 1.0A	±29.985V (= 30V -1LSB)
Output Current	(see Figure 5 and Note 1.)
Factory Adjusted Output Current Limit	1.2A typ
Output Resistance	1Ω max
POWER SUPPLY REQUIREMENTS	
Rated Voltages	±15VDC, +5VDC, ±35VDC
Power Supply Operating Ranges	±5%
Supply Drain	
±15V	±25mA
+5	+80mA
±35V	±40mA ±output current
TEMPERATURE RANGE	
Specification	0°C to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C

NOTE 1: Output amplifier is capable of sourcing or sinking 2 amps continuously. Resistors R_M and R_p have been selected to current limit the output current to ±1.2A typ. To increase I_{out} capability, or modify the current limit setting, replace R_M and R_p according to instructions on page 6-175. Internal power dissipation should be considered, especially at low output voltages.

ABSOLUTE MAXIMUM RATINGS

+5V Supply	+7V
±15V Supplies	±20V
±35 Supplies	±40V
Digital Inputs	+7.0V with +5V supply = +7V
Power Amp Case Temp	+125°C
Output Amplifier Power Dissipation	20W max in free air, derate 0.2W/°C above +25°C
Output Current	See Figure 5 and Note 1

MECHANICAL



Material: Extruded, black-anodized, aluminum heat sink and discrete components mounted on glass epoxy printed circuit board.

4804 Connector: Amp 2 - 86479 - 3

Recommended mating Connectors: PC card: 0806MC
Flexable: Scotchflex 3417 - 0000

Diameter of mounting holes: 3.56mm (0.14")

PIN CONNECTIONS

BOTTOM	PIN	TOP
-35V	1	-35V
Output	2	Output
+35V	3	+35V
N.C.	4	N.C.
-15V	5	-15V
Ana. Com.	6	Ana. Com.
+15V	7	+15V
Ana. Com.	8	Ana. Com.
N.C.	9	+30V Range
Offset Adj.	10	V_{out} Range Adj.
Strobe	11	Gain Adj.
+5V	12	+5V
Dig. Com.	13	Dig. Com.
Bit 2	14	Bit 1
Bit 4	15	Bit 3
Bit 6	16	Bit 5
Bit 8	17	Bit 7
Bit 10	18	Bit 9
Bit 12	19	Bit 11

TYPICAL PERFORMANCE CURVES

(Typical @ 25°C and ±15VDC Power Supplies unless otherwise noted)

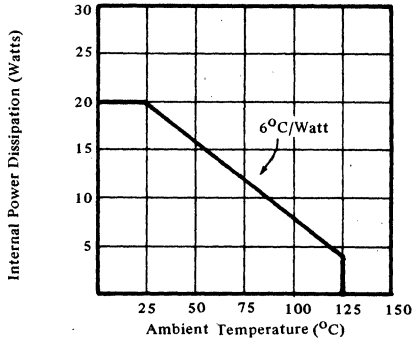


FIGURE 2. Power Derating Curve.

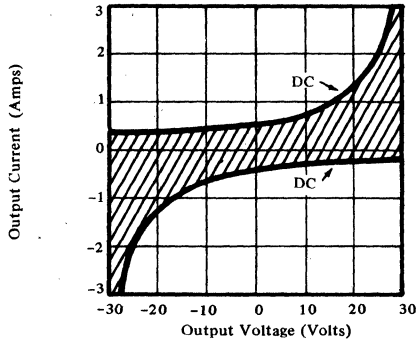


FIGURE 3. Safe Operating Area.

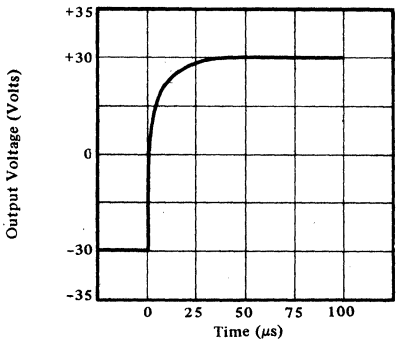


FIGURE 4. Pulse Response.

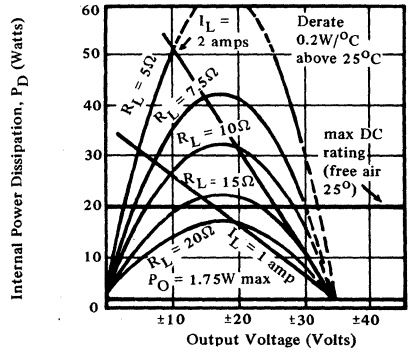


FIGURE 5. Output Amplifier Power Dissipation vs. Output Voltage.

4804

DIGITAL INPUT CODES VS. V_{OUT}		
INPUT CODE MSB LSB	**NOMINAL OUTPUT VOLTAGE**	
	±30V RANGE	**VARIABLE RANGE**
1111 11111 111	+30.000V	$+10.000\left(\frac{R_G}{10k}\right)$ V
1111 1111 1110	+29.985V	$+9.995\left(\frac{R_G}{10k}\right)$ V
1000 00000 000	+14.65mV	$+4.88\left(\frac{R_G}{10k}\right)$ mV
0 11111111 111	0.000V	0.000V
0 111111111 10	-14.65mV	$-4.88\left(\frac{R_G}{10k}\right)$ mV
0000000000001	-29.971V	$-9.990\left(\frac{R_G}{10k}\right)$ V
000000000000	-29.985V	$-9.995\left(\frac{R_G}{10k}\right)$ V

TABLE I.

PROCEDURES FOR ADJUSTING OFFSET AND GAIN ERRORS...

OFFSET AND GAIN ADJUSTMENT

The offset and gain of the D/A converter stage may be trimmed using externally connected OFFSET ADJUST and GAIN ADJUST potentiometers. The adjustment procedure is outlined below. Since the GAIN ADJUST is connected to a high impedance point in the D/A converter, a ceramic capacitor connected between this point and analog common is recommended to minimize noise pickup. The offset error should always be nulled before adjusting the gain error potentiometer.

OFFSET ADJUST PROCEDURE

Apply the digital code which could give the maximum positive voltage output and adjust the OFFSET ADJUST potentiometer for the proper output voltage. For example, if the 4804 is connected for a full scale range of ±30V, apply all ones to the input and adjust the potentiometer for an output of +30.000V.

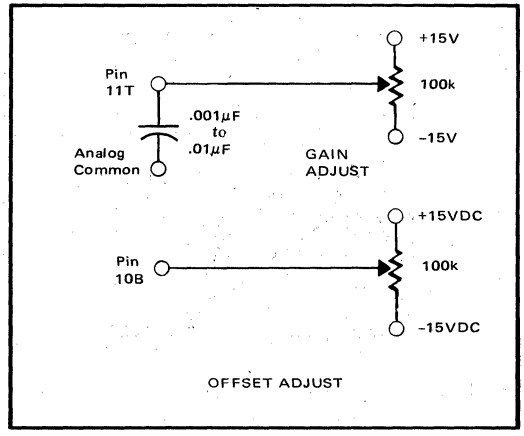


FIGURE 6.

GAIN ADJUST PROCEDURE

Apply the digital code which should give the maximum negative voltage output, and adjust the GAIN ADJUST potentiometer for the proper output voltage. For example, if the 4804 is connected for a full scale range of ±30V, apply all zeros and adjust the potentiometer for an output of -29.985V.

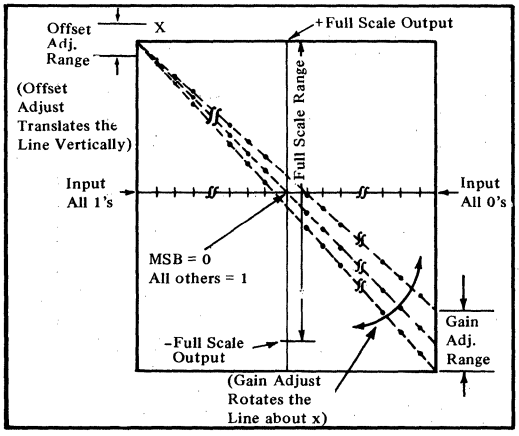


FIGURE 7.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The 4804 accepts TTL and CMOS compatible input codes in binary format. Table I shows the output voltage for selected inputs.

ACCURACY

Total Accuracy is the maximum deviation from the ideal output over the full output range. It is tested at 25°C and represents the maximum allowed value of the sum of the individual errors. The total accuracy is specified as a maximum with the 4804 in the ±30V range configuration. If an output range less than ±30V is selected, the accuracy will improve as the power amplifier gain is reduced.

Lineary Error for the 4804 is specified as a maximum over the temperature range of 0°C to +70°C. This means that the analog output will not vary by more than ±½ LSB maximum from an ideal straight line drawn between the "all bits ON" and "all bits OFF" end points.

Differential Linearity is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error spec of ±½ LSB means that the output voltage step sizes can be anywhere from ½ LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

Monotonicity over 0°C to +70°C is guaranteed in the 4804. This insures that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is measure of the change in the full scale range analog output over temperature. The GAIN DRIFT is determined by testing the end point differences at 0°C, +25°C and +70°C, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change. This specification is expressed in ppm/°C.

Offset Drift is a measure of the actual change in the output with all bits OFF (all 0's) over the specified temperature range, and is measured at 0°C, +25°C and +70°C. The maximum change in OFFSET is referenced to the OFFSET at 25°C divided by the temperature range. This drift is expressed in parts per million of full scale ranges per °C (ppm of FSR/°C).

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the effect of a power supply voltage variation on the 4804 output. It is defined as a change in output voltage per change in supply voltage with the ±30V output range. Power supply rejection is improved if a full scale range less than ±30V is selected.

OPERATING INSTRUCTIONS

REMOTE SENSING

In applications requiring that the load be located some distance from the Power DAC, the line resistance from the 4804 to the load can cause significant error, especially during operation at high currents. To minimize this problem, connect the circuit with the line resistance inside the feedback loop of the output amplifier, as shown in Figure 8. This technique effectively divides the line resistance by the open loop gain of the output amplifier (94 dB min, with R_{LOAD} 5Ω). To minimize noise pickup, the external feedback resistor should be located as close as possible to the 4804.

Since the amplifier must still overcome the voltage drop in the line inside the feedback loop, the dynamic range of the load voltage will be reduced by approximately I_{LOAD} x R_{LINE}. Proper grounding of the 4804, load, and digital stimulus will also reduce errors caused by ground loops.

THERMAL CONSIDERATIONS

The absolute maximum internal power dissipation of the output amplifier is 20 watts in free air at 25°C. Derate by 0.2W/°C above 25°C. Thermal resistance from amplifier junction to ambient is 6°C/watt. Figure 5 shows internal power dissipation as a function of otuput voltage and load resistance with ±35V supply voltages.

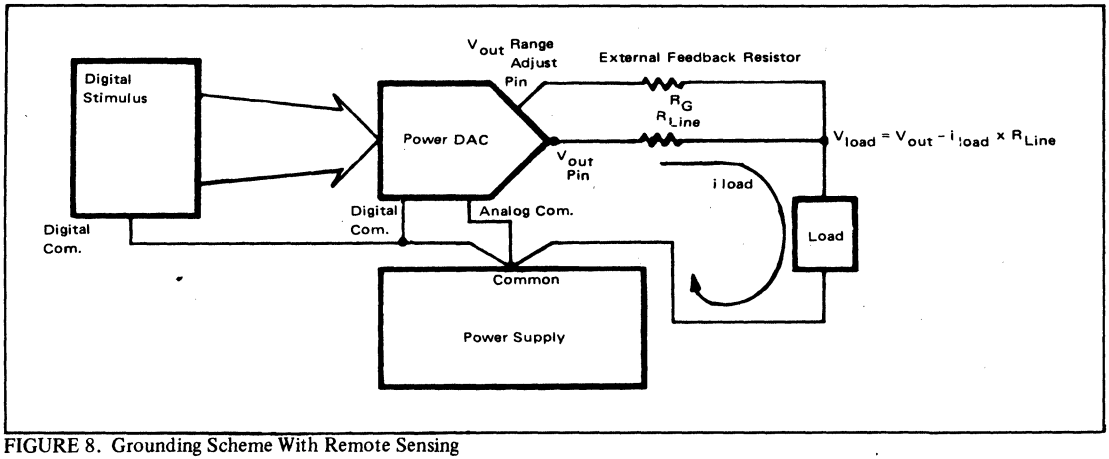
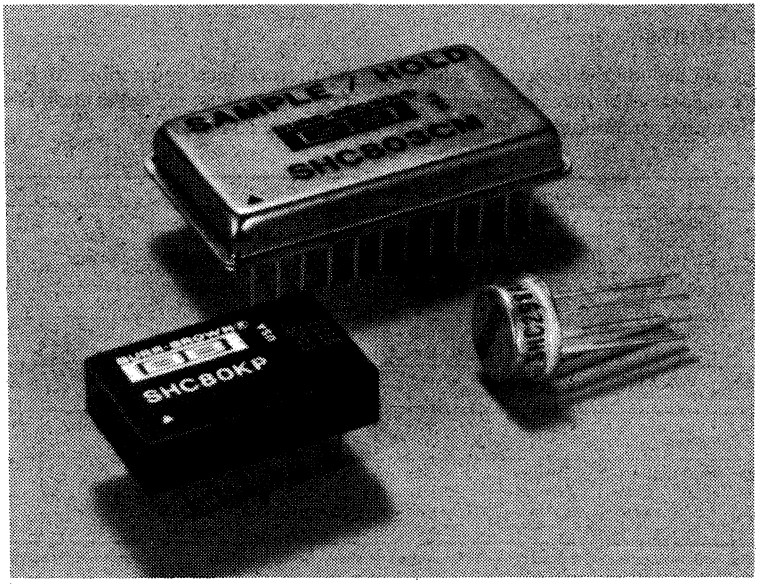


FIGURE 8. Grounding Scheme With Remote Sensing

SAMPLE/HOLD AMPLIFIERS



7

For any application requiring use of a sample/hold amplifier, consider the variety of products listed in the Selection Guide in this section. The products range from SHC298, a low cost solution for your medium-speed 12-bit system, to SHC803 and SHC804, high speed sample/holds optimized for your high bandwidth requirements.

If your needs include high performance and small size over either industrial or military temperature ranges, turn to SHC80 and SHC85. These popular products are fully self-contained, including holding capacitor.

Use of a carefully selected sample/hold can increase the sampling bandwidth of an analog-to-digital converter by up to four orders of magnitude, while insuring that an accurate value of the signal is captured at a specific point in time. In many applications not viewed as requiring high bandwidth data acquisition, optimum performance and cost may still be achieved by use of combinations of very high speed multiplexers, sample/holds, and A/D converters.

Sample/hold amplifiers—another part of the complete data acquisition solution.

SELECTION GUIDE

SAMPLE/HOLD CIRCUITS

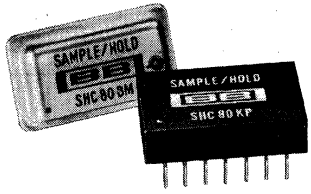
Proven technologies applied to these circuits achieve very high speed and accuracy for demanding applications. SHC298AM is a low cost monolithic. Designed to be performance compatible to Burr-Brown A/D and D/A converters, the application of all of these S/H circuits is quick and easy.

SAMPLE/HOLD CIRCUITS								
Description	Model[1]	Gain/Offset Error (%) (mV)	Charge Offset (mV)	Droop Rate (mV/msec)	Tempco (ppm of 20V/°C)	Acquisition Time (μsec)[2]	Package	Page
Low Cost, Complete	SHC80KP	±0.01, ±2 max	±2 max	0.5 max	3	10 max	DIP	7-3
High Speed, Complete	SHC85, (Q)	±0.01, ±2 max	±2 max	0.5 max	3	4.5 max	DIP[3]	7-7
	SHC85ET, (Q)	±0.01, ±2 max	±2 max	0.5 max	3	4.5 max	DIP[3]	7-7
Low Cost, Monolithic	SHC298AM	±0.01, ±7 max	±25 max	10 max[4]	4	10 max	TO-99[3]	7-11
Very-High Speed	SHM60	±0.01, ±1.5	±1.5	5	2	1 max	Module	7-23
Ultra-High Speed	SHC803BM	±0.1, ±5 max	±10 max	±5 max	±10 max	300nsec max	DIP	7-17
	SHC803CM	±0.1, ±3 max	±5 max	±5 max	±5 max	300nsec max	DIP	7-17
	SHC804BM	±0.1, ±5 max	±10 max	±5 max	±10 max	300nsec max	DIP	7-17
	SHC804CM	±0.1, ±3 max	±5 max	±5 max	±5 max	300nsec max	DIP	7-17

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See Q Program. (2) 10V step to 0.01% of final value. (3) Hermetic. (4) With 1000pF external holding capacitor.

BURR-BROWN®

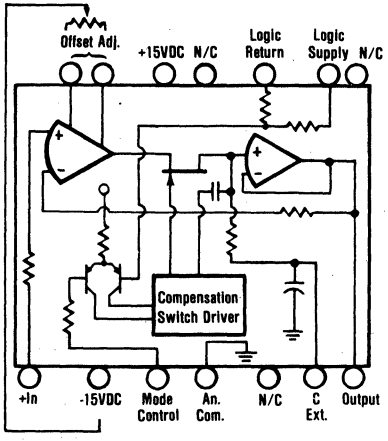
SHC80



Fast IC SAMPLE/HOLD AMPLIFIERS

FEATURES

- 14-PIN DIP PACKAGE
- 10μsec ACQUISITION TIME
- COMPLETE WITH HOLDING CAPACITOR
- ±0.01% ACCURACY
- -25°C TO +85°C TEMPERATURE RANGE (SHC80BM)



DESCRIPTION

Ultra-linear performance and fast acquisition speeds - that's the combination that makes the SHC80 models ideal for your demanding data acquisition and control applications.

The SHC80 acquires and holds up to ±10V analog signals to an accuracy of ±0.01% of full scale. Acquisition time is 12μsec for a 20V step or 10μsec for a 10V step. High performance results from the use of internally compensated circuits normally found only in larger, more expensive sample holds.

Two models give you a choice of operating temperature range: the SHC80KP (0°C to +70°C) in an epoxy package, also the SHC80BM (-25°C to +85°C) in a hermetic metal case. These units are well suited for:

Data Acquisition Systems
Data Distribution Systems
Analog Delay Circuits
Pulse Amplitude Modulation Circuits
Waveform Amplitude Measurement

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

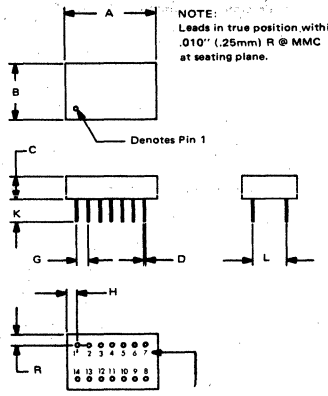
Typical at 25°C with rated supply and 1000pF internal capacitor unless otherwise noted.

MODELS	SHC80KP	SHC80BM	UNITS
INPUT			
ANALOG INPUT			
Voltage Range	±10	±10	V
Maximum Safe Input Signal	±15	±15	V
Impedance	10^8 || 5	10^8 || 5	Ω || pF
Bias Current	400	400	nA
DIGITAL INPUT	Logic Supply Voltage +5V	Logic Supply Voltage +15V	
(TTL/MOS Compatible)			Current
Mode Control			
"Sample" - Logic "1"	$2 < e < 8V$	$5.5 < e < 15V$	+50nA
"Hold" - Logic "0"	$0 < e < 0.8V$	$0 < e < 3.5V$	-50μA
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Dynamic Nonlinearity, max	±0.01(1)	±0.01	% of 20V
At min "Hold" time	1000	1000	μsec
Gain	+1.0	+1.0	V/V
Gain Error	0.01	0.01	% of 20V
Throughput Offset, max (adjust to zero)	2	2	mV
Droop Rate, max	0.5	0.5	mV/msec
Droop Rate, typ	0.2	0.2	mV/msec
Throughput Nonlinearity	±0.005	±0.005	% of 20V
Noise (rms) (10Hz to 100kHz)	100	100	μV, rms
Supply Rejection (0 to 50kHz)	200	200	μV/V
ACCURACY DRIFT			
Gain Drift	2	2	ppm of 20V/°C
Offset Drift	20	20	μV/°C
Droop Rate(2)			
At 70°C, max	10	10	mV/msec
At 85°C, max	--	25	mV/msec
DYNAMIC CHARACTERISTICS			
Full Power Bandwidth(3)	75	75	kHz
Output Slew Rate	5	5	V/μsec
Aperture Time	40	40	nsec
Aperture Time Jitter	1	1	nsec
Acquisition Time to 0.01%			
10V Step, max	10	10	μsec
20V Step, max	12	12	μsec
Feedthrough in Hold Mode	±0.02	±0.005	% of Input Step
Charge Offset, max	2	2	mV
Sample to Hold Transient			
Peak Amplitude	150	150	mV
Settling to 1mV	1	1	μsec
OUTPUT			
ANALOG OUTPUT			
Voltage Range, min	±10	±10	V
Current Range, min	±5	±5	mA
Impedance	0.5	0.5	Ω
TEMPERATURE			
Specification	0 to +70	-25 to +85	°C
Storage	-25 to +85	-55 to +125	°C
POWER SUPPLY			
Rated Voltage	±15	±15	V
Range	±14.5 to ±15.5	±14.5 to ±15.5	V
Current	±20	±20	mA
LOGIC SUPPLY			
Rated Voltage	+5	+5	V
Range	+4.75 to +15.5	+4.75 to +15.5	V
Current	1	1	mA

NOTES:
1. ±0.015 including feedthrough for SHC80KP.
2. May double every 10°C over temperature.
3. Small signal bandwidth 750kHz.

MECHANICAL

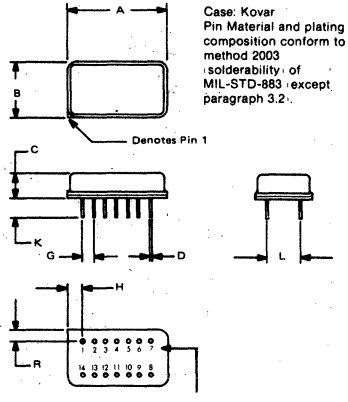
EPOXY PACKAGE - SHC80KP



Pin numbers shown for reference only.
Numbers are not marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

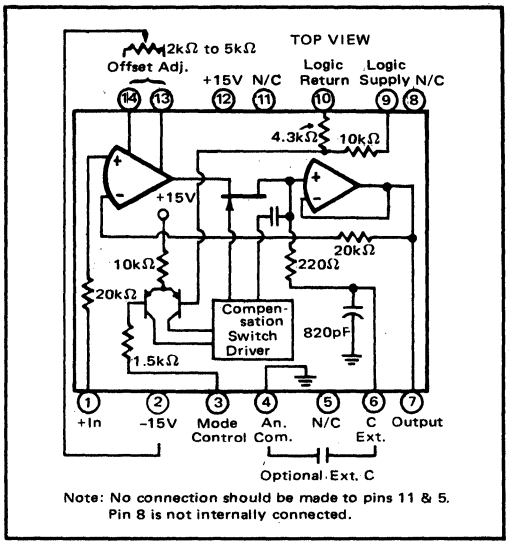
METAL PACKAGE - SHC80BM



Pin numbers shown for reference only.
Numbers are not marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

CONNECTION DIAGRAM



Note: No connection should be made to pins 11 & 5. Pin 8 is not internally connected.

DEFINITION OF SPECIFICATIONS

DYNAMIC NONLINEARITY

This is the total nonadjustable input-to-output error. It includes errors due to throughput nonlinearity, droop, thermal transients and feedthrough; in short, all errors that cannot be adjusted to zero for a 10V input change after a 10μsec acquisition time and a 1msec hold time. Offset errors may be adjusted to zero by the offset control, but gain errors must be removed by a gain adjustment elsewhere in the system. (Gain adjust not included in SHC80.)

GAIN ACCURACY

The difference due to amplifier gain errors between Input and Output voltage when in the "sample" mode.

DROOP RATE

The voltage decay at the output during the "hold" mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

The amount of input voltage change that appears at the output when the amplifier is in the "hold" mode.

THROUGHPUT - NONLINEARITY

The total charge offset and gain nonlinearity, i.e., the inaccuracy due to these two errors that cannot be corrected by gain and offset adjustments. Throughput - nonlinearity is specified over the 20V input range.

THROUGHPUT OFFSET

The sum of sample offset and charge offset.

CHARGE OFFSET

The offset that results from charge transferred from the holding capacitor to the gate capacitance of the switching FET. This charge is partially restored by a special compensation circuit when the unit goes into the "hold" mode.

ACQUISITION TIME

The time required for the output to settle to its final value within a given error band when the Mode control is switched from "hold" to "sample" (see Figure 2).

APERTURE TIME

The time required to switch from "sample" to "hold". It is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

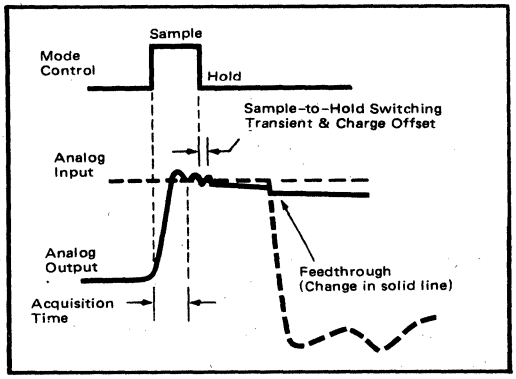


FIGURE 1. Example of Specifications.

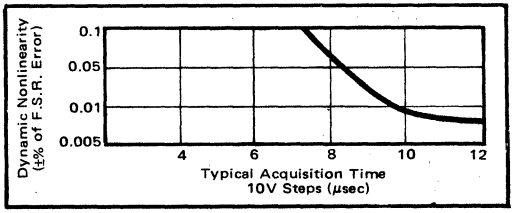


FIGURE 2. Acquisition Time vs Full Scale Range Error.

OPERATING INSTRUCTIONS

OPTIONAL EXTERNAL CAPACITOR SELECTION

The value of the external capacitor determines the droop, charge offset, and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table.

Figure 3 shows the behavior of acquisition time with added external capacitance. The behavior of droop with external C is determined by:

$$\text{Droop} = \frac{dv}{dt} = \left(\frac{0.5 \times 10^{-9}}{1000\text{pF} + C_{ext}\text{pF}}\right) \frac{\text{mV}}{\text{msec}}$$

Capacitors with high insulation resistance and low dielectric absorption, such as teflon or polystyrene should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor to minimize droop errors.

OFFSET ADJUSTMENT

Connect a 2kΩ to 5kΩ multiturn potentiometer with a max TCR or 150ppm/°C as shown in the Connection Diagram, and adjust the offset with the input grounded. During the adjustment, the sample/hold should be switching continuously between the "sample" and the "hold" mode. Adjust the error to zero when the unit is in the "hold" mode. This procedure insures that charge offset as well as amplifier offset error will be removed.

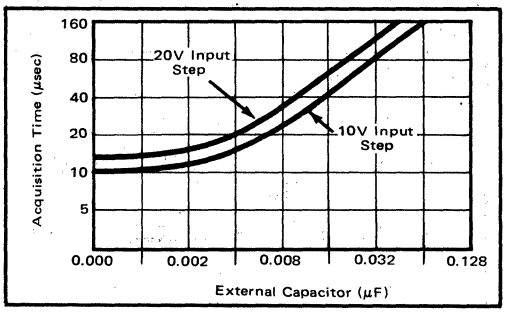


FIGURE 3. Acquisition Time vs External Capacitor.

LOGIC THRESHOLD PROGRAMMING

Pin 10 is normally connected to the logic return and pin 9 to a positive logic supply. The logic threshold is determined by the 4.3kΩ and 10kΩ resistors shown in the connection diagram. The threshold is 1.5V for logic operated on a +5V supply and 4.5V for a +15V logic supply. If it is not convenient to connect a logic return and supply to the SHC80, pin 10 may be connected to the analog return and pin 9 to +15V for 15V logic or to +15V, through a 27kΩ resistor for 5V logic. The mode control switching transistors have sufficient current gain to allow the mode control pin to be driven from MOS logic. The mode control polarity may be reversed by connecting an externally-derived threshold voltage to pin 3 and by connecting pins 9 and 10 to the mode control source.

APPLICATIONS

DATA ACQUISITION SYSTEM

The SHC80 makes an excellent device for reducing aperture time and eliminating conversion noise from high gain circuitry in data acquisition systems. When it is combined with Burr-Brown's 16-channel MPC-16S Analog Multiplexer and ADC80 A/D Converter, you have a compact 16-channel data acquisition system with 25kHz throughput sampling rates and ±0.02% (RSS) accuracy.

SIMULTANEOUS SAMPLE/HOLD

Time correlation of sampled data signals may be implemented by using one sample/hold for each analog signal prior to input to an analog multiplexer. The SHC80's low aperture time of 40nsec practically eliminates channel-to-channel time slew. The throughput sampling rate and the number of data chanels will determine the maximum "hold" time and hence, the worst-case droop error of the sample/hold in the last channel to be sampled prior to the next "refresh" or sample/hold command. This droop error may be minimized by adding external capacitance to the SHC80 as shown in Figure 3.

The droop error is computed by:

Max Droop Error (Channel N) = (T x n)(Droop rate)

Where T = 1/System Sample Rate and

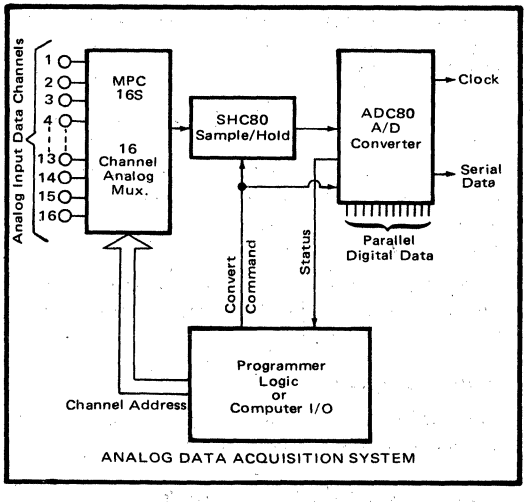
n = number of multiplexer data channels.

Example:

For a 10-bit, 32-channel system with throughput sample rate of 25kHz, assuming no external capacitance, the droop error of channel N is:

Droop Error (E_D) = (1/25kΩ)32 x (500 x 10^{-3}) = 640µV.

For ±10V input signal range and 10-bit resolution, the resolution of ±1/2LSB is ±9.77mV. This droop error is less than 0.032LSB (negligible), and no external C is needed to reduce the droop of the SHC80.



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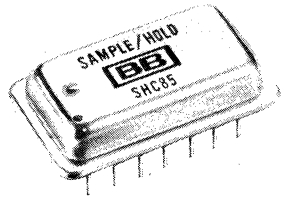
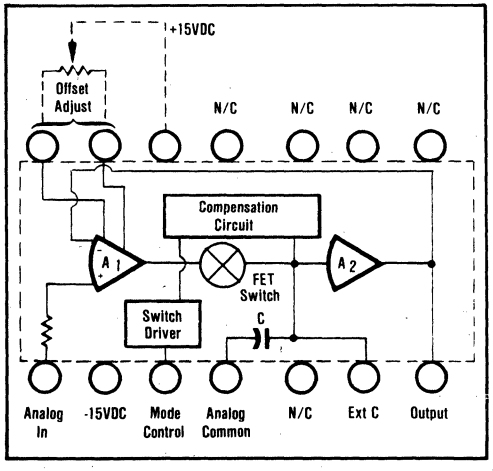


SHC85
SHC85ET

Fast IC
SAMPLE/HOLD AMPLIFIERS

FEATURES

- 14-PIN DIP PACKAGE
- 5μsec ACQUISITION TIME
- COMPLETE WITH HOLDING CAPACITOR
- ±0.01% ACCURACY
- −55°C TO +125°C TEMPERATURE RANGE (SHC85ET)



DESCRIPTION

The SHC85 is designed to acquire and hold up to ±10VDC analog signals to an accuracy of ±0.01% of full scale range in 5μsec for a 20-volt step or 4.5μsec for a 10VDC step. Featuring internally compensated circuits normally found only in more expensive and larger sample/holds, the SHC85 offers ultra-liner performance and fast acquisition speeds for the most demanding data acquisition and control applications.

Two models are available: the SHC85 is specified for 0°C to 70°C operation, and the SHC85ET is specified for -55°C to +125°C operation.

The SHC85/SHC85ET are well suited for use in:

Data Acquisition Systems
Data Distribution Systems
Analog Delay Circuits
Pulse Amplitude Modulation Circuits
Waveform Amplitude Measurement

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SPECIFICATIONS

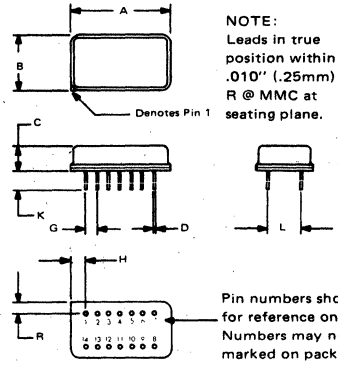
Typical at 25°C with rated supply and a 1000pF internal capacitor unless otherwise noted.

ELECTRICAL

MODELS	SHC85	SCH85ET	UNITS
INPUT			
ANALOG INPUT			
Voltage Range	±10	±10	V
Maximum Safe Input Signal	±15	±15	V
Resistance	10^8	10^8	Ω
Bias Current	50	50	nA
DIGITAL INPUT (TTL Compatible)			
Mode Control	Voltage	Current	
"Sample" - Logic "1"	+2.0V < e < +8V	50nA	
"Hold" - Logic "0"	0V < e < +0.8V	-50μA	
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Dynamic Nonlinearity, max	±0.01	±0.01	% of 20V
At min. "Hold" Time	1000	1000	μsec
Gain	+1.0	+1.0	V/V
Gain Error	±0.01	±0.01	% of 20V
Throughput Offset, max (adjust to zero)	2	2	mV
Droop Rate, max	0.5	0.5	mV/msec
Droop Rate, typical	0.125	0.125	mV/msec
Throughput Nonlinearity	±0.005	±0.005	% of 20V
Noise, rms (10Hz to 100kHz)	100	100	μV
Supply Rejection (0 to 50kHz)	100	100	μV/V
ACCURACY DRIFT			
Gain Drift	±2	±2	ppm of 20V/°C
Offset Drift	±25	±25	μV/°C
Droop Rate			
At 70°C, max	10	10	mV/msec
At +125°C, max	--	200	mV/msec
DYNAMIC CHARACTERISTICS			
Bandwidth (Full Power (1))	200	200	kHz
Output Slew Rate	20	20	V/μsec
Aperture Time	30	30	nsec
Acquisition Time (to ±0.01%)			
10V Step, max	4.5	4.5	μsec
20V Step, max	5.0	5.0	μsec
Feedthrough in Hold Mode	±0.005	±0.005	% of step change
Charge Offset, max, at 0V Input	±2	±2	mV
Sample-to-Hold Transient			
Peak Amplitude	50	50	mV
Settling to 1mV	0.5	0.5	μsec
OUTPUT			
ANALOG OUTPUT			
Voltage Range	±10	±10	V
Current Range	±10	±10	mA
Impedance	0.1	0.1	Ω
TEMPERATURE			
Specification	0 to +70	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C
POWER SUPPLY			
Rated Voltage	±15	±15	VDC
Range	±14.5 to ±15.5	±14.5 to ±15.5	VDC
Current	±13	±13	mA

NOTE:
1. Small signal bandwidth is 3MHz.

MECHANICAL



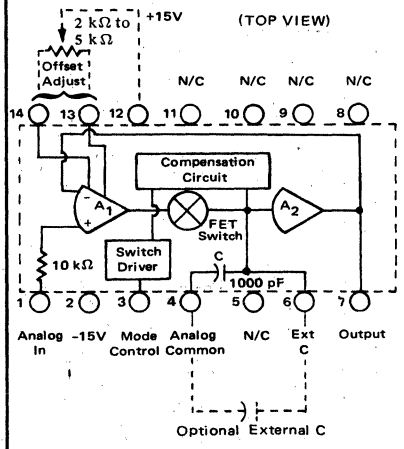
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Case: Kovar
Pin material and plating composition conform to method 2003 solderability of MIL-STD-883 except paragraph 3.2 . Mating Connector: 0145MC

CONNECTION DIAGRAM



NOTE: Pins 5, 8, 9, 10 and 11 are not internally connected.

DEFINITION OF SPECIFICATIONS

DYNAMIC NONLINEARITY
This is the total nonadjustable input to output error. This specification includes throughput nonlinearity and errors due to droop, thermal transients and feedthrough, in short, all errors that cannot be adjusted to zero for a 10V input change after a 5μsec acquisition time and a 1msec hold time. Offset errors must be adjusted to zero by the offset control and gain errors must be adjusted to zero by a gain adjustment elsewhere in the system (gain adjust not included in SHC85).

GAIN ACCURACY
The difference due to amplifier gain errors between Input and Output voltage when in the "sample" mode.

DROOP RATE
The voltage decay at the output when in the "hold" mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH
The amount of the input voltage change that appears at the output when the amplifier is in the "hold" mode (see Figure 1).

THROUGHPUT - NONLINEARITY
The total charge offset and gain nonlinearity. That is, the inaccuracy due to these two errors that cannot be corrected by gain and offset adjustments. Throughput - nonlinearity is specified over the 20V input range.

THROUGHPUT OFFSET
The sum of sample offset and charge offset.

CHARGE OFFSET
The offset that results from charge transferred from the holding capacitor to the gate capacitance of the switching FET. This charge is partially restored by a special compensation circuit when the unit goes into the "hold" mode.

ACQUISITION TIME
The time required for the output to settle to its final value within a given error band, when the Mode control is switched from "hold" to "sample" (see Figure 2).

APERTURE TIME
The time required to switch from "sample" to "hold". The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

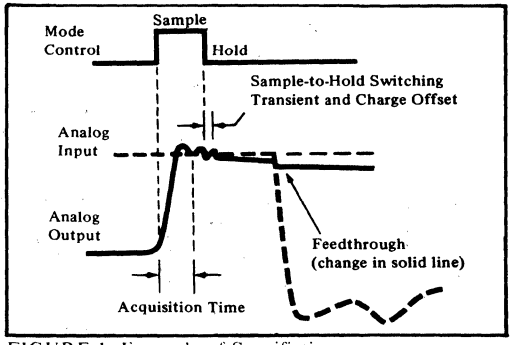


FIGURE 1. Example of Specifictions.

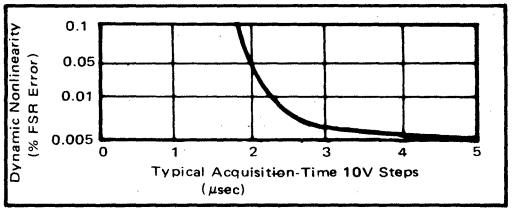


FIGURE 2. Acquisition Time vs Full Scale Range Error.

OPERATING INSTRUCTIONS

OPTIONAL EXTERNAL CAPACITOR SELECTION
The value of the external capacitor determines the droop, charge offset and acquisiiton time of the sample hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table.

Figure 3 shows the behavior of acquisition time with added external capacitance. The behavior of droop with external C is determined by:

$$\text{Droop} = dv/dt = (0.5 \times 10^{-9})/(1000\text{pF} + C_{ext})$$

Capacitors with high insulation resistance and low dielectric absorption, such as teflon or polystyrene should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor; this will minimize droop errors.

OFFSET ADJUSTMENT
Connect a 2kΩ to 5kΩ multiturn potentiometer with a TCR of 150ppm °C or less as shown in the Connection Diagram. The offset should be adjusted with the input grounded. During the adjustment, the sample hold should be switching continuously between the "sample" and the "hold" mode. The error should then be adjusted to zero where the unit is in the "hold" mode. In this way, charge offset as well as amplifier offset will be adjusted.

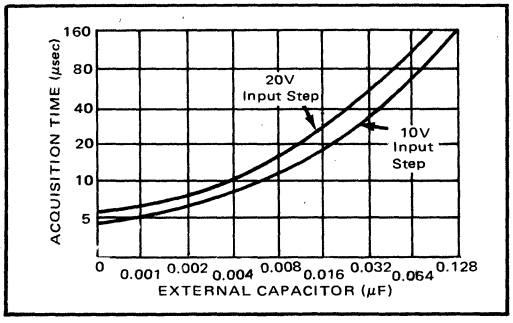
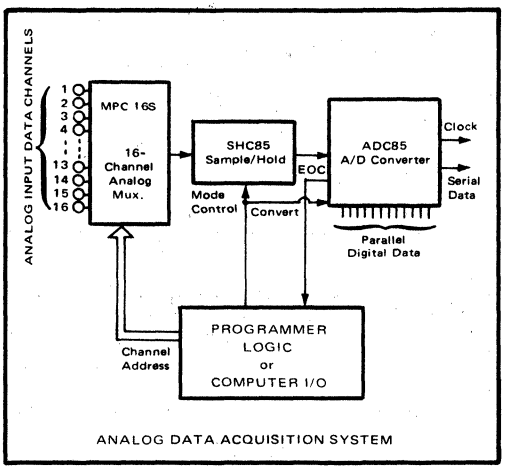


FIGURE 3. Acquisition Time vs External Capacitor.

APPLICATIONS

DATA ACQUISITION SYSTEM

The SHC85 makes an excellent device for reducing aperture time in a data acquisition system. When combined with Burr-Brown's 16-channel MPC-16S Analog Multiplexer and ADC85 10- or 12-bit A D Converter, you can have a compact 16-channel data acquisition system with 50kHz to 65kHz throughput sampling rates and 0.02 percent (RSS) system accuracy.



ANALOG DATA ACQUISITION SYSTEM

SIMULTANEOUS SAMPLE/HOLD

Time correlation of sampled data signals may be implemented by using one sample, hold for each analog signal prior to input to an analog multiplexer. The SCH85 low aperture time of 30nsec practically eliminated channel-to-channel time slew. The throughput sampling rate and the number of data channels will determine the maximum Hold time and hence, the worst-case droop error of the sample hold in the last channel to be sampled prior to the next "refresh" or sample hold command. This droop error may be minimized by adding external capacitance to the SHC85 as shown in Figure 3.

The droop error is computed by:

MAX DROOP ERROR (CHANNEL N)=(T x n) (Droop rate)

Where T = 1 System Sampling Rate and n = number of multiplexer data channels.

EXAMPLE:

For a 10-bit, 32-channel system with throughput sample rate of 50kHz, assuming no external capacitance, the droop error of channel N is:

Droop Error (E_D) = [(1 50kΩ) x 32][(500 x 10^{-3})] = 320μV.

For ±10V input signal range and 10-bit resolution, the resolution of ±1 2LSB is ±9.77mV. This droop error is less than 0.016LSB (negligible), and no external C need be added to reduce the droop of the SHC85.

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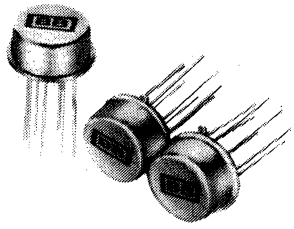


SHC298AM

Low Cost Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

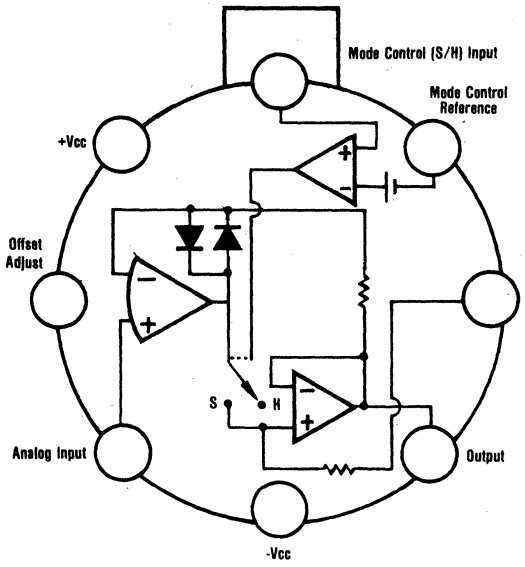
- 12-BIT THROUGHPUT ACCURACY
- LESS THAN 10μsec ACQUISITION TIME
- WIDEBAND NOISE LESS THAN 20μV, rms
- RELIABLE MONOLITHIC CONSTRUCTION
- $10^{10}\Omega$ INPUT RESISTANCE
- TTL/PMOS/CMOS-COMPATIBLE LOGIC INPUT

DESCRIPTION

The SHC298AM is a high performance monolithic sample/hold circuit which features very-high DC accuracy with fast acquisition times and a low droop rate. With the addition of one external holding capacitor, 12-bit accuracy can be achieved with a 6μsec acquisition time. Droop rates less than 5mV/min can be achieved with a 1μF holding capacitor.

The fully differential logic inputs have low input current, and are compatible with TTL, PMOS, and CMOS logic families. The input offset adjustment can be made using a single external potentiometer and resistor, and the adjustment does not degrade input offset drift.

The SHC298AM will operate with power supplies ranging from ±5VDC to ±18VDC. It is available in a hermetically sealed 8-lead low profile package, and is specified for a temperature range from -25°C to +85°C. The SHC298AM is the best price/performance bargain in its class. It is well suited for use in data acquisition systems, data distribution systems, analog delay circuits, and pulse amplitude modulation circuits.



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SPECIFICATIONS

ELECTRICAL

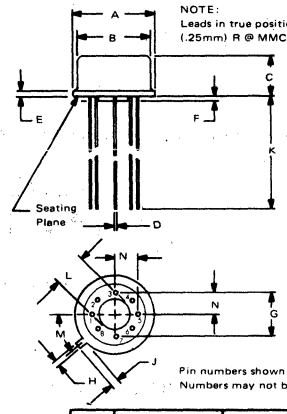
Specifications at T_J = +25°C, ±15V supplies, 1000pF holding capacitor, -11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5V unless otherwise noted.

	SHC298AM			
MODEL	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
ANALOG INPUT				
Resistance		10^{10}		Ω
Bias Current (1)		10	50	nA
DIGITAL INPUT	Pin 7	Pin 8	Circuit State	
Mode Control Truth Table	0V	+2.4V	Sample (Track)	
	0V	+0.8V	Hold	
	+2.4V	+2.8V	Hold	
	+0.8V	+2.8V	Sample (Track)	
Mode Control and Mode Control Reference Input Current			10	μA
Differential Logic Threshold	0.8	1.4	2.4	V
TRANSFER CHARACTERISTICS				
ACCURACY (+25°C)				
Throughput Nonlinearity for Hold Time < 1msec		±0.010	±0.015	% of 20V
Gain		+1.0		V/V
Gain Error		±0.004	±0.010	%
Input Voltage Offset (adjust to zero) (1)		±2	±7	mV
Droop Rate (1)		±30	±200	μV/msec
Charge Offset (2)		±15	±25	mV
Noise (rms) 10Hz to 100kHz		10	20	μV
Power Supply Rejection		±25	±100	μV/V
ACCURACY DRIFT				
Gain Drift		3	4	ppm/°C
Input Offset Drift		15	70	μV/°C
Charge Offset Drift C = 1000pF		50	150	μV/°C
Charge Offset Drift C = 10,000pF		20	50	μV/°C
Droop Rate at T_J = +85°C		1	10	mV/msec
DYNAMIC CHARACTERISTICS				
Full Power Bandwidth, C = 1000pF	75	125		kHz
Full Power Bandwidth, C = 10,000pF	10	16		kHz
Output Slew Rate, C = 1000pF	7	10		V/μsec
Output Slew Rate, C = 10,000pF	1.4	2		V/μsec
Aperture Time				
Negative Input Step		125	200	nsec
Positive Input Step		30	45	nsec
Acquisition Time (C = 1000pF)				
to ±0.01%, 10V step		6	10	μsec
to ±0.01%, 20V step		8	12	μsec
to ±0.1%, 10V step		5	9	μsec
to ±0.1%, 20V step		7	11	μsec
Sample/Hold Transient				
Peak Amplitude		160		mV
Settling to 1mV		1.0	1.5	μsec
Feedthrough (Response to 10V Input Step)		±0.007	±0.015	% of 20V
OUTPUT				
ANALOG OUTPUT				
Voltage Range	±11.5			V
Current Range	±2			mA
Impedance (In hold mode)		0.5	4	Ω
POWER SUPPLY				
Rated Voltage		±15		VDC
Range	±5.0		±18	VDC
Current (1)		±4.5	±6.5	mA

NOTES:

1. These parameters guaranteed over a supply voltage range of ±5V to = ±18V.
2. Charge offset is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the charge offset is inversely proportional to hold capacitor value.

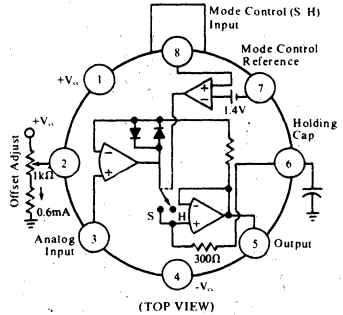
MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
³H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin Material and Plating Composition: Conforms to MIL-STD-883 method 2003 (solderability).
Hermeticity: Conforms to MIL-STD-883, method 1014, condition C, step 1, Fluorocarbon (gross leak) and method 1014, condition A, Helium, 5 x 10^{-8}cc/sec (fine leak).
Connector: None.

PIN CONFIGURATION



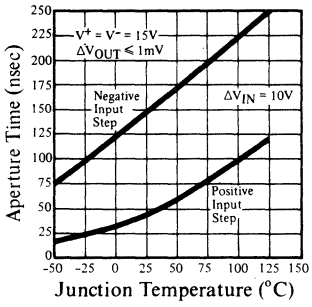
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 1)	500mW
Operating Temperature Range	-25°C to +85°C
Storage Temperature Range	-65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic-to-Logic Reference Differential Voltage (Note2)	+7V, -30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10sec
Lead Temperature (soldering, 10 seconds)	300°C

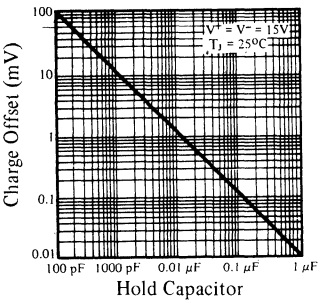
NOTES:
1. The maximum junction temperature is +100°C, when operating at elevated ambient temperature, the power dissipation must be derated based on a thermal resistance (θ_{JA}) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

TYPICAL PERFORMANCE CURVES

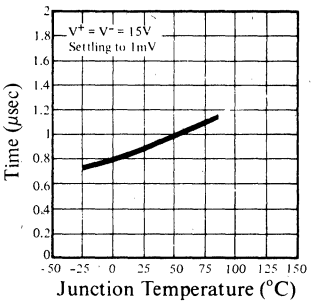
APERTURE TIME



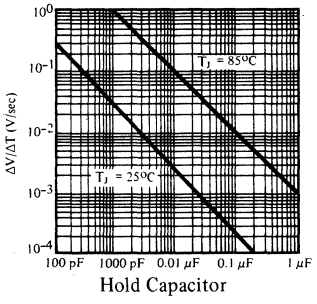
CHARGE OFFSET



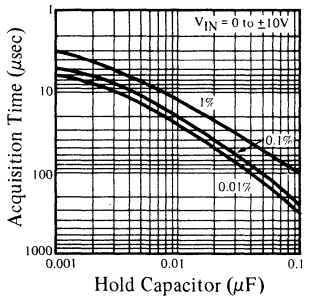
SAMPLE/HOLD TRANSIENT SETTLING TIME



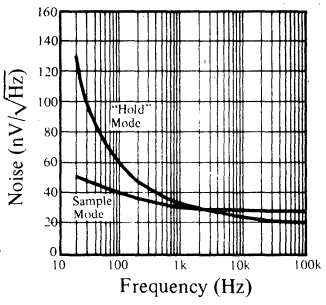
OUTPUT DROOP RATE



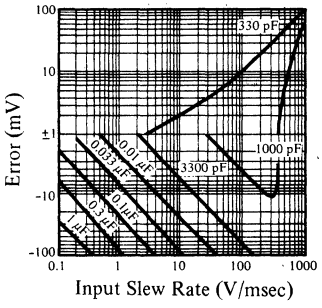
ACQUISITION TIME



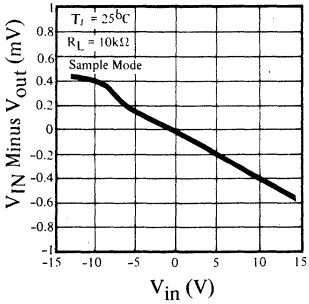
OUTPUT NOISE



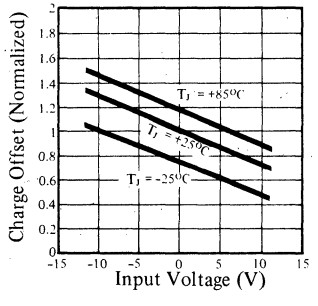
DYNAMIC SAMPLING ERROR



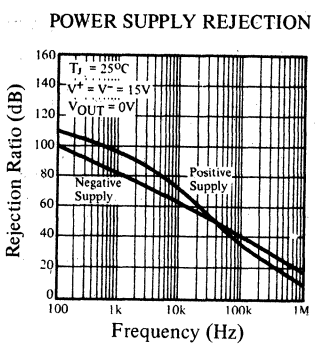
GAIN ERROR

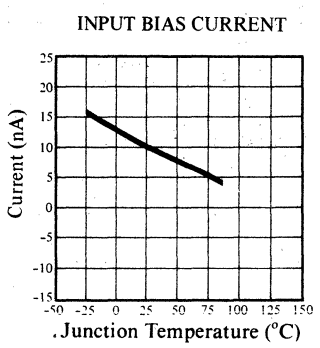


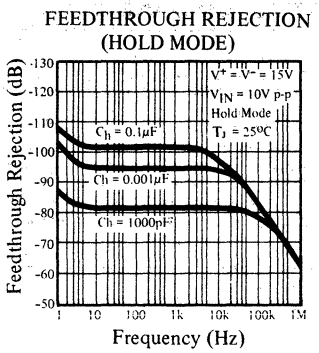
CHARGE OFFSET



SHC298







DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

Throughput nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, 1msec of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000pF holding capacitor, 10V input changes, 10μsec acquisition time, and 1msec Hold time (see Figure 1).

GAIN ACCURACY

Gain Accuracy is the difference between Input and Output voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

Feedthrough is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

APERTURE TIME

Aperture Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.

CHARGE OFFSET

Charge Offset is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

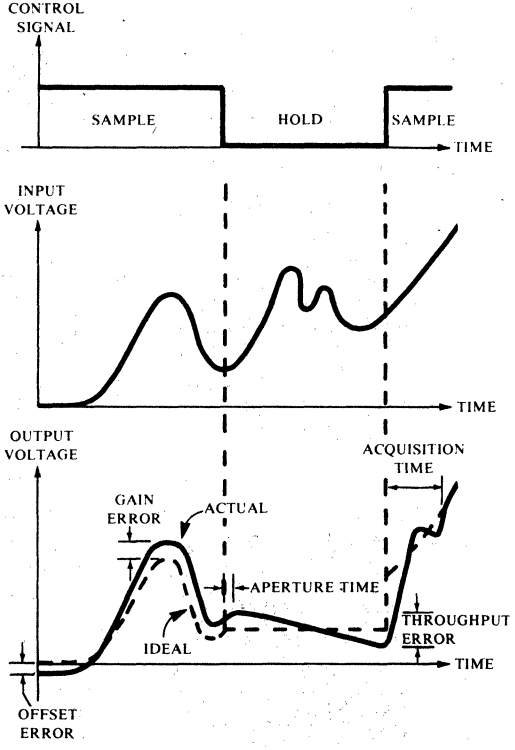


FIGURE 1. Sample/Hold Errors.

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as teflon, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce chage offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample/Hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001μF capacitor. With a capacitor of 0.01μF the droop will reduce to approximately 2.5μV/msec and the charge offset to approximately 1.5mV. The behavior of acquisition time with changes in external capacitance is shown in Typical Performance Curves.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001μF capacitor is used, it will not be possible to adjust the full offset error at the sample/hold. It should be adjusted elsewhere in the system.

APPLICATIONS

DATA ACQUISITION

The SHC298AM may be used to hold data for conversion with an analog-to-digital converter or used to provide Pulse Amplitude Modulation (PAM) data output (see Figures 2 and 3).

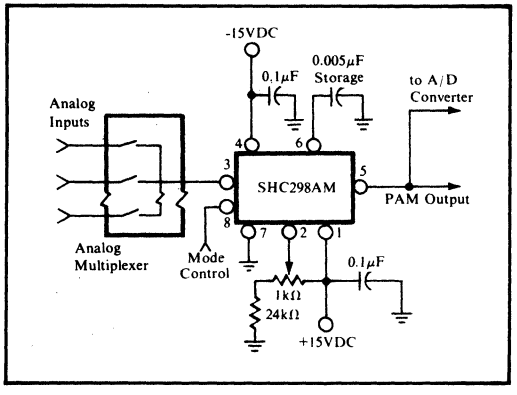


FIGURE 2. Data Acquisition.

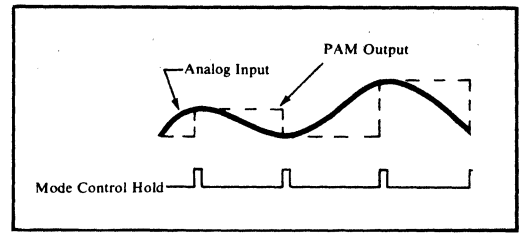


FIGURE 3. PAM Output.

DATA DISTRIBUTION

The SHC298AM may be used to hold the output of a digital-to-analog converter whose digital inputs are multiplexed (see Figure 4).

TEST SYSTEMS

The SHC298AM is also well suited for use in test systems to acquire and hold data transients for human operators or for other parts of the test system such as comparators, digital voltmeters, etc.

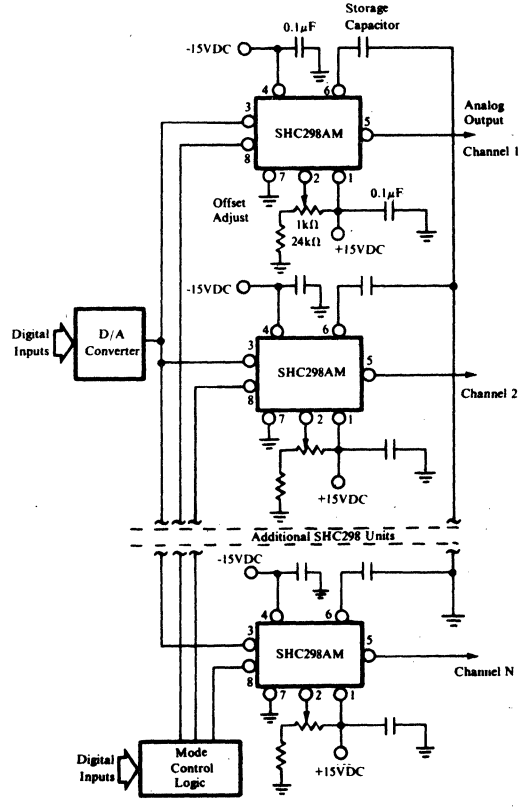


FIGURE 4. Data Distribution.

SHC298

With a 0.1μF storage capacitor, the output may be held 10sec with less than 0.1% error. With a 1μF storage capacitor, the output may be held more than 15 minutes with less than 1% error.

CAPACITIVE LOADING

SHC298 is sensitive to capacitive loading on the output and may oscillate. When driving long lines, a buffer should be used.

HIGH SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the analog-to-digital converter. If two or more sample/holds are used with a high speed multiplexer, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched on to the ADC, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this data by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed (see Figure 5). For low level systems, an instrumentation amplifier and double-ended multiplexer may be connected to the sample/hold inputs. The settling time of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the channel conversion time as before.

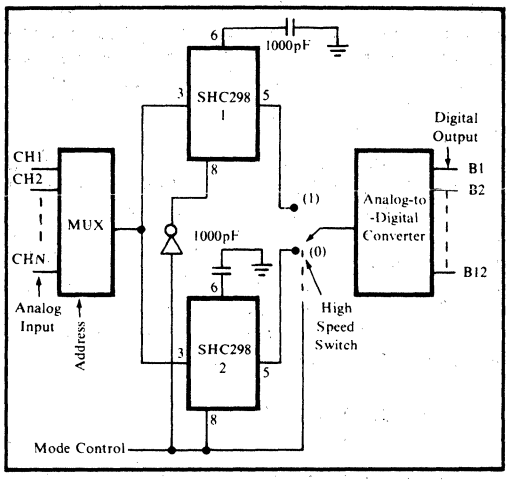
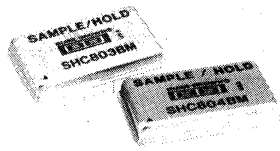


FIGURE 5. "Ping-Pong" Sample Holds.

BURR-BROWN®

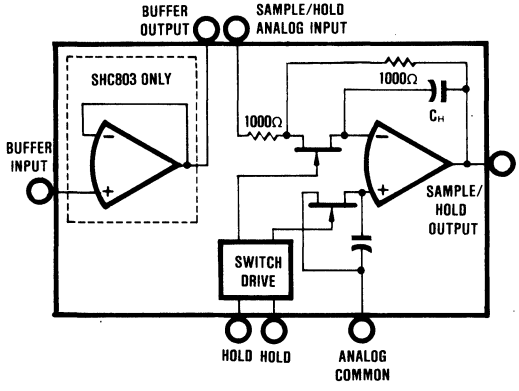


SHC803BM, CM
SHC804BM, CM

Ultra-High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- 350nsec max ACQUISITION TIME
- ±0.01% THROUGHPUT NONLINEARITY
- 150nsec max SAMPLE-TO-HOLD SETTLING TIME
- INPUT BUFFER (SHC803)
- 24-PIN HERMETICALLY-SEALED METAL PACKAGE



DESCRIPTION

The SHC803 and SHC804 are high speed sample/hold amplifiers designed for use in fast 12-bit data acquisition systems and signal processing systems. The SHC803 contains a fast-settling unity-gain amplifier for buffering high impedance sources or for use with CMOS multiplexers.

The SHC804 acquires a 10V signal change in less than 350nsec to ±1/2LSB at 12 bits. Throughput nonlinearity error is guaranteed to be within ±1/2LSB for 12-bit systems. Stability over temperature is excellent, with only ±5ppm/°C of gain drift and ±4ppm of FSR/°C of charge offset drift over the −25 to +85°C temperature range.

The ±25psec maximum aperture uncertainty of SHC803 and SHC804 permits sampling (to ±0.01% of Full Scale Range) of signals with rates of change of up to 100V/μsec. These sample/holds have been optimized for use with Burr-Brown's high speed 12-bit analog-to-digital converter, model ADC803. Together these components are capable of accurately digitizing fast changing signals at sample rates as high as 500k samples per second.

The digital inputs (HOLD and $\overline{\text{HOLD}}$) are TTL-compatible. Power supply requirements are ±15V and +5V and the specification temperature range is −25°C to +85°C. The SHC803 and SHC804 are packaged in a 24-pin dual-in-line hermetic metal package. SHC804 is pin-compatible with other sample/holds on the market with similar performance characteristics.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies and a 1kΩ output load unless otherwise specified.

MODEL	SHC803/SHC804BM			SHC803/804CM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
SAMPLE/HOLD INPUTS [without input buffer]							
ANALOG							
Voltage Range	±10.25	±11		*	*		V
R_{IN}		1.00			*		kΩ
DIGITAL [HOLD, $\overline{HOLD}$]							
V_{IH}	+2.0			*			V
V_{IL}			+0.8			*	V
I_{IH}, V_{IN} = +2.7V			+60			*	µA
I_{IL}, V_{IN} = +0.4V			−1.2			*	mA
SAMPLE/HOLD TRANSFER CHARACTERISTICS [without input buffer]							
ACCURACY							
Sample Mode							
Gain		−1			*		V/V
Gain Error			±0.1			*	%
Temperature Coefficient		±3	±10		±1	±5	ppm/°C
Linearity Error		±0.001	±0.005		*	*	% of FSR[1]
Zero Offset		±1	±5		±0.5	±3	mV
Temperature Coefficient		±1	±2.5		±0.5	±1.5	ppm of FSR/°C
Hold Mode							
Charge Offset		±2	±10		±1	±5	mV
Temperature Coefficient		±3	±10		±2	±4	ppm of FSR/°C
Droop Rate: at +25°C		±0.5	±5		*	*	µV/µsec
+85°C			±0.5			±0.1	mV/µsec
Throughput Nonlinearity			±0.01			*	% of FSR
Power Supply Sensitivity[2]: ±V_{CC}			±0.002			*	% of FSR/%V_{CC}
V_{DD}			±0.003			*	% of FSR/%V_{DD}
DYNAMIC CHARACTERISTICS							
Acquisition Time (with 10V step)							
to within: ±0.1% (±10mV)		220			*		nsec
±0.01% (±1mV)		250	350		*	*	nsec
Sample-to-Hold Settling Time							
to within ±0.01% (±1mV)		100	150		*	*	nsec
Sample-to-Hold Transient Amplitude		60	150		*	*	mV_{peak}
Aperture Delay Time[3]		15	25		*	*	nsec
Aperture Uncertainty		±10	±25		*	*	psec
Sample Mode: Output Slew Rate		160			*		V/µsec
Full Power Bandwidth		1			*		MHz
Small Signal Bandwidth		16			*		MHz
Hold Mode Feedthrough Rejection							
(10V square wave input)	±0.03	±0.005		*	*		%
SAMPLE/HOLD OUTPUT							
Voltage Range	±10.25	±11		*	*		V
Output Current	±50			*			mA
Short Circuit Protection		Indefinite to Common			*		
Output Impedance (at DC)		0.01	0.1		*	*	Ω
INPUT BUFFER CHARACTERISTICS [SHC803 only]							
INPUT							
Offset Voltage		±1/2	±5		*	*	mV
vs Temperature		±1.5	±2.5		*	*	ppm of FSR/°C
Bias Current			±25			*	nA
Impedance		10^8‖5			*		Ω‖pF
V_{IN} Range	±10.25	±11		*	*		V
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth		320			*		kHz
Slew Rate[4]		10			*		V/µsec
Settling Time[4] to ±2mV for 10V Step		2.5			*		µsec
OUTPUT							
V_{OUT} Range	±10.25			*			V
Output Current	±10.25			*			mA

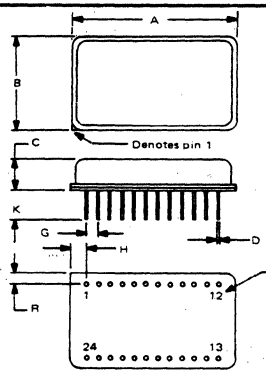
ELECTRICAL [CONT]

MODEL	SHC803/SHC804BM			SHC803/804CM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY REQUIREMENTS							
Rated Voltage: $\pm V_{CC}$	±13.5	±15	±16.5	*	*	*	V
V_{DD}	+4.75	+5.00	+5.25	*	*	*	V
Quiescent Current (no load)							
SHC804: $+V_{CC}$		30	35		*	*	mA
$-V_{CC}$		15	20		*	*	mA
V_{DD}		5	10		*	*	mA
SHC803: $+V_{CC}$		33	40		*	*	mA
$-V_{CC}$		18	25		*	*	mA
V_{DD}		5	10		*	*	mA
Power Dissipation: SHC804		700	875		*	*	mW
SHC803		790	1100		*	*	mW
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−55		+125	*		*	°C

*Specification same as SHC803/SHC804BM.

NOTES: (1) FSR means Full Scale Range and is 20V for SHC803 and SHC804. (2) Sensitivity of Offset plus Charge Offset. (3) With respect to $\overline{HOLD}$. For HOLD add 5nsec typical. (4) With buffer connected to the sample/hold amplifier.

MECHANICAL



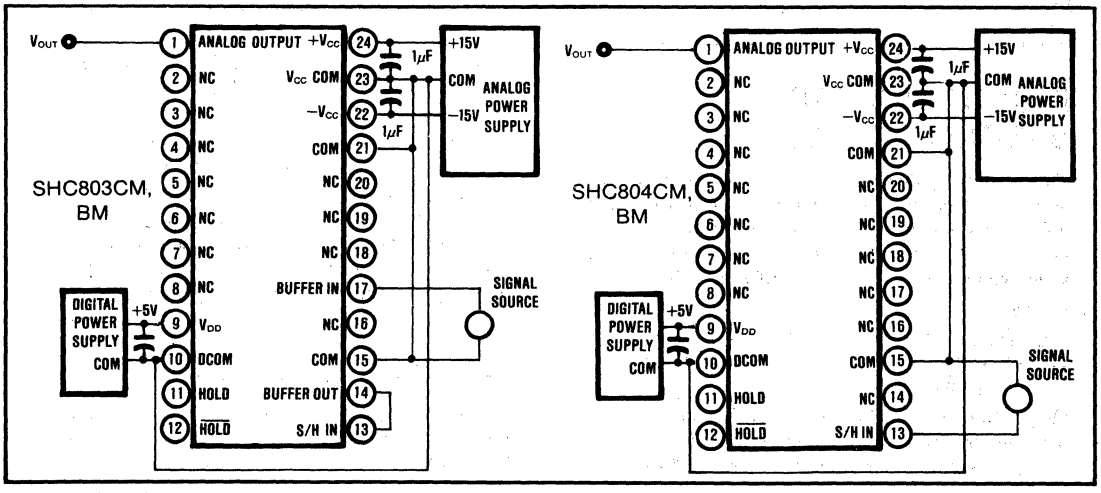
CASE: Nickel-plated steel
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3oz)
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of MIL-STD-883 (gross leak)

Pin numbers shown for reference only. Numbers may not be marked on package.

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Input Overvoltage ..... ±15V
$+V_{CC}$ to V_{CC} COMMON ..... 0 to +18V
$-V_{CC}$ to V_{CC} COMMON ..... 0 to −18V
Voltage on Digital Inputs
(pins 11 and 12) .....−0.5V to +7V
Power Dissipation 1500mW
V_{DD} to DCOM .....−0.5V
Analog Output .... Indefinite Short to V_{CC} COM

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN ASSIGNMENTS

Pin	Name	Description
1	Sample/Hold Output	Analog voltage output
2	NC	Not connected
3	NC	Not connected
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	V_{DD}	Logic supply
10	DCOM	Logic supply common
11	HOLD	Logic "1" = HOLD
12	$\overline{HOLD}$	Logic "0" = HOLD
13	S/H In	SHC804 input; for SHC803 connect pin 13 to pin 14
14	Buffer Out, SHC803 only	Not connected for SHC804
15	COM	Signal common
16	NC	Not connected
17	Buffer In, SHC803 only	Not connected for SHC804
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	COM	Signal Common
22	$-V_{CC}$	−15V supply
23	V_{CC} COM	Analog power common, connected to case
24	$+V_{CC}$	+15V supply

DISCUSSION OF SPECIFICATIONS

Throughput Nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

Gain Error is the difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

Feedthrough is the amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

Aperture Delay Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the Hold mode control transition to the time at which the output stops tracking the input.

Aperture Uncertainty Time is the nonrepeatibility of aperture delay time.

Acquisition Time is the time required for the sample/hold output to settle to within a given error band of its final value when the sample/hold is switched from Hold to Sample.

Charge Offset (Pedestal) is the output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.

Sample-to-Hold Switching Transient is the switching transient which appears on the output when the sample/hold is switched from Sample to Hold. Both the magnitude and the settling time of the transient are specified.

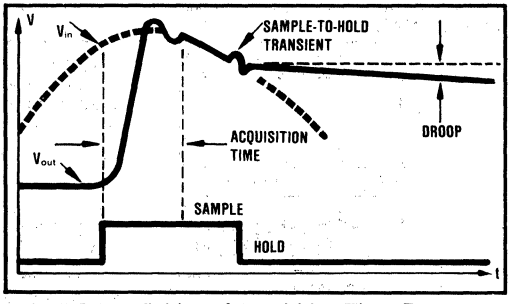


FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

OPERATION

A simplified circuit diagram of SHC803/804 is shown on page 1. The SHC803 includes a noninverting unity-gain op amp to serve as a source-impedance buffer when the sample/hold is used with CMOS analog multiplexers. The SHC804 and SHC803 are identical except for this buffer.

In the Sample (track) mode the circuit acts as a unity-gain inverting amplifier. In the Hold mode, the capacitor, C_H, holds the value of the output at the time the unit was switched to the Hold mode. Additional circuits compensate for switching transients and provide switch leakage current cancellation. The amplifier provides high current drive and low output impedance to external loads.

GAIN, OFFSET, CHARGE OFFSET

SHC803 and SHC804 have been internally-trimmed to eliminate the need for external trim potentiometers for Gain, Offset (in Sample mode) and Charge Offset (Pedestal). System Gain and Offset errors can be adjusted elsewhere in the system, at an input amplifier preceding the sample/hold, or at an analog-to-digital converter following the sample/hold.

INSTALLATION

GROUNDING AND BYPASSING

SHC803 and SHC804 have four COMMON pins (pins 10, 15, 21, and 23) and all must be tied together and connected to the system analog common ($V_{CC}COM$) as close to the package as possible. It is preferable to have a large ground plane surrounding the sample/hold and have all four common pins soldered directly to it. Note that the metal case is internally connected to pin 23; therefore, care must be taken to avoid a ground loop if the case is allowed to contact the ground plane.

Most digital return currents pass through pin 10. Noise from the switch-drive circuit may couple directly into the main op amp summing junction, a very noise-sensitive node. Care must be taken to insure that no voltage differences occur between pin 10 and the other common pins. This is the reason pin 10 must be connected directly to the ground plane.

For the same reason, the logic supply should be kept as free of noise as possible. $\pm V_{CC}$ supply lines (pins 24 and 22) are internally bypassed to common with 0.01μF capacitors. It is recommended that the user install additional external 0.1μF to 1μF tantalum bypass capacitors at each supply pin.

SAMPLE/HOLD CONTROL

A TTL logic "0" at pin 11 (or a logic "1" at pin 12) switches the SHC803/804 into the Sample (track) mode. In this mode, the device acts as a unity-gain inverting amplifier, the output following the inverse of the input. A logic "1" at pin 11 (or a logic "0" at pin 12) will switch the SHC803/804 into the Hold mode. The output voltages will be held constant at the value present when the Hold command is given.

If pin 11 is used, pin 12 must be connected to the DCOM (pin 10). If pin 12 is used, pin 11 must be tied to V_{DD}. Using the HOLD and $\overline{\text{HOLD}}$ inputs as a logic function may adversely affect the charge offset (pedestal). A clean digital signal (no overshoot) at the HOLD or $\overline{\text{HOLD}}$ inputs will also reduce charge offset errors. Pins 11 and 12 present less than one standard TTL load (two LSTTL loads) to the digital drive circuit.

OUTPUT LOADING

Care must be taken when loading the output of the SHC803/804 to avoid possible oscillations, current limiting and performance variations over temperature.

The maximum capacitive load to avoid oscillations is about 300pF. Recommended resistive load is 500Ω or more, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω in parallel with capacitive loads up to 100pF. Higher capacitances will affect acquisition and settling times.

ANALOG SIGNAL SOURCE CONSIDERATIONS

The output impedance of the signal source driving the SHC804 will affect the accuracy of the sample and hold operation both statically (at DC) and dynamically. The ouput impedance of the signal source should be low and remain low over a wide bandwidth. A small capacitor at the driving source may help to improve the charge offset errors that are affected by dynamic source impedance.

SHC803 BUFFER AMPLIFIER

The buffer amplifier incorporated in the SHC803 provides appropriate drive characteristics to the sample/hold amplifier. Again a 20pF to 50pF capacitor added to the output of the buffer amplifier may improve charge offset performance.

The buffer amplifier is optimized for fast settling with $10V_{p-p}$ signals. However, for step input signals greater than 10V, a protection network (Figure 2) is required to prevent the buffer from overload, resulting in excessive settling time.

The data sheet for the Burr-Brown model ADC803 analog-to-digital converter contains a sample printed circuit board layout incorporating many of the above considerations.

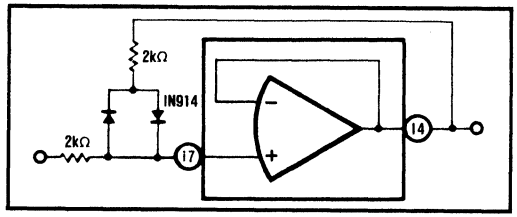


FIGURE 2. SHC803 Buffer Amplifier Protection For Input Steps Greater Than 10V.

APPLICATIONS

SIGNAL DIGITIZATION

Sample/hold amplifiers are commonly used to hold input voltages to an A/D converter constant during conversion. Digitizing errors result if the analog signal being digitized varies excessively during conversion.

For example, the Burr-Brown ADC803 is a 12-bit successive-approximation converter with a 1.5μsec conversion time. To insure the accuracy of the output data, the analog input signal to the A/D converter must not change more than 1/2LSB during the conversion.

The maximum rate of change for sine wave inputs is dv/dt (max) = $2\pi Af$(V/sec). If one allows a 1/2LSB change (2.44mV) for a ±10V input swing to the A/D converter, the allowable input rate-of-change limit would be 2.44mV/1.5μsec = 1.63mV/μsec. Thus the sampled sinusoidal signal frequency limit is

$$f = (1.63 \times 10^3)/2\pi A = 259/A(\text{Hz})$$

where A is the amplitude of the sine wave. For a ±10V sine wave this corresponds to a frequency of 26Hz.

A sample/hold in front of the A/D converter "freezes" the converter's input signal whenever it is necessary to make a conversion. The rate-of-change limitation calculated above no longer exists. If a sample/hold has acquired an input signal and is tracking it, the sample/hold can be commanded to hold at any instant. There is

a short delay between the time the hold command is asserted and the time the circuit actually holds. This delay is called aperture delay. The hold command signal can usually be advanced in time to cause the amplifier to hold when one wants it to hold.

The uncertainty in aperture delay, called aperture jitter, is a key consideration. For the SHC803/804 there is a 25psec maximum period during which the input signal should not change, for example, more than 1/2LSB for 12-bit systems. For a ±10V input range (1/2LSB = 2.44mV), the input signal rate of change limitation is 2.44mV/25psec = 97.6V/μsec. The equivalent input sine wave frequency is

$$f = 97.6 \times 10^6 / 2\pi A = 15.5/A(MHz),$$

60,000 times higher than using the A/D alone.

However, there are other considerations. The resampling rate of an ADC803 is 1.5μsec (A/D conversion time) + 0.3μsec (sample/hold acquisition time) = 1.8μsec. If one samples a sine wave at the Nyquist rate this permits sampling a frequency of 278kHz. The above analysis assumed that the droop rate of the sample/hold is negligible—less than 1/2LSB during the conversion time—and that the large signal bandwidth response of the sample/hold causes negligible waveform distortion.

USING THE SHC804 WITH THE ADC803

ADC803 is a 1.5μsec, 12-bit successive approximation A/D converter. Its input circuitry has been designed to minimize high frequency current transients that appear at the input of successive approximation A/D converters. The SHC803 and SHC804 have been designed with a fast-settling, low output-impedance amplifier to further minimize the effects of high frequency transient currents present in an output load.

A typical SHC804/ADC803 connection for high-speed digitization is illustrated in Figure 3. A short delay must occur before the A/D start command is asserted since the ADC803 makes its first conversion decision 100nsec after the start command is asserted. Because the SHC804 sample-to-hold settling time is 150nsec (maximum) the additional delay required is about 50nsec. This can be achieved using a one-shot or by using the delay provided by the six inverters of a hex inverter integrated circuit. This combination can be triggered at rates of over 500k samples per second.

Using the input buffer of the SHC803 provides a high input impedance sample/hold for CMOS analog multiplexers such as the high speed Burr-Brown MPC800. The high input impedance of the SHC803 buffer minimizes DC errors caused by the ON resistance of the multiplexer switches and/or relatively high impedance signal sources (Figure 4). The multiplexer can be switched to a new channel as soon as the SHC803 is switched to the Hold mode. The multiplexer/buffer combination settles to the new input value during the sample/hold acquisition time and A/D conversion time. This "overlap" technique results in little or no loss in throughput rate.

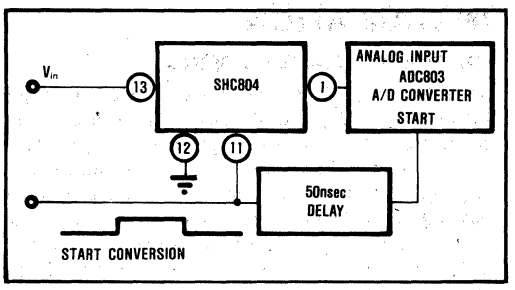


FIGURE 3. SHC804 and ADC803 Provide Sampling Rates Over 500k Samples Per Second.

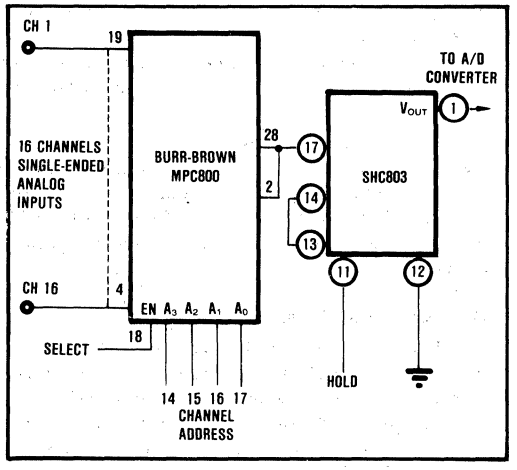
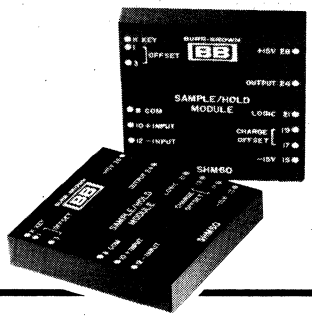


FIGURE 4. Using SHC803 With The MPC800 Analog Multiplexer.

BURR-BROWN®



SHM60

High Speed SAMPLE/HOLD

FEATURES

- 1μsec ACQUISITION
- .01% ACCURACY
- SELECTABLE GAINS - ±1 to ±1000
- 12nsec APERTURE TIME
- LOW FEEDTHROUGH - 0.005%

DESCRIPTION

Designed for use with fast A/D and D/A converters and analog multiplexers, the Burr-Brown Model SHM60 high-speed sample/hold acquires analog signals of up to ±10V amplitude and settles to 0.01% in less than 1.5μsec for a 20V input step, and in less than 1μsec for a 10V input step. Both analog input terminals are available for user selection of gains from unity to 1000.

Internal compensation of charge storage effects and dielectric absorption are provided to assure accurate and fast operation. The SHM60 dynamic nonlinearity of 0.01% is specified for hold periods of up to 15μsec to simplify the user's task of computing system throughput error for specific operating conditions.

The 2" x 2" x 0.4" encapsulated modular package operates from ±15VDC power and is compatible with Burr-Brown's line of fast A/D and D/A converters such as Models ADC85 and ADC80 and ADC84 A/D converters, and DAC85, DAC80 and DAC85 D/A converters.

A few of the more popular applications for the SHM60 are:

A/D converter aperture error reduction
Time correlation of sampled signals
i.e., simultaneous sample/hold
Multiplexing D/A converter outputs
Generation of pulse-amplitude-modulation (PAM) telemetry signals
Analog memory for analog computations

... and many more.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

Typical at 25°C and rated supplies unless otherwise noted.

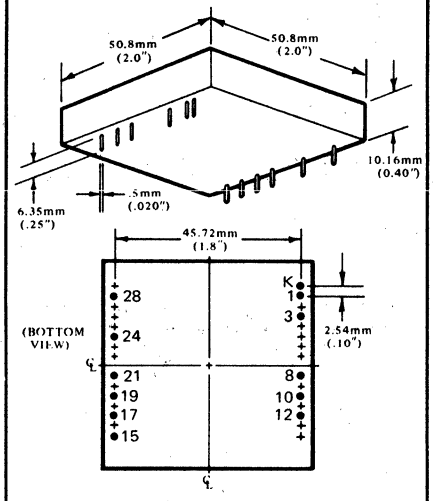
ELECTRICAL

MODEL	SHM60			
	Min	Typ	Max	Units
INPUT				
ANALOG INPUT				
Signal Voltage	-10		+10	V
Maximum Safe Input[1]	-15		+15	V
Impedance		10^{11}		Ω
Bias Current		50		pA
DIGITAL INPUT (Mode Control)[2]				
Sample Mode (Logic 1)				
at 100 μA Source	+2.4		+5.0	V
Hold Mode (Logic 0)				
at 50 nA Sink	0.0		+0.8	V
Rise Time for Specified Performance			5	nsec
INPUT POWER				
+15V Supply Voltage Range	+14.55	+15	+15.45	Vdc
-15V Supply Voltage Range	-14.55	-15	-15.45	Vdc
Quiescent Current				
+15V Supply - Sample Mode		25		mA
- Hold Mode		17		mA
-15V Supply - Sample Mode		15		mA
- Hold Mold		15		mA
TRANSFER CHARACTERISTICS				
ACCURACY at Gain of 1 V/V[3]				
Dynamic Nonlinearity[4]		±0.005	±0.01	% of 20V
Gain Error		±0.005	±0.01	% of 20V
Throughput Offset (Adj. to Zero)[5]		3		mV
Droop Rate		1	5	μV/μsec
Dielectric Absorption[4]		±0.005		% of ΔV
Noise		100		μV rms
Common Mode Rejection Ratio	10^{-4}			V/V
Power Supply Rejection		10	30	ppm/%
ACCURACY DRIFT (0°C to +70°C)				
Throughput Drift		±2		ppm of 20V/°C
Droop Rate		doubles every 10°C		
DYNAMIC CHARACTERISTICS				
Bandwidth (Full Power)		400		kHz
Output Slew Rate		25		V/μsec
Acquisition Time (to ±0.01%)				
10V Step		0.8	1	μsec
20V Step		1.2	1.5	μsec
Aperture Time		12		nsec
Sample-to-Hold Transient				
Peak Amplitude		50		mV
Settling to .01%			200	nsec
Feedthrough in Hold Mode			±0.005	% of Step Change at input
OUTPUT				
Voltage Range	±10			V
Current Range	±20			mA
Impedance (Short Circuit Protected)			1.0	Ω
TEMPERATURE				
Specification		0 to +70		°C
Storage		-55 to +125		°C

NOTES:

1. Input should never exceed supply by more than 0.6 volts.
2. Shottky TTL compatible.
3. Gain is user selectable.
4. For 1 μsec SAMPLE and 15 μsec HOLD times.
5. Includes voltage and charge offsets.

MECHANICAL

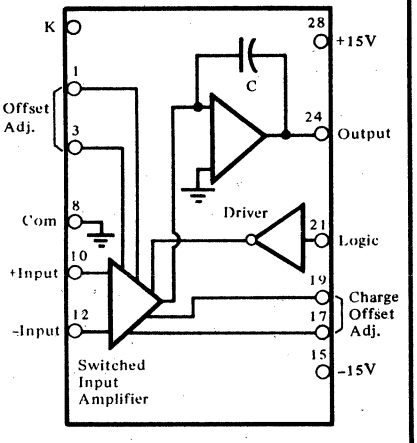


Dimensions in parentheses are in inches.

WEIGHT: 56.7 grams (2 oz)
MATING CONNECTORS:
2300 - P.C. Card and Terminals
2301 - Set of 2 - 16 Pin Connector Strips
PINS: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

CONNECTION DIAGRAM

(TOP VIEW)



DISCUSSION OF SPECIFICATIONS

ACCURACY

All SHM60 sample/hold units are tested for accuracy and are factory trimmed to assure that all units meet critical specifications.

DYNAMIC NONLINEARITY

This is the unadjustable throughput error from input to output for a 1 microsecond SAMPLE period and a 15 microsecond HOLD period. Errors included in this specification are throughput nonlinearity, dielectric absorption, droop, thermal transients and feedthrough. Offset errors must be adjusted to zero with an offset trim control and gain errors must be adjusted to zero with a gain trim control elsewhere in the system.

ACCURACY – UNITY GAIN OPERATION

The initial accuracy of the SHM60 is ±0.01% maximum of full scale range when operated as a unity gain voltage follower.

GAIN and OFFSET ERRORS - GAINS OTHER THAN UNITY

The SHM60 should be treated in the same manner as an operational amplifier when gains other than unity are employed. The gain setting resistor parameters such as absolute accuracy and tracking ratio must be considered when computing error effects for gains other than unity.

THROUGHPUT DRIFT

The input to output accuracy drift over a 0°C to +70°C temperature range is the throughput drift - it is ±2 ppm/°C or ±0.0002% of 20 volts.

THROUGHPUT OFFSET

The output offset voltage encountered in the HOLD mode after sampling a grounded input is throughput offset. This error includes charge offset at zero volts input as well as amplifier d.c. voltage offsets.

ACQUISITION TIME

The acquisition time of the SHM60 is defined as shown in Figure 1. This is the time required for the SHM60 to turn on, slew and settle to 0.01% of the input voltage when the mode is changed from HOLD to SAMPLE.

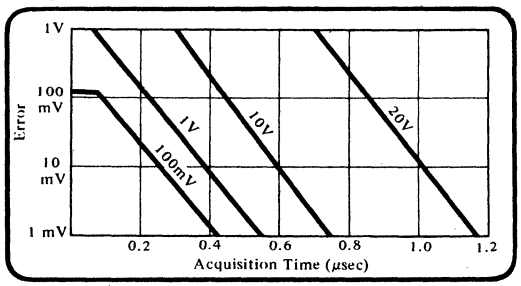


FIGURE 1. Error vs. Acquisition Time (Unity Gain Follower).

SAMPLE-TO-HOLD SWITCHING TRANSIENT

When the mode control is changed from SAMPLE -to-HOLD, the switching transient that appears on the output is the sample-to-hold switching transient.

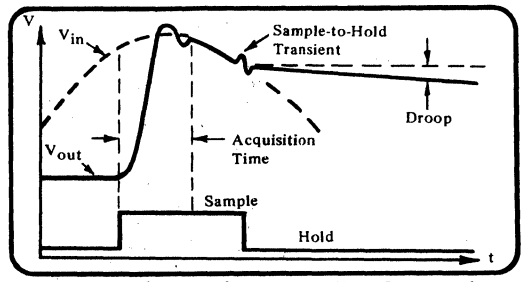


FIGURE 2. Definition of Acquisition Time Droop and Sample-to-Hold Transient.

DROOP RATE

Droop in a sample/hold is the voltage decay at the output due to output amplifier bias current when operating in the HOLD mode. To determine the effects of droop on system accuracy, the droop rate is multiplied by the HOLD period.

FEEDTHROUGH

The amount of input voltage change seen at the output when the sample/hold is in the HOLD mode is feedthrough error. The low feedthrough error of 0.005% preserves the accuracy of the sampled signal and can be used to increase the throughput sample rate, especially in time multiplexed applications.

APERTURE TIME

Aperture time is the delay between the time the sample/hold is given the command to HOLD the input signal and the time that this actually occurs. The SHM60 aperture time of 12 nanoseconds is sufficiently small to make aperture errors negligible for most applications.

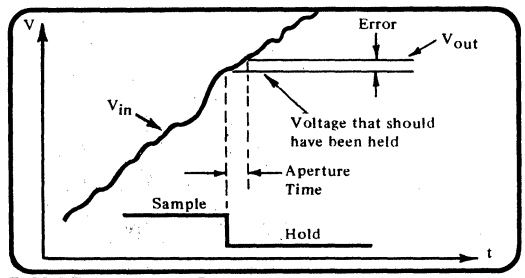


FIGURE 3. Aperture Error.

SYSTEM ERROR CONSIDERATIONS

The 1 μsec acquisition time and 12 nanoseconds aperture window of the SHM60 offer an excellent way of reducing system sampling error at high throughput rates for sinusoidal data. Taking the maximum slope of a sine wave at the zero crossing where maximum sampling error occurs, the error voltage as a percentage of full scale is proportional to the product of frequency and aperture time (Δt):

$$\% \text{ Aperture Error} = \frac{\Delta V}{V} \times 100 = 2\pi f \Delta t \times 100$$

where ΔV = Aperture error
V = Peak signal amplitude
f = Maximum signal frequency
Δt = Aperture time

INSTALLATION and OPERATING INSTRUCTIONS

OPTIONAL VOLTAGE and CHARGE OFFSET ADJUSTMENTS

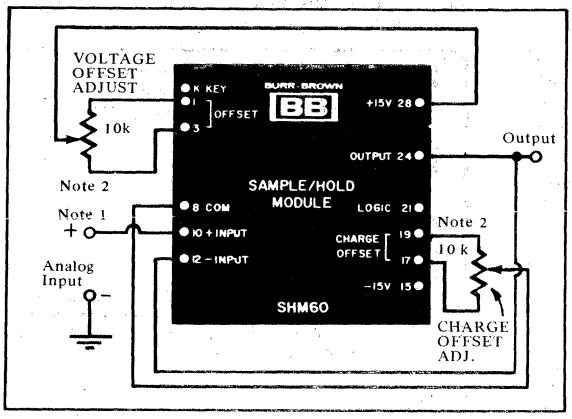


FIGURE 4. Optional CHARGE and VOLTAGE OFFSET Adjustment Connections.

Throughput OFFSET error may normally be adjusted to zero with a single external VOLTAGE OFFSET adjust control, as shown in Figure 4. A small CHARGE OFFSET error of 1 mV to 3 mV in the HOLD mode may occur. This CHARGE OFFSET error may also be adjusted to zero with an optional external CHARGE OFFSET adjustment as shown in Figure 4.

NOTES.

1. The analog input signal should not be run under or over the module as this may degrade feedthrough in the HOLD mode.
2. Potentiometers should have a TCR of 100 ppm/°C or less.

- Care must be taken to provide a good low impedance common as there is an appreciable amount of current returned to the power supplies.
- Power supply bypass capacitors are provided in the module, but additional bypassing may be required if excessive noise is present on the power supply lines.

CONNECTIONS FOR GAINS OTHER THAN UNITY

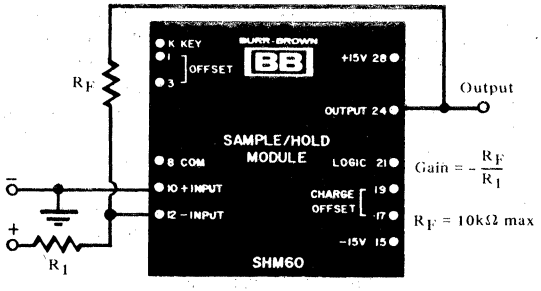


FIGURE 5. SHM60 Connections for Inverting GAIN.

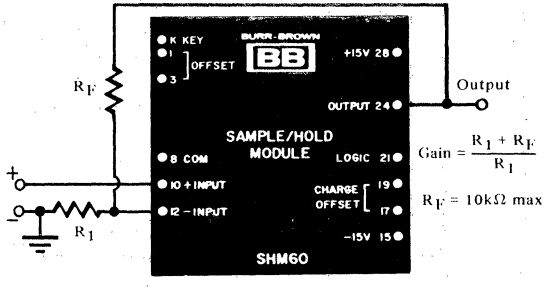


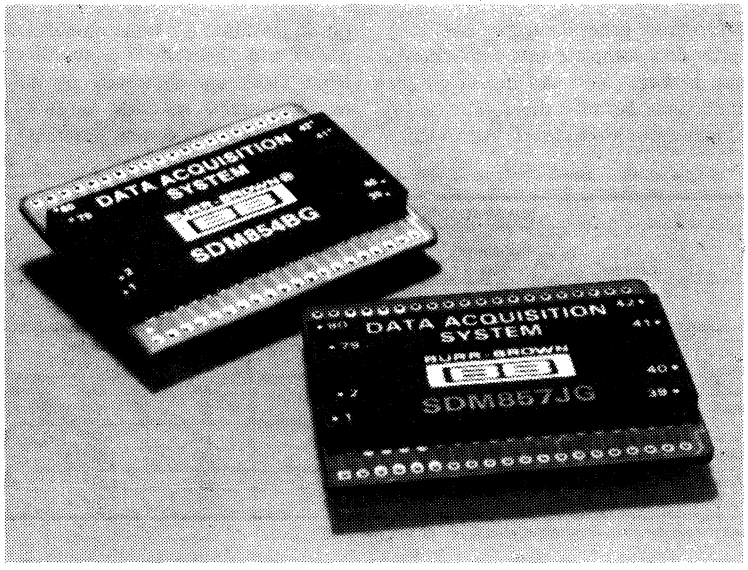
FIGURE 6. SHM 60 Connections for Non-Inverting GAIN.

Although optimum performance is at unity gain, the SHM60 may be operated to provide gains ranging from ±1 to ±1000 as shown in Figures 5 and 6. For these configurations, the unit may be treated as an operational amplifier. Acquisition time will get longer as gain increases, approximately 2.5 μsec settling to ±0.01% for a gain of 5 and 4 μsec for a gain of 10 for 10 volt output steps. Voltage drift can be computed as with an op amp using 10 μV/°C as the input drift.

NOTES:

- Gain accuracy and drift is dependent on the absolute accuracy and thermal tracking properties of the gain setting resistors R_1 and R_F. Metal film or better quality low drift resistors are recommended.
- Charge offset is independent of gain, and is referred to the output.

DATA ACQUISITION SUBSYSTEMS



8

If your system requires data acquisition and conversion, you may want to consider one of our system data modules (SDM) or microprocessor compatible modules (MP). Each contains a multiplexer, A/D converter, and timing and control logic, with instrumentation amplifiers and sample/hold circuits also available in some modules for use in capturing low-level and high-frequency signals. The microprocessor compatible modules (MPs) are SDMs which contain address decoding and specialized control logic, making them compatible with most available microprocessors. These subsystems, fully tested at the factory, have a proven record of reliability.

Modules of this type are very popular in applications requiring rapid design turn-around, and also where the user lacks the necessary skill and experience in performing fully optimized analog circuit layouts and component performance matching. Typical applications include industrial measurement and control (such as process monitoring), test equipment, and any other application requiring total guaranteed performance with a minimum of utilized space.

As with all Burr-Brown conversion products, these units are designed to provide a total solution.

SELECTION GUIDE

DATA ACQUISITION SYSTEMS

Designed for high performance general purpose applications, these systems provide a complete data acquisition function in one small package. You can devote your design efforts to other tasks because the totally self-contained system includes input multiplexer, instrumentation amplifier (in some models), sample-and-hold amplifier and 12-bit A/D converter. Timing and control logic, clock and reference are all internal. A host of features—even tri-state outputs for microprocessor buses—make this system practical, even in high volume buys.

DATA ACQUISITION SYSTEMS							
Description	Model	Channels	Resolution (Bits)	Throughput Accuracy (% of FSR)	Throughput Rate (kHz)	Package	Page
Modular	SDM853	16 single-ended, 8 differential	12	±0.025	30[1]	Module	8-59
Low Level	SDM858	16 single-ended, 8 differential	12	±0.025[2]	8[1]	Module	8-87
Hybrid ±10V Input	SDM854AG SDM854BG	16 single-ended, 8 differential	12 12	±0.048 ±0.024	40 29	QIP QIP	8-65 8-65
Hybrid	SDM856JG SDM856KG	16 single-ended, 8 differential	12 12	±0.048 ±0.024	33 25	QIP QIP	8-81 8-81
Hybrid Low Level	SDM857JG SDM857KG	16 single-ended, 8 differential	12 12	±0.048 ±0.024	25 18	QIP QIP	8-81 8-81

NOTES: (1) Can be increased if short-cycled to 8- or 10-bit resolution. (2) At gain = 100.

MICROPROCESSOR INTERFACED ANALOG INPUT AND OUTPUT SYSTEMS

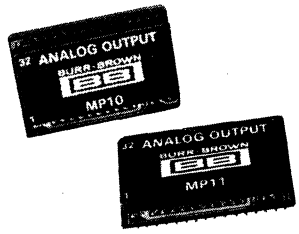
These data acquisition and analog data distribution systems are complete—totally interfaced to the microprocessor bus with no external interfacing components required. They provide an instant solution by preserving your valuable engineering design resources.

16-channel analog input systems and two-channel analog output systems talk directly to popular buses under control of the microprocessor. They are truly design-in-and-forget solutions to analog interface problems.

MICROPROCESSOR INTERFACED ANALOG INPUT SYSTEMS							
Description	Model	Channels	Resolution (Bits)	Accuracy (% of FSR) max	Tempco (ppm/°C) max	Package	Page
8080-, SC/MP-Compatible	MP20	16 single-ended, 8 differential	8	±0.8, high ±0.4, low	±40	QIP	8-11
6800-, 6502-Compatible	MP21	16 single-ended, 8 differential	8	±0.8, high ±0.4, low	±40	QIP	8-23
Universal	MP22BG	16 single-ended, 8 differential	12	±0.4, high ±0.1, low	±25[1]	QIP	8-35
High-Accuracy	MP32BG MP32CG	16 single-ended, 8 differential	12 12	±0.05 ±0.025	±60 ±60	QIP QIP	8-43 8-43
MICROPROCESSOR INTERFACED ANALOG OUTPUT SYSTEMS							
8080-, SC/MP-Compatible	MP10	2	8	±0.4	±80	Ceramic 32-pin DIP	8-3
6800-, 6502-Compatible	MP11	2	8	±0.4	±80	Ceramic 32-pin DIP	8-3

NOTES: (1) Unipolar, excluding IA.

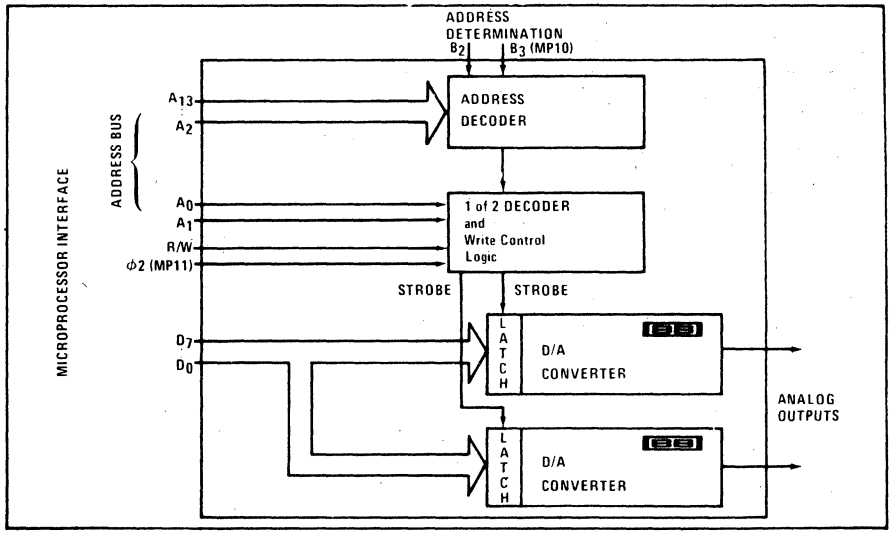
BURR-BROWN®



MP10
MP11

Microprocessor-Interfaced 8-BIT ANALOG OUTPUT SYSTEM

MP10, MP11 BLOCK DIAGRAM



FEATURES

- USE AS ANALOG INPUT AND OUTPUT
- EASY TO USE
  - Completely compatible with most microprocessors
  - No external logic required
  - Timing compatible
  - Memory-mapped
- SAVES DEVELOPMENT MONEY AND TIME
- COMPLETELY SELF-CONTAINED
- COMPATIBLE WITH:
  - 8080 (Intel)
  - 9080A (AMD)
  - Z-80 (Zilog)
  - 6800 (Motorola)
  - 8008 (Intel)
  - F-8 (Fairchild)
  - SC/MP (National)
  - 650X (MOS Technology)

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

These microprocessor peripherals provide an analog interface compatible with most microprocessors. The MP10 and MP11 are electrically and functionally microprocessor-compatible in static or dynamic situations.

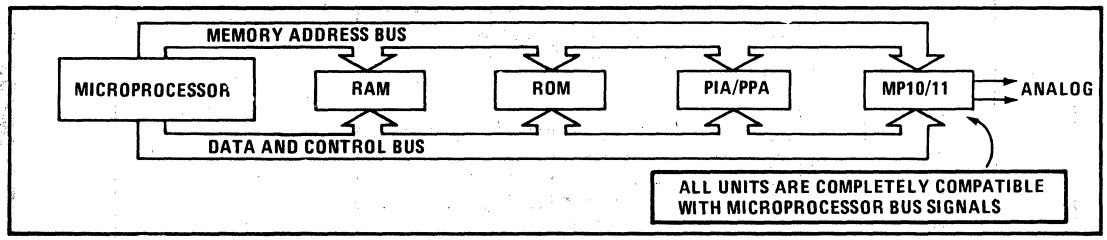
These units are complete analog systems packaged in 32-pin triple-wide dual-in-line packages. They contain two 8-bit D/A converters which are internally trimmed for gain and offset so that no external trimming is required. All necessary interface, timing and address decoding logic is also included.

The MP10 is designed to be used with 8080A and 8008 type microprocessors. It can be used with SC/MP if pull-up resistors are added to the address bus, with the F-8 Dynamic or Static memory interface chip if the RAM WRITE signal is a minimum of 430nsec and with the Z-80 if t_w (ϕH) = t_w (ϕL) = 500nsec. The MP11 is designed to be used with 6800 and 650X type microprocessors.

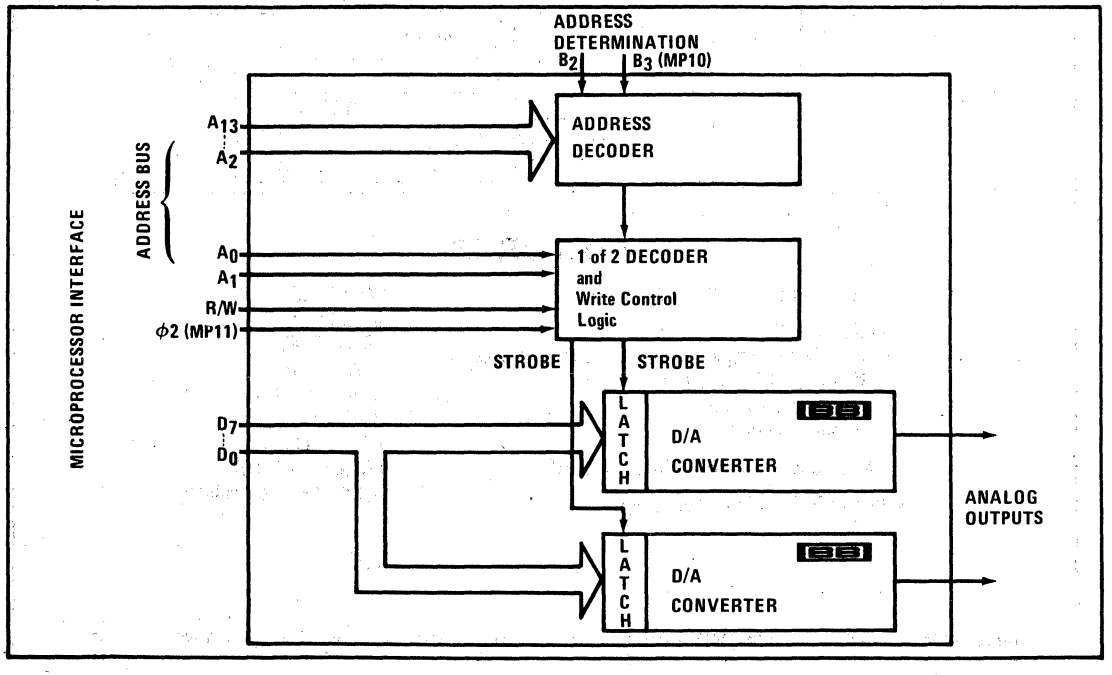
The address lines A_2 through A_{13}, B_2 and B_3 of the MP10 are CMOS compatible so that they can be directly connected to the address bus of an 8080 or 8008. All other input lines require standard TTL voltages. The address lines A_2 through A_{13} and B_2 of the MP11 are LSTTL compatible so they can be directly connected to the address bus of a 6800 or 650X. All other input lines require standard TTL voltages but are high impedance and require only microamp drive currents.

THEORY OF OPERATION

When programming these peripherals, the user treats them as memory. Because the D/A converter input is an 8 bit word, one 8 bit memory location is required for each channel. Since these units are treated as memory, a single instruction is all that's needed to write to an output channel. For instance, when the MP10 is used with an 8080, a single instruction, SHLD, can be used to output data to both D/A converter channels from the H and L register pair. Likewise, when the MP11 is used with the 6800 or 650X, a single STX instruction can be used to output data to both D/A converter channels from the index register. The MP10 and the MP11 require an initialization as would any programmable peripheral.



MP10, MP11 BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

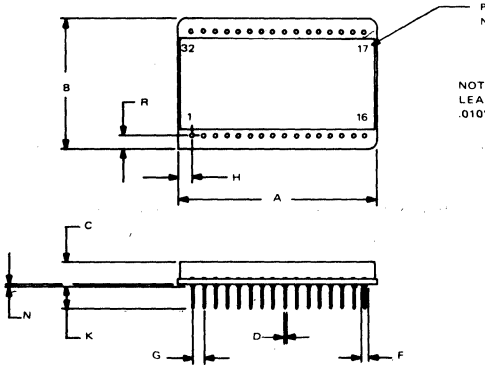
(Typical at 25°C and rated supplies unless otherwise noted.)

	MP10/MP11
ANALOG OUTPUT	
Number of analog outputs	2
Output voltage range	±10V
Output impedance	1Ω
Output settling time	25μsec
TRANSFER CHARACTERISTICS	
Resolution	8 bit binary (complementary binary)
One LSB	78.1mV
Throughput accuracy (max)	±0.4% FSR[1,2]
Throughput accuracy (typical)	±0.25% FSR
Temperature coefficient of accuracy	±0.008% FSR/°C

	MP10/MP11
DIGITAL INPUT/OUTPUT	
All signals compatible with the microprocessor bus	
An analog output channel selected by:	A0
Input data bits read by:	D0 - D7
POWER REQUIREMENTS	
	+5VDC ±5% at 90 mA
	+15V ±3% at 30 mA
	-15V ±3% at 30 mA
TEMPERATURE RANGE	
Operating temperature range	0°C to 70°C
Storage temperature range	-55°C to +85°C

1. FSR is Full Scale Range = 20V.
2. Accuracy components are: Linearity Error = ±0.2% FSR; Gain Error = ±0.1% FSR, Offset Error = ±0.1% FSR.

MECHANICAL SPECIFICATIONS



NOTE:
LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

MATERIAL: Ceramic
WEIGHT: 14 grams (0.5 oz)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATING CONNECTOR: 2302MC (Set of two, 16-pin strips)

MP10/11

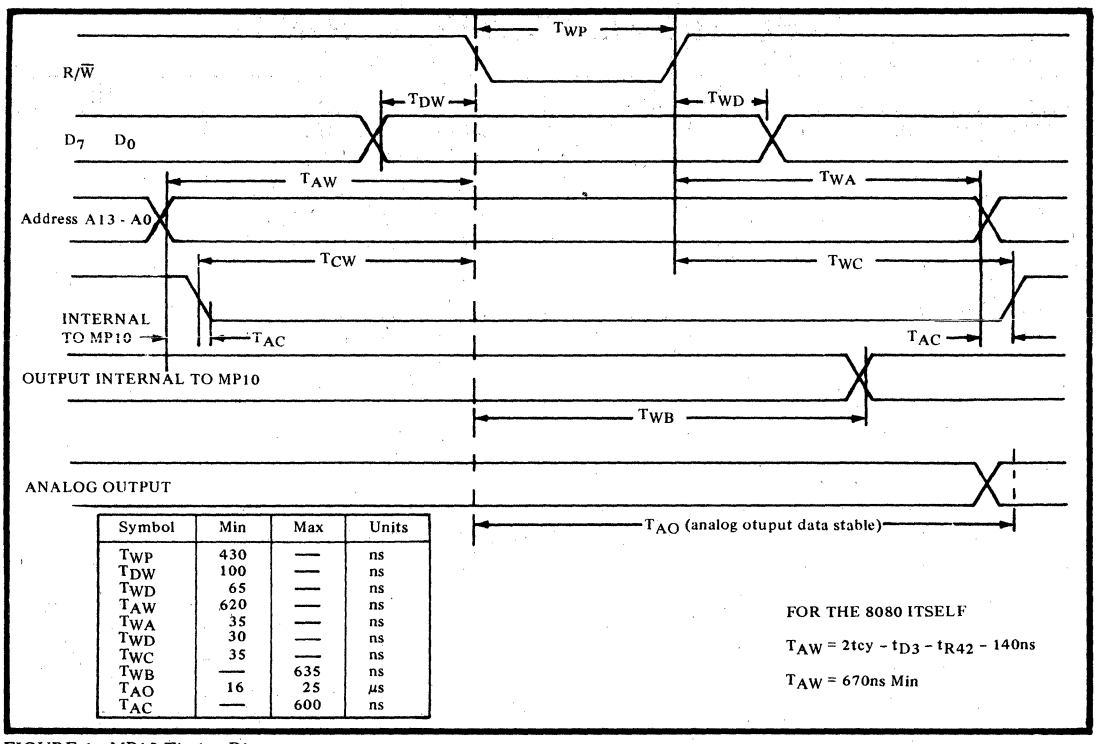
PIN CONNECTIONS

8080 Pin Connections					8080 Pin Connections
1	1	A10	A11	32	40
2	2	Common	A13	31	38
3	3	D4	A12	30	37
4	4	D5	A 9	29	35
5	5	D6	A 8	28	34
6	6	D7	A 7	27	33
7	7	D3	A 6	26	32
8	8	D2	A 5	25	31
9	9	D1	A 4	24	30
10	10	D0	A 3	23	29
12	11	Reset	A 2	22	27
18	12	R/$\overline{W}$	B 2	21	—
26	13	A1	B 3	20	—
25	14	A0	+5V	19	20
—	15	+15VDC	Out 1	18	—
—	16	-15VDC	Out 2	17	—

MP10

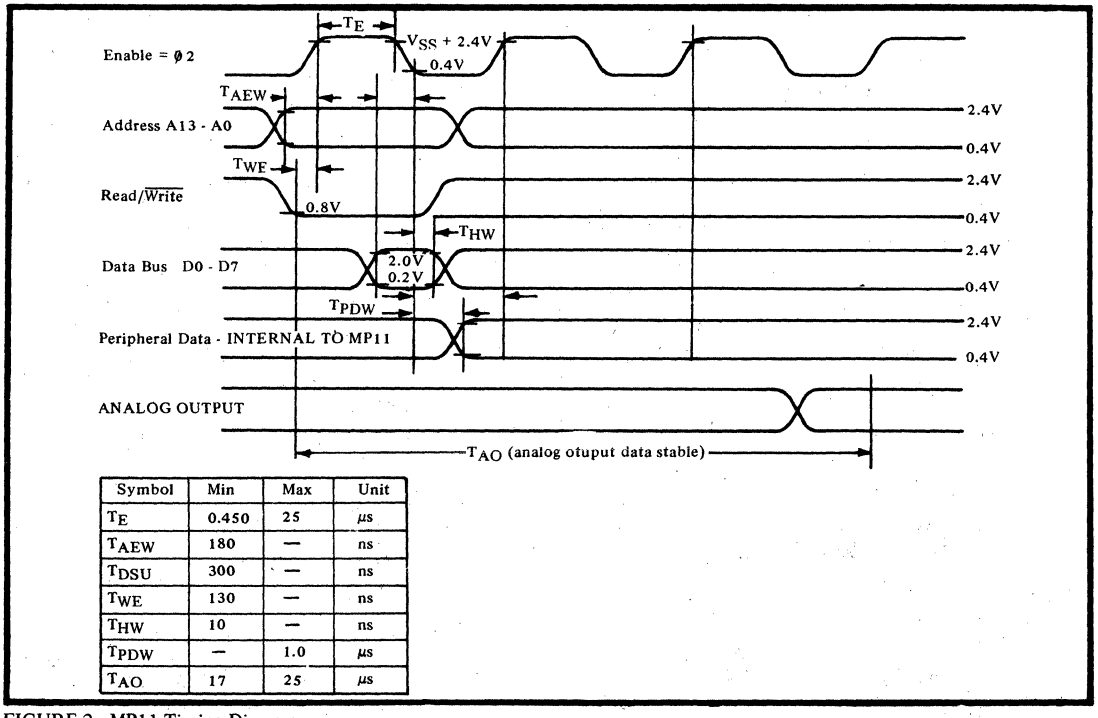
6800 Pin Connections					6800 Pin Connections
—	1	Output 1	-15VDC	32	—
—	2	Output 2	+15VDC	31	—
8	3	+5VDC	R/$\overline{W}$	30	34
37	4	Enable	$\overline{Reset}$	29	40
9	5	A0	D0	28	33
10	6	A1	D1	27	32
11	7	A2	D2	26	31
12	8	A3	D3	25	30
13	9	A4	D4	24	29
14	10	A5	D5	23	28
15	11	A6	D6	22	27
16	12	A7	D7	21	26
17	13	A8	Common	20	21
18	14	A9	B2	19	—
19	15	A10	A13	18	23
20	16	A11	A12	17	22

MP11



Symbol	Min	Max	Units
T_{WP}	430	—	ns
T_{DW}	100	—	ns
T_{WD}	65	—	ns
T_{AW}	620	—	ns
T_{WA}	35	—	ns
T_{WD}	30	—	ns
T_{WC}	35	—	ns
T_{WB}	—	635	ns
T_{AO}	16	25	μs
T_{AC}	—	600	ns

FIGURE 1. MP10 Timing Diagram.



Symbol	Min	Max	Unit
T_E	0.450	25	μs
T_{AEW}	180	—	ns
T_{DSU}	300	—	ns
T_{WE}	130	—	ns
T_{HW}	10	—	ns
T_{PDW}	—	1.0	μs
T_{AO}	17	25	μs

FIGURE 2. MP11 Timing Diagram.

PROGRAMMING

These units are easily programmed since all are treated as memory locations. They use any memory reference instruction that can write data from internal registers or the accumulator. A single instruction can be used to write data to one or both channels. When the MP10 is used with an 8080, a single SHLD instruction referenced to the lower of the two addresses will automatically transfer the data in the H register to DAC1 and the data in the L register to DAC2. An STA instruction will transfer the data in the accumulator to either DAC. When the MP11 is used with a 6800, a single STX instruction referenced to the lower of the two addresses will automatically transfer the eight upper bits of the index register to DAC1 and the eight lower bits to DAC2. An STAA instruction will transfer the contents of the accumulator to either DAC. Of course, if direct addressing is not desired, MOV instructions may be used to transfer data from internal registers to a specific DAC memory location. As with any programmable peripheral, the MP10 and MP11 must be initialized.

MP10 INITIALIZATION

The RESET input controls the status of the control register of the MP10. An active high on this line will reset the control register to all "zeros".

The MP10 will require initialization every time RESET is activated. If RESET is connected to ground, the MP10 must be initialized only once before output of the data.

MP10 INITIALIZATION SEQUENCE:

1. Load initialization address
2. Load initialization data

MP10 INITIALIZATION ADDRESS:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X	X	1	1	1	1	1	1	1	1	1	1	a	a	1	1
												User Defined			

X = don't care, not connected to MP10
1 = True

MP10 INITIALIZATION DATA

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	0	0	0	0	0	0	0	$= 80_{16}$

For 8080 the sequence may look as follows:

LXI H, ADDR; ADDR = Initialization address
Loads H & L registers with initialization address

MVI M, DATA; DATA = 80
Loads initialization data (80_{16}) to initialization address

The initialization sequence assigns internal registers to function as input registers for the D/A converters. Now data can be written into the MP10. This is accomplished by outputting the correct MP10 address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	1	1	1	1	1	1	1	1	1	a	a	0	0	OUTPUT 1
												User Defined				
1	1	1	1	1	1	1	1	1	1	1	1	a	a	0	1	OUTPUT 2
												User Defined				

The B_2 and B_3 inputs determine the address to which the MP10 will respond. The four memory locations which are possible are outlined below:

B_2	B_3	A_2	A_3
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

At the time that the address appears on the address bus, data will appear on the data bus and a R/$\overline{W}$ pulse will be generated by the microprocessor. After 25μsec, the analog voltage will be stable at the selected output. Timing requirements shown in Figure 1 must be satisfied in order for the MP10 to be initialized and operate correctly. These timing requirements are completely compatible with the 8080.

MP11 INITIALIZATION

The $\overline{\text{RESET}}$ input controls the status of the control and peripheral registers of the MP11. The initialization sequence will differ if $\overline{\text{RESET}}$ is connected to a master reset line of a microprocessor or if it is hard-wired to V_{cc}. The MP11 will require initialization every time the $\overline{\text{RESET}}$ line is activated low. If the $\overline{\text{RESET}}$ line is hard wired to V_{cc}, the MP11 must be initialized only once before output of the data is attempted.

MP11 ADDRESS STRUCTURE

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X	X	1	1	1	1	1	1	1	1	1	1	0	a	Y	Y

A_{15}, A_{14} - don't care, not connected to MP11
A_2 - Address is user selectable
A_0, A_1 - Addresses control the initialization sequence

Initialization sequence when $\overline{\text{RESET}}$ is hard wired to V_{cc}:

1. Load accumulator with "zeros"
2. Store accumulator at memory locations:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	0	Address of Control register A
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	1	Address of Control register B

3. Load accumulator with "ones"
4. Store accumulator at memory locations:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	0	Address of Peripheral register A
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	1	Address of Peripheral register B
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	0	Address of Control register A
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	1	Address of Control register B

For the 6800 this sequence can be written as follows:

	LDAA	"zeros"	Loads Zeros in accumulator
	STAA	Address of control register A	Stores zero's in C.R.A.
	STAA	Address of control register B	Stores zero's in C.R. B
	LDAA	"ones"	Loads one's in accumulator
	STAA	Address of peripheral register A	Stores one's in P.R.A
	STAA	Address of peripheral register B	Stores one's in P.R.B.
	STAA	Address of control register A	Stores one's in C.R.A
	STAA	Address of control register B	Stores one's in C.R.B
Or as:	LDX	# $0000	Loads zero's in index register
	STX	$ Address control register A	Stores zero's in C.R. A and B
	LDX	# $1111	Loads one's in index register
	STX	$ Address peripheral register A	Stores one's in P.R. A and B
	STX	$ Address control register A	Stores one's in C.R. A and B

Initialization sequence when $\overline{\text{RESET}}$ line is connected to master reset (control registers A and B are always set to zero after master reset and only ones need to be stored in the registers):

LDAA	"ones"
STAA	Address Peripheral register A
STAA	Address Peripheral register B
STAA	Address Control register A
STAA	Address Control register B

or as:

LDXX	# $1111
STX	$ Address Peripheral register A
STX	$ Address Control register A

Now data can be written into MP11. This is accomplished by outputting the correct MP11 address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	0	OUTPUT 1
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	1	OUTPUT 2

At the time that the address appears on the address bus, data will appear on the data bus, and if the R/W and Enable pulses are correctly timed, 25μsec from the true address the analog voltage will be stable at the selected output.

Timing requirements shown in Figure 1 must be satisfied for the MP11 to be initialized and operate correctly. All timing requirements are completely compatible with 6800 microprocessors. User definable address line A_2 used in conjunction with the B_2 input allows the user to place the MP11 in two different memory locations or use two different MP11's in order to expand the analog system to four outputs. When B_2 is wired to logical 1, the MP11 responds to an A_2 address of 0 and when B_2 is wired to a logical 0, the MP11 responds to an A_2 address of 1.

TEST PROGRAMS

The test circuit and test programs following allow the user to test the operation of the MP10 or MP11. The test may be conducted by setting up the MP10/MP11 as shown in Figure 3. The microprocessor system should have a teletype/CRT terminal interface. The programs will step through several output voltage levels for each DAC output (see Figure 4). Notice how the software is different for the two test programs to illustrate two software approaches.

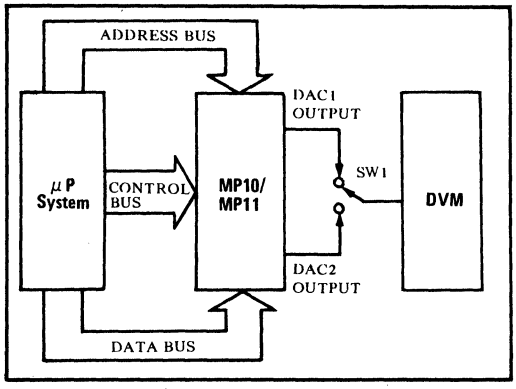


FIGURE 3. Test Circuit for MP10/MP11.

MP10 Test Program

```
                    Initialize MP10
        LXI H ADDR X    Address of the first
                        byte of data.
LOOP 1  MOV A, M        Load ACC with first byte
                        of data.
        STA ADDR2       Output to MP10 DAC1
        INX H           Increment ADDR1
        CALL CI         Call Input routine
        CPI             Wait for any character
        8D              except carriage return
        JNZ LOOP1
        LXI ADDR X
LOOP 2  MOV A, M
        STA ADDR3       Output to MP10 DAC2
        INX H           Increment ADDR1
        CALL CI
        CPI             Wait for any character
        8D              except carriage return
        JNZ LOOP2
        RET
```

The MP10 test program will output five different voltages from DAC1 and then from DAC2 (see Figure 4). DAC1 will initially output -10V. To step through the other values for DAC1 enter any character other than carriage return (CR). To transfer control to DAC2, enter CR. DAC2 will output -10V. To step through the other values for DAC2 enter any character except CR. To exit the test program, enter CR.

Store the following codes in memory beginning with location ADDR X:

ADDR X ← FF
ADDR X + 1 ← BF
ADDR X + 2 ← 7F
ADDR X + 3 ← 3F
ADDR X + 4 ← 00

ADDR 2 is the address of output 1, ADDR 3 is the address of output 2:

MP11 Test Program

```
                        Initialize MP11
        LDX  # $ FFFF;  Load index register
        STX  ADDR 1;    Store FF in each DAC
        JSR  INP
        LDX  # $ BFBF;  Load index register
        STX  ADDR 1;    Store BF in each DAC
        JSR  INP
        LDX  # $ 7F7F;  Load index register
        STX  ADDR 1;    Store 7F in each DAC
        JSR  INP
        LDX  # $ 3F3F;  Load index register
        STX  ADDR 1;    Store 3F in each DAC
        JSR  INP
        LDX  # $ 0000;  Load index register
        STX  ADDR 1;    Store 00 in each DAC
        JSR  INP
INP     LDAA ADDR X     Load Status of ACIA   } Wait for TTY input
        Bit A  #01
        BEQ  INP
        LDA A ADDR X + 1 Load Data From ACIA  } Jump back to test program or return to main program
        CMP  A
        8D
        BNE  Back
        JMP  Return
BACK RTS
```

The MP11 test program will output -10V from both DAC1 and DAC2 then wait for an input from the TTY. Any character except CR will advance both DAC's of the MP11 to the next value as defined in Figure 4. CR terminates test program by jumping to RETURN.

ADDR 1 is the address of output 1, ADDR X is the address of the ACIA.

Step	Ideal Output	Actual Output Limits
1	-10V	-9.922V to -10.078V
2	-5.0V	-4.922 to -5.078
3	0.000V	-0.078 to +0.078
4	+5.0V	+4.972 to +5.078
5	+9.922V	+9.844 to +10.000

FIGURE 4. Output Voltages for Test Programs.

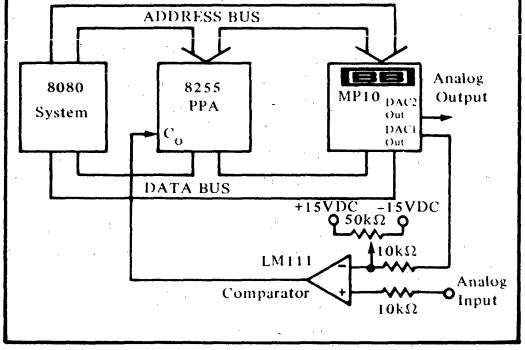
APPLICATIONS

ANALOG INPUT AND ANALOG OUTPUT

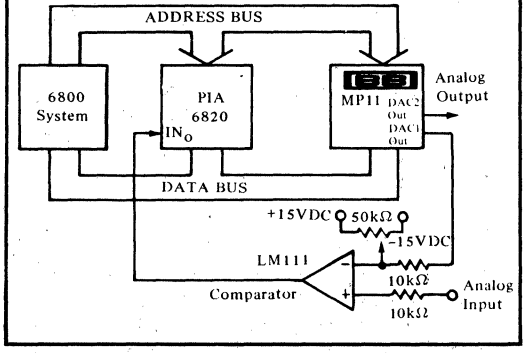
Although the MP10 and MP11 are analog output peripherals, they can be easily adapted to provide both analog inputs and outputs.

With the addition of a few external components, these units can each provide one analog input and one analog output for your system as shown below:

MP10 ANALOG INPUT/OUTPUT



MP11 ANALOG INPUT/OUTPUT



These systems use the microcomputer system to perform the logic of a successive approximation A/D converter, using one channel of the MP10 or MP11 to provide the D/A converter reference function required. In a successive approximation converter, the analog input is compared to known outputs of a D/A converter. First, the microcomputer turns the MSB on, waits for the settling time of the MP10 or MP11, and the switching time of the comparator, then reads the status. If the comparator indicates that the MSB voltage is smaller than the analog input, the MSB input to the MP10/MP11 stays "on" and the next most significant bit is turned on. If the comparator indicates that the MSB value is larger than the analog input, the microcomputer will turn the MSB "off" and turn "on" the next most significant bit. In this way all 8 bits of the D/A converter are tested. When the conversion is complete, the input of the D/A converter will be a digital representation of the analog input. This value will also be stored in the microprocessor's accumulator (complementary binary).

The A/D conversion will require approximately 900 microseconds when performed in this manner. Burr-Brown will shortly have available a detailed application note describing this process including all software required.

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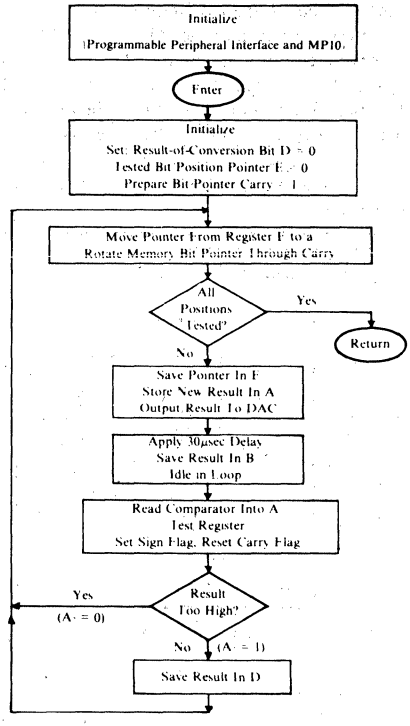
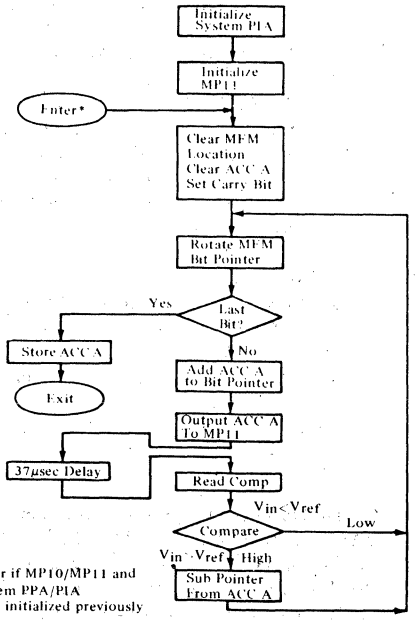
FLOWCHART USING 8080 and MP10



FLOWCHART USING 6800 and MP11



* Enter if MP10/MP11 and system PPA/PIA were initialized previously

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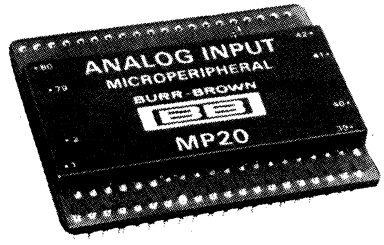


MP20

8-BIT MICROPROCESSOR-INTERFACED DATA ACQUISITION SYSTEM

FEATURES

COMPATIBLE WITH:
- 8080A
- 8085
- 8008
- 8048
- Z-80
- SC/MP

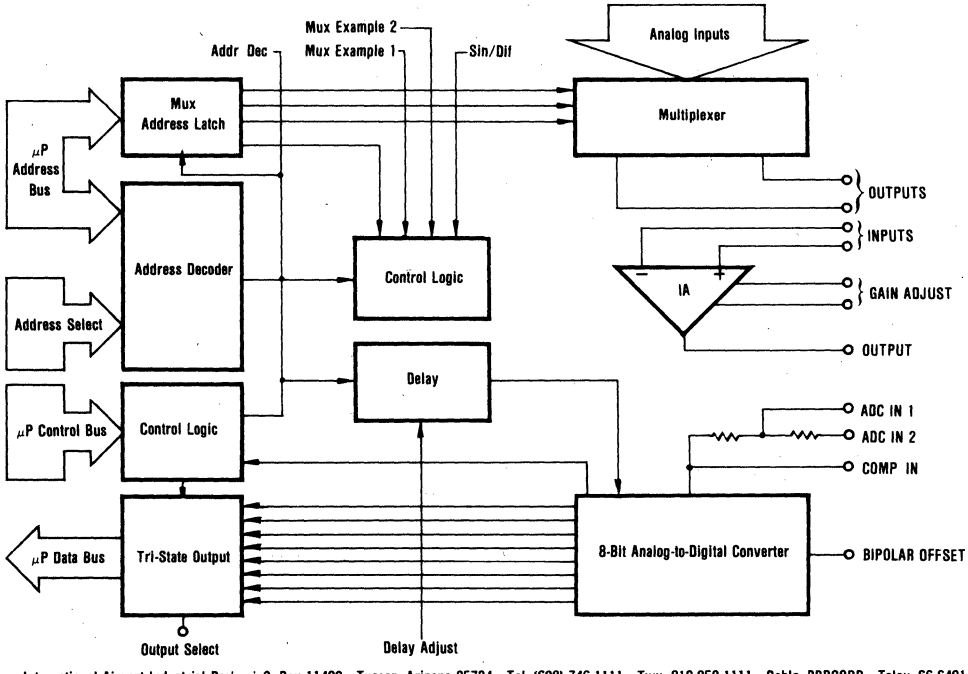
EASY TO PROGRAM
- Choice of ways to interface:
  - Memory-mapped or I/O mapped
  - Only one instruction to acquire data

EASY TO USE
- Completely compatible with 8080A microprocessors
- PPA is not needed
- No external logic needed
- No external adjustments
- Low or high level analog inputs
- Unlimited expansion

COMPLETELY SELF-CONTAINED

LOW COST

SAVES DEVELOPMENT TIME AND MONEY



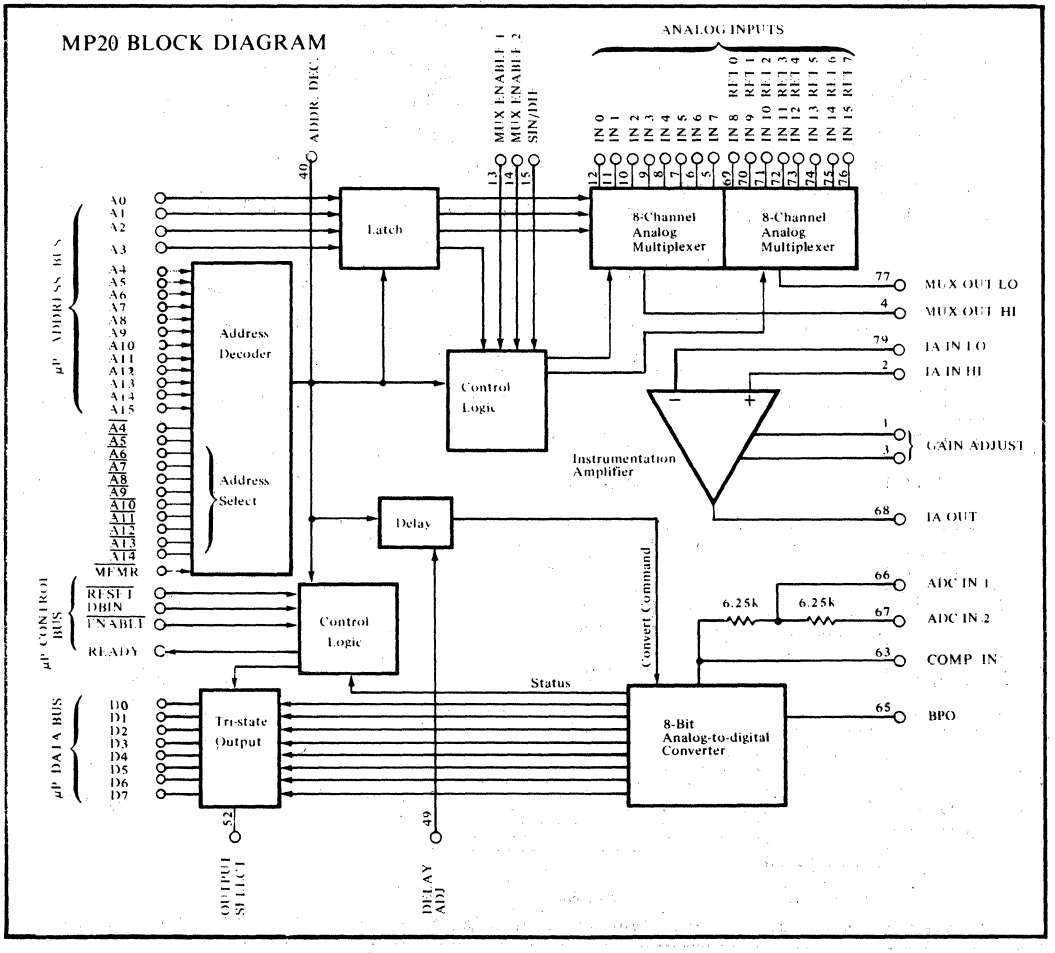
International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

The MP20 is a complete analog input system packaged in an 80-pin quad-in-line package. It is completely compatible with 8080A and 8008 microprocessors. It is also compatible with SC MP and with the Z-80. The MP20 contains a high speed 8-bit A D converter, an instrumentation amplifier, an input multiplexer that can accept up to 16 single-ended signals or 8 differential signals as well as interface, timing and address decoding logic. The gain and offset are internally laser trimmed so that no external adjustments are required on the ±5V or 0 to +5V input range to obtain an absolute accuracy of better than ±0.4% (1LSB). The system can digitize low level or high level analog signals. The gain of the internal instrumentation amplifier can be programmed with a single external resistor to allow input signal ranges as low as ±10mV. This means that the MP20 can be connected to low level sensors such as thermocouples and strain gauges without external signal amplification.

The address lines A0 through A15 are low power Schottky TTL compatible and can be connected directly to the address bus of an 8080A or 8008. All digital input lines require standard LSTTL voltages.

When programming these peripherals, the user treats them as memory. Each analog input channel occupies one memory location. Any memory reference instruction can be used. Since most microprocessors have been optimized for memory usage, memory reference instructions are the most powerful instructions in a microprocessor's repertoire. The MP20 is treated as memory to simplify software and allow an almost unlimited number of systems to be connected to a single processor. Pins $\overline{A4}$ to $\overline{A14}$ are made available so that the microperipheral address can be hardwired for almost any possible memory location. Since these units are treated as memory, a single instruction is all that's needed to read an input channel. For instance, when the MP20 is used with an 8080A, a single instruction, LHLD, can be used to input data to the H and L registers from two consecutive analog inputs. Likewise, a single LDA or MOV instruction will input data from one channel to the CPU.



SPECIFICATIONS

ELECTRICAL

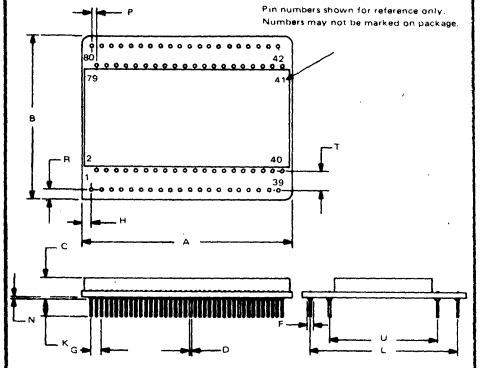
Typical at 25°C unless otherwise noted.

TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
Number of channels	16 single-ended/8 differential
Throughput rate(1), max	40μsec/channel
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	2 to 250
Amplifier gain equation	$G = 2 + (50k\Omega/R_{EXT})$ (2)
Max input voltage without damage(3)	±20V
Max input voltage for multiplexer operation	±6V
Input impedance	$5 \times 10^9\Omega$ || 10pF - OFF channel $5 \times 10^9\Omega$ || 100pF - ON channel
Bias current 25°C	100nA
Bias current 0°C to 70°C	200nA
Amplifier output noise Gain = 100, $R_S = 500\Omega$	400μV, rms (10Hz to 10kHz
Amplifier input offset voltage, max	±1mV
Amplifier offset voltage drift	±(6 + (50/G)) μV/°C
Amplifier settling time (to 0.1% FSR	
G = 2	20μsec
G = 10	25μsec
G = 50	50μsec
G = 100	100μsec
G = 200	200μsec
CMRR (for differential inputs G = 2	70dB DC to 60Hz
ACCURACY	
Throughput accuracy ±5V range, max(4)	±0.4% of FSR(5)
0 to 5V range, max(4)	±0.4% of FSR
±50mV range, max(6)	±0.8% of FSR
0 to 50mV range, max(6)	±0.8% of FSR
Linearity, max(4)	±0.2% of FSR
Differential linearity(4)	±0.2% of FSR
Quantizing error	±1/2LSB
Gain error(4)	±0.1%
Offset error(4)	±0.1% of FSR
Power supply sensitivity ±15V	$\pm 0.02\%/\%\Delta V_{CC}$
+5V	$\pm 0.002\%/\%\Delta V_{CC}$
STABILITY OVER TEMPERATURE	
System accuracy drift(7), max	±40ppm/°C
Linearity, max	±20ppm/°C
Monotonicity (0°C to +70°C)	Guaranteed
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microprocess bus	
Output coding	Binary or Binary two's complement
Logic loading	All digital inputs are one LSTTL load
Output drive (D0 - D7)	5 TTL loads or 20 LSTTL loads
An analog input channel is selected by:	A0 - A3
The output data bits are read into:	D0 - D7
POWER REQUIREMENTS	
Rated voltages	±15V, +5V
Range for rated accuracy	4.75V to 5.25V and ±14.5V to ±15.5V
Supply drain ±15V	±30mA
Supply drain +5V	+90mA
TEMPERATURE RANGE	0°C to +70°C

NOTES:
1. Includes 35μsec for mux and amplifier settling time and 5μsec for ADC conversion time.
2. R_{EXT} is the resistance between pins 1 and 3.
3. With power applied.
4. Gain = 2, with no external adjustments.
5. FSR is Full Scale Range (FSR is 10V for ±5V range).
6. Gain = 100, with external gain and offset trim.
7. Includes gain drift, offset drift and linearity drift.

MECHANICAL

NOTE:
LEADS IN TRUE POSITION WITHIN .015" (.38mm)R @ MMC AT SEATING PLANE.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	

MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz
PINS: Pin material and plating composition conform to method 2003 solderability of MIL-STD-883 except paragraph 3.2
MATING CONNECTOR: 2350MC (set of four 20-pin strips

PIN CONNECTIONS

Pin		Pin	
1	IA GAIN ADJUST	41	$\overline{A14}$
2	IA IN HI	42	$\overline{A14}$
3	IA GAIN ADJUST	43	A15
4	MUX OUT HI	44	$\overline{MEMR}$
5	IN 7	45	$\overline{DBIN}$
6	IN 6	46	$\overline{ENABLE}$
7	IN 5	47	$\overline{RESET}$
8	IN 4	48	READY
9	IN 3	49	DELAY ADJ
10	IN 2	50	+5V
11	IN 1	51	DIG COM
12	IN 0	52	OUTPUT SELECT
13	MUX ENABLE 1	53	D7 (MSB)
14	MUX ENABLE 2	54	D6
15	SIN DIP	55	D5
16	A0	56	D4
17	A1	57	D3
18	A2	58	D2
19	A3	59	D1
20	A4	60	D0 (LSB)
21	$\overline{A4}$	61	-15V
22	A5	62	+15V
23	$\overline{A5}$	63	COMP IN
24	A6	64	ANA COM
25	$\overline{A6}$	65	BPO
26	A7	66	R2
27	$\overline{A7}$	67	R1
28	A8	68	IA OUT
29	$\overline{A8}$	69	IN 8 REF 0
30	A9	70	IN 9 REF 1
31	$\overline{A9}$	71	IN 10 REF 2
32	A10	72	IN 11 REF 3
33	$\overline{A10}$	73	IN 12 REF 4
34	A11	74	IN 13 REF 5
35	$\overline{A11}$	75	IN 14 REF 6
36	A12	76	IN 15 REF 7
37	$\overline{A12}$	77	MUX OUT LO
38	A13	78	OFFSET NULL
39	$\overline{A13}$	79	IA IN LO
40	ADDR DECODE OUT	80	OFFSET NULL

PIN FUNCTIONS

IA GAIN ADJUST (Optional). Pin 1 and Pin 3. By connecting a resistor between pin 1 and 3 the gain of the internal instrumentation amplifier can be varied as follows:

$$\text{Gain} = 2 + (50k\Omega / R)$$

where R is the gain setting resistor. The IA is factory adjusted for a gain of 2 without any external resistor.

Important: If a gain greater than 10 is required an external capacitor must be connected from "DELAY" (pin 49) to +5V. This increases an internal delay to allow for the increased settling time of the instrumentation amplifier.

IA IN HI Pin 2. This is the positive input of the internal instrumentation amplifier. This should be connected to pin 4 (MUX OUT HI) for normal operation.

MUX OUT HI Pin 4. This is the high output of the analog input multiplexer. This is connected to pin 2 (IA IN HI) for differential operation. It is connected to pin 77 (MUX OUT LO) and pin 2 for single-ended input operation.

IN7 - IN0 Pins 5 - 12. The first 8 (of 16) analog inputs for single-ended operation or the 8 positive inputs for 8 channel differential input operation.

MUX ENABLE 1 Pin 13. Leave open for single-ended input operation. Connect to pin 14 (MUX ENABLE 2) for differential input operation.

MUX ENABLE 2 Pin 14. Connect to pin 15 (SIN/DIF) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.

SIN/DIF Pin 15. Single/Differential input operation connect to pin 14 (MUX ENABLE 2) for single-ended operation. Leave open for differential input operation.

A0 - A3 Pin 16 - 19. Address lines that select one of 16 analog input signals (IN0 - IN15). 0000 selects channel 0 and 1111 selects channel 15 when the correct address is presented to the MP20. Connect A3 to ground for 8 channel differential operation.

A4 - A15 Address lines. Pins 20, 22, 24, 26, 28 30, 32, 34, 36, 38, 41, and 43. When the proper address is presented to the MP20 in addition to the $\overline{\text{MEMR}}$ (pin 44) pulse, the conversion is initiated.

$\overline{\text{A4}}$ - $\overline{\text{A14}}$ Address select lines. Pin 21, 23, 25, 27, 29, 31, 33, 35, 37, 39 and 42. By connecting these lines to DIG COM or +5 volts (through a 1kΩ resistor) almost any address can be assigned to the MP20. For example if $\overline{\text{A4}}$ is connected to GND., the correct (valid) address for A4 is a "1" (> + 2.0).

ADDR DEC Pin 40. A positive pulse will appear when a valid address appears on the MP20 address lines and $\overline{\text{MEMR}}$ (pin 44) is low. The rising edge of this pulse strobes the input channel select information (A0 - A3) into a latch. It can also be used for external purposes.

$\overline{\text{MEMR}}$ Pin 44. Memory read. A "Low" pulse on this line along with a correct address will enable D0 - D7 (data lines). Also used to initiate a conversion.

DBIN Pin 45. Connect to DBIN on 8080.

$\overline{\text{ENABLE}}$ Pin 46. Enables MP20 output. Connect to ground for normal operation (see figure 7).

$\overline{\text{RESET}}$ Pin 47. A "Low" on this line is required to RESET the MP20. Connect to RESIN input of the system's 8224 or invert 8080's RESET input.

READY Pin 48. When the MP20 is "Read" by the microprocessor, the READY line will go "Low" until conversion is complete. If the READY line is used to halt the CPU, the 8080 will enter a "Wait" state (T_w) until the multiplexer, instrument amp, and A/D converter have completed converting the analog data to a binary 8-bit code (40μsec) with gain ≤ 10). The READY line will then return to its "High" state which releases the processor from the T_w state. The output data appears on the data bus (D0 - D7) during the T_3 state.

DELAY ADJ Pin 49. When the MP20 is addressed, an internal delay of approximately 35μsec is initiated to allow for multiplexer and instrumentation amplifier settling time. When the IA is operated with gain > 10 this delay must be increased (see Figure 4 and Figure 5) to allow for the increased settling time of the IA.

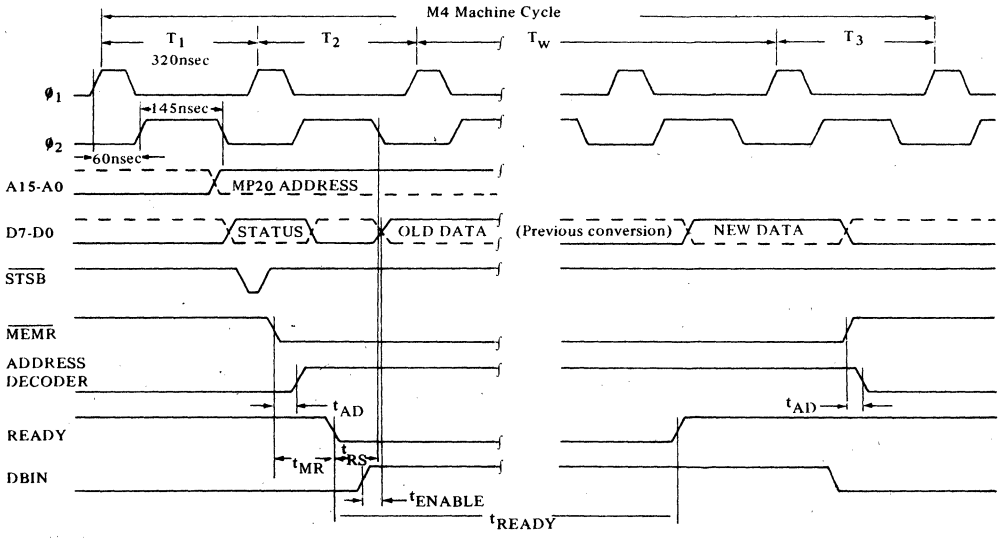
+5V Pin 50. +5V at 140mA maximum, 90mA typical.

DIG COM Pin 51. Digital common. This pin should be connected to analog common (pin 64) as close to the MP20 as possible for optimum performance.

OUTPUT SELECT Pin 52. This pin should be connected to DIG COM to obtain binary data at D0 - D7. To obtain two's complement data (bipolar mode) connect pin 52 to +5V through a 1kΩ resistor.

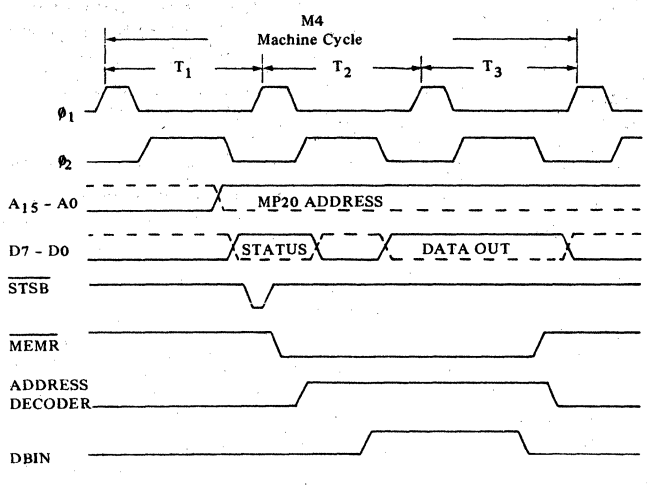
D7 - D0 Pin 53 - 60. 8-bit data bus. Tri-state low power Schottky TTL compatible.

-15V	Pin 61. -15 volt at 30mA typical.
+15V	Pin 62. +15 volt at 30mA typical.
COMP IN	Pin 63. Comparator input of 8-bit A/D converter (successive-approximation). Leave open for unipolar operation or connect to "BPO" (pin 65) for bipolar operation. NOTE: This point is extremely sensitive to noise. Any connection to this line should be as short as possible and shielded by ANA COM or ±15 volt supply patterns.
ANA COM	Pin 64. Analog common should be connected to digital common (pin 51) as close to the MP20 as possible for optimum performance.
BPO	Pin 65. A/D converter bipolar offset. It should be connected to ANA COM (pin 64) for unipolar operation of COMP IN (pin 63) for bipolar operation.
R2	Pin 66. A/D converter input resistor. Connect to IA OUT (pin 68) for 0 to +5V input unipolar operation or ±2.5V input bipolar operation. Leave open for ±5V input bipolar operation.
R1	Pin 67. A/D converter input resistor. Connect to IA OUT for ±5 volt operation. Leave open for other input ranges.
IA OUT	Pin 68. Instrumentation amplifier output. Connect to R1 (pin 67) or R2 (pin 66) for normal operation.
IN8 - IN15 RET0-RET7	Pin 69 - 76. Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
MUX OUT LO	Pin 77. Multiplexer output for IN8 – IN15 RET0 – RET7 Connect to "MUX OUT HI" (pin 4) and "IA IN HI" (pin 2) for single-ended input operation or connect to "IA IN LO" (pin 79) for differential input operation.
OFFSET NULL	Pin 78, 80. Optional instrumentation amplifier offset adjust (see figure 1).
IA IN LO	Pin 79. Negative input of instrumentation amplifier. Connect to ANA COM (pin 64) for single-ended input operation or "MUX OUT LO" (pin 77) for differential input operation.



All waveforms shown are for an 8080A - 1 microprocessor operating at:
CLOCK PERIOD (t_{CY}) = 320nsec
INSTRUCTION CYCLE =1.3μsec
ϕ_1 and ϕ_2 clock signals are shown for reference only. They are not required for operation of MP20.

MP20 Timing Diagram Normal Operation (LDA Instruction using READY to stop microprocessor during conversion).



SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AD}	Delay from MEMR to ADDR. DEC.	-	25	nsec
t_{MR}	Delay from MEMR and correct address to READY	-	100	nsec
t_{RS}	Delay from READY to ϕ_2	-	90	nsec
t_{ENABLE}	Output Data Stable from DBIN	-	40	nsec
t_{READY}	Conversion time READY low	-	40	μsec

The LDA Instruction will READ the data from the previous conversion and start a new conversion. The new data can be read in 40μsec (max).
CAUTION: Do not read the MP20 while a conversion is in progress or an erroneous output may result.

MP20 Timing Diagram (LDA Instruction without stopping microprocessor during conversion).

OPERATING INSTRUCTIONS

PROGRAMMING

The MP20 is easily programmed since it is treated as memory. It uses any memory reference instruction that can read data. A single instruction can read data from one channel (LDA) or two adjacent channels (LHLD).

Example: MP20 used with an 8080. MP20 base address - FF70; acquire data from channels FF70 through FF72. Normal operation.

LHLD FF70	Acquires data and transfers channel 0 (FF70) data to L register and channel 1 (FF71) data to H register.
LDA FF72	Acquires data from channel 2 (FF72) and transfers to the accumulator.

The MP20 may be operated in several programming modes. The minimum software approach (i.e., one instruction to acquire data as described above) is to halt the CPU during conversion (40 μsec). This mode of operation is effected by connecting the READY line (pin 48) of the MP20 to the 8080's READY input. The MP20 may also be operated without halting the CPU. In this mode of operation conversion may be initiated by a memory read instruction referenced to the proper channel. When the conversion is complete, the data value may be acquired by another read instruction. The second read instruction can be referenced to any channel address of the MP20. This instruction should be addressed to the next channel to be acquired since it will start a conversion cycle.

Example: MP20 used with an 8080. MP20 base address - FF70; acquire data from channels FF70 through FF72. Do not halt CPU.

LDA FF70	Starts conversion of channel 0 (FF70).
⋮	At least 40 microseconds of software here to insure that conversion is complete.
LDA FF71	Transfers conversion data from channel 0 (FF70) to accumulator and starts conversion of channel 1 (FF71).
⋮	At least 40 microseconds of software.
LDA FF72	Transfers conversion data from channel 1 (FF71) to accumulator and starts conversion of channel 2 (FF72).
⋮	At least 40 microseconds of software.
LDS FF7X	Transfers conversion data from channel 2 (FF72) to accumulator and starts conversion of any other channel of data.

The time required for conversion may be between 40μsec and 200μsec depending upon the gain of the internal instrumentation amplifier. Therefore, the 40μsec time between LDA instructions shown above could be as long as 200μsec for a system used in the highest gain mode. If desired, the READY line may be polled to determine that conversion is complete and the data output valid. Of course, if direct addressing is not desired, MOV instructions may also be used.

Example: MP20 used with an 8080. MP20 base address FF70. Normal Operation. Read and Print the value of all 16 input channels and then stop.

```
CROUT   EQU 01F3H (01EEH)
NMOUT   EQU 02C2H (02C3H)
        LXI SP 3FFF H (13EDH)
        LXI H 0FF70 H     :Address for channel zero
BEG 1:  MOV D, M          :Read data from board
        CALL CROUT        :Print CR & LF
        MOV A, D
        CALL NMOUT        :Print data
```

```
        INX H           :Next channel
        MOV A, L
        CPI 10          :Have all 16 channels
                         been read?
        JZ WHOA
        JMP BEG 1
WHOA:   HLT
```

This program assumes that the system is under the control of the SBC80/10 prototype package monitor (M80P, version 1.0, March 1, 1976). The locations in parenthesis are used with the MCS-80 system design kit.

The base address of the MP20 is set by inputs $\overline{A4}$ through $\overline{A14}$. Address lines A4 through A14 respond to the inverse of inputs $\overline{A4}$ through $\overline{A14}$. For instance, if $\overline{A6}$ is grounded, A6 will respond to a "high" input. A15 is internally connected to respond to a "high" input.

ANALOG INPUT RANGE SELECTION

The MP20 may be set for any range between ±5V and ±10 mV. Table I shows the pin connections for the various high level ranges available.

TABLE I. Analog Input Range Pin Connections.

MP20 Input Range	Gain	ADC Range	Pin Connections
±5V	2	±10V	65 to 63; 66 open; 67 to 68
±2.5V	2	±5V	65 to 63; 66 to 68; 67 open
±1.25V	2	±2.5V	65 to 63; 66 to 68; 63 to 67
0 to 5V	2	0 to 10V	65 to 64; 66 to 68; 67 open
0 to 2.5V	2	0 to 5V	65 to 64; 66 to 68; 63 to 67

The MP20 may be set to output data with straight binary coding (pin 52 grounded) or two's complement coding (pin 52 to +5VDC through a 1kΩ resistor). Straight binary coding is typically used with unipolar input ranges and two's complement coding with bipolar input ranges. Table II describes the coding.

The internal instrumentation amplifier is factory set for a gain of 2. This gain can be increased to 250 by adding an external resistance (R_{ext}) between pins 1 and 3. R_{ext} should be a stable resistor (10 ppm °C) since this temperature drift will add to the accuracy temperature coefficient. The gain of the amplifier can be determined by this formula:

$$\text{Gain} = 2 + \frac{50k\Omega}{R_{ext}}$$

With pins 1 and 3 open, the gain is 2.

Since the amplifier input offset will be multiplied by the amplifier gain, an offset adjust may be required (see figure 1b).

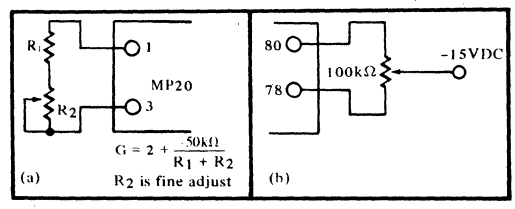


FIGURE 1. (a) MP20 Gain Adjust; (b) Offset Adjust.

SINGLE ENDED VS. DIFFERENTIAL INPUTS

The MP20 analog inputs may be connected as single-ended, differential or pseudo-differential. Single-ended operation may be used for high level (over one volt full scale) signals in low noise environments (Figure 3). Differential operation will reject common-mode noise appearing on both inputs (Figure 2). It should be used in noisy environments or with any low level signal (less than one volt). In the pseudo-differential mode, the MP20 is connected as for the single-ended mode in Figure 3 except the I.A. low input, pin 79, is not grounded. Pin 79 is connected to an external ground that is common to all of the analog inputs. In cases with a noisy remote ground where little noise will be picked up between sensor and MP20, the pseudo-differential mode may be used.

The MP20 is set for single-ended operation when wired as shown in Figure 3. The microprocessor address lines are connected as indicated in the Pin Connections table on page 3. Differential operation occurs when the unit is connected as in Figure 2. However, address line A3 (Pin 19) should be grounded and A3 on the microprocessor connected to A4 on the MP20. The remainder of the higher ordered microprocessor address bits should be connected to the next higher bit on the MP20.

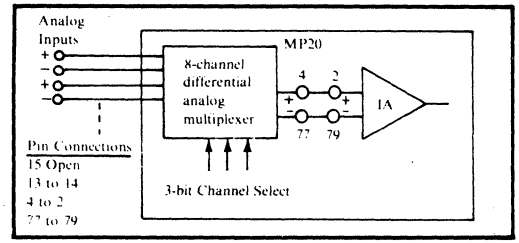


FIGURE 2. Differential Input Connections.

TABLE II. Analog Input Values.

	DIGITAL OUTPUT		ANALOG INPUT		
Straight Binary Code	Two's Complement Code		±5V	0 to +5V	±10mV
1111 1111 (FF_{16})	0111 1111 ($7F_{16}$)	+Full Scale	+4.961V	+4.980V	+9.92mV
1000 0000 (80_{16})	0000 0000 (00_{16})	Mid-Scale	0.000V	2.500V	0.000V
0000 0000 (00_{16})	1000 0000 (80_{16})	-Full Scale	-5.000V	0.000V	-10.00mV
		One LSB	39mV	19.5mV	78μV

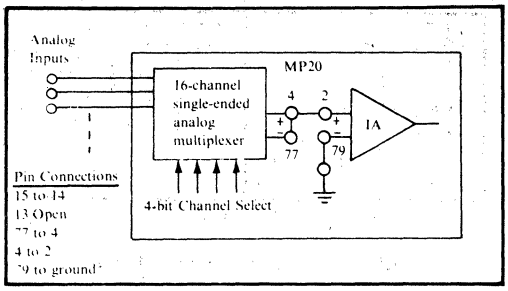


FIGURE 3. Single-ended Input Connections.

DELAY TIMING

A delay time between channel selection and start of conversion is built into the MP20 to allow the analog multiplexer and instrumentation amplifier (I.A.) time to settle before starting the A/D converter. As the gain of the amplifier is increased, the settling time required increases. The factory set delay time (35μsec) is sufficient for gains of up to 10. At higher gains, a capacitor must be added from pin 49 to the +5 VDC supply to increase the delay time. Figure 4 shows the settling time of the MP20 vs. gain. Figure 5 shows the value of capacitance required to increase the delay.

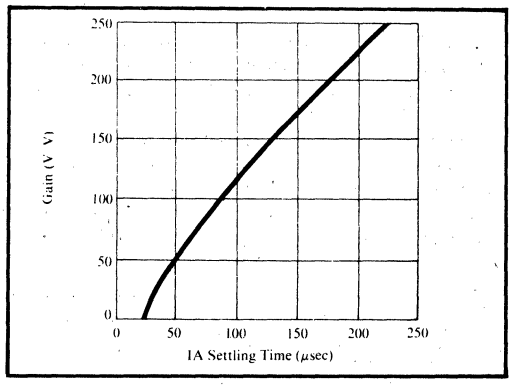


FIGURE 4. Typical IA Settling Time vs Gain (Output Settling to ±0.1%).

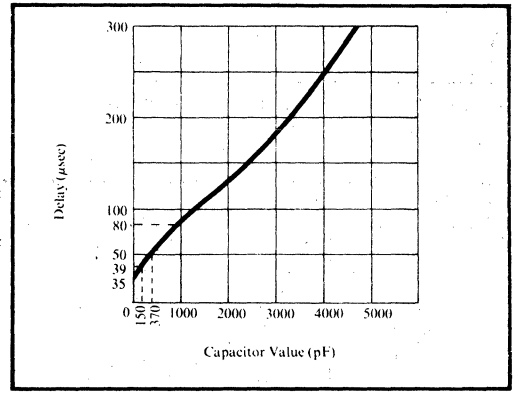


FIGURE 5. Typical Delay Time vs Capacitor Value.

The only external factor, other than gain, that effects the MP20 settling time is the impedance of the source connected to a channel. Figure 6 shows a circuit model of an "ON" channel.

The signal at the output of the multiplier must be allowed to settle to ±0.1% (six time constants) to maintain the full accuracy of the system. The multiplexer time constant can be calculated with the equation: $\tau = (R_S + R_{ON})C_o$. For R_S = 1kΩ and C_o = 50pF, $\tau = (1.5 + 1)k\Omega \times 50pF$ = 125nsec. Thus 0.75μsec is needed to settle to ±0.1%. For high input impedances requiring more than 10μsec for multiplexer settling time, the required delay time may be calculated with this formula: $T_D = \sqrt{T^2_{mux} + T^2_{IA}}$, where T_{mux} is the settling time of the multiplexer and T_{IA} is the settling time of the instrumentation amplifier as shown in Figure 4. If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large capacitance across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5μF is sufficient. For such a capacitance the multiplexer time constant becomes 80nsec.

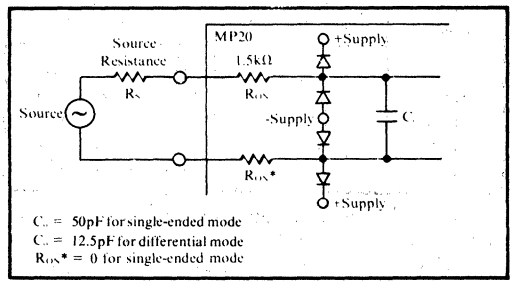


FIGURE 6. "ON" Channel Circuit Model.

INPUT OVERVOLTAGE PROTECTION

As shown in Figure 6, the analog inputs have reverse biased diode circuits which protect from damage by overvoltage (such as static). It is still reasonable to take precautions against static discharge. The same circuitry protects the inputs from steady-state overvoltage damage during operation. The MP20's overvoltage protection can be increased by adding series resistors at each input. The input resistance must limit the current flowing through the input protection diodes to 10mA. For instance, if 15kΩ resistors are added to each input, the protection is increased to 165V (16.5kΩ x 10mA). Increased input resistance will, of course, increase the amount of time necessary for the multiplexer to settle as described in the previous section.

OUTPUT ENABLE

The circuitry used to enable the tristate output lines (D7 - D0) on the MP20 can be connected in such a way as to meet a wide variety of timing requirements. The output is enabled only when the address decoder output (pin 40) is high, DBIN (pin 45) is high, and $\overline{\text{ENABLE}}$ (pin 46) is low. Any other combination of digital signals on these lines will result in D7 - D0 being in a high impedance state (see Figure 7).

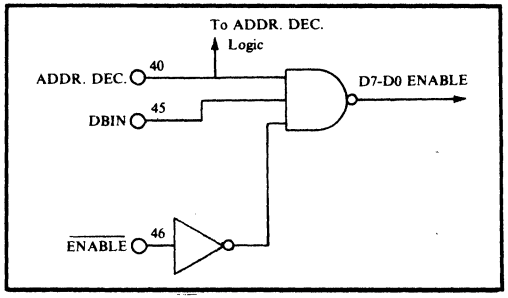


FIGURE 7. Output Enable Circuitry.

The combination of a correct address and a memory read ($\overline{MEMR}$ - pin 44) command will cause the address decoder output to go high. If $\overline{ENABLE}$ is not used it should be connected to DIG COM. If DBIN is not used it should be connected to +5V through a 1kΩ resistor. Most applications will only require the use of one of these lines. lines.

RESET

It is important to reset the MP20 on start up with a low pulse on the $\overline{RESET}$ line (pin 47) if the READY line (pin 48) is being used to halt the processor. The reset pulse simply clears an internal flip-flop and guarantees that on start up the READY line will go high thereby not halting CPU.

If the MP20 conversion cycle is being timed out by software control, a reset pulse is not necessary. If the $\overline{RESET}$ line is not used it should be connected to +5V.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

HIGHER SPEED OPERATION

The MP20's internal instrumentation amplifier requires 35μsec to allow for settling time. If this internal amplifier is not used, substantial improvements in throughput rate can be obtained. This is easily done since neither the inputs nor the output of the instrument amplifier are internally connected. For instance, Burr-Brown's 3507J high speed op amp (for single-ended inputs) may be used, with a settling time of 0.2μsec for gains of up to 100. The total delay time necessary may be calculated by this formula:

$$T_D = \sqrt{T^2_{MUX} + T^2_{IA}},$$

where T_{MUX} is the settling time of the multiplexer (750nsec) and T_{IA} is the settling time of the instrument amplifier. For a T_{IA} of 0.2μsec we have T_D = 0.78μsec. Using 3μsec for the delay time to allow for unit to unit variation, the total throughput time will be 8μsec (including 5μsec for ADC conversion time) or 125kHz. A resistor between pin 49 and +5VDC will reduce the delay time from the factory set value of 35μsec (see Figure 8).

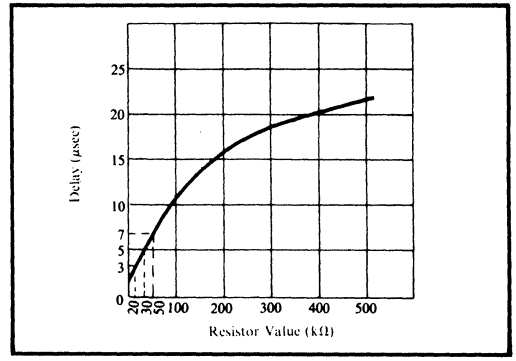


FIGURE 8. Typical Resistor Value to decrease Delay Time.

CALIBRATION

The MP20 is laser trimmed at the factory to ±0.4% accuracy when using the ±5V or 0 to +5V ranges. If one of these ranges is used, no adjustments are required. If the ±2.5V, ±1.25V or 0 to +2.5V ranges are used, an offset adjust only is required. For other ranges, both the gain and offset must be adjusted. Figure 1 shows the adjustment connections. The gain adjustment should be made such that the transition to a full scale output (1111 1110 to 1111 1111 for straight binary) occurs with an input of positive full scale less 3/2LSB. One least significant bit (LSB) is the full scale range (FSR) divided by 2^n where n is the number of bits of the A/D converter. For the MP20, one LSB is FSR/2^8 = FSR/256. The offset adjustment should be made such that the transition to minus full scale output (0000 0001 to 0000 0000 for straight binary) occurs with an input of negative full scale plus 1/2LSB. For a range of ±50mV, 1LSB = 100mV/256 = 0.39mV. The gain adjustment should be made at +50mV - (1.5)(0.39mV) = +49.42mV. The offset adjustment should be made at -50mV + (0.5)(0.39mV) = 49.80mV. Table III shows offset and gain calibration values for typical ranges.

Table III. Calibration Values.

MP20 Input Range	Instrument Amp Gain	ADC Range	Calibration Values	
			Offset	Gain
±5V	2	±10V	-4.980V	+4.941V
0 to +5V	2	0 to +10V	+9.8mV	+4.971V
±2.5V	2	±5V	-2.490V	+2.471V
0 to +2.5V	2	0 to +5V	+4.9mV	+2.485V
±1.25V	2	±2.5V	-1.245V	+1.235
0 - 50mV	100	0 to +5V	+98μV	+49.7mV
±25mV	100	±2.5V	-24.9mV	+24.7mV
0 - 25mV	200	0 to +5V	+49 μV	+24.9mV

The following program may be used to adjust gain and offset.

```
REF     EQU  00H              Offset Ref=00H
                              Full Scale Ref = FFH

CO      EQU  01E8H(01E3H)     Monitor routines

CROUT   EQU  01F3H(01EEH)
```

```
NMOUT  EQU    02C2H(02C3H)
;
       ORG    3C50H
;
       LXI    H, 0FF7ØH      Initialize
       LXI    SP,3FFFH(13EDH)
BEG1:  MVI    E,10H
BEG2:  LXI    B, 0
CLP:   MOV    A, M           :Read data from
                              board
       SUI    REF            :Increment data
                              count if data =
                              REF
       JNZ    NEQ
       INR    B
NEQ:   INR    C              :Have 100
                              conversions
                              been made?
       MVI    A, 64H
       SUB    C
       JNZ    CLP
       MOV    A, B           :Yes, Print data
                              count
       CALL   NMOUT
       MVI    C,20H          :Print a space
       CALL   CO
       DCR    E              :Full line been
                              printed?
       JNZ    BEG2
       CALL   CROUT          :Yes, Print CR
                              & LF
       JMP    BEG1
       END
```

This program assumes that the system is under the control of the SBC80/10 prototype package monitor (M80P, version 1.0, March 1, 1976). The locations in parenthesis are used to allow the program to work with the MCS-80 system design kit. It may be used for both offset and gain calibration. The system offset should be adjusted first, followed by the gain adjustment.

The address of channel zero is assumed to be FF7Ø. If it is not, the LXI H instruction should reflect that change. The reference values on the first line assume straight binary coding. For offset binary coding, Offset Ref = 80 and Full Scale Ref = 7F.

A G3C50 monitor command will begin program execution. After 100 conversions have been made, the value (in hex) of the B register will be printed. This value represents the number of times the data read from the board was equal to "REF" (00 for offset; FF for gain).

Calibration is performed by connecting a voltage source capable of 0.01% accuracy to input channel zero (this could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.01% DVM).

The offset adjustment is made first by using the appropriate offset calibration voltage. Run the calibration program and adjust the on board offset potentiometer until the B register contains a value between $1E_{16}$ and 46_{16} (30_{10} and 70_{10}).

To perform the gain adjustment change the data labeled "REF" in the calibration program from 00 to FF, set the input voltage to the correct value as shown in Figure 8 and adjust the on board gain potentiometer in the same manner as described for offset.

If the SBC80 monitor is available, the substitute (S) command can be used to interrogate an input channel.

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70 $\mu V/^{\circ}C$ and operating ranges of minus hundreds to plus thousands of degrees centigrade. When the MP20 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60Hz or higher frequencies. When the MP20 is used as an 8-channel differential input system, the high common-mode rejection of the instrument amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices cannot always be observed, a differential RC filter may be used. Figure 9 shows such a system.

The 10kΩ resistors and 10μF capacitor provide low pass filtering (f_c = 0.8Hz) while the optional 1MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±5V range of the multiplexer. If the sensor is earth grounded, the 1MΩ resistors are not required. The 1MΩ resistor do not enter into an error calculation for input errors because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias current of each input. See the overvoltage protection section for a discussion of the effects fo the 10kΩ in the input filter. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 9 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2mV/°C.

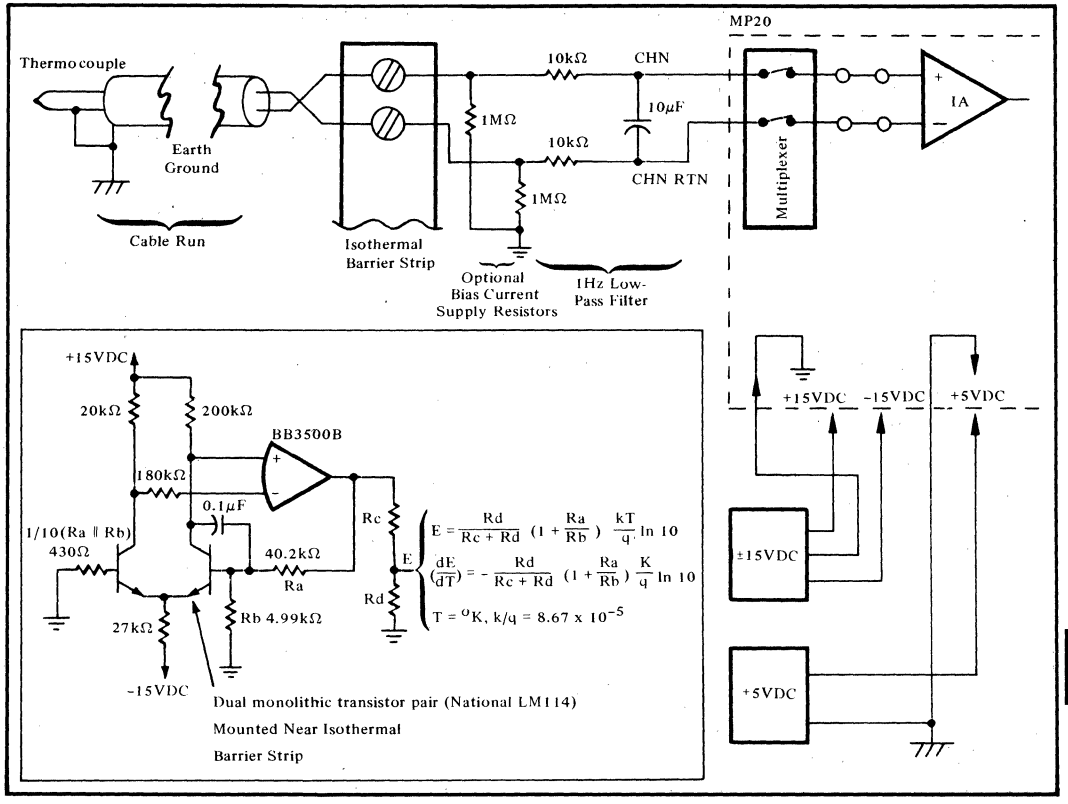


FIGURE 9. Thermocouple Input System Using MP20.

MP20

PIN CONNECTION SUMMARY

	JUMPER		JUMPER
Single-ended Multiplexer	4 to 2; 4 to 77; 79 to 64; 15 to 14; 13 open	Address Bus (A0-A15)	Connect to 8080's address bus, A0-A15
Differential Multiplexer	4 to 2; 77 to 79; 13 to 14; 15 open	Address Select ($\overline{A4}$-$\overline{A14}$)	Connect to +5V* or Ground
Amplifier	1 and 3 open for G = 2; R_{ext} between 1 and 3 for G≠2.	Control Bus	44 to 8228's $\overline{MEMR}$ output (pin 24) 45 to 8080's DBIN output (pin 17) 46 to ground 47 to 8224's $\overline{RESIN}$ input (pin 23) for normal operation 48 open for operation without halting CPU.
Input Range ±5V ±2.5V ±1.25V 0 - 5V 0 - 2.5V	 65 to 63; 66 open; 67 to 68 65 to 63; 66 to 68; 67 open 65 to 63; 66 to 68; 63 to 67 65 to 64; 66 to 68; 67 open 65 to 64; 66 to 68; 63 to 67		
Output Coding	52 to 51 for binary; 52 to 50* for two's complement.	Data Bus (D0 - D7)	Connect to 8080's data bus.
* Through a 1kΩ resistor			

MICROPROCESSOR INTERCONNECTION

The following diagrams show interconnections of the MP20 (described in this data sheet) and also of Burr-Brown's MP10 analog output microperipheral (PDS-363) with Intel's 8080, National's SC/MP and Zilog's Z-80.

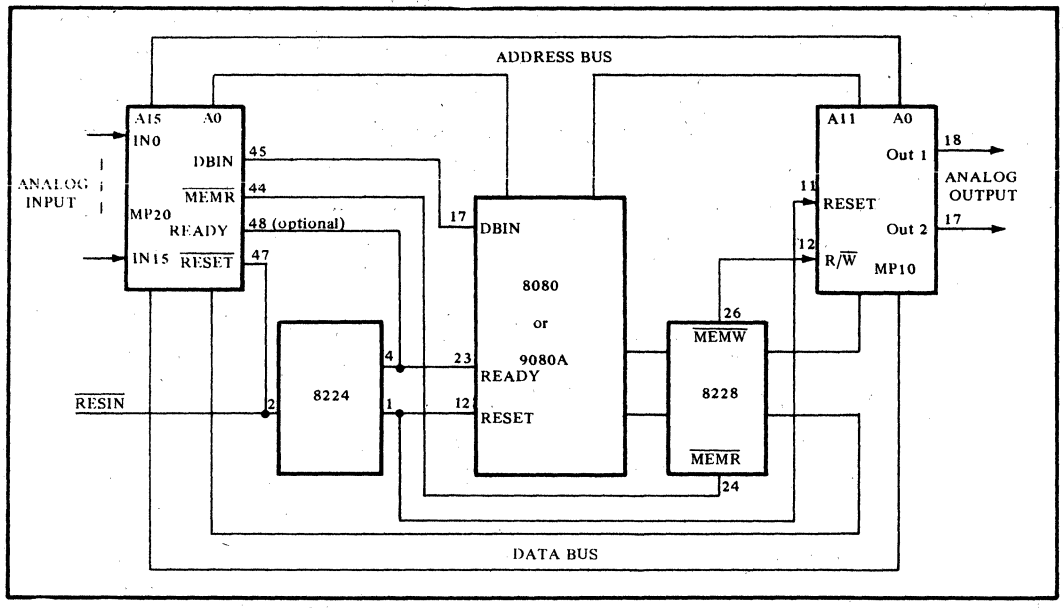


FIGURE 10. MP10 and MP20 Used With the 8080.

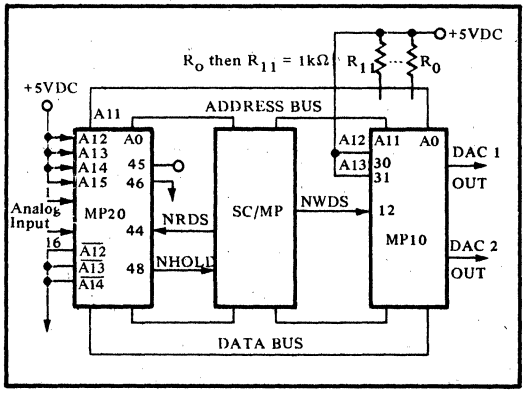


FIGURE 11. MP10 and MP20 Used With the SC/MP.

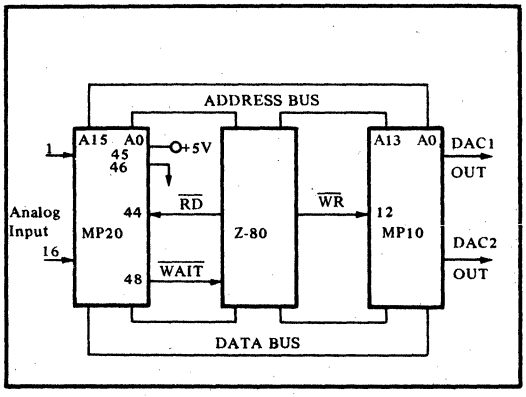


FIGURE 12 MP10 and MP20 Used With the Z-80.

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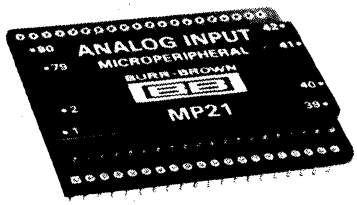
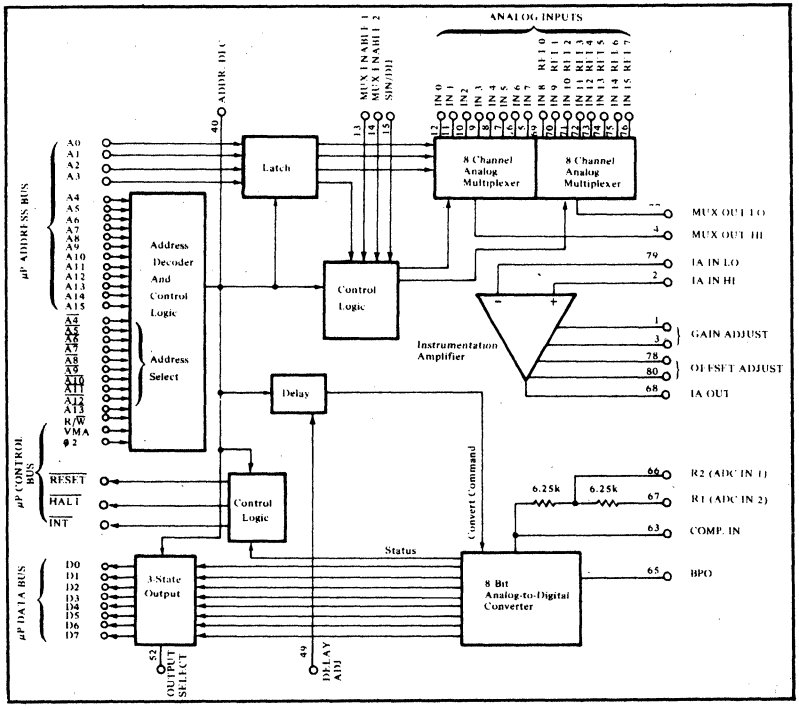


MP21

Microprocessor-Interfaced 8-BIT ANALOG INPUT SYSTEM



FEATURES

- COMPATIBLE WITH:
  - 6800
  - 650X
  - F-8
- EASY TO PROGRAM
  - Choice of ways to interface:
    - Memory-mapped
    - Interrupt capability
- SAVES DEVELOPMENT TIME AND MONEY
- EASY TO USE
  - PIA is not needed
  - No external logic needed
  - No external adjustments
  - Low or high level analog inputs
  - Unlimited expansion
- COMPLETELY SELF-CONTAINED
- LOW COST

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

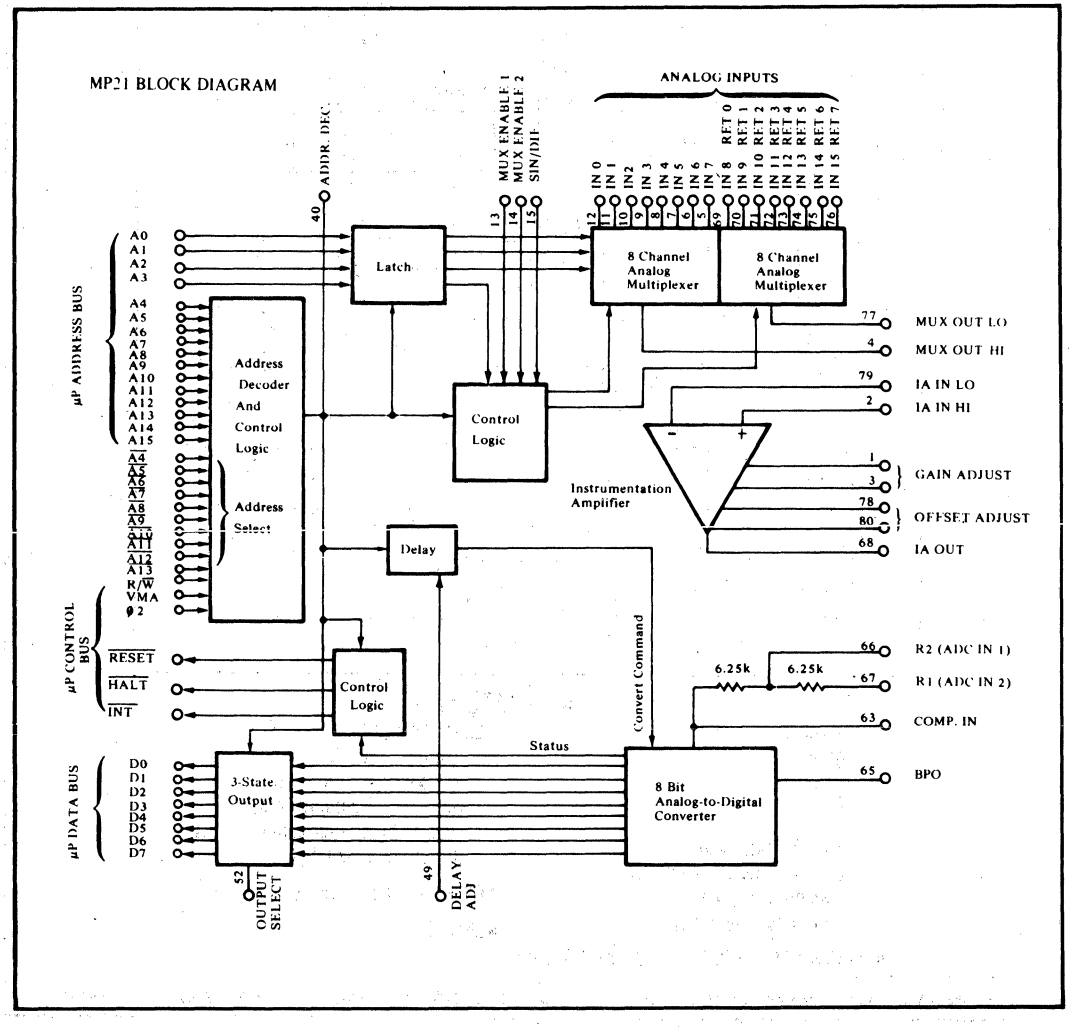
DESCRIPTION

The MP21 is a complete analog input system packaged in a 80-pin quad-in-line package. It is completely compatible with 6800 microprocessors. It is also compatible with the 650X and with the F-8. The MP21 contains a high speed 8-bit A/D converter, an instrumentation amplifier, an input multiplexer that can accept up to 16 single-ended signals or 8 differential signals as well as interface, timing and address decoding logic. The gain and offset are internally laser trimmed so that no external adjustments are required on the ±5V or 0 to +5V input range to obtain an absolute accuracy of better than ±0.4% (1 LSB). The system can digitize low level or high level analog signals. The gain of the internal instrumentation amplifier can be programmed with a single external resistor to allow input signal ranges as low as ±10 mV. This means that the MP21 can be connected to low level sensors such as thermocouples and strain gauges without external signal amplification.

All control lines are fully compatible with the microprocessor bus and operate at low power Schottky TTL levels. The MP21 input lines present one LS TTL load while all outputs can drive up to 20 LS TTL loads.

PROGRAMMING

When programming these peripherals, the user treats them as memory. Each analog input channel occupies one memory location. Any memory reference instruction can be used. Pins $\overline{A4}$ to $\overline{A13}$ are made available so that the microperipheral address can be hardwired for any of 1024 possible memory location bands. Since these units are treated as memory, a minimum of instructions are needed to read an input channel. The MP21's versatile memory mapped operation allows it to be used with or without halting the CPU or in the interrupt mode.



SPECIFICATIONS

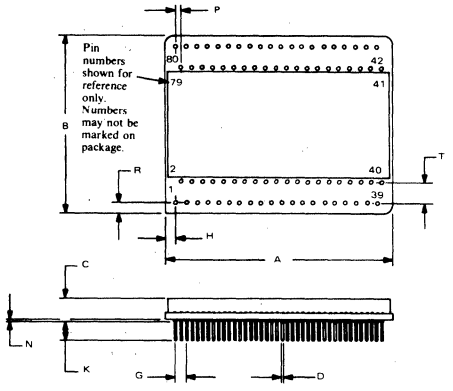
Typical at 25°C unless otherwise noted.

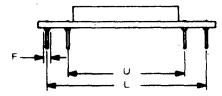
ELECTRICAL

TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
Number of channels	16 single-ended/8 differential
Throughput rate[1] (max)	40μsec/channel
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	2 to 250
Amplifier gain equation	$G = 2 + 50k\Omega/R_{ext}$[2]
Max input voltage without damage[3]	±23 volts
Max input voltage for multiplexer operation	±6 volts
Input impedance	$5 \times 10^9\Omega$ || 10 pF - OFF channel $5 \times 10^9\Omega$ || 100 pF - ON channel
Bias current 25°C	100 nA
0 - 70°C	200 nA
Amplifier output noise	
Gain = 100, $R_S = 500\Omega$	400μV rms (10 Hz to 10 kHz)
Amplifier input offset voltage (max)	±1 mV
Amplifier offset voltage drift	±(6 + 50/G)μV/°C
Amplifier settling time (to .1% FSR)	
G = 2	20μs
G = 10	25μs
G = 50	50μs
G = 100	100μs
G = 200	200μs
CMRR (for differential inputs) (G = 2)	70 dB (DC to 60 Hz)
ACCURACY	
Throughput accuracy	
±5V, ±2.5V, ±1.25V range (max)[4]	±0.4% of FSR[5]
0-5V, 0-2.5V range (max)[4]	±0.4% of FSR
±50 mV range (max)[6]	±0.8% of FSR
0-50 mV range (max)[6]	±0.8% of FSR
Linearity (max)[4]	±0.2% of FSR
Differential linearity[4]	±0.2% of FSR
Quantizing error	±1/2 LSB
Gain error (max)[4]	±0.1%
Offset error (max)[4]	±0.1% of FSR
Power supply sensitivity	
±15V	±0.02%/%ΔV$_{CC}$
+5V	±0.002%/%ΔV$_{CC}$
STABILITY OVER TEMPERATURE	
System accuracy drift[7] (max)	±40 ppm/°C
Linearity (max)	±20 ppm/°C
Monotonicity (0°C to +70°C)	Guaranteed
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microprocessor bus	
Output coding	Binary or Binary two's complement
Logic loading	All digital inputs are one LSTTL load
Output drive (D0 - D7)	5 TTL loads or 20 LSTTL loads
An analog input channel is selected by:	A0 - A3
The output data bus are read into:	D0 - D7
POWER REQUIREMENTS	
Rated voltages	±15V, +5V
Range for rated accuracy	4.75 to 5.25 and ±14.5 to ±15.5V
Supply drain ±15V	±30 mA
+5V	+90 mA
TEMPERATURE RANGE	0°C to +70°C

(1) Includes 35μsec for mux and amplifier time and 5μec for ADC conversion time.
(2) R_{ext} is an external resistor connected between pins 1 and 3.
(3) With power applied.
(4) With no external adjustments.
(5) FSR is Full Scale Range (FSR is 10V for ±5V range).
(6) Gain = 100 with external gain and offset trim.
(7) Includes gain drift, offset drift and linearity drift.

MECHANICAL





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	

NOTE: LEADS IN TRUE POSITION WITHIN .015" (.38mm) R AT MMC AT SEATING PLANE.

MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz) PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2) MATING CONNECTOR: 2350MC (Set of four 20 pin strips)

PIN CONNECTIONS

Pin		Pin	
1	IA GAIN ADJUST	41	A14
2	IA IN HI	42	R/W
3	IA GAIN ADJUST	43	A15
4	MUX OUT HI	44	INT
5	IN 7	45	VMA
6	IN 6	46	Ø2
7	IN 5	47	RESET
8	IN 4	48	HALT
9	IN 3	49	DELAY ADJ
10	IN 2	50	+5V
11	IN 1	51	DIG COM
12	IN 0	52	OUTPUT SELECT
13	MUX ENABLE 1	53	D7 (MSB)
14	MUX ENABLE 2	54	D6
15	SIN DIF	55	D5
16	A0	56	D4
17	A1	57	D3
18	A2	58	D2
19	A3	59	D1
20	A4	60	D0 (LSB)
21	A4	61	-15V
22	A5	62	+15V
23	A5	63	COMP IN
24	A6	64	ANA COM
25	A6	65	BPO
26	A7	66	R2 (ADC IN 1)
27	A7	67	R1 (ADC IN 2)
28	A8	68	IA OUT
29	A8	69	IN 8 RET 0
30	A9	70	IN 9 RET 1
31	A9	71	IN 10 RET 2
32	A10	72	IN 11 RET 3
33	A10	73	IN 12 RET 4
34	A11	74	IN 13 RET 5
35	A11	75	IN 14 RET 6
36	A12	76	IN 15 RET 7
37	A12	77	MUX OUT LO
38	A13	78	OFFSET NULL
39	A13	79	IA IN LO
40	ADDR DECODE OUT	80	OFFSET NULL

MP21

PIN FUNCTIONS

IA GAIN ADJUST (Optional). Pin 1 and Pin 3. By connecting a resistor between pin 1 and 3 the gain of the internal instrumentation amplifier can be set as follows:

$$\text{Gain} = 2 + 50k\Omega/R_{ext}$$

Where R_{ext} is the gain setting resistor. The IA is factory adjusted for a gain of 2 without any external resistor.

Important: If a gain greater than 10 is required an external capacitor must be connected from "DELAY" (pin 49) to +5V. This increases an internal delay to allow for the increased settling time of the instrumentation amplifier. (See page 6-224)

IA IN HI Pin 2. This is the positive input of the internal instrumentation amplifier. This should be connected to pin 4 (MUX OUT HI) for normal operation.

MUX OUT HI Pin 4. This is the output of the analog input multiplexer. This is connected to pin 2 (IA IN HI) for differential operation. It is connected to pin 77 (MUX OUT LO) and pin 2 for single-ended input operation.

IN7 - IN0 Pins 5 - 12. The first 8 (of 16) analog inputs for single-ended operation or the 8 positive inputs for 8 channel differential input operation.

MUX ENABLE 1 Pin 13. Leave open for single-ended input operation. Connect to pin 14 (MUX ENABLE 2) for differential input operation.

MUX ENABLE 2 Pin 14. Connect to pin 15 (SIN/DIF) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.

SIN/DIF Pin 15. Single/Differential input operation connect to pin 14 (MUX ENABLE 2) for single-ended operation. Leave open for differential input operation.

A0 - A3 Pin 16 - 19. Address lines that select one of 16 analog input signals (IN0 - IN15). 0000 selects channel 0 and 1111 selects channel 15 when the correct address is presented to the MP21. Note: A3 should be connected to DIG COM for 8 channel differential input operation.

A4 - A15 Address lines. Pins 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 41, and 43. Connect to A4 - A15 of the 6800.

$\overline{A4}$ - $\overline{A13}$ Address select lines. Pin 21, 23, 25, 27, 29, 31, 33, 35, 37, and 39. By connecting these lines to DIG COM or +5 volts (through a 1kΩ resistor) any of 1024 address bands can be assigned to the MP21. For example, if $\overline{A4}$ is connected to GND., the correct (valid) address for A4 is a "1" (> + 2.4V).

ADDR DEC Pin 40. A positive pulse will appear when a valid address appears on the MP21 address lines and when R/$\overline{W}$ (pin 42), and Ø2 (pin 46) and VMA (pin 45) are high. The rising edge of this pulse strobes the input channel select information (A0 - A3) into a latch. It can also be used for external purposes.

R/$\overline{W}$ Pin 42. Read/Write control line. Connect to R/$\overline{W}$ of 6800.

$\overline{INT}$ Pin 44. Interrupt output. Connect to $\overline{IRQ}$ or $\overline{NMI}$ of the 6800 if interrupt operation is desired. When conversion has been completed, a 10μsec pulse (negative) is generated on this line. (Not an open collector output.)

VMA Pin 45. Connect to VMA on 6800.

Ø2 Pin 46. Connect to Ø2 on 6800.

$\overline{RESET}$ Pin 47. A "Low" on this line is required to reset the MP21. Connect to the $\overline{RESET}$ input of the 6800.

$\overline{HALT}$ Pin 48. When the MP21 is "Read" by the microprocessor via any memory reference instruction the $\overline{HALT}$ line will go "Low" until conversion is complete. If the $\overline{HALT}$ line is used to halt the CPU, the 6800 will halt upon completion of the next instruction. When the multiplexer, instrument amp, and A/D converter have completed converting the analog data to a binary 8 bit code (40μsec with gain ≤ 10) the $\overline{HALT}$ line will then return to its "High" state which releases the processor. The output data can then be read with a second memory reference instruction. (Not an open collector output.)

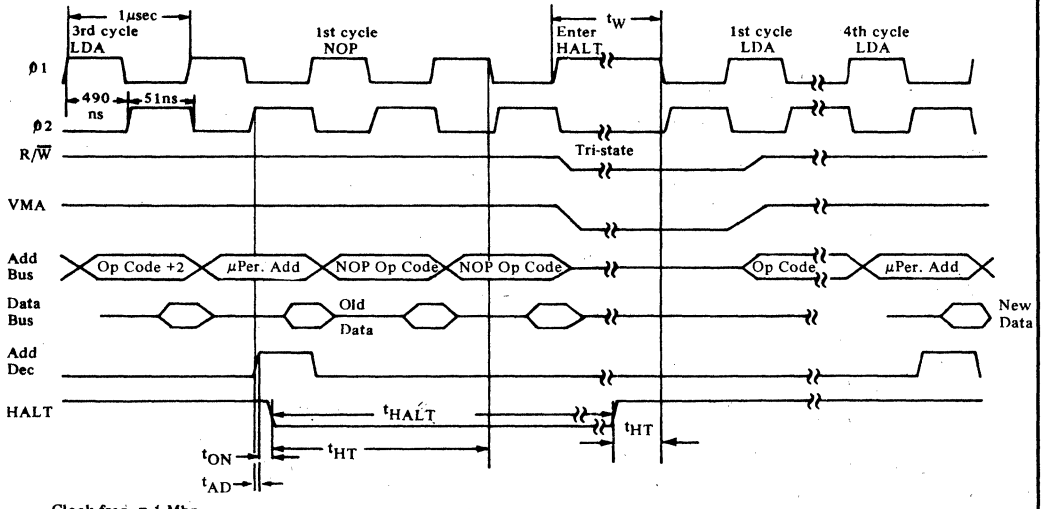
DELAY ADJ Pin 49. When the MP21 is addressed, an internal delay of approximately 35μsec is initiated to allow for multiplexer and instrumentation amplifier settling time. When the IA is operated with gain > 10 this delay must be increased (see Figure 4) to allow for the increased settling time of the IA. This is done by adding a capacitor between pin 49 and +5V. (See Figure 5)

+5V Pin 50. +5 volt at 140 mA maximum, 90 mA typical.

DIG COM Pin 51. Digital common. This pin should be connected to analog common (pin 64) as close to the MP21 as possible for optimum performance.

OUTPUT SELECT Pin 52. This pin should be connected to DIG COM to obtain binary data at D0 - D7. To obtain two's complement data (bipolar mode) connect pin 52 to +5V through a 1kΩ resistor.

D7 - D0	Pin 53 - 60. 8 bit data bus. 3-state low power Schottky TTL compatible.
-15V	Pin 61. -15 volt at 30 mA typical.
+15V	Pin 62. +15 volt at 30 mA typical.
COMP IN	Pin 63. Comparator input of 8 bit A/D converter (successive-approximation). Leave open for unipolar operation or connect to "BPO" (pin 65) for bipolar operation. NOTE: This point is extremely sensitive to noise. Any connection to this line should be as short as possible and shielded by ANA COM or ±15 volt supply patterns.
ANA COM	Pin 64. Analog common should be connected to digital common (pin 51) as close to the MP21 as possible for optimum performance.
BPO	Pin 65. A/D converter bipolar offset. It should be connected to ANA COM (pin 64) for unipolar operation or COMP IN (pin 63) for bipolar operation.
R2	Pin 66. A/D converter input resistor. Connect to IA out (pin 68) for 0 to +5V input unipolar operation or ±2.5V input bipolar operation. Leave open for ±5V input bipolar operation.
R1	Pin 67. A/D converter input resistor. Connect to IA out for ±5 volt operation. Connect to Pin 63 for 0 to +2.5V and ±1.25V ranges.
IA OUT	Pin 68. Instrumentation amplifier output. Connect to R1 (pin 67) or R2 (pin 66) for normal operation.
IN8-IN15 RET0-RET7	Pin 69-76. Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
MUX OUT LO	Pin 77. Multiplexer output for IN8-IN15 or RET0-RET7. Connect to "MUX OUT HI" (pin 4) and "IA IN HI" (pin 2) for single-ended input operation or connect to "IA IN LO" (pin 79) for differential input operation.
OFFSET NULL	Pin 78, 80. Optional instrumentation amplifier offset adjust (see Figure 1).
IA IN LO	Pin 79. Negative input of instrumentation amplifier. Connect to ANA COM (pin 64) for single-ended input operation or "MUX OUT LO" (pin 77) for differential input operation.



Clock freq. = 1 Mhz

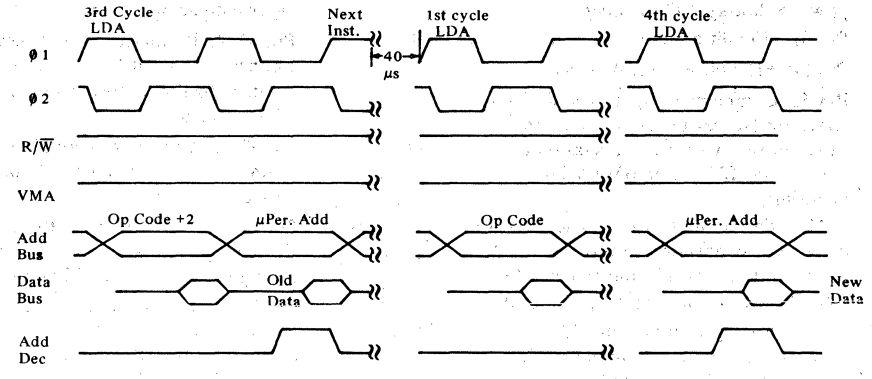
t_{HT} = 200ns min before falling edge of ϕ1

t_{HALT} = 40μsec (max)

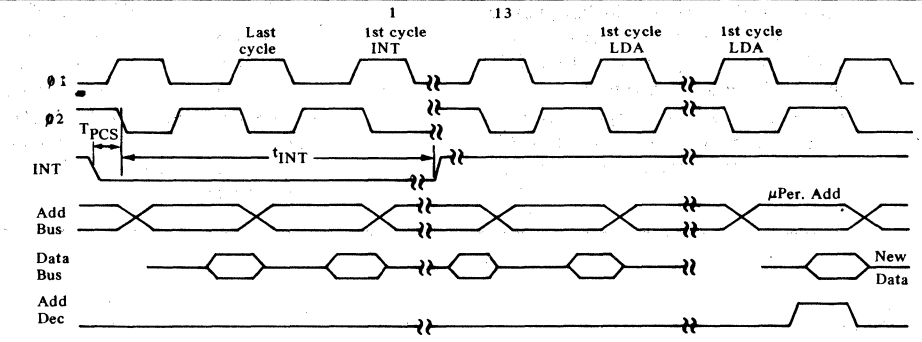
t_{ON} = 70nsec (max)

t_{AD} = 30nsec (max)

MP21 Timing Diagram (using HALT to stop microprocessor during conversion).



MP21 Timing Diagram (without stopping microprocessor during conversion).



t_{PCS} = 200ns min before falling edge of next to last φ2 clock pulse of instruction

t_{INT} = 12μsec (max)

MP21 Timing Diagram (using Interrupt).

OPERATING INSTRUCTIONS

PROGRAMMING

The MP21 is easily programmed since it is treated as memory. It uses any memory reference instruction that can read data.

The MP21 can be operated in four modes:

1) Start data conversion, halting the microprocessor for the 40μsec* conversion time. This is the simplest approach. It should be used if 40μsec of software time is available. (MP21's $\overline{\text{HALT}}$ line, pin 48, connected to the 6800's $\overline{\text{HALT}}$ input, pin 2.)

Example: LDA XXXX starts conversion of channel at location XXXX
NOP CPU halts at the end of this instruction
LDA XXXX transfers data from channel at location XXXX to accumulator

2) Start data conversion, then go to a different part of the program. When 40μsec* or more have passed, come back to the MP21 to read the converted data. This mode uses the least amount of time; it should be used when software time is at a minimum. (MP21's $\overline{\text{HALT}}$ line, pin 48, is open.)

Example: LDA XXXX starts conversion of the channel at location XXXX
•
•
• } at least 40μsec* of software here
LDA XXXX transfers data from channel at location XXXX to accumulator

* The conversion time of the MP21 may be between 40 and 200 microseconds depending upon the gain of the internal instrumentation amplifier. See Figure 4.

3) Start data conversion, then go to a different part of the program. Periodically, check the MP21's $\overline{\text{HALT}}$ line (pin 48) to detect if conversion is complete. This mode should

be used if a positive check of a complete conversion is needed. (MP21's $\overline{HALT}$ line, pin 48, could be interfaced to a 6820 PIA for instance.)

```
Example:  LDA $XXXX starts conversion of channel at
                   location XXXX
            •
            •      } other software
            •
          LDA $YYYY, loop to determine if conversion
                   is complete
       AA ANDA $ZZ } YYYY is location of 6820 PIA
                   with HALT information
                   ZZ is mask used for determin-
                   ing if end of conversion bit
                   is set
          BEQ AA
          LDA $XXXX transfers data from channel at
                   location XXXX to accumulator
```

4) Start conversion, then go to a different part of the program. The MP21 will interrupt at the end of conversion. The interrupt mode is very useful when the MP21 is at high gains with conversion times longer than 40μsec, see Figure 4.(MP21's $\overline{INT}$ line, pin 44, connected to the 6800's $\overline{IRQ}$ line, pin 4.)

Example: MP21 used with a 6800. MP21 base address 92E0. Processor halted operation. Read and Print the value of all 16 input channels and then stop.

```
                        NAM   MP21
      E0BF   OUT2H      EQU   $E0BF
      F1D1   OUTEEE     EQU   $E1D1
      E1AC   INEEE      EQU   $E1AC
0100                    ORG   $100
0100  CE 92E0 START     LDX   #$92E0   Base address for MP21
0103  5F               CLR B          Clear Counter
0104  A6 00   CONV      LDA A,X        Initiate Conversion
0106  01 01             NOP
0107  A6 00             LDA A, X       Read Data
0109  FF 0137           STX   STRE1    Store Index Reg.
010C  F7 0139           STA B STRE2    Store Counter
010F  B7 013B           STA A STRE3    Store Data
0112  CE 013B           LDX   #STRE3
0115  BD E0BF           JSR   OUT2H    Print Data
0118  86 0D             LDA A #$0D
011A  BD E1D1           JSR   OUTEEE
011D  86 0A             LDA A #$0A
011F  BD E1D1           JSR   OUTEEE
0122  F6 0139           LDA B STRE2
0125  FE 0137           LDX   STRE1
0128  5C                INC B          Next Channel
0129  C1 10             CMP B #$10     Have 16 channels been
                                       read?
012B  27 04             BEQ   STOP     Yes
012D  08                INX
012E  7E 0104           JMP   CONV     Do another conversion
0131  BD E1AC STOP      JSR   INEEE    Input character
                                       to begin again
0134  7E 0100           JMP   START
0137  0002     STRE1    RMB   2
0139  0001     STRE2    RMB   1
013A  0001     STRE3    RMB   1
                        END
```

This program assumes that the system is under the control of the MIK BUG monitor, Revision 9. To read and print the value of all 16 channels again, input any character from the keyboard.

ADDRESS SELECTION

The base address of the MP21 is set by inputs $\overline{A4}$ through $\overline{A13}$. Address lines A4 through A13 respond to the inverse of inputs $\overline{A4}$ through $\overline{A13}$. For instance, if $\overline{A6}$ is grounded, A6 will respond to a "High" input. A14 and A15 are internally connected to respond to a "High" input.

ANALOG INPUT RANGE SELECTION

The MP21 may be set for any range between ±5V and ±10 mV. Table I shows the pin connections for the various high level ranges available.

MP21 Input Range	Gain	ADC Range	Pin Connections
±5V	2	±10V	65 to 63; 66 open; 67 to 68
±2.5V	2	±5V	65 to 63; 66 to 68; 67 open
±1.25V	2	±2.5V	65 to 63; 66 to 68; 63 to 67
0 - 5V	2	0 - 10V	65 to 64; 66 to 68; 67 open
0 - 2.5V	2	0 - 5V	65 to 64; 66 to 68; 63 to 67

Table I. Analog Input Range Pin Connections

The MP21 may be set to output data with straight binary coding (pin 52 grounded) or two's complement coding (pin 52 to +5VDC through a 1kΩ resistor). Straight binary coding is typically used with unipolar input ranges and two's complement coding with bipolar input ranges. Table II describes the coding.

The internal instrumentation amplifier is factory set for a gain of 2. This gain can be increased to 250 by adding an external resistor (R_{ext}) between pins 1 and 3. R_{ext} should be a stable resistor (10 ppm/°C) since this temperature drift will add to the accuracy temperature coefficient. The gain of the amplifier can be determined by this formula:

$$\text{Gain} = 2 + \frac{50k\Omega}{R_{ext}}$$

. With pins 1 and 3 open, the gain is 2.

Since the amplifier input offset will be multiplied by the amplifier gain, an offset adjust may be required at high gains (see Figure 1b).

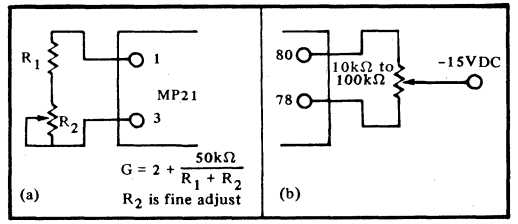


FIGURE 1. (a) MP21 Gain Adjust; (b) Offset Adjust

SINGLE-ENDED VS. DIFFERENTIAL INPUTS

The MP21 analog inputs may be connected as single-ended, differential or pseudo-differential. Single-ended operation may be used for high level (over one volt full scale) signals in low noise environments (Figure 3). Differential operation will reject common-mode noise appearing on both inputs (Figure 2). It should be used in noisy environments or with any low level signal (less than one volt). In the pseudo-differential mode, the MP21 is

	DIGITAL OUTPUT		ANALOG INPUT		
Straight Binary Code	Two's Complement Code		±5V	0 to +5V	±10mV
1111 1111 (FF_{16})	0111 1111 ($7F_{16}$)	+Full Scale	+4.961V	+4.980V	+9.92mV
1000 0000 (80_{16})	0000 0000 (00_{16})	Mid-Scale	0.000V	2.500V	0.000V
0000 0000 (00_{16})	1000 0000 (80_{16})	-Full Scale	-5.000V	0.000V	-10.00mV
		One LSB	39mV	19.5mV	78μV

TABLE II. Analog Input Values

connected as for the single-ended mode in Figure 3 except the IA low input, pin 79, is not grounded. Pin 79 is connected to an external ground that is common to all of the analog inputs. In cases with a noisy remote ground where little noise will be picked up between sensor and MP21, the pseudo-differential mode may be used.

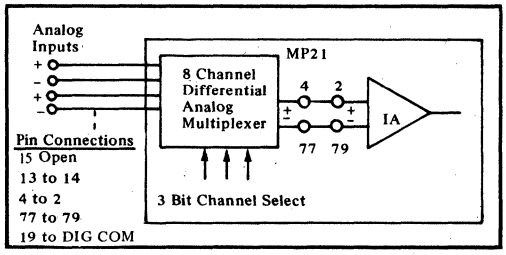


FIGURE 2. Differential Input Connections

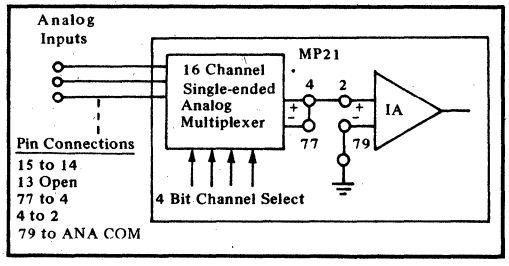


FIGURE 3. Single-ended Input Connections

DELAY TIMING

A delay time between channel selection and start of conversion is built into the MP21 to allow the analog multiplexer and instrumentation amplifier (IA) time to settle before starting the A/D converter. As the gain of the amplifier is increased, the settling time required increases. The factory set delay time (35μsec) is sufficient for gains of up to 10. At higher gains, a capacitor must be added from pin 49 to the +5 VDC supply to increase the delay time. Figure 4 shows the settling time of the MP21 vs. gain. Figure 5 shows the value of capacitance required to increase the delay.

The only external factor, other than gain, that affects the MP21 settling time is the impedance of the source connected to a channel. Figure 6 shows a circuit model of an "ON" channel.

The signal at the output of the multiplexer must be allowed to settle to ±0.1% (six time constants) to maintain the full accuracy of the system. The multiplexer time constant can be calculated with the formula: $\tau = (R_s + R_{on} + R_{on}^*)C_o$. For $R_s = 1k\Omega$ and $C_o = 50pF$, $\tau = (1.5+1)$ kΩ x 50pF = 125ns (single-ended operation). Thus 0.75μs is needed to settle to ±0.1%. For high input impedances requiring more than 10 microseconds for multiplexer settling time, the required delay time may be calculated with this formula: $T_D = \sqrt{T^2_{mux} + T^2_{IA}}$, where T_{mux} is the settling time of the multiplexer and T_{IA} is the settling time of the instrumentation amplifier as shown in Figure 4. If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large capacitance across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5μF is sufficient. For such a capacitance the multiplexer time constant becomes 80ns.

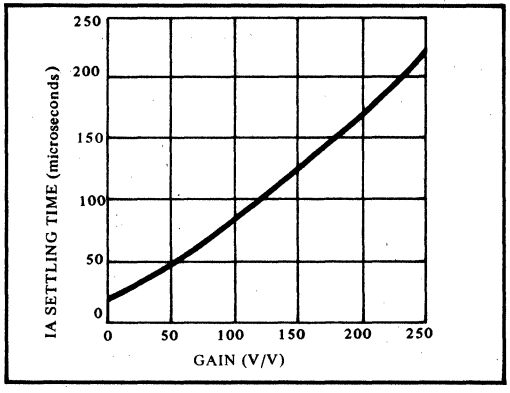


FIGURE 4. Typical IA Settling Time vs. Gain (Output Settling to ±0.1%).

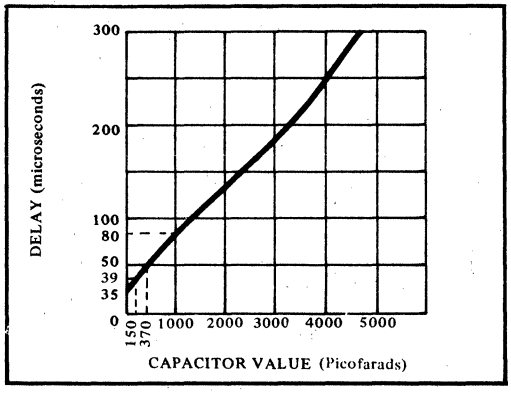


FIGURE 5. Typical Delay Time vs. Capacitor Value.

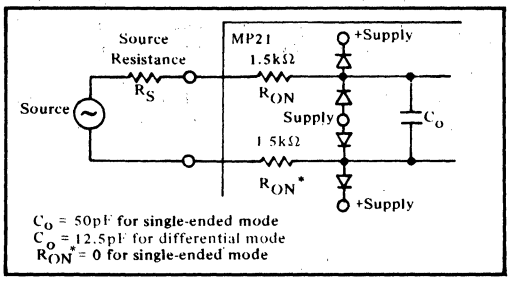


FIGURE 6. "ON" Channel Circuit Model.

INPUT OVERVOLTAGE PROTECTION

As shown in Figure 6, the analog inputs have reverse biased diode circuits which protect from damage by overvoltage (such as static). It is still advisable to take precautions against static discharge. The same circuitry protects the inputs from steady-state overvoltage damage during operation. The MP21's overvoltage protection can be increased by adding series resistors at each input. The input resistance must limit the current flowing through the input protection diodes to 10mA. For instance, if 15kΩ resistors are added to each input, the protection is increased to 165V (16.5kΩ x 10mA). Increased input resistance will, of course, increase the amount of time necessary for the multiplexer to settle as described in the previous section and increase the offset voltage by the drop caused when the bias current passes through this resistance.

NON 6800 OPERATION

The circuitry used to enable the 3-state output lines (D7 - D0) and begin conversion on the MP21 can be connected in such a way as to meet a wide variety of timing requirements. The output is enabled only when a valid address appears on the address inputs and when VMA (pin 45), R $\overline{W}$ (pin 42), and $\emptyset 2$ (pin 46) are high. Any other combination of digital signals on these lines will result in D7 - D0 being in a high impedance state (see Figure 7).

All that is required to use the MP21 with a system other than a 6800, is that these signals be brought to their active levels. When this occurs, operation begins as previously described. Applications using the MP21 with other processors are shown in Figure 10 and 11.

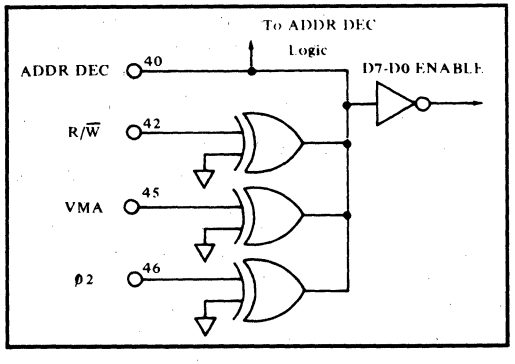


FIGURE 7. Output Enable Circuitry

RESET

It is important to reset the MP21 on startup with a low pulse on the $\overline{RESET}$ line (pin 47). The reset pulse clears an internal flip-flop and guarantees that the next read instruction to the unit will start a conversion. Thereafter, every other read instruction will initiate a conversion as previously described.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

HIGHER SPEED OPERATION

The MP21's internal instrumentation amplifier requires 35 microseconds to allow for settling time. If this internal amplifier is not used, substantial improvements in throughput rate can be obtained. This is easily done since neither the inputs nor the output of the instrument amplifier are internally connected. For instance, Burr-Brown's 3622 high speed instrument amplifier (for differential inputs) or 3505J high speed op amp (for single-ended inputs) may be used, with a settling time of 1μsec for gains of up to 100. The total delay time necessary may be calculated by this formula:

$$T_D = \sqrt{T^2_{MUX} + T^2_{IA}},$$

where T_{MUX} is the settling time of the multiplexer (750ns) and T_{IA} is the settling time of the instrument amplifier. For a T_{IA} of 1μsec we have T_D = 1.3μsec. Using 3μsec for the delay time to allow for unit to unit variation, the total throughput time will be 8μsec (including 5 microseconds for ADC conversion time) or 125 kHz. A resistor between pin 49 and +5 VDC will reduce the delay time from the factory set value of 35 microseconds (see Figure 8).

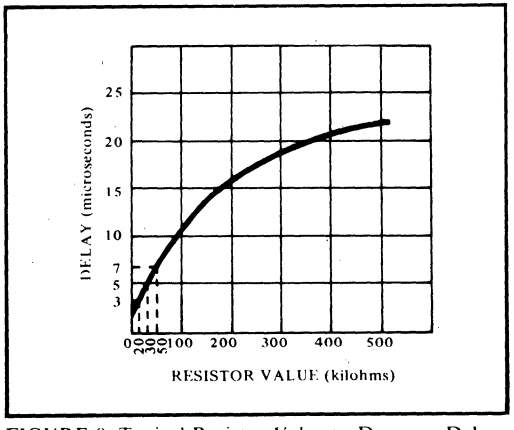


FIGURE 8. Typical Resistor Value to Decrease Delay Time.

CALIBRATION

The MP21 is laser trimmed at the factory to ±0.4% accuracy when using the ±5V, ±2.5V, ±1.25V, 0 to +2.5V or 0 to +5V ranges. If one of these ranges is used, no adjustments are required. For other ranges ($G \neq 2$), both the gain and offset must be adjusted. Figure 1 shows the adjustment connections. The offset adjustment should be made such that the transition to minus full scale output (0000 0001 to 0000 0000 for straight binary) occurs with an input of negative full scale plus 1/2 LSB. One least significant bit (LSB) is equal to the full scale range (FSR) divided by 2^n where n is the number of bits of the A/D converter. For the MP21, 1 LSB is $FSR/2^8 = FSR/256$. The gain adjustment should be made such that the transition to a full scale output (1111 1110 to 1111 1111 for straight binary) occurs with an input of positive full scale less 1/2 LSB. Since 128 states are used for negative inputs and one state is used for zero, only 127 states are available for the remaining positive range. Thus the positive full scale voltage is 1 LSB less than nominal full scale. For a range of ±50 mV, 1 LSB = 100 mV/256 = 0.39 mV. The gain adjustment should be made at +49.61mV* -(0.5)(0.39 mV) = +49.42 mV. The offset adjustment should be made at -50 mV + (0.5)(0.39mV) = -49.80 mV. Table III shows offset and gain calibration values for typical ranges.

* (50mV - 1 LSB = 49.61mV)

MP21 Input Range	Instrument Amp Gain	ADC Range	Calibration Values	
			Offset	Gain
±5V	2	±10V	-4.980V	+4.941V
0 to +5V	2	0 to +10V	+9.8mV	+4.971V
±2.5V	2	±5V	-2.490V	+2.471V
0 to +2.5V	2	0 to +5V	+4.9mV	+2.485V
±1.25V	2	±2.5V	-1.245V	+1.235
0 - 50mV	100	0 to +5V	+98μV	+49.7mV
±25mV	100	±2.5V	-24.9mV	+24.7mV
0 - 25mV	200	0 to +5V	+49μV	+24.9mV

Table III. Calibration Values.

The following program may be used to adjust gain and offset.

```
                    ORG  $100
START  0100  86     LDA A #$64
             64
       0102  B7     STA A COUNT
             01
             1A
       0105  4F     CLR A          Clear Accumulators.
       0106  5F     CLR B
CONV   0107  B6     LDA A $92 E0   Begin Conversion.
             92
             E0
       010A  01     NOP
       010B  B6     LDA A $92 E0   Read Data.
             92
             E0
       010E  81     CMP A #REF     Is Data = REF?
             REF
       0110  26     BNE AA         No. Do not count.
             01
       0112  5C     INC B          Yes. Do count.
AA     0113  7A     DEC COUNT      Have 100 conversions
                                    been done.
             01
             1A
       0116  26     BNE CONV       No. Do another.
             EF
       0118  20     BRA START      Yes. Begin next run.
             E6
COUNT  011A          RMB  1
                     END
```

This program assumes that the program is under control of the Motorola EXORciser EXbug monitor. If the Mikbug monitor is available, the following printout software may be added by using it to replace all codes starting from location 0118. In addition the references to count at 0104 and 0115 must be replaced with 2E.

```
OUT 2H  EQU  $E0   BF
OUT EEE EQU  $E1   D1

0118 F7     STA  B  STR0
     01
     2E
011B CE     LDX  #STR0
     01
     2E
011E BD     JSR  OUT 2H  Print no. of true conversions.
     E0
     BF
0121 86     LDA A  #0D
     0D
0123 BD     JSR  OUTEEE
     E1
     D1
012E        RMB  1          COUNT
012F        RMB  1          STR0
            END
```

This program may be used for both offset and gain calibration. The system offset should be adjusted first, followed by the gain adjustment.

The address of channel zero is assumed to be 92EO. If it is not, the LDA instructions should reflect that change. The reference values for Ref assume straight binary coding, Offset Ref = 00 and Gain Full Scale Ref = FF. For two's complement binary coding, Offset Ref = 80 and Gain Full Scale Ref = 7F.

A 100;G command to Exbug will begin program execution. For Mikbug the user's stack must be loaded with 1ØØ and then a G command executed to begin program execution. For those applications not using the printer portion of the program insert a breakpoint via a 118;V command. After 100 conversions have been made, the value (in hex) of the B accumulator will be printed if using Mikbug program. This value represents the number of times the data read from the board was equal to "REF" (00 for offset; FF for gain).

Calibration is performed by connecting a voltage source capable of 0.01% accuracy to input channel zero (this could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.01% DVM).

The offset adjustment is made first by using the appropriate offset calibration voltage and REF value. Run the calibration program and adjust the offset potentiometer until the B register contains a value between $1E_{16}$ and 46_{16} (30_{10} and 70_{10}).

To perform the gain adjustment, change the data labeled "REF" in the calibration program to its correct gain value. Set the input voltage to the correct value as shown in Figure 8 and adjust the gain potentiometer in the same manner as described for offset.

If EXbug is used the program will halt and the B accumulator can be examined from the program register display produced by the breakpoint.

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70μV/°C and operating ranges of minus hundreds to plus thousands of degrees centrigrade. When the MP21 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60 Hz or higher frequencies. When the MP21 is used as an eight channel differential input system, the high common-mode rejection of the instrument amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule, an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices cannot always be observed, a differential RC filter may be used. Figure 9 shows such a system.

The 10 kΩ resistors and 10μF capacitor provide low pass filtering (f_c = 0.8 Hz) while the optional 1 MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±5 volt range of the multiplexer. If the sensor is earth grounded, the 1MΩ resistors are not required. The 1 MΩ resistors do not enter into an error calculation for input errors because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias current of each input. See the overvoltage protection section for a discussion of the effects of the 10kΩ resistors in the input filter. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 9 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2 mV/°C.

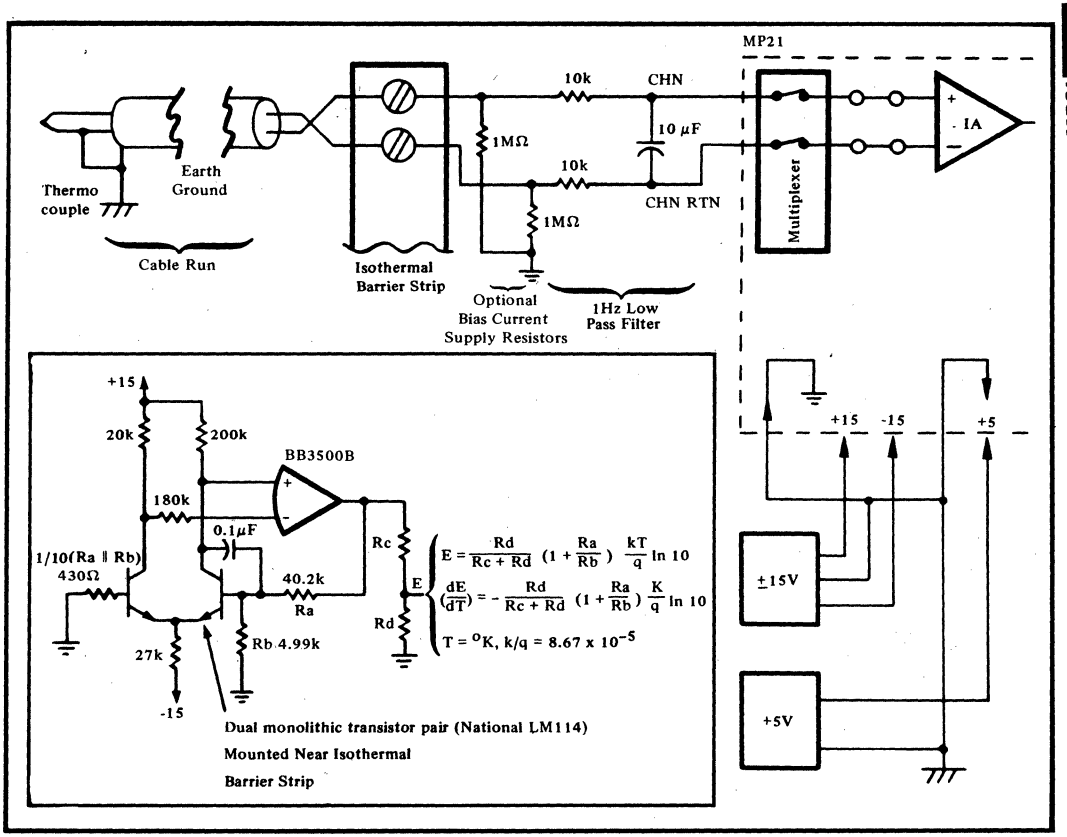


FIGURE 9. Thermocouple Input System Using MP21.

PIN CONNECTION SUMMARY

	JUMPER		JUMPER
Single-ended Multiplexer	4 to 2; 4 to 77; 79 to 64; 15 to 14; 13 open	Address Bus (A0 - A15)	Connect to 6800's address bus A0 - A15
Differential Multiplexer	4 to 2; 77 to 79; 13 to 14; 15 open	Address Select ($\overline{A4}$ - $\overline{A13}$)	Connect to +5V* or Ground
Amplifier	1 and 3 open for G = 2; R_{ext} between 1 and 3 for G ≠ 2.	Control Bus	42 to 6800's R/$\overline{W}$ (pin 39) 44 optionally to 6800's IRQ (pin 4) 45 to 6800's VMA (pin 5) 46 to 6800's Ø2 (pin 37) 47 to 6800's $\overline{RESET}$ (pin 40) 48 to 6800's $\overline{HALT}$ (pin 2) open for operation without halting CPU.
Input Range ±5V ±2.5V ±1.25V 0 - 5V 0 - 2.5V	 65 to 63; 66 open; 67 to 68 66 to 63; 66 to 68; 67 open 65 to 63; 66 to 68; 63 to 67 65 to 64; 66 to 68; 67 open 65 to 64; 66 to 68; 63 to 67		
Output Coding	52 to 51 for binary; 52 to 50* for two's complement.	Data Bus (D0 - D7)	Connect to 6800's data bus.

* Through a 1kΩ resistor.

MICROPROCESSOR INTERCONNECTION

The following diagrams show interconnections of the MP21 (described in this data sheet) and also of Burr-Brown's MP10 and MP11 analog output microperipherals (PDS-363) with Motorola's 6800, MOS Technology's 650X, and Fairchild's F-8. Although Burr-Brown's analog microperipherals are optimized for 8 bit microprocessors, with the addition of a few external components, they can be used with any 4 through 16 bit microprocessors.

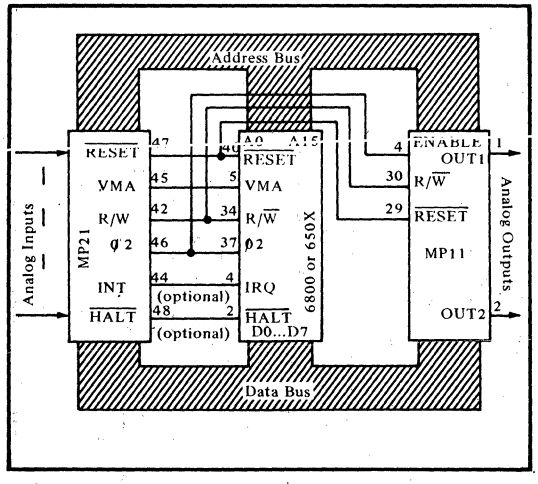


FIGURE 10. MP21 and MP11 Used With the 6800 or 650X.

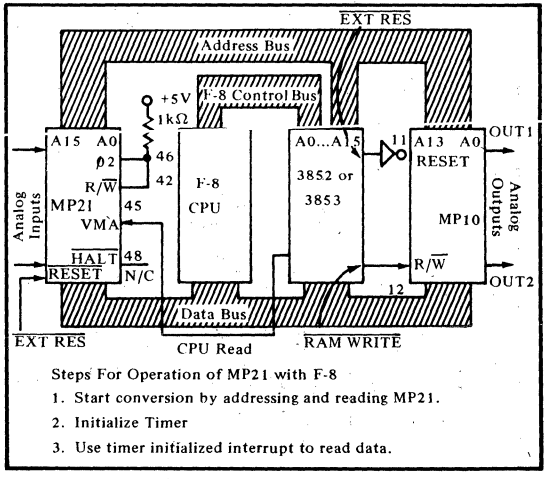
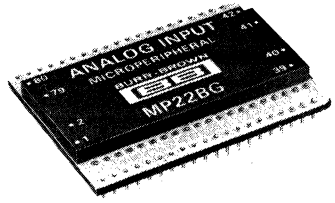


FIGURE 11. MP21 and MP10 Used With the F-8.

BURR-BROWN

MP22BG



Microprocessor-Interfaced 12-BIT DATA ACQUISITION SYSTEM

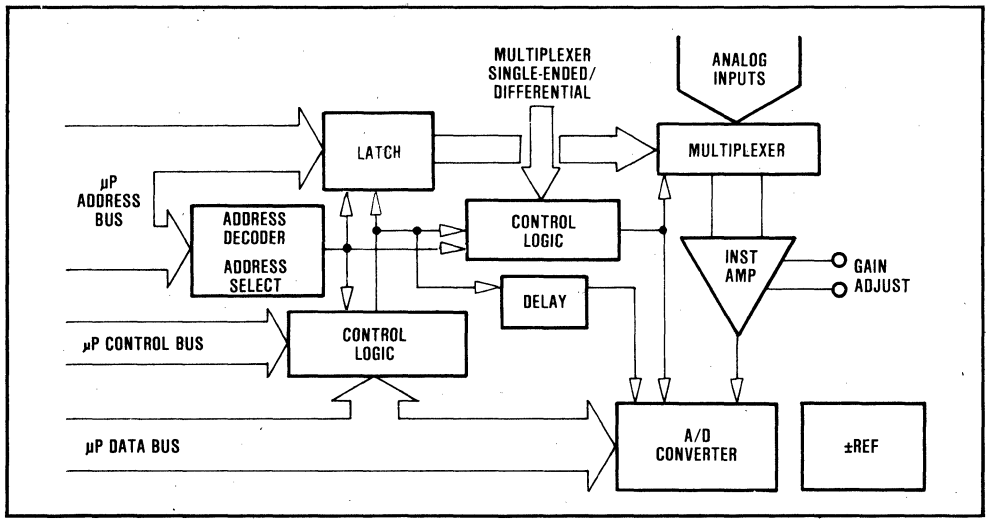
FEATURES

- **INTERFACES WITH 8080A, 8048, Z-80, SC/MP MICROPROCESSOR WITHOUT ADDITIONAL COMPONENTS**
- **INTERFACES WITH 6800, 650X, F8, 8085 MICROPROCESSORS WITH MINIMAL EXTERNAL LOGIC**
- **COMPATIBLE WITH PDP-8, PDP-11, NOVA, ECLIPSE MINICOMPUTERS**
- **EASY TO PROGRAM**
  - **One instruction acquires data as a memory mapped device**
  - **Two instructions acquire data as an accumulator I/O device**

DESCRIPTION

A complete analog input system, the MP22BG interfaces to many microprocessors without additional external components. Contained in an 80-pin quad-in-line package, it includes a 12-bit CMOS A D converter, instrumentation amplifier, input multiplexer that accepts up to 16 single-ended signals or 8 differential signals, an address decoder, and control logic. Logic to generate interrupt, halt, and direct memory access request signals is also included.

The system can digitize low-level or high-level analog signals. Gain of the internal instrumentation amplifier can be programmed with a single external resistor allowing input ranges as low as ±10mV.



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ANALOG MULTIPLEXERS

Two 8-channel CMOS analog multiplexers are used on the input which permits selection of 16 single-ended or 8 differential inputs. A pseudo 16 channel differential mode of operation can also be achieved by connecting the amplifier's inverting input to a common, remote signal ground. Channels are addressed by the address decoder which is connected directly to the microprocessor address bus. The number of input channels can be expanded without limit using external multiplexers.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity and gain programming with an external resistor. Gain may be selected from unity to 500.

ANALOG-TO-DIGITAL CONVERTER

The 12-bit A/D converter is a CMOS, successive approximation device with 45μsec conversion time and three-state outputs. Laser-trimmed, compatible thin-film networks are used to assure linearity and stability over wide temperature ranges.

ADDRESS DECODER

Typical microprocessor systems have several thousand memory locations, teletype or CRT terminals, and possibly several MP22s. By using 12 address lines the microprocessor can communicate with as many as 2^{12} or 4096 memory locations or peripheral devices, with each having its own unique address.

The MP22's address decoder is made up of exclusive-or gates which have open collector outputs so that the outputs of several gates may be connected together through a single pull-up resistor. The address of the MP22 is determined by wiring the address select lines to either ground or +5 volts. Only when all of the address lines (A inputs) are in opposite states of their respective address select lines ($\overline{A}$ inputs) will the address decoder output go high.

DELAY TIMER

A time delay between channel selection and start of conversion is built into the MP22. This allows the analog multiplexer and the instrumentation amplifier time to settle before starting the A/D converter. As amplifier gain increases, settling time increases. See Figure 8. Factory set delay time (15μsec) is sufficient for gains from unity to 50. At higher gains a capacitor must be added between pins 49 and 50 to increase delay. Figure 7 indicates the capacitance required to increase delay time.

CONTROL LOGIC

The control logic generates signals to halt or interrupt the CPU while conversion takes place and to signal the CPU when conversion is complete and data can be read. Enable signals are also generated to gate the data onto the data bus.

REFERENCE

The internal voltage reference of the MP22 has been optimized for stable outputs with respect to temperature. Output current up to 2mA can be drawn externally from the reference outputs.

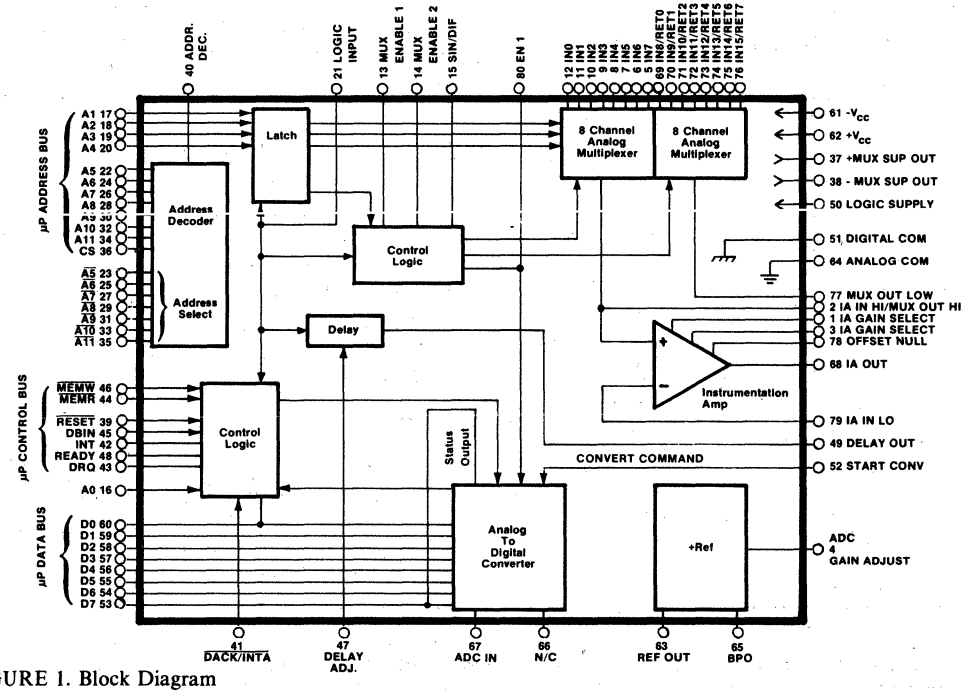
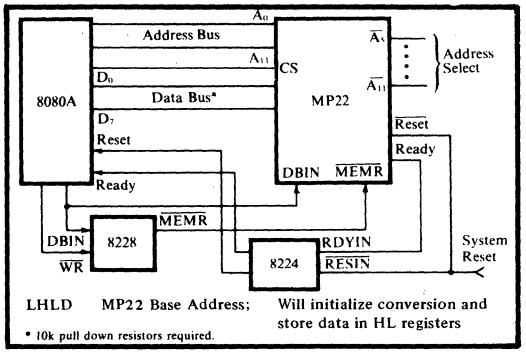


FIGURE 1. Block Diagram

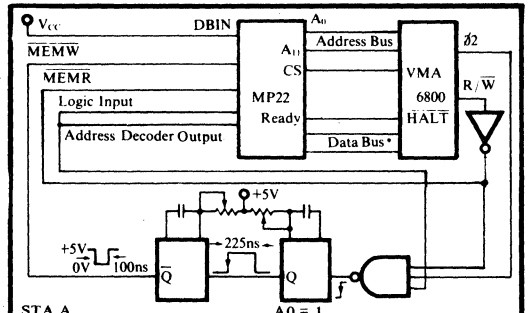
MICROPROCESSOR CONNECTION DIAGRAMS



LHLD MP22 Base Address; Will initialize conversion and store data in HL registers

* 10k pull down resistors required.

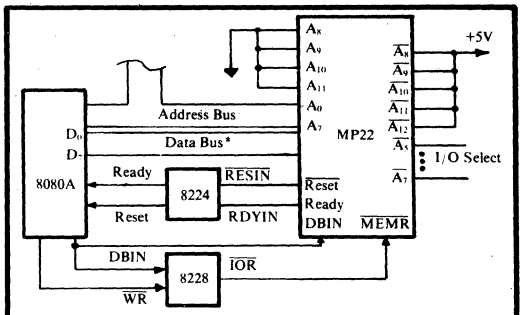
FIGURE 2. MP22 Used with 8080 Halt Mode Memory Mapped



STA A	A0 = 1	
Destination Address	D0 = 0	Starts conversion
NOP		Halt
LDA		
Destination Address	A0 = 0	8 LSB's, Resets MP22
LDA		
Destination Address	A0 = 1	4 MSB's

* 10k pull down resistors required.

FIGURE 3. MP22 Used with 6800



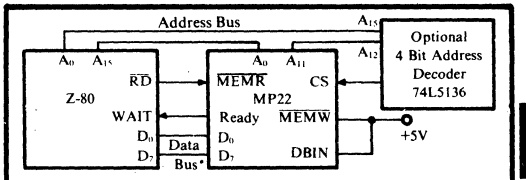
IN MP22 Base Address; $A_0 = 0$ A_1 - A_4 channel select A_5 - A_7 I/O select initializes conversion and reads 8 LSB's

MOV C, A Store 8 LSB's in REG C

IN MP22 Base Address; $A_0 = 1$ A_5 - A_7 I/O select reads 4 MSB's

* 10k pull down resistors required.

FIGURE 4. MP22 Used with 8080 Halt Mode Accumulator I/O



Program to READ and STORE 16 channels of data using Block Transfer Instruction.

LD HL, NN	NN points to channel 0 MP22
LD DE, MM	MM points to the first location of the destination
LD BC, 0100_H	byte counter (2 bytes/channel x 16) = 32_{10}
LDI	Load and increment

Total Execution Time with tcy = .4μs and conversion rate 40μs is T = 3 (4μs) + 16 (6.4 + 40μs) = 754.4μs.

* 10k pull down resistors required.

FIGURE 5. MP22 Used with Z-80 (Halt Mode)

MP22

DELAY TIME COMPONENT SELECTION CURVES

FIGURE 6. Typical Resistor Value to Decrease Delay Time

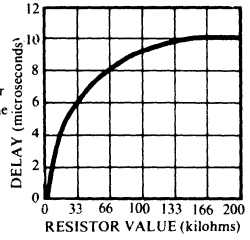
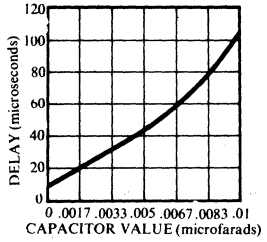


FIGURE 7. Typical Delay Time vs Capacitor Value



TYPICAL PERFORMANCE CURVES

FIGURE 8. Differential Amplifier Settling Time vs Gain

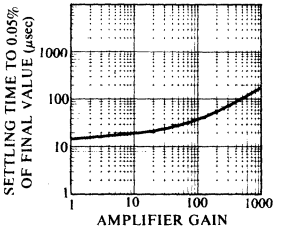
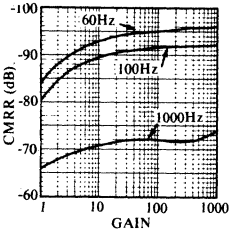


FIGURE 9. Differential Amplifier Common-mode Rejection vs Gain



ELECTRICAL SPECIFICATIONS

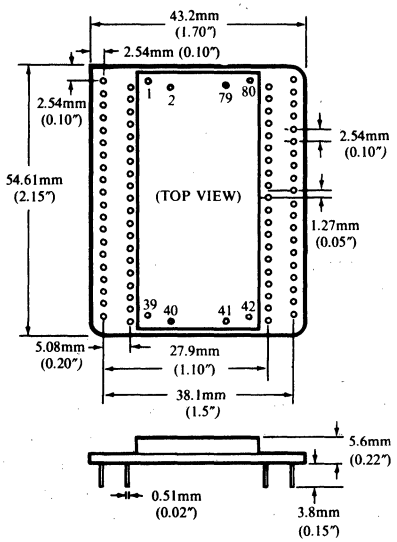
Typical at +25°C and rated supplies unless otherwise noted.

MODEL	MP22BG Min	MP22BG Typ	MP22BG Max	Units
TRANSFER CHARACTERISTICS				
Resolution[1]	12	12	12	Bits
Number of Channels		16 Single-Ended/8 Differential		
Throughput Rate[1] at G = 1	40	45	55	µs/Channel
ANALOG INPUTS				
ADC Gain Ranges				
Bipolar[3]		±5		Volts
Unipolar[1]		0-5		Volts
Amplifier Gain Range		1 to 500		
Gain Equation		$\left(1+\frac{25k\Omega}{R_{EXT}}\right)$		
Input Voltage Without Damage			±16	Volts
Input Voltage for Multiplexer Operation			±6.0	Volts
Input Impedance				
Off Channel		5 x $10^9\Omega$ || 10pF		
On Channel		5 x $10^9\Omega$ || 100pF		
Bias Current				
25°C			300	nA
0°C to +70°C			400	nA
Amplifier Output Noise G = 100, R_S = 150Ω		1.2		mV, rms
		7.0		mV, p-p
Amplifier Input Offset		±0.5	±7.0	mV
Amplifier Offset Drift (R_{max} = 1.5k)		±(7 + 90/G)	±(26 +190/G)	µV/°C
Amplifier Gain Drift, (R_{EXT} ≤10 ppm/°C)				
G = 1			10	ppm/°C
G = 10			110	ppm/°C
G = 100			120	ppm/°C
G = 1000			120	ppm/°C
Amplifier Settling Time to ±0.05% of FSR				
G = 1[1]			15	µs
G = 10		20		µs
G = 100		25		µs
G = 500		100		µs
CMRR for Differential Inputs Dc to 60Hz	74	84		dB
ACCURACY				
System RSS Accuracy[2] at 25kHz Throughput				
G = 1			±0.1	% FSR
Linearity			±0.05	% FSR
Differential Linearity		±0.05		% FSR
Gain Error		Adjustable to Zero		
Offset Error		Adjustable to Zero		
System RSS Accuracy at Gain = 500 and 1kHz Throughput			±0.39	% FSR
ADC Accuracy Drift				
Linearity			±3	ppm/°C
Gain			±10	ppm/°C
Reference Drift				
Ref Out (Pin 63)			±15	ppm/°C
BPO (Pin 65)			±25	ppm/°C
System Accuracy Drift (Excluding I.A.)				
Unipolar			±25	ppm/°C
Bipolar			±60	ppm/°C
Monotonicity (-25 to +85°C)		Guaranteed		
No Missing Codes (-25 to +85°C) (10 bits only)		Guaranteed		
Power Supply Sensitivity (Excluding I.A.)				
±V_{CC}			±0.008	% FSR/%ΔV
Logic Supply			±0.0002	% FSR/%ΔV
Instrumentation amplifier				
Power Supply Sensitivity			$(1+2/G)10^{-4}$	% FSR/%ΔV

MODEL	MP22BG			Units
	Min	Typ	Max	
DIGITAL INPUT/OUTPUT				
Bipolar Code		Bipolar Offset Binary		
Unipolar Code		Unipolar Straight Binary		
Logic Loading Pin (21)			3LSTTL	
Pin (60)			2LSTTL	
Output Drive	1 TTL Load			
Analog Input Channels Selected By:		A1-A4		
Output Data:		D0-D7		
POWER REQUIREMENTS				
Rated Voltages[1]		±15, +5		Volts
Range for Rated Accuracy (Logic Supply, $\pm V_{cc}$)		4.75 to 5.25 and ±11.4 to ±15.75		Volts
$\pm V_{cc}$ Operating Range	±10		±18	Volts
Supply Drain				
$+V_{cc}$		10	20	mA
$-V_{cc}$		15	20	mA
Logic Supply		80	160	mA
Power Dissipation ($\pm V_{cc}$ = ±12V)		700	1300	mW
TEMPERATURE RANGE				
Specification	-25		+85	°C
Operating	-40		+100	°C
Storage	-55		+125	°C

NOTES: 1. These parameters are 100% tested.
2. Gain and offset adjusted to zero.
3. External amplifier required.

MECHANICAL



MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz.)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20 pin strips)
HERMETICITY: Fluorocarbon (gross leak)

PIN CONNECTIONS

Pin		Pin	
1	IA GAIN SELECT	41	$\overline{\text{DACK/INTA}}$
2	IA IN HI/MUX OUT HIGH	42	INT
3	IA GAIN SELECT	43	$\overline{\text{DRQ}}$
4	ADC GAIN ADJUST	44	$\overline{\text{MEMR}}$
5	IN7	45	$\overline{\text{DBIN}}$
6	IN6	46	$\overline{\text{MEMW}}$
7	IN5	47	DELAY ADJ.
8	IN4	48	READY
9	IN3	49	DELAY OUTPUT
10	IN2	50	+5V LOGIC SUPPLY
11	IN1	51	DIG. COMMON
12	IN0	52	START CONV.
13	MUX ENABLE 1	53	D7 (MSB)
14	MUX ENABLE 2	54	D6
15	SIN/DIF	55	D5
16	A0	56	D4
17	A1	57	D3
18	A2	58	D2
19	A3	59	D1
20	A4	60	D0 (LSB)
21	LOGIC INPUT	61	$-V_{cc}$
22	$\overline{\text{A5}}$	62	$+V_{cc}$
23	A5	63	REF OUT
24	$\overline{\text{A6}}$	64	ANA. COMMON
25	A6	65	BPO
26	$\overline{\text{A7}}$	66	NO CONNECTION
27	A7	67	ADC IN
28	$\overline{\text{A8}}$	68	IA OUT
29	A8	69	IN8 RET0
30	$\overline{\text{A9}}$	70	IN9 RET1
31	A9	71	IN10 RET2
32	$\overline{\text{A10}}$	72	IN11 RET3
33	A10	73	IN12 RET4
34	$\overline{\text{A11}}$	74	IN13 RET5
35	A11	75	IN14 RET6
36	CHIP SELECT (CS)	76	IN15 RET7
37	+MUX SUPPLY OUTPUT	77	MUX OUT LOW
38	-MUX SUPPLY OUTPUT	78	OFFSET NULL
39	$\overline{\text{RESET}}$	79	IA IN LO
40	ADDR DECODE	80	EN1

OPERATING INSTRUCTIONS

The MP22 is designed to be used as a memory-mapped or an accumulator I/O. Since there are many powerful memory reference instructions, the MP22 is used most efficiently as a memory-mapped device. Pins $\overline{A5}$ through $\overline{A11}$ are provided so that the microperipheral can be hardwired for any base address within a 4096 word block of the memory field. The address decoder output is available and can be easily expanded to 16 bits.

If used as a memory-mapped microperipheral, the MP22 can provide three modes of operation: HALT Mode, INTERRUPT Mode and DMA Mode.

More detailed application instructions are given in the operating manual, available upon request.

HALT MODE

After power up (or manual) reset, the MP22 is automatically set for operation in the HALT Mode. This mode requires minimum software to acquire data. To use the MP22 in the HALT Mode connect the MP22 READY line to the 8080 READY input (see Figure 2). When a memory reference instruction such as LHLD is executed, the READY line goes low, halting the CPU for the duration of the data conversion (45 μsec, gain = 1). When the conversion is complete the READY line goes high, signaling the CPU exit the wait state and enter the T_3 state to read the 8 LSB's. After reading the 8 LSB's, the CPU increments the memory address register and reads the 4 MSB's. When the most significant data byte has been read, the internal logic resets and the MP22 is ready for the next conversion.

Example:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	1	1	1	1	1	0	1	1	1	0	0	1	0
			MP22 Base Address								Channel Select				

MP22 used with 8080; read MP22 base address: $1F72_H$ channel 10.

LHLD $1F72_H$ acquires and transfers data to CPU from channel 10.

The 8 LSB's (at location $1F72_H$) are transferred to register L and the 4 MSB's (at location $1F73_H$) are transferred to register H.

Total time: 16 tcy + 40μsec = 47.8μsec (for tcy = 488 nsec [8080A]).

INTERRUPT MODE

To use the MP22 in the INTERRUPT Mode connect the INT and $\overline{DACK}/\overline{INTA}$ lines to the 8080's INT input and INTA output respectively. Conversion is initiated by writing D0 = 0 into the MP22. When the conversion is complete the MP22 generates an INT signal which will remain low until INTA is received from the 8080.

Example: MP22 base address $1F72_H$.

```
MVIA   00H                 START conversion
STA    1F72H
 .
 .                         Continue with program. INT will
 .                         arrive 40 μsec after start of conversion.
INCA
                           INT arrives here
CPIA                       User will jam RST instruction which
                           will provide address of an interrupt handling routine and store program counter.
INTERRUPT Subroutine:
       PUSH PSW            Store Acc. and Flags
       PUSH H  }
       PUSH D  }           Store reg. if necessary
       PUSH B  }
       EI                  Enable interrupt
       LHLD 1F72H          READ DATA from MP22
                           Channel 10 L = 8 LSB's
                                      H = 4 MSB's
                           Process data
       POP B   }
       POP D   }           Restore registers and flags
       POP H   }
       POP PSW             Restore program counter
       RET
```

The user must supply an instruction op code to the processor during the next DBIN time after the $\overline{INTA}$ status appears. This is usually done through use of an RST instruction.

DIRECT MEMORY ACCESS MODE

To use the MP22 in the DMA Mode connect the MP22 to the DMA controller. The controller is initialized by the CPU before reading data from the MP22. To accomplish a block move the CPU loads the 8257 with the starting address of the source block (the MP22 location) with A0 = 0 and the length of the block (L = 1) into channel 0. Channel 1 is programmed with the starting location of the destination block and the length (L = 1).

Next, start conversion by writing D0 = 0 into the MP22. When the conversion is complete, the MP22 will generate a DRQ request on channels 0 and 1. The 8257 is initialized to the rotating priority mode, therefore the first DMA cycle is from channel 0 which latches data from the first location of the source block into the 8212. The second cycle will be from channel 1 which will store the latched data in the first location of the destination block. The next cycle will return to channel 0 and the sequence will start over again until the terminal count is reached. When the terminal count for channel 1 is reached, $\overline{DACK1}$ and TC signals are generated and MP22 DRQ line is reset.

ANALOG INPUT RANGE SELECTION

The MP22 may be set for any range between ±5V and ±10mV. Pin connections for the high level ranges available are shown in Table I.

MP22 Input Range	Gain	ADC Range	Pin Connections
±5V	1	±5V	See bipolar operation
0 - 5V	1	0-5V	65, 63 open; connect 67 to 68

TABLE I. Analog Input Range Pin Connections

In the unipolar mode the MP22 output data is straight binary. In the bipolar mode it is bipolar offset binary. If two's complement output is needed an external three-state inverting buffer is required.

Gain of the internal instrumentation amplifier (without external gain adjust) is 1.0. This gain can be increased to any value between 1.0 and 500 by adding an external resistor between pins 1 and 3. This external resistor (R) should be stable (10 ppm/°C or better) because its drift will add to the system accuracy temperature coefficient. Gain of the amplifier is determined by this formula:

External resistor R_{ext} connected: Gain = $1 + 25k\Omega / R_{ext}$

Pins 1 and 3 open: Gain = 1.0 ±0.02%

OPERATION WITH BIPOLAR INPUT VOLTAGES

To operate the MP22 with bipolar input voltages of ±5V, connect the unit as shown in Figure 10. Amplifier A1 divides the magnitude of the input by two, and the connection of a 12.5kΩ resistor between pin 63 (ref out) and pin 78 (offset null) offsets the signal such that the A/D converter sees a unipolar voltage from 0 to +5V.

To null the gain and offset errors of this circuit, follow this procedure:

1. Input - 5.0000V to any MP22 channel.
2. Adjust R1 until a digital output of all zeros is obtained.
3. Input +4.99817V to that MP22 channel.
4. Adjust R2 until a digital output of $0FFF_H$ is obtained.

POWER SUPPLY CONSIDERATIONS

For best performance and noise rejection, power supplies should be decoupled with 1.0μf tantalum or electrolytic capacitors in parallel with 0.01μF ceramic capacitors. To insure proper power supply sequencing, a diode should be connected between the pins 50 and 62 with the anode connected to pin 50.

A 0.1μF ceramic capacitor is required on each of the lines +MUX SUPPLY OUT (pin 37) and -MUX SUPPLY OUT (pin 38). Each is tied from the respective pin to ground.

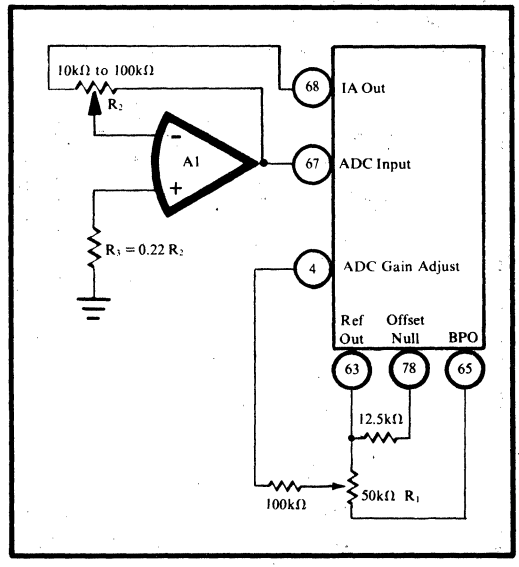


FIGURE 10. Connection for ±5V Input

	ANALOG INPUT			DIGITAL OUTPUT		
	±5V	0 to +5V	±5mV	OFFSET BINARY	STRAIGHT BINARY	TWO'S COMPLEMENT
+Full Scale	4.9975V	4.9988 V	4.9975 mV	FFF_H	FFF_H	$7FF_H$
Mid Scale	0.0000V	2.5000 V	0.0000	800_H	800_H	000_H
-Full Scale	-5.0000V	0.0000 V	-5.0000 mV	000_H	000_H	800_H
One LSB	2.44mV	1.22mV	2.44μV			

TABLE II. Analog Input, Digital Output Relationship

DATA ACQUISITION FROM THERMOCOUPLE INPUTS

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70μV/°C and operating ranges of minus hundreds to plus thousands of degrees centrigrade. When the MP22 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60 Hz or higher frequencies. When the MP22 is used as an eight channel differential input system, the high common-mode rejection of the instrument amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule, an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices cannot always be observed, a differential RC filter may be used. Figure 11 shows such a system.

The 10 kΩ resistors and 10μF capacitor provide low pass filtering (f_c = 0.8 Hz) while the optional 1 MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±5 volt range of the multiplexer. If the sensor is earth grounded, the 1MΩ resistors are not required. The 1 MΩ resistors do not enter into an error calculation for input errors, because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias currents of the two inputs. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 11 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2 mV/°C.

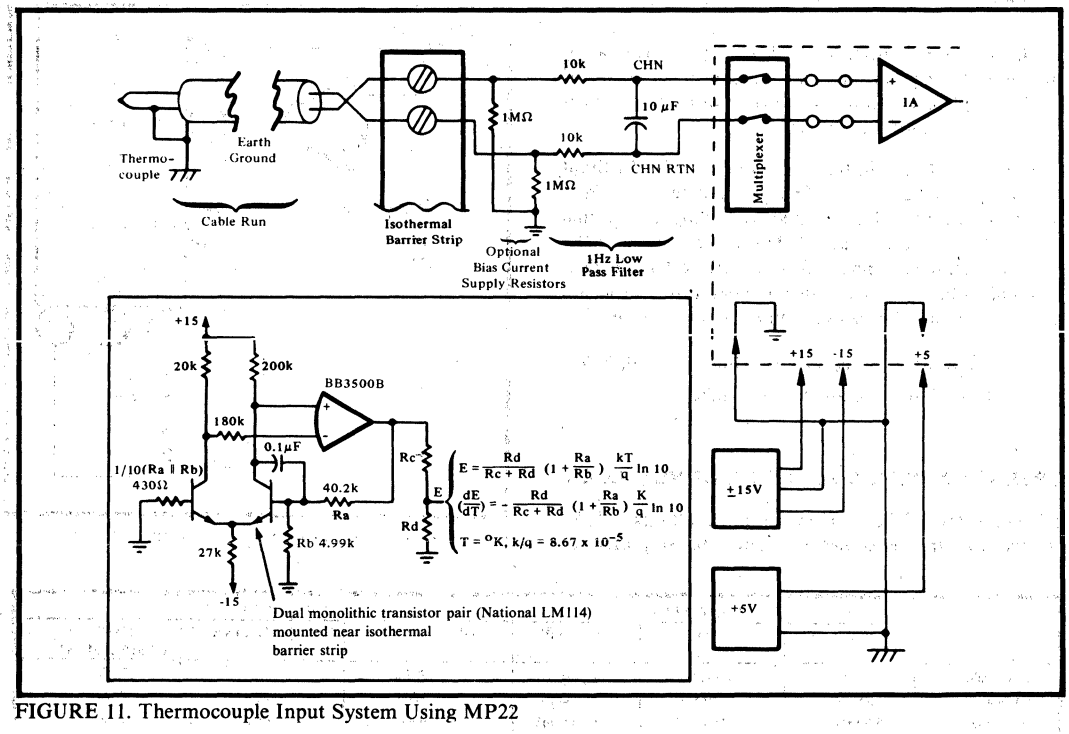


FIGURE 11. Thermocouple Input System Using MP22

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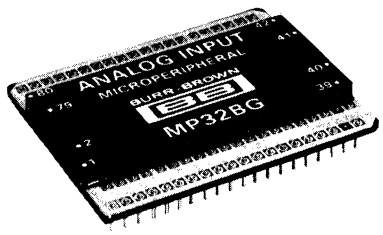


MP32

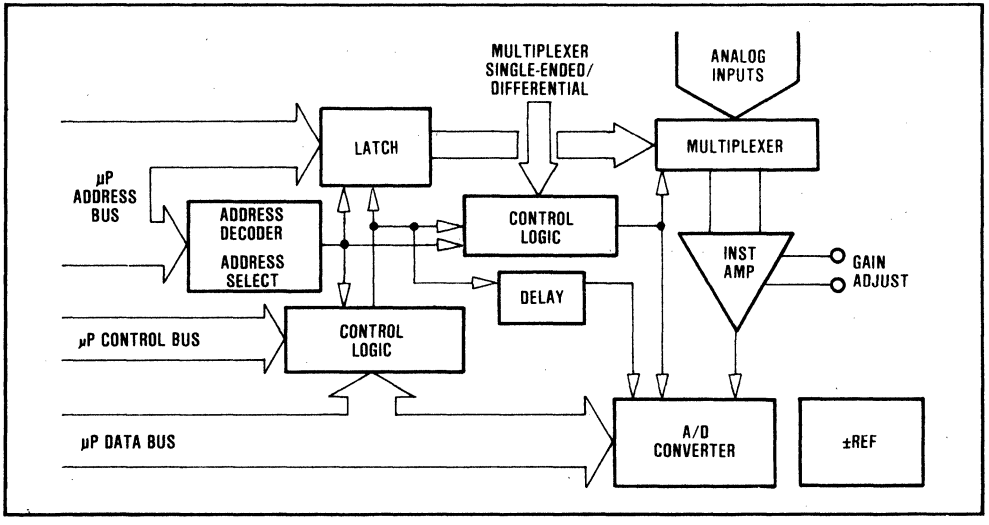
Microprocessor-Interfaced 12-BIT DATA ACQUISITION SYSTEM

FEATURES

- INTERFACES WITH 8080A, 8048, Z-80, SC/MP MICROPROCESSOR WITHOUT ADDITIONAL COMPONENTS
- INTERFACES WITH 6800, 650X, F8, 8085 MICROPROCESSORS WITH MINIMAL EXTERNAL LOGIC
- COMPATIBLE WITH PDP-8, PDP-11, NOVA, ECLIPSE MINICOMPUTERS
- EASY TO PROGRAM
  - One instruction acquires data as a memory-mapped device
  - Two instructions acquire data as an accumulator I/O device

DESCRIPTION

The MP32 is a complete analog input system and interfaces to many microprocessors without additional external components. Contained in an 80-pin quad-in-line package, it includes a 12-bit CMOS A/D converter, instrumentation amplifier, input multiplexer that accepts up to 16 single-ended signals or 8 differential signals, an addess decoder, and control logic. Logic to generate interrupt, halt, and direct memory access request signals is also included. The system can digitize low level or high level analog signals. Gain of the internal instrumentation amplifier can be programmed with a single external resistor allowing input ranges as low as ±10mV.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION (CONT)

ANALOG MULTIPLEXERS

Two 8-channel CMOS analog multiplexers are used on the input which permits selection of 16 single-ended or 8 differential inputs. A 16-channel pseudo-differential mode of operation can also be achieved by connecting the amplifier's inverting input to a common, remote signal ground. Channels are addressed by the address decoder which is connected directly to the microprocessor address bus. The number of input channels can be expanded without limit using external multiplexers.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity and gain programming with an external resistor. Gain may be selected from unity to 500.

ANALOG-TO-DIGITAL CONVERTER

The 12-bit A/D converter is a CMOS, successive approximation device with 40μsec conversion time and three-state outputs. Laser-trimmed, compatible thin-film networks are used to assure linearity and stability over wide temperature ranges.

ADDRESS DECODER

The 12-bit address decoder has been included in the MP32 so the device can be uniquely specified within 4k bands of the address field. If further decoding is required, the chip select (CS) pin can provide a 13th bit or the output of an external decoder can be connected to the internal address decoder output "wired-AND" node.

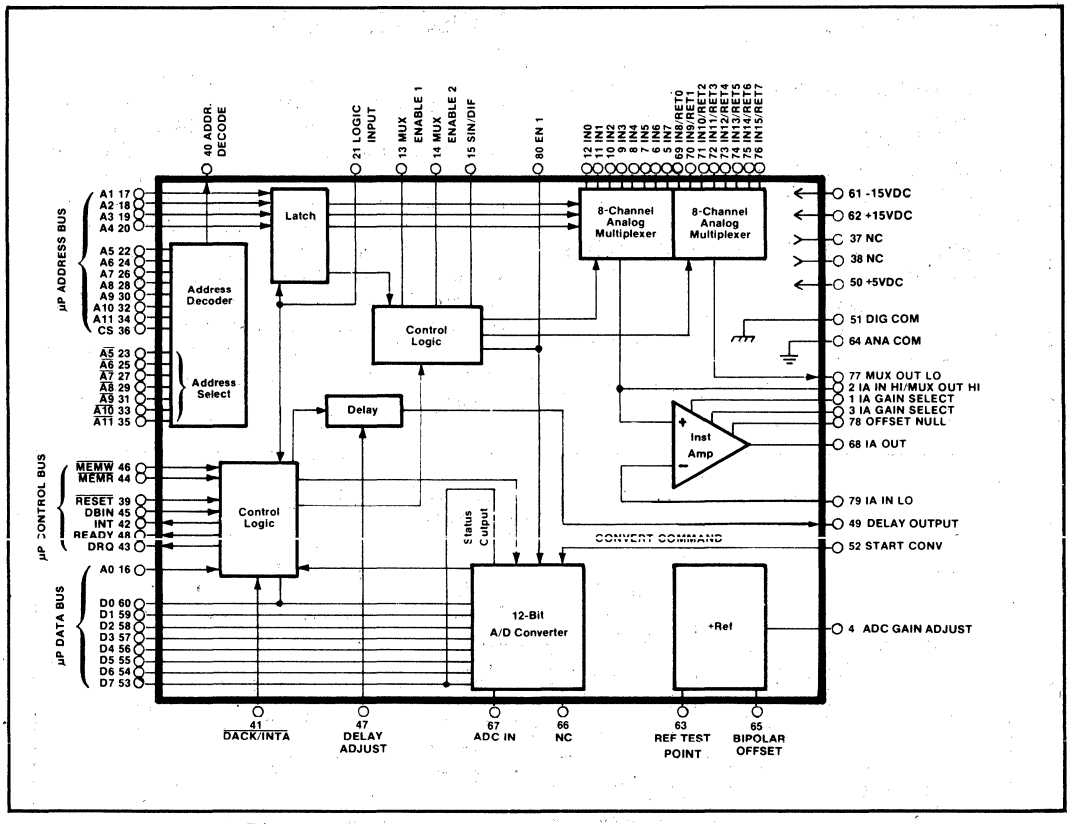


FIGURE 1. System Block Diagram.

DELAY TIMER

A time delay between channel selection and start of conversion is built into the MP32 and is described in detail in the Analog Input Configuration section.

CONTROL LOGIC

The control logic generates signals to halt or interrupt the CPU while conversion takes place and to signal the CPU when conversion is complete and data can be read. Enable signals are also generated to gate the data onto the data bus.

REFERENCE

The internal voltage reference of the MP32 has been optimized for stable outputs with respect to temperature. Output current up to 2mA can be drawn externally from the reference outputs.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated supplies unless otherwise noted.

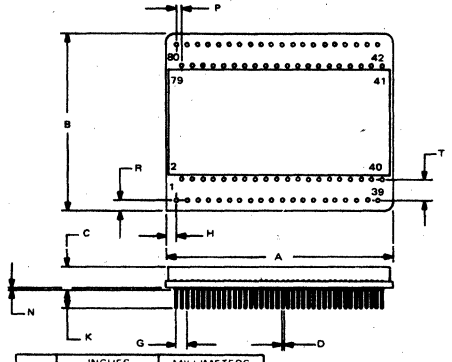
MODEL	MP32BG AND MP32CG MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS				
Resolution(1)	12	12	12	Bits
Number of Channels		16 Single-ended/8 Differential		
Throughput Rate(1) at G = 1	50	70	80	µsec/Channel
ANALOG INPUT/OUTPUT				
ADC Voltage Input Ranges(2)				
Bipolar(3)		±10		V
Unipolar(1)		0 to +10		V
Amplifier Gain Range		1 to 500		V/V
Gain Equation		1 + (25kΩ/R_{EXT})		
Input Voltage Without Damage			±35	V
Input Voltage for Multiplexer Operation			±10	V
Input Impedance				
Off Channel			10^{18}	Ω
On Channel		1.5	1.8	kΩ
Bias Current				
+25°C			300	nA
0°C to +70°C			400	nA
Amplifier Output Noise G = 100, R_S = 1500Ω		1.2		mV, rms
		7.0		mV, p-p
Amplifier Input Offset		±0.5	±7.0	mV
Amplifier Input Offset Drift (R_{source} = 1.5kΩ max)		±|7 + (90/G)|	±|26 + (190/G)|	µV/°C
Amplifier Gain Drift, (R_{EXT} ≤ 10ppm/°C)				
G = 1			±10	ppm/°C
G = 10			±110	ppm/°C
G = 100			±120	ppm/°C
G = 500			±120	ppm/°C
Amplifier Settling Time to ±0.01% of FSR				
G = 1(1)			15	µsec
G = 10		20		µsec
G = 100		25		µsec
G = 500		100		µsec
CMRR for Differential Inputs DC to 60Hz	80	84		dB
Instrumentation Amplifier				
Power Supply Sensitivity			|1 + (2/G)| 10^{-4}	% FSR/%ΔV
ACCURACY				
System RSS Accuracy(4) at 25kHz Throughput				
G = 1, BG			±0.05	
CG			±0.025	
Linearity, BG			±0.025	% FSR
CG			±0.0125	% FSR
Differential Linearity, BG		±0.025		% FSR
CG		±0.0125		% FSR
Gain Error		Adjustable to Zero		
Offset Error		Adjustable to Zero		
System RSS Accuracy at 1kHz Throughput				
G = 500			±0.39	%FSR
ADC Accuracy Drift				
Linearity			±3	ppm/°C
Gain			±10	ppm/°
Reference Drift				
Ref Out (Pin 63)			±15	ppm/°C
Bipolar Offset (Pin 65)			±25	ppm/°C
System Accuracy Drift (Excluding IA)				
Unipolar			±25	ppm/°C
Bipolar			±60	ppm/°C
No Missing Codes (-25°C to +85°C)(Bits 1 thru 12)CG		Guaranteed		
(Bits 1 thru 11)BG		Guaranteed		

ELECTRICAL (CONT)

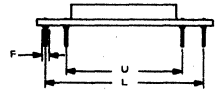
MODEL	MP32BG AND MP32CG			
	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (Excluding IA)				
±15VDC			±0.008	% FSR/%ΔV
+5VDC			±0.0002	% FSR/%ΔV
DIGITAL INPUT/OUTPUT				
Biopolar Code		Bipolar Offset Binary		
Unipolar Code		Unipolar Straight Binary		
Logic Loading Pin (21)			3LSTTL	
Logic Loading Pin (60)			2LSTTL	
All Other Digital Inputs			1LSTTL	
Output Drive	1TTL Load			
Analog Input Channels Selected By:		A1-A4		
Output Data		D0-D7		
POWER REQUIREMENTS				
Rated Power Supply Voltages(1)		±15, +5		VDC
Power Supply Ranges for Rated Accuracy		+4.75 to +5.25 and ±11.4 to ±15.75		VDC
Power Supply Operating Range (±15VDC only)	±10		±18	VDC
Supply Drain				
+15VDC		10	20	mA
-15VDC		15	20	mA
+5VDC		80	160	mA
Power Dissipation (at rated supplies)		700	1300	mW
TEMPERATURE RANGE				
Specification	-25		+85	°C
Operating	-40		+100	°C
Storage	-55		+125	°C

NOTES:
1. These parameters are 100% tested. 2. Input voltage must be kept 2V below supply voltage. 3. External amplifier required. 4. Gain and offset adjust to zero.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	



NOTE:
LEADS IN TRUE POSITION WITHIN 0.015" 0.38mm R@ MMC AT SEATING PLANE.

Pin numbers shown for reference only. Numbers may not be marked on package.

MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz.)
MATING CONNECTOR: 2350MC (set of four 20 pin strips)

PIN ASSIGNMENTS

	Pin	No.	
IA GAIN SELECT	1	41	$\overline{\text{DACK/INTA}}$
IA IN HI/MUX OUT HI	2	42	INT
IA GAIN SELECT	3	43	$\overline{\text{DRQ}}$
ADC GAIN ADJUST	4	44	$\overline{\text{MEMR}}$
IN7	5	45	$\overline{\text{DBIN}}$
IN6	6	46	$\overline{\text{MEMW}}$
IN5	7	47	DELAY ADJUST
IN4	8	48	READY
IN3	9	49	DELAY OUTPUT
IN2	10	50	+5VDC
IN1	11	51	DIG COM
IN0	12	52	START CONV
MUX ENABLE 1	13	53	D7 MSB
MUX ENABLE 2	14	54	D6
SIN/DIF	15	55	D5
A0	16	56	D4
A1	17	57	D3
A2	18	58	D2
A3	19	59	D1
A4	20	60	D0 LSB
LOGIC INPUT	21	61	-15VDC
$\overline{\text{A5}}$	22	62	+15VDC
A5	23	63	REF TEST POINT
$\overline{\text{A6}}$	24	64	ANA COM
A6	25	65	BIPOLAR OFFSET
$\overline{\text{A7}}$	26	66	NC
A7	27	67	ADC IN
$\overline{\text{A8}}$	28	68	IA OUT
A8	29	69	IN8/RET0
$\overline{\text{A9}}$	30	70	IN9/RET1
A9	31	71	IN10/RET2
$\overline{\text{A10}}$	32	72	IN11/RET3
A10	33	73	IN12/RET4
$\overline{\text{A11}}$	34	74	IN13/RET5
A11	35	75	IN14/RET6
CHIP SELECT CS	36	76	IN15/RET7
NC	37	77	MUX OUT LO
$\overline{\text{NC}}$	38	78	OFFSET NULL
$\overline{\text{RESET}}$	39	79	IA IN LO
ADDR DECODE	40	80	EN1

DESCRIPTION OF PIN FUNCTIONS

NUMBER	DESIGNATION	DESCRIPTION
Pins 1 and 3	IA GAIN SELECT	(Optional). By connecting a resistor between pins 1 and 3, the gain of the internal instrumentation amplifier can be varied as follows: Gain = 1 + (25kΩ/R) where R is the gain setting resistor. Gain can be set from 1 to 500. Important: If a gain greater than 50 is required, an external capacitor must be connected from DELAY ADJUST (pin 47) to +5VDC (pin 50). This increases an internal delay to allow for the increased settling time required by the instrumentation amplifier.
Pin 2	IA IN/ HI MUX OUT HI	This is the positive input of the internal instrumentation amplifier, and the "high side" of the multiplexer. For differential operation this pin is left open. For single-ended operation connect pin 2 to pin 77 and pin 79 to pin 64.
Pin 4	ADC GAIN ADJUST	This pin is used to adjust gain of the ADC (see Figures 6 and 7). If no external gain adjustment is needed, this pin is left open.
Pins 5 thru 12	IN7-IN0	The first 8 (of 16) analog inputs for single-ended operation or the 8 positive inputs for 8-channel differential input operation.
Pin 13	MUX ENABLE 1	Leave open for single-ended operation. Connect to MUX ENABLE 2 (pin 14) for differential input operation.
Pin 14	MUX ENABLE 2	Connect to SIN/ DIF (pin 15) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.
Pin 15	SIN/ DIF	Connect to MUX ENABLE 2 (pin 14) for single-ended operation. Leave open for differential input operation.
Pin 16	A0	In the Halt Mode A0 = "0" and $\overline{\text{MEMR}}$ = "0" will start conversion and enable 8LSB's; A0 = "1" enables 4MSB's. At the start of conversion, the output registers are not cleared.
Pins 17 thru 20	A1-A4	Address lines that select one of 16 analog input signals (IN0-IN15). 0000 selects channel 0 and 1111 selects channel 15 when the correct address is presented to the MP32. A4 is connected to DIG COM (pin 51) for differential operation.
Pin 21	LOGIC INPUT	Connect to pin 40. See signal description under pin 40.
Pins 22,24,26, 28, 30, 32, 34, 36	A5-A11, CS	Address lines. When the proper address is presented to the MP32, the internal logic is enabled for conversion or data output. CS is used as a chip select or the most significant address bit. It must be "1" to enable the unit.
Pins 23, 25, 27, 29, 31, 33, 35	$\overline{\text{A5-A11}}$	Address select lines. These lines are used to program the address decoder to respond to a particular address. This is done by connecting these pins to +5VDC or ground such that the bit pattern is the complement of the desired address that appears on the corresponding bit lines.
Pin 37	NC	No connection.
Pin 38	NC	No connection.
Pin 39	$\overline{\text{RESET}}$	A "low" on this line is required to RESET the MP32. Connect to system reset line.
Pin 40	ADDR DECODE	A positive pulse will appear when a valid address appears on the MP32 address lines. This pin is usually connected to LOGIC INPUT (pin 21). The rising edge of this pulse strobes the input channel select information (A1-A4) into an internal latch. It can also be used by the user for other system timing.
Pin 41	$\overline{\text{DACK/INTA}}$	In the Interrupt Mode, this pin is connected to the microprocessor interrupt acknowledge pin. This is an active low signal. If not used, connect to +5VDC through a 1kΩ resistor.
Pin 42	INT	In the Interrupt Mode, this signal is connected to the microcomputer system interrupt. Once the conversion is completed the MP32 generates an INT signal which will remain high until an $\overline{\text{INTA}}$ signal is received from the microcomputer. This is an open-collector LSTTL signal and must be pulled up with an external resistor.
Pin 43	DRQ	In the DMA Mode, this pin is connected to the direct memory access request line of the microcomputer system. Once conversion is complete, the MP32 will generate a DRQ signal which will remain high until $\overline{\text{DACK}}$ is received.
Pin 44	$\overline{\text{MEMR}}$	Memory read. A "low" pulse on this line is used to start a conversion in the Halt Mode. If not used, connect to +5VDC through a 1kΩ resistor.
Pin 45	DBIN	Connect the DBIN on 8080A. If used with any other microprocessor, connect through 1kΩ resistor to +5VDC.
Pin 46	$\overline{\text{MEMW}}$	Memory write. A "low" pulse on this line along with D0 = 0 will start conversion in the Interrupt or DMA Modes provided that LOGIC INPUT (pin 21) is "1". If not used, connect to +5VDC through a 1kΩ resistor.
Pin 47	DELAY ADJUST	When the IA is operated with gain greater than 50, the delay time must be increased (see Figure 11) to allow for the increased settling time of the IA.
Pin 48	READY	In the Halt Mode connect this output signal to the input that will cause the microprocessor to enter the "Wait" state (such as the READY input on the 8080). A logic "0" causes the microprocessor to halt to allow time for the analog circuitry to settle and the conversion to be completed (70μsec with gain ≤ 50). After conversion, the READY line will return to logic "1" which releases the microprocessor from the "Wait" state. The output data then appears on the data bus.
Pin 49	DELAY OUTPUT	When the MP32 is addressed, an internal delay of approximately 15μsec is initiated to allow for multiplexer and instrumentation amplifier settling time. Pin 49 must be connected to START CONV (pin 52). This point may be connected to a sample/ hold control input if an external S/ H is used.
Pin 50	+5VDC	+5VDC at 160mA, max.
Pin 51	DIG COM	Digital commmon. This pin should be connected to ANA COM (pin 64) as close to the MP32 as possible for optimum performance.
Pin 52	START CONV	This pin should be connected to DELAY OUTPUT (pin 49).
Pins 53 thru 60	D7-D0	8-bit data bus. Tri-state low power Schottky TTL-compatible.
Pin 61	-15VDC	-15VDC at 20mA, max.
Pin 62	+15VDC	+15VDC at 20mA, max.
Pin 63	REF TEST POINT	Test point for reference testing.
Pin 64	ANA COM	Analog common. This should be connected to DIG COM (pin 51) as close to the MP32 as possible for optimum performance.
Pin 65	BIPOLAR OFFSET	+10VDC voltage reference output. 2mA can be supplied from this pin without degradation.

DESCRIPTION OF PIN FUNCTIONS (CONT)

NUMBER	DESIGNATION	DESCRIPTION
Pin 66	NC	No connection.
Pin 67	ADC IN	A/D converter input. Connect to IA OUT (pin 68). If external S/H used, connect to S/H output.
Pin 68	IA OUT	Instrumentation amplifier output. Connect to ADC IN (pin 67) for normal operation. If external S/H used, connect to S/H input.
Pins 69 thru 76	IN8/RET0 -IN15/RET7	Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
Pin 77	MUX OUT LO	Multiplexer output for IN8/RET0 - IN15/RET7. Connect to IA IN HI/MUX OUT HI (pin 2) for single-ended input operation or connect to IA IN LO (pin 79) for differential input operation.
Pin 78	OFFSET NULL	Instrumentation amplifier offset adjust (see Figures 5, 6, and 7).
Pin 79	IA IN LO	Negative input of the instrumentation amplifier. Connect to ANA COM (pin 64) for single-ended input operation or MUX OUT LO (pin 77) for differential input operation.
Pin 80	EN1	Output signal which enables 4MSB's. See Figure 14 for utilization to obtain two's complement. For a straight binary output this pin is left open.

OPERATING INSTRUCTIONS

ADDRESSING MODES

In the memory-mapped addressing mode, the MP32 is regarded as a block of memory locations, each with its own unique address. Since the output data word is 12 bits long, it requires two address locations for each word.

The MP32 is connected to the microprocessor just as though it were memory, using the memory control lines. The address word format is illustrated in Figure 2. Address bits A5 through A12 (A12 is connected to CS, or CS can be used as a chip select) identify a particular MP32 unit. The bit pattern of A5 through A12 is selected by the user by connecting inputs $\overline{A5}$ through $\overline{A12}$ to logic 1 or logic 0. A1 through A4 select the particular analog input channel. A0 is used as a byte select (see Description of Pin Functions). The byte select bit is sequenced as specified in the discussion on operational modes. The advantage of using memory-mapped addressing is the flexibility of programming. All of the many memory reference instructions can be used to control MP32 operation.

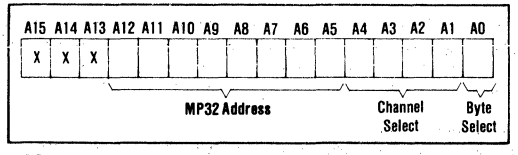


FIGURE 2. Address Word Format

Input/Output Addressing

Input/output addressing is accomplished by considering the MP32 as an input/output or peripheral device. Thus the I/O control signals are used to operate the unit. The addressing scheme is the same as that described in the Memory-Mapped Addressing section. The user may be forced to use I/O addressing if all of the available memory addresses have been taken up with memory or other memory-mapped devices.

Address Expansion

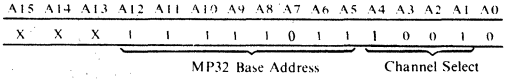
The 8-bit MP32 base address (A5 through A11 and CS) enables one of 256 bands of locations in the address field. The top 3 bits of the 16-bit microprocessor address bus are not used by the MP32. If it is necessary to expand the addressing capability to include these 3 additional bits, the output of an external 3-bit address decoder can be used in conjunction with the ADDR DECODE signal output of the MP32, to provide the LOGIC INPUT signal required by the MP32.

OPERATIONAL MODES (Memory-Mapped)

Halt Mode

After powerup (or manual) reset, the MP32 is automatically set for operation in the Halt Mode. This mode requires minimum software to acquire data. To use the MP32 in the Halt Mode connect the MP32 READY line to the 8080 READY input (see Figure 15). When a memory reference instruction such as LHLD is executed, the READY line goes low, halting the CPU for the duration of the data conversion (50μsec, gain = 1). When the conversion is complete the READY line goes high, signaling the CPU to exit the wait state and enter the T_3 state to read the 8LSB's. After reading the 8LSB's, the CPU increments the memory address register and reads the 4MSB's. When the most significant data byte has been read the internal logic resets and the MP32 is ready for the next conversion.

Example:



MP32 used with 8080; read MP32 base address: 1F72H channel 9.
LHD 1F72H acquires and transfers data to CPU from channel 9.
The 8LSB's (at location 1F72H) are transferred to register L and the 4MSB's (at location 1F73H) are transferred to register H.
Total time: 16tcy + 50μsec = 57.8μsec (for tcy = 488nsec 8080 A)

Interrupt Mode

To use the MP32 in the Interrupt Mode connect the INT and DACK/INTA lines to the 8080's INT input and

$\overline{\text{INTA}}$ output respectively (see Figure 16). Conversion is initiated by writing D0 = into the MP32. When the conversion is complete the MP32 generates an INT signal which will remain low until $\overline{\text{INTA}}$ is received from the 8080.

Example: MP32 base address 1F72H

```
MVI A,0H    00H
STA         1F72H       START conversion
.
.                       Continue with program. INT will
.                       arrive 50μsec after start of conversion.
.                       INT arrives here
                        User will generate RST instruction
.                       (usually done with an 8227) which
.                       will provide the address of an
.                       interrupt handling routine and store
                        program counter.
INTERRUPT Handler:
    PUSH PSW            Store acc. and flags
    PUSH H  }
    PUSH D  }           Store reg. if necessary
    PUSH B  }
    EI                  Enable interrupt
    LHLD 1F72H          READ DATA from MP32
                        Channel 10 L = 8LSB's
                                   H = 4MSB's
                        Process data
    POP B   }
    POP D   }           Restore registers and flags
    POP H   }
    POP PSW             Restore program counter
    RET
```

Polled Mode

The electrical connections for the Polled Mode are the same as that for the Halt Mode, except that the MP32 READY line is not connected.

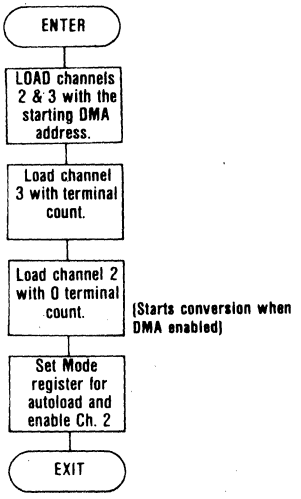
Programming in the Polled Mode is also similar to that of the Halt Mode except that after starting the conversion with a memory reference instruction, the program continues to run. After sufficient time has elapsed for the completion of the conversion, the most significant data byte is read. If the MSB is set, the conversion is still in progress. When it has been determined that the conversion has been completed, the least significant, and then the most significant data bytes are read. Reading of the data will begin a new conversion which may either be ignored or it can access the next analog channel of interest. In either case, the data from the first conversion will not be affected.

Direct Memory Access Mode

Data from the MP32 can be updated automatically and stored in a dedicated part of system memory by using the Direct Memory Access (DMA) mode of operation. Figure 3 illustrates the DMA connection for an 8080 microprocessor. Since the MP32 address decoder is not needed for this mode of operation it can be used to provide address selection for the DMA controller (model 8257). This interface is designed to operate on the I/O bus.

The following program can be used to operate the DMA interface. Any number of adjacent MP32 channels can be cycled repeatedly by inserting the desired memory starting address and the terminal count into the program.

Programming For DMA Operation




```
ENTER:  MVI A, XX   :Load Channel 2 with DMA Starting Address
        OUT X4H
        MVI A, YY
        OUT X4H
        MVI A, XX   :Load Channel 3 with DMA Starting Address
        OUT X6H
        MVI A, YY
        OUT X6H
        MVI A, XX   :Load Channel 3 with Terminal Count
        OUT X7H
        MVI A, 0
        OUT X7H
        MVI A, 0    :Load Channel 2 with 0 Terminal Count
        OUT X5H
        MVI A, 0
        OUT X5H
        MVI A, 84H  :Set Mode Reg. for Autoload and enable Channel 2
        OUT X8H
```

The interface is designed to always start on analog input channel 0. The interface requires one pass through all channels to intialize. The data put in memory through this initial pass will most likely be erroneous and should be disregarded.

OPERATIONAL MODES (Input/Output)

Each memory-mapped operational mode can also be used on the I/O bus. When used with the I/O bus the appropriate address lines and timing signals (i.e., $\overline{\text{I/OR}}$ instead of $\overline{\text{MEMR}}$) must be applied. In addition, the appropriate READ and WRITE instructions must be used. For the 8080 this would mean substituting the following sequence for LHLD XXXXH:

```
IN XXH
MOV L, A
IN XX+1H
MOV H, A
```

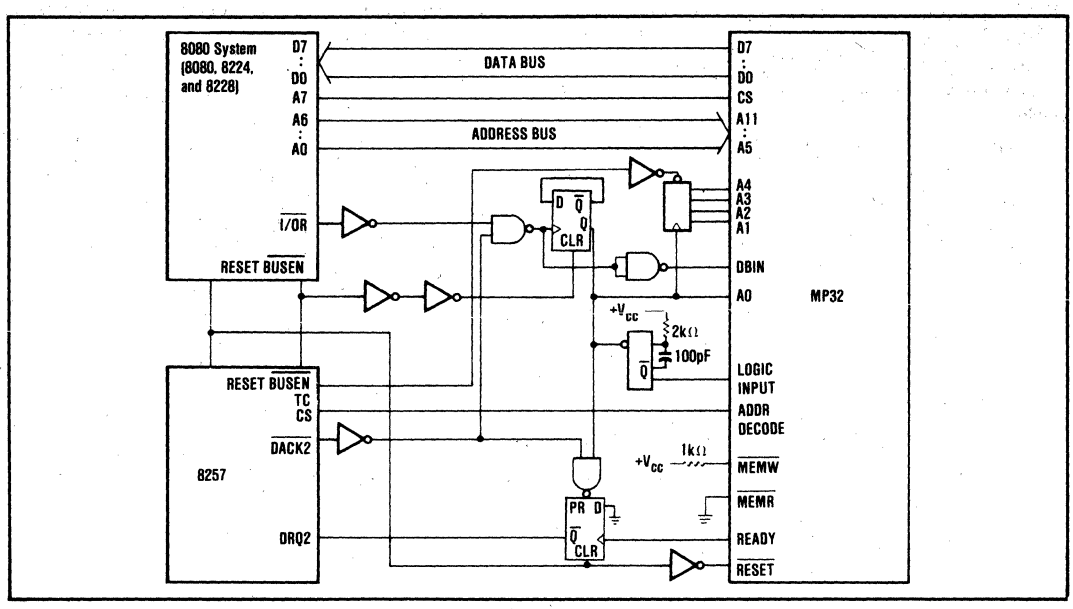


FIGURE 3. MP32 / 8080 Connection for DMA Operation (I/O Mapped).

TIMING

The internal timing diagram and timing constraints of the MP32 are shown in Figure 4 and Table I. The MP32 is compatible with any digital system that can operate within the timing constraints shown.

ANALOG INPUT CONFIGURATION

UNIPOLAR AND BIPOLAR OPERATION

The MP32 will convert either unipolar or bipolar voltage inputs. Unipolar input ranges vary from +10mV to +10V (full scale). Bipolar ranges are from ±10mV to ±10V. For bipolar input signal ranges from ±5V to ±10V, an external amplifier is used to divide the input signal by 2 and an offset is introduced to give a 0 to +5V input to the ADC. Use the connection diagram shown in Figure 5. For bipolar input signal ranges of ±5V down to ±10mV, the external amplifier is not used. Use the connection diagram shown in Figure 6.

TABLE I. MP32BG/CG Timing Diagram Parameters.

Symbol	Parameter	Min	Max	Unit
t_{ad}	Delay - Valid Addr. to Addr. Decoder Out		30	nsec
t_T	Delay - $\overline{MEMW}$ to DELAY Out		128	nsec
t_T	Delay - $\overline{MEMR}$ to DELAY Out		98	nsec
t_{delay}	Analog Settling Time	1	1000	µsec
t_R	Delay - DELAY to READY Out		52	nsec
$t_{conversion}$	Total Channel Conversion Time	45	55	µsec
t_D	Delay - End of Conversion to DRQ		25	nsec
t_I	Delay - End of Conversion to INT		70	nsec
t_{Da}	Delay - $\overline{DACK/INTA}$ to DRQ Out		60	nsec
t_{Ia}	Delay - $\overline{DACK/INTA}$ to INT Out		75	nsec

The unipolar input connection diagram is shown in Figure 7. Table II gives a summary of circuit configurations for several input ranges.

TABLE II. Analog Input Configurations.

Input Range	IA Gain	Circuit Configuration	Delay Adjust Required
±10V	1	Figure 5	No
±7.5V	1.33	Figure 5	No
±5V	1	Figure 6	No
±1.0V	5	Figure 6	No
±100mV	25	Figure 6	No
±20mV	250	Figure 6	Yes
0 to +10V	1	Figure 7	No
0 to +5V	2	Figure 7	No
0 to +20mV	500	Figure 7	Yes

INSTRUMENTATION AMPLIFIER GAIN SELECTION

The internal instrumentation amplifier gain may be set to any value between 1 and 500 by connecting an external gain resistor between pins 1 and 3. With the pins open the gain is 1 ±0.02%. The gain of the amplifier is determined by: $G = 1 + (25k\Omega/R_{ext})$, where R_{ext} is the gain resistor value. The external resistor should be stable (10ppm/°C or beter) since its drift will add to the gain temperature coefficient.

SINGLE-ENDED VERSUS DIFFERENTIAL INPUTS

The MP32 analog inputs may be connected in single-ended, differential, or pseudo-differential configurations. Single-ended operation may be used for high level (over 1V full scale) signals in low noise environments (see Figure 8). Differential operation will reject common-mode noise that appears on both inputs (see Figure 9). It should be used in noisy environments or with any low level signal (less than 1V). In the pseudo-differential mode, the MP32 is connected the same as single-ended

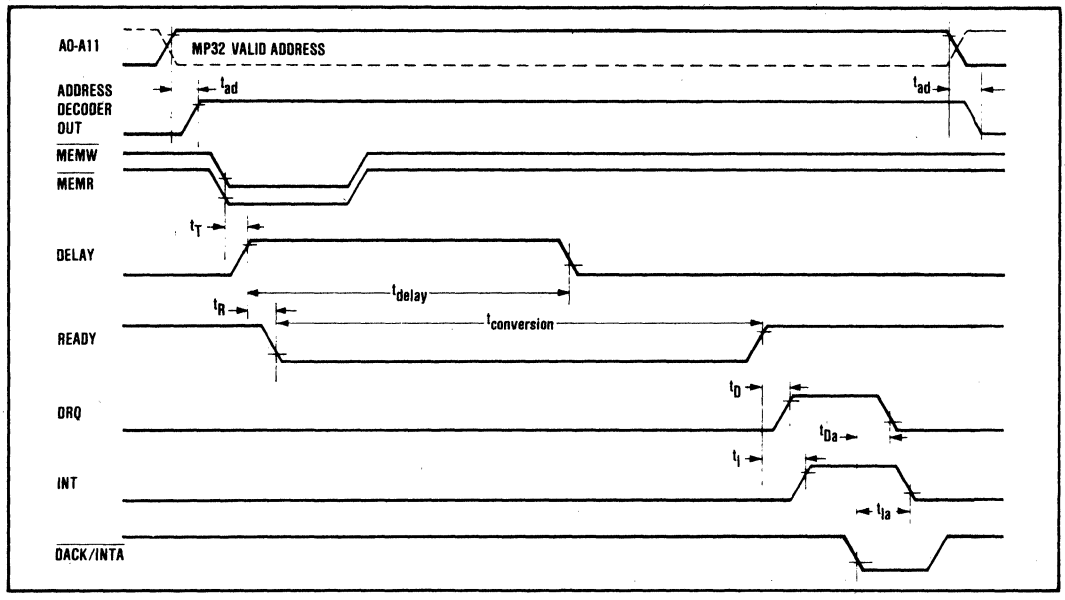


FIGURE 4. MP32 Timing Diagram.

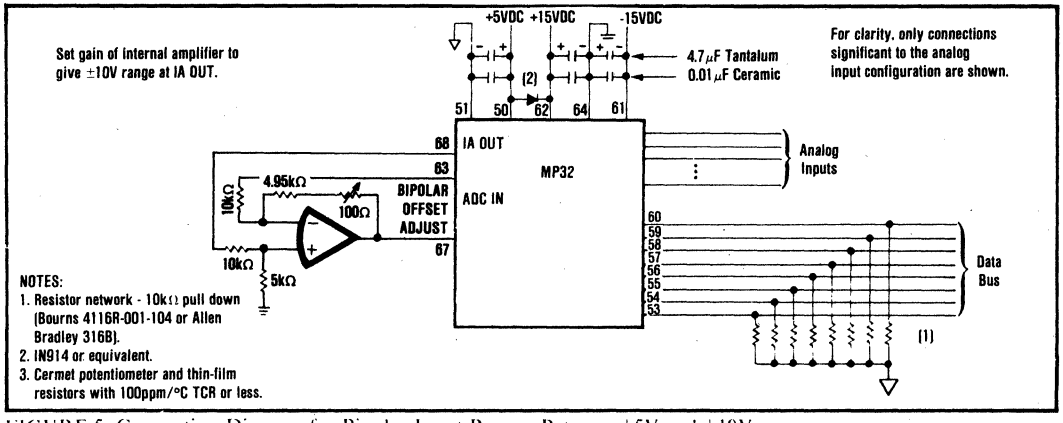


FIGURE 5. Connection Diagram for Bipolar Input Ranges Between ±5V and ±10V.

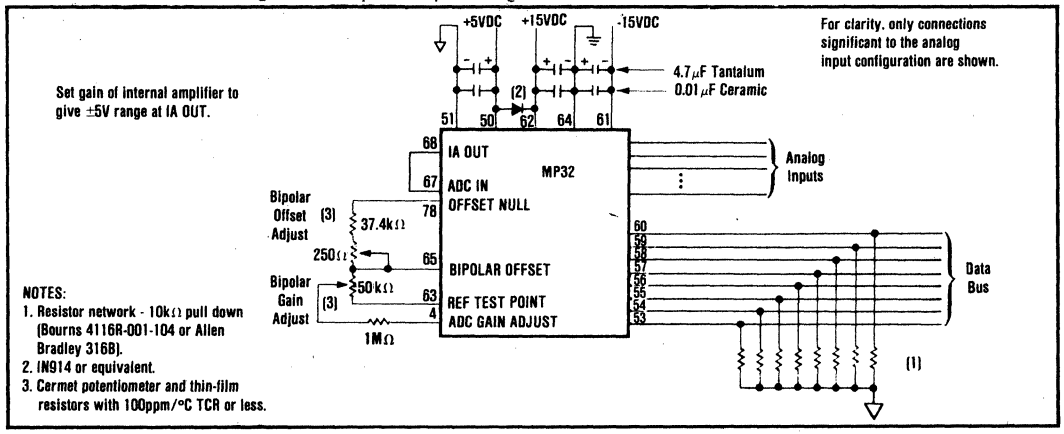


FIGURE 6. Connection Diagram for Bipolar Input Ranges of ±5V or Less.

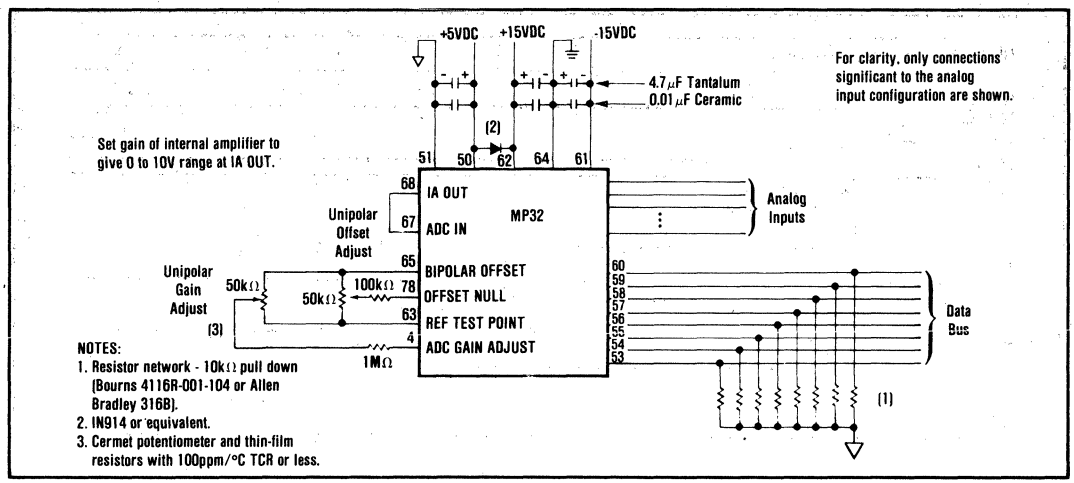


FIGURE 7. Connection Diagram for Unipolar Input Ranges.

mode except the IA low input (pin 79) is connected to a remote ground that is common to the analog inputs.

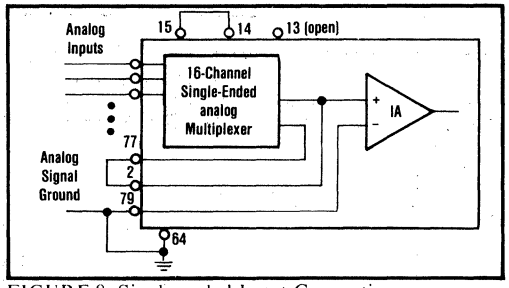


FIGURE 8. Single-ended Input Connections.

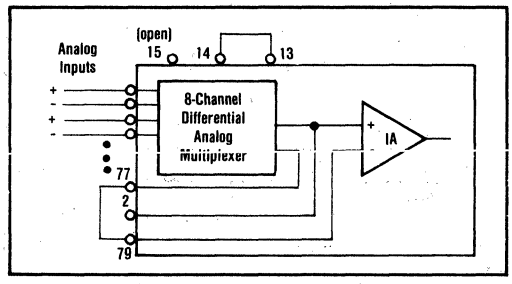


FIGURE 9. Differential Input Connections.

INPUT OVERVOLTAGE PROTECTION

As shown in Figure 10, the analog inputs have reverse biased diode circuits which protect them from damage by overvoltage (such as static). It is still reasonable to take precautions against static discharge. The same circuitry protects the inputs during operation against damage by steady-state differential or common-mode overvoltage. The MP32 overvoltage protection can be increased by adding series resistors at each input. The input resistance must limit the current flowing through the input protection diodes to 10mA. For instance, if 15kΩ resistors are added to each input, the protection is increased to 165V (16.5kΩ x 10mA). Care should be taken to insure safe power dissipation in these resistors. In this case, the power dissipated is 1.65 watts. Increased input resistance will, of course, increase the amount of time necessary for the multiplexer to settle as described in the following section.

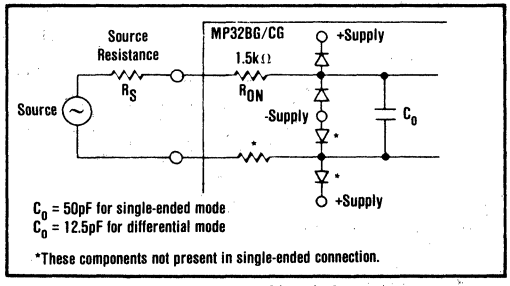


FIGURE 10. "ON" Channel Circuit Model.

SETTLING TIME AND DELAY TIME ADJUST

A delay time between channel selection and start of conversion is built into the MP32 to allow the analog multiplexer and instrumentation amplifier time to settle before starting the A/D converter. As the gain of the amplifier is increased, the settling time required increases (see Figure 11). The factory-set delay time (15μsec) is sufficient for gains of up to 50. At higher gains, a capacitor must be connected between pin 47 and pin 50 to increase the delay time. Figure 12 shows the value of capacitance required to increase the delay.

The only external factor, other than gain, that affects the MP32 settling time is the impedance of the source connected to a channel. Figure 10 shows a circuit model of an "ON" channel.

The signal at the output of the multiplexer must be allowed to settle to ±0.01% (9.2 time constants) to maintain the full accuracy of the system. The multiplexer

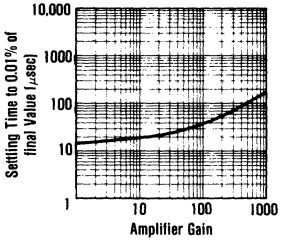


FIGURE 11. Differential Amplifier Settling Time vs Gain.

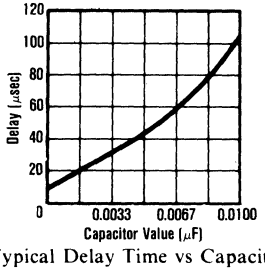


FIGURE 12. Typical Delay Time vs Capacitor Value.

time constant can be calculated with the formula:

$$\tau = (R_S + R_{ON})C_o.$$

For $R_S = 1k\Omega$ and $C_o = 50pF$, $\tau = (1.5 + 1)k\Omega \times 50pF =$ 125nsec. The 1.5μsec is needed to settle to ±0.01%. For high input impedances requiring more than 10μsec for multiplexer settling time, the required delay time may be calculated with this formula:

$$T_D = \sqrt{T_{mux}^2 + T_{1A}^2},$$

where T_{mux} is the settling time of the multiplexer and T_{1A} is the settling time of the instrumentation amplifier as shown in Figure 11. If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large capacitance across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5μF is sufficient. For such a capacitance the multiplexer time constant becomes 80nsec.

For switching of large signals it must be remembered that the "ON" resistance is the channel resistance of a FET which is a nonlinear function of the applied voltage. As a result the previous calculations are only an approximation derived from a linearized model. Another factor not considered is the addressing delay of the multiplexer. This is typically 250nsec and is additive to the above calculated times.

For differential units the same considerations apply. Even though two input circuits are involved there is sufficient component matching within the multiplexer to prevent measurable differences in the transfer functions for each half of the signals. Therefore, the time constant for only one circuit can be considered the time constant for the entire channel.

The MP32 internal instrumentation amplifier requires 15μsec to 100μsec for settling time. If this internal amplifier is not used, improvements in throughput rate can be obtained. This is easily done since neither the inputs nor the outputs of the instrumentation amplifier are internally connected. For instance, Burr-Brown's model 3507J high speed op amp may be used, with a settling time of 1μsec for gains of up to 100.

For a T_{1A} of 1μsec we have $T_D = 1.3$μsec. Using 3μsec for the delay time to allow for unit-to-unit variation, the total throughput time will be 33μsec (including the ADC conversion time of 30μsec—see Figure 13).

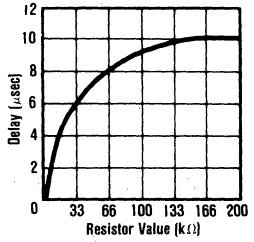


FIGURE 13. Typical Resistor Value to Decrease Delay Time.

DATA OUTPUT CODING

Table III gives the relationship of various input voltage levels to corresponding output digital words. The coding for unipolar input ranges is called Unipolar Straight Binary; bipolar input ranges yield Bipolar Offset Binary codes. Another popular output code used with bipolar input is Two's Complement. It is identical to the Bipolar Offset Binary except the MSB is inverted.

TABLE III. Voltage Input/ Digital Output Relationship.

Analog Input			Digital Output
Unipolar Straight Binary	Bipolar Offset Binary	Bipolar Two's Complement	MSB LSB
+Full Scale -1LSB	+Full Scale -1LSB	-1LSB	111111111111
+1/2 Full Scale	Zero	-Full Scale	100000000000
+1/2 Full Scale -1LSB	-1LSB	+Full Scale -1LSB	011111111111
Zero	-Full Scale	Zero	000000000000

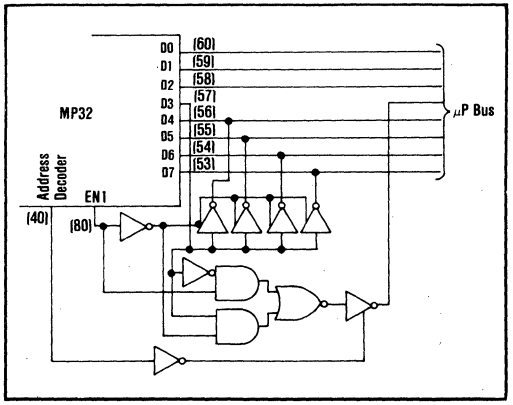


FIGURE 14. Two's Complement Coding - Output Circuit.

The two's complement output code may be obtained by software programming or by hardware, using a 4-bit

tri-state inverter as shown in Figure 14. The EN1 (pin 80) signal is used to gate $\overline{MSB}$ on the microprocessor bus during the time when the second byte of data is enabled. Thus $\overline{MSB}$ replaces MSB in this byte. The top four bits (D4-D7), normally not used in the second byte, are made equal to MSB to make two's complement addition easier.

SETUP AND CALIBRATION

RESET

It is important to reset the MP32 on start-up with a low pulse on the $\overline{RESET}$ line (pin 39). The reset pulse clears internal control logic and guarantees that at start-up all control lines are in the proper state.

GAIN AND OFFSET ADJUST CIRCUITS

The components required to null gain and offset errors for unipolar and bipolar inputs are shown in Figure 5, 6, and 7.

The offset is adjusted at the lowest input voltage transition point. (The input voltage at which the output code changes from 000000000000 to 000000000001.) The gain is adjusted at the highest input voltage transition point. Offset is adjusted first, then gain.

CALIBRATION WHEN USED WITH INTEL MODEL 8080

Before calibration, the MP32 should be allowed to warm up for 15 minutes (power applied). Calibration is performed by connecting a precision voltage source (capable of 0.005% accuracy) to an input channel. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.005% DVM.) The offset and gain adjustments on the MP32 are made while applying the voltages shown in Table IV.

The following program is used to calibrate:

```
        ORG     10H
AD:     LXI     B0          ;Clear B and C Reg. pair
AC:     LHLD    1F70H       ;Read data from
        MOV     A, L        ;Is Data = Low Ref?
        SUI     XXXX*
        JZ      AA
        INR     C           ;No. Increment count
        JMP     AB
AA:     INR     B           ;Yes. Increment count
AB:     MOV     A, B        ;Have 100 conversions
                            ; been made
        ADD     C
        CPI     64H
        JNZ     AC
AE:     JMP     AD          ;Yes. Begin program again
        END
```

*XXXX is 0000 for offset, 0FFF for gain.

The program assumes that the MP32 is wired for channel 0 located at 1F70H. If the MP32 is wired for a different address, the address associated with the LHLD instruction AC must reflect this change.

After assembling and loading the program, set a breakpoint at AE. The program is then started using a G10 Command. After 100 conversions, the breakpoint will be reached and control will return to the monitor. The B and C registers are then examined for an approximately equal count (within 10_{16} of each other). Both the Offset and Gain adjustments require that this process be repeated until the approximately equal count is reached.

CALIBRATION WHEN USED WITH MOTOROLA MODEL 6800

The procedure is the same in concept as that described in the 8080 calibration procedure. Again the unit should be allowed to warm up (power applied) for 15 minutes. The MP32 is connected as shown in Figure 21.

The 6800 calibration program is:

```
        ORG $100
START   LDAA #$64       86
                        64
        STAA COUNT      B7
                        01
                        21
        CLRA            4F      Clear accumulators
        CLRB            5F
CONV    LDX #0000       CE
                        00
                        00
        STX $1F70       FF      Begin conversion
                        1F
                        70
        NOP             01
        LDX $1F70       FE      Read data
                        1F
                        70
        CPX #$XXXX*     8C      Is Data = Low Ref
                        00
                        00
        BEQ AA          27
                        03
        INCB            5C      No. Increment count
        BRA AB          20
                        01
AA      INCA            4C      Yes. Increment count
AB      DEC COUNT       7A      Have conversions reached 100?
                        01
                        21
        BNE CONV        26      No. Do another conversion
                        F0
        BRA START       20      Yes. Begin next run
                        DF
COUNT
        END
```

*XXXX is 0000 for offset, 0FFF for gain.

The program assumes that the MP32 is set for channel located at $1F70_{16}$ and $1F71_{16}$. If the MP32 has been reprogrammed for some other address this value should be reflected in the program's STX instructions that refer to the MP32.

After assembling and loading, insert a breakpoint at location 11C via a "V" command.

Calibration is performed by connecting a precision voltage source capable of 0.005% accuracy to CH0. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.005% DVM.) The offset adjustment is made first by using the appropriate offset calibration voltage. The calibration program is then run and after 100 conversions will halt at the breakpoint. Control will return to the monitor which will then print the contents of all of the program registers at the time of the breakpoint. The contents of each accumulator should be compared for approximately equal values. If a difference of more than 10_{16} is present, slightly readjust the offset control and restart the program with a ;P command. Repeat this procedure until the accumulators' contents are within 10_{16} of each other.

TABLE IV. Calibration Input Voltages.

	Input Voltage Range(1)	Full Scale Range	LSB Value	V_{in} for Offset Adjustment	V_{in} for Gain Adjustment
Unipolar	0 to +10V 0 to +5V 0 to +1V	10V 5V 1V	2.44mV 1.22mV 244μV	+1.22mV +0.610mV +0.122mV	9.99634 4.99817 +0.99963V
Bipolar	-10V to +10V -5V to +5V -1V to +1V	20V 10V 2V	4.88mV 2.44mV 488μV	-9.99756 -4.9988 -0.99976V	9.99268 4.99634 +0.99927V
General Equation	V_1 to V_2	$V_2 - V_1$	$\frac{V_2 - V_1}{2^n}$(2)	V_1 + 1/2LSB	V_2 - 3/2LSB

NOTES:
1. For other ranges, compute the proper input voltages using the general equation.
2. n = resolution (12 bits for MP32BG/CG

The gain adjustment is made in much the same manner. However, the data associated with the CPX instruction in the calibration program must be changed from 0000_{16} to $0FFF_{16}$.

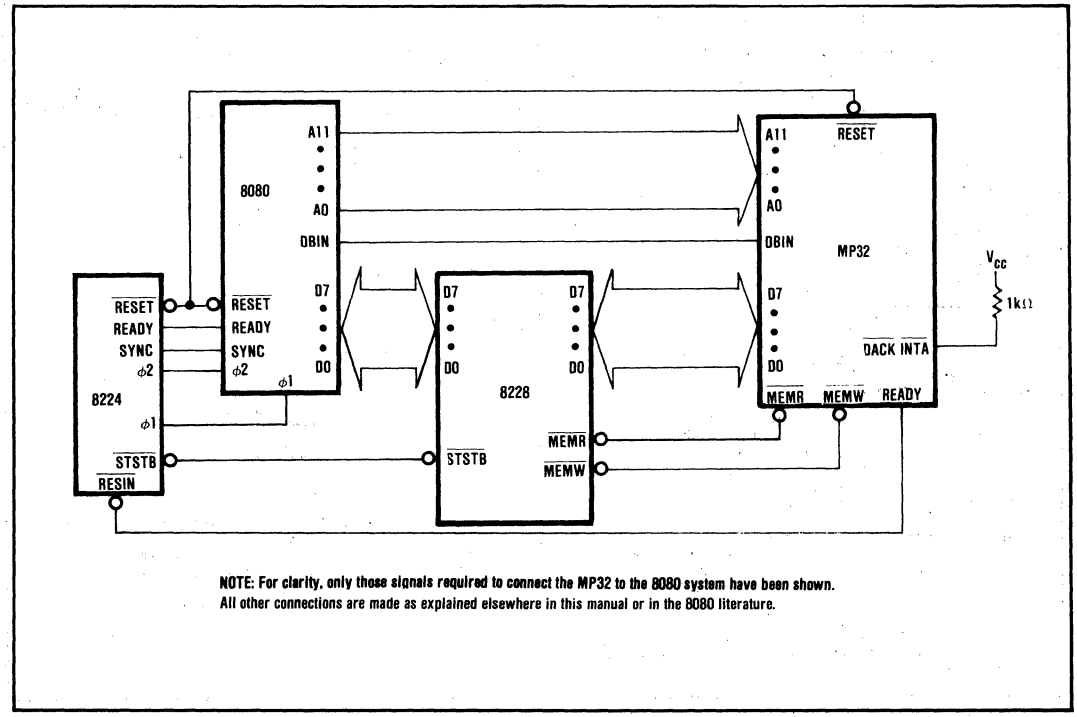
CALIBRATION WHEN USED WITH OTHER MICROPROCESSORS

The same technique used in calibrating the MP32 with the 8080 and 6800 can be used with any processor. Repetitive conversions are made around the "edge" of an output digital step or transition (the lowest for offset, the highest for gain), and then look for 50% of the conversions to be on each side of the edge. The program should be written to convert with the input at the transition voltage a large number of times and record in two registers the number of conversions that fall on each side of the transition voltage. When the numbers are approximately equal (within 10_{16}), the converter is calibrated. This must be done for offset first, then gain. Refer to Table IV for the high and low transition voltages.

Again, the unit should be allowed to warm up for 15 minutes with power applied prior to calibration.

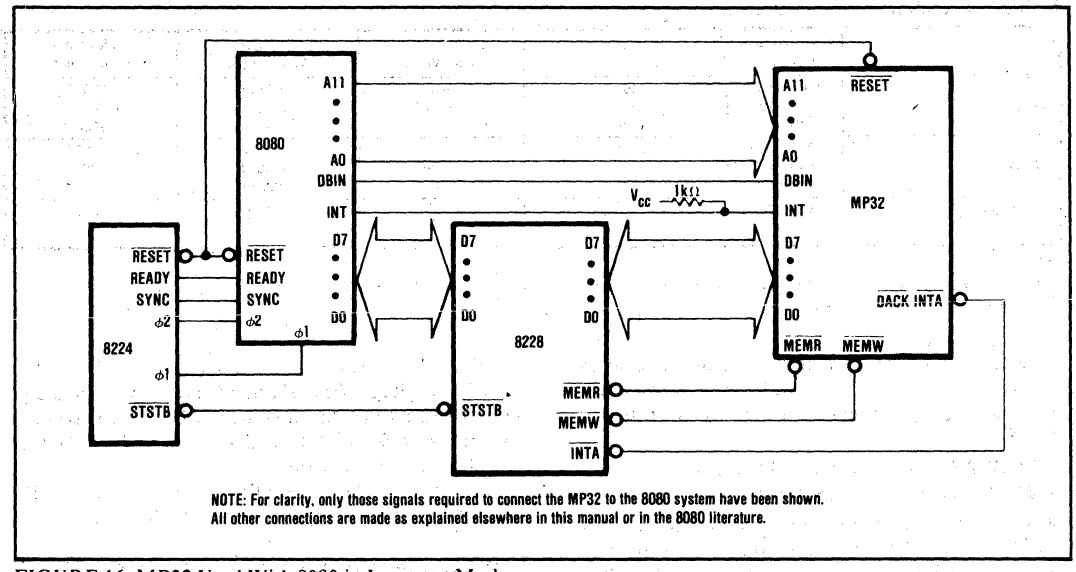
INTERFACE CONNECTION DIAGRAMS

The MP32 is designed to easily interface with most micoprocessors. The following pages illustrate the use of the MP32 with several different CPU's. The basic software to operate the units is also shown except where previously discussed in the text.



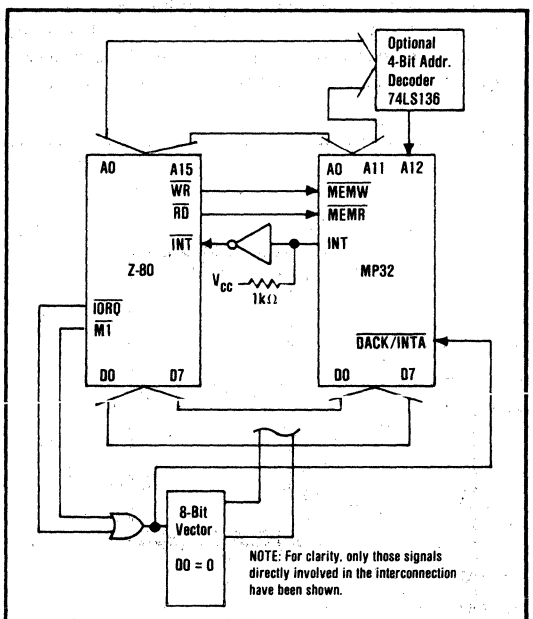
NOTE: For clarity, only those signals required to connect the MP32 to the 8080 system have been shown. All other connections are made as explained elsewhere in this manual or in the 8080 literature.

FIGURE 15. MP32 Used With 8080 in Halt Mode.



NOTE: For clarity, only those signals required to connect the MP32 to the 8080 system have been shown.
All other connections are made as explained elsewhere in this manual or in the 8080 literature.

FIGURE 16. MP32 Used With 8080 in Interrupt Mode.



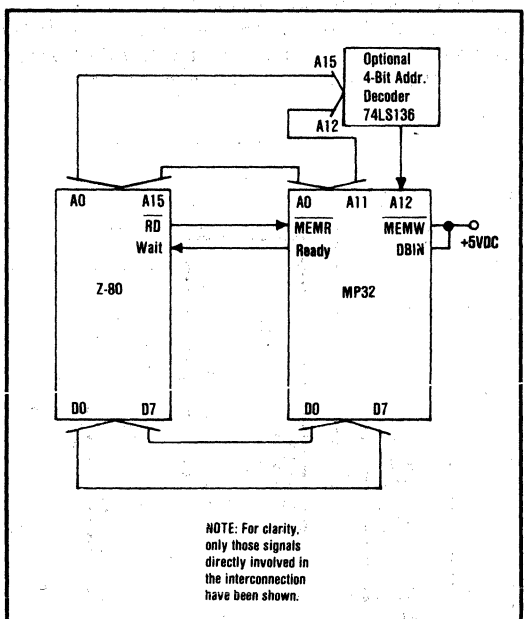
NOTE: For clarity, only those signals directly involved in the interconnection have been shown.

Z-80 is initialized to interrupt MODE 2
Conversion is started by these instructions: LDA, 0
LD (XXXX), A
The following routine is used to service the interrupt:

```
INTR:   PUSH HL          ;Save HL register pair
        LD HL, (XXXX)    ;Read data
        LD (YYYY), HL    ;Store data in memory
        POP HL           ;Restore HL register pair
        RET1
```

XXXX is the starting address of the desired channel.
YYYY is the starting address of the locations in memory where data is stored.

FIGURE 17. MP32 Used With Z-80 (Interrupt Mode).



NOTE: For clarity, only those signals directly involved in the interconnection have been shown.

Program to READ and STORE 16 channels of data using Block Transfer Instruction.

```
LD HL, NN        ;NN point to channel 0 MP32
LD DE, MM        ;MM points to the first location of the destination
LD BC, 40H       ;Byte counter (2 bytes channel x 16) = 32(10)
LDI              ;Load and increment
JP PE, LOAD      ;Has last byte been transferred?
```

FIGURE 18. MP32 Used With Z-80 (Halt Mode).

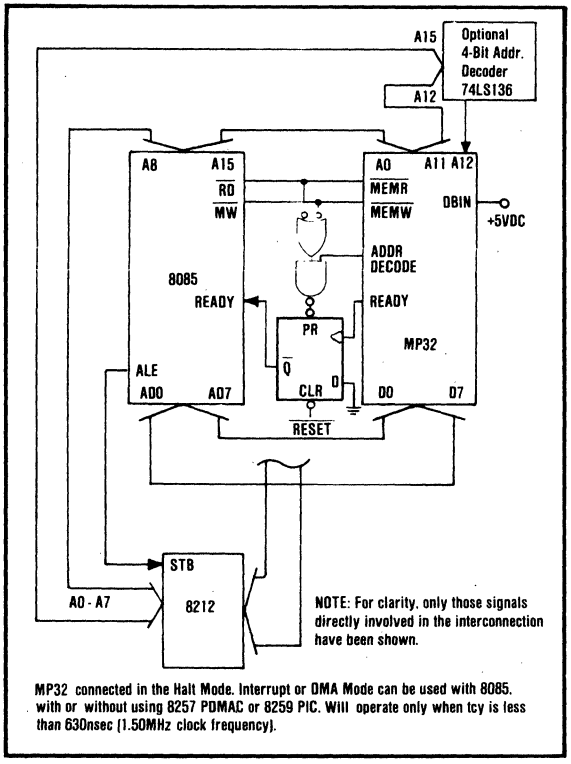


FIGURE 19. MP32 Used With 8085.

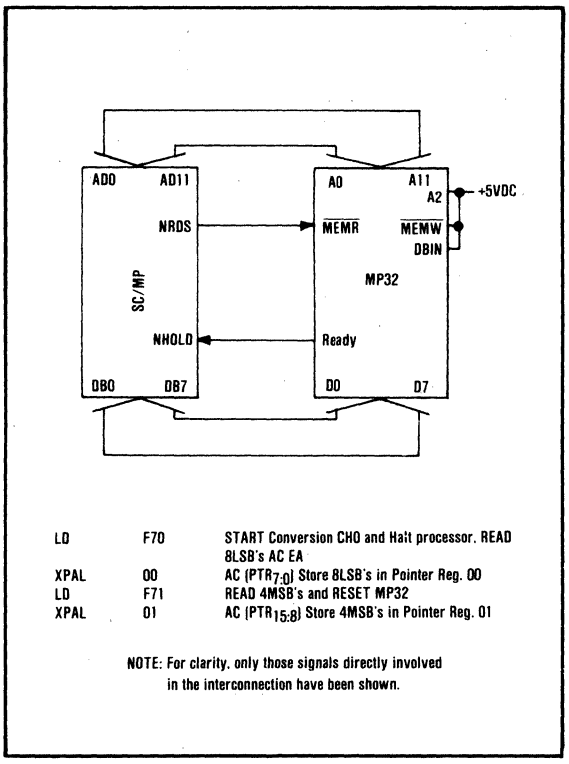


FIGURE 20. MP32 Used With SC/MP (Halt Mode).

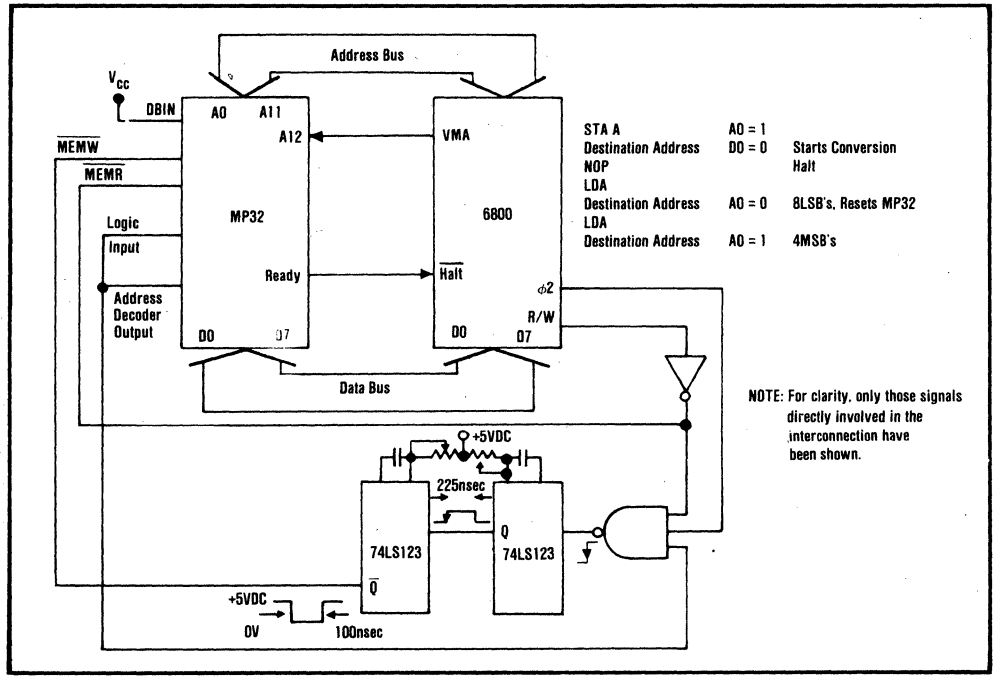


FIGURE 21. MP32 Used With 6800.

APPLICATION NOTE

DATA ACQUISITION FROM THERMOCOUPLE INPUTS

Thermocouples are often used as temperature sensors for porcess control systems. Thermocouples are characterized by temperature coefficients of 10μV/°C to 70μV/°C and operating ranges of minus hundreds to plus thousands of degrees centrigrade. When the MP32 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60Hz or higher frequencies. When the MP32 is used as an 8-channel differential input system, the high common-mode rejection of the instrumentation amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule, an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices can not always be observed, a differential RC filter may be used. Figure 22 shows such a system.

The 10kΩ resistors and 10μF capacitor provide low-pass filtering (f_c = 0.8Hz) and the optional 1MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth-grounded to prevent common-mode voltages from exceeding the ±5V range of the multiplexer. If the sensor is earth-grounded, the 1MΩ resistors are not required. The 1MΩ resistors do not enter into an error calculation for input errors because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias currents of the two inputs. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold-junction compensated. Figure 22 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2mV/°C.

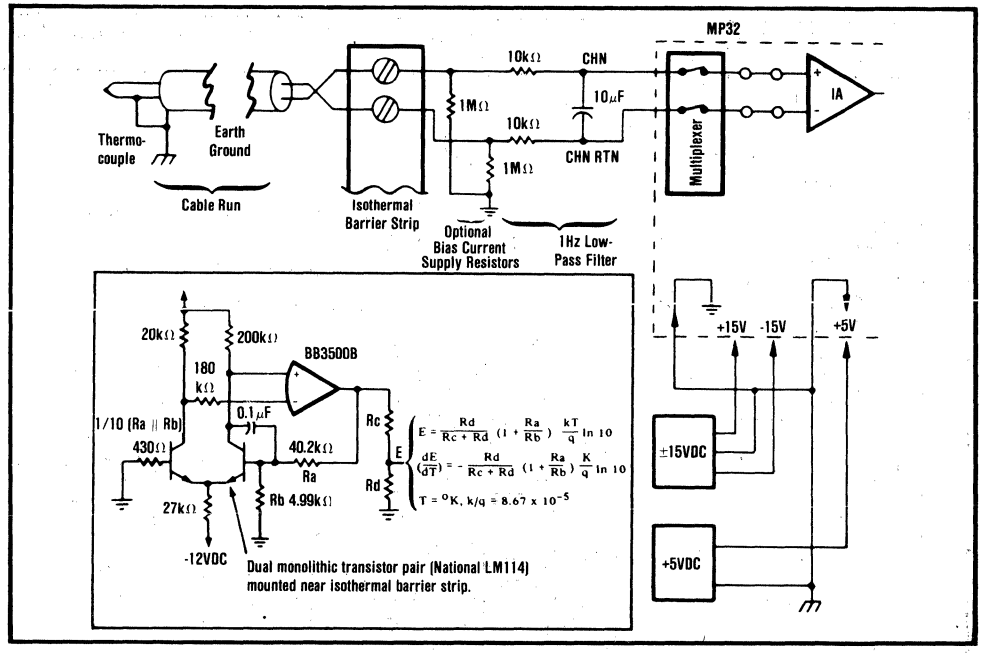


FIGURE 22. Thermocouple Input System Using MP32.

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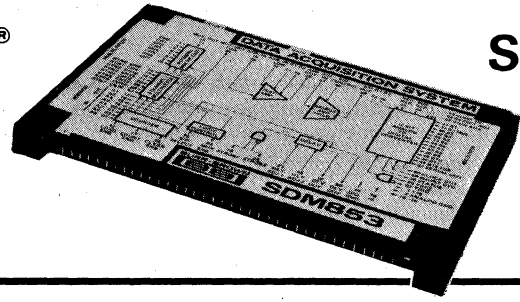


SDM853

DATA ACQUISITION SYSTEM

FEATURES

- SAVES DESIGN TIME
- RELIABLE - 168-hour bake
- LOW LEVEL OR HIGH LEVEL INPUTS
- SAVES SPACE
- FLEXIBLE - Up to four modes of operation
- LOW COST

DESCRIPTION

The SDM853 is a complete 8- or 16-channel data acquisition system in a compact 4.6" x 3.0" x 0.375" metal case. This system differs from most in that it can acquire and digitize low level or high level analog signals. A built-in high quality instrumentation amplifier allows input signal ranges of ±10mV to ±10V. This means that the SDM853 can be connected to low level sensors such as thermocouples and strain gauges without external signal conditioning.

This expandable module accepts either 16 single-ended or 8 differential inputs and converts the multiplexed data signals into 12-bit digial words with an accuracy of ±0.025% at throughput rates of up to 33,000 samples per second.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DISCUSSION OF PERFORMANCE

The SDM853 is a complete modular "off-the-shelf" data acquisition system. With this system it is possible to configure complete data acquisition systems in one-fourth the space for a fraction of the cost previously possible.

These systems contain all the components necessary to multiplex and convert ±10mV to ±10V analog data into equivalent digital outputs yielding resolutions of 2.4μV to 2.4mV. The minimum throughput sampling rates are up to 30kHz for 12-bit and up to 43kHz for 8-bit resolution. The model SDM853 contains an analog multiplexer which can be connected in a 16-channel single-ended or 8-channel differential mode, instrumentation amplifier, sample/hold, 12-bit successive approximation A/D converter and programming logic. The amplifier and sample/hold are not internally interconnected. This allows maximum application flexibility. These systems can be expanded without limit using Burr-Brown's MPC-16S and MPC-8D monolithic multiplexers. Figure 1 shows the components of the SDM853. The system is designed to be mounted on a printed circuit card. The only requirement for system operation are input signals, power and the interconnection of the system components into the desired operating configuration.

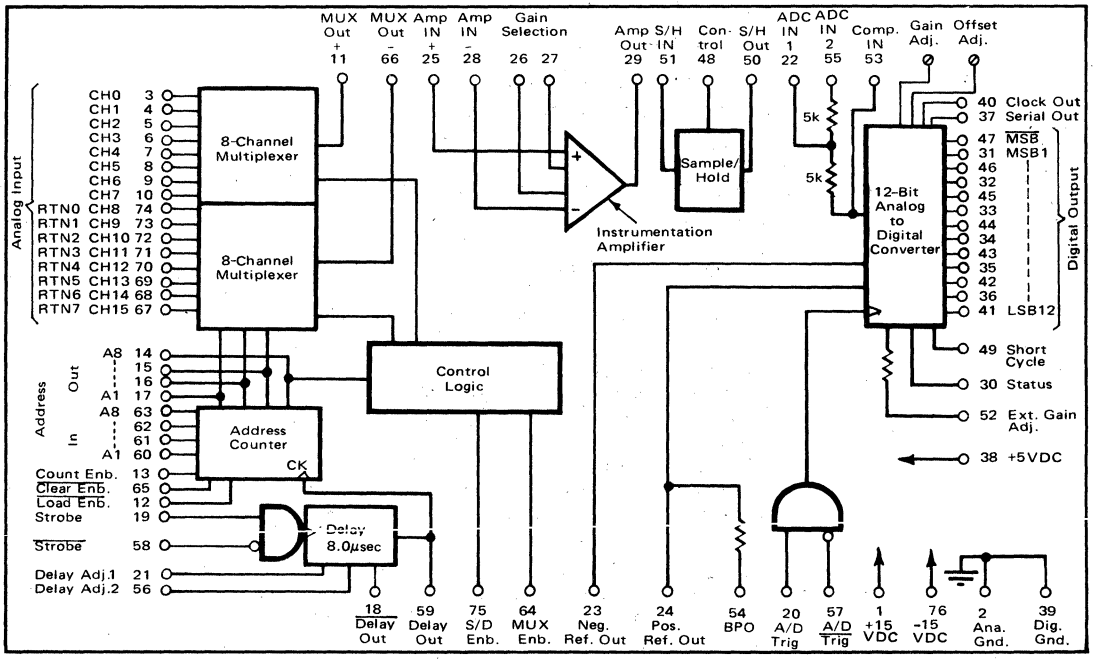


FIGURE 1. SDM853 Block Diagram.

ANALOG MULTIPLEXER

Two one-of-eight CMOS analog multiplexers are used to allow user selection by external jumpers of 16 single-ended channel or 8 double-ended channel operation. In 16-channel operation the multiplexer may be used in a pseudo differential mode by connecting the amplifier inverting input to a common, remote, signal ground. Channel selection is by a 3- or 4-bit binary word stored in a presettable address counter. Channel capacity is expandable without limit.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity, and external gain-programming with an external resistor. With the gain-programming pins open, the gain is unity. Gain may be selected from unity to 60 dB.

SAMPLE AND HOLD AMPLIFIERS

The sample and hold amplifier is a complete, stand alone, sample and hold circuit featuring buffered output, 7μsec acquisition time, and 30nsec aperture time. Input, output and mode control functions are brought to separate connector pins. This allows maximum system flexability for performing such functions as automatic gain ranging with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a ceramic packaged, 12-bit converter featuring 24μsec conversion time and 0.01% accuracy. Thin-film networks and current switching are used to assure linearity over wide temperature ranges.

ADDRESS COUNTER

A 4-bit binary address counter is connected to the multiplexer. This counter may be externally loaded, cleared, clocked or enabled. The address outputs are brought to connector pins for convenient system control.

DELAY TIMER

The delay timer is provided to allow for the settling time of the multiplexer, amplifier, and sample and hold circuits. The delay time is adjustable over a wide range by an external potentiometer and/or external capacitor. This allows for the longer settling time of the instrument amplifier at high gains.

CONTROL LOGIC

Delay and ADC trigger functions are edge-triggered and gated. Counter control functions are synchronous with the counter clock which is internally connected to the delay timer output.

CHANNEL EXPANSION

The number of analog input channels of these systems can easily be increased using Burr-Brown's MPC8D and MPC16S CMOS multiplexers. the MPC8D is an 8-channel differential model and the MPC16S is a 16-channel single-ended model. These are latch-free devices which contain internal binary decoding, TTL or MOS logic levels, and may be integrated into a system with minimum external logic.

SYSTEM PERFORMANCE

The SDM853 can be configured to continuously sequence through all analog channels, to accept random addresses or to sequence through all analog channels on command from an external trigger.

The status signal, pin 30, is connected to the strobe not input of the delay timer, pin 58, for normal program sequencing with a minimum throughput sampling rate of 30kHz for 12-bit resolution.

By using "overlap" programming, the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced, extending throughput sampling rates up to 32kHz for 12-bit and 43kHz to 8-bit resolution. This mode of operation is most useful when converting low level inputs to accommodate the increased settling time of the instrumentation amplifier. Overlap programming is accomplished by connecting the status signal, pin 30, to the strobe input of the delay timer, pin 19, and extending the delay time. The internal logic will then select analog channel (n + 1) while channel n is being converted.

SYSTEM PERFORMANCE

(Typical at 25°C and rated supplies)

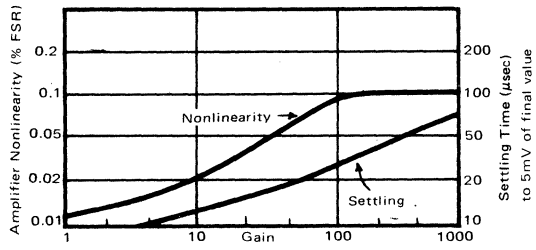


FIGURE 2. Nonlinearity and Settling Time vs. Amplifier Gain.

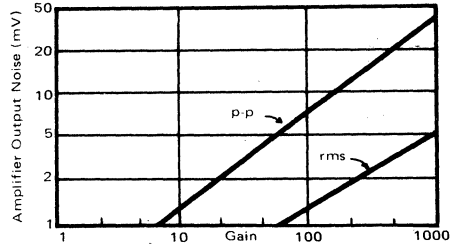


FIGURE 3. Output Noise vs. Amplifier Gain.

System Gain	System Accuracy	Throughput Rate (Channels/sec)		Delay Time (μsec)	
V/V		Normal	Overlap	Normal	Overlap
1	±0.025% FSR	30k	32k	9	31
10	±0.035% FSR	25k	32k	18	31
100	±0.08% FSR	20k	32k	25	31
1000	±0.1% FSR	10k	14k	70	70

TABLE I. Throughput Rate vs. Gain for Normal and Overlap Modes.

FSR	ADC Range	Amplifier Gain	Resolution	Delay for Settling to ±0.2% (μsec)	Delay for Settling to ±0.05% (μsec)	Delay for Settling to 0.01% (μsec)
20V	±10V	1	4.88mV	7	8	9
1V	0 to 10V	10	244μV	10	15	18
0.1V	0 to 10V	100	24.4μV	20	25	30
10mV	0 to 10V	1000	2.44μV*	60	70	-

TABLE II. This table shows the delay timer setting required to allow for the settling time of the instrumentation amplifier to the accuracies specified. Add the 24μsec conversion time of the A/D converter to the above delay times to obtain channel conversion times. * Depends on desired S/N ratio.

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	SDM853
TRANSFER CHARACTERISTICS	
Throughput Rate, min	30kHz, 33μsec/channel
Resolution	12 Bits
Number of Channels	16 single-ended/8 differential
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	1 to 1000
Amplifier gain equation	$G = 1 + 20k\Omega/R_{EXT}$ [1]
Max. input voltage without damage	±16V
Max. input voltage for multiplexer operation	±10.24V
Input impedance	100MΩ, 10pF OFF channel 100MΩ, 100pF ON channel
Bias current	
25°C	20nA
0°C to 70°C	50nA
Differential Bias Current (25°C)	10nA
Differential Bias Current Drift	0.1nA/°C
Amplifier output noise (Gain = 100, R_s = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage, max	400μV
Amplifier voltage offset drift	2 + 20/GμV/°C
ACCURACY[2]	
System RSS accuracy at 25°C (Gain = 1)	±0.025% FSR[3] at 30kHz throughput
Linearity (Gain = 1)	±1/2LSB, at 30kHz throughput
Differential linearity (Gain = 1)	±1/2LSB, at 30kHz throughput
Quantizing error	±1/2LSB
Gain error	Adjustable to zero
Offset error	Adjustable to zero
Power supply sensitivity	±0.005% FSR/% change of supply voltage
STABILITY OVER TEMPERATURE	
System accuracy drift, max	±30ppm/°C of reading
Linearity drift	±3ppm of FSR/°C
DYNAMIC ACCURACY	
Sample & Hold aperture time	30nsec
Aperture time uncertainty	±5nsec
Error for full scale transition between successively addressed channels	1LSB at 30kHz
Differential amplifier CMRR (Gain = 1)	74dB at 1kHz 65dB at 3kHz (100dB at 60Hz Gain = 1000)
Channel cross talk	80dB down at 2kHz, for OFF channel to ON channel
Sample & Hold feedthrough	80dB down at 5kHz
Sample & Hold decay rate	10μVμsec
OUTPUT	
Output Coding (Complementary)	Unipolar Straight Binary, Bipolar Offset, Binary Two's Complement
Gain trim[4]	Adjustable to zero error
Offset trim[4]	Adjustable to zero error
A/D Conversion Time	24μsec
Delay	9μsec nominal, externally adjustable from 5.5μsec to 14μsec[5]
POWER REQUIREMENTS	±15VDC ±3% at +50mA, 5mV, rms, ripple -15VDC ±3% at -75mA, 5mV, rms, ripple +5VDC ±5% at +300mA, 25mV, rms, ripple
ENVIRONMENTAL	
Operating temperature	0°C to 70°C
Storage temperature	-25°C to +85°C
Relative humidity	95% noncondensing

1. With R_{EXT} between pins 26 and 27.
2. No missing codes guaranteed.
3. FSR means Full Scale Range.
4. Gain and Offset controls are located in the module. The adjustment ranges are ±0.1% FSR for Gain and ±0.1% FSR for Offset.
5. Adjustable to 10 seconds with external capacitor.

DIGITAL INPUT SPECIFICATIONS	
Address inputs	One standard TTL load, positive true
Coding	4-bit binary
$\overline{\text{Load Enable}}$	One standard TTL load, negative true, address loaded with strobe inputs.
$\overline{\text{Clear Enable}}$	One standard TTL load, negative true, address loaded with strobe inputs.
Strobe & $\overline{\text{Strobe}}$	One standard TTL load; STROBE and $\overline{\text{STROBE}}$ edge trigger the delay timer and clock the address counter. STROBE must be high to enable $\overline{\text{STROBE}}$ and $\overline{\text{STROBE}}$ must be low to enable STROBE.
Count Enable	Two standard TTL loads, positive true, logic "0" allows the Strobe inputs to trigger the delay timer, but prevents the MUX address counter from being clocked.
ADC trigger	One standard TTL load, a positive going edge at TRIG initiates conversion, a negative going edge at $\overline{\text{TRIG}}$ initiates conversion; $\overline{\text{TRIG}}$ must be "0" to enable TRIG; TRIG must be "1" to enable $\overline{\text{TRIG}}$.
Short cycle	One standard TTL load, logical 1 for 12-bit resolution, connected to the N + 1 bit output for N bit resolution.
Multiplexer Enable	
Multiplexer Enable	Two standard TTL loads, logical 1 enable multiplexer output and logical 0 turns off all channels.
S/D select	Two standard TTL loads, logical 1 enables 16-channel single-ended operation and logical 0 enable 8-channel differential operation.
DIGITAL OUTPUT SPECIFICATIONS	
Data outputs	
Parallel B1, B1 . . . B12	2 Standard TTL loads, negative true.
Serial out	2 Standard TTL loads, negative true, time serial data output beginning with B1. (see timing diagram).
Address outputs	5 Standard TTL loads, positive true, 4-bit binary code, internal 2kΩ pull-up resistors.
Delay out (Delay Out)	5 Standard TTL loads high (low) during the delay period, triggered by $\overline{\text{Strobe}}$ and Strobe inputs.
Clock	5 Standard TTL loads for synchronizing serial out data (see timing diagram).
Status	5 Standard TTL loads, high during the A/D conversion.

SYSTEM TIMING DIAGRAMS

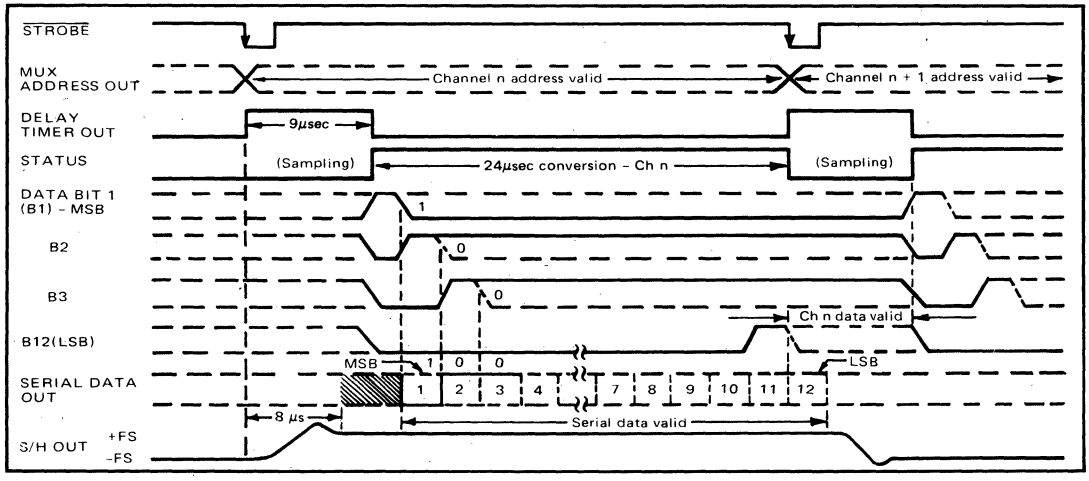


FIGURE 4. Timing Diagram for Sequential Addressing Normal Programming Mode.

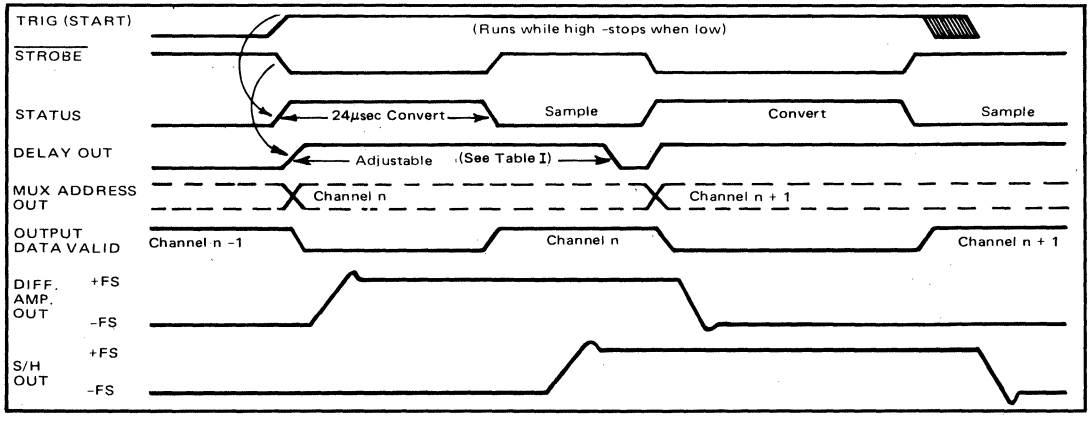
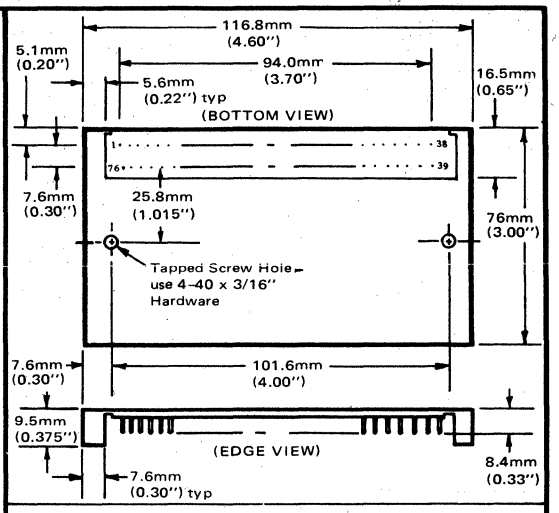


FIGURE 5. Timing Diagram for Sequential Overlap Programming Mode. (Delay must be adjusted to status pulse.)

PACKAGE AND PIN CONFIGURATION

SDM853 CONNECTOR PIN DIAGRAM

+15VDC	1	76	-15VDC
ANA. GND.	2	75	S/D ENB
CH 0 IN	3	74	CH 8 IN (0 RTN)
CH 1 IN	4	73	CH 9 IN (1 RTN)
CH 2 IN	5	72	CH 10 IN (2 RTN)
CH 3 IN	6	71	CH 11 IN (3 RTN)
CH 4 IN	7	70	CH 12 IN (4 RTN)
CH 5 IN	8	69	CH 13 IN (5 RTN)
CH 6 IN	9	68	CH 14 IN (6 RTN)
CH 7 IN	10	67	CH 15 IN (7 RTN)
MUX OUT HI	11	66	MUX OUT LO
$\overline{\text{LOAD ENB}}$	12	65	$\overline{\text{CLR ENB}}$
COUNT ENB	13	64	MUX ENB
A8 OUT	14	63	A8 IN
A4 OUT	15	62	A4 IN
A2 OUT	16	61	A2 IN
A1 OUT	17	60	A1 IN
$\overline{\text{DLY.}}$	18	59	DLY.
STROBE	19	58	$\overline{\text{STROBE}}$
ADC TRIG	20	57	ADC $\overline{\text{TRIG}}$
DLY. ADJ. 1	21	56	DLY. ADJ. 2
R1	22	55	R2
NEG REF OUT	23	54	BPO
POS. REF OUT	24	53	COMP IN
AMP IN HI	25	52	GAIN ADJ.
G2	26	51	S/H IN
G1	27	50	S/H OUT
AMP IN LO	28	49	SHT. CYC.
AMP OUT	29	48	S/H CONTROL
STATUS	30	47	$\overline{\text{B1}}$
B1 MSB	31	46	B2
B3	32	45	B4
B5	33	44	B6
B7	34	43	B8
B9	35	42	B10
B11	36	41	B12 LSB
SER OUT	37	40	CLK. OUT
+5	38	39	DIG RTN



CASE MATERIAL: Insulated Steel
CONNECTOR PINS: Gold Flashed
WEIGHT: 145 grams (5 oz.)

MOUNTING INSTRUCTIONS:

MOUNTING FLUSH ON PC CARD

1. Use strip connectors or two 14-pin and three 16-pin low profile IC sockets (shipped with each unit).
2. Use 4-40 x 3/16" (4.8mm) LG Pan HD Hardware to secure the SDM853 to PC Card.

ORDERING INFORMATION

Model	Description			Model	Description		
SDM853	16 Channel Single-ended or 8 Channel Differential Data Acquisition System			MPC16S	16 Channel Single-ended CMOS Multiplexer in 28 pin DIP		
MPC 8D	8 Channel Differential CMOS Multiplexer in 28 pin DIP			546	±5V to ±15VDC/DC Converter		

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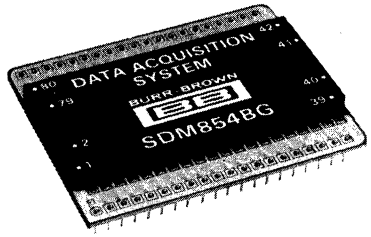


SDM854

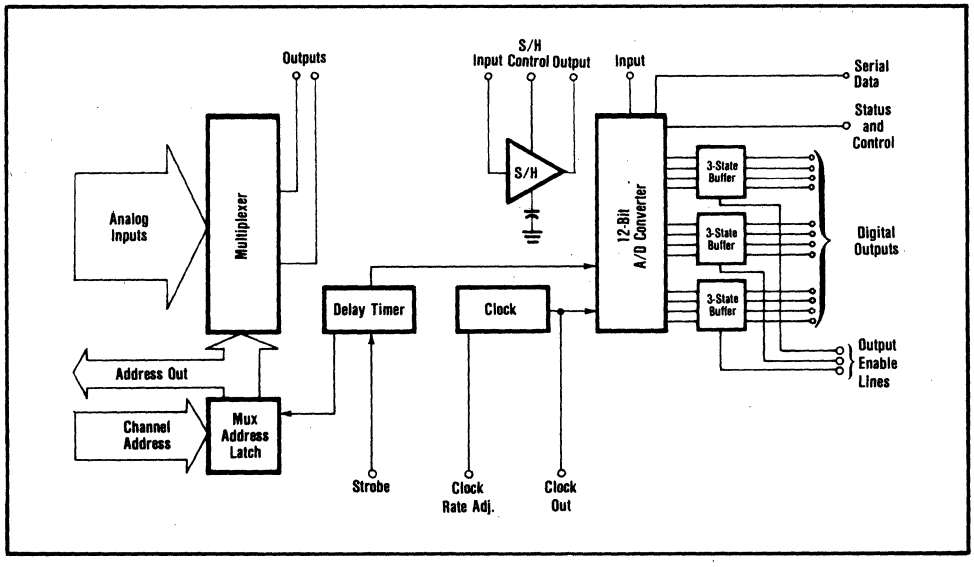
HYBRID DATA ACQUISITION SYSTEM

FEATURES

- MINIATURE SIZE
- LOW COST
- 12-BIT, ±0.012% LINEARITY ERROR
- INPUTS UP TO ±10 VOLTS
- WIDE TEMPERATURE RANGE
- SELECTABLE 16 SINGLE, 8 DIFFERENTIAL INPUTS
- THREE-STATE OUTPUT BUFFERS

DESCRIPTION

The SDM854 is a complete data acquisition system contained in a miniature 2.2" x 1.7" x 0.22" (55.9mm x 43.2mm x 5.6mm) ceramic package. This system offers all the functions available in large modular data acquisition systems. Inputs up to ±10V can be accepted and low-level inputs can be accommodated by connecting an external instrumentation amplifier to the output of the multiplexer and to the input of the sample hold amplifier. Digital resolution is 12 bits with accuracy of ±0.024% at a throughput rate of 27kHz.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SYSTEM DESCRIPTION

The SDM854 contains all components necessary to multiplex and convert analog signals up to ±10V into equivalent digital outputs. Throughput sampling rates are from 27kHz (12-bit resolution) to 70kHz (8-bit resolution) in the overlap mode of operation. The SDM854 can be configured to accept either 8-channel differential or 16-channel single-ended signals and can be expanded almost without limit with external multiplexers. Three-state outputs are provided for easy interface to microprocessor and other bus-structure systems. The system components are illustrated in Figure 1 and described in the following paragraphs.

ANALOG MULTIPLEXER

The analog multiplexer consists of two CMOS integrated circuits. Pin interconnects are used to select 16-channel single-ended or 8-channel differential operation. In single-ended operation the multiplexer can be used in a pseudo-differential mode by connecting an external amplifier's inverting input to common remote signal ground. Channel selection is made by an internally latched 3- or 4-bit binary word, for differential or single-ended operation respectively.

SAMPLE/HOLD

A complete stand-alone circuit, the sample hold amplifier features buffered output, 10μsec acquisition time, and 100nsec aperture time.

Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions, such as automatic gain ranging, with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a 12-bit, 25μsec converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight binary or two's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution or accuracy.

THREE-STATE OUTPUT BUFFERS

Digital outputs of the ADC are internally buffered by LSTTL three-state buffers. Three separate enable lines are brought out for easy interfacing to 4-, 8- or 16-bit data buses. $\overline{\text{MSB}}$ and BUSY are also buffered by separate three-state devices, each with its own enable line.

ADDRESS LATCH

Outputs of the 4-bit TTL register latch are connected to the address inputs of the multiplexer. This latch serves as an address storage register for the selected analog input. It may be loaded through 4 address inputs. Other inputs are LOAD and $\overline{\text{CLEAR}}$. The 3 least significant bits are used for 8-channel differential mode addressing.

DELAY TIMER

A delay timer allows settling time for the multiplexer and sample hold circuits before conversion begins. The delay is adjustable over a wide range by use of an external resistor or capacitor. This allows for longer settling time if an external instrumentation amplifier is used and is operating at high gains, or shorter settling time for lower resolution operation.

CHANNEL EXPANSION

The number of analog input channels of the SDM854 can be easily increased by using Burr-Brown's MPC8D (8-channel differential) and MPC16S (16-channel single-ended) multiplexers. These are latch-free devices which contain internal binary decoding at TTL or MOS levels and may be integrated into a system with minimal external logic.

SYSTEM PERFORMANCE

The SDM854 is configured for random channel selection. With the addition of an external counter they can be

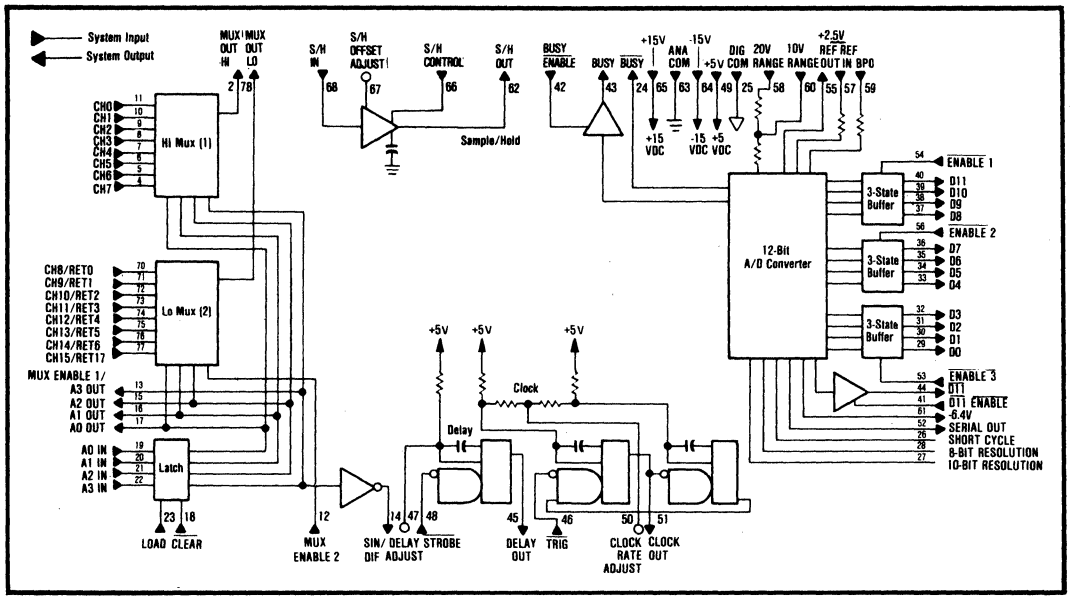


FIGURE 1. SDM854 Block Diagram.

configured to continuously sequence through all analog channels or sequence through all analog channels on command from an external trigger.

With the appropriate 4-bit (single-ended) or 3-bit (differential) channel address on the latch inputs, and DELAY OUT (pin 45) tied to the LOAD input (pin 23), a negative going edge is applied to the $\overline{\text{STROBE}}$ input (pin 48). This starts the delay timer, latches the multiplexer address, and allows the input signal to pass through the multiplexer, and sample hold before starting the A/D conversion. The DELAY OUT signal (pin 45) is also connected to the $\overline{\text{TRIG}}$ input (pin 46) and the A/D conversion is initiated on the negative-going edge. The S/H CONTROL input (pin 66) is connected to $\overline{\text{BUSY}}$ (pin 24) so that the sample hold is in the HOLD mode during the A/D conversion.

By using overlap programming the settling time effects of the analog multiplexer and external instrumentation amplifier (if used) can be reduced, extending throughput sampling rates up to 27kHz for 12-bit and 70kHz for 8-bit resolution (ADC short-cycled). This mode of operation is most useful when converting low-level inputs to accommodate the increased settling time of the external instrumentation amplifier. Overlap programming is accomplished by connecting $\overline{\text{BUSY}}$ to $\overline{\text{STROBE}}$ and S/H CONTROL; DELAY OUT to LOAD and $\overline{\text{TRIG}}$. In this mode of operation the address of the next channel to be converted is latched and the output of the external instrumentation amplifier allowed to settle to a new value during the present conversion.

DIGITAL INPUT SPECIFICATIONS

Address Inputs (A0 - A3)	One standard LSTTL load, positive true
Address Coding	4-bit binary
LOAD	One standard LSTTL load, positive true, address loaded on positive edge.
$\overline{\text{CLEAR}}$	One standard LSTTL load, negative true, low level clears address latch.
$\overline{\text{STROBE}}$	One standard TTL load, high-to-low transition triggers the delay timer.
$\overline{\text{TRIG}}$	One standard TTL load, a negative going edge initiates the A/D conversion.
SHORT CYCLE	One standard LSTTL load, logic 1 for 12-bit resolution. Connect to "8-bit" or "10-bit" for 8- or 10-bit resolution.
$\overline{\text{ENABLE 1}}$, $\overline{\text{ENABLE 2}}$, $\overline{\text{ENABLE 3}}$, DT1 $\overline{\text{ENABLE}}$, BUSY $\overline{\text{ENABLE}}$	One standard LSTTL load, a low level enables the 3-state output.
S/H CONTROL	TTL compatible, 10μA maximum input current. Logic 0 = Hold mode, Logic 1 = Sample (track) mode.
MUX ENABLE 2	TTL compatible, 2μA input current, logic 0 enables multiplexer 2 (channels 8-15).

DIGITAL OUTPUT SPECIFICATIONS

Parallel Data Outputs	5 standard TTL loads, positive true 3-state.
Serial Output	2 standard TTL loads, positive true, NRZ, time serial data output beginning with DT1 (see Timing Diagram).
$\overline{\text{DT1}}$	5 standard TTL loads, positive true, 3-state.
$\overline{\text{BUSY}}$	5 standard TTL loads, low during A/D conversion.
BUSY	5 standard TTL loads, high during A/D conversion, 3-state
CLOCK OUT	5 standard TTL loads, for synchronizing serial out data (see Timing Diagram).
Address Outputs (A0 - A3)	5 LSTTL or 2 standard TTL loads, positive true
DELAY OUT	5 standard TTL loads, high during delay period, triggered by Strobe input.
SIN/DIF	5 LSTTL or 2 standard TTL loads, high while addressing channels 0-7, low while addressing channels 8-15.

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS				
Resolution	12			Bits
Number of Analog Channels		16SIN/8DIF		
Throughput Rate Normal mode				
SDM854AG	33	35		kHz
SDM854BG	25	27		kHz
Throughput Rate Overlap mode				
SDM854AG	38	40		kHz
SDM854BG	27	29		kHz
ANALOG INPUTS				
ADC Input Voltage Ranges		0 to +10, ±5, ±10		V
Mux Input Voltage Range				
Absolute max without damage			±35	V
For linear operation			±15	V
Mux Input Impedance, OFF Channel			10^{11}	Ω
Mux Input Impedance, ON Channel		1.5	1.8	kΩ
Input Leakage, OFF Channel		0.02		nA
Output Leakage, All Channels Disabled		0.2		nA
Output Leakage with Input Overvoltage of				
+35V		1		nA
-35V		1		μA
TEMPERATURE STABILITY				
System Accuracy				
Unipolar		±15	±25	ppm/°C
Bipolar		±10	±20	ppm/°C
Linearity Drift			±2	ppm/°C of FSR
REFERENCE VOLTAGES				
Positive Output	+2.490	+2.500	+2.510	V
Positive Output Drift		±5	±10	ppm/°C
Negative Output	-6.0	-6.4	-6.8	V
Negative Output Drift		±15	±10	ppm/°C
ACCURACY				
Throughput Accuracy				
0 to +10V, ±5V, ±10V, AG			±0.048	% of FSR(1)
0 to +10V, ±5V, ±10V, BG			±0.024	% of FSR
Linearity				
AG			±0.024	% of FSR
BG			±0.012	% of FSR
Differential Linearity				
AG		±0.024	±0.048	% of FSR
BG		±0.012	±0.024	% of FSR
Quantizing Error			±0.012	% of FSR
System Gain Error(2)		±0.1	±0.3	%
System Offset Error(2)		±0.1	±0.3	% of FSR
Power Supply Sensitivity +15V		±0.0007		%/%ΔV
Power Supply Sensitivity -15V		±0.0007		%/%ΔV
Power Supply Sensitivity +5V		±0.001		%/%ΔV
DYNAMIC ACCURACY				
Sample/Hold Characteristics				
Aperture Time		100		nsec
Acquisition Time		10		μsec
Feedthrough 10V step		±1.4		mV
OUTPUTS				
Digital Output Coding		Binary, Offset Binary, Two's Complement		
Serial Output Coding		Nonreturn to zero NRZ		
ADC Conversion Time(3)		25	30	μsec
Clock Frequency(3)		520		kHz
Delay(4)		15		μsec

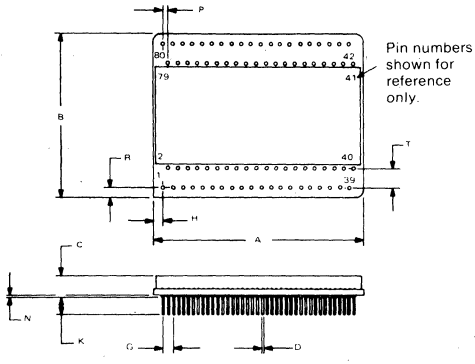
PARAMETER	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS				
Rated Voltage for Specified Accuracy	±14.5	±15	±15.5	V
	+4.75	+5	+5.25	V
Quiescent Current				
+15VDC		+10	+20	mA
-15VDC		-35	-50	mA
+5VDC		+170	+220	mA
Power Dissipation		1300	1750	mW
ENVIRONMENTAL				
Specification Temperature Range	-25		+85	°C
Operating Temperature Range	-40		+85	°C
Storage Temperature Range	-55		+125	°C

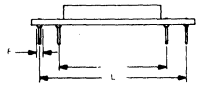
NOTES:
1. FSR means Full Scale Range. FSR is 20V for ±10V range.
2. Adjustable to zero.
3. Conversion time and clock frequency can be externally adjusted from 13μsec f_{clock} = 1.0MHz to 110μsec f_{clock} = 118kHz. Conv. times are for 12-bit resolution. See Figure 9.
4. Can be externally adjusted from 3μsec to 300μsec.

PIN DESIGNATIONS

NC	1	80	NC
MUX OUT HI	2	79	NC
NC	3	78	MUX OUT LO
CH7	4	77	CH15/RET7
CH6	5	76	CH14/RET6
CH5	6	75	CH13/RET5
CH4	7	74	CH12/RET4
CH3	8	73	CH11/RET3
CH2	9	72	CH10/RET2
CH1	10	71	CH9/RET1
CH0	11	70	CH8/RET0
MUX ENABLE 2	12	69	NC
MUX ENABLE I/A3 OUT	13	68	S/H IN
SIN/DIF	14	67	S/H OFFSET ADJUST
A2 OUT	15	66	S/H CONTROL
A1 OUT	16	65	+15VDC
A0 OUT	17	64	-15VDC
$\overline{\text{CLEAR}}$	18	63	ANA COM
A0 IN	19	62	S/H OUT
A1 IN	20	61	-6.4V REF OUT
A2 IN	21	60	10V RANGE
A3 IN	22	59	BIPOLAR OFFSET
$\overline{\text{LOAD}}$	23	58	20V RANGE
$\overline{\text{BUSY}}$	24	57	+2.5V REF IN
DIG COM	25	56	$\overline{\text{ENABLE 2}}$
SHORT CYCLE	26	55	+2.5V REF OUT
10-BIT RESOLUTION	27	54	$\overline{\text{ENABLE 1}}$
8-BIT RESOLUTION	28	53	$\overline{\text{ENABLE 3}}$
D0 LSB	29	52	SERIAL OUT
D1	30	51	CLOCK OUT
D2	31	50	CLOCK RATE ADJUST
D3	32	49	+5VDC
D4	33	48	$\overline{\text{STROBE}}$
D5	34	47	DELAY ADJUST
D6	35	46	$\overline{\text{TRIG}}$
D7	36	45	DELAY OUT
D8	37	44	$\overline{\text{D11}}$
D9	38	43	BUSY
D10	39	42	BUSY $\overline{\text{ENABLE}}$
D11 MSB	40	41	$\overline{\text{D11}}$ $\overline{\text{ENABLE}}$

MECHANICAL





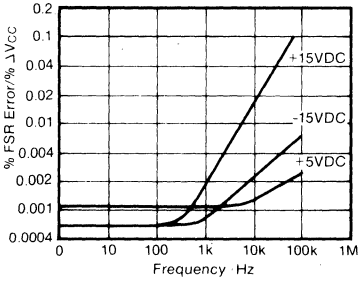
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	

NOTE:
Leads in true position within 0.015" 0.38mm R at MMC at seating plane.

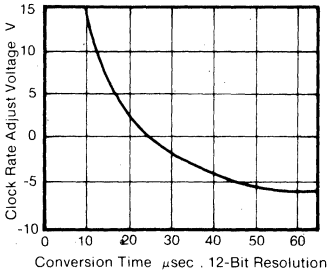
MATERIAL: Ceramic
WEIGHT: 32 grams 1.2 oz
MATING CONNECTOR:
2350MC set of four 20-pin strips or
0422MC assembled unit

TYPICAL PERFORMANCE CURVES

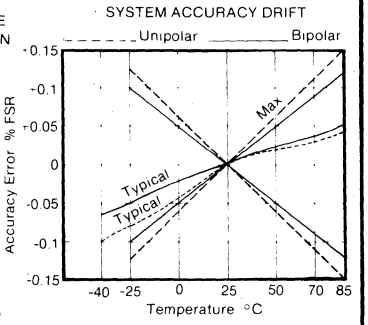
POWER SUPPLY REJECTION VS POWER SUPPLY RIPPLE FREQUENCY



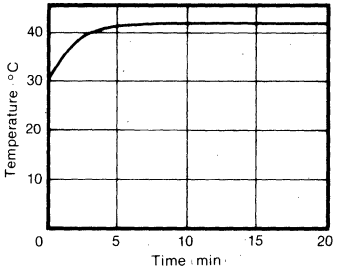
A/D CONVERSION TIME VS CLOCK RATE CONTROL VOLTAGE, 12-BIT RESOLUTION



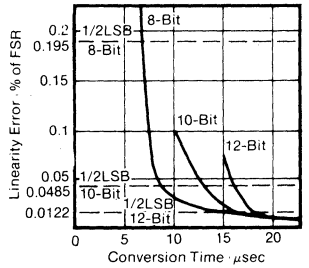
SYSTEM ACCURACY DRIFT



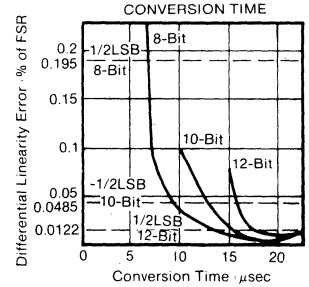
CASE TEMPERATURE VS TIME WITH NO HEAT SINK OR AIR FLOW



A/D CONVERTER LINEARITY ERROR VS CONVERSION TIME



A/D CONVERTER DIFFERENTIAL LINEARITY ERROR VS CONVERSION TIME



SDM854

DESCRIPTION OF PIN FUNCTIONS

NUMBER	DESIGNATION	DESCRIPTION
Pin 1	NC	No connection.
Pin 2	MUX OUT HI	High output of the analog input multiplexer. Connect to pin 78 (MUX OUT LO) and pin 68 (S/H IN) for single-ended input operation.
Pin 3	NC	No connection.
Pins 4 thru 11	CH7-CH0	The first 8 (of 16) analog inputs for single-ended operation or for 8-channel differential input operation.
Pin 12	MUX ENABLE 2	Connect to pin 14 (SIN/DIF) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.
Pin 13	MUX ENABLE 1 A3 OUT	Leave open for single-ended input operation. Connect to pin 12 (MUX ENABLE 2) for differential input operation. Also, A3 output line.
Pin 14	SIN/DIF	Single/Differential input operation. Connect to pin 12 (MUX ENABLE 2) for single-ended operation. Leave open for differential input operation.
Pins 15, 16, 17	A0 OUT - A2 OUT	Output lines from input channel address latch (A3 OUT is on pin 13).
Pin 18	$\overline{\text{CLEAR}}$	A low on this line clears the address latch causing the SDM854 to address channel 0 regardless of the information present on A0 IN - A3 IN. Connect to +5VDC or to user logic circuitry.
Pins 19, 20, 21, 22	A0 IN - A3 IN	Address lines that select one of 16 analog input signals (CH0-CH15). 0000 selects channel 0 and 1111 selects channel 15. Connect A3 to ground for 8-channel differential operation. The address is latched with a positive TTL edge on the LOAD (pin 23).
Pin 23	LOAD	A positive TTL edge on this pin latches the input channel address present on A0 IN - A3 IN (pins 19, 20, 21, 22).
Pin 24	$\overline{\text{BUSY}}$	This signal will be low during the A/D conversion (≈25μsec). Output data is not valid while this signal is low. Connect to S/H CONTROL (pin 66).
Pin 25	DIG COM	Digital common. Connect to ANA COM (pin 63) as close to the SDM854 as possible.
Pin 26	SHORT CYCLE	This pin allows short cycling the A/D converter for lower resolutions thereby obtaining faster conversion times. Connect to +5VDC (pin 49) for 12-bit resolution, (pin 27) for 10-bit resolution, or (pin 28) for 8-bit resolution.
Pin 27	10-BIT RESOLUTION	To short cycle to 10-bit resolution connect to pin 26. Otherwise, make no connection.
Pin 28	8-BIT RESOLUTION	To short cycle to 8-bit resolution, connect to pin 26. Otherwise, make no connection.
Pins 29 thru 40	D0-D11	12-bit data bus, 3-state low power Schottky TTL-compatible.
Pin 41	$\overline{\text{D11 ENABLE}}$	$\overline{\text{D11}}$ (pin 44) is enabled when $\overline{\text{D11 ENABLE}}$ is low.
Pin 42	BUSY $\overline{\text{ENABLE}}$	BUSY (pin 43) is enabled when BUSY $\overline{\text{ENABLE}}$ is low.
Pin 43	BUSY	3-state output that will be high only while an A/D conversion is in process. Output data is not valid while this signal is high.
Pin 44	$\overline{\text{D11}}$	$\overline{\text{MSB}}$. Use instead of D11 when two's complement output is required.
Pin 45	DELAY OUT	This pulse is used to delay the beginning of the A/D conversion to allow for the settling of the multiplexer and sample/hold.
Pin 46	$\overline{\text{TRIG}}$	A negative TTL edge on this pin initiates the A/D conversion. Connect to DELAY OUT (pin 45).
Pin 47	DELAY ADJUST	When the SDM854 is addressed, an internal delay of approximately 15μsec is initiated to allow for multiplexer and sample/hold settling time. The delay can be shortened for faster lower-resolution operation.
Pin 48	$\overline{\text{STROBE}}$	A negative TTL edge on this pin initiates the DELAY OUT pulse.
Pin 49	+5VDC	+5VDC at 200mA maximum, 170mA typical.
Pin 50	CLOCK RATE ADJUST	Varying the voltage at this pin changes the clock frequency and thereby changes the conversion speed of the A/D converter. Connect to DIG COM (pin 25) for 12-bit operation (25μsec A/D conversion time). Connect to +5VDC for 10-bit operation and connect to +15VDC for 8-bit operation (see page 11).
Pin 51	CLOCK OUT	A/D converter clock output. Output is present only during A/D conversion. N + 1 TTL pulses are output at a 520kHz rate where N is the resolution.
Pin 52	SERIAL OUT	Serial output data in NRZ format is synchronous with CLOCK OUT (pin 51) signal. Use negative edge of CLOCK OUT to strobe each bit.
Pins 53, 54, 56	$\overline{\text{ENABLE 3}}$ $\overline{\text{ENABLE 1}}$ $\overline{\text{ENABLE 2}}$	3-state enable lines for data bus D11 - D0 (MSB = D11). $\overline{\text{ENABLE 1}}$ (pin 54) enables D11 - D8; $\overline{\text{ENABLE 2}}$ (pin 56) enables D7 - D4; $\overline{\text{ENABLE 3}}$ (pin 53) enables D3 - D0. A low on the enable line enables data outputs.
Pin 55	+2.5V REF OUT	Positive voltage reference output. Connect to REF IN (pin 57) (through 50Ω) for unipolar or bipolar operation (unless an external reference is used). Also connect to BPO (pin 59) (through 25Ω) for bipolar operation.
Pin 57	+2.5V REF IN	Reference voltage input. Connect to +2.5V REF OUT (pin 55) (through 50Ω resistor or 100Ω pot) or use external +2.5V reference (+2.5V ±10mV at 0.5mA required).
Pin 58	20V RANGE	**A/D converter input resistor. Leave open unless an external 1A with a gain greater than 2 is used. (Input multiplexers are limited to ±10V maximum input voltage.)**
Pin 59	BIPOLAR OFFSET	A/D converter bipolar offset. Connect to REF OUT (pin 55) through a 25Ω resistor or a 50Ω pot for bipolar operation. Leave open for unipolar operation.
Pin 60	10V RANGE	A/D converter input resistor. Using without 1A: connect to S/H OUT (pin 62) for ±5V max input operation.
Pin 61	-6.4V REF OUT	Negative voltage reference output. Maximum current drain from this point without degradation of specifications is 200μA.
Pin 62	S/H OUT	Sample/hold output. Connect to 10V RANGE (pin 60) or 20V RANGE (pin 58) for normal operations.

DESCRIPTION OF PIN FUNCTIONS [CONT]

NUMBER	DESIGNATION	DESCRIPTION
Pin 63	ANA COM	Analog common. Connect to DIG COM (pin 25) as close to the SDM854 as possible.
Pin 64	-15VDC	-15VDC at 30mA typical.
Pin 65	+15VDC	+15VDC at 30mA typical.
Pin 66	S/H CONTROL	A low signal on this line causes the sample/hold to enter the hold mode. Connect to $\overline{\text{BUSY}}$ (pin 24).
Pin 67	S/H OFFSET ADJUST	Offset adjust for sample/hold (see Figure 8).
Pin 68	S/H IN	Input to sample/hold amplifier. Connect to MUX OUT HI (pin 2) and MUX OUT LO (pin 78).
Pin 69	NC	No connection.
Pins 70 thru 77	CH8-CH15 RE10 - RE17	Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
Pin 78	MUX OUT LO	Multiplexer output for CH8-CH15 (single-ended) or RE10-RE17 (differential). Connect to MUX OUT HI (pin 2) and S/H IN (pin 68) for single-ended operation.
Pin 79	NC	No connection.
Pin 80	NC	No connection.

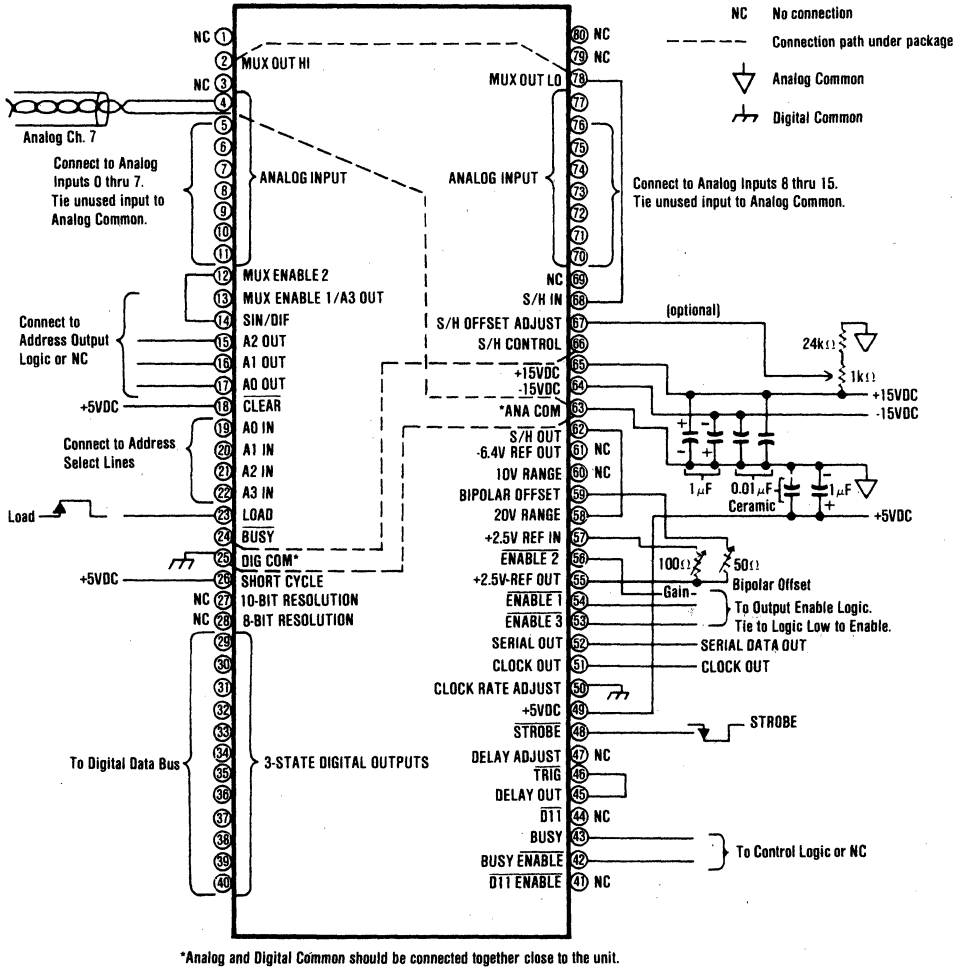


FIGURE 2. Connection Diagram for SDM854 Operating Under These Conditions:
Analog Input: Bipolar, single-ended; Reference Voltage: Internal; Resolution: 12-bits; Mode: Normal; Digital Output: Binary.

SETUP PROCEDURE

INPUT CONNECTIONS

Unused analog inputs must be connected to ANA COM, pin 63. When long leads are connected to the inputs, care must be taken that leads do not pick up excessive noise from external equipment and wiring. When low-level applications are undertaken, it is usually advisable to operate the system as an 8-channel, differential input system. This will require an external differential amplifier to be wired in between the output of the multiplexer and the sample hold amplifier. In this way any noise will be common to both input wires, and will be rejected by the instrumentation amplifier. For best noise rejection use twisted shielded pair cable. The inputs of the SDM854 are protected from damage by voltage as high as ±35 volts and from short spikes well in excess of this for a few microseconds; however, careful wiring and cable routing practices are recommended.

Single-Ended Inputs

For single-ended inputs connect pin 2 and pin 78 (MUX OUT HI and MUX OUT LO) to pin 68 (SAMPLE HOLD amplifier input), all unused inputs to the multiplexer and all signal returns to pin 63 (ANA COM).

Differential Inputs With External Instrumentation Amplifier

Connect the signal inputs to pins 4 through 11, and their returns to 77 through 70. Connect pin 12 to 13. Connect pins 2 and 78 to the noninverting and inverting input of the amplifier respectively. The output of the amplifier is connected to pin 68.

SAMPLE/HOLD

Connect S H CONTROL, pin 66, to the ADC $\overline{\text{BUSY}}$ output, pin 24.

ANALOG-TO-DIGITAL CONVERTER INPUT VOLTAGE RANGE

The analog-to-digital converter is essentially a current input device having a current input range of 0 to 2mA. The input may be considered a virtual ground summing point. To convert voltage to current, a center tapped 10kΩ resistor is internally connected to this summing point. This is illustrated in Figure 3.

The interconnection of the ADC pins and the S H OUT, pin 62, are shown in Table I.

TABLE I. ADC Range Jumpers.

Input Range, V	Jumper
0 to +10	59 Open, 60 to 62, 58 Open
-5 to +5	59 to 55, 60 to 62, 58 Open
-10 to +10	59 to 55, 58 to 62, 60 Open

NOTE: Input ranges in Table I apply to ADC only.

OUTPUT CODE

For unipolar binary and offset binary use D11 (pin 40) for the most significant bit. Two's complement binary is obtained by using pin 44, $\overline{\text{D11}}$, as the most significant bit. One's complement code may be obtained by a different offset adjustment in the calibration procedure. Two's complement and one's complement codes are usually used only for bipolar signal ranges. For 12-bit resolution, SHORT CYCLE (pin 26) is left open or taken to +5VDC. Connect pin 26 to pin 27 (10-bit) or pin 28 (8-bit) to obtain lower resolution. The conversion time will be shortened by the following formula:

(Conversion Time) = (25μsec) x [1 - (12-R 13)]
where R is the resolution desired.

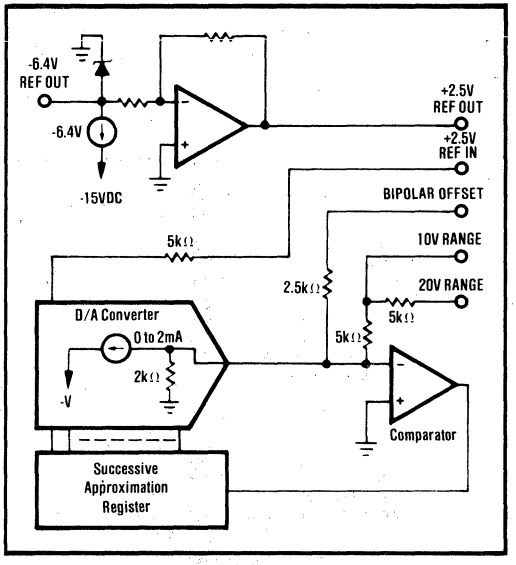


FIGURE 3. Analog-to-Digital Converter.

NORMAL AND OVERLAP MODE

The two basic modes of system operation are normal and overlap. In normal operation the channel address, N, is loaded or clocked into the address latch. The addressed channel will remain selected during its analog-to-digital conversion. In overlap mode channel N + 1 is selected while channel N is being converted. This can be used to increase the system throughput rate by allowing the multiplexer and external instrumentation amplifier to settle while a conversion is being made. In this way the throughput rate is limited by the sample hold acquisition time and the analog-to-digital converter conversion time. For this reason, the overlap mode is more desirable for low-level signals. Table II and Figures 4 and 5 provide additional timing details. At high signal levels a high source resistance may increase the multiplexer settling time to an extent which makes the overlap mode desirable.

Normal Mode Connections

Connect DELAY OUT, pin 45 to $\overline{\text{TRIG}}$, pin 46.

Overlap Mode Connections

Connect $\overline{\text{BUSY}}$, pin 24 to $\overline{\text{STROBE}}$, pin 48, and DELAY OUT, pin 45 to TRIG, pin 46. Adjust the delay as

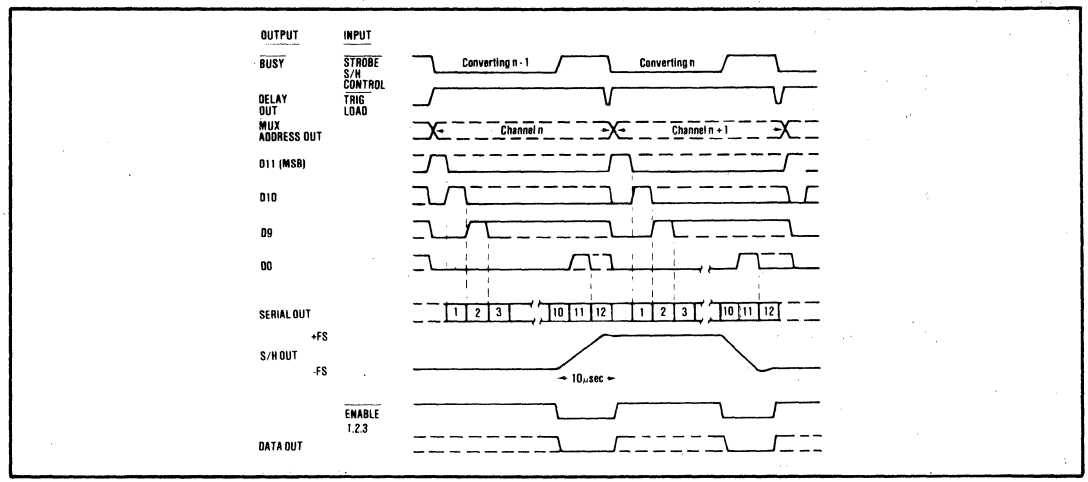


FIGURE 4. System Timing for Overlap Operation.

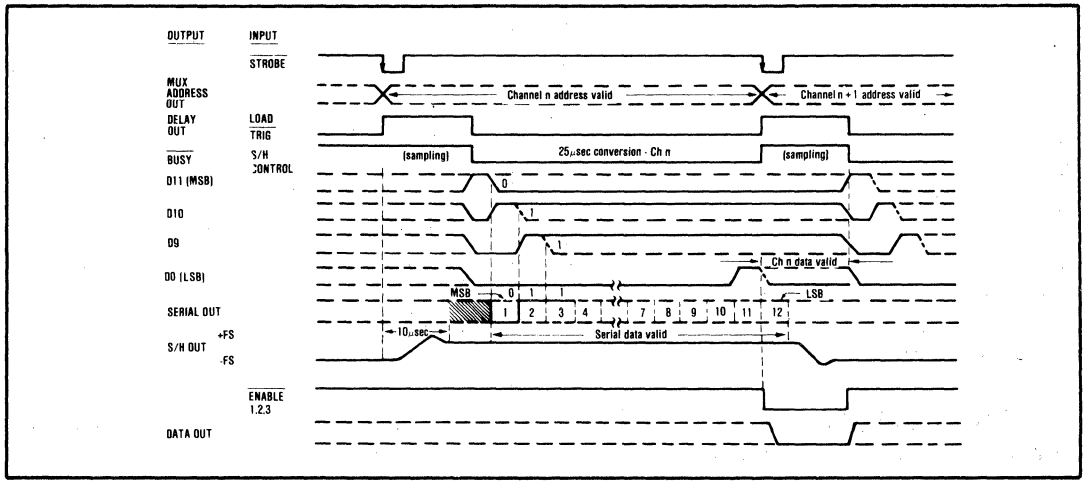


FIGURE 5. System Timing for Normal Operation.

described in the following paragraph.

DELAY ADJUSTMENT

The delay timer may be adjusted with an external capacitor or resistor from DELAY ADJUST (pin 47) to +5VDC. A capacitor will increase the delay to allow for increased settling time while a resistor will decrease the delay to allow for increased throughput rate with an external high speed instrumentation amplifier or lower resolution operation.

The values of R and C versus delay are shown in Figures 6 and 7.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

GROUNDING CONSIDERATIONS

The circuit configuration of a high speed successive approximation A/D converter is such that low-level analog and digital signals are in close proximity. In fact the two circuits are actually interconnected; for this reason no AC noise voltage should be allowed to exist between digital and analog ground. Digital and analog ground should be connected as close to the unit as possible. In a typical application an SDM module will be used near a computer. For best results the SDM digital ground should be connected to the computer's +5VDC supply ground at the supply terminal. The ±15VDC supply ground should be connected to the +5VDC supply ground at the SDM only. The Burr-Brown Model 546 +5VDC to ±15VDC DC/DC converter is a convenient way to do this. For single-ended systems, signal returns are connected to analog ground.

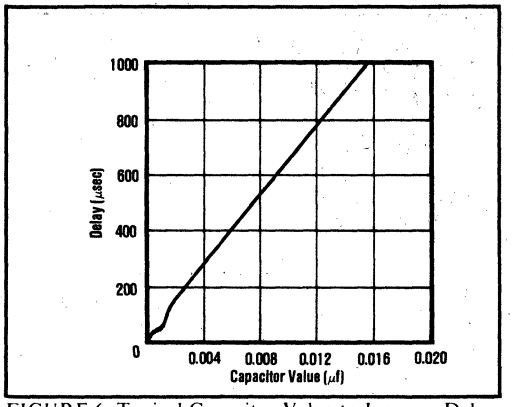


FIGURE 6. Typical Capacitor Value to Increase Delay Time*.

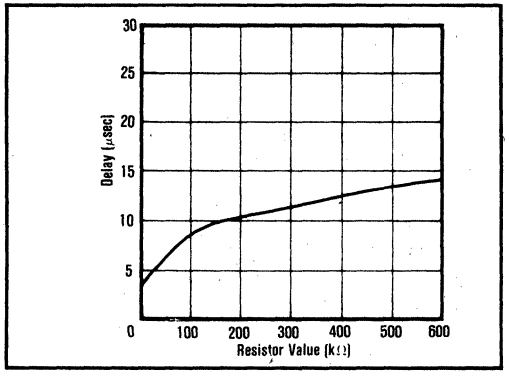


FIGURE 7. Typical Resistor Value to Decrease Delay Time.*

*Capacitor or resistor is connected from pin 47 to +5V supply.

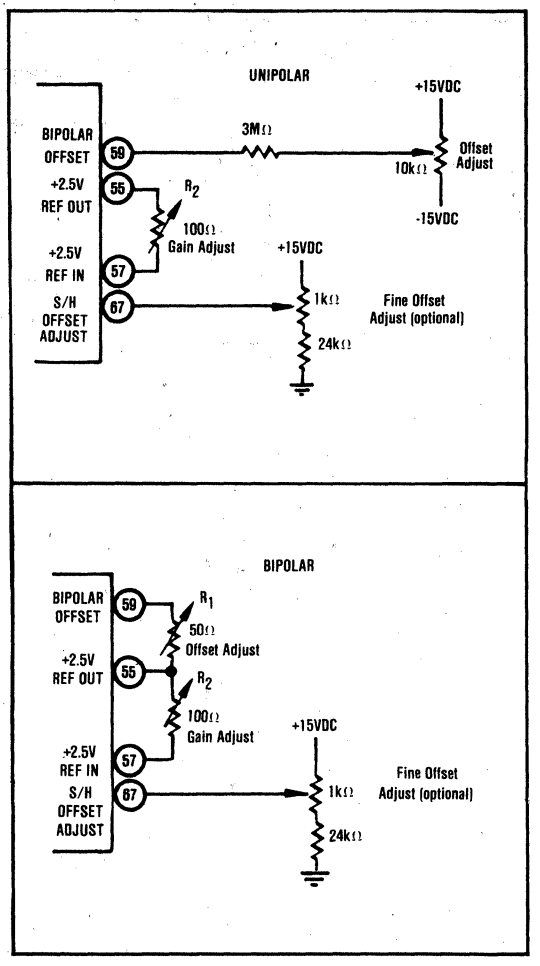


FIGURE 8. External Gain and Offset Adjustment.

CALIBRATION PROCEDURE

GAIN AND OFFSET ADJUSTMENT

External gain and offset adjustment potentiometers are shown in Figure 8. Cermet pots with a T.C.R. of ±100ppm °C or less should be used. The adjustments shown each have a range of ±0.3% of the Full Scale Range.

If adjustment of gain and offset is not required R1 and R2 should be replaced with 25Ω and 50Ω resistors respectively. These resistors should be low T.C. (<±100ppm °C) metal film or equivalent.

The S/H OFFSET ADJUST (pin 67) may be used as a fine offset adjustment.

The easiest way to calibrate the device is to connect a voltage source to multiplexer input CH0 (either differential or single-ended input operation may be used). Channel zero will be addressed by simply connecting $\overline{\text{CLEAR}}$ to DIG COM.

After the CH0 voltage source has been addressed, set it to the most negative value of the input range being used plus 1 2LSB. Twelve-bit LSB voltage values are given in Table III. Connect a triggering source to $\overline{\text{STROBE}}$ and adjust the offset potentiometer until all output bits are logic 0 with bit D0 dithering between logic 0 and 1. Change the source voltage to the most positive value of the input range minus 3 2LSB. Adjust the gain potentiometer until all output bits are logic 1 with bit D0 dithering between logic 1 and 0. When a resolution less than 12 bits is used, the LSB voltage is given by the formula in Table II where N is the number of output bits. One's complement coding is obtained by shifting the previous adjustments up by 1 2LSB using the offset potentiometer.

TABLE II. LSB Values for 12-Bit Resolution.

LSB Volts = Range / 2^N

Range	LSB Voltage 12-Bits
5V	1.22mV
10V	2.44mV

CLOCK RATE ADJUSTMENT

To obtain higher throughput rates at lower accuracy the A D clock rate can be adjusted by varying the voltage on the clock rate adjust pin. This point should be connected to digital common for 12-bit accuracy, +5VDC for 10-bit accuracy, or +15VDC for 8-bit accuracy giving conversion times of 25μsec, 15μsec and 10μsec respectively. The conversion speed can also be continuously varied from about 13μsec to 110μsec (12-bit resolution) with a potentiometer as shown in Figure 9.

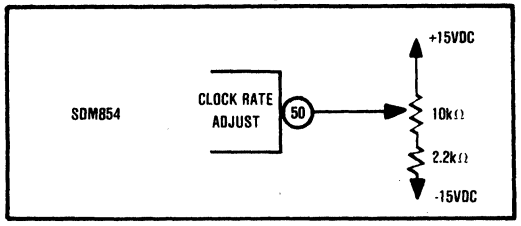


FIGURE 9. Clock Rate Adjustment.

CHECKOUT PROCEDURE

Checkout is essentially accomplished by the calibration procedure. Before the unit is plugged into a new installation, it is well to go over the pin connection list to be sure that all 80 pins have been properly connected in the setup. Linearity and monotonicity may be verified by varying the input voltage over the complete range during the calibration procedure.

LATCH

Latch operation can be verified by connecting a pulse generator to the LOAD input. The address inputs (A0 IN - A3 IN) should appear at the address outputs (A0 OUT -A3 OUT).

MULTIPLEXER

To check the multiplexer connect a voltmeter to the multiplexer output (pin 2 and pin 78) and observe that the output changed when the address was changed.

SAMPLE/HOLD

The sample hold circuit can be checked during the calibration procedure by observing the output of the S H OUT (pin 62) with an oscilloscope. The waveform should be approximately as in Figure 10.

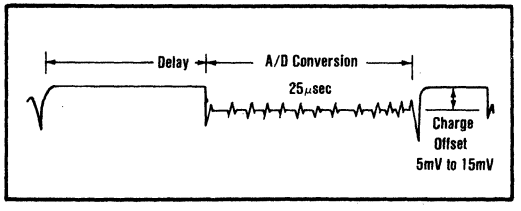


FIGURE 10. Sample Hold Output Waveform.

The charge offset will vary in a linear manner from about 5mV for -10V to 15mV for +10V. This is compensated for by the offset and gain adjustments of the A D converter. The spikes during conversion are normal noise caused by the converter operation.

ANALOG-TO-DIGITAL CONVERTER

The ADC can be checked out as an individual circuit element. Connect a fixed voltage to either 20V RANGE (pin 58) or 10V RANGE (pin 60). After adjusting the gain and offset errors as described on page 10, the digital output should represent the analog input as shown in Table III. To enable the three-state buffers, pins 53, 54 and 56 should be connected to logic 0.

TABLE III. Delay Timer Settings for Specified Settling Time Accuracies Using an External Burr-Brown 3630 Instrumentation Amplifier.

Full Scale Input Range	ADC Range	Amplifier Gain	Resolution	Delay Timer Setting μsec		
				To ±0.2%	To ±0.05%	To ±0.01%
20V ±10V	-10 to +10	1	4.88mV	60	75	100
1V	0 to +10	10	244μV	50	60	75
0.1V	0 to +10	100	24.4μV	100	115	150
10mV	0 to +10	1000	2.44μV	500	700	1000

In overlap, when the external amplifier multiplexer settling time is less than the ADC conversion time, set the delay timer for the ADC conversion time plus the sample hold acquisition time (30μsec plus 10μsec). When the external amplifier multiplexer settling time exceeds the ADC conversion time plus the S H acquisition time, set the delay timer for the external amplifier multiplexer time.

APPLICATION NOTES

CHANNEL CAPACITY EXPANSION

The SDM854 may be easily expanded to any number of channels by using Burr-Brown Models MPC8D and MPC16S. The MPC8D is an 8-channel double-ended multiplexer, and the MPC16S is a 16-channel single-ended multiplexer. The devices are CMOS FET units which can operate from supply voltages up to ±20VDC. They feature latch-free operation with full input protection. Binary decoding and level shifting circuits are included. Logic levels are jumper selectable for TTL or CMOS. Packaging is a 28-pin DIP.

There are two methods for using these devices for channel capacity expansion. The SDM854 multiplexer may be expanded by shunt or series connected multiplexers. Shunt connection refers to connecting the output of several multiplexers together and enabling each in sequence. The disabled devices present a very high resistance to the common output line. The disadvantages to this scheme are increased leakage current and output capacitance. For these reasons shunt connections are usually used only when it is desired to expand the capacity by a factor of two or three. A shunt connected system logic diagram is shown in Figure 11. Forty-eight single-ended

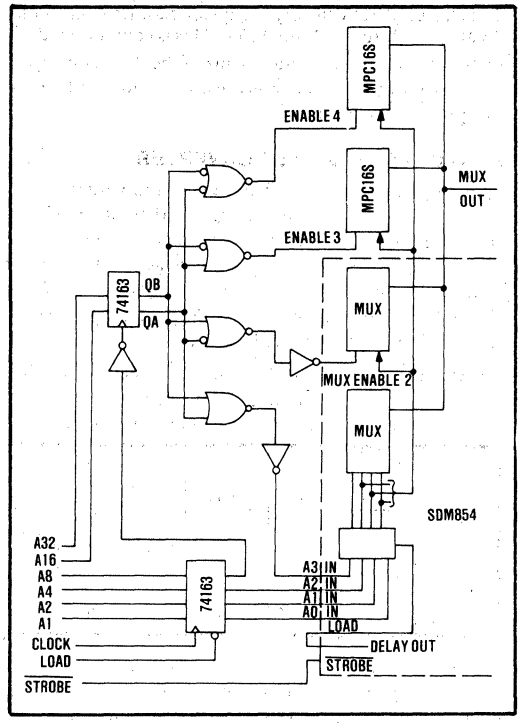


FIGURE 11. Shunt Connected Multiplexer System, 32 Single-Ended Channels.

channels are indicated; however, 24 double-ended channels could easily be realized by using two MPC8D's and connecting the two-sided outputs appropriately. For large systems series connected expansion is usually used. In this method the outputs of a second tier of multiplexers are connected to the inputs of the SDM854 multiplexer. This allows up to 256 single-ended or 128 double-ended channels to be addressed. A third tier can be used for 4096 single or 2048 double-ended channels. A logic diagram of a series system is shown in Figure 12. Double-ended operation can be obtained by using the MPC8D instead of the MPC16S and connecting the SDM854 for double-ended operation.

SEQUENTIAL ADDRESSING

Simply adding an external counter will allow sequential addressing of all 16 input channels (see Figure 13).

MULTIPLEXER CIRCUIT OPERATION

At the address and enable inputs a voltage is interpreted as a logic "1" if it is greater than 2.4 volts; and "0" if less than 0.8 volts.

When an input channel has been selected the "on resistance" from input to output is 3kΩ. The input capacitance for each channel is approximately 7pF, while the output capacitance is approximately 25pF for each 8-channel multiplexer. A circuit model of an ON channel is shown in Figure 14.

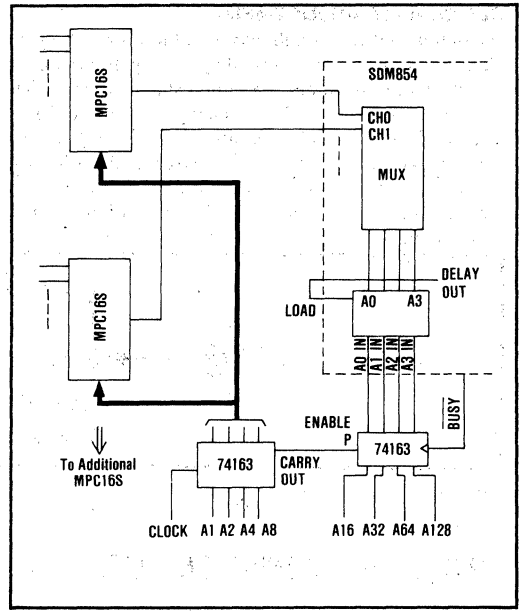


FIGURE 12. Series Connected Multiplexers, 256 Single-Ended Channels (Sequential Addressing).

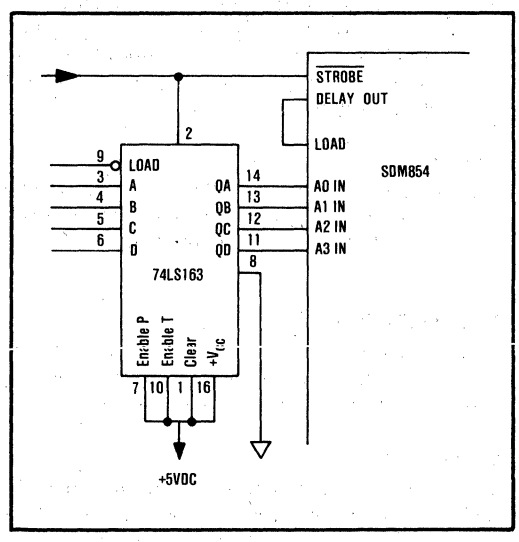


FIGURE 13. Sequential Addressing.

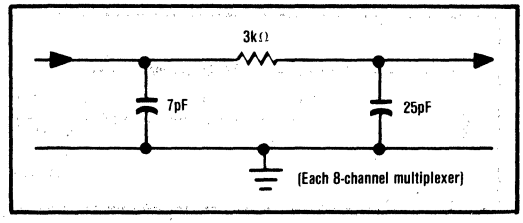


FIGURE 14. ON Channel Circuit Model.

This model is very important when high speed switching of high output impedance sources is required. For example, if the full accuracy and resolution of the system is required, the signal at the output of the multiplexer must be allowed to settle to about 0.01%. If the source impedance is 1kΩ, the 7pF can be neglected and the multiplexer has a time constant of 2.8kΩ x 50pF = 140nsec. It requires approximately 9 time constants to settle to 0.01%; 1.26μsec is well within the 15μsec of the SDM854 delay timer. However, if the source impedance had been 10kΩ, the 0.01% settling time would have approached 6μsec. For high speed multiplexing of higher impedance sources, it will usually be desirable to parallel the 7pF input capacitor with a large capacitor; however, this could limit the source bandwidth. In any case there is no point in making it any larger than 10^4 times the output capacitance, or 0.5μF. When this size storage capacitor is used, the output time constant is 1.8kΩ x 50pF = 90nsec. This means that the system settling time is essentially determined by the settling time of a differential amplifier and sample hold circuit. For switching of large signals it must be remembered that the ON resistance is the channel resistance of a FET, and, as such, it is a nonlinear function of the applied voltages. Any FET will current limit at its I_{DSS} value. As a result, the previous calculations are only an approximation derived from a linearized model. The settling time to 0.01% for a 20V step is approximately 4.0μsec for source impedance less than 1kΩ.

The analog and digital inputs have reverse biased diode circuits which prevent damage from discharge of static electricity. However, it is still wise to take reasonable preeaution against static discharge.

BINARY SCALING

Binary scaling of the A/D converter provides LSB voltages of 2.5mV, 2.5mV, and 5.0mV for voltage ranges of 0 to 10.24V, -5.12V to +5.12V, and -10.24V to ±10.24 respectively. These may be obtained by adding external resistors in series with input resistors of the A/D converter. Metal film resistors with temperature coefficients of less than 100ppm/°C are recommended. This is shown in Figure 15.

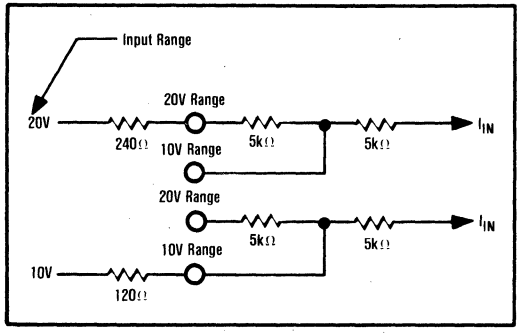


FIGURE 15. Binary Scaling.

USING AN INSTRUMENTATION AMPLIFIER WITH THE SDM854

When low-level signals are being converted, such as with thermocouples, strain gauges, etc., it will be necessary to use an instrumentation amplifier (IA) with the SDM854 to utilize the full dynamic range of a 12-bit system. This can be done by connecting the IA between the multiplexer and sample hold amplifier because the output of the multiplexer and the input of the sample hold amplifier are both brought out separately on the SDM854.

There are two ways an external IA can be connected to increase the versatility of the system. The most accurate way is to use the amplifier in a true differential mode as shown in Figure 16, where a Burr-Brown 3630 is connected

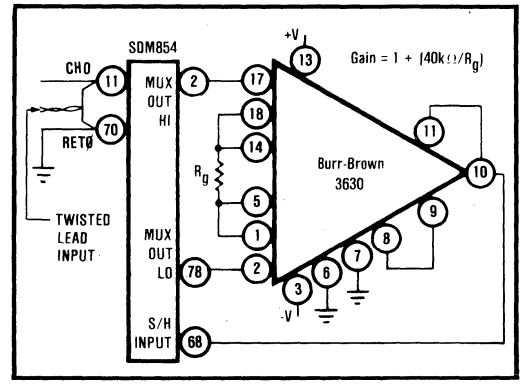


FIGURE 16. Instrumentation Amplifier Connection for True Differential Input.

to the SDM854 for differential operation. This configuration is ideal where the input lines run over a long distance or through noisy environments. For best results the input links should be in twisted shielded pairs with the shield grounded at one end to prevent ground loop currents from forming.

A second way to use an IA is in the pseudo-differential mode as shown in Figure 17. This method is ideal if all of

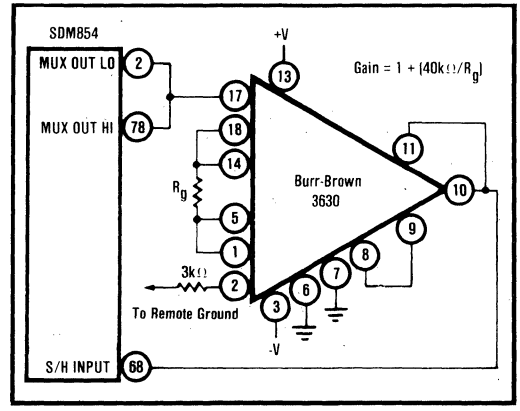


FIGURE 17. Instrumentation Amplifier Connection for Pseudo-Differential Input.

the input signals come from the same general area and at the same ground potential. In this application the inverted input of the IA can be used as a ground sense line. The IA will then reject the difference in ground potential and any common noise pick up from the ground sense line and the signal path. Care should be taken to match the impedance to ground from both inputs of the IA. This will insure the rejection of bias current effects from the IA. For better noise rejection the input lines should be grouped and shielded with the shield grounded at one end as in the true differential connection. One advantage of the pseudo-differential connection is that the multiplexers are operated in the single-ended mode allowing for 16 different input signals versus only 8 inputs in the true differential operation.

In both the true differential and pseudo-differential operation care should be taken in choosing the correct IA to maintain the high accuracy and linearity of the system.

Some of the important characteristics are:

1. Linearity error $\leq 0.012\%$ at all gains
2. Offset current drift ≤ 1 2LSB (Gain)$(R_{source})\Delta T$
3. CMRR $>$ CM_{signal} 1 2LSB
4. Offset voltage drift $<$ 1 2LSB (GAIN) ΔT
5. High input impedance $> R_{source} \times 10^4$

The importance of initial offsets are somewhat minimized by the capability to cancel out offset at several points in the system. The Burr-Brown 3630 was chosen for this application because of its high linearity, good drift spec and CMRR characteristics. Some of the accuracy calculations for the Burr-Brown 3630 are as follows:

Nonlinearity = $\pm 0.002 + 10^{-5}$ (Gain) % FS at G $\leq$ 100
nonlinearity is $\leq 0.003\%$ FS

Input impedance = $10^9\Omega$ so source impedance up to 100kΩ can be used.

Voltage offset drift at Gain = 100
0.25μV °C $\leq$ 1.22mV 100ΔT so $\Delta T \leq 49$°C
for errors $\leq$ 1 2LSB.

CMRR at Gain = 100 is 110dB

CM range = 10V 1.22mV = 78dB.

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10μV °C to 70μV °C and operating ranges of minus hundreds to plus thousands of degrees centigrade. When the SDM854 is operated with an external instrumentation amplifier gain of 100 to 1000, it may be connected directly to these devices. However, electronic instrumentation is usually mounted in a temperature controlled environment with long runs of thermocouple wire to the actual point of temperature measurement. These long wire runs often pick up large common-mode noise signals of 60Hz or higher frequencies. When the SDM854 is used as an 8-channel differential input system, the high common-mode rejection of the external instrumentation amplifier will reject common-mode noise. To minimize differential mode noise, signal wires should be twisted and possibly shielded. As a rule, an open twisted pair is better than a coax, and a shielded, twisted pair better still. In applications where these wiring practices cannot always be observed, a differential RC filter may be used (see Figure 18).

The 10kΩ resistors and a 10μF capacitor provide low-pass filtering ($f_c = 0.8$Hz) while the 1MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the $\pm$15V range of the multiplexer. This will usually supply bias current; however, the resistors provide a back up. It is not obvious what resistance the bias currents of the amplifiers will see. The 1MΩ resistors do not enter into an error calculation for input drift because the low resistance of the sensor shorts any differential current of the amplifier. Offset or difference current is merely the difference between the bias currents of each input. See page 15 for a worst-case error analysis of the input filter for multiplexed data acquisition systems. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the

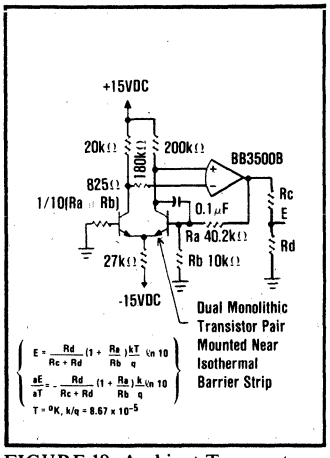


FIGURE 18. Ambient Temperature Sensor

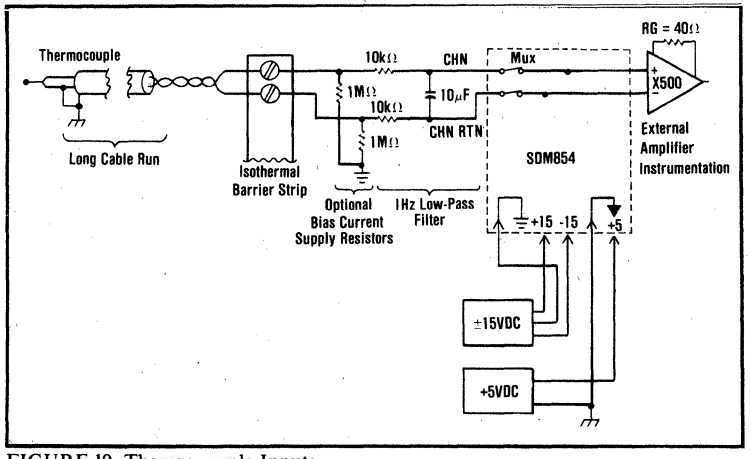


FIGURE 19. Thermocouple Inputs

need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip in an enclosed cabinet with even air circulation is usually adequate. The temperature of this barrier strip must be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 19 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer.

INPUT FILTER DESIGN FOR LOW-LEVEL SYSTEMS

When the SDM854 is used to acquire low-level sensor data, it is often desired to place a low-pass, passive filter on each input. This is usually done to reduce any differential mode, power line frequency pickup. Figure 20 shows such a circuit.

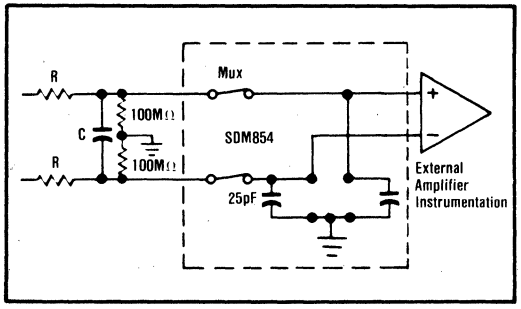


FIGURE 20. Input Filter Design for Low-Level System.

This circuit is deceptive in its simplicity. Actually four errors sources should be considered in its design. They are loading, offset current, charge transfer, and pump out current.

The static loading error is simply the resistive divider created by the filter resistors and the 100MΩ input resistance. For low-level sensors, 0.1% system accuracy is usually adequate. Thus R should be less than 10^{-3} x (100MΩ) = 100kΩ. However, if the inputs are scanned at a high speed, and between scans the multiplexer can be addressed to a unique channel having a lower resistance, higher filter resistance can be tolerated because the large filter capacitor will act as a voltage source during the 30μsec to 100μsec period required to read each channel. The filter capacitors will then recharge between scans.

The input offset current caused by the bias currents of the external instrumentation amplifier as well as any leakage current of the multiplexer will cause an error voltage proportional to the size of the filter resistors ($E = I_{OS} \times 2R$). Of course, this is a static error and as for loading error, may not be important for some operating conditions. If all channels have the same resistance most of this error may be corrected by the offset adjustment of the analog-to-digital converter. If the offset current drift is 0.1nA °C the error is 2R x 0.1nV °C. For 10kΩ resistors this would be 2μV °C.

When the multiplexer scans, charge will be transferred from the filter capacitor to the 25pF output capacitance of the multiplexer. For less than 0.1% of full scale error, the filter capacitor must be large than 25000pF. This assumes that adjacent channels may differ by the full scale voltage.

Pumpout current refers to charge being transferred from the filter capacitor to the multiplexer capacitance at time intervals short enough that the filter capacitor does not have time to recharge between scans. At high scan rates this may be considered a DC current which may add to the offset current. Assume a 10μF capacitor sampled once per millisecond. For a 20mV full scale range, the maximum effective current is (20mV x 25pF) 1msec = 0.5nA. If the filter resistors are 10kΩ, a 0.5nA x 20kΩ = 10μV error is created.

When no input filter is used, the signal source must be able to charge the multiplexers and any cable capacitance during the channel acquisition time of the multiplexer and external amplifier. This is discussed on page 13. When all of these errors as well as the basic 2.0μV °C input offset voltage drift of the external amplifier are considered, the overall system accuracy may be estimated.

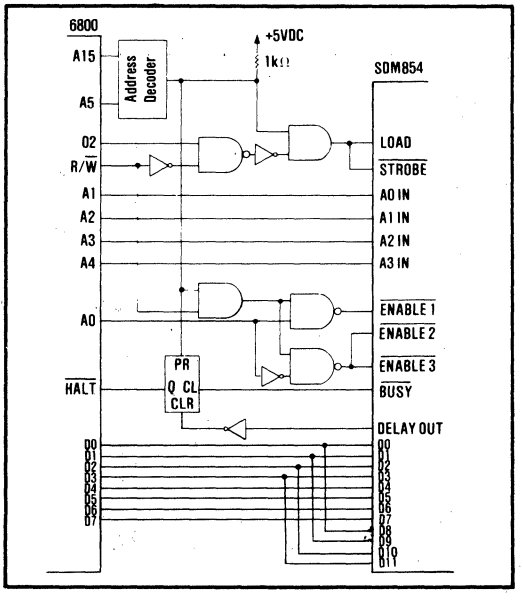


FIGURE 21. SDM854 Interfaced to 6800 Microprocessor.

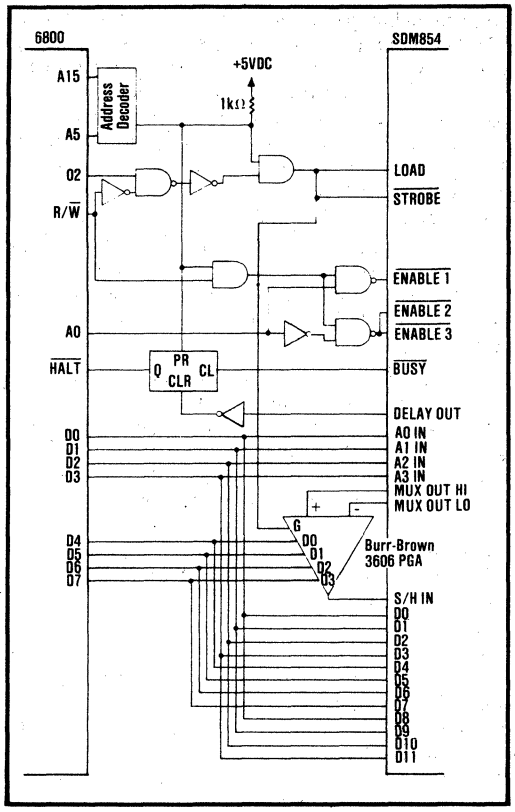


FIGURE 22. SDM854 and 3606 PGA Interfaced to 6800.

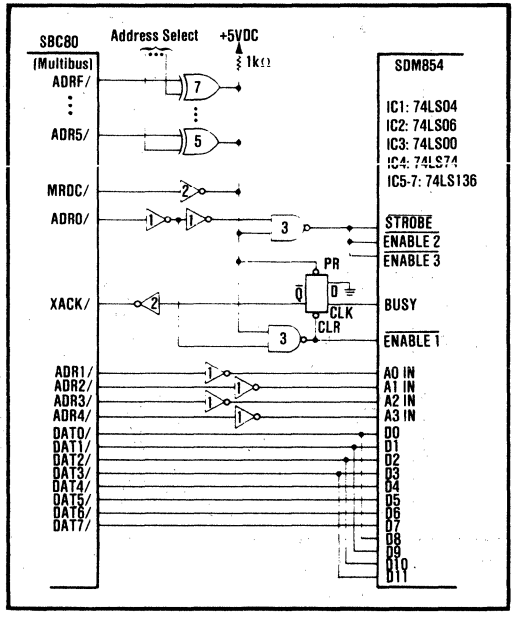


FIGURE 23. SDM854 Interfaced to SBC80 Multibus.

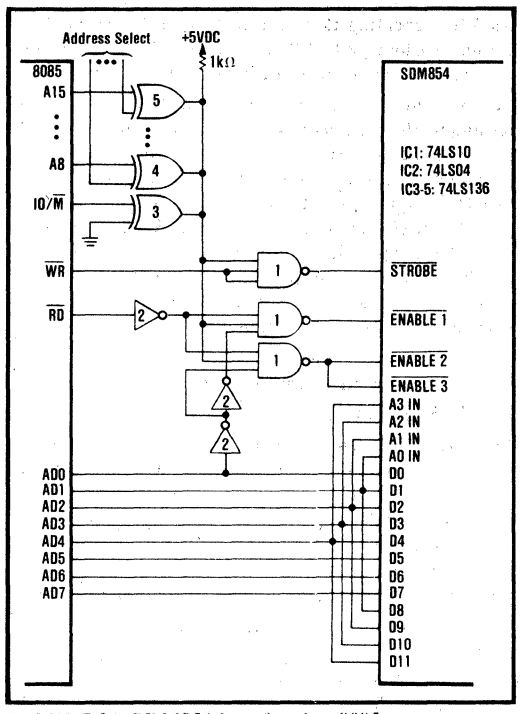


FIGURE 24. SDM854 Interfaced to 8085.

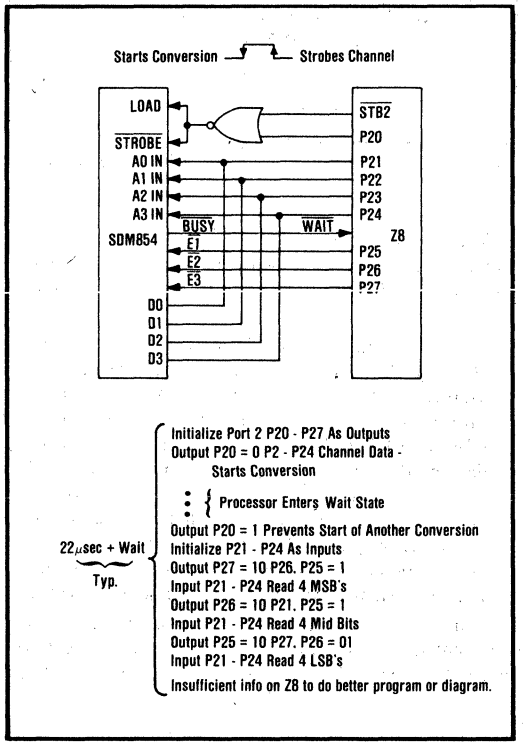


FIGURE 25. SDM854 Interfaced to Z8.

BURR-BROWN

SDM856
SDM857

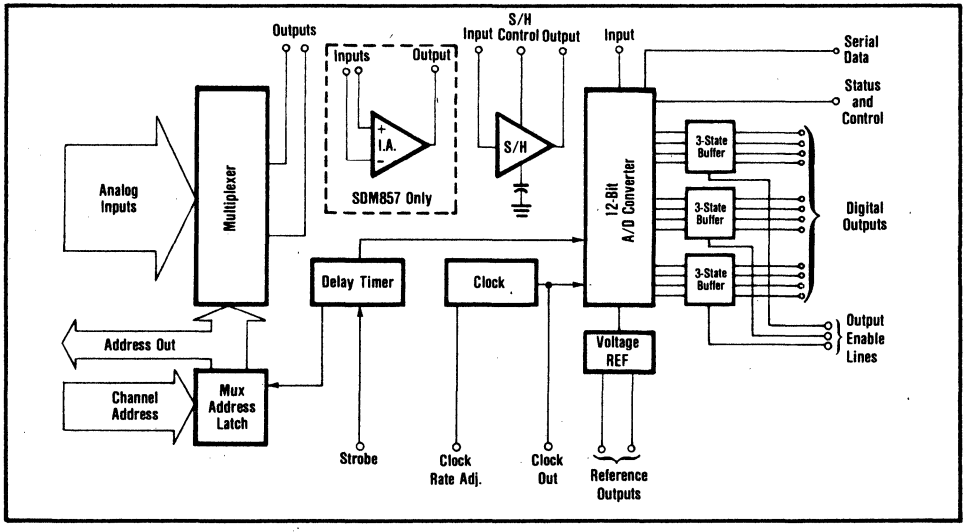
HYBRID DATA ACQUISITION SYSTEM

FEATURES

- MINIATURE SIZE
- LOW COST
- 12-BIT, ±0.012% LINEARITY ERROR
- INSTRUMENT AMP OPTION
- LOW LEVEL INPUTS (SDM857)
- SELECTABLE 16 SINGLE, 8 DIFFERENTIAL INPUTS
- THREE-STATE OUTPUT BUFFERS
- THROUGHPUT RATES (SDM857 Overlap Mode)
  - 8-Bit Accuracy: 70kHz
  - 10-Bit Accuracy: 32kHz
  - 12-Bit Accuracy: 29kHz

DESCRIPTION

The SDM856 and SDM857 are complete data acquisition systems contained in a miniature 2.2" x 1.7" x 0.22" ceramic package. These systems offer all the functions available in large modular data acquisition systems and are available with an optional internal instrumentation amplifier (SDM857). Inputs as low as ±10mV can be accepted by the SDM857; thermocouples, strain gages, and other low level signal sensors don't require external signal conditioning. Both models are fully expandable from the basic 16 channel single-ended or 8 channel differential input capability. Digital resolution is 12 bits with accuracy of ±0.024% at a throughput rate of 29kHz (SDM856KG).



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DISCUSSION OF PERFORMANCE

INTRODUCTION

SDM857 contains all components necessary to multiplex and convert analog signals as low as ±10mV and as high as ±5V into equivalent digital outputs. Throughput sampling rates are from 29kHz (12-bit resolution) to 70kHz (8-bit resolution) in the overlap mode of operation. A complete low drift instrumentation amplifier allows selection of gains from 2 to 500 with one external resistor. SDM856 is identical to SDM857, but does not include the instrumentation amplifier. This provides the option of adding an external instrumentation amplifier for specific requirements such as high speed, digital programming, etc. Both models can be configured to accept either 8-channel differential or 16-channel single-ended signals and can be expanded almost without limit with external multiplexers. Three-state outputs are provided for easy interface to microprocessor and other bus-structured systems. Figure 1 illustrates all system components which are described in the following paragraphs.

ANALOG MULTIPLEXER

The analog multiplexer consists of two CMOS integrated circuits. Pin interconnects are used to select 16 channel single-ended or 8 channel differential operation. In single-ended operation the multiplexer can be used in a pseudo-differential mode by connecting the amplifier inverting input to common remote signal ground. Channel selection is made by an internally latched 3 or 4 bit binary word, for differential or single-ended operation respectively.

INSTRUMENTATION AMPLIFIER (SDM857 only)

Offering low drift and high accuracy, the internal instrumentation amplifier may be programmed by a single external resistor for gains from 2 to 500. With gain programming pins open, the gain is 2.

SAMPLE AND HOLD

A complete stand alone circuit, the sample and hold amplifier features buffered output, 10μsec acquisition time, and 100nsec aperture time.

Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions, such as automatic gain ranging, with no loss of aperture time.

ANALOG TO DIGITAL CONVERTER

The ADC is a 12-bit, 25μsec converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight binary or two's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution.

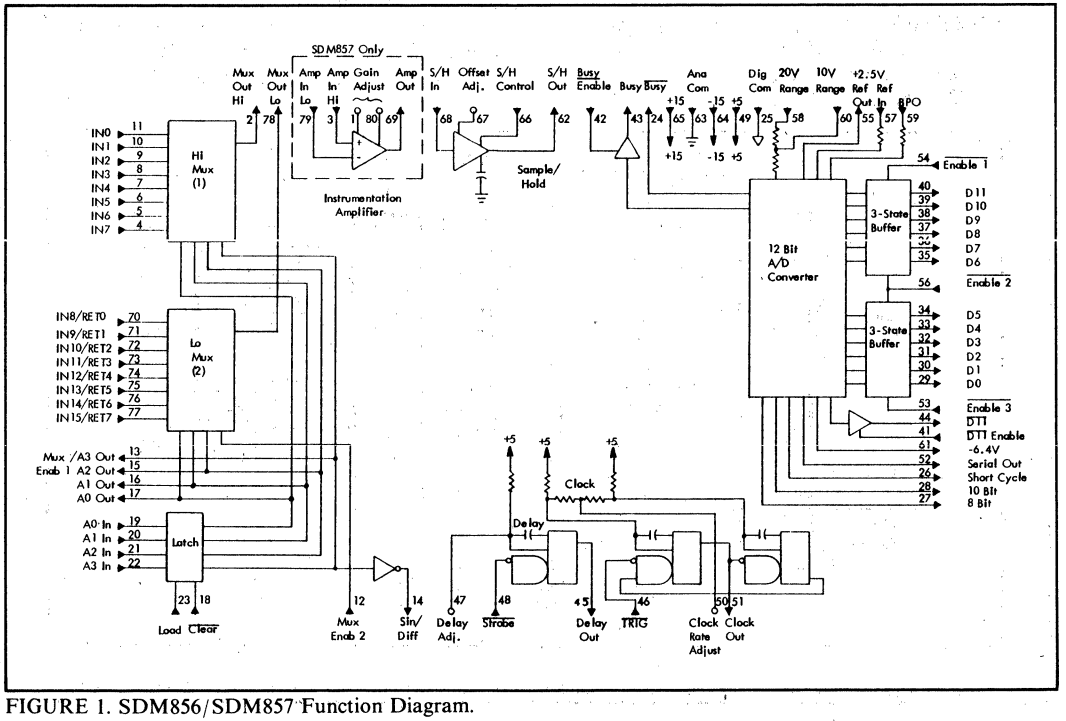


FIGURE 1. SDM856/SDM857 Function Diagram.

DISCUSSION OF PERFORMANCE (CONTINUED)

THREE-STATE OUTPUT BUFFERS

Digital outputs of the ADC are internally buffered by LSTTL three-state buffers. Three separate enable lines are brought out for easy interfacing to 4-, 8- or 16-bit data buses. $\overline{\text{MSB}}$ and BUSY are also buffered by separate three-state devices, each with its own enable line.

ADDRESS LATCH

Outputs of the 4-bit LSTTL register latch are connected to the address inputs of the multiplexer. This latch serves as an address storage register for the selected analog input. It may be loaded through 4 address inputs. Other inputs are LOAD and $\overline{\text{CLEAR}}$. The 3 least significant bits are used for 8 channel differential mode addressing.

DELAY TIMER

A delay timer allows settling time for the multiplexer, amplifier and sample/hold circuits before conversion begins. The delay is adjustable over a wide range by use of an external resistor or capacitor. This allows for longer settling time of the instrumentation amplifier when operating at high gains, or shorter settling time for lower resolution operation.

CHANNEL EXPANSION

The number of analog input channels of the SDM856 and SDM857 can be easily increased by using Burr-Brown's MPC8D (8 channel differential) and MPC16S (16 channel single-ended) multiplexers. These are latch-free devices which contain internal binary decoding at TTL or MOS levels and may be integrated into a system with minimal external logic.

SYSTEM PERFORMANCE

SDM856 and SDM857 are configured for random channel selection. With the addition of an external counter they can be configured to continuously sequence through all analog channels or sequence through all analog channels on command from an external trigger.

With the appropriate 4-bit (single-ended) or 3-bit (differential) channel address on the latch inputs, and DELAY OUT (pin 45) tied to the LOAD input (pin 23), a negative going edge is applied to the $\overline{\text{STROBE}}$ input (pin 48). This starts the delay timer, latches the multiplexer address, and allows the input signal to pass through the multiplexer, instrumentation amplifier and sample/hold and settle to its final value before starting the A/D conversion. The DELAY OUT signal (pin 45) is also connected to the $\overline{\text{TRIG}}$ input (pin 46) and the A/D conversion is initiated on the negative-going edge. The S/H CONTROL input (pin 66) is connected to $\overline{\text{BUSY}}$ (pin 24) so that the sample/hold is in the HOLD mode during the A/D conversion.

By using overlap programming the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced, extending throughput sampling rates up to 29kHz for 12-bit and 70kHz for 8-bit resolution (ADC short-cycled). This mode of operation is most useful when converting low level inputs to accommodate the increased settling time of the instrumentation amplifier. Overlap programming is accomplished by connecting $\overline{\text{BUSY}}$ to $\overline{\text{STROBE}}$ and S/H CONTROL; DELAY OUT to LOAD and $\overline{\text{TRIG}}$. In this mode of operation the address of the next channel to be converted is latched and the output of the instrumentation amplifier allowed to settle to a new value during the present conversion.

SYSTEM TIMING DIAGRAMS

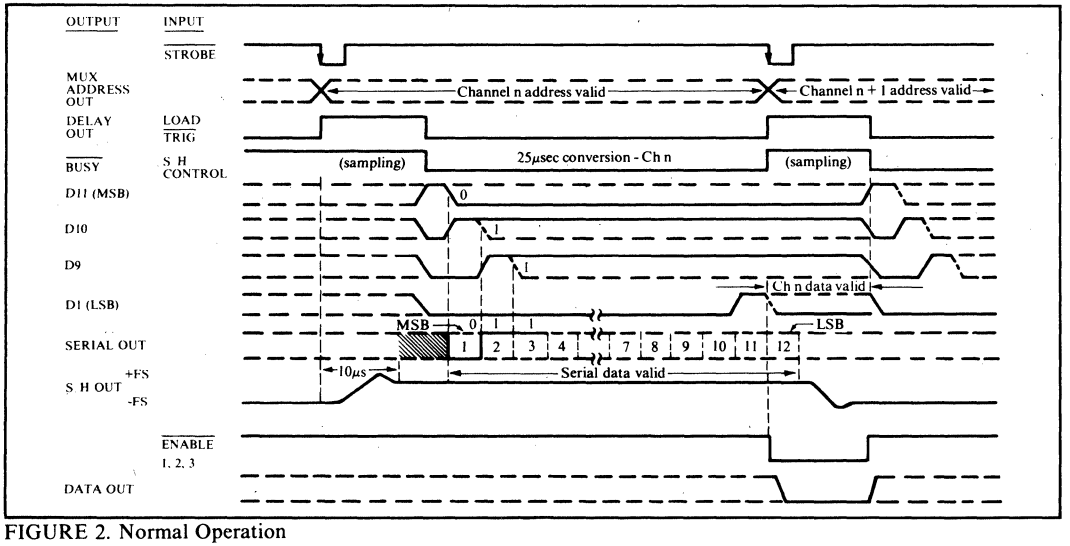


FIGURE 2. Normal Operation

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	SDM856/SDM857			
TRANSFER CHARACTERISTICS	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution	12			Bits
Number of Analog Channels		16SIN/8DIF		
Throughput Rate (Normal Mode)				
SDM856JG	33	35		kHz
SDM856KG	25	27		kHz
SDM857JG	22	24		kHz
SDM857KG	18	20		kHz
Throughput Rate (Overlap mode)				
SDM856JG	38	40		kHz
SDM856KG	27	29		kHz
SDM857JG	38	40		kHz
SDM857KG	27	29		kHz
ANALOG INPUTS				
ADC Input Voltage Ranges		0 to +10, ±5, ±10		V
Mux Input Voltage Range				
Absolute max without damage			±20	V
For linear operation			±6	V
Mux Input Impedance, OFF Channel		$5 \times 10^9 \| 10$		Ω||pF
Mux Input Impedance, ON Channel		1800||7		Ω||pF
Amplifier Characteristics				
(SDM857 only)				
Input Impedance		$5 \times 10^9 \| 3$		Ω||pF
Gain Range	2		500	
Gain Equation		$G = 2 + (20k\Omega/R_{EXT}$[1])		
Input Bias Current at +25°C			±50	nA
0°C to +70°C		±1.1		nA/°C
Offset Current at +25°C			±20	nA
0°C to +70°C		±0.6		nA/°C
Input Offset Voltage		±0.1		mV
Input Offset Voltage Drift (G > 100)		±4	±6	µV/°C
Output Noise (10Hz – 10kHz)				
G = 100, R_S = 500Ω		400		µV, rms
Common-mode Rejection (DC)				
G = 2		90		dB
G = 1000		97		dB
Sample/Hold DC Characteristics				
Input Impedance		$10^{10} \| 3$		Ω||pF
Bias Current		50		nA
Output Offset Voltage		7		mV
REFERENCE VOLTAGES				
Output Voltage: Positive	+2.490	+2.500	+2.510	V
Negative	−6.0	−6.4	−6.8	V
Temperature Coefficient				
(each output)		±5	±10	ppm/°C
Current Available for External Loads				
Positive[2]	0			µA
Negative	−200			µA
ACCURACY				
Throughput Accuracy				
0 to +5V, ±5V ranges JG			±0.048	% of FSR[3]
0 to +5V, ±5V ranges KG			±0.024	% of FSR
0 to +20mV, ±10mV JG				
(SDM857 only)			±0.11	% of FSR
0 to +20mV, ±10mV KG				
(SDM857 only)			±0.08	% of FSR
Linearity (G = 1): JG			±0.024	% of FSR
KG			±0.012	% of FSR
Differential Linearity (G = 1): JG		±0.024	±0.048	% of FSR
KG		±0.012	±0.024	% of FSR
Quantizing Error			±0.012	% of FSR
System Gain Error[4]		±0.1	±0.3	%
System Offset Error[4]		±0.1	±0.3	% of FSR
Power Supply Sensitivity: +15V		±0.0007		%/%ΔV
−15V		±0.0007		%/%ΔV
+5V		±0.001		%/%ΔV
TEMPERATURE STABILITY	**MIN**	**TYP**	**MAX**	**UNITS**
System Accuracy Drift[5]: Unipolar			±25	ppm/°C
Bipolar			±20	ppm/°C
Linearity Drift			±2	ppm of FSR/°C

DYNAMIC ACCURACY				
Sample/Hold Characteristics				
Aperture Time		100		nsec
Acquisition Time		10		µsec
Feedthrough (10V step)		±1.4		mV
Amplifier Characteristics				
(SMD857 only)				
Amplifier CMRR at 60Hz, G = 2		90		dB
G = 500		95		dB
Amplifier Overload Recovery Time		200		µsec
OUTPUTS				
Digital Output Coding		Binary, Offset Binary, Two's Complement		
Serial Output Coding		Non-return to zero (NRZ)		
ADC Conversion Time[6]		25	30	µsec
Clock Frequency[6]		520		kHz
Delay[7]: SDM856		15		µsec
SDM857		30		µsec
POWER REQUIREMENTS				
Rated Voltage for Specified Accuracy	±14.5	±15	±15.5	V
	+4.75	+5	+5.25	V
Quiescent Current				
SDM856, +15VDC		+10	+20	mA
SDM856, −15VDC		−35	−50	mA
SDM856, +5VDC		+120	+140	mA
SDM857, +15VDC		+15	+25	mA
SDM857, −15VDC		−40	−55	mA
SDM857, +5VDC		+120	+140	mA
Power Dissipation: SDM856		1300	1750	mW
SDM857		1400	1900	mW
ENVIRONMENTAL				
Specification Temperature Range	0		+70	°C
Storage Temperature Range	−55		+100	°C

PRICES	1-24	25-99	100-249	
SDM856JG	174	145	125	$
SDM856KG	219	184	158	$
SDM857JG	194	154	130	$
SDM857KG	242	192	162	$

NOTES:
1. R_{EXT} is the external gain-setting resistor. (Connect between pins 1 and 80.)
2. External loading of the +2.5V reference output is not recommended.
3. FSR means Full Scale Range, e.g., FSR is 10V for ±5V range.
4. Adjustable to zero.
5. Includes gain, offset, and linearity drifts.
6. Conversion time and clock frequency can be externally adjusted from 13µsec (f_{clock} = 1.0MHz) to 110µsec (f_{clock} = 118kHz). Conversion times are for 12-bit resolution.
7. Can be externally adjusted from 3µsec to 300µsec.

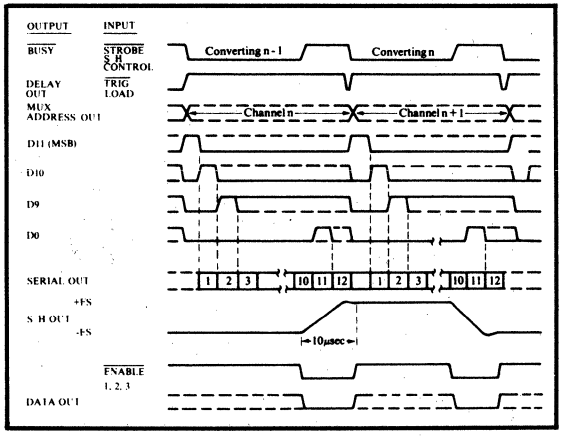


FIGURE 3. Overlap Operation

DIGITAL INPUT SPECIFICATIONS

Address Inputs (A0 - A3)	One standard LSTTL load, positive true
Address Coding	4-bit binary
Load	One standard LSTTL load, positive true, address loaded on positive edge.
$\overline{\text{Clear}}$	One standard LSTTL load, negative true, low level clears latch.
$\overline{\text{Strobe}}$	One standard LSTTL load, high-to-low transition triggers the delay timer.
$\overline{\text{TRIG}}$	One standard LSTTL load, a negative going edge initiates the A D conversion.
Short Cycle	One standard LSTTL load, logical 1 for 12-bit resolution connect to "8-bit" or "10-bit" for 8- or 10-bit resolution.
$\overline{\text{Enable 1}}$, $\overline{\text{Enable 2}}$, $\overline{\text{Enable 3}}$, $\overline{\text{D11}}$ $\overline{\text{Enable}}$, Busy $\overline{\text{Enable}}$	One standard LSTTL load, a low level enables the 3-state output.
S H Control	TTL compatible, 10μA maximum input current. Logic 0 = Hold mode, Logic 1 = Sample (track) mode.
Mux Enable 2	TTL compatible, 2μA input current, Logic 0 enables multiplexer 2 (channels 8-15).

DIGITAL OUTPUT SPECIFICATIONS

Parallel Data Outputs	5 standard TTL loads, positive true, 3-state.
Serial Output	2 standard TTL loads, positive true, NRZ, time serial data output beginning with D11 (see Timing Diagram).
$\overline{\text{D11}}$	5 standard TTL loads, positive true, 3-state.
$\overline{\text{Busy}}$	5 standard TTL loads, low during A, D conversion.
Busy	5 standard TTL loads, high during A D conversion, 3-state
Clock Out	5 standard TTL loads, for synchronizing serial out data (see Timing Diagram).
Address Outputs (A0 - A3)	5 standard TTL loads, positive true
Delay Out	5 LSTTL loads, high during delay period, triggered by $\overline{\text{Strobe}}$ input.
Sin Diff	5 LSTTL loads, high while addressing channels 0-7, low while addressing channels 8-15.

TYPICAL PERFORMANCE CURVES

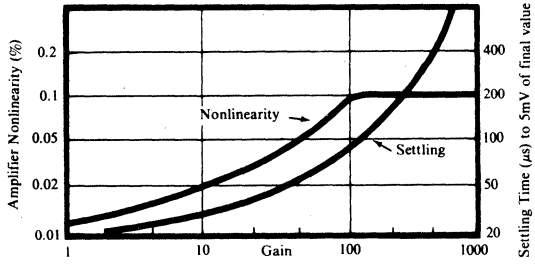


FIGURE 4. Nonlinearity and Settling Time vs. Amplifier Gain

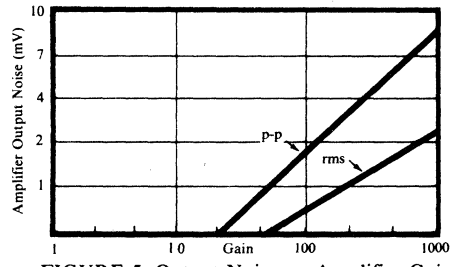


FIGURE 5. Output Noise vs. Amplifier Gain

SDM856/857

THROUGHPUT ACCURACY AND TIMING RELATIONSHIPS

System Gain		System Accuracy		Throughput Rate (min) (Channels/sec)				Delay Time (μsec)		
				Normal		Overlap		Normal	Overlap	
V/V		KG	JG	JG	KG	JG	KG	JG and KG	JG	KG
1	856 only	±0.024%	±0.048%	33k	25k	38k	27k	15	26	35
2	857 only	±0.024%	±0.048%	22k	18k	38k	27k	30	26	35
10	857 only	±0.035%	±0.06%	22k	18k	38k	27k	30	26	35
100	857 only	±0.08%	±0.11%	10k	9k	11k	11k	90	90	
500	857 only	±0.1%	±0.15%	2.5k	2.4k	2.6k	2.6k	390	390	

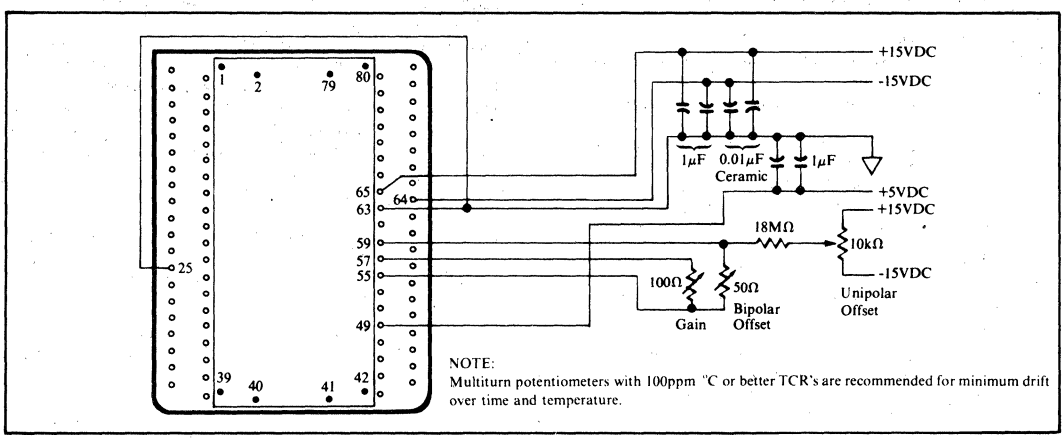
TABLE II. Throughput rate and delay time vs gain for normal and overlap modes.

Full Scale Input Range	ADC Range	Amplifier Gain	Resolution	Amplifier/Multiplexer Settling Time (μsec)		
				To ±0.2%	To ±0.05%	To ±0.01%
10V	-10 to +10	2	2.44mV	8	10	20
1V	0 to +10	10	244μV	12	14	24
0.1V	0 to +10	100	24.4μV	65	80	90
20mV	0 to +10	500	4.88μV	320	390	450

TABLE III. This table shows the delay timer setting required to allow for the settling time of the instrumentation amplifier to the accuracies specified.

In overlap, when the amplifier/multiplexer settling time is less than the ADC conversion time, set the delay timer for the ADC conversion time plus the sample/hold acquisition time (30μsec plus 10μsec). When the amplifier/multiplexer settling time exceeds the ADC conversion time plus the S/H acquisition time, set the delay timer for the amplifier/multiplexer settling time.

CONNECTION DIAGRAM



NOTE:
Multiturn potentiometers with 100ppm °C or better TCR's are recommended for minimum drift over time and temperature.

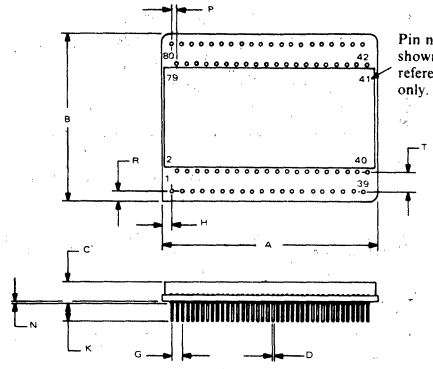
FIGURE 6. Connection Diagram for power supply decoupling and gain and offset adjustment.

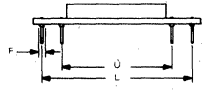
PIN DESIGNATIONS

IA GAIN ADJUST	*1	*80	IA GAIN ADJUST
MUX OUT HI	2	*79	IA IN LO
IA IN HI	*3	78	MUX OUT LO
CH7	4	77	CH15/RET7
CH6	5	76	CH14/RET6
CH5	6	75	CH13/RET5
CH4	7	74	CH12/RET4
CH3	8	73	CH11/RET3
CH2	9	72	CH10/RET2
CH1	10	71	CH9/RET1
CH0	11	70	CH8/RET0
MUX ENABLE 2	12	*69	IA OUT
MUX ENABLE 1/A3 OUT	13	68	S/H IN
SIN DIF	14	67	S/H OFFSET ADJUST
A2 OUT	15	66	S/H CONTROL
A1 OUT	16	65	+15VDC
A0 OUT	17	64	-15VDC
CLEAR	18	63	ANA COM
A0 IN	19	62	S/H OUT
A1 IN	20	61	-6.4V REF OUT
A2 IN	21	60	10V RANGE
A3 IN	22	59	BPO
LOAD	23	58	20V RANGE
BUSY	24	57	+2.5V REF IN
DIG COM	25	56	ENABLE 2
SHORT CYCLE	26	55	+2.5V REF OUT
10-BIT RESOLUTION	27	54	ENABLE 1
8-BIT RESOLUTION	28	53	ENABLE 3
D0 (LSB)	29	52	SERIAL OUT
D1	30	51	CLOCK OUT
D2	31	50	CLOCK RATE ADJUST
D3	32	49	+5VDC
D4	33	48	STROBE
D5	34	47	DELAY ADJUST
D6	35	46	TRIG
D7	36	45	DELAY OUT
D8	37	44	D11
D9	38	43	BUSY
D10	39	42	BUSY ENABLE
D11 (MSB)	40	41	D11 ENABLE

*For SDM857 only. Make no connection in SDM856.

MECHANICAL



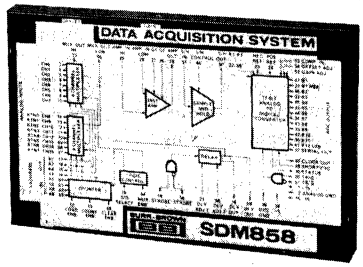


NOTE:
Leads in true position within .015" (.38mm)R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	

MATERIAL: Alumina
WEIGHT: 32 grams (1.2 oz.)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20-pin strips) or 0422MC (assembled unit).

BURR-BROWN®



SDM858

Low-Level Input, 12-Bit DATA ACQUISITION SYSTEM

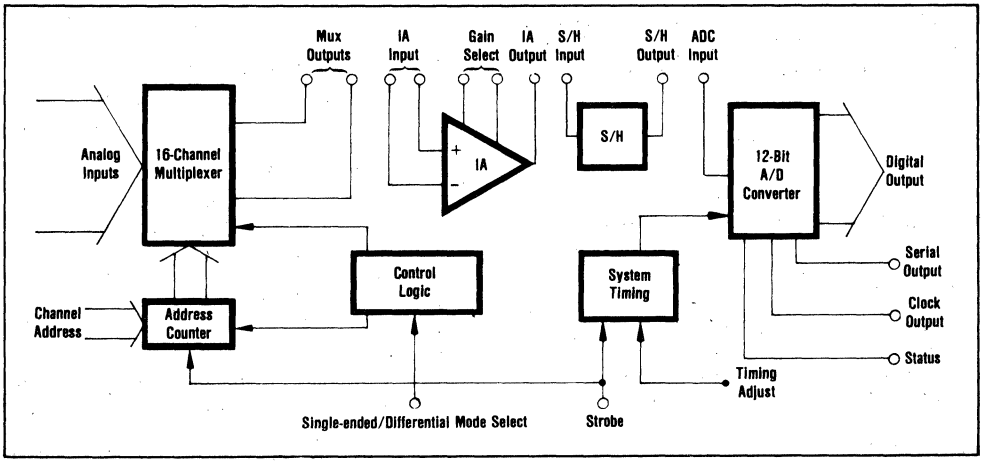
FEATURES

- HIGH ACCURACY WITH LOW LEVEL INPUT SIGNALS
- LOW COST
- SAVES DESIGN TIME
- RELIABLE - 70°C BAKE FOR 160 HOURS
- SAVES SPACE
- FLEXIBLE - FOUR MODES OF OPERATION

DESCRIPTION

The SDM858 is a complete 8- or 16-channel data acquisition system in a compact 4.6" x 3.0" x 0.375" metal case. This system is specifically designed to give high accuracy with low level analog input signals. A built-in high quality instrumentation amplifier allows input signal ranges of ±5mV to ±10V. It is especially useful with thermocouple and strain gage inputs since it yields only ±0.025% (of Full Scale Range) error at a gain of 100.

This expandable module accepts either 16 single-ended or 8 differential inputs and converts the multiplexed data signals into 12-bit digital words with an accuracy of ±0.025% at throughput rates of up to 8000 samples per second.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SYSTEM DESCRIPTION

The SDM858 contains all the components necessary to multiplex and convert ±5mV to ±10V analog data into equivalent digital outputs yielding resolutions of 2.4μV to 4.88mV. It has been designed specifically to acquire and convert low level signals. The throughput sampling rate is 8kHz for 12-bit resolution at a gain of 10. This system contains an analog multiplexer (which can be connected for 16-channel single-ended or 8-channel differential signals), instrumentation amplifier, sample/hold circuit, 12-bit successive approximation A/D converter, and control and timing logic. The amplifier and sample/hold are not internally connected, allowing maximum application flexibility. These systems can be expanded almost without limit using Burr-Brown's MPC16S, MPC8D, MPC8S, and MPC4D monolithic multiplexers. The SDM858 is designed to be mounted on a printed circuit card. The only requirements for system operation are input signals, power, and the interconnection of system components into the desired operating configuration. The components of the SDM858 are shown in Figure 1 and described in the following paragraphs.

ANALOG MULTIPLEXER

Two, one-of-eight, CMOS analog multiplexers are used to allow user selection (by external jumpers) of 16 single-ended channel or 8 differential channel operation. In 16-channel operation the multiplexer may be used in a pseudo-differential mode by connecting the amplifier inverting input to a common, remote, signal ground. Channel selection is by a 3- or 4-bit binary word stored in a presettable address counter.

INSTRUMENTATION AMPLIFIER

The SDM858 instrumentation amplifier has been optimized for low drift and high accuracy with analog inputs as low as ±5mV full scale. Input noise and thermal feedback have been minimized to improve accuracy when amplifying such signals as thermocouple and strain gage outputs. The gain is programmed with an external resistor connected between pins 26 and 27. Gain may be selected from 1 to 2000.

The amplifier used in the SDM858 is the Burr-Brown Model 3630. More information is available in the 3630 product data sheet.

SAMPLE/HOLD

The sample/hold circuit is a complete monolithic unit featuring buffered output and maximum acquisition and aperture times of 52μsec and 200nsec. Input, output, and mode control functions are brought to separate connector pins. This allows maximum system flexibility for performing such functions as automatic gain ranging with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a ceramic-packaged, 12-bit converter featuring 24μsec conversion time and 0.01% accuracy. Stable thin-film networks and current switching are used to assure linearity over wide temperature ranges.

ADDRESS COUNTER

A 4-bit binary address counter is connected to the multiplexer. This counter may be externally loaded, cleared, clocked, or enabled. The address outputs are brought to connector pins for convenient system control.

DELAY TIMER

The delay timer is provided to allow for the settling time of the multiplexer, amplifier, and sample/hold circuits prior to start of conversion. The delay time is adjustable over a wide range by an external potentiometer and/or external capacitor. This allows for the longer settling time of the instrumentation amplifier at high gains. The timer is adjusted at the factory for optimum operation at a gain of 100.

CONTROL LOGIC

Delay and ADC trigger functions are edge-triggered and gated. Counter control functions are synchronous with the counter clock which is internally connected to the delay timer output.

CHANNEL EXPANSION

The number of analog input channels of these systems can easily be increased using Burr-Brown's CMOS multiplexers. These latch-free devices contain internal binary decoding, TTL or MOS logic levels, and may be integrated into a system with minimum external logic. The following devices offer a variety of input channel configurations.

MPC4D	4-channel differential
MPC8D	8-channel differential
MPC8S	8-channel single-ended
MPC16S	16-channel single-ended

SYSTEM PERFORMANCE

The SDM858 can be configured to continuously sequence through all analog channels, to accept random addresses or to sequence through all analog channels on command from an external trigger.

The STATUS signal, pin 30, is connected to the $\overline{\text{STROBE}}$ input of the delay timer, pin 58, for normal program sequencing with a minimum throughput sampling rate of 2kHz for 12-bit resolution and a gain of 100. A throughput rate of 8kHz with 12-bit resolution can be achieved for a gain of 10 by decreasing the delay time.

By using "overlap" programming, the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced slightly. Overlap programming is accomplished by connecting the STATUS signal, pin 30, to the STROBE input of the delay timer, pin 19, and extending the delay time. The internal logic will then select analog channel (n + 1) while channel n is being converted.

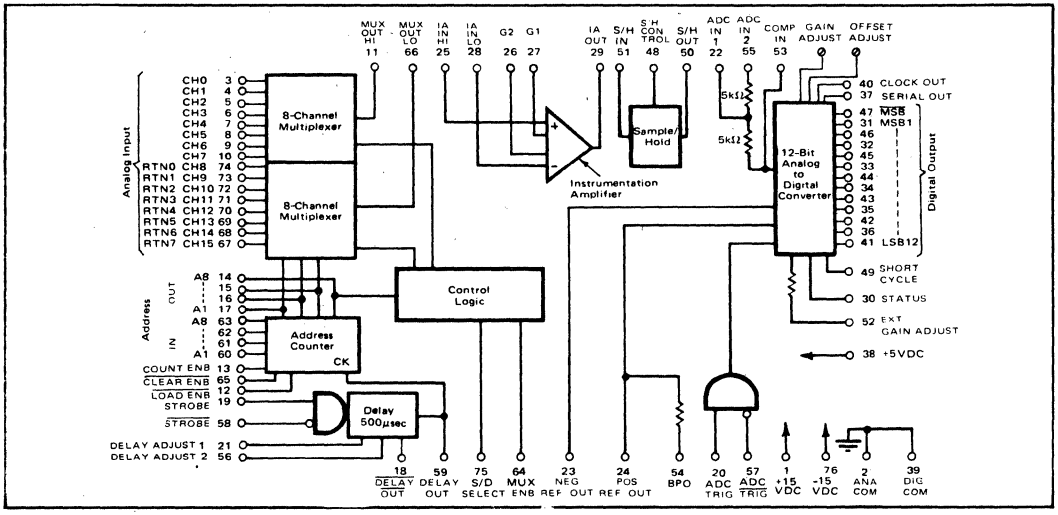


FIGURE 1. Detailed Block Diagram of SDM858.

SPECIFICATIONS

ELECTRICAL	
Typical at +25°C with ±15VDC and +5VDC power supplies unless otherwise noted.	
MODEL	SDM858
TRANSFER CHARACTERISTICS	
Throughput Rate, min	
G = 1	8kHz, 125μsec/channel
G = 100	2kHz, 500μsec/channel
G = 1000	1kHz, 1msec/channel
G = 2000	500Hz, 2msec/channel
Resolution	12 bits
Number of Channels	16 single-ended or pseudo-differential/8 differential
ANALOG INPUTS	
ADC Voltage Input Ranges	0 to +5V, 0 to +10V, ±2.5V, ±5V, ±10V
Amplifier Gain Range	1 to 2000
Amplifier Gain Equation	$G = 1 + (40k\Omega / R_{EXT})$[1]
Max. Input Voltage without Damage	±16V
Max. Input Voltage for Multiplexer Operation	±10.24V
Common-Mode Input Voltage, max	
G = 1	±10V
G > 1	±5V
Input Impedance	100MΩ, 10pF OFF channel 100MΩ, 100pF ON channel[2]
Bias Current	
+25°C	±10nA, typ; ±30nA, max
0°C to +70°C	±20nA, typ; ±60nA, max
Differential Bias Current	±10nA, typ; ±30nA, max
Differential Bias Current Drift	±0.4nA °C typ; ±1.0nA/°C, max
Amplifier Input Offset Voltage, max	±25 ±(200 G)μV
Amplifier Voltage Offset Drift, max	±0.75 ±(10 G)μV °C
vs Supply, max	±2 ±(200 G)μV V
vs Time	±2 ±(40 G)μV mo
Amplifier Input Noise	
Voltage	
0.01Hz to 10Hz	1.2μV, p-p
10Hz to 1kHz	1.0μV, rms
Current	
0.01Hz to 10Hz	70pA, p-p
10Hz to 1kHz	20pA, rms
Amplifier Output Noise (G = 100, R_S = 500Ω)	
0.01Hz to 10Hz	0.12mV, p-p
10Hz to 10kHz	0.32mV, rms
Thermal Feedback[3]	0.1μV V_{Input}
Channel-to-Channel Input Voltage Error[4]	±5μV

ACCURACY[5]	
System Accuracy, max (Gain = 100)	±0.025% FSR[6] at 2kHz throughput rate
Linearity	±[1/2 + (G/2400)] LSB
Differential Linearity (Gain = 100)	±1/2LSB at 2kHz throughput rate
Quantizing Error	±1/2LSB
Gain Error	Adjustable to zero
Offset Error	Adjustable to zero
Power Supply Sensitivity	±0.005% FSR/% change of supply voltage
STABILITY OVER TEMPERATURE	
System Offset Drift, max ($Z_{IN} \leq 400\Omega$)	
G = 1	±5ppm of FSR/°C
G = 10	±7ppm of FSR/°C
G = 100	±30ppm of FSR/°C
G = 1000	±300ppm of FSR/°C
G = 2000	±600ppm of FSR/°C
System Gain Drift,[7] max	
G = 1	±35ppm of reading/°C
G = 10	±80ppm of reading/°C
G = 100	±85ppm of reading/°C
G = 2000	±85ppm of reading/°C
ADC Offset Drift (Unipolar)	±3ppm of FSR/°C
ADC Offset Drift (Bipolar)	±15ppm of FSR/°C
ADC Linearity Drift	±3ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time	125nsec, typ; 200nsec, max
Sample/Hold Acquisition Time (to 0.025%)	26μsec, typ; 52μsec, max
Error for Full Scale Transition Between Successively Addressed Channels	
G = 1	±1LSB at 8kHz
G = 100	±1LSB at 2kHz
G = 1000	±2LSB at 1kHz
G = 2000	±4LSB at 500Hz
Amplifier CMRR, min; 1kΩ Source Imbalance	
G = 1, f = 60Hz	86dB
G = 1, f = 1kHz	70dB
G = 10, f = 60Hz	96dB
G ≥ 100, f = 60Hz	100dB
Channel Cross Talk	-80dB at 2kHz, OFF channel to ON channel
Sample/Hold Feedthrough	±0.007% of 20V
Sample/Hold Decay Rate, (+70°C)	1μV/μsec, typ; 10μV/μsec, max
OUTPUT	
Output Coding (Complementary)	Unipolar straight binary, bipolar offset binary, binary two's complement
Gain Error[8]	Adjustable to zero
Offset Error[8]	Adjustable to zero
A/D Conversion Time	24μsec typ, 30μsec max
Delay	470μsec nominal, externally adjustable[9]
POWER REQUIREMENTS	+15VDC ±3% at +65mA, ripple < 5mV, rms -15VDC ±3% at -75mA, ripple < 5mV, rms +5VDC ±5% at 300mA, ripple < 25mV, rms
ENVIRONMENTAL	
Operating Temperature	0°C to 70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	95% noncondensing

NOTES:
1. With R_{EXT} between pins 26 and 27.
2. With multiplexer output connected to 1A input.
3. Drift due to internal heating.
4. Error due to thermoelectric effects of dissimilar metal junctions.
5. No missing codes guaranteed.
6. FSR means full scale range.
7. Exclusive of gain resistor drift.
8. Gain and offset controls are located in the module. The adjustment ranges are ±0.1% FSR for gain and ±0.1% FSR for offset.
9. Adjustable to 10 seconds with external capacitor, to 50μsec with an external resistor.

DIGITAL INPUT

Address inputs	One standard TTL load, positive true
LOAD ENABLE	One standard TTL load, negative true, address loaded with strobe inputs.
CLEAR ENABLE	One standard TTL load, negative true, address cleared with strobe inputs.
STROBE & $\overline{\text{STROBE}}$	One standard TTL load, STROBE and $\overline{\text{STROBE}}$ edge trigger the delay timer and clock the address counter. STROBE must be high to enable $\overline{\text{STROBE}}$ and $\overline{\text{STROBE}}$ must be low to enable STROBE.
COUNT ENABLE	Two standard TTL loads, positive true, logic "0" allows the Strobe inputs to trigger the delay timer, but prevents the MUX address counter from being clocked.
ADC TRIGGER	One standard TTL load, a positive going edge at TRIG initiates conversion, a negative going edge at $\overline{\text{TRIG}}$ initiates conversion; $\overline{\text{TRIG}}$ must be "0" to enable TRIG; TRIG must be "1" to enable $\overline{\text{TRIG}}$.
SHORT CYCLE	One standard TTL load, logic "1" for 12-bit resolution, connected to the N + 1 bit output for N bit resolution.
MULTIPLEXER ENABLE	Two standard TTL loads, logic "1" enables multiplexer output and logic "0" turns off all channels.
MULTIPLEXER ENABLE	Two standard TTL loads, logic "1" enables 16-channel single-ended operation and logic "0" enables 8-channel differential operation.
S/D SELECT	

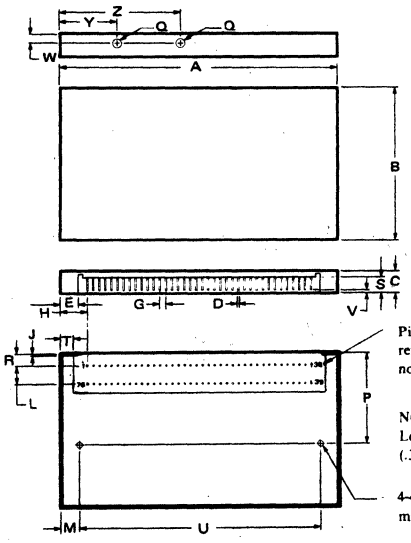
DIGITAL OUTPUT

Data outputs	
Parallel B1, B1 . . . B12	2 Standard TTL loads, negative true.
SERIAL OUT	2 Standard TTL loads, negative true, time serial data output beginning with B1.
Address outputs	5 Standard TTL loads, positive true, 4-bit binary code, internal 2kΩ pull-up resistors.
DELAY OUT and $\overline{\text{DELAY OUT}}$	5 Standard TTL loads high (low) during the delay period, triggered by STROBE and $\overline{\text{STROBE}}$ inputs.
CLOCK OUT	5 Standard TTL loads for synchronizing serial out data.
STATUS	5 Standard TTL loads, high during the A/D conversion.

PIN DESIGNATIONS

+15VDC	1	76	-15VDC
ANA COM	2	75	S/D SELECT
CH0 IN	3	74	CH8 IN (RTN0)
CH1 IN	4	73	CH9 IN (RTN1)
CH2 IN	5	72	CH10 (RTN2)
CH3 IN	6	71	CH11 IN (RTN3)
CH4 IN	7	70	CH12 IN (RTN4)
CH5 IN	8	69	CH13 IN (RTN5)
CH6 IN	9	68	CH14 IN (RTN6)
CH7 IN	10	67	CH15 IN (RTN7)
$\overline{\text{MUX OUT HI}}$	11	66	MUX OUT LO
LOAD ENABLE	12	65	$\overline{\text{CLEAR ENABLE}}$
COUNT ENABLE	13	64	MUX ENABLE
A8 OUT	14	63	A8 IN
A4 OUT	15	62	A4 IN
A2 OUT	16	61	A2 IN
$\overline{\text{A1 OUT}}$	17	60	A1 IN
DELAY OUT	18	59	$\overline{\text{DELAY OUT}}$
STROBE	19	58	$\overline{\text{STROBE}}$
ADC TRIG	20	57	ADC $\overline{\text{TRIG}}$
DELAY ADJUST 1	21	56	DELAY ADJUST 2
R1	22	55	R2
NEG REF OUT	23	54	BPO
POS REF OUT	24	53	COMP IN
IA IN HI	25	52	GAIN ADJUST
G2	26	51	S/H IN
G1	27	50	S/H OUT
IA IN LO	28	49	SHORT CYCLE
IA OUT	29	48	S/H CONTROL
STATUS	30	47	$\overline{\text{B1 (MSB)}}$
B1 MSB	31	46	B2
B3	32	45	B4
B5	33	44	B6
B7	34	43	B8
B9	35	42	B10
B11	36	41	B12 LSB
SERIAL OUT	37	40	CLOCK OUT
+5VDC	38	39	DIG COM

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	4.580	4.620	116.33	117.35
B	2.980	3.020	75.69	76.71
C	.350	.380	8.89	9.65
D	.018	.021	0.46	0.53
E	.280	.320	7.11	8.13
G	.100 BASIC		2.54 BASIC	
H	.420	.480	10.67	12.19
J	.017	.023	0.43	0.58
L	.300 BASIC		7.62 BASIC	
M	.270	.330	6.85	8.38
P	1.480	1.520	37.59	38.61
Q	.130	.170	3.30	4.32
R	.170	.230	4.32	5.84
S	.235	.285	5.97	7.24
T	.170	.260	4.32	6.60
U	3.980	4.020	101.09	102.11
V	.030	.070	0.76	1.78
W	.130	.180	3.30	4.57
Y	.930	.970	23.62	24.64
Z	1.980	2.020	50.29	51.31

Pin numbers shown for reference only. Numbers may not be marked on package.

NOTE:
Leads in true position within .015" (.38mm)R at MMC at seating plane.

4-40 thread, .190" (4.83mm) min. depth, 2 places.

CASE MATERIAL: Insulated Steel
CONNECTOR PINS: Gold Flashed
WEIGHT: 145 grams (5 oz.)

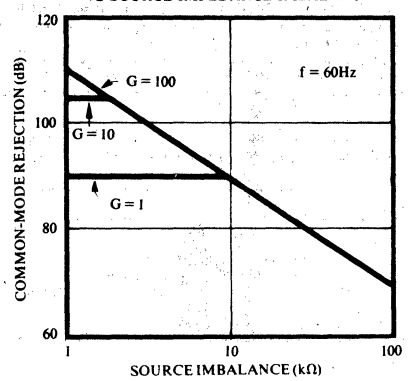
MOUNTING INSTRUCTIONS:
(Mounting flush on PC Card.)

1. Use strip connectors or two 14-pin and three 16-pin low profile IC sockets (shipped with each unit).

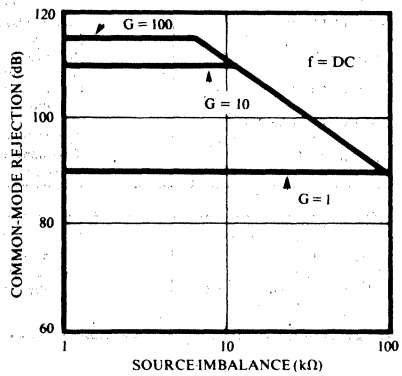
2. Use 4-40 x 3/16" (4.8mm) LG Pan HD Hardware to secure the SDM858 to PC Card.

TYPICAL PERFORMANCE CURVES

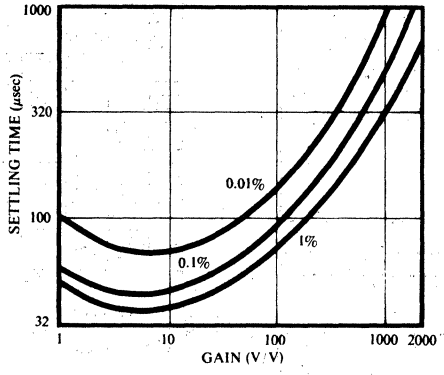
AMPLIFIER COMMON-MODE REJECTION
VS SOURCE IMPEDANCE IMBALANCE



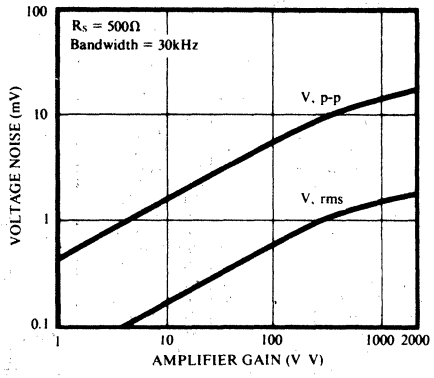
AMPLIFIER COMMON-MODE REJECTION
VS SOURCE IMPEDANCE IMBALANCE



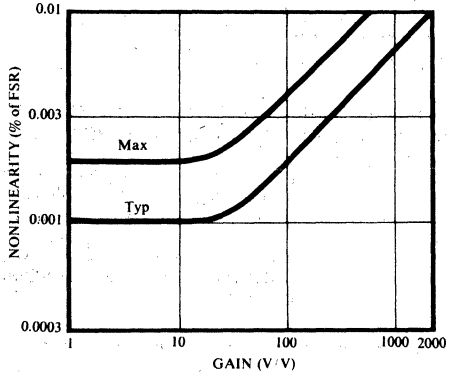
AMPLIFIER SETTLING TIME VS GAIN



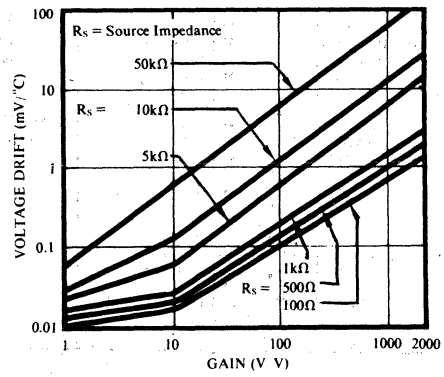
SYSTEM NOISE VS AMPLIFIER GAIN



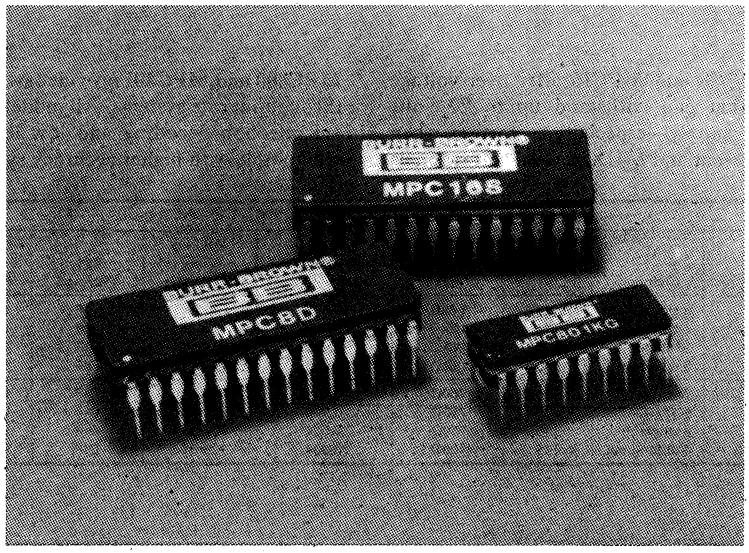
AMPLIFIER NONLINEARITY VS GAIN



AMPLIFIER OUTPUT OFFSET
VOLTAGE DRIFT VS GAIN



MULTIPLEXERS



Burr-Brown multiplexers allow for a very low cost-per-channel figure in multiple-channel data conversion or data distribution systems. Twc types are offered—a low-cost, high quality family of devices that range from 4 to 16 channels and can accommodate either single-ended or differential signals and a very-fast-switching family, again single-ended or differential, for high throughput rate applications. All are TTL-and CMOS-compatible, have input protection in excess of the maximum power supply voltages, and can be operated singly or in multitiered matrices.

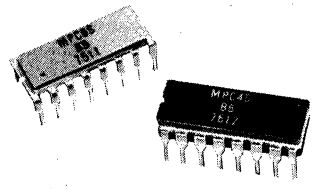
SELECTION GUIDE

MULTIPLEXERS

Models MPC4, MPC8 and MPC16 offer over-voltage protected inputs that can withstand up to 20 volts greater than either supply—especially important when input signals are present and MUX power is off. Models MPC800 and MPC801 provide fast settling time for high throughput rate systems. All models have internal channel selection decoding and low leakage current to be compatible with higher accuracy systems.

MULTIPLEXERS								
Description	Model	Channels	Input Range (V)	On Resistance max	Crosstalk (% of OFF Channel Signal)	Settling Time (to 0.01%)	Package	Page
Protected Inputs	MPC8S	8 single	±15	1.8kΩ	0.005	5µsec	DIP	9-3
	MPC4D	4 differential	±15	1.8kΩ	0.005	5µsec	DIP	9-3
	MPC16S	16 single	±15	1.8kΩ	0.005	7µsec	DIP	9-10
	MPC8D	8 differential	±15	1.8kΩ	0.005	7µsec	DIP	9-10
High Speed	MPC800KG	16 single or	±15	750Ω	0.004	800nsec	DIP	9-17
	MPC800SG	8 differential	±15	750Ω	0.004	800nsec	DIP	9-17
	MPC801KG	8 single or	±15	750Ω	0.004	800nsec	DIP	9-24
	MPC801SG	4 differential	±15	750Ω	0.004	800nsec	DIP	9-24

BURR-BROWN®



MPC4D
MPC8S

CMOS ANALOG MULTIPLEXERS

FEATURES

- **LOW POWER CONSUMPTION**
  CMOS analog switches
  15mW at 100kHz
- **PROTECTS SIGNAL SOURCES**
  Break-before-make switching
- **HIGH THROUGHPUT RATE**
- **RELIABLE MONOLITHIC CONSTRUCTION**

DESCRIPTION

The MPC8S is a single-ended monolithic 8-channel analog multiplexer and the MPC4D is a monolithic 4-channel differential input output multiplexer. The digital and analog inputs are protected from overvoltage inputs that exceed either power supply. These CMOS devices feature self-contained binary channel address decoding and are compatible with DTL, TTL, or CMOS input levels. Channel interaction is eliminated during overvoltage conditions and also in the event of a power loss. They are packaged in a 16-pin DIP and dissipate typically 7.5mW.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

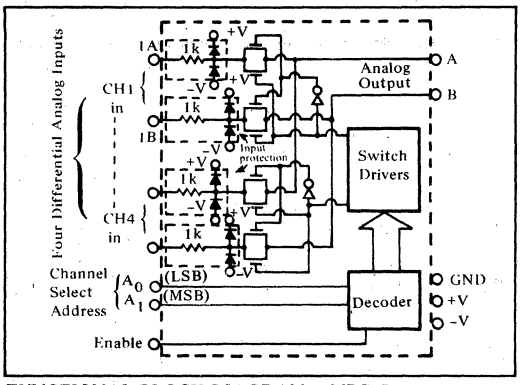
The MPC8S is a single-ended monolithic 8-channel analog multiplexer and the MPC4D is a monolithic differential input/output channel analog multiplexer constructed with failure-protected CMOS devices. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200kHz from signal sources of up to ±10 volts amplitude.

These DTL/TTL/CMOS compatible devices feature self-contained binary channel address decoding. An ENABLE line is also made available which allows the user to individually enable an 8-channel group (MPC8S) or a 4-channel group (MPC4D) facilitating channel expansion in either single-mode or multitiered matrix configurations.

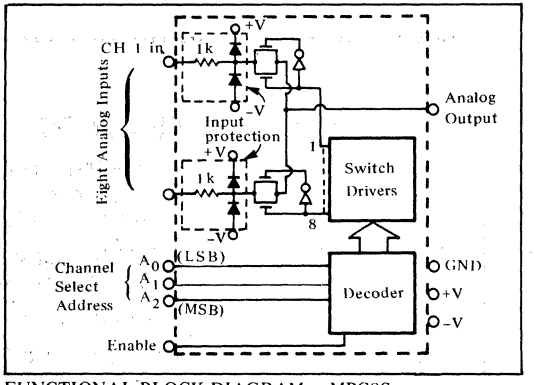
Digital and analog inputs are failure protected from either overvoltages that exceed the power supplies or from the loss of power.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, high OFF resistance, low feedthrough capacitance and fast settling time.

These devices are housed in compact 16-pin dual-in-line packages, and are specified for operation over a 0°C to +75°C temperature range. They are pin and package compatible with the 508/509 series.



FUNCTIONAL BLOCK DIAGRAM – MPC4D



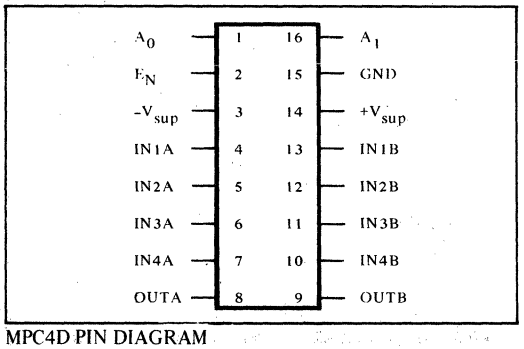
FUNCTIONAL BLOCK DIAGRAM – MPC8S

A_1	A_0	E_N	"On" Switch Pair
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

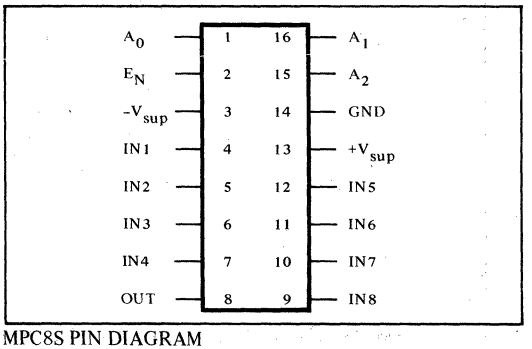
TRUTH TABLE –MPC4D

A_2	A_1	A_0	E_N	On Switch
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

TRUTH TABLE – MPC8S



MPC4D PIN DIAGRAM



MPC8S PIN DIAGRAM

SPECIFICATIONS

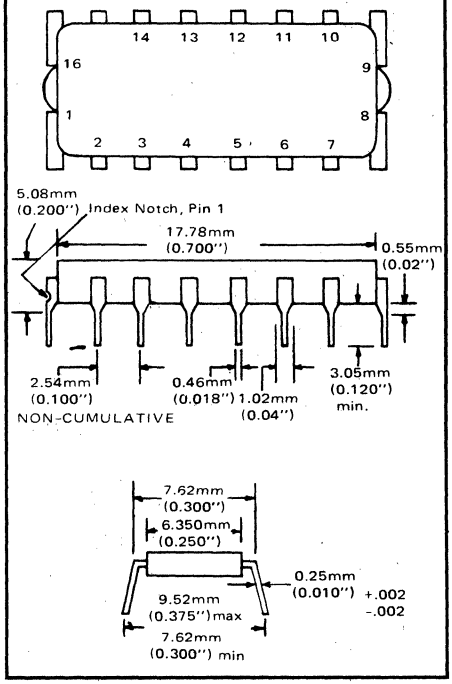
Typical for following conditions: V + = +15V, V - = -15V, $R_{source} \leq 1000\ \Omega$, $T_A = 25°C$ unless otherwise noted.

ELECTRICAL

MODELS	MPC8S	MPC4D	Units
INPUT			
ANALOG INPUT			
Voltage Range	±15		V
Maximum Overvoltage	+V supply +20 -V supply -20		V V
Current at Maximum Overvoltage per channel[1]	±18		mA
Number of Input Channels			
Single-ended	8		
Differential		4	
ON Characteristics			
ON Resistance (R_{ON})			
Typical	1.5		kΩ
Maximum	1.8		kΩ
R_{ON} Drift vs. Temperature (0°C to +75°C)	0.25		%/°C
R_{ON} Mismatch			
Channel-to-channel	50	50	Ω
Differential	N/A	50	Ω
Input Leakage (I_I)	0.1		nA
Input Leakage Drift	See Figure 9		
OFF Characteristics			
OFF Resistance	10^{11}		Ω
Output Leakage (All channels disabled)	0.2		nA
Input Leakage[6]	0.02		nA
Leakage Drift	See Figure 9		
Output Leakage with Input Overvoltage			
of +35V	1		nA
of -35V	1		μA
DIGITAL INPUTS			
Logic "0" (V_L)[1][2]	-V supply ≤ V_L < 0.8 at 1 nA		V
Logic "1" (V_H)[1][2]	+4V ≤ V_H ≤ + V supply at 1 nA		V
Channel Select	3 bit binary code - one of eight	2 bit binary code - one of four	
Enable	Logic "0" (low) disables all channels. Logic "1" (high) enables channel select to turn on selected channel.		
POWER REQUIREMENTS			
Rated Power Supply Voltages	±15		V
Supply Range			
+Supply	+10 to ±20		V
-Supply	-10 to -20		V
Supply Drain			
At 1 MHz Switching Speed	+4, -2		mA
AT 100 kHz Switching Speed	±0.5		mA
Typical Power Consumption			
DC to 10 kHz	7.5		mW
DYNAMIC CHARACTERISTICS			
Gain Error (20 MΩ load) maximum	0.01		%
Crosstalk[3]	0.005		% of OFF channel signal
Settling Time[4]			
To ±2mV ±(0.01%)	5		μs
To ±20mV ±(0.10%)	2		μs
Common-mode Rejection (minimum)	N/A	120	dB
Switching Time			
Turn ON	0.5		μs
Turn OFF	0.3		μs
Recovery Time from Input Overvoltage Pulse of 35V for 100 μsec			
To 0.01%	150		μs
To 0.10%	15		μs
OUTPUT			
Voltage Range	±15		V
Capacitance to Ground	25	12[5]	pF
Capacitance Mismatch	N/A	±10	%
TEMPERATURE			
Specification	0 to +75		°C
Storage	-65 to +150		°C

MPC4D AND MPC8S

16 Pin Ceramic Lead Frame TOP VIEW



NOTES:

1. Total power dissipation due to input overvoltage current flowing in the input protection circuitry must be limited to 0.75 watt for both (a) normal operation with power supplies turned on or (b) during a fault condition when the supplies are shorted to ground.
2. Maximum overvoltage is ±Vsupply ±4 volts at ±15 mA.
3. 20 volt peak-to-peak 1000 Hz sinewave; $R_{SOURCE} = 1000\Omega$, same signal on all unused channels.
4. For 20 volts between switched channels, $R_{SOURCE} = 1000\Omega$. See Figure 5 for settling time vs. source impedance (R_S).
5. From each side of MPC4D to ground.
6. Leakage measurement made with all OFF channel inputs fed in parallel to +20 volts.

DISCUSSION OF PERFORMANCE

Static Transfer Accuracy

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

SINGLE-ENDED MULTIPLEXER STATIC ACCURACY

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of 10^8 ohms or greater will keep resistive loading errors to 0.002% or less for 1000 ohm source impedances. A 10^6 ohm load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000 ohm source resistance will present less than 0.001% loading error and 10,000 ohm source resistance will increase source loading error to 0.01% with a 10^8 ohm load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\in(R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

INPUT OFFSET VOLTAGE

Bias current generates an input OFFSET voltage as result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10 nanoamperes will generate an offset voltage of 20μV if a 1000 ohm source is used, and 200μV if a 10,000 ohm source is used. In general, for the MPC8S, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_b + I_L)(R_{ON} + R_S)$$

where I_b = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{SOURCE} = Source resistance

DIFFERENTIAL MULTIPLEXER STATIC ACCURACY

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full scale ranges of 10 to 100 millivolts.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

The effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications. Refer to Figure 2.

LOAD (OUTPUT DEVICE) CHARACTERISTICS

- Use devices with very low bias current. Generaly, FET input amplifiers should be used for low level signals less than 50mV RSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be 10^{10} ohms or higher.

SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC4D is used for multiplexing high-level signals of ±1 volt to ±10 volts full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

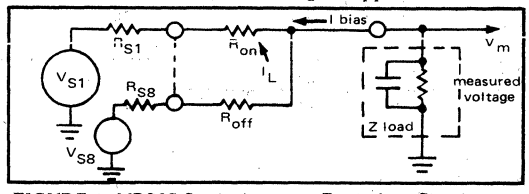


FIGURE 1: MPC8S Static Accuracy Equivalent Circuit.

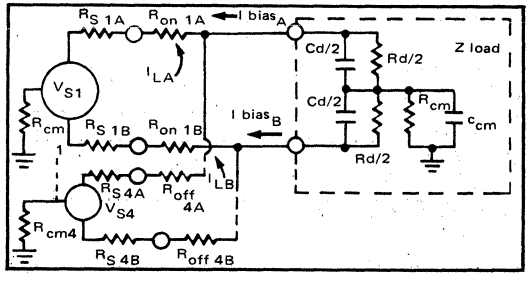


FIGURE 2: MPC4D Static Accuracy Equivalent Circuit.

SETTLING TIME

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C\frac{dV}{dt}$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figure 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. If effect, the amplitude of the transients seen at the source and load are:

$$dV_{load} = \frac{i}{C}\,dt$$

where $i = C\frac{dV}{dt}$ of the CMOS FET switches

C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in Figure 5. This graph shows the settling time for a 20 volt step change on the input. The settling time for smaller step changes on the input will be less than that shown in Figure 5.

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10 volt signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the three (MPC4D) or seven (MPC8S) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel OFF resistance and junction capacitances in series with the R_{ON} and R_{SOURCE} impedances of the ON channel. Crosstalk is measured with a 20 volt pk-pk 1000 Hertz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in Figure 6.

COMMON-MODE REJECTION (MPC4D ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC4D, protection is provided for common-mode signals of ±20 volts above the power supply voltages with no damage to the analog switches.

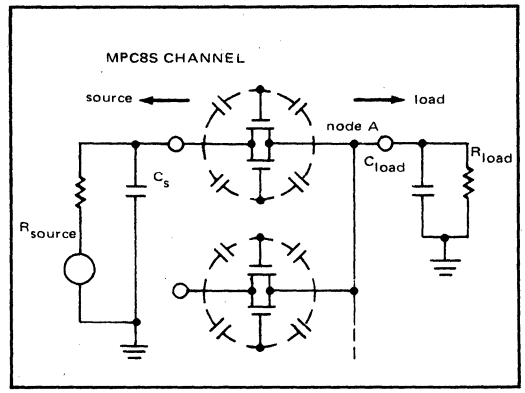


FIGURE 3: Settling Time Effects – MPC8S

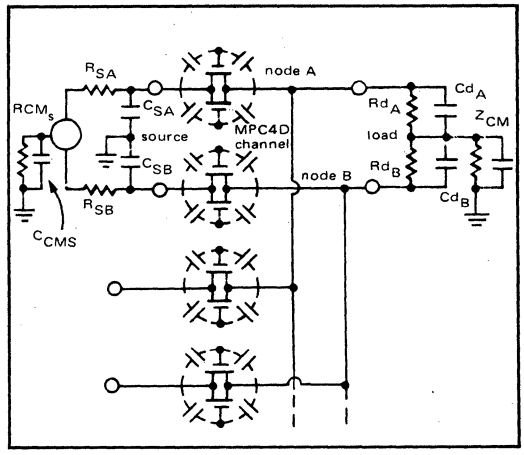


FIGURE 4: Settling & Common-Mode Effects – MPC4D.

The CMR of the MPC4D and Burr-Brown's model 3660 Instrumentation Amplifier is 120 dB at DC to 1 Hz with a 6 dB/octave rolloff to 70 dB at 1000 Hz. This measurement of CMR is shown in Figure 8 and is made with a Burr-Brown model 3660 Instrumentation Amplifier connected for a gain of 1000 and with source unbalance of 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

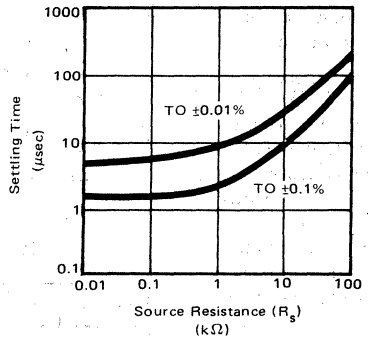


FIGURE 5. Settling time vs source resistance for 20 volt step change.

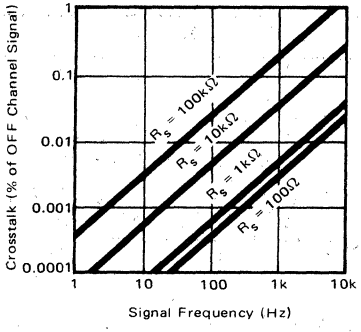


FIGURE 6. Crosstalk vs signal frequency.

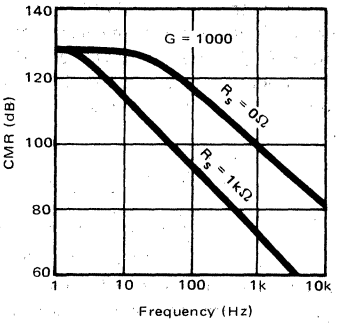


FIGURE 7. CMR vs frequency for Model 3660 IA and MPC4D (G = 1000).

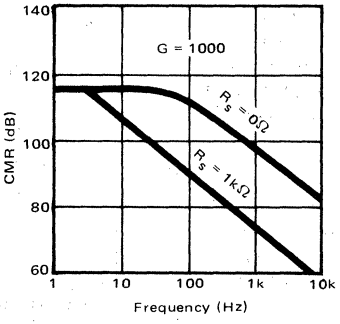


FIGURE 8. Combined CMR vs frequency for Model 3670 IA (G = 1000) and MPC4D.

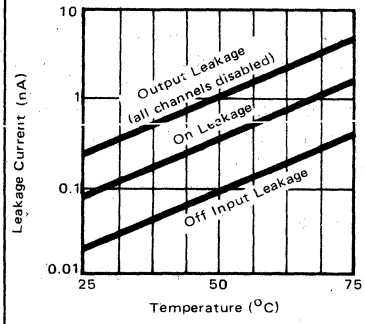


FIGURE 9. Leakage current vs temperature.

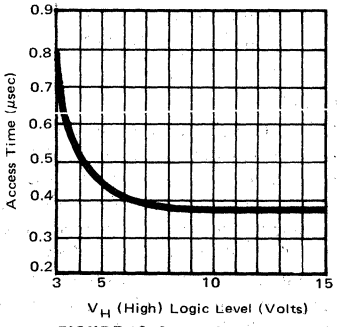


FIGURE 10. Access time vs logic level (high).

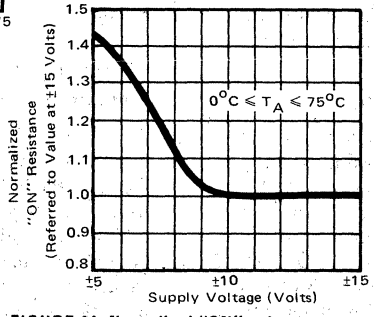


FIGURE 11. Normalized "ON" resistance vs supply voltage.

OPERATION & INSTALLATION INSTRUCTIONS

The ENABLE input, pin 2, is included for expansion of the number of channels on a single node as illustrated in Figure 12. With ENABLE line at a logic 1, the channel is selected by the 2 bit (MPC4D) or 3 bit (MPC8S) Channel Select Address (shown in the Truth Tables on page 9-4) If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15 volt and/or -15 volt supply voltage is absent or shorted to ground, the MPC4D and MPC8S multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded (see Footnote 1, page 9-5).

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended. See Figure 10 (access time).

To preserve common-mode rejection of the MPC4D, use twisted-shielded pair wire for signal lines and inter-tier connections and or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as closely as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

SINGLE-ENDED MULTIPLEXER (MPC8S)

Up to 32 channels (4 multiplexers) can be connected to a single node, or up to 64 channels using 9 MPC8S multiplexers on a two-tiered structure as shown in Figure 12 and 13.

DIFFERENTIAL MULTIPLEXER (MPC4D)

Single or multi-tiered configurations can be used to expand multiplexer channel capacity up to 32 channels using a 32 x 1 or 16 channels using a 4 x 4 configuration.

SINGLE NODE EXPANSION

The 32 x 1 configuration is simply eight MPC4D units tied to a single node. Programming is accomplished with a 5 bit counter, using the 2 LSB's of the counter to control Channel Address inputs A_0 and A_1 and the 3 MSB's of the counter to drive a 1 of 8 decoder. The 1 of 8 decoder then is used to drive the ENABLE inputs (pin 2) of the MPC4D multiplexers.

TWO TIER EXPANSION

Using a 4 x 4 2-tier structure for expansion to 16 channels, the programming is simplified A 4-bit counter output does not require a 1 of 8 decoder. The 2 LSB's of the counter drive the A_0 and A_1 inputs of the four first tier multiplexers and the 2 MSB's of the counter are applied to the A_0 and A_1 inputs of the second tier multiplexer.

Single vs. Multi-Tiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single node configuration, data cannot be taken from any channel, where as only one channel group is failed (4 or 8) in the multi-tiered configuration.

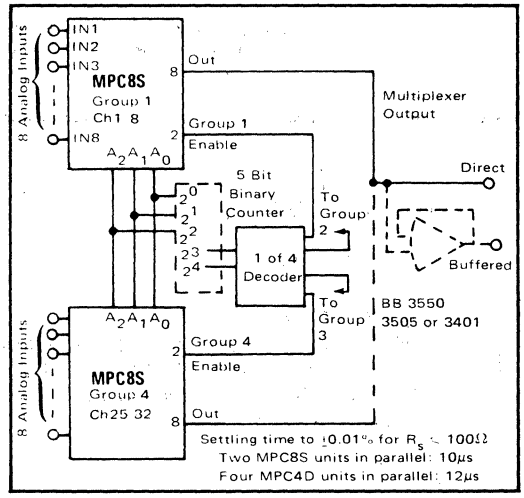


FIGURE 12. 32 Channel, Single-Tier Expansion.

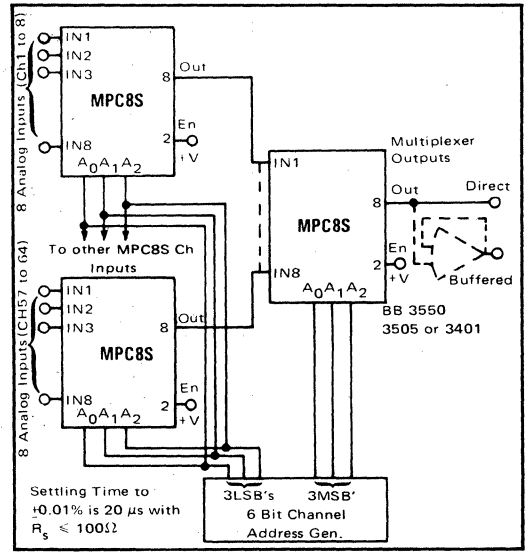


FIGURE 13. Channel Expansion Up to 64 Channels Using 8X8 Two-Tiered Expansion.

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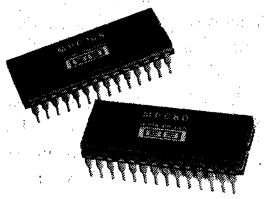
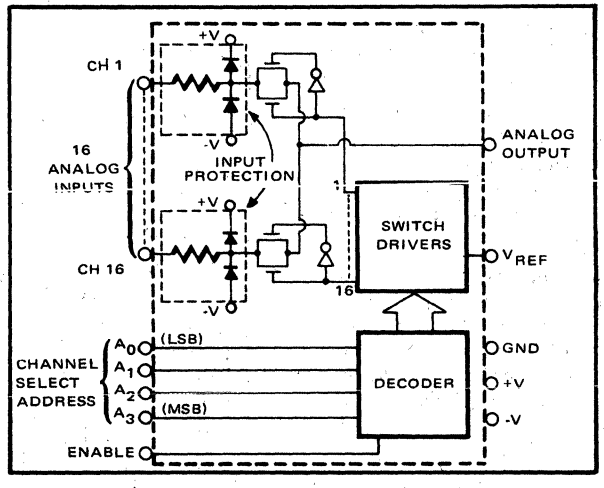


MPC8D
MPC16S

CMOS ANALOG MULTIPLEXERS

FEATURES

- LOW POWER CONSUMPTION
  CMOS analog switches
  15mW at 100kHz
  7.5mW standby power
- COMPACT DESIGN
  Self-contained with internal channel address decoder
  8-channel dual (MPC8D) for differential inputs or
  16-channel (MPC16S) for single-ended inputs
  28-pin 0.600 inch-wide space-saving package
- WILL NOT SHORT SIGNAL SOURCES
  Break-before-make switching
- FAST SWITCHING SPEEDS PROVIDE HIGH THROUGHPUT RATES
  7μsec settling to 0.01%
  3μsec settling to 0.1%
- WIDE SUPPLY RANGE
  ±10VDC to ±20VDC



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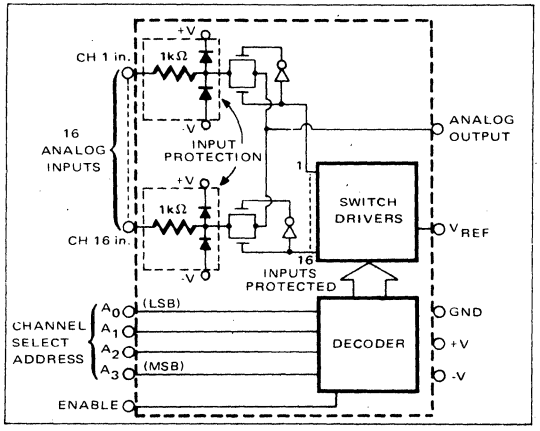
DESCRIPTION

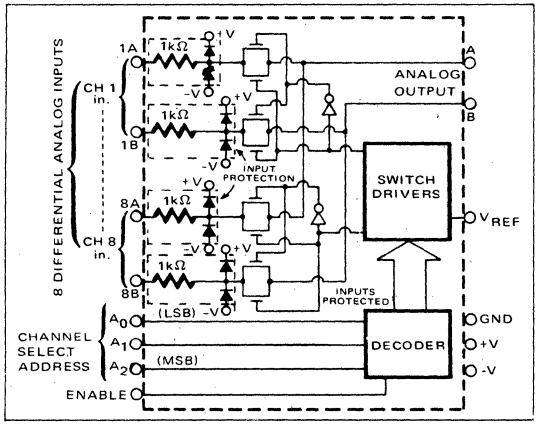
The MPC16S is a single-ended monolithic 16-channel analog multiplexer and the MPC8D is a monolithic dual 8-channel analog multiplexer constructed with failure protected CMOS devices. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200kHz from signal sources of up to ±10V amplitude.

These DTL TTL CMOS compatible devices feature self-contained binary channel address decoding. An ENABLE line is also made available which allows the user to individually enable a 16-channel group (MPC16S) or an 8-channel group (MPC8D) facilitating channel expansion in either single-node or multitiered matrix configurations.

Digital and analog inputs are failure protected from



FUNCTIONAL BLOCK DIAGRAM–MPC16S

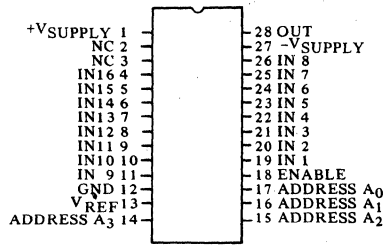


FUNCTIONAL BLOCK DIAGRAM–MPC8D

either overvoltages that exceed the power supplies or from the loss of power.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, high OFF resistance, low feedthrough capacitance and fast settling time.

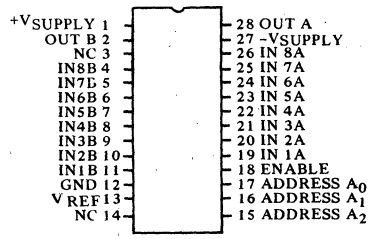
These devices are housed in compact 28-pin dual-in-line packages, and are specified for operation over a 0°C to +75°C temperature range. They are pin and package compatible with the 506 507 series.



MPC16S PIN DIAGRAM

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

TRUTH TABLE–MPC16S



MPC8D PIN DIAGRAM

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

TRUTH TABLE–MPC8D

SPECIFICATIONS

ELECTRICAL

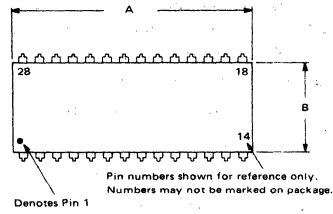
Typical for following conditions:

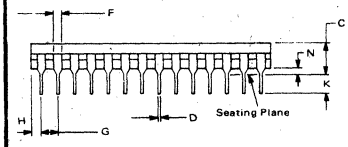
$V+ = +15V$, $V- = -15V$, $R_{source} \leq 1000\Omega$, $T_A = 25°C$ unless otherwise noted.

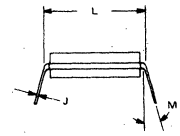
MODELS	MPC16S	MPC8D	UNITS
INPUT			
ANALOG INPUT			
Voltage Range	±15V		V
Maximum Overvoltage	+V supply +20 -V supply -20		V V
Current at Maximum Overvoltage per Channel(1)	±18		mA
Number of Input Channels			
Single-Ended	16		
Differential		8	
Reference Voltage Range(2)	+6 to +10		V
ON Characteristics			
ON Resistance (R_{ON})			
Typical	1.3		kΩ
Maximum	1.8		kΩ
R_{ON} Drift vs. Temperature (0°C to +75°C)	0.25		%/°C
R_{ON} Mismatch			
Channel-to-channel	50	50	Ω
Differential	N/A	50	Ω
Input Leakage (I_L)	1.0		nA
Input Leakage Drift	See Typical Performance Curves		
OFF Characteristics			
OFF Resistance	10^{11}		Ω
Output Leakage			
(all channels disabled)	0.2		nA
Input Leakage(3)	0.02		nA
Leakage Drift	See Typical Performance Curves		
Output Leakage with Input Overvoltage			
of +35V	1		nA
of -35V	1		µA
DIGITAL INPUTS			
Logic "0" (V_L)(1)(4)	-V supply ≤ V_L < 0.8 at 1nA		V
Logic "1" (V_H)(1)(4)	+4 ≤ V_H ≤ +V supply at 1nA		V
Channel Select	4-bit binary code - one of sixteen	3-bit binary code - one of eight	
Enable	Logic "0" (low) disables all channels. Logic "1" (high) enables channel select to turn on selected channel.		
POWER REQUIREMENTS			
Rated Power Supply Voltages	±15		V
Supply Range			
+Supply	+10 to +20		V
-Supply	−10 to −20		V
Supply Drain			
At 1MHz Switching Speed	+4, -2		mA
At 100kHz Switching Speed	±0.5		mA
Typical Power Consumption Dc to 10kHz	75		mW
DYNAMIC CHARACTERISTICS			
Gain Error (20MΩ load) maximum	0.01		%
Crosstalk(5)	0.005		% of OFF channel signal
Settling Time(6)			
To 2mV (0.01%)	7		µsec
To 20mV (0.10%)	3		µsec
Common-mode Rejection, min	N/A	120	dB
Switching Time			
Turn ON	0.5		µsec
Turn OFF	0.3		µsec
Recovery Time from Input Overvoltage Pulse of 35V for 100µsec			
To 0.01%	150		µsec
To 0.10%	15		µsec
OUTPUT			
Voltage Range	±15		V
Capacitance to Ground	50	30(7)	pF
Capacitance Mismatch	N/A	±10	%
TEMPERATURE			
Specification	0 to +75		°C
Storage	-65 to +150		°C

MECHANICAL

NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.







DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.360	1.470	34.54	37.34
B	.500	.550	12.70	13.97
C	– –	.200	– –	5.08
D	.015	.021	0.38	0.53
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.007	.013	0.18	0.33
K	.100	– –	2.54	– –
L	.600 BASIC		15.24 BASIC	
M	– –	15°	– –	15°
N	.020	.090	0.51	2.29

NOTES:
1. Total power dissipation due to input overvoltage current flowing in the input protection circuitry must be limited to one watt for both (a) normal operation with power supplies turned on or (b) during a fault condition when the supplies are shorted to ground.
2. Reference voltage controls noise immunity level. Normally not used (pin 13 left open).
3. Leakage measurement made with all OFF channel inputs fed in parallel to +20V.
4. Maximum overvoltage is $\pm V_{supply}$ ±4V at ±15mA. Logic levels specified are for V_{REF} pin 13 open. For V_{REF} = +10V, $V_{H\ MIN}$ = +6V.
5. 20V, pk-pk 1000Hz sinewave; $R_{source} = 1000\Omega$, same signal on all unused channels.
6. For 20V between switched channels, $R_{source} = 1000\Omega$. See Typical Performance Curves for settling time vs. source impedance (R_S).
7. From each side of MPC8D to ground.

DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and mulitplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.001% loading error and $10k\Omega$ source resistance will increase source loading error to 0.01% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\in_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\% \text{ where } \begin{array}{l} R_S = R_{source} \\ R_L = \text{load resistance} \\ R_{ON} = \text{multiplexer ON resistance.} \end{array}$$

Input Offset Voltage

Bias current generates an input Offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. **A load bias current of 10nA will generate an offset voltage of 20μV if a 1000Ω source is** used, and 200μV if a $10k\Omega$ source is used. In general, for the MPC16S, the Offset voltage at the output is determined by:

$$V_{OFFSET} = (I_b + I_L)(R_{ON} + R_{source}) \quad \text{where}$$

I_b = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{source} = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC8D is used for multiplexing high-level signals of 1V to 10V full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

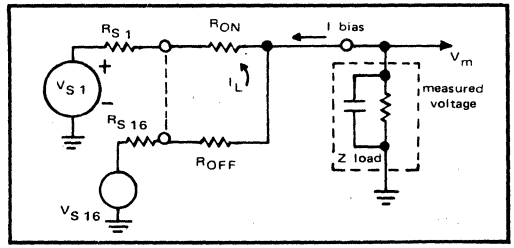


FIGURE 1. MPC16S State Accuracy Equivalent Circuit.

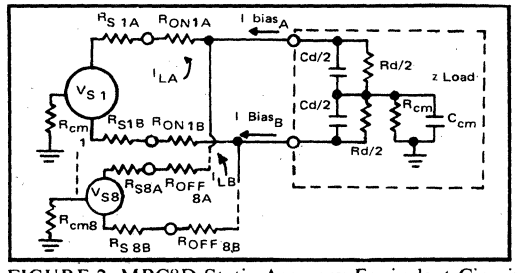


FIGURE 2. MPC8D Static Accuracy Equivalent Circuit.

SETTLING TIME

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C(dV/dt)$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$dV_{load} = (i/C)dt$
where $i = C(dV/dt)$ of the CMOS FET switches
C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The settling time for smaller step changes on the input will be less than that shown in the graph.

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 7 (MPC8D) or 15 (MPC16S) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{source} impedances of the ON channel. Crosstalk is measured with a 20V, pk-pk 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (MPC8D ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC8D, protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

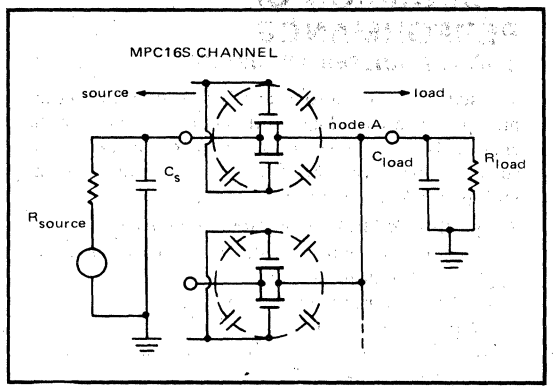


FIGURE 3. Settling Time Effects–MPC16S.

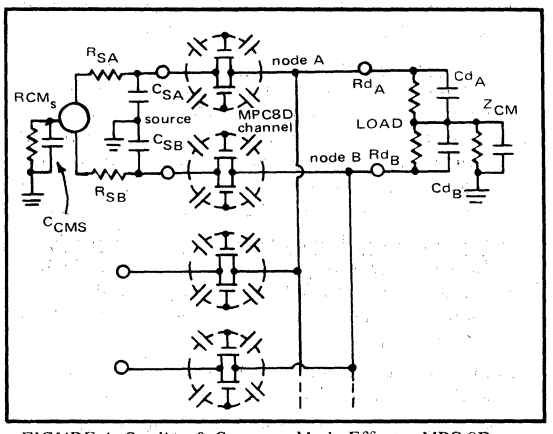


FIGURE 4. Settling & Common-Mode Effects–MPC-8D.

The CMR of the MPC8D and Burr-Brown's model 3660 instrumentation amplifier is 110dB at DC to 1Hz with a 6dB octave rolloff to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3660 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

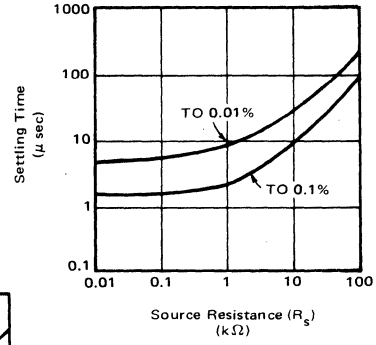
Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance.

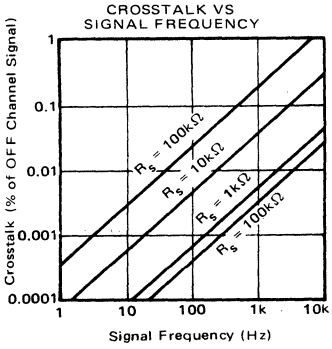
AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

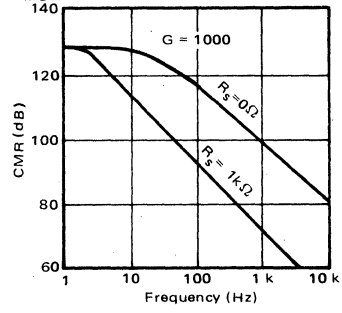
SETTLING TIME VS SOURCE RESISTANCE FOR 20V STEP CHANGE



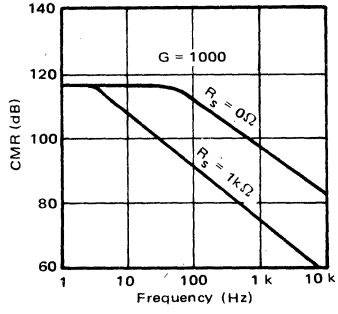
CROSSTALK VS SIGNAL FREQUENCY



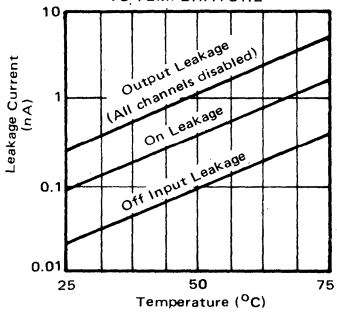
CMR VS FREQUENCY FOR MODEL 3660 IA AND MPC8D (G = 1000)



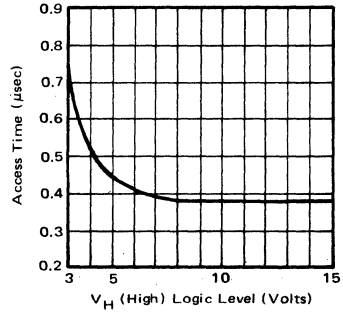
COMBINED CMR VS FREQUENCY FOR MODEL 3660 IA AND MPC8D (G = 1000)



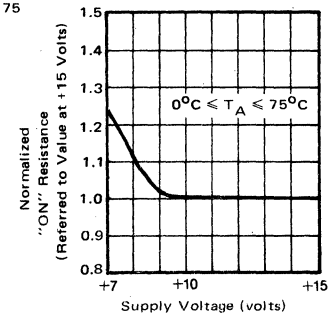
LEAKAGE CURRENT VS TEMPERATURE



ACCESS TIME VS LOGIC LEVEL (HIGH)



NORMALIZED "ON" RESISTANCE VS SUPPLY VOLTAGE



The ENABLE input, pin 18, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the 3-bit (MPC8D) or 4-bit (MPC16S) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15V and/or -15V supply voltage is absent or shorted to ground, the MPC8D and MPC16S multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded (see Note 1 of Electrical Specifications).

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended (see Typical Performance Curves, access time).

To preserve common-mode rejection of the MPC8D, use twisted-shielded pair wire for signal lines and inter-tier connections and or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

SINGLE-ENDED MULTIPLEXER (MPC16S)

Up to 64 channels (4 multiplexers) can be connected to a single-node, or up to 256 channels using 17 MPC16S multiplexers on a two-tiered structure as shown in Figures 5 and 6.

DIFFERENTIAL MULTIPLEXER (MPC8D)

Single or multi-tiered configurations can be used to expand multiplexer channel capacity up to 64 channels using a 64 x 1 or 8 x 8 configuration.

SINGLE-NODE EXPANSION

The 64 x 1 configuration is simply eight MPC8D units tied to a single-node. Programming is accomplished with a 6-bit counter, using the 3LSB of the counter to control Channel Address inputs A_0, A_1 and A_2 and the 3MSB of the counter to drive an 8 of 1 decoder. The 8 of 1 decoder then is used to drive the ENABLE inputs (pin 18) of the MPC8D multiplexers.

TWO-TIER EXPANSION

Using an 8 x 8 two-tier structure for expansion to 64 channels, the programming is simplified. The 6-bit counter output does not require an 8 of 1 decoder. The 3LSB of the counter drive the A_0, A_1, and A_2 inputs of the eight first tier multiplexers and the 3MSB of the counter are applied to the A_0, A_1, and A_2 inputs of the second tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (8 or 16) in the multitiered configuration.

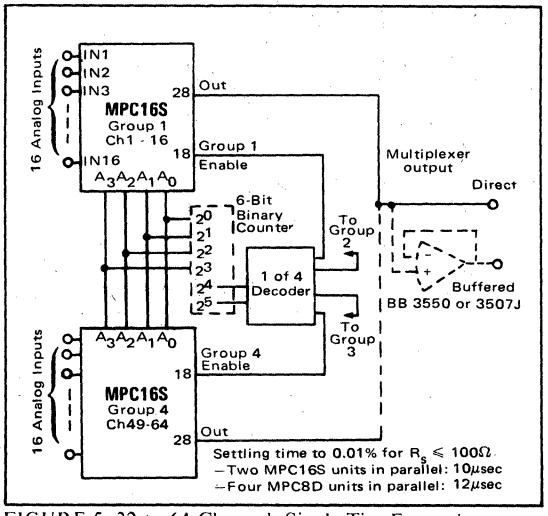


FIGURE 5. 32 to 64 Channel, Single-Tier Expansion.

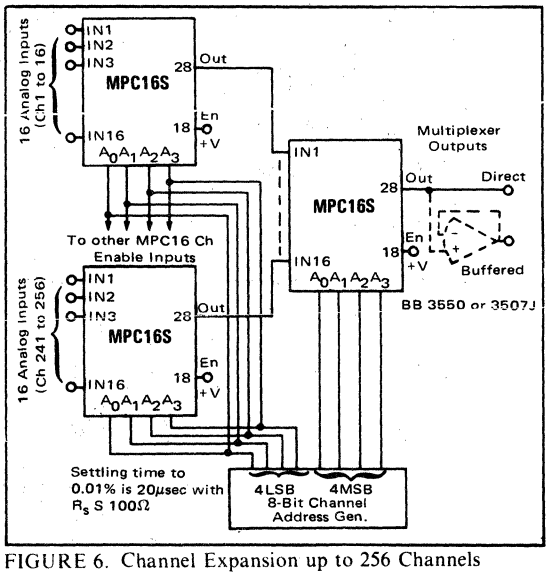


FIGURE 6. Channel Expansion up to 256 Channels Using 16 x 16 Two-Tiered Expansion.

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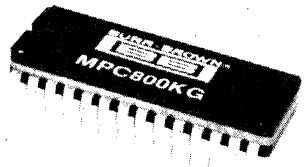
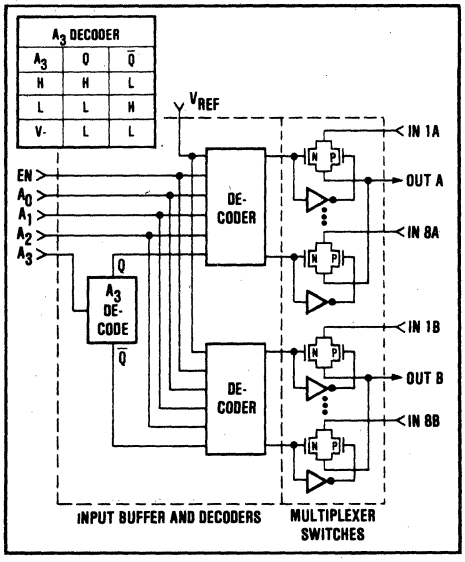


MPC800

High Speed CMOS ANALOG MULTIPLEXER

FEATURES

- HIGH SPEED
  - 100nsec access time
  - 800nsec settling to 0.01%
  - 250nsec settling to 0.1%
- USER-PROGRAMMABLE
  - 16-channel single-ended or
  - 8-channel differential
- SELECTABLE TTL or CMOS COMPATIBILITY
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER
- 28-PIN HERMETIC DUAL-IN-LINE PACKAGE



DESCRIPTION

The MPC800 is a high speed multiplexer that is user-programmable for 16-channel single-ended operation or 8-channel differential operation and for TTL or CMOS compatibility.

The MPC800 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC800KG for operation from 0°C to +75°C and the MPC800SG for operation from -55°C to +125°C.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

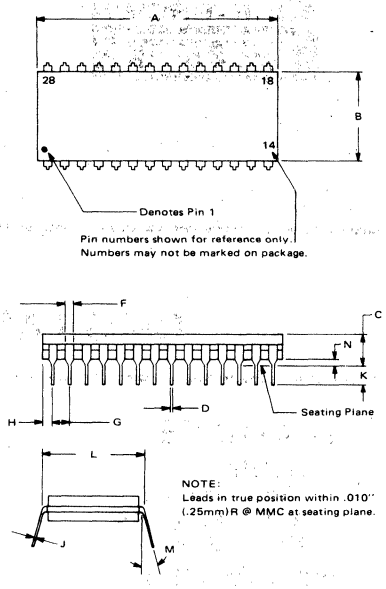
SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

MODEL	MPC800KG, MPC800SG			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
ANALOG INPUT				
Voltage Range	-15		+15	V
Maximum Overvoltage	-V_{CC} -2		+V_{CC}, +2	V
Number of Input Channels				
Differential	8			
Single-Ended	16			
Reference Voltage Range(1)	6		10	V
ON Characteristics(2)				
ON Resistance (R_{ON}) at +25°C		620	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature	See Typical Performance Curves			
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0.04		nA
Over Temperature Range		0.6	100	nA
ON Channel Leakage Drift	See Typical Performance Curves			
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.01		nA
Over Temperature Range		0.38	50	nA
OFF Channel Input Leakage Drift	See Typical Performance Curves			
OFF Channel Output Leakage		0.035		nA
Over Temperature Range		0.48	100	nA
OFF Channel Output Leakage Drift	See Typical Performance Curves			
Output Leakage (All channels disabled)(3)		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
-16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL(4)				
Logic "0" (V_{AL})			0.8	V
Logic "1" (V_{AH})	2.4			V
I_{AH}		0.05	1	μA
I_{AL}		4	25	μA
TTL Input Overvoltage	-6		6	V
CMOS				
Logic "0" (V_{AL})			0.3V_{REF}	V
Logic "1" (V_{AH})	0.7 V_{REF}			V
CMOS Input Overvoltage	-2		+V_{CC} +2	V
Address A_3 Overvoltage	-V_{CC} -2		+V_{CC} +2	V
Digital Input Capacitance		5		pF
Channel Select(5)				
Single-Ended	4-bit binary code one of 16			
Differential	3-bit binary code one of 8			
Enable	Logic "0" inhibits all channels			
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between Supply Pins			33	V
Total Power Dissipation		525		mW
Allowable Total Power Dissipation(6)			1200	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+35, -39		mA
At 100kHz Switching Speed		+25, -29		mA
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Cross Talk(7)	See Typical Performance Curves			
T_{OPEN} (Break before make delay)		20		nsec
Access Time at +25°C		100	150	nsec
Over Temperature Range		120	200	nsec
Settling Time(8)				
to 0.1% (20mV)		250		nsec
to 0.01% (2mV)		800		nsec
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
Channel Input Capacitance, C_S (off)		2.5		pF
Channel Output Capacitance, C_O (off)		18		pF
Input to Output Capacitance, C_{DS} (off)		0.02		pF

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.360	1.475	34.54	37.47
B	.500	.550	12.70	13.97
C	---	.220	---	5.59
D	.015	.021	0.38	0.53
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.007	.013	0.18	0.33
K	.100	---	2.54	---
L	.600 BASIC		15.24 BASIC	
M	---	15°	---	15°
N	.020	.090	0.51	2.29

PIN CONFIGURATION

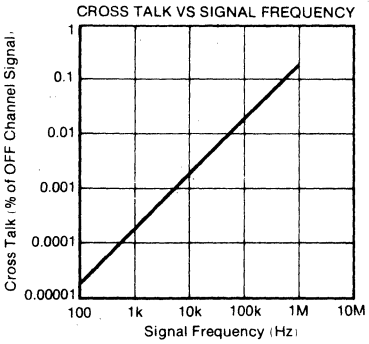
TOP VIEW

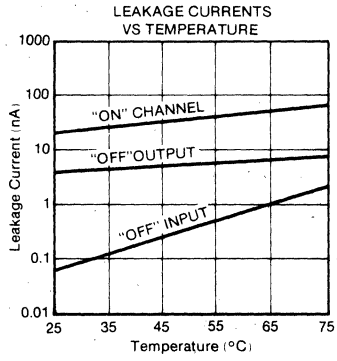
+V_{CC}	1	28	OUT A
OUT B	2	27	-V_{CC}
NC	3	26	IN 8/8A
IN16/8B	4	25	IN7/7A
IN15/7B	5	24	IN6/6A
IN14/6B	6	23	IN5/5A
IN13/5B	7	22	IN4/4A
IN12/4B	8	21	IN3/3A
IN11/3B	9	20	IN2/2A
IN10/2B	10	19	IN1/1A
IN9/1B	11	18	ENABLE
GND	12	17	A_0
V_{REF}	13	16	A_1
A_3	14	15	A_2

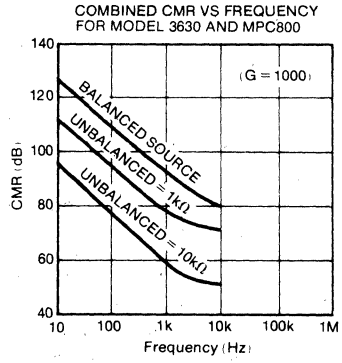
MODEL	MPC800KG, MPC800SG			
PARAMETER	MIN	TYP	MAX	UNITS
TEMPERATURE				
MPC800KG				
Specification	0		+75	°C
Storage	-65		+150	°C
MPC800SG				
Specification	-55		+125	°C
Storage	-65		+150	°C

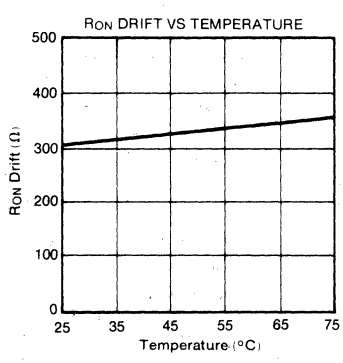
NOTES:
1. Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility.
2. $V_{IN} = \pm 10V$, $I_{OUT} = 100\mu A$.
3. Single-ended mode.
4. Logic levels specified for V_{REF} (pin 13) open.
5. For single-ended operation, connect output A (pin 28) to output B (pin 2) and use A_3 (pin 14) as an address line. For differential operation connect A_3 to -V_{CC}.
6. Derate 8mW/°C above $T_A = +75°C$.
7. 10V, p-p, sine wave on all unused channels. See Typical Performance Curves.
8. For 20V step input to ON channel, into 1kΩ load.

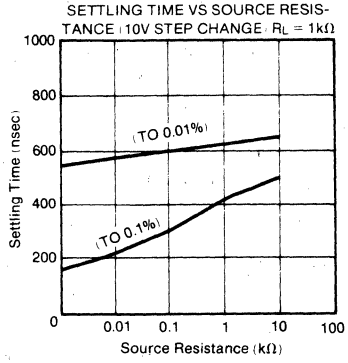
TYPICAL PERFORMANCE CURVES











DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

RESISTIVE LOADING ERRORS

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.002% loading error and $10k\Omega$ source resistance will increase source loading error 0.02% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\epsilon\ (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = R_{source}
R_L = Load Resistance
R_{ON} = Multiplexer ON resistance

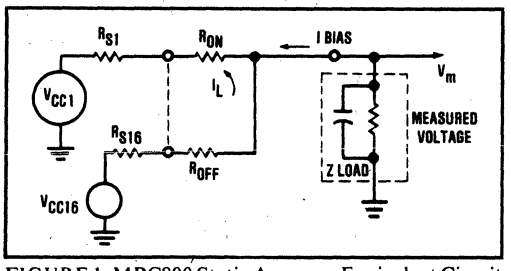


FIGURE 1. MPC800 Static Accuracy Equivalent Circuit (Single-ended Operation).

Input Offset Voltage

Bias and leakage currents generate an input Offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of $19\mu V$ if a 1000Ω source is used, and $118\mu V$ if a $10k\Omega$ source is used. In general, for the MPC800 the Offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_{source}) \text{ where}$$

I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{source} = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

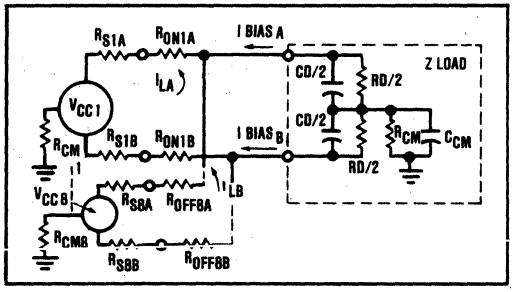


FIGURE 2. MPC800 Static Accuracy Equivalent Circuit (Differential Operation).

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC800 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low level signal applications

SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input. The settling time of the MPC800 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RC's. For the MPC800 the internal capacitance is approximately 20pF differential or 40pF single-ended. With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40nsec. This means the source resistance should be kept to less than 2kΩ (assume high load resistance) to maintain fast settling times.

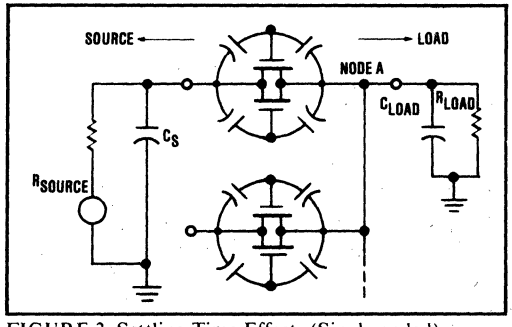


FIGURE 3. Settling Time Effects (Single-ended).

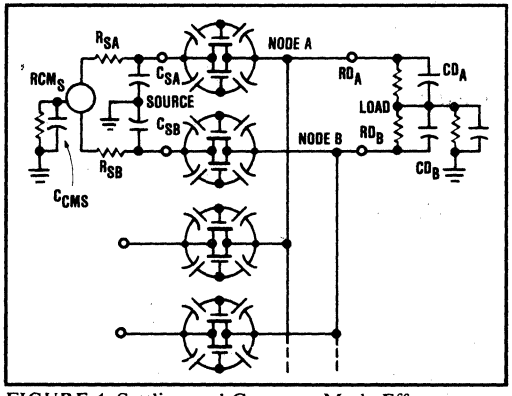


FIGURE 4. Settling and Common-Mode Effects (Differential).

ACCESS TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 7 differential or 15 single-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{source} impedances of the ON channel. Crosstalk is measured with a 20V, pk-pk, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (DIFFERENTIAL MODE ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC800 and Burr-Brown's model 3630 Instrumentation Amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.

- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.
- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION & OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC800 use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{REF} (pin 13) open or CMOS-compatible by connecting the V_{REF} to V_{DD} (CMOS supply voltage).

16-CHANNEL SINGLE-ENDED OPERATION

To use the MPC800 as a 16-channel single-ended multiplexer, output A (pin 28) is connected to output B (pin 2) to form a single output, then all four address lines (A_0, A_1, A_2 and A_3) are used to address the correct channel.

The MPC800 can also be used as a dual 8-channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

8-CHANNEL DIFFERENTIAL OPERATION

To use the MPC800 as an 8-channel differential multiplexer, connect address line A_3 to $-V_{CC}$ then use the remaining three address lines (A_0, A_1 and A_2) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC800 used as 16-channel single-ended multiplexer or 8-channel dual multiplexer.

USE A_3 AS DIGITAL ADDRESS INPUT					"ON" CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

For 16-channel single-ended function, tie "out A" to "out B, for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

MPC800 used as 8-channel differential multiplexer.

A_3 CONNECT TO $-V_{CC}$				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

CHANNEL EXPANSION

Single-tier Expansion

Up to four MPC800's can be connected to a single node to form a 64-channel single-ended multiplexer or up to eight MPC800's can be connected to two nodes to form a 64-channel differential multiplexer. Programming is accomplished with a six-bit address and a 1 of 4 decoder for 64-channel single-ended expansion (see Figure 5) or an eight-bit address and a 1 of 8 decoder for 64-channel

differential expansion. The decoder drives the enable inputs of the MPC800, turning on only one multiplexer at a time.

Two-tier Expansion

Up to seventeen MPC800's can be connected in a two-tier structure to form a 256-channel single-ended multiplexer (see Figure 6) or up to nine MPC800's can be connected in a two-tier structure to form a 64-channel differential multiplexer. Programming is accomplished with a 8-bit address.

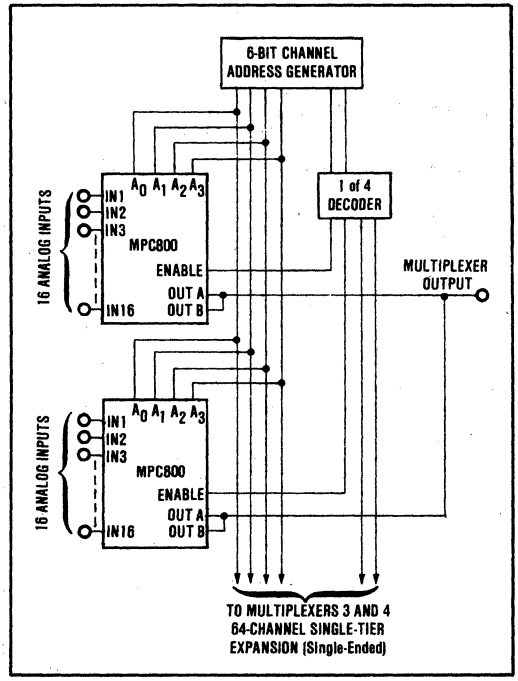


FIGURE 5. 32- to 64-Channel, Single-tier Expansion.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF-channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one-channel group is failed (8 or 16) in the multitiered configuration.

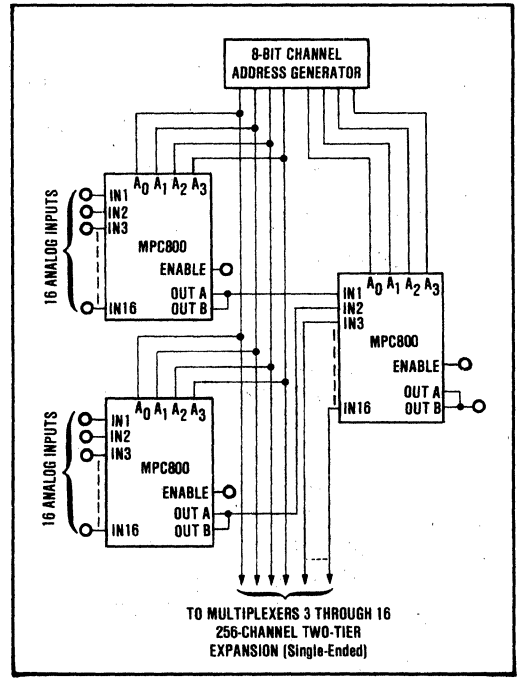
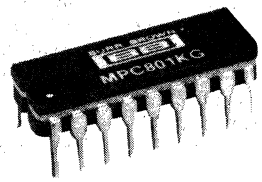


FIGURE 6. Channel Expansion up to 256 Channels using 16 x 16 Two-tiered Expansion.

BURR-BROWN®

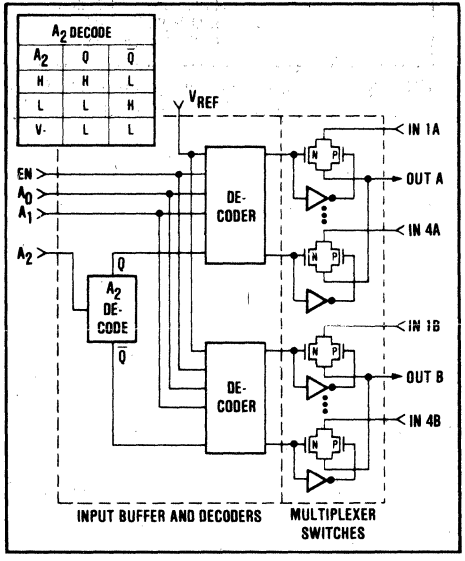


MPC801

High Speed CMOS ANALOG MULTIPLEXER

FEATURES

- HIGH SPEED
  - 80nsec access time
  - 800nsec settling to 0.01%
  - 250nsec settling to 0.1%
- USER-PROGRAMMABLE
  - 8-channel single-ended or
  - 4-channel differential
- SELECTABLE TTL or CMOS COMPATIBILITY
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER
- 18-PIN HERMETIC DUAL-IN-LINE PACKAGE



DESCRIPTION

The MPC801 is a high speed multiplexer that is user-programmable for 8-channel single-ended operation or 4-channel differential operation and for TTL or CMOS compatibility.

The MPC801 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC801KG for operation from 0°C to +75°C and the MPC801SG for operation from -55°C to +125°C.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

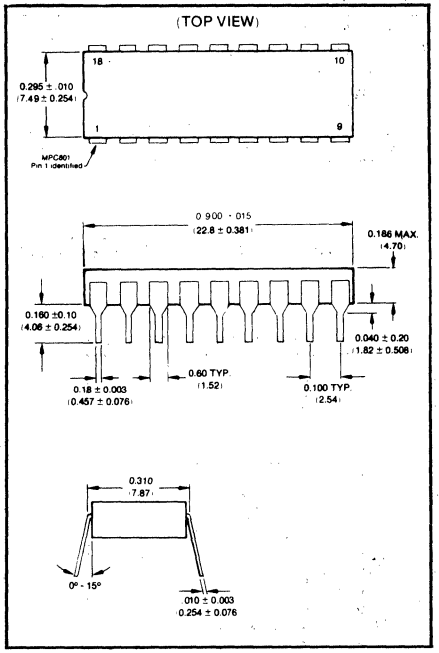
SPECIFICATIONS

ELECTRICAL

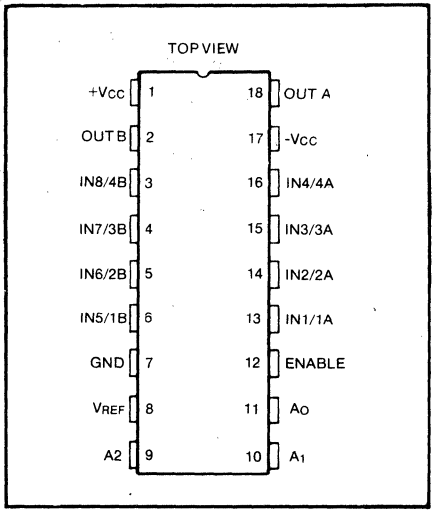
At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL	MPC801KG, MPC801SG			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
ANALOG INPUT				
Voltage Range	-15		+15	V
Maximum Overvoltage	$-V_{CC}$ -2		$+V_{CC}$ +2	V
Number of Input Channels				
Differential	4			
Single-Ended	8			
Reference Voltage Range(1)	6		10	V
ON Characteristics(2)				
ON Resistance (R_{ON}) at +25°C		500	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature	See Typical Performance Curves			
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0.1		nA
Over Temperature Range		0.3	50	nA
ON Channel Leakage Drift	See Typical Performance Curves			
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.05		nA
Over Temperature Range		0.6	50	nA
OFF Channel Input Leakage Drift	See Typical Performance Curves			
OFF Channel Output Leakage		0.1		nA
Over Temperature Range		0.30	50	nA
OFF Channel Output Leakage Drift	See Typical Performance Curves			
Output Leakage (All channels disabled)(3)		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
-16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL(4)				
Logic "0" (V_{AL})			0.8	V
Logic "1," (V_{AH})	2.4			V
I_{AH}		0.05	1	μA
I_{AL}		4	20	μA
TTL Input Overvoltage	-6		6	V
CMOS				
Logic "0" (V_{AL})			$0.3V_{REF}$	V
Logic "1" (V_{AH})	$0.7\ V_{REF}$			V
CMOS Input Overvoltage	-2		$+V_{CC}$ +2	V
Address A_2 Overvoltage	$-V_{CC}$ -2		$+V_{CC}$ +2	V
Digital Input Capacitance		5		pF
Channel Select(5)				
Single-Ended	3-bit binary code one of 8			
Differential	2-bit binary code on of 4			
Enable	Logic "0" inhibits all channels			
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between Supply Pins			33	V
Total Power Dissipation		360		mW
Allowable Total Power Dissipation(6)			725	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+14, -12.5		mA
At 100kHz Switching Speed		+12.5,-12.5		mA
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Cross Talk(7)	See Typical Performance Curves			
T_{OPEN} (Break before make delay)		20		nsec
Access Time at 25°C		80	125	nsec
Over Temperature Range		110	150	nsec
Settling Time(8)				
to 0.1% (20mV)		250		nsec
to 0.01% (2mV)		800		nsec
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
OFF Channel Input Capacitance, C_S (off)		1.9		pF
OFF Channel Output Capacitance, C_O (off)		10		pF
OFF Input to Output Capacitance, C_{DS} (off)		0.02		pF

MECHANICAL



PIN CONFIGURATION

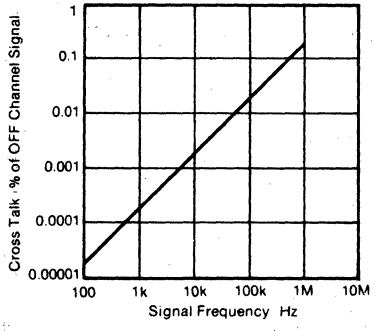


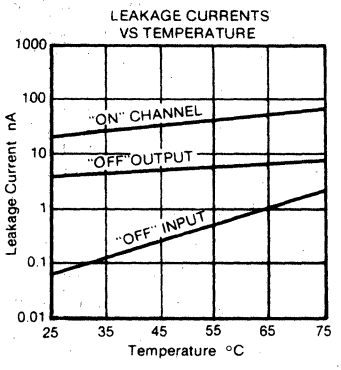
ELECTRICAL (CONT)

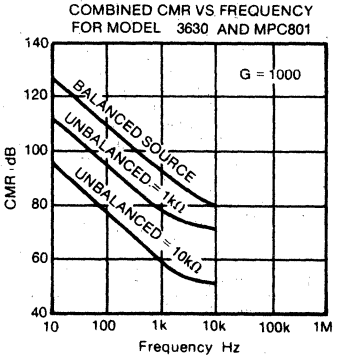
MODEL	MPC801KG, MPC801SG			
PARAMETER	MIN	TYP	MAX	UNITS
TEMPERATURE				
MPC801KG				
Specification	0		+75	°C
Storage	-65		+150	°C
MPC801SG				
Specification	-55		+125	°C
Storage	-65		+150	°C

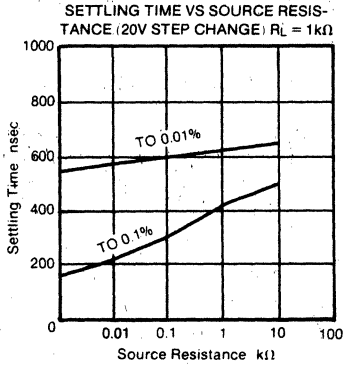
NOTES:
1. Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility.
2. $V_{IN} = \pm 10V$, $I_{OUT} = 100\mu A$.
3. Single-ended mode.
4. Logic levels specified for V_{REF} (pin 8) open.
5. For single-ended operation, connect output A (pin 18) to output B pin 2 and use A_2 (pin 9) as an address line. For differential operation connect A_2 to $-V_{CC}$.
6. Derate 8mW/°C above $T_A = +75°C$.
7. 10V, p-p, sine wave on all unused channels. See Typical Performance Curves.
8. For 20V step input to ON channel, into 1kΩ load.

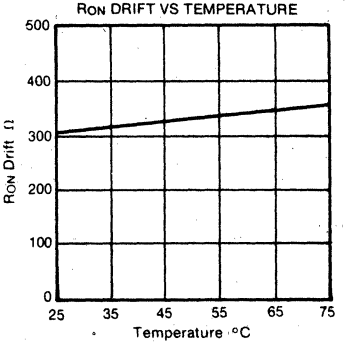
TYPICAL PERFORMANCE CURVES











DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

RESISTIVE LOADING ERRORS

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.002% loading error and $10k\Omega$ source resistance will increase source loading error 0.02% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\epsilon\,(R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\% \text{ where}$$

$R_S = R_{source}$
R_L = Load resistance
R_{ON} = Multiplexer ON resistance.

Input Offset Voltage

Bias and leakage currents generate an input Offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of $19\mu V$ if a 1000Ω source is used, and $118\mu V$ if a $10k\Omega$ is used. In general, for the MPC801 the Offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_{source}) \text{ where}$$

I_B = Bias Current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{source} = Source resistance.

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

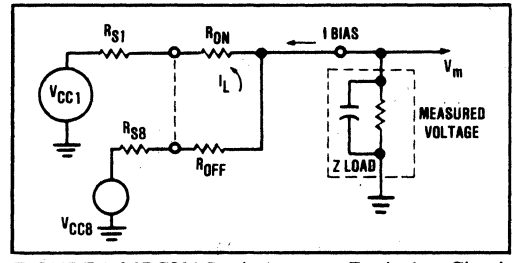


FIGURE 1. MPC801 Static Accuracy Equivalent Circuit (Single-ended Operation).

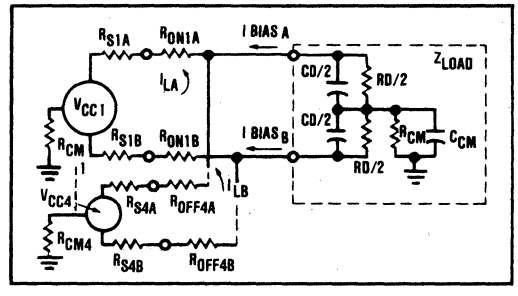


FIGURE 2. MPC801 Static Accuracy Equivalent Circuit (Differential Operation).

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC801 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low level signal applications

SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input. The settling time of the MPC801 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RC's. For the MPC801 the internal capacitance is approximately 10pF differential or 20pF single-ended.

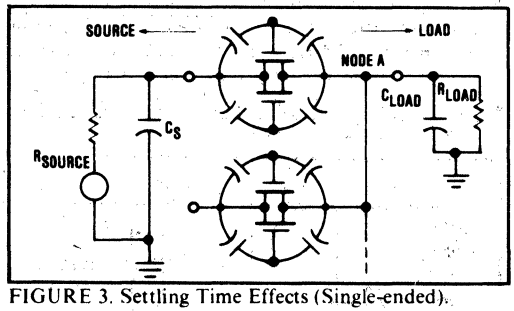


FIGURE 3. Settling Time Effects (Single-ended).

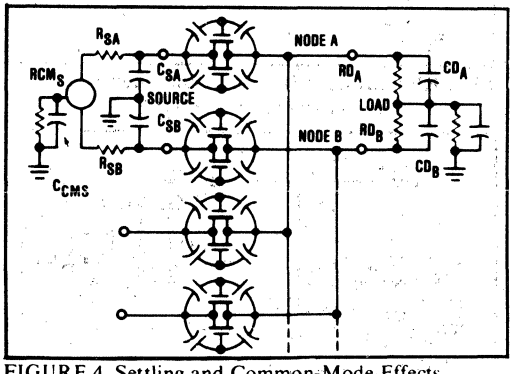


FIGURE 4. Settling and Common-Mode Effects (Differential).

With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40nsec. This means the source resistance should be kept to less than 4kΩ (assume high load resistance) to maintain fast settling times.

ACCESS TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 3 differential or 7 single-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{source} impedances of the ON channel. Crosstalk is measured with a 20V, pk-pk, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (DIFFERENTIAL MODE ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC801 and Burr-Brown's model 3630 Instrumentation Amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.
- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.

- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION & OPERATING INSTRUCTIONS

The ENABLE input, pin 12, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC801 use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{REF} (pin 8) open or CMOS-compatible by connecting the V_{REF} to V_{DD} (CMOS supply voltage).

8-CHANNEL SINGLE-ENDED OPERATION

To use the MPC801 as an 8-channel single-ended multiplexer, output A (pin 18) is connected to output B (pin 2) to form a single output, then all three address lines (A_0, A_1, and A_2) are used to address the correct channel.

The MPC801 can also be used as a dual channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

4-CHANNEL DIFFERENTIAL OPERATION

To use the MPC801 as an 4-channel differential multiplexer, connect address line A_2 to $-V_{CC}$ then use the remaining two address lines (A_0 and A_1) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC801 used as 8-channel single-ended multiplexer or 4-channel dual multiplexer.

USE A_2 AS DIGITAL ADDRESS INPUT				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

For 8-channel single-ended function, tie "out A" to "out B", for dual 4-channel function use the A_2 address pin to select between MUX A and MUX B, where MUX A is selected with A_2 low.

MPC801 used as 4-channel differential multiplexer.

A_2 CONNECT TO $-V_{CC}$			"ON" CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

CHANNEL EXPANSION

Single-tier Expansion

Up to eight MPC801's can be connected to a single node to form a 64-channel single-ended multiplexer or up to eight MPC801's can be connected to two nodes to form a 32-channel differential multiplexer. Programming is accomplished with a 6-bit address and a 1 of 8 decoder (Figure 5). The decoder drives the enable inputs of the MPC801, turning on only one multiplexer at a time.

Two-tier Expansion

Up to nine MPC801's can be connected in a two-tier structure to form a 64-channel single-ended multiplexer (Figure 6) or up to five MPC801's can be connected in a two-tier structure to form a 16-channel differential multiplexer. Programming is accomplished with a 6-bit address.

SINGLE VS MULTITIERED CHANNEL EXPANSION

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-

node configuration, data cannot be taken from any channel, whereas only one channel group is failed (4 or 8) in the multitiered configuration.

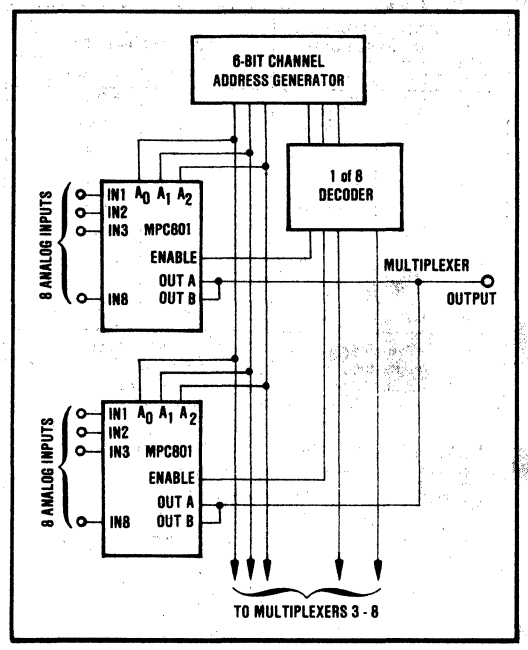


FIGURE 5. 64-Channel, Single-Tier, Single-Ended Expansion.

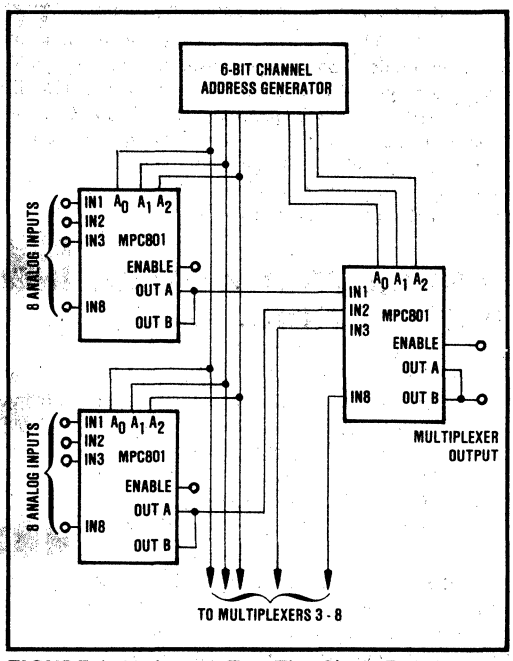
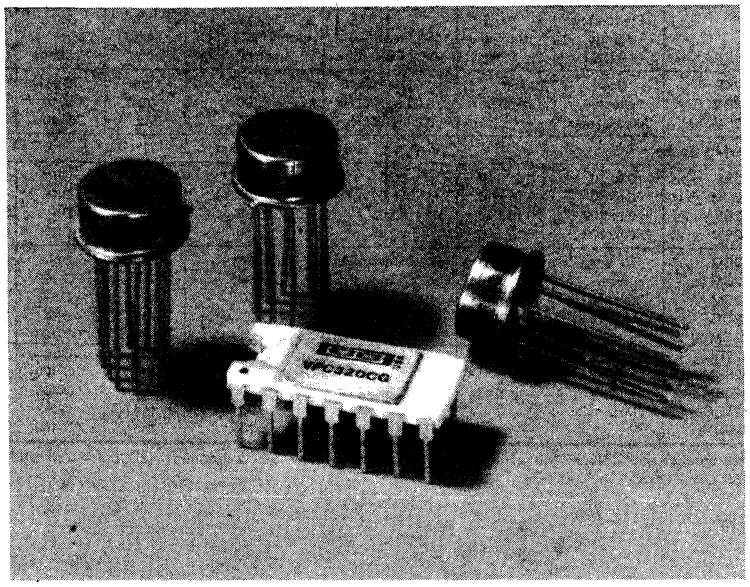


FIGURE 6. 64-channel, Two-Tier, Single-Ended Expansion.

VOLTAGE TO FREQUENCY CONVERTERS



VFC's provide a simple, low cost way of converting analog signals into digital form. They provide an important alternative to other analog to digital conversion techniques. Their integrating input properties make them an appropriate choice when operating in noisy environments. The combination of high accuracy and linearity, low temperature drift, and monotonicity often provide performance characteristics unattainable with other techniques.

Since an analog quantity represented as a frequency is inherently serial data, it is easily handled in large multi-channel systems. Frequency information can be transmitted over long lines with excellent noise immunity using low cost digital line transmitters and receivers. Isolation can be accomplished with optical or transformer couplers without loss in accuracy. Outputs from multiple VFC's can be gated to common counter circuitry with simple digital logic.

Burr-Brown monolithic VFC's include the VFC32, VFC62, and VFC320 which provide industry standard performance and reliability in such applications as precision test and measurement equipment, data acquisition systems, and communications equipment.

SELECTION GUIDE

V/F CONVERTERS								
Description	Model[1]	Frequency Range (kHz)	V_{IN} Range (V)	Linearity (% of FSR) max	Tempco (ppm of FSR/°C) max	Temp Range[2]	Package	Page
Low Cost, Monolithic	VFC32KP	User-selected, 500kHz, max	User-selected	±0.01 at 10kHz	75 typ	Com	DIP	10-3
	VFC32BM, (Q)			±0.05 at 100kHz	±100	Ind	TO-100	10-3
	VFC32SM, (Q)			±0.2 at 500kHz	±150	MIL	TO-100	10-3
Military	VFC32/MIL Series	See Military Products						
Hybrid, Complete	VFC42BP	0 to 10	0 to +10	±0.01	±100	Ind	DIP	10-11
	VFC42SM	0 to 10	0 to +10	±0.01	±100	MIL	DIP	10-11
	VFC52BP	0 to 100	0 to +10	±0.05	±150	Ind	DIP	10-11
	VFC52SM	0 to 100	0 to +10	±0.05	±150	MIL	DIP	10-11
High Performance, Monolithic	VFC62BG	User-selected, 1MHz max	User-selected	±0.005 at 10kHz	±50	Ind	DIP	10-17
	VFC62BM			±0.005 at 10kHz	±50	Ind	TO-100	10-17
	VFC62SM			±0.005 at 10kHz	±50	MIL	TO100	10-17
	VFC62CG			±0.002 at 10kHz	±20	Ind	DIP	10-17
	VFC62CM			±0.002 at 10kHz	±20	Ind	TO-100	10-17
	VFC320BG	User-selected, 1MHz max	User-selected	±0.005 at 10kHz	±50	Ind	DIP	10-25
	VFC320BM			±0.005 at 10kHz	±50	Ind	TO-100	10-25
	VFC320SM			±0.005 at 10kHz	±50	MIL	TO-100	10-25
	VFC320CG			±0.002 at 10kHz	±20	Ind	DIP	10-25
	VFC320CM			±0.002 at 10kHz	±20	Ind	TO-100	10-25

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See Q Program. (2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

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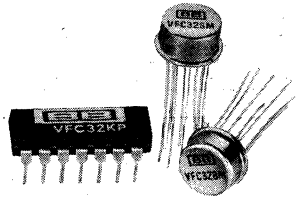


VFC32

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- RELIABLE MONOLITHIC CONSTRUCTION
- HIGH LINEARITY
  - ±0.01% max at 10kHz FS
  - ±0.05% max at 100kHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- VOLTAGE OR CURRENT INPUT
- OUTPUT DTL/TTL/CMOS COMPATIBLE

APPLICATIONS

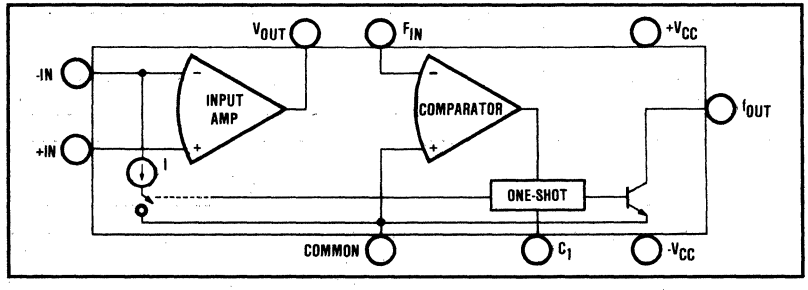
- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC32 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families.

The converter requires two external resistors and two external capacitors to operate. Full scale frequency and input voltage are determined by one resistor (in series with -IN) and two capacitors (one-shot timing and input amplifier integration). High linearity is achieved with relatively few external components, e.g., ±0.01% at 10kHz. The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$).

The VFC32 is available in three models and two package configurations. The TO-100 versions are hermetically sealed, and specified for the -25°C to +85°C and -55°C to +125°C ranges, and the epoxy dual-in-line unit is specified from 0°C to +70°C.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC32KP MIN	VFC32KP TYP	VFC32KP MAX	VFC32BM MIN	VFC32BM TYP	VFC32BM MAX	VFC32SM MIN	VFC32SM TYP	VFC32SM MAX	UNITS
INPUT (V/F CONVERTER)	$F_{OUT} = V_{IN} / 7.5\ R_1C_1$, Figure 6										
Voltage Range[1]											
Positive Input		>0		+0.25mA x R_1	*		*	*		*	V
Negative Input		>0		-10	*		*	*		*	V
Current Range[1]		>0		+0.25	*		*	*		*	mA
Bias Current											
Inverting Input			20	100		*	*		*	*	nA
Noninverting Input			100	250		*	*		*	*	nA
Offset Voltage[2]			1	4		*	*		*	*	mV
Differential Impedance		300 ‖ 10	650 ‖10		*	*		*	*		kΩ ‖ pF
Common-mode Impedance		300 ‖ 3	500 ‖ 3		*	*		*	*		MΩ ‖ pF
INPUT (F/V CONVERTER)	$V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9										
Impedance		50 ‖ 10	150 ‖ 10		*	*		*	*		kΩ ‖ pF
Logic "1"			+1.0		*		*	*		*	V
Logic "0"			−0.05		*		*	*		*	V
Pulse-width Range		0.1		150k/F_{MAX}	*		*	*		*	µsec
ACCURACY											
Linearity Error[3]	0.01Hz ≤ oper freq ≤ 10kHz		±0.005	±0.010[4]		*	*		*	*	% of FSR[5]
	0.1Hz ≤ oper freq ≤ 100kHz		±0.025	±0.05		*	*		*	*	% of FSR
	0.5Hz ≤ oper freq ≤ 500kHz		±0.05			*			*		% of FSR
Offset Error Input											
Offset Voltage[2]			1	4		*	*		*	*	mV
Offset Drift[6]			±3			*			*		ppm of FSR/°C
Gain Error[2]			5			*	*		*	*	% of FSR
Gain Drift[6]	f = 10kHz		±75			±50	±100		±70	±150	ppm/°C
Full Scale Drift (offset drift & gain drift)[6][7]	f = 10kHz		±75			±50	±100		±70	±150	ppm of FSR/°C
Power Supply Sensitivity	f = DC, ±V_{CC} = 12VDC to 18VDC			±0.015			*			*	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, Logic "0"	I_{SINK} = 8mA	0	0.2	0.4	*	*	*	*	*	*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*		*	*	µA
Voltage, Logic "1"	External pull-up resistor required (see Figure 4)			V_{PU}			*			*	V
Pulse Width	For Best Linearity		0.25/F_{MAX}			*			*		sec
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			*			*	nsec
OUTPUT (F/V CONVERTER) V_{OUT}											
Voltage	I_o ≤ 7mA	0 to +10			*			*			V
Current	V_o ≤ 7VDC	+10			*			*			mA
Impedance	Closed loop			1			*			*	Ω
Capacitive Load	Without oscillation			100			*			*	pF
DYNAMIC RESPONSE											
Full Scale Frequency				500[8]	*			*			kHz
Dynamic Range		6			*			*			decades
Settling Time	V/F to specified linearity for a full scale input step		[9]			*			*		
Overload Recovery	< 50% overload		[9]			*			*		
POWER SUPPLY											
Rated Voltage			±15								V
Voltage Range		±11		±20					*		V
Quiescent Current			±5.5	±6.0		*	*		*		mA
TEMPERATURE RANGE											
Specification		0		+70	-25		+85	-55		+125	°C
Operating		-25		+85	-55		+125	-55		+125	°C
Storage		-25		+85	-65		+150	-65		+150	°C

*Specification the same as VFC32KP

NOTES:
1. A 25% duty cycle (0.25mA input current) is recommended where possible to achieve best linearity.
2. Adjustable to zero. See Offset and Gain Adjustment section.
3. Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. Above 200kHz, it is recommended all grades be operated below +85°C.
4. ±0.015% of FSR for negative inputs shown in Figure 7. Positive inputs are shown in Figure 6.
5. FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).
6. Exclusive of external components' drift.
7. Positive drift is defined to be increasing frequency with increasing temperature.
8. For operation above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections.
9. One pulse of new frequency plus 1μsec.

ABSOLUTE MAXIMUM RATINGS

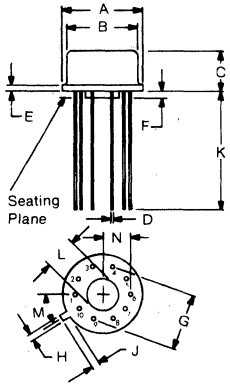
Supply Voltages	±22
Output Sink Current (F_{OUT})	50mA
Output Current (V_{OUT})	+20mA
Input Voltage, −Input	±Supply
Input Voltage, +Input	±Supply
Comparator Input	±Supply
Storage Temperature Range	
VFC32BM, SM	−65°C to +150°C
VFC32KP	−25°C to +85°C

MECHANICAL

VFC32BM, VFC32SM TO-100 PACKAGE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

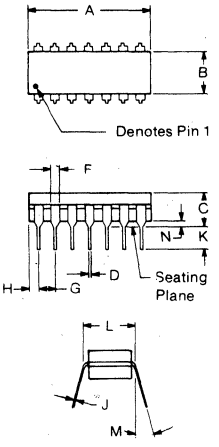
Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

VFC32KP EPOXY DUAL-IN-LINE

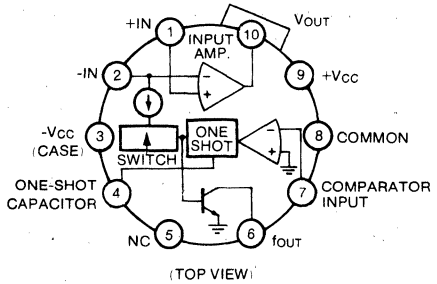
NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.660	.785	16.76	19.94
B	.220	.280	5.59	7.11
C		.200		5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100		2.54	
L	.300 BASIC		7.62 BASIC	
M		15°		15°
N	.020	.050	0.51	1.27

PIN CONFIGURATIONS

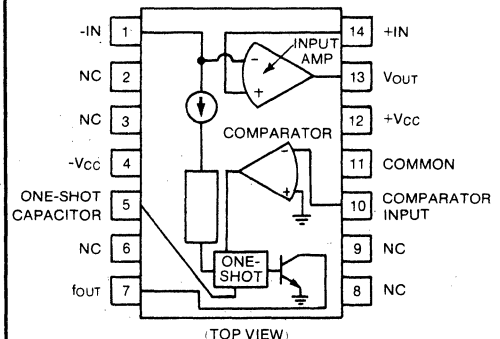
VFC32BM, VFC32SM
TO-100 PACKAGE



(TOP VIEW)

NC = NO INTERNAL CONNECTION.
EXTERNAL CONNECTION PERMITTED.

VFC32KP
EPOXY DUAL-IN-LINE PACKAGE



(TOP VIEW)

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (90% of full scale input or frequency and 0.1% of full scale called zero). Linearity is the true measure of voltage-to-frequency converter's performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. For a given full scale frequency, the linearity error decreases with decreasing operating frequency as shown in Figure 2. Also, best linearity is achieved at lower gains ($\Delta F_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC32 makes the device an excellent choice for use as the front end of A/D converters with 8- to 12-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire serial data transmission).

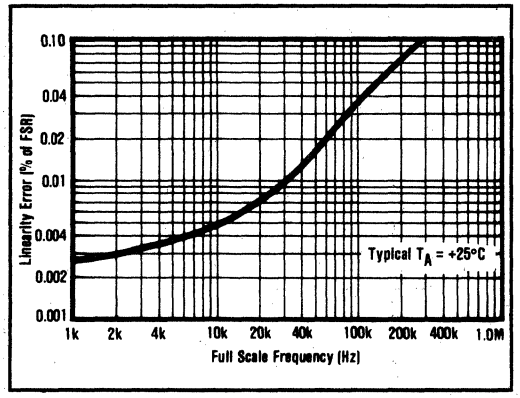


FIGURE 1. Linearity Error vs Full Scale Frequency. (25% Duty Cycle)

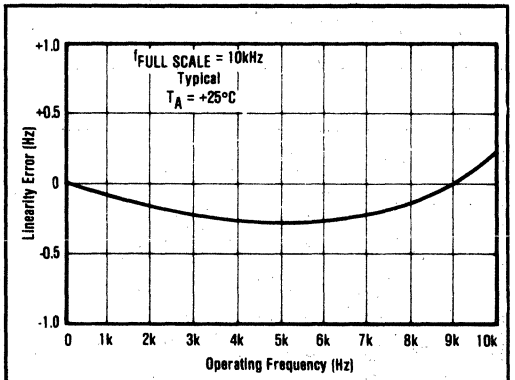


FIGURE 2. Linearity Error vs Operating Frequency. (25% Duty Cycle)

FREQUENCY STABILITY vs TEMPERATURE

The full scale frequency drift of the VFC32 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 100kHz, and this should be taken into account for specific applications. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC32. Above 200kHz, it is recommended all grades be operated below +85°C. Higher duty cycle (up to 50%) and higher output transistor collector current (up to 15mA) will be required. Linearity will, however, be degraded.

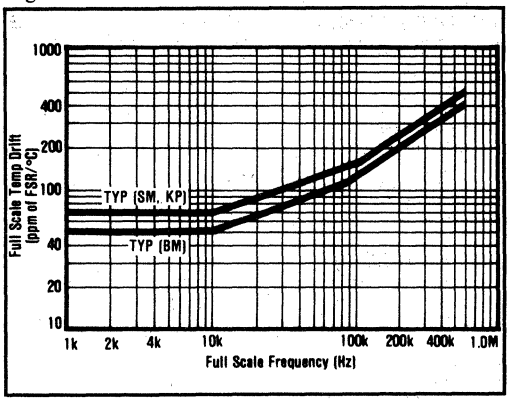


FIGURE 3. Full Scale Drift vs Full Scale Frequency. (25% Duty Cycle)

RESPONSE

Response of the VFC32 to changes in input signal level is specified for a full scale step, and is 1 microsecond plus 1 pulse of the new frequency. For a 10 volt input signal step with the VFC32 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 11 microseconds.

THEORY OF OPERATION

The VFC32 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage in Figure 4.

Essentially, the input amplifier acts as an integrator that produces a 2-part ramp. The first part is a function of the input voltage, and the second part dependent on the current sink. When a positive input voltage is applied at V_{IN}, a constant current will flow through the input resistor, causing the voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time, the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and integrating components. When the ramp reaches a voltage close to zero, the comparator will cause the one-shot to fire. The one-shot period is determined by an internal 7.5V reference and C_1. The f_{OUT} signal will then change logic states, going from a "0" to a "1", and the switch will close, enabling the constant current sink. The ramp voltage will then change direction and begin to ramp up. Since V_{IN}/R_1 is always set up to be less than 1mA, the current in the integrating capacitor will flow toward the summing junction, and the ramp voltage rate of change will be:

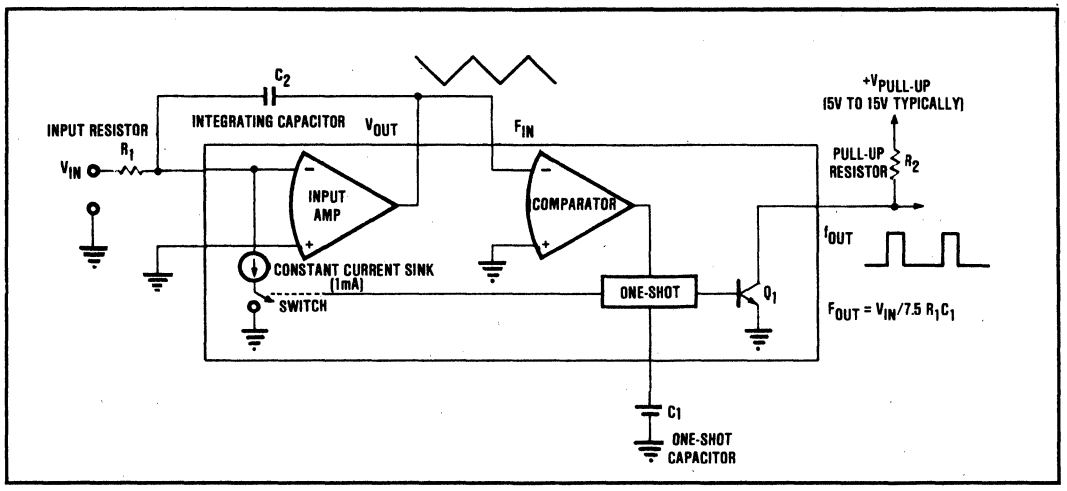


FIGURE 4. Functional Block Diagram of the VFC32.

$$\frac{dV}{dt} = \frac{\frac{V_{IN}}{R_1} - 1mA}{C_2}.$$

Before the ramp voltage can saturate the input amplifier, the one-shot will reset, disabling the current sink, changing the output state back to logic "0", and restarting the cycle. Since the integrating capacitor C_2 affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to V_{IN}/R_1, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

To operate the VFC32 as a highly linear frequency-to-voltage converter, open the connection between V_{OUT} and f_{IN}, and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}, and a positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. For details see Installation and Operating Instructions.

The total VFC period is determined by the following equations, which is shown graphically in Figure 5.

$$f_o = \frac{1}{t}$$

$$t = t_1 + t_2 \text{ and } i = c\, dv/dt$$

$$t = \Delta V_{OUT}\, t_1 \frac{C_2}{V_{IN}/(R_1)} + \Delta V_{OUT}\, t_2 \frac{C_2}{V_{IN}/(R_1) - 1mA}$$

and:

$$-\Delta V_{OUT} t_1 = +\Delta V_{OUT} t_2$$

$$t_2 = C_1 \frac{7.5V}{1mA}$$

The equations reduce to:

$$f_o = \frac{V_{IN}}{7.5(R_1)\, C_1}$$

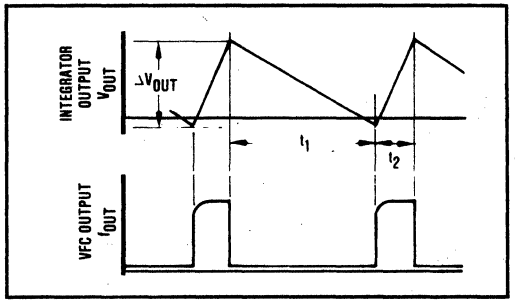


FIGURE 5. Integrator and VFC Output Timing.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). It is measured at the full scale input voltage, which gives the full scale output frequency, F_{FS}.

$$D = \frac{t_2}{t_1 + t_2} = PW \times F_{FS}$$

$$PW = \frac{D}{F_{FS}}$$

Duty cycle is related to the maximum input current and the 1mA (nominal) current sink. By reducing the equations for t_2 and f_0:

$$D = \frac{V_{IN}\ max/(R_1)}{1mA} = \frac{I_{IN}\ max}{1mA}$$

A 25% duty cycle or less is recommended to achieve the best linearity. This corresponds to a maximum input

current of 0.25mA. However, for frequencies above 200kHz a higher duty cycle (up to 50%) will provide more stable high temperature operation at a sacrifice in linearity.

In general, designs with the VFC32 include: (1) Choosing F_{MAX}, (2) Choosing the duty cycle (D = 0.25 typically), (3) Determining the one-shot PW, and (4) Calculating C_1, C_2, R_1, R_2, and R_3.

INSTALLATION AND OPERATING INSTRUCTIONS

The VFC32 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

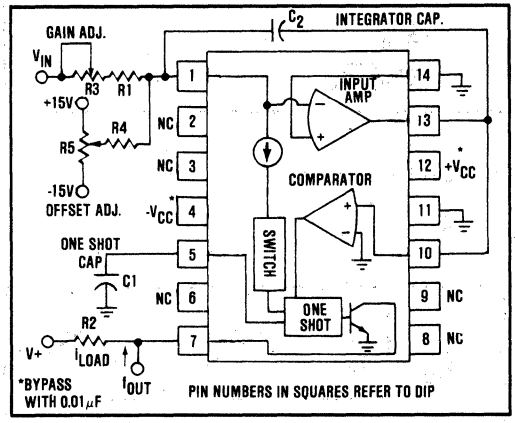


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

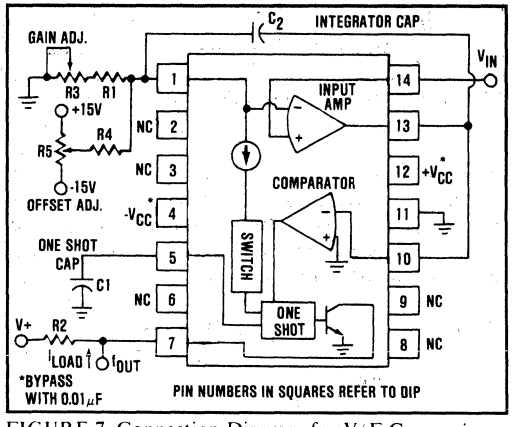


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

Differential inputs are also possible (in Figure 7 lift ground on R_3 and drive R_3 and pin 14 differentially). Note, no CMR will be present.

The full scale frequency and full scale input voltage (current) are established by the selection of values for R1, C2, and C1. Most applications will require a gain adjustment pot (R3), but the offset adjust network (R4, R5) can be omitted if input offset voltages of 1mV to 4mV can be tolerated. R2 is an output pull up resistor and its value depends on the pull up voltage and output drive requirements.

EXTERNAL COMPONENT SELECTION CRITERIA

One-shot Capacitor, C1. This capacitor determines the duration of the output pulse, and is a function of the full scale frequency, according to this equation:

$$C1(pF) = 33 \times 10^6 / f_{MAX} - 30$$

Above 425kHz use 47pF

Select the closest standard value to the capacitance given by the equation. The initial tolerance of this capacitor is not critical since R3 will be adjusted to remove initial gain errors. The temperature drift is critical, since it will add directly to the errors in the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize the parasitic capacitance at this connection to the VFC32 and C1 should be mounted as close as possible. Figure 8 shows pulse width and FS frequency for various values of C1.

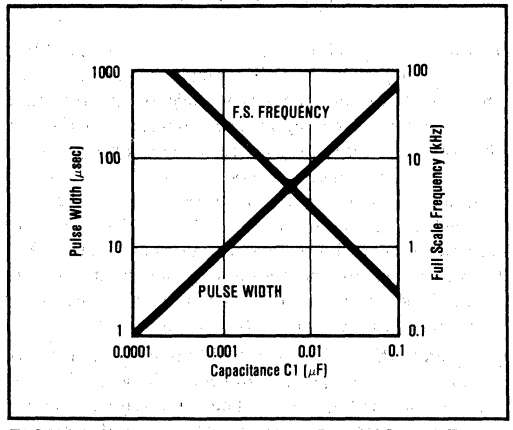


FIGURE 8. Output Pulse Width (D = 0.25) and Full Scale Frequency vs External One-shot Capacitance.

Input Resistor R1 and R3. R1 and R3 determine the magnitude of the current which charges the integrator capacitor. It is a function of the full scale input voltage, according to this equation for 25% duty cycle.

$$R1\ (k\Omega)\ [90\% - \%\ \text{tolerance C1}] \times V_{IN}\ \text{max}/0.25mA$$

R1 is scaled down by [1-(initial C1 tolerance + 0.1)] to allow the addition of a series gain adjusting pot, R3.

$$R_3\ (k\Omega) = V_{IN}\ \text{max}/0.25mA - R_1$$

R1 should have a very low temperature coefficient since this drift adds directly to the errors in the transfer function. If the input signal is a current rather than a voltage, R1 and R3 should be replaced with a short circuit, and the full scale input current should be 0.25mA (25% duty cycle). Removal of gain error then requires adjustment of C1.

Integrating Capacitor C2. C2 is a function of the full scale frequency, according to this equation:

$$C_2(\mu F) = 10^2 / f_{MAX} \text{ below } 100kHz$$
$$0.001\mu F \text{ min above } 100kHz$$

Select the closest standard value to the capacitance given by the equation. The initial tolerance and temperature stability are not critical since these errors do no affect the transfer function. Since the leakage current of the capacitor introduces a gain error, select a capacitor with leakage that is small compared to the full scale input current e.g., 0.25mA. A mylar type is recommended.

Output Pull Up Resistor R2. The open collector output can sink up to 8mA and still be TTL-compatible. Select R2 according to this equation:

$$R_2 \text{ min } (\Omega) = V_{PULL\,UP} / (8mA - i_{LOAD})$$

A 10% carbon composition resistor is suitable for use as R2.

Operation above 200kHz up to 500kHz requires higher duty cycles up to 50% ($I_{IN} = 0.5mA$) and a pull-up resistor that permits 15mA to flow in the output transistor. At this speed, capacitive loading should be minimized to 100pF or less to allow the output voltage time to rise to logic one. Due to the large collector current, the logic zero may rise above +0.4V. This may require an interface circuit such as diode clamp or voltage comparator for coupling to TTL inputs. Note, that linearity will degrade. Also, it is recommended to stay below +85°C at high frequencies.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC32 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses -0.6V. Choose C3 for appropriate value of t (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero, to insure that the input signal at pin 10 crosses the -0.6V threshold. Errors are nulled following the procedure given on this page, using 0.001X full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC32 is 0.015% of FSR/% max. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Current in the f_{OUT} pin (logic sink current) flows in the common connection (pin 11 of DIP package). It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by logic current flowing through any ground return impedance.

Trimming Components R3, R4, R5.

R5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R4 can be a 20% carbon composition resistor with a value of 10MΩ.

R3 nulls the gain errors of the converter and compensates for initial tolerances of R1 and C1. Its total resistance should be at least 20% of R1, if R1 is selected 10% low (see R1 equation). Its temperature coefficient should be no greater than five times that of R1, to maintain a low drift of the R3 - R1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 X full scale.
2. Adjust R5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

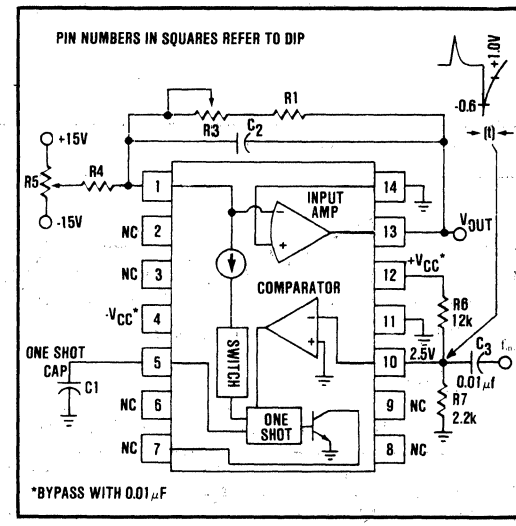


FIGURE 9. Connection Diagram for F/V Conversion.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1

$$C_1 = 33 \times 10^6 / f_{MAX} - 30$$
$$= 33 \times 10^6 / 100kHz - 30$$
$$= 300pF$$

Choose a 300pF NPO ceramic capacitor with ±1% tolerance.

Selecting R_1 and R_3 (for D = 0.25; for D = 0.5 use 0.5mA)

$$R_1 = [90\% - \% \text{ tolerance of } C_1] \times V_{IN} \text{ max} / 0.25mA$$
$$= [0.9 - 0.1] \times 10V / 0.25mA$$
$$= 32k\Omega$$

Choose a 32.4kΩ metal film resistor with ±1% tolerance.

$R_3 = 10V / 0.25mA - R_1$

$= 8k\Omega$

Choose a 10kΩ cermet potentiometer

Selecting C_2

$C_2 = 10^2 / F_{MAX}$

$= 10^2 / 100kHz$

$= 0.001\mu F$

Choose a 0.001μF mylar capacitor with ±5% tolerance.

Selecting R_2

$R_2 = V_{PULLUP} / (8mA - i_{LOAD})$

$= 5V / (8mA - 1.6mA)$, one TTL-load = 1.6mA

$= 781\Omega$

Choose a 750Ω 1/4-watt carbon composition resistor with ±5% tolerance.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC32 ideal for a variety of VFC applications. High accuracy allows the VFC32 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 12-bits.

Figures 10 - 14 show typical applications of the VFC32.

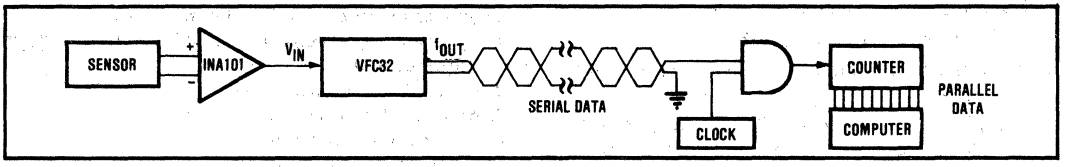


FIGURE 10. Inexpensive A/D with Serial Transmission of Digital Data.

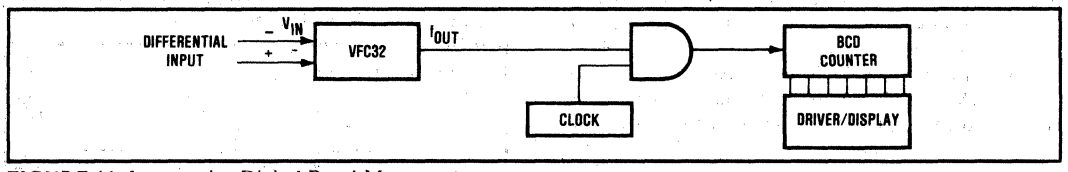


FIGURE 11. Inexpensive Digital Panel Meter.

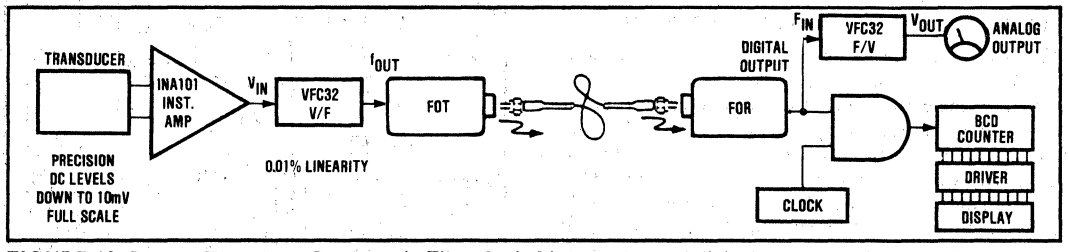


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

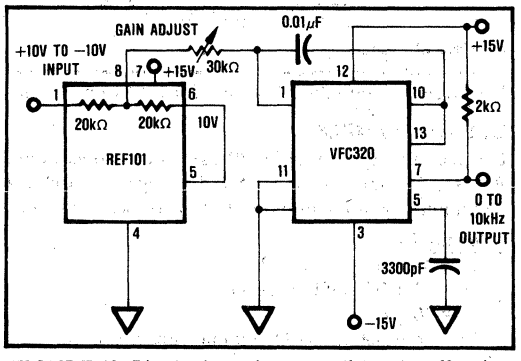


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

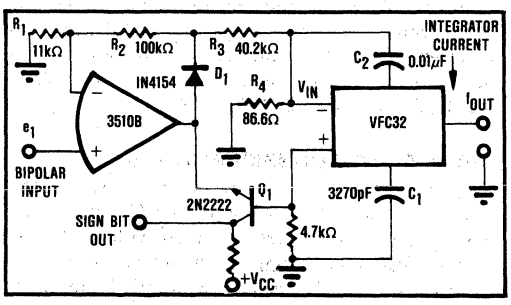


FIGURE 14. Absolute value circuit with the VFC32. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.

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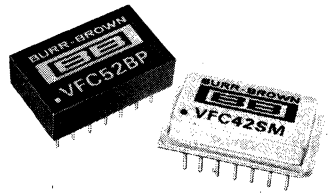


VFC42
VFC52

VOLTAGE-TO-FREQUENCY AND FREQUENCY-TO-VOLTAGE CONVERTER

FEATURES

- V/F OR F/V CONVERSION
- TWO FREQUENCY RANGES
  10kHz (VFC42)
  100kHz (VFC52)
- LOW NONLINEARITY
  ±0.01% max (VFC42)
  ±0.05% max (VFC52)
- MINIMAL EXTERNAL COMPONENTS REQUIRED
  Add only one external resistor for V/F operation
- 6 DECADE DYNAMIC RANGE
- OUTPUT DTL/TTL/CMOS COMPATIBLE

DESCRIPTION

VFC42 and VFC52 are hybrid microcircuits which can be connected as voltage-to-frequency or frequency-to-voltage converters. They provide a simple, low cost method of converting analog signals into an equivalent digital form. The digital output is an open collector which can be made compatible with DTL, TTL, or CMOS logic. The output is a train of constant-amplitude, constant-width pulses whose repetition rate is proportional to the amplitude of the analog input voltage. In the frequency-to-voltage mode the pulses become the input and the proportional DC voltage, the output.

Both models are offered in epoxy (−25°C to +85°C) and hermetic metal (−25°C to +85°C and −55°C to +125°C) 14-pin DIP packages.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

THEORY OF OPERATION

VFC42 and VFC52 hybrid voltage-to-frequency converters provide a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. To understand the circuit's operation see Figure 1.

The input amplifier is connected in an integrator configuration. When a positive input voltage is applied at V_{IN}, a constant current flows through the input resistor causing voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_2$. During this time the constant current sink is disabled by the switch. When the ramp reaches zero volts, the comparator causes the one-shot to fire. The f_{out} signal then changes states, going from logic 0 to logic 1 and the switch closes, enabling the constant current sink. Ramp voltage then changes direction and begins to ramp up. Since V_{IN}/R_1 is always set to be less than 1mA, current in the integrating capacitor flows toward the summing junction and ramp voltage range of change will be

$$\frac{dV}{dt} = \frac{\left(\frac{V_{in}}{R_1}\right) - 1mA}{C_2}$$

Before the ramp voltage can saturate the input amplifier, the one-shot resets, disabling the current sink, changing the output state back to logic 0 and restarting the cycle.

To operate VFC42 and VFC52 as highly linear frequency-to-voltage converters, open the connection between V_{OUT} and F_{IN} and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}. A positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. An external capacitor connected between pins 13 and 14 (paralleling C2) should be added to reduce output ripple. Refer to Operating Instructions for detailed information on F/V operation.

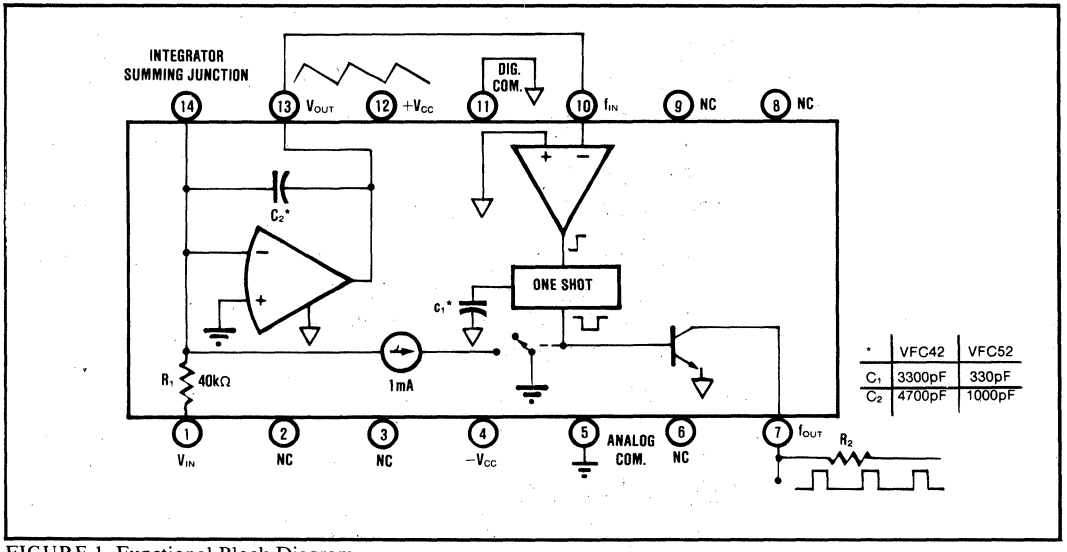


FIGURE 1. Functional Block Diagram.

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity, the maximum deviation of the actual transfer function from a straight line drawn between the end points (full scale input and zero input), is the true measure of a FVC's performance and is a function of full scale frequency. The high linearity of VFC42 and VFC52 makes these devices an excellent choice for use in A/D converters with 10 (0.05%) and 12 bit (0.012%) accuracy and for highly accurate analog data transfer over long lines in noisy environments.

FREQUENCY STABILITY VS TEMPERATURE

Frequency stability vs temperature is expressed as parts per million of full scale range per °C. Since frequency drift is a function of the specified temperature range, the "SM" models will meet the lower drift specifications of the "BM" models over the narrower −25°C to +85°C temperature range. Error sources do not drift linearly over temperature, consequently the units drift much less at higher temperatures.

RESPONSE TIME

Response time of VFC42 and VFC52 to input signal level changes is specified for a full scale step and is 1μsec plus 1 period of the new frequency. Typical settling time to within rated linearity for a positive input voltage step of +10V is 101μsec for VFC42 and 11μsec for VFC52.

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, and ±15VDC power supplies unless otherwise noted.

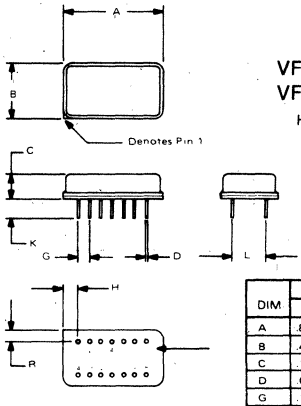
MODEL	VFC42			VFC52			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Full Scale Frequency		10			100		kHz
INPUT							
Analog Input (V/F)							
Voltage Range	0		10	0		+10	V
Current Range	0		+0.25	0		+0.25	mA
Input Bias Current (pin 14) Inverting Input		6	8		6	8	nA
Input Offset Voltage (trimmable to zero)		100	200		100	200	µV
Input Impedance (pin 1)	32	40	48	32	40	48	kΩ
Frequency Input (F/V) (pin 10)							
Logic Levels: Logic "0"	$-V_{CC}$		−0.6	$-V_{CC}$		−0.6	V
Logic "1"	+1.0		$+V_{CC}$	+1.0		$+V_{CC}$	V
Pulse Width Range (t_2, Fig. 2)	0.1		15	0.1		1.5	µsec
Impedance	1 ‖ 10	1.2 ‖ 10		1 ‖ 10	1.2 ‖ 10		MΩ ‖ pF
TRANSFER CHARACTERISTICS							
Transfer Functions	$f_{OUT} = V_{IN}(1.00 \times 10^3)$ $V_{OUT} = f_{IN}(10 \times 10^{-4})$			$f_{OUT} = V_{IN}(1.00 \times 10^4)$ $V_{OUT} = f_{IN}(10 \times 10^{-5})$			Hz VDC
Accuracy							
Full Scale Gain (adjustable to zero)		0.1	0.2		0.1	0.2	%
Linearity Error: 0.01Hz ≤ F ≤ 10kHz		0.005	0.01				% of FSR[1]
0.1Hz ≤ F ≤ 100kHz					0.025	0.05	% of FSR
Offset Error (pin 1)		0.001	0.002		0.001	0.002	% of FSR
Power Supply Sensitivity[2]			0.015			0.015	% of FSR/%
Temperature Stability							
Analog Input							
Full Scale Drift (gain and offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Offset Drift							
Grade: BP		±1	±3		±1	±3	ppm of FSR/°C
BM		±1	±3		±1	±3	ppm of FSR/°C
SM		±1	±3		±1	±3	ppm of FSR/°C
Frequency Input							
Full Scale Drift (gain and offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Dynamic Response							
Settling Time to within linearity specification for full scale input step	1 period of new frequency + 1µsec			1 period of new frequency + 1µsec			
Overload Recovery Time	1 period of new frequency + 1µsec			1 period of new frequency + 1µsec			
OUTPUT							
Voltage Output							
Voltage Range ($I_O \leq$ 5mA)	0 to +10			0 to +10			V
Output Current ($V_O \geq$ 7V)	+10			+10			mA
Output Impedance (closed loop)			1			1	Ω
Capacitive Load			100			100	pF
Frequency Output (open collector)							
Pulse Characteristics: Logic "1"			$+V_{PULL-UP}$			$+V_{PULL-UP}$	V
Logic "0" (at $I_O \leq$ −8mA)	0		+0.4	0		+0.4	V
Pulse Width	20	25		2.0	2.5		µsec
Output Sink Current (Logic "0", ≤ 0.4V)			8			8	mA
Output Leakage Current (Logic "1")			1			1	µA
Fall Time (I_{OUT} = −5mA, C_{LOAD} = 500pF)			400			400	nsec
POWER SUPPLY REQUIREMENTS							
Rated Supplies		±15			±15		V
Supply Range	±9		±20	±9		±20	V
Supply Drain (independent of operating frequency)		±5.5	±6.5		±5.5	±6.5	mA
TEMPERATURE RANGE							
Specification: BP, BM	−25		+85	−25		+85	°C
SM	−55		+125	−55		+125	°C
Operating: BM, SM	−55		+125	−55		+125	°C
BP	−25		+85	−25		+85	°C
Storage: BM, SM	−55		+125	−55		+125	°C
BP	−25		+85	−25		+85	°C

NOTES: 1) % of FSR = % of Full Scale Range. 2) Rated at full scale input and ±15V supplies. 3) Hot = +20°C to highest rated temperature; cold = lowest rated temperature to +20°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±22V
Output Sink Current (F_{output})	50mA
Output Current (V_{output})	+20mA
Input Voltage, Pin 14	±Supply
Input Voltage, Pin 1	±Supply
Storage Temperature Range	
Grade: BM, SM	−55°C to +125°C
BP	−25°C to +85°C

MECHANICAL



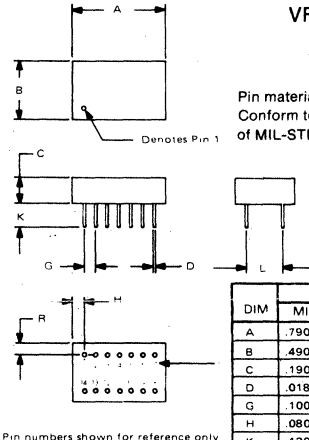
Pin numbers shown for reference only
Numbers are not marked on package

VFC42BM, VFC42SM
VFC52BM, VFC52SM

Hermetic Metal Package
14-Pin DIP

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Tolerance (inches): .xxx ±0.005; .xx ±0.02
Connector: 14-pin DIP (145MC)
Case Material: Base - gold plated kovar, Cap - nickel-plated kovar or steel
Pin material and plating compositions: Conforms to MIL-STD-883, Method 2003 (solderability) except paragraph 3.2 (aging).
Hermeticity: Conforms to MIL-STD-883, Method 1014, Condition C, Step 1, Fluorocarbon (gross leak).



Pin numbers shown for reference only
Numbers are not marked on package.

VFC42BP, VFC52BP

Epoxy Package
14-Pin DIP

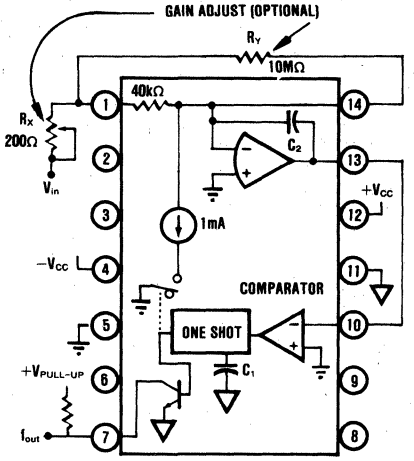
Pin material and plating composition:
Conform to Method 2003 (solderability)
of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

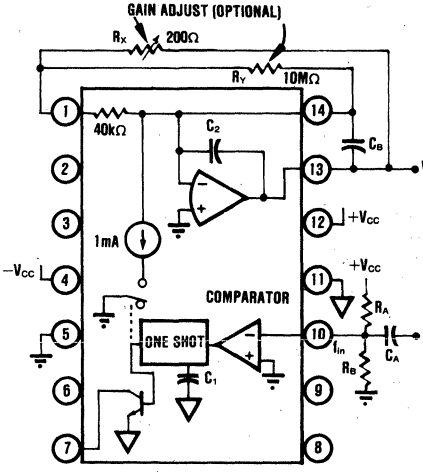
Tolerance (inches): .xxx ±0.005
.xx ±0.02
Connector: 14-pin DIP (145MC)
Case Material: Epoxy

CONNECTION DIAGRAMS

V/F Operation



F/V Operation



OPERATING INSTRUCTIONS

VFC42 and VFC52 can be connected for either V/F or F/V operation. Only one external component, the output pull-up resistor, is required for V/F operation. F/V operation requires the pull-up resistor and input biasing components. Gain error is the most significant error in either configuration and may be nulled out with the optional trim circuit (R_X and R_Y). The offset error is laser trimmed at the factory and no external adjustment is required.

Power Supply Consideration: Power supplies stable to within ±1% are recommended to maintain conversion accuracy. Each supply should be bypassed with 0.01μF capacitors located as close to the VFC as possible.

VOLTAGE-TO-FREQUENCY OPERATION

Calculating the Value of Pull-Up Resistor, R_P: The open collector output can be used to drive DTL, TTL, CMOS or discrete circuits. The maximum collector current allowed for TTL circuits in logic 0 is 8mA. R_P may be calculated by this equation:

$$R_P \text{ min} = V \text{ pull-up}/(8mA - i_{LOAD}).$$

A 10% carbon composition resistor is suitable for this purpose. The collector current may be as great as 30mA if a logic 0 voltage of 1.0V is tolerable.

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Connection Diagram. Apply positive full scale voltage to the input and adjust R_X until 10kHz ±1Hz (VFC42) or 100kHz ±10Hz (VFC52) is obtained at f_{OUT}. R_X and R_Y should have temperature coefficients of <500ppm. These external components will add less than 5ppm/°C to temperature drift.

FREQUENCY-TO-VOLTAGE OPERATION

Input Characteristics: VFC42 and VFC52 can be connected as frequency-to-voltage converters as shown in Connection Diagram. f_{IN} should be a positive pulse train with minimum pulse width of 1.0μsec and rise and fall times of ≤ 300nsec. The input train (f_{IN}) is differential and applied to the input of the comparator (pin 10) (see Figure 2). Threshold voltage of the comparator lies between −0.6 and +1.0V. When comparator input is less than −0.6V it triggers the one-shot.

Selecting R_A, R_B, and C_A Input components R_A, R_B and C_A are selected so that the trigger voltage (V_T) is more negative than −0.6V and transition time (t_2) is between 0.3μsec and 15μsec for VFC42 and between 0.3μsec and 1.5μsec for VFC52. Table I give values for input components for several common signal sources. Values for R_A, R_B and C_A may be selected by the user when input signal characteristics differ from those listed. Conditions described above for trigger voltage and transition time must be observed.

TABLE I. F/V Input Component Selection

Input Type	V_{INPUT} (V)		V_{BIAS} (V)	VFC42			VFC52		
	Low	High		R_A (kΩ)	R_B (kΩ)	C_A (pF)	R_A (kΩ)	R_B (Ω)	C_A (pF)
TTL	≤+0.4	≥+2.8	+1.1	12	1.0	1000	8.2	680	680
5V CMOS	≤+0.5	≥+4.5	+1.2	18	1.6	2200	9.1	820	680
10V CMOS	≤+1.0	≥+9.0	+1.1	12	1.0	2200	6.2	510	680
15V CMOS	≤+1.5	≥+13.5	+1.1	12	1.0	2200	6.2	510	680

Equations to calculate trigger voltage and transition time are:

$$V_T = V_B + V_{in}(e^{-t_1/\tau} - 1)$$

$$t_2 = -\tau \ln\left[\frac{1 - V_B}{V_{in}(e^{-t_1/\tau} - 1)}\right]$$

V_B = Bias voltage on pin 10

V_{in} = Input pulse amplitude

t_1 = Input pulse width

τ = Time constant of R_A, R_B C_A as connected

If input pulse amplitude is greater than $+V_{CC} - 1V$, a voltage larger than $+V_{CC}$ will be applied to pin 10. Since this may damage the unit, a diode connected across R_A with the cathode tied to $+V_{CC}$ is required.

Output Characteristics: Selecting C_B: Output ripple voltage amplitude is inversely proportional to the input frequency and to the value of the integrating capacitance, $C_2 + C_B$. Conversely, time required for the output to settle is directly proportional to the value of $C_2 + C_B$ and is least with small values of $C_2 + C_B$. There is, therefore, a trade-off between output ripple amplitude and output settling time.

Because ripple amplitude is greatest at lowest input frequency it is at this point where the trade-off will usually be made. Ripple voltage and integrating capacitance value are related in this manner:

$$C_B = \frac{-(25 \times 10^{-6})t_{sec}}{\ln\left[1 - \frac{V_{Ripple}}{30V}\right]} \text{ farads}$$

where t is equal to 25μsec in the VFC42 and 2.5μsec in the VFC52 and C is the integrating capacitance.

Calculating output response time versus integrating capacitance is an iterative process and is plotted in Figure 3. These curves are for zero to full scale input frequency transitions. If faster response time with lower ripple voltage is desired, a low-pass filter can be connected in series with the output.

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Connection Diagram. Apply full scale frequency to the input and adjust R_X until the full scale voltage is +10V ±1mV (discounting ripple). R_X and R_Y should have temperature coefficients of < 500ppm. These external components will add less than 5ppm/°C to temperature drift.

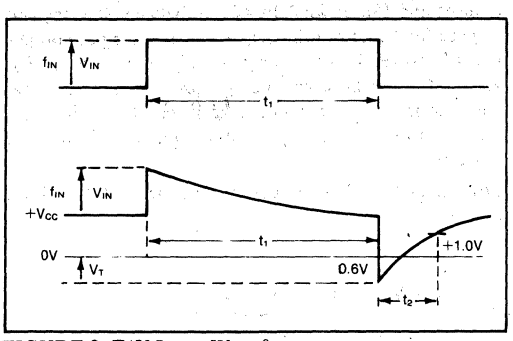


FIGURE 2. F/V Input Waveforms.

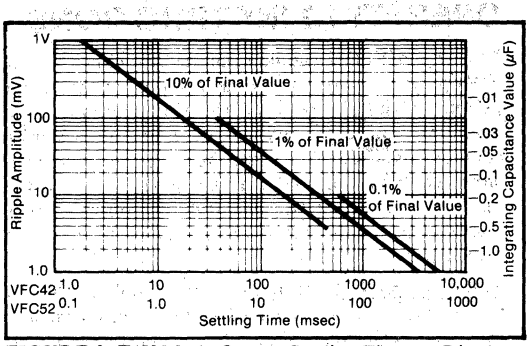


FIGURE 3. F/V Mode Output Settling Time vs. Ripple Voltage Amplitude for Full Scale Frequency Change.

APPLICATION

VFC42 and VFC52 can be used to convert analog data into a digital pulse train for transmission over long lines through high EMI environments. Illustrated in Figure 4 is a V/F, F/V combination that can be used to transmit analog data of 0 to +10V over a 100Ω shielded, twisted-pair. The voltage ripple amplitude at the output will be 10mV for a 10V output and the settling time for a full scale 0 to +10V change is 60 milliseconds.

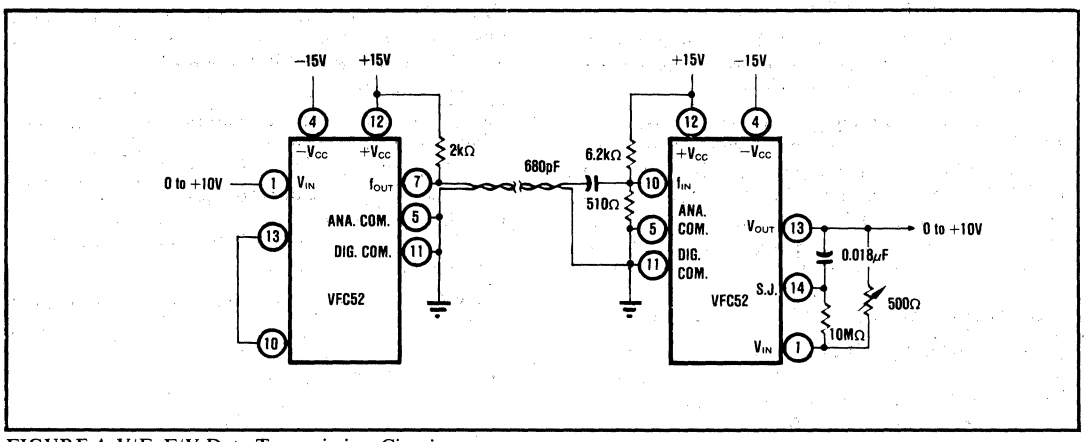
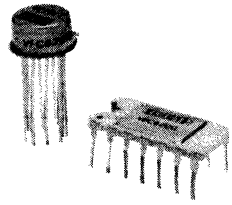


FIGURE 4. V/F, F/V Data Transmission Circuit.

BURR-BROWN®



VFC62

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY, 12 to 14 bits
  - ±0.005% max at 10kHz FS
  - ±0.03% max at 100kHz FS
  - ±0.1% typ at 1MHz FS
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT DTL/TTL/CMOS COMPATIBLE
- ACTIVE PULL-UP OUTPUT

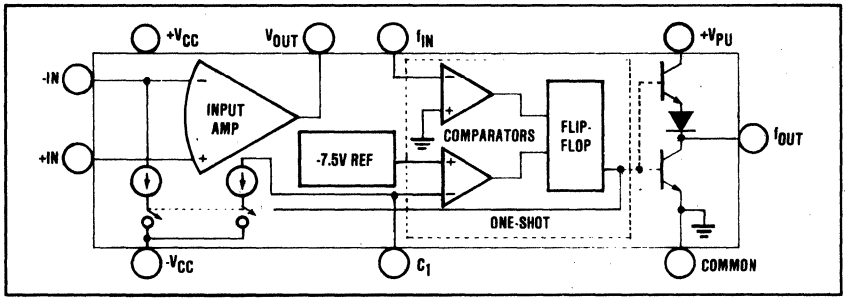
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- 2-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC62 monolithic voltage-to-frequency and frequency-to voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. In the noise-immune digital form the analog signal may be transmitted long distances without degradation. It may be converted to a binary number with a counter or microprocessor or may be returned to analog form using a frequency-to-voltage converter.

The digital output is an active pull-up type which provides better load driving capability than the usual open collector outputs. Output pulses are DTL, TTL and CMOS compatible. High accuracy (±0.005% max nonlinearity at 10kHz) is achieved with relatively few external components. Only one resistor and two capacitors are required.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC62BG/BM/SM MIN	VFC62BG/BM/SM TYP	VFC62BG/BM/SM MAX	VFC62CG/CM MIN	VFC62CG/CM TYP	VFC62CG/CM MAX	UNITS
V/F CONVERTER $f_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig. 4 with $e_2 = 0$	> 0		Note 2	*		*	V
	Fig. 4 with $e_1 = 0$	< 0		-10	*		*	V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage(3)				±0.15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 || 5	650 || 5		*	*		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		*	*		kΩ || pF
ACCURACY								
Linearity Error(1)(4)(5)	Fig. 4 with e_2 + = 0(6)							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% of FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.03		*	*	% of FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% of FSR
Offset Error	Input Offset Voltage(3)			±15			*	ppm of FSR
Offset Drift(7)			±0.5			*		ppm of FSR/°C
Gain Error(3)			±5	±10		*	*	% of FSR
Gain Drift(7)	f = 10kHz			50			20	ppm of FSR/°C
Full Scale Drift (offset drift & gain drift(7)(8)(9))	f = 10kHz			50			20	ppm of FSR/°C
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			*	% of FSR/%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		Note 10			*		
Overload Recovery	< 50% overload		Note 10			*		
ACTIVE PULL-UP OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Voltage, Logic "1"		V_{PU} - 2.6		V_{PU}	*		*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100			*		nsec
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 || 10	150 || 10		*	*		kΩ || pF
Logic "1"		+1.0		+V_{CC}	*		*	V
Logic "0"		-V_{CC}		-0.05	*		*	V
Pulse-width Range		0.25			*			µsec
OUTPUT FROM OP AMP								
Voltage	I_O = 7mA	0 to +10			*			V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-loop			0.1			*	Ω
Capacitive Load	Without oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range, V_{CC}		±13		±20	*		*	V
Pull-up Voltage		+3.5		+V_{CC}	*		*	V
Quiescent Current	not including load current		±6	±6.7		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Operating								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Storage		-65		+150	-65		+150	°C

*Specification the same as for VFC62BG/BM/SM.

NOTES:
1. A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity.
2. Determined by R_{IN} and full scale current range constraints.
3. Adjustable to zero. See Offset and Gain Adjustment section.
4. Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section.
5. When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy.
6. For $e_1 = 0$ typical linearity errors are 0.01% at 10kHz, 0.2% at 100kHz.
7. Exclusive of external components drift.
8. FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).
9. Positive drift is defined to be increasing frequency with increasing temperature.
10. One pulse of new frequency plus 50nsec typical.

ABSOLUTE MAXIMUM RATINGS

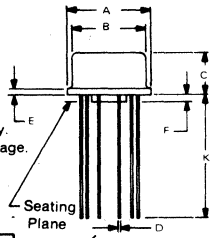
Supply Voltages	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, -Input	±V_{CC}
Input Voltage, +Input	±V_{CC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

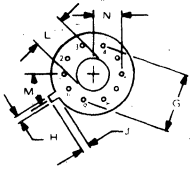
MECHANICAL

VFC62BM, CM/SM
TO-100 PACKAGE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

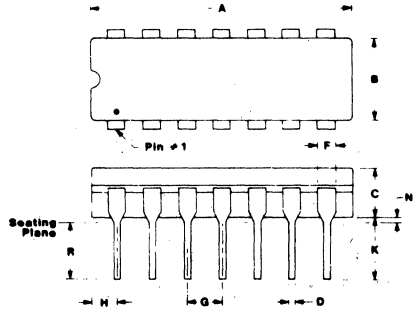


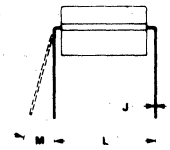


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
	.335	.370	8.51	9.40
	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	- -	12.70	
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

VFC62BG/CG
CERAMIC DUAL-IN-LINE

NOTES: 1. Leads in true position within 0.01" (0.25mm) R at seating plane.

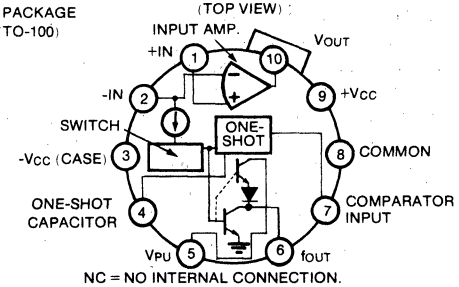




DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.753	.787	19.13	19.48
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.085	—	2.16
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	0.3 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

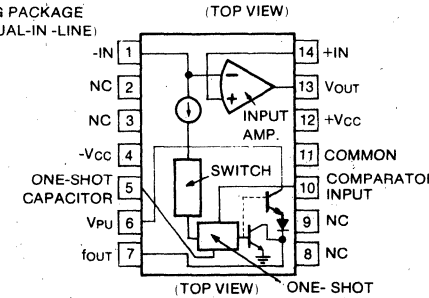
PIN CONFIGURATIONS

M PACKAGE
(TO-100)



NC = NO INTERNAL CONNECTION.
EXTERNAL CONNECTION PERMITTED.

G PACKAGE
(DUAL-IN-LINE)



DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero). Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC62 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission).

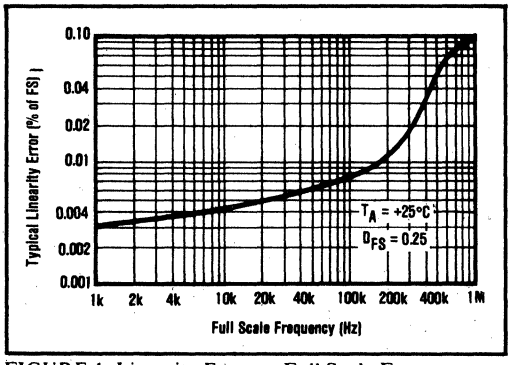


FIGURE 1. Linearity Error vs Full Scale Frequency.

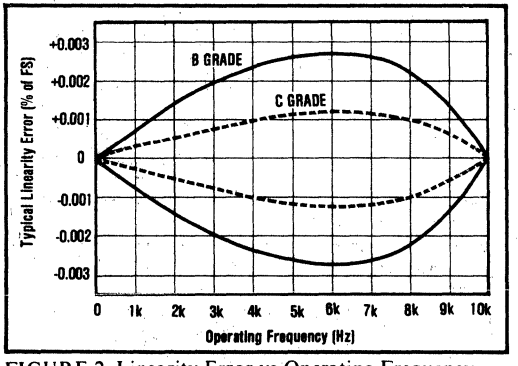


FIGURE 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC62 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC62.

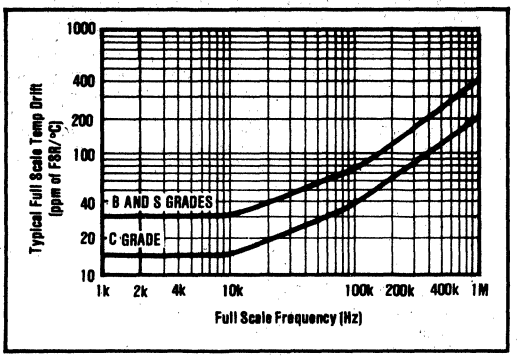


FIGURE 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC62 to changes in input signal level is specified for a full scale step, and is 50nsec plus 1 pulse of the new frequency. For a 10V input signal step with the VFC62 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10μsec.

THEORY OF OPERATION

The VFC62 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a one-shot), two switched current sinks, and an active pull-up output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = -7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this -7.5V threshold comparator B resets the flip-flop, and the ramp voltage begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC62 is derived as follows

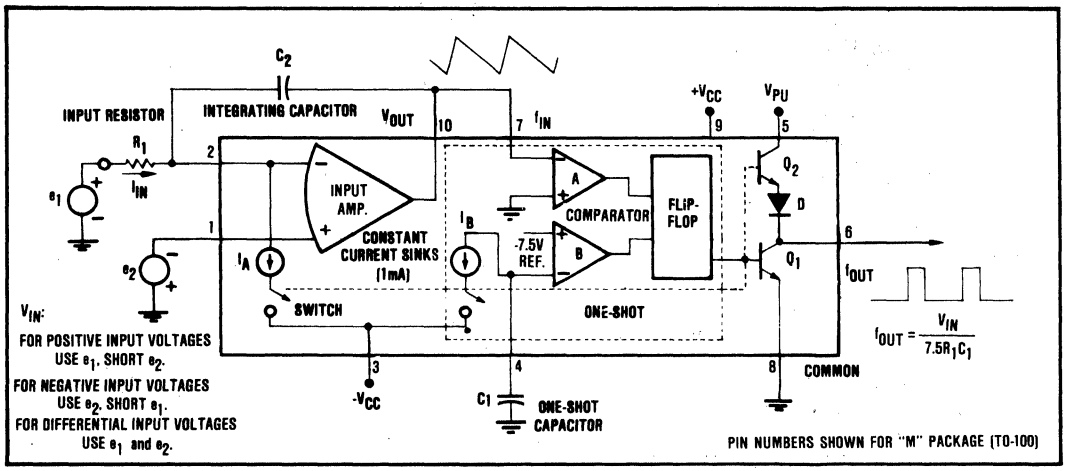


FIGURE 4. Functional Block Diagram of the VFC62.

for the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$

In the time $t_1 + t_2$, the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN}\, t_1 + (I_{IN} - I_A)\, t_2 \quad (2)$$

$$\text{So that } I_{IN}\,(t_1 + t_2) = I_A\, t_2 \quad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A R_1 t_2} \quad (6)$$

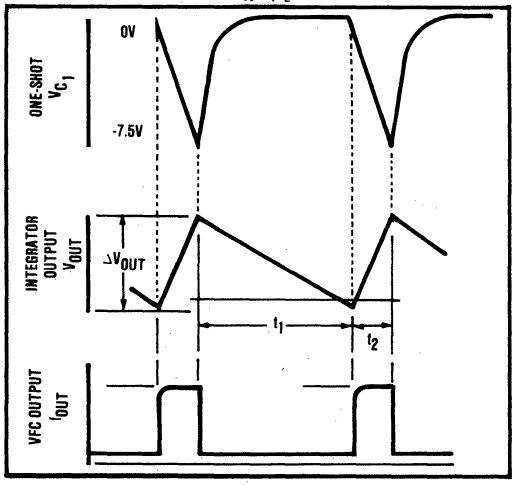


FIGURE 5. Integrator and VFC Output Timing.

In the time t_2, I_B charges the one-shot capacitor C_1 until its voltage reaches -7.5V and trips comparator B.

$$\text{Thus } t_2 = \frac{C_1\, 7.5}{I_B} \quad (7)$$

$$\text{Using (7) in (6) yields } f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$$

$$\text{Since } I_A = I_B \text{ the result is}$$

$$f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \quad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC62 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC62, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user-determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\ max\ /\ R_1}{1mA} = \frac{I_{IN}\ max}{1mA}$$

Thus $D_{FS} = 0.25$ corresponds to $I_{IN}\ max = 0.25mA$.

determine a range of acceptable values.

$$C_2\ (\mu F) = \begin{cases} \frac{100}{f_{FS}}\ ;\ \text{if } f_{FS} \leq 100kHz \\ 0.001;\ \text{if } 100kHz < f_{FS} \leq 500kHz \\ 0.0005;\ \text{if } f_{FS} > 500kHz \end{cases} \quad (13)$$

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for intitial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1, to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 x full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC62 is 0.015% of FSR/% maximum. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the f_{OUT} pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 ($D_{FS} = 0.25$)

$C_1 = [(33 \times 10^6)/f_{MAX}] - 15$ $\quad [(66 \times 10^6)/f_{MAX}] - 15$ if $D_{FS} = 0.5$

$= [(33 \times 10^6)/100kHz] - 15$

$= 315pF$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 ($D_{FS} = 0.25$)

$R_1 + R_3 = V_{IN}\ max/0.25mA$ $\quad V_{IN}\ max/0.5mA$ if $D_{FS} = 0.5$

$= 10V/0.25mA$

$= 40k\Omega$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$C_2 = 10^2/F_{max}$

$= 10^2/100kHz$

$= 0.001\mu F$

Choose a 0.001μF capacitor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC62 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1T (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold. Errors are nulled following the procedure given on this page, using 0.001 x full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

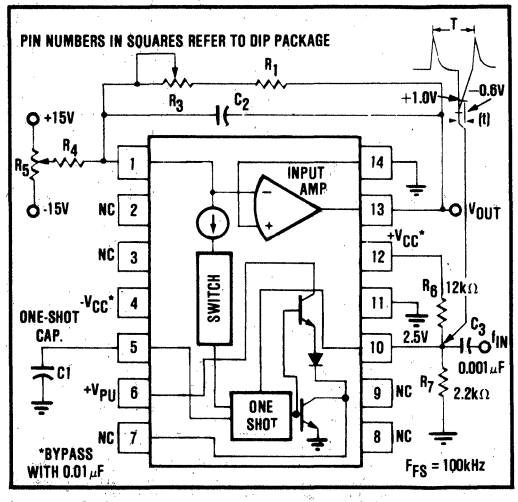


FIGURE 9. Connection Diagram for F/V Conversion.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC62 ideal for a variety of VFC applications. High accuracy allows the VFC62 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits.

Figures 10 - 14 show typical applications of the VFC62.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VFC62 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

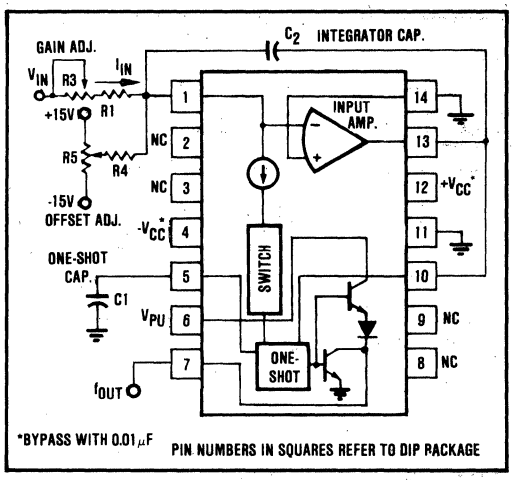


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

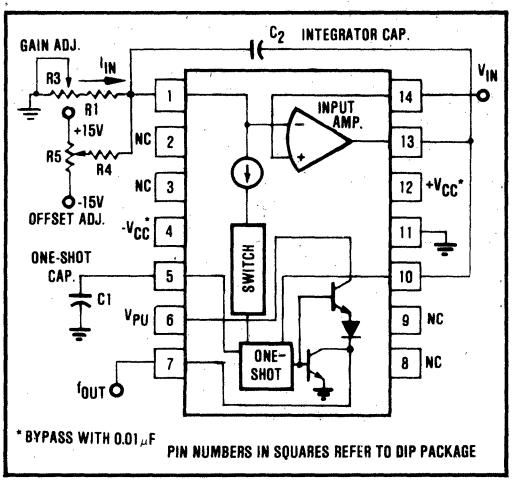


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, and (5) selecting the integrator capacitor C_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected. The nominal value of R_1 is

$$R_1 = \frac{V_{IN}\ max}{0.25mA} \qquad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\ nom} = \frac{V_{IN}}{7.5\ R_1\ f_{OUT}} \qquad (11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1\ (pF) = \frac{33 \times 10^6}{f_{FS}} - 15 \qquad (12)$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC62 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at $D_{FS} = 25\%$.

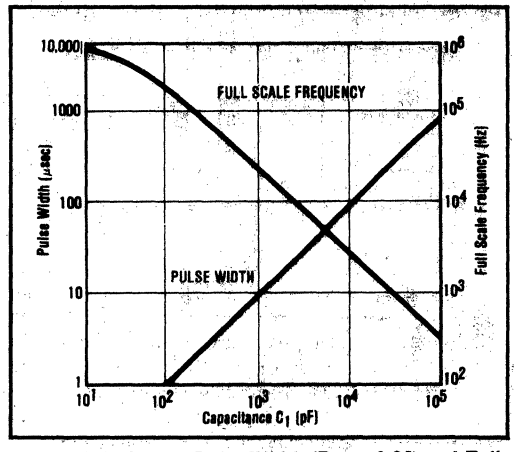


FIGURE 8. Output Pulse Width ($D_{FS} = 0.25$) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator

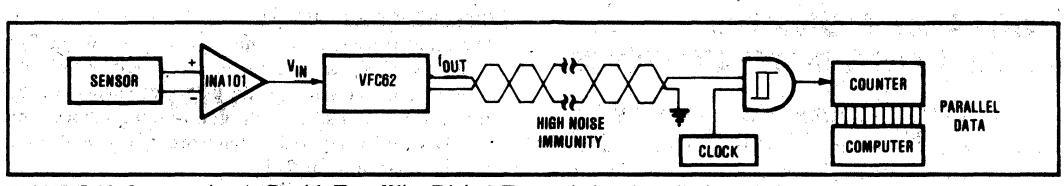


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

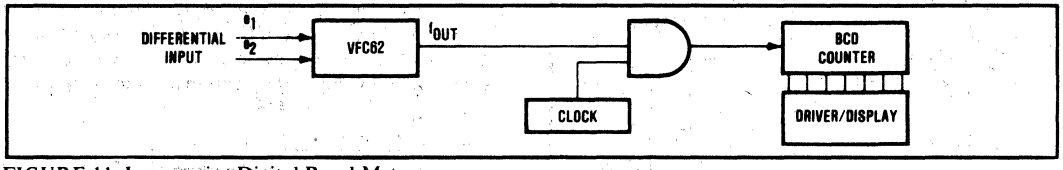


FIGURE 11. Inexpensive Digital Panel Meter.

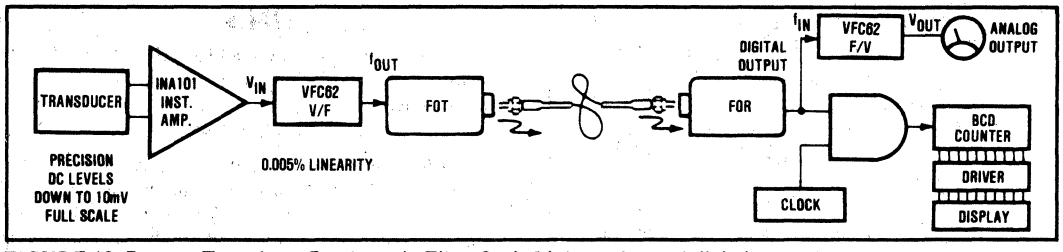


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

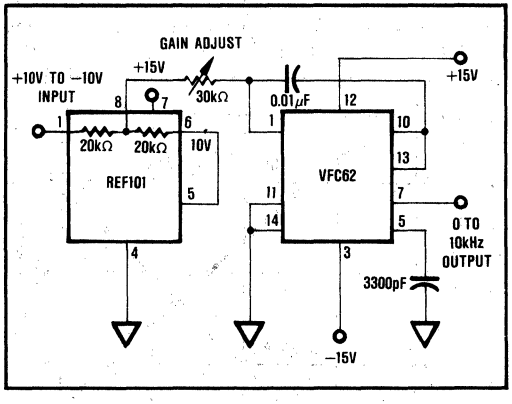


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

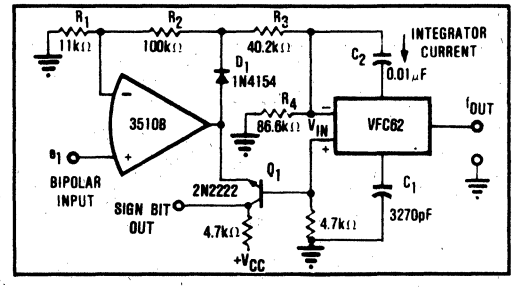


FIGURE 14. Absolute value circuit with the VFC62. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.

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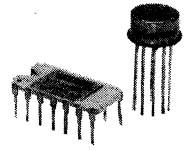


VFC320

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY, 12 to 14 bits
  - ±0.005% max at 10kHz FS
  - ±0.03% max at 100kHz FS
  - ±0.1% typ at 1MHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT DTL/TTL/CMOS COMPATIBLE

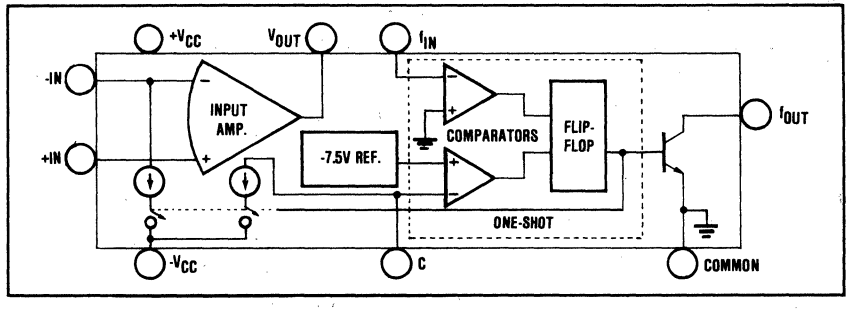
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC320 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved with relatively few external components. Two external resistors and two external capacitors are required to operate. Full scale frequency and input voltage are determined by a resistor in series with -IN and two capacitors (one-shot timing and input amplifier integration). The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$). The VFC320 is available in three performance/temperature grades and two package configurations. The TO-100 versions are hermetically sealed, and specified for the -25°C to +85°C and -55°C to +125°C ranges, and the dual-in-line units are specified from -25°C to +85°C.



SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC320BG/BM/SM MIN	VFC320BG/BM/SM TYP	VFC320BG/BM/SM MAX	VFC320CG/CM MIN	VFC320CG/CM TYP	VFC320CG/CM MAX	UNITS
V/F CONVERTER $F_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig. 4 with $e_2 = 0$	> 0		Note 2				V
	Fig. 4 with $e_1 = 0$	< 0		-10				V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage(3)				±0.15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 || 5	650 || 5		*	*		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		*	*		kΩ || pF
ACCURACY								
Linearity Error(1)(4)(5)	Fig. 4 with $e_2 = 0$(6)							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% of FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.030		*	*	% of FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% of FSR
Offset Error Input Offset Voltage(3)				±15			*	ppm of FSR
Offset Drift(7)			±0.5			*		ppm of FSR/°C
Gain Error(3)			±5	±10		*	*	% of FSR
Gain Drift(7)	f = 10kHz			50			20	ppm of FSR/°C
Full Scale Drift (offset drift & gain drift)(7)(8)(9)	f = 10kHz			50			20	ppm of FSR/°C
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			*	% of FSR/%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		Note 10			*		
Overload Recovery	< 50% overload		Note 10			*		
OPEN COLLECTOR OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*	µA
Voltage, Logic "1"	External pull-up resistor required (see Figure 4)			V_{PU}			*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100	*		*		nsec
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 || 10	150 || 10		*	*		kΩ || pF
Logic "1"		+1.0		+V_{CC}	*		*	V
Logic "0"		-V_{CC}		-0.05	*		*	V
Pulse-width Range		0.25			*			µsec
OUTPUT FROM OP AMP								
Voltage	I_O = 7mA	0 to +10			*			V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-loop			0.1			*	Ω
Capacitive Load	Without oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		±13		±20	*		*	V
Quiescent Current			±6	±6.7		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades		−25		+85	*		*	°C
S Grade		−55		+125				°C
Operating								
B and C Grades		−25		+85	*		*	°C
S Grade		−55		+125				°C
Storage		−65		+150	*		*	°C

*Specification the same as for VFC320BG/BM/SM.

NOTES:
1. A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity.
2. Determined by R_{IN} and full scale current range constraints.
3. Adjustable to zero. See Offset and Gain Adjustment section.
4. Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section.
5. When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy.
6. For $e_1 = 0$ typical linearity errors are: 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz.
7. Exclusive of external components' drift.
8. FSR = Full Scale Range (corresponds to full scale and full scale input voltage.
9. Positive drift is defined to be increasing frequency with increasing temperature.
10. One pulse of new frequency plus 50nsec typical.

ABSOLUTE MAXIMUM RATINGS

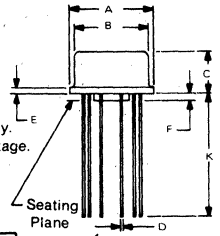
Supply Voltages	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, -Input	$\pm V_{CC}$
Input Voltage, +Input	$\pm V_{CC}$
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL

VFC320BM/CM/SM
TO-100 PACKAGE

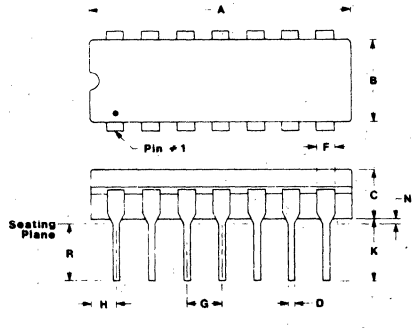
NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
	.335	.370	8.51	9.40
	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

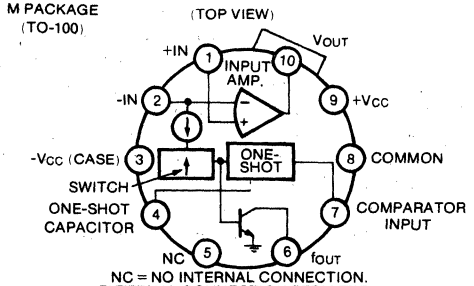
NOTES: 1. Leads in true position within 0.01" (0.25mm) R at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.753	.767	19.13	19.48
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	--	.085	--	2.16
J	.008	.012	0.20	0.30
K	.150	--	3.80	--
L	0.3 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

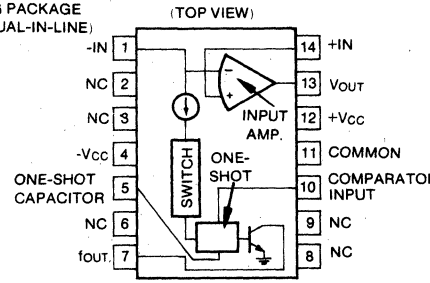
PIN CONFIGURATIONS

M PACKAGE
(TO-100)



NC = NO INTERNAL CONNECTION.
EXTERNAL CONNECTION PERMITTED.

G PACKAGE
(DUAL-IN-LINE)



DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero). Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC320 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission).

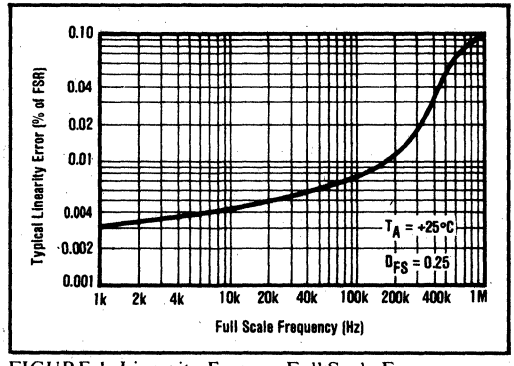


FIGURE 1. Linearity Error vs Full Scale Frequency.

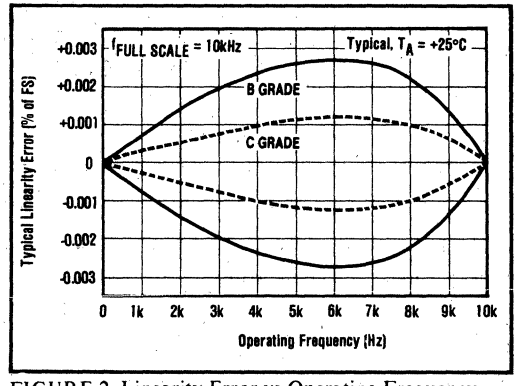


FIGURE 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC320 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC320.

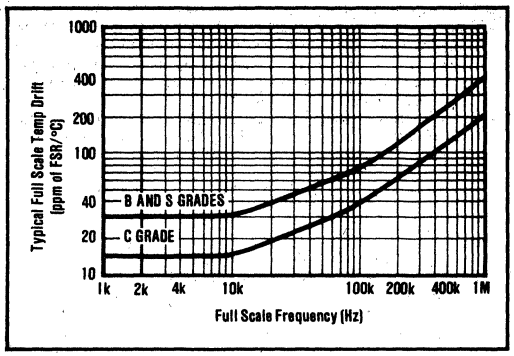


FIGURE 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC320 to changes in input signal level is specified for a full scale step, and is 50nsec plus 1 pulse of the new frequency. For a 10V input signal step with the VFC320 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10μsec.

THEORY OF OPERATION

The VFC320 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a one-shot), two switched current sinks, and an open collector output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = -7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this -7.5V threshold point at C_1, comparator B resets the flip-flop, and the ramp voltage begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC320 is derived for the

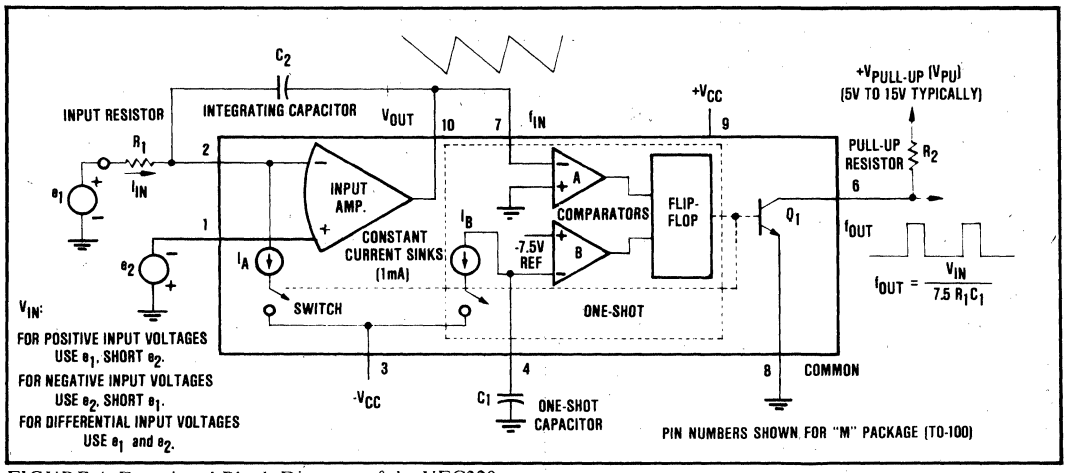


FIGURE 4. Functional Block Diagram of the VFC320.

the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$

In the time $t_1 + t_2$ the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN}\, t_1 + (I_{IN} - I_A)\, t_2 \quad (2)$$

$$\text{So that } I_{IN}\,(t_1 + t_2) = I_A\, t_2 \quad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A R_1 t_2} \quad (6)$$

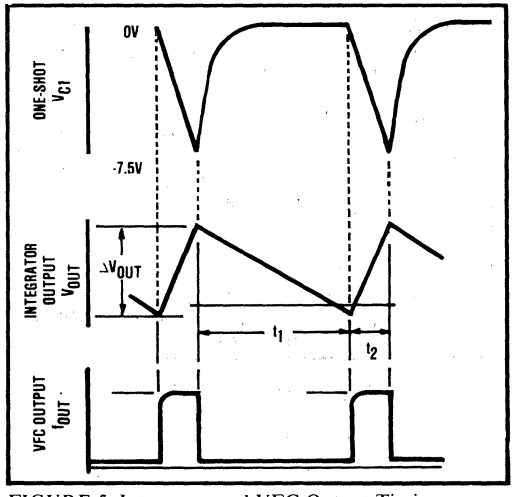


FIGURE 5. Integrator and VFC Output Timing.

In the time t_2, I_B charges the one-shot capacitor C_1 until its voltage reaches -7.5V and trips comparator B.

$$\text{Thus } t_2 = \frac{C_1\, 7.5}{I_B} \quad (7)$$

$$\text{Using (7) in (6) yield } f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$$

$$\text{Since } I_A = I_B \text{ the result is}$$

$$f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \quad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC320 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC320, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle, D, is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\ max\ /\ R_1}{1mA} = \frac{I_{IN}\ max}{1mA}$$

Thus $D_{FS} = 0.25$ corresponds tc $I_{IN}\ max = 0.25mA$.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VFC320 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

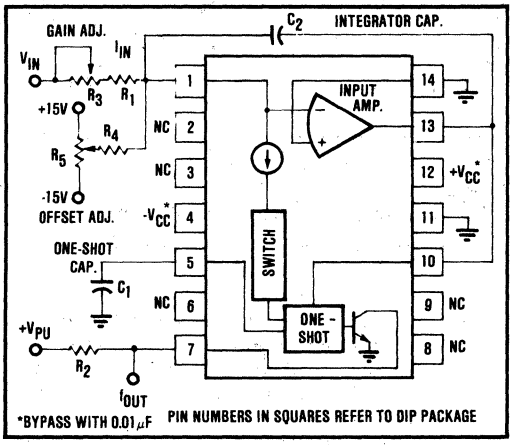


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

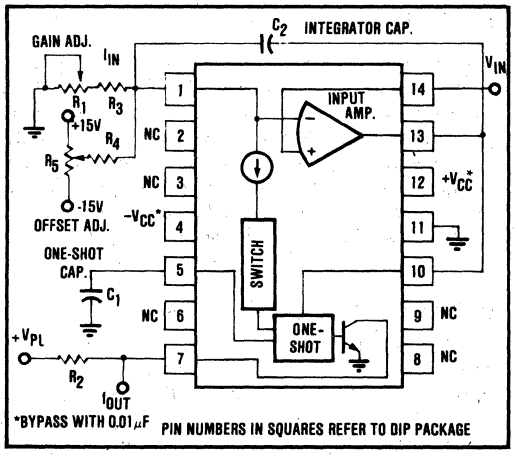


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, (5) selecting the integrator capacitor C_2, and (6) selecting the output pull-up resistor, R_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected. The nominal value is R_1 is

$$R_1 = \frac{V_{IN}\ max}{0.25mA} \qquad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\ nom} = \frac{V_{IN}}{7.5\ R_1\ f_{OUT}} \qquad (11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1(pF) = \frac{33 \times 10^6}{f_{FS}} - 15 \qquad (12)$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC320 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at $D_{FS} = 25\%$.

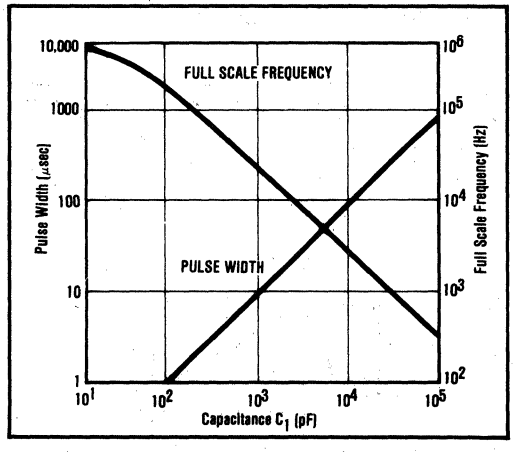


FIGURE 8. Output Pulse Width ($D_{FS} = 0.25$) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator

determine a range of acceptable values,

$$C_2\ (\mu F) = \begin{cases} 100/f_{FS};\ \text{if } f_{FS} \leq 100\text{kHz} \\ 0.001;\ \text{if } 100\text{kHz} < f_{FS} \leq 500\text{kHz} \\ 0.0005;\ \text{if } f_{FS} > 500\text{kHz} \end{cases} \quad (13)$$

Output Pull Up Resistor R_2.

The open collector output can sink up to 8mA and still be TTL-compatible. Select R_2 according to this equation:

$$R_2\ \text{min}\ (\Omega) = V_{PULLUP}/(8\text{mA} - i_{LOAD})$$

A 10% carbon film resistor is suitable for use as R_2.

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for intitial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1, to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 x full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC320 is 0.015% of FSR/% max. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommeded. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the f_{OUT} pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 ($D_{FS} = 0.25$)

$C_1 = [(33 \times 10^6)/f_{MAX}] - 15$ $\quad [(66 \times 10^6)/f_{MAX}] - 15$ if $D_{FS} = 0.5$

$= [(33 \times 10^6)/100\text{kHz}] - 15$

$= 315\text{pF}$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 ($D_{FS} = 0.25$)

$R_1 + R_3 = V_{IN}\ \text{max}/0.25\text{mA}$ $\quad V_{IN}\ \text{max}/0.5\text{mA}$ if $D_{FS} = 0.5$

$= 10\text{V}/0.25\text{mA}$

$= 40\text{k}\Omega$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$C_2 = 10^2/F_{max}$

$= 10^2/100\text{kHz}$

$= 0.001\mu\text{F}$

Choose a 0.001μF capacitor with ±5% tolerance.

Selecting R_2

$R_2 = V_{PULLUP}/(8\text{mA} - i_{LOAD})$

$= 5\text{V}/(8\text{mA} - 1.6\text{mA})$, one TTL-load = 1.6mA

$= 781\Omega$

Choose a 750Ω 1/4-watt carbon compensation resistor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC320 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1t (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero, to insure that the input signal at pin 10 crosses the zero threshold. Errors are nulled following the procedure given on this page, using 0.001 x full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

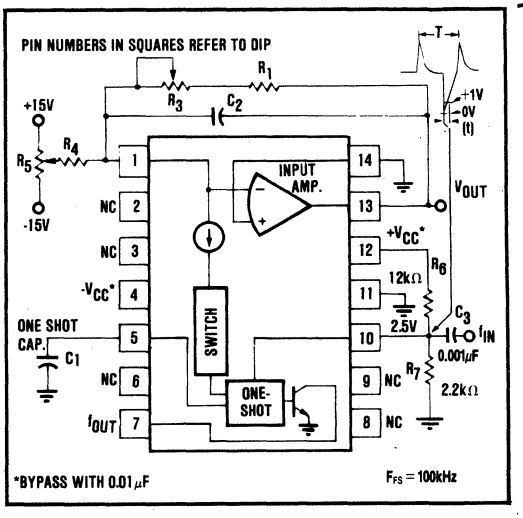


FIGURE 9. Connection Diagram for F/V Conversion.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC320 ideal for a variety of VFC applications. High accuracy allows the VFC320 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits.

Figures 10 - 14 show typical applications of the VFC320.

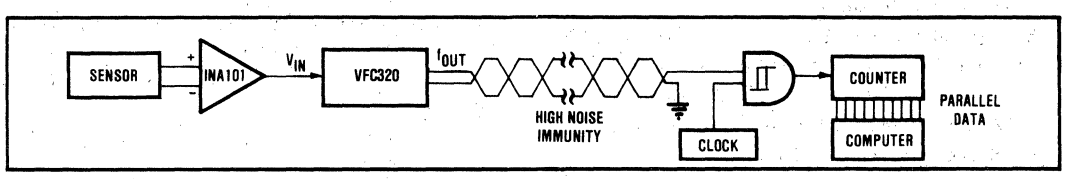


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

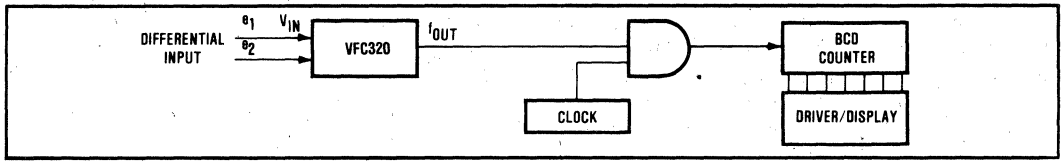


FIGURE 11. Inexpensive Digital Panel Meter.

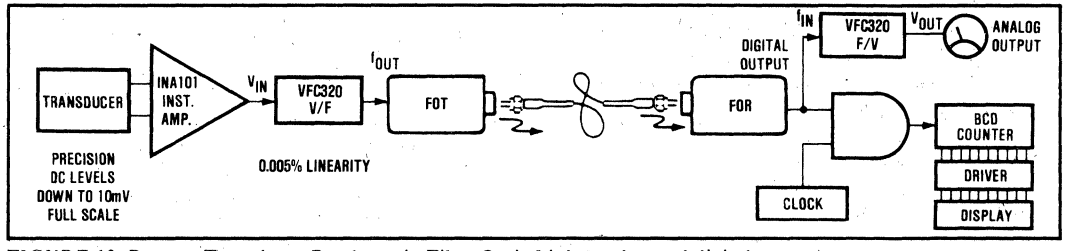


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

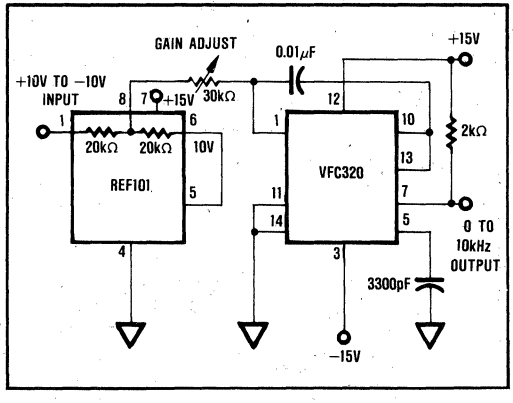


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

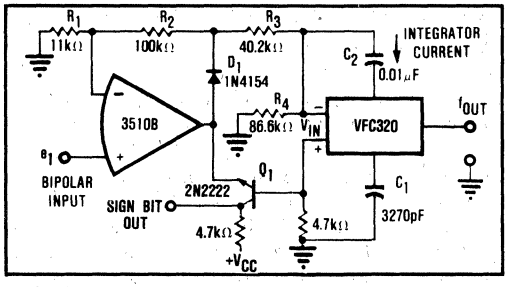


FIGURE 14. Absolute value circuit with the VFC320. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.

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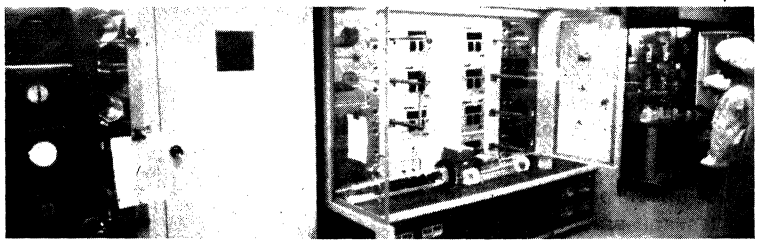
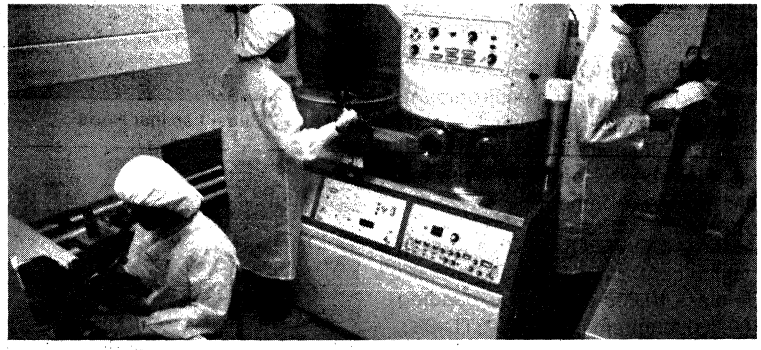


Wafer Processing



Wafer Processing

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All product families are fully specified from -55°C to +125°C with up to three performance grades and two product assurance levels (/883B and /MIL).

The /883B models are 100% screened to MIL-STD-883, level B, method 5004 or 5008. The /MIL models have additional requirements of 10% PDA and QCI consisting of groups A and B on each inspection lot.

How stringently our Military Products group controls and documents the assembly and testing of its products is described in the product flow section that follows.

All materials used by the Military Products group have unique component specifications to assure their conformity to MIL-STD-883, methods 2010 and 2017.

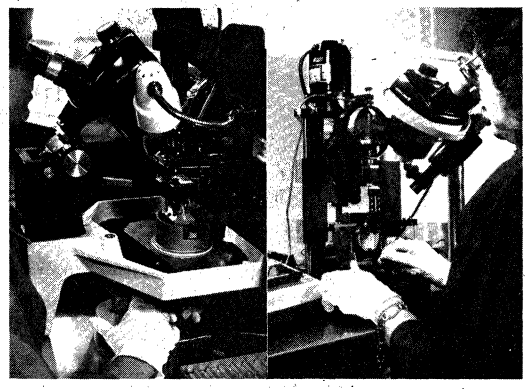
Environmental control in our clean room areas meets and often exceeds Federal Standard 209B requirements for particle count. ESD (electrostatic discharge) procedures are fully observed through every stage of material handling, product assembly, testing, storage and shipment. Operator training, certification and re-certification conform to MIL-M-38510.

MTTF data is based on actual product performance, not just calculated values. Qualification reports and test data are available. All data sheets follow military slash sheet format and, because of their completeness, can be transferred directly to your drawings with minimal modification. This standard QPL slash sheet format simplifies your requests to government agencies for non-standard parts approval.

A CONTROLLED MANUFACTURING FACILITY DEDICATED EXCLUSIVELY TO MILITARY QUALITY PRODUCTION

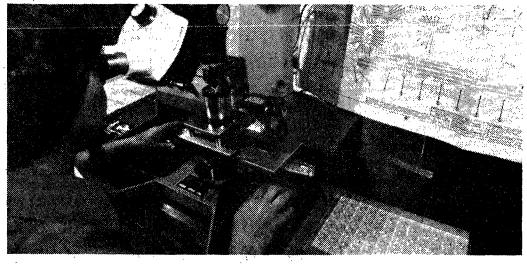
- PERSONNEL - All production and quality control personnel directly involved with fabrication, inspection, testing and handling perform their functions according to appropriate MIL specs.
- TRAINING - Operator training and certification programs provide trained personnel qualified to assemble and test the products. Certification requires classroom training and written examinations for initial certification. Periodic written exams must be passed to maintain certification.
- WORK-IN-PROCESS ENVIRONMENT - All work-in-process is stored in a nitrogen environment. Critical assembly processes; die visual, die attach, wirebond and all inspections are performed under laminar flow hoods - equipped with ion grids - in a class 100 environment.
- ENVIRONMENTAL CONTROL - Clean room procedures, which conform to Federal Standard 209B, provide class 10,000 clean air exceeding the class of 100,000 requirement of MIL-STD-883.
- MATERIAL CONTROL - Each product has a complete and current flow chart and flow sheet to assure accurate processing through assembly and test. Each manufacturing lot contains the lot numbers of its components listed by the quality control inspection identification (QCID number) all traceable back to the incoming vendor's lot number.
- MANUFACTURING LOT CONTROL - Each lot has a unique flow sheet which documents lot number, parts list, operation, quantity, date of operation and operator's identification.
- EQUIPMENT CALIBRATION - Performed under the guidance of MIL-STD-45662.
- QUALIFICATION - All /MIL models are initially qualified per MIL-STD-883, method 5004 or 5008, groups A, B, C and D as described in the products' detailed specification.
- STATIC CONTROL - To minimize static (ESD) damage, antistatic smocks, stainless steel table tops, stainless steel work-in-process trays, ground straps, ion grids under laminar flow hoods and anti-static shipping materials are used.
- RECORD RETENTION - All flow sheets containing process data and inspection records are retained for three years.

Assembly Under Laminar Hood



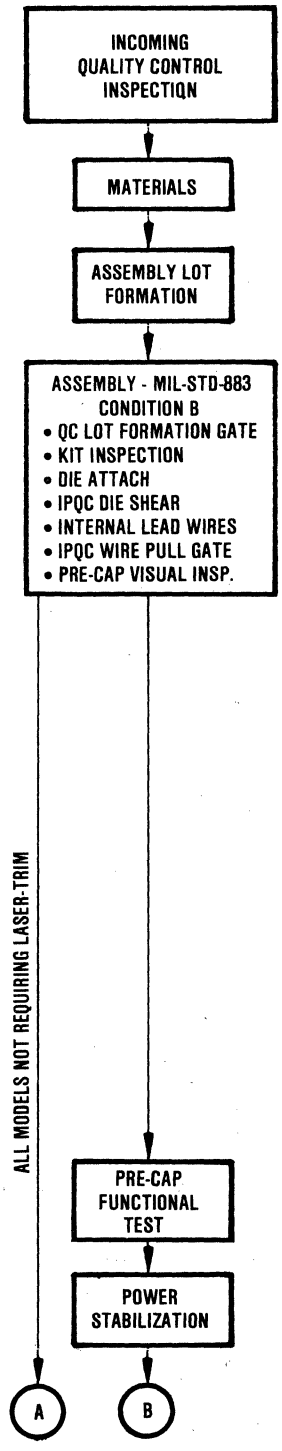
Wirebond (Gold) **Die Shear**

Wirebond (Aluminum)



Die Attach

PRODUCT FLOW



Assures that all materials meet requirements of the applicable component specification. Usage tests are performed and vendor lot traceability begins.

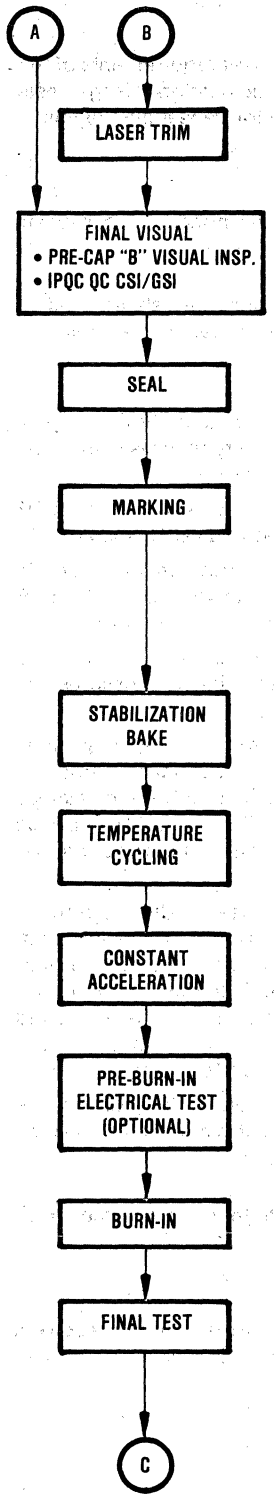
All material is maintained in a bonded stockroom to assure traceability.

Orgination of manufacturing flow sheets, bill of material, materials and lot traceability records.

- QC Lot Formation Gate - matches flow sheet, bill of materials and traceability records with materials issued from the stockroom
- Kit Inspection - piece parts and die are 100% visually inspected to methods 2010 and 2017.
- Die Attach - eutectic (providing low ohmic contact) and non-conductive epoxy (cured at 25°C above storage temperature in nitrogen).
- In Process Die Shear Gate - performed to method 2019 on each manufacturing lot. Assures the integrity of the die attach method.
- Internal Lead Wires - Wires are of the same metal as the die metalization. Aluminum ultrasonic wirebond machines are mounted on shock tables to insure quality bonds. Gold-to-gold wirebonds are performed with thermosonic wirebond machines.
- In Process Wire Pull Gates - bonding operations are monitored at the beginning of each shift, every four hours, with a new lot, new operator or a machine adjustment. Both destruct and non-destruct tests are performed and the length and width of each wirebond is measured to verify conformance to method 2010 or 2017.
- Pre-Cap Visual Inspection - Although not required by MIL-STD-883 it is performed by Burr-Brown to method 2010 or 2017.

Performed on all products that require laser trimming.

All products that require laser-trimming receive a 72-hour burn-in, in nitrogen, at +125°C.



Resistor networks are laser-trimmed to meet applicable specifications.

- Pre-Cap "B" Visual Inspection - a 100% visual inspection to method 2010 or 2017.
- In Process QC Pre-Cap "B" Visual Gate - performed to method 2010 or 2017. (Source Inspection performed if required.)

Following a vacuum bake at +125°C (to meet method 5004 or 5008 moisture content requirements) products are welded, gold/tin or glass sealed.

Marking is in accordance with MIL-M-38510 and consists of;

- Part number
- Seal date code
- Manufacturer's identification (BURR-BROWN®)
- Manufacturer's designating symbol (CEBS)
- Country of origin

A 24-hour minimum bake at +150°C per MIL-STD-883, method 1008, condition C.

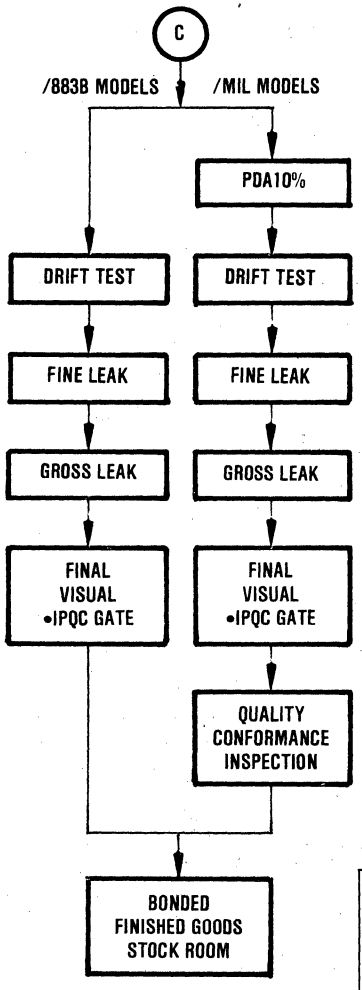
Ten cycles, from -65°C to +150°C per MIL-STD-883, method 1010, condition C.

Performed to MIL-STD-883, method 2001, in the Y_1 axis only.

Product performance is compared to the specified DC parameters at 25°C.

Total burn-in time is 160 hours minimum at an ambient temperature of +125°C per MIL-STD-883, method 1015.

Product performance is compared to the specified DC parameters at 25°C. All 25°C parameters specified in the data sheets are read and recorded.



The assembly lot PDA (percent defective allowable) cannot exceed 10%.

All drift parameters as specified in the data sheet are 100% tested at -55°C, -25°C, +25°C, +85°C and +125°C.

100% test to MIL-STD-883, method 1014, test condition A.

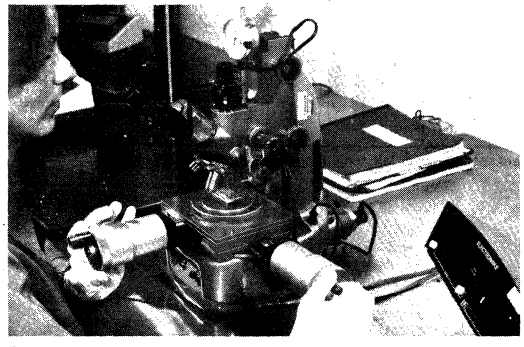
100% test to MIL-STD-883, method 1014, condition C.

100% external visual inspection to MIL-STD-883, method 2009.

- Final Visual Quality Control Gate - to MIL-STD-883, method 2009.

Groups A and B inspection of MIL-STD-883, method 5005 or 5008 are performed on each inspection lot. Groups C and D inspections are performed when agreed to by contract. A report of the most recent Groups C and D inspections is available from Burr-Brown at a nominal charge.

This product flow illustrates major operations only. Space does not allow a complete description of the numerous details of all operations. Processes and flows may change to conform to latest revisions or to improved product performance and quality.



Bond Measurement

Wire Pull

SELECTION GUIDE

ANALOG-TO-DIGITAL CONVERTERS								
Model	Resolution Bits	Linearity ±LSB, max	Conversion Time μsec, max	Gain Drift ±ppm/°C, max	Input Range V	Operating Temperature Range[1]	Package	Page
ADC87/MIL	12	1/2	8	15	±2.5,	MIL	32-pin DIP	11-8
ADC87/883B	12	1/2	8	15	±5,	MIL		11-8
ADC87	12	1/2	8	15	±10,	MIL		11-8
ADC87U/883B	12	1/2	8	15	0 to +5,	MIL		11-8
ADC87U	12	1/2	8	15	0 to +10	MIL		11-8

DIGITAL-TO-ANALOG CONVERTERS									
Model	Resolution Bits	Linearity ±LSB, max	Monotonicity	Gain Drift ±ppm/°C, max	Settling Time max	Output Ranges	Operating Temperature Range[1]	Package	Page
DAC87-CBI-V/MIL	12	1/2	−55°C/+125°C	20	7μsec	±2.5,	MIL	24-pin DIP	11-24
DAC87-CBI-V/B	12	1/2	−55°C/+125°C	20	7μsec	±5,	MIL	24-pin DIP	11-24
DAC87-CBI-V	12	1/2	−55°C/+125°C	20	7μsec	±10,	MIL	24-pin DIP	11-24
DAC87U-CBI-V/B	12	1/2	−25°C/+85°C	20	7μsec	+5,	MIL	24-pin DIP	11-24
DAC87U-CBI-V	12	1/2	−25°C/+85°C	20	7μsec	+10	MIL	24-pin DIP	11-24
DAC87-CBI-I/B	12	1/2	−55°C/+125°C	20	400nsec		MIL	24-pin DIP	11-36
DAC87-CBI-I	12	1/2	−55°C/+125°C	20	400nsec	0 to 2mA,	MIL	24-pin DIP	11-36
DAC87U-CBI-I/B	12	1/2	−25°C/+85°C	20	400nsec	±1mA	MIL	24-pin DIP	11-36
DAC87U-CBI-I	12	1/2	−25°C/+85°C	20	400nsec		MIL	24-pin DIP	11-36
DAC870V/MIL	12	1/2	−55°C/+125°C	25	7μsec		MIL		11-48
DAC870V/883B	12	1/2	−55°C/+125°C	25	7μsec		MIL	24-pin DIP ceramic	11-48
DAC870V	12	1/2	−55°C/+125°C	25	7μsec		MIL		11-48
DAC870U/883B	12	1/2	−25°C/+85°C	20	7μsec	±2.5,	MIL		11-48
DAC870U	12	1/2	−25°C/+85°C	20	7μsec	±5, ±10,	MIL		11-48
DAC870VL/MIL	12	1/2	−55°C/+125°C	25	7μsec	0 to +5,	MIL	28-terminal leadless chip carrier	11-48
DAC870VL/883B	12	1/2	−55°C/+125°C	25	7μsec	0 to +10	MIL		11-48
DAC870VL	12	1/2	−55°C/+125°C	25	7μsec		MIL		11-48
DAC870UL/883B	12	1/2	−25°C/+85°C	20	7μsec		MIL		11-48
DAC870UL	12	1/2	−25°C/+85°C	20	7μsec		MIL		11-48

VOLTAGE-TO-FREQUENCY CONVERTERS							
Model	V_{IN} Range V	F_{OUT} Range kHz, max	Linearity % FSR, max	Full Scale Drift ppm FSR/°C, max	Operating Temperature Range[1]	Package	Page
VFC32WM/883B	±10	200	±0.006 at 10kHz	±100 at 10kHz	MIL	TO-100	11-120
VFC32WM	±10	200	±0.006 at 10kHz	±100 at 10kHz	MIL	TO-100	11-120
VFC32VM/MIL	±10	200	±0.01 at 10kHz	−400, +150 at 200kHz	MIL	TO-100	11-120
VFC32VM/883B	±10	200	±0.01 at 10kHz	−400, +150 at 200kHz	MIL	TO-100	11-120
VFC32VM	±10	200	±0.01 at 10kHz	−400, +150 at 200kHz	MIL	TO-100	11-120
VFC32UM/883B	±10	200	±0.01 at 10kHz	±150 at 10kHz	MIL	TO-100	11-120
VFC32UM	±10	200	±0.01 at 10kHz	±150 at 10kHz	MIL	TO-100	11-120

MULTIPLIERS								
Model	Accuracy at 25°C ±%, max	Accuracy at 125°C ±%, max	Feedthrough ±mV, max	Output Offset ±mV, max	Output V, mA, min	Operating Temperature Range[1]	Package	Page
4213WM/883B	1/2	4	50	25	±10, ±5	MIL	TO-100	11-151
4213WM	1/2	4	50	25	±10, ±5	MIL	TO-100	11-151
4213VM/MIL	1	4	100	30	±10, ±5	MIL	TO-100	11-151
4213VM/883B	1	4	100	30	±10, ±5	MIL	TO-100	11-151
4213VM	1	4	100	50	±10, ±5	MIL	TO-100	11-151
4213UM/883B	1	2[2]	100	50	±10, ±5	MIL	TO-100	11-151
4213UM	1	2[2]	100	50	±10, ±5	MIL	TO-100	11-151

NOTES: (1) U grade specified temperature range is −25°C to +85°C; all others specified over MIL temp range. (2) At +85°C.

OPERATIONAL AMPLIFIERS

Description	Model	Offset Voltage at 25°C ±mV, max	Offset Voltage drift ±μV/°C max	Bias Current nA, max	Bandwidth Unity Gain MHz, min	Slew Rate V/μs, min	ts ±0.01% ns	Compensation	Output V, mA, min	Operating Temp. Range[1]	Package	Page
Wideband	OPA600VM/MIL	2	20	−100pA	5000,[2] A = 1000	400	125	external	±10, ±200	MIL	16-pin DIP	11-94
	OPA600VM/883B	2	20	−100pA		400	125	external	±10, ±200	MIL		11-94
	OPA600VM	2	20	−100pA		400	125	external	±10, ±200	MIL		11-94
	OPA600UM/883B	5	80	−100pA		400	150	external	±10, ±200	MIL		11-94
	OPA600UM	5	80	−100pA		400	150	external	±10, ±200	MIL		11-94
General Purpose Bipolar	3500R/MIL	5	20	±30	1	0.6	—	internal	±10, ±10	MIL	TO-99	11-132
	3500R/883B	5	20	±30	1	0.6	—	internal	±10, ±10	MIL	TO-99	11-132
	3500U/883B	5	20[3]	±30	1	0.6	—	internal	±10, ±10	MIL	TO-99	11-132
Precision Bipolar	3510VM/MIL	0.12	2	±25	0.25	0.5	—	internal	±10, ±10	MIL	TO-99	11-143
	3510VM/883B	0.12	2	±25	0.25	0.5	—	internal	±10, ±10	MIL	TO-99	11-143
Low Drift, Low Bias	OPA105WM/MIL	250	2	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105WM/883B	250	2	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105WM	250	2	1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105VM/MIL	250	5	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105VM/883B	250	5	1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105VM	250	5	1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105UM/883B	250	15[3]	1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
	OPA105UM	250	15[3]	1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	11-74
Ultra Low Bias Current	OPA106WM/MIL	250	5	100fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106WM/883B	250	5	100fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106WM	250	5	100fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106VM/MIL	250	10	150fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106VM/883B	250	10	150fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106VM	250	10	150fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106UM/883B	250	20[3]	300fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
	OPA106UM	250	20[3]	300fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	11-84
Power	OPA8780VM/MIL	10	30	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	11-110
	OPA8780VM/883B	10	30	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	11-110
	OPA8780VM	10	30	.05	5	15	—	internal	±30, ±60	MIL	TO-3	11-110
	OPA8780UM/883B	10	50	.05	5	15	—	internal	±30, ±60	MIL	TO-3	11-110
	OPA8780UM	10	50	−.05	5	15	—	internal	±30, ±60	MIL	TO-3	11-110

NOTES: (1) U grade specified temperature range is −25°C to +85°C; all others specified over MIL temp range. (2) Gain-bandwidth product. (3) −25°C/+85°C.

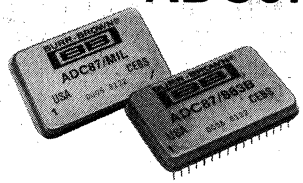
INSTRUMENTATION AMPLIFIERS

Description	Model	Range[1]	Gain Error (% FS) 25°C G = 100, max	Non-Linearity (%), 25°C, G = 100 max	CMR, DC to 60Hz, G = 10 1kΩ, Unbal...min T_A	$V_{IO}/\Delta T$ (μV/°C) max G =1000	Slew Rate (V/μsec) 25°C G = 100 R_C= 2kΩ	Operating Temp. Range[2]	Package	Page
Very High Accuracy	INA258WG/MIL	1-1000	0.1	0.007	96dB	0.5	0.2	MIL	18-pin DIP	11-61
	INA258WG/883B	1-1000	0.1	0.007	96dB	0.5	0.2	MIL		11-61
	INA258WG	1-1000	0.1	0.007	96dB	0.5	0.2	MIL		11-61
	INA258VG/MIL	1-1000	0.1	0.007	96dB	1.0	0.2	MIL		11-61
	INA258VG/883B	1-1000	0.1	0.007	96dB	1.0	0.2	MIL		11-61
	INA258VG	1-1000	0.1	0.007	96dB	1.0	0.2	MIL		11-61
	INA258UG/883B	1-1000	0.1	0.007	96dB	1.8[3]	0.2	MIL		11-61
	INA258UG	1-1000	0.1	0.007	96dB	1.8[3]	0.2	MIL		11-61
	INA258WL/MIL	1-1000	0.1	0.007	96dB	0.5	0.2	MIL	20-Terminal LCC	11-61
	INA258WL/883B	1-1000	0.1	0.007	96dB	0.5	0.2	MIL		11-61
	INA258WL	1-1000	0.1	0.007	96dB	0.5	0.2	MIL		11-61
	INA258VL/MIL	1-1000	0.1	0.007	96dB	1.0	0.2	MIL		11-61
	INA258VL/883B	1-1000	0.1	0.007	96dB	1.0	0.2	MIL		11-61
	INA258VL	1-1000	0.1	0.007	96dB	1.0	0.2	MIL		11-61
	INA258UL/883B	1-1000	0.1	0.007	96dB	1.8[4]	0.2	MIL		11-61
	INA258UL	1-1000	0.1	0.007	96dB	1.8[4]	0.2	MIL		11-61

NOTES: (1) Set with external resistor. (2) MIL = −55°C to +125°C; U grade specified temperature is −25°C to +85°C; all others specified over MIL temperature range. (3) −25°C to +85°C.

BURR-BROWN®

ADC87/MIL SERIES



MODEL NUMBERS:

ADC87/MIL ADC87U/883B
ADC87/883B ADC87U
ADC87

REVISION A
DECEMBER, 1982

12-BIT -55°C to +125°C Military ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **HI-REL MANUFACTURE**
- **ACCURATE**
  - **±1/2LSB max Linearity Error**
  - **±0.1% FSR max Full Scale Absolute Accuracy**
  - **±15ppm max Gain Drift**
- **8μsec MAX CONVERSION TIME**
- **-55°C TO +125°C OPERATION**
- **COMPLETE**
  - **Internal Reference**
  - **Internal Buffer**
  - **Internal Clock**
- **MIL-STD-883 SCREENING**

DESCRIPTION

The ADC87 MIL Series is a high performance, analog-to-digital converter. It features ±1 2LSB linearity, ±0.1% full scale accuracy, ±15ppm drift, 8μsec conversion time, -55°C to +125°C operation and optional MIL-STD-883 screening.

The ADC87 uses successive approximation. It resolves the most significant bit first, then the second bit, then the third, etc. Successive approximation is the most popular high performance design as it is fast and accurate.

The ADC87 is a hybrid microcircuit. It is complete with an internal reference, an input buffer amplifier and an internal clock. The converter may be short cycled to provide faster conversions to less resolution. Five analog input ranges, ±2.5V, ±5V, ±10V, 0 to +10V and 0 to +20V, are available, and the digital output data is available in parallel and serial format. All digital outputs and inputs are TTL compatible. Standard power supply voltages, ±15VDC and +5VDC, are required.

Two electrical performance grades are available. The premium grade operates from -55°C to +125°C and is designed for military, aerospace, and demanding industrial applications. The U grade has specifications from -25°C to +85°C and from -55°C to +125°C. Applications include test equipment, shipboard, and ground support equipment where operation is normally between -25°C and +85°C and full temperature range operation must be assured.

The ADC87 MIL Series is manufactured on a separate Hi-Rel manufacturing line with impeccable clean room conditions which assures inherent quality and provides for long product life. The ADC87 is hermetically sealed in a metal, welded, dual-in-line package.

Three product assurance levels are available: Standard, 883B and MIL. The Standard product assurance level offers Hi-Rel manufacturing where many MIL-STD-883 screens are performed routinely. The 883B product assurance level, 883B suffix, offers Hi-Rel manufacturing plus 100% screening per MIL-STD-883 method 5008 (class B). The MIL product assurance level, MIL suffix, offers Hi-Rel manufacturing, 100% screening per MIL-STD-883B method 5008 and 10% PDA. Quality assurance further processes MIL devices, by performing group A and B inspections on each inspection lot and group C and D inspections periodically and when specified on the customer's purchase order. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
ANALOG-TO-DIGITAL CONVERTER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detailed requirements for a precision 12-bit, integrated circuit, analog-to-digital converter.

1.2 Part number. The complete part number is as shown below.

ADC87		MIL
Basic model number	Grade (see 1.2.1)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, analog-to-digital converter.
There are two electrical performance grades. The premium grade has no grade designation in the part number and features specifications and tests from -55°C to +125°C. The U grade has a U grade designation in the part number and features specifications and tests from -25°C to +85°C, and specifications from -55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinquishes the product assurance levels as follows:

Hi-Rel Product Designator	Requirements
MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
883B	Standard model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is as defined in Figure 1. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±18VDC
Supply voltage, V_{DD}	+7VDC
Analog inputs (pins 24 and 25)	±25VDC
Buffer input	±18VDC
Digital inputs	+5.5VDC
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60sec)	+300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: +4.75VDC to +5.25VDC
Case temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A	Maximum θ J-A
32-lead can	Figure 1	1500mW at T_A = 125°C	7°C/W	25°C/W	32°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510, except that organic and polymeric materials may be used for substrate and die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-STD-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. All dice utilized are glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

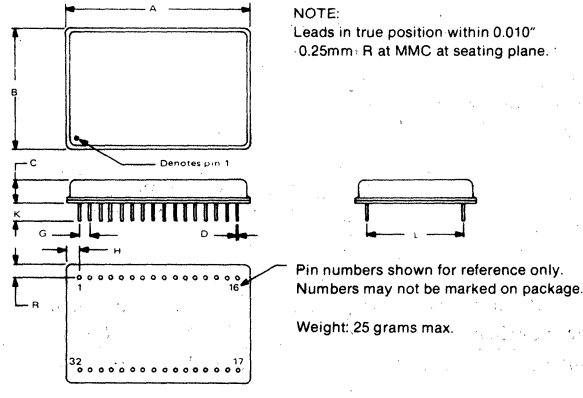
3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connection. The circuit diagram and terminal connections are shown in Figure 2.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating case temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Input Range. The analog input range is as specified in Table V when externally connected as shown therein.

3.3.2 Output Code. Coding is complementary binary. The digital output codes corresponding to analog input voltages are shown in Table VI.



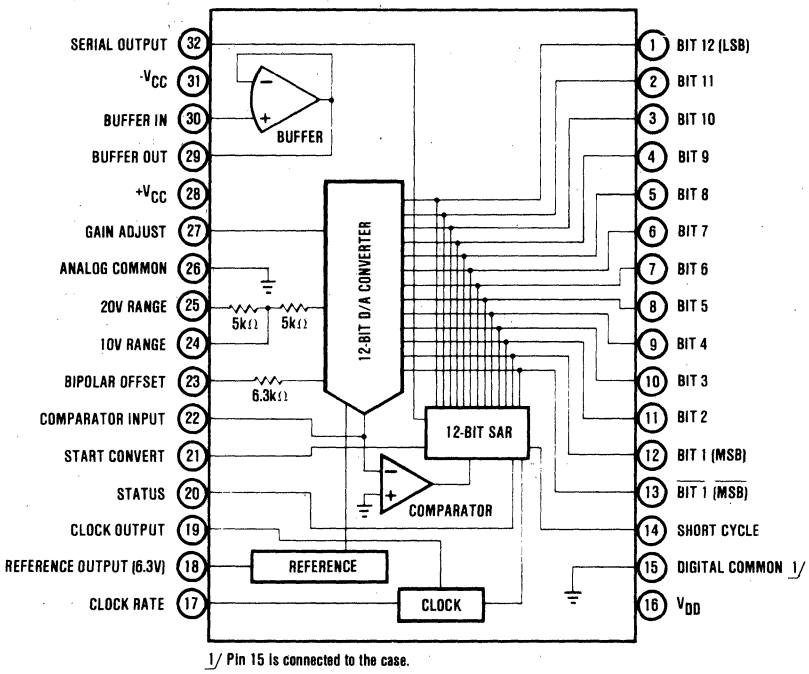
NOTE:
Leads in true position within 0.010" 0.25mm R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

Weight: 25 grams max.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

FIGURE 1. Case Outline (Triple-Wide DIP Configuration).



1/ Pin 15 is connected to the case.

FIGURE 2. Circuit Diagram and Terminal Connections (Bottom View).

3.3.3 Transfer Function. An A/D converter represents an analog input voltage in a digital output format. The converter resolves the analog input into 12 bits of resolution, or 2^{12}, or 4096 voltage segments. For each voltage segment there is a unique digital output code.

The ideal transfer curve, as shown in Figure 3, is a "stair-case" connecting the extremes of the analog input range. Minus full scale (-FS) corresponds to digital 1111 1111 1111, the first transition occurs at -FS +1/2LSB, each bit is 1LSB wide, and +FS -1LSB corresponds to digital 0000 0000 0000. An ideal straight line connects each end point and the center of each bit. A best fit straight line is parallel to the ideal straight line and biased to minimize linearity errors. Note, the coding is complementary.

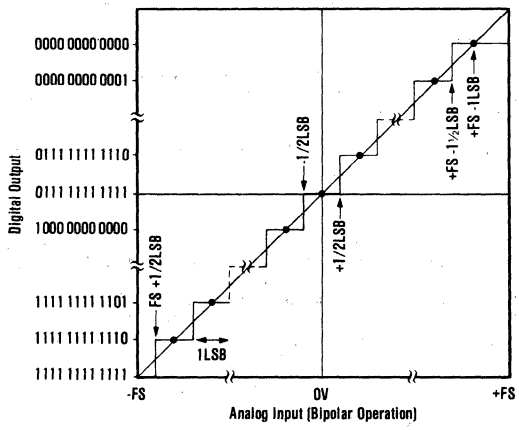
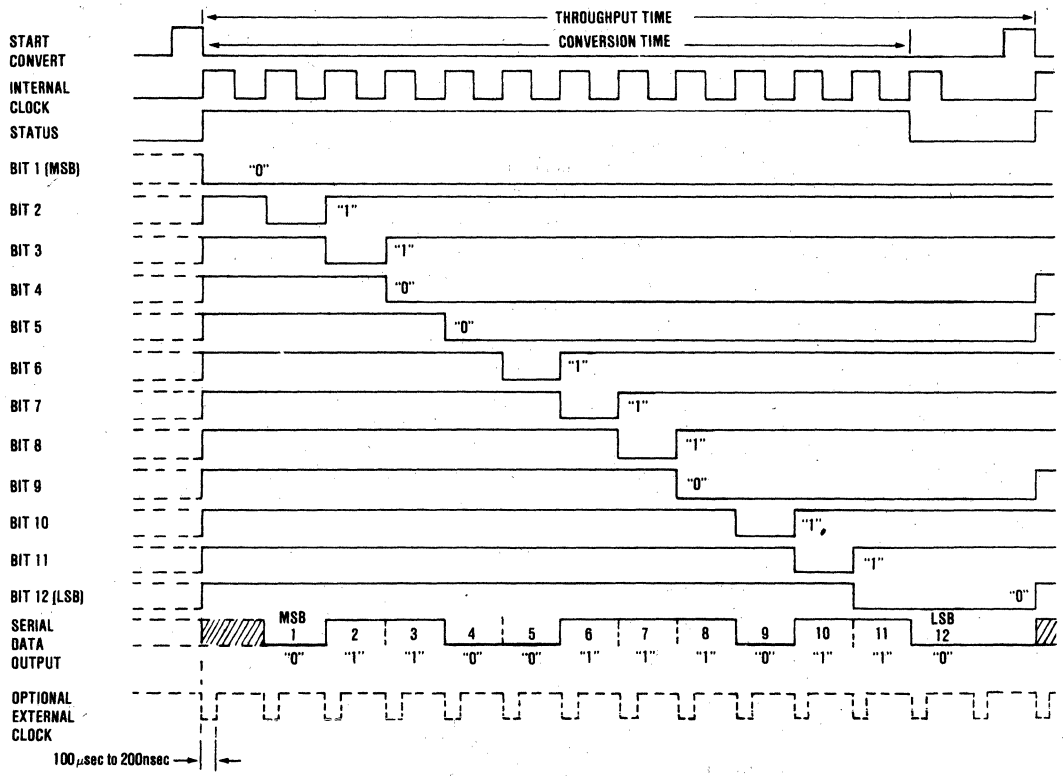


FIGURE 3. Ideal A/D Converter Transfer Function.

The 'basic' converter is unipolar in design; that is, 0VDC analog input produces one digital extreme and plus full scale VDC produces the other digital extreme. There are two unipolar input ranges. For bipolar operation, a bias (bipolar offset) is introduced into the input such that 0VDC analog input produces midscale digital output. This allows plus and minus analog inputs (see Figure 3). There are three bipolar input ranges.

The errors from the best fit transfer function are specified in Table I. Linearity and Differential Linearity are the most meaningful ADC87 accuracy indicators, as they are not externally adjustable. They are factory laser-trimmed. Zero error and gain error are laser-trimmed and may be externally nulled if necessary for the application. The inherent quantization uncertainty due to resolving or quantizing the analog input into bits is $\pm 1/2$LSB.

3.3.4 Timing Considerations. The timing diagram is shown in Figure 4. A start convert, positive going pulse, initiates a conversion. The most significant bit (MSB) is determined during the second clock pulse, and each successive bit is determined during the next 11 clock pulses. When conversion is complete, Status output drops to Logic 0. Digital output data is available in parallel or serial format. Serial output data may be strobed out bit-by-bit, during the clock period after the bit is determined. If desired, an external clock may be used. Further information is available in Applications Information, paragraph 7.



1. Start Convert must be at least 50nsec wide and must remain low during conversion. Conversion is initiated by the Start Convert trailing edge. Once a conversion has begun, a second start pulse will not reset the converter.
2. Parallel data will be valid 140nsec after status goes low and remains valid until another conversion is initiated.
3. Serial data will be valid 140nsec after an internal clock rising edge and 200nsec after an external clock falling edge.
4. When using an external clock, conversion is initiated by the falling edge of the first clock pulse following status going low. The converter will continuously convert.

FIGURE 4. Timing Diagram.

3.3.5 Zero error and gain error adjustment. Zero error and gain error may be externally nulled using the circuits shown in Figure 6. See Applications Information, paragraph 7.4.

3.3.6 Required external connections. For specified accuracy and speed, connect Clock Rate, pin 17, to 0VDC, pin 15.

For a 12-bit conversion cycle, connect Short Cycle, pin 14, to Logic 1, pin 16. See Applications Information, paragraph 7, for additional information.

3.4 Electrical test requirements. Electrical test requirements are as specified in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragraph 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin (U.S.A.)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the MIL Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability, for MIL, is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for MIL and 883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

Screening for the standard model, includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition A), and external visual inspection per MIL-STD-883, method 5008, hybrid class.

For the MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the MIL Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

1/ A 4-digit date code, indicating year and week of seal, is marked on 883B and (none) Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics.

T_C = -55°C to +125°C, Supply Voltages ±15VDC and +5VDC, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	LIMITS						UNITS
		ADC87/MIL ADC87/883B ADC87			ADC87U/883B ADC87U			
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION		12			•			Bits
ANALOG INPUTS								
Input Voltage Ranges: Unipolar			0 to +5, 0 to +10			•		V
Bipolar			±2.5, ±5, ±10			•		V
Direct Input Impedance: 0 to +5V, ±2.5V			2.5			•		kΩ
0 to +10V, ±5V			5			•		kΩ
±10V			10			•		kΩ
Buffer Amplifier: Gain Accuracy			±0.01			•		%
Input Impedance	T_C = +25°C		50		•	•		MΩ
Input Bias Current	T_C = +25°C		100			•		nA
Offset Voltage	T_C = +25°C		2	5		•		mV
Settling Time	20V step to ±0.01% FSR		2			•		µsec
DIGITAL INPUTS								
Start Convert Command: 1/								
Positive Pulse Width		50			•			nsec
Logic Loading				1			•	TTL Load 2/
Short Cycle Logic Loading				1			•	TTL Load
Logic Levels: Logic "1"		2			•			V
Logic "0"				0.8			•	V
All Digital Inputs								
DIGITAL OUTPUTS								
Parallel Data Coding: 3/								
Unipolar Ranges			CSB			•		
Bipolar Ranges			COB, CTC			•		
Output Drive		2			•			TTL Loads
Serial Data Coding NRZ 3/			CSB, COB			•		
Output Drive		2			•			TTL Loads
Status Bit Coding			Logic 1 During Conversion					
Output Drive		2			•			TTL Loads
Internal Clock Output Drive		2			•			TTL Loads
Logic Levels: Logic "1"		2.4			•			V
Logic "0"				0.4				V
All Outputs								
TRANSFER CHARACTERISTICS*								
Zero Error, Bipolar 4/	+25°C		±0.02	±0.05		±0.02	±0.07	% FSR 5/
Bipolar Major Transition Error	-25°C to +85°C					±0.05	±0.15	% FSR
	-55°C to +125°C		±0.05	±0.1			±0.3	% FSR
Full Scale Absolute Accuracy Error, 4/	+25°C		±0.05	±0.1		±0.05	±0.15	% FSR
Bipolar 6/	-25°C to +85°C					±0.1	±0.25	% FSR
	-55°C to +125°C		±0.1	±0.2			±0.6	% FSR
Gain Error 4/	+25°C		±0.05	±0.1		±0.05	±0.1	%
	Drift 7/		±10	±15		±10	±15	ppm/°C
Zero Error, Unipolar 4/	+25°C	+0.05	+0.10	+0.15	+0.05	+0.10	+0.2	% FSR
	-25°C to +85°C					±0.15	±0.3	% FSR
	-55°C to +125°C		±0.15	±0.2			±0.6	% FSR
Full Scale Absolute Accuracy Error, 4/	+25°C		±0.1	±0.2		±0.1	±0.25	% FSR
Unipolar	-25°C to +85°C					±0.2	±0.4	% FSR
	-55°C to +125°C		±0.2	±0.3			±0.9	% FSR
Linearity Error	+25°C		±1/4	±1/2		•	•	LSB 8/
	-25°C to +85°C					±1/2	±1	LSB
	-55°C to +125°C		±1/2	±1			±4	LSB
	Drift			±2			•	ppm of FSR/°C
Inherent Quantization Uncertainty			±1/2			•		LSB
Differential Linearity Error	+25°C		±1/4	±1/2		•	•	LSB
	-25°C to +85°C						±1	LSB
	-55°C to +125°C			±1			±3	LSB
	Drift		±2			•		ppm of FSR/°C
No Missing Codes		-55		+125	-25		+85	°C
Monotonicity		-55		+125	-25		+85	°C
Zero Adjustment Range		0.3	0.4		•	•		% FSR
Gain Adjustment Range		0.5	0.55		•	•		% FSR
DYNAMIC CHARACTERISTICS*								
Conversion Time 9/			7.5	8		•	•	µsec
Internal Clock Frequency 9/		1.5	1.6		•	•		MHz

*Transfer and dynamic characteristics are specified without the optional buffer amplifiers.

TABLE I. Electrical Performance Characteristics (cont).

Tc = -55°C to +125°C, Supply Voltages ±15VDC and +5VDC, unless otherwise specified.)

CHARACTERISTICS	CONDITIONS	LIMITS						UNITS
		ADC87/MIL ADC87/883B ADC87			ADC87U/883B ADC87U			
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE								
Internal Reference: Voltage		6.0	+6.3	6.6	*	*	*	V
Drift	-55°C to +125°C			±5			*	ppm/°C
External Current				200			*	μA
POWER SUPPLY								
Power Supply Range: ±15V Supply		±14.5	±15	±15.5	*	*	*	V
+5V Supply		+4.75	+5	+5.25	*	*	*	V
Quiescent Current: +15V			35	45		*	*	mA
-15V			35	45		*	*	mA
+5V			40	50		*	*	mA
Power Consumption	Quiescent		1300	1500		*	*	mW
Power Supply Rejection: +15VDC			±0.002			*		% FSR/%Vcc
-15VDC			±0.002			*		% FSR/%Vcc
+5VDC			±0.001			*		% FSR/%Vcc
THERMAL CHARACTERISTICS								
Operating Temperature Range	Ambient	-55		+125	-55		+125	°C
Storage Temperature Range	Ambient	-65		+150	-65		+150	°C
Thermal Impedance: Case to Ambient, θ_{CA}			20			*		°C/W
Junction to Case, θ_{JC}			5			*		°C

*Specifications the same as ADC87/MIL.

NOTES:

1/ Trailing edge (logic 1 to logic 0) initiates conversion.

2/ A TTL Load is defined as 40μA max at V_{IN} = 2.4VDC (logic 1), and -1.6mA max at V_{IN} = 0.4VDC (logic 0).

3/ CSB = Complementary Straight Binary; COB = Complementary Offset Binary; CTC = Complementary Two's Complement. Serial and parallel output data is in Nonreturn to Zero (NRZ) format. See Output Coding and Timing Diagram.

4/ Externally adjustable to zero. This specification is without external adjustment.

5/ FSR = Full Scale Range. The ±10V analog input range is a 20V FSR. The ±5V or 0 to 10V input range is a 10V FSR.

6/ Applies to +Full Scale and to -Full Scale.

7/ Gain drift is defined as the absolute value of the change from +25°C to the hot temperature, plus the absolute value of the change from +25°C to the cold temperature, and that quantity divided by the temperature span. This is a 3-point drift. The hot temperature change is usually greater than the cold temperature change.

8/ ±1LSB = ±0.024% FSR.

9/ Conversion time is defined as the width of the status pulse. It is specified using the internal clock, with Clock Rate, pin 17, connected to 0VDC and Short Cycle, pin 14, connected to logic 1.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883 TEST REQUIREMENTS (HYBRID CLASS) / MODELS	ADC87/MIL	ADC87/883B ADC87	ADC87U/883B ADC87U
	Subgroups (see Table III)		
Interim electrical parameters (preburn-in) (method 5008)	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4, 6, 7	1, 2, 3, 4, 6, 7	1, 2U, 3U, 4, 6, 7
Group A test requirements (method 5008)	1, 2, 3, 4, 6, 7	--	--
Group C end point electrical parameters (method 5008)	Table IV delta limits and limits	--	--

*PDA applies to subgroup 1 (see 4.3.d)

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	CONDITIONS 1/	LIMITS ADC87/MIL ADC87/883B ADC87 MIN	LIMITS ADC87/MIL ADC87/883B ADC87 MAX	LIMITS ADC87U/883B ADC87U MIN	LIMITS ADC87U/883B ADC87U MAX	UNITS
1	Zero error, bipolar 2/	±10V range 3/		±10		±14	mV
T_C = +25°C	Full scale error, -FS bipolar 2/	±10V range 3/		±20		±30	mV
	Full scale error, +FS bipolar 2/	±10V range 3/		±20		±30	mV
	Gain error 2/	±10V range		±20		±20	mV
	Linearity error			±1/2		±1/2	LSB
	Differential linearity error 4/			±1/2		±1/2	LSB
	No missing codes		Pass		Pass		Pass/fail
	Internal reference voltage		+6.0	+6.6	+6.0	+6.6	V
	Zero error, unipolar 2/	0 to +10V range 3/	+5	+15	+5	+15	mV
	Full scale error, unipolar 2/	0 to +10V range 3/		±20		±20	mV
	Gain error, unipolar 2/	0 to +10V range		±10		±10	mV
2	Zero error, bipolar	±10V range 3/		±20			mV
T_C = +125°C	Full scale error, -FS bipolar 2/	±10V range 3/		±40			mV
	Full scale error, +FS bipolar 2/	±10V range 3/		±40			mV
	Gain drift	See subgroup 3					
	Linearity error			±1			LSB
	Differential Linearity error			±1			LSB
	No missing codes		Pass				Pass/fail
2U	Zero error, bipolar 2/	±10V range 3/				±30	mV
T_C = +85°C	Full scale error, -FS bipolar 2/	±10V range 3/				±50	mV
	Full scale error, +FS bipolar 2/	±10V range 3/				±50	mV
	Gain drift	See subgroup 3U					
	Linearity error					±1	LSB
	Differential linearity error					±1	LSB
	No missing codes				Pass		Pass/fail
3	Zero error, bipolar 2/	±10V range 3/		±20			mV
T_C = -55°C	Full scale error, -FS bipolar 2/	±10V range 3/		±40			mV
	Full scale error, +FS bipolar 2/	±10V range 3/		±40			mV
	Gain drift	5/		±54			mV
	Linearity error			±1			LSB
	Differential linearity error			±1			LSB
	No missing codes		Pass				Pass/fail
3U	Zero error, bipolar 2/	±10V range 3/				±30	mV
T_C = -25°C	Full scale error, -FS bipolar 2/	±10V range 3/				±50	mV
	Full scale error, +FS bipolar 2/	±10V range 3/				±50	mV
	Gain drift	6/				±33	mV
	Linearity error					±1	LSB
	Differential linearity error					±1	LSB
	No missing codes				Pass		Pass/fail
4							
T_C = +25°C	Conversion time			8		8	µsec
5							
T_C = +125°C	Conversion time			8		8	µsec
6							
T_C = -55°C	Conversion time			8		8	µsec
7	Quiescent current	No load, all bits logic 1					
T_C = +25°C	$+V_{CC}$			45		45	mA
	$-V_{CC}$			45		45	mA
	V_{DD}			50		50	mA
	Power consumption	Quiescent		1500		1500	mW
	Zero adjustment range	±10V range	±60		±60		mV
	Gain adjustment range	±10V range	±100		±100		mV
	MSB inverted output		Pass		Pass		Pass/fail
	Serial output		Pass		Pass		Pass/fail

NOTES:

1/ $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, no load, without the optional buffer amplifier, unless otherwise specified. The internal clock is used. Clock Rate, pin 17, is connected to 0VDC. Short Cycle, pin 14, is connected to logic 1.

2/ Without external adjustment.

3/ For the ±10V range: bipolar +FS is ideally at +9.995117VDC; bipolar zero is ideally at 0.000VDC; bipolar -FS is ideally at -10.000VDC. For the 0 to +10V range: unipolar +FS is ideally at +9.997559VDC; unipolar zero is ideally at 0.000VDC. Refer to Figure 3 and Table VI.

4/ Monotonicity is assured by differential linearity ≤±1LSB.

5/ The absolute value of the gain change from +25°C to +125°C, is added to the absolute value of the gain change from +25°C to -55°C. This provides a 3-point drift.

6/ The absolute value of the gain change from +25°C to +85°C, is added to the absolute value of the gain change from +25°C to -55°C. This provides a 3-point drift.

TABLE IV. Group C, End Point Electrical Parameters.
(T_C = +25°C, $\pm V_{CC}$ = 15VDC, V_{DD} = +5VDC)

TEST	LIMIT	DELTA
Zero error, bipolar	20mV	10mV
+Full scale error, bipolar	30mV	10mV
-Full scale error, bipolar	30mV	10mV
Gain error, bipolar	30mV	10mV
Linearity	1LSB	1/2LSB
Differential linearity	1LSB	1/2LSB

TABLE V. Analog Input Range Selection Connections.

	DIRECT INPUT						BUFFERED INPUT				
Input Range	Input Signal to Pin	Input Impedance	Required External Pin Connections				Input Signal to Pin	Input Impedance	Required External Pin Connections		
±2.5V	24	2.5kΩ	30 to 26	29 open	23 to 22	22 to 25	30	50MΩ	29 to 24	23 to 22	22 to 25
±5V	24	5kΩ	30 to 26	29 open	23 to 22		30	50MΩ	29 to 24	23 to 22	
±10V	25	10kΩ	30 to 26	29 open	23 to 22		30	50MΩ	29 to 25	23 to 22	
0 to +5V	24	2.5kΩ	30 to 26	29 open	23 to 26	22 to 25	30	50MΩ	29 to 24	23 to 26	22 to 25
0 to +10V	24	5kΩ	30 to 26	29 open	23 to 26		30	50MΩ	29 to 24	23 to 26	

TABLE VI. Ideal Analog Input Voltage vs Digital Output Code.

	DIGITAL OUTPUT CODE			
	MSB LSB	MSB LSB	MSB LSB	
Input Range	1111 1111 1111	0111 1111 1111	0000 0000 0000	1LSB
±2.5V	-2.500V	0V	+2.498779V	1.2207mV
±5V	-5.000V	0V	+4.997559V	2.4414mV
±10V	-10.000V	0V	+9.995117V	4.8828mV
0 to +5V	0V	+2.500V	+4.998779V	1.2207mV
0 to +10V	0V	+5.000V	+9.997559V	2.4414mV

NOTE:

Analog voltages are the center of the bit range. Transitions occur 1/2LSB before and 1/2LSB after the bit center.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specified by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1.The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition A, Y_1 axis only.
b. Interim and final electrical test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) T_A = 125°C minimum
   (4) Test duration is 160 hours minimum
d. Percent defective allowable (PDA). The PDA, for the MIL Hi-Rel product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
e. External visual inspection need not include measurement of case and lead dimensions.

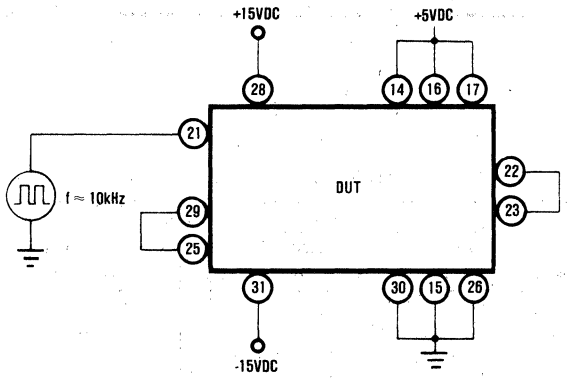


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Group D, subgroup 1, seal test, of MIL-STD-883, method 5008, is performed on each lot of packages procured. Groups C and D inspections (except for subgroup 1, seal test) of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodicaly performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) T_A = 125°C minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirements for certificate of compliance, if desired.

6.4 Definitions.

Full Scale Absolute Accuracy Error. Full scale absolute accuracy error is the difference between the ideal and the actual, unadjusted, analog input voltage at the full scale points. It applies to unipolar plus full scale, bipolar minus full scale, and bipolar plus full scale. Absolute accuracy includes zero, gain, linearity, and noise errors and, when specified over temperature, includes the drifts of these errors. It is measured at the first or last transition, as appropriate. The error is expressed in LSBs or % of FSR.

Bipolar Zero Error. Bipolar zero error is the difference between the ideal and the actual analog input voltage for the digital output code 0111 1111 1111. It is measured at the 1000 0000 0000 to 0111 1111 1111 transition which ideally occurs at 0VDC -1 2LSB.

Bipolar zero error is also known as bipolar major transition error.

Unipolar Zero Error. Unipolar zero error is the difference between the ideal and the actual analog input voltage for the digital output code 1111 1111 1111 (unipolar). It is measured at the 1111 1111 1111 to 1111 1111 1110 transition which ideally occurs at 0VDC +1 2LSB.

Gain Error. Gain error is the difference between the ideal and the actual analog input voltage span. It applies to both unipolar and bipolar input ranges. It is measured between the first transition and the last transition which is ideally FSR -2LSB.

Gain error in some literature describes what is defined herein to be unipolar full scale error and bipolar plus full scale error.

Offset Error. This term is not used with the ADC87. Offset error in some literature describes what is defined herein to be unipolar zero error and/or bipolar minus full scale error.

Linearity Error. Linearity error is the difference between the ideal and the actual bit transition when zero error and gain error equal zero.

Differential Linearity Error. Differential linearity error is the difference between the ideal and the actual bit step width. Zero differential linearity error means each bit step width is 1LSB. A maximum differential linearity error of ±1 2LSB means a bit step width may be between 1/2LSB and 3 2LSB.

Monotonicity. Monotonicity is the condition where the digital output code remains the same or increases for an increasing analog input signal.

Quantization Uncertainty. Quantization uncertainty is the inherent uncertainty of being able to determine the analog voltage which produces a digital code. Because the analog input voltage is divided or quantized into a finite number of bits, each digital code represents an analog voltage span equal to 1LSB. Quantization uncertainty is ±1 2LSB. Its magnitude may be reduced only by using a higher resolution converter.

6.5 Microcircuit group assignment. These microcircuits are Technology Group F as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. APPLICATIONS INFORMATION

7.1 Layout. To produce clean, noise-free, accurate conversions, high frequency layout techniques should be used. Wide, low inductance conductor patterns, short and direct external component leads, power supply decoupling, and a ground plane are recommended. Long runs should be avoided. Coupling and runs, which might cause input-to-output coupling, should be avoided. High impedance points should be given special consideration. The input to the buffer, the comparator input (particularly sensitive) and the external adjustment pins are sensitive. Shielding by Analog Common or ±15VDC supply patterns my be helpful.

7.2 Grounding. A ground plane under the ADC87 is recommended.

Analog Common (pin 26) and Digital Common (pin 15) must be connected together and to the analog system ground. Preferably, connect both commons directly to the ground plane under the ADC87. If these commons must be run separately, use wide conductor patterns and connect a 0.01μF ceramic capacitor between the commons at the unit. The case is connected to Digital Common, pin 15.

7.3 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum capacitor and a 0.01μF ceramic capacitor from each power supply to the ground plane. Locate the capacitors close to the converter.

7.4 Optional External Zero and Gain Adjustments. The ADC87 zero error and gain error are factory laser-trimmed to position the staircase transfer function within Table I specifications. Optionally, two adjustments null zero error and gain error (see Figure 6).

Zero adjustment moves the entire staircase left-to-right. For unipolar ranges, -FS, 0VDC, is nulled. For bipolar ranges, midscale, 0VDC, is nulled. (Alternately, bipolar -FS may be nulled.)

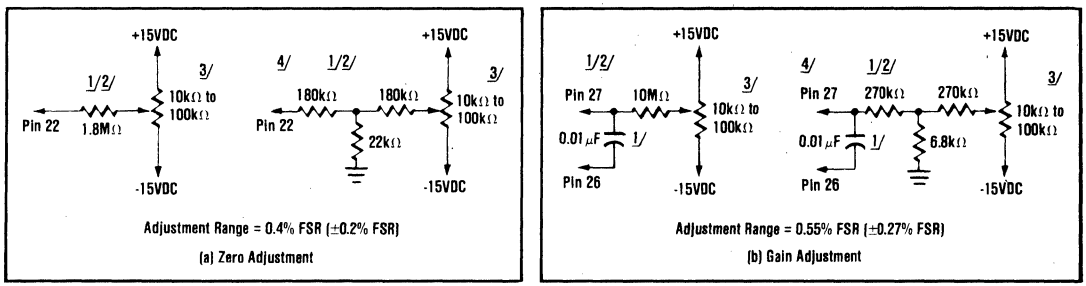
Gain adjustment adjusts the span of the staircase. Adjustment effectively rotates the staircase about -FS. For unipolar and bipolar ranges, zero adjustment should be made first, then +FS error is nulled.

Adjustments should be made after a 10 minute warm-up. Fixed, selected resistors may be substituted for the potentiometers after the adjustments have been determined, if desired. If adjustments are not used, pin 22 (zero adjust) should only be connected as required for analog input range selection and pin 27 (gain adjust) should be either grounded (recommended) or open.

7.4.1 Zero Adjustment Procedure. For the selected unipolar range, apply the analog input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition ideally occurs, 0VDC +1/2LSB. While continuously converting, adjust the zero potentiometer until the transition "flickers".

For the selected bipolar range, apply the analog input voltage at which the 1000 0000 0000 to 0111 1111 1111 transition ideally occurs, 0VDC -1/2LSB. While continuously converting, adjust the zero potentiometer until the transition "flickers".

7.4.2 Gain Adjustment Procedure. Make zero adjustment first. For all input ranges, apply the analog input voltage at which the 0000 0000 0001 to 0000 0000 0000 transition ideally occurs, +FS -3/2LSB. While continuously converting, adjust the gain potentiometer until the transition "flickers". For bipolar ranges, repeat zero and gain adjustments as they are interactive.



Notes:
1/ Locate as close as possible to the converter to minimize noise pickup.
2/ 5% carbon composition or better.
3/ Use multiturn potentiometers with 100ppm/°C TCR or less to minimize drift with temperature.
4/ An attentuator network may be substituted for the series resistor for lower impedance and lower noise susceptibility.

FIGURE 6. Optional External Zero and Gain Adjustment Circuits.

7.5 Start Convert and Status. To start a conversion, a positive pulse with a minimum pulse width of 50nsec must be applied to the Start Convert terminal, pin 21. The trailing edge (falling edge) resets the converter, starts the internal clock and initiates a conversion. The start convert input must remain logic 0 during conversion, as the internal clock is stopped by logic 1 and the output will be erroneous. Another start convert pulse during a conversion does not reset and restart a conversion; it may momentarily stop the internal clock and produce an erroneous output.

Status output, pin 20, is logic 1 during conversion. When a conversion is complete, Status drops to logic 0 and the internal clock is turned off. Refer to the timing diagram, Figure 4.

7.6 Continuous Conversion. The ADC87 will continuously convert, commencing a new conversion immediately after the last conversion, when wired to accept an external clock. See paragraph 7.8 and Timing Considerations, paragraph 3.3.4. Alternately, the internal clock may be used with a new start convert common every 8.7μsec or slower.

7.7 Internal Clock and Clock Rate. The ADC87 is specified and tested using the internal clock. The internal clock is factory adjusted to 1.6MHz with Clock Rate, pin 17, connected to 0VDC (Digital Common). Under these conditions, the ADC87 will meet all the conversion speed and accuracy specifications.

The internal clock frequency may be increased or decreased by applying a positive or negative voltage to Clock Rate, pin 17 (see Figure 7). The circuits shown in Figure 8 may be used. Increasing the clock frequency decreases the conversion time; however, linearity errors increase as shown in Figures 9 and 10. Decreasing the clock frequency is accomplished by using a negative voltage or using an external clock (see paragraph 7.8).

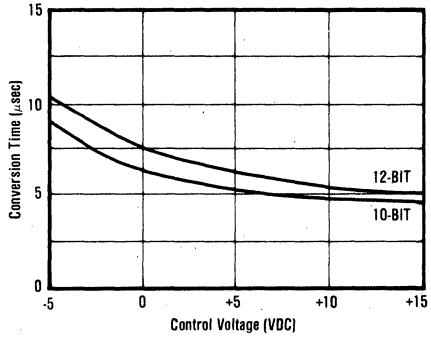
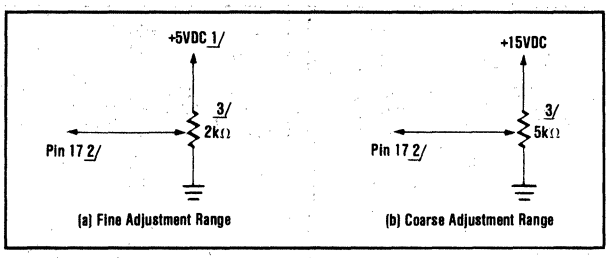


FIGURE 7. Clock Rate Control Voltage.



Notes:
1/ Use negative supply to decrease the clock frequency.
2/ Pin 17 is not connected to 0VDC when using clock rate adjustment potentiometer.
3/ Multiturn potentiometer with 100ppm/°C TCR or less.

FIGURE 8. Clock Rate Adjustment, Optional.

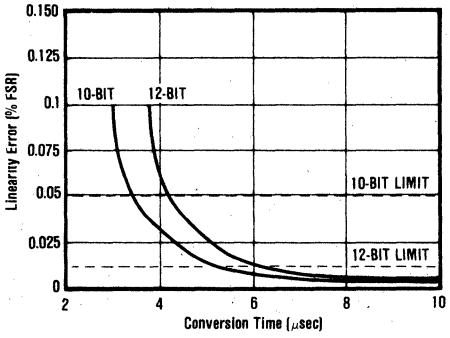


FIGURE 9. Linearity vs Conversion Time.

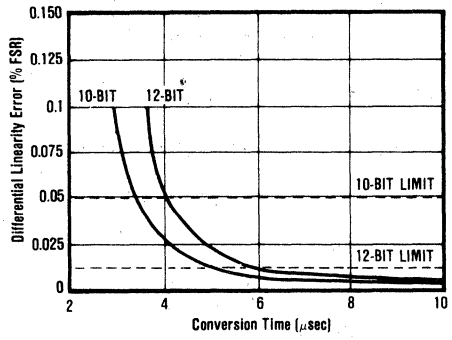


FIGURE 10. Differential Linearity vs Conversion Time.

7.8 External Clock. An external clock may be used with the ADC87 for synchronization or special timing applications. The external clock frequency must be lower than the internal clock frequency. However, the internal clock frequency may be increased; see paragraph 7.7.

The external clock is connected to the Start Convert terminal, pin 21. The normal, start convert positive pulse signal is not required. The external clock must be a negative-going pulse, 100nsec to 200nsec wide, at a frequency lower than the internal clock. The falling edge (leading edge) of the external clock starts the internal clock. The internal clock completes one cycle, then ceases as the Start Convert terminal, pin 21, is logic 1 at that time. The next external clock falling edge turns on the internal clock again, for one cycle. The Clock Output signal, pin 19, displays the internal clock synchronized to the lower, external clock frequency. A conversion is complete and Status output drops to logic 0 after 13 clock pulses.

The converter will provide continuous conversions as long as the external clock signal is present. A conversion is complete when Status output drops to logic 0. Status remains logic 0 for one external clock period. The next conversion starts on the next falling edge of the external clock following conversion completion. Conversions cease when Start Convert input is logic 1.

A circuit to generate an external clock signal from a clock with an arbitrary duty cycle is shown in Figure 11. A circuit to generate an external clock signal from a convert command is shown in Figure 12.

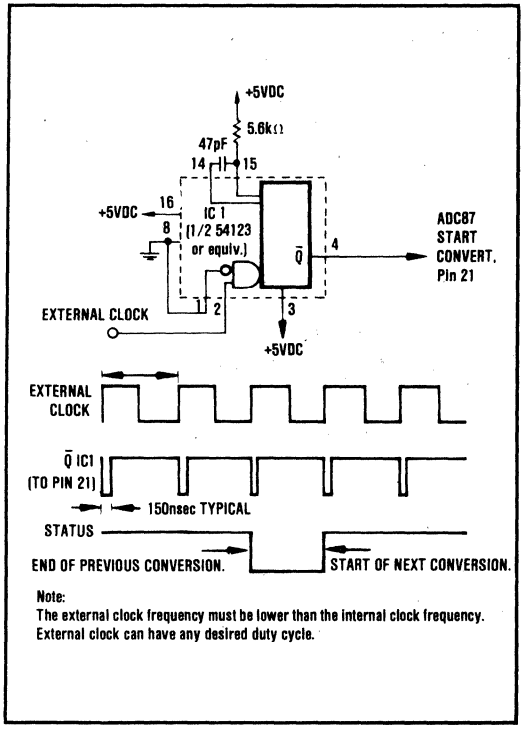


FIGURE 11. Continuous Conversion Using External Clock with Arbitrary Duty Cycle.

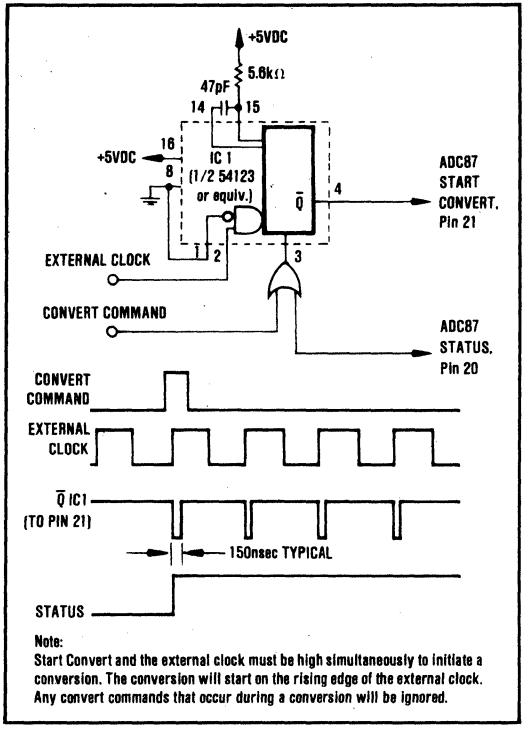


FIGURE 12. Conversion Initiated by Convert Command Using Continuous External Clock.

7.9 Short Cycle. The ADC87 conversion cycle may be stopped prior to converting all 12 bits. This provides faster conversions to less resolution. For conversions to n bits, connect the n + 1 bit output to Short Cycle, pin 14. The remaining bits are truncated.

Figure 13 shows a complete cycle and a short cycle to 10 bits. For 10 bits the internal clock frequency has been increased to provide the minimum conversion time. See Clock Rate, paragraph 7.7.

Resolution (bits)	12	10
Clock Rate connect pin 17 to pin	15	16
Short Cycle connect pin 14 to pin	16	2
Conversion Speed μsec. max	8	5

FIGURE 13. Short Cycle Connections.

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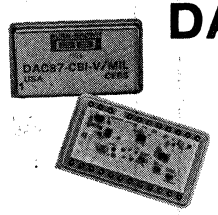


DAC87/MIL SERIES

MODEL NUMBERS:
DAC87-CBI-V/MIL DAC87U-CBI-V/B
DAC87-CBI-V/B DAC87U-CBI-V
DAC87-CBI-V 1/

REVISION D
APRIL, 1984

12-Bit -55°C to +125°C Military DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **HI-REL MANUFACTURE**
- **COMPLETELY SPECIFIED, -55°C to +125°C**
- **ACCURATE**
  - **±1/2LSB max Linearity, over temperature**
  - **±20ppm/°C max Gain Drift**
  - **±0.2% Total Error, over temperature**
  - **Monotonic, over temperature**
- **OPTIONAL MIL-STD-883 SCREENING**
- **DAC85 PIN-COMPATIBLE**
- **COMPLETE - INTERNAL REFERENCE AND OUTPUT AMPLIFIER**

DESCRIPTION

The DAC87/MIL Series is a high performance, 12-bit, TTL-compatible, -55°C to +125°C digital-to-analog converter in a metal, welded, hermetically sealed package, and it is manufactured on a separate hi-rel production line. It is pin-compatible with DAC85 converters and has five user-selected output ranges. Each DAC is a complete device with an internal output amplifier and an ultra-stable reference.

The DAC87/MIL Series is designed for high accuracy, wide temperature applications. The total accuracy without external trim adjustments is ±0.1% of FSR, decreasing to only ±0.3% of FSR over -55°C to +125°C. With external offset and gain trim adjustments at +25°C, the total accuracy is less than ±0.2% of FSR over -55°C to +125°C. Gain drift is less than 20ppm/°C. Linearity error, contributed mostly by the internal current switches and resistive ladder, is reduced by laser trimming to less than ±1/2LSB over temperature. Differential linearity is less than ±1LSB over temperature thereby guaranteeing monotonicity from -55°C to +125°C.

There are two electrical performance grades and three product assurance levels allowing a wide application/budget choice. The DAC87-CBI-V model grade features excellent performance from -55°C to +125°C and finds wide military, aerospace, and industrial applications. The DAC87U-CBI-V model grade features excellent performance from -25°C to +85°C, and guarantees specifications from -55°C to +125°C. Applications include test equipment, shipboard, ground support, and shirt-sleeve environments where operation is between -25°C and +85°C but full temperature operation must be assured.

The three product assurance levels available are: standard; /B (100% screened per MIL-STD-883 method 5008, hybrid class, class B); and /MIL (100% screened, plus PDA = 10%, plus Groups A and B testing on each inspection lot, plus Groups C and D performed initially, periodically, and when specified on the customer's purchase order). See paragraph 1.2.2 for more details. Each device is manufactured in a hi-rel environment with clean room conditions which assures "built-in" quality.

1/ Current output models are also available. Contact Burr-Brown.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
DIGITAL-TO-ANALOG CONVERTER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a 12-bit, TTL-compatible, integrated circuit, digital-to-analog converter.

1.2 Part Number. The complete part number is as shown below.

DAC87		—	CBI	—	V	MIL
Basic model number	Grade (see 1.2.1)		Input coding (Complementary Binary)		Voltage output 1/	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, digital-to-analog converter. The input coding is complementary binary. The device may be externally pin-connected for either Complementary Straight Binary (CSB) or Complementary Offset Binary (COB) coding (see Tables V and VI).

There are two electrical performance grades. The premium grade has no grade designation in the part number and features specifications and tests from -55°C to +125°C. The U grade has a U grade designation in the part number and features specifications and tests from -25°C to +85°C, and specifications from -55°C to +125°C.

Electrical specifications are shown in Table I; electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel Product Designator	Requirements
MIL	Standard model, plus 100% MIL-STD-883 Class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
	Additional electrical testing is performed in / MIL models.
B	Standard model, plus 100% MIL-STD-883 Class B screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is as defined in Figure 1. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±18VDC
Supply voltage, V_{DD}	0VDC to +18VDC
Data input voltage	-1VDC to +7VDC
Output short circuit duration	Unlimited 2/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60sec)	+300°C
Junction temperature	T_J = 175°C

1/ Current output models are also available. Contact Burr-Brown.
2/ Short circuit may be to ground only. Rating applies to 115°C case temperature or 65°C ambient temperature.

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: +4.75VDC to +5.25VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
24-lead can	Figure 1	1350mW at T_A = 125°C	7°C/W 1/	37°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

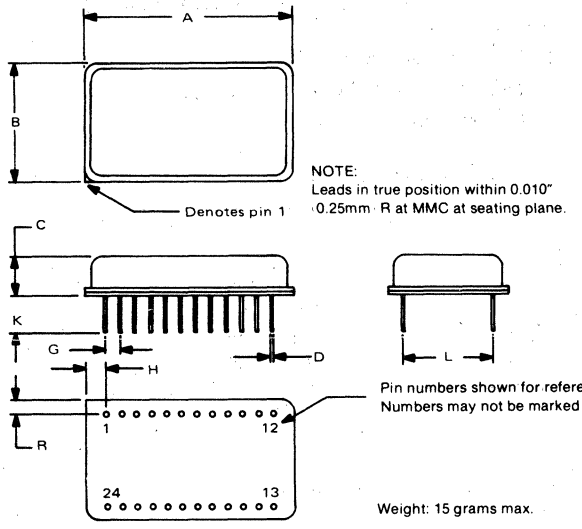
3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1. Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510 except organic and polymeric materials may be used for substrate and die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

FIGURE 1. Case Outline (Double-Wide DIP Configuration).

1/ Rating applies to normal device operation. For the output short circuit condition, the maximum θJ-C of the output die of 100°C/W must be applied to the output short circuit current.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice utilized are glassivated.

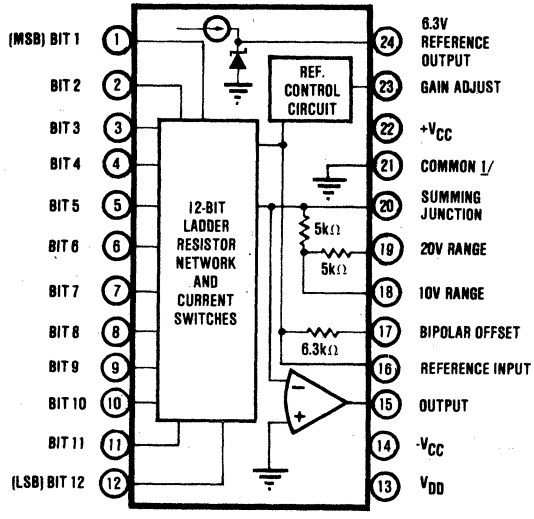
3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Offset and gain error adjustment. The DAC is capable of being externally adjusted to zero offset error and to zero gain error using the circuits in Figure 3. See applications information, paragraph 7.3.

3.3.2 Input coding. The input coding is complementary binary. The digital input code to yield the corresponding output voltage for the output ranges is specified in Table V.

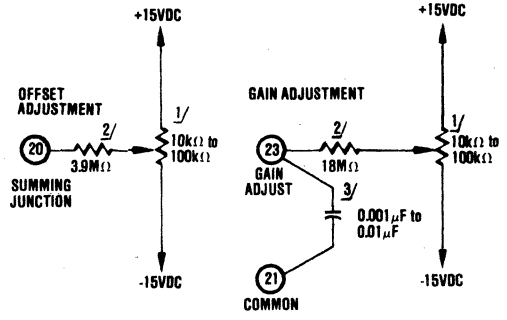
3.3.3 Output range. The output range is specified in Table VI when externally connected as shown therein.

3.4 Electrical test requirements. Electrical test requirements are specified in Table II. The subgroups of Table III and limits of Table IV which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.



1/ Pin 21 is connected to the case.

FIGURE 2. Terminal Connections.



1/ ≤100ppm/°C.
2/ ±20% carbon composition or better. Locate close to the DAC87 to prevent noise pickup.
3/ Ceramic.

FIGURE 3. Offset and Gain Error Adjustment Circuits.

TABLE I. Electrical Performance Characteristics.

CHARACTERISTICS	CONDITIONS 1/	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MIN	TYP	MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	TYP	MAX	UNITS 2/
RESOLUTION		12			12			Bits
DIGITAL INPUTS								
Input voltage								
Logic "1"	T_A = +25°C	2.0		5.5	*		*	V
	-55°C ≤ T_A ≤ +125°C	2.4		5.5	*		*	V
Logic "0"	T_A = +25°C	0		0.8	*		*	V
	-55°C ≤ T_A ≤ +125°C	0		0.4	*		*	V
Input Current								
Logic "1"	V_{IN} = 2.4V			+40			*	μA
Logic "0"	V_{IN} = 0.4V	-1.6		0	*		*	mA
ACCURACY								
Total error, untrimmed 3/	T_A = +25°C			±0.10			*	% of FSR
Unipolar	-25°C ≤ T_A ≤ +85°C						±0.25	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.30				% of FSR
Bipolar	T_A = +25°C			±0.10			*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.25	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.30				% of FSR
Total error, trimmed 3/ 4/								
Unipolar	T_A = +25°C		±0.006	±0.0122		*	*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.15	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.20				% of FSR
Bipolar	T_A = +25°C		±0.006	±0.0122		*	*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.15	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.20				% of FSR
Linearity error	T_A = +25°C		±0.25	±0.50		±0.25	±0.50	LSB
	-25°C ≤ T_A ≤ +85°C						±0.50	LSB
	-55°C ≤ T_A ≤ +125°C			±0.50			±3	LSB
Differential linearity error 5/	T_A = +25°C		±0.50	±0.75		±0.50	±0.75	LSB
	-25°C ≤ T_A ≤ +85°C						±1.0	LSB
	-55°C ≤ T_A ≤ +125°C			±1.0			±3	LSB
Monotonicity temperature range 5/		-55		+125	-25		+85	°C
Offset error 6/								
Unipolar 7/	T_A = +25°C		±0.02	±0.05		±0.02	±0.05	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.068	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.08				% of FSR
Bipolar 7/	T_A = +25°C		±0.02	±0.05		±0.02	±0.05	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.10	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.10				% of FSR
Offset temperature sensitivity 7/								
Unipolar	-25°C to +85°C					±1	±3	ppm of FSR/°C
	-55°C to +125°C		±1	±3				ppm of FSR/°C
Bipolar	-25°C to +85°C						±10	ppm of FSR/°C
	-55°C to +125°C		±5	±10			±30	ppm of FSR/°C
Offset adjustment range		±0.15	±0.2		*	*		% of FSR
Gain error 6/ 8/								
Unipolar 7/	T_A = +25°C		±0.05	±0.10		±0.05	±0.10	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.20	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.25				% of FSR
Bipolar 7/	T_A = +25°C		±0.05	±0.10		±0.05	±0.10	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.20	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.25				% of FSR
Gain temperature sensitivity 7/								
Unipolar	-25°C to +85°C					±10	±20	ppm/°C
	-55°C to +125°C		±10	±20				ppm/°C
Bipolar	-25°C to +85°C					±10	±20	ppm/°C
	-55°C to +125°C		±10	±20			±60	ppm/°C
Gain adjustment range		±0.2	±0.3		*	*		% of FSR
DYNAMIC CHARACTERISTICS								
Slew rate		10	20		*	*		V/μsec
Settling time	ΔV_O = 20V to ±1/2LSB		5	7		*	*	μsec
	ΔV_O = 10V to ±1/2LSB		3	6		*	*	μsec
	ΔV_O = 1LSB to ±1/2LSB		1.5	3		*	*	μsec
ANALOG OUTPUT								
Output voltage range 9/				±10			*	V
Output current 10/		±5			*			mA
Output resistance, DC			0.05	0.2		*	*	Ω
Output short circuit current	T_A = +25°C	±5		±40	*		*	mA

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	CONDITIONS 1/	LIMITS						UNITS 2/
		DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V			DAC87U-CBI-V/B DAC87U-CBI-V			
		MIN	TYP	MAX	MIN	TYP	MAX	
INTERNAL REFERENCE								
Internal reference voltage V_R		±6.0	±6.3	±6.6	*	*	*	V
Internal reference temperature sensitivity	-25°C to +85°C					±5	±10	ppm of V_R/°C
	-55°C to +125°C		±5	±10			±30	ppm of V_R/°C
Output current from internal reference	for specified V_R			200			*	µA
POWER SUPPLY								
Power supply range								
$+V_{CC}$		+14.0	+15	+16.0	*	*	*	V
$-V_{CC}$		-14.0	-15	-16.0	*	*	*	V
V_{DD}		+4.75	+5	+15.5	*	*	*	V
Power supply sensitivity								
$\pm V_{CC}$	$\pm V_{CC}$ = 15V ±0.5V		±0.002	±0.004		*	*	% of FSR/%V_{CC}
V_{DD}	V_{DD} = 5V ±0.25V		±0.001	±0.002		*	*	% of FSR/%V_{DD}
Power supply current (quiescent)								
$\pm V_{CC}$	T_A = +25°C		±20	±30		*	*	mA
	-55°C ≤ T_A ≤ +125°C			±30			*	mA
V_{DD}	T_A = +25°C		20	25		*	*	mA
	-55°C ≤ T_A ≤ +125°C			25			*	mA
TEMPERATURE RANGE								
Operating		-55		+125	*		*	°C
Storage		-65		+150	*		*	°C

*Specification same as DAC87-CBI-V

NOTES:

1/ $\pm V_{CC}$ = 15V, V_{DD} = 5V, -55°C ≤ T_A ≤ +125°C, unless otherwise specified.

2/ FSR = Full Scale Range (Example: The FSR is 20V for ±10V range, 10V for ±5V range, and 10V for 0 to +10V range.) LSB = Least Significant Bit.

3/ Total error includes all errors at any fixed power supply voltage within the recommended supply voltage range, including the internal reference, linearity error, offset error, and gain error.

4/ Offset and gain externally trimmed to zero error at T_A = +25°C.

5/ Monotonicity is assured by testing differential linearity to ±1LSB maximum.

6/ Externally adjustable to zero.

7/ The reference error is included.

8/ The offset error is specified separately and is not included herein.

9/ The output voltage range is determined by external conditions (see Table VI).

10/ Limit is assured by testing output resistance where R_{LOAD} = 2kΩ.

TABLE II. Electrical Test Requirements

(The individual tests within the subgroups appear in Table III)

MODELS / MIL-STD-883 test requirements (hybrid class)	DAC87-CBI-V/MIL	DAC87-CBI-V/B DAC87-CBI-V	DAC87U-CBI-V/B DAC87U-CBI-V
	Subgroups (see Table III)		
Interim electrical parameters (preburn-in) (method 5008)	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4	1, 2, 3	1, 2U, 3U
Group A test requirements (method 5008)	1, 2, 3, 4	--	--
Group C end point electrical parameters (method 5008)	Table IV delta limits and limits	--	--
Additional electrical subgroups performed prior to Group C inspections	2C, 3C, 5, 6	--	--

*PDA applies to subgroup 1 (see 4.3.d)

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragraph 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufactuer's designating symbol (CEBS)
f. Country of origin (U.S.A.)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and trainings, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding, for the MIL Hi-Rel product designation are in accordance with MIL-M-38510.

1 A 4-digit date code, indicating year and week of seal, and a 4- or 5-digit lot identifier is marked on each unit.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for /MIL and/B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, Class B, except as modified in paragraph 4.3 herein.

Screening for the standard model, (none) Hi-Rel product designation, includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle, constant acceleration (condition D), and external visual inspection per MIL-STD-883, method 5008, Class B.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the MIL Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MIN	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MAX	UNITS
1	Offset error, bipolar	4	±10V range (ideal value = -10.000V)		±10		±10	mV
T_A = +25°C	Gain error, bipolar	4	±10V range (ideal value = +9.995117V) 2/		±20		±20	mV
	Linearity error, bipolar	4	±10V range 3/ 4/					
			For + bit errors		+2.44		+2.44	mV
			For - bit errors		-2.44		-2.44	mV
	Differential linearity error, bipolar	4	±10V range 4/ 5/		±3.66		±3.66	mV
	Total error, untrimmed, bipolar	4			±20		±20	mV
	Total error, trimmed, bipolar	6/			--		--	
	Internal reference voltage	4		+6.0	+6.6	+6.0	+6.6	V
	Input voltage	—	Logic "1", all inputs, V_{in} = 5.0VDC to 2.0VDC, measure ΔV_O		±4		±4.8	mV
		—	Logic "0", all inputs, V_{in} = 0VDC to 0.8VDC, measure ΔV_O		±4		±4.8	mV
	Input current	—	Logic "1", each input, V_{in} = +2.4VDC		+40		+40	µA
		—	Logic "0", each input, V_{in} = +0.4VDC	-1.6	0	-1.6	0	mA
	Power supply current	4	No load $+V_{CC}$		30		30	mA
		4	No load $-V_{CC}$		30		30	mA
		4	No load V_{DD}		25		25	mA
	Output resistance	4	$R_O = \frac{(V_O \text{ no load}) - (V_O \text{ 2k}\Omega \text{ load})}{5\text{mA}}$ *		0.2		0.2	Ω
	Output short circuit current	—	R_{load} = 1Ω, V_O = +FS and -FS	±5	±40	±5	±40	mA
	Power supply sensitivity	4	±10V range, V_O = +FS, ΔV_{CC} = +0.5V and -0.5V		±2.6		±2.6	mV
			±10V range, V_O = +FS, ΔV_{DD} = +0.25V and -0.25V		±2.0		±2.0	mV
	Offset adjustment range	3	±10V range	±30		±30		mV
	Gain adjustment range	3	±10V range	±40		±40		mV
	Offset error, unipolar	4	0 to +10V range (ideal value = 0.00V)		±5		±5	mV
	Gain error, unipolar	4	0 to +10V range (ideal value = +9.997559V) 2/		±10		±10	mV
	Total error, untrimmed, unipolar	4	0 to +10V range		±10		±10	mV
2	Offset error, bipolar (V_{OE})	4	±10V range (ideal value = -10.000V)		±20			mV
T_A = +125°C	Gain error, bipolar (G_E)	4	±10V range (ideal value = +9.995117V) 2/		±50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE125} - V_{OE25}}{100°C}$		±0.20			mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E125} - G_{E25}}{100°C}$		±0.40			mV/°C
	Linearity error, bipolar	4	±10V range, 3/ 4/					
			For + bit errors		+2.44			mV
			For - bit errors		±2.44			mV
	Differential linearity error, bipolar	4	±10V range 4/ 5/		±4.88			mV
	Total error, untrimmed, bipolar	4	±10V range		±60			mV

*V_O = +full scale

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MIN	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MAX	UNITS
	Total error, trimmed, bipolar	4	±10V range 7/		+40			mV
	Internal reference voltage	4		+6.0	+6.6			V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R125} - V_{R25}}{100°C}$		±63			µV/°C
2C T_A = +125°C	Power supply current	4	No load +V_{CC}		30			mA
		4	No load -V_{CC}		30			mA
		4	No load V_{DD}		25			mA
2U T_A = +85°C	Offset error, bipolar (V_{OE})	4	±10V range (ideal value = -10.000V				+20	mV
	Gain error, bipolar (G_E)	4	±10V range (ideal value = +9.995117V 2/				±40	mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE85} - V_{OE25}}{60°C}$				+0.20	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{GE}}{\Delta T} = \frac{G_{E85} - G_{E25}}{60°C}$				+0.40	mV/°C
	Linearity error, bipolar	4	±10V range, 3/ 4/					
			For + bit errors				+2.44	mV
			For - bit errors				-2.44	mV
	Differential linearity error, bipolar	4	±10V range 4/ 5/				+4.88	mV
	Total error, untrimmed, bipolar	4	±10V range				+50	mV
	Total error, trimmed, bipolar	4	±10V range 7/				+30	mV
	Internal reference voltage	4				+6.0	+6.6	V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R85} - V_{R25}}{60°C}$				±63	µV/°C
3 T_A = -55°C	Offset error, bipolar	4	±10V range (ideal value = -10.000V		+20			mV
	Gain error, bipolar	4	±10V range (ideal value = +9.995117V 2/		+50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-55}}{80°C}$		+0.20			mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-55}}{80°C}$		+0.40			mV/°C
	Linearity error, bipolar	4	±10V range 3/ 4/					
			For + bit errors		+2.44			mV
			For - bit errors		-2.44			mV
	Differential linearity error, bipolar	4	±10V range 4/ 5/		+4.88			mV
	Total error, untrimmed bipolar	4	±10V range		+60			mV
	Total error, trimmed bipolar	4	±10V range 7/		+40			mV
	Internal reference voltage	4		+6.0	+6.6			V
	Internal reference temperature sensitivity		$\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R\ 55}}{80°C}$		±63			µV/°C
3C T_A = -55°C	Power supply current	4	No load +V_{CC}		30			mA
		4	No load -V_{CC}		30			mA
		4	No load V_{DD}		25			mA
3U T_A = -25°C	Offset error, bipolar	4	±10V range (ideal value = -10.000V)				+20	mV
	Gain error, bipolar	4	±10V range (ideal value = +9.995117V 2/				+40	mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-25}}{50°C}$				+0.20	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-25}}{50°C}$				+0.40	mV/°C
	Linearity error, bipolar	4	±10V range 3/ 4/					
			For + bit errors				+2.44	mV
			For - bit errors				-2.44	mV
	Differential linearity error, bipolar	4	±10V range 4/ 5/				+4.88	mV
	Total error, untrimmed bipolar	4	±10V range				+50	mV
	Total error, trimmed bipolar	4	+10V range 7/				+30	mV
	Internal reference voltage	4				+6.0	+6.6	V
	Internal reference temperature sensitivity		$\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R\ 25}}{50°C}$				±63	µV/°C

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS				UNITS
				DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V		DAC87U-CBI-V/B DAC87U-CBI-V		
				MIN	MAX	MIN	MAX	
4 T_A = +25°C	Settling time Slew rate	5 5	To ±1/2LSB, ΔV_O = 20V ΔV_O = 20V, 10% to 90%	 10	7			µsec V/µsec
5 T_A = +125°C	Settling time Slew rate	5 5	To ±1/2LSB, ΔV_O = 20V ΔV_O = 20V, 10% to 90%	 10	7			µsec V/µsec
6 T_A = -55°C	Settling time Slew rate	5 5	To ±1/2LSB, ΔV_O = 20V V_O = 20V, 10% to 90%	 10	7			µsec V/µsec

NOTES:
1/ $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, Logic 1 = 4V, Logic 0 = 0.2V, no load, unless otherwise specified.
2/ Offset error corrected to zero.
3/ The individual bit errors that are positive are switched on and compared to 1/2LSB. The individual bit errors that are negative are switched on and compared to 1/2LSB. This guarantees ±1/2LSB maximum linearity error.
4/ Offset error and gain error correction factors for the Device Under Test (DUT), if any, are applied to the DUT output voltage before comparing the DUT output voltage to the ideal output voltage. This is the basis for linearity error and differential linearity error relative to a straight line through the end points of the transfer function.
5/ Differential linearity error is tested at all combinations of the four most significant bits.
6/ Total error, trimmed, (bipolar) is the same as linearity error, bipolar.
7/ Offset and gain errors adjusted to zero at T_A = +25°C.

TABLE IV. Group C, End Point Electrical Parameters.
(T_A = +25°C, $\pm V_{CC}$ = 15VDC, V_{DD} = +5VDC)

Test	Limit	Delta
Total error, untrimmed, bipolar	±0.15% of FSR	±0.12% of FSR
Linearity error, bipolar	±1.0LSB	±0.75LSB
Differential linearity error, bipolar	+1.2LSB, -1.0LSB	±0.6LSB
Monotonicity	Yes	--
Offset error, bipolar	±0.125% of FSR	±0.10% of FSR
Gain error, bipolar	±0.25% of FSR	±0.25% of FSR

TABLE V. Ideal Output Voltage vs Digital Input Code.

Output Range	Digital Input Code (Complementary 12-Bit Binary)		
	1111 1111 1111	0111 1111 1111	0000 0000 0000
-2.5V to +2.5V	-2.500V	0	+2.498779V
-5V to +5V	-5.000V	0	+4.997559V
-10V to +10V	-10.000V	0	+9.995117V
0 to +5V	0	+2.500V	+4.998779V
0 to +10V	0	+5.000V	+9.997559V

NOTES:
1. One LSB = 1.2207mV for a 5-volt full scale range. One LSB = 2.4414mV for a 10-volt full scale range. One LSB = 4.8828mV for a 20-volt full scale range.
2. Digital input codes are shown with the MSB listed first.

TABLE VI. Output Range Selection.

Output Range	Required External Pin Connections			
-2.5V to +2.5V	15 to 18	17 to 20	19 to 20	16 to 24
-5V to +5V	15 to 18	17 to 20	19 NC	16 to 24
-10V to +10V	15 to 19	17 to 20	19 to 15	16 to 24
0 to +5V	15 to 18	17 to 21	19 to 20	16 to 24
0 to +10V	15 to 18	17 to 21	19 NC	16 to 24

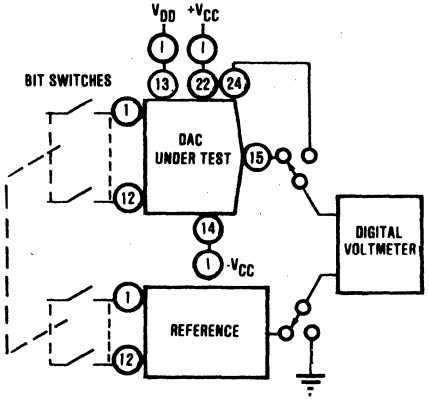


FIGURE 4. Test Circuit—Simplified.

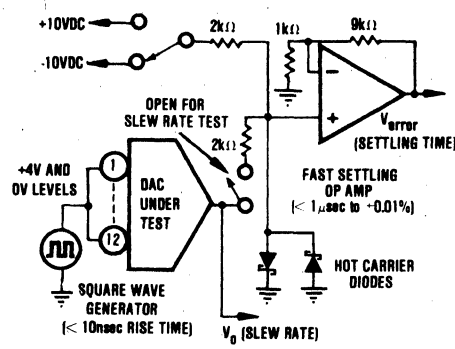


FIGURE 5. Slew Rate and Settling Time Test Circuit.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, medhod 5008, except as modifed herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, Class B, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.
b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 6 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

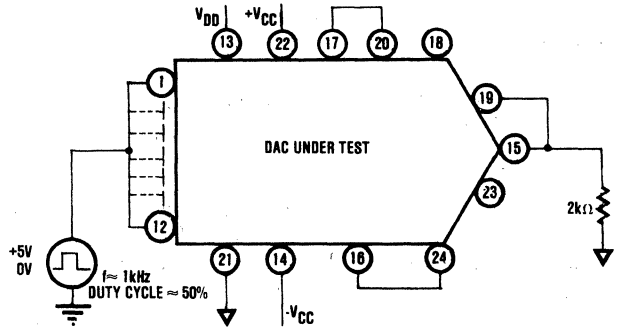


FIGURE 6. Test Circuit—Burn-in and Operating Life Test.

d. Percent defective allowable (PDA). The PDA, for /MIL Hi-Rel product designations only, is 10 percent and includes both parametric and catastropic failures. It is based on failures from group A, subgroup 1 test after

cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 6 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Offset error. Offset error is the difference between the ideal analog output voltage and the actual output voltage, when all the input bits are off (digital input code 1111 1111 1111).

Gain error. Gain error is the difference between the ideal analog output voltage span and the actual output voltage span, between when all the input bits are off (digital input code 1111 1111 1111) and when all the input bits are on (digital input code 0000 0000 0000).

Linearity error. Linearity error is the difference between the ideal analog output voltage and the actual output voltage, when the offset error and the gain error equal zero.

Differential linearity. Differential linearity is the difference between the ideal (1LSB) analog output voltage change, for 1-bit change in digital input code, and the actual output voltage change. A differential linearity of ±1LSB means that the output can change anywhere from 0LSB to 2LSB when the input changes from one adjacent input code to the next. Differential linearity of ±1LSB or less guarantees monotonicity.

Monotonicity. Monotonicity is the condition where the analog output increases or remains the same for an increase in input codes.

Unipolar output. Unipolar is an output characteristic that displays zero volts output at one input extreme and full scale volts output at the other input extreme.

Bipolar output. Bipolar is an output characteristic that displays full scale output voltage at one input extreme and the opposite full scale output voltage at the other input extreme.

6.5 Microcircuit group assignment. These microcircuits are in Technology Group F as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. APPLICATIONS INFORMATION

7.1 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum capacitor from each power supply pin to the ground plane.

7.2 Power supply sensitivity. Power supply sensitivity is specified in Table I. Power supply sensitivity versus ripple frequency is shown in Figure 7.

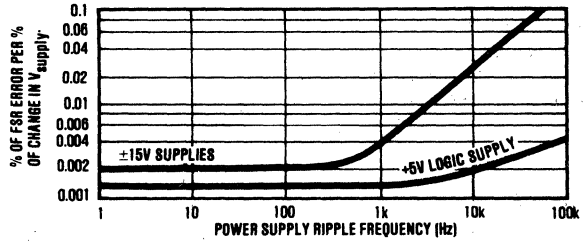


FIGURE 7. Typical Power Supply Sensitivity vs Power Supply Ripple.

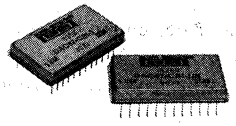
7.3 External offset and gain error adjustment. The untrimmed accuracy of the DAC87/MIL Series is very good and is adequate for many applications. However, when the initial offset and gain errors are greater than what can be allowed in the application, the circuits shown in Figure 3 may be connected and the offset and gain errors adjusted to zero.

7.3.1 Offset adjustment. Apply the digital input code, 1111 1111 1111, which should produce zero volts output for the unipolar ranges, or minus full scale for the bipolar ranges. Adjust the offset potentiometer until the output, for the output range being used, is exactly as depicted in Table V.

7.3.2 Gain adjustment. Apply the digital input code, 0000 0000 0000, which should produce positive full scale. Adjust the gain potentiometer until the output, for the output range being used, is exactly as depicted in Table V.

BURR-BROWN®

DAC87-CBI-I SERIES



MODEL NUMBERS:

DAC87-CBI-I/B	DAC87U-CBI-I/B
DAC87-CBI-I	DAC87U-CBI-I

REVISION NONE
DECEMBER, 1983

12-Bit −55° C to +125° C Military DIGITAL-TO-ANALOG CONVERTER

FEATURES

- HI-REL MANUFACTURE
- COMPLETELY SPECIFIED, −55°C to +125°C
- ACCURATE
  - ±1/2LSB max Linearity, over temperature
  - ±20ppm/°C max Gain Drift
  - ±0.2% Total Error, over temperature
  - Monotonic, over temperature
- OPTIONAL MIL-STD-883 SCREENING
- DAC85 PIN-COMPATIBLE
- COMPLETE—INTERNAL REFERENCE

DESCRIPTION

The DAC87-CBI-I Series is a high performance, 12-bit, TTL-compatible, current output, −55°C to +125°C digital-to-analog converter in a metal, welded, hermetically sealed package, and it is manufactured on a separate hi-rel production line. It is pin-compatible with DAC85 converters and has five user-selected output ranges. Each DAC is a complete device with an internal output amplifier and an ultra-stable reference.

The DAC87-I Series is designed for high accuracy, wide temperature applications. The total accuracy without external trim adjustments is ±0.1% of FSR, decreasing to only ±0.3% of FSR over −55°C to +125°C. With external offset and gain trim adjustments at +25°C, the total accuracy is less than ±0.2% of FSR over −55°C to +125°C. Gain drift is less than 20ppm/°C. Linearity error, contributed mostly by the internal current switches and resistive ladder, is reduced by laser trimming to less than ±1/2LSB over temperature. Differential linearity is less than ±1LSB over temperature thereby guaranteeing monotonicity from −55°C to +125°C.

There are two electrical performance grades and three product assurance levels allowing a wide application/budget choice. The DAC87-CBI-I model/grade features excellent performance from −55°C to +125°C and finds wide military, aerospace, and industrial applications. The DAC87U-CBI-I model/grade features excellent performance from −25°C to +85°C, and guarantees specifications from −55°C to +125°C. Applications include test equipment, shipboard, ground support, and shirt-sleeve environments where operation is between −25°C and +85°C but full temperature operation must be assured.

The two product assurance levels available are standard, and /B (100% screened per MIL-STD-883 method 5008, hybrid class, class B). See paragraph 1.2.2 for more details. Each device is manufactured in a hi-rel environment with clean room conditions which assures "built-in" quality.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION MICROCIRCUITS, LINEAR DIGITAL-TO-ANALOG CONVERTER HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a 12-bit, TTL-compatible, integrated circuit, current output, digital-to-analog converter.

1.2 Part Number. The complete part number is as shown below.

DAC87		CBI	I	B
Basic model number	Grade (see 1.2.1)	Input coding (Complementary Binary)	Current output	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, digital-to-analog converter. The input coding is complementary binary. The device may be externally pin-connected for either Complementary Straight Binary (CSB) or Complementary Offset Binary (COB) coding (see Tables V and VI).

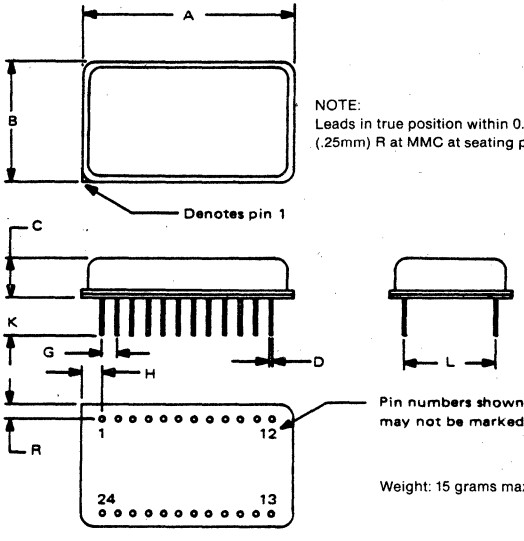
There are two electrical performance grades. The premium grade has no grade designation in the part number and features specifications and tests from −55°C to +125°C. The U grade has a U grade designation in the part number and features specifications and tests from −25°C to +85°C, and specifications from −55°C to +125°C.

Electrical specifications are shown in Table I; electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator position of the part number distinguishes the product assurance levels as follows:

Hi-Rel Product Designator	Requirements
/B	Standard model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is as defined in Figure 1. The case is metal and is conductive.



NOTE:
Leads in true position within 0.010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

Pin numbers shown for reference only. Numbers may not be marked on package.

Weight: 15 grams max.

FIGURE 1. Case Outline (Double-Wide DIP Configuration).

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±18VDC
Supply voltage, V_{DD}	0VDC to +18VDC
Data input voltage	−1VDC to +7VDC
Output short circuit duration	Unlimited 1/
Storage temperature range	−65°C to +150°C
Lead temperature (soldering, 60sec)	+300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: +4.75VDC to +5.25VDC
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
24-lead can	Figure 1	1350mW at T_A = 125°C	7°C/W 2/	37°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510 - Microcircuits, General Specification for.

STANDARD
MILITARY
MIL-STD-883 - Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510 except organic and polymeric materials may be used for substrate and die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice utilized are glassivated.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C, unless otherwise specified.

1/ Short circuit may be to ground only.

2/ Rating applies to normal device operation. For the output short circuit condition, the maximum θJ-C of the output die of 100°C/W must be applied to the output short circuit.

3.3.1 Offset and gain error adjustment. The DAC is capable of being externally adjusted to zero offset error and to zero gain error using the circuits in Figure 3. See applications information, paragraph 7.3.

3.3.2 Input coding. The input coding is complementary binary. The digital input code to yield the corresponding output current for the output ranges is specified in Table V.

3.3.3 Output range. The output range is specified in Table VI and Figures 4 and 5 when externally connected as shown therein.

3.4 Electrical test requirements. Electrical test requirements are specified in Table II. The subgroups of Table III and limits of Table IV which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.

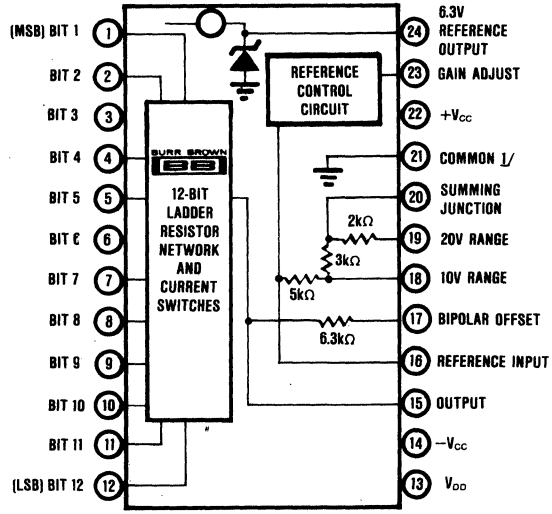
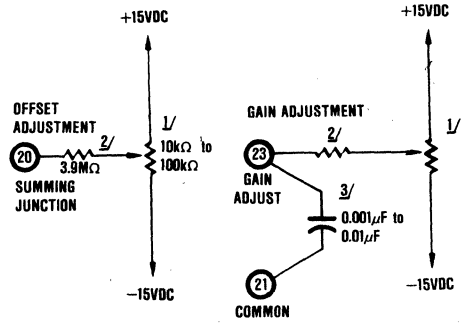


FIGURE 2. Terminal Connections.

1/ Pin 21 is connected to the case.



1/ ≤100ppm/°C.
2/ ±20% carbon composition or better. Locate close to the DAC87 to prevent noise pickup.
3/ Ceramic.

FIGURE 3. Offset and Gain Error Adjustment Circuits.

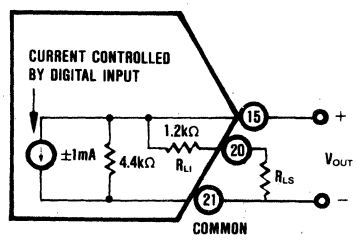


FIGURE 4. Alternate 1 Output Range Selection (Output Voltage with Resistive Load.)

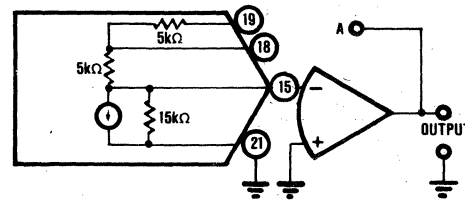


FIGURE 5. Alternate 2 Output Range Selection.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragrpah 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin (U.S.A.)

1/ A 4-digit date code, indicating year and week of seal, and a 4- or 5-digit lot identifier is marked on each unit.

TABLE I. Electrical Performance Characteristics.

CHARACTERISTICS	CONDITIONS 1/	LIMITS						UNITS 2/
		DAC87-CBI-I/B DAC87-CBI-I			DAC87U-CBI-I/B DAC87U-CBI-I			
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION		12			12			Bits
DIGITAL INPUTS								
Input voltage								
Logic "1"	$T_A = +25°C$	2.0		5.5	*		*	V
	$-55°C \le T_A \le +125°C$	2.4		5.5	*		*	V
Logic "0"	$T_A = +25°C$	0		0.8	*		*	V
	$-55°C \le T_A \le +125°C$	0		0.4	*		*	V
Input Current								
Logic "1"	$V_{IN} = 2.4V$			+40			*	μA
Logic "0"	$V_{IN} = 0.4V$	−1.6		0	*		*	mA
ACCURACY								
Total error, untrimmed 3/	$T_A = +25°C$			±0.10			*	% of FSR
Unipolar	$-25°C \le T_A \le +85°C$						±0.25	% of FSR
	$-55°C \le T_A \le +125°C$		±0.30				*	% of FSR
Bipolar	$T_A = +25°C$			±0.10			*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.25	% of FSR
	$-55°C \le T_A \le +125°C$			±0.30				% of FSR
Total error, trimmed 3/ 4/								
Unipolar	$T_A = +25°C$		±0.006	±0.0122		*	*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.20				% of FSR
Bipolar	$T_A = +25°C$		±0.006	±0.0122		*	*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.20				% of FSR
Linearity error	$T_A = +25°C$		±0.25	±0.50		*	*	LSB
	$-25°C \le T_A \le +85°C$						±0.50	LSB
	$-55°C \le T_A \le +125°C$			±0.50			±3	LSB
Differential linearity error 5/	$T_A = +25°C$		±0.50	±0.75		*		LSB
	$-25°C \le T_A \le +85°C$						*.0	LSB
	$-55°C \le T_A \le +125°C$			±1.0			±3	LSB
Monotonicity temperature range 5/		−55		+125	−25		+85	°C
Offset error 6/								
Unipolar 7/	$T_A = +25°C$		±0.02	±0.05		*	*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.068	% of FSR
	$-55°C \le T_A \le +125°C$			±0.08				% of FSR
Bipolar 7/	$T_A = +25°C$		±0.02	±0.05		*	*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.10	% of FSR
	$-55°C \le T_A \le +125°C$			±0.10				% of FSR
Offset temperature sensitivity 7/								
Unipolar	−25°C to +85°C					±1	±3	ppm of FSR/°C
	−55°C to +125°C		±1	±3				ppm of FSR/°C
Bipolar	−25°C to +85°C						±10	ppm of FSR/°C
	−55°C to +125°C		±5	±10			±30	ppm of FSR/°C
Offset adjustment range		±0.15	±0.2		*	*		% of FSR
Gain error 6/ 8/								
Unipolar 7/	$T_A = +25°C$		±0.05	±0.10		*	*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.20	% of FSR
	$-55°C \le T_A \le +125°C$			±0.25				% of FSR
Bipolar 7/	$T_A = +25°C$		±0.05	±0.10		*	*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.20	% of FSR
	$-55°C \le T_A \le +125°C$			±0.25				% of FSR
Gain temperature sensitivity 7/								
Unipolar	−25°C to +85°C					±10	±20	ppm/°C
	−55°C to +125°C		±10	±20				ppm/°C
Bipolar	−25°C to +85°C					±10	±20	ppm/°C
	−55°C to +125°C		±10	±20			±60	ppm/°C
Gain adjustment range		±0.2	±0.3		*	*		% of FSR
DYNAMIC CHARACTERISTICS								
Settling time	ΔI_o = 2mA to ±1/2LSB, $R_L = 250\Omega$		200	400		*	*	nsec

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	CONDITIONS 1/	LIMITS						UNITS 2/
		DAC87-CBI-I/B DAC87-CBI-I			DAC87U-CBI-I/B DAC87U-CBI-I			
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUT								
Output current range	9/	−2.1		−1.9	*		*	mA
Output compliance		±2.5			*			V
Output impedance								
Unipolar				15			*	kΩ
Bipolar				4.4			*	kΩ
INTERNAL REFERENCE								
Internal reference voltage V_R		±6.0	±6.3	±6.6	*	*	*	V
Internal reference temperature sensitivity	−25°C to +85°C					±5	±10	ppm of V_R/°C
	−55°C to −125°C		±5	±10			±30	ppm of V_R/°C
Output current from internal reference	for specified V_R			200			*	μA
POWER SUPPLY								
Power supply range								
$+V_{CC}$		+14.0	+15	+16.0	*	*	*	V
$-V_{CC}$		−14.0	−15	−16.0	*	*	*	V
V_{DD}		+4.75	+5	+15.5	*	*	*	V
Power supply sensitivity								
$\pm V_{CC}$	$\pm V_{CC}$ = 15V ±0.5V		±0.002	±0.004		*	*	mA
V_{DD}	V_{DD}= 5V ±0.25V		±0.001	±0.002		*	*	% of FSR/%V_{DD}
Power supply current (quiescent)								
$\pm V_{CC}$	T_A = +25°C		±20	±30		*	*	mA
	−55°C ≤ T_A ≤ +125°C			±30			*	mA
	T_A = −25°C		20	25		*	*	mA
V_{DD}	−55°C ≤ T_A ≤ +125°C			25			*	mA
TEMPERATURE RANGE								
Operating		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C

*Specification same as DAC87-CBI-I

NOTES:
1/ $\pm V_{CC}$ = 15V, V_{DD} = −55°C ≤ T_A ≤ −125°C, unless otherwise specified.
2/ FSR = Full Scale Range (Example: the FSR is 20V for ±10V range, 10V for ±5V range, and 10V for 0 to +10V range). LSB = Least Significant Bit.
3/ Total error includes all errors at any fixed power supply voltage within the recommended supply voltage range, including the internal reference, linearity error, offset error, and gain error.
4/ Offset and gain externally trimmed to zero error at T_A = +25°C.
5/ Monotonicity is assured by testing differential linearity to ±1LSB maximum.
6/ Externally adjustable to zero.
7/ The reference error is included.
8/ The offset error is specified separately and is not included herein.
9/ The output voltage range is determined by external conditions (see Table VI).

TABLE II. Electrical Test Requirements.
(The individual tests within the subgroups appear in Table III).

Models	DAC87-CBI-I/B DAC87-CBI-I	DAC87U-CBI-I/B DAC87U-CBI-I
MIL-STD-883 test requirements (hybrid class)	Subgroups (see Table III)	
Interim electrical parameters (preburn-in)(method 5008)	1	1
Final electrical test parameters (method 5008)	1, 2, 3	1, 2U, 3U
Group A test requirements (method 5008)	—	—
Group C end point electrical parameters (method 5008)	—	—
Additional electrical subgroups performed prior to Group C inspections	—	—

*PDA applies to subgroup 1 (see 4.3.d)

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-I/B DAC87-CBI-I MIN	LIMITS DAC87-CBI-I/B DAC87-CBI-I MAX	LIMITS DAC87U-CBI-I/B DAC87U-CBI-I MIN	LIMITS DAC87U-CBI-I/B DAC87U-CBI-I MAX	UNITS
1	Offset error, bipolar	6	±10V range (ideal value = −10.000V)		±10		*	mV
T_A = +25°C	Gain error, bipolar	6	±10V range (ideal value = +9.995117V) 2/		±20		*	mV
	Linearity error, bipolar	6	±10V range 3/ 4/ For + bit errors		+2.44		*	mV
			For − bit errors		−2.44		*	mV
	Differential linearity error, bipolar	6	±10V range 4/ 5/		±3.66		*	mV
	Total error, untrimmed, bipolar	6			±20		*	mV
	Total error, trimmed, bipolar 6/				—		—	
	Internal reference voltage	6		+6.0	+6.6	*	*	V
	Input voltage	—	Logic "1", all inputs, V_{in} = 5.0VDC to 2.0VDC, measure ΔV_o		±4		±4.8	mV
		—	Logic "0", all inputs, V_{in} = 0VDC to 0.8VDC, measure ΔV_o		±4		±4.8	mV
	Input current	—	Logic "1", each input, V_{in} = +2.4VDC		+40		*	µA
		—	Logic "0", each input, V_{in} = +0.4VDC	−1.6	0	*	*	mA
	Power supply current	6	No load $+V_{CC}$		30		*	mA
		6	No load $-V_{CC}$		30		*	mA
		6	No load V_{DD}		25		*	mA
	Power supply sensitivity	6	±10V range, V_o = +FS, ΔV_{CC} = +0.5V and −0.5V		±2.6		*	mV
			±10V range, V_o = +FS, ΔV_{DD} = +0.25V and −0.25V		±2.0		*	mV
	Offset adjustment range	3	±10V range	±30		*		mV
	Gain adjustment range	3	±10V range	±40		*		mV
	Offset error, unipolar	6	0 to +10V range (ideal value = 0.00V)		±5		*	mV
	Gain error, unipolar	6	0 to +10V range (ideal value = +9.997559V) 2/		±10		*	mV
	Total error, untrimmed, unipolar	6	0 to +10V range		±10		*	mV
2	Offset error, bipolar (V_{OE})	6	±10V range (ideal value = −10.000V)		±20			mV
T_A = +125°C	Gain error, bipolar (G_E)	6	±10V range (ideal value = +9.995117V) 2/		±50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE125} - V_{OE25}}{100°C}$		±0.20			mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E125} - G_{E25}}{100°C}$		±0.40			mV/°C
	Linearity error, bipolar	6	±10V range 3/ 4/ For + bit errors		+2.44			mV
			For − bit errors		±2.44			mV
	Differential linearity error, bipolar	6	±10V range 4/ 5/		±4.88			mV
	Total error, untrimmed, bipolar	6	±10V range		±60			mV
	Total error, trimmed, bipolar	6	±10V range 7/		±40			mV
	Internal reference voltage	6		+6.0	+6.6			V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R125} - V_{R25}}{100°C}$		±63			µV/°C
2C	Power supply current	6	No load $+V_{CC}$		30			mA
T_A = +125°C		6	No load $-V_{CC}$		30			mA
		6	No load V_{DD}		25			mA
2U	Offset error, bipolar (V_{OE})	6	±10V range (ideal value = −10.000V)				±20	mV
T_A = +85°C	Gain error, bipolar (G_E)	6	±10V range (ideal value = +9.995117V) 2/				±40	mV
	Offset temperature sensitivity, bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE85} - V_{OE25}}{60°C}$				±0.20	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{GE}}{\Delta T} = \frac{G_{E85} - G_{E25}}{60°C}$				±0.40	mV/°C
	Linearity error, bipolar	6	±10V range 3/ 4/ For + bit errors				+2.44	mV
			For − bit errors				+2.44	mV
	Differential linearity error, bipolar	6	±10V range 4/ 5/				±4.88	mV
	Total error, untrimmed, bipolar	6	±10V range				±50	mV
	Total error, trimmed, bipolar	6	±10V range 7/				+30	mV
	Internal reference voltage	6				+6.0	+6.6	V
	Internal reference temperature sensitivity	— —	±10V range, $\frac{\Delta V_R}{\Delta T} = \frac{V_{R85} - V_{R25}}{60°C}$				±63	µV/°C

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-I/B DAC87-CBI-I MIN	LIMITS DAC87-CBI-I/B DAC87-CBI-I MAX	LIMITS DAC87U-CBI-I/B DAC87U-CBI-I MIN	LIMITS DAC87U-CBI-I/B DAC87U-CBI-I MAX	UNITS
3 $T_A = -55°C$	Offset error, bipolar	6	±10V range (ideal value = −10.000V)		±20			mV
	Gain error, bipolar	6	±10V range (ideal value = +9.995117V) 2/		±50			mV
	Offset temperature sensitivity, bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-55}}{80°C}$		±0.20			mV/°C
	Gain temperature sensitivity, bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-55}}{80°C}$		±0.40			mV/°C
	Linearity error, bipolar	6	±10V range 3/ 4/ For + bit errors For − bit errors		+2.44 −2.44			mV mV
	Total error, untrimmed bipolar	6	±10V range		±60			mV
	Total error, trimmed bipolar	6	±10V range 7/		±40			mV
	Internal reference voltage	6		+6.0	+6.6			V
	Internal reference temperature sensitivity	—	$\frac{V_R}{\Delta T} = \frac{V_{R25} - V_{R55}}{80°C}$		±63			μV/°C
3C $T_A = -55°C$	Power supply current	6	No load $+V_{CC}$		30			mA
		6	No load $-V_{CC}$		30			mA
		6	No load V_{DD}		25			mA
3U $T_A = -25°C$	Offset error, bipolar	6	±10V range (ideal value = −10.000V)		±20			mV
	Gain error, bipolar (G_E)	6	±10V range (ideal value = +9.995117V) 2/				±40	mV
	Offset temperature sensitivity, bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-25}}{50°C}$				±0.20	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-25}}{50°C}$				±0.40	mV/°C
	Linearity error, bipolar	6	±10V range 3/ 4/ For + bit errors For − bit errors				+2.44 −2.44	mV mV
	Differential linearity error, bipolar	6	±10V range 4/ 5/				±4.88	mV
	Total error, untrimmed, bipolar	6	±10V range				±50	mV
	Total error, trimmed, bipolar	6	±10V range 7/				+30	mV
	Internal reference voltage	6				+6.0	+6.6	V
	Internal reference temperature sensitivity	— —	±10V range, $\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R-25}}{50°C}$				±63	μV/°C
4 $T_A = +25°C$	Settling time	7	T_O ±1/2LSB, ΔI_o = 2mA		400			nsec
5 $T_A = +125°C$	Settling time	7	T_O ±1/2LSB, ΔV_o = 20V, ΔI_o = 2mA		400			nsec
6 $T_A = -55°C$	Settling time	7	T_O ±1/2LSB, ΔV_o = 20V, ΔI_o = 2mA		400			μsec

*Specification same as DAC87-CBI-I.

NOTES:

1/ $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, Logic 1 = 4V, Logic 0 = 0.2V, no load, unless otherwise specified.

2/ Offset error corrected to zero.

3/ The individual bit errors that are positive are switched on and compared to 1/2LSB. The individual bit errors that are negative are switched on and compared to 1/2LSB. This guarantees ±1/2LSB maximum linearity error.

4/ Offset error and gain error correction factors for the Device Under Test (DUT), if any, are applied to the DUT output voltage before comparing the DUT output voltage to the ideal output voltage. This is the basis for linearity error and differential linearity error relative to a straight line through the end points of the transfer function.

5/ Differential linearity error is tested at all combinations of the four most significant bits.

6/ Total error, trimmed, (bipolar) is the same as linearity error, bipolar.

7/ Offset and gain errors adjusted to zero at $T_A = +25°C$.

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and trainings, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding, for the /MIL Hi-Rel product designation are in accordance with MIL-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

TABLE IV. Group C, End Point Electrical Parameters.
(T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC)

Test	Limit	Delta
Total error, untrimmed, bipolar	±0.15% of FSR	±0.12% of FSR
Linearity error, bipolar	±1.0LSB	±0.75LSB
Differential linearity error, bipolar	+1.2LSB, −1.0LSB	±0.6LSB
Monotonicity	Yes	—
Offset error, bipolar	±0.125% of FSR	±0.10% of FSR
Gain error, bipolar	±0.25% of FSR	±0.25% of FSR

TABLE V. Ideal Output Current vs Digital Input Code.

Output Range	Digital Input Code (Complementary 12-Bit Binary)		
	1111 1111 1111	0111 1111 1111	0000 0000 0000
0 to −2mA	0.0000mA	−1.0000mA	−1.9995mA
±1mA	+1.0000mA	0.0000mA	−0.9995mA

NOTES:
1/ One LSB = 0.488μA.
2/ Digital input codes are shown with the MSB listed first.

TABLE VI. Output Range Selection.

Output Range	Required External Pin Connections				
0 to −2mA 1/	16 to 24	17 to 21	18 NC	19 NC	20 NC
+1mA to −1mA 1/	16 to 24	17 to 15	18 NC	19 NC	20 NC
Alternate 1 Output Range Selection 2/					
0 to −2V	16 to 24	17 to 21	105Ω 1/ between 18 and 21	19 to 18	20 to 15
+1V to −1V	16 to 24	17 to 15	18 to 15	19 to 18	90.9Ω 1/ between 20 and 21
Alternate 2 Output Range Selection 3/ 4/					
−2.5 V to +2.5V	16 to 24	17 to 15	18 to A	19 to 15	20 NC
−5V to +5V	16 to 24	17 to 15	18 to A	19 NC	20 NC
−10V to +10V	16 to 24	17 to 15	18 NC	19 to A	20 NC
0 to +5V	16 to 24	17 to 21	18 to A	19 to 15	20 NC
0 to +10V	16 to 24	17 to 21	18 to A	19 NC	20 NC

NOTES:
1/ ±5%.
2/ External 1% metal film resistor required.
3/ External operational amplifiers (Burr-Brown 3510VM/MIL or equivalent) required (see Figure 5).
4/ Burr-Brown DAC87-CBI-V/MIL provides these output range selections and contains an integral operational amplifier.

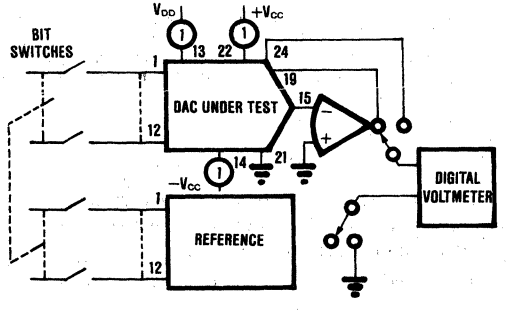


FIGURE 6. Test Circuit—Simplified.

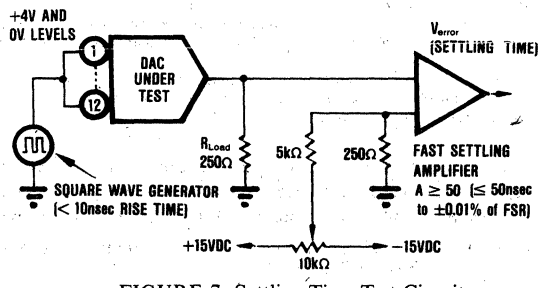


FIGURE 7. Settling Time Test Circuit.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for /B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

Screening for the standard model, (none) Hi-Rel product designation, includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle, constant acceleration (condition D), and external visual inspection per MIL-STD-883, method 5008, hybrid class.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

4.3 Screening. Screening for the /B Hi-Rel product designation is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883), method 2001) is test condition B, Y_1 axis only.
b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 8 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum
d. External visual inspection need not include measurement of case and lead dimensions.

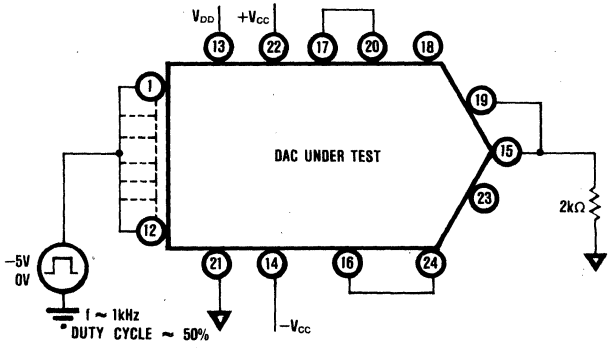


FIGURE 8. Test Circuit—Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspection of MIL-STD-883, method 5008, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 8 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:
   a. Complete part number (see paragraph 1.2)
   b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Offset error. Offset error is the difference between the ideal analog output voltage and the actual output voltage, when all the input bits are off (digital input code 1111 1111 1111).

Gain error. Gain error is the difference between the ideal analog output voltage span and the actual output voltage span, between when all the input bits are off (digital input code 1111 1111 1111) and when all the input bits are on (digital input code 0000 0000 0000).

Linearity error. Linearity error is the difference between the ideal analog output voltage and the actual output voltage, when the offset error and the gain error equal zero.

Differential linearity. Differential linearity is the difference between the ideal (1LSB) analog output voltage change, for 1-bit change in digital input code, and the actual output voltage change. A differential linearity of ±1LSB means that the output can change anywhere from 0LSB to 2LSB when the input changes from one adjacent input code to the next. Differential linearity of ±1LSB or less guarantees monotonicity.

Monotonicity. Monotonicity is the condition where the analog output increases or remains the same for an increase in input codes.

Compliance. Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy.

Unipolar output. Unipolar is an output characteristics that displays zero current output at one input extreme and full scale current output at the other input extreme.

Bipolar output. Bipolar is an output characteristic that displays full scale output current at one input extreme and the opposite full scale output current at the other input extreme.

6.5 Microcircuit group assignment. These microcircuits are in Technology Group F as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. APPLICATIONS INFORMATION

7.1 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum capacitor from each power supply pin to the ground plane.

7.2 Power supply sensitivity. Power supply sensitivity is specified in Table I. Power supply sensitivity versus ripple frequency is shown in Figure 9.

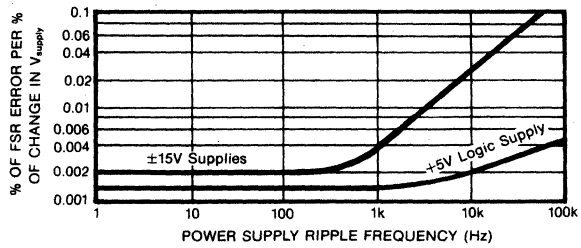


FIGURE 9. Typical Power Supply Sensitivity vs Power Supply Ripple.

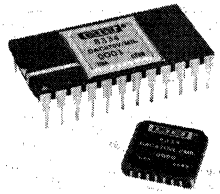
7.3 External offset and gain error adjustment. The untrimmed accuracy of the DAC87/MIL Series is very good and is adequate for many applications. However, when the initial offset and gain errors are greater than what can be allowed in the application, the circuits shown in Figure 3 may be connected and the offset and gain errors may be adjusted to zero.

7.3.1 Offset adjustment. Apply the digital input code, 1111 1111 1111, which should produce zero volts output for the unipolar ranges, or minus full scale for the bipolar ranges. Adjust the offset potentiometer until the output, for the output range being used, is exactly as depicted in Table V.

7.3.2 Gain adjustment. Apply the digital input code, 0000 0000 0000, which should produce positive full scale. Adjust the gain potentiometer until the output, for the output range being used, is exactly as depicted in Table V.

BURR-BROWN®

DAC870/MIL SERIES



MODEL NUMBERS:

DAC870V/MIL	DAC870U/883B
DAC870VL/MIL	DAC870UL/883B
DAC870V/883B	DAC870U
DAC870VL/883B	DAC870UL
DAC870V	
DAC870VL	

REVISION NONE
OCTOBER, 1983

12-Bit −55°C to +125°C Military DIGITAL-TO-ANALOG CONVERTER

FEATURES

- HI-REL MANUFACTURE
- COMPLETELY SPECIFIED, −55°C to +125°C
- ACCURATE
  - ±1/2LSB max Linearity, over temperature
  - ±25ppm/°C max Gain Drift
  - ±0.3% Total Error, over temperature
  - Monotonic, over temperature
- MIL-STD-883 SCREENING
- DAC87 PIN-COMPATIBLE
- COMPLETE—INTERNAL REFERENCE AND OUTPUT AMPLIFIER

DESCRIPTION

The DAC870 Series is a high performance, 12-bit, TTL-compatible, −55°C to +125°C digital-to-analog converter in either a 24-pin ceramic side-brazed package or a 28-terminal leadless chip carrier, and it is manufactured on a separate Hi-Rel production line. It is pin-compatible with DAC87 converters and has five user-selected output ranges. Each DAC is a complete device with an internal output amplifier and an ultra-stable reference.

The DAC870 Series is designed for high accuracy, wide temperature applications. The total accuracy without external trim adjustments is ±0.25% of FSR, decreasing to only ±0.4% of FSR over −55°C to +125°C. With external offset and gain trim adjustments at +25°C, the total accuracy is less than ±0.3% of FSR over −55°C to +125°C. Gain drift is less than 25ppm/°C. Linearity error, contributed mostly by the internal current switches and resistive ladder, is reduced by laser trimming to less than ±1/2LSB over temperature. Differential linearity is less than ±1LSB over temperature, thereby guaranteeing monotonicity from −55°C to +125°C.

There are two electrical performance grades and three product assurance levels, allowing a wide application/budget choice. The DAC870V model/grade features excellent performance from −55°C to +125°C and finds wide military, aerospace, and industrial applications. The DAC870U model/grade features excellent performance from −25°C to +85°C, and guarantees specifications from −55°C to +125°C. Applications include test equipment, shipboard, ground support, and shirt-sleeve environments where operation is between −25°C and +85°C but full temperature operation must be assured.

The three product assurance levels available are: standard; /883B (100% screened per MIL-STD-883 method 5008, class B); and /MIL (100% screened, plus PDA =10%, plus Groups A and B testing on each inspection lot, plus Groups C and D performed initially, periodically, and when specified on the customer's purchase order). See paragraph 1.2.2 for more details. Each device is manufactured in a Hi-Rel environment with clean room conditions which assures "built-in" quality.

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DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
DIGITAL-TO-ANALOG CONVERTER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a 12-bit voltage output digital-to-analog converter hybrid microcircuit.

1.2 Part Number. The complete part number is as shown below.

DAC870	V	L	/MIL
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, voltage output digital-to-analog converter. The input coding is complementary binary. The device may be externally pin-connected for either Complementary Straight Binary (CSB) or Complementary Offset Binary (COB) coding (see Tables V and VI).

There are two electrical performance grades. The V grade designation is the premium grade and features specifications and tests from −55°C to +125°C. The U grade designation features specifications and tests from −25°C to +85°C and operation from −55°C to +125°C.

Electrical specifications are shown in Table I; electrical tests are shown in Tables II and III.

1.2.2 Device class. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

Hi-Rel product designator	Requirements
/MIL	Standard model plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
/883B	Standard model, plus 100% MIL-STD-883 Class B screening.
(NONE)	Standard model including 100% electrical testing.

1.2.3 Case outline. Two case outlines are available.

1.2.3.1 24-pin ceramic side-brazed (DIP). No package identifier is utilized to specify the 24-pin ceramic side-brazed package, which is MIL-M-38510, Appendix C, designator D-3, configuration 3. Figure 1 depicts the case outline for this package type.

1.2.3.2 28-terminal leadless chip carrier (LCC). The "L" package identifier is utilized to specify the 28-terminal square leadless chip carrier package, which is MIL-M-38510, Appendix C, designator C-4. Figure 1 depicts the case outline for this configuration.

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±20VDC
Supply voltage, V_{DD}	0VDC to +18VDC
Data input voltage	−1VDC to +7VDC
Output short circuit duration	Continuous to ground
Storage temperature range	−65°C to +165°C
Lead temperature (soldering, 10sec)	+300°C
Junction temperature	T_J = +165°C

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: ±4.75VDC to +5.25VDC
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C
24-lead DIP	Figure 1	850mW	48°C/W
28-terminal LCC	Figure 1	950mW	42°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510 - Microcircuits, General Specification for.

STANDARD
MILITARY
MIL-STD-883 - Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

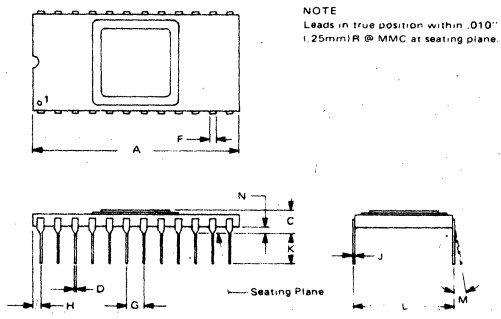
3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

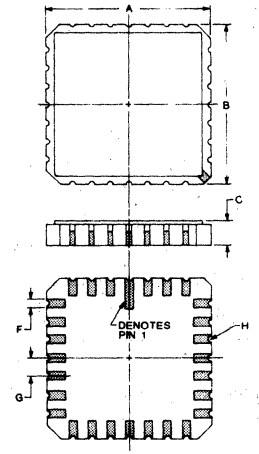
3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	— —	10°	— —	10°
N	.025	.060	0.64	1.52

(a) 24-pin side braze; package ID: (none)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.442	.458	11.23	11.63
B	.442	.458	11.23	11.63
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
H	.008R TYP.		0.20R TYP.	

(b) 28-terminal LCC; package ID: "L"

FIGURE 1. Case Outlines.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections for the ceramic side-brazed package are shown in Figure 2 and the circuit diagram and terminal connections for the leadless chip carrier package are shown in Figure 3.

3.2.8 Glassivation. The microcircuit dice are glassivated.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

3.3.1 Offset and gain error adjustment. The DAC is capable of being externally adjusted to zero offset error and to zero gain error using the circuits in Figure 4. See applications information paragraph 7.3.

3.3.2 Input coding. The input coding is complementary binary. The digital input code to yield the corresponding output voltage for the various output ranges is specified in Table V.

3.3.3 Output range. The output range is specified in Table VI when externally connected as shown therein.

3.4 Electrical test requirements. Electrical test requirements are shown in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.

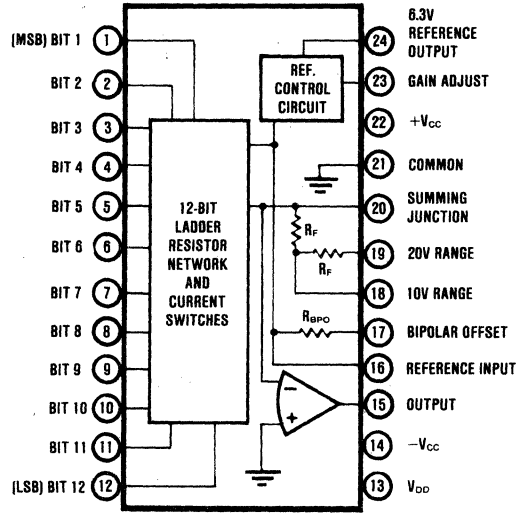


FIGURE 2. Terminal Connections (24-pin Ceramic Side Braze).

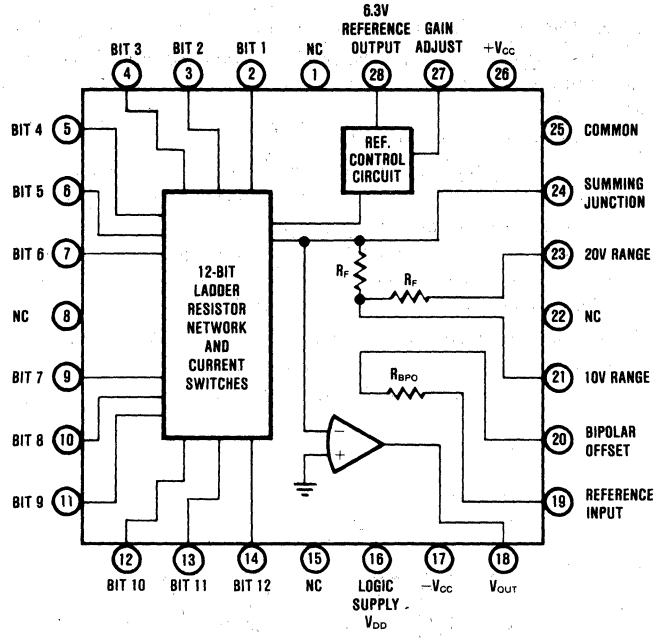
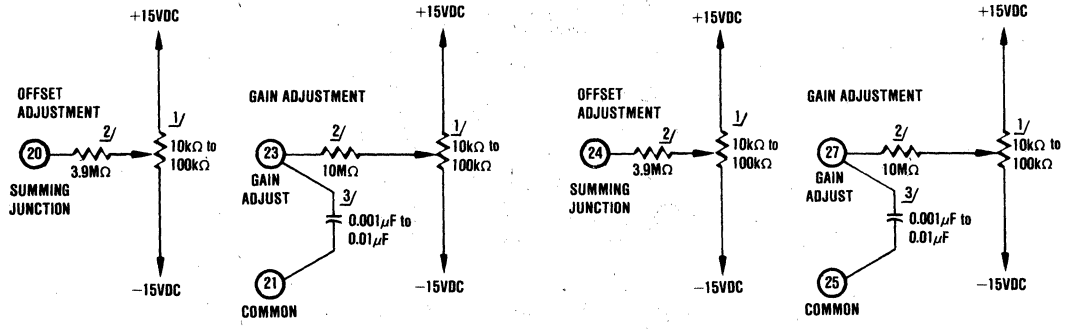


FIGURE 3. Terminal Connections (28-terminal LCC).



1/ ≤100ppm/°C.
2/ ±20% carbon composition or better. Locate close to the DAC870 to prevent noise pickup.
3/ Ceramic.

FIGURE 4. Offset and Gain Error Adjustment Circuits.

TABLE I. Electrical Performance Characteristics.

CHARACTERISTICS	CONDITIONS [1]	LIMITS †DAC870V/MIL DAC870V/883B DAC870V MIN	†DAC870VL/MIL DAC870VL/883B DAC870VL TYP	†DAC870VL/MIL DAC870VL/883B DAC870VL MAX	DAC870U/883B DAC870U MIN	DAC870U/883B DAC870U TYP	DAC870UL/883B DAC870UL MAX	UNITS [2]
RESOLUTION		12			12			Bits
DIGITAL INPUTS								
Input voltage: Logic "1"	$T_A = +25°C$	2.0		5.5	*		*	V
	$-55°C \le T_A \le +125°C$	2.4		5.5	*		*	V
Logic "0"	$T_A = +25°C$	0		0.8	*		*	V
	$-55°C \le T_A \le +125°C$	0		0.4	*		*	V
Input Current: Logic "1"	$V_{IN} = 2.4V$			+40			*	μA
Logic "0"	$V_{IN} = 0.4V$	−1.6		0	*		*	mA
ACCURACY								
Total error, untrimmed [3]: Unipolar	$T_A = +25°C$			±0.25			*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.25	% of FSR
	$-55°C \le T_A \le +125°C$			±0.40				% of FSR
Bipolar	$T_A = +25°C$			±0.25			*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.25	% of FSR
	$-55°C \le T_A \le +125°C$			±0.40				% of FSR
Total error, trimmed [3,4]: Unipolar	$T_A = +25°C$		±0.006	±0.0122		*	*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.30				% of FSR
Bipolar	$T_A = +25°C$		±0.006	±0.0122		*	*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.30				% of FSR
Linearity error	$T_A = +25°C$		±0.25	±0.50		*	*	LSB
	$-25°C \le T_A \le +85°C$						±0.50	LSB
	$-55°C \le T_A \le +125°C$			±0.50			±3	LSB
Differential linearity error [5]	$T_A = +25°C$		±0.50	±0.75		*	*	LSB
	$-25°C \le T_A \le +85°C$						±1.0	LSB
	$-55°C \le T_A \le +125°C$			±1.0			±3	LSB
Monotonicity temperature range [5]		−55		+125	−25		+85	°C
Offset error [6]: Unipolar [7]	$T_A = +25°C$			±0.10			*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.118	% of FSR
	$-55°C \le T_A \le +125°C$			±0.15				% of FSR
Bipolar [7]	$T_A = +25°C$			±0.10			*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.15				% of FSR
Offset temperature sensitivity [7]: Unipolar	−25°C to +85°C						±3	ppm of FSR/°C
	−55°C to +125°C			±3				ppm of FSR/°C
Bipolar	−25°C to +85°C						±15	ppm of FSR/°C
	−55°C to +125°C			±15			±45	ppm of FSR/°C
Gain error [6,8]: Unipolar [7]	$T_A = +25°C$			±0.15			*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.20	% of FSR
	$-55°C \le T_A \le +125°C$			±0.25				% of FSR
Bipolar [7]	$T_A = +25°C$			±0.15			*	% of FSR
	$-25°C \le T_A \le +85°C$						±0.20	% of FSR
	$-55°C \le T_A \le +125°C$			±0.25				% of FSR
Gain temperature sensitivity [7]: Unipolar	−25°C to +85°C						±20	ppm/°C
	−55°C to +125°C			±25				ppm/°C
Bipolar	−25°C to +85°C						±20	ppm/°C
	−55°C to +125°C			±25			±75	ppm/°C
Gain adjustment range		0.15			*			% of FSR
DYNAMIC CHARACTERISTICS								
Slew rate		10			*			V/μsec
Settling time	$\Delta V_O = 20V$ to ±1/2LSB		5	7		*	*	μsec
	$\Delta V_O = 10V$ to ±1/2LSB		3	6		*	*	μsec
	$\Delta V_O = 1LSB$ to ±1/2LSB		1.5	3		*	*	μsec
ANALOG OUTPUT								
Output voltage range [9]				±10			*	V
Output current [10]		±5			*			mA
Output resistance, DC			0.05	0.2		*	*	Ω
Output short circuit current	$T_A = +25°C$	±5		±40	*		*	mA

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	CONDITIONS[1]	LIMITS †DAC870V/MIL DAC870V/883B DAC870V MIN	†DAC870V/MIL DAC870V/883B DAC870V TYP	†DAC870V/MIL DAC870V/883B DAC870V MAX	†DAC870VL/MIL DAC870VL/883B DAC870VL MIN	†DAC870VL/MIL DAC870VL/883B DAC870VL TYP	†DAC870VL/MIL DAC870VL/883B DAC870VL MAX	UNITS[2]
INTERNAL REFERENCE								
Internal reference voltage (V_R)		±6.23	±6.3	±6.37	*	*	*	V
Internal reference temperature sensitivity	−25°C to +85°C						±20	ppm of V_R/°C
	−55°C to +125°C			±25				ppm of V_R/°C
Output current from internal reference	for specified V_R	1.5			*			mA
POWER SUPPLY								
Power supply range: $+V_{CC}$		+13.5	+15	+16.5	*	*	*	V
$-V_{CC}$		−13.5	−15	−16.5	*	*	*	V
V_{DD}		+4.5	+5	+16.5	*	*	*	V
Power supply sensitivity: $\pm V_{CC}$	$\pm V_{CC}$ = 15V ±0.5V		±0.002	±0.004		*	*	% of FSR/%V_{CC}
V_{DD}	V_{DD} = 5V ±0.25V		±0.001	±0.002		*	*	% of FSR/%V_{DD}
Power supply current (quiescent): $+V_{CC}$	−55°C ≤ T_A ≤ +125°C			+12			*	mA
$-V_{CC}$				−25			*	mA
V_{DD} [11]				+10			*	mA
TEMPERATURE RANGE								
Operating		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C

† DAC870V/MIL and DAC870VL/MIL available after March, 1984.
* Specification same as DAC870V.

NOTES:
1/ $\pm V_{CC}$ = 15V, V_{DD} = 5V, −55°C ≤ T_A ≤ +125°C, unless otherwise specified.
2/ FSR = Full Scale Range (Example: The FSR is 20V for ±10V range, 10V for ±5V range, and 10V for 0 to +10V range.) LSB = Least Significant Bit.
3/ Total error includes all errors at any fixed power supply voltage within the recommended supply voltage range, including the internal reference, linearity error, offset error, and gain error.
4/ Offset and gain externally trimmed to zero error at T_A = +25°C.
5/ Monotonicity is assured by testing differential linearity to ±1LSB maximum.
6/ Externally adjustable to zero.
7/ The reference error is included.
8/ The offset error is specified separately and is not included herein.
9/ The output voltage range is determined by external conditions (see Table VI).
10/ Limit is assured by testing output resistance where R_{LOAD} = 2kΩ.
11/ Power dissipation is an additional 100mW, when V_{DD} is operated at +15V.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883 test requirements [hybrid class] \ Models	DAC870V/MIL DAC870VL/MIL	DAC870V/883B DAC870VL/883B DAC870V DAC870VL	DAC870U/883B DAC870UL/883B DAC870U DAC870UL
	Subgroups (see Table III)		
Interim electrical parameters (preburn-in) (method 5008)	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4	1, 2, 3	1, 2U, 3U
Group A test requirements (method 5008)	1, 2, 3, 4	—	—
Group C end point electrical parameters (method 5008)	Table IV delta limits and limits	—	—
Additional electrical subgroups performed prior to Group C inspections	2C, 3C, 5, 6	—	—

*PDA applies to subgroup 1 (see 4.3.d)

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum:

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin (U.S.A.)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /MIL product designation, are in accordance with MIL-M-38510.

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

3.7 Traceability. Traceability for the /MIL product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for /MIL and /883B Hi-Rel product designations is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition E), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

For the /MIL product designations, all microcircuits will have passed the screening requirements prior to qualification of quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /MIL product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS [1]	LIMITS DAC870 "V" Grade MIN	LIMITS DAC870 "V" Grade MAX	LIMITS DAC870 "U" Grade MIN	LIMITS DAC870 "U" Grade MAX	UNITS
1	Offset error, bipolar	5	±10V range (ideal value = −10.000V)		±20		*	mV
T_A = +25°C	Gain error, bipolar	5	±10V range (ideal value = +9.995117V) [2]		±30		*	mV
	Linearity error, bipolar	5	±10V range [3] [4]					
			For + bit errors		+2.44		*	mV
			For − bit errors		−2.44		*	mV
	Differential linearity error, bipolar	5	±10V range [4] [5]		±3.66		*	mV
	Total error, untrimmed, bipolar	5			±50		*	mV
	Total error, trimmed, bipolar				—		—	
	Internal reference voltage	5		+6.23	+6.37	*	*	V
	Input voltage [6]	—	Logic "1", all inputs, V_{in} = 5.0VDC to 2.0VDC, measure ΔV_O		±4		±4.8	mV
		—	Logic "0", all inputs, V_{in} = 0VDC to 0.8VDC, measure ΔV_O		±4		±4.8	mV
	Input current	—	Logic "1", each input, V_{in} = +2.4VDC		+40		*	µA
		—	Logic "0", each input, V_{in} = +0.4VDC	−1.6	0	*	*	mA
	Power supply current	5	No load $+V_{CC}$		12		*	mA
		5	No load $-V_{CC}$		25		*	mA
		5	No load V_{DD}		10		*	mA
	Output resistance	5	$R_o = \frac{(V_O \text{ no load}) - (V_O \text{ 2k}\Omega \text{ load})}{5\text{mA}}$		0.2		*	Ω
	Output short circuit current	—	R_{load} = 1Ω, V_O = +FS and −FS	±5	±40	*	*	mA
	Power supply sensitivity	5	±10V range, V_O = +FS, ΔV_{CC} = +0.5V and −0.5V		±2.6		*	mV
			±10V range, V_O = +FS, ΔV_{DD} = +0.25V and −0.25V		±2.0		*	mV
	Gain adjustment range	4	±10V range	±30		*		mV
	Offset error, unipolar	5	0 to +10V range (ideal value = 0.00V)		±10		*	mV
	Gain error, unipolar	5	0 to +10V range (ideal value = +9.997559V) [2]		±15		*	mV
	Total error, untrimmed, unipolar	5	0 to +10V range		±25		*	mV
2	Offset error, bipolar (V_{OE})	5	±10V range (ideal value = −10.000V)		±30			mV
T_A = +125°C	Gain error, bipolar (G_E)	5	±10V range (ideal value = +9.995117V) [2]		±50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE125} - V_{OE25}}{100°C}$		±0.30			mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E125} - G_{E25}}{100°C}$		±0.50			mV/°C
	Linearity error, bipolar	5	±10V range, [3] [4]					
			For + bit errors		+2.44			mV
			For − bit errors		−2.44			mV
	Differential linearity error, bipolar	5	±10V range [4] [5]		±4.88			mV
	Total error, untrimmed, bipolar	5	±10V range		±80			mV
	Total error, trimmed, bipolar	5	±10V range [7]		±60			mV
	Internal reference voltage	5		+6.23	+6.37			V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R125} - V_{R25}}{100°C}$		±157			µV/°C

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS [1]	LIMITS DAC870 "V" Grade MIN	LIMITS DAC870 "V" Grade MAX	LIMITS DAC870 "U" Grade MIN	LIMITS DAC870 "U" Grade MAX	UNITS
2C $T_A = +125°C$	Power supply current	5 5 5	No load $+V_{CC}$ No load $-V_{CC}$ No load V_{DD}		12 25 10			mA mA mA
2U $T_A = +85°C$	Offset error, bipolar (V_{OE}) Gain error, bipolar (G_E) Offset temperature sensitivity, Bipolar Gain temperature sensitivity, Bipolar Linearity error, bipolar Differential linearity error, bipolar Total error, untrimmed, bipolar Total error, trimmed, bipolar Internal reference voltage Internal reference temperature sensitivity	5 5 — — 5 5 5 5 5 —	±10V range (ideal value = −10.000V) ±10V range (ideal value = +9.995117V) [2] ±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE85} - V_{OE25}}{60°C}$ ±10V range, $\frac{\Delta VG_E}{\Delta T} = \frac{G_{E85} - G_{E25}}{60°C}$ ±10V range, [3] [4] For + bit errors For − bit errors ±10V range [4] [5] ±10V range ±10V range [7] $\frac{\Delta V_R}{\Delta T} = \frac{V_{R85} - V_{R25}}{60°C}$		 +6.23 	 ±0.15 ±0.40 +2.44 −2.44 ±4.88 ±50 ±30 +6.37 ±126	mV mV mV/°C mV/°C mV mV mV mV V µV/°C
3 $T_A = -55°C$	Offset error, bipolar Gain error, bipolar Offset temperature sensitivity, Bipolar Gain temperature sensitivity, Bipolar Linearity error, bipolar Differential linearity error, bipolar Total error, untrimmed, bipolar Total error, trimmed, bipolar Internal reference voltage Internal reference temperature sensitivity	5 5 — — 5 5 5 5 5 —	±10V range (ideal value = −10.000V) ±10V range (ideal value = +9.995117V) [2] ±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-55}}{80°C}$ ±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-55}}{80°C}$ ±10V range, [3] [4] For + bit errors For − bit errors ±10V range [4] [5] ±10V range ±10V range [7] $\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R-55}}{80°C}$	 +6.23 	±30 ±50 ±0.30 ±0.50 +2.44 −2.44 ±4.88 ±80 ±60 +6.37 ±157	 	 	mV mV mV/°C mV/°C mV mV mV mV mV V µV/°C
3C $T_A = -25°C$	Power supply current	5 5 5	No load $+V_{CC}$ No load $-V_{CC}$ No load V_{DD}		12 25 10			mA mA mA
3U $T_A = -55°C$	Offset error, bipolar Gain error, bipolar Offset temperature sensitivity, Bipolar Gain temperature sensitivity, Bipolar Linearity error, bipolar Differential linearity error, bipolar Total error, untrimmed, bipolar Total error, trimmed, bipolar Internal reference voltage Internal reference temperature sensitivity	5 5 — — 5 5 5 5 5 —	±10V range (ideal value = −10.000V) ±10V range (ideal value = +9.995117V) [2] ±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-25}}{50°C}$ ±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-25}}{50°C}$ ±10V range, [3] [4] For + bit errors For − bit errors ±10V range [4] [5] ±10V range ±10V range [7] $\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R-25}}{50°C}$		 +6.23 	±30 ±40 ±0.30 ±0.40 +2.44 −2.44 ±4.88 ±50 ±30 +6.37 ±126	mV mV mV/°C mV/°C mV mV mV mV mV V µV/°C
4 $T_A = +25°C$	Settling Time Slew Rate	6 6	To ±1/2LSB, $\Delta V_O = 20V$ $\Delta V_O = 20V$, 10% to 90%	 10	7 	 	 	µsec V/µsec
5 $T_A = +125°C$	Settling Time Slew Rate	6 6	To ±1/2LSB, $\Delta V_O = 20V$ $\Delta V_O = 20V$, 10% to 90%	 10	7 	 	 	µsec V/µsec
6 $T_A = -55°C$	Settling Time Slew Rate	6 6	To ±1/2LSB, $\Delta V_O = 20V$ $\Delta V_O = 20V$, 10% to 90%	 10	7 	 	 	µsec V/µsec

NOTES:
1/ $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, Logic 1 = 4V, Logic 0 = 0.2V, no load, unless otherwise specified.
2/ Offset error corrected to zero.
3/ The individual bit errors that are positive are switched on and compared to 1/2LSB. The individual bit errors that are negative are switched on and compared to 1/2LSB. This guarantees ±1/2LSB maximum linearity error.
4/ Offset error and gain error correction factors for the Device Under Test (DUT), if any, are applied to the DUT output voltage before comparing the DUT output voltage to the ideal output voltage. This is the basis for linearity error and differential linearity error relative to a straight line through the end points of the transfer function.
5/ Differential linearity error is tested at all combinations of the four most significant bits.
6/ Total error, trimmed, (bipolar) is the same as linearity error, bipolar.
7/ Offset and gain errors adjusted to zero at T_A = +25°C.

TABLE IV. Group C, End Point Electrical Paramters.
(T_A = +25°C, $\pm V_{CC}$ = 15VDC, V_{DD} = +5VDC)

Test	Limit	Delta
Total error, untrimmed, bipolar	±0.25% of FSR	*
Linearity error, bipolar	±0.5LSB	*
Differential linearity error, bipolar	±0.75LSB	*
Monotonicity	Yes	—
Offset error, bipolar	±0.10% of FSR	*
Gain error, bipolar	±0.15% of FSR	*

*Delta limits to be finalized upon completion of qualification.

TABLE V. Ideal Output Voltage vs Digital Input Code.

	Digital Input Code [Complementary 12-Bit Binary]		
Output Range	1111 1111 1111	0111 1111 1111	0000 0000 0000
−2.5V to +2.5V	−2.500V	0	+2.498779V
−5V to +5V	−5.000V	0	+4.997559V
−10V to +10V	−10.000V	0	+9.995117V
0 to +5V	0	+2.500V	+4.998779V
0 to +10V	0	+5.000V	+9.997559V

NOTES:
1. One LSB = 1.2207mV for a 5-volt full scale range. One LSB = 2.4414mV for a 10-volt full scale range. One LSB = 4.8828mV for a 20-volt full scale range.
2. Digital input codes are shown with the MSB listed first.

TABLE VI. Output Range Selection.

24-pin Side Braze Package				
Output Range	Required External Pin Connections			
−2.5V to +2.5V	15 to 18	17 to 20	19 to 20	16 to 24
−5V to +5V	15 to 18	17 to 20	19 NC	16 to 24
−10V to +10V	15 to 19	17 to 20	19 to 15	16 to 24
0 to +5V	15 to 18	17 to 21	19 to 20	16 to 24
0 to +10V	15 to 18	17 to 21	19 NC	16 to 24
28-Terminal LCC Package				
Output Range	**Required External Pin Connections**			
−2.5V to +2.5V	18 to 21	20 to 24	23 to 24	19 to 28
−5V to +5V	18 to 21	20 to 24	23 NC	19 to 28
−10V to +10V	18 to 23	20 to 24	23 to 18	19 to 28
0 to +5V	18 to 21	20 to 25	23 to 24	19 to 28
0 to +10V	18 to 21	20 to 25	23 NC	19 to 28

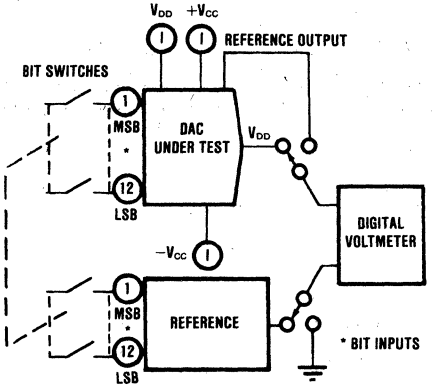


FIGURE 5. Test Circuit—Simplified.

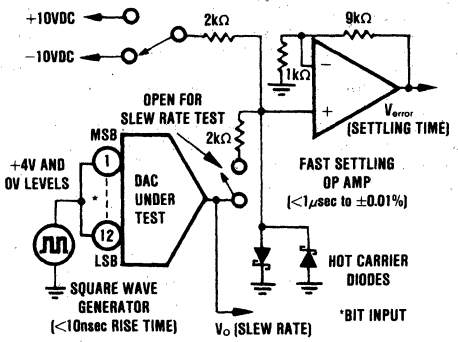


FIGURE 6. Slew Rate and Settling Time Test Circuit.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the /MIL and /883B Hi-Rel product designations is in accordance with MIL-STD-883, method 5008, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.

b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 7 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

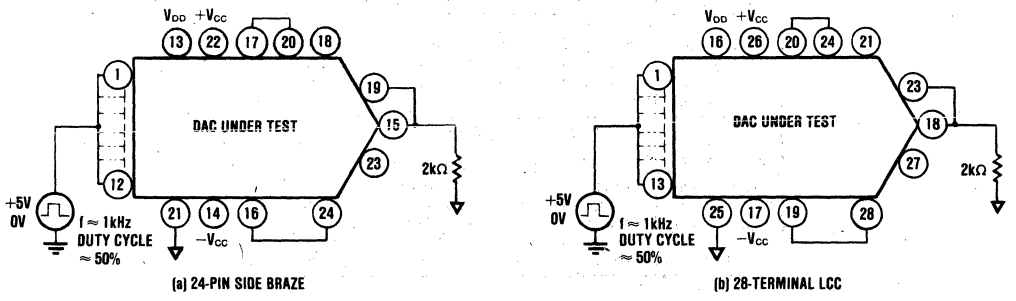


FIGURE 7. Test Circuit-Burn-in and Operating Life Test.

c. Percent defective allowable (PDA). The PDA, for / MIL product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, class B, is performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, class B are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008, class B. A report of the most recent group C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 (class B).

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 (class B), and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 (class B) and as follows:

a. End point electrical parameters are specified in Table IV herein.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Offset error. Offset error is the difference between the ideal analog output voltage and the actual output voltage, when all the input bits are off (digital input code: 1111 1111 1111).

Gain error. Gain error is the difference between the ideal analog output voltage span and the output voltage span, between when all the input bits are off (digital input code: 1111 1111 1111) and when all the input bits are on (digital input code: 0000 0000 0000).

Linearity error. Linearity error is the difference between the ideal analog output voltage and the actual output voltage, when the offset error and the gain error are equal to zero.

Differential linearity. Differential linearity is the difference between the ideal (1LSB) analog output voltage change, for a 1-bit change in digital input code and the actual output voltage change. A differential linearity of ±1LSB means that the output can change anywhere from 0LSB to 2LSB when the input changes from one adjacent input code to the next. Differential linearity of ±1LSB or less guarantees monotonicity.

Monotonicity. Monotonicity is the condition where the analog output increases or remains the same for a 1LSB increase in input codes.

Unipolar output. Unipolar is an output characteristic that displays zero volts output at one input extreme and full scale volts output at the other extreme.

Bipolar output. Bipolar is an output characteristic that displays full scale output voltage at one input extreme and the opposite full scale output voltage at the other input extreme.

6.5 Microcircuit group assignment. These microcircuits are assigned to Technology Group I as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

7. APPLICATION INFORMATION

7.1 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum or electrolytic capacitor from each power supply pin to the ground plane. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

7.2 Power Supply Sensitivity. Power supply sensitivity is specified in Table I. Power supply sensitivity versus ripple frequency is shown in Figure 8.

7.3 External offset and gain error adjustment. The untrimmed accuracy of the DAC870 series is very good and is adequate for many applications. However, when the initial offset and gain errors are greater than what can be allowed in the application, the circuits shown in Figure 4 can be utilized to adjust the offset and gain errors to zero.

7.3.1 Offset adjustment. Apply the digital input code, 1111 1111 1111, which should produce zero volts output for the unipolar ranges, or minus full scale for the bipolar ranges. Adjust the offset potentiometer until the output, for the output range employed, is exactly the value indicated in Table V.

7.3.2 Gain adjustment. Apply the digital input code, 0000 0000 0000, which should produce positive full scale. Adjust the gain potentiometer until the output is exactly as depicted in Table V for the output range being utilized.

7.4 Reference supply. All models of the DAC870 are supplied with an internal 6.3V reference voltage supply. This voltage has a tolerance of ±1% and must be connected to the Reference Input for specified operation. This reference may be used externally also. The external current drain is limited to sourcing 2.5mA up to +85°C and 1mA up to +125°C exclusive of the current required by the bipolar offset circuit. An external buffer amplifier is recommended if this reference will be used to drive other system components, because variations in a load driven from the reference will result in bipolar offset variations of the DAC870 converter. Gain and bipolar offset adjustments should be made under constant load conditions. It should be noted that because of the design of the DAC870 an external reference voltage cannot be used with the DAC870.

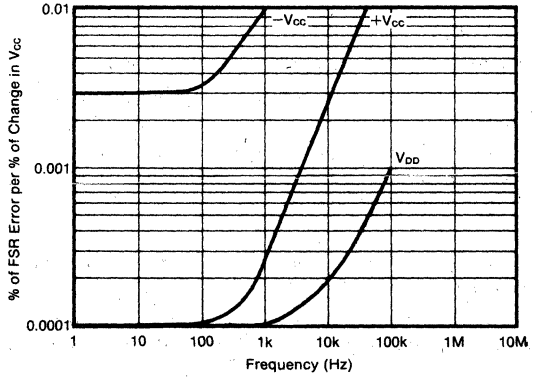


FIGURE 8. Power Supply Sensitivity vs Power Supply Ripple.

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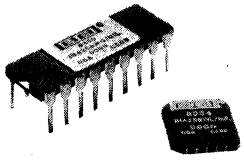


INA258/MIL SERIES

MODEL NUMBERS:

INA258WG/MIL	INA258VG/MIL	INA258UG/883B
INA258WL/MIL	INA258VL/MIL	INA258UL/883B
INA258WG/883B	INA258VG/883B	INA258UG
INA258WL/883B	INA258VL/883B	INA258UL
INA258WG	INA258VG	
INA258WL	INA258VL	

REVISION NONE
MARCH, 1984

Very-High Accuracy Military INSTRUMENTATION AMPLIFIER

FEATURES

- VERSATILE FOUR-OP AMP DESIGN
- ULTRA-LOW VOLTAGE DRIFT, 0.5μV/°C
- LOW OFFSET VOLTAGE, 50μV
- LOW NONLINEARITY, 0.005%
- LOW NOISE, 13nV/$\sqrt{\text{Hz}}$ at f_o = 1kHz
- HIGH CMR, 106dB at 60Hz
- HIGH INPUT IMPEDANCE, $10^{10}\Omega$

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gauges
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS

DESCRIPTION

The INA258 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very high performance is desired.

A multiamplifier, monolithic design, which uses Burr-Brown's ultra-low drift, low noise technology, provides the highest performance with maximum versatility at the lowest cost. This makes the INA258 ideal for even high volume applications.

Burr-Brown's compatible thin film resistors and state-of-the-art wafer level laser trimming techniques are used for minimizing offset voltage and temperature drift. This advanced technique also maximizes common mode rejection and gain accuracy.

The INA258 also contains a fourth operational amplifier, specified separately, which can conveniently be used for some important applications, such as single-capacitor active low-pass filtering and easy output level shifting.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
INSTRUMENTATION AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a very high accuracy instrumentation amplifier. For description of operation see paragraph 8.

1.2 Part number. The complete part number is as shown below.

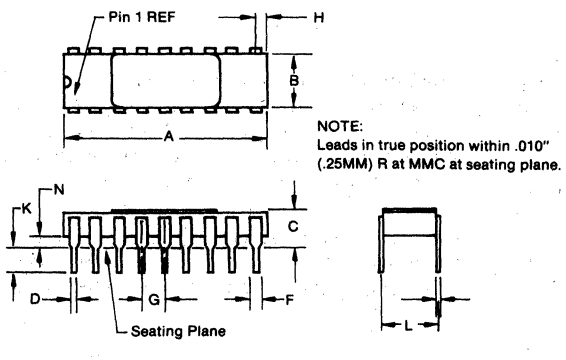
INA258	W	G	/MIL
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single instrumentation amplifier. Three electrical performance grades (W, V, and U) are provided. The electrical performance characteristics are shown in Table I.

1.2.2 Device class. The device class is similar to the class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

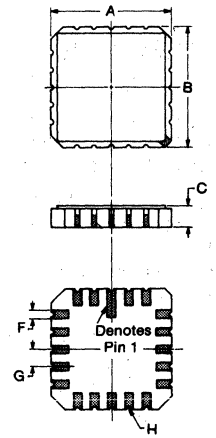
Hi-Rel Product Designator	Requirements
/MIL	Standard model plus 100% MIL-STD-883 class B screening, with 5% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
/883B	Standard model, plus 100% MIL-STD-883 Class B screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. Two case outlines are available. The case outline for the "G" package is D-6, configuration 3 (18-lead ceramic side braze), and the outline for the "L" package is C-2 (20-terminal square leadless chip carrier) as defined in MIL-M-38510 Appendix C. Figure 1 depicts the case outlines for both package types.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	.960	—	24.38
B	.220	.310	5.59	7.87
C	—	.200	—	5.08
D	.014	.023	.36	.58
F	.030	.070	.76	1.78
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.015	.20	.38
K	.125	.200	3.18	5.08
L	.290	.320	7.37	8.13
N	.015	.060	.38	1.52

(a) 18-pin side braze; package ID: "G"



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.342	.358	8.69	9.09
B	.342	.358	8.69	9.09
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
A	.008R TYP.		0.20 TYP.	

(b) 20-terminal leadless chip carrier ID: "L"

FIGURE 1. Case Outlines.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	$\pm V_{CC}$
Internal power dissipation	600mW
Storage temperature range	−65°C to +165°C
Output short circuit duration	Continuous to ground
Lead temperature (soldering, 10 sec.)	+300°C

1.2.5 Recommended operating conditions.

Supply voltage range	±5VDC to ±20VDC
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case Outline	Maximum allowable power dissipation	Maximum θ_{JC}
18-lead DIP	Figure 1	600mW	41°C/W
20-terminal LCC	Figure 1	600mW	40°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510—Microcircuits, General Specification for.

STANDARD
MILITARY
MIL-STD-883—Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections for the "G" package are shown in Figure 2 and the circuit diagram and terminal connections for the "L" package are shown in Figure 3.

3.2.8 Glassivation. The microcircuit die is glassivated.

3.2.9 Schematic circuits. Simplified schematic circuits for "G" and "L" packages are shown in Figures 2 and 3 respectively.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Additional electrical performance curves are shown in paragraph 7.

3.3.2 Offset null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 4. If nulling is unnecessary, delete the potentiometer and make no connections.

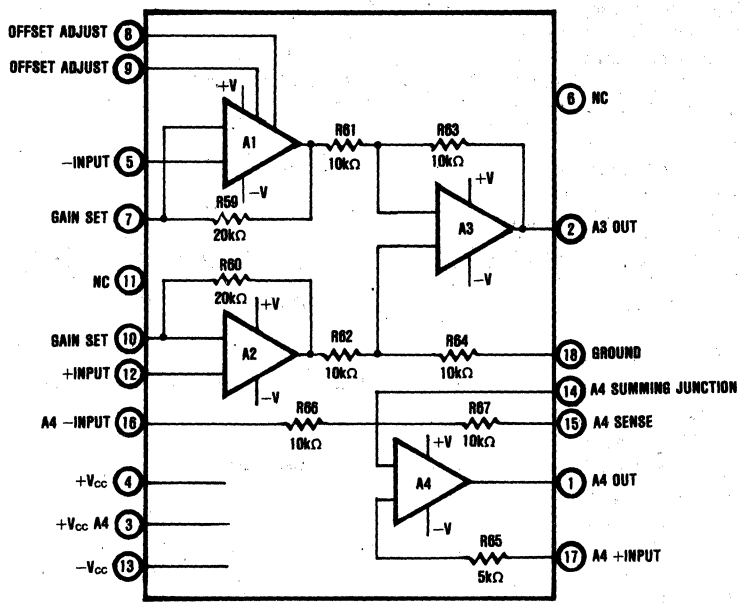


FIGURE 2. INA258 "G" Circuit Diagram and Terminal Connections.

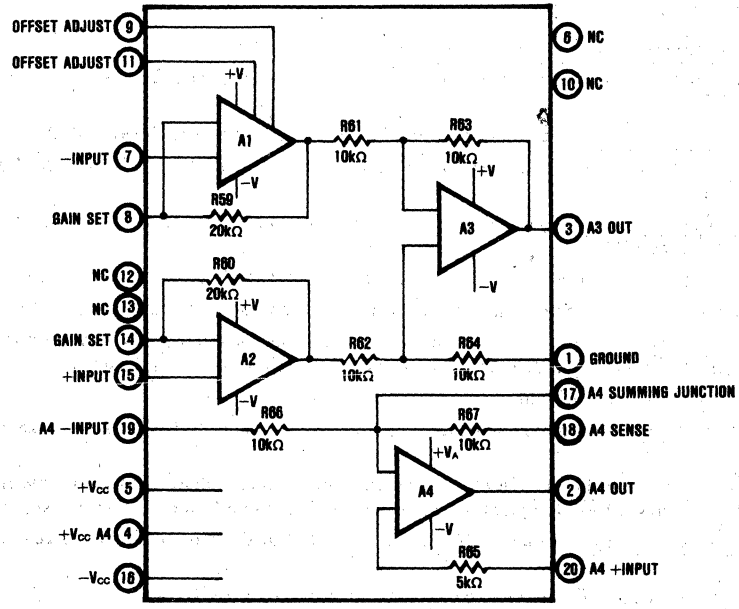


FIGURE 3. INA258 "L" Package Circuit Diagram and Terminal Connections.

TABLE I. Electrical Performance Characteristics.

All characteristics at $-55°C \le T_A \le +125°C$, $\pm V_{CC} = 15VDC$, unless otherwise specified.

CHARACTERISTICS	SYMBOL	CONDITIONS	INA258WG/MIL[1] INA258WL/MIL[1] INA258WG/883B INA258WL/883B INA258WG INA258WL			INA258VG/MIL[1] INA258VL/MIL[1] INA258VG/883B INA258VL/883B INA258VG INA258VL			INA258UG/883B INA258UL/883B INA258UG INA258UL			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN												
Range of Gain	A_V	$A_V = 1 + (40k/R_G)$ [2]	1		1000	*		*	*		*	V/V
Gain Equation Error	E_{AV}	$A_V = 1$, $T_A = +25°C$			.05							% FS
		$A_V = 10$, $T_A = +25°C$			.10							% FS
		$A_V = 100$, $T_A = +25°C$			.10							% FS
		$A_V = 1000$, $T_A = +25°C$			.40							% FS
Gain Tempco[3]	$\Delta A_V/\Delta T$	$A_V = 1$		2			*			*		ppm/°C
		$A_V = 10$		20			*			*		ppm/°C
		$A_V = 100$		22			*			*		ppm/°C
		$A_V = 1000$		22			*			*		ppm/°C
DC Nonlinearity	NL	$A_V = 1$, $T_A = +25°C$			0.005							%
		$A_V = 10$, $T_A = +25°C$			0.005							%
		$A_V = 100$, $T_A = +25°C$			0.007							%
		$A_V = 1000$, $T_A = +25°C$			0.025							%
RATED OUTPUT												
Voltage	V_{OP}	$R_L = 2k\Omega$, $T_A = +25°C$	±10			*			*			V
Current	I_O		±5			*			*			mA
Impedance	Z_O			2			*			*		Ω
INPUT OFFSET VOLTAGE												
Initial	V_{io}	$A_V = 1$, $T_A = +25°C$			±250			*			*	μV
	V_{io}	$A_V = 1000$, $T_A = +25°C$			±50			*			*	μV
vs Temperature	$\Delta V_{io}/\Delta T$	$A_V = 1$, $-55°C \le T_A \le +125°C$			10			15			45	μV/°C
		$A_V = 1000$, $-55°C \le T_A \le +125°C$			0.5			1.0			3.0	μV/°C
		$A_V = 1$, $-25°C \le T_A \le +85°C$									20	μV/°C
		$A_V = 1000$, $-25°C \le T_A \le +85°C$									1.8	μV/°C
vs Supply	PSRR	$A_V = 1$, $\Delta V_{CC} = \pm 5VDC$, $T_A = +25°C$			1			*			*	μV/V
		$A_V = 1000$, $\Delta V_{CC} = \pm 5VDC$, $T_A = +25°C$			20			*			*	μV/V
INPUT BIAS CURRENT												
Initial	I_{ib}	$T_A = +25°C$			±20			*			*	nA
Tempco	$\Delta I_{ib}/\Delta T$			±.2			*			*		nA/°C
INPUT OFFSET CURRENT												
Initial	I_{io}	$T_A = +25°C$			±20			*			*	nA
Tempco	$\Delta I_{io}/\Delta T$			±.5			*			*		nA/°C
INPUT IMPEDANCE												
Differential	Z_{ID}	$T_A = +25°C$	$10^{10}\|\|3$		*			*		Ω||pF		
Common Mode	Z_{ICM}	$T_A = +25°C$	$10^{10}\|\|3$		*			*		Ω||pF		
INPUT VOLTAGE												
Linear Response Range	V_{IN}		±10			*			*			V
Common Mode Rejection	CMR	DC-60Hz, $A_V = 1k\Omega$ Source Imbalance, $T_A = +25°C$	80			*			*			dB
		DC-60Hz, $A_V = 10$, $1k\Omega$ Source Imbalance $T_A = +25°C$	96			*			*			dB
		DC-60Hz, $A_V = 100$-1000, $1k\Omega$ Source Imbalance, $T_A = +25°C$	106			*			*			dB
INPUT NOISE												
Input Voltage Noise	E_{NPP}	$f_B = 0.01$ to 10Hz, $T_A = +25°C$		.8			*			*		μV, p-p
	E_N	$A_V = 1000$, $f_O = 10Hz$, $T_A = +25°C$		18			*			*		$nV/\sqrt{Hz}$
		$A_V = 1000$, $f_O = 100Hz$, $T_A = +25°C$		15			*			*		$nV/\sqrt{Hz}$
		$A_V = 1000$, $f_O = 1kHz$, $T_A = +25°C$		13			*			*		$nV/\sqrt{Hz}$
Input Current Noise	I_{NPP}	$f_B = 0.01Hz$ to 10Hz, $T_A = +25°C$		50			*			*		pA, p-p
	I_N	$f_O = 10Hz$, $T_A = +25°C$		.8			*			*		$pA/\sqrt{Hz}$
		$f_O = 100Hz$, $T_A = +25°C$		.46			*			*		$pA/\sqrt{Hz}$
		$f_O = 1kHz$, $T_A = +25°C$		.35			*			*		$pA/\sqrt{Hz}$
DYNAMIC RESPONSE												
Slew Rate	SR	$A_V = 1$ to 100, $R_L = 2k\Omega$, $T_A = +25°C$	0.2									V/μsec
Bandwidth	BW	3dB small signal, $A_V = 1$, $T_A = +25°C$		300			*			*		kHz
		$A_V = 10$, $T_A = +25°C$		140			*			*		kHz
		$A_V = 100$, $T_A = +25°C$		25			*			*		kHz
		$A_V = 1000$, $T_A = +25°C$		2.5			*			*		kHz
	BW	Full power $A_V = 1$ to 1000, $T_A = +25°C$		6.4								kHz
Settling Time	T_S	.01%, $A_V = 1$, $T_A = +25°C$		30			*			*		μsec
		$A_V = 100$, $T_A = +25°C$		50			*			*		μsec
		$A_V = 1000$, $T_A = +25°C$		500			*			*		μsec

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	SYMBOL	CONDITIONS	INA258WG/MIL[1] INA258WL/MIL[1] INA258WG/883B INA258WL/883B INA258WG INA258WL			INA258VG/MIL[1] INA258VL/MIL[1] INA258VG/883B INA258VL/883B INA258VG INA258VL			INA258UG/883B INA258UL/883B INA258UG INA258UL			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY												
Rated Voltage	$\pm V_{CC}$		±5	±15	±20	*	*	*	*	*	*	V
Quiescent Current	I_Q	$T_A = +25°C$			±8			*			*	mA
FOURTH OP AMP												
Input Offset Drift	V_{io}	$T_A = +25°C$			5000			*			*	µV
Tempco	$\Delta V_{io}/\Delta T$	$-55 \leq T_A \leq +125°C$		±5			*			*		µV/°C
Input Bias Current	I_{IB}	$T_A = +25°C$			50			*			*	nA
Input Offset Current	I_{IO}	$T_A = +25°C$			50			*			*	nA
Quiescent Current	I_Q	$T_A = +25°C$		2	4			*			*	mA

*Same as INA258W grade.

NOTES: 1/ /MIL models available in third quarter 1984.
2/ Typically the tolerance of R_G will be the major source of gain error.
3/ Not including TCR of R_G.
4/ Adjustable to zero at any one gain.

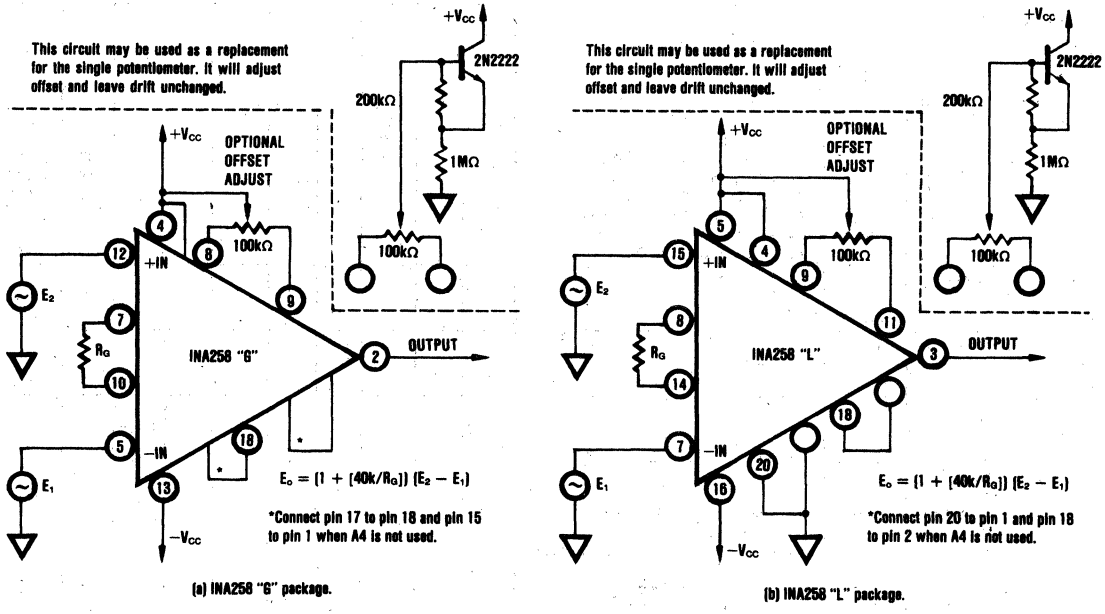


FIGURE 4. Basic Circuit Connection for the INA258 Including Optional Input Offset Null Potentiometer.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin (U.S.A.)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /MIL product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the /MIL product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for /MIL and /883B Hi-Rel product designations is in accordance with MIL-STD-883, method 5004, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition E), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

For the /MIL product designations, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III).

MIL-STD-883 REQUIREMENTS (Class B)	INA258WG/MIL INA258WL/MIL	INA258WG/883B INA258WG INA258WL/883B INA258WL	INA258VG/MIL INA258VL/MIL	INA258VG/883B INA258VG INA258VL/883B INA258VL	INA258UG/883B INA258UG INA258UL/883B INA258UL
Interim electrical parameters (preburn-in) (method 5004)	1	1	1	1	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4	1, 2, 3, 4	1*, 2, 3, 4	1, 2, 3, 4	1, 2U, 3U, 4
Group A test requirements (method 5005)	1, 2, 3, 4	—	—	—	—
Group C end point electrical parameters (method 5005)	Table IV limits and delta limits	—	Table IV limits and delta limits	—	—

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD or equivalent	CONDITIONS (±V_{CC} = 15VDC unless otherwise specified)	LIMITS						UNITS
				INA258WG/MIL[1] INA258WL/MIL[1] INA258WG/883B INA258WL/883B INA258WG INA258WL		INA258VG/MIL[1] INA258VL/MIL[1] INA258VG/883B INA258VL/883B INA258VG INA258VL		INA258UG/883B INA258UL/883B INA258UG INA258UL		
				MIN	MAX	MIN	MAX	MIN	MAX	
1 T_A = 25°C	V_{io}	4001	A_V = 1		±250		±250		±250	µV
			A_V = 1000		±50		±50		±50	µV
	I_{ib}	4001			±20		±20		±20	nA
	I_{io}	4001			±20		±20		±20	nA
	I_Q	4005	Each Supply		±8		±8		±8	mA
	PSRR	4003	A_V = 1, ΔV_{CC} = ±5VDC		1		1		1	µV/V
			A_V = 1000, ΔV_{CC} = ±5VDC		20		20		20	µV/V
	CMR	4003	DC, A_V = 1, 1kΩ Source Imbalance	80		80		80		dB
			DC, A_V = 10, 1kΩ Source Imbalance	96		96		96		dB
			DC, A_V = 100-1000, 1kΩ Source Imbal.		106	106		106		dB
	V_{io}[2]	4001			5000		5000		5000	µV
	I_{ib}[2]	4001			50		50		50	nA
	I_{io}[2]	4001			50		50		50	nA
	I_Q[2]	4005			4		4		4	mA
2 T_A = 125°C	V_{io}	4001	A_V = 1		1250		1750		5250	µV
			A_V = 1000		100		150		450	µV
	$\Delta V_{io}/\Delta T$	4001	A_V = 1 [V_{io} (125°C) − V_{io} (25°C)] ÷ 100		10		15		45	µV/°C
			A_V = 1000 [V_{io} (125°C) − V_{io} (25°C)] ÷ 100		0.5		1.0		3.0	µV/°C
2U T_A = 85°C	V_{io}	4001	A_V = 1						1575	µV
			A_V = 1000						150	µV
	$\Delta V_{io}/\Delta T$	4001	A_V = 1 [V_{io} (85°C) − V_{io} (25°C)] ÷ 60						20	µV/°C
			A_V = 1000 [V_{io} (85°C) − V_{io} (25°C)] ÷ 60						1.8	µV/°C

c. Percent defective allowable (PDA). The PDA, for /MIL product designation only, is 5 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5004, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

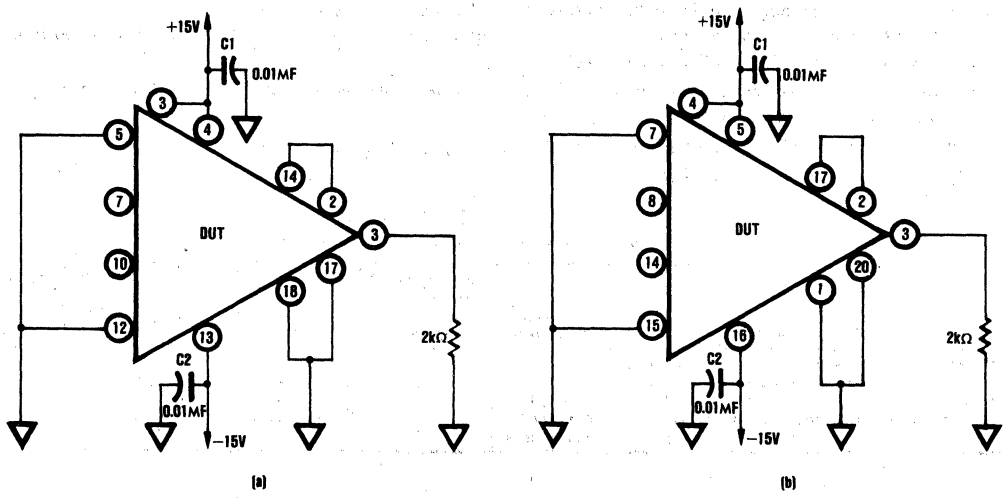


FIGURE 5. (a) Test Circuit Burn-In and (b) Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, is performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5005, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5005. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005 (class B).

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005 (class B), and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum

b. End point electrical parameters are specified in Table IV herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005 (class B) and as follows:

a. End point electrical parameters are specified in Table IV herein.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming are intended for use in applications where the use of screened parts is required or desirable.

6.3 Order data. The contract or purchase order should specify the following:

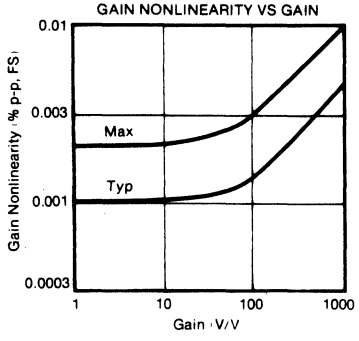
a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

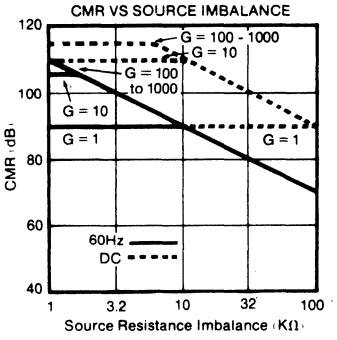
6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group D as defined in MIL-M-38510, Appendix E.

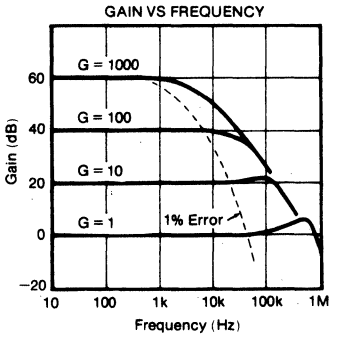
6.5 Electrostatic sensitivity. CAUTION—These microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

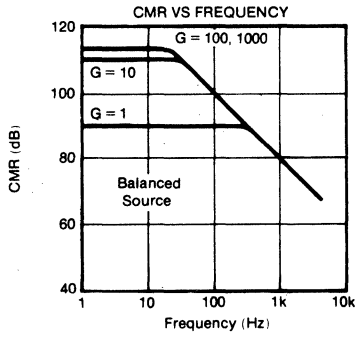
7. ELECTRICAL PERFORMANCE GRADES

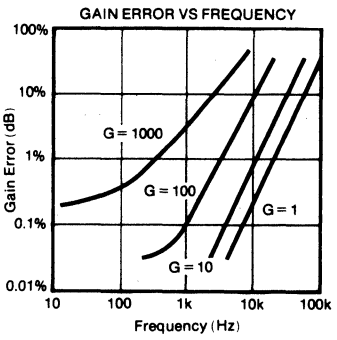
(Typical at +25°C and $\pm V_{CC}$ = 15VDC unless otherwise specified.)

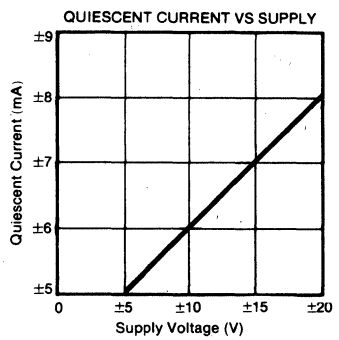


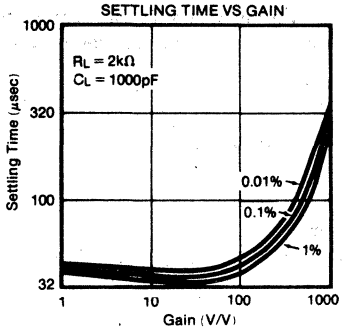


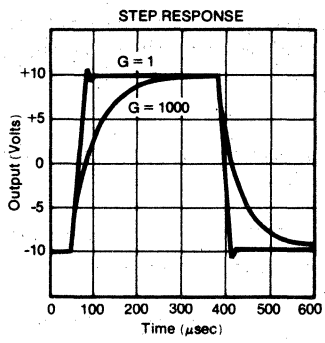


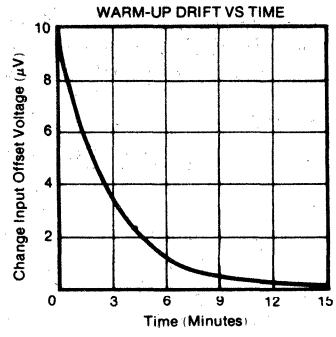


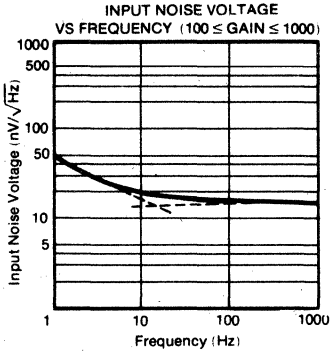


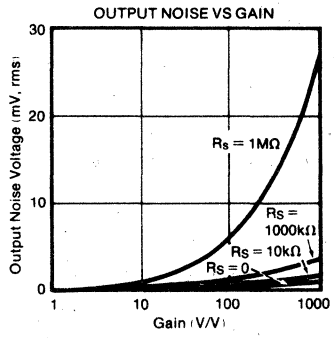












8. APPLICATION INFORMATION

8.1 Description. The INA258 is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers. See simplified schematics in Figures 2 and 3.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature are low due to the monolithic design, and are improved even further by state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA258 is operated over wide temperature ranges.

The fourth op-amp (A4) of the INA258 adds a great deal of versatility and convenience to the amplifier. Its use allows easy implementation of active low-pass filtering, output offsetting, and additional gain generation. The pin connections make the use of this stage optional and the specifications appear separately in the table of Electrical Specifications.

8.2 Using the INA258. Figure 4 shows the simplest configuration of the INA258. The gain is set by the external resistor, R_G, with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

TABLE III. Group A Inspection (cont).

SUBGROUP	SYMBOL	MIL-STD-883 METHOD or equivalent	CONDITIONS ($\pm V_{CC}$ = 15VDC unless otherwise specified)	LIMITS: INA258WG/MIL[1/] INA258WL/MIL[1/] INA258WG/883B INA258WL/883B INA258WG INA258WL		LIMITS: INA258VG/MIL[1/] INA258VL/MIL[1/] INA258VG/883B INA258VL/883B INA258VG INA258VL		LIMITS: INA258UG/883B INA258UL/883B INA258UG INA258UL		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
3 $T_A = -55°C$	V_{io}	4001	$A_V = 1$		1050		1450		5250	μV
			$A_V = 1000$		90		150		450	μV
	$\Delta V_{io}/\Delta T$	4001	$A_V = 1$ [V_{io} (25°C) − V_{io} (−55°C)] ÷ 80		10		15		45	$\mu V/°C$
			$A_V = 1000$ [V_{io} (25°C) − V_{io} (−55°C)] ÷ 80		1.5		1.0		3.0	$\mu V/°C$
3U $T_A = -25°C$	V_{io}	4001	$A_V = 1$						1380	μV
			$A_V = 1000$						135	μV
	$\Delta V_{io}/\Delta T$	4001	$A_V = 1$ [V_{io} (25°C) − V_{io} (−25°C)] ÷ 50						20	$\mu V/°C$
			$A_V = 1000$ [V_{io} (25°C) − V_{io} (−25°C)] ÷ 5						1.8	$\mu V/°C$
4 $T_A = 25°C$	E_{AV}		Gain Equation Error $A_V = 1$		0.05		0.05		0.05	% FS
			$A_V = 10$		0.10		0.10		0.10	% FS
			$A_V = 100$		0.10		0.10		0.10	% FS
			$A_V = 1000$		0.40		0.40		0.40	% FS
	V_{OP}	4004	$R_L = 2k\Omega$	±10		±10		±10		V
	SR		$R_L = 2k\Omega$	0.2		0.2		0.2		V/μsec
	NL[3/]	Figure 4	$A_V = 1$		0.005		0.005		0.005	%
			$A_V = 10$		0.005		0.005		0.005	%
			$A_V = 100$		0.007		0.007		0.007	%
			$A_V = 1000$		0.025		0.025		0.025	%

NOTES: 1/ /MIL models available third quarter 1984.
2/ Fourth op amp.
3/ E_1 = 0V and E_2 is varied to enable nonlinearity error to be measured by sampling 21 points between $-10V \leq E_{OUT} \leq +10V$ and determining worst case deviation from straight line connecting these end points at each gain setting.

TABLE IV. Group C, End Point Electrical Parameters.

($T_A = +25°C$, $\pm V_{CC}$ = 15VDC, V_{CM} = 0V)

TEST	LIMIT	DELTA
V_{IO} ($A_V = 1$)	±250μV	*
V_{IO} ($A_V = 1000$)	±50μV	*
I_{ib}	±20nA	*

*Delta limits to be finalized upon completion of qualification.

3.11 Quality conformance inspection. Quality conformance inspection, for the /MIL product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the /MIL and /883 Hi-Rel product designations is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.

b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

8.3 Basic circuit connection. The basic circuit connection for the INA258 is shown in Figure 4. The output voltage is a function of the differential input voltage times the gain.

Figure 4 does not include additional internal op amp A4. Power supply bypassing with a 1μF tantalum capacitor or equivalent is always recommended.

In applications which do not use the fourth internal amplifier, insure the A4 $+V_{CC}$ is not connected to V_{CC}, the A4 + input is connected to common and A4 sense is connected to A4 output.

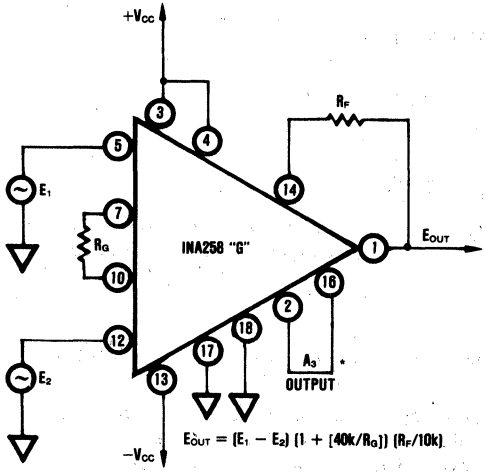
8.4 Typical applications. Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gauges, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA258 accomplishes all of these with high precision.

Figures 6, 7, and 8 show some typical applications circuits.

Figure 6 shows how the output stage may be used to provide additional gain. If gains greater than 1000V/V (10,000 up to 100,000 and greater) are desired, it is better to place some gain in the output amplifier rather than the input stage, due to the low values of R_G required ($R_G < 40\Omega$ for $[1 + 40k/R_G] > 1000$). Note, however, that accuracy can degrade due to very high amplification of offset, drift, and noise errors.

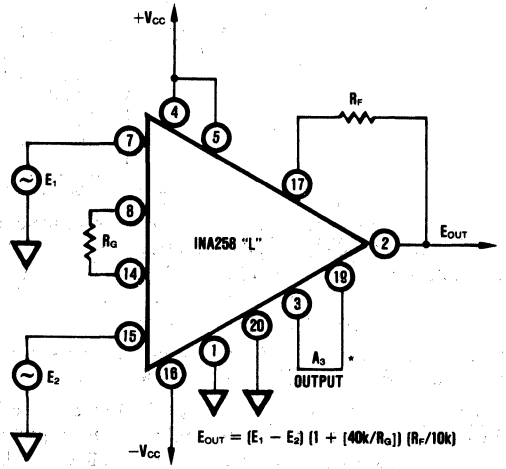
Output offsetting ("zero suppression" or "zero elevation") may be more easily accomplished with the INA258 than with most other IC instrumentation amplifiers, as shown in Figure 7. The use of the extra internal op amp, A4, means that CMR of the instrument amp is not disturbed, and that a convenient value of variable resistor can be used.

Amplifier A4 also allows active low-pass filtering to be implemented conveniently with a single capacitor. Filtering can be used for noise reduction or band-limiting of the output signal as shown in Figure 8.



*NOTE: A4 inverts the output of the instrumentation amplifier, pin 2 to pin 16. Therefore the equation for E_{OUT} shows $E_1 - E_2$ instead of $E_2 - E_1$.

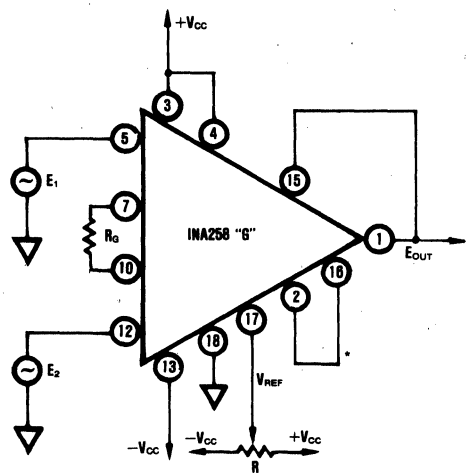
(a) INA258 "G".



*NOTE: A4 inverts the output of the instrumentation amplifier, pin 3 to pin 19. Therefore the equation for E_{OUT} shows $E_1 - E_2$ instead of $E_2 - E_1$.

(b) INA258 "L".

FIGURE 6. Additional Gain From Output Stage.

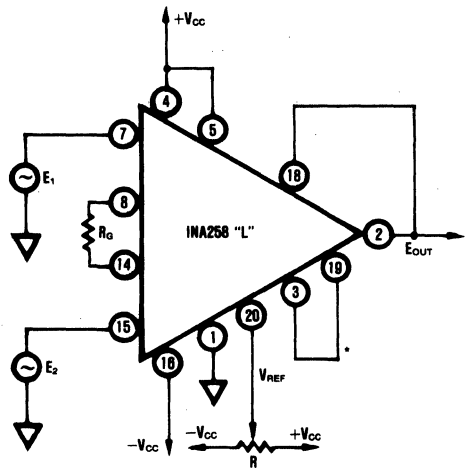


R = a convenient value (<100kΩ typically)

$E_{OUT} = (E_1 - E_2)\,(1 + [40k/R_G]) + 2V_{REF}$

*NOTE: A4 inverts, see Figure 6.

(a) INA258 "G".



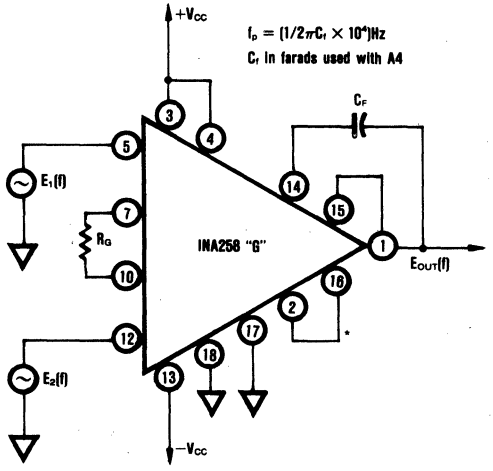
R = a convenient value (<100kΩ typically)

$E_{OUT} = (E_1 - E_2)\,(1 + [40k/R_G]) + 2V_{REF}$

*NOTE: A4 inverts, see Figure 6.

(b) INA258 "L."

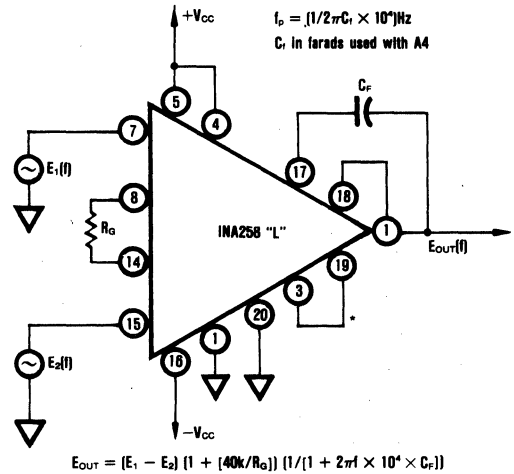
FIGURE 7. Output Offsetting.



$E_{OUT} = (E_1 - E_2)\,(1 + [40k/R_G])\,(1/[1 + 2\pi f \times 10^4 \times C_F])$

*NOTE: A4 inverts, see Figure 6.

(a) INA258 "G"



$E_{OUT} = (E_1 - E_2)\,(1 + [40k/R_G])\,(1/[1 + 2\pi f \times 10^4 \times C_F])$

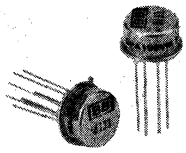
*NOTE: A4 inverts, see Figure 6.

(b) INA258 "L".

FIGURE 8. Active Low-Pass Filtering.

BURR-BROWN®

OPA105/MIL SERIES



MODEL NUMBERS:

OPA105VM/MIL
OPA105VM/883B
OPA105VM
OPA105UM/883B
OPA105UM
OPA105WM/MIL
OPA105WM/883B
OPA105WM

REVISION A
MARCH, 1983

FET Input Military OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, 1pA, max
- HIGH INPUT IMPEDANCE, $10^{13}\Omega$
- ULTRA-LOW DRIFT, $2\mu V/°C$, max
- LOW OFFSET VOLTAGE $250\mu V$, max
- LOW QUIESCENT CURRENT, 1.5mA, max
- HERMETICALLY SEALED TO-99 PACKAGE

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS

DESCRIPTION

The OPA105/MIL Series is a low bias current operational amplifier. Guaranteed low initial offset voltage ($250\mu V$, max) and associated drift versus temperature ($2\mu V/°C$, max) is achieved by laser-adjusting the amplifier during manufacturing. This feature, and guaranteed low bias current (1pA, max), allow greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA105/MIL Series include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA105/MIL Series allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a FET input, low bias current, low drift, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

OPA105	V	M	/MIL
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single operational amplifier. Three electrical performance grades are provided. The W grade features $\pm 2\mu V/^{\circ}C$ drift (-55°C to +125°C). The V grade features $\pm 5\mu V/^{\circ}C$ drift (-55°C to +125°C). The U grade features excellent performance ($\pm 15\mu V/^{\circ}C$) from -25°C to +85°C and guarantees performance from -55°C to +125°C. Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel product designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and periodically thereafter. Additional electrical testing is performed on /MIL models.
/883B	Standard model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is A-1 (8-lead can, TO-99) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC [1]
Differential input voltage range	±40VDC [1]
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited [2]
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±5VDC to ±20VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-A
8-lead can	Figure 1	225mW at T_A =125°C	220°C/W

1 The absolute maximum input voltage is equal to the supply voltage.
2 Short circuit may be to ground only. Rating apples to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

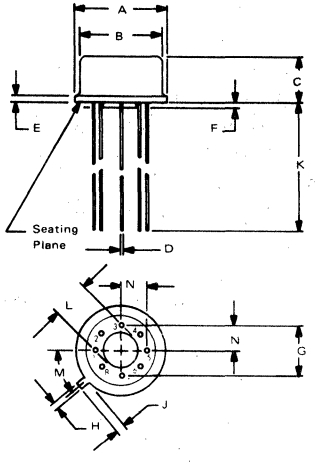
3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510. See Figure 1 for the case outline.



Note:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 1. Case Outline (TO-99) Package Configuration.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice are glassivated.

3.2.9 Schematic Circuit. A simplified schematic circuit is shown in Figure 3.

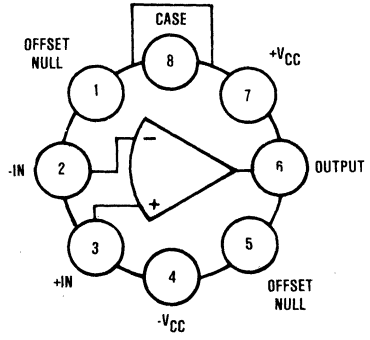
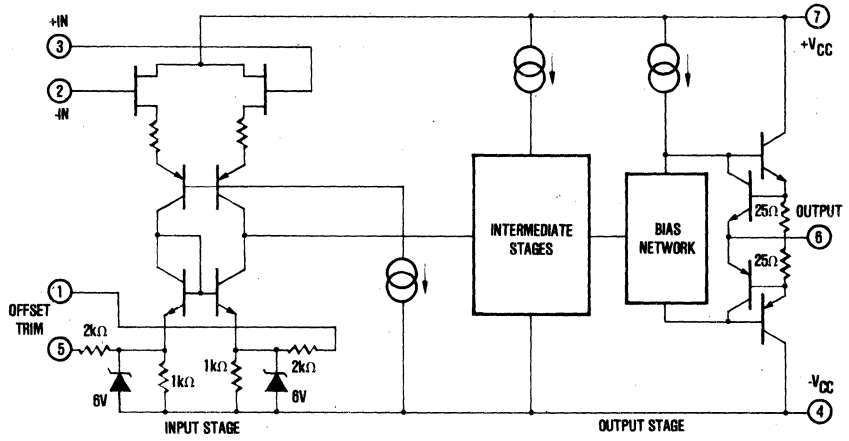


FIGURE 2. Circuit Diagram and Terminal Connections.



3.3 Electrical Performance Characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Additional Electrical Performance Characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Offset null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 4. If nulling is unnecessary for the application, delete the three components and make no connections.

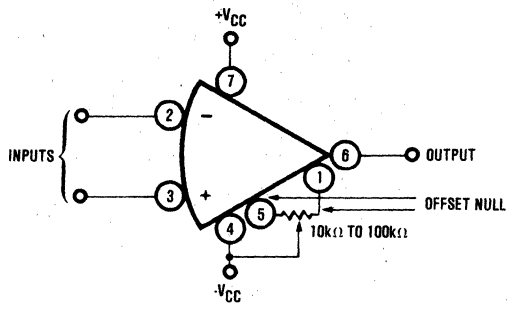


FIGURE 4. Offset Null Circuit.

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated at any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code [1]
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin (U.S.A.)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the MIL Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for / MIL Hi-Rel product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

[1] A 4-digit date code, indicating year and week of seal, is marked on 883B and (none) Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics.

All characteristics at -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise specified.

CHARACTERISTIC	SYM-BOL	CONDITIONS	OPA105WM/MIL OPA105WM/883B OPA105WM MIN	TYP	MAX	OPA105VM/MIL OPA105VM/883B OPA105VM MIN	TYP	MAX	OPA105UM/883B OPA105UM MIN	TYP	MAX	UNITS
GAIN												
Open-Loop Voltage Gain	A_{VS}	R_L = 2kΩ, V_O = ±10V, F = 0Hz; T_A = +25°C	106	112		*	*		*	*		dB
		R_L = 2kΩ, V_O = ±10V, F = 0Hz; -55°C ≤ T_A ≤ +125°C	95	102		*	*		*	*		dB
RATED OUTPUT												
Voltage	V_O	R_L = 1kΩ	±10			*	*		*	*		V
Current	I_O		±10			*	*		*	*		mA
Impedance	Z_O	T_A = +25°C		3			*			*		kΩ
Load Capacitance	C_L	T_A = +25°C	500	1000		*	*		*	*		pF
Short Circuit Current	I_{OS}	To Ground	10	25		*	*		*	*		mA
DYNAMIC RESPONSE												
Bandwidth	BW	Unity Gain-Small Signal T_A = +25°C		1			*			*		MHz
Bandwidth	BW	Full Power T_A = +25°C	14	20		*	*		*	*		kHz
Slew Rate	SR	R_L = 2kΩ, T_A = +25°C	0.9	1.3		*	*		*	*		V/μsec
Settling Time (0.1%)	T_S	T_A = +25°C		9			*			*		μsec
Settling Time (0.01%)	T_S	T_A = +25°C		20			*			*		μsec
Overload Recovery 1/	T_r	T_A = +25°C		4	15		*	*		*	*	μsec
INPUT OFFSET VOLTAGE												
Initial Offset	V_{IO}	T_A = +25°C			±250			*			*	μV
Temperature Sensitivity	DV_{IO}	$\frac{V_{IO}(T_A) - V_{IO}(+25°C)}{\Delta T}$										
		-55 ≤ T_A ≤ +125°C			±2			±5			±25	μV/°C
		-25 ≤ T_A ≤ +85°C									±15	μV/°C
vs Power Supply	PSRR	V_{CC} = ±5, V_{CC} = ±20VDC			±74			*			*	dB
INPUT BIAS CURRENT												
Initial Bias 2/	I_{IB}	T_A = +25°C			1			*			*	pA
vs Supply Voltage		T_A = +25°C		0.005			*			*		pA/V
INPUT OFFSET CURRENT												
Initial Offset	I_{IO}	T_A = +25°C		±0.2			*			*		pA
INPUT IMPEDANCE												
Differential	Z_{Id}	T_A = +25°C		10^{13} || 1.6			*			*		Ω || pF
Common-Mode	Z_{ICM}	T_A = +25°C		10^{15} || 1.8			*			*		Ω || pF
INPUT NOISE												
Voltage	e_n	f_O = 10Hz T_A = +25°C		55			*			*		nV/√Hz
		f_O = 100Hz T_A = +25°C		35			*			*		nV/√Hz
		f_O = 1kHz T_A = +25°C		30			*			*		nV/√Hz
		f_O = 10kHz T_A = +25°C		25			*			*		nV/√Hz
		f_B = 0.1Hz to 10Hz T_A = +25°C		3			*			*		μV/, p-p
Current	i_n	f_B = 0.1Hz to 10Hz T_A = +25°C		0.01			*			*		pA, p-p
		f_B = 10Hz to 10kHz T_A = +25°C		0.03			*			*		pA, rms
		f_O = 1kHz T_A = +25°C		0.6			*			*		fA/√Hz
INPUT VOLTAGE RANGE												
Differential	V_{DI}	T_A = +25°C	±20			*			*			V
Common-Mode		T_A = +25°C	±10	±12		*	*		*	*		V
Common-Mode Rejection	CMRR	V_{IN} = ±10V T_A = +25°C	76	86		*	*		*	*		dB
POWER SUPPLY												
Rated Voltage	V_{DI}			±15			*			*		VDC
Voltage Range			±5		±20	*		*	*		*	VDC
Quiescent Current	I_Q			1.0	1.5		*	*		*	*	mA
TEMPERATURE RANGE (ambient)												
Operating			-55		+125	*		*	*		*	°C
Storage			-65		+150	*		*	*		*	°C

*Same as OPA105W grade **OPA105WM/MIL and OPA105VM/MIL available 2nd quarter 1983.

NOTES:

1/ Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.

2/ Bias current is tested and guaranteed at T_A = +25°C. For higher temperature the bias current doubles every +10°C.

3.9 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle, constant acceleration (condition B), and external visual inspection per MIL-STD-883, method 5008, hybrid class.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for MIL Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883B REQUIREMENTS (hybrid class) / MODELS	OPA105WM/MIL	OPA105WM/883B OPA105WM	OPA105VM/MIL	OPA105VM/883B OPA105VM	OPA105UM/883B OPA105UM
Interim electrical parameters (pre burn-in) (method 5008)	1, 4	1, 4	1, 4	1, 4	1, 4
Final electrical test parameters (method 5008)	1*, 2, 3, 4	1, 2, 3, 4	1*, 2, 3, 4	1, 2, 3, 4	1, 2U, 3U, 4
Group A test requirements (method 5008)	1, 2, 3, 4	---	1, 2, 3, 4	---	---
Group C end point electrical parameters (method 5008)	Table IV limits and delta limits	---	Table IV limits and delta limits	---	---
Additional electrical subgroups for Group C inspections	5, 6 1/	---	5, 6	---	---

*PDA applies to subgroups 1, 4 (see 4.3d)

1/LTPD for these additional tests is 15%.

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC}$ = 15VDC unless otherwise specified	LIMITS OPA105WM/MIL OPA105WM/883B OPA105WM MIN	MAX	OPA105VM/MIL OPA105VM/883B OPA105VM MIN	MAX	OPA105UM/883B OPA105UM MIN	MAX	UNITS
1	V_{IO}	4001			±250		±250		250	µV
	I_{IB}	4001			±1		±1		±1	pA
	V_O		R_L = 2kΩ	±10		±10		±10		V
	I_Q				1.5		1.5		1.5	mA
T_A = +25°C	CMRR	4003	V_{CM} ±10V	76		76		76		dB
	PSRR		V_{CC} = ±5V, V_{CC} = ±20V	74		74		74		dB
2 T_A = +125	DV_{IO}	4001	$\frac{V_{IO}(+125) - V_{IO}(+25)}{100}$		2		5			µV/°C
2U T_A = +85°C	DV_{IO}	4001	$\frac{V_{IO}(+85) - V_{IO}(+25)}{60°C}$						15	µV/°C
3 T_A = -55°C	DV_{IO}	4001	$\frac{V_{IO}(+25) - V_{IO}(-55)}{80}$		2		5			µV/°C
3U T_A = -25°C	DV_{IO}	4001	$\frac{V_{IO}(+25) - V_{IO}(-25)}{50}$						15	µV/°C
4	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	106		106		106		dB
T_A = +25°C	SR	4002	R_L = 2kΩ, V_O = ±10V	0.9		0.9		0.9		V/µsec
5 T_A = +125°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	95		95				dB
6 T_A = -55°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	95		95				dB

TABLE IV. Group C, End Point Electrical Parameters.

(T_A = +25°C, ±V_{CC} = 15VDC, V_{CM} = 0V)

TEST	LIMIT	DELTA
V_{IO}	±250μV	±125μV
I_{IB}	±1pA	±0.8pA

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.
b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) T_A = +125°C minimum
   (4) Test duration is 160 hours minimum
d. Percent defective allowable (PDA). The PDA, for /MIL Hi-Rel product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
e. External visual inspection need not include measurement of case and lead dimensions.

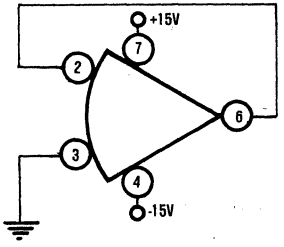


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, is performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

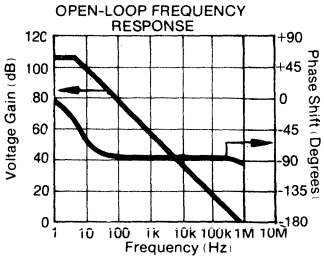
a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

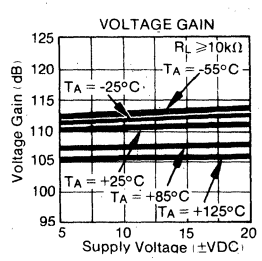
6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group F as defined in MIL-M-38510, Appendix E.

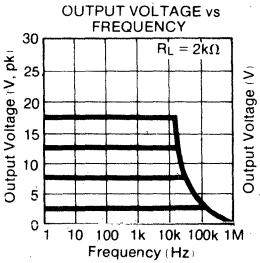
6.5 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

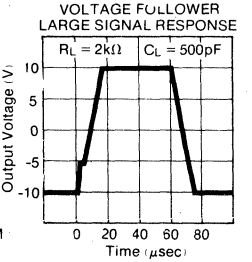
7. ELECTRICAL PERFORMANCE CURVES.

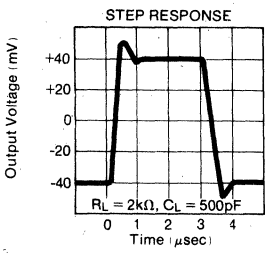
(Typical at $T_A = +25°C$ and $\pm V_{CC} = 15VDC$ unless otherwise specified).

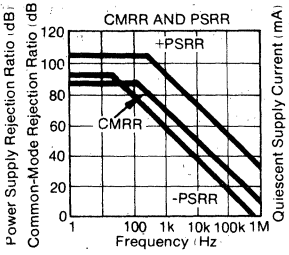


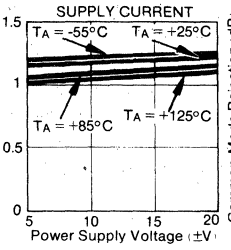


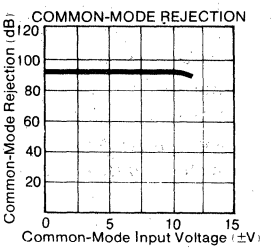












8. APPLICATION INFORMATION

8.1 Offset voltage adjustment. Although the OPA105/MIL Series has a low intital offset voltage (250μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C for every 100μV of offset adjustment.

8.2 Guarding and shielding. The ultra-low bias current and high input impedance of the OPA105/MIL Series are well-suited to a number of stringent applications, however, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA105/MIL Series.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the amplifier's bias current of the OPA105/MIL Series. To avoid leakage problems, it is recommended that the signal input lead of the OPA105/MIL Series be wired to a Teflon standoff. If the OPA105/MIL Series is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low input impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 6 illustrates the use of the guard. The resistor R_3 shown in Figure 6 is optional. It may be used to compensate effects of very large source resistances. However, note that its use would also increase the noise due to the thermal noise of R_3.

8.3 Thermal response time. Thermal response time is an important parameter in low drift operational amplifiers like the OPA105/MIL Series. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA105/MIL Series is 20 seconds.

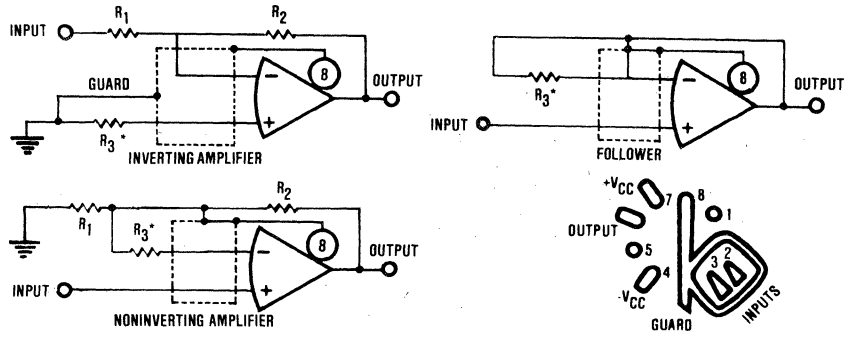
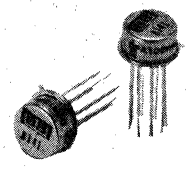


FIGURE 6. Connection of Input Guard.

BURR-BROWN®

OPA106/MIL SERIES



MODEL NUMBERS:

OPA106WM/MIL	OPA106VM/MIL
OPA106WM/883B	OPA106VM/883B
OPA106WM	OPA106VM
OPA106UM/883B	REVISION A
OPA106UM	MARCH, 1984

FET Input Military
OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, 100fA, max
- HIGH INPUT IMPEDANCE, $10^{13}\Omega$
- LOW DRIFT, $5\mu V/°C$, max
- LOW OFFSET VOLTAGE $250\mu V$, max
- LOW QUIESCENT CURRENT, 1.5mA, max
- HERMETICALLY SEALED TO-99 PACKAGE

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS

DESCRIPTION

The OPA106/MIL Series is a low bias current 100fA, max) operational amplifier. Guaranteed low initial offset voltage ($250\mu V$, max) and associated drift versus temperature ($5\mu V/°C$, max) is achieved by laser-adjusting the amplifier during manufacturing. This feature, and guaranteed low bias current allow greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA106/MIL Series include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA106/MIL Series allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a FET input, low bias current, low drift, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

OPA106	V	M	/MIL
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single operational amplifier. Three electrical performance grades are provided. The W grade features ±5μV/°C drift (-55°C to +125°C). The V grade features ±10μV/°C drift (-55°C to +125°C). The U grade features ±20μV/°C drift from -25°C to +85°C and guarantees performance from -55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel product designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening, with 10% PDA, plus quality conformance inspection (QC1) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and periodically thereafter. Additional electrical testing is performed on /MIL models.
/883B	Standard model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is A-1 (8-lead can, TO-99) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC [1]
Differential input voltage range	±40VDC [1]
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited [2]
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = +175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±5VDC to ±20VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C
8-lead can	Figure 1	225mW at T_A = +125°C	220°C/W

1 The absolute maximum input voltage is equal to the supply voltage.
2 Short circuit may be to ground only. Rating applies to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

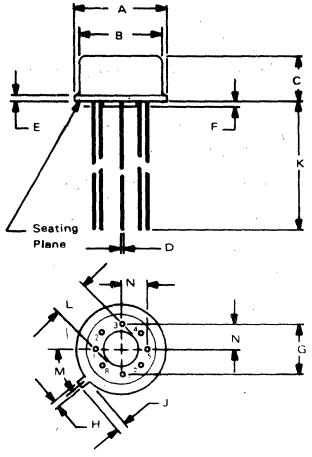
3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510. See Figure 1 for the case outline.



Note:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 1. Case Outline (TO-99) Package Configuration.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice utilized are glassivated.

3.2.9 Schematic Circuit. The schematic circuit is shown in Figure 3.

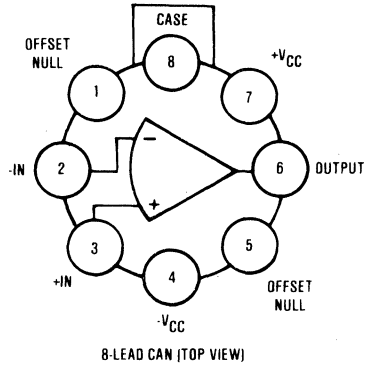


FIGURE 2. Circuit Diagram and Terminal Connections.

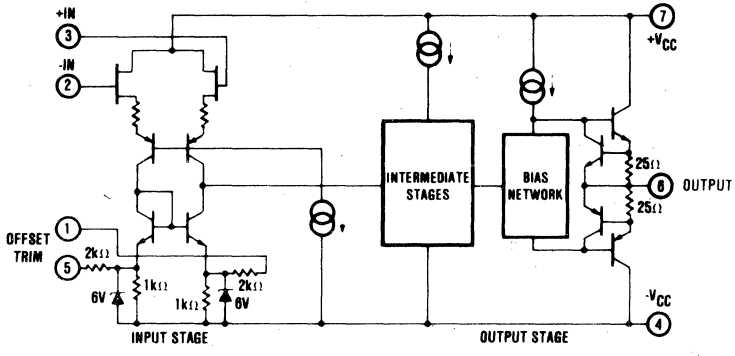


FIGURE 3. Simplified Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Offset null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 4. If nulling is unnecessary for the application, delete the potentiometer and make no connections.

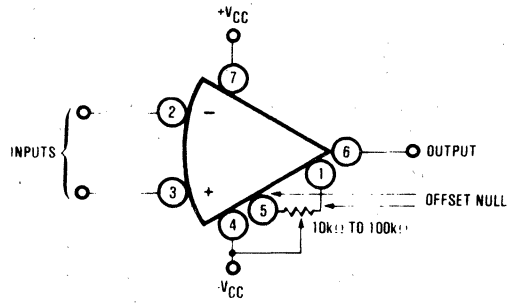


FIGURE 4. Offset Null Circuit.

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated at any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1
d. Manufacturer's identification (BURR-BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin (U.S.A)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the / MIL product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for / MIL product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

1/ A 4-digit date code, indicating year and week of seal, is marked on /883B and (none) Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics.

All characteristics at -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise specified.

CHARACTERISTIC	SYMBOL	CONDITIONS		OPA106WM/MIL OPA106WM/883B OPA106WM			OPA106VM/MIL OPA106VM/883B OPA106VM			OPA106UM/883B OPA106UM			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN													
Open-Loop		R_L = 2kΩ	T_A = +25°C	103	109		•	•		•	•		dB
Voltage Gain	A_{VS}	V_O = ±10V, F = 0Hz	-55°C ≤ T_A ≤ +125°C	93	101		•	•		•	•		dB
RATED OUTPUT													
Voltage	V_O	R_L = 1kΩ		±10			•			•			V
Current	I_O			±10			•			•			mA
Impedance	Z_O		T_A = +25°C		3			•			•		kΩ
Load Capacitance	C_L		T_A = +25°C	500	1000		•	•		•	•		pF
Short Circuit Current	I_{OS}	To Ground		10	25		•	•		•	•		mA
DYNAMIC RESPONSE													
Bandwidth	BW	Unity Gain-Small, Signal	T_A = +25°C		1			•			•		MHz
Bandwidth	BW	Full Power	T_A = +25°C	19	28		•	•		•	•		kHz
Slew Rate	SR	R_L = 2kΩ,	T_A = +25°C	1.2	1.8		•	•		•	•		V/μsec
Settling Time (0.1%)	T_S		T_A = +25°C		6			•			•		μsec
Settling Time (0.01%)	T_S		T_A = +25°C		18			•			•		μsec
Overload Recovery 1/	T_r		T_A = +25°C		4	15		•	•		•	•	μsec
INPUT OFFSET VOLTAGE													
Initial Offset	V_{IO}		T_A = +25°C			±250			•			•	μV
Temperature Sensitivity	DV_{IO}	$\frac{V_{IO}(T_A) - V_{IO}(+25°C)}{\Delta T}$											
			-55°C ≤ T_A ≤ +125°C			±5			±10			50	μV/°C
			-25°C ≤ T_A ≤ +85°C									±20	μV/°C
vs Power Supply	PSRR	V_{CC} = ±5, V_{CC} = ±20VDC				±80			•			•	dB
INPUT BIAS CURRENT													
Initial Bias	I_{ib}		T_A = +25°C			100			-150			-300	fA
vs Supply Voltage			T_A = +25°C		1			•			•		fA/V
INPUT OFFSET CURRENT 2/													
Initial Offset	I_{IO}		T_A = +25°C		±40			±80			±80		fA
INPUT IMPEDANCE													
Differential	Z_{ID}	T_A = +°C			10^{13} || 0.8			•			•		Ω || pF
Common-Mode	Z_{ICM}				10^{15} || 1.6			•			•		Ω || pF
INPUT NOISE													
Voltage	e_n	f_O = 10Hz	T_A = +25°C		75			•			•		nV/√Hz
		f_O = 100Hz	T_A = +25°C		55			•			•		nV/√Hz
		f_O = 1kHz	T_A = +25°C		35			•			•		nV/√Hz
		f_O = 10kHz	T_A = +25°C		35			•			•		nV/√Hz
		f_B = 0.1Hz to 10Hz	T_A = +25°C		6			•			•		μV/, p-p
Current	i_n	f_B = 0.1Hz to 10Hz	T_A = +25°C		3			•			•		fA, p-p
		f_B = 10Hz to 10kHz	T_A = +25°C		10			•			•		fA, rms
		f_O = 1kHz	T_A = +25°C		0.25			•			•		fA/√Hz
INPUT VOLTAGE RANGE													
Differential	V_{di}		T_A = +25°C	±20			•			•			V
Common-Mode			T_A = +25°C	±10	±12		•	•		•	•		V
Common-Mode Rejection	CMRR	V_{IN} = ±10V	T_A = +25°C	76	86		•	•		•	•		dB
POWER SUPPLY													
Rated Voltage	±V_{CC}				±15			•			•		VDC
Voltage Range				±5		±20	•		•	•		•	VDC
Quiescent Current	I_Q				1.0	1.5		•	•		•	•	mA
TEMPERATURE RANGE (ambient)													
Operating				-55		+125	•		•	•		•	°C
Storage				-65		+150	•		•	•		•	°C

*Same as OPA106W Grade

NOTES:
1/ Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.
2/ Bias current is tested and guaranteed at T_A = +25°C. For higher temperature the bias current doubles every +10°C.

3.9 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle (condition C), constant acceleration (condition B), and external visual inspection per MIL-STD-883, method 5008, hybrid class.

For the /MIL product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for /MIL product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883B REQUIREMENTS (hybrid class) / MODELS	OPA106WM/MIL	OPA106WM/883B OPA106WM	OPA106VM/MIL	OPA106VM/883B OPA106VM	OPA106UM/883B OPA106UM
Interim electrical parameters (pre burn-in) (method 5008)	1, 4	1, 4	1, 4	1, 4	1, 4
Final electrical test parameters (method 5008)	1*, 2, 3, 4	1, 2, 3, 4	1*, 2, 3, 4	1, 2, 3, 4	1, 2U, 3U, 4
Group A test requirements (method 5008)	1, 2, 3, 4	---	1, 2, 3, 4	---	---
Group C end point electrical parameters (method 5008)	Table IV limits and delta limits	---	Table IV limits and delta Limits	---	---
Additional electrical subgroups for Group C inspections	5, 6 1/	---	5, 6 1/	---	---

*PDA applies to subgroups 1 - 4 (see 4.3.d)

1/ LTPD for these additional tests is 15%.

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC}$ = 15VDC unless otherwise specified	LIMITS						UNITS
				OPA106WM/MIL OPA106WM/883B OPA106WM		OPA106VM/MIL OPA106WM/883B OPA106WM		OPA106UM/883B OPA106UM		
				MIN	MAX	MIN	MAX	MIN	MAX	
1 T_A = +25°C	V_{IO}	4001			±250		±250		±250	µV
	I_{IB}	4001			±100		±150		±300	fA
	V_O		R_L = 2kΩ	±10		±10		±10		V
	I_Q				1.5		1.5		1.5	mA
	CMRR	4003	V_{CM} ±10V	76		76		76		dB
	PSRR		V_{CC} = ±5V, V_{CC} = ±20V	80		80		80		dB
2 T_A = +125°C	DV_{IO}	4001	$\frac{V_{IO}\ (125) - V_{IO}\ (25)}{100}$		5		10			µV/°C
2U T_A = +85°C	DV_{IO}	4001	$\frac{V_{IO}\ (85) - V_{IO}\ (25)}{60}$						20	µV/°C
3 T_A = -55°C	DV_{IO}	4001	$\frac{V_{IO}\ (25) - V_{IO}\ (-55)}{80}$		5		10			µV/°C
3U T_A = -25°C	DV_{IO}	4001	$\frac{V_{IO}\ (25) - V_{IO}\ (-25)}{50}$						20	µV/°C
4 T_A = +25°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	103		103		103		dB
	SR	4002	R_L = 2kΩ V_O = ±10V	1.2		1.2		1.2		V/µsec
5 T_A = +125°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	93		93				dB
6 T_A = -55°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	93		93				dB

TABLE IV. Group C, End Point Electrical Parameters.

(T_A = +25°C, $\pm V_{CC}$ = 15VDC, V_{DD} = +5VDC)

TEST	LIMIT	DELTA
V_{IO}	±250μV	±125μV

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening, for / MIL and / 883 Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.

b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

B c. Burn-in test (MIL-STD-883, method 1015) conditions:

(1) Test condition B

(2) Test circuit is Figure 5 herein

(3) T_A = +125°C minimum

(4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for / MIL product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

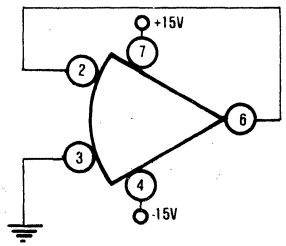


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, is performed on each lot. Groups C and D inspections of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table X, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table XI.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table XII, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum.
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table V.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

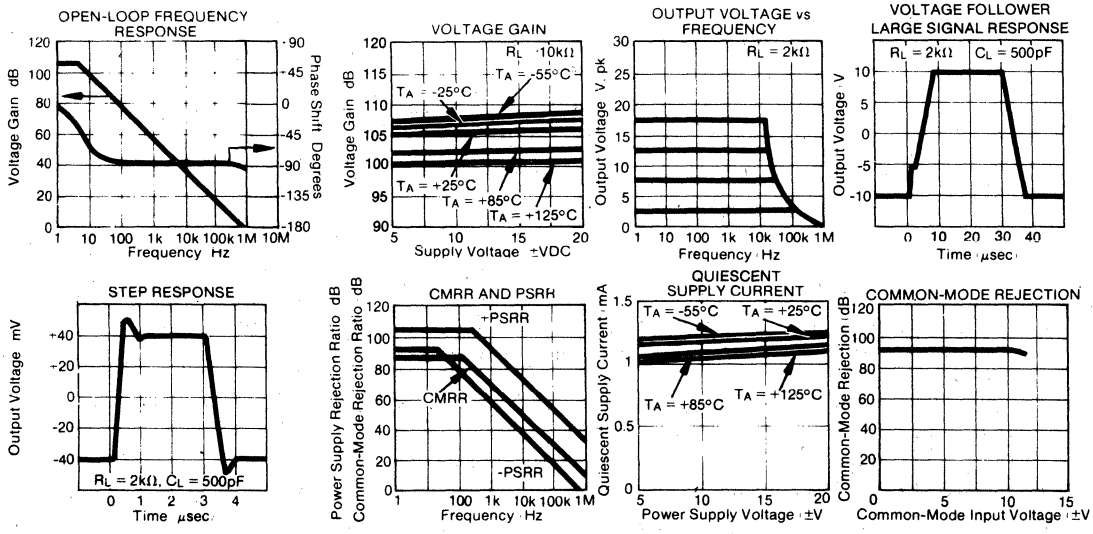
a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group F as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. ELECTRICAL PERFORMANCE CURVES.

(Typical at $T_A = +25°C$ and $\pm V_{CC} = 15VDC$ unless otherwise specified).



8. APPLICATION INFORMATION

8.1 Offset voltage adjustment. Although the OPA106/MIL Series has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C for every 100μV of offset adjustment.

8.2 Guarding and shielding. The ultra-low bias current and high impedance of the OPA106/MIL Series are well-suited to a number of stringent applications, however, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA106/MIL Series.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA106/MIL Series. To avoid leakage problems, it is recommended that the signal input lead of the OPA106/MIL Series be wired to a Teflon standoff. If the OPA106/MIL Series is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low input impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 6 illustrates the use of the guard. The resistor R_3 shown in Figure 6 is optional. It may be used to compensate effects of very large source resistances. However, note that its use would also increase the noise due to the thermal noise of R_3.

8.3 Thermal response time. Thermal response time is an important parameter in low drift operational amplifiers like the OPA106/MIL Series. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA106/MIL Series is approximately 20 seconds.

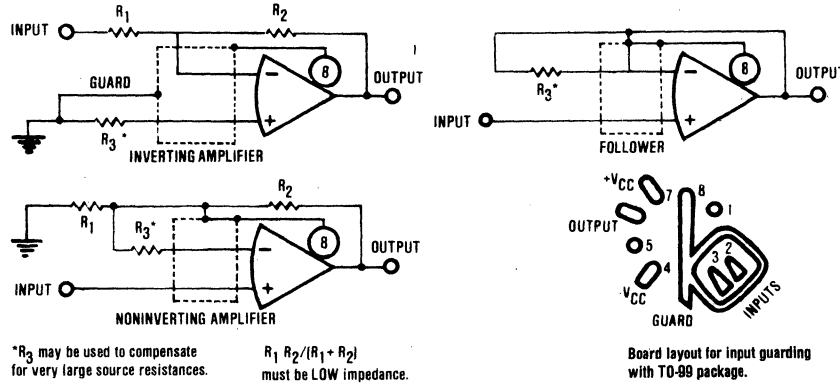
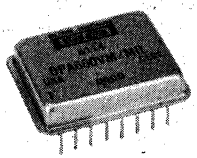


FIGURE 6. Connection of Input Guard.

BURR-BROWN®

OPA600/MIL SERIES



MODEL NUMBERS:

OPA600VM/MIL OPA600UM/883B
OPA600VM/883B OPA600UM
OPA600VM

REVISION C
JULY, 1983

Fast Settling - Wideband OPERATIONAL AMPLIFIER

FEATURES

- **FAST SETTLING**
  80nsec to ±0.1%
  115nsec to ±0.01%
- **FULL DIFFERENTIAL FET INPUT**
- **-55°C TO +125°C OPERATION**
- **LARGE OUTPUT**
  ±10V, ±200mA (50Ω)
- **GAIN-BANDWIDTH PRODUCT - 5GHz**

APPLICATIONS

- **VOLTAGE CONTROLLED OSCILLATOR DRIVER**
- **LARGE SIGNAL, WIDEBAND DRIVERS**
- **HIGH SPEED DAC OUTPUT AMPLIFIER**
- **VIDEO PULSE AMPLIFIER**

DESCRIPTION

The OPA600 is a wideband operational amplifier specifically designed for fast settling to ±0.01% accuracy. It is stable, easy to use, has good phase margin with minimum overshoot, and it has excellent DC performance. It utilizes a FET input stage to give low input bias current in contrast to the higher currents usually associated with very-fast amplifiers. Its DC stability with temperature is outstanding. Its -3dB bandwidth of 100MHz is available at a closed loop gain of 10. The slew rate exceeds 400V/μsec. All of this combines to form an outstanding amplifier for large and small signals.

Settling time is the best measure of this amplifier's total dynamic capability. High accuracy with fast settling is achieved by the large open-loop gain, which provides the accuracy at the upper frequencies. The thermally balanced design maintains this accuracy without droop or thermal tail. External compensation allows the user to optimize the settling time in his application.

The OPA600 is built to be reliable and is designed to operate from T_A = -55°C to +125°C. It is a hybrid microcircuit in a welded, hermetic, metal package and is available with MIL-STD-883 screening. The circuit is built on an alumina substrate which has a metallic attach to the package for good thermal transfer and reliable high temperature operation. The metal package provides electrostatic shielding. The circuit uses thin-film resistors and all glassivated, high speed silicon die. The gold or aluminum wirebonds utilized produce a monometallic system wherever possible, eliminating metal migration, a time-temperature reliability problem. The amplifier is actively laser-trimmed and is thoroughly tested. Reliability is emphasized during each phase of manufacture.

The OPA600 is useful in a broad range of video, high speed, and ECM applications. It is particularly well suited to operate as a voltage controlled oscillator (VCO) driver. It makes an excellent digital-to-analog converter output amplifier. It is a workhorse in test equipment where fast pulses, large signals, and 50Ω drive are important. It is a good choice for sample/holds, integrators, fast waveform generators, and multiplexers.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a hybrid, fast settling, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

OPA600	V	M	/MIL
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, operational amplifier. Two electrical performance grades are provided, the U grade and the V grade. The V grade offers the higher performance. Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. **The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:**

Hi-Rel product designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883, method 5008, class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and periodically thereafter. Additional electrical testing is performed in /MIL models.
/883B	Standard Model, plus 100% MIL-STD-883, method 5008, class B screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline (16-lead can) is as defined in Figure 6. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±17VDC
Input voltage range	±17VDC 1/
Differential input voltage range	±25VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	A few seconds 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±9VDC to ±16VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A
16-lead can	Figure 4	2.6W at T_{CASE} = +125°C	See Applications Information	35°C/W

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Duration is limited by device heat sinking (thermal resistance). Short circuit may be to ground only.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510, except that organic and polymeric materials (epoxy) are used for attach of some of the die. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

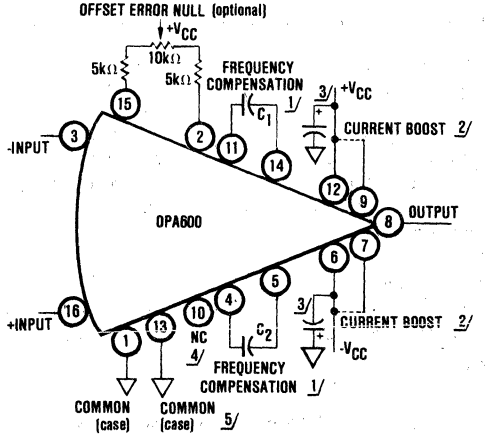
3.2.4 Lead material and finish. The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

3.2.8 Glassivation. Glassivation is in accordance with MIL-M-38510.



1/ Refer to Figure 4 for recommended frequency compensation.
2/ Connect pin 9 to pin 12 and connect pin 7 to pin 6 for maximum output current. See Application Information for further information.
3/ Bypass each power supply lead as close as possible to the amplifier pins. A 1μF CS13 tantalum capacitor is recommended.
4/ There is no internal connection. An external connection may be made.
5/ It is recommended that the amplifier be mounted with the case in contact with a ground plane for good thermal transfer and optimum AC performance.

FIGURE 1. Circuit Diagram and Terminal Connections.

3.2.9 Schematic Circuit. The schematic circuit is shown in Figure 2.

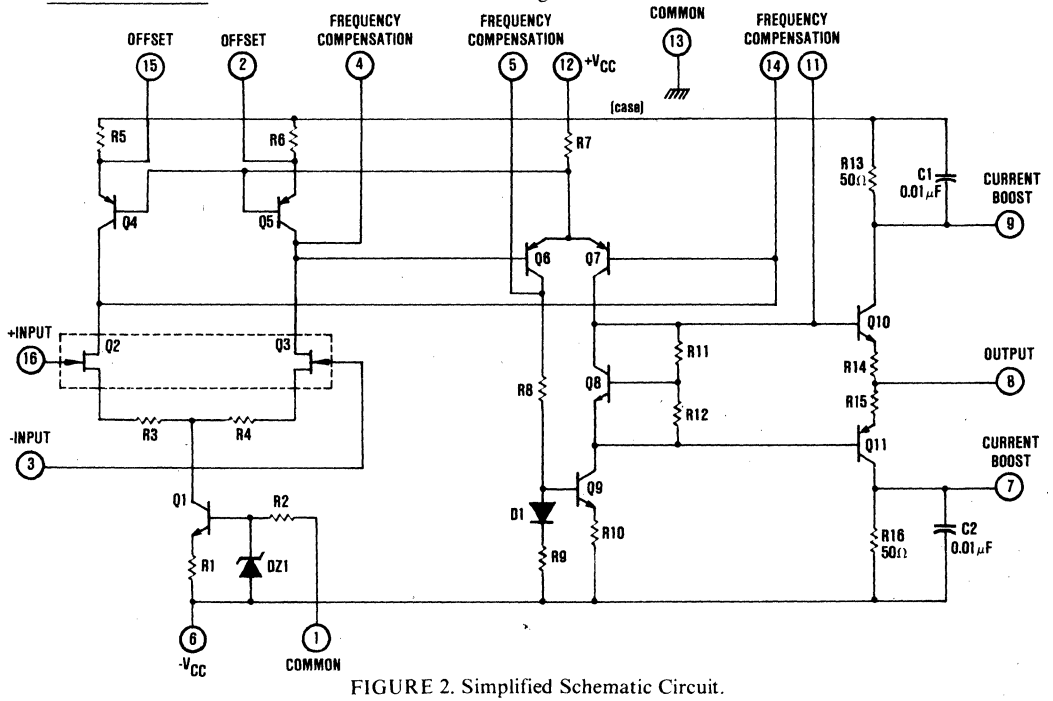


FIGURE 2. Simplified Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance characteristic curves are shown in paragraph 7.

3.3.2 Offset error null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 3. If nulling is unnecessary for the application, delete the three components and make no connections.

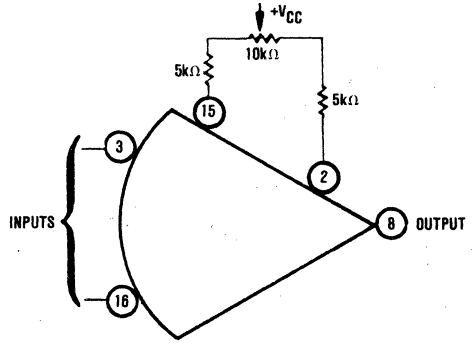


FIGURE 3. Offset Null Circuit.

3.3.3 Frequency compensation. The amplifier must be externally frequency compensated. See Figure 4.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragraph 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin (USA)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding, for the /MIL Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for /MIL Hi-Rel product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

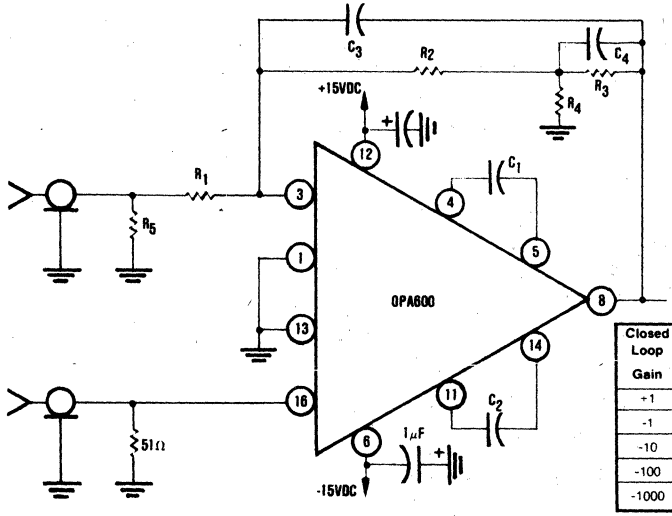
3.9 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model, includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle, constant acceleration (condition B), and external visual inspection per MIL-STD-883, method 5008, class B.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for /MIL Hi-Rel product designation, is in accordance with MIL-M-38510, expect as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.



Closed Loop Gain	R_1	R_2	R_3	R_4	C_1, C_2	C_3	C_4	R_5
+1	open	100	short	open	6.8	0	0	--
-1	620	620	short	open	3.3	4.7	0	56
-10	100	1k	short	open	1	2.2	0	100
-100	100	3.3k	3.3k	3.2k	0	1	0	100
-1000	100	3.3k	3.3k	116	0	0	4.7	100

Note: Resistance is in ohms, capacitance is in pF, gain is volts/volt.

FIGURE 4. Recommended Amplifier Circuits and Frequency Compensation.

1/ A 4-digit date code, indicating year and week of seal, and a 4- or 5-digit lot indentifier is marked on each unit.

TABLE I. Electrical Performance Characteristics

All characters from -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise noted.

CHARACTERISTICS	CONDITIONS		OPA600VM/MIL OPA600VM/883B OPA600VM MIN	TYP	MAX	OPA600UM/883B OPA600UM MIN	TYP	MAX	UNITS
OUTPUT									
Voltage (V_O)	R_L = 2kΩ		±10	±11		•	•		V
	R_L = 50Ω 1/		±9	±10		•	•		V
Current (I_O)	R_L = 50Ω 1/		±180	±200		•	•		mA
Current, pulse (I_{OP})	R_L = 50Ω 2/		±180	±200		•	•		mA
Resistance (R_O)	Open-loop, DC			75	150		•	•	Ω
Short Circuit Current (I_{OS})	To ground only, t_{MAX} = 1sec 3/			250	300		•	•	mA
DYNAMIC RESPONSE									
Settling Time, ±0.01% 4/ (t_S)	ΔV_O = 10V	T_A = 25°C		115	125		125	150	nsec
		T_A = -25°C to +85°C					135	165	nsec
		T_A = -55°C to +125°C		125	140			175	nsec
±0.1%	ΔV_O = 20V	T_A = +25°C		105	130		•	•	nsec
	ΔV_O = 10V	T_A = +25°C		80	105		•	•	nsec
±1%	ΔV_O = 20V	T_A = +25°C		80	105		•	•	nsec
	ΔV_O = 5V	T_A = +25°C		55	75		•	•	nsec
Post Settling Time Stability (t_S+) 5/	±0.01%	t = 1μsec to 500msec		0.5	1		•	•	mV
Gain-Bandwidth Product (open-loop) (GBP)	C_C = 0pF, G = 1 V/V	T_A = +25°C		150			•		MHz
	C_C = 0pF, G = 10V/V	T_A = +25°C		500			•		MHz
	C_C = 0pF, G = 100V/V	T_A = +25°C		1.5			•		GHz
	C_C = 0pF, G = 1000V/V	T_A = +25°C		5			•		GHz
	C_C = 0pF, G = 10,000V/V	T_A = +25°C		10			•		GHz
Bandwidth (BW) -3dB, small signal 6/	G = +1V/V	T_A = +25°C	100	125		•	•		MHz
	G = -1V/V	T_A = +25°C	75	90		•	•		MHz
	G = -1V/V	T_A = -55°C to +125°C	70	90	135	•	•		MHz
	G = -10V/V	T_A = +25°C	80	95		•	•		MHz
	G = -10V/V	T_A = -55°C to +125°C	70	95	135	•	•	•	MHz
	G = -100V/V	T_A = +25°C	15	20		•	•		MHz
	G = -1000V/V	T_A = +25°C	5	6		•	•		MHz
Full Power Bandwidth (BW_{FP})	V_O = ±5V, G = -1V/V, C_C = 3.3pF, R_L = 100Ω	T_A = +25°C	13	16		•	•		MHz
Slew Rate (SR)	V_O = ±5V, G = 1000V/V, C_C = 0pF, R_L = 100Ω	T_A = +25°C, ΔV_O = 10V		500					V/μsec
	V_O = ±5V, G = -1V/V 4/	T_A = +25°C, ΔV_O = 10V	400	440		•	•		V/μsec
		T_A = -55°C to +125°C	350			•			V/μsec
Phase Margin	G = -1V/V, C_C = 3.3pF	T_A = +25°C		40			•		Degrees
GAIN									
Open-Loop Voltage Gain (A_{VS})	f = D.C., R_L = 2kΩ	T_A = +25°C	86	94		•	•		dB
		T_A = -55°C to +125°C	74			•			dB
INPUT									
Offset Voltage (V_{IO}) 7/		T_A = +25°C		1	4		2	5	mV
		T_A = -25°C to +85°C						10	mV
		T_A = -55°C to +125°C			6			15	mV
Offset Voltage vs Temperature (DV_{IO})		T_A = -25°C to +25°C					50	80	μV/°C
		T_A +25°C to +85°C					25	80	μV/°C
		T_A = -55°C to +25°C		10	20			100	μV/°C
		T_A = +25°C to +125°C		10	20			100	μV/°C
Bias Current (I_{IB})		T_A = +25°C	0	-20	-100	•	•	•	pA
		T_A = +25°C to +125°C	0	-20	-100	•	•	•	nA
Offset Current (I_{IO})		T_A = +25°C		20	50		•	•	pA
		T_A = -55°C to +125°C		20	50		•	•	nA

TABLE I. Electrical Performance Characteristics (cont)

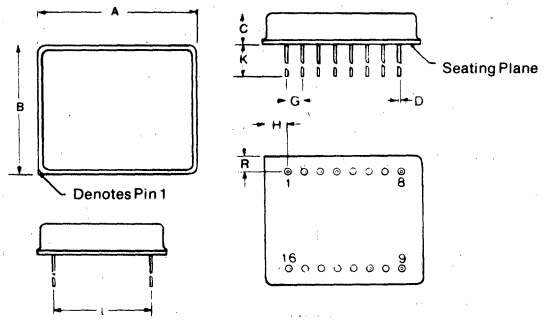
All characteristics from -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise noted.

		OPA600VM/MIL OPA600VM/883B OPA600VM			OPA600UM/883B OPA600UM			
CHARACTERISTICS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply Rejection Ratio (PSRR)	V_{CC} = ±15V, ±1V T_A = +25°C		200	500		*	*	µV/V
Common-Mode Voltage Range (CMV)	T_A = +25°C	-10		+7	*		*	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = -5V to +5V T_A = +25°C	60	80		*	*		dB
Impedance (Z_{IN})	Differential T_A = +25°C		10^{11} ‖ 2			*		Ω ‖ pF
	Common-mode T_A = +25°C		10^{11} ‖ 2			*		Ω ‖ pF
Voltage Noise (e_n)	f = 10kHz T_A = +25°C		20			*		$nV/\sqrt{Hz}$
POWER SUPPLY								
Rated (V_{CC})			±15			*		VDC
Operating Range (V_{CC})		±9		±16	*		*	VDC
Quiescent Current (I_Q)			±30	±38		*	*	mA
TEMPERATURE RANGE (ambient)								
Operating		-55		+125	-55		+125	°C
Storage		-65		+150	-65		+150	°C
θ_{JC} (junction to case)	See applications information							
θ_{CA} (case to ambient)			35			*		°C/W

*Specifications the same as V grade.

NOTES:

1/ Pin 9 connected to +V_{CC}, pin 7 connected to -V_{CC}. Observe power dissipation ratings.
2/ Pin 9 and pin 7 open. Single pulse t = 100nsec. Observe power dissipation ratings.
3/ Pin 9 and pin 7 open. See paragraph 8.8.
4/ G = −1V/V. Optimum settling time and slew rate achieved by individually compensating each device. Refer to paragraph 8.3.
5/ Post settling time stability is a measure of the pulse droop, or thermal tail, after the output has settled.
6/ Compensation per paragraph 8.3.
7/ Adjustable to zero.



NOTES:
1. Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
2. Pin numbers shown for reference only.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.963	.980	24.46	24.89
B	.760	.805	19.30	20.45
C	.175	.190	4.45	4.83
D	.014	.022	0.36	0.56
G	.100 BASIC		2.54 BASIC	
H	.135	.155	3.43	3.94
K	.230	.270	5.84	6.86
L	.600 BASIC		15.24 BASIC	
R	.095	.115	2.41	2.92

FIGURE 5. Case Outline.

TABLE II. Electrical Test Requirements.
(The individual tests within the subgroups appear in Table III)

MODELS / MIL-STD-883 TEST REQUIREMENT (hybrid class)	OPA600VM/MIL.	OPA600VM/883B OPA600VM	OPA600UM/883B OPA600UM
	Subgroups (see Table III)		
Interim electrical parameters (pre burn-in)(method 5008)	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4, 7, 9, 10, 11	1, 2, 3, 4, 7, 9	1, 2, 2U, 3, 3U, 4, 7, 9
Group A test requirements (method 5008)	1, 2, 3, 4, 7, 9	--	--
Group C end point electrical parameters (method 5008)	Table IV limits and delta limits	--	--
Additional electrical subgroups performed prior to Group C inspections	None	--	--

*PDA applies to subgroup 1 (see 4.3.d)

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC}$ = 15V, unless otherwise specified	LIMITS OPA600VM/MIL OPA600VM/883B OPA600VM MIN	LIMITS OPA600VM/MIL OPA600VM/883B OPA600VM MAX	LIMITS OPA600UM/883B OPA600UM MIN	LIMITS OPA600UM/883B OPA600UM MAX	UNITS
1	V_{IO}	4001	V_{CM} = 0	-4	+4	-5	+5	mV
T_A = +25°C	I_{IB}	4001	V_{CM} = 0	0	-100	0	-100	pA
	+PSRR	4003	+V_{CC} = 15V, ±1V, -V_{CC} = 15V	-500	+500	-500	+500	µV/V
	-PSRR	4003	+V_{CC} = 15V, -V_{CC} = 15V, ±1V	-500	+500	-500	+500	µV/V
	CMR	4003	V_{CM} = -5V to +5V	60		60		dB
	I_Q	4005			38		38	mA
2	V_{IO}	4001		-6	+6	-15	+15V	mV
T_A = +125°C	DV_{IO}	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (+125°C)}{100°C}$	-20	+20	-100	+100	µV/°C
2U	V_{IO}	4001				-10	+10	mV
T_A = +85°C	DV_{IO}	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (+85°C)}{60°C}$			-80	+80	µV/°C
3	V_{IO}	4001		-6	+6	-13	+13	mV
T_A = -55°C	DV_{IO}	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (-55°C)}{80°C}$	-20	+20	-100	+100	µV/°C
3U	DV_{IO}	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (-25°C)}{50°C}$			-9	+9	mV
T_A = -25°C						-80	+80	µV/°C
4	V_O	4004	R_L = 2kΩ	±10		±10		V
T_A = +25°C	I_O	4004	R_L = 50Ω, pin 9 to +V_{CC}, pin 7 to -V_{CC}	±180		±180		mA
	A_{VS}	4004	R_L = 2kΩ, f = 0Hz, V_O = ±10V	86		86		dB
7	V_O	4004	R_L = 2kΩ, ±V_{CC} = 16VDC	±11		±11		V
T_A = +25°C	V_O	4004	R_L = 2kΩ, ±V_{CC} = 12VDC	±7		±7		V
9	ts 2/	4002	To ±0.01%, Figure 10 final value at t = 1µsec		125		150	nsec
T_A = +25°C	SR 2/	4002	G = -1, V_O = ±5V, Figure 10 10% to 90%	400		400		V/µsec
10	ts 1/ 2/	4002	To ±0.01%, Figure 10 G = -1, V_o = ±5V		140			nsec
T_A = +125°C								
11	ts 1/ 2/	4002	To ±0.01%, Figure 10 G = -1, V_o = ±5V		140			nsec
T_A = -55°C								

NOTE:
1/ This test required for /MIL suffix only. Sample test per MIL-STD-105 level II, 4.0% AQL, normal inspection.
2/ G = −1V/V. Optimum settling time and slew rate achieved by individually compensating each device. Refer to paragraph 8.3.

TABLE IV. Group C, End Point Electrical Parameters.

(T_A = +25°C, ±V_{CC} = 15VDC)

TEST	LIMIT	DELTA
Input Offset Voltage	4mV	3mV
Open-Loop Voltage Gain	86dB	6dB
Settling Time (to 0.01%, ΔV_o = 10V, G = -1)	125nsec	—

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specified by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /883 Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, class B, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.
b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 6 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for /MIL Hi-Rel product designation only, is 10 percent and includes both parametric and catastropic failures. It is based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

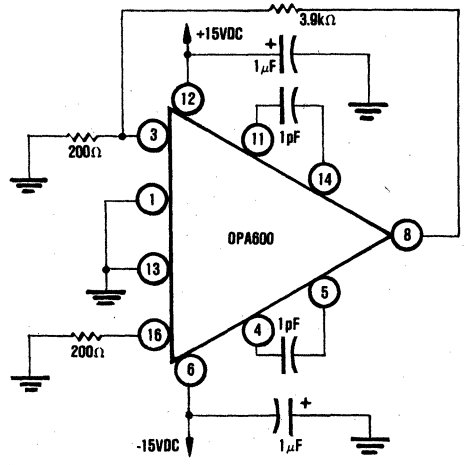


FIGURE 6. Test Circuit Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 6 herein
   (3) $T_A = 125°C$ minimum
   (4) Test duration is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of packaging. Inspection of packaging shall be as specified in MIL-M-38510.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2)

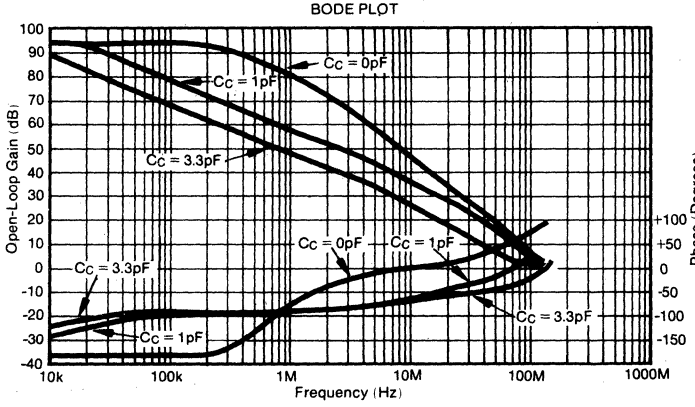
b. Requirement for certificate of compliance, if desired.

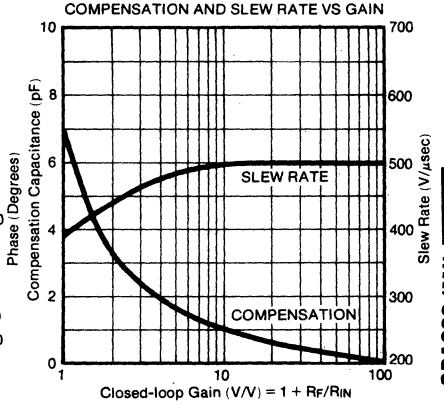
6.4 Microcircuit group assignment. These mircocircuits are assigned to Technology Group F as defined in MIL-M-38510, Appendix E.

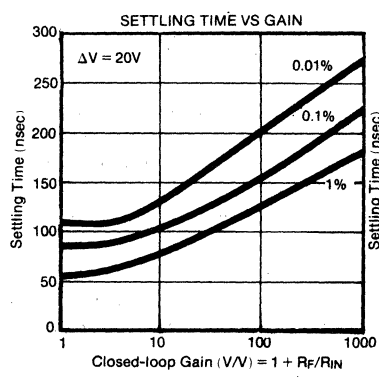
6.5 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

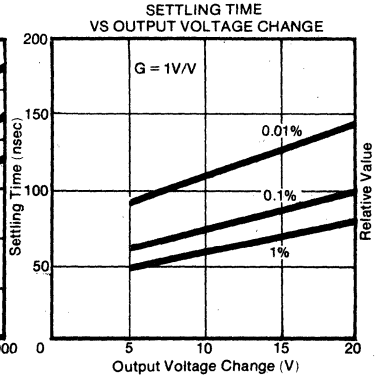
7. ELECTRICAL PERFORMANCE CURVES

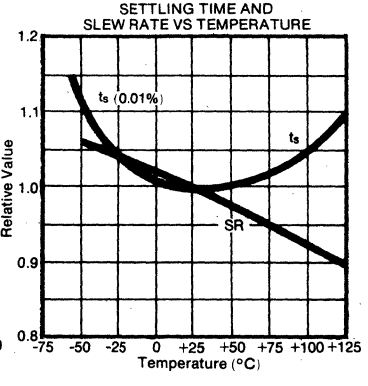
(Typical at T_A = +25°C and ±V_{CC} = 15VDC, unless otherwise specified).

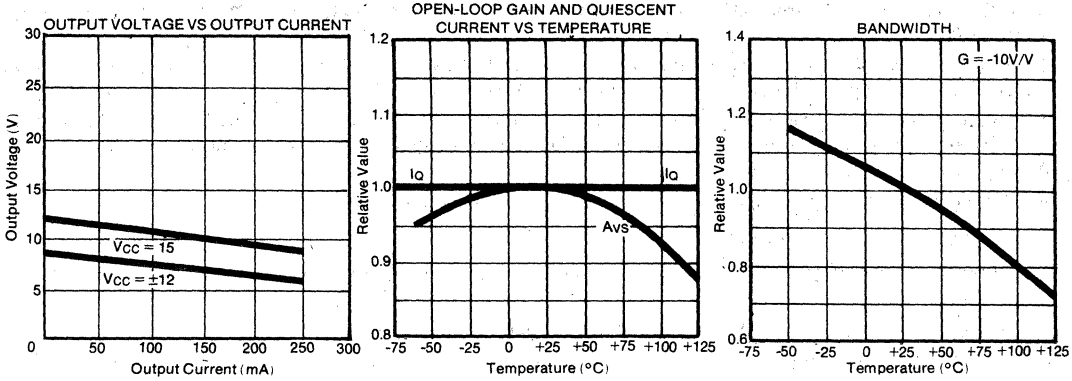












8. APPLICATIONS INFORMATION

8.1 Wiring precautions. The OPA600 is a wideband, high frequency operational amplifier with a gain-bandwidth product exceeding 5GHz. This capability can be realized by observing a few wiring precautions and using high frequency layout techniques. Of all the wiring precautions, grounding is the most important and is described in detail in the next section.

In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths and should be as short as possible. The entire physical circuit should be as small as is practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the input terminals of the amplifier and compensation pins. Stray signal coupling from the output to the input should be minimized. All circuit element leads should be as short as possible and low values of resistance should be used. This will give the best circuit performance as it will minimize the time constants formed with the circuit capacitances and will eliminate stray, unwanted tuned circuits.

8.2 Grounding. Grounding is the most important applications consideration for the OPA600, as it is with all high frequency circuits. Ultra-high frequency transistors are used in the design of the OPA600 and oscillations at frequencies of 500MHz and above can be stimulated if good grounding techniques are not used. A ground plane is highly recommended. It should connect all areas of the pattern side of the printed circuit that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pickup. It eliminates parasitic circuits from what would otherwise be long, component leads.

Point-to-point wiring is not recommended. However, if point-to-point wiring is used, a single-point ground should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This eliminates common current paths or ground loops which can cause unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A 1μF CS13 tantalum capacitor is recommended. A parallel 0.01μF ceramic may be added if desired. This is especially important when driving high current loads. Properly bypassed and modulation free power supply lines allow full amplifier output and optimum settling time performance.

OPA600 circuit common is connected to pins 1 and 13; these pins should be connected to the ground plane. The input signal return, load return, and power supply common should also be connected to the ground plane.

The case of the OPA600 is internally connected to circuit common, and as indicated above, pins 1 and 13 should be connected to the ground plane. Ideally, the case should be mechanically connected to the ground plane for good thermal transfer but because this is difficult in practice, the OPA600 should be fully inserted into the printed circuit board with the case very close to the ground plane to make the best possible thermal connection. If the case and ground plane are physically connected or are in close thermal proximity, the ground plane will provide heat sinking which will reduce the case temperature rise. The minimum OPA600 pin length will minimize lead inductance, thereby maximizing performance.

To repeat, proper grounding is the single most important aspect of high frequency circuitry.

8.3 Compensation. The OPA600 uses external frequency compensation so that the user may optimize the bandwidth or settling time for his particular application. Several performance curves aid in the selection of the correct compensations capacitance value. The Bode plot shows amplitude and phase versus frequency for several values of compensation. A

related curve shows the recommended compensation capacitance versus closed-loop gain.

Figure 4 shows a recommended circuit schematic. Component values and compensation for amplifiers with several different closed-loop gains are shown. This circuit will yield the specified settling time. Because each device is unique and slightly different, as is each user's circuit, optimum settling time will be achieved by individually compensating each device in its own circuit, if desired. A 10% to 20% improvement in settling time has been experienced from the values indicated in Table I.

The primary compensation capacitors are C_1 and C_2 (see Figure 4). They are connected between pins 4 and 5 and between pins 11 and 14. Both C_1 and C_2 should be the same value. As Figure 4 and the performance curves show, larger closed-loop configurations require less capacitance and improved gain-bandwidth product can be realized. Note that no compensation capacitor is required for closed-loop gains equal to or above 100V/V. If upon initial application the user's circuit is unstable, and remains so after checking for proper bypassing, grounding, etc., it may be necessary to increase the compensation slightly to eliminate oscillations. Do not over compensate. It should not be necessary to increase C_1 and C_2 beyond 10pF to 15pF. **It may also be necessary to individually optimize C_1 and C_2 for improved performance.**

The flat high frequency response of the OPA600 is preserved and high frequency peaking is minimized by connecting a small capacitor in parallel with the feedback resistor (see Figure 4). This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1kΩ) and up to 10pF for circuits using larger resistances. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator is recommended to avoid using a large value resistor with its long time constant.

For heavy capacitive loads, greater than 50pF, refer to the section on capacitive loads, paragraph 8.6. For particularly difficult applications where the wiring layout may not be the best or where there may be 1000pF loads, parasitics, strays, long lead lengths, changing capacitive loads, etc., doublet compensation is recommended. This is discussed in paragraph 8.12 and is shown in Figure 9. This circuit offers increased stability at the expense of increasing the settling time by approximately 50%. Also, this circuit is especially useful for functional testing at low frequency and incoming inspection.

8.4 Settling time. Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition.

Settling time is a complete dynamic measure of the OPA600's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open-loop gain. Performance curves show the OPA600 settling time to ±1%, ±0.1%, and ±0.01%. The best settling time is achieved in low closed-loop gain circuits.

Settling time is dependent upon compensation. Under-compensation will result in small phase margin, overshoot or instability. Over-compensation will result in poor settling time. Refer to paragraph 8.3.

Figure 4 shows the recommended compensation to yield the specified settling tine. Improved or optimum settling time may be achieved by individually compensating each device in the user's circuit since individual devices vary slightly from one to another as do user's circuits.

8.5 Slew rate. Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or the small signal bandwidth. Slew rate is dependent upon compensation and decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve.

8.6 Capacitive loads. The OPA600 will drive large capacitive loads (up to 100pF) when properly compensated and settling times of under 150nsec are achievable. The effect of a capacitive load is to decrease the phase margin of the amplifier which may cause high frequency peaking or oscillations. A solution is to increase the compensation capacitance, somewhat slowing the amplifier's ability to respond. The recommended compensation capacitance value as a function of load capacitance is shown in Figure 7. (Use two capacitors, each with the value indicated.) Alternately, without increasing the OPA600's compensation capacitance, the capacitive load may be buffered by connecting a small resistance, usually 5Ω to 50Ω, in series with the Output, pin 8.

For very-large capacitive loads, greater than 100pF, it will be necessary to use doublet compensation. Refer to Figure 9 and paragraph 8.12. This places the dominant pole at the input stage. Settling time will be approximately 50% slower; slew rate should increase. Load capacitance should be minimized for optimum high frequency performance.

Because of its large output capability, the OPA600 is particularly well suited for driving loads via coaxial cables. Note that the capacitance of coaxial cable (29pF/foot of length for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

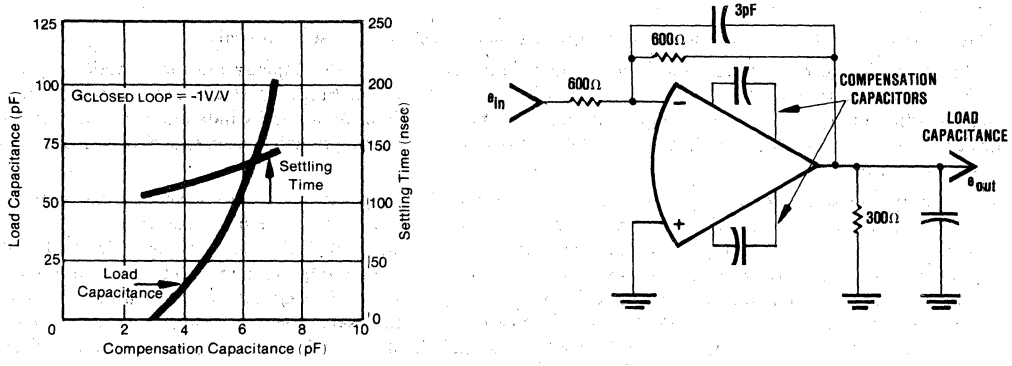


FIGURE 7. Capacitive Load Compensation and Response.

8.7 Offset voltage adjustment. The offset voltage of the OPA600 may be adjusted to zero by connecting a 5kΩ resistor in series with a 10kΩ linear potentiometer in series with another 5kΩ resistor between pins 2 and 15, as shown in Figure 3. It is important that one end of each of the two resistors be located very close to pins 2 and 15 to isolate and avoid loading these sensitive terminals. The potentiometer should be a small, noninductive type with the wiper connected to the positive supply. The leads connecting these components should be short, no longer than 0.5-inch, to avoid stray capacitance and stray signal pick-up. If the potentiometer must be located away from the immediate vicinity of the OPA600, extreme care must be observed with the sensitive leads. Locate the two 5kΩ resistors very close to pins 2 and 15.

Never connect $+V_{CC}$ directly to pin 2 or 15. Do not attempt to eliminate the 5kΩ resistors because at extreme rotation, the potentiometer will directly connect $+V_{CC}$ to pin 2 or pin 15 and permanent damage will result.

Offset voltage adjustment is optional. The potentiometer and two resistors are omitted when the offset voltage is considered sufficiently low for the particular application. For each microvolt of offset voltage adjusted, the offset voltage temperature sensitivity will change by $\pm 0.004 \mu V/^{\circ}C$.

8.8 Current boost. External ability to bypass the internal current limiting resistors has been provided in the OPA600. This is referred to as current boost. Current boost enables the OPA600 to deliver large currents into heavy loads (±200mA at ±10V). To bypass the resistors and activate the current boost, connect pin 7 to $-V_{CC}$ at pin 6 with a short lead to minimize lead inductance and connect pin 9 to $+V_{CC}$ at pin 12 with a short lead.

CAUTION - Activating current boost by bypassing the internal current limiting resistors can permanently damage the OPA600 under fault conditions. See paragraph 8.9.

Not activating current boost is especially useful for initial breadboarding. The 50Ω (±5%) current limiting resistor in the collector circuit of each of the output transistors causes the output transistors to saturate; this limits the power dissipation in the output stage in case of a fault. Operating with the current boost not activated may also be desirable with small-signal outputs (i.e.±1V) or when the load current is small.

Each resistor is internally capacitively-bypassed (0.01μF, ±20%) to allow the amplifier to deliver large pulses of current, such as to charge diode junctions or circuit capacitances and still respond quickly. The length of time that the OPA600 can deliver these current pulses is limited by the RC time constant.

The internal voltage drops, output voltage available, power dissipation, and maximum output current can be determined for the user's application by knowing the load resistance and computing:

$$V_{OUT} = 14 \left(\frac{R_{LOAD}}{50 + R_{LOAD}} \right)$$

This applies for R_{LOAD} less than 100Ω and the current boost not activated. When R_{LOAD} is large, the peak output voltage is typically ±11V, which is determined by other factors within the OPA600.

8.9 Short circuit protection. The OPA600 is a short-circuit-protected for momentary short to common (<5sec), typical of those encountered when probing a circuit during experimental breadboarding or troubleshooting. This is true only if pins 7 and 9 are open (current boost not activated). An internal 50Ω resistor is in series with the collector of each of the output transistors which under fault conditions will cause the output transistors to saturate and limit the power dissipation in the output stage. Extended application of an output short can damage the amplifier due to excessive power dissipation.

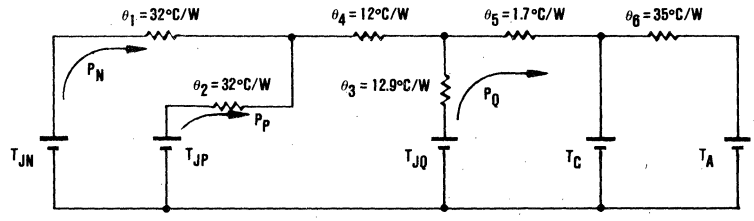
The OPA600 is not short-circuit-protected when the current boost is activated. The large output current capability of the OPA600 will cause excessive power dissipation and permanent damage will result even for momentary shorts to ground.

Output shorts to either supply will generally destroy the OPA600 whether the current boost is activated or not.

8.10 Heat sinking and power dissipation. The OPA600 is intended as a printed circuit board mounted device and as such, does not require a heat sink. It is specified for ambient temperature operation from -55°C to +125°C. However, the power dissipation must be kept within safe limits. At extreme temperature and under full load conditions, some form of heat sinking will be necessary. The use of a heat sink, or other heat dissipating means such as proximity to the ground plane, will result in cooler operating temperatures, better temperature performance, and improved reliability.

The thermal model used to describe the OPA600 is more complete than is usual for operational amplifiers. The thermal resistances for the output stages have been separated from the thermal resistrance for the balance of the OPA600. For most monolithic op amps and hybrids, thermal properties are usually represented by one thermal resistance, θJC; and in general, that is fairly accurate because the total power dissipation is low and the heat that is generated is in one area. For packaged power transistors, thermal properties are also accurately represented by one thermal resistance, θJC; all the power is dissipated in one point source. The OPA600 op amp however, has a large power handling capability and large power dissipations occur in different locations within the amplifier under differing load conditions.

The total power dissipation within the OPA600 is the sum of all the individual sources of dissipation. By making some simplifying assumptions and neglecting second order effects, the dissipations are grouped into three sources - quiescent power, NPN output transistor power, and PNP output transistor power. Using the thermal model shown in Figure 8 and the absolute maximum junction temperature rating (derate the maximum, if desired) and solving the Thevenin equivalent simultaneous equations that result, the user can determine junction, internal substrate, and case temperatures. It will be apparent that the output stages contribute significantly to the thermal rise. Under light loading, the requirements to dissipate the generated heat are much less than the requirements to dissipate heat under full load conditions at a maximum temperature. Using this expanded thermal information allows the user to safely apply the OPA600.



T_{JN} = Junction temperature of NPN output transistor.
T_{JP} = Junction temperature of PNP output transistor.
T_{JQ} = Worst case temperature of any device in the balance of the amplifier.
T_C = Case temperature.
T_A = Ambient temperature.
θ_1, θ_2 = Thermal resistance, output transistors.
θ_3, θ_4 = Thermal resistance, substrate.
θ_5 = Thermal resistance, substrate attach and package.
θ_6 = Thermal resistance, case to ambient.
P_N = Worst case power dissipation in the NPN output transistor.
P_P = Worst case power dissipation in the PNP output transistor.
P_Q = Quiescent power dissipation.

FIGURE 8. OPA600 Thermal Model.

Below are two examples of using the thermal model.

1. Find the worst case internal junction temperature rise above ambient.

Conditions: $P_Q = 1$ W
$P_N = P_P = 0.1$ W
no heatsink

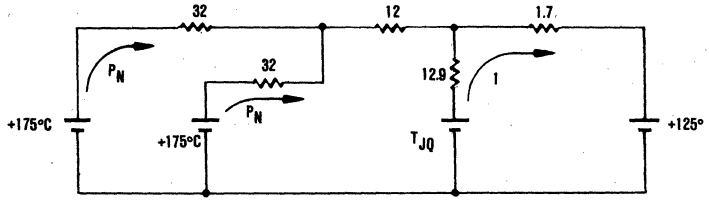
Solution: $T_{JN} = 80.7P_N + 48.7P_P + 36.7P_Q + T_A$
$T_{JN} - T_A = 49.6°C$
as $P_N = P_P$ $T_{JP} - T_A = 49.6°C$
$T_{JQ} = 49.6P_Q + 36.7P_N + 36.7P_P + T_A$
$T_{JQ} - T_A = 57°C$

Answer: 57°C

2. Find the maximum output stage power dissipation allowed with a maximum case temperature of +125°C and not exceeding the maximum junction temperature of +175°C.

Conditions: $P_Q = 1$ Watt
$P_N = P_P$

Solution:



$T_{JN} = P_N\ 32 + (P_N + P_P)12 + (P_N + P_P)\ 1.7 + P_Q\ 1.7 + T_C$
$175 = 59.4\ P_N + 1.7 + 125$
$P_N = 0.813W$

Checking T_{JQ}: $T_{JQ} = (1)\ 12.9 + (2x\ 0.813 + 1)\ 1.7 + 125$
$T_{JQ} = 142°C$ (i.e. $< 175°C$)

Answer: 0.813W may be dissipated in each output transistor.

It may be necessary to physically connect the OPA600 to the printed circuit board ground plane, attach fins, tabs, etc., to dissipate the generated heat. Because of the wide variety of possibilities, this task is left to the user. For all applications it is recommended that the OPA600 be fully inserted into the printed circuit board and that the pin length be short. Heat will be dissipated through the ground plane and the AC performance will be its best. See paragraphs 8.1 and 8.2

8.11 Testing. For static and low frequency dynamic measurements, the OPA600 may be tested in conventional operational amplifier test circuits, provided proper grounding techniques are observed, excessive lead lengths are avoided, and care is maintained to avoid parasitic oscillations. See the above sections, especially paragraphs 8.1 and 8.2. The circuit in Figure 9 is recommended for low frequency functional testing, incoming inspection, etc. This circuit is less susceptible to stray capacitance, excessive lead length, parasitic tuned circuits, changing capacitive loads, etc. It does not yield optimum settling time. We recommend placing a resistor (approximately 300Ω) in series with each piece of test equipment, such as a DVM, to isolate loading effects on the OPA600.

To realize the full performance capabilities of the OPA600, high frequency techniques must be employed and the test fixture must not limit the amplifier. Settling time is the most critical dynamic test and Figure 10 shows a recommended OPA600 settling time test circuit schematic. Good grounding, truly square drive signals, minimum stray coupling, and small physical size are important.

The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. A circuit that generates a ±5V flat topped pulse is shown in Figure 11.

Every OPA600 is thoroughly tested prior to shipment assuring the user that all parameters equal or exceed their specifications.

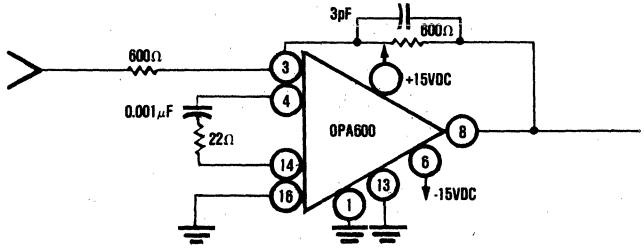


FIGURE 9. Amplifier Circuit for Increased Stability.

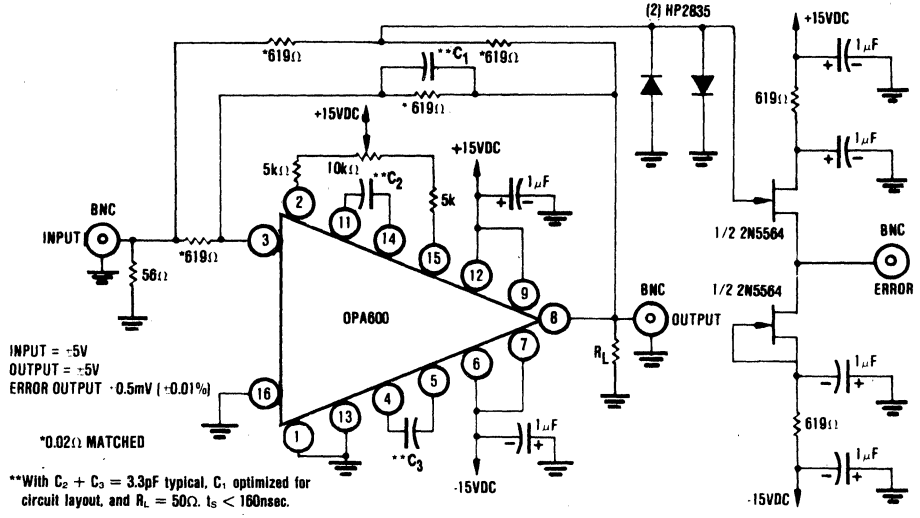


FIGURE 10. Settling Time and Slew Rate Test Circuit.

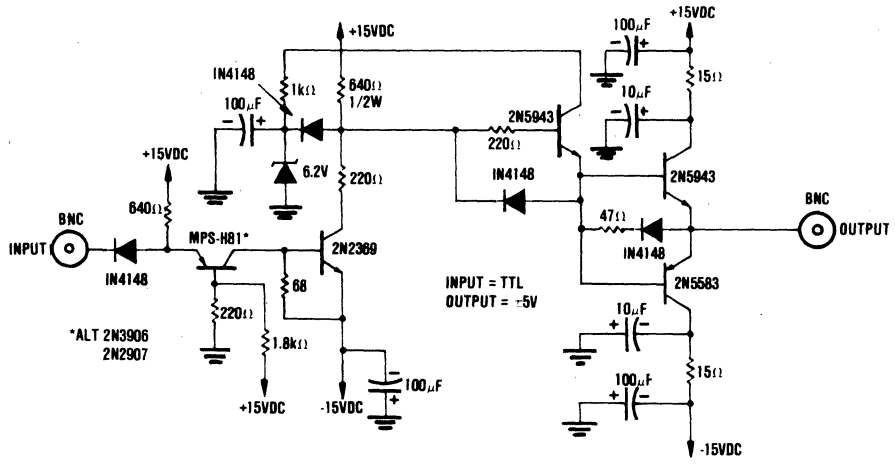


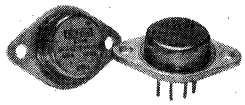
FIGURE 11. Flat Top Pulse Generator.

8.12 Increased Slew Rate. The OPA600 slew rate may be increased by using an alternate compensation shown in Figure 9. The slew rate will increase between 700 and 800V/μsec typical with 0.01% settling time increasing to between 175 and 190nsec typical and 0.1% settling time increasing to between 110 and 120nsec typical.

For alternate doublet compensation refer to Figure 9. For a closed-loop gain equal -1, delete C1 and C2 and add a series RC circuit (R = 22Ω, C = 0.001μF) between pins 14 and 4. Make no connections to pins 11 and 5. Absolutely minimize the capacitance to these pins. If a connector is used for the OPA600, it is recommended that sockets for pins 11 and 5 be removed. For a PC board mount, it is recommended that the PC board holes be overdrilled for pins 11 and 5 and adjacent ground plane copper be removed. Effectively this compensation places the dominant pole at the input stage, allowing the output stage to have no compensation and to slew as fast as possible. Bandwidth and settling time are impaired only slightly. For closed-loop gains other than -1, different values of R and C may be required.

BURR-BROWN®

OPA8780/MIL SERIES



MODEL NUMBERS:

OPA8780VM/MIL* **OPA8780UM/883B**
OPA8780VM/883B **OPA8780UM**
OPA8780VM

REVISION NONE
DECEMBER, 1983

High Voltage OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT SWING, ±30V
- LARGE LOAD CURRENT, ±60mA
- DIFFICULT TO DAMAGE, automatic thermal shutoff
- REDUCES SOURCE LOADING, 100GΩ input impedance
- PRESERVES SYSTEM ACCURACY, 106db CMR, 20pA bias current
- FAST SLEWING, 15V/μsec

APPLICATIONS

- LARGE SIGNAL DRIVERS
- HIGH POWER AUDIO AMPLIFIER

DESCRIPTION

The OPA8780 is the first military version integrated circuit operational amplifier that provides high output swings up to ±30V. The monolithic FET input stage has low bias current (20pA) which minimizes the offset voltage caused by the bias current and the large resistance normally associated with high voltage circuits.

The OPA8780 is packaged in a TO-3 package which will dissipate over 3W of power without a heat sink and 4.5W with a suitable heat sink.

The input stage is protected against overvoltage and the output stage is protected against short-circuits to ground. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

*Available 3rd quarter 1984

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a very-high accuracy, operational amplifier.

1.2 Part number. The complete part number is as shown below.

OPA8780	V	M	/MIL
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single operational amplifier. Two electrical performance grades are provided: the V grade (−55°C to +125°C) and U grade (−25°C to +85°C). The electrical performance characteristics are shown in Table I.

1.2.2 Device class. The device class is similar to the class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

Hi-Rel Product Designator	Requirements
/MIL	Standard model plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
/883B	Standard model, plus 100% MIL-STD-883 Class B screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is an 8-pin TO-3 package. Figure 1 depicts the case outline for the package.

1.2.4 Absolute maximum ratings.

Supply voltage range	±35VDC
Input voltage range	[±(V_{CC})−5]
Internal power dissipation	4.5W with heat sink
Case storage temperature range	−55°C to +150°C
Lead temperature (soldering, 60 sec.)	300°C

1.2.5 Recommended operating conditions.

Supply voltage range	±15VDC to ±35VDC
Case temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum $\theta J-C$
8-lead CAN	Figure 1	4.5W with heat sink at T_C +25°C	10°C/W with heat sink

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510—Microcircuits, general specification for.

STANDARD
MILITARY
MIL-STD-883—Test methods and procedures for microcircuits.

3. REQUIREMENTS

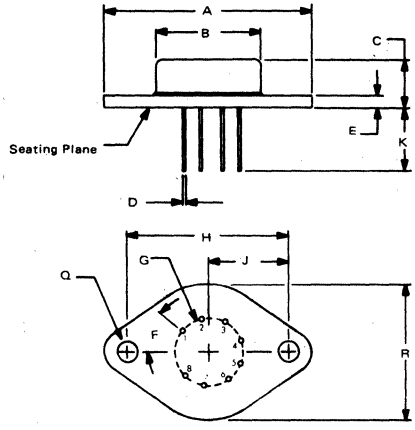
3.1. General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

FIGURE 1. Case Outline (TO-3) Package Configuration.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragrpah 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections for the TO-3 package are shown in Figure 2.

3.2.8 Glassivation. The microcircuit die is glassivated.

3.2.9 Schematics circuit. A simplified schematic circuit is shown in Figure 3.

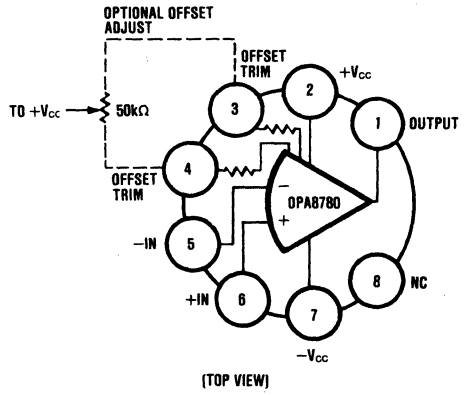


FIGURE 2. Connection Diagram.

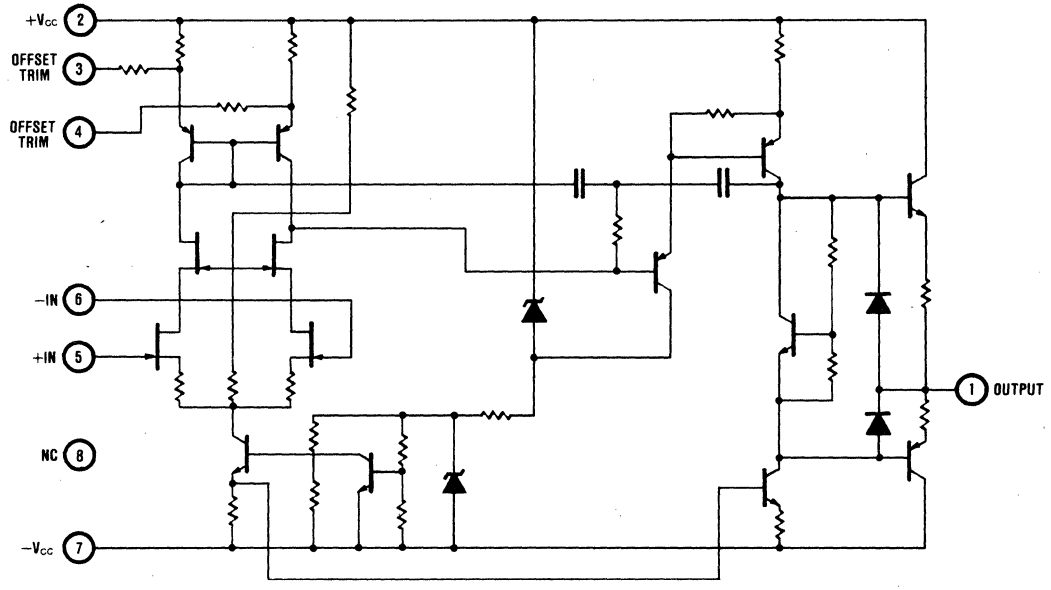


FIGURE 3. Simplified Schematic.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Additional electrical performance curves are shown in paragraph 7.

3.3.2 Offset null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 2. If nulling is unnecessary delete the potentiometer and make no connections.

TABLE I. Electrical Performance Characteristics.

All characteristics from $-55°C \leq T_C \leq +125°C$, $\pm V_{CC} = 35VDC$ unless otherwise noted.

CHARACTERISTICS	CONDITIONS	OPA8780VM/MIL OPA8780VM/883B OPA8780VM			OPA8780UM/883B OPA8780UM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Voltage $\pm V_{CC}$		±15		±35	*		*	V
Quiescent Current	$T_C = +25°C$			±10			*	mA
RATED OUTPUT								
Voltage (V_O)	$T_C = +25°C$	±10		±30	*		*	V
Current	$T_C = +25°C$	±60			*			mA
Current, Short Circuit		±70		±200	*		*	mA
Load Capacitance				10			*	nF
OPEN LOOP GAIN								
No Load, DC			106			*		dB
Rated Load, DC	$T_C = +25°C$	90			*			dB
FREQUENCY RESPONSE								
Unity Gain Bandwidth	Small Signal	5			*			MHz
Full Power Bandwidth			100			*		kHz
Slew Rate	$T_C = +25°C$	15	20		*	*		V/µsec
	$T_C = -25°C$	10	12		*	*		V/µsec
	$T_C = -55°C$	9	12					V/µsec
	$T_C = +85°C$	10	12		*	*		V/µsec
	$T_C = +125°C$	4	6					V/µsec
Settling Time	0.1%		12			*		µsec
INPUT OFFSET VOLTAGE								
Initial	$T_C = +25°C$		±1	±10			*	mV
	$T_C = -55°C$ to $+125°C$			±15				mV
	$T_C = -25°C$ to $+85°C$			±15			*	mV
Drift vs Temperature				30			50	µV/°C
Drift vs Supply Voltage			100			*		µV/V
Drift vs Time			100			*		µV/mo
INPUT BIAS CURRENT								
Initial	$T_C = +25°C$		±20	±50			*	pA
Drift vs Temperature			Doubles every 10°C			*		
Drift vs Supply Voltage			0.5			*		pA/V
INPUT OFFSET CURRENT								
Initial	$T_C = +25°C$		±20			*		pA
Drift vs Temperature			Doubles every 10°C			*		
Drift vs Supply Voltage			0.5			*		pA/V
INPUT IMPEDANCE								
Differential			100			*		GΩ
Common Mode			100			*		GΩ
INPUT NOISE								
Voltage	0.01Hz to 10Hz p-p		5			*		µV
	10Hz to 1000Hz rms		1			*		µV
Current	0.1Hz to 10Hz p-p		1			*		pA
INPUT VOLTAGE RANGE								
Max Safe Differential Voltage			$+V_{CC} + \lvert -V_{CC} \rvert$			*		V
Max Safe Common-Mode Voltage			$+V_{CC}$ to $-V_{CC}$			*		V
Common-Mode Voltage, Linear Operation			$\pm(\lvert V_{CC} \rvert - 8)$			*		V
Common-Mode Rejection			86			*		dB
TEMPERATURE RANGE [CASE]								
Operating		−55		+125	*		*	°C
Storage		−55		+150	*		*	°C
Specification		−55		+125	−25		+85	°C

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III).

MIL-STD-883 TEST REQUIREMENTS (Hybrid Class)	OPA8780VM/MIL	OPA8780VM/883B OPA8780VM	OPA8780UM/883B OPA8780UM
Interim electrical parameters (preburn-in) (method 5008)	1	1	1
Final electrical test parameters (method 5008)	1, 2, 3, 4	1, 2, 3, 4	1, 2U, 3U, 4
Group A test requirements (method 5008)	1*, 2, 3, 4	1, 2, 3, 4	1, 2U, 3U, 4
Group C end point electrical parameters (method 5008)	Table IV limits and delta limits	—	—

*PDA applies to subgroup 1 (see 4.3.c)

TABLE III. Group A Inspection.

			LIMITS				
			OPA8780VM/MIL OPA8780VM/883B OPA8780VM		OPA8780UM/883B OPA8780UM		
SUBGROUP	PARAMETERS	CONDITIONS	MIN	MAX	MIN	MAX	UNITS
4	Initial Input Offset Voltage	$T_C = +25°C$		±10		*	mV
	Slew Rate	$T_c = +25°C$, $R_L = 500\Omega$	15		*		V/μsec
2	Initial Input Offset Voltage	$T_C = +125°C$		±15			mV
	Slew Rate	$T_c = +125°C$, $R_L = 500\Omega$	4				V/μsec
2U	Initial Input Offset Voltage	$T_C = +85°C$		±15		*	mV
	Slew Rate	$T_c = +85°C$, $R_L = 500\Omega$	10		*		V/μsec
3	Initial Input Offset Voltage	$T_C = -55°C$		±15			mV
	Slew Rate	$T_c = -55°C$, $R_L = 500\Omega$	9				V/μsec
3U	Initial Input Offset Voltage	$T_c = -25°C$		±15		*	mV
	Slew Rate	$T_c = +25°C$, $R_L = 500\Omega$	10		*		V/μsec
1	Initial Input Offset Voltage	$T_C = +25°C$		±10		*	mV
	Quiescent Current	$T_C = +25°C$		±10		*	mA
	Initial Bias Current	$T_C = +25°C$		±50		*	pA
	Open-Loop Gain	$T_c = +25°C$, $R_L = 500\Omega$	90		*		dB
	Slew Rate	$T_c = +25°C$, $R_L = 500\Omega$	15		*		V/μsec
	Short-Circuit Current	$T_C = +25°C$, $R_{SC} = 10\Omega$	±70	±200	*	*	mA

*Specification is the same as for the V grade.

TABLE IV. Group C, End Point Electrical Parameters

($T_C = +25°C$, $\pm V_{CC} = \pm 35VDC$)

TEST	LIMIT	DELTA	UNITS
Quiescent Current	±10	±3	mA
Input Offset Voltage	±10	±5	mV
Slew Rate	15	±5	V/μsec
Open-Loop Gain	90	±10	dB
Short Circuit Current	±200	±25	mA
Bias Current	−50	±25	pA

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated in any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin (U.S.A.)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

1/ A 4-digit date code, indicating year and week of seal, and a 4- or 5-digit lot identifier is marked on each unit.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /MIL product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the /MIL product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for /MIL and /883B Hi-Rel product designations is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition A), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

For the /MIL product designations, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /MIL product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the /MIL and /883B Hi-Rel product designations is in accordance with MIL-STD-883, method 5008, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.

b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 4 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

c. Percent defective allowable (PDA). The PDA, for /MIL product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available form Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 (class B).

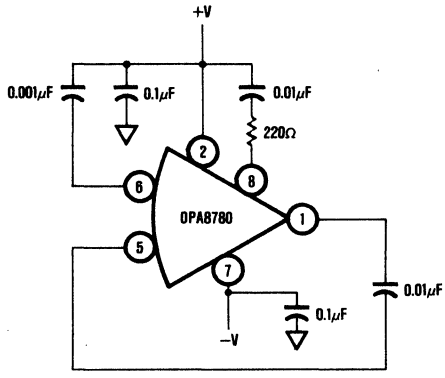


FIGURE 4. Burn-In Circuit.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 (class B), and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 4 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 (class B) and as follows:

a. End point electrical parameters are specified in Table IV herein.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage), are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

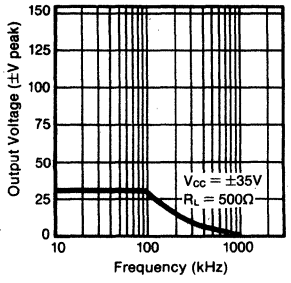
6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group H as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

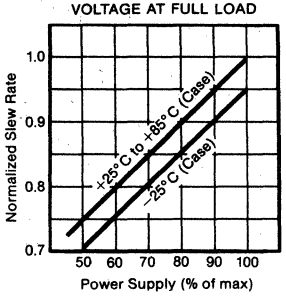
7. ELECTRICAL PERFORMANCE CURVES

T_{CASE} = +25°C and $\pm V_{CC}$ max unless otherwise noted.

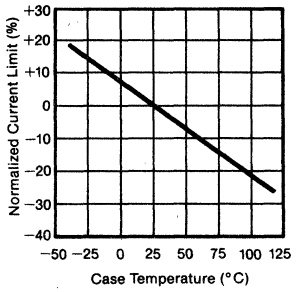
OUTPUT VOLTAGE VS FREQUENCY



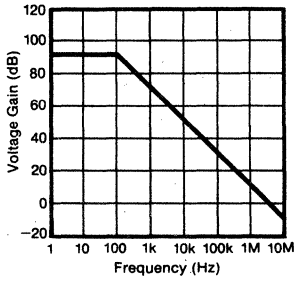
SLEW RATE VS SUPPLY VOLTAGE AT FULL LOAD



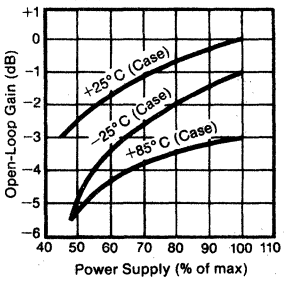
CURRENT LIMIT VS TEMPERATURE



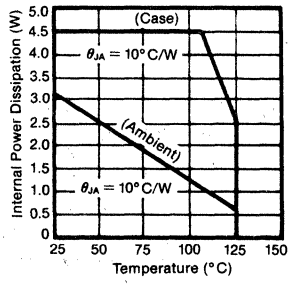
OPEN-LOOP FREQUENCY RESPONSE—FULL LOAD



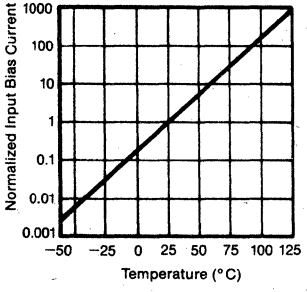
OPEN-LOOP GAIN VS SUPPLY VOLTAGE AT MAX LOAD



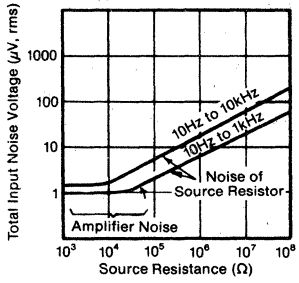
MAXIMUM POWER DISSIPATION



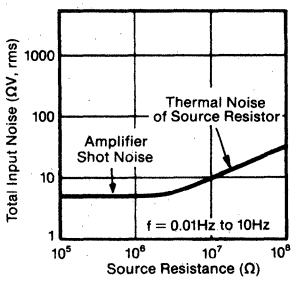
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



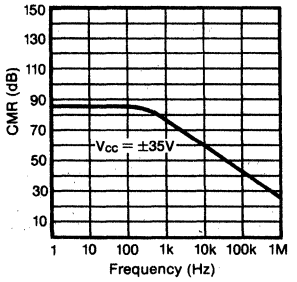
TOTAL INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



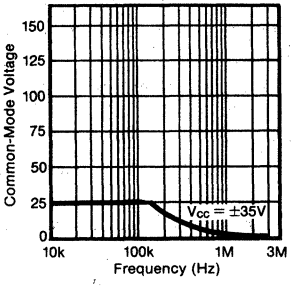
TOTAL LOW FREQUENCY INPUT NOISE VS SOURCE RESISTANCE



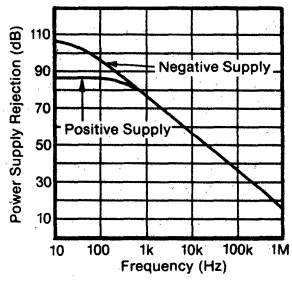
COMMON-MODE REJECTION VS FREQUENCY



MAXIMUM COMMON-MODE VOLTAGE VS FREQUENCY



POWER SUPPLY REJECTION VS FREQUENCY



8. APPLICATION INFORMATION

8.1 Offset voltage adjustment. If offset adjustment is necessary this may be done as indicated in Figure 2, by adding a 100kΩ potentiometer between pins 3 and 4 with the center tap connected to $+V_{CC}$.

8.2 Case connection. The case is electrically isolated. It is recommended that the case be grounded during use.

8.3 Single supply operation. It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 5 illustrates a typical application.

Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should also be noted that the OPA8780 is short-circuit limited, thermally protected, and protected from short circuits to ground.

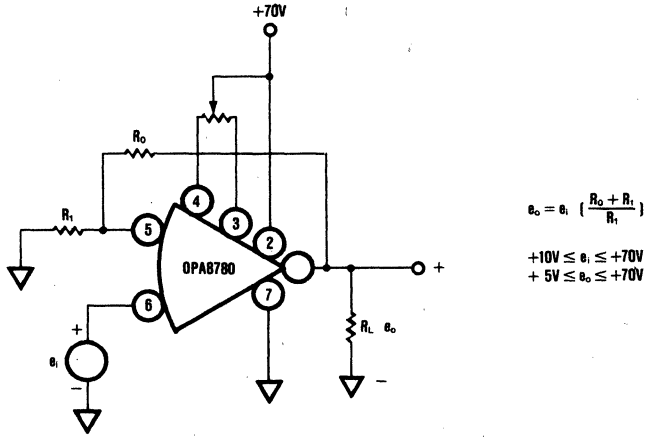


FIGURE 5. Operation From a Single Supply.

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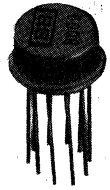


VFC32/MIL SERIES

MODEL NUMBERS:

VFC32WM/883B
VFC32WM
VFC32UM/883B
VFC32UM
VFC32VM/MIL
VFC32VM/883B
VFC32VM

REVISION C
APRIL, 1984

VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- **HIGH LINEARITY**
  - **±0.006% max (13 bits) and ±0.01% max (12 bits) at 10kHz FS**
  - **±0.05% max at 100kHz FS**
  - **±0.1% max at 200kHz FS**
- **HI-REL MANUFACTURE**
- **6-DECADE DYNAMIC RANGE**
- **OUTPUT DTL/TTL/CMOS COMPATIBLE**
- **V/F OR F/V CONVERSION**

DESCRIPTION

The VFC32 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple, low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families.

The converter requires two external resistors and two external capacitors to operate. One external resistor and one external capacitor set up the full scale frequency, with a guaranteed nonlinearity of ±0.1% maximum at 200kHz. The other capacitor is the one-shot capacitor; for best performance it should have a low temperature coefficient. The other resistor is a noncritical open collector pull-up resistor.

The VFC32/MIL Series converter is available in three electrical performance grades. The V grade has 200kHz specifications and tests. The W grade has premium linearity, ±0.006% of FSR, and premium full scale accuracy temperature coefficient of 100ppm/°C. The U grade is specified from -25°C to +85°C and from -55°C to +125°C. It is primarily for high performance test equipment, shipboard, ground support and industrial applications, where operation is normally between -25°C and +85°C and full temperature operation must be assured. All are packaged in welded, hermetically-sealed, TO-100 cans.

All devices are manufactured on a separate Hi-Rel manufacturing line with impeccable clean room conditions to assure "built-in" quality.

Three product assurance levels are available: standard, /883B, and /MIL. The standard models have many MIL-STD-883 screens performed routinely. The /883 suffixed devices are 100% screened per MIL-STD-883 method 5004 class B and each /MIL suffixed device is Hi-Rel manufactured, 100% screened per MIL-STD-883 method 5004 class B, and has 5% PDA.

Quality assurance further processes /MIL devices, performing group A and B inspections on each inspection lot and group C and D inspections periodically and when specified on the customer's purchase order. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
VOLTAGE-TO-FREQUENCY CONVERTER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a very linear, voltage-to-frequency converter. For the description of operation see paragraph 3.3.3.

1.2 Part Number. The complete part number is as shown below.

VFC32	V	M	/MIL
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, voltage-to-frequency converter; it will also function as a single, frequency-to-voltage converter. Three electrical performance grades are provided. The V grade features specifications and tests at 200kHz. The W grade features premium linearity (13 bits) and premium full scale accuracy. The U grade features specified and tested performance from -25°C to +85°C and maintains -55°C to +125°C operation.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the product assurance level class B, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level as follows:

Hi-Rel Product Designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
/883B	Standard model, plus 100% MIL-STD-883 class B screening.
(none)	Standard model including 100% electrical testing.

1.2.3. Case outline. The case outline is A-2 (10-lead can, TO-100) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±22VDC
Input voltage range, +input, pin 1	±22VDC 1/
Input voltage range, -input, pin 2	±22VDC 1/
Output pull-up supply voltage (V_{PU})	±22VDC 1/ 2/
Output sink current, pin 6	16mA
Comparator input voltage	±22VDC 1/
Output current pin 10	±20mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ V_{PU} is the supply voltage connected to pin 6 via R_S, see Figure 2.

1.2.5 Recommended operating conditions.

Supply voltage range	±11VDC to ±20VDC
Output pull-up supply (V_{PU})	+4.5VDC to +20VDC
Input voltage range, (V_{IN})	0VDC to +[0.00025 x (R_1 + R_3)]VDC 1/ 2/
	-10VDC to 0VDC 3/
Input current range, pin 2	0mA to +0.25mA
	0mA to +0.50mA 2/
Full scale frequency	100kHz 4/
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A	Maximum θ J-A
10-lead can (TO-100)	A-2	225mW at T_A = 125°C	70°C/W	150°C/W	220°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1. Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4. Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. The microcircuit die is glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

3.2.9 Schematic circuit. The functional schematic circuit is shown in Figure 1.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown within paragraph 7.

3.3.2 Connection diagram. The connection diagrams for voltage-to-frequency operation are shown in Figures 2 and 3. The connection diagram for frequency-to-voltage operation is shown in Figure 4.

1/ For positive input voltages (see Figure 2).
2/ For frequencies 100kHz to 200kHz 50% duty cycle is recommended (see paragraph 3.3.3.1).
3/ For negative input voltages (see Figure 3).
4/ For best line linearity.

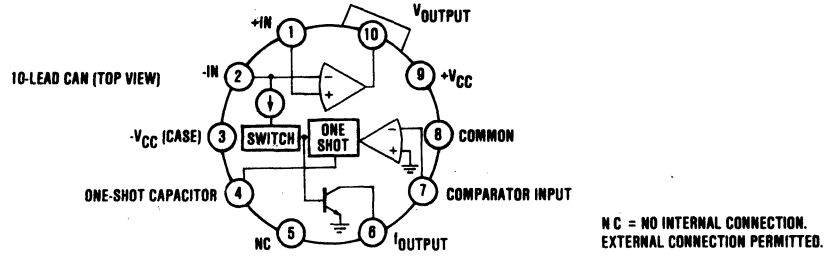


FIGURE 1. Terminal Connections and Functional Schematic Circuit.

3.3.3. Description of Operation. The input amplifier of the VFC is connected as an integrator (see Figure 2). When a positive input voltage is applied at V_{IN}, a constant current, $V_{IN}/(R_1 + R_3)$, will flow through the input resistor, $(R_1 + R_3)$, charging capacitor C_2. At this time the current sink is disabled as the switch is open and the VFC output, pin 6, is logic "0". The voltage at the amplifier output (comparator input) will ramp down from a positive voltage toward zero, according to $dv/dt = V_{IN}/[(R_1 + R_3)\,C_2]$. When the ramp reaches a voltage close to zero ($\approx$ -0.6V), the comparator changes state, and fires the one shot. Note, this period of time is a function of the input voltage, V_{IN}.

As the one-shot fires, the VFC output, pin 6, changes from logic "0" to logic "1", and the switch closes enabling the 1mA current sink. The length of time the one shot fires is determined by a reference (7.5V) within the one shot and the external one shot capacitor C_1. Note, this period of time is not a function of the input voltage. For good over temperature performance C_1 must have a low temperature coefficient. When the current sink is enabled, the current in the integrating capacitor, C_2, reverses direction and flows toward the summing junction. This occurs because the constant input current, $V_{IN}/(R_1 + R_3)$, is set up to always be less than the 1mA current sink. The voltage at the amplifier output ramps up according to $dv/dt = [(V_{IN}/(R_1 + R_3)) - (1mA)]/C_2$. Before the ramp voltage saturates the amplifier, the one shot resets.

When the one shot resets, the switch opens, the current sink is disabled, the VFC output changes back to logic "0" and the cycle repeats.

The total VFC period is determined by the following equations:

$$f_o = \frac{1}{t}$$

$$t = t_1 + t_2$$

$$t = \Delta V_{OUT}\, t_1 \frac{C_2}{V_{IN}/(R_1 + R_3)} + \Delta V_{OUT}\, t_2 \frac{C_2}{V_{IN}/(R_1 + R_3) - 1mA}$$

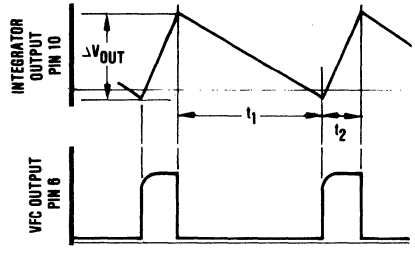
and:

$$-\Delta V_{OUT}\, t_1 = +\Delta V_{OUT}\, t_2$$

$$t_2 = C_1 \frac{7.5V}{1mA}$$

The equations reduce to:

$$f_o = \frac{V_{IN}}{7.5\,(R_1 + R_3)\,C_1}$$



Note, the output frequency is not dependent upon C_2, and the temperature coefficients of R_1, R_3, and C_1 are critical to the VFC's over-temperature performance. These temperature coefficient effects must be added to the drift specifications of the integrated circuit itself.

3.3.3.1 Duty cycle. The duty cycle (D) of the VFC is the percent the one-shot period (t_2) is of the total VFC period ($t_1 + t_2$). It is measured at the full scale input voltage, which is the full scale frequency.

$$D = \frac{t_2}{t_1 + t_2}$$

Duty cycle is related to the maximum input current and the 1mA (nominal) current sink. By reducing the equations for t_2 and f_o:

$$D = \frac{V_{IN}\,max/(R_1 + |R_3)}{1mA} = \frac{I_{IN}\,max}{1mA}$$

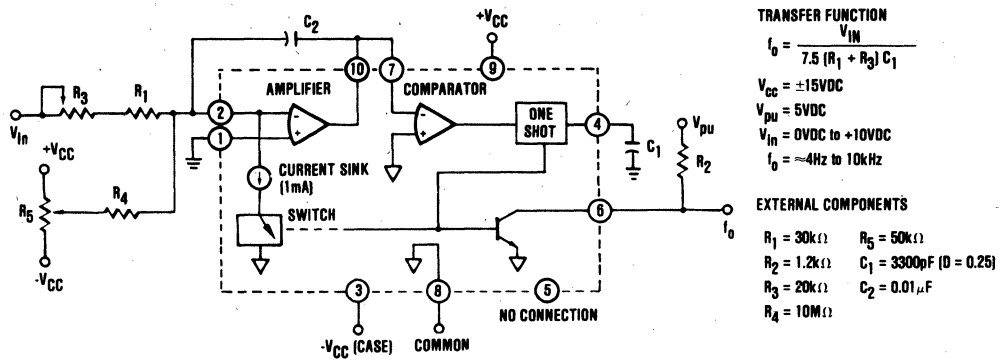


FIGURE 2. Connection Diagram, Voltage-to-Frequency Operation, Positive Input.

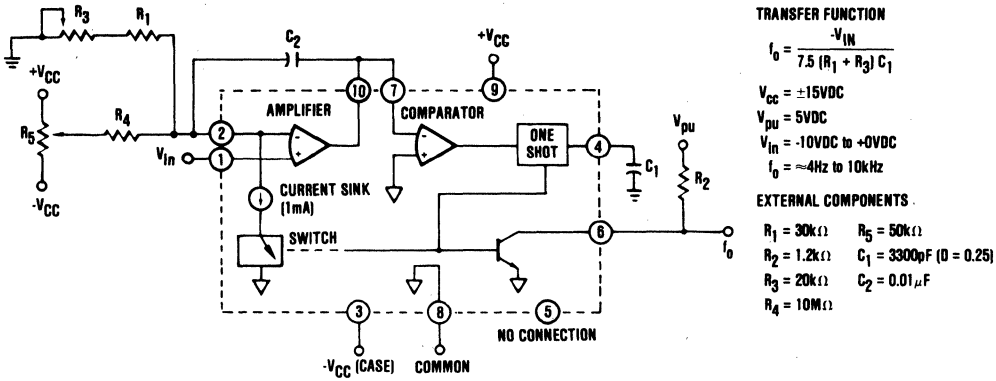


FIGURE 3. Connection Diagram, Voltage-to-Frequency Operation, Negative Input.

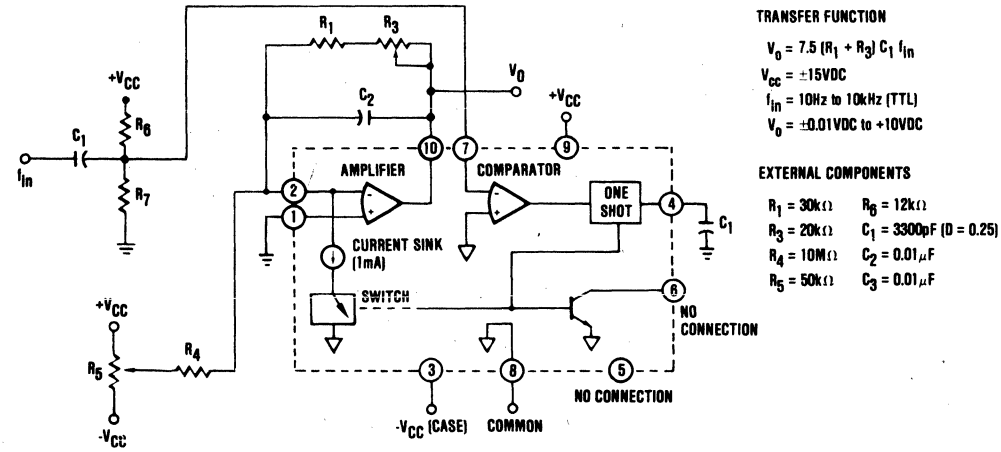


FIGURE 4. Connection Diagram, Frequency-to-Voltage Operation.

External component selection is typical. See paragraph 3.3.3.

The duty cycle (D) may be selected by the user to any value $\leq 70\%$ ($D \leq 0.70$). The 70% limit is due to component tolerances, offset, temperature effects, etc., and allowing 0.70mA as the minimum value for the 1mA (nominal) current sink, the worst case, maximum input current, $V_{IN}/(R_1 + R_3)$, is 0.50mA.

The normal, recommended duty cycle is 25% ($D = 0.25$) because this yields the best linearity. This is a maximum input current, $V_{IN}/(R_1 + R_3)$, of 0.25mA. The value of the external capacitor C_1 is the primary determinant of duty cycle and it is selected first; it determines the period t_2. Then the maximum input current, V_{IN} $(R_1 + R_3)$, is computed to satisfy the VFC transfer function, which determines the total VFC period, $t_1 + t_2$.

For frequencies above 100kHz, the recommended duty cycle is 50% ($D = 0.50$); that is, 0.50mA maximum input current. This provides additional time for t_2 and compensates for the inherent delay time within the integrated circuit. This additional time allows the output transistor to turn off, providing a logic "1" output pulse, especially at elevated temperature.

3.3.4. External component selection. Refer to Figures 2, 3, and 4 for examples of external components' selection. One-shot capacitor C_1. This capacitor determines the duration of the logic "1" output pulse. For a 25% duty cycle ($D = 0.25$), 0.25mA maximum input current, use the first equation and select the closest standard value. For any duty cycle, D, use the second equation.

$$C_1\,(pF) = \frac{33 \times 10^6}{f_{MAX}} - 30 \quad \text{or} \quad C_1\,(pF) = \frac{D \times 133 \times 10^6}{f_{MAX}} - 30 \qquad (150pF\ min)$$

The initial tolerance of this capacitor is not critical because R_3 can be adjusted to remove the initial gain error. The temperature coefficient is critical because it adds directly as a transfer function error. An NPO ceramic type capacitor is recommended. Every effort should be made to minimize parasitic capacitance and C_1 should be mounted as close as possible to the VFC.

Input resistor $R_1 + R_3$. $R_1 + R_3$ determines the magnitude of the input current which charges the integrating capacitor C_2. The total resistance is calculated according to

$$R_1 + R_3 = \frac{V_{IN}\ max}{I_{IN}}$$

Normally, I_{IN} is 0.25mA; refer to paragraph 3.3.3.1. R_1, as a percentage of the R_1 and R_3 total resistance, should be 90% minus the percent initial tolerance of C_1. R_3 is the initial gain error adjustment, and as a percentage of the $R_1 + R_3$ total resistance, R_3 should be 20% plus twice the percent initial tolerance of C_1. The initial tolerance of R_1 and R_3 are not critical, but the temperature coefficients are critical because they add directly as transfer function errors. If the input signal is current rather than a voltage, R_1 and R_3 are replaced with a short circuit, and the removal of a gain error then requires adjustment of C_1.

Trimming components R_4 and R_5. R_5 nulls the offset voltage of the input amplifier (VFC offset error). It should have a resistance between 10kΩ and 100kΩ and a temperature coefficient less than or equal to 100ppm °C. R_4 should be 10MΩ and may be a 20% carbon composition resistor.

Output pull-up resistor R_2. Select a 10% carbon composition resistor according to

$$R_{2\ min} = \frac{V\ pull\text{-}up}{5mA - I_{from\text{-}the\text{-}load}}$$

For high frequency operation, $f \geq 100kHz$, it is necessary to minimize the capacitive loading of the output terminal, pin 6, to allow the open collector output voltage to rise rapidly to logic "1". One way to shorten the time constant formed by the pull-up resistance and the capacitance at this node is to lower the pull-up resistance. A constant current supply of 5mA to the output terminal with a diode clamp works well. The best way to shorten the time constant is to minimize the capacitive loading. The use of a TTL buffer is effective.

Integrating capacitor C_2. C_2 is a function of the full scale frequency and is selected according to

$$C_2\,(\mu F) = \frac{10^2}{f_{max}} \qquad (0.001\mu F\ min)$$

Select the closest standard value to the calculated value. The initial tolerance and temperature coefficient are not critical since C_2 does not appear in the transfer function. The leakage current of C_2 is critical as it introduces a gain error. Select a capacitor type with small leakage compared to the full scale input current (0.25mA); a mylar type is recommended.

Frequency-to-voltage operation R_6, R_7, C_3.
To interface with TTL logic, the input should be coupled through a capacitor (C_3), and the minus input to the comparator, pin 7, biased near +2.5V (see Figure 4). The converter will detect the falling edge of the input pulse train as the voltage at

pin 7 crosses -0.6V. The converter will reset as the voltage at pin 7 goes positive and crosses +1.0V. Choose C_3 for an appropriate R_6, R_7, C_3 time constant such that the time, t, from -0.6V to +1.0V, meets the specified pulse width range requirements (Table I). For input signals with amplitudes less than 5V, it will be necessary to bias pin 7 closer to zero to insure that the input signal at pin 7 crosses the -0.6V threshold. Errors may be nulled (see paragraph 3.3.5) using 0.001 of full scale frequency to null the offset, and full scale frequency to null the gain error.

Power supply bypass capacitors. Each power supply should be bypassed to ground as close as possible to the converter with 0.01μF capacitors.

3.3.5. Offset and gain error null. The VFC is capable of being nulled to zero offset and zero gain error using the circuits shown in Figures 2, 3, and 4. R_5 effects zero offset error; R_3 effects zero gain error.

The offset and gain error null adjustment procedure is:

a. Apply an input voltage that should produce an output frequency of 0.001 of full scale.
b. Adjust R_5 for 0.001 of full scale frequency.
c. Apply full scale input voltage. 1/
d. Adjust R_3 for full scale frequency.
e. Repeat steps a through e.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

3.4 Electrical Tests. Electrical test requirements are as specified in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2).
b. Inspection lot identification code. 2/
c. Manufacturer's identification (BURR-BROWN®).
d. Manufacturer's designating symbol (CEBS).
e. Country of origin (U.S.A.).

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions for /MIL and /883B Hi-Rel product designations, including rebonding, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5004, class B, except as modified in paragraph 4.3.

For the standard model, Hi-Rel product designation (none), routine manufacturing processing includes Burr-Brown internal visual inspection, stabilization bake, fine leak, gross leak, constant acceleration, and external visual inspection per MIL-STD-883, method 5004, class B.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /MIL Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to mircocircuit delivery.

NOTE:

1. For optimum linearity it is recommended that gain error nulling be performed at 90% of full scale frequency rather than at 100% of full scale frequency.

2. A four-digit date code, indicating year and week of seal, is marked on 883B and (none) Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics

All characteristics T_A = -55°C to +125°C, $\pm V_{CC}$ = 15VDC, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	VFC32 V GRADE MIN	VFC32 V GRADE TYP	VFC32 V GRADE MAX	VFC32 W GRADE MIN	VFC32 W GRADE TYP	VFC32 W GRADE MAX	VFC32 U GRADE MIN	VFC32 U GRADE TYP	VFC32 U GRADE MAX	UNITS
INPUT (V/F CONVERTER)											
Bias current	T_A = +25°C										
Inverting input			10	40		•	•		•	•	nA
Noninverting input			50	100		•	•		•	•	nA
Offset voltage 1/	T_A = +25°C		1	4		•	•		•	•	mV
Differential impedance	T_A = +25°C	330 ‖ 10	650 ‖ 10		•	•		•	•		kΩ ‖ pF
Common-mode impedance	T_A = +25°C	300 ‖ 3	500 ‖ 3		•	•		•	•		MΩ ‖ pF
INPUT (F/V CONVERTER)											
Impedance	T_A = +25°C	50 ‖ 10	150 ‖ 10		•	•		•	•		kΩ ‖ pF
Logic "1"		+1.0		+V_{CC}	•		•	•		•	V
Logic "0"		-V_{CC}		-0.6	•		•	•		•	V
Pulse-width range		0.1		150k/F_{MAX}	•		•	•		•	μsec
ACCURACY											
Linearity error 2/	T_A = +25°C, 0.01Hz ≤ oper freq ≤ 10kHz		±0.005	±0.010 3/		±0.003	±0.006		±0.005	±0.010	% of FSR 4/
	T_A = +25°C, 10kHz ≤ oper freq ≤ 100kHz		±0.025	±0.050		•	•		•	•	% of FSR
	T_A = +25°C, 100kHz ≤ oper freq ≤ 200kHz		±0.050	±0.100		•	•		•	•	% of FSR
Offset error (input offset voltage) 1/	T_A = +25°C			±4			•			•	mV
Offset drift 5/	-25°C to +85°C			±3			±3			±3	ppm of FSR/°C
	-55°C to +125°C			±3			±3			±9	ppm of FSR/°C
Gain error 1/	T_A = +25°C		5	10		•	•		•	•	% of FSR
Gain drift 5/	f = 10kHz -25°C to +85°C						±100			±150	ppm/°C
	f = 10kHz -55°C to +125°C			±200			±100			±300	ppm/°C
Full scale drift (offset drift & gain drift) 5/6/	f = 10kHz -25°C to +25°C				-100	-50	0	-150		+50	ppm of FSR/°C
	+25°C to +85°C				0	+25	+100	-50		+150	ppm of FSR/°C
	f = 10kHz -55°C to +25°C	-200	-50	+100	-100	-50	0	-300		+100	ppm of FSR/°C
	+25°C to +125°C	-100	+50	+200	0	+50	+100	-100		+300	ppm of FSR/°C
	f = 200kHz -55°C to +25°C	-400	-200	0							ppm of FSR/°C
	+25°C to +125°C		0	±150							ppm of FSR/°C
Power supply sensitivity	f = DC, $\pm V_{CC}$ = 12VDC to 18VDC		±0.030	±0.040		•	•		•	•	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, logic "0"	I_{SINK} = 8mA	0	0.2	0.4	•	•	•	•	•	•	V
Leakage current, logic "1"	V_O = 15V T_A = +25°C		0.01	1.0		•	•		•	•	μA
Voltage, logic "1"	External pull-up resistor required (see Figure 2)			V_{PU}			•			•	V
Pulse width			0.25/F_{MAX}			•			•		sec
Fall time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			•			•	nsec
OUTPUT (F/V CONVERTER)											
Voltage	I_o = 7mA, T_A = +25°C	0 to +10			•			•			V
Current	V_O = 7VDC	+10			•			•			mA
Impedance	Closed loop			0.1			•			•	Ω
Capacitive load	Without oscillation			100			•			•	pF
DYNAMIC RESPONSE											
Full scale frequency		200			•			•			kHz
Dynamic range		6			•			•			decades
Settling time	(V/F) to specified linearity, ΔV_{IN} = 10V		7/			•			•		
Overload recovery	<50% overload		7/			•			•		
POWER SUPPLY											
Quiescent current	T_A = +25°C		±4.5	±6.0		•	•		•	•	mA
TEMPERATURE RANGE (ambient)											
Operating		-55		+125	•		•	•		•	°C
Storage		-65		+150	•		•	•		•	°C

*Specification the same as V grade.

NOTES:

1/ Adjustable to zero. See paragraph 3.3.5.

2/ Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See paragraph 7.

3/ ±0.015% of FSR for negative inputs.

4/ FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).

5/ Exclusive of external components' drift.

6/ Positive drift is defined to be increasing frequency with increasing temperature.

7/ One pulse of new frequency plus 1μsec.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MODELS	VFC32VM/MIL	VFC32VM VFC32VM/883B	VFC32WM VFC32WM/883B	VFC32UM VFC32UM/883B
MIL-STD-883 test requirement (class B)	SUBGROUPS (SEE TABLE III)			
Interim electrical parameters (preburn-in) (method 5004)	1	1	1	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 5U, 6, 6U	1, 2, 3, 4, 5, 5U, 6, 6U
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6	--	--	--
Groups C and D end point electrical parameters (method 5005)	Table IV	--	--	--

*PDA applies to subgroup 1 (see 4.3.c).

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	CONDITIONS $+V_{CC}$ = 15V, unless otherwise specified	LIMITS VFC32 V GRADE MIN	VFC32 V GRADE MAX	VFC32 W GRADE MIN	VFC32 W GRADE MAX	VFC32 U GRADE MIN	VFC32 U GRADE MAX	UNITS
1	Input offset voltage			4		*		*	mV
T_A = +25°C	Input bias current (inverting input)			40		*		*	nA
	Input bias current (noninverting input)			100		*		*	nA
	Output logic "0"	Pin 6 I_{SINK} = 8mA		0.4		*		*	V
	Output leakage current (logic 1)	Pin 6 V_{OUT} = 15V		1.0		*		*	µA
	Quiescent current	$+V_{CC}$ and $-V_{CC}$		±6.0		*		*	mA
2									
T_A = +125°C	Output logic "0"	Pin 6 I_{SINK} = 5mA		0.4		*			V
3									
T_A = -55°C	Output logic "0"	Pin 6 I_{SINK} = 5mA		0.4		*			V
4									
T_A = +25°C	Gain error, unadjusted	f = $f_{FULL\ SCALE}$= 200kHz		±20					kHz
	Linearity error	f = 200kHz		±200					Hz
	$f_{FULL\ SCALE}$ = 200kHz 1/	f = 150kHz		±200					Hz
		f = 100kHz		±100					Hz
		f = 50kHz		±100					Hz
		f = 10kHz		±20					Hz
		f = 5kHz		±20					Hz
		f = 1kHz		±20					Hz
	Gain error, unadjusted	f = $f_{FULL\ SCALE}$= 10kHz				±1		±1	kHz
	Linearity error	f = 10kHz				±0.6		±1	Hz
	$f_{FULL\ SCALE}$ = 10kHz 1/	f = 7kHz				±0.6		±1	Hz
		f = 5kHz				±0.6		±1	Hz
		f = 1kHz				±0.6		±1	Hz
		f = 0.5kHz				±0.6		±1	Hz
		f = 0.1kHz				±0.6		±1	Hz
5									
T_A = +125°C	Full scale drift	f = 200kHz 2/ +25°C to +125°C	-3.0	+3.0					kHz
	Full scale drift	f = 10kHz 2/ +25°C to +125°C			0	+100			Hz
5U									
T_A = +85°C	Full scale drift	f = 10kHz 2/ +25°C to +85°C			0	+60	-30	+90	Hz
6									
T_A = -55°C	Full scale drift	f = 200kHz 2/ -55°C to +25°C	-6.4	0					kHz
	Full scale drift	f = 10kHz 2/ -55°C to +25°C			-80	0			Hz
6U									
T_A = -25°C	Full scale drift	f = 10kHz 2/ -25°C to +25°C			-50	0	-75	+25	Hz

*Limits the same as V grade.

NOTE:

1/ Linearity error is adjusted or normalized to zero at 90% of full scale frequency and at 0.1% of full scale frequency.

2/ Subtract the frequency at the colder temperature from the frequency at the hotter temperature.

TABLE IV. Groups C and D, End Point Electrical Parameters (T_A = +25°C, $\pm V_{CC}$ = 15VDC).

TEST	LIMITS VFC32VM/MIL
Input Offset Voltage	4mV
Input Bias Current (-)	40nA
Input Bias Current (+)	100nA
Full Scale Drift	±3kHz (Hot) -6.4kHz, 0Hz (Cold)

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005 except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices. The following additional criteria apply:

a. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) T_A = +125°C minimum
   (4) Test duration is 160 hours minimum
c. Percent defective allowable (PDA). The PDA, for MIL Hi-Rel Product designations only, is 5 percent based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5004, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter test prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
d. External visual inspection need not include measurement of case and lead dimensions.

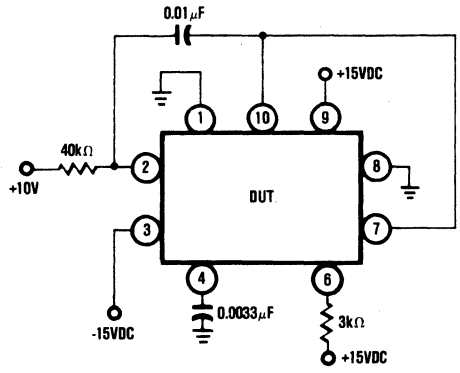


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5005, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5005. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table I and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table II (class B).

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table III, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.

4.4.4. Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table IV, and as follows:

a. End point electrical parameters are specified in Table IV herein.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group D as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. Caution - these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

7. DISCUSSION OF SPECIFICATIONS.

7.1 Linearity. Linearity is the maximum deviation of the actual transfer function from the straight line intersecting 90% of the full scale frequency (90% of full scale input) and 0.1% of the full scale frequency (≈ zero input). Linearity is the true measure of a VFC's performance. Linearity error is a function of the full scale frequency as shown in Figure 6. For a given full scale frequency the linearity error decreases with decreasing operating frequency as shown in Figure 7. To allow the user to benefit with improved linearity at lower frequencies, linearity error is specified in bands of operating frequency (see Table I).

7.2 Frequency stability versus temperature. The full scale frequency drift of the VFC32 versus temperature is shown in Figure 8. The temperature coefficient effects of the external components (especially R_1 and C_1) must be added to the drift of the converter.

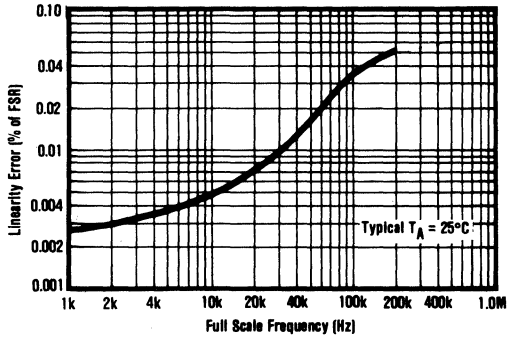


FIGURE 6. Linearity Error vs Full Scale Frequency.

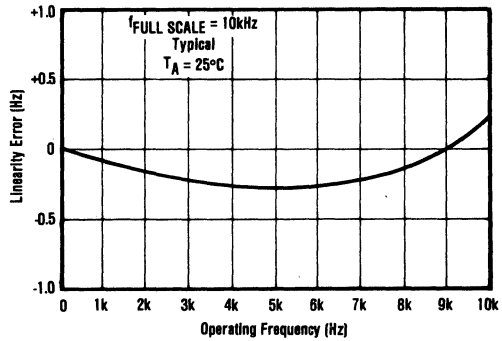


FIGURE 7. Linearity Error vs Operating Frequency.

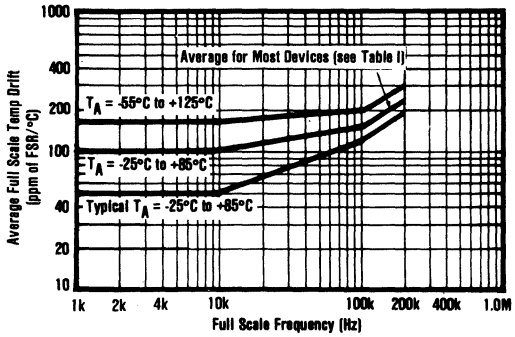


FIGURE 8. Full Scale Drift vs Full Scale Frequency.

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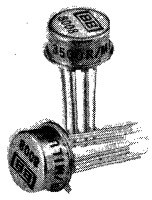


3500/MIL SERIES

MODEL NUMBERS:
3500R/MIL
3500R/883B
3500U/883B

REVISION A
OCTOBER, 1981

General Purpose - Military OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, ±30nA, MAX
- LOW DRIFT, ±20μV/°C, MAX
- LOW NOISE, 1.4μV, rms
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- HI-REL MANUFACTURE

APPLICATIONS

- GENERAL PURPOSE AMPLIFIER
- ANALOG COMPUTATION
- PRECISION BUFFER
- LOW DRIFT INTEGRATOR
- BRIDGE AMPLIFIER
- STABLE REFERENCE CIRCUITS

DESCRIPTION

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high impedance, both differential and common-mode.

The 3500 is also a low noise IC op amp. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated for unconditional stability for all feedback configurations, even with capacitive loads. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30 volts, thus the amplifier can be used as a sensitive comparator. The output stage is internally current-limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.

These devices are manufactured in a hi-rel environment with clean room conditions which assures "built-in" quality. Each device is 100% internally visually inspected per MIL-STD-883 method 2010 and after the cap is welded on, the balance of the MIL-STD-883 method 5004 class B screening is completed.

The /MIL suffixed devices are processed further by Quality Assurance, performing groups A and B inspections on each inspection lot and groups C and D inspections when specified on the customer's purchase order. A report containing the most recent groups A, B, C, and D tests is available for a nominal charge.

The R grade devices offer the best performance over the ambient temperature range of -55°C to +125°C. However, if the operating ambient temperature range will not exceed -25°C to +85°C, such as with test equipment, the U grade device provides full performance at lower cost.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

3500	R	/MIL
Basic model number	Grade (see 1.2.1)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, operational amplifier. Two electrical performance grades are provided, the R grade and the U grade, with the R grade offering the higher electrical performance.

1.2.2 Device class. The device class is similar to the product assurance level class B, as defined in MIL-M-38510.

The Hi-Rel product designator portion of the part number distinquishes the product assurance level as follows.

Hi-Rel product designator	Requirements
/MIL	**Basic model, plus 100% MIL-STD-883 class B screening with 5% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and periodically thereafter.**
/883B	Basic model, plus 100% MIL-STD-883 class B screening.

1.2.3 Case outline. The case outline (8-lead can) is as defined in Figure 4. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC 1/
Differential input voltage range	±40VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±3VDC to ±20VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A
8-lead can	FIGURE 4	225mW at T_A = 125°C	70°C/W	220°C/W

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Short circuit may be to ground only. Rating applies to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead finish is gold plate. The lead material and finish is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. The microcircuit die is glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

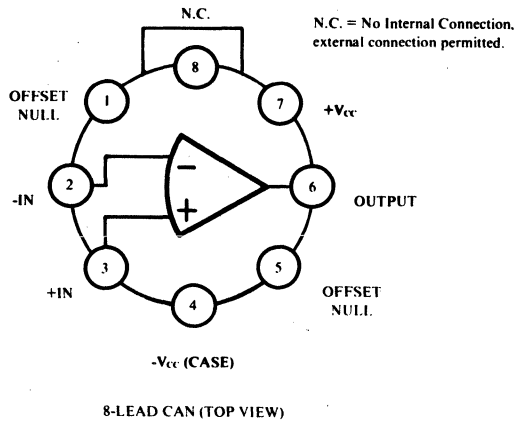


FIGURE 1. Terminal Connections.

FIGURE 2. Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Offset and gain error null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 2. If nulling is unnecessary for the application, delete the potentiometer and make no connections.

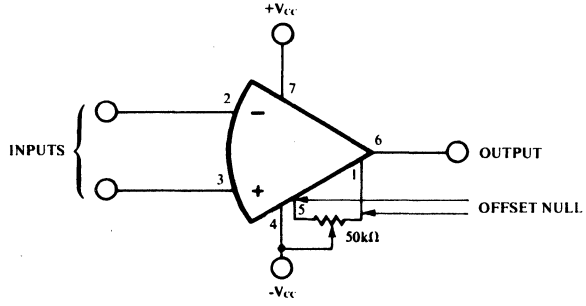


FIGURE 2. Offset Null Circuit.

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated at any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table III. The sub-groups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcirucit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin (U.S.A)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions for the MIL Hi-Rel product designation, including rebonding, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening is in accordance with MIL-STD-883, method 5004, class B, except as modified in paragraph 4.3 herein.

For the /MIL Hi-Rel product designator, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection for the MIL Hi-Rel product designation is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

1/ A four-digit data code, indicating year and week of seal, is marked on /883B Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics.

All characteristics at -55°C ≤ T_A ≤ +125°C, $\pm V_{CC}$ = 15VDC, unless otherwise specified.

Characteristics	Symbol	Conditions		3500R MIL 3500R 883B Min	Typ	Max	3500U/883B Min	Typ	Max	Units
OUTPUT										
Voltage	V_O	R_L = 1kΩ		±10	±12		*	*		V
Current	I_O	R_L = 1kΩ		±10			*			mA
Resistance	R_O				2			*		kΩ
Current, short circuit	I_{OS}	To ground	T_A = 25°C	±10	±22		*	*		mA
OPEN-LOOP VOLTAGE GAIN	A_{VS}	f = 0Hz, No load		93	106		*	*		dB
DYNAMIC RESPONSE										
Bandwidth	BW	Unity gain	T_A = 25°C	1	1.5	2	*	*	*	MHz
			-55°C ≤ T_A ≤ +125°C	0.75	1.2		*	*		MHz
Bandwidth, full power	BW_{FP}		T_A = 25°C	10	25		*	*		kHz
Slew rate	SR		T_A = 25°C	0.6	1.2		*	*		V/μsec
			-55°C ≤ T_A ≤ +125°C	0.4			*			V/μsec
INPUT										
Offset voltage	V_{IO}	V_{CM} = 0	T_A = 25°C		±2	±5		*	*	mV
Offset voltage temperature sensitivity	$\Delta V_{IO}/\Delta T$		-25°C ≤ T_A ≤ +85°C						±20	μV/°C
			-55°C ≤ T_A ≤ +125°C			±20			±60	μV/°C
Bias current	I_B	V_{CM} = 0	T_A = 25°C		±10	±30		*	*	nA
Bias current temperature sensitivity	$\Delta I_B/\Delta T$		-25°C ≤ T_A ≤ +85°C						±1.0	nA/°C
			-55°C ≤ T_A ≤ +125°C			±1.5			±3.0	nA/°C
Offset current	I_{IO}	V_{CM} = 0	T_A = 25°C		±10	±30		*	*	nA
Offset current temperature sensitivity	$\Delta I_{IO}/\Delta T$		-25°C ≤ T_A ≤ +85°C					±0.5	±1.0	nA/°C
			-55°C ≤ T_A ≤ +125°C		±0.7	±1.5			±3.0	nA/°C
Power supply rejection	PSRR		T_A = 25°C		±40			*		μV/V
Common-mode voltage range	CMV	Linear operation	T_A = 25°C	±11	±12		*	*		V
Common-mode rejection	CMR	V_{CM} = ±10V	T_A = 25°C	90	100		*	*		dB
			-55°C ≤ T_A ≤ +125°C	80			*			dB
Impedance	Z_{IS}	T_A = 25°C	Differential		10^7 || 3			*		Ω || pF
			Common mode		10^9 || 3			*		Ω|| pF
Noise voltage	e_n	0.3Hz to 10Hz	T_A = 25°C		2	3		*	*	μV, p-p
		10Hz to 10kHz	T_A = 25°C		1.4	2		*	*	μV, rms
Noise, current	i_n	0.3Hz to 10Hz	T_A = 25°C		200	300		*	*	pA, p-p
		10Hz to 10kHz	T_A = 25°C		35	100		*	*	pA, rms
POWER SUPPLY										
Quiescent current	I_Q		T_A = 25°C		±2.5	±3.5		*	*	mA
TEMPERATURE RANGE (ambient)										
Operating				-55		+125	-55		+125	°C
Storage				-65		+150	-65		+150	°C

Notes:
*Specifications the same as 3500R/MIL.

TABLE II. Electrical Test Requirements.
(The individual tests within the subgroups appear in Table III.)

MODELS / MIL-STD-883 Test Requirement (class B)	3500R/MIL	3500R/883B 3500U/883B
	SUBGROUPS (see Table III)	
Interim electrical parameters (pre burn-in)(method 5004)	1	1
Final electrical test parameters (method 5004)	1*, 2, 4, 5, 6	1, 2A, 4, 5, 6
Group A test requirements (method 5005)	1, 2, 4, 5, 6	---
Groups C and D end point electrical parameters (method 5005)	Table IV delta limits and limits	---
Additional electrical subgroups for group C inspections	7	---

*PDA applies to subgroup 1 (see 4.3d)

TABLE III. Group A Inspection

Subgroup	Symbol	MIL-STD-883 method or equivalent	Conditions $\pm V_{CC}$ = 15V unless otherwise specified	Limits				Units
				3500R/MIL. 3500R/883B		3500U/883B		
				Min	Max	Min	Max	
1	V_{IO}	4001			±5		±5	mV
T_A = 25°C	I_B	4001			±30		±30	nA
	I_{IO}	4001			±30		±30	nA
	I_Q	4005			±3.5		±3.5	mA
	CMR	4003	V_{CM} = ±10V	90		90		dB
2	$\Delta V_{IO}/\Delta T$	4001			±20			µV/°C
T_A = +125°C	$\Delta I_B/\Delta T$	4001			±1.5			nA/°C
to	$\Delta I_{IO}/\Delta T$	4001			±1.5			nA/°C
T_A = -55°C								
2A	$\Delta V_{IO}/\Delta T$	4001					±20	µV/°C
T_A = +85°C	$\Delta I_{IB}/\Delta T$	4001					±1.0	nA/°C
to	$\Delta I_O/\Delta T$	4001					±1.0	nA/°C
T_A = -25°C								
4	A_{VS}	4004	f = 0Hz, no load	93		93		dB
T_A = 25°C	SR	4002		0.6		0.6		V/µsec
5	A_{VS}	4004	f = 0Hz, no load	93		93		dB
T_A = +125°C	SR	4002	G = +1, ΔV_o = 10V, R_L = 1kΩ	0.4		0.4		V/µsec
6	A_{VS}	4004	f = 0Hz, no load	93		93		dB
T_A = -55°C	SR	4002	G = +1, ΔV_o = 10V, R_L = 1kΩ	0.4		0.4		V/µsec
7	e_n		0.3Hz to 10Hz		3			µV, p-p
T_A = 25°C			10Hz to 10kHz		2			µV, rms
	i_n		0.3Hz to 10Hz		300			pA, p-p
			10Hz to 10kHz		100			pA, rms

TABLE IV. Groups C and D, End Point Electrical Parameters
(T_A = +25°C, $\pm V_{CC}$ = 15, V_{CM} = 0V)

Test	Limit	Delta
V_{IO}	±5mV	±2.5mV
I_{IB}	±36nA	±30nA

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005 except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

Burr-Brown has performed and successfully completed qualification inspection as described below. The qualification report is available from Burr-Brown.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

4.3 Screening. Screening is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition D, Y_1 axis only.

b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 3 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for the /MIL Hi-Rel product designation only, is 5 percent based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with MIL-STD-883, method 5004, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter test prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

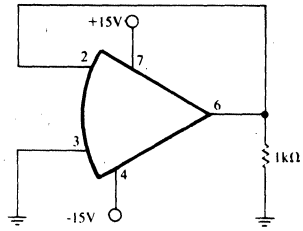


FIGURE 3 Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5005, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5005. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table I, and as follows:

a. Tests are specified in Table II herein.

b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table II (class B).

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table III, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 3 herein
   (3) $T_A = 125°C$ minimum
   (4) Test duration is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table IV, and as follows:

a. End point electrical parameters are specified in Table IV herein.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

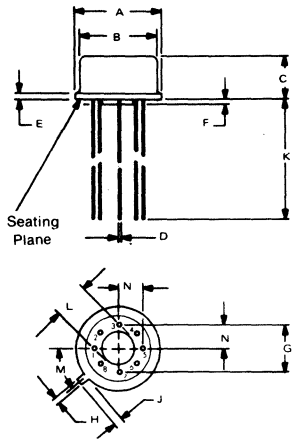
a. Complete part number (see paragraph 1.2)

b. Requirement for certificate of compliance, if desired.

6.4 Substitutability. Mircocircuits furnished under this specification are similar to Burr-Brown model 3500.

6.5 Microcircuit group assignment. These mircocircuits are assigned to Technology Group D as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.



NOTE:
Leads in true position within 0.10" (25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.
Weight: 3 grams max.

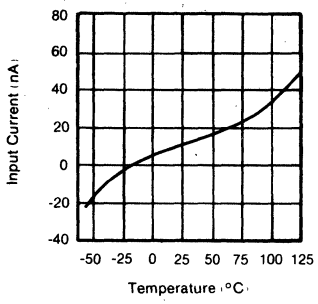
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 4. Case Outline (TO-99 Package Configuration).

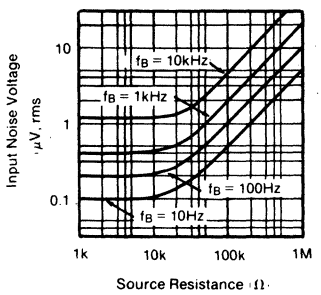
7. ELECTRICAL PERFORMANCE CURVES.

(Typical at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise specified).

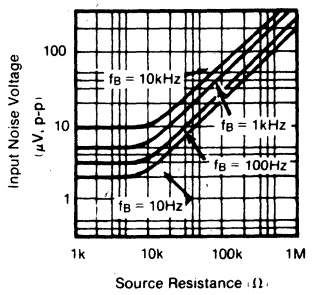
INPUT BIAS CURRENT vs. TEMPERATURE



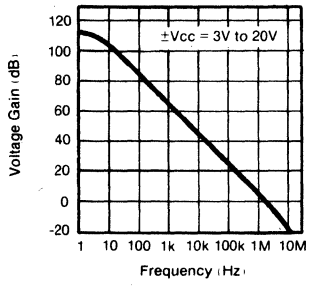
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



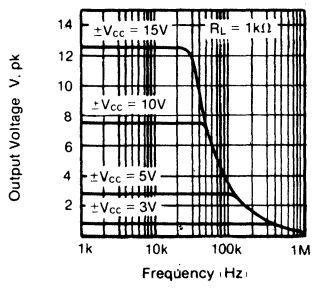
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



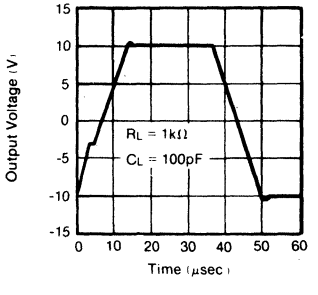
OPEN-LOOP FREQUENCY RESPONSE



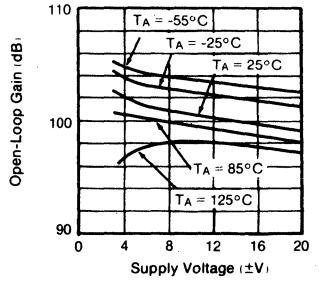
OUTPUT VOLTAGE vs. FREQUENCY



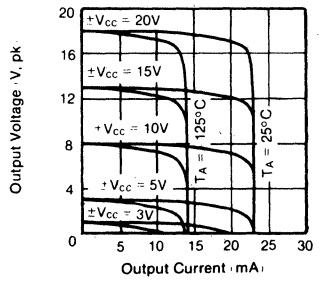
VOLTAGE FOLLOWER STEP RESPONSE



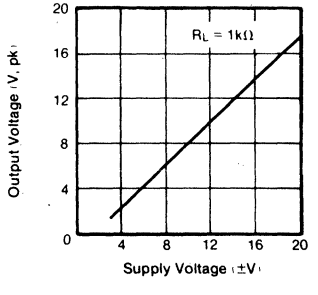
VOLTAGE GAIN vs. SUPPLY VOLTAGE



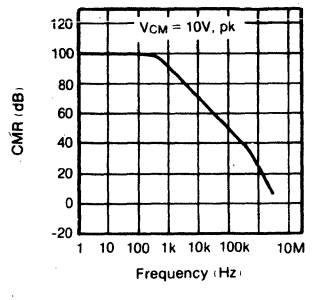
OUTPUT VOLTAGE vs. OUTPUT CURRENT



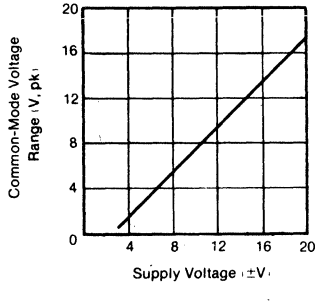
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



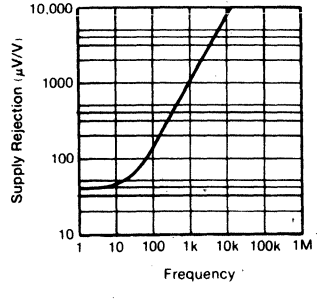
COMMON-MODE REJECTION vs. FREQUENCY



COMMON-MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



8. APPLICATIONS INFORMATION

8.1 Offset Adjustment. The input offset voltage of the Model 3500 may be adjusted to zero by connecting a 50kΩ potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 5a). This provides an adjustment range of approximately ±10mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the 3500 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3μV/°C change of drift for each 1.0mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers, this effect must be considered. By use of a transistor as in Figure 5b the effect of the offset adjustment on drift can be substantially reduced (by approximately a factor of six).

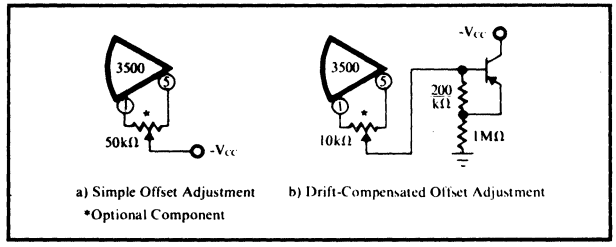


FIGURE 5. Offset Adjustment Techniques.

8.2 Bias Current Effects. Input bias current of the amplifier creates additional offset voltages by flowing in the impedances of the signal source and the feedback network. Although the bias currents of the 3500 are quite small, their effects may be appreciable when these impedances are large. The bias currents at the two inputs tend to be equal and the difference current smaller than either. Thus equalizing the resistance from each input to common, as in Figure 6, is an effective means of reducing DC offset due to bias current.

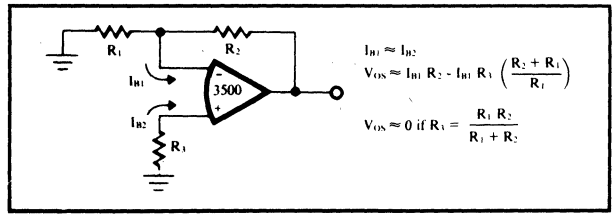


FIGURE 6. Minimization of Bias Current Effects.

8.3 Operation on a Single Supply. Although virtually any op amp can be operated on a single supply if input and output voltage limitations are observed, the Model 3500 is particularly suitable for such use. Its wide supply range of ±3VDC to ±20VDC translates to a single supply operating range of 6VDC to 40VDC, plus or minus. Two possible modes of operation on a single supply are shown in Figure 7. The following conditions must be observed to keep the amplifier within its linear region of operation.

1) $+2 < V_O < (V_{CC} - 2)$

2) $+3 < V_{IN} < (V_{CC} - 3)$. Figure 7b.

When operating on a single supply ($+V_{CC}$), shorting the output to common is equivalent to a short to supply and the internal power dissipation is approximately twice that which occurs for a short to common with balanced supplies of $\pm(V_{CC}/2)$. This dissipation may exceed safe limits for single supply voltages greater than 20V and must be prevented by use of a series limiting resistor or other device, if short circuit protection is desired.

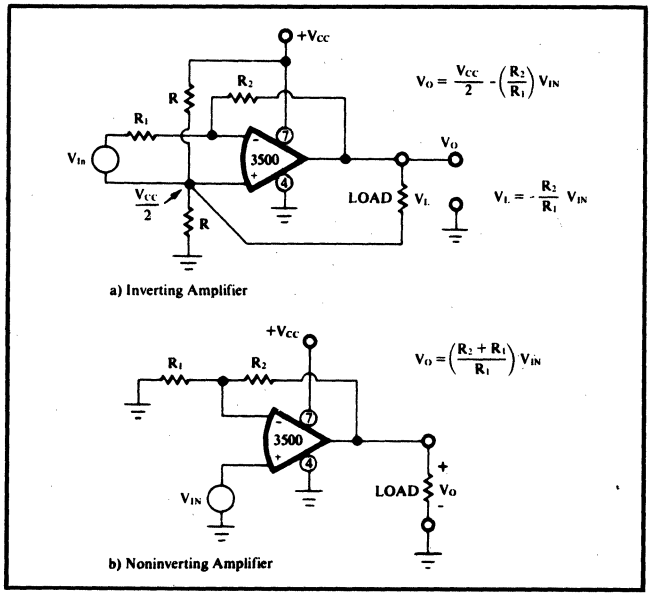
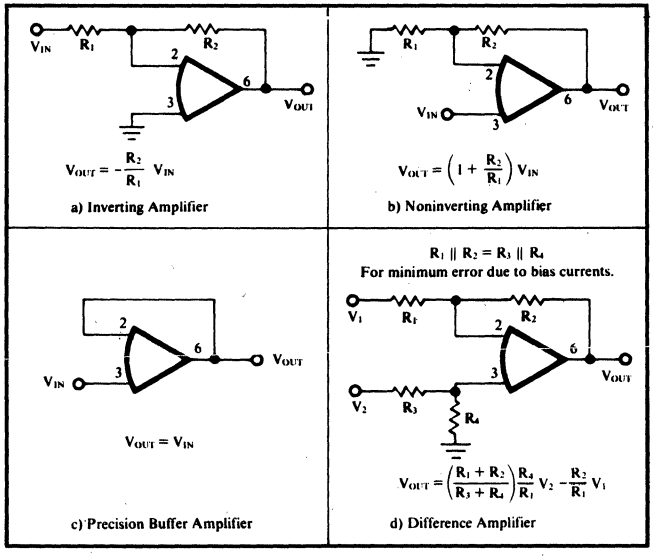


FIGURE 7. Operation on a Single Supply.

8.4 Wiring Precautions. In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 0.001μF ceramic capacitor from pins 7 and 4 to the power supply common.

8.5 Typical Applications.



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3510VM/MIL

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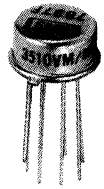
MARCH, 1984



DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic, low offset voltage drift, integrated circuit operational amplifier.

1.2 Part number. The complete part number is as shown below.

3510	V	M	/MIL
Basic model number	Grade	Metal package	Hi-Rel product designator

1.2.1 Device type. The device is a single, operational amplifier.

1.2.2 Device class. The device class is similar to the product assurance level class B, as defined in MIL-M-38510.

1.2.3 Case outline. The case outline (8-lead can) is as defined in Figure 5. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC 1/
Differential input voltage range	±40VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Short circuit may be to ground only. Rating applies to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

1.2.5 Recommended operating conditions.

Supply voltage range ---------- ±3VDC to ±20VDC
Ambient temperature range ---------- -55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
8-lead can	Figure 5	225mW at T_A = 125°C	70°C/W	220°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510 - Microcircuits, general specification for.
STANDARD
MILITARY
MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead finish is gold plate. The lead material and finish is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. All die are glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

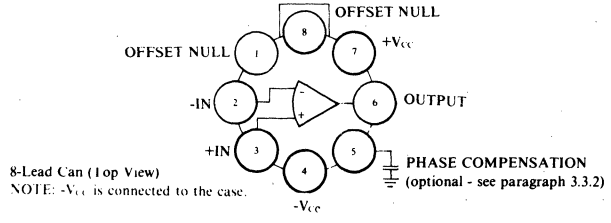


FIGURE 1. Terminal Connections.

3.2.9 Schematic circuit. The schematic circuit is shown in Figure 2.

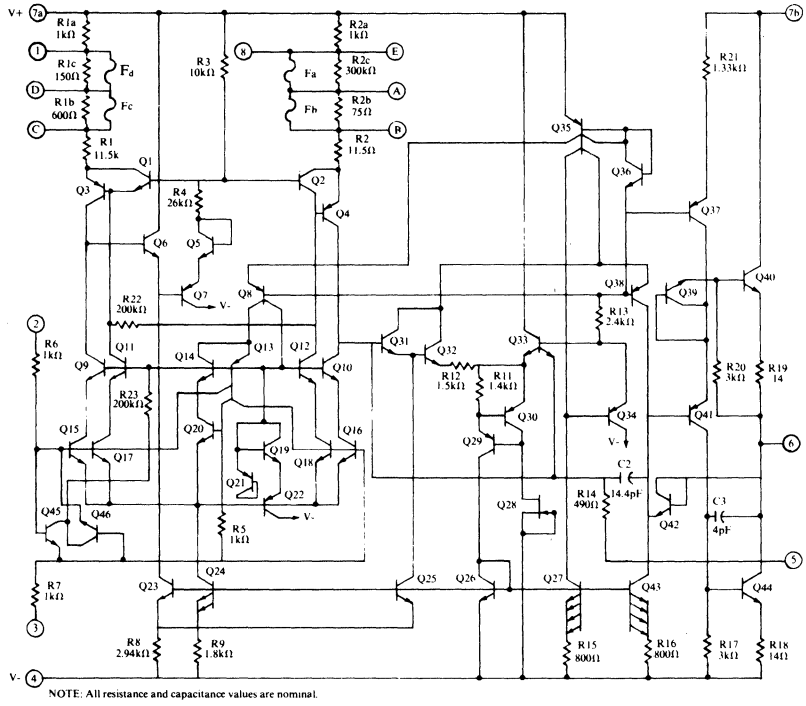


FIGURE 2. Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Offset and gain error null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 3.

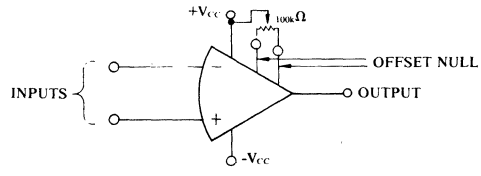


FIGURE 3. Offset Null Circuit.

3.3.2 Frequency compensation. The amplifier is free of oscillation when operated at a gain of 10 or greater with no external compensation and a source resistance of $\leq$10kΩ and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table III. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code
c. Manufacturer's identification
d. Manufacturer's designating symbol
e. Country of origin

TABLE I. Electrical Performance Characteristics.

Characteristics	Symbol	Conditions ($\pm V_{CC}$ = 15V, unless otherwise specified)		Limits Min	Limits Max	Units
Input offset voltage	V_{IO}		T_A = 25°C		±120	µV
			-55°C ≤ T_A ≤ +125°C		±350	µV
Input offset voltage temperature sensitivity (unnulled V_{IO})	$\frac{\Delta V_{IO}}{\Delta T}$	Δ T_A from -55°C to +25°C			±2	µV/°C
		Δ T_A from +25°C to +125°C			±2	µV/°C
Input offset current	I_{IO}		T_A = 25°C		±15	nA
			-55°C ≤ T_A ≤ +125°C		±55	nA
Input offset current temperature sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	Δ T_A from -55°C to +25°C			±0.4	nA/°C
		Δ T_A from +25°C to +125°C			±0.4	nA/°C
Input bias current	I_{IB}		T_A = 25°C		±25	nA
			-55°C ≤ T_A ≤ +125°C		±85	nA
Input bias current temperature sensitivity	$\frac{\Delta I_{IB}}{\Delta T}$	Δ T_A from -55°C to +25°C			±0.6	nA/°C
		Δ T_A from +25°C to +125°C			±0.6	nA/°C
Power supply rejection ratio	+PSRR	+V_{CC} = 10V -V_{CC} = -15V	T_A = 25°C		3	µV/V
Power supply rejection ratio	-PSRR	+V_{CC} = 15V -V_{CC} = -10V	T_A = 25°C		3	µV/V
Input voltage common-mode rejection	CMR	V_{CM} = -10V to +10V	T_A = 25°C	110		dB
Adjustment for input offset voltage	V_{IO} ADJ (±)			±1.5		mV
Output short circuit current (for positive output)	I_{OS} (+)		+25°C ≤ T_A ≤ +125°C	10	30	mA
			-55°C ≤ T_A ≤ +25°C	10	40	mA
Output short circuit current (for negative output)	I_{OS} (-)		+25°C ≤ T_A ≤ +125°C	10	30	mA
			-55°C ≤ T_A ≤ +25°C	10	40	mA
DC power dissipation (quiescent)	P_D	±V_{CC} = 20V	T_A = -55°C		170	mW
			T_A = +25°C		150	mW
			T_A = +125°C		130	mW
Single-ended input impedance (noninverting input)	Z_{IS1}		T_A = 25°C	1.5		MΩ
			-55°C ≤ T_A ≤ +125°C	1.0		MΩ
Single-ended input impedance (inverting input)	Z_{IS2}		T_A = 25°C	1.5		MΩ
			-55°C ≤ T_A ≤ +125°C	1.0		MΩ
Output voltage swing (maximum)	V_{OM}		R_L = 10kΩ	±11		V
			R_L = 1kΩ	±10		V
Open-loop voltage gain (single-ended) 1/	A_{VS} (±)	R_L = 2kΩ f = 0Hz	T_A = 25°C	120		dB
			-55°C ≤ T_A ≤ +125°C	114		dB
Open-loop voltage gain (single-ended) 1/	A_{VS} (±)	R_L = 2kΩ f = 0Hz	±V_{CC} = 3V T_A = 25°C	95		dB
Bandwidth, unity gain, small signal	BW		T_A = 25°C	0.25		MHz
Slew rate	SR (±)	V_{OUT} = ±10V, R_L = 1kΩ, A = +10, T_A = 25°C		0.5		V/µsec
Bandwidth, full power	BW_{FP}	V_{OUT} = ±10V, R_L = 1kΩ, A = +10, T_A = 25°C 2/		7		kHz
Input noise voltage	e_n	T_A = 25°C	0.1Hz to 10Hz		4.0	µV, pk-pk
			f_o = 1kHz		25	nV/√Hz
Input noise current	I_n	T_A = 25°C	0.1Hz to 10Hz		250	pA, pk-pk
			f_o = 1kHz		0.7	pA/√Hz

1/ Note that gain is not specified at $V_{IO\ ADJ}$ extremes. Some gain reduction is usually seen at $V_{IO\ ADJ}$ extremes.
2/ This parameter is untested. It is guaranteed by the slew rate test.

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared by Burr-Brown in fullfillment of the product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding, are in accordance with MIL-M-38510.

TABLE II. Electrical Test Requirements.

MIL-STD-883 test requirement (class B)	Subgroups (see Table III)
Interim electrical parameters (pre burn-in)(method 5004)	1A
Final electrical test parameters (method 5004)	1A*, 2A, 3A, 4A
Group A test requirements (method 5005)	1A, 2A, 3A, 4A, 7
Groups C and D end point electrical parameters (method 5005)	Table IV delta limits and limits
Additional electrical subgroups for group C inspections	1C, 2C, 3C, 4C, 5, 6

*PDA applies to subgroup 1A (see 4.3.c)

TABLE III. Group A Inspection.

Subgroup	Symbol	MIL-STD-883 method or equivalent	Test	Conditions $\pm V_{CC}$ = 15V, unless otherwise specified	Limits Min	Limits Max	Units
1A T_A = 25°C	V_{IO}	4001	1			±120	µV
	I_{IO}	4001	2			±15	nA
	I_{IB}	4001	3			±25	nA
	+PSRR	4003	4	+V_{CC} = 10V, -V_{CC} = -15V		3	µV/V
	-PSRR	4003	5	+V_{CC} = 15V, -V_{CC} = -10V		3	µV/V
	CMR	4003	6	V_{CM} = -10V to +10V	110		dB
	I_{OS}(+) 1/	3011	7	5sec. min 2/	10	30	mA
	I_{OS}(-) 1/	3011	8	5sec. min 2/	10	30	mA
	P_D	4005	9			105	mW
	$V_{IO\ ADJ}$		10		±1.5		mV
1C T_A = 25°C	$Z_{IS}1$		11		1.5		MΩ
	$Z_{IS}2$		12		1.5		MΩ
2A T_A = 125°C	V_{IO}	4001	13			±350	µV
	$\Delta V_{IO}/\Delta T$		14	$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}\ (test\ 13) - V_{IO}\ (test\ 1)}{100°C}$		±2	µV/°C
	I_{IB}	4001	15			±50	nA
	$\Delta I_{IB}/\Delta T$		16	$\frac{\Delta I_{IB}}{\Delta T} = \frac{I_{IB}\ (test\ 15) - I_{IB}\ (test\ 3)}{100°C}$		±0.6	nA/°C
	I_{IO}	4001	17			±20	nA
	$\Delta I_{IO}/\Delta T$		18	$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}\ (test\ 17) - I_{IO}\ (test\ 2)}{100°C}$		±0.4	nA/°C
2C T_A = 125°C	$V_{IO\ ADJ}$		19		±1.5		mV
	$Z_{IS}1$		20		1.0		MΩ
	$Z_{IS}2$		21		1.0		MΩ
3A T_A = -55°C	V_{IO}	4001	22			±310	µV
	$\Delta V_{IO}/\Delta T$		23	$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}\ (test\ 22) - V_{IO}\ (test\ 1)}{80°C}$		±2	µV/°C
	I_{IB}	4001	24			±85	nA
	$\Delta I_{IB}/\Delta T$		25	$\frac{\Delta I_{IB}}{\Delta T} = \frac{I_{IB}\ (test\ 24) - I_{IB}\ (test\ 3)}{80°C}$		±0.6	nA/°C
	I_{IO}	4001	26			±55	nA
	$\Delta I_{IO}/\Delta T$		27	$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}\ (test\ 26) - I_{IO}\ (test\ 2)}{80°C}$		±0.4	nA/°C
3C T_A = -55°C	$V_{IO\ ADJ}$		28		±1.5		mV
	$Z_{IS}1$		29		1.0		MΩ
	$Z_{IS}2$		30		1.0		MΩ
4A T_A = 25°C	V_{OM}	4004	31	R_L = 10kΩ, $\pm V_{CC}$ = 20V	±16		V
	V_{OM}	4004	3/	R_L = 1kΩ	±10		V
	A_{VS}	4004	32	R_L = 2kΩ, V_{OUT} = ±10V, f = 0Hz	120		dB
	SR(±)	4002	33	V_{OUT} = ±10V, R_L = 1kΩ, A = +10	0.5		V/µsec
4C T_A = 25°C	A_{VS}		34	±V_{CC} = 3V, R_L = 1kΩ	95		dB
5 T_A = 125°C	A_{VS}		35	R_L = 1kΩ, V_{OUT} = ±10V	114		dB
6 T_A = -55°C	A_{VS}		36	R_L = 1kΩ, V_{OUT} = ±10V	114		dB
7 T_A = 25°C	e_n		37	f_B = 0.1Hz to 10Hz		4.0	µV, pk-pk
	i_n		38	f_n = 0.1Hz to 10Hz		250	pA, pk-pk

NOTES:

1/ Due to significant power dissipation and associated device heating, these tests shall always be the last tests performed in any given sequence, followed by operational verification.

2/ The five second minimum test duration for I_{OS} test shall apply only for group A sampling inspections. For screening final electrical test, test duration for I_{OS} may be reduced to be consistent with automated test procedures.

3/ This parameter is untested. It is guaranteed by the conditions of the slew rate test.

TABLE IV. Groups C and D, End Point Electrical Parameters.
(T_A = 25°C, $\pm V_{CC}$ = 15, V_{CM} = 0V)

Test	Limit	Delta
V_{IO}	±180μV	±60μV
I_{IB}	±45nA	±20nA
I_{IO}	±17.5nA	±2.5nA

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing processes which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening is in accordance with method 5004 of MIL-STD-883, class B, except as modified in paragraph 4.3 herein. All microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening is in accordance with method 5004 of MIL-STD-883, class B, and is conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria apply:

a. Interim and final electrical test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
b. Burn-in test (method 1015 of MIL-STD-883) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 4 herein
   (3) T_A = 125°C minimum
   (4) Test duration is 160 hours minimum
c. Percent defective allowable (PDA). The PDA is 5 percent based on failures from group A, subgroup 1A test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameters tests prior to burn-in are omitted, then all screening failures are included in the PDA. The verified failures of group A, subgroup 1A after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
d. External visual inspection need not include measurement of case and lead dimensions.

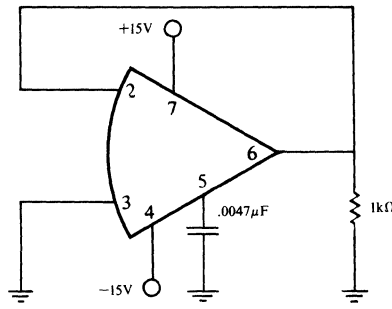


FIGURE 4. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of method 5005, MIL-STD-883, are conducted on each inspection lot. Groups C and D inspections of method 5005, MIL-STD-883, are not required unless specifically required by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of method 5005, MIL-STD-883. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in Table I of method 5005 of MIL-STD-883 and as follows:

a. Tests are specified in Table II herein.
b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in Table II (class B) of method 5005 of MIL-STD-883. The package does not contain a desiccant and, therefore, the internal water vapor content test is not required.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in Table III of method 5005 of MIL-STD-883 and as follows:

a. Steady state life test (method 1005 of MIL-STD-883) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 4 herein
   (3) T_A = 125°C minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table IV herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in Table IV of method 5005 of MIL-STD-883 and as follows:

a. Internal water-vapor content test is not required.
b. End point electrical parameters are specified in Table IV herein.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

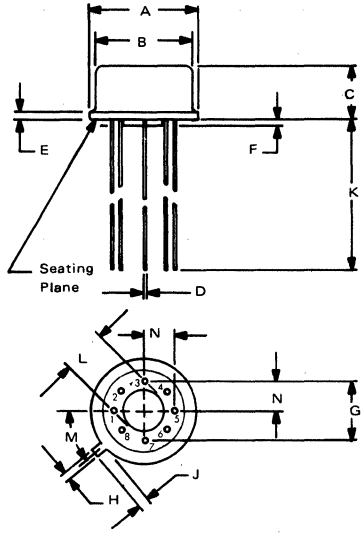
6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:
a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

6.4 Substitutability. Microcircuits furnished under this specification are similar to Burr-Brown model 3510.



NOTE:
Leads in true position within .010"
(.25mm) R at MMC at seating plane.

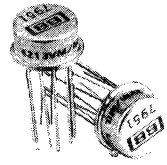
Pin numbers shown for reference only.
Numbers may not be marked on package.

Weight: 3 grams max.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	---	12.7	---
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 5. Case Outline (TO-99 Package Configuration).

BURR-BROWN®



4213/MIL SERIES

MODEL NUMBERS:

4213WM/883B
4213WM
4213UM/883B
4213UM
4213VM/MIL
4213VM/883B
4213VM

REVISION B
DECEMBER, 1982

Military
MULTIPLIER - DIVIDER

FEATURES

- **HI REL MANUFACTURE**
- **ACCURATE**
  ±1/2% TOTAL ERROR (W grade)
  ±1% TOTAL ERROR (V and U grades)
- **4-QUADRANT MULTIPLICATION**
  2-QUADRANT DIVISION
- **NO EXTERNAL COMPONENTS NECESSARY**
- **DIFFERENTIAL INPUT**
- **MIL-STD-883B SCREENING**
- **-55°C TO +125°C SPECIFICATIONS**

DESCRIPTION

The 4213/MIL Series is a high performance, precision multiplier/divider with a total full scale error of ±1/2% or ±1%. It is intended for transducer and analog computation applications; it will also square, square root, and perform trigonometric computations. It has differential inputs and is ideal for instrumentation applications. The operating range is -55°C to +125°C. The 4213/MIL is a hybrid microcircuit consisting of a monolithic bipolar IC and a precision laser-trimmed thin-film network. It is assembled into a hermetic TO-100 (10-lead can).

These devices are manufactured on a separate Hi-Rel manufacturing line with impeccable clean room conditions which assures "built-in" quality and provides for a long product life.

The 4213/MIL Series is available in three electrical performance grades. The W grade features premium accuracy (±1/2% total error, ±50mV feedthrough, and ±25mV offset error). The V grade features ±1% total error, ±100mV feedthrough, and ±30mV offset error. The U grade has excellent performance from -25°C to +85°C and is also specified from -55°C to +125°C. U grade applications include test equipment, shipboard, ground support, and industrial applications where operation is normally between -25°C and +85°C and full temperature operation must be assured.

Three product assurance levels are available: standard, /883B, and /MIL. The standard models have many MIL-STD-883 screens performed routinely. The /883B suffixed devices are 100% screened per MIL-STD-883 method 5008 hybrid class (class B). /MIL suffixed devices feature Hi-Rel manufacture, 100% screening per MIL-STD-883 method 5008 hybrid class, and a 10% PDA. Quality assurance further processes /MIL devices, performing group A and B inspections on each inspection lot and group C and D inspections periodically and when specified on the customer's purchase order. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

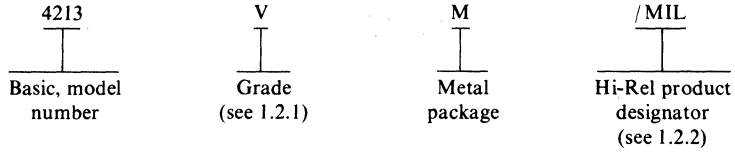
International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
MULTIPLIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a precision, integrated circuit multiplier.

1.2 Part Number. The complete part number is as shown below.



1.2.1 Device type. The device is a single, four-quadrant, analog multiplier; it will also function as a single, two-quadrant, analog divider, a squarer, a square rooter, etc. (see paragraph 8.3). Three electrical performance grades are provided. The W grade features premium accuracy of ±1/2% total error, ±50mV feedthrough and ±25mV offset error. The V grade features ±1% total error, ±100mV feedthrough and ±30mV offset error. The U grade features excellent performance from -25°C to +85°C and guarantees performance from -55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device Class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level as follows:

Hi-Rel product designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
/883	Standard model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model, including 100% electrical testing.

1.2.3 Case outline. The case outline is A-2 (10-lead can, TO-100) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range (X, Y, and Z inputs)	±20VDC 1/
Differential input voltage (X, Y, and Z inputs)	±40VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Short circuit may be to ground only. Rating applies to +125°C case temperature or +75°C ambient temperature at ±15VDC supply voltage.

1.2.5 Recommended operating conditions.

Supply voltage range	±8.5VDC to ±20VDC
Ambient temperature range	-55°C to +125°C
Input voltage range ($\pm V_{CC}$ = 15VDC)	±10VDC

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
10-lead can (TO-100)	A-2	225mW at T_A = 125°C	70°C/W	220°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510, except that organic and polymeric materials are used for die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. The dice utilized are glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

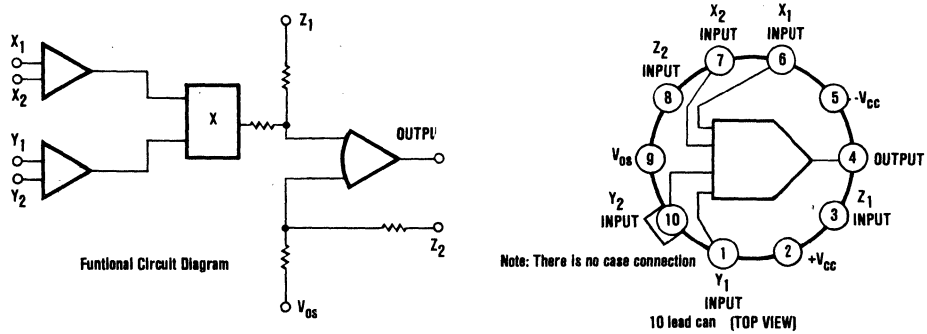


FIGURE 1. Functional Circuit Diagram and Terminal Connections.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

TABLE I. Electrical Performance Characteristics.

All characteristics T_A = -55°C to +125°C, ±V_{CC} = 15VDC, unless otherwise noted.

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMITS 4212WM/883B 4213WM MIN	TYP	MAX	4213VM/MIL 4213VM/883B 4213VM MIN	TYP	MAX	4213UM/883B 4213UM MIN	TYP	MAX	UNITS
ACCURACY												
Total Error	E_T	Each quadrant T_A = +25°C			1/2			1			1	±% of FSR
		-25°C to +85°C									2	±% of FSR
		T_A = -55°C			3			3			4	±% of FSR
		T_A = +125°C			4			4			8	±% of FSR
Feedthrough												
X Input	FT_X	V_X = 20V, p-p T_A = +25°C		30	50		30	100			100	±mV, p-p
		V_Y = 0, f = 50Hz -55°C to +125°C			100			200			200	±mV, p-p
Y Input	FT_Y	V_X = 0, f = 50Hz T_A = +25°C		25	40		25	80			80	±mV, p-p
		V_Y = 20V, p-p -55°C to +125°C			80			180			180	±mV, p-p
Nonlinearity												
X Input	LIN_X	V_X = 20V, p-p, V_Y = ±10V T_A = +25°C		0.08			*			*		±% of FSR
Y Input	LIN_Y	V_Y = 20V, p-p, V_X = ±10V T_A = +25°C		0.01			*			*		±% of FSR
INPUT												
Input Resistance	R_{IN}	X, Y, Z inputs, pin 9 open	3.5	10		*	*		*	*		MΩ
Input Bias Current	I_{IB}	X, Y, Z inputs T_A = +25°C		1.4	2.5		*	*		*	*	μA
		-55°C to +125°C			6			*			*	μA
Input Voltage Range	V_{IN}	Rated Operation	±10			*			*			V
Common-mode Rejection	CMR	+10V, -6V	60			*			*			dB
DYNAMIC CHARACTERISTICS												
Small Signal Bandwidth ±3dB	BW_{3dB}	X and Y inputs T_A = +25°C	450	550		*	*		*	*		kHz
Bandwidth ±1 flatness	$BW_{1\%}$	X and Y inputs T_A = +25°C	70			*			*			kHz
Full Power Bandwidth	BW_{FP}	T_A = +25°C	130			*			*			kHz
Slew Rate	SR	X and Y inputs T_A = +25°C	20			*			*			V/μsec
OUTPUT												
Output Voltage	V_{OM}	R_L = 2kΩ, C_L = 1000pF	10			*			*			±V
Output Resistance	R_O	Closed loop		1.5	10		*	*		*	*	Ω
Output Noise	N	T_A = +25°C { 1Hz to 10kHz			200			*			*	μV, rms
		{ 1Hz to 10MHz			1000			*			*	μV, rms
Output Offset Error 1/	V_{OO}	T_A = +25°C			25			30			50	±mV
		-25°C to +85°C									100	±mV
		-55°C to +125°C			100			100			200	±mV
Output Offset Error	$\frac{\Delta V_{OO}}{\Delta T}$	-25°C to +85°C									1.7	±mV/°C
Temperature Sensitivity		-55°C to +125°C			1.0			1.0			2.0	±mV/°C
Short Circuit Current	I_{OS}	T_A = +25°C	5		20	*		*	*		*	mA
		-55°C to +125°C	5		30	*		*	*		*	mA
POWER SUPPLY												
Power Supply Range			8.5	15	20	*	*	*	*	*	*	±V
Power Dissipation, Quiescent		T_A = +25°C		150	180		*	*		*	*	mW
		-55°C to +125°C			225			*			*	mW
TEMPERATURE RANGE (AMBIENT)												
Operating			-55		+125	*		*	*		*	°C
Storage			-65		+150	*		*	*		*	°C

*Specifications same as 4213WM

NOTE:

1/ Externally adjustable to zero.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Transfer functions. The transfer functions for multiplier and divider connections are shown in Figure 2.

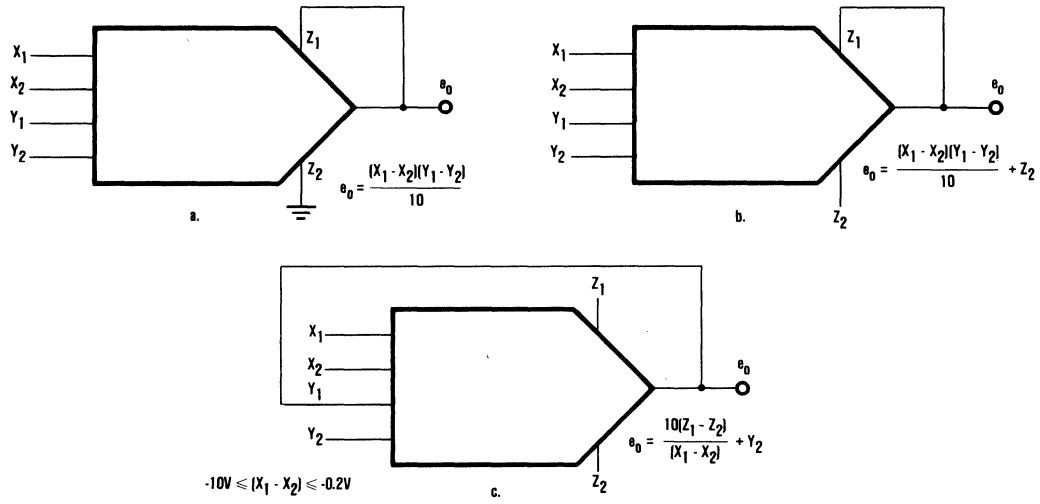


FIGURE 2. Transfer Functions.

3.3.3 Output offset error null. The multiplier is capable of being nulled to zero offset error using the circuit in Figure 3.

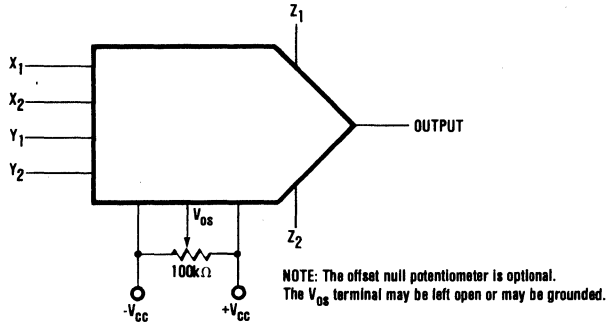


FIGURE 3. Offset Null Circuit.

3.4 Electrical tests. Electrical test requirements are specified in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883 TEST REQUIREMENTS (HYBRID CLASS) / MODELS	4213WM/883B 4213WM	4213VM/MIL	4213VM/883B 4213VM	4213UM/883B 4213UM
	Subgroups (see Table III)			
Interim electrical parameters (pre burn-in) (method 5008)	1	1	1	1
Final electrical test parameters (method 5008)	1, 2, 3, 4, 5, 6	1*, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6	1, 2U, 3U, 4, 5U, 6U
Group A test requirements (method 5008)	--	1, 2, 3, 4, 5, 6, 4A	--	--
Group C end point electrical parameters (method 5008)	--	Table IV limits and delta limits	--	--
Additional electrical subgroups performed prior to Group C inspections	--	1C, 2C, 3C, 5C, 6C, 7C	--	--

*PDA applies to subgroup 1 (see 4.3.d)

TABLE III. Group A Inspection.

SUBGROUP	PARAMETER SYMBOL	CONDITIONS $\pm V_{CC}$ = 15VDC, pin 9 open unless otherwise specified	LIMITS 4213 V GRADE MIN	4213 V GRADE MAX	4213 W GRADE MIN	4213 W GRADE MAX	4213 U GRADE MIN	4213 U GRADE MAX	UNITS
1 T_A = +25°C	V_{OO} I_{IB} P_D	X_1 Input		±30 2.5 180		±25 2.5 180		±50 2.5 180	mV µA mW
1C T_A = +25°C	CMR R_{IN} R_o I_o	X = Y = +10V to -6V	60 3.5 5	 10 20					dB MΩ Ω mA
2 T_A = +125°C	V_{OO}			±100		±100			mV
2U T_A = +85°C	V_{OO}							±100	mV
2C T_A = +125°C	I_{IB} $\frac{\Delta V_{OO}}{\Delta T}$ P_D CMR	X_1 Input $\frac{\Delta V_{OO}}{\Delta T} = \frac{V_{OO}(+125°C) - V_{OO}(+25°C)}{100°C}$ X = Y = +10V to -6V	 60	6 ±1 225					µA mV/°C mW dB
3 T_A = -55°C	V_{OO}			±100		±100			mV
3U T_A = -25°C	V_{OO}							±100	mV
3C T_A = -55°C	I_{IB} $\frac{\Delta V_{OO}}{\Delta T}$ P_D CMR	X_1 Input $\frac{\Delta V_{OO}}{\Delta T} = \frac{V_{OO}(-55°C) - V_{OO}(+25°C)}{80°C}$ X = Y = +10V to -6V	 60	6 ±1 225					µA mV/°C mW dB
4 T_A = +25°C	E_T FT_X FT_Y	Each quadrant X = 20V, p-p; Y = 0; f = 50Hz X = 0; Y = 20V, p-p; f = 50Hz		±1 100 80		±1/2 50 40		±1 100 80	% mV, p-p mV, p-p
4A T_A = +25°C	V_{OM}	R_L = 2kΩ, C_L = 1000pF		±10					V
5 T_A = +125°C	E_T	Each quadrant		±4		±4			%
5U T_A = +85°C	E_T	Each quadrant						±2	%
5C T_A = +125°C	V_{OM} FT_X FT_Y	R_L = 2kΩ, C_L = 1000pF X = 20V, p-p; Y = 0; f = 50Hz X = 0; Y = 20V, p-p; f = 50Hz		±10 200 180					V mV, p-p mV, p-p
6 T_A = -55°C	E_T	Each quadrant		±3		±3			%
6U T_A = -25°C	E_T	Each quadrant						±2	%
6C T_A = -55°C	V_{OM} FT_X FT_Y	R_L = 2kΩ, C_L = 1000pF X = 20V, p-p; Y = 0; f = 50Hz X = 0; Y = 20V, p-p; f = 50Hz		±10 200 180					V mV, p-p mV, p-p
7C T_A = +25°C	$BW_{1\%}$ $BW_{1\%}$ SR SR BW_{3dB} BW_{3dB} BW_{FP} N N	X = 20V, p-p; Y = 10V X = 10V; Y = 20V, p-p X = +20V-step; Y = 10V; R_L = 2kΩ X = 10V; Y = +20V-step; R_L = 2kΩ X = 1V, rms; Y = 10V X = 10V; Y = 1V, rms R_L = 20kΩ, V_o = ±10V f_B = 1Hz to 10kHz f_B = 1Hz to 10MHz	70 70 20 20 450 450 130	 200 1000					kHz kHz V/µsec V/µsec kHz kHz kHz µV, rms µV, rms

TABLE IV. Group C, End Point Electrical Parameters.

(T_A = 25°C, $\pm V_{CC}$ = 15VDC)

Test	Limit	Delta
E_T	1.0%	0.66%
V_{OO}	±60mV	25mV

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin (U.S.A)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, for the /MIL Hi-Rel product designation, including rebonding, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

For the standard model, Hi-Rel product designation (none), routine manufacturing processing includes Burr-Brown internal visual inspection, and stabilization bake, fine leak, gross leak, burn-in (72 hours, performed preseal), constant acceleration (condition D) and external visual inspection per MIL-STD-883 method 5008 hybrid class.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /MIL Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

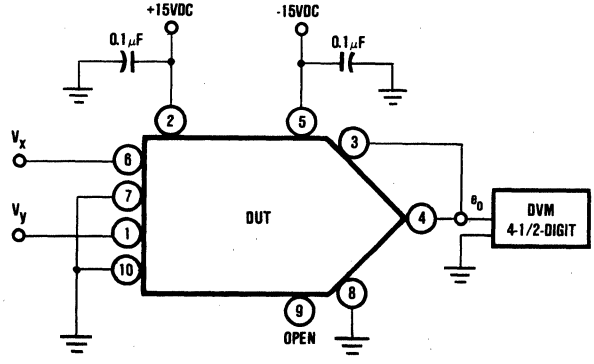


FIGURE 4. Test Circuit for Total Error.

1/ A four-digit date code, indicating year and week of seal, is marked on /883B and (none) Hi-Rel product designations.

PROCEDURE:

1. Set $V_x = V_y = +10.000VDC \pm 1mV$, measure $E_o = E_{o1}$.
2. Set $V_x = V_y = -10.000VDC \pm 1mV$, measure $E_o = E_{o2}$.
3. Set $V_x = +10.000VDC \pm 1mV$ and $V_y = -10.000VDC \pm 1mV$, measure $E_o = E_{o3}$.
4. Set $V_x = -10.000VDC \pm 1mV$ and $V_y = +10.000VDC \pm 1mV$, measure $E_o = E_{o4}$.
5. Calculate $V_{o1} = |E_{o1} - 10|$, $V_{o2} = |E_{o2} - 10|$, $V_{o3} = |E_{o3} + 10|$ and $V_{o4} = |E_{o4} + 10|$.
6. V_{ox} is the largest of V_{o1}, V_{o2}, V_{o3} or V_{o4}.

$$E_T(\%) = \frac{V_{ox}}{10} \times 100$$

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008 except as modified herein.

4.2 Qualification. Qualification is not required unless specified by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for / MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition D, Y_1 axis only.

b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for the / MIL Hi-Rel product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

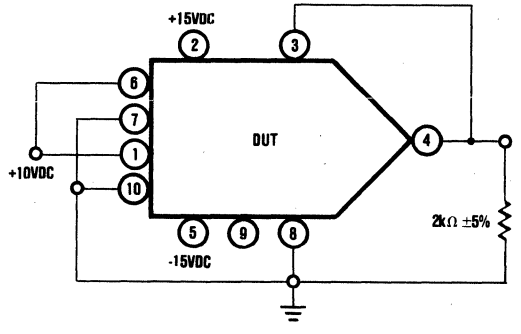


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs Group C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as follows.

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = 125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Total error. Total error (E_T) is the difference between the actual output voltage and the ideal output voltage expressed as a percentage of the maximum output voltage, 10 volts. It is the sum of the individual errors and includes feedthrough and output offset voltage.

Feedthrough. Feedthrough (FT_X or FT_Y) is the output voltage when the ideal output voltage is zero (i.e., $X = 0$, $Y = \pm V$ or $X = \pm V$, $Y = 0$).

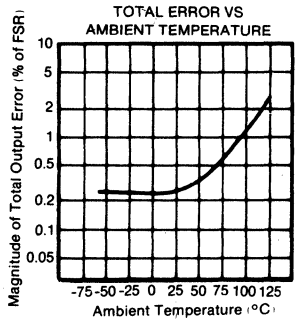
6.5 Microcircuit group assignment. These mircocircuits are assigned to Technology Group F as defined in MIL-M-38510, Appendix E.

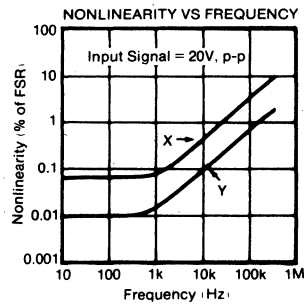
6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

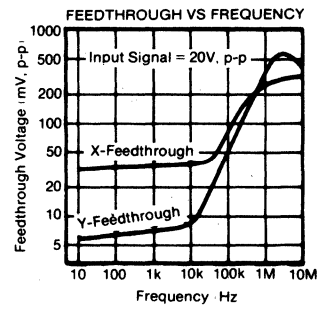
6.7 Power Supply Sequencing. Apply, and remove, both supplies together. Alternatively, apply the positive supply first. Permanent damage may occur if the minus supply is applied with an input greater than +6VDC.

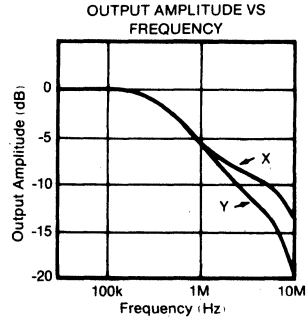
7. ELECTRICAL PERFORMANCE CURVES.

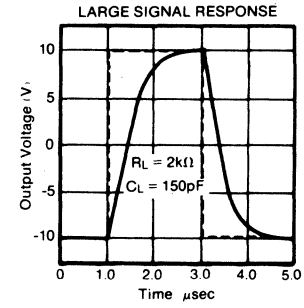
(Typical at T_A = +25°C and ± V_{CC} = 15VDC unless otherwise specified.)

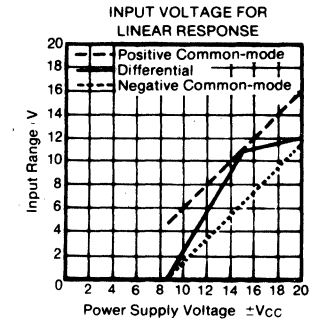


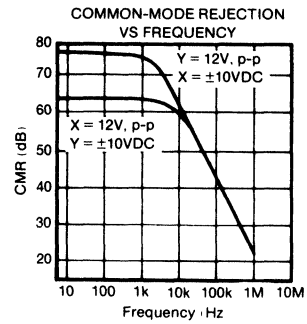


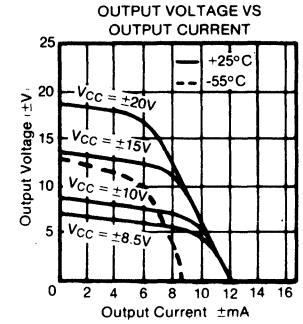


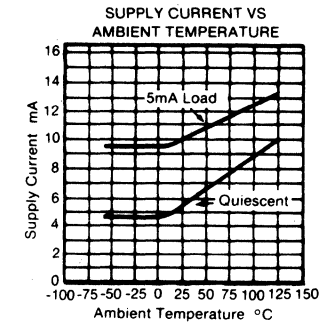












8. APPLICATIONS INFORMATION

8.1 Power supply decoupling. For optimum performance and to prevent frequency instability due to power supply lead inductance, each power supply should be decoupled by connecting a 1μF tantalum capacitor from each power supply pin to ground (power supply common).

8.2 Capacitive loads. Stable operation is maintained with capacitive loads up to 1000pF, except for the square root mode which is limited to 50pF. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

8.3 Typical Applications.

8.3.1 Multiplication. The basic connection for four-quadrant multiplication is shown in Figures 2a and 2b. Optional offset nullling is shown in Figure 3. Feedthrough may be minimized by applying an external nulling voltage to the X and/or Y input, as appropriate. Usually, the nulling voltage is applied to X_2 or Y_2. If Z_2 input is not used, it should be grounded.

Figure 6 shows how to achieve a scale factor larger than 0.1 (i.e., a denominator less than 10). A larger scale factor is electrically advantageous in some applications, but this has the disadvantage of proportionately increasing the output offset voltage. Note, the offset may be nulled as shown in Figure 3. Also, the small signal bandwidth is reduced to about 50kHz.

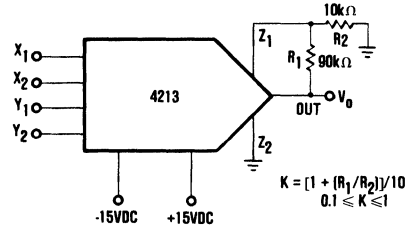


FIGURE 6. Connection for Unity Scale Factor.

8.3.2 Division. The basic connection for two-quadrant division is shown in Figure 2c.
Divider error is approximately

$$\epsilon_{divider} = \frac{10\epsilon_{multiplier}}{X_1 - X_2}$$

Note, the divider error will become very large for small values of $(X_1 - X_2)$. A 10 to 1 denominator range is a practical limit.

8.3.3 Squaring. The basic connection is shown in Figure 7.

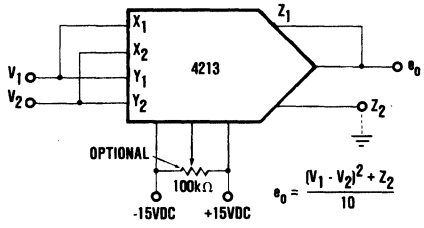


FIGURE 7. Squaring Connection.

8.3.4 Square Root. Figure 8 shows the connection for taking the square root of the voltage $V_{Z1} - V_{Z2}$. The diode prevents a latching condition which could occur if the input momentarily changed polarity. The load resistance R_L must be in the range of $10k\Omega \leq R_L \leq 1M\Omega$ to provide the current necessary to operate the diode. The output offset should be nulled for optimum performance; allow the input to be its smallest expected value and adjust R_1 for the proper output voltage. The square root mode accuracy is then approximately that of the multiply mode.

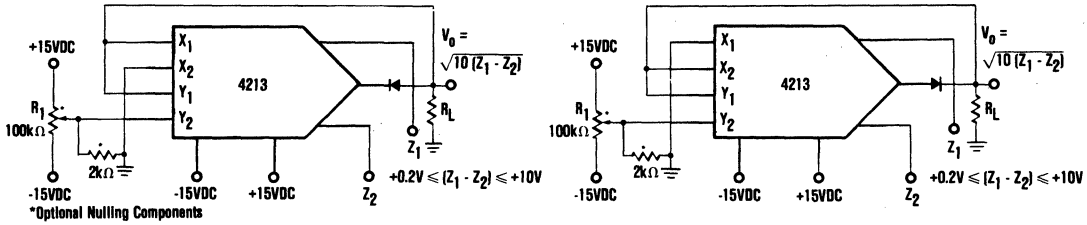


FIGURE 8. Square Root Connection.

8.3.5 Percent. The circuit of Figure 9 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2/R_1.

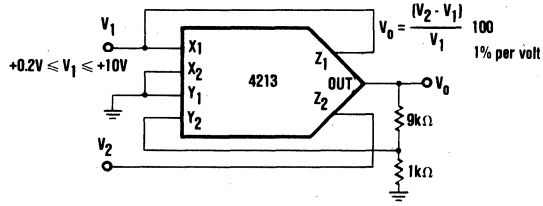


FIGURE 9. Percentage Computation.

8.3.6 Sine Function Generator. The circuit in Figure 10 uses implicit feedback to implement the following sine function approximation: $V_O = (1.5715V_I - 0.004317V_I^3)/(1 + 0.001398V_I^2) = 10 \text{ sine } (9V_I)$.

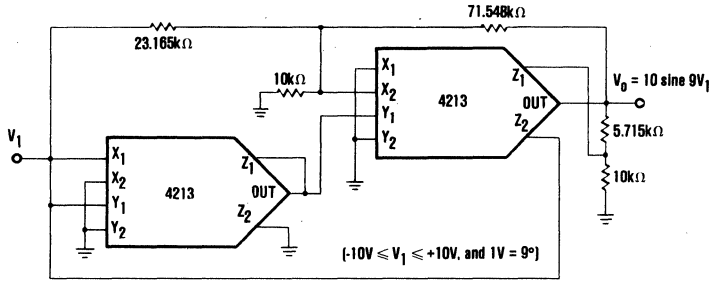


FIGURE 10. Sine Function Generator.

8.3.7 Single-phase Power Measurement. Figure 11 shows a circuit for measurement of single-phase instantaneous and real power.

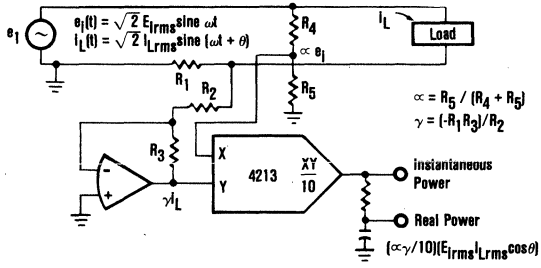
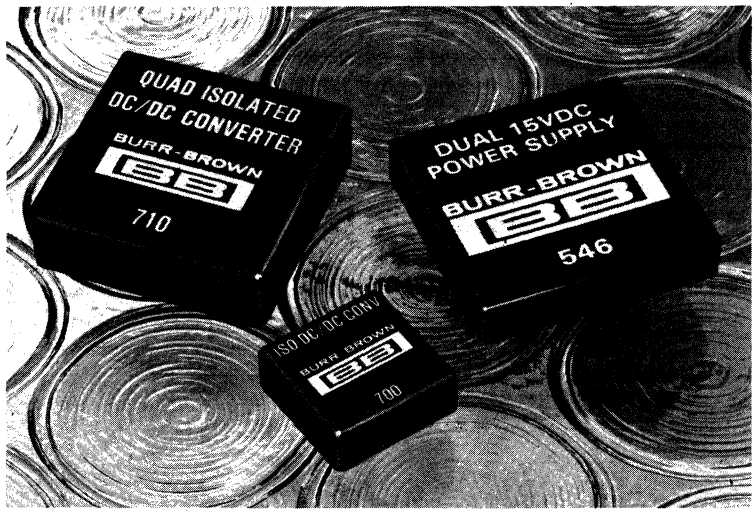


FIGURE 11. Single-Phase Instantaneous and Real Power Measurement.

MODULAR POWER SUPPLIES



Well-regulated DC power is usually required to power modern electronic circuits. Over the years electronic circuits have changed in terms of size and performance. Packaged in small integrated circuit packages or in hybrid modules, more and more electronic circuits now provide significantly improved performance. Burr-Brown encapsulated power supplies have kept up with changing times. We provide a broad line of reliable, self-contained, ready to use power supplies, at low cost, to meet OEM and design engineers' power supply requirements.

Burr-Brown standard series AC/DC power supplies and DC/DC converters provide maximum flexibility in systems design. They are particularly useful for powering analog interface circuitry involving operational amplifiers, A/D and D/A converters, instrumentation and isolation amplifiers, analog circuit functions, and so forth, in digital and analog systems. A wide range of output voltage and current ratings are available; international input voltage ratings are also available.

The AC/DC supplies are available in both the PC board-mountable and chassis-mountable versions. The chassis mount type provides the same reliable performance as the PC board mount type, but the input and output connections are made on a terminal strip via screw terminals rather than pins. They are useful in applications where use of PC boards or sockets is either undesirable or impractical.

The DC/DC converters are available in small encapsulated PC board-mountable packages. They provide high input-output isolation, making them suitable in computer interface applications where, if necessary, the analog circuitry can be "floated" completely independent of digital ground. Specially designed DC/DC converters are available for use with optically-coupled isolation amplifiers and for applications where isolation voltage ratings of 3000 volts and more are required.

All Burr-Brown power supplies are extensively tested before and after encapsulation to ensure reliable operation. Computerized automatic testing equipment is used to implement stringent quality control. Years of linear and digital engineering expertise have gone into the design and manufacture of Burr-Brown products. Most of these power supplies are available from stock in both small and large quantities.

SELECTION GUIDE

AC/DC CONVERTERS								
Description	Model	Rated Output	Rated Input	Regulation No Load to Full Load	Regulation Overrated Line Voltage	Output[1] Ripple/ Noise	Package	Page
Dual ±15VDC Supply P.C.B. Mount	550	±15V, ±25mA	105VAC to 125VAC, 50Hz to 400Hz [2] [3] [4]	±0.1%	±0.05%	2mV	Module	12-3
	551	±15V, ±50mA		±0.05%	±0.05%	0.5mV	Module	12-3
	552	±15V, ±100mA		±0.05%	±0.05%	0.5mV	Module	12-3
	553	±15V, ±200mA		±0.05%	±0.05%	0.5mV	Module	12-3
	554	±15V, ±350mA		±0.02%	±0.02%	0.5mV	Module	12-3
Dual ±15VDC Supply Chassis Mount	556	±15V, ±200mA	105VAC to 125VAC, 50Hz to 400Hz [2] [3] [4]	±0.05%	±0.05%	1mV	Module	12-3
	558	±15V, ±500mA		±0.05%	±0.05%	1mV	Module	12-3
5VDC Supply P.C.B. Mount	560	5V[5], ±250mA	105VAC to 125VAC, 50Hz to 400Hz [2] [3] [4]	±0.1%	±0.05%	1mV	Module	12-3
	561	5V[5], ±500mA		±0.1%	±0.05%	1mV	Module	12-3
	562	5V[5], ±1000mA		±0.1%	±0.05%	1mV	Module	12-3

DC/DC CONVERTERS							
Description	Model	Input	Output	Isolation	Leakage Current	Package	Page
Regulated	546	4.5VDC to 5.5VDC 400mA	Single-Bipolar ±15V, 120mA	300V	Not Specified	Module	12-3
Isolated	PWR70	10VDC to 18VDC	±1%VDC, ±100mA	2000VDC	1μA, max	Module	12-9
	700	10VDC to 18VDC 89mA	±10VDC to ±18VDC (±1V tolerance) at 60mA total	1500Vp	1μA, max	Module	12-11
	700U[5]	10VDC to 18VDC 89mA	±10VDC to ±18VDC (±1V tolerance) at 60mA total	2000Vp	1μA, max	Module	12-11
	710[6]	10VDC to 18VDC 100mA	Four sets of outputs each set: ±10VDC to ±18VDC (±1V tolerance) at 76mA total all outputs	1000Vp	1μA, max	Module	12-13
	722 722BG	5VDC to 16VDC 120mA	Two-Bipolar ±15V, 64mA	3500V[5] 8000V[6]	1μA at 240V, 60Hz	DIP	12-17
	724	5VDC to 16VDC 125mA	Four-Bipolar ±8V	1000V[5] 3000V[6]	1μA at 240V, 60Hz	DIP	12-24

NOTES: (1) At full load, rms (max). (2) 205VAC, 50Hz to 400Hz option available. (3) 90VAC to 110VAC, 50Hz to 400Hz option available. (4) 220VAC to 260VAC, 50Hz to 400Hz option available. (5) Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields. Model 700M and 700UM are similar to Models 700/700U but, in addition, they are 100% screened to patient-connected circuit requirements for the leakage current (par. 27.5) and withstand voltage (par. 31.11) of UL544. Additional per unit charge for 700M or 700UM. See Product Data Sheet for complete specifications. (6) Model 710 provides 4 channels (sets) of isolated outputs. See Product Data Sheet for complete specifications.

REGULATED BATTERY-BACKED POWER SUPPLY						
Model	Rated Output	Output Ripple	Current Limit	Rated Input	Features	Page
PSB100	+5VDC, 11.2A +12VDC, 1.2 A −12VDC, 1.2 A −5VDC, 100mA	150mV, p-p 360mV, p-p 360mV, p-p 40mV, p-p	12.0A ±5% 1.5A ±5% 1.5A ±5% None	100-130VAC or 200-260VAC	Designed for use with microcomputer systems such as Multibus™ system. Provides signals for line power loss, or low internal battery.	12-7

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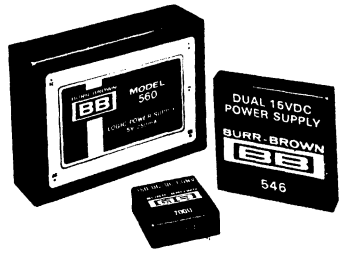

MODULAR AC/DC AND DC/DC POWER SUPPLIES

FEATURES

- PC BOARD-COMPATIBLE
- CHASSIS MOUNTABLE
- HIGH RELIABILITY, FULLY TESTED
- LOW INSTALLED COST
- COMPLETELY SELF-CONTAINED

DESCRIPTION

Burr-Brown standard series power supplies and DC/DC converters provide maximum flexibility in systems design. They are particularly useful for powering analog interface circuitry in digital and analog systems and have a wide range of output voltage and current ratings. They are completely self-contained, ready to use encapsulated units. For most OEM users they eliminate engineering start-up/documentation costs and manufacturing delays at prices generally far below internal manufacturing costs.

The AC/DC power supplies have a current limiting circuit in the output stage, designed to withstand output short-circuit-to-common or substantial overload conditions for long periods of time, without causing damage to the power supply.

In applications where isolation between input and output is an essential requirement (such as powering isolation amplifier input and output stages) the Burr-Brown isolated DC/DC converters provide up to 1500VDC of isolation protection.

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MODULAR AC/DC POWER SUPPLIES

- PC BOARD/CHASSIS MOUNT TYPE
- ±15VDC DUAL OUTPUTS, +5VDC SINGLE OUTPUT
- 25mA TO 1000mA CURRENT CAPABILITY
- CURRENT-LIMITED OUTPUTS FOR SHORT CIRCUIT PROTECTION
- INTERNATIONAL AC INPUT VOLTAGE OPTIONS AVAILABLE

SPECIFICATIONS COMMON TO ALL AC/DC POWER SUPPLIES

Input Voltage: 105VAC to 125VAC, 50Hz to 400Hz. For international AC input voltages see options E, F, and H.

Input Isolation: 50MΩ

Breakdown Voltage: 500V, min.

Output Voltage: Error, ±1%; temperature coefficient, ±0.02%/°C

Output Protection: Current limiting protection for output to withstand overloads and direct short circuits to ground to prevent excessive temperature within the unit.

Rated Operating Temperature: -25°C to +71°C. May be operated at higher temperatures with proper derating.

Storage Temperature: -25°C to +85°C.

DC/DC CONVERTERS, ±15VDC OUTPUT

- REGULATED ±15VDC FROM UNREGULATED DC INPUT
- DIFFERENT DC INPUT VOLTAGE RANGES AVAILABLE
- HIGH CURRENT CAPABILITY WITH CURRENT LIMIT PROTECTION
- ISOLATED DC/DC CONVERTERS, 75% EFFICIENCY AT FULL LOAD
- LOW COUPLING CAPACITANCE (8pF)
- HIGH ISOLATION VOLTAGE (1500VDC)
- LOW EMI, SHIELDED AND UNSHIELDED UNITS
- UP TO FOUR FULLY ISOLATED OUTPUT CHANNELS (Model 710)
- SMALL SIZE

AC/DC CONVERTERS

	Dual ±15VDC Supplies							5VDC Logic Supplies		
	PC Board Mount					Chassis Mount		PC Board Mount		
Model	550	551	552	553	554	556	558	560	561	562
RATED OUTPUT										
Voltage (nom)	±15V	±15V	±15V	±15V	±15V	±15V	±15V	5V[1]	5V[1][2]	5V[1][2]
Current (max)	±25mA	±50mA	±100mA	±200mA	±350mA	±200mA	±500mA	250mA	500mA	1000mA
RATED INPUT										
Voltage	105 - 125VAC, 50 - 400Hz					105 - 125VAC 50 - 400Hz		105 - 125VAC, 50 - 400Hz		
Options[3]	E, F, H					E,F,H		E, F, H		
REGULATION										
No load to full load (max)	±0.1%	±0.05%	±0.05%	±0.05%	±0.02%	±0.05%	±0.05%	±0.1%	±0.1%	±0.1%
Over rated line voltage (max)	±0.05%	±0.05%	±0.05%	±0.05%	±0.02%	±0.05%	±0.05%	±0.05%	±0.05%	±0.05%
OUTPUT RIPPLE AND NOISE										
At full load, rms (max)	2mV	0.5mV	0.5mV	0.5mV	0.5mV	1mV	1mV	1mV	1mV	1mV

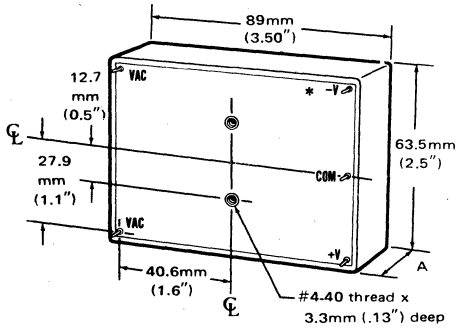
DC/DC CONVERTERS ±15VDC Output

	Low Profile	Isolated[6]	
MODEL	546	700/700U[4]	710[5]
RATED INPUT			
Voltage	4.5VDC to 5.5VDC	10VDC to 18VDC	10VDC to 18VDC
Current, Quiescent	400mA, max	20mA at ±3mA load	40mA at total output of 24mA
Current, full load	1.8A, max	89mA max at ±30mA load	100mA at total output of 76mA
RATED OUTPUT			
Voltage (no load)	±15V	$\pm V_{IN}$ w/1V tolerance	4 sets of $\pm V_{IN}$ w/1V tolerance
Current	120mA, max	total 60mA, max.	total 76mA max; any single output -60mA, max
Short circuit current	180mA, max	120mA, max	120mA, max
REGULATION			
Line at full load	0.1%, max	—	—
Load, zero to full load	0.02% typ, 0.1% max	35mV/mA	75mV/mA
OUTPUT VOLTAGE TEMP. COEFFICIENT	±3mV/°C	—	—
OUTPUT RIPPLE	10mV peak, typ; 20mV peak, max; 0.8mV, rms max	±15mV peak at ±3mA load; ±80mV peak, max, at ±30mA load	±25mV peak at ±3mA load; ±80mV peak; max, at ±9.5mA load
INPUT-OUTPUT ISOLATION			
Test voltage, 5sec at 60Hz		4200Vp/5000Vp	2200V, rms
Voltage, continuous, derated	300VDC	1500Vp/2000Vp	600V, rms, 1000Vp
Impedance	$10^{10}\Omega$ || 50pF	$10^{10}\Omega$ || 5pF/$10^{10}\Omega$ || 3pF	$10^{10}\Omega$ || 8pF
Leakage current at 240V/60Hz, tested		1μA, max	1μA, max
TEMPERATURE RANGE			
Operating	0°C to 71°C	-25°C to +85°C	-25°C to +85°C
Storage	-55°C to +100°C	-55°C to +125°C	-55°C to +110°C

1. The output may be connected as +5V or -5V.
2. These 5V supplies have over-voltage protection which limits the output voltage to 7V (max) in a fault condition.
3. International input voltage rating available. Specify: E option - 205VAC to 240VAC, 50Hz to 400Hz.
   F option - 90VAC to 110VAC, 50Hz to 400Hz.
   H option - 220VAC to 260VAC, 50Hz to 400Hz.
4. Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields. Model 700M and 700UM are similar to Models 700, 700U but, in addition, they are 100% screened to patient connected circuit requirements for the leakage current (par. 27.5) and dielectric withstand voltage (par. 31.11) of UL544. See Product Data Sheet for complete specifications.
5. Model 710 provides 4 channels (sets) of isolated outputs. See Product Data Sheet for complete specifications.
6. For newer designs, the models 722 and 724 (hybrid isolated DC/DC converters) which are smaller in size and better in performance are recommended. Please refer to models 722 and 724 product data sheets.

PACKAGE DRAWINGS

DRAWING NO. 1



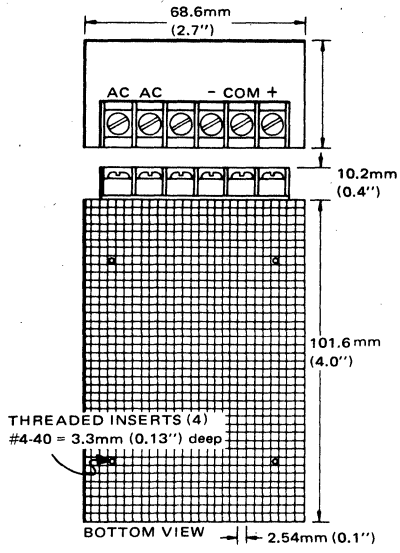
Pin Diameter 1.02mm (0.04")
* No Connection for Models 560, 561, 562.

For Models 550, 551, 560 – A = 22.2mm (0.875")
Weight: 340 grams (12 oz)

For Models 552, 553, 561, 562 – A = 32mm (1.25")
Weight: 425 grams (15 oz)

For Model 554 – A = 4.1cm (1.62")
Weight: 750 grams (26 oz)

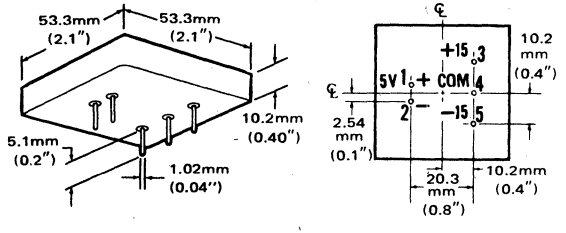
DRAWING NO. 2



For Model 556 – A = 36.6mm (1.44")

For Model 558 – A = 50.8mm (2.00")

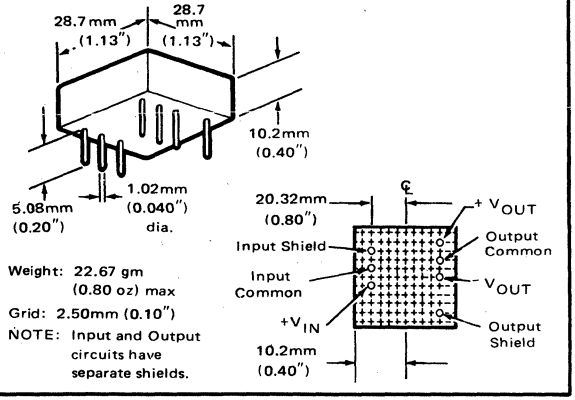
DRAWING NO. 3 Model 546



WEIGHT - 50 grams (1.7 oz)

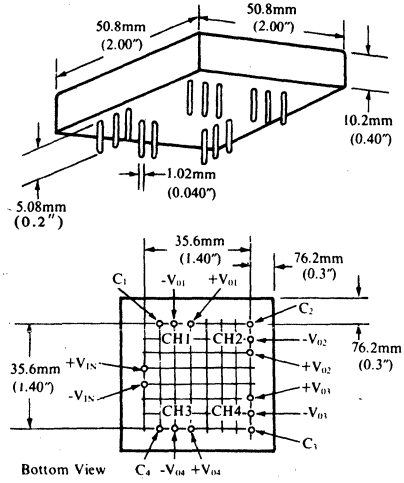
BOTTOM VIEW

DRAWING NO. 4 Model 700



Weight: 22.67 gm
(0.80 oz) max
Grid: 2.50mm (0.10")
NOTE: Input and Output
circuits have
separate shields.

DRAWING NO. 5 Model 710



Weight: 25 grams (0.9 oz.)
Grid: 5.08mm (.20")

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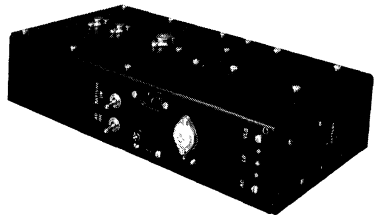


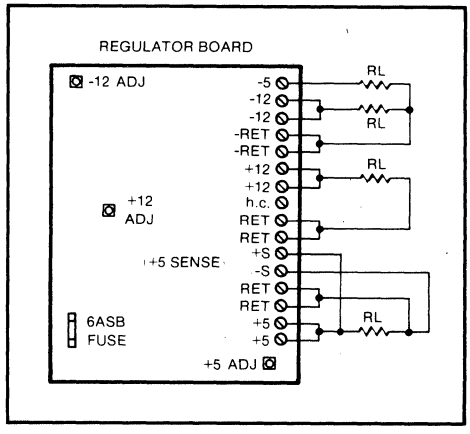
PSB100

REGULATED DC POWER SUPPLY WITH BATTERY BACK-UP

DESCRIPTION

Customers building critical control systems can now purchase a power supply with a self-contained battery back-up, eliminating the need for separate, expensive UPS systems.

PSB100 supplies all common voltages used in microcomputer systems, such as the Multibus™ system. The supply unit includes an internal 24V battery pack and charger, three TTL outputs and LED indicators that indicate power system status. Signals are provided for line power loss, low battery, and very low battery. Internal batteries provide a minimum of 30 minutes back-up at full load. An external 24VDC battery pack can be added to extend back-up time.



INPUT

Line Voltage	(1) 100-130VAC/200-260 VAC
Battery (Internal)	(2) 18-24 VAC 2.5AHR
Line Fuse	1.5ASB-115VAC/.75ASB-230VAC

(1) Operation above 130/260VAC may damage unit. 115/230VAC operation is switch selectable.

(2) An external 24VDC lead acid battery may be connected. No fuse protection is provided for the external battery.

OUTPUTS

		RIPPLE (MAX)	CURRENT	CURRENT LIMIT
+5VDC	±5%	150mV P-P	11.2A	12.0A ±5%
+12VDC	±5%	360mV P-P	1.2A	1.5A ±5%
-12VDC	±5%	360mV P-P	1.2A	1.5A ±5%
-5VDC	±1%	40mV	100mA	NONE

Multibus™ - Intel Corp.

OPERATION

1. Insure proper line and load connection to unit.
2. Insure proper line voltage selection, 115/230VAC.
3. Place AC switch in ON position; the AC indicator should light. The unit is now operating.
4. Place BATTERY switch in ON position. Battery back-up of supply is now operational. Note that the supply is not battery-startable.
5. To turn unit off once started, both the AC switch and the BATTERY switch must be in the OFF position.

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BATTERY BACK-UP

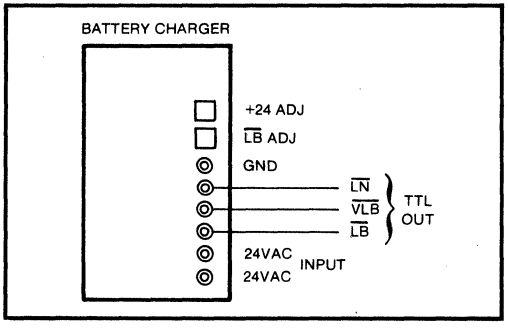
PSB100 contains a 24VDC 2.5 AHR lead acid battery pack. The battery is charged and maintained by an internal battery charger. Upon loss of AC power, the battery will maintain operation of a full load for 30 minutes minimum if fully charged. An external 24VDC rechargeable battery may be connected if desired. If an external battery is installed, the internal battery should be disconnected (remove battery fuse). The internal charger will supply 24VDC at 500mA to charge or maintain external batteries.

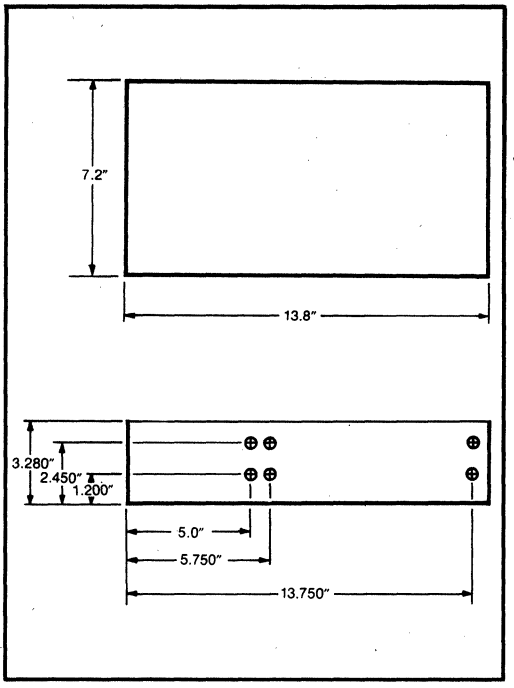
BATTERY CHARGER

24VDC at 500mA
Low battery (LB) indication 21VDC
Very low battery (VLB) indication 19.5VDC

LB and VLB indication are operational only during battery discharge cycle.

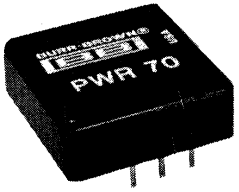
Three TTL compatible outputs are provided on the charger circuit board for low battery (LB), very low battery (VLB) and line loss (LN). All three outputs are active low.





BURR-BROWN®

PWR70



ISOLATED DC/DC CONVERTER
Low Cost—Unregulated Outputs
OUTPUT POWER TO 3 WATTS

FEATURES

- OUTPUT POWER TO 3 WATTS
- HIGH ISOLATION VOLTAGE 2000VDC
- SIX-SIDED SHIELDING
- INPUT AND OUTPUT FILTERING
- LOW PROFILE PACKAGE 0.4" HIGH

APPLICATIONS

- SPOT REGULATOR
- POWER FOR DATA ACQUISITION, OP AMPS, ETC.
- PROCESS CONTROL
- PORTABLE EQUIPMENT
- TEST EQUIPMENT

DESCRIPTION

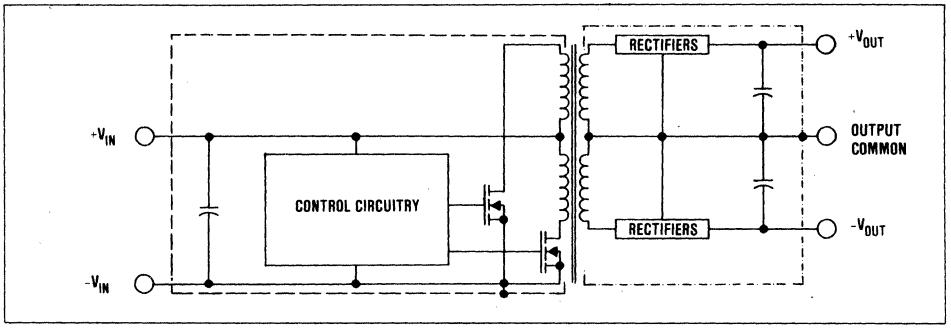
The PWR70 is a single-channel, dual-output DC/DC converter designed for general purpose power conversion applications where high efficiency is more important than load regulation.

The PWR70 provides a plus and minus output voltage approximately equal to the input voltage magnitude. It operates over an input voltage range of 10VDC to 18VDC. Isolation voltage is a minimum of 2000VDC.

Six-sided shielding suppresses electromagnetic radiation which could disturb sensitive analog measurements or interfere with system timing signals. Input filtering minimizes reflected ripple current. Output ripple voltage and switching transients are reduced by filtering the PWR70 outputs.

Momentarily connecting an output pin to the output common will not damage the PWR70. Short circuit protection is accomplished by using power MOSFETs in the PWR70's input circuitry.

SIMPLIFIED CIRCUIT DIAGRAM



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{IN}$ = 15VDC, and I_{OUT} = ±15mA unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Rated Voltage			15		VDC
Voltage Range		10		18	VDC
Input Current	I_{OUT} = ± 3mA		25		mA
	I_{OUT} = ±33mA			100	mA
Ripple Current	I_{OUT} = ± 3mA		±10		mA, pk
	I_{OUT} = ±33mA		±10		mA, pk
ISOLATION					
Rated Voltage		2000			VDC
Resistance			10G		Ω
Capacitance			6		pF
Leakage Current	V_{ISO} = 240VAC, 60Hz			1	μA
OUTPUT					
Rated Voltage			±15		VDC
Voltage Accuracy				3	%
Rated Current			±15		mA
Current Range		0		±100	mA
Line Regulation	10VDC ≤ V_{IN} ≤ 18VDC		1.08		V/V
Load Regulation	±3mA ≤ I_{OUT} ≤ ±33mA		35		mV/mA
Ripple Voltage	I_{OUT} = ±3mA		±10		mV, pk
	I_{OUT} = ±33mA			±80	mV, pk
TEMPERATURE					
Specification		-25		+85	°C
Operating		-55		+125	°C
Storage		-65		+150	°C

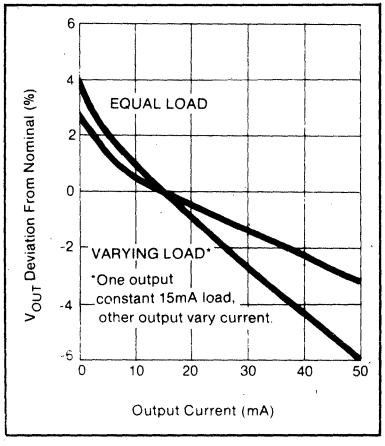


FIGURE 1. Load Regulation.

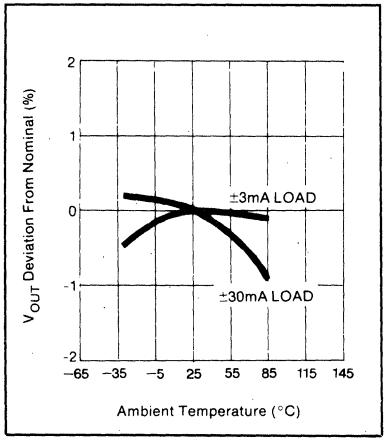
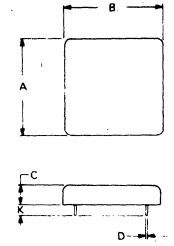


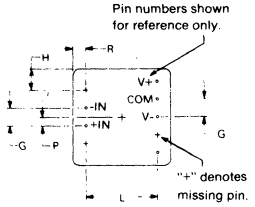
FIGURE 2. Temperature Drift.

ABSOLUTE MAXIMUM RATINGS

Input Voltage 18VDC
Output Current ..... ±150mA
Output Short-Circuit Duration ..... Momentary

MECHANICAL



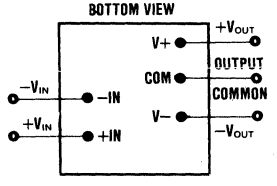


NOTE: Input and output circuits have separate shields.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.075	1.135	27.31	28.83
B	1.075	1.135	27.31	28.83
C	.350	.410	8.89	10.41
D	.038	.042	0.97	1.07
G	.200 BASIC		5.08 BASIC	
H	.212	.312	5.38	7.92
K	.170	.350	4.32	8.89
L	.800 BASIC		20.32 BASIC	
P	.100 BASIC		2.54 BASIC	
R	.112	.212	2.84	5.38

Material: Black Epoxy
Weight: 22.67 gm (0.80 oz.)
Grid: 2.50mm (0.10")

CONNECTION DIAGRAM



NOTE: Input and output circuits have separate shields. Input shield is connected to $-V_{IN}$. Output shield is connected to output common.

BURR-BROWN®

700/700U

ISOLATED DC-TO-DC CONVERTER

FEATURES

- HIGH BREAKDOWN VOLTAGE 5000V PEAK
- LOW LEAKAGE CAPACITANCE ≈ 3pF
- SHIELDED AND UNSHIELDED UNITS
- COMPLETELY SPECIFIED

APPLICATIONS

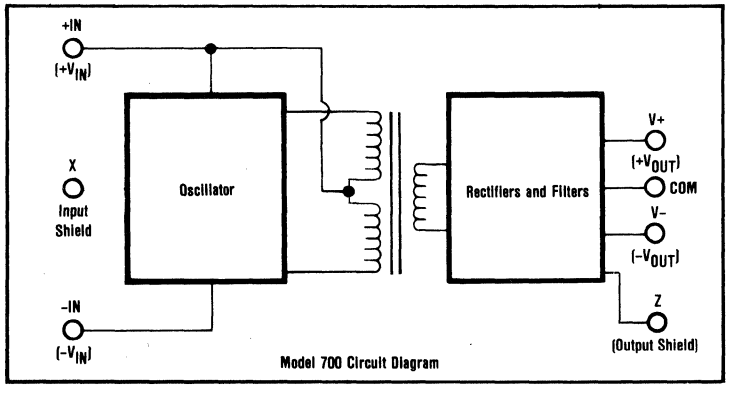
- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTATION
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS

BENEFITS

- HIGH VOLTAGE RATING PROTECTS EXPENSIVE INSTRUMENTATION
- LOW LEAKAGE CURRENT PROTECTS HUMAN LIFE
- EXCELLENT ISOLATION CMR IMPROVES SYSTEM PERFORMANCE
- SHIELDING PREVENTS ELECTROSTACTIC AND EMI PROBLEMS

DESCRIPTION

The Model 700 converts a 10VDC to 18VDC input to a dual output of the same value as the input voltage. The internal hybrid integrated circuit reduces size and cost. A self-contained frequency stable 130kHz oscillator drives switching circuitry which is designed to minimize the common problem of spiking due to transformer saturation. Regulation and short circuit protection, if desired, can easily be added (see Figure 3). Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields.



Model 700 Circuit Diagram

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SPECIFICATIONS

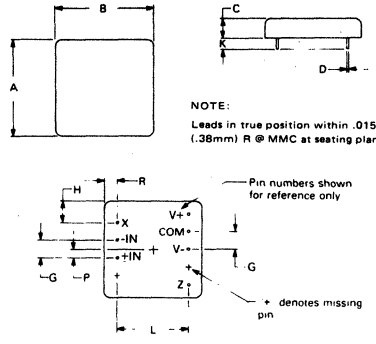
ELECTRICAL

Typical at 25°C with 15VDC supply unless otherwise noted.

MODEL	700/700M	700U/700UM
INPUT		
Voltage Range(1)	10V to 18V	
Current at ±3mA Load	20mA	
Current at ±30mA Load	±100mA, max	
Ripple Current at ±3mA Load	±3mA, peak	
Ripple Current at ±30mA Load	±100mA, peak	
ISOLATION(2)		
Voltage, Test, 5sec at 60Hz	4200V, p	5000V, p
Voltage, Continuous, derated	1500V, p	2000V, p
Impedance	10GΩ || 5pF	10GΩ || 3pF
Leakage Current at 240V/60Hz	1μA, max	1μA, max
OUTPUT		
V_{OUT} at ±3mA to ±30mA Load	$\pm V_{IN}$ with ±1V tolerance	
Operating Current total of both outputs	60mA, max	
Safe Nondestructive Current at 25°C	120mA, max	
Sensitivity to Input Voltage	1.08V/V	
Load Regulation	35mV/mA	
Ripple Voltage at ±3mA Load	±15mV, peak	
Ripple Voltage at ±30mA Load	±80mV, peak max	
Balance of +V and -V at +I = -I	±20mV	
TEMPERATURE RANGE		
Operating	-25°C to +85°C	
Storage	-55°C to +125°C	

NOTES:
1. Derate to 16V max between $+V_{IN}$ and $-V_{IN}$ above 70°C.
2. A medical grade unit is available which is 100% screened to Patient Connected Circuit requirements for the leakage current (par. 27.5) and dielectric withstand voltage (par. 31.11) of UL544. Specify 700M or 700UM.

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.075	1.135	27.31	28.83
B	1.075	1.135	27.31	28.83
C	.350	.410	8.89	10.41
D	.038	.042	0.97	1.07
G	.200 BASIC		5.08 BASIC	
H	.212	.312	5.38	7.92
K	.170	.350	4.32	8.89
L	.800 BASIC		20.32 BASIC	
P	.100 BASIC		2.54 BASIC	
R	.112	.212	2.84	5.38

Material: Black Epoxy
Weight: 22.67 gm (0.80 oz.)
Grid: 2.50mm (0.10")

NOTE: Input and Output circuits have separate shields.

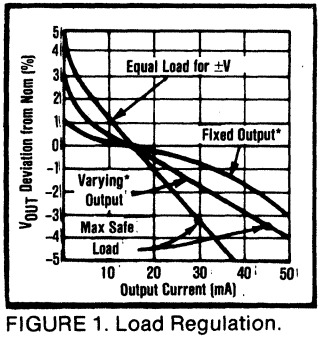


FIGURE 1. Load Regulation.

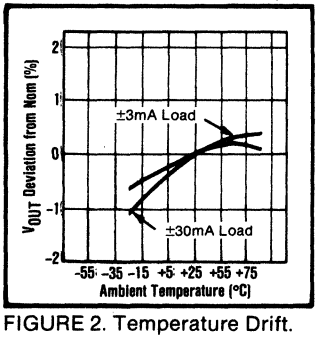


FIGURE 2. Temperature Drift.

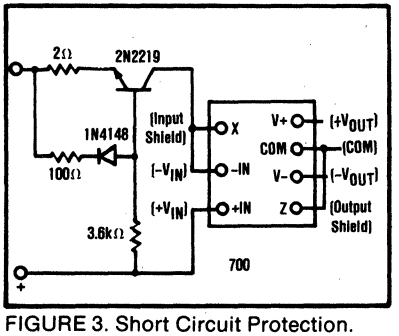


FIGURE 3. Short Circuit Protection.

*For one output with constant 15mA load and varying current on other output. (A minimum load of 3mA is recommended for each output).

USE WITH ISOLATION AMPLIFIERS:

When the Model 700/700U is used with isolation amplifiers such as the Burr-Brown 3650 and 3652 special attention should be given to current ratings to avoid over designing. Since the isolation amplifiers do not draw maximum current simultaneously from the V+ and V− Model 700/700U terminals, it is possible to drive more isolation amplifiers per Model 700/700U than one might initially expect. The Model 700/700U is capable of providing a total output current of 60mA balanced or unbalanced between the two outputs. A minimum load of 3mA is recommended for each output.

BURR-BROWN®

710

QUAD-ISOLATED DC-TO-DC CONVERTER

FEATURES

- FOUR ISOLATED ±10VDC to ±18VDC OUTPUTS
- DRIVES FOUR 3650/3652 ISOLATION AMPS
- HIGH BREAKDOWN VOLTAGE, 2200VDC TEST
- LOW LEAKAGE CAPACITANCE, 8pF
- LOW LEAKAGE CURRENT, 1μA @ 240V/60Hz
- LOW COST PER ISOLATED CHANNEL

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The Model 710 converts a single 10VDC to 18VDC input into four dual isolated outputs of the same value as the input voltage. The converter is capable of providing a total of 76mA at rated output voltage accuracy and can provide isolated power to four independently isolated 3650/3652 optically coupled isolation amplifiers with the entire assembly mounted on one 5" x 7" card.

Extensive use is made of hybrid integrated circuits to reduce size and cost. A self-contained frequency stable 130 kHz oscillator drives switching circuitry which is designed to minimize the common problem of spiking due to transformer saturation.

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DESCRIPTION

OUTPUT CURRENT RATINGS

The Model 710 is capable of providing a total of 76mA of output current divided among its eight outputs. The maximum current available from any one output is shown in Figure 9. A minimum average current of 3mA is recommended for each output in order to maintain output voltage accuracy. Thus, the current may be balanced (such as +9.5mA and -9.5mA) or unbalanced (such as +16mA and -3mA). The best output voltage accuracy will be obtained under balanced conditions.

Channels may be connected in series or parallel for higher voltage or current. For parallel operation connection of channel 1 to 2 or channel 3 to 4 will result in lowest ripple.

In some cases the 710 may drive larger loads than would be apparent from a cursory examination of the specifications. For example, see Figures 1 and 2. The most total current drawn from the pair of $+V_o$ and $-V_o$ output is $I_{max} + I_Q$ (not 2 x I_{max}). For the 3650 this is a maximum of 12mA +1.2mA = 13.2mA (instead of 24mA).

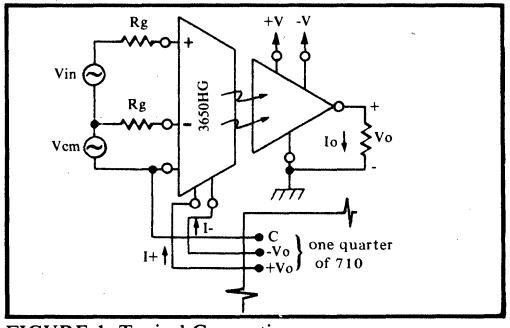


FIGURE 1. Typical Connection

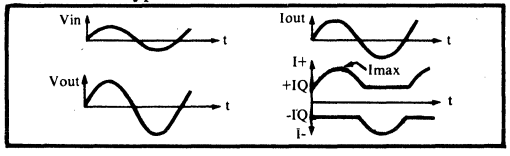


FIGURE 2. Waveforms

ISOLATION VOLTAGE RATINGS

It is important that the user understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated minimum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000$ V. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

* Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS I-109 and ICS I-111.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 710 in order to protect it from damage in situations where too much current is demanded from the outputs – such as a short circuit from an output to its common. The circuit limits the input current to approximately 100 mA for an input voltage of 15 VDC (for β of 2N2219 of 50).

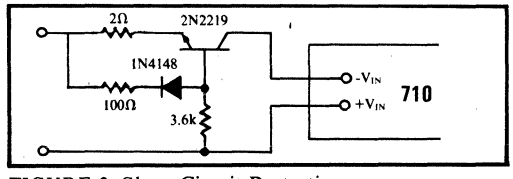


FIGURE 3. Short Circuit Protection

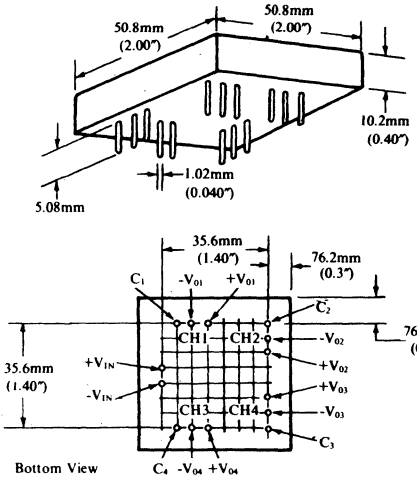
SPECIFICATIONS

Typical at 25°C with 15V supply unless otherwise noted.

ELECTRICAL

MODEL	710
INPUT	
Voltage Range[1][2]	10V to 18V
Current at Total Output Current of 24mA	40mA
Current at Total Output Current of 76mA	100mA, max
Ripple at Total Output Current of 24mA	15mA, peak
Ripple at Total Output Current of 76mA	40mA, peak
ISOLATION[3]	
Voltage Accuracy[5]	2200V, rms at 60Hz
Current for Rated Accuracy: Total of all currents	600V, rms AC, 1000VDC
Maximum Current: Any one output	10GΩ ‖ 8pF
Leakage Current at 240V/60 Hz	1μA, max
OUTPUT	
Voltage Accuracy[5]	See Figure 8
Current for Rated Accuracy: Total of all currents	76mA, max
Any one output	60mA, max
Total Safe Nondestructive Current at 25°C	120mA, max
Sensitivity to Input Voltage	1.08V/V
Load Regulation[6]	75mV/mA
Ripple Voltage at ±3mA Load	±25mV, peak
Ripple Voltage at ±9.5mA Load	±80mV, peak max
Balance of +V and -V at +I = -I	±20mV
ΔV_{out} vs Temperature -25°C to +85°C	3.0%
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +110°C

MECHANICAL



Material: Black Epoxy
Weight: 25 grams (0.9 oz.)
Grid: 5.08mm (.20")
Pin: Material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

NOTES:
1. Derate to 16V max between $+V_{IN}$ and $-V_{IN}$ above 70°C.
2. Operation down to 5V is possible with reduced output current and accuracy.
3. Isolation specifications are applicable to input to output isolation as well as channel to channel isolation.
4. See discussion on previous page; 2200V, rms ≃ 3000V peak.
5. A minimum output current of ±3mA per channel is recommended to maintain output voltage accuracy.
6. Load regulation for one channel with other channels at ±9.5mA load.

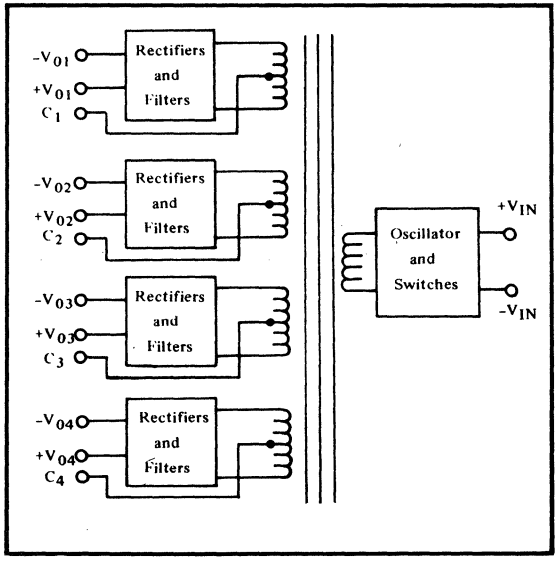


FIGURE 4. Functional Diagram

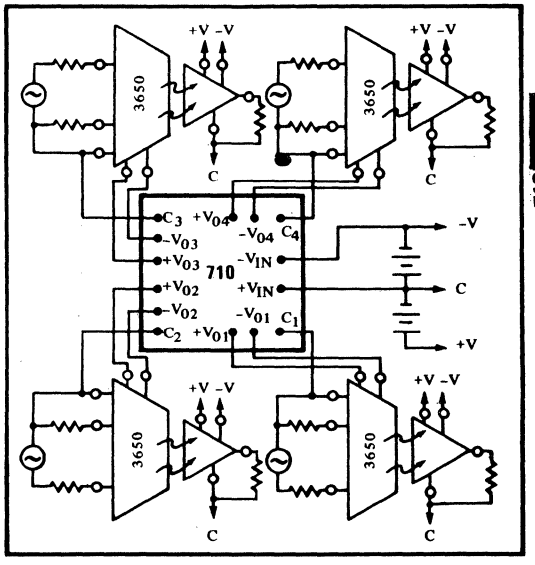


FIGURE 5. Typical Connection with Four 3650 Isolation Amplifiers.

TYPICAL PERFORMANCE CURVES

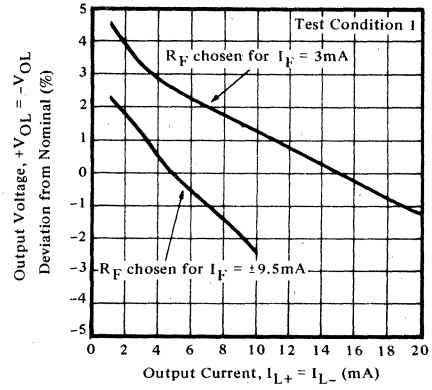


FIGURE 6. LOAD REGULATION - balanced load

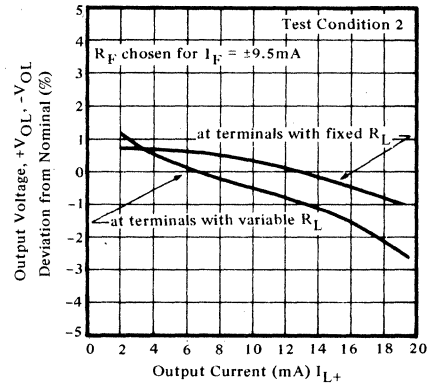


FIGURE 7. LOAD REGULATION - unbalanced load

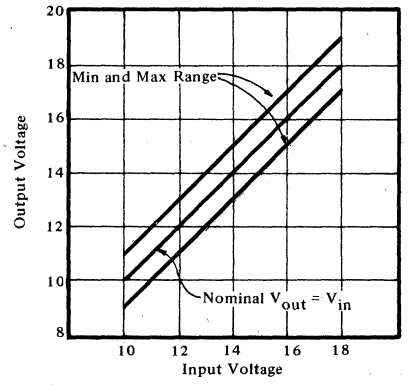


FIGURE 8. OUTPUT VOLTAGE ACCURACY VS INPUT VOLTAGE

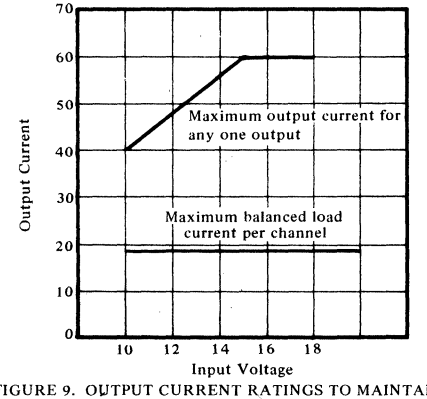


FIGURE 9. OUTPUT CURRENT RATINGS TO MAINTAIN OUTPUT VOLTAGE TOLERANCE

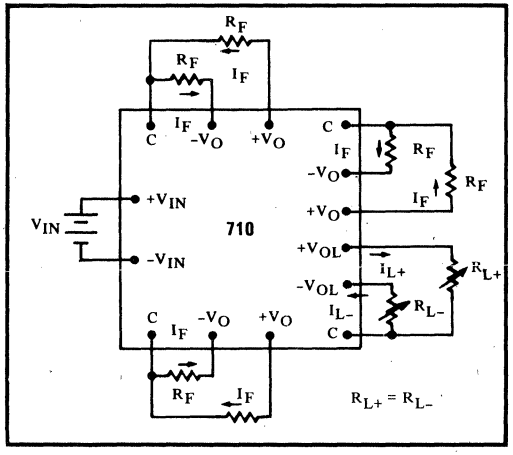


FIGURE 10. Test Condition 1: Balanced Load

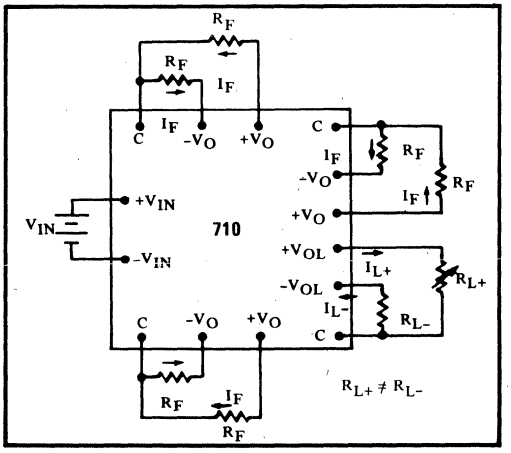


FIGURE 11. Test Condition 2: Unbalanced Load

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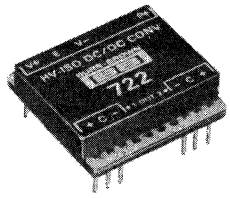


722

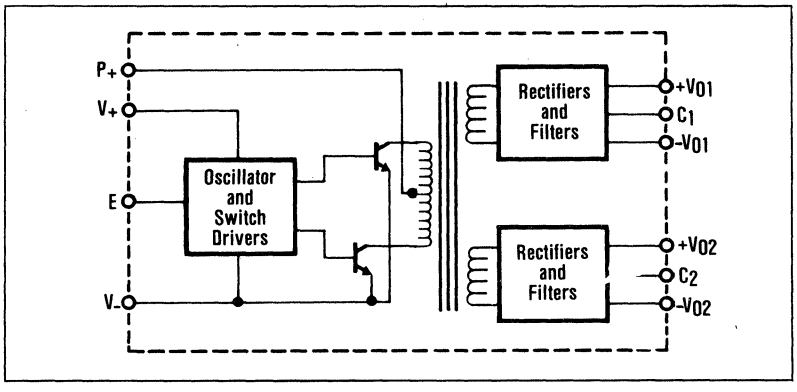
DUAL ISOLATED DC/DC CONVERTER

FEATURES

- DUAL ISOLATED ±5V TO ±16V OUTPUTS
- HIGH BREAKDOWN VOLTAGE, 8000V TEST
- LOW LEAKAGE CURRENT, <1 μA AT 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE, 27.9mm x 27.9mm x 7.6mm (1.1" x 1.1" x 0.3")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION



DESCRIPTION

The 722 converts a single 5VDC to 16VDC input into a pair of bipolar output voltages of the same value as the input voltage. The converter is capable of providing a total output current of 64mA at rated voltage accuracy and up to 250mA without damage.

The two output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage or in parallel for higher output current, as a single channel isolated DC/DC converter.

Integrated circuit construction of the 722 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 900kHz oscillator drives switching circuitry which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.

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DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 722 is capable of providing 64mA divided among its four outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

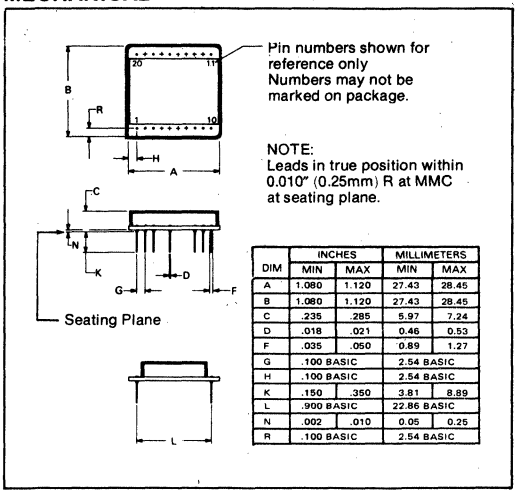
The fact that the two outputs of the 722 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows Burr-Brown's 3650 Optically Coupled Isolation Amplifier connected in three-port configuration. One of the 722 channels provides power to the 3650's input. The other channel supplies power to the 3650's output. The amplifier's input and output are isolated from each other and the system's power supply common. In this configuration the 722's channel-to-channel isolation specification applies to the amplifier input-to-output voltage.

Figure 3 illustrates how the 722 may provide isolated input power to the input stage of two 3650's connected in the two-port configuration. Power for the output stage is provided by the system +15V and -15V supplies. Input stages are isolated from each other and from the system supply. In this situation the 722's input-to-output isolation specification applies to the amplifiers' input-to-output voltages while the channel-to-channel 722 specification applies to the voltage existing between "I/P Com # 1" and "I/P Com # 2."

(1) "output" denotes a single output terminal (+V or -V) and its associated common
(2) "channel" denotes a pair of outputs (+V and -V) and their associated common

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.080	1.120	27.43	28.45
B	1.080	1.120	27.43	28.45
C	.235	.285	5.97	7.24
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.100 BASIC		2.54 BASIC	

SHORT CIRCUIT PROTECTION

The circuit in Figure 2 may be added to the input of the 722 to protect it from damage in situations where too much current is demanded from the outputs - such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

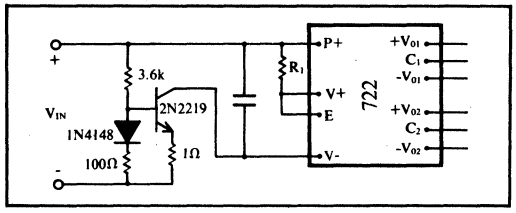


FIGURE 2. Short Circuit Protection

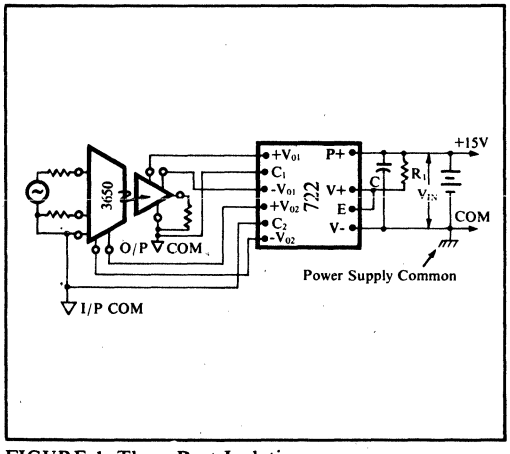


FIGURE 1. Three-Port Isolation

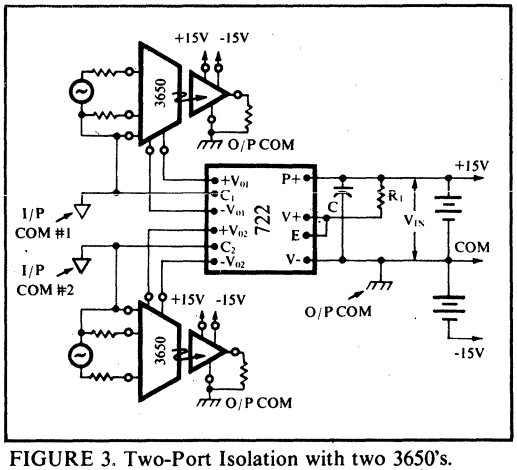


FIGURE 3. Two-Port Isolation with two 3650's.

ELECTRICAL SPECIFICATIONS

Specifications at T_A = +25°C, V_{IN} = 15VDC, C = 0.47μF, R_1 Selected per Typical Performance Curve.

PARAMETER	CONDITIONS	722			722BG			722MG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
Rated Input Voltage			15			•			•		VDC
Input Voltage Range(1)		5		16	•		•	•		•	VDC
Input Current	Total output current = 12mA		50			•			•		mA
	Total output current = 64mA		105	120		•	•		•	•	mA
	Total output current = 64mA at T_A = +85°C		120			•			•		mA
	Total output current = 160mA		-	-		225	275		-	-	mA
Input Ripple(2)	Total output current = 12mA		3			•			•		mA, pk
	Total output current = 64mA		6			•			•		mA, pk
	Total output current = 160mA		-			12			-		mA, pk
ISOLATION											
Test Voltages(3)	Input-to-output, 5 seconds, min			8000			•			•	V, pk
	Input-to-output, 1 minute, min			-			-			2500	V, rms
	Channel-to-channel, 5 seconds, min			5000			•			•	V, pk
Rated Voltage(3)	Input-to-output, continuous			3500			•			•	V
	Channel-to-channel, continuous			2000	•		•			•	V
Isolation Impedance	Input-to-output		10‖6			•			•		GΩ‖pF
Leakage Current(4)	Input-to-output, 240V, 60Hz			1			•			•	μA
OUTPUT											
Rated Output Voltage(5)	I_{Load} = 3mA per output	15.4		16.0	•		•	•		•	VDC
	I_{Load} = 16mA per output	14.3		15.3	•		•	•		•	VDC
	I_{Load} = 40mA per output	-	-	-	13.7	14.2	15.0	-	-	-	VDC
Output Current	Total of all outputs			200			•			•	mA
	Any one output(6)	3		100	•		•	•		•	mA
Load Regulation			Note 5			•			•		
Ripple Voltage	I_{Load} = 3mA per output		15			•			•		mV, pk
	I_{Load} = 16mA per output		35	100		•	•		•	•	mV, pk
	I_{Load} = 40mA per output		-			50			•		mV, pk
Tracking Error Between Dual Outputs	Balanced loads		±100			•			•		mVDC
Sensitivity to Input Voltage Changes			1.13			•			•		V/V
Output Voltage Temperature Coefficient	T_A = $T_{Specification\ Range}$		±0.02			•			•		%/°C
TEMPERATURE											
Specification	$I_{Load} \leq$ 16mA per output	-25		+85	•		•	•		•	°C
	$I_{Load} \leq$ 40mA per output	-25		+60	•		•	•		•	°C
Storage		-55		+125	•		•	•		•	°C
Junction Temperature				+125			•			•	°C

*Specifications same as 722.

NOTES:
1. For ambient temperature above 70°C the input voltage is 12.5V max. The input voltage remains 16V max if case temperature is kept below 85°C.
2. External capacitor across "P+" to "V-" pins and 12" of #24 wire to V_{IN}.
3. Relationship between test and rated is $V_{test} = (V_{rated} \times 2) + 1000V$.
4. Reference UL544, paragraph 27.5, Leakage Current.
5. See "Typical Performance Curves".
6. A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.

INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 722 are shown in Figures 1 and 3. Primary power (V_{IN}) is applied at the "P+" and "V-" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V-"; the only requirement is that "P+" and "V+" must be positive with respect to "V-."

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor R_1. The value of R_1 as a function of V_{IN} is shown in the TYPICAL PERFORMANCE CURVES section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5V to +7.5V positive with respect to "V-". If a separate source is used, the V+ input must be applied before the "P+" input to avoid possible damage to the unit. P+ and V+ must remain positive with respect to V- at all times (including transients). If necessary, diode clamps should be put across these inputs.

The "E" pin enables the converter when connected to "V+" and disables it when connected to "V-."

An external capacitor, "C", (0.47μF ceramic) is used to reduce input ripple. It should be connected as close to the "P+" and "V-" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 722 is not internally shielded, external shielding may be appropriate in applications where RFI at the 900kHz nominal oscillator frequency is a problem.

Each output is filtered with an internal 0.22μF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10μF between each output and its common.

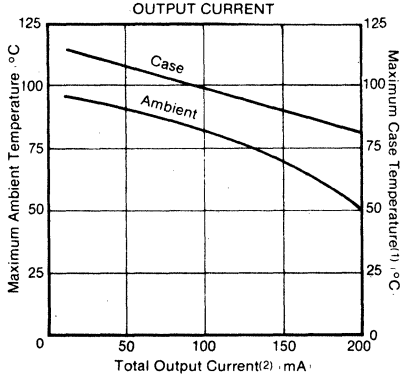
TYPICAL PERFORMANCE CURVES

Specifications at $T_A = +25°C$, $V_{IN} = 15VDC$, $C = 0.47\mu F$, R_1 selected per typical performance curve.

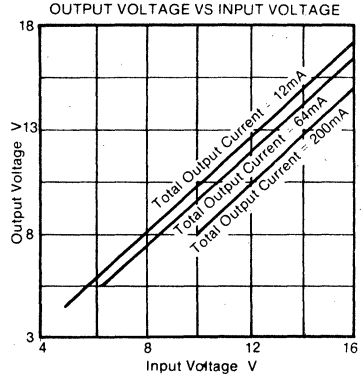
SELECTION OF R_1 OR EXTERNAL VOLTAGE V+ FOR MINIMUM INTERNAL POWER DISSIPATION

Input Voltage V	Maximum Output Current From Any Single Output		
	<16mA	16mA to 30mA	>30mA
>13	1.3kΩ	820Ω	510Ω
11 to 13	820Ω	510Ω	200Ω
9 to 11	510Ω	200Ω	0Ω
8 to 9	200Ω	0Ω	-
<8	0Ω	-	-
→ V+EXT	6.5V	7.5V	9.0V

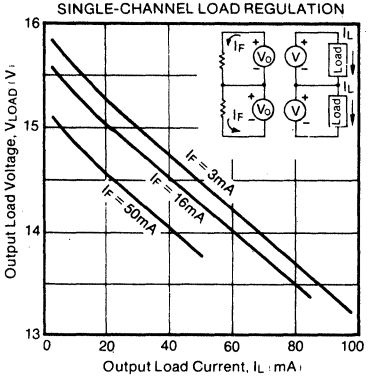
MAXIMUM SAFE OPERATING TEMPERATURE VS TOTAL OUTPUT CURRENT



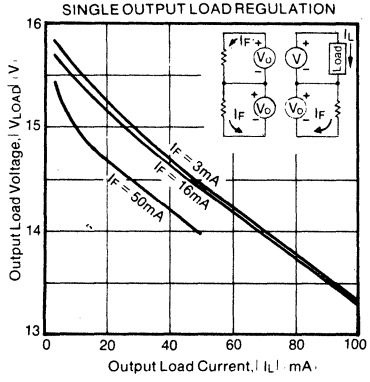
OUTPUT VOLTAGE VS INPUT VOLTAGE



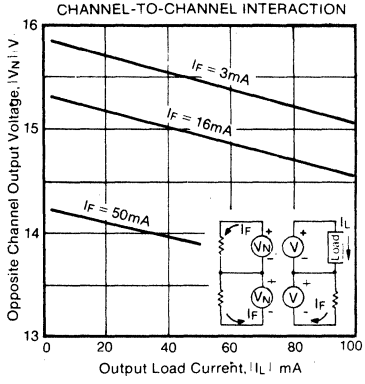
SINGLE-CHANNEL LOAD REGULATION



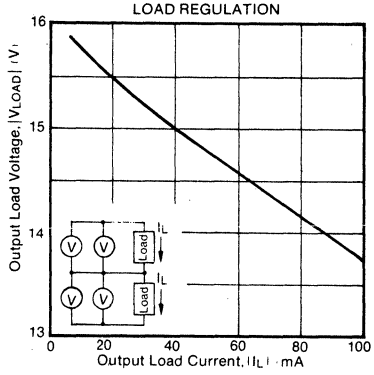
SINGLE OUTPUT LOAD REGULATION



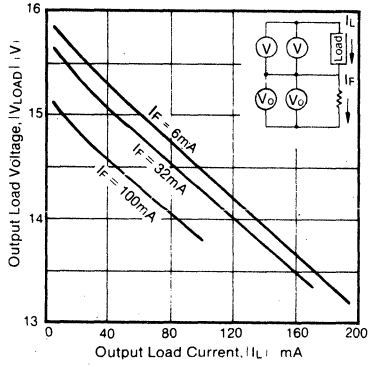
CHANNEL-TO-CHANNEL INTERACTION



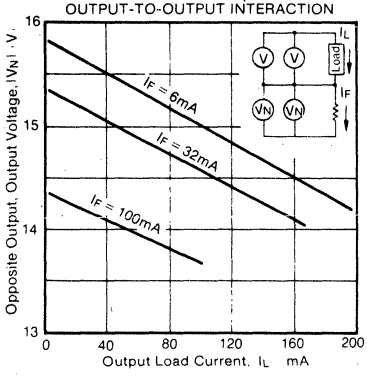
PARALLEL OUTPUT BALANCED LOAD REGULATION



PARALLEL OUTPUT UNBALANCED LOAD REGULATION



OUTPUT-TO-OUTPUT INTERACTION

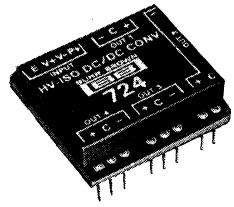


Notes:

1. Using a 104mm x 19mm x 1.6mm aluminum strip mounted to the bottom of the case with heat sink compound.
2. Total output current is the sum of the currents for each individual output.

BURR-BROWN®

724



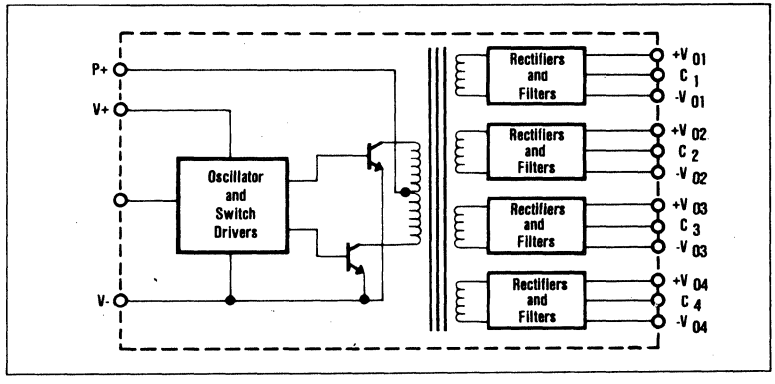
QUAD ISOLATED DC/DC CONVERTER

FEATURES

- QUAD ISOLATED ±8V OUTPUTS
- HIGH BREAKDOWN VOLTAGE, 3000V TEST
- LOW LEAKAGE CURRENT, <1μA AT 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE, 27.9mm x 27.9mm x 6.6mm (1.1" x 1.1" x 0.26")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION



DESCRIPTION

The 724 converts a single 5VDC to 16VDC input into four pairs of bipolar output voltages of approximately half the input voltage. The converter is capable of providing a total output current of 128mA at rated voltage accuracy and up to 500mA without damage.

The four output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage, or in parallel for higher output current as a single channel isolated DC/DC converter.

Integrated circuit construction of the 724 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 800kHz oscillator drives switching circuitry which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.

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724

DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 724 is capable of providing 128mA divided among its eight outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

The fact that the four outputs of the 724 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows two of Burr-Brown's 3650 Optically Coupled Isolation Amplifiers connected in three-port configuration. Two of the 724 channels provide power to the 3650's inputs. The other channels supply power to both 3650's outputs. Each amplifier's input and output are isolated from each other and the system's power supply common. Isolation specification applies to the amplifier input-to-output voltage isolation specification.

Figure 2 illustrates how the 724 may provide isolated input power to the input stage of four 3650's connected in the two-port configuration. Power for the four output stages is provided by the system +15VDC and -15VDC supplies. Input stages are isolated from each other and from the system supply. In this situation the 724's isolation specification applies to the amplifier's input-to-output voltage and to the voltage existing between any two I/P COM terminals.

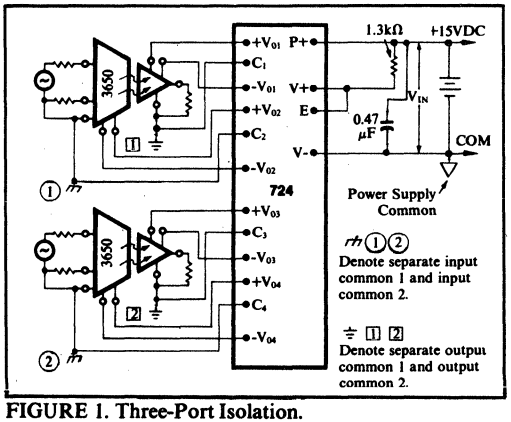


FIGURE 1. Three-Port Isolation.

ISOLATION VOLTAGE RATINGS

Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated maximum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.[3] Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

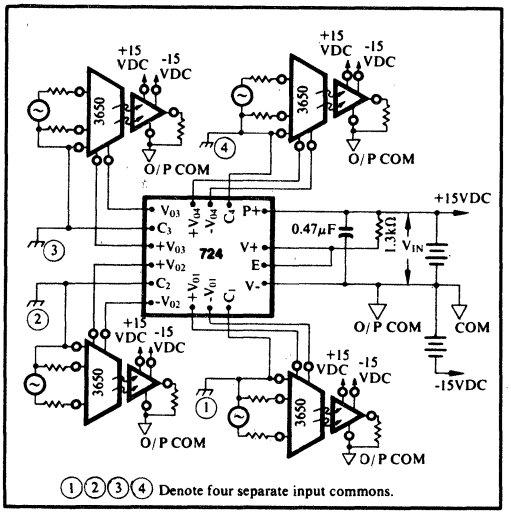


FIGURE 2. Two-Port Isolation with Four 3650's.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 724 to protect it from damage in situations where too much current is demanded from the outputs - such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

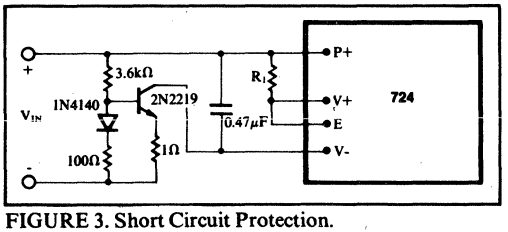


FIGURE 3. Short Circuit Protection.

(1) "output" denotes a single output terminal (+V or -V) and its associated common
(2) "channel" denotes a pair of outputs (+V and -V) and their associated common
(3) Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111.

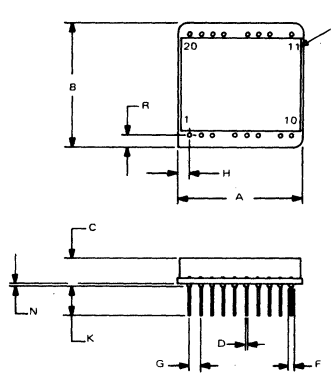
ELECTRICAL SPECIFICATIONS

At 25°C with V_{IN} = 15V, R_L = 1.3kΩ, C = 0.47μF unless noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Input Voltage		5	15	16	VDC
Input Current	Σ I_{OUT} = 24mA		50		mA
	Σ I_{OUT} = 128mA, 25°C		110	125	mA
	Σ I_{OUT} = 128mA, 85°C		120		mA
Input Ripple[1][5]	Σ I_{OUT} = 24mA, C = 0.47μF		10		mA, pk
	Σ I_{OUT} = 128mA, C = 0.47μF			25	mA, pk
ISOLATION					
Test Voltage[2]	Input-to-output, 5sec min			3000	VDC
	Channel-to-channel, 5sec min			3000	VDC
Rated Voltage[2]	Input-to-output, continuous			1000	VDC
	Channel-to-channel, continuous			1000	VDC
Isolation Impedance	Input-to-output		10 ‖ 6		GΩ ‖ pF
Leakage Current	Input-to-output, 240V/60Hz			1.0	μA
OUTPUT					
Voltage[3]	At 15V input I_L = 3mA	8.0	8.5	9.0	V
	I_L = 16mA	7.5	7.9	8.3	V
Current for Rated Voltage	Total of all outputs			128	mA
	Any one output[4]	3			mA
Total Safe Nondestructive Current	Total of all outputs			500	mA
	Any one output			200	mA
Load Regulation[3]			Note 4		
Ripple Voltage[5]	I_L = 3mA		35		mV, pk
	I_L = 16mA			200	mV, pk
Difference of $+V_0$ and $-V_0$	$+I_L = -I_L$		±30		mV
Sensitivity to Input Voltage Change			0.63		V/V
Output Voltage Change Over Temperature	-25°C to +85°C		2		%
TEMPERATURE RANGE					
Operating		-25		+85	°C
Storage		-55		+125	°C

NOTES:
1. 0.47μF external capacitor across "P+" to "V-" pins and 12" of # 24 wire to V_{IN}.
2. See "Isolation Voltage Ratings" on preceding page. The input to output and channel to channel continuous AC rating is 700V, rms.
3. See "Typical Performance Curves."
4. A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.
5. Test bandwidth 10MHz, max.

MECHANICAL



Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.080	1.120	27.43	28.45
B	1.080	1.120	27.43	28.45
C	.235	.285	5.97	7.24
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.100 BASIC		2.54 BASIC	

NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

PIN POSITION	PIN DESIGNATION
1	$+V_{04}$
2	C_4
3	$-V_{04}$
4	No pin present
5	$+V_{03}$
6	C_3
7	$-V_{03}$
8	No pin present
9	$+V_{02}$
10	C_2
11	$-V_{02}$
12	No pin present
13	$+V_{01}$
14	C_1
15	$-V_{01}$
16	No pin present
17	P+
18	V-
19	V+
20	E

INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 724 are shown in Figures 1 and 2. Primary power (V_{IN}) is applied at the "P+" and "V-" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V-"; the only requirement is that "P+" and "V+" must be positive with respect to "V-."

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor R_1. The value of R_1 as a function of V_{IN} is shown in the "Typical Performance Curves" section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5VDC to +7.5VDC positive with respect to "V-." If a separate source is used, the V+ input must be applied before the "P+" input to avoid possible damage to the unit. P+ and V+ must remain positive with respect to V- at all times (including transients). If necessary, diode clamps should be put across these inputs.

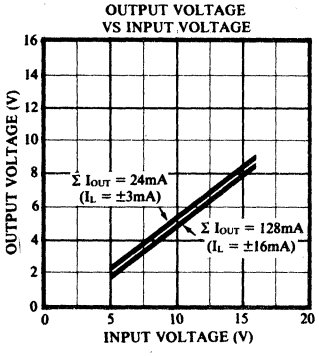
The "E" pin enables the converter when connected to "V+" and disables it when connected to "V-."

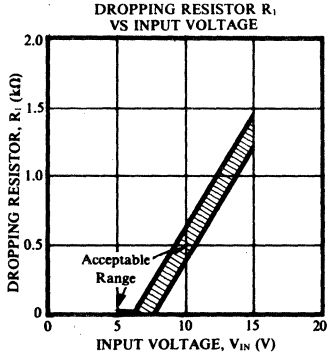
An external capacitor, "C", (0.47μF ceramic) is used to reduce input ripple. It should be connected as close to the "P+" and "V-" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 724 is not internally shielded, external shielding may be appropriate in applications where RFI at the 800kHz nominal oscillator frequency is a problem.

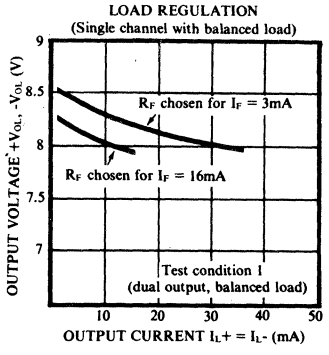
Each output is filtered with an internal 0.047μF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10μF between each output and its common.

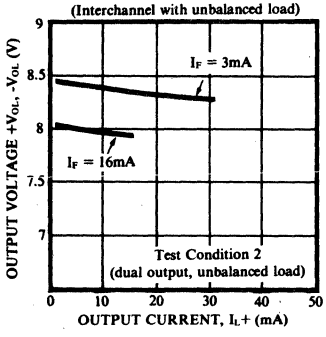
TYPICAL PERFORMANCE CURVES

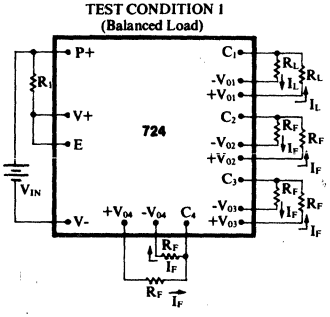
All specifications typical at 25°C unless otherwise noted.

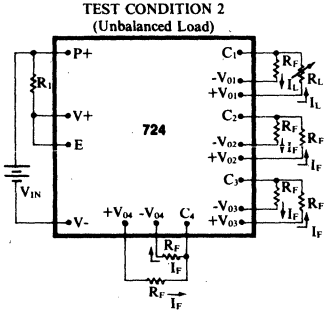












DATA ENTRY AND DISPLAY TERMINALS

MICROTERMINAL™

Pioneering New Concepts In Data Collection

If your system's data entry/control/display requirements are sophisticated but limited in volume, you don't need to buy big, expensive and fragile CRTs or printing terminals to do the job efficiently.

"Microterminal™" terminals—uniquely flexible in application versatility—are designed expressly to fill the human interface demands of widely dispersed control and communications networks—in machine and process control, energy management systems, inventory control and factory floor data collection, and information processing systems. Microterminals™, because of their interface flexibility, appearance, size, durability, and easy installation, function equally well as consoles and control centers for instruments and small systems. They also perform as I/O terminals in diagnostic applications.

Rugged And Reliable

- Tough—100% solid state (no video tubes, no moving parts).
- 0 to +60°C operating temperature range.
- Dust proof/water resistant front panel protects display, indicators, keys.

Easy To Design In

- Very compact (8.5" × 4.5"), mounts on flat surface.
- Operates on factory floor, on the production line, in labs, computer room or office.

Easy To Interface

- Serial ASCII communications.
- EIA RS-232-C/CCITT V.24, 20mA current loop or RS-422.
- 110 to 19,200 baud.
- Up to 63 Microterminal control panels per serial interface.
- Digital I/O available.
- Buffered data entry to reduce on-line time, or data transmission on keystroke for conversational mode.

Easy To Use

- Bar code reader models available.
- Magnetic stripe readers available.
- Full alphanumeric and simple numeric keyboards.
- One stroke function keys enter complex preprogrammed data strings.
- Function indicators to confirm those instructions.
- Indicators to report operational status and steps.
- Tactile touch key feedback that confirms data entry.

Practically Priced

- Low cost terminal functions.
- One-year warranty.
- Complete—no add-ons or interface.
- Simple system integration.
- Special operator training not required.

MICROTERMINAL SELECTION GUIDE

		Low Cost		General Purpose				Digital I/O		MIL Spec	Bar Code Reader[7]		Mag Stripe Reader[7]	
Model Number		TM25 -300-XX	TM27	TM70	TM76	TM71	TM77	TM71 -I/O	TM77 -I/O	TM71M	TM71B -XX	TM77B -XX	TM71MS -XX	TM77MS -XX
Display Type[1]		HEX	HEX	A/N	A/N	A/N	A/N	A/N	A/N	A/N	A/N	A/N	A/N	A/N
Number of Characters in Display		8	8	12	12	16	16	16	16	16	16	16	16	16
Internal Buffer Size (input and output)		8	8	36	36	80	80	80	80	80	80	80	80	80
Keypad Type[1]		HEX & NUM	HEX or NUM	A/N	NUM	A/N	NUM	A/N	NUM	A/N	A/N	NUM	A/N	NUM
Data Transmission[2] (Nonpolled Mode)		Block	[5]	Echo	Echo	Block	Block	Block	Block	Block	Block	Block	Block	Block
Communication Interface[3]		RS232 & C/L	RS422	RS232 & C/L	RS232 & C/L	RS232 & C/L or RS422	same as TM71	same as TM71	same as TM71	RS232 or C/L	RS232 TM71B	same as TM71B or RS422	same as TM71B	same as
Multidrop Capacity		8	63	15	15	15 or 63	15 or 63	15 or 63	15 or 63	N/A	63	63	63	63
Function Keys[4]		7	6	8	8	14	14	14	14	14	16	16	16	16
Baud Rate		300	300 to 4800[6]	300 & 1200	300 & 1200	110 to 19,200	110 to 19,200	110 to 19,200	110 to 19,200	110 to 9600	110 to 19,200	110 to 19,200	110 to 19,200	110 to 19,200
Digital Inputs		No	3	No	No	No	No	No[6]	No[6]	No	No	No	No	No
Digital Outputs w/LED's		No	5	2	2	2	2	2[6]	2[6]	2	2	2	2	2
User EPROM		No	No	No	No	Yes	Yes	Yes	Yes	No	No	No	No	No
8-Bit I/O Port	Output w/LED's	No	No	No	No	No	No	Yes	Yes	No	No	No	No	No
	Bidirectional	No	No	No	No	No	No	Yes	Yes	No	Yes	Yes	Yes	Yes

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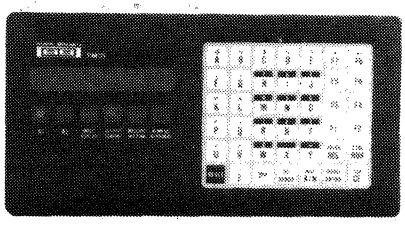
MICROTERMINAL SELECTION GUIDE													
	Low Cost		General Purpose				Digital I/O		MIL Spec	Bar Code Reader[7]		Mag Stripe Reader[7]	
Power Supply	15VDC	8-12VDC voltage regulator	5VDC	5VDC	5VDC	5VDC	5VDC	5VDC	5VDC 20-30 VDC + 15-28 VAC	5VDC or TM71B	same as TM71B	same as TM71B	same as
Unit Price ($)	265	250	495	495	595	595	695	695	5950	1495	1495	1495	1495
Internal Buffer Size (input and output)	8	8	36	36	80	80	80	80	80	80	80	80	80

NOTES: (1) A/N = Alphanumeric, HEX = Hexadecimal, NUM = Numeric. (2) In Echo mode each character is sent upon key press. In Block mode the entire line is sent when Enter key is pressed; no echo is needed. (3) C/L = Current Loop with optical isolation. For TM71, 77, 71-I/O, and 77-I/O add "-21" for RS 422. No suffix for RS232 and C/L. (4) On all but TM25, the function keys can be programmed. (5) TM27 operates only in the polled mode. (6) The TM71-I/O and 77-I/O have 8-bit I/O ports. (7) Re: Two digit suffix "-XX". The first digit designates communication interface: 1 = RS232, 2 = RS422. The second digit is for power supply: 1 = 5VDC, 2 = 20-30VDC and 15-28VAC. (8) 300, 1200, 2400, 4800.

TM71 Microterminal™

Full Feature, High Speed Alphanumeric



You can enter and display alphanumeric data using TM71. Its 42-key keyboard (shiftable to generate 80 characters including A-Z and 0-9) lets you enter messages up to 80 characters long. TM71 operates in standard baud rate steps from 110 to 19,200bps.

A 16-character LED display with horizontal scroll-left/scroll-right keyboard controls allows you to review and edit data entered before it's transmitted. In the edit mode you can backspace and advance the cursor position to insert and delete characters.

Two 80-character buffers are provided for keyboard generated data: the output buffer holds a message being written, reviewed or edited; the transmit buffer holds an already-prepared message ready for CPU acceptance. This feature lets you prepare a second message while the first awaits acceptance by your host CPU. Similarly, two 80-character buffers are available for incoming host CPU-generated messages. Incoming messages are automatically transferred to the input buffer and displayed for operator attention and action.

TM71's display features include host CPU control of flashing, scrolling or blanking features. Host CPU command will also lock out the keyboard. Two LED indicators are independently controlled by the host CPU while four other LEDs indicate terminal status.

In addition to data input and control keys, TM71's keyboard includes programmable function keys that provide fast, one-key input to your host CPU. These function key output codes are set at the factory. If you prefer, you may program these function keys to provide any sequence of up to 80 ASCII characters. These custom function key definitions may be loaded into the TM71 by the host CPU or by inserting an EPROM/ROM module into the terminal. The EPROM/ROM can also control baud rate, multidrop station number and set parity. TM71 offers carefully selected features to enhance and simplify its human and systems interface compatibility: ASCII code; RS-232C/V.24 and 20mA communications with selectable parity; 110 to 19,200 baud; remote reset and two TTL-compatible digital outputs to control external equipment. With the remote "enter" command, the host CPU can test all communications lines and circuitry.

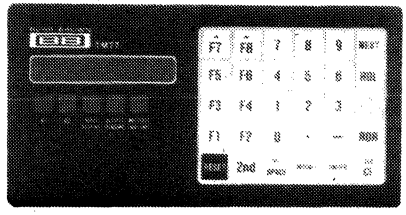
Up to 15 terminals may be connected on the same serial interface. A +5VDC supply requirement further simplifies TM71's application requirements.

Man/machine interface is enhanced with brilliant 0.14" high LED display characters, six LED indicators, and tactile feedback keyboard in the tough, water-resistant front panel.

An RS-422 model is available.

TM77 Microterminal™

An Alphanumeric Display With Simplified Numeric Data Entry

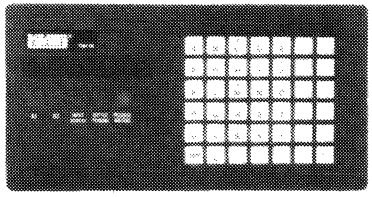


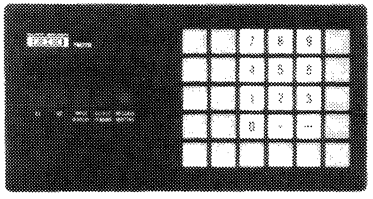
All of the functional features of the TM71 alphanumeric terminal—including the scrollable 16-character alphanumeric LED display—are offered by the TM77. Its operation, protocol and pinouts are identical to the TM71.

TM77, however, offers a simplified keyboard. Larger, more visible key tops—with 0.65" spacing—allow fast, accurate entry of numeric data in work floor environments. Skills and training to operate this terminal are less demanding. Six of TM77's eight function keys (F1 through F6) are shiftable to permit entry of 14 user preprogrammed alphanumeric messages (each up to 80 characters long). Function key messages are transmitted error-free with one keystroke.

TM71B, TM77B Microterminals™

With Integral Bar Code Reader





These models are designed for data collection and tracking operations that require both bar code inputs and limited keyboard entries—plus data display.

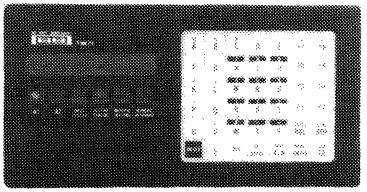
These models add a number of features to those of the TM71 and TM77 that enhance their integral bar code reader feature. Both include an additional four, 50-alphanumeric character bar code buffers.

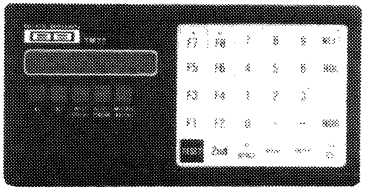
Communications protocol of these models is also expanded to permit full CPU and operator control of the bar code function. RS-232C or RS-422 serial interface options are available. Up to 63 TM71Bs and/or TM77Bs can be polled on a single RS-422 serial interface. In addition to the two TTL-compatible digital outputs of the TM71 and TM77, eight TTL-compatible digital inputs/outputs are offered in the bar code reader models. These units also include a user optional Extended Control mode for more secure data communications. The following bar codes can be read by these units: Code 39, 2 of 5, Interleaved 2 of 5, EAN, and Codabar.

Depth of these terminals is only 35mm (1.35"). The 216mm (8.5") width and 115mm (4.5") height is maintained along with simple mounting on any flat surface.

TM71MS, TM77MS Microterminals™

With Integral Mag Stripe Reader



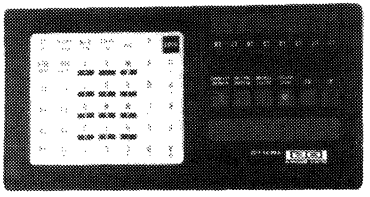


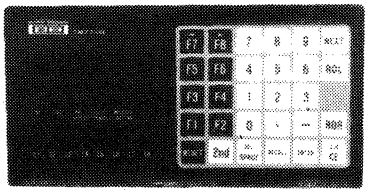
These models have the same outstanding features as the TM71B and TM77B Microterminals™ except that data may be input using the integral Mag Stripe Reader. The data recording specificaiton is ABA Track 2 format which is commonly used on all credit cards using a mag stripe.

Depth of these terminals is only 35mm (1.35"). The 216mm (8.5") width and 115mm (4.5") height is the same as all other Microterminal™ models, with simple mounting on any flat surface.

TM71-I/O, TM77-I/O Microterminals™

Numeric/Alphanumeric With System Input/Output Flexibility





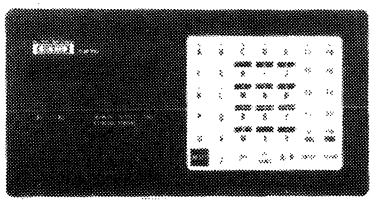
System digital inptus—as well as operator inputs—can be accepted by TM71-I/O and TM77-I/O. These models let you connect your CPU to instruments, weighing stations, switches, counters, magnetic card readers, bar code readers, punched hole readers, printers—wherever human keyboard inputs and display capability must augment the system's input/output. These I/O versions combine an independent TM71 alphanumeric or TM77 numeric data entry/display function with your system's I/O features. The result: flexibility expanded to offer a general purpose data gathering and data distribution station —far more capability than provided by a "conventional" terminal!

I/O versions of the TM71 and TM77 provide an eight-line TTL output port and an eight-line TTL input/output port. These ports are connected through an additional 20-pin I/O connector located on the rear panel. The eight-line output port is integrated with eight additional LED indicators on the front panel. Labelled L1-L8, these indicators let the operator monitor processes as they occur, provide operator sequence instructions, control alarms and report system status.

The eight-line input/output port allows input data to be routed directly through the serial interface to and from the CPU.

TM70 Microterminal™

Low Cost Conversational Mode Alphanumeric



For less demanding applications—and those situations where you want data transmission on keystroke—TM70 offers full 80-character (including A-Z and 0-9) generation from a shiftable 42-key keyboard. A single 36-character buffer accommodates both data input and output. The operator, using keyboard scroll controls, can view the entire buffer on the 12-character LED display. The message display can also be scrolled by the host CPU.

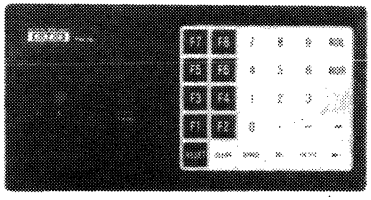
ASCII characters are transmitted (in non-polled mode) as keys are depresssed and, therefore, must be echoed back to the TM70 from the host CPU to be displayed. This step is useful when data entry and transmission accuracy must be verified and also insures operation with many host terminal handlers. In the polled mode, after data is entered by the operator, it is held in the buffer until called for by the host CPU.

TM70's keyboard includes eight programmable keys that offer fast, one-key input to your host CPU. Function key output codes are factory set, but if you prefer, you may program them to provide any sequence of up to four ASCII characters. Custom function key definitions are loaded into TM70 by the host CPU.

A variety of features simplify TM70's human and systems interface compatibiility: ASCII code, RS-232C/V.24 and 20mA communications, 300 and 1200 baud rates, reset and two TTL-compatible digital outputs to control external equipment. The TTL outputs are connected to two front panel LEDs. Three status LEDs indicate OUTPUT PENDING, NUMERIC KEYBOARD (for the numeric key pad and the A/N key) and 2nd (shifted, or upper case) mode. As many as 15 TM70s (and TM71s) can be connected on the same serial interface. A +5VDC supply requirement further simplifies TM70's application. TM70 offers a compatible subset of the TM71 communications protocol, and can, therefore, operate on the same communication line. These models can be interchanged to upgrade or downgrade a station's data entry capability.

TM76 Microterminal™

Low Cost With Alphanumeric Display/Numeric Keyboard



This low cost unit offers the same alphanumeric display capacity, buffer size, function key performance, digital outputs and communications interface as the TM70. It, too, is designed for conversational mode applications where data transmission

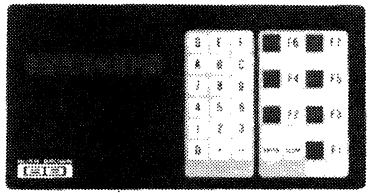
on keystroke is desirable. Like the TM70, TM76 can also operate in polled mode with up to 15 terminals on a single communications line.

Its keyboard is numeric only—with large key tops on 0.65" spacing to improve data entry accuracy in more difficult environments.

TM76 communications protocol is exactly the same as TM70, a subset of TM71 and TM77.

TM25 Microterminal™

Numeric/Hexadecimal

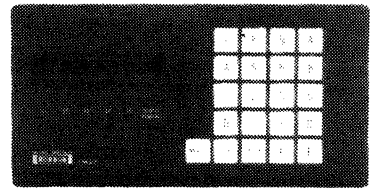


For dedicated applications you can choose 18-key hexadecimal or 12-key numeric keyboard versions of this low cost TM25. An 8-character display shows numbers (0-9) and hex letters (A-F). Seven function keys and seven function indicators are included on the waterproof front panel.

When a function key is depressed, the adjacent function indicator is illuminated. When data is ready to be sent to the host CPU from TM25, the status of the function indicators is encoded as two ASCII characters and transmitted. Conversely, any function indicator on the TM25 panel can be turned on or off on command from the host CPU.

TM27 Microterminal™

High Speed, Polled Numeric/Hexadecimal



This low cost data entry/display terminal is designed for factory data collection and machine control applications. TM27 communicates in serial ASCII with RS-422 conditioning at 300 to 4800 baud. Up to 63 TM27s can be multi-dropped on one CPU communications port. A large, 0.3" high, eight-character seven-segment LED display presents CPU generated data and also allows reviewing and editing data entered before transmission to the CPU. Thirty-nine different symbols can be displayed and two eight-character buffers hold input and output messages. Up to six one-character function messages can be defined by the host CPU and are transmitted to the CPU when the appropriate function key (labeled A through F) is depressed on the keyboard.

Five LED indicators are controlled by the CPU and are driven by TTL-compatible outputs which are also available at the TM27's rear panel connector. These digital outputs can be used to control external equipment. Three TTL-compatible digital inputs can be accepted by TM27. CPU command can lock out the keyboard and initiate remote reset.

DISPLAY

16-Character Alphanumeric LED Display, 80-Character Message Length

Scrolls Through 80-Character Buffer

LED Terminal Status Indicators

Two LED Indicators Independently Controlled by Host CPU

Eight LED Indicators Independently Controlled

CPU Programmable Display Blanking

CPU Programmable, Scroll and Flash

KEYBOARD

Shiftable 42-Key Tactile Feedback Keyboard Generates 80 ASCII Characters

Function Keys Permit Initiating Complex Preprogrammed Actions with a Single Keystroke (user programmable)

Insert or Delete Character

Edit Function Key

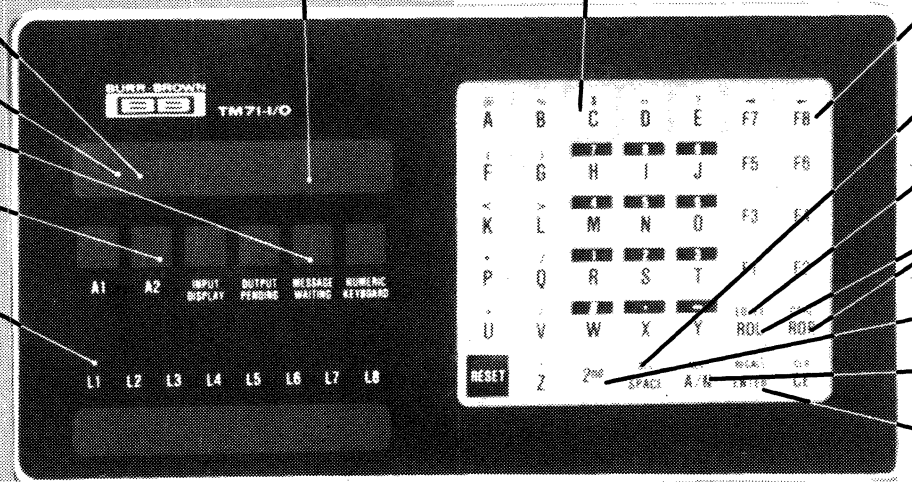
Roll Left and Roll Right Keys Permit Review and Editing of Data

Shift Key

Numeric Pad Selector

Transmit Key

Host CPU Programmable Keyboard Lockout



CONSTRUCTION

- Rugged, Compact, Panel-Mount Case
- Tough, Water and Dust Resistant Front Panel
- Mounts with Four Screws on Any Flat Surface
- 0 to +60°C Operating Temperature Range

SYSTEM INTERFACE

- RS-232-C and 20mA Current Loop or RS-422 Connection on Rear Panel
- Polled: 1 to 15 Terminals on a Single Serial Interface
- Power and Signal Through a Single Connector
- 110 to 19,200 Baud
- Optional EPROM for User-defined Function Keys
- 10 TTL Outputs Controlled by Host CPU
- 8-Line TTL Input/Output Port Controlled by Host CPU

SPECIFICATIONS

Common To All
MICROTERMINAL™ Products

ENVIRONMENTAL
0°C to +60°C*
95% Relative Humidity,
Non-condensing

MECHANICAL DIMENSIONS
Width: 215mm (8.5")
Height: 114mm (4.5")
Thickness: 15mm (0.6"); 35mm (1.35") for TM71B and TM77B;
22mm (0.85") for TM71M

KEYBOARD
Sealed
Tactile feedback

*0°C to +50°C on "B" models.

COMMUNICATIONS PROTOCOL SUMMARY

Host System to MICROTERMINAL™

Input message
Request transmit buffer
Clear all*
Clear input buffer*
Define function message
Delete function message
Delete all function messages
Output to A1
Output to A2
Scroll display
Flash display*
Blank display*
Keyboard lockout
Set turnaround time*
Re-transmit last message
Remote Enter (to test com lines)*
Read Port A, ASCII or Decimal*
Output to Port A, ASCII or Decimal*
Port A input/output continuous ASCII or Decimal*
Halt continuous I/O*
Output to Port B*
Auto/manual wand*
Extend control mode*
Audible alarm control*

MICROTERMINAL™ to Host System

Output message
Output already polled
Port A data*
Acknowledge*
Negative acknowledge*
*Not available on all models

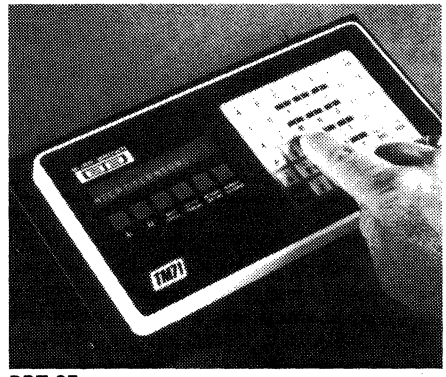
Model TM25 Only

Host System to MICROTERMINAL™

Input message
Clear

MICROTERMINAL™ to Host System

Output message



DPT-05: Powered Desk-Top Stand.

Provides a 15 degree mounting base for all "70" Series Microterminal products except TM71B and TM77B. Provides +5V supply for operation.

DTP-05E designed for 240VAC input supply.

PSX-24: Plug-in transformer provides 24VAC supply for TM71B and TM77B operation. PSX-24E for 240VAC input supply.

ORDERING INFORMATION

TM25-300HT	nonpolled, hex keyboard
TM25-300NT	nonpolled, numeric keyboard
TM27	
TM71M	
TM71	
TM71-I/O	
TM77	complete model number
TM77-I/O	all options included
TM70	
TM76	
TM71B-12	RS-232-C
TM71B-22	RS-422
TM77B-12	RS-232-C
TM77B-22	RS-422
DTP-05 (E)*	Desk-Top Stand and Power Supply
PSX-24 (E)*	Plug-in 24VAC Supply (Bar Code Readers)

*240VAC input supply

Mating Connectors

Communications (and power) connector all models except TM27: DB-25P. Burr-Brown 2525MC connector kit includes a DB-25P. 2525MC not included in basic model above; must be ordered separately if needed.

I/O connector for TM71-I/O and TM77-I/O required in addition to communications connector. I/O connector is 20 pins - two parallel rows of 0.025" (0.64mm) square posts on 0.100" (2.54mm) spacing. BERG 489-005 and 65 489-007 are ribbon cable connectors. Burr-Brown part number 2020MC is a BERG 65 489-007.

TM27 connector: 26-pins, 2 parallel rows of 0.025" (0.64mm) square posts on 0.100" (2.54mm) spacing.

TMC900 . . . a communications processor for . . .

FACTORY FLOOR DATA COLLECTION SYSTEMS

. . . using Microterminals . . .

You can feed up to 128 Microterminals into one host port using—

TMC900

TMC900 — a communications processor — offers an integrated, off-the-shelf data collection system. It controls, collects, and processes data from dozens of Microterminals and provides an economical solution to many problems associated with factory floor data collection systems.

TMC900 interfaces as many as 128 Microterminals to a single communications port in the host computer. In addition, it also performs such essential tasks as terminal polling, local validation, error recovery and basic transaction processing. Definitions of as many as 100 transactions can be down-loaded to the TMC900. Each of these can have up to 10 prompt/reply editing specifications. Unless specific validation by the host is specified, the host will receive only the variable data for the transaction — tagged and time stamped — when the inputs are complete.

TMC900 HARDWARE SPECIFICATIONS

Central Processor

— 8088 microprocessor at 5MHz
— 2 serial I/O ports for asynchronous communication
  • Host Computer RS-232 or RS-422 to 19.2K baud
  • Local Console RS-232 to 19.2K baud
  • TMC-TMC Link for redundant operation
  • High speed, interrupt-driven parallel interface to Peripheral Processors
— 128K bytes of RAM
— 128K bytes of ROM
— Realtime, Multitasking Operating System
— Time of Day Clock
— S.A.S.I. Hard disk interface

Peripheral Processor[s]
(Terminal I/O Processors, max 2 Per System)

—Z80A microprocessor at 3.7MHz
— 2 or 4 Terminal Lines - RS-422 or 20mA current loop
— Up to 16 Microterminals per line
— 8K bytes of RAM
— 16K bytes of ROM
— Realtime, Multitasking Operating System

Front Panel Status Indicators

— Nine diagnostic LEDs
  • Host Port TX, RX
  • Console Port TX, RX
  • Link Port TX, RX
  • Run (CPU)
  • Poll (indicates active polling of Network)
  • Power

Optional Power Supply

— Battery Backup
— 115VAC or 24 VAC
— Integral sealed dry lead-acid batteries
— External Battery (24VDC) Connection
— Provides full system operation
  • 30 minutes nominal
  • 60 minutes maximum on full charge

Disk Storage System (optional)

— 5-1/4" Winchester Type
— 5Mb unformatted storage capacity
— 19" Rack Mount

MICROCOMPUTER I/O SYSTEMS

This full line of μC compatible I/O boards is available off-the-shelf. Design features let you put your microcomputer-based system together fast, using these analog and digital I/O's that offer: simple software requirements; memory-mapped designs; up to 64 input channels per board; analog inputs and outputs on the same board; 9- or 12-bit resolutions; software programmable gains; relay outputs; isolated digital I/O. Plug compatible with Intel, DEC, National, Motorola, Rockwell, Zilog, Synertek, AMC and others.

SELECTION GUIDE

MULTIBUS™ ANALOG I/O

Model	Analog Input	Analog Output	Inputs: High Level	Inputs: Low Level	Analog Resolution (bits)	Number Channels: Input	Number Channels: Output	Features	Price ($) 1-49	Page
MP8304		•	•		12		4	Individual D/A converters	725	14-45
MP8305		•	•		12		4	MP8304 without cable	590	14-45
MP8316-V		•	•		12		16	Low cost per channel	550	14-49
MP8316-I		•			12		16	4 to 20mA inputs	650	14-49
MP8418	•		•	•	12	15 DIF/31 SE		Resistor programmable gain	675	14-51
MP8418-AO	•	•	•	•	12	15 DIF/31 SE	2	Resistor programmable gain	850	14-51
MP8418-PGA	•		•	•	12	15 DIF/31 SE		Software programmable gain	775	14-51
MP8418-PGA-AO	•	•	•	•	12	15 DIF/31 SE	2	Software programmable gain	935	14-51
MP8418-EXP	(1)		(1)	(1)	(1)	48 DIF/96 SE		Analog input expander	495	14-55
MP8418-ISOE	(1)		(1)	(1)	(1)	16 DIF		400V isolation	750	14-57
MP8430	•		•	•	12	16 DIF		Excitation resistor compensation	850	14-58
MP8450	•		•	•	12	16 DIF		1000V transformer isolated	1495	14-60
MP8608	•		•	•	8	8 DIF		Low cost	550	14-69
MP8608-AO	•	•	•	•	8	8 DIF	2	Low cost	695	14-69
MP8616	•		•	•	8	16 SE		Low cost	550	14-69
MP8616-AO	•	•	•	•	8	16 SE	2	Low cost	695	14-69
MP8632	•		•	•	8	32 DIF/64 SE		Low cost	650	14-69
MP8632-AO	•	•	•	•	8	32 DIF/64 SE	2	Low cost	850	14-69

MULTIBUS™ DISCRETE I/O

Model	Digital Input	Digital Output	Number Channels	Isolated	Features	Price ($) 1-49	Page
MP801		•	16	•	Relay output	350	14-8
MP802		•	32	•	Relay output	575	14-8
MP810	•		24	•	Contact closure input	450	14-10
MP810-NS	•		24	•	Voltage input	375	14-10
MP810-LV	•		24	•	Low voltage inputs	375	14-10
MP810-AC	•		24	•	AC sense inputs	475	14-10
MP810-DB	•		24	•	Debounce circuit	460	14-10
MP820-05	•		5	•	Count to 65,536	425	14-12
MP820-15	•		15	•	Count to 65,536	700	14-12
MP821-05	•		5	•	Time measurement	425	14-12
MP821-15	•		15	•	Time measurement	750	14-12
MP830-72	•		72		Output read back	450	14-13

NOTES: (1) Must be used with MP8418, MP8418-AO, MP8418-PGA or MP8418-PGA-AO which govern MP8418-EXP or MP8418-ISOE performance.

MOTOROLA MICROMODULES ANALOG I/O									
			Inputs		Analog	Number Channels			
Model	Analog Input	Analog Output	High Level	Low Level	Resolution (bits)	Input	Output	Features	Page
MP7104		•			12		4	General purpose	14-33
MP7208	•		•	•	12	8 DIF/16 SE		General purpose	14-33
MP7216	•		•	•	12	8 DIF/16 SE		General purpose	14-33
MP7218	•		•	•	12	16 SE		Low cost	14-37
MP7408	•		•	•	8	8 DIF/16 SE		Low cost	14-39
MP7408-NS	•		•	•	8	8 DIF/16 SE		Low cost	14-39
MP7408-AO	•	•	•	•	8	8 DIF/16 SE	2	Low cost	14-39
MP7408-NS-AO	•	•	•	•	8	8 DIF/16 SE	2	Low cost	14-39
MP7432	•		•	•	8	32 DIF/64 SE		Low cost	14-39
MP7432-NS	•		•	•	8	32 DIF/64 SE		Low cost	14-39
MP7432-AO	•	•	•	•	8	32 DIF/64 SE	2	Low cost	14-39
MP7432-NS-AO	•	•	•	•	8	32 DIF/64 SE	2	Low cost	14-39
MP7504		•			8		4	Isolated-fused outputs	14-41
MP7608	•		•	•	12	8 DIF		200VDC protection	14-43
MP7608-1	•		•		12	8 DIF		Fused inputs	14-43

MOTOROLA MICROMODULES DIGITAL I/O						
Model	Digital Input	Digital Output	Number Channels	Isolated	Features	Page
MP701		•	16	•	Reed relays	14-4
MP702		•	32	•	Reed relays	14-4
MP710	•		24	•	Dry contact closures	14-6
MP710-NS	•		24	•	Wet contact closures	14-6

DEC Q-BUS ANALOG I/O									
			Inputs		Analog	Number Channels			
Model	Analog Input	Analog Output	High Level	Low Level	Resolution (bits)	Input	Output	Features	Page
MP1104		•			12		4	Individual D/A converters	14-14
MP1216	•		•	•	12	32 SE		Resistor programmable gain	14-16
MP1216-PGA	•		•	•	12	32 SE		Software programmable gain	14-16

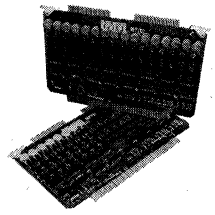
ZILOG MCB ANALOG I/O									
			Inputs		Analog	Number Channels			
Model	Analog Input	Analog Output	High Level	Low Level	Resolution (bits)	Input	Output	Features	Page
MP2216	•		•	•	12	32SE		Resistor programmable gain	14-19
MP2216-A0	•	•	•	•	12	32SE	2	Resistor programmable gain	14-19

STD BUS BOARDS			
Model	Function	Description	Page
MP6102-0	CPU	Z80A single board computer, memory to 8k bytes, 24-bit TTL I/O, RS-232-C port, 2.5MHz.	14-21
MP6102-1	CPU	Z80A single board computer, memory to 8k bytes, 24-bit TTL I/O, RS-232-C port, 4.0MHz.	14-21
MP6202-0	Memory	EPROM/RAM memory board for up to 32k bytes EPROM or 16k bytes RAM supplied with 2716 EPROMS.	14-23
MP6202-1	Memory	EPROM/RAM memory board for up to 32k bytes EPROM or 16k bytes RAM without memory devices.	14-23
MP6202-2	Memory	EPROM/RAM memory board for up to 32k bytes EPROM or 16k bytes RAM supplied with 2016 RAMs.	14-23
MP6303-8	Analog Input	8-channel differential analog input, fixed gain, 12-bit. Requires MP6309 ±15VDC power supply or equivalent.	14-24
MP6303-16	Analog Input	16-channel differential analog input, fixed gain, 12-bit. Requires MP6309 ±15VDC power supply or equivalent.	14-24
MP6303-24	Analog Input	24-channel differential analog input, fixed gain, 12-bit. Requires MP6309 ±15VDC power supply or equivalent.	14-24
MP6303-32	Analog Input	32-channel differential analog input, fixed gain, 12-bit. Requires MP6309 ±15VDC power supply or equivalent.	14-24
MP6304	Parallel I/O	48-channel parallel I/O board.	14-25
MP6305-4	Analog Output	4-channel analog output, ±10V, 8-bit. Requires MP6309 ±15VDC power supply or equivalent.	14-26
MP6305-8	Analog Output	8-channel analog output, ±10V, 8-bit. Requires MP6309 ±15VDC power supply or equivalent.	14-26
MP6309-0	Power Supply	DC/DC power supply, +5VDC input, ±15VDC output at 300mA.	14-27
MP6309-1	Power Supply	DC/DC power supply, +5VDC input, ±15VDC output at 150mA.	14-27
MP6311	IEEE-488	IEEE-488 controller.	14-28
MP6394-0	Parallel I/O	40-channel intelligent parallel I/O board with Z80 CPU, 2k bytes EPROM and 1k byte RAM.	14-30
MP6421	EPROM Programmer	EPROM programmer board for JEDEC EPROMs with optional personality modules.	14-32

VMEbus ANALOG I/O								
	Channels		Inputs					
Model	Inputs	Outputs	High Level	Low Level	Resolution (bits)	Throughput Time (μsec)	Features	Page
MPV901	16DIF/32SE		•	•	12	60	Resistor programmable gain	14-72
MPV901A	16DIF/32SE	2	•	•	12	60	Resistor programmable gain	14-72
MPV901P	16DIF/32SE	2	•	•	12	75	Software programmable gain	14-72
MPV904I[1]		16			12		Current Output	14-79
MPV904V[1]		16			12		Voltage output	14-79
MPV950D[2]	8SE[2]		•		12	3	High speed	14-84
MPV950S[2]	16SE		•		12	3	High speed	14-84

NOTES: (1) Preliminary Data Sheet. (2) The MPV950D has 8 SE channels plus 8 channels which can be configured for differential operation, single ended operation, and current inputs.

BURR-BROWN®



MP701
MP702

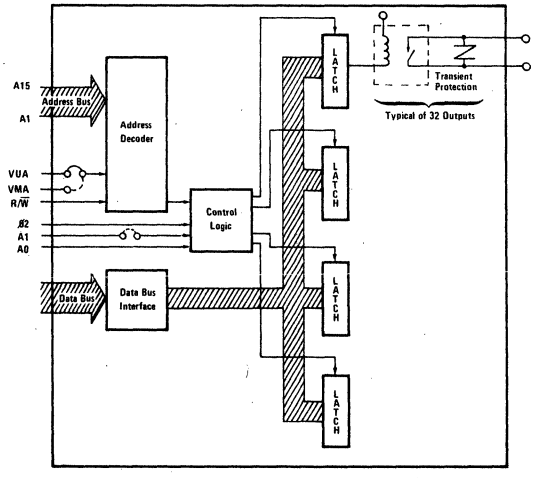
MICROCOMPUTER DIGITAL OUTPUT SYSTEMS

DESCRIPTION

The MP701 and MP702 are digital output microperipheral boards designed to be used with Motorola 6800 microcomputer systems. The microperipheral boards are electrically and mechanically compatible with Motorola's Micromodule and EXORciser development system. The MP701 has 16 digital output channels, and the MP702 has 32 digital output channels. Each digital output channel is implemented with a protected reed relay.

Relays are used to provide low "on-impedance", high output current and output isolation. Each output is isolated from the computer bus up to 600VDC and from channel to channel up to 300VDC. This means that the computer is protected from voltage transients and malfunctions. In addition, since each channel is isolated, the voltage switched by each line is not critical, and ground loops are avoided. The varistors protect each relay contact by suppressing high voltage transients such as those encountered in inductive circuits.

These boards appear as memory locations to the user. Data written on the data bus controls the status of each output. A "1" will close an output, a "0" will open an output. Any memory write command may be used. Each write command controls the status of eight channels. Address bits A0 and A1 on the MP702 and A0 on the MP701 select which set of eight outputs are controlled. The remainder of the address lines are used to select the board itself. Because the address block occupied by each board is user selectable, it can be placed anywhere in memory.



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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated supplies unless otherwise noted.

NUMBER OF CHANNELS	
MP701	16
MP702	32
DIGITAL OUTPUT	
Watts DC (resistive load) max	10W
Amps (resistive load) max	0.5A
Voltage (resistive load) max	28V, rms
Life (resistive load) min	10^6 operations
Initial contact resistance max	0.2Ω
Actuate Time	250μsec
De-Actuate Time	250μsec
Bounce Time	150μsec
TRANSIENT PROTECTION	
Continuous Power Rating	250mW
Discharge Capacity	30 watt-seconds
COMPUTER BUS	
All signals compatible with Motorola EXORciser and Micromodules system	
Logic Loading	1LSTTL
Output Coding	0 Open Contact 1 Close Contact
POWER REQUIREMENTS	
Voltage	5VDC, ±5% V
Supply Drain max, MP701	0.4A
Supply Drain max, MP702	0.7A
ISOLATION VOLTAGE	
Between Microcomputer Bus and Outputs	600VDC
Between Outputs	300VDC
OPERATING TEMPERATURE	0°C to +70°C
STORAGE TEMPERATURE	-55°C to +125°C

MECHANICAL

Compatible with Micromodules and EXORciser® card spacing.

Minimum card spacing: 12.7mm (0.5″).

Microcomputer bus connector required: 86-pin PC edge connector with 0.156″ contact centers (SAE-43D/1-2).

50-pin output edge connector on board.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). A Scotchflex connector is available from 3M: 3415-0001.

OPERATING INSTRUCTIONS

PROGRAMMING

Each digital output channel appears as one bit of memory to the microcomputer. The channels are selected in groups of eight by A0 on the MP701 and by A1-A0 on the MP702. Writing a 1 to an output channel closes the output contact; writing a 0 to an output channel opens the output contact. Once an output is defined, it will remain in that state until redefined by another write to that byte. For example, to open channels 0, 2, 6, and close channels 1, 3, 4, 5, 7 with an MP702 as shipped from the factory execute:

```
LDA #$BA
STA $91FC
```

where BA (1011 1010) is the data written to the board and 91FC is the address of channels 0-7. Refer to Table I for a description of which data and address lines control which output channels.

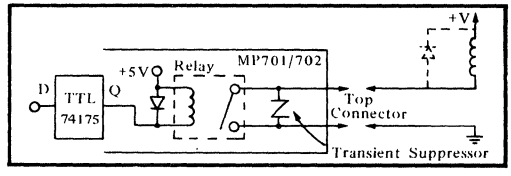
TABLE I. Data - Address - Channel Relationship.
0 = open, 1 = close.

Data Bus	ADDRESS LINES (A1, A0)			
	00	01	10	11
$\overline{D7}$	7	15	23	31
$\overline{D6}$	6	14	22	30
$\overline{D5}$	5	13	21	29
$\overline{D4}$	4	12	20	28
$\overline{D3}$	3	11	19	27
$\overline{D2}$	2	10	18	26
$\overline{D1}$	1	9	17	25
$\overline{D0}$	0	8	16	24
	Channel Number			

The MP701 and MP702 are passive during a read to their memory locations. Therefore, other memory or I/O devices may be placed at the same address without interfering with the microperipheral's activities.

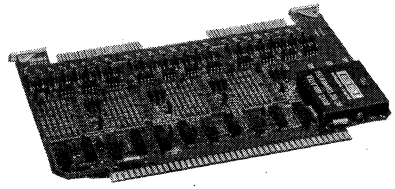
DIGITAL OUTPUT CHANNEL

Each output is capable of switching an inductive load. Transient suppressors are used across each output switch to protect the output relay from damage due to surges when the contact is opened. A typical output circuit and the load circuit that it might drive are shown in the figure below.



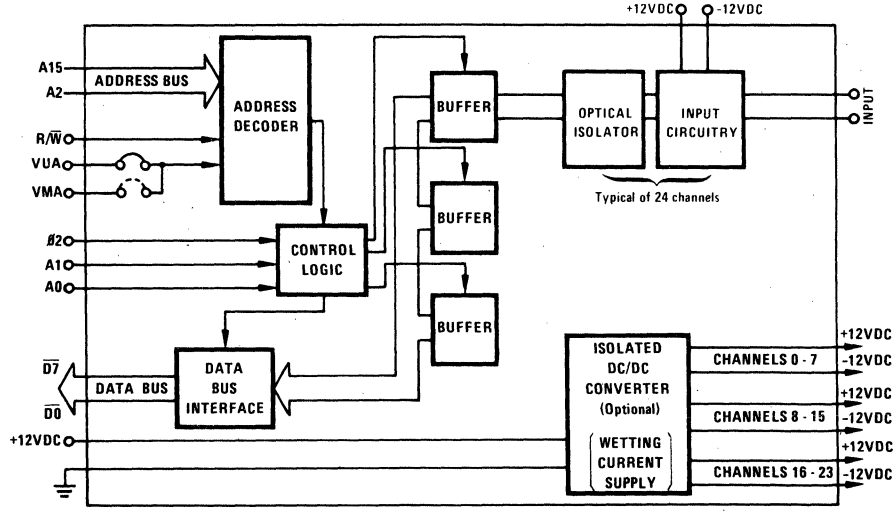
BURR-BROWN®

MP710



MICROCOMPUTER DIGITAL INPUT SYSTEM

A 24-CHANNEL ISOLATED DIGITAL INPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE/EXORciser® AND ROCKWELL SYSTEM 65



FEATURES

- ISOLATED FROM COMPUTER BUS AND CHANNEL TO CHANNEL
- CONTACT CLOSURE OR VOLTAGE INPUTS
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Easy to program
  - Operates from computer power supply
- 70°C BURN-IN

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DESCRIPTION

This microperipheral board provides 24 digital input channels that interface electrically and mechanically with Motorola Micromodule® and EXORciser® microcomputers. It is contained on a single printed circuit board that operates from the computer's +5VDC power supply. Digital inputs enter through a card edge connector located opposite the bus connector.

The MP710 operates with dry relay contacts - MP710-NS operates with voltage inputs (wet relay contacts). The MP710 may be modified by jumper selection to operate with voltage or contact closure inputs, or a mixture of both. Inputs are arranged in groups of eight. Each group is isolated from other groups and from the computer bus up to 600VDC. Isolation between inputs is 300VDC (MP710-NS). Isolation protects the computer from voltage transients and malfunctions. In addition, since each input is isolated, the voltage switched by each line is not critical and ground loops are avoided.

MP710's are programmed as memory locations. Each input is one memory bit and any read command may be used. When the board is read, logic 0 represents an open contact (low voltage); logic 1, a closed contact (high voltage). Each read command inputs the status of eight channels. Address bits A0 and A1 select the set of inputs to be read. The remainder of the address lines are used to select the board itself. The address block occupied by each board is selectable and can be located anywhere in memory.

®Motorola

INSTALLATION

These units are shipped from the factory ready for immediate use. Installation requires only plugging the card into any empty slot in the computer and wiring the input connector.

MECHANICAL

Compatible with Micromodule and EXORciser card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Two 50-in output edge connectors on board.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25 1JN5, solder tab). A Scotchflex connector is available from 3M: 3415-0001.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated supplies unless otherwise noted.

INPUT CHARACTERISTICS	
Number of Channels	24
Input Impedance	15kΩ
Input Delay Times	
Open to closed	25μsec, max
Closed to open	100μsec, max
VOLTAGE SENSE	
MP710-NS	
Minimum voltage to detect a logic 1	17V
Maximum voltage to detect a logic 0	4V
CONTACT CLOSURE SENSE	
R_{CLOSED}	
MP710 (on-board ±12V supply)	6kΩ, max
MP710-NS	
at 24V across contacts	6kΩ, max
at 48V across contacts	30kΩ, max
at 60V across contacts	42kΩ, max
R_{OPEN}	
MP710 (on-board ±12V supply)	80kΩ, min
MP710-NS	
at 24V across contacts	80kΩ, min
at 48V across contacts	175kΩ, min
at 60V across contacts	235kΩ, min
Maximum voltage (V_S) across input without damage	
MP710	120VAC, rms, max 60VDC, max
MP710-NS	168VAC, rms, max 84VDC, max
ISOLATION VOLTAGE	
Between microcomputer bus and inputs	600VDC
Between inputs (MP710-NS only)	300VDC
Between groups of 8 inputs	600VDC
POWER REQUIREMENTS	
MP710	+5VDC ±5% at 400mA +12VDC ±5% at 100mA
MP710-NS	+5VDC ±5% at 400mA
COMPUTER BUS	
All signals compatible with Motorola Micromodule and EXORciser systems	
Logic loading	1LSTTL Load
Input coding	Logic 0: open contact Logic 1: closed contact
TEMPERATURE RANGE	
Operating	0°C to +70°C
Storage	-55°C to +125°C

DEFINITION OF SPECIFICATIONS

INPUT DELAY TIME

OPEN TO CLOSED - The delay required to detect an input contact closure switching from open to closed.

CLOSED TO OPEN - The delay required to detect an input contact closure switching from closed to open.

CONTACT CLOSURE IMPEDANCES

R_{CLOSED} - The impedance of an input contact closure when closed. R_{CLOSED} specifications are the maximum impedance allowed to reliably detect a closure.

R_{OPEN} - The impedance of an input contact closure when open. R_{OPEN} specification is the lowest impedance allowed to reliably detect an open contact.

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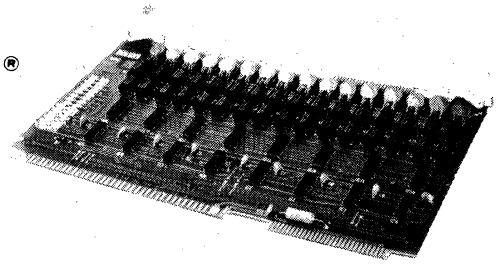
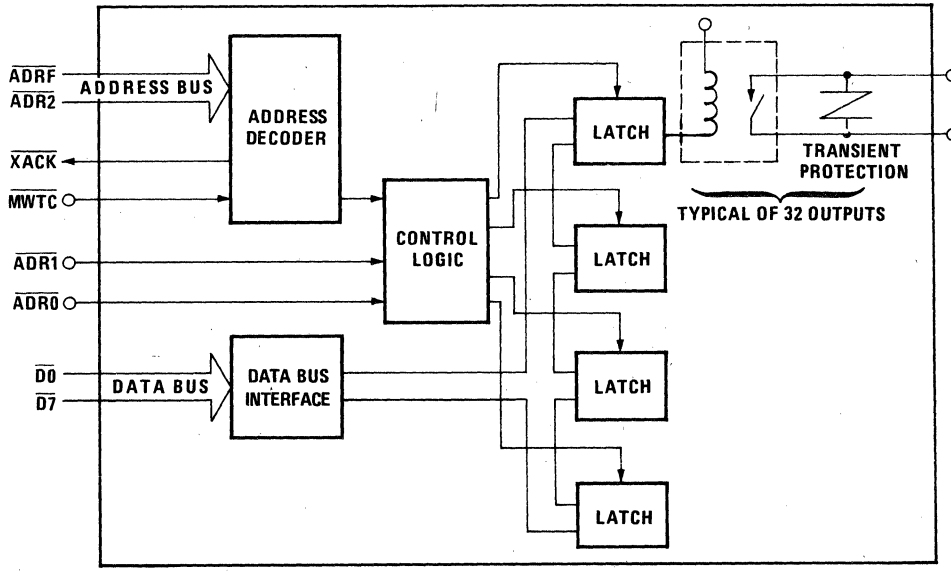


MP801
MP802

MICROCOMPUTER DIGITAL OUTPUT SYSTEMS

A 16- OR 32-CHANNEL RELAY OUTPUT SYSTEM COMPATIBLE WITH INTEL SBC80 AND INTELLEC MDS MICROCOMPUTERS



FEATURES

- ISOLATED FROM COMPUTER BUS AND CHANNEL TO CHANNEL
- TRANSIENT PROTECTION
- EASY TO PROGRAM AND USE
- MEMORY-MAPPED
- BURNED-IN

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DESCRIPTION

The MP801 and MP802 are digital output (contact closure) microperipheral boards that are electrically and mechanically compatible with Intel's SBC80 and Intellec MDS microcomputer systems. The MP801 offers 16 digital output channels and the MP802, 32 digital output channels.

Each channel is implemented by a protected reed relay and can handle up to 10 watts. Relays provide low "on-impedance" and high output current and isolate output channels from the computer bus and from channel to channel. Isolation insures that ground loop problems are avoided. The computer is protected from component failures caused by voltage transients and malfunctions occurring in the outside world.

MP801 and MP802 appear as memory locations and data written on the data bus controls the status of each output. A logic 1 will close an output. A logic 0 will open an output. Any memory write instruction may be used.

SPECIFICATIONS

Typical at +25°C and rated supplies unless otherwise noted

ELECTRICAL

NUMBER OF CHANNELS	
MP801	16
MP802	32
DIGITAL OUTPUT	
Watts DC (resistive load) max	10 watts
Amps (resistive load) max	0.5 amps
Voltage (resistive load) max	28 Vrms
Life (resistive load) min	10^6 operations
Initial contact resistance max	0.3 ohms
Actuate Time	1msec
De-Actuate time	250μsec
Bounce time	150μsec
TRANSIENT PROTECTION	
Continuous power rating	250mW
Discharge capacity	30 watt-seconds
Leakage current through transient suppressor at 28V	5mA
COMPUTER BUS	
All signals compatible with Intel SBC 80 and MDS Systems	
Logic Loading	1 LSTTL
Output Coding	0 Open Contact 1 Close Contact
POWER REQUIREMENTS	
Voltage	5VDC, ±5%
Supply Drain max, MP801	0.3 amp
Supply Drain max, MP802	0.5 amp
ISOLATION VOLTAGE	
Between microcomputer bus and outputs	600VDC
Between outputs	300VDC
OPERATING TEMPERATURE	0 to +70°C

TABLE I. Electrical Specifications

MECHANICAL

Compatible with SBC 80 and Intellec MDS card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Two 50 pin output edge connectors on board. One is used for MP801, both are used for MP802.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). A Scotchflex connector is available from 3M: 3415-0001.

OPERATING INSTRUCTIONS

PROGRAMMING

Each digital output channel appears as one bit of memory to the microcomputer. The channels are selected in groups of eight by $\overline{ADR0}$ on the MP801 and by $\overline{ADR1}$-$\overline{ADR0}$ on the MP802. The remainder of the address lines are used to select the board itself. Because the address block occupied by each board is user selectable, it can be placed anywhere in memory. Writing a logic 1 to an output channel closes the output contact; writing a logic 0 to an output channel opens the output contact. Once an output is defined, it will remain in that state until redefined by another write to that byte. For example, to open channels 0, 2, 6, and close channels 1, 3, 4, 5, 7 with an MP802 as shipped from the factory execute:

```
MVI   A, BAH
STA   F700H
```

where BA (1011 1010) is the data written to the board and F700 is the address of channels 0-7. Refer to Table II for a description of which data and address lines control which output channels.

Data Bus	ADDRESS LINES (A1, A0)			
	00	01	10	11
$\overline{D7}$	7	15	23	31
$\overline{D6}$	6	14	22	30
$\overline{D5}$	5	13	21	29
$\overline{D4}$	4	12	20	28
$\overline{D3}$	3	11	19	27
$\overline{D2}$	2	10	18	26
$\overline{D1}$	1	9	17	25
$\overline{D0}$	0	8	16	24

TABLE II. Data - Address - Channel Relationship. Logic 0 = open, Logic 1 = close.

The MP801 and MP802 are passive during a read to their memory locations. Therefore, other memory or I/O devices may be placed at the same address without interfering with the microperipheral's activities.

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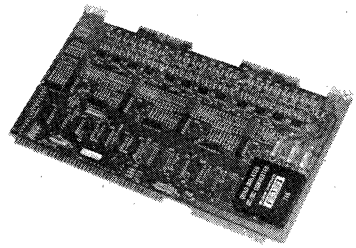
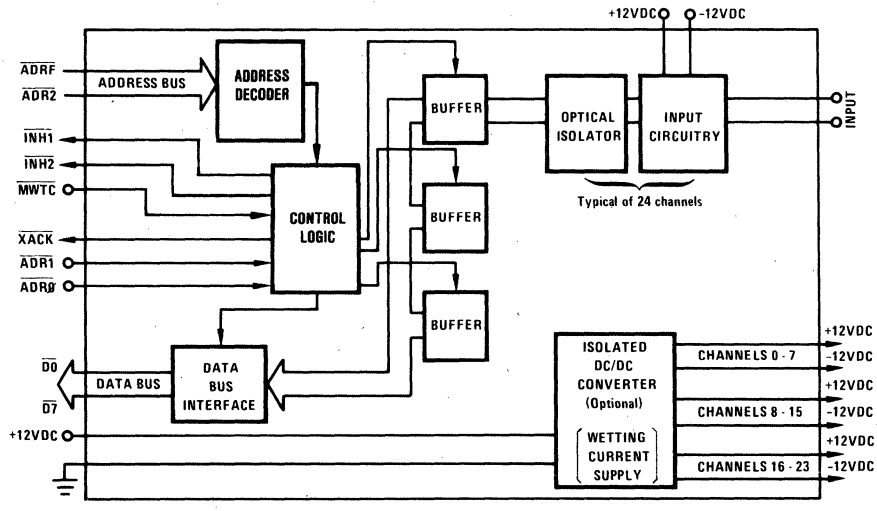


MP810
MP810-DB
MP810-NS
MP810-LV
MP810-AC

MICROCOMPUTER DIGITAL INPUT SYSTEM

A 24-CHANNEL ISOLATED DIGITAL INPUT SYSTEM COMPATIBLE WITH IEEE-796 (MULTIBUS™)



Multibus™ - Intel Corp.

FEATURES

- ISOLATION - FIELD TO COMPUTER
- ISOLATION - CHANNEL TO CHANNEL
- CONTACT CLOSURE
- CONTACT WETTING CURRENT
- VOLTAGE INPUTS DC/AC
- DEBOUNCE
- TTL-COMPATIBLE INPUTS
- 20-BIT ADDRESSABLE
- +70°C BURN-IN

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DESCRIPTION

The MP810 series provides 24 optically-isolated discrete inputs for Multibus (IEEE-796) based microcomputer systems. Input signal types include 1) dry contact closures, 2) wetted contact closures, 3) DC voltages, and 4) AC voltages. Isolation protects the computer from input voltage transients and malfunctions of field inputs. In addition, channel-to-channel isolation minimizes channel interaction and avoids ground loop problems.

Full hardware integration allows cards to be inserted directly into the system back panel. Power for the card is provided by the system bus; therefore, no external power supplies are required.

The MP810 is memory-mapped. Data is acquired through any memory read operation. Each input is 1 bit of an 8-bit word. An open contact (low voltage) is represented by a logic 0 and a closed contact (high voltage) is represented by logic 1.

Contact debounce is available on some models. This prevents erroneous data that could be caused by relay contact bounce. The hardware approach unburdens the processor and reduces system overhead normally required to debounce contact closures.

SPECIFICATIONS

Electrical

Typical at +25° C and rated supplies unless otherwise noted.

MODEL	MP810	MP810-DB	MP810-NS	MP810-LV	MP810-AC	UNITS
INPUT CHARACTERISTICS						
Number of Inputs	24	24	24	24	24	
Input Resistor	15K, 1/2W	15K, 1/2W	15K, 1/2W	1.5K, 1/2W	56K, 1/2W	Ω
Delay Times						
Open-to-Closed(1)	0.025	65(3)	0.025	0.025	1(3)	msec
Closed-to-Open(2)	0.100	65(3)	0.100	0.100	80(3)	msec
VOLTAGE SENSE						
Logic 0	Open(4)	Open(4)	4VDC	2VDC	10V rms(6)	V, max
Logic 1	Closed(4)	Closed(4)	17VDC	3.5VDC	48V rms(6)	V, min
MAXIMUM VOLTAGE (V_S) ACROSS INPUT WITHOUT DAMAGE						
VDC, max	60	60	84	20	120	VDC
VAC, max	120	120	168	40	250	VAC, rms
VOLTAGE SOURCE (contact wetting)	±12V	±12V	None	None	None	
ISOLATION VOLTAGE						
System-to-Field	600	600	600	600	600	VDC
Channel-to-Channel	(7)	(7)	300	300	300	VDC
Input Blocks(5)	600	600	600	600	600	VDC
POWER REQUIREMENTS	+5/+12	+5/+12	+5	+5	+5	VDC
	400/100	400/100	400	400	400	mA
BUS INTERFACE	Meets electrical and mechanical specifications of IEEE-796 (Multibus)					
ENVIRONMENT						
Operating Temperature	0 - +70° C					
Storage Temperature	-55° C to +125° C					
Relative Humidity	95% noncondensing					

NOTES:
1. OPEN-TO-CLOSED: The delay required to detect an input contact closure switching from open-to-closed.
2. CLOSED-TO-OPEN: The delay required to detect an input contact closure switching from closed-to-open.
3. Contact debounce time.
4. Contact state.
5. The on-board DC-to-DC converter provides three isolated voltages. Each voltage services one block of eight input channels.
6. This is for a 60Hz signal.
7. Common power supplies used for contact wetting degrades channel-to-channel isolation.

MECHANICAL SPECIFICATIONS

Compatible with IEEE-796 (Multibus) specifications
Minimum card spacing: 0.6" (15.2mm)
Board Thickness: 0.062" (1.57mm)
Bus connector: P1: 43/86 pin on 0.156" (3.9mm) centers
P2: auxiliary: 30/60 pin on 0.10" (2.5mm) centers
I/O connectors: P3/P4: 25/50 pin on 0.10" (2.5mm) centers

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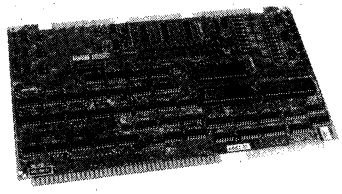


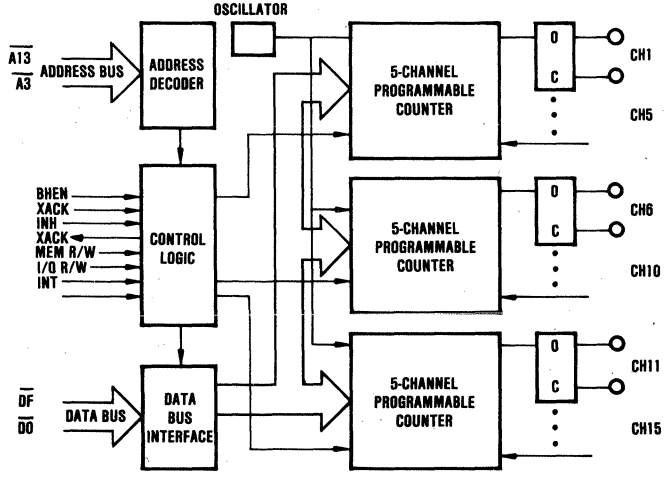
MP820-05
MP820-15
MP821-05
MP821-15

MICROCOMPUTER DIGITAL INPUT SYSTEM

5- or 15-Channel Isolated Pulse Counter/Measurement System Compatible with IEEE-796 (Multibus™)

FEATURES

- 5 OR 15 CHANNELS
- 16-BIT COUNTER
- SINGLE OR DOUBLE PRECISION
- REGISTER TRANSFER
- MEMORY OR I/O MAPPED
- OPTICALLY-ISOLATED INPUTS
- DEBOUNCE
- FREQUENCY (MP821 ONLY)
- PULSE DURATION (MP821 ONLY)
- MULTIBUS™ COMPATIBLE
- 20-BIT ADDRESS BUS
- 16-BIT DATA BUS
- BURNED-IN



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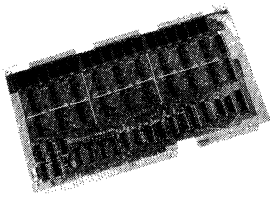


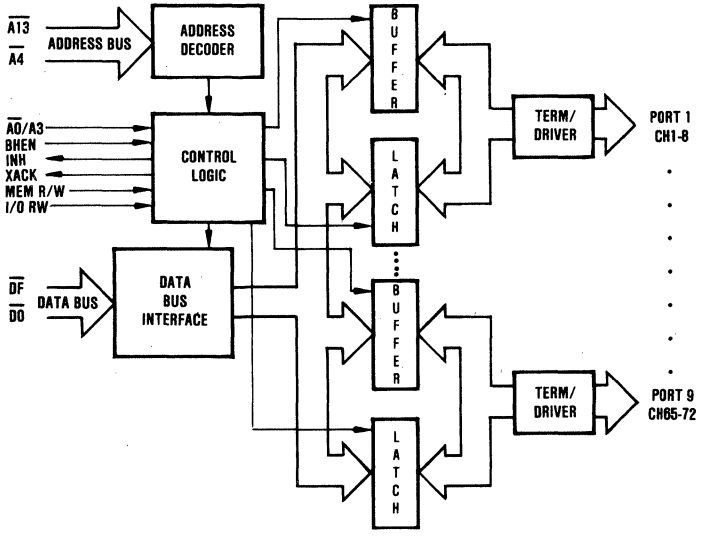
MP830-72

MICROCOMPUTER TTL INPUT/OUTPUT SYSTEM

72-Channel TTL Input/Output Systems Compatible with IEEE-796 (Multibus™)

FEATURES

- 72 CHANNELS
- IN/OUT BLOCKS OF 8
- SOCKETED I/O TERMINATIONS
- OUTPUT READ BACK
- LATCHED OUTPUTS
- NO POWER-UP GLITCH
- MEMORY (I/O) MAPPED
- MULTIBUS™ COMPATIBLE
- BURNED-IN



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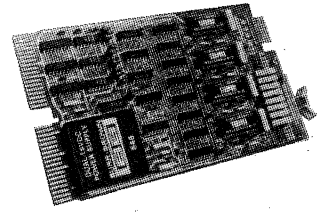


MP1104

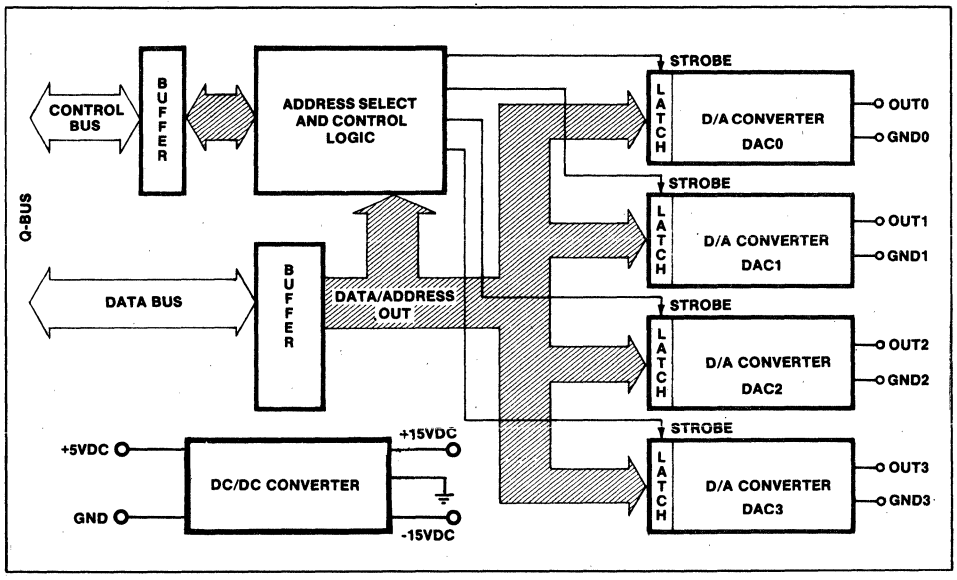
MICROCOMPUTER ANALOG OUTPUT SYSTEM

A 4-CHANNEL ANALOG OUTPUT SYSTEM COMPATIBLE WITH DIGITAL EQUIPMENT CORP. LSI-11, LSI-11/2, LSI-11/23, PDP-11/03, AND PDP-11/23 MICROCOMPUTERS

DESCRIPTION

The MP1104 analog output peripheral is electrically and mechanically compatible with and interfaces directly to DEC's Q bus.

The MP1104 consists of four 12-bit D/A converters with address decoding and control logic. It also includes a DC/DC converter for operation from the computer's 5VDC supply. The MP1104 is burned-in before shipment.



MP1104 BLOCK DIAGRAM

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SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG OUTPUT	MP1104
OUTPUT CHARACTERISTICS	
Number of Channels	4
Output Voltage Ranges (Jumper Selectable)(1)	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA
Output Impedance	0.01Ω
Short Circuit Protection	Yes
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Output Settling Time, max(2)	10μsec
ACCURACY	
Output Accuracy, max(3)	±0.025% FSR(4)
Temperature Coefficient of Accuracy Drift(5)	±30ppm of FSR/°C
POWER REQUIREMENTS	
MP1104	+5V ±5% at 1.25A
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Relative Humidity	95% of noncondensing

NOTES:
1. Factory set for ±10V range.
2. Settling to ±0.01% of FSR for a full scale change.
3. Includes linearity errors with gain and offset errors adjusted to zero.
4. FSR means Full Scale Range.
5. Includes offset drift, gain drift and linearity drift.

MECHANICAL

Compatible with DEC LSI-11, LSI-11/2, LSI-11/23, PDP-11/03, and PDP-11/23 card spacing.

Minimum card spacing: 12.7mm (0.5").

Analog Output Connector: one 20-pin PC edge connector on top edge of board.

Analog Output Mating Connector:

Mating connector available from Burr-Brown: 2220MC (Viking #3VH10/1JN5, solder tab)

A flat cable connector is available from Berg: 65764-001

OPERATING INSTRUCTIONS

INSTALLATION

MP1104 is shipped from the factory calibrated and ready to use. Installation consists of plugging the card into any empty slot in the computer and wiring the analog connector.

PROGRAMMING

The MP1104 is programmed as memory locations and any memory write instruction can be used. The D/A converter input occupies the 12 least significant bits of a word. The address block occupied by the MP1104 is user-selectable and can be placed anywhere in the upper 4k of memory.

MP1104's are jumpered at the factory with a base address of 170440 (channel 0). Channel one is at location 170442, channel two is at location 170444, and channel three is at location 170446 (see Table I).

TABLE I. D/A Converter Data Assignments.

WRITE DATA															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

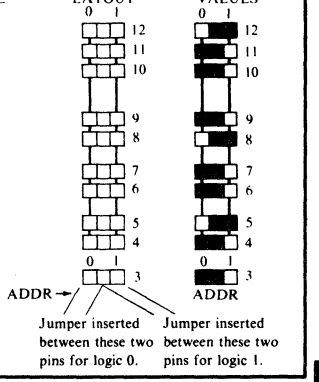
MEMORY MAP	
Channel 0	Base Address
Channel 1	Base Address +2
Channel 2	Base Address +4
Channel 3	Base Address +6

ADDRESS MODIFICATION

The base address of a board can be set to any 4-word boundry by properly jumpering (with push-on sockets) its address selector. The base address set at the factory is 170440. To change the sense of a bit simply remove the present jumper and insert the jumper for that bit (see Tables II and III).

TABLE II. Base Address Jumpers.

ADDRESS LINES	FACTORY SET VALUE	JUMPER MATRIX LAYOUT	FACTORY SET VALUES
A12	1		
A11	0		
A10	0		
A9	0		
A8	1		
A7	0		
A6	0		
A5	1		
A4	0		
A3	0		



ANALOG OUTPUT RANGE SELECTION

Each D/A converter is wire wrap jumpered at the factory for ±10V operation with two's complement coding. It is possible, however, to alter jumpers on the board for other output voltages and coding. When making a change, just remove those jumpers indicated for the present range and replace them with the jumpers required for the desired range.

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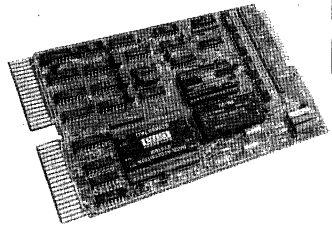


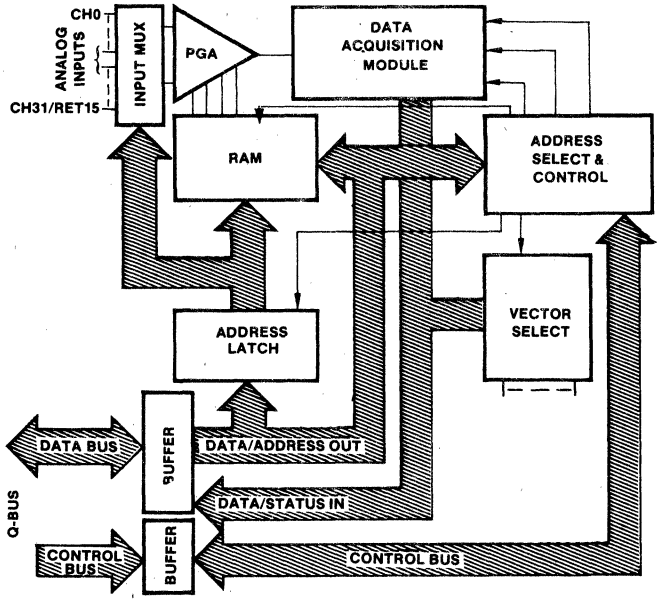
MP1216
MP1216-PGA

MICROCOMPUTER ANALOG INPUT SYSTEMS

A 32-CHANNEL ANALOG INPUT SYSTEM COMPATIBLE WITH DIGITAL EQUIPMENT CORPORATION LSI-11, LSI-11/2, LSI-11/23, PDP-11/03 AND PDP-11/23 MICROCOMPUTERS

FEATURES:

- HIGH AND LOW LEVEL INPUTS
- SOFTWARE PROGRAMMABLE GAIN (1 to 1024) AMPLIFIER OPTION
- EASILY PROGRAMMED
- BURN-IN



DESCRIPTION

The MP1216 analog input peripherals are electrically and mechanically compatible with and interface directly to DEC's LSI-11/2 family. The boards use one dual-wide card slot.

The MP1216 includes: over-voltage protection to 26VDC; an analog multiplexer; resistor programmed instrumentation amplifier (MP1216), or a software programmable amplifier with gains of 1 to 1024 (MP1216-PGA); sample/hold amplifier and; a 12-bit A/D converter.

These units are 16-channel differential (user strapable as 32-channel single-ended) analog input systems.

Gains of 1 to 1024 are software selectable for the programmable amplifier version (MP1216-PGA), and the gain for each channel is stored in an on-board RAM. The proper gain for each channel is then selected automatically by the MP1216-PGA.

The MP1216-PGA is particularly recommended for low-level inputs.

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SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG INPUT SECTION	MP1216/MP1216-PGA
INPUT CHARACTERISTICS	
Number of Channels	32 single-ended or 16 differential
ADC Gain Ranges (jumper selectable)(1)	±10V, 0-10V
Amplifier Gain Ranges	
Resistor Programmable(2) (MP1216)	1 to 1000
Software Programmable (MP1216-PGA)	1 to 1024
Maximum Input Voltage without Damage(3)	±26V
Input Impedance	100MΩ, 10pF OFF Channel 100MΩ, 100pF ON Channel
Bias Current	
Resistor Programmable	±20nA
Software Programmable	±15nA
Amplifier Input Offset Voltage	
Resistor Programmable	±400μV
Software Programmable	±40μV
Amplifier Input Offset Voltage Drift	
Resistor Programmable	±2μV/°C
Software Programmable	±0.5μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Conversion Time, max G = 1	
Resistor Programmable(4)	40μsec
Software Programmable	375μsec
Conversion Time, max G = 1024	
Resistor Programmable	100μsec
Software Programmable	375μsec
ACCURACY	
System Accuracy at +25°C, max(5) G = 1	±0.025% FSR(6)
System Accuracy at +25°C, max G = 1024	
Resistor Programmable	±0.1% FSR
Software Programmable	±0.05% FSR
System Output Noise G = 1, rms	
Resistor Programmable	1mV
Software Programmable	1mV
System Output Noise G = 1024, rms	
Resistor Programmable	15mV
Software Programmable	2mV
Linearity	±1/2LSB
Differential Linearity	±1/2LSB
Quantizing Error	±1/2LSB
Gain Error	Adjustable to zero(7)
Offset Error	Adjustable to zero
Monotonicity(8)	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE (Bipolar)(9)	
System Accuracy Drift, max G = 1	±45ppm of FSR/°C
System Accuracy Drift, max G = 1024	
Resistor Programmable	±200ppm of FSR/°C
Software Programmable	±100ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time	125nsec
Aperture Time Uncertainty	±5nsec
Differential Amplifier CMRR G = 1	74dB (DC to 1kHz)
Channel Crosstalk	80dB down at 1kHz, for OFF Channel to ON Channel
POWER REQUIREMENTS	
MP1216/MP1216-PGA	+5V ±5% at 1.0A
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Relative Humidity	95% noncondensing

NOTES:
1. Factory set for ±10V range.
2. Factory set for Gain = 1.
3. With power off (±36 volts with power on).
4. With delay inhibited, 22μsec.
5. Includes linearity errors with gain and offset errors adjusted to zero.
6. FSR means Full Scale Range.
7. When any one gain range is adjusted to zero gain error, the gain error for any other range is less than ±0.02% when using the software programmable amplifier.
8. No missing codes guaranteed.
9. Includes offset drift, gain drift, and linearity drift.

MECHANICAL

Compatible with LSI-11, LSI-11/2, LSI-11/23, PDP-11/03 and PDP-11/23 card spacing.

Minimum card spacing: 12.7mm (0.5").

Analog Input Connector: One 40-pin analog edge connector on board for analog inputs.

Analog Input Mating Connector:
Mating connector available from Burr-Brown: 2240MC (Viking #3VH20/1JN5 solder tab); a flat cable connector is available from Berg: 65764-007.

OPERATING INSTRUCTIONS

INSTALLATION

MP1216 is shipped from the factory calibrated and ready to use. Installation consists of plugging the card into any empty slot in the computer and wiring the analog connector. See Figure 1 for the block diagram.

PROGRAMMING

This peripheral is programmed as memory locations; any memory reference instruction can be used. Two 16-bit memory locations are used. One for the Read/Write data register; the other for the Control Status register (see Figure 2). The addresses occupied by each MP1216 are user selectable and can be placed anywhere in the upper 4K of memory.

On MP1216-PGA's (with software programmable gain amplifiers) an on-board random access memory (RAM) is used to store the gain for each channel.

When the Gain Control bit (D8) of the Write Data Register is a logic 1, the data contained in bits D9-D12 of the same register are written to the on-board RAM to control the gain for the channel also written in the same word (bits D0-D4). On subsequent operations if the Gain Control bit is a logic 0, the programmable gain amplifier will use the gain already stored in on-board RAM for that channel.

These boards are factory set with Data Register at location 170402 and the Status/Control Register at location 170400.

A conversion is started by writing the channel number to bits D0-D4 of the data register. This write operation selects the proper analog multiplexer channel and starts a delay one-shot which allows time for the multiplexer, instrument amplifier and sample/hold amplifier to settle to the new channel's value. At the end of the delay time, the sample/hold amplifier is switched to the hold mode and the A/D converter starts its conversion.

When the conversion is complete, the board can be operated in one of two modes:

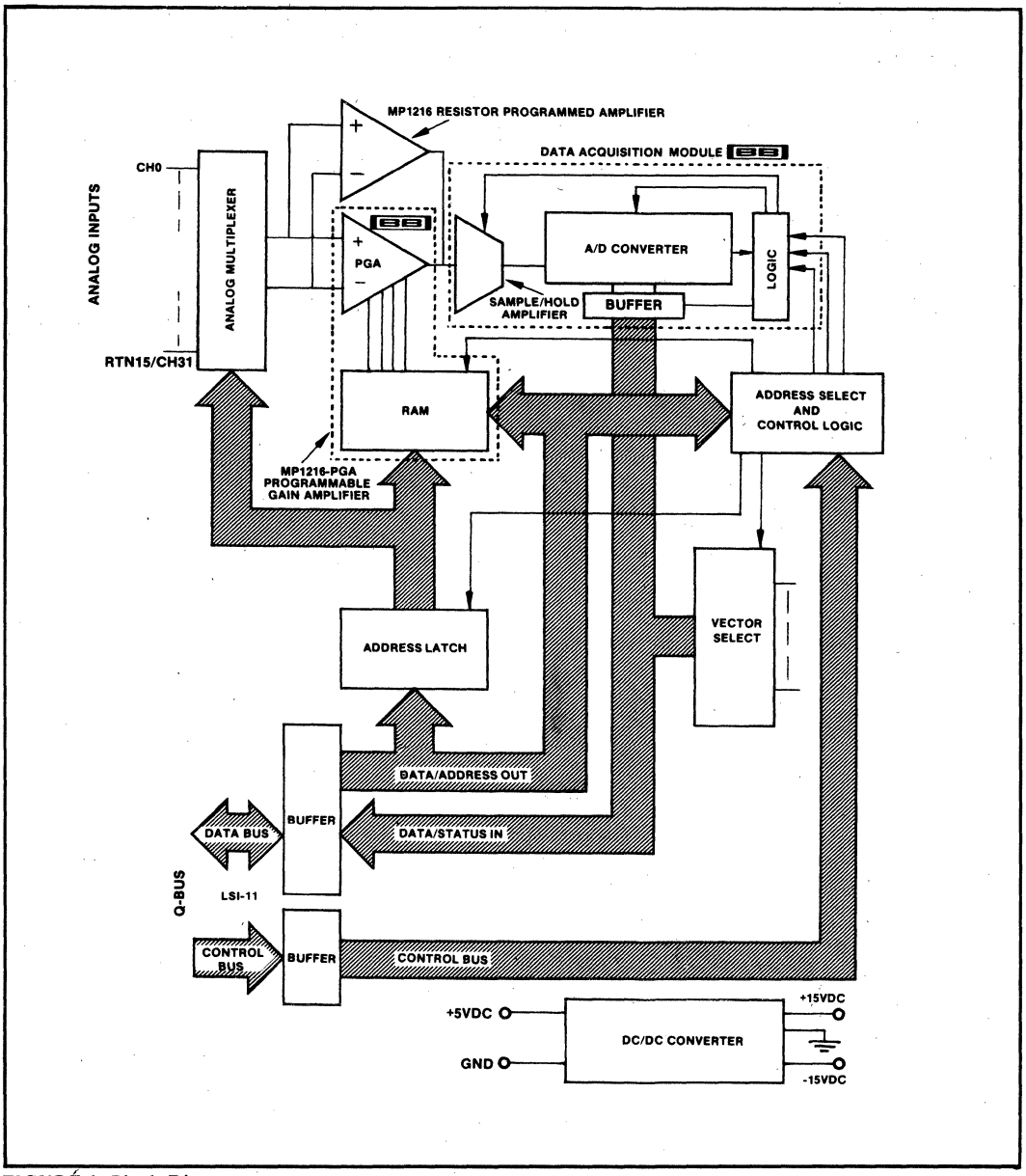

FIGURE 1. Block Diagram.

Interrupt Mode

In the Interrupt Mode, when the conversion is complete, the MP1216 asserts the bus interrupt request line (BIRO). When the LSI-11 responds with a bus interrupt acknowledgement (BIAKI), the MP1216 asserts the bus reply line (BRPY) and gates an interrupt "vector" onto the bus. The vector address is selected by jumpers on the board. The Interrupt Mode is enabled by writing a logic 1 to bit D6 of the Control Register.

Polling Mode

In the Polling Mode, the CPU must periodically scan bit D7 of the STATUS Register to determine if the conversion is complete. A logic 1 indicates that conversion is complete. A read of the Data Register will then produce the data word. The board is in the Polling Mode if the Interrupt Mode is disabled by writing a logic 0 to bit D6 of the Control Register.

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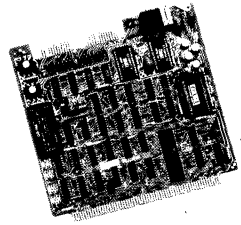


MP2216

MICROPERIPHERAL ANALOG INPUT/OUTPUT SYSTEM

A 12-BIT 32 CHANNEL ANALOG INPUT/ 2 CHANNEL ANALOG OUTPUT SYSTEM COMPATIBLE WITH ZILOG MICROCOMPUTERS

FEATURES

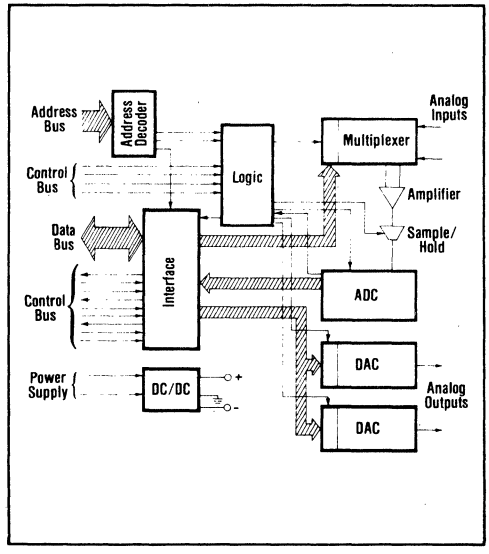
- ANALOG I/O ON THE SAME BOARD
- OPERATES FROM COMPUTER POWER SUPPLY
- HIGH LEVEL OR LOW LEVEL INPUTS
- BURNED-IN

DESCRIPTION

Completely compatible with Zilog's Z-80 MCB® and Z-80 MCS series of microcomputers, MP2216 provides a single board 12-bit resolution analog input/output system. The input section accepts 16 differential or 32 single-ended channels. Inputs ranging from millivolts to volts can be digitized because of MP2216's variable gain instrumentation amplifier.

Two optional channels of analog voltage are provided in the output section of the MP2216. The input data for each digital-to-analog converter is double buffered to minimize output glitches during a data update. Several output ranges and bipolar or unipolar operation are selected by on-board programming.

The MP2216 is mechanically, electrically and logically compatible with the Zilog systems. Power is derived from the +5V logic supply. Logic levels and drive capacity are matched to the system bus. Interfacing is accomplished primarily through a Z-80 PIO contained within the system.



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THEORY OF OPERATION

The MP2216 interfaces with the Z-80 I/O bus occupying 10 locations for the complete input/output system. The first four locations are required for the PIO. The next two locations transfer input channel address and board status. The remaining locations are used to pass data to the two digital-to-analog converters.

Data can be acquired from the analog inputs in either the POLLING or INTERRUPT mode:

POLLING MODE - A conversion is initiated by writing the analog channel address to the address register. The program must then periodically test the conversion bit in the status register to determine when the conversion is completed. During initialization of the MP2216's PIO, the interrupt enable must be reset (both ports) to prevent generation of interrupts.

The following program may be used to input a channel of data to the BC register pair:

```
LDA, XX          Load accumulator with channel address (XX) of data
                 to be converted.
OUT (YY), A      Outputs channel address to MP2216's address
                 register (location YY). This starts conversion.
  :
  :              Other software if desired for conversion time.
STATUS IN A, (ZZ) Input status bit from location ZZ.
BIT 0, A         Test status bit.
JP Z, STATUS     Jump to STATUS until conversion is complete.
IN A, (WW)       Transfers the least significant byte to the
                 accumulator. WW is PIO port A DATA register.
LD C, A
IN A, (WW + 1)   Transfers the most significant byte to the
                 accumulator. WW + 1 is PIO port B DATA register.
LD B, A
```

INTERRUPT MODE - After setting the board's PIO interrupt enable and vector address, conversion is initiated by writing to the address register. Program execution may then continue until the conversion is complete. At that point the system PIO generates an interrupt vector causing the CPU to begin execution of the MP2216's interrupt service routine. Software for this mode is the same as that of the polling mode, but without the status loop.

Outputting of data from the MP2216's two digital-to-analog converters is straightforward. Each converter occupies two addresses on the I/O bus. The least significant 8 bits of the 12-bit data word are written to the first of these data words while the four most signficant bits are written to the second data word.

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG INPUT SECTION	
INPUT CHARACTERISTICS	
Number of Channels	32 single-ended/16 differential
ADC Gain Ranges (Jumper Selectable)	0 - 5V, 0 - 10V, ±2.5V, ±5V, ±10V
Amplifier Gain Ranges (resistor programmable)	1 to 1000
Maximum Input Voltage Without Damage	±26 volts
Input Impedance	100MΩ, 10pF OFF Channel
	100MΩ, 100pF ON Channel
Bias Current	20nA
Differential Bias Current	10nA
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Throughput Time (max) G = 1	45μsec/channel
Throughput time (max) G = 1000	100μsec/channel
ACCURACY	
System Accuracy G = 1 (max)[1]	±0.025% FSR[2]
System Accuracy G = 1000	±0.1% FSR
Linearity	±1/2 LSB
Differential Linearity	±1/2 LSB
Quantizing Error	±1/2 LSB
Monotonicity[3]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE[4]	
System Accuracy Drift (max) G = 1	±30 ppm of FSR/°C
System Accuracy Drift (max) G = 1000	±80 ppm of FSR/°C
DYNAMIC ACCURACY	
Sample and Hold Aperture Time	30ns
Aperture Time Uncertainty	±5ns
Differential Amplifier CMR	74dB (DC to 1kHz)
Channel Crosstalk	80dB down at 1kHz, for OFF channel to ON channel
ANALOG OUTPUT SECTION	
OUTPUT CHARACTERISTICS	
Number of Channels	2
Output Voltage Range (strap selectable)	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA
Output Impedance	1Ω
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Output Settling Time (max)	10μsec
ACCURACY	
Output Accuracy	±0.0125% FSR
Temperature Coefficient of Accuracy	±30 ppm of FSR °C
POWER REQUIREMENTS	
MP2216, MP2216-AO	+5V ±5% at 1.6 amp
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Relative Humidity	95% noncondensing

TABLE I. Electrical Specifications

NOTES:
1. Includes offset errors, gain errors, linearity errors.
2. FSR means Full Scale Range.
3. No missing codes guaranteed.
4. Includes offset drift, gain drift and linearity drift.

SYSTEM CONFIGURATIONS

The MP2216 microperipheral board is available in two versions.
MP2216-AO: All features of the MP2216 system are included in this configuration.
MP2216: Provides all features except the two digital-to-analog converters.

MP8004: Cable assembly - two required.

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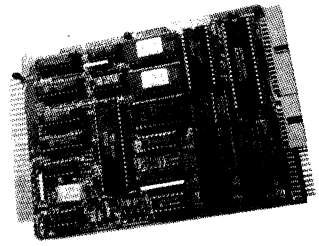

MP6102

STD BUS
SINGLE BOARD COMPUTER

FEATURES

- Z80A
- MEMORY CAPACITY TO 8k BYTES
- PROGRAMMABLE 24-BIT PARALLEL I/O
- RS-232-C SERIAL I/O
- SELECTABLE POWER ON/RESET JUMP ADDRESS
- ONBOARD COUNTER/TIMER
- MULTILEVEL INTERRUPT CONTROLLER
- SOFTWARE-PROGRAMMABLE BAUD RATE
- ONBOARD MONITOR/BIOS SOFTWARE IN EPROM

DESCRIPTION

The MP6102 is a Z80-based computer which generates all STD-Z80 signals. A great degree of flexibility is built into the MP6102 through the use of fuse-link PROMs for memory and I/O control allowing the user to modify functional control to suit a specific application.

Interrupt control is performed by an AM9519 Universal Interrupt Controller, which provides management and priority resolution for up to eight maskable interrupt inputs. Parallel I/O is provided by an 8255A Peripheral Interface, supplying 24 bits of multiple mode input or output.

The onboard Z80A-CTC provides three channels of user-definable counter/timer functions. One of the channels is software-programmable as the time base for the RS-232-C port. This serial I/O port, programmable to 9600 baud, is based upon the I8251A USART, and afford the user a number of communications protocols from which to choose. All I/O connectors are on the user edge of the card on 0.100″ grid centers.

The EPROM-resident Monitor program provides for keyboard functions and the basic I/O software (BIOS) for CP/M® compatible disk and terminal I/O.

CP/M is a registered trademark of Digital Research

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SPECIFICATIONS

ADDRESS AND I/O INFORMATION

ADDRESS SELECTION

The MP6102 can occupy as much as one 8k byte page in memory. As shipped, the two EPROM sockets occupy the third and fourth 2k byte blocks, configured for 2716 EPROMs, while the byte-wide RAM occupies the second 2k byte block for a total of 6k bytes of resident onboard memory. The first 2k byte block is considered to be offboard.

The board is shipped with memory paged to locations E800 to FFFF with the Monitor/BIOS EPROM occupying F000 to F7FF (EPROM 1). F000 is also the power-on jump address.

I/O ADDRESSING

Sixteen I/O ports are occupied by onboard functions, as follows:

	Port
USART data	0, 2
USART control/status	1, 3
Z80-CTC	4, 5, 6, 7
Interrupt data	8, A
Interrupt control	9, B
PIO channels A, B, C	C, D, E
PIO control	F

Any other references cause data transfers to occur from the bus.

OPTIONS AND SPECIAL FEATURES

Onboard memory may be deactivated using the PHANTOM line and the lower EPROM may be unconditionally asserted using PROM 1 request.

Special memory or I/O decoder PROMs are available from the factory.

MEMEXP and IOEXP may be programmable using an onboard parallel port bit.

EPROMs can be of 2716 or 2732 type, within the confines of the selected 8k page. (Standard shipping configuration is 2716 for each EPROM socket.)

The user interface allows for cascading interrupt controllers, bringing onboard three external control functions and providing the selected baud clock for external use.

ORDERING INFORMATION

When ordering the MP6102, please specify desired configurations as shown below:

MP6102-0	2.5MHz
MP6102-1	4.0MHz

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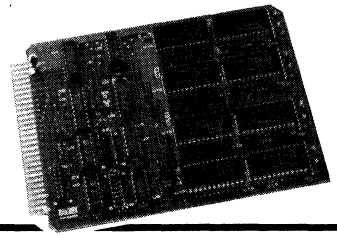

MP6202

STD BUS EPROM/RAM MEMORY CARD

FEATURES

- SOCKETED FOR 32K EPROM
- ALTERNATE 16K RAM
- EPROM AND RAM MIX
- SELECTABLE MEMORY ADDRESS
- 1K MEMORY BOUNDARIES
- MEMEX SUPPORT
- MINIMUM MEMORY SPACE CONFIGURABLE

DESCRIPTION

The MP6202 EPROM/RAM Memory Card has been designed to meet the varied requirements of STD bus system designs which call for a mix of EPROM and RAM.

System memory may be mapped in the smallest logical increments, relieving the requirement for allocating entire 8k or 16k blocks to EPROM/RAM which only use a portion of that block. The MP6202 memory may be configured from 1k byte to 4k byte blocks; however, the memory type selected for both EPROM and RAM must be of the same family type.

Through jumper options, any logical memory address boundary may be occupied. Depending upon the application, the card may be populated with only as many memory chips as required; therefore, only memory space in use is allocated.

User-selectable options allow the MP6202 to be enabled upon either the occurrence of a low active or a high active MEMEX signal. Thus, two banks of memory are easily implemented.

SPECIFICATIONS

SYSTEM CLOCK RATE, max
4.0MHz

MEMORY SUPPORT CAPABILITY
32k bytes, max

MEMORY ORGANIZATION
Selectable, depending upon memory type installed; addressable on the minimum logical boundary, as defined by the memory type in use.

IC MEMORY TYPES
2508 Intel/TI
2516 (2716) Intel/TI
2732 Intel
4016 TI
4801 Mostek

BUS LOADING
1LSTTL load

BUS DRIVE
24mA sink, 15mA source

CARD DIMENSIONS
4.5" x 6.5"

VOLTAGE REQUIREMENTS
+5VDC at 250mA (not including memory chips)

OPERATING TEMPERATURE RANGE
0°C to 55°C

STD BUS COMPATIBILITY
All 8-bit microprocessors

ORDERING INFORMATION

The MP6202 is available in the following configurations. To order, please specify as shown below:

MP6202-0	EPROM/RAM Memory Card, supplied with eight Intel 2716 EPROMs or equivalent
MP6202-1	EPROM/RAM Memory Card, supplied without EPROMs
MP6202-2	EPROM/RAM Memory Card, supplied with TMM2016 RAM or equivalent

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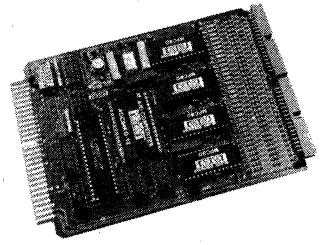

MP6303

STD BUS
ANALOG INPUT BOARD

FEATURES

- 32-CHANNEL
- DIFFERENTIAL INPUTS
- 12-BIT RESOLUTION
- SELECTABLE INPUT RANGES
- USER-CONFIGURABLE INPUT CONDITIONING
- VARIABLE RESISTOR-SELECTABLE GAINS
- SAMPLE/HOLD
- HALT MODE OPERATION
- I/O MAPPED
- REGISTER TRANSFER OF DATA

DESCRIPTION

The MP6303 is a 32-channel, 12-bit differential input analog-to-digital converter for data acquisition in the STD bus microsystem environment.

The converter can be configured to operate with input signals in the range of ±2.5VDC, ±5VDC, ±10VDC, 0 to 5VDC or 0 to 10VDC. The MP6303 can perform a conversion in 10μsec, plus filter and multiplexer settling time.

The A/D converter contains a high performance instrumentation amplifier with a gain setting from 1V/V to 1000V/V, to accommodate low level sensors such as strain gauges and thermocouples, and high level signals such as power supply outputs.

SPECIFICATIONS

(Typical at +25°C and rated power unless otherwise noted)

NUMBER OF CHANNELS	32 differential
RESOLUTION	12-bit
THROUGHPUT TIME [G = 5]	16μsec
INPUT SIGNAL RANGE	±2.5mV to ±10V
ADC RANGE	0 to 5V, 0 to 10V, ±2.5V, ±5V, ±10V
AMPLIFIER GAIN RANGE[1]	1 to 1000
INPUT IMPEDANCE	10GΩ
BIAS CURRENT	35nA
CMRR	90dB
AMPLIFIER INPUT OFFSET	1.5mV
AMPLIFIER INPUT OFFSET DRIFT	5mV/°C
BUS LOADING	1LSTTL load per line
POWER	+5VDC at 100mA, ±15VDC at 80mA
OPERATING TEMPERATURE	0°C to 55°C
STD BUS COMPATIBILITY	STD-Z80, STD-8080, STD-8085, STD-6800, STD-6502

NOTE: 1. Potentiometer adjustment factory set to X5.

POWER SUPPLY OPTION ... MP6309 External ±15VDC Power Supply Card

ORDERING INFORMATION

The MP6303 is available in 8-channel increments, up to 32 channels. To order, specify number of channels as shown.

MP6303-08	8 Analog Input Channels
MP6303-16	16 Analog Input Channels
MP6303-24	24 Analog Input Channels
MP6303-32	32 Analog Input Channels

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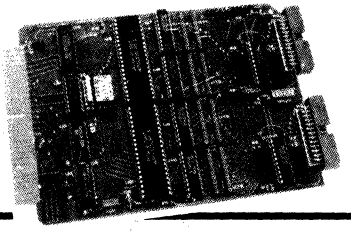

MP6304

STD BUS
PARALLEL INPUT/OUTPUT

FEATURES

- I/O ADDRESSING
- SELECTABLE INTERFACE LEVELS
- COMMON FAMILY LOGIC ELEMENTS
- MULTIMODE PROGRAMMABILITY

DESCRIPTION

The MP6304 is a versatile, programmable parallel TTL input/output card designed for the STD bus microsystem environment. The flexibility of the card allows it to be used in practically all STD bus environments, including STD-Z80, STD-8080, and others.

A number of user-selectable options are provided so that the card may be configured for a wide variety of application requirements.

Addressing is switch-selectable so that the card may be located in any contiguous 8-location group throughout the entire I/O range. All I/O lines are buffered with inverting or noninverting buffers of the users' choice.

Provision is made for common family logic elements in the input and output buffer areas. The onboard Intel 8255A peripheral interface circuits may be programmed to operate as either input, output, bidirectional and bit set/reset, latched or strobed or a combination thereof.

SPECIFICATIONS

SYSTEM CLOCK RATE, max
4.0MHz

I/O ORGANIZATION
8 consecutive I/O ports; 48 bits, 32 definable as input or output in 8-bit groups, 16 definable as input or output on a bit-for-bit basis.

I/O ADDRESSING
Switch-selectable

INTERFACE LEVELS
All I/O lines are buffered with inverting or noninverting buffers of the user's choice.

OPERATING RANGE
0°C to 55°C

CARD DIMENSIONS
4.5" x 6.5"

CARD FORMAT
STD bus

VOLTAGE REQUIREMENTS
+5VDC at 400mA

I/O CIRCUIT TYPE
Intel 8255A

STD BUS COMPATIBILITY
STD-Z80, STD-8080, STD-8085, STD-6800, STD-6502

USER SELECTABLE OPTIONS

The following information describes the jumper and switch options provided as standard features with each MP6304.

SWITCH GROUP U5

Switch	I/O Address Line
1	A7
2	A6
3	A5
4	A4
5	A3

A switch placed to the ON position conditions the card-select decoder to expect a low condition on the input address lines to produce the select signal. To set the card to occupy addresses 00H through 07H, therefore, all switches are set to the ON position.

8255A PORT C BUFFER ELEMENTS

Jumper Groups A and B are provided for the 8255A Port C functions so that the driver/receiver elements may be configured on a bit-wise basis, compatible with the function of Port C.

8255A PORT A AND B BUFFER ELEMENTS

The rows of octal TTL elements U8 through U11 and U12 through U15 are provided so that the 8255A Ports A and B may be configured as Input or Output. If a port will be programmed to be OUTPUT, the logic element (Element A) is installed in the U8 row and becomes a driver. If that port will be programmed to be an INPUT, the logic element is installed in the U12 row and becomes a receiver.

Note that in both the Element A and Element B positions, provision has been made for "generic" or equivalent circuit usage, where pins 1 and 19 of each of the elements are left definable by the user.

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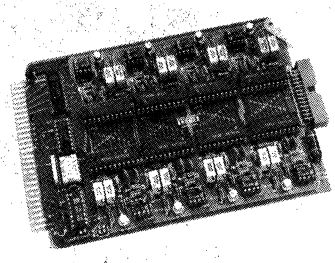

MP6305

STD BUS
8-CHANNEL DIGITAL-TO-ANALOG CONVERTER

FEATURES

- VOLTAGE OR CURRENT MODE
- 8-BIT RESOLUTION
- FAST SETTLING TIME
- SELECTABLE OUTPUT RANGE
- SELECTABLE ADDRESSING
- MULTIMODE OPERATION
- SELECTABLE POWER SOURCE

DESCRIPTION

Designed with a full array of features, the MP6305 is an 8-channel digital-to-analog converter for data conversion applications in the STD bus microsystem environment.

With each channel independently configurable, the MP6305 can operate in either the current or voltage mode. In the current mode, the current source may be provided onboard or offboard. If jumpers are installed around the current source, operation in the voltage mode is enabled, with the output configurable for unipolar (0—10V) or bipolar (±5V) operation.

I/O addresses may occupy a range between 00H and FFH as provided by user-selectable miniswitches. Jumper-selectable options allow positive and negative voltages to be supplied by either the microsystem or an external supply. In both cases, all channels are referenced to ground.

SPECIFICATIONS

OUTPUT RANGE
0 to 10VDC at 10mA voltage mode unipolar
−5VDC to +5VDC at 10mA voltage mode bipolar
4mA to 20mA current mode (typical)
[may require external current source]

D/A CONVERTER ACCURACY
0.1%

D/A CONVERTER SETTLING TIME
2.3μsec, max (all bits high to low)

SYSTEM CLOCK RATE, max
4.0MHz

I/O ADDRESSING
Any 8 consecutive I/O addresses between 00H and FFH.

VOLTAGE REQUIREMENTS
+12VDC at 135mA
−12VDC at 140mA
+5VDC at 90mA

OPERATING TEMPERATURE RANGE
0°C to 55°C

CARD DIMENSIONS
4.5" x 6.5"

OUTPUT CONNECTOR TYPE
26-pin (0.100" x 0.100")

STD BUS COMPATIBILITY
STD-Z80
STD-8080
STD-8085
STD-6800
STD-6502

ORDERING INFORMATION

The MP6305 is available in either 4- or 8-channel versions. To order, please specify configuration as shown below:

MP6305-4	4 Analog Output Channels
MP6305-8	8 Analog Output Channels

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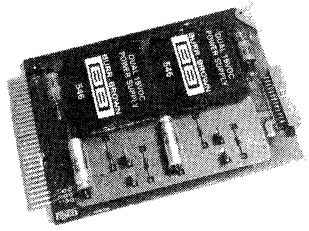

MP6309

STD BUS DC POWER SUPPLY

FEATURES

- POWERED FROM SYSTEM BUS
- LOW PROFILE
- ISOLATED
- CURRENT LIMITED
- REGULATED
- EASY TO CONNECT

DESCRIPTION

The MP6309 power supply provides the STD user with precision ±15VDC outputs on a single low profile STD format board. The MP6309 is useful in a variety of applications which provide non-STD auxiliary voltage, especially for powering analog interface circuitry.

Utilizing modular DC/DC converters, the MP6309 provides a choice of 240mA (MP6309-0) or 120mA (MP6309-1) rated current outputs for the voltages supplied.

Requiring only a +5VDC input from the STD bus, the MP6309 provides a +15V and −15V to the front edge connector for external routing to boards or devices requiring these voltages. A strapping option is provided which can provide the ±15V to the STD bus (pin 55—auxiliary positive voltage, pin 56—auxiliary negative voltage).

The supply provides 300VDC of input-output isolation protection. Outputs are current-limit-protected to withstand overloads and direct short circuits to ground.

SPECIFICATIONS

RATED OUTPUT ..... ±15VDC
LOAD REGULATION ..... 0.02% typ, 0.1% max
ISOLATION 300VDC
OUTPUT RIPPLE ..... 20mV peak, max; 0.8mV rms, max
VOLTAGE/TEMPERATURE COEFFICIENT ..... ±3mV/°C
OPERATING TEMPERATURE RANGE ..... 0°C to 55°C
CARD FORMAT ..... STD
CARD DIMENSIONS ..... 4.5" x 6.5" x 0.465"
REMOTE CONNECTOR TYPE ..... 2 x 13 on 0.1" centers
DC/DC CONVERTER TYPE ..... Burr-Brown 546 or equivalent
STD BUS COMPATIBILITY ..... All

INPUT/OUTPUT CONNECTOR [P1] PINOUT	
Pin	Signal
9, 22	AGND
11, 24	−15V
12, 25	+15V

BUS CONNECTOR PINOUT	
Pin	Signal
1, 2	+5V
3, 4	GND
53, 54	AUX GND
55	AUX +V
56	AUX −V

NOTE: AUX GND, AUX +V and AUX −V can be jumpered to AGND, +15V and −15V respectively.

ORDERING INFORMATION

	Voltage Requirements	Current Output
MP6309-0	+5VDC at 3.6A (max load)	240mA
MP6309-1	+5VDC at 1.8A (max load)	120mA

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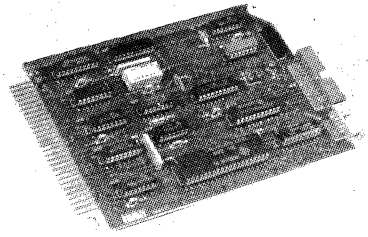

MP6311

STD BUS
IEEE-488 CONTROLLER

FEATURES

- FULL IEEE-488 IMPLEMENTATION
- DMA CAPABILITY
- INTERRUPT CAPABILITY
  - —POLLED
  - —VECTORED
  - —DAISY-CHAINED
  - —EXTERNALLY PRIORITIZED
- I/O MAPPED
- SOFTWARE SUPPORT
- STAR OR LINEAR BUS
- EASY TO INTERFACE

DESCRIPTION

The MP6311 is an IEEE-488 General Purpose Interface Bus (GPIB) to STD bus interface designed to be compatible with most any CPU on the STD bus. It is based on the TMS9914A GPIB Adapter I.C. and can be software-programmed to be a talker, listener, or controller.

The unit is designed to be compatible with most STD processor standards, and is software-programmable for the talker, listener, or controller modes. Other user-definable options allow various interrupt or DMA operations to be implemented, with those inputs and outputs routed to the front edge of the circuit card for ease of access.

A comprehensive software support package is supplied, at no cost, with each unit. The package consists of a CP/M®-compatible diskette, which contains a driver program to allow the user to configure the system in any of the modes. Also provided is a complete technical manual with program listings and typical application guidelines. An interface cable (4311 to IEEE) is provided.

SPECIFICATIONS

TRANSFER RATE, max
1M byte/sec with shielded, twisted-pair cable over limited distance; 250k byte to 500k byte/sec typical

INTERRUPT OPTIONS [connector P2]
STD bus-compatible: Z80 Mode 2, NMIRQ
(nonmaskable interrupt request)
External interrupt controller through front edge connector

DMA OPTIONS [connector P2]
STD bus ST4101 processor-compatible (Z80-DMA controller)
External DMA controller, signals compatible with Intel I8257, Motorola MC6844, and TI TMS9911, through front edge connector

VISUAL INDICATORS
LED array for GPIB control/status lines

I/O ADDRESSING
Any 16 consecutive I/O addresses between 00H and FFH; extended addressing with IOEXP

SYSTEM CLOCK RATE, max
4.0MHz

VOLTAGE REQUIREMENTS
+5VDC, 550mA

CONNECTOR TYPES
GPIB: 2 x 12 male, 0.1" centers
Ext DMA/INT: 2 x 5 male, 0.1" centers

OPERATING RANGE
0°C to 55°C

COMPATIBILITY
STD-8080, STD-Z80, STD-8085

CP/M is a trademark of Digital Research, Inc.

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EDGE CONNECTOR PIN ASSIGNMENTS

P2 Front edge connector

Pin	Function	Pin	Function
1	Ground	2	Interrupt request (active low)
3	NC	4	NC
5	Ground	6	DMA request (active low)
7	NC	8	NC
9	Ground	10	DMA grant (active low)

P3 Front edge connector

Pin	Function	GPIB Pin	Pin	Function	GPIB Pin
1	DI01	1	2	DI05	13
3	DI02	2	4	DI06	14
5	DI03	3	6	DI07	15
7	DI04	4	8	DI08	16
9	EOI	5	10	REN	17
11	DAV	6	12	GND	18
13	NRFD	7	14	GND	19
15	NDAC	8	16	GND	20
17	IFC	9	18	GND	21
19	SRQ	10	20	GND	22
21	ATN	11	22	GND	23
23	GND	12	24	GND	24

SOFTWARE DESCRIPTION

Subroutine	Description
GPCLR	Set MP6311 address and clear all devices on bus with Interface Clear
GPABT	Abort communications and put controller in idle state
GPWRT	Write a string to addressed device using programmed I/O
GPWRTD	Write a string to addressed device using DMA
GPWRT1	Set up interrupt-driven write string to addressed device and output first byte
GPWIST	Get status of interrupt-driven write
GPRED	Read a string into a buffer from addressed device using programmed I/O
GPREDD	Read a string into a buffer from addressed device using DMA
GPREDI	Set up interrupt-driven read string from addressed device
GPRIST	Get status of interrupt-driven read string
PRTSTR	Print string on output console

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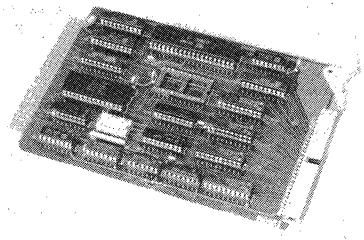


MP6394

STD BUS
INTELLIGENT PARALLEL INPUT/OUTPUT

FEATURES

- ONBOARD Z80 PROCESSOR
- 2K EPROM
- 1K RAM
- 8-BIT TTL OUTPUT FROM ONBOARD PROCESSOR
- 32-BIT TTL INPUT TO ONBOARD PROCESSOR
- BIDIRECTIONAL COMMUNICATION AMONG PROCESSORS
- ONBOARD COUNTER/TIMER
- +5VDC ONLY
- 4MHz OPERATION
- Z80 MODE 2 INTERRUPT CAPABILITY

DESCRIPTION

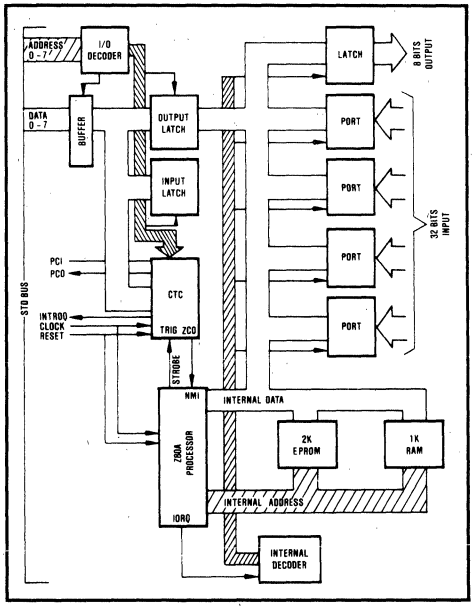
Intended for digital data acquisition and intelligent controller applications, the MP6394 Intelligent Parallel I/O provides 32 bits of input and 8 bits of output in STD bus systems.

With 1k byte of RAM and 2k byte of EPROM for program storage, the onboard Z80 processor communicates with the host processor via one 8-bit input port, one 8-bit output port and a counter/timer circuit (CTC). The CTC, resident in the host I/O space, generates interrupts.

The host interrupts conform to Z80 Mode 2 while onboard interrupts are nonmaskable interrupts (NMI) from an output of the CTC.

When utilized in environments which require the monitoring and control of a large number of logic level inputs and outputs, the MP6394 can outperform other types of parallel I/O cards because the onboard processor can execute the monitor/control program and leave the host processor free for system level tasks. Thus, the host processor is interrupted only upon the occurrence of a preprocessed event, and system throughput is greatly enhanced.

The I/O organization of the unit allows residence in any consecutive 4-port group, switch-selectable by the user.



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SPECIFICATIONS

HOST I/O ORGANIZATION
4 ports; 1 for input, 1 for output, and 2 for CTC interrupts. All ports addressable to any even 4-port boundary from 00 to FC.

HOST I/O ADDRESSING
4 consecutive, switch selectable I/O locations:
Base +0 ..... 8 bits output to onboard Z80 processor (write only)
+1 ..... 8 bits input from onboard processor (read only)
+2 ..... CTC channel (read/write)
+3 ..... CTC channel (read/write)

INTERNAL I/O ORGANIZATION
8 fixed I/O locations:
0 ..... 8 bits input from STD bus (read only)
1 ..... 8 bits output from STD bus (write only)
2 ..... strobe CTC channel 1 (read/write)
3 ..... 8 bits output to P2, pins 5—12 (write only)
4 ..... 8 bits input from P2 (read only)
5 ..... 8 bits input from P2 (read only)
6 ..... 8 bits input from P2 (read only)
7 ..... 8 bits input from P2 (read only)

INTERNAL MEMORY ORGANIZATION
1kbyte RAM, 2kbyte EPROM:
0000—07FF ..... EPROM
0800—0BFF ..... RAM

PROCESSOR TYPE
Z80A (4.0MHz), Z80B (6.0MHz)

RAM TYPE
2114-type or equivalent

EPROM TYPE
2716-type or equivalent

CONNECTOR TYPE
Data connector (P2):
one 2 x 25-pin male shrouded connector, 0.1" spacing

VOLTAGE REQUIREMENTS
+5VDC ±5% at 660mA

MAXIMUM HOST SYSTEM CLOCK RATE
4.0MHz

INPUT LOADING
1LSTTL load per signal line (IORQ: 2LSTTL loads per signal line)

OPERATING TEMPERATURE RANGE
0°C to 55°C

CARD DIMENSIONS
4.5" x 6.5"

CARD FORMAT
STD bus

STD BUS COMPATIBILITY
STD-Z80, STD-8080*, STD-8085*
(If Z80 Mode 2 interrupts are used, compatibility is STD-Z80 only.)
*No vectored interrupt capability.

ORDERING INFORMATION

The MP6394 is available in two versions, depending on the configuration of the host processor. Please specify version when ordering:

MP6394-0 4.0MHz operation
MP6394-1 6.0MHz operation

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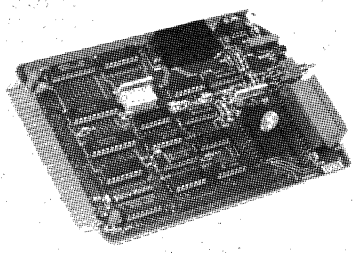

MP6421

STD BUS
UNIVERSAL EPROM PROGRAMMER

FEATURES

- JEDEC EPROMS (+5V only)
- VARIABLE MEMORY WINDOW
- MEMEX SUPPORT
- SELF-SEQUENCING
- PERSONALITY MODULES
- POWER FROM BUS
- MULTIPLE POWER SUPPLY DEVICES
- REMOTE HARDWARE

DESCRIPTION

The MP6421 provides comprehensive EPROM programming capability for the STD bus environment.

The unit will program all single supply (+5V only) JEDEC type EPROMs currently available. Trisupply EPROMs may be read only.

EPROMs are read and programmed through a variable size memory window. MEMEX is decoded to allow optional segregation of the EPROM memory window from system memory. All timing necessary for EPROM programming is generated onboard and is synchronized with the processor via the WAITRQ line. This feature eliminates the need for additional software overhead.

All non-STD bus voltages required for EPROM programming are provided by an onboard voltage converter.

Inexpensive personality modules are available for all single supply EPROMs. Front edge connectors are provided for attaching remote programming sockets and are pin-compatible with the optional PS48-0 and PS48-1 front panel modules. A complete technical manual is provided.

SPECIFICATIONS

MEMORY ADDRESSING
1k to 8k, switch-selectable to any 1k boundary, onboard or offboard generated and decoded MEMEX.

I/O ADDRESSING
2 ports, jumper-selectable to any 8-port boundary.

EPROM TYPES
I2716, I2732, I2732A, I2764, I27128, MK2764, TMS2516, TMS2532, TMS2758, TMS2764, etc.

SYSTEM CLOCK RATE, max
4.0MHz

INPUT LOADING
1LSTTL load per signal line

VOLTAGE REQUIREMENTS
+5VDC
−5VDC for trisupply EPROMs only
−12VDC for trisupply EPROMs only

OPERATING TEMPERATURE RANGE
0°C to 55°C

CARD DIMENSIONS
4.5" X 6.5" X 1.2"

REMOTE CONNECTOR TYPES
2 X 17 on 0.1" centers
2 X 10 on 0.1" centers

STD BUS COMPATIBILITY
STD-Z80 if WAITRQ* option used; STD processor independent otherwise

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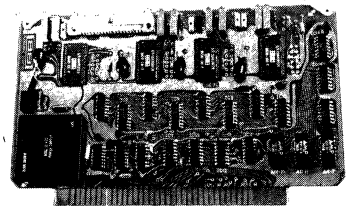


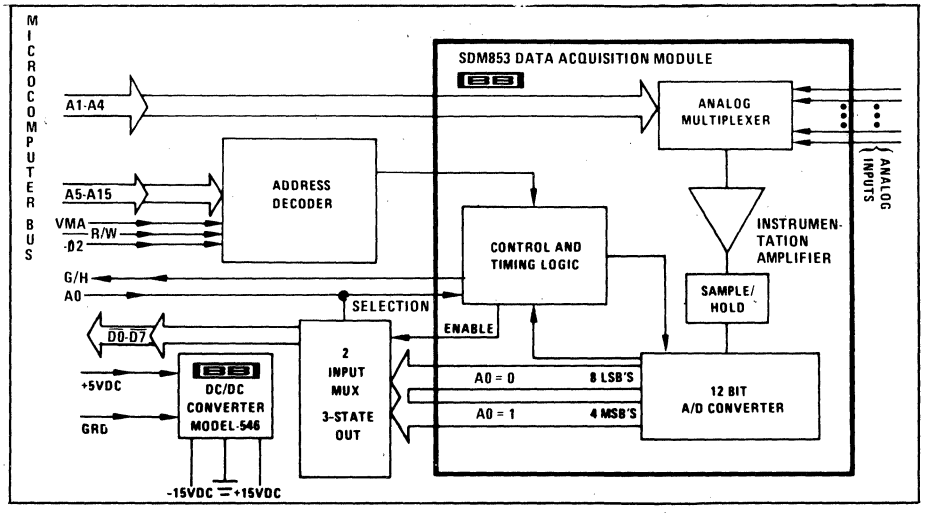
MP7104
MP7208
MP7216

MICROCOMPUTER ANALOG I/O SYSTEMS

MP7104 - Analog Output System
MP7208 - Data Acquisition System
MP7216 - Data Acquisition System

FEATURES

- COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser®
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Operates from +5VDC power supply
- EASY TO USE
  - All cabling and connectors are included



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DESCRIPTION

These microcomputer peripherals provide two much needed functions that interface directly to Motorola's Micromodule and EXORciser microcomputers. The functions are: 1) Analog Data Acquisition and 2) Analog Output. The devices are electrically and mechanically compatible with Motorola microcomputers. Each analog system is contained on a single printed circuit board that is treated as memory input and output by the CPU. The cards will mate to any memory or I/O slot. The analog interface for each system is at a flat cable connector at the opposite edge of the board from the bus connector.

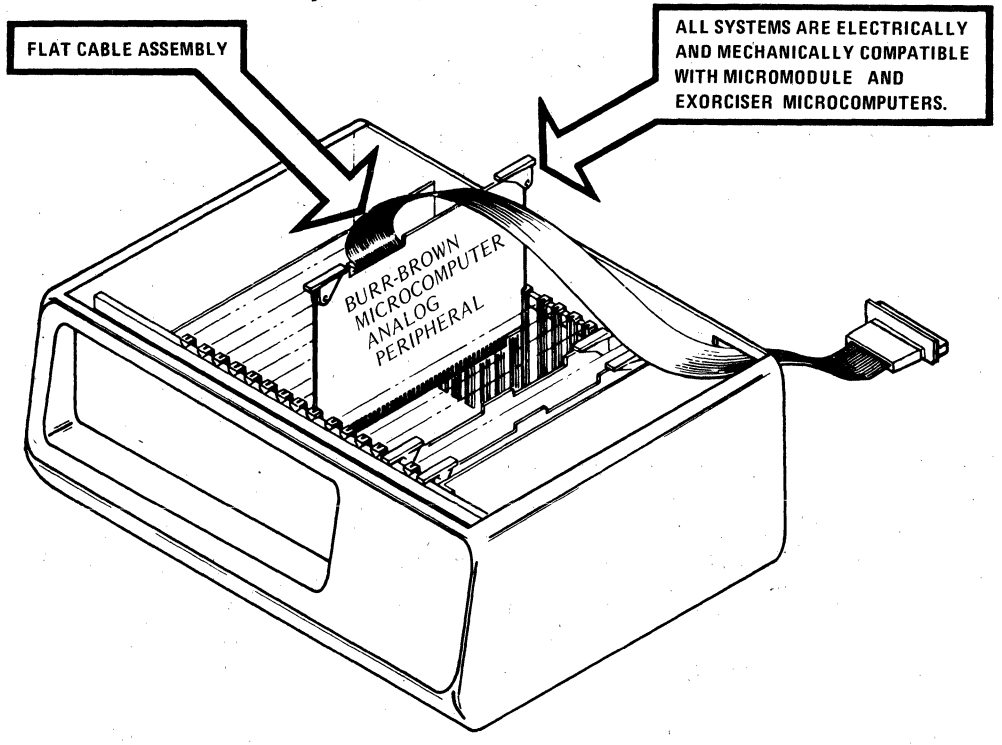
The Data Acquisition Systems consist of the MP7208, an 8 channel differential input system; and the MP7216, a 16 channel single-ended input system. Burr-Brown's SDM853 modular data acquisition system is used to implement these systems. The data acquisition systems include an input multiplexer, high gain instrumentation amplifier, sample/hold and 12 bit A/D converter along with all the necessary timing, decoding and control logic. The model 546 DC/DC converter (+5V to ±15V) is also used so that only the microcomputer's +5VDC power supply is required.

The MP7104, an analog output system, provides four analog output channels (using four of Burr-Brown's hybrid 12 bit DAC80 D/A converters). This board also contains the 546 DC/DC converter to assure operation on +5VDC power. The input of the D/A converters are double buffered so that a complete 12 bit word can be strobed into a D/A converter's input register to minimize output glitches.

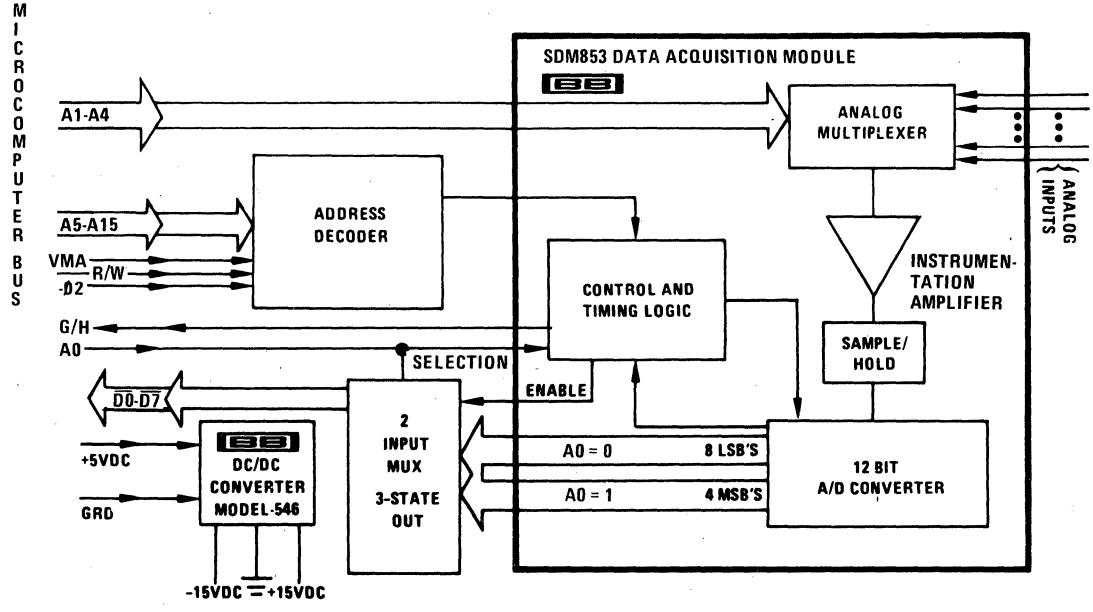
THEORY OF OPERATION

When programming with these peripherals, they are treated as memory locations. Both the A/D converter output and the D/A converter input are 12 bit words so two 8 bit memory locations are needed for each channel. But, because the address block occupied by each peripheral is switch selectable, it can be placed anywhere in memory. Since these units are treated as memory, a single instruction is all that's needed to set the input of a D/A converter. For instance, the STX (write) instruction followed by the proper address is used to write data from the index register to the MP7104. The four most significant bits are written first followed by the eight least significant bits. Through double buffering in the MP7104 only one 12 bit data transfer is made to the DAC to minimize glitching.

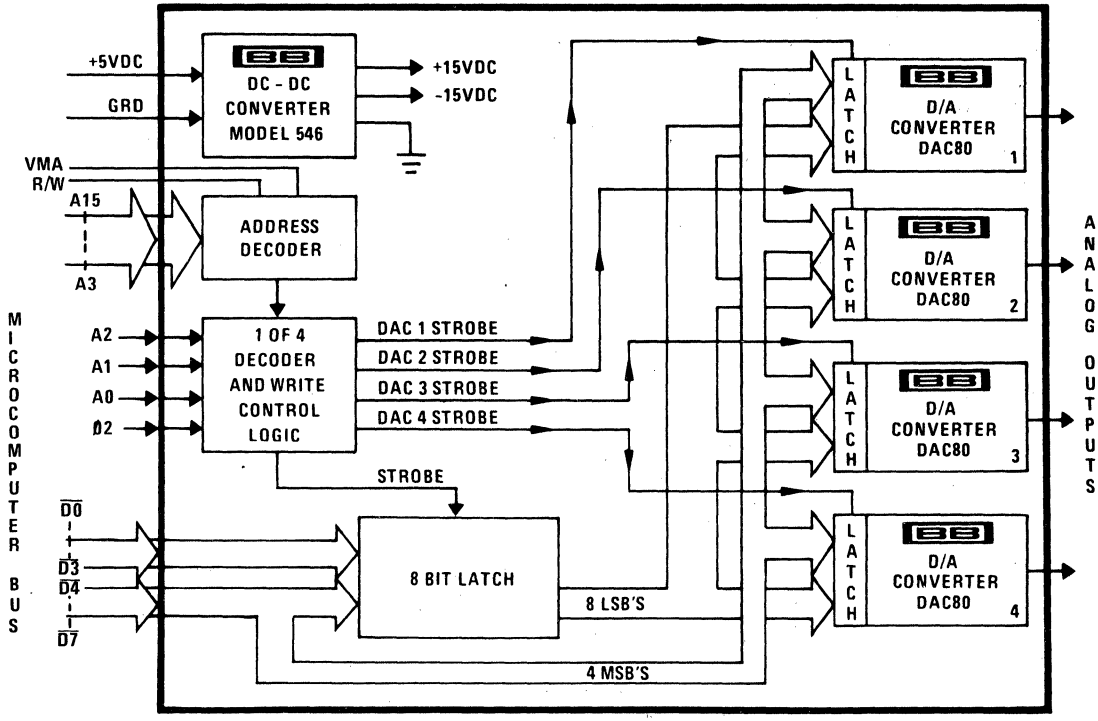
All of these systems are jumpered at the factory with the first channel at address $EF00_{16}$ (that's 1110 1111 0000 0000 in binary). Each subsequent channel is two memory locations past the start of the last channel so that the second channel is at location $EF02_{16}$ (1110 1111 0000 0010).



ANALOG INPUT SYSTEM - MP7208/7216



ANALOG OUTPUT SYSTEM - MP7104



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT	
Number of analog inputs	MP7208
8 channel differential	MP7216
16 channel single-ended	
Input voltage range[1]	±10mV to ±10V
Input current loop ranges (resistor programmable)	4-20mA, 10-50mA
ADC gain ranges (strap selectable)	±10V, 0 to 10V, 0 to 5V ±5, ±2.5V
Amplifier gain range (resistor programmable)	1 to 1000 V/V
Amplifier gain equation (resistor programmable)	$G = 1 + 20k\Omega / R_{TSI}$
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C	20nA
0 to 70°C	50nA
Amplifier output noise (Gain = 100 R_S = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage (max)[4]	400μV
Amplifier input offset voltage drift (max)	$2 + \frac{20}{G}$ μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy, ±10V range (max)	±0.025% FSR[2]
±10mV range	±0.1% FSR
Temperature coefficient of accuracy	
±10V range (max)	±0.003% FSR/°C
±10mV range	±0.01% FSR/°C
Conversion time ±10V range	33 microseconds
±10mV range	100 microseconds
CMRR (for differential inputs)	74 dB (DC to 2000 Hz)
Sample/hold aperture time	30ns
DIGITAL INPUT/OUTPUT	
All signals are compatible with Micro-computer bus	
Output coding	Bipolar, Two's Complement; unipolar, straight binary
An analog input channel is selected by:	A1 through A4
The output data bits are read into:[3]	D0 through D7
POWER REQUIREMENTS	
MP7208, MP7216	+5VDC ±5% at 1 amp, 25mV ripple
MP7217-NS, MP7209-NS	+5VDC ±5% at +500mA, 25mV ripple +15VDC±3% at +50mA, 5mV ripple -15VDC ±3% at -75mA, 5mV ripple
TEMPERATURE RANGE	
Temperature	0 to 70°C
ANALOG OUTPUT	
Number of analog outputs: 4	MP7104
Output voltage range[1]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time	< 10 microseconds
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy (max)	±0.0125% FSR
Temperature coefficient of accuracy	
Unipolar	±0.003% FSR/°C
Bipolar	±0.0045% FSR/°C
DIGITAL INPUT/OUTPUT	
All signals are compatible with Micro-computer bus	
An analog output channel is selected by:	A1 and A2
The input data bits are read by:	D0 through D7
POWER REQUIREMENTS	
MP7104	+5VDC ±5% at +1 amp, 25mV ripple
MP7105-NS	+5VDC ±5% at +500 mA ±5mV ripple +15VDC±3% at +100mA, 5mV ripple -15VDC ±3% at -100mA, 5mV ripple
TEMPERATURE RANGE	
Temperature	0 to 70°C

OPERATING INSTRUCTIONS

INSTALLATION

The MP7104, MP7208 and the MP7216 are shipped from the factory calibrated and ready for immediate use. Installation requires only plugging the card into any empty slot in the EXORciser or with a Micromodule and routing the board's mating I/O cable to the back panel. The cable supplied with each board is shielded and, in the case of the MP7104, provided with the proper terminations.

PROGRAMMING

Programming of these analog I/O boards is easily accomplished since all are treated as memory locations. The MP7104 uses any memory reference instruction that can write data from the index and stack point registers or the accumulators. In a similar manner a channel in the MP7208 or MP7216 can be read by any memory reference instruction that can read data into the index and stack pointer registers or the accumulators.

The voltage data for these boards is represented by a 12 bit two's complement binary number. Each bit has a value of 4.88mV, with the polarity of the voltage indicated by the sign of the binary number. Since the index, stack pointer and A and B accumulator pair registers are 16 bits long and the data word is 12 bits, the MP7208 and MP7216 set these unused bits to the same value as the most significant bit of the data. This assures the proper representation of the data's sign.

Each board is set at the factory for a block of addresses beginning at EF00. Any analog data channel requires two memory locations since the digital data is 12 bits. The most significant 4 bits of data are always located in an even location while the remaining 8 bits are located in the next higher location. Thus, the first analog channel is located at EF00 and EF01 while the second analog channel is located at EF02 and EF03. When moving data, all boards require that the most significant bits (even addresses) be referenced first. In addition, the MP7208 and MP7216 systems require the most significant data to be read followed by a NOP instruction for proper starting of the conversion process. This can be illustrated as shown below:

```
LDAA    EF00    Starts conversion of CH0
NOP             Allows processor to halt
                during conversion
LDX     EF00    Reads data as soon as
                conversion is complete
```

(1) Connected at the factory for ±10V range.
(2) FSR is Full Scale Range (i.e., 20V for ±10V range, 10V for 0 to +10V range).
(3) The 4 MSB's when conversion is complete, followed by the 8 LSB's.
(4) Adjustable to zero.

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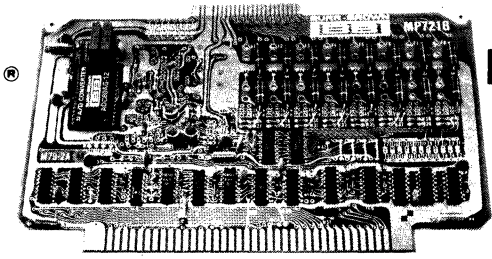
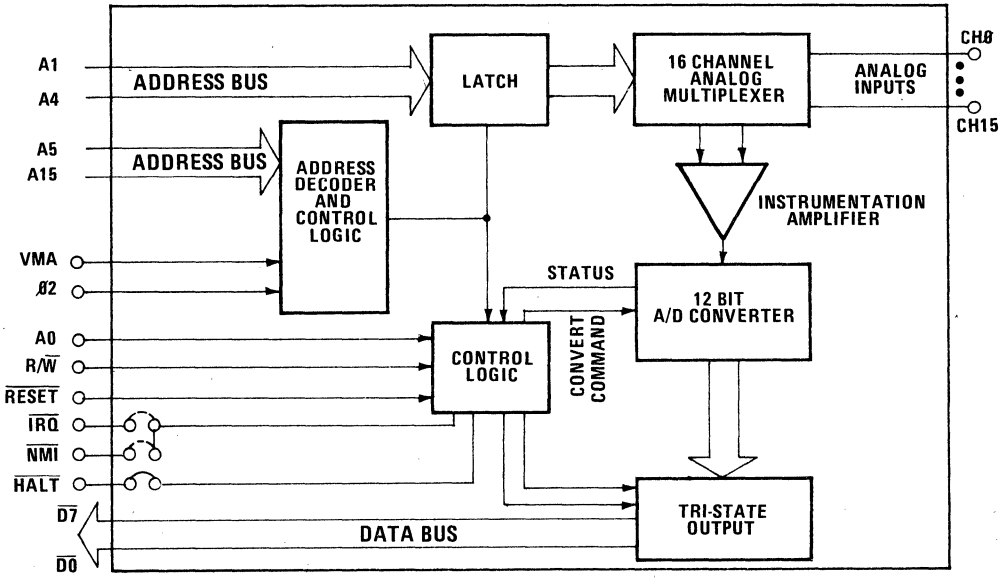


MP7218

MICROCOMPUTER ANALOG INPUT SYSTEM

A LOW-COST 12-BIT, 16-CHANNEL ANALOG INPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® MICROCOMPUTERS



FEATURES

- 70°C BURN-IN
- OPERATES FROM COMPUTER'S ±12VDC, +5VDC POWER SUPPLY
- ACCEPTS LOW LEVEL INPUTS
- EASY TO PROGRAM

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DESCRIPTION

The MP7218 is an analog input microperipheral board designed to be used with Motorola's Micromodule and EXORciser®microcomputer systems. It is electrically and mechanically compatible with these systems. The analog system is contained on a single printed circuit board that is treated as memory by the CPU. The analog interface is at a connector on the opposite edge of the board from the bus connector.

This data acquisition system includes 25V input overvoltage protection, an analog multiplexer, high gain instrumentation amplifier, and 12 bit A/D converter along with all the necessary timing, decoding and control logic. The unit operates from the microcomputer's +5VDC and ±12VDC power supplies. The MP7218 is capable of interfacing ±10mV to ±5V signal levels.

When programming with this peripheral, it is treated as memory. The A/D converter output is a 12 bit word so two 8 bit memory locations are needed for each channel. Address bits A15-A5 select the board and A4-A1 select the analog input channel to be digitized. To start a conversion the board is written to using an STA or similar instruction. After conversion data remains in the output latches waiting to be read until another conversion is initiated. This unit may be used with or without halting the CPU or in the interrupt mode.

The MP7218 is jumpered at the factory with the first channel at address $93E0_{16}$, the second at $93E2_{16}$, etc. By changing jumpers, the boards may be placed anywhere in memory.

SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT	MP7218
Number of analog inputs	8 differental/16 single-ended[1]
Input range	±10mV to ±5V[2]
ADC gain ranges (strap selectable)	0 to 5V ±5V, ±2.5V
Amplifier gain range	1 to 1000
Factory set gain	1
Amplifier gain equation (resistor programmable)	$G = 1 + 20k\Omega/R_{EXT}$
Input overvoltage protection	±25V
Input impedance, DC	100 megohms
Bias current 25°C 0 to 70°C	 20nA 50nA
Amplifier output noise (Gain = 100 R_S = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage, max	400μV
Amplifier input offset voltage drift, max	(2 + 20/G)μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy, (±5V range, max) ±10mV range	±0.025% FSR[3] ±0.1% FSR
Temperature coefficient of accuracy range, max ±5V ±10mV range	 ±0.004% FSR/°C ±0.01% FSR/°C
Conversion time ±5V range ±10mV range	50 microseconds 100 microseconds
CMRR (for differential inputs)	90dB (DC to 60 Hz)
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer bus	
Output coding	Bipolar, two's complement[4]
Logic loading (all inputs)	One LSTTL load
Data bus output drive	20 TTL loads
HALT, $\overline{IRQ}$, $\overline{NMI}$ output drive	10 TTL loads
POWER REQUIREMENTS	
Power supply voltages	+5VDC at 100mA, +12VDC at 50mA -12VDC at 75mA
Range for rated accuracy	4.75V to 5.25V and ±11.4V to ±12.6V
TEMPERATURE RANGE	
Temperature	0°C to 70°C

(1) Connected at the factory as 8 channels differential.
(2) Connected at the factory for ±5V range.
(3) FSR is Full Scale Range (i.e., 10V for ±5V range, 5V for 0 to +5V range).
(4) Straight binary jumper selectable. (W80, W81)

MECHANICAL CHARACTERISTICS

Compatible with EXORciser and Micromodule card spacing.

Minimum card spacing: 12.7mm (0.5″)

Microcomputer bus connector required: 86 pin PC edge connector with 0.156″ contact centers (SAE-43D/1-2).

Analog connector: 50 pin PC edge connector with 0.100″ contact centers. Burr-Brown part number: 2250MC (Viking # 3VH25/1JN5 - solder tab). Scotchflex cable connector also available from 3M (# 3415-0001).

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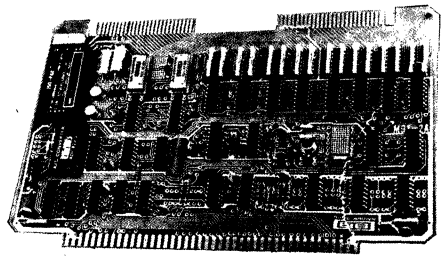
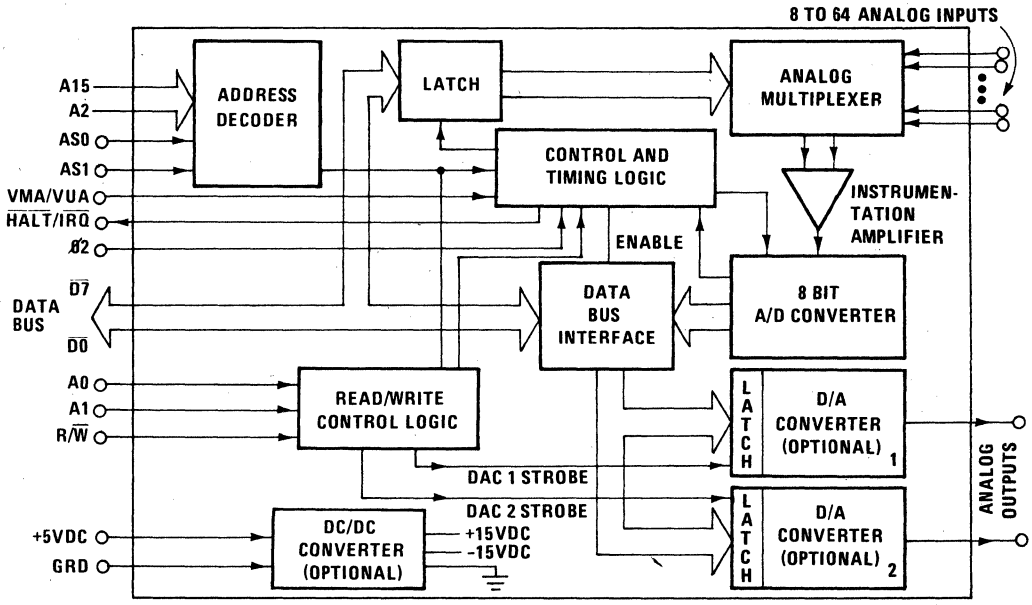


MP7408
MP7432

MICROCOMPUTER ANALOG I/O SYSTEM

A LOW-COST 64-CHANNEL ANALOG INPUT/2 CHANNEL ANALOG OUTPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® SYSTEMS



FEATURES

- EASY TO PROGRAM
  Systems are treated as memory
- REDUCES SYSTEM DEVELOPMENT TIME
- EASY TO USE
  8 to 64 input channels on one board
  Analog input and output on one board
  High level or low level inputs
- 70°C BURN-IN

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

This microcomputer peripheral provides two functions that interface directly to Motorola's Micromodule and EXORciser microcomputers. The functions are: (1) Analog Data Acquisition and (2) Analog Output. Both analog input and output systems are contained on a single printed circuit board that is treated as memory input or output by the CPU. The analog interface is at connectors on the opposite edge of the board from the bus connector.

The Data Acquisition System is available with up to 32 channels differential (64 channels single-ended) on one board. It includes an input multiplexer, high gain instrumentation amplifier, 8-bit A/D converter along with all the necessary timing, decoding and control logic. This system can digitize low level or high level analog signals. The gain of the internal instrumentation amplifier can be programmed with a single external resistor to allow input signal ranges as low as ±2.5mV. This means that the MP7400 can be connected to low level sensors such as thermocouples and strain gauges without external signal amplification. A DC/DC converter (+5V to ±15V) is also available so that only the computer's power supply is required. The Data Acquisition System is available with two optional 8-bit D/A converters to provide analog output in addition to input on the same board.

THEORY OF OPERATION

When programming these peripherals, they are treated as memory locations. Any memory reference instruction can be used. Two memory locations are used by the analog input system. One location is used to select the channel and start conversion. The same location provides status information when read. The other location contains the converted data. The analog output system also uses two memory locations, one for each channel.

Because these units are treated as memory, a minimum of instructions are needed to read an input channel or to set the output of a D/A converter. The MP7400's versatile memory mapped operation allows it to be used with or without halting the CPU or in the interrupt mode.

All of these units are jumpered at the factory for address 95F0 through 95F3.

SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT/OUTPUT SYSTEM	
ANALOG INPUT	
Number of analog inputs	
8 differential (16 signal-ended)[5]	MP7408
32 differential (64 single-ended)[6]	MP7432
Input voltage range[1]	±5mV to ±5V
ADC gain ranges[1]	±10V, 0 to 10V 0 to 5V
(strap selectable)	±5V, ±2.5V
Amplifier gain range[1]	1 to 1000
(resistor programmable)	
Amplifier gain equation	$G = 100k\Omega / R_{EXT}$
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C (max)	+300nA
0°C to 70°C	-2nA °C
Amplifier input offset voltage drift	$\pm\left(5 + \frac{1000}{G}\right)$ μV/°C
ANALOG INPUT TRANSFER CHARACTERISTICS	
Resolution	8 bit binary
Throughput accuracy ±5V range (max)	±0.4% FSR[2]
Throughput accuracy ±10mV range	±0.5% FSR
Temperature coefficient of accuracy	
±5V range (max)	±0.02% FSR/°C
±10mV range	±0.07% FSR/°C
Conversion time ±5V range (max)	44 microseconds
Conversion time ±10mV range (max)	84 microseocnds
CMRR (for differential inputs)[3]	66 dB (Gain = 2)
	86 dB (Gain = 100)
ANALOG OUTPUT	
Number of analog outputs	2
Output voltage range[4]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time (max)	< 5 microseconds
ANALOG OUTPUT TRANSFER CHARACTERISTICS	
Resolution	8 bit binary
Throughput accuracy (max)	±0.4% FSR
Temperature coefficient of accuracy	
Unipolar	±0.005% FSR/°C
Bipolar	±0.01% FSR °C
DIGITAL INPUT/OUTPUT	
All signals are compatible with Motorola Microcomputer Bus	
Output coding	Bipolar, two's complement; Unipolar, straight binary
An analog input channel is selected by:	$\overline{D0}$ through $\overline{D5}$
An analog output channel is selected by:	A0
The input/output data bits are read through:	$\overline{D0}$ through $\overline{D7}$
POWER REQUIREMENTS	
MP7408, MP7432	+5VDC +5% at 1 amp
MP7408-NS, MP7432-NS	+5VDC ±5% at 500mA +15VDC ±5% at 40mA -15VDC ±5% at 40mA
With analog output	
MP7408-AO, MP7432-AO	+5VDC ±5% at 2 amp
MP7408-NS-AO, MP7432-NS-AO	+5VDC ±5% at 500mA +15VDC ±5% at 100mA -15VDC ±5% at 100mA
TEMPERATURE RANGE	0°C to 70°C

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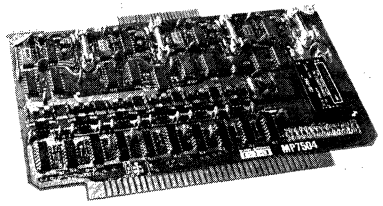
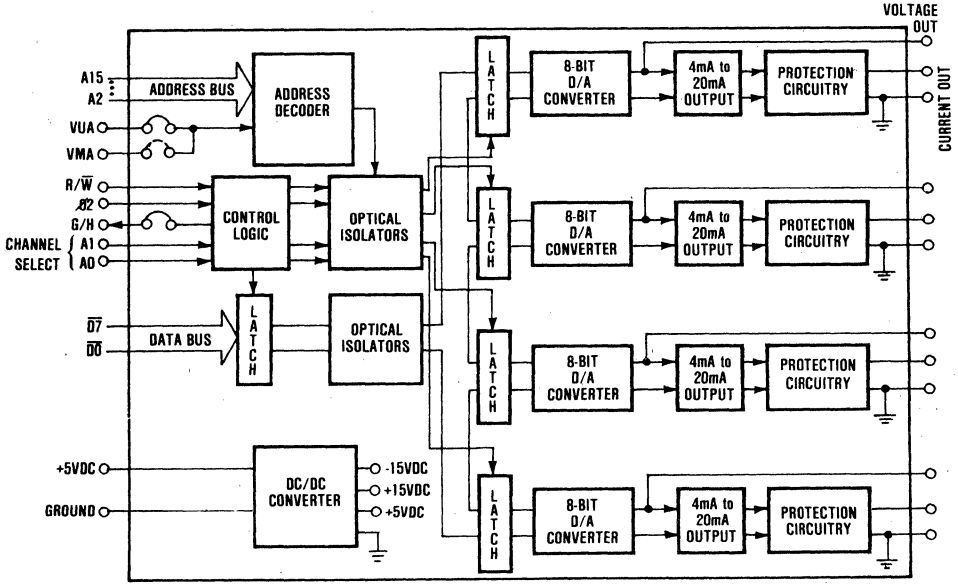


MP7504

MICROCOMPUTER ANALOG OUTPUT SYSTEM

A 4-CHANNEL, 8-BIT ISOLATED ANALOG OUTPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® MICROCOMPUTERS



FEATURES

- OUTPUT ISOLATION/OUTPUT PROTECTION
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Operates from computer power supply
  - Easy to program
- COMPATIBLE WITH ROCKWELL SYSTEM 65
- MOTOROLA MICROMODULE AND EXORciser COMPATIBLE
- 4-CHANNEL ANALOG OUTPUT SYSTEM
- 4mA TO 20mA OUTPUT
- 70°C BURN-IN

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

This microcomputer peripheral, burned in at 70°C to increase reliability and reduce aging shift, provides four optically-isolated 8-bit fused analog outputs that interface directly with Motorola's Micromodule and EXORciser microcomputers. The MP7504, electrically and mechanically compatible with these MPU's, is contained on a single printed circuit board that operates from the computer's +5 VDC power supply. Analog interface is through a card edge (direct) connector located on the opposite edge of the board from the bus connector.

The MP7504 which outputs 4mA to 20mA and 0-10V on each channel is programmed as memory locations. The address block used by each peripheral is selectable and can be placed anywhere in memory. A single instruction sets the input of a D/A converter.

ELECTRICAL SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

MODEL	MP7504
ANALOG OUTPUT	
Number of analog outputs	4
Output current range	4mA to 20mA
Maximum load	400Ω
Compliance	8V
Output settling time	50μsec
Output voltage range	0-10V at 5mA
Output impedance	1Ω
Output settling time	30μsec
TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
One LSB (voltage)	39.1mV
One LSB (current)	62.5μA
Throughput accuracy, max	±0.4% of FSR
Temperature coefficient of accuracy	
Voltage output	±50ppm of FSR/°C
Current output	±150ppm of FSR/°C
ISOLATION	
Isolation voltage between microcomputer bus and outputs	600VDC
DIGITAL INPUT/OUTPUT	
All signals compatible with microcomputer bus	
Logic loading (all inputs)	One LSTTL load
Analog output channels selected by:	A0, A1
Input data read by:	$\overline{D0}$-$\overline{D7}$
POWER REQUIREMENTS	
Rated voltage	+5VDC
Range for rated accuracy	4.75VDC to 5.25VDC
Supply drain at 5VDC	1.2A, typical; 1.8A max
TEMPERATURE RANGE	
Operating	0°C to 70°C

MECHANICAL

Compatible with Micromodule and EXORciser card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Analog Connector: 50-pin output P.C.B. edge connector. A mating connector is available from Burr-Brown:

2250MC (Viking # 3 VH25/1JN5, solder tab).

A Scotchflex connector (3415-0001) is available from 3M.

OPERATING INSTRUCTIONS

PROGRAMMING

Because this analog output board is treated as memory, programming is simple. The MP7504 uses any memory reference instruction that can write data from the CPU.

Each board is factory set for a block of addresses beginning at 94FC. Each analog data channel requires one memory location. When a data word is written to the MP7504 it is stored in an input latch. The optical isolators following the input latch require 15 microseconds to transfer new data to the D/A converter latches. Do not write to the board during this transmission period. To insure proper operation, use one of these modes:

1) HALT mode (shipped in this mode):

Jumper W33 is installed. The conversion command (write instruction) is followed with a NOP instruction. In this mode, the board halts the processor during data transfer sequences. For example:

```
STAA 94FE   Transfers data in accumulator to
            MP7504 for channel 2.
NOP         Allows MP7504 to halt processor for 15
            microseconds during transfer of data to
            channel 2.
```

2) COUNT DOWN mode

Jumper W33 is removed. Software control does not permit the program to write to the board for 15 microseconds. For example:

```
STAA 94FE   Transfers data in accumulator to
            MP7504 for channel 2.
 :          { System software does not allow another
 :          { write to the MP7504 for 15 microseconds.
```

CHANNEL	FACTORY SET LOCATION
0	94FC
1	94FD
2	94FE
3	94FF

TABLE I. Analog Output Channel Locations.

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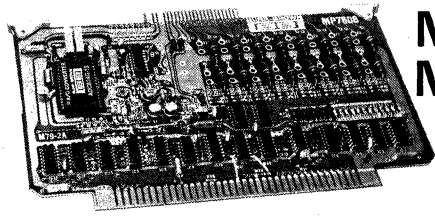
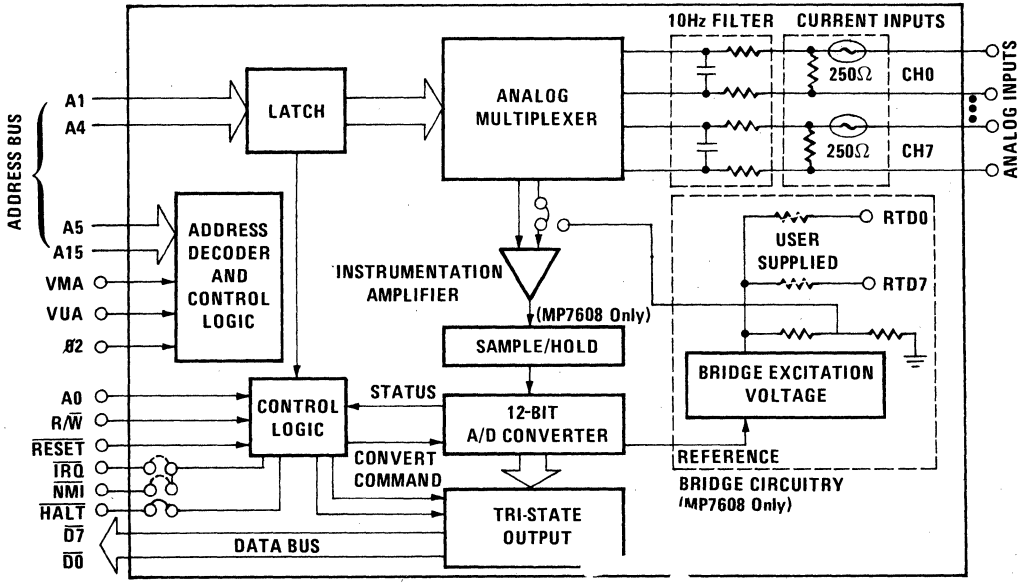


MP7608
MP7608-I

MICROCOMPUTER ANALOG INPUT SYSTEMS

A 12-BIT, 8-CHANNEL "INDUSTRIAL" ANALOG INPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® MICROCOMPUTERS



FEATURES

- CURRENT-LOOP INPUTS
- HIGH OR LOW LEVEL VOLTAGE INPUTS
- INPUTS PROTECTED TO 200VDC
- CURRENT INPUTS FUSED
- IMMUNE TO NOISE
  Input filter on each channel
  Differential inputs
- BRIDGE INPUTS
- 70°C BURN-IN

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

The MP7608 and MP7608-I are analog input microperipheral boards designed to be used with Motorola's Micromodule and EXORciser microcomputer systems. They are electrically and mechanically compatible with Motorola microcomputers. Each analog system is contained on a single printed circuit board that is treated as memory by the CPU. The analog interface for each system is at a connector at the opposite edge of the board from the bus connector.

These data acquisition systems include 200V input overvoltage protection, an input filter, analog multiplexer, high gain instrumentation amplifier, sample/hold and 12 bit A/D converter along with all the necessary timing, decoding and control logic. They operate from the microcomputer's +5VDC and ±12VDC power supplies.

The MP7608 is a voltage input system capable of interfacing ±10mV to ±5V signal levels. Excitation and bridge circuitry is also included on this board for interface to sensors, such as RTD's and strain gages. The MP7608-I is a current input system designed to interface to 4-20mA current loop signals. The MP7608-I also includes input fuses to protect the 250Ω precision input current resistors.

THEORY OF OPERATION

When programming with these peripherals, they are treated as memory locations. The A/D converter output is a 12 bit word so two 8 bit memory locations are needed for each channel. Address bits A15-A5 select the board and A4-A1 select the analog input channel to be digitized. To start a conversion the board is written to using an STA or similar instruction. The data remains in the output latches waiting to be read until another conversion is initiated. These peripherals may be used with or without halting the CPU or in the interrupt mode.

The MP7608/MP7608-I are jumpered at the factory with the first channel at address $93E0_{16}$, the second at $93E2_{16}$, etc. By changing jumpers, the boards may be placed anywhere in memory.

SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ELECTRICAL

ANALOG INPUT	MP7608-I	MP7608
Number of analog inputs	8 differential[1]	8 differential[1]
Input range	0-20mA[2]	±10mV to ±5V[3]
ADC gain ranges (strap selectable)	±10V, 0 to 10V, 0 to 5V ±5V, ±2.5V	±10V, 0 to 10V, 0 to 5V, ±5V, ±2.5V
Amplifier gain range	1 to 500	1 to 500
Factory set gain	1	1[5]
Amplifier gain equation (resistor programmable)	$G = 1 + 20k\Omega/R_{EXT}$	$G = 1 + 20k\Omega/R_{EXT}$
Input overvoltage protection	±200V	±200V
Input filter	One pole RC, 10Hz	One pole RC, 10Hz
Input impedance, DC	250Ω	100 megohms
Bias current		
25°C	20nA	7nA
0 to 70°C	50nA	10nA
Amplifier output noise (Gain = 100 R_X = 500Ω)	1.2mV rms; 7mV p-p	0.5mV rms; 3mV p-p
Amplifier input offset voltage, max	400μV	200μV
Amplifier input offset voltage drift, max	2 + 20/G μV/°C	1 + 20/G μV/°C
TRANSFER CHARACTERISTICS		
Resolution	12 bits binary	12 bits binary
Throughput accuracy,		
±5V or 0-20mA range, max	±0.025% FSR[4]	±0.025% FSR[4]
±10mV range	±0.1% FSR	±0.1% FSR
Temperature coefficient of accuracy		
±5V or 0-20mA range, max	±0.004% FSR/°C	±0.004% FSR/°C
±10mV range	±0.01% FSR/°C	±0.01% FSR/°C
Conversion time ±5V or 0-20mA range	60 microseconds	175 microseconds
±10mV range	125 microseconds	525 microseconds
CMRR (for differential inputs)	90dB (DC to 60Hz)	90dB (DC to 60Hz)
DIGITAL INPUT/OUTPUT		
All signals are compatible with Microcomputer bus		
Output coding	unipolar, straight binary	bipolar,[6] two's complement
Logic loading (all inputs)	one LSTTL load	one LSTTL load
Data bus output drive	20 TTL loads	20 TTL loads
$\overline{HALT}$, $\overline{IRQ}$, $\overline{NMI}$ output drive	10 TTL loads	10 TTL loads
POWER REQUIREMENTS		
Power supply voltages	+5VDC at 100mA, +12VDC at 50mA, -12VDC at 75mA	+5VDC at 100mA, +12VDC at 50mA, -12VDC at 75mA
Range for rated accuracy	4.75V to 5.25V and ±11.4V to ±12.6V	4.75V to 5.25V and ±11.4V to ±12.6V
TEMPERATURE RANGE		
Temperature	0 to 70°C	0 to 70°C

(1) May be connected as 16 channels single-ended without input filtering.
(2) May be set up to accept voltage signals.
(3) Connected at the factory for ±5V range.
(4) FSR is Full Scale Range (i.e., 10V for ±5V range, 5V for 0 to +5V range).
(5) Gains of 5 and 100 can be attained by adding jumpers.
(6) Unipolar straight binary is jumper selectable (W80, W81).

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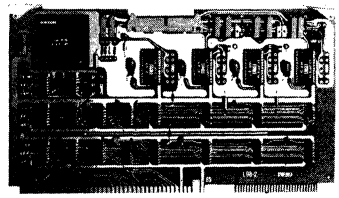


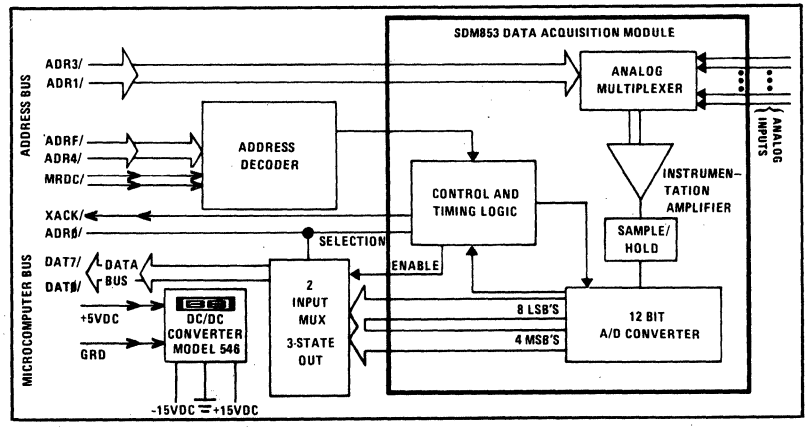
MP8304
MP8408
MP8416

MICROCOMPUTER ANALOG I/O SYSTEMS

INTEL - SBC80 and Intellec MDS Compatible
NATIONAL BLC80 Compatible
MP8304 - Analog Output System
MP8408 - Data Acquisition System
MP8416 - Data Acquisition System

FEATURES

- EASY TO PROGRAM
  Systems are treated as memory
- REDUCES SYSTEM DEVELOPMENT TIME
  System engineered and specified
  Operates from computer's +5VDC power supply if desired
- EASY TO USE
  All cabling and connectors are included



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

These microcomputer peripherals provide two much needed functions that interface directly to Intel's SBC80/10 and Intellec MDS microcomputers. The functions are: 1) Analog Data Acquisition and 2) Analog Output. The devices are electrically and mechanically compatible with any SBC80/10 and Intellec MDS. Each analog system is contained on a single printed circuit board that is treated as memory input or output by the CPU. The cards will mate to any memory or I/O slot. They are compatible with the 0.6" spacing of the SBC80/10 or the 0.75" spacing of the Intellec MDS. The analog interface for each system is at a flat cable connector at the opposite edge of the board from the bus connector.

The Data Acquisition systems consist of the MP8408, an 8 channel differential input system; and the MP8416, a 16 channel single-ended input system. Burr-Brown's SDM853 modular data acquisition system is used to implement these systems. The data acquisition systems include an input multiplexer, high gain instrumentation amplifier, sample/hold and 12 bit A/D converter along with all the necessary timing, decoding and control logic. The model 546 DC/DC converter (+5V to ±15V) is also used so that only the computer's +5VDC power supply is required.

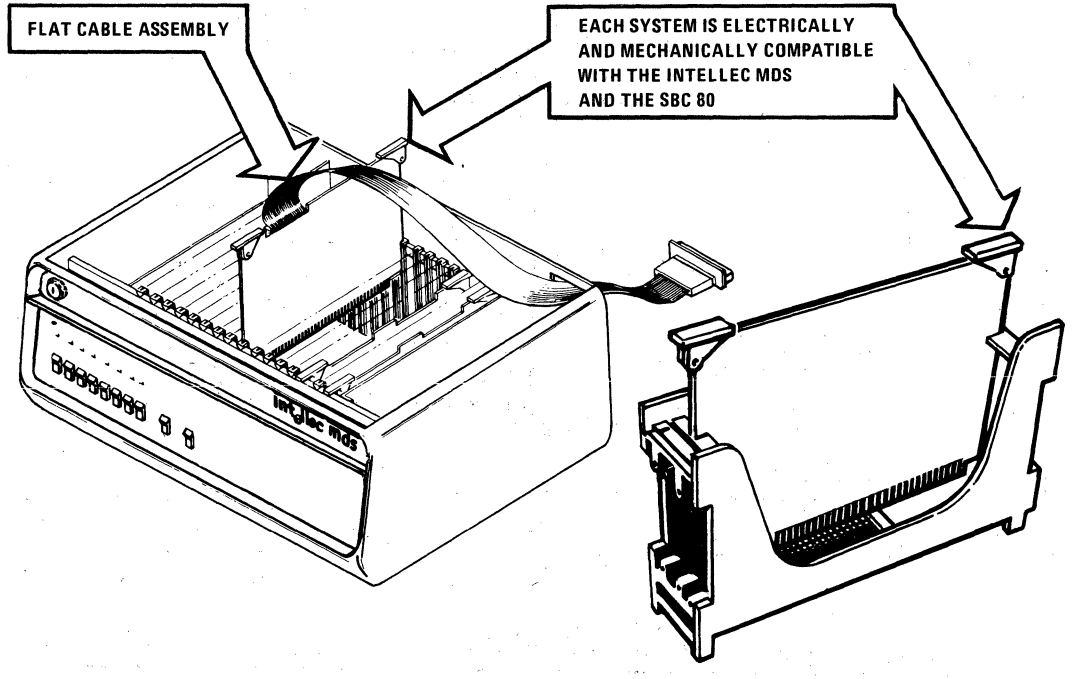
The MP8304, an analog output system, provides four analog output channels (using four of Burr-Brown's hybrid 12 bit DAC80 D/A converters). This board also contains the 546 DC/DC converter to assure operation on +5VDC power. The input of the D/A converters are double buffered so that a complete 12 bit word can be strobed into a D/A converter's input register to minimize output glitches. All of these systems are also offered in an OEM version without the DC/DC converter and cable.

THEORY OF OPERATION

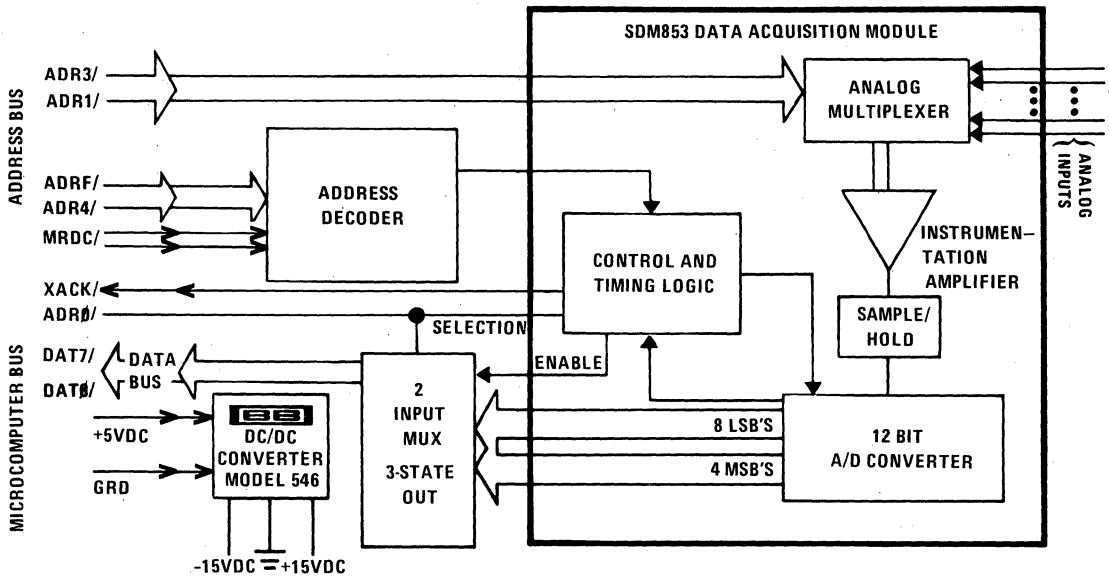
When programming with these peripherals, they are treated as memory locations. Both the A/D converter output and the D/A converter input are 12 bit words so two 8 bit memory locations are needed for each channel. But because the address block occupied by each peripheral is user selectable, it can be placed anywhere in memory. Existing memory can be overlapped since the peripherals inhibit all other memory that occupies the same memory locations.

Because these units are treated as memory, a single instruction is all that's needed to read an input channel or to set the input of a D/A converter. For instance, the LHLD (load) instruction followed by the proper address is used to read data from the MP8408 or MP8416. It will automatically select the desired channel, initiate conversion and when conversion is complete, transfer the A/D converter output for that channel to the 8080's H and L registers. The eight least significant bits are read first followed by the four most significant bits.

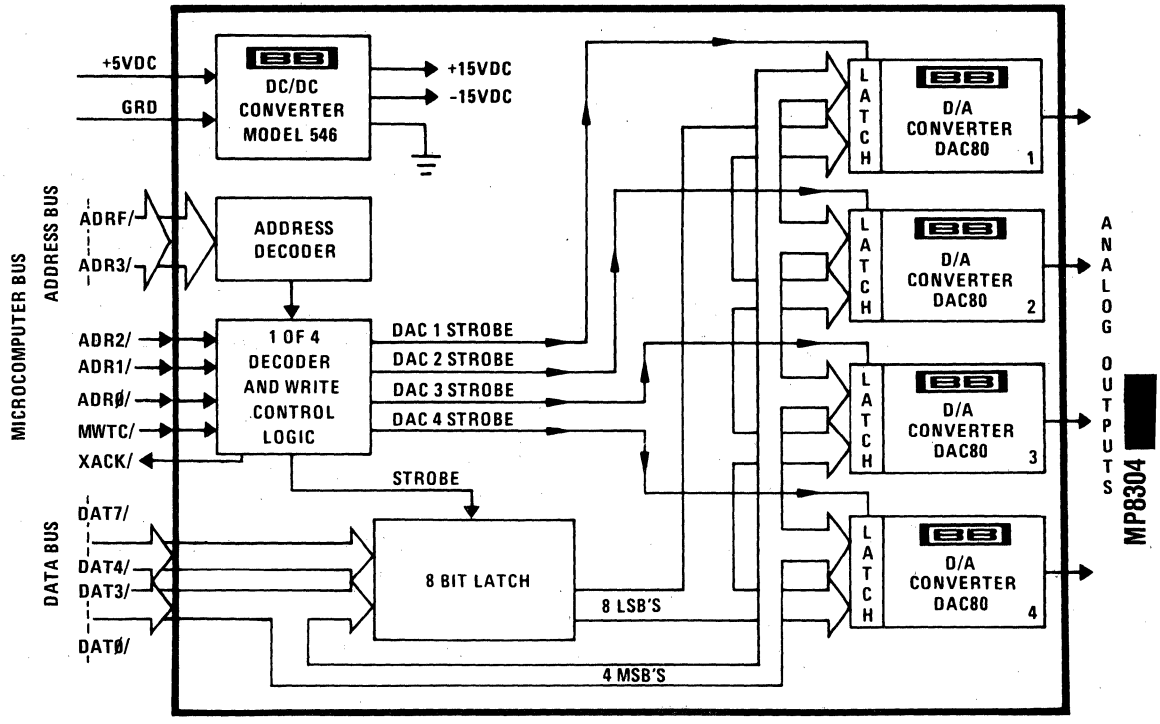
All of these systems are jumpered at the factory with the first channel at address $F720_{16}$. Each subsequent channel is two memory locations past the start of the last channel so that the second channel is at location $F722_{16}$.



ANALOG INPUT SYSTEM - MP8408/8416



ANALOG OUTPUT SYSTEM - MP8304



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT SYSTEMS	MP8408/MP8416
ANALOG INPUT	
Number of analog inputs	
8 differential	MP8408
16 single-ended	MP8416
Input voltage range[1]	±10mV to ±10V
Input current loop ranges (resistor programmable)	4-20mA 10-50mA, etc.
ADC gain ranges (strap selectable)	±10V, 0 to 10V, 0 to 5V ±5V, ±2.5V
Amplifier gain range (resistor programmable)	1 to 1000 V/V
Amplifier gain equation	$G = 1 + 20\ k\Omega / R_{EXT}$ (resistor programmable)
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C	20nA
0°C to 70°C	50nA
Amplifier output noise (Gain = 100 R_S = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage (max)[4]	400μV
Amplifier input offset voltage drift	$2 + \frac{20}{G}$ μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy ±10V range (max)	±0.025% FSR[2]
±10mV range	±0.1% FSR
Temperature coefficient of accuracy	
±10V range (max)	±0.003% FSR/°C
±10mV range	±0.01% FSR/°C
Conversion time ±10V range	33 microseconds
±10mV range	100 microseconds
CMRR (for differential inputs)	74 dB (DC to 2000 Hz)
Sample hold aperture time	30ns
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer bus	
Output coding	Bipolar, Two's Complement; unipolar, straight binary
An analog input channel is selected by:	ADR1 through ADR4
The output data bits are read into:[3]	DAT0 through DAT7
POWER REQUIREMENTS	
MP8408, MP8416	+5VDC ±5% at 1 amp, 25mV ripple
MP8417-NS, MP8409-NS	+5VDC ±5% at +500mA, 25mV ripple +15VDC ±3% at +50mA, 5mV ripple -15VDC ±3% at -75mA, 5mV ripple
TEMPERATURE RANGE	
Temperature range	0°C to 70°C

ANALOG OUTPUT SYSTEMS	MP8304
ANALOG OUTPUT	
Number of analog outputs	4
Output voltage range[1]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time	< 10 microseconds
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy (max)	±0.0125% FSR
Temperature coefficient of accuracy	
Unipolar	±0.003% FSR/°C
Bipolar	±0.0045% FSR/°C
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer bus	
An analog output channel is selected by:	ADR1/ and ADR2/
The input data bits are read by:	DAT0/ through DAT7/
POWER REQUIREMENTS	
MP8304	+5VDC ±5% at +1 amp, 25mV ripple
MP8305-NS	+5VDC ±5% at +1 amp, 25mV ripple +15VDC ±3% at +100mA, 5mV ripple -15VDC ±3% at -100mA, 5mV ripple
TEMPERATURE RANGE	
Temperature range	0°C to 70°C

OPERATING INSTRUCTIONS

INSTALLATION

The MP8304, MP8408 and the MP8416 are shipped from the factory calibrated and ready for immediate use. Installation requires only plugging the card into any empty slot in the computer and routing the board's mating I/O cable. Cable placement is shown on page 10-30. The cable supplied with each board is shielded and, in the case of the MP8304, provided with the proper termination.

PROGRAMMING

Programming of these analog I/O boards is easily accomplished since all are treated as memory locations. The MP8304 uses a single SHLD instruction to load any of its four digital to analog converters from the H and L registers. In a similar manner a channel in the MP8408 or MP8416 is read by a single LHLD instruction.

The voltage data for these boards is represented by a 12 bit two's complement binary number. Each bit has a value of 4.88mV, with the polarity of the voltage indicated by the sign of the binary number. Since the H and L register pair is 16 bits long and the data word is 12 bits, the MP8408 and MP8416 set these unused bits to the same value as the most significant bit of the data. This assures proper representation of the data's sign.

Each board is set at the factory for a block of addresses beginning at F720. Any analog data channel requires two memory locations since the digital data is 12 bits. The least significant 8 bits of data are always located in an even location while the remaining 4 bits are located in the next higher location. Thus, the first analog channel is located at F720 and F721 while the second analog channel is located at F722 and F723. These boards can occupy the same address space as memory since they inhibit memory whenever they become active.

MECHANICAL CHARACTERISTICS

Compatible with Intellec MDS and SBC-604/614 card spacing.

Minimum card spacing: 12.7mm (0.5")

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers.

40 pin analog connector (3M - 3432) provided on board. Mating connector (for OEM versions) is 3M - 3417. Recommended cable also by 3M; 3476/40.

(1) Connected at the factory for ±10V range.
(2) FSR is Full Scale Range (i.e., 20V for ±10V range, 10V for 0 to +10V range).
(3) The 4 MSB's when conversion is complete, followed by the 8 LSB's.
(4) Adjustable to zero.

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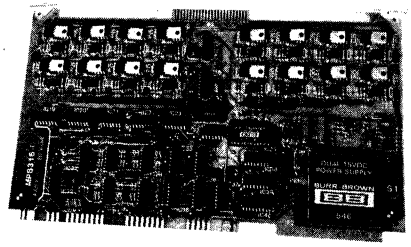


MP8316-I
MP8316-V

MICROCOMPUTER ANALOG OUTPUT SYSTEM

FEATURES

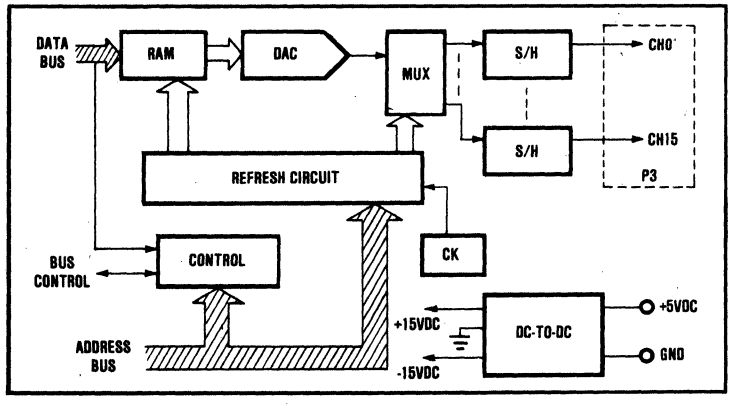
- 16 CHANNELS
- 0 - 24.57mA or ±10V OUTPUTS
- SINGLE GAIN AND OFFSET ADJUSTMENT
- MEMORY MAPPED or I/O OPERATION
- UP TO 20-BIT ADDRESS BUS
- 12-BIT RESOLUTION
- MULTIBUS™ COMPATIBLE

Multibus™ - Intel Corp.

DESCRIPTION

Dynamic analog outputs allow the MP8316 to provide high channel density on a single board. This approach frees system space for other peripherals and minimizes per channel power requirement. An on-board DC-to-DC converter powers the MP8316 from the system +5VDC supply. Channel data is stored in an on-board RAM and used by the refresh circuit to update outputs. Each channel is factory-adjusted to allow system calibration to be accomplished with a single gain and offset adjustment. Memory mapped or I/O operation is a jumper-programmable option on the board.

Two models of the MP8316 are available. Both models have 16 analog outputs and 12-bit resolution. The current output model (MP8316-I) will sink up to 24.57mA on each channel and is well suited for 4mA to 20mA operation. The voltage output model (MP8316-V) can be jumpered for bipolar or unipolar operation. Both units conform to Intel's Multibus™ specification.



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SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise specified.

MODEL	MP8316-I	MP8316-V
OUTPUTS		
Type	Current sink	Voltage
Number of Channels	16	16
Resolution	12-bit	12-bit
Range	0 to 24.57mA 10V min 80V max 1W max	±10V, ±5V, ±2.5V 0 to +10V 0 to +5V at 5mA max
ACCURACY		
Total Accuracy(1) max	±0.1% FSR(2)	±0.07% FSR
Offset Error	±1/2LSB (0.012%)	±1/2LSB (0.012%)
Linearity	±1/2LSB	±1/2LSB
Gain Error	0.1% FSR	0.05% FSR
Crosstalk	±1/2LSB	±1/2LSB
Temperature Coefficient	±50ppm/°C	±30ppm/°C
TIMING		
Refresh Scan Time	845µsec	845µsec
Charge Time per Scan	46.2µsec	46.2µsec
Settling Time		
to 0.1% of FSR	8.5msec	3.5msec
to 1/2LSB	11msec	5msec
DATA HOLD TIME ON BUS	200nsec	200nsec
BUS CONFIGURATION	Multibus ™	Multibus ™
POWER		
+5V ±5% (system bus)	1.5A	1.5A
ENVIRONMENT		
Operating Temperature	0°C to +70°C	
Relative Humidity	95% noncondensing	

NOTES:
1. With gain and offset error calibrated as described under Calibration, includes linearity error, channel-to-channel offset error, channel-to-channel gain error and crosstalk.
2. FSR is full scale range.

MECHANICAL

Compatible with Intellec MDS and iSBC-604/614 card spacing.
Minimum card spacing: 15.2mm (0.6").
Microcomputer bus connector required: 86-pin PC edge connector with 0.156" contact centers.
50-pin analog edge connector on board for analog outputs, 0.100" contact centers.
Mating connectors:
Burr-Brown 2250MC (Viking 3VH25/1JNS, solder tab).
3M Corporation 3415-0001 (Scothflex, for flat cable).

THEORY OF OPERATION

The dynamic output approach uses a single digital-to-analog converter (DAC) to drive all 16 outputs. Digital data for each channel is stored in an on-board RAM and analog output data for each channel is stored in separate sample/hold circuits. The refresh circuit contains a channel counter that selects the appropriate DAC input from RAM for the channel being updated and multiplexes the DAC output to the appropriate channel sample/hold. Thus, the output data is updated independent of the host CPU. The CPU changes data in RAM by a write operation to the appropriate channel. When this occurs, the refresh circuit disables the multiplexer to prevent output glitches and to allow the CPU to change the RAM data.

Table I describes the Multibus™ control signals used by the MP8316. The pinout of the bus connector (P1) conforms to the Multibus™ specifications. Control lines BPRN/ and BPRO/ are connected so that the MP8316 will not interfere with multiple processor operation when the serial priority technique is used. The auxiliary connector (P2) is not used.

TABLE I. Description of Control Lines.

Control Line	Description
INIT/	This signal resets the system.
INH 1/	Prevents RAM from responding.
INH 2/	Prevents ROM from responding.
MWTC/	Memory write command.
IOWC/	I/O write command.
XACK/	Slave acknowledge to host CPU that data has been taken from data bus for write operation or that valid data has been placed on the bus for read operation.
BPRN/	BUS PRIORITY IN - indicates that no higher priority module is requesting the bus.
BPRO/	BUS PRIORITY OUT - passed to BPRN/ input of the next lower priority module.

OPERATING INSTRUCTIONS

INSTALLATION

The MP8316 comes factory-adjusted and ready for use. Analog outputs are available on connector P3. Current outputs require an external current source (see Figure 1).

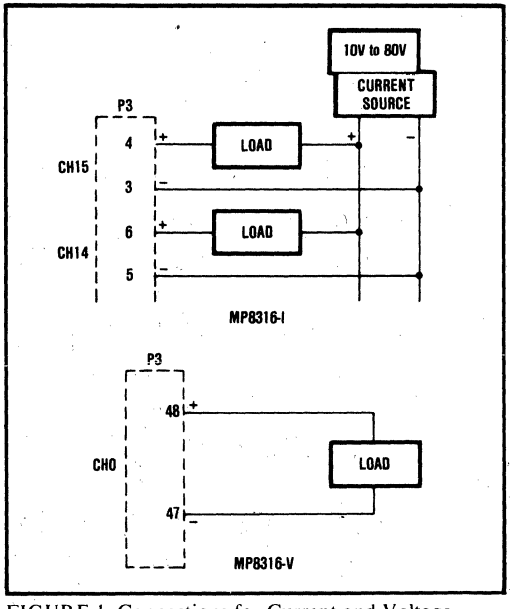

FIGURE 1. Connections for Current and Voltage Outputs.

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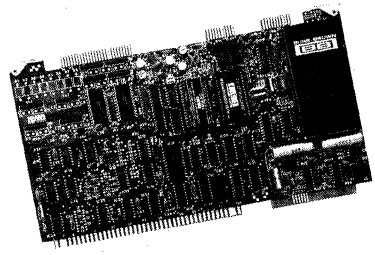


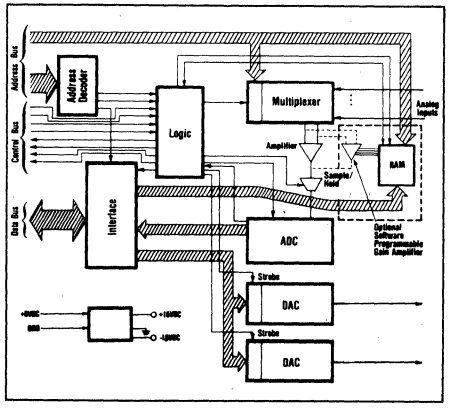
MP8418

MICROCOMPUTER ANALOG I/O SYSTEMS

A 31-CHANNEL ANALOG INPUT, 2-CHANNEL OUTPUT SYSTEM COMPATIBLE WITH INTEL SBC80, INTELLEC® MDS AND NATIONAL BLC-80 MICROCOMPUTERS

FEATURES

- HIGH AND LOW LEVEL INPUTS
- SOFTWARE PROGRAMMABLE GAIN (1 to 1024) AMPLIFIER OPTION
- ANALOG INPUT AND OUTPUT ON ONE BOARD
- EASILY PROGRAMMED
- MEMORY MAPPED
- LOW COST
- BURN-IN



DESCRIPTION

The MP8418 series of analog I/O peripherals are electrically and mechanically compatible with and interface directly to Intel's MULTIBUS® and other microcomputers of similar configuration. These analog systems are treated as memory by the CPU.

The analog input portion of the MP8418 includes: over-voltage protection to 26VDC; provision for up to eight 4mA to 20mA inputs; an analog multiplexer; resistor programmed instrument amplifier or, a software programmable amplifier (gain of 1 to 1024); sample/hold amplifier and; a 12-bit A/D converter. An optional analog output system is included on the same board. It consists of two 12-bit D/A converters with double buffered inputs to minimize glitches, and control logic.

MP8418 is a 15-channel differential (user strapable as 31 channel single-ended) analog input system. With one expander board the system can be expanded to 63 differential channels (strapable as 127 single-ended channels). Another input channel is grounded on the board so that it may be used as ground reference for automatic calibration.

Gains of 1 to 1024 are software selectable for the programmable amplifiers and the gain for each channel (up to 127 channels) may be stored in an on-board RAM if desired. The proper gain for each channel is then selected automatically by the MP8418.

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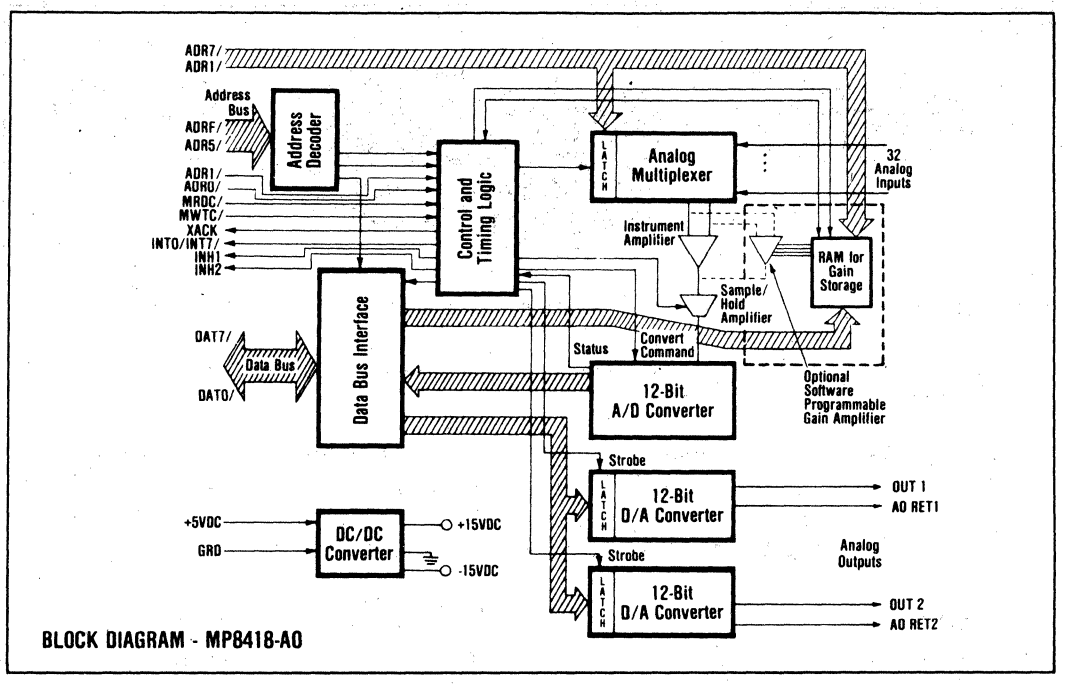

BLOCK DIAGRAM - MP8418-A0

MECHANICAL SPECIFICATIONS

Compatible with Intellec MDS and SBC-604/614 card spacing.

Minimum card spacing: 15.2mm (0.6").

Microcomputer bus connector required: 86-pin PC edge connector with 0.156" contact centers.

One 50-pin analog edge connector on board for analog inputs.
Mating connector available from Burr-Brown: 2250MC. (Viking #3VH25/1JN5, solder tab); from 3M: 3415-0001 (Scotchflex).

Two 20-pin analog edge connectors on board for analog outputs and analog input expansion.
Mating connector available from Burr-Brown: 2220MC. (Viking #3VH10/1JN5).

OPERATING INSTRUCTIONS

INSTALLATION

MP8418 is shipped from the factory calibrated and ready to use. Installation requires only plugging the card into any empty slot in the computer and wiring the analog connector.

PROGRAMMING

This peripheral is programmed as a memory location and any memory reference instruction can be used. Both the A/D converter output and D/A converter input are 12-bit words, therefore, two memory locations are needed for each channel. The address block occupied by each MP8418 is user selectable and can be placed anywhere in memory.

Because these peripherals are treated as memory, a minimum of instructions are needed to read an input channel, or to set the input of a D/A converter. For example: when the MP8418 is connected in the HALT mode, the LHLD (load) instruction followed by the proper address can be used to read data from an analog input channel. It will automatically select the desired channel, initiate conversion and when conversion is complete, transfer the A/D converter output to the 8080's H and L registers. The eight least significant bits (LSB's) of the data word are transferred to the CPU first followed by the four most significant bits (MSB's). The four MSB's are in data bus positions 0-3. A single SHLD instruction can be used to write data to one analog output channel. The eight LSB's are written first, followed by the four MSB's (in D0-D3). When the four MSB's are written to the board, all twelve bits of the data word are transferred simultaneously to the D/A converter input.

ADC/DAC Bit Placement

	D7	D6	D5	D4	D3	D2	D1	D0
Low Byte	B_3	B_2	B_1	B_0	B_1	B_2	B_3	B_0
High Byte	X	X	X	X	B_{11}	B_{10}	B_9	B_8

On MP8418's, with the software programmable gain amplifier, an on-board random access memory (RAM) may be used to store the gain for each channel. In this

mode, (Control Register D4 = 1), the proper gain is automatically selected from the RAM when a channel is converted. If the RAM is not used (Control Register D4 = 0), the amplifier gain must be written to an on-board register (Control Register D0-D3).

All these systems are jumpered at the factory with a base address of $F700_{16}$. Each subsequent channel is two memory locations past the start of the last channel, consequently channel one is at location $F702_{16}$, channel two is at location $F704_{16}$, etc.

The input system operates in several modes:

INTERRUPT MODE: A read instruction to the board (ADR0 = 0) starts the conversion. An interrupt is generated at the end of the conversion. The interrupt can be connected to any of eight vector locations and may also be disabled by software. Control Register D6 = 1 enables interrupt for interrupt mode.

POLLING MODE: A read to the board starts the conversion. The interrupt is disabled by software and the CPU may then read the status word to determine when conversion is complete. Control Register D6 = 0 disables interrupt for polling mode.

HALT MODE: a read instruction to the board starts the conversion. The MP8418 halts the CPU until conversion is complete, at which point the data is transferred to the CPU. Only one instruction is needed to start conversion and to transfer data to the CPU (an LHLD or POP referenced to the channel's LSB's can be used).

CONTINUOUS MODE: A read instruction to the board starts the conversion. The CPU is not halted, but reads the status of the MP8418 to determine when conversion is complete (Control Register D6 = 0) - or the CPU waits for an interrupt (Control Register D6 = 1). When conversion is complete, the CPU reads the data. The read instruction is addressed to the next channel to be converted. The data from the last conversion is thus transferred to the CPU and conversion is started for the next channel.

EXTERNAL TRIGGER: This mode allows a conversion to be started independent of the CPU. A read instruction is required to set the proper channel. Once the board has been set, a low to high transition of the EXTERNAL TRIGGER input (P5, pin 20) will start conversion. End of conversion can be detected by polling or interrupt technique. Data is obtained by any read command. The external trigger will start conversion independent of other board functions. The busy input (P5, pin 19) goes high at the start of conversion and goes low when the MSB of the converted data is read by CPU.

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG INPUT SECTION	MP8418
INPUT CHARACTERISTICS	
Number of Channels	31 single-ended, 15 differential
ADC Gain Ranges (Jumper Selectable)[1]	0 to 5V, 0 to 10V, ±2.5V, ±5V, ±10V
Amplifier Gain Ranges	
Resistor Programmable[2]/Software Programmable	1 to 1000/1 to 1024
Maximum Input Voltage Without Damage[3]	±26 volts
Input Impedance	100MΩ, 10pF OFF Channel
	100MΩ, 100pF ON Channel
Bias Current (25°C)	±20nA
Bias Current (0 to 70°C)	±50nA
Differential Bias Current	±10nA
Amplifier Input Offset Voltage G = 1000	
Resistor Programmable/Software Programmable	±400μV, ±4μV
Amplifier Input Offset Voltage Drift G = 1000	
Resistor Programmable/Software Programmable	±2μV/°C, ±1μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Throughput Time (max) G = 1	
Resistor Programmable/Software Programmable	38μsec, 350μsec
Throughput Time G = 1024	
Resistor Programmable/Software Programmable	100μsec, 350μsec
ACCURACY	
System Accuracy at +25°C (max)[4] G = 1	±0.0325% FSR[5]
System Accuracy at +25°C[4] G = 1024	
Resistor Programmable/Software Programmable	±0.1% FSR, ±0.05% FSR (max)
Linearity	±1 2LSB
Differential Linearity	±1 2LSB
Quantizing Error	±1 2LSB
Gain Error	Adjustable to Zero[6]
Offset Error	Adjustable to Zero
Monotonicity[7]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE (Bipolar)[8]	
System Accuracy Drift (max) G = 1	±45ppm of FSR °C
System Accuracy Drift G = 1024	±100ppm of FSR, °C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time	125nsec
Aperture Time Uncertainty	±5nsec
Differential Amplifier CMRR G = 1	86dB (DC to 60Hz)
Channel Crosstalk	80dB down at 1kHz, for OFF Channel to ON Channel
ANALOG OUTPUT SECTION (AO option)	
OUTPUT CHARACTERISTICS	
Number of Channels	2
Output Voltage Ranges (Strap Selectable)	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA
Output Impedance	1Ω
Short Circuit Protection	Yes
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Output Settling Time (max)	10μsec
ACCURACY	
Output Accuracy	±0.0125% FSR
Temperature Coefficient of Accuracy	±30ppm of FSR °C
POWER REQUIREMENTS	
MP8418, MP8418-PGA	+5V ±5% at 1.2A
MP8418-AO, MP8418-PGA-AO	+5V ±5% at 2.0A
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Relative Humidity	95% noncondensing

NOTES:
1. Factory set for ±10V range.
2. Factory set for Gain = 1.
3. With power off. ±36 volts with power on.
4. Includes linearity errors with gain and offset errors adjusted to zero.
5. FSR means Full Scale Range.
6. When any one gain range is adjusted to zero gain error, the gain error for any other range is less than ±0.02% when using the software programmable amplifier.
7. No missing codes guaranteed.
8. Includes offset drift, gain drift and linearity drift.

FACTORY MODE CONNECTIONS	
MODEL	FACTORY SET MODE
MP8418	HALT
MP8418-AO	HALT
MP8418-PGA	POLLING INTERRUPT*
MP8418-PGA-AO	POLLING INTERRUPT*

Note: Any model can be connected in any mode.
*Int 1 Factory Set

TABLE I. Programming Mode Connections.

JUMPER REQUIRED	
Halt Mode	JP17, JP29, JP30, JP81
Polling and Interrupt Mode	JP17, JP29, JP81
Continuous Mode	JP17, JP31, JP82
External Trigger Mode	JP16, JP29, JP81

TABLE II. Mode Selection Jumpers.

JUMPERS REQUIRED FOR INTERRUPT VECTOR	
INT0	JP70
INT1	JP71
INT2	JP72
INT3	JP73
INT4	JP74
INT5	JP75
INT6	JP76
INT7	JP77

TABLE III. Interrupt Selection.

MEMORY MAP

Factory Set	ADR7 ... ADR0		READ		WRITE	
F700	0000 0000	CH0	8LSB's of offset		N/A	GAIN 0*
F701	0000 0001	IN	STATUS		CONTROL	
F702	0000 0010	CH1	LSB		N/A	GAIN 1*
F703	0000 0011	IN	MSB		N/A	
F704	0000 0100	CH2	LSB	CH0 OUT	LSB	GAIN 2*
F705	0000 0101	IN	MSB	or GAIN	MSB	
F706	0000 0110	CH3	LSB	CH1 OUT	LSB	GAIN 3*
F707	0000 0111	IN	MSB	or GAIN	MSB	
F708	0000 1000	CH4	LSB		N/A	GAIN 4*
F709	0000 1001	IN	MSB		N/A	
			⋮		⋮	
F71E	0001 1110	CH15	LSB		N/A	GAIN 15*
F71F	0001 1111	IN	MSB		N/A	
F710	0001 0000	CH16	LSB		N/A	GAIN 16*
F711	0001 0001	IN	MSB		N/A	
			⋮		⋮	

N/A - Not used.

*Used only on PGA versions when RAM gain storage is used.

A read instruction (other than a STATUS REGISTER read) should not be made to the board during a conversion. Contact factory for more details.

STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
Convert Complete	Interrupt Enable	Write* Enable	RAM* Enable	--------	GAIN X*	----------	

*Used only on versions with software programmable amplifier.

Convert Complete - The bit is low during conversion. It goes high on completion of conversion and remains high until the MSB of a data word is read.

Interrupt enable: status of interrupt enable
Write enable: status of write enable
RAM enable: status of RAM enable
GAIN X: current value stored in PGA GAIN control register.

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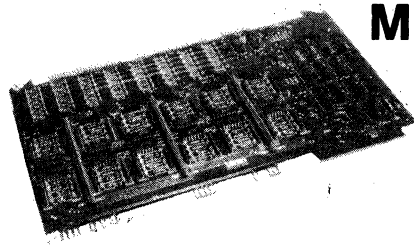


MP8418-EXP

MICROCOMPUTER ANALOG INPUT EXPANDER FOR MP8418

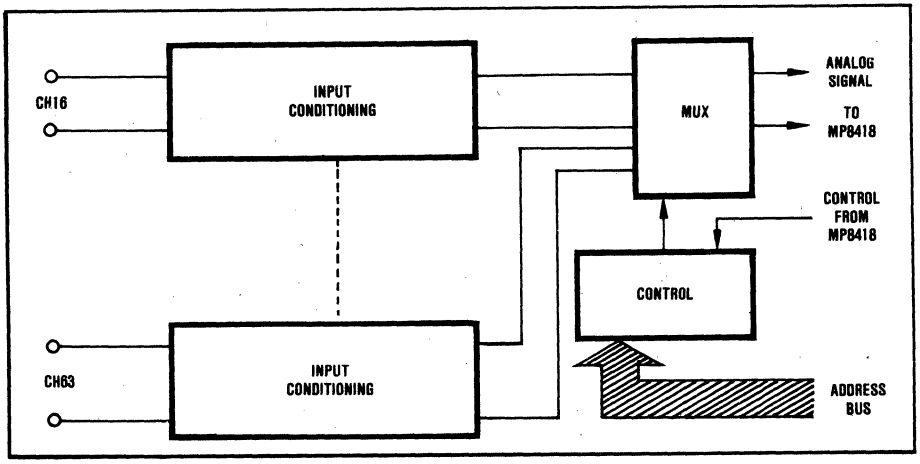
FEATURES

- 48 DIFFERENTIAL CHANNELS/ 96 SINGLE-ENDED CHANNELS
- SOLID STATE MULTIPLEXING
- 26V OVERVOLTAGE PROTECTION WITH DIODE CLAMPS
- MULTIBUS™ COMPATIBLE

Multibus™ - Intel Corp.

DESCRIPTION

MP8418-EXP is a bank of multiplexers that expand the analog input channel capacity of the MP8418 series microperipheral. Differential input capability is expanded from 15 channels to 63 channels. Single-ended capability is expanded from 31 channels to 127 channels. Control signals and power are passed to the expander from the MP8418. The analog input signal is passed to the MP8418 from the expander. Multiplexer channel addresses are latched on the expander board. The expander occupies the memory space immediately above the MP8418. Gain, data conversion, and bus interface are performed by the MP8418. Channel gains can be stored in a RAM on the PGA versions.



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SPECIFICATIONS

ELECTRICAL

Inputs	48 differential 96 single-ended
Input Protection	26V
Power +5V +15V -15V	110mA (from system bus) 30mA (from MP8418) 20mA (from MP8418)

See MP8418 Specifications for all other input characteristics.

MECHANICAL

Compatible with Intellec MDS and iSBC-604/614 card spacing.
Minimum card spacing: 15.2mm (0.6").
Microcomputer bus connector required: 86-pin PC edge connector with 0.156" contact centers.
Two 50-pin analog edge connectors on board for analog inputs.
Mating connectors:
Burr-Brown 2250MC (Viking #VH25/1JN5), solder tab;
3M Corporation: 3415-0001 (Scotchflex).
Interface Cable: 20-conductor ribbon cable with a card edge connector mass terminated on each end, available from Burr-Brown:
MP8005, 1" long
SM50123-001, 9.5" long

INTERFACE CONNECTOR

Bottom		P5		Top
+15VDC	1		2	+15VDC
Analog GND	3		4	Analog GND
-15VDC	5		6	-15VDC
Dig GND	7		8	Addr. Out
Dig GND	9		10	EXP/
Dig GND	11		12	Dig GND
Analog GND	13		14	Analog GND
Analog GND	15		16	Analog GND
Analog GND	17		18	IA IN-
Analog GND	19		20	IA IN+

INSTALLATION

If possible, adjacent slots in the system should be used for the MP8418 and MP8418-EXP. This is particularly important for low level operation where longer cables introduce noise and offset errors. Analog inputs connect to P3 and P4. Connector P5 on the MP8418-EXP connects to P4 on the MP8418 to interface the two units (see Figure 1). Tables I and II show jumper configurations for the expander and additional jumper changes required on the MP8418.

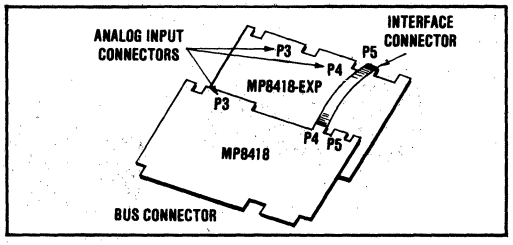

FIGURE 1. System Interface.

TABLE I. Jumper Requirements for Differential Operation.

	MP8418	MP8418-EXP
Install	JP44, 45 JP33, 36 JP66, 67, JP3, 4, 7	JP2 JP3
Remove	JP42, 39 JP2, 5	JP1

TABLE II. Jumper Requirements for Single-ended Operation.

	MP8418	MP8418-EXP
Install	JP44 JP33, 37 JP66, 67, 68 JP2, 5	JP1
Remove	JP39, 42, 43, 36, 45 JP3, 4, 7	JP2 JP3

INPUT NETWORK

The input network is shown in Figure 2. The switch shown represents two CMOS multiplexers in series. Input protection is provided by the series resistors and diode clamps. The clamps prevent the multiplexer inputs from exceeding the supply voltages. An optional resistor (R) allows the user to convert current inputs to voltage that can be detected by the MP8418. The optional capacitor (C) in combination with the input resistors form a low-pass filter. Low-leakage high-quality capacitors should be used to minimize errors. The optional resistor and capacitor are only useful for differential operation.

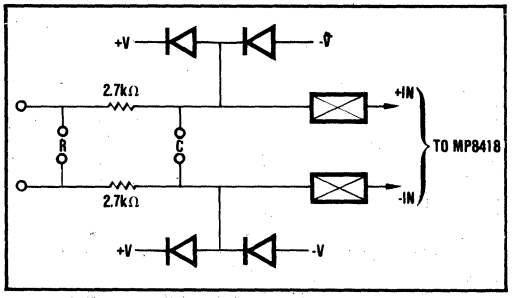

FIGURE 2. Analog Input Circuit.

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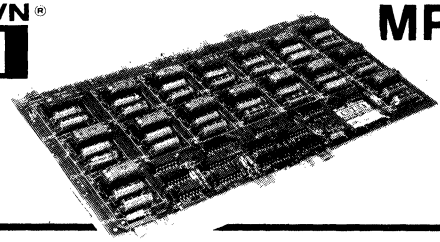
MP8418-ISOE



MICROCOMPUTER ISOLATED ANALOG INPUT EXPANDER FOR MP8418

FEATURES

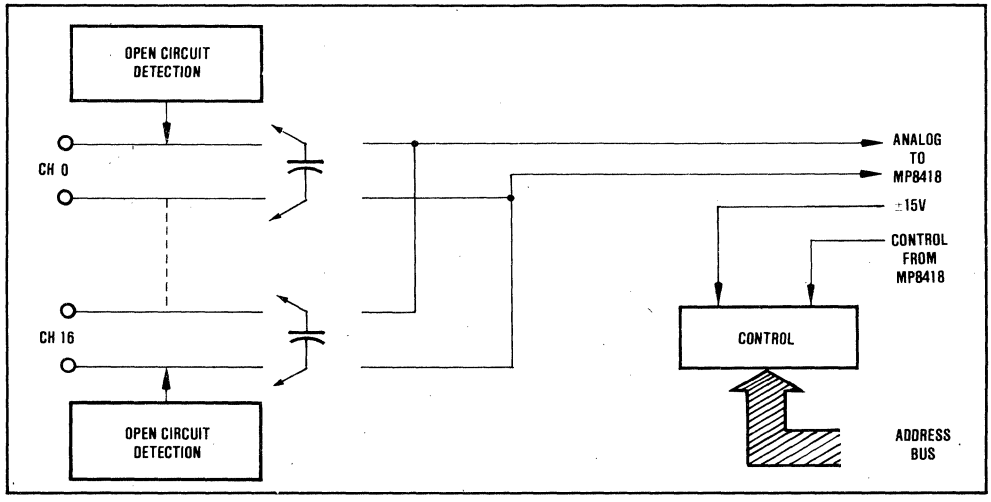
- 400V ISOLATION
- 16 CHANNEL FLYING CAPACITOR MULTIPLEXER
- 8Hz LOW-PASS FILTER
- MULTIBUS™
- LOW THERMAL EMF RELAYS

DESCRIPTION

The MP8418-ISOE expands the analog input capability of the MP8418 family of microcomputer boards from 15 channels to 31, 47 or 63 channels by using one, two or three MP8418-ISOE's. (Note: Only expander channels are isolated. The 15 channels on the MP8418 are standard CMOS multiplexed inputs.) A flying capacitor technique is used to provide 400V input and channel-to-channel isolation. Low thermal EMF relays minimize errors for low level operation. A low-pass input filter on each input provides 60Hz normal-mode rejection.

System interface, signal amplification, and data conversion are provided by the MP8418. Software options and analog signal ranges on the MP8418 are applicable to the MP8418-ISOE. Both boards conform to Intel's Multibus™ specifications.

Multibus™ - Intel Corp.



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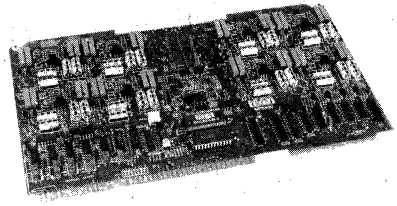


MP8430

MICROCOMPUTER RTD INPUT SYSTEM

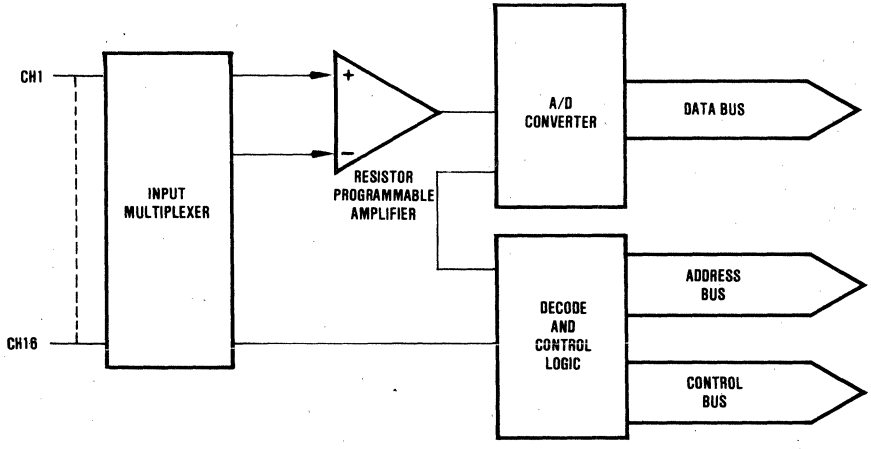
FEATURES

- 16 THREE-WIRE RTD INPUT CHANNELS
- SOLID-STATE MULTIPLEXING
- PROGRAMMABLE GAIN INSTRUMENT AMPLIFIER
- MULTIBUS™ COMPATIBLE (IEEE-796)
- MEMORY OR I/O MAPPED
- LINE LENGTH COMPENSATED

Multibus™-Intel Corporation

DESCRIPTION

The MP8430 is a multiplexed 16-channel RTD input digitizer. Each channel is line length compensated by an exciter circuit which may be calibrated to the device with balance and span adjustments. This circuit produces a voltage, proportional to the temperature of the RTD, which is filtered, multiplexed, amplified, and presented to a 12-bit analog-to-digital converter circuit. The converter in turn is interfaced to the microcomputer bus, thus providing a digital representation of the RTD temperature to the computer.



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SPECIFICATIONS

ELECTRICAL

Typical specifications at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	MP8430
INPUT	
Type	3-wire resistive temperature device (RTD)
Resolution	12-bit (one-part in 4096)
Zero (balance)	
Setting	100Ω
Range (25-turn)	0Ω to 200Ω
Excitation Current	
Setting (nominal)	0.7546mA
Range	0.73mA to 0.78mA
Gains Fixed	x31, x100
Gain Equation	$\frac{R107 + 25k\Omega}{R107}$
user set gain	
ADC Input Range	-5VDC to +5VDC
Maximum Line Resistance	4000Ω
1/2-loop resistance	
One-Pole Input Filter	0.33Hz
ACCURACY	
System Accuracy at +25°C	±0.10Ω
Temperature Drift	100ppm/°C
THROUGHPUT	
Throughput Time	85μsec
Settling Time	60μsec
Conversion Time	25μsec
BUS STRUCTURE	Multibus™ (IEEE-796)
POWER REQUIREMENTS	
+5VDC, ±5%	0.35 amp
+12VDC, ±5%	0.35 amp
-12VDC, ±5%	0.14 amp
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	95% noncondensing

INSTALLATION

MP8430 is shipped from the factory ready for use. Installation consists of setting the correct address, plugging the card into any empty slot in the Multibus computer, and wiring the RTD connector.

ADDRESSING

MP8430 may be operated either memory-mapped or I/O-mapped (jumper selected). The board occupies four bytes of address space and can be placed on any four byte boundary. Eight, 12, 16, or 20-bit memory or I/O mapping are selectable.

PROGRAMMING

MP8430 is programmed in either the polled-mode or interrupt-mode, the difference being that the status register must be read in the polled-mode to determine completion of a conversion, whereas the interrupt-mode signals completion of a conversion by setting an interrupt to the processor.

Interrupt-mode is enabled by writing a "1" to bit 'D6' in the Status register (base address + 1). The appropriate interrupt jumper (W31-W38) must also be installed on the board.

A conversion is initiated by writing a channel number to the Control register (base address). The channel number is a hexidecimal 0 through F to select one of 16-channels. During conversion, bit "D7" of the Status register will be a '1'. When the conversion is completed, this bit will return to '0' indicating that valid data is in the data registers.

Data is typically read first from the Data Low register (base address + 2), then from the Data High register (base address + 3). This can be done with a single "LHLD" instruction. Writing a '1' to bit 'D4' of the Status register will clear the interrupt if operating in the interrupt-mode.

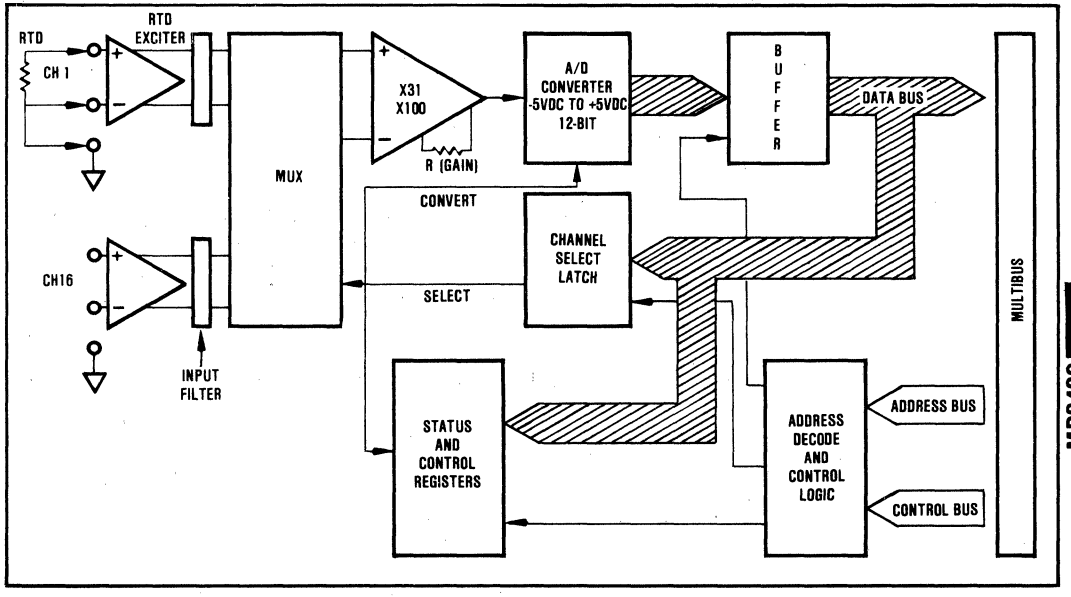

FIGURE 1. Block Diagram.

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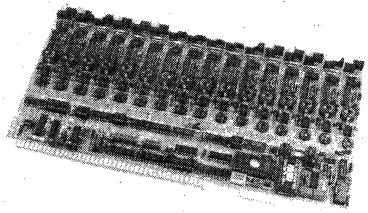


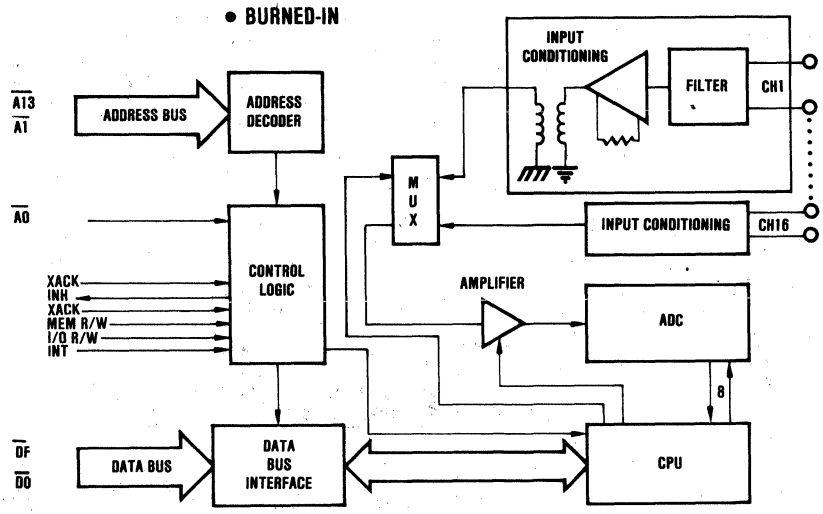
MP8450

MICROCOMPUTER ANALOG INPUT SYSTEMS

16-Channel Analog Input System Compatible with IEEE-796 (Multibus™)

FEATURES

- TRANSFORMER-ISOLATED INPUTS
- 1000V ISOLATION INPUT TO BUS
- 700V CHANNEL-TO-CHANNEL
- INPUT FILTER
- OPEN CIRCUIT DETECTION
- RESISTOR-PROGRAMMABLE-GAIN PER CHANNEL
- MEMORY OR I/O MAPPED
- REGISTER TRANSFER OF DATA
- 20-BIT ADDRESSABLE
- BURNED-IN



Multibus™ - Intel Corp.

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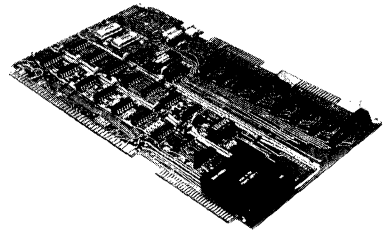
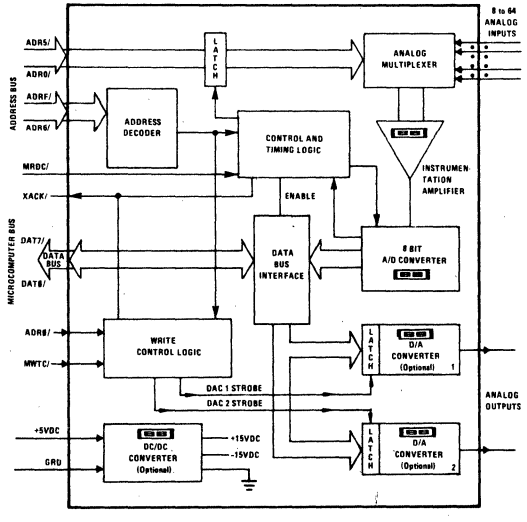


MP8608
MP8616
MP8632

MICROCOMPUTER ANALOG I/O SYSTEMS

FEATURES

- INTEL-SBC80 and INTELLEC MDS COMPATIBLE
- NATIONAL-BLC80 COMPATIBLE
- LOW COST
- 70°C BURN-IN
- EASY TO PROGRAM
  Systems are treated as memory
- REDUCES SYSTEM DEVELOPMENT TIME
  System engineered and specified
  Operates from computer's +5VDC
  power supply if desired
- EASY TO USE
  8 to 64 input channels on one board
  Analog input and output on one board



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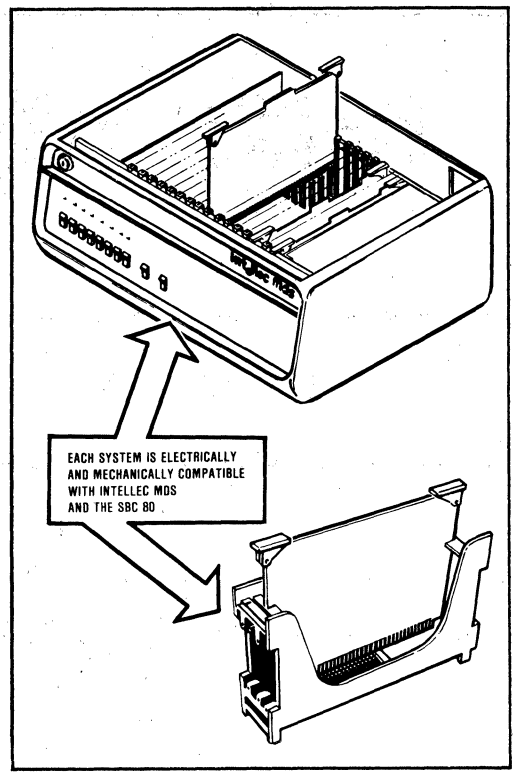
DESCRIPTION

These microcomputer peripherals provide two functions that interface directly to Intel's SBC80 and Intellec MDS microcomputers. The functions are: (1) Analog Data Acquisition and (2) Analog Output. The devices are electrically and mechanically compatible with any SBC80 and Intellec MDS. Both analog input and output systems are contained on a single printed circuit board that is treated as memory input or output by the CPU. The cards will mate to any memory or I/O slot. They are compatible with the 0.6" spacing of the SBC80 or the 0.75" spacing of the Intellec MDS. The analog interface for each system is a connector at the opposite edge of the board from the bus connector.

The Data Acquisition system is available with up to 64 channels single-ended on one board. It includes an input multiplexer, high gain instrumentation amplifier, 8-bit A/D converter along with all the necessary timing, decoding and control logic. A DC/DC converter (+5V to ±15V) is also available so that only the computer's power supply is required. The Data Acquisition System is available with two optional 8-bit D/A converters to provide analog input and output on the same board.



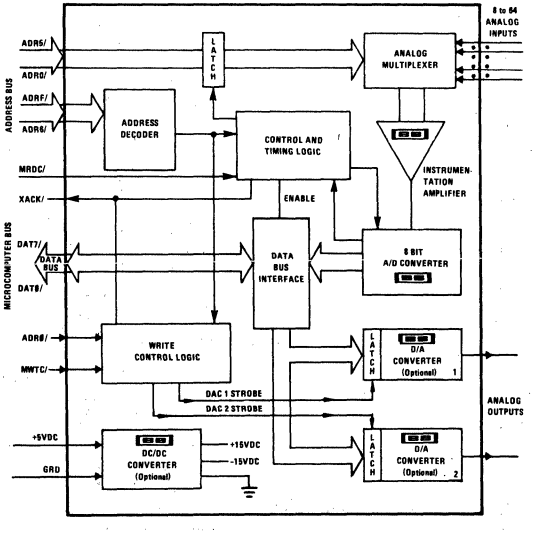
THEORY OF OPERATION

When programming with these peripherals, they are treated as memory locations. Any memory reference instruction can be used. Both the A/D converter output and the D/A converter input are 8-bit words so one memory location is needed for each channel. Because the address block occupied by each peripheral is user selectable, it can be placed anywhere in memory.

Because these units are treated as memory, a minimum of instructions are needed to read an input channel or to set the input of a D/A converter. For instance, the LHLD (load) instruction followed by the proper address can be used to read data from two successive analog input channels. It will automatically select the desired channel, initiate conversion and, when conversion is complete, transfer the A/D converter output for the first channel to the 8080's L register and the second channel to the H register. Likewise a single LDA instruction can be used to read one analog input channel.

All of these systems are jumpered at the factory with the first channel at address $F700_{16}$. Each subsequent channel is one memory location past the start of the last channel so that the second channel is at location $F701_{16}$.

ANALOG INPUT/ OUTPUT SYSTEM



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT/OUTPUT SYSTEM

ANALOG INPUT

Number of analog inputs	
8 differential	MP8608
16 single-ended	MP8616
32 differential or 64 single-ended [5]	MP8632
Input voltage range[1]	±10mV to ±5V
ADC gain ranges[1]	±10V, 0 to 10V, 0 to 5V
(strap selectable)	±5V, ±2.5V
Amplifier gain range[1]	1 to 1000 V/V
(resistor programmable)	
Amplifier gain equation	$G = 100k\Omega / R_{EXT}$
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C (max)	+300nA
0°C to 70°C	-2nA °C
Amplifier input offset voltage	±2mV
Amplifier input offset voltage drift	$\pm(5 + \frac{1000}{G})$ μV °C

ANALOG INPUT TRANSFER CHARACTERISTICS

Resolution	8 bit binary
Throughput accuracy ±5V range (max)	±0.4% FSR[2]
±10mV range	±0.5% FSR
Temperature coefficient of accuracy	
±5V range (max)	±0.02% FSR °C
±10mV range	±0.07% FSR °C
Conversion time ±5V range	44 microseconds
±10mV range	84 microseconds
CMRR (for differential inputs)[3]	66 dB (Gain = 2)
	86 dB (Gain = 100)

ANALOG OUTPUT

Number of analog outputs	2
Output voltage range[4]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V
	at 5mA (strap selectable)
Output impedance	1Ω
Output settling time (max)	< 5 microseconds

ANALOG OUTPUT TRANSFER CHARACTERISTICS

Resolution	8 bits binary
Throughput accuracy (max)	±0.4% FSR
Temperature coefficient of accuracy	
Unipolar	±0.005% FSR/°C
Bipolar	±0.01% FSR/°C

DIGITAL INPUT/OUTPUT

All signals are compatible with Microcomputer Bus	
Output coding	Bipolar, two's complement; Unipolar, straight binary
An analog input channel is selected by:	ADR0/ through ADR5/
An analog output channel is selected by:	ADR0/
The input/output data bits are read through:	DAT0/ through DAT7/

POWER REQUIREMENTS

MP8608, MP8616, MP8632,	+5VDC ±5% at 1 amp, 25mV ripple
With analog output	
MP8608-AO, MP8616-AO, MP8632-AO	+5VDC ±5% at 2 amp, 25mV ripple

TEMPERATURE RANGE

0°C to 70°C

(1) Connected at the factory for ±5V range (ADC range = ±10V, Gain = 2).
(2) FSR is Full Scale Range (i.e., 10V for ±5V range).
(3) DC to 60Hz with 1kΩ source unbalance.
(4) Connected at the factory for ±10V range.
(5) Connected at the factory as 32 differential.

OPERATING INSTRUCTIONS

PROGRAMMING

Programming of this analog I/O board is easily accomplished since all channels are treated as memory locations. Any memory reference instruction can be used. A single STA instruction may be used to load the accumulator contents to one of the D/A converters. Likewise a single LDA instruction can be used to read an analog input channel.

Single instructions can also be used to set the inputs of both D/A converters and read two adjacent analog input channels. An SHLD instruction referenced to DAC 1 will load the contents of the L register into DAC 1 and the contents of the H register into DAC 2. An LHLD instruction will read the channel addressed and the next higher channel. The channel addressed will be transferred to the L register and the next higher channel to the H register. Of course, any MOV instruction may also be used if direct addressing is not desired.

The normal operation of this board halts the CPU during the conversion time of the analog input system. This is because the software in this mode is simpler than in any other (i.e., only one instruction required!). If the halt feature is not desirable, it may be disabled.

For operation without halting the CPU, the conversion should be started by using a single channel memory reference instruction (LDA or MOV). Then the CPU should execute a routine which will take longer than the conversion time (44 to 84 microseconds). When the CPU now uses an LDA or MOV referenced to the same memory location, the converted data will be transferred to the CPU.

The voltage data for these boards is represented by an 8-bit two's complement binary number. With a ±5V range, each bit has a value of 39.1mV, with the polarity of the voltage indicated by the sign of the binary number.

Each board is set at the factory for a block of addresses beginning at F700. Any analog data channel requires one memory location. Thus the first analog channel is located at F700 while the second analog channel is located at F701.

MECHANICAL CHARACTERISTICS

Compatible with Intellec MDS and SBC-604/614 card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers.

50 pin analog edge connector on board.

Mating connector available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab); from 3M: 3415-0001 (Scotchflex).

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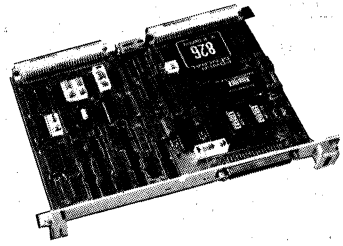


MPV901
MPV901A
MPV901P

MICROCOMPUTER ANALOG I/O SYSTEMS

32-CHANNEL ANALOG INPUT, 2-CHANNEL OUTPUT SYSTEMS WITH VMEbus COMPATIBILITY

FEATURES

- HIGH AND LOW LEVEL INPUTS (±10V to ±10mV)
- SOFTWARE-PROGRAMMABLE-GAIN (1 to 1000) AMPLIFIER OPTION (MPV901P)
- 32 ANALOG INPUTS AND 2 OUTPUTS ON ONE BOARD
- AMPLIFIER GAIN INDIVIDUALLY PROGRAMMABLE FOR EACH CHANNEL USING ON-BOARD RAM
- ADDRESS SELECTABLE IN WHOLE 16MBYTE MEMORY SPACE
- 12-BIT RESOLUTION

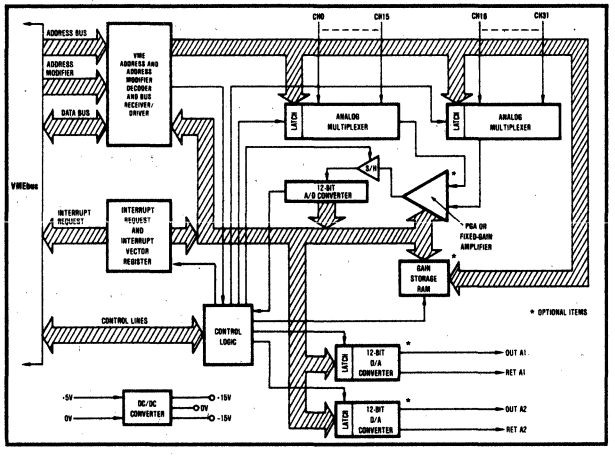
DESCRIPTION

The MPV901 series of analog I/O boards are electrically and mechanically compatible with, and interface directly to, the VMEbus.

The analog input section of the MPV901 includes: an analog multiplexer suitable for 32 single-ended or 16 differential channels, resistor-programmed instrumentation amplifier (MPV901, MPV901A) or a software-programmable amplifier (MPV901P, gain of 1 to 1000), sample/hold amplifier and 12-bit A/D converter. An optional analog ouput system is included on the MPV901A and MPV901P, consisting of two 12-bit D/A converters and associated control logic.

The PGA gain setting and channel selection are dynamically-monitored and the settling time of the PGA calculated to allow maximum data throughput rates.

Gains of 1 to 1000 are software-selectable for the PGA and the gain for each channel may be stored in an on-board RAM if desired. The proper gain for each channel is then selected automatically by the MPV901.



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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated power supplies (as defined in VMEbus specification) unless otherwise stated.

ANALOG INPUT SECTION	
INPUT CHARACTERISTICS	
Number of Channels	32 single-ended/16 differential
ADC Gain Ranges (Jumper-Selectable)[1]	0 to 5V, 0 to 10V, ±2.5V, ±5V, ±10V
Amplifier Gain Ranges	
Resistor-Programmable[2] (MPV901, MPV901A)	1 to 1000
Software-Programmable (MPV901P)	1 to 1000 (steps of 1, 10, 100, 1000)
Maximum Input Voltage Without Damage	±25V (Power Off), ±35V (Power On)
Input Impedance	>100MΩ, 5pF OFF Channel >100MΩ, 50pF ON Channel
Bias Current (+25°C), max	±35nA
(0°C to +70°C), max	±60nA
Differential Bias Current	±35nA
Amplifier Input Offset Voltage[3]: MPV901P	±320μV
MPV901, A	±160μV
Amplifier Input Offset Voltage Drift	
Resistor-Programmable (MPV901, MPV901A)	±10μV/°C
Software-Programmable (MPV901P)	±10μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Throughput Time, G = 1:	
Resistor-Programmable (MPV901, MPV901A)	100μsec, max
Software-Programmable (MPV901P)	100μsec, max
Throughput Time, G = 1000:	
Resistor-Programmable (MPV901, MPV901A)	720μsec, max
Software-Programmable (MPV901P)	720μsec, max
ACCURACY	
System Error at +25°C, max[4]	
MPV901P: G = 1, G = 1000	±0.05%, ±0.075% FSR[5]
MPV901, A: G = 1, G = 1000	±0.05%, ±0.4% FSR
System Linearity	±0.025% FSR
A/D Converter	
Linearity	±1/2LSB
Differential Linearity	±1/2LSB
Quantizing Error	±1/2LSB
Gain Error	Adjustable to Zero
Offset Error	Adjustable to Zero
Monotonicity[6]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE	
System Accuracy Drift	
MPV901P: G = 1, G = 1000	50ppm, 50ppm of FSR/°C
MPV901, A: G = 1, G = 1000	40ppm, 100ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time	125nsec
Aperture Time Uncertainty	±5nsec
Differential Amplifier CMRR, G = 1:	
MPV901P	90dB (DC to 60Hz)
MPV901, A	80dB (DC to 60Hz)
Channel Crosstalk	75dB down at 1kHz for OFF Channel to ON Channel
ANALOG OUTPUT SECTION [MPV901A, MPV901P]	
OUTPUT CHARACTERISTICS	
Number of Channels	2
Output Voltage Ranges (Switch-Selectable)	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V, at 5mA
Output Impedance (at DC)	0.05Ω
Short Circuit Protection, Duration	Indefinite to Common
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Output Settling Time, max	5μsec
ACCURACY	
Output Error, max	±0.15% FSR
Temperature Coefficient of Accuracy	±25 ppm of FSR/°C
POWER REQUIREMENTS	
MPV901	+5V ±5% at 1.5A max
MPV901P	+5V ±5% at 2.0A max
MPV901A	+5V ±5% at 2.0A max
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Storage Temperature	−25°C to +85°C
Relative Humidity	90% noncondensing

NOTES: (1) Factory set for ±10V operation. (2) Factory set for Gain = 1. (3) Adjustable to zero. (4) Includes linearity errors with gain and offset errors adjustable to zero. (5) FSR means Full Scale Range. (6) No missing codes guaranteed.

MECHANICAL

Compatible with double-height VMEbus card-racking systems. Minimum card spacing 20.34mm (0.8") [VMEbus specification-compatible]. One 37-pin 'D' type analog connector on board for analog inputs/outputs. Use Cannon 'D' type connector part number DC37P/1A1N or equivalent.

OPERATING INSTRUCTIONS

INSTALLATION

The MPV901 is shipped from the factory calibrated and ready to use. Installation only requires plugging the card into an empty slot in the VMEbus card cage and wiring the analog connector.

PROGRAMMING

The board is programmed as 64 successive memory locations (word locations), switch-selectable in the whole 16M byte address range. Both the A/D converter output and D/A converter inputs are 12-bit words, therefore data word accesses are required for each channel.

A minimum of instructions are needed to read an input channel or to set the input of a D/A converter. For example, a read instruction, addressed to the next channel to be converted, will acquire the converted data of the current channel and upon completion of the data transfer, initiate a conversion at the new channel address just selected.

On the MPV901P version the on-board RAM may be used to store a gain value for each channel. In the case where the RAM is not used (Control Register D12 = 0), or is not available (MPV901, A), the gain must be written to an on-board register (Control Registers D08 and D09). All boards are jumpered at the factory with a base address of FFF780H. Each subsequent channel is two memory locations past the start of the last channel, consequently channel 0 is at location FFF780H, channel 1 is at location FFF782H.

The input system operates in the following modes:

Interrupt Mode. A read instruction to the board starts the conversion. An interrupt is generated at the end of the conversion. The interrupt can be connected to any one of seven interrupt request lines and may also be disabled by software. (Control Register D14 = 1 enables the board for Interrupt Mode.)

Polling Mode. A read instruction to the board starts the conversion. The interrupt is disabled either by software or by setting all switches on the interrupt request lines to the OFF position. The CPU determines the end of conversion by reading the Status Register. (Control Register D14 = 0 disables interrupt for Polling Mode.) When conversion is complete, the CPU reads the data. The read instruction is addressed to the next channel to be

converted. The data from the last conversion is thus transferred to the CPU and conversion is started for the next channel.

During the Interrupt Mode of operation, the MPV901 supplies the interrupt vector on data lines D00-D07 when requested by the CPU. The vector is user-definable as illustrated in Table I. The MPV901 can also be selected to interrupt on any one of seven interrupt request lines as shown in Table II. Interrupt capability can be disabled either by software (Control Register D14 = 0) or by hardware (no switches selected).

TABLE I. Interrupt Vector Selection

DATA LINE	SWITCH POSITION FOR "0"	SWITCH POSITION FOR "1"
D00	SW4 psn 1 ON	SW4 psn 1 OFF
D01	2 ON	2 OFF
D02	3 ON	3 OFF
D03	4 ON	4 OFF
D04	5 ON	5 OFF
D05	6 ON	6 OFF
D06	7 ON	7 OFF
D07	8 ON	8 OFF

TABLE II. Interrupt Line Selection.

REQUEST INTERRUPT ON LINE	SWITCH SELECTED (ONE ONLY)
IRQ1*	SW1 psn 10, 3, 2 ON
IRQ2*	9, 3, 1 ON
IRQ3*	8, 3 ON
IRQ4*	7, 2, 1 ON
IRQ5*	6, 2 ON
IRQ6*	5, 1 ON
IRQ7*	4 ON

SW4 is used to set the interrupt vector while SW1 selects the interrupt line on which the request is to be made. (Note that switch SW1 should be set to select interrupt capability on ONE line only.)

STATUS REGISTER

D15	D14	D13	D12	D11	D10	D09	D08
CONV COMP	INT EN	R/W EN	RAM EN	SHORT CYCLE	NOT USED	G1*	G0*

*Used only with software-programmable amplifier.

CONV COMP - This bit is low during conversion. It goes high on completion of conversion.

INT EN - Status of interrupt enable.

R/W EN - Status of write enable.

RAM EN - Status of RAM enable.

SHORT CYCLE - Status of short cycle.

G1, G0 - Gain Control - current value of gain stored in control register.

CONTROL REGISTER

D15	D14	D13	D12	D11	D10	D09	D08
NOT USED	INT EN	R/W EN	RAM EN	SHORT CYCLE	NOT USED	G1*	G0*

*Used only with software-programmable amplifier.

INT EN - A 1 enables interrupt, a 0 disables interrupt.

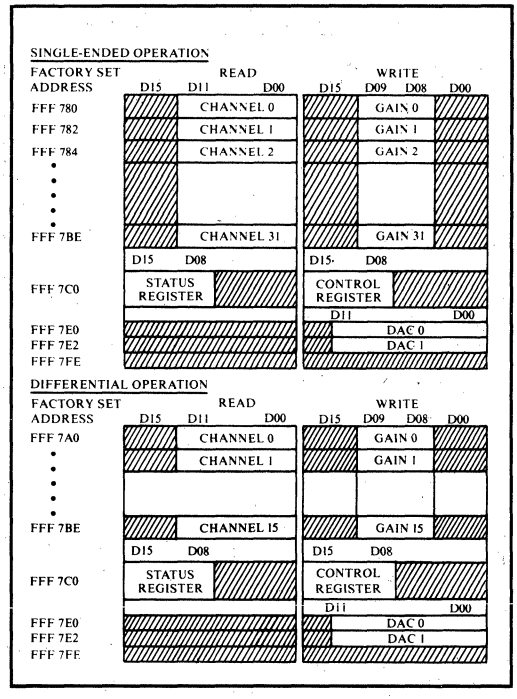
R/W EN - A 0 enables the CPU to write the gain for each channel to RAM. A 1 prevents the CPU from writing to RAM.

RAM EN - A 0 disables the internal RAM and the CPU must write a gain (G1, G0) into the Control Register. A 1 enables the RAM to supply gains as stored.

SHORT CYCLE - A 0 enables 10-bit conversion to take place (for increased speed and reduced accuracy operation). A 1 disables short cycle and allows full 12-bit operation.

G1, G0 - If the RAM is not used to store gain information the gain may be written on G1 and G0. The gain remains as written until a new value overwrites the old value.

MEMORY MAP



ADDRESS MODIFICATION

The base address of a board can be set to any value by properly setting its address selectors. The base address set at the factory is FFF780H. To change the sense of a bit simply change the position of the switch setting for that bit (address line A07 is factory set to a "1").

TABLE III. Address Switch Selection.

ADDRESS LINE	FACTORY SET	SWITCH POSITION FOR "0"	"1"
A07	1		
A08	1	SW2 psn 1 ON	SW2 psn 1 OFF
A09	1	2 ON	2 OFF
A10	1	3 ON	3 OFF
A11	0	4 ON	4 OFF
A12	1	5 ON	5 OFF
A13	1	6 ON	6 OFF
A14	1	7 ON	7 OFF
A15	1	8 ON	8 OFF
A16	1	SW3 psn 8 ON	SW3 psn 8 OFF
A17	1	7 ON	7 OFF
A18	1	6 ON	6 OFF
A19	1	5 ON	5 OFF
A20	1	4 ON	4 OFF
A21	1	3 ON	3 OFF
A22	1	2 ON	2 OFF
A23	1	1 ON	1 OFF

ANALOG OUTPUT RANGE SELECTION

Each DAC is jumpered at the factory for ±10V operation (complementary offset binary coding). It is possible, however, to alter jumpers on the board for other output voltages and coding (see Table IV). When making a change, first set all switch positions on SW6 to the OFF position and then set to the ON position those switches required for the desired range.

TABLE IV. Analog Output Range Selection.

RANGE	OUT 0	OUT 1
±10V	SW6 psn 2,3 ON	SW6 psn 7,8 ON
±5V	1,3 ON	6,8 ON
±2.5V	1,3,5 ON	6,8,10 ON
0 to +5V	1,4,5 ON	6,9,10 ON
0 to +10V	1,4 ON	6,9 ON

NOTE: The analog outputs default, on power-up, to the most positive value in the selected range.

ANALOG OUTPUT CHECKOUT

It is simple to perform static checks of the two analog outputs by loading the D/A locations with an output data word. The base addresses of the analog outputs are factory set to values of FFF7E0H and FFF7E2H. The ideal values for plus and minus full scale are shown in Table V.

TABLE V. DAC Full Scale Values.

DATA WORD	RANGE ±2.5V	±5.0V	±10.0V	0 to +5V	0 to +10V
(X) FFF	-2.5000V	-5.000V	-10.000V	0.0000V	0.0000V
(X) 000	+2.4988V	+4.9976V	+9.9951V	+4.9988V	+9.9976V

(X) Indicates don't care states

The following Motorola 68000 assembly language program performs a simple dynamic check of the two analog outputs. A ramp (sawtooth) waveform with amplitude plus and minus full scale and frequency approximately 1.25kHz will be produced at each output.

NOTE: The constant "STEP" in the program can be altered to give different frequencies and number of steps in the output waveform. (e.g., changing STEP to 63H will give an output frequency of 2.5kHz)

```
        MPV901A.P    DYNAMIC DAC CHECK.....IB 6983.....*/
BASEADD:  EQU        @$FFF780;        /*BOARD BASE ADDRESS */
OUT0ADD:  EQU        BASEADD+$60;     /*DAC0 ADDRESS */
OUT1ADD:  EQU        BASEADD+$62;     /*DAC1 ADDRESS*/
STEP:     EQU        #$0031;          /*SET FREQ. AND NO. STEPS */

          MOVE.W     $0000,D0;        /*STARTING VALUE (FOR FULL SCALE) */
LOOP      MOVE.W     D0, OUT0ADD;
          MOVE.W     D0, OUT1ADD;
          ADDI       STEP,D0;
          JMP        LOOP;,
```

ANALOG OUTPUT CALIBRATION

The analog outputs can be calibrated as follows. Install the board in a VMEbus racking system and allow it to reach thermal equilibrium (about 15 minutes under power) before starting the procedure.

Start calibration by loading both DACs with data that will produce the most negative ouput, which for complementary straight binary operation is FFFH. The DACs should then be set by their offset control (RV6 for OUT 0 and RV8 for OUT 1) to the appropriate voltage value shown in Table VI. The gain control (RV5 for OUT 0 and RV7 for OUT 1) is adjusted in a similar manner after setting the DACs to their most positive output which for straight binary is 000H. The gain control is used to set the DAC output to the HIGH voltage value indicated in Table VI.

TABLE VI. DAC Calibration Values.

RANGE	LOW	HIGH	1 LSB
±10V	−10.000V	+9.9951V	4.88mV
±5V	−5.000V	+4.9976V	2.44mV
±2.5V	−2.500V	+2.4988V	1.22mV
0 to +5V	0.000V	+4.9988V	1.22mV
0 to +10V	0.000V	+9.9976V	2.44mV

ANALOG INPUT RANGE SELECTION

Software-Programmable Amplifier (MPV901P)

The analog input system as shipped from the factory can be software-set for input ranges of ±10V to ±10mV. Table VII gives the input ranges for each gain value.

TABLE VII. Software-Programmable Amplifier Input Ranges.

GAIN SETTING	AMPLIFIER GAIN	INPUT RANGE*	LSB VALUE
00	1	±10V	4.88mV
01	10	±1V	0.488mV
10	100	±100mV	48.8μV
11	1000	±10mV	4.88μV

*Assumes A/D converter range of ±10V.

Resistor-Programmable Amplifier (MPV901,MPV901A)

The analog input system can be set for any range between ±10V and ±10mV. It is set for ±10V (complementary offset binary coding) at the factory.

There are two gain-determining elements in this system—the A/D converter and the instrumentation amplifier. The

A/D converter is factory-set for a ±10V range and the amplifier for a gain of 1. The A/D converter can be set for other ranges by simply changing the jumper links as shown in Table VIII (before adding new jumpers, remove those indicated for the present range).

TABLE VIII. A/D Converter Range-Setting Jumpers.

RANGE	INSERT JUMPERS
±10V	J7, J9
±5V	J6, J9
±2.5	J6, J8, J9
0 to +5V	J6, J8, J10
0 to +10V	J6, J10

MPV901 is factory-set for complementary offset binary coding with switch SW5 position 4 ON and position 3 OFF. For operation in the complementary two's complement mode, switch SW5 position 3 is ON and position 4 is OFF.

Table IX shows the output codes for the analog input section.

TABLE IX. Output Codes for Analog Input Section.

COMPLEMENTARY TWO'S COMPLEMENT		
(XXXX)* 0111 1111 1111	(X) 7FFH	Negative Full Scale
(XXXX)* 1111 1111 1111	(X) FFFH	Midscale
(XXXX)* 1000 0000 0000	(X) 800H	Positive Full Scale
*Four MSB's are unused and set to 1111		
COMPLEMENTARY STRAIGHT BINARY		
(XXXX)* 1111 1111 1111	(X) FFFH	Negative Full Scale
(XXXX)* 0111 1111 1111	(X) 7FFH	Midscale
(XXXX)* 0000 0000 0000	(X) 000H	Positive Full Scale
*Four MSB's are unused and set to 1111		

ANALOG INPUT LOW LEVEL OPERATION

Resistor-Programmable Amplifier (MPV901, MPV901A)

Binding posts for the external gain setting resistor are provided in order that the instrumentation amplifier can be user set for gains up to 1000. Use the following formula to calculate the value of the resistor, Rg.

$$\text{Gain} = 1 + (40/\text{Rg})$$

where Rg is the gain setting resistor, (value in kΩ).

A stable resistor (with temperature coefficient of resistance 5ppm/°C or better) should be used in this application. As shipped from the factory, gain is set to 1.

Settling time of the amplifier increases as gain increases. A delay of 50μsec is set at the factory to allow for multiplexer and amplifier settling times. This delay time is sufficient for amplifier gains up to 50. For gains larger than 50 a longer delay time is required. The appropriate delay for a selected value of gain can be set by inserting the jumper links at position IC43 as shown in Table X.

TABLE X. Amplifier Settling Time Jumpers.

GAIN RANGE	SETTLING TIME REQUIRED	CONNECT PINS ON IC43
1-10	45μsec max	Pin 6-7
11-100	70μsec max	Pins 2-3, 6-7, 14-15
101-1000	650μsec max	Pins 2-3, 6-7, 10-11, 14-15

For lowest system noise, the ADC range should be set at the ±10V or 0 to +10V ranges with the amplifier providing all the system gain.

Single-Ended/Differential Operation

All boards are connected at the factory for 32 channels single-ended operation but can be converted to 16 channels differential operation by simply changing a few board jumpers/switches. Table XI indicates those jumpers/switches that must be present for a given mode of operation.

TABLE XI Channel Conversion.

JUMPER/SWITCH SETTINGS REQUIRED FOR	
SINGLE-ENDED	DIFFERENTIAL
32 channels SW5 psn 1 ON, psn 2 OFF J1, J3 IN; J2 OUT	16 channels SW5 psn 2 ON, psn 1 OFF J2 IN; J1, J3, OUT

In noisy environments the differential mode of operation is recommended for use with low level analog signals which are more prone to common-mode noise interference.

ANALOG INPUT CALIBRATION

If the input range of the resistor-programmable amplifier is to be changed, use the following procedure to adjust gain and offset. The gain and offset errors of the MPV901 may be optimized for any one range by calibrating the unit on that range. The board is factory-calibrated on the ±10V range.

Calibration is performed by connecting a voltage source capable of 0.002% accuracy to any input channel (this could also be a DC voltage source of less absolute accuracy whose output is monitored by a DVM capable of 0.002% accuracy). Offset and gain adjustments are made while applying the voltages listed in Table XII.

TABLE XII. Analog Input Calibration Values.

RANGE	OFFSET	GAIN
0 to +5V	+0.610mV	+4.9982V
0 to +10V	+1.221mV	+9.9963V
±5V	−4.9988V	+4.9963V
±10V	−9.9976V	+9.9972V

For other ranges, offset voltage adjustment is made at the most negative value of the range, plus 1/2LSB. An LSB is equal to the full-scale range divided by 4096 (for 12-bit resolution). Gain adjustment is made at the most positive value of the range less 3/2LSB. Thus for a range of ±50mV, 1LSB is 100mV/4096 = 24.4μV. The offset adjustment is made at −50mV + 12.2μV = −49.9878mV and the gain adjustment at +50mV − 36.6μV = 49.963mV. Before making these adjustments allow the MPV901 to reach thermal equilibrium (about 15 minutes under power). The offset adjustment is made first by using the offset calibration voltage and the following procedure:

1. Set input voltage to appropriate value.
2. Adjust the on-board offset potentiometer (RV4) until the output code reads FFFEH.
3. Adjust the offset potentiometer until the position where the output code makes the transition from FFFEH to FFFFH.

To perform the gain adjustment, perform the following procedure:

1. Set input voltage to appropriate value.
2. Adjust the on-board gain potentiometer (RV3) until output code reads F001H.
3. Adjust the gain potentiometer until the position where the output code makes the transition from F001H to F000H.

Calibration is now complete.

OPERATION SUMMARY

All boards are shipped from the factory ready for immediate use, however, they do have a number of user-selectable options. These options, which have already been described, are summarized below.

1. Programming Mode

   Units are factory-set to the non-interrupt mode and default, on power-up, to the polling mode. Selection of the interrupt mode and interrupt vector is made as outlined earlier. Table I describes the selection of one of seven interrupt vectors.

2. Address/Address Modifier

   The units are factory-set for a base address of FFF780H and to respond to short address decoding (as outlined in the VMEbus specification). Table III describes the jumpers which allow the user to configure the units for any address. Address modifier code response can be altered by programming the PROM to suit user requirements (consult factory for details). If address modifier operation is required, refer to Table XIII.

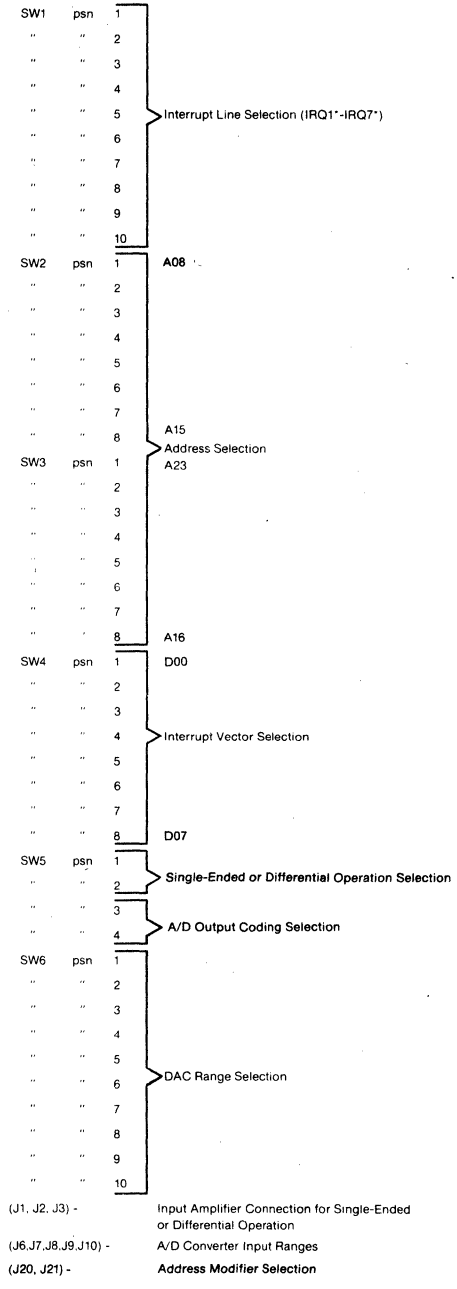
3. Analog Input Range

   Two input amplifier systems are available with the units — resistor-programmable amplifier or software-programmable amplifier. In both cases the A/D converter may be set to any of five input ranges for a gain of 1. The resistor-programmable amplifier may be user-set for gains between 1 and 1000. The gain of the software-programmable amplifier may be stored in an on-board RAM for each channel with gains of 1 to 1000 (Table VII). These units are factory-connected as 32-channel single-ended operation and may be user-connected for 16-channel differential as shown in Table XI.

4. Analog Output Range

   The on-board D/A converters are factory-set for ±10V ranges. Other ranges can be selected as previously described, in section headed Analog Output Range Selection.

SWITCH SUMMARY



See Figure 1 for switch and jumper locations.

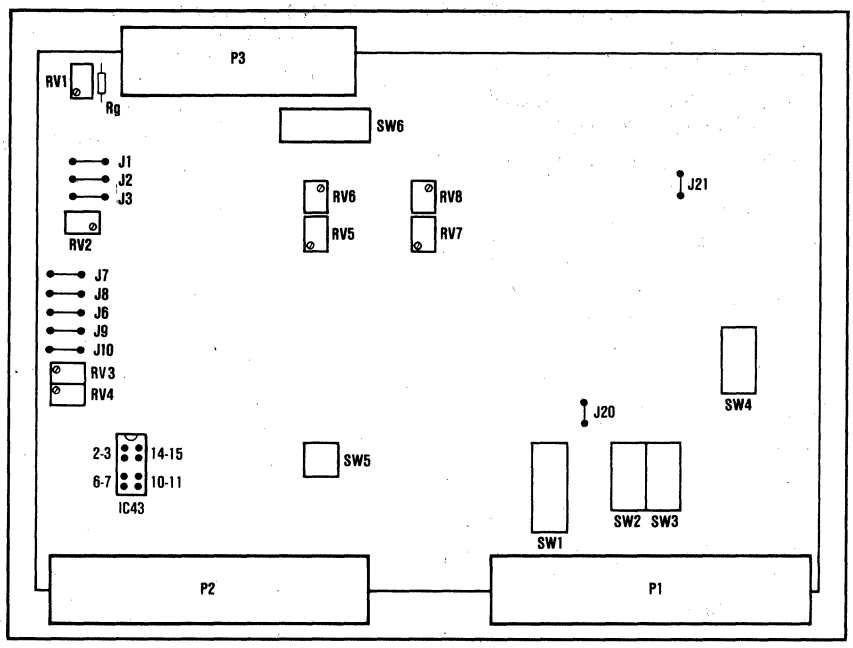


FIGURE 1. MPV901 Series Switch and Jumper Positions.

CONNECTOR PINOUT ("D" TYPE)

PIN NO.		PIN NO.	
1	IN15	20	IN07
2	IN11	21	IN03
3	IN13	22	IN05
4	IN09	23	IN01
5	IN00	24	IN08
6	IN04	25	IN12
7	IN02	26	IN10
8	IN06	27	IN14
9	IN31/RET15	28	IN23/RET7
10	IN27/RET11	29	IN19/RET3
11	IN29/RET13	30	IN21/RET5
12	IN25/RET9	31	IN17/RET1
13	IN16/RET0	32	IN24/RET8
14	IN20/RET4	33	IN28/RET12
15	IN18/RET2	34	IN26/RET10
16	IN22/RET6	35	IN30/RET14
17	0V (ANALOG COMMON)	36	OUT 0
18	0V (ANALOG COMMON)	37	OUT 1
19	0V (ANALOG COMMON)		

NOTE: UNUSED INPUTS SHOULD BE CONNECTED TO 0V (ANALOG COMMON) PINS.

TABLE XIII. Address/Address Modifier (AM) Response.

J20	J21	AM CODES	ADDRESS DECODING
*Insert	Insert	N/A	A01-A15
Insert	Remove	N/A	A01-A23
Remove	Remove	3D, 39	A01-A23

*Factory-set option.

ORDERING INFORMATION

The following options are available when ordering MPV901 series boards.

DESCRIPTION	MODEL
32 channels analog input, resistor-programmable amplifier	MPV901
32 channels analog input, resistor-programmable amplifier 2 channels analog output	MPV901A
32 channels analog input, software-programmable amplifier 2 channels analog output	MPV901P

BURR-BROWN®

MPV904V
MPV904I

ADVANCE INFORMATION
Subject to Change

MICROCOMPUTER ANALOG OUTPUT SYSTEM

16-Channel Analog Output System With VMEbus Compatibility

FEATURES

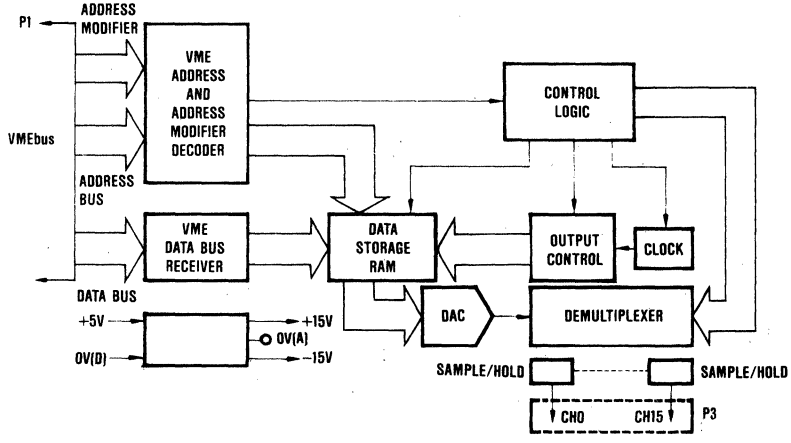
- 16 CHANNELS
- 12-BIT RESOLUTION
- SINGLE GAIN AND OFFSET ADJUSTMENT
- ADDRESS SELECTABLE IN WHOLE 16M BYTE MEMORY SPACE
- SINGLE +5V SUPPLY OPERATION

DESCRIPTION

The MPV904 series of analog output boards are electrically and mechanically compatible with, and interface directly to, the VMEbus.

Dynamic analog outputs allow the MPV904 to provide high channel density on a single board. This approach frees system space for other peripherals and minimizes per-channel power requirement. An on-board DC-to-DC converter powers the MPV904 from the +5VDC system supply. Channel data is stored in an on-board RAM and used by the refresh circuit to update outputs. Each channel has been designed such that system calibration can be accomplished with a single gain and offset adjustment. Address and address modifier decoding are jumper programmable.

Two models of the MPV904 are available, both having 16 analog outputs and 12-bit resolution. The voltage output model (MPV904V) can be jumpered for unipolar or bipolar operation. The current ouptut model (MPV904I) will sink up to 20mA.



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SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise stated.

MODEL	MPV904V	MPV904I
OUTPUT CHARACTERISTICS		
Type	Voltage	Current sink
Number of Channels	16	16
Resolution	12 bits	12 bits
Range (jumper-selectable)	±10V, ±5V, ±2.5V, 0 to +5V, 0 to +10V	0 to 20mA
External Supply Requirements	N/A	15V to 80V[1]
Max Dissipation Per Channel at 5mA		1W, max
ACCURACY		
Total Error[2], max	±0.075%	±0.15% FSR[3]
Offset Error	±0.012%	±0.012%
Gain Error	±0.05% FSR	±0.1%
Linearity	±0.012%	±0.012%
STABILITY OVER TEMPERATURE		
Accuracy Drift	±30ppm of FSR/°C	±60ppm of FSR/°C
TIMING		
Refresh Scan Time	320µsec	320µsec
Charge Time Per Channel	10µsec	10µsec
Settling Time: to 0.1% of FSR	3.5msec	5msec
to 0.01% of FSR, max	5msec	10msec
POWER REQUIREMENTS	+5V ±5% at 1.5A max	+5V ±5% at 1.5A max
ENVIRONMENTAL		
Operating Temperature	0°C to +60°C	0°C to +60°C
Storage Temperature	−25°C to +85°C	−25°C to +85°C
Relative Humidity	90% noncondensing	90% noncondensing

NOTES: (1) See Figure 1. (2) With gain and offset error adjusted as described under Calibration. (3) FSR means Full Scale Range.

MECHANICAL

Compatible with double-height VMEbus card-racking systems. Minimum card spacing 20.34mm (0.8"). One 37-pin 'D' type analog connector on the front panel board for analog outputs.

For 'D' type analog connector use Cannon part number DC37P/1A1N or equivalent.

THEORY OF OPERATION

The design of the MPV904 series analog output boards is based on a dynamic output approach. This uses a single digital-to-analog converter (DAC) to drive all 16 outputs. Digital data for each channel is stored in an on-board RAM while analog output data for each channel are stored in separate sample/hold circuits. The control and refresh circuitry contains a channel counter that selects, from RAM, the appropriate DAC input for the channel being updated and multiplexes the DAC output to the appropriate sample/hold. Thus the output data is updated independently of the CPU.

The CPU changes data in RAM by a write operation on data lines D00-D11 (D00 is the LSB), to the appropriate channel. When this occurs, the control logic disables the refresh circuitry to prevent output glitches and to allow the CPU to change the data stored in RAM.

OPERATING INSTRUCTIONS

INSTALLATION

The MPV904 is shipped from the factory calibrated and ready to use. Installation only requires plugging the card into an empty slot in the VMEbus card cage and wiring the analog connector. Current sink outputs (MPV904I) require the use of an external current source (Figure 1).

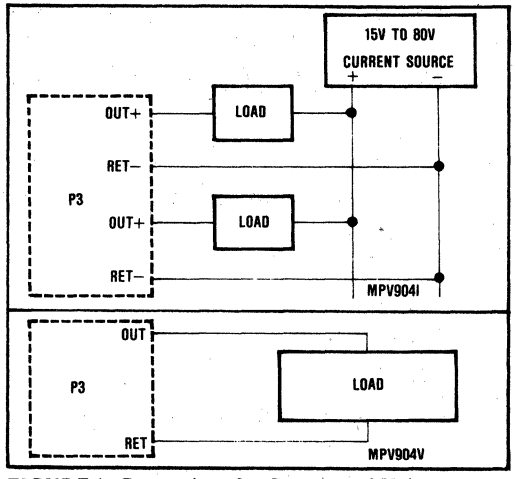


FIGURE 1. Connections for Current and Voltage Outputs.

ORDERING INFORMATION

PROGRAMMING

The board is programmed as 16 successive memory locations (word locations), jumper-selectable in the whole 16M byte address range. Since the output resolution is 12 bits, data word accesses are required for each channel.

A minimum of instructions are needed to set an output channel. In fact, a single write instruction to a particular channel is all that is needed to set that channel.

All boards are jumpered at the factory with a base address of FFF800H. Each subsequent channel is two memory locations past the start of the last channel, consequently channel 0 is at location FFF800H, channel 1 is at location FFF802H.

Memory Map.

Factory Set Address	WRITE ONLY D15 D11 D00
FFF800	OUT 0
FFF802	OUT 1
FFF804	OUT 2
•	•
•	•
•	•
FFF81E	OUT 15

ADDRESS MODIFICATION

The base address of a board can be set to any value by properly setting its address selectors. The base address set at the factory is FFF800H. To change the sense of a bit simply change the jumper setting for that bit (Table I).

TABLE I. Address Selection.

Address Line	Factory Set	Jumper
A05	0	J1 PSN 1
A06	0	2
A07	0	3
A08	0	J2 PSN 1
A09	0	2
A10	0	3
A11	1	4
A12	1	5
A13	1	6
A14	1	7
A15	1	8
A16	1	J3 PSN 1
A17	1	2
A18	1	3
A19	1	4
A20	1	5
A21	1	6
A22	1	7
A23	1	8

0 = insert jumper, 1 = remove jumper.

ADDRESS MODIFIER RESPONSE

The board is factory set to respond to short address decoding (as outlined in the VMEbus specification). If an alternative response is desired, refer to Table II, which describes the jumper arrangements and responses possible with the factory version of the PROM.

Alternative address modifier code response can be accommodated by programming the PROM to suit user requirements (consult factory for details).

TABLE II. Address Address Modifier (AM) Response*.

J20	J21	AM Codes	Address Decoding
Insert	Insert	N/A	A01-A15
Insert	Remove	N/A	A01-A23
Remove	Remove	3D, 39	A01-A23

*Factory set option.

ANALOG OUTPUT RANGE SELECTION

The output range set at the factory is ±10V for the MPV904V and 0 to 20mA for the MPV904I.

To select an alternative voltage output range (MPV904V) refer to Table III which shows the available output ranges and jumper settings. When making a change, first remove all jumpers and then insert those required for the desired range.

The output range for the current version (MPV904I) is not intended to be altered from the factory setting of 0 to 20mA. However, for those users who must have an alternative output range, Table IV lists the available output ranges and jumper settings. When making a change, first remove all jumpers and then insert those required for the desired range. The range can be software-configured for 4 to 20mA.

Table IV shows the DAC full scale values for each range and their associated code values.

TABLE III. Voltage Output Range Selection (MPV904V).

	J5 Jumper Selection	
Range	Insert	Remove
±10V	2, 3	1, 4, 5
±5V	2, 4	1, 3, 5
±2.5V	1, 2, 4	3, 5
0 to +10V	4, 5	1, 2, 3
0 to +5V	1, 4, 5	2, 3

NOTE: The analog outputs default on power up to the most negative value within the selected range.

TABLE IV. Current Sink Output Range Selection (MPV904I).

	J5 Jumper Selection	
Range	Insert	Remove
0 to 20mA	4, 5	1, 2, 3
0 to 10mA	1, 4, 5	2, 3

NOTE: Software-configurable for 4 to 20mA.

TABLE V. Output Full Scale Values.

Data Word	Range						
	+10V	+5.0V	+2.5V	0 to -10V	0 to -5V	0 to 20mA	0 to 10mA
(X)FFF	10.000V	5.000V	2.5000V	0.0000V	0.0000V	0.000mA	0.000mA
(X)000	-9.9951V	-4.9976V	-2.4988V	9.9976V	4.9988V	19.995mA	9.9976mA

(X) indicates don't care states.

ANALOG OUTPUT CALIBRATION

The analog outputs can be calibrated by means of a single gain and offset adjustment as follows. Install the board in a VMEbus-racking system and allow it to reach thermal equilibrium (about 20 minutes under power), before starting the procedure.

1. Connect a DVM (5 1 2 digit) to the calibration point (TP11).
2. Load the RAM (all locations) with the code XFFFH.
3. Adjust the offset control, RV2, until the DVM reads, for the range of interest, the value indicated in Table VI.
4. Load the RAM (all locations) with the code X000H.
5. Adjust the gain control, RV1, until the DVM reads the value, for the range of interest, indicated in Table VI.

Calibration is now complete.

TABLE VI. DAC Calibration Values.

Range	Data (X)FFFH	Data (X)000H	1LSB
±10V	-10.000V	+9.9991V	4.88mV
±5V	-5.000V	+4.9976V	2.44mV
±2.5V	-2.5000V	+2.4988V	1.22mV
0 to -10V	0.0000V	-0.0076V	0.44mV
0 to -5V	0.0000V	+4.9988V	1.22mV
0 to 20mA	0.0000V	-9.9976V	2.44mV
0 to 10mA	0.0000V	-4.9988V	1.22mV

ANALOG OUTPUT CONNECTORS

The 16 analog outputs are available on a 37-pin front panel 'D' type connector.

DEMONSTRATION PROGRAM

The following Motorola MC68000 assembly language program performs a simple dynamic check of all analog outputs. A ramp (sawtooth) waveform with amplitude plus and minus full scale and frequency approximately 1kHz will be produced at each output.

This simple program can be used to check correct operation of all channels.

NOTE: The constant "STEP" in the program can be altered to give different frequencies and number of steps in the output waveform (e.g. changing step to 63H will give an output frequency of 2.0kHz).

```
/.....MPV904.....DYNAMIC OUTPUT CHECK.....
```

JUMPER SUMMARY

1. Address Selection

J1 PSN	3 A07	J2 PSN 8 A15	J3 PSN 8 A23
	2 A06	7 A14	7 A22
	1 A05	6 A13	6 A21
		5 A12	5 A20
		4 A11	4 A19
		3 A10	3 A18
		2 A09	2 A17
		1 A08	1 A16

2. Address Modifier Selection

J4 PSN { 2 / 1 — Refer to Table II.

3. Range Selection

J5 PSN { 5 / 4 / 3 / 2 / 1 — Refer to Table III.

OPERATION SUMMARY

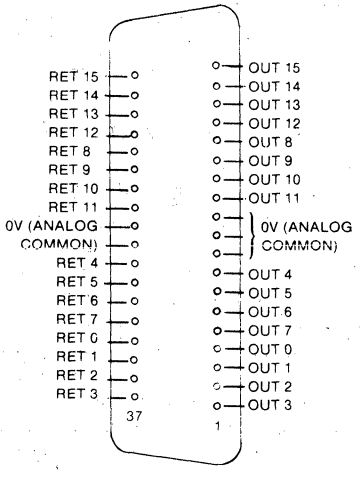
The board is shipped from the factory ready for immediate use. However, it does have a number of user-selectable options. These options, which have already been described, are summarized below.

1. Address
   The board is factory set to a base address of FFF800H. Table I describes jumpers which allow the user to configure the units for any address.
2. Address Modifier
   The board is factory-set to respond to short address decoding (as outlined in the VMEbus specification Revision B) and to ignore (i.e. respond to all) address modifier codes.
3. Analog Output Range
   The factory set output range is ±10V for the MPV904V and 0 to 20mA for the MPV904I. Other ranges can be selected as previously described in section headed Analog Output Range Selection.

CONNECTOR PINOUTS

'D' TYPE

PIN NO.		PIN NO.	
1	OUT 3	20	RET 3
2	OUT 2	21	RET 2
3	OUT 1	22	RET 1
4	OUT 0	23	RET 0
5	OUT 7	24	RET 7
6	OUT 6	25	RET 6
7	OUT 5	26	RET 5
8	OUT 4	27	RET 4
9	0V (ANALOG COMMON)	28	0V (ANALOG COMMON)
10	0V (ANALOG COMMON)	29	0V (ANALOG COMMON)
11	0V (ANALOG COMMON)	30	RET 11
12	OUT 11	31	RET 10
13	OUT 10	32	RET 9
14	OUT 9	33	RET 8
15	OUT 8	34	RET 12
16	OUT 12	35	RET 13
17	OUT 13	36	RET 14
18	OUT 14	37	RET 15
19	OUT 15		



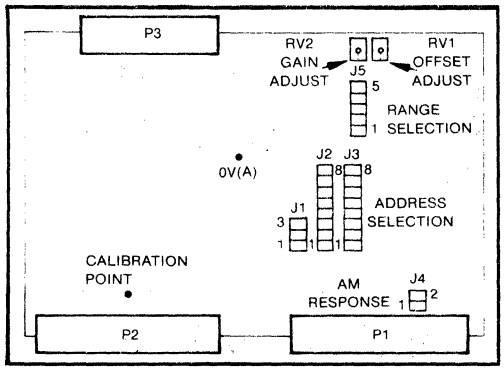


FIGURE 2. MPV904 Jumper Positions.

ORDERING INFORMATION

The following options are available when ordering MPV904 series boards.

Description	Model
16-channel analog output: voltage output	MPV904V
16-channel analog output: current sink	MPV904I

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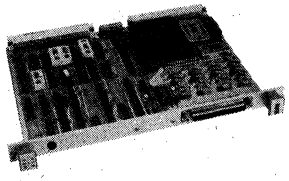


MPV950D
MPV950S

High Speed, 16-Channel, VMEbus-Compatible ANALOG INPUT SYSTEM

FEATURES

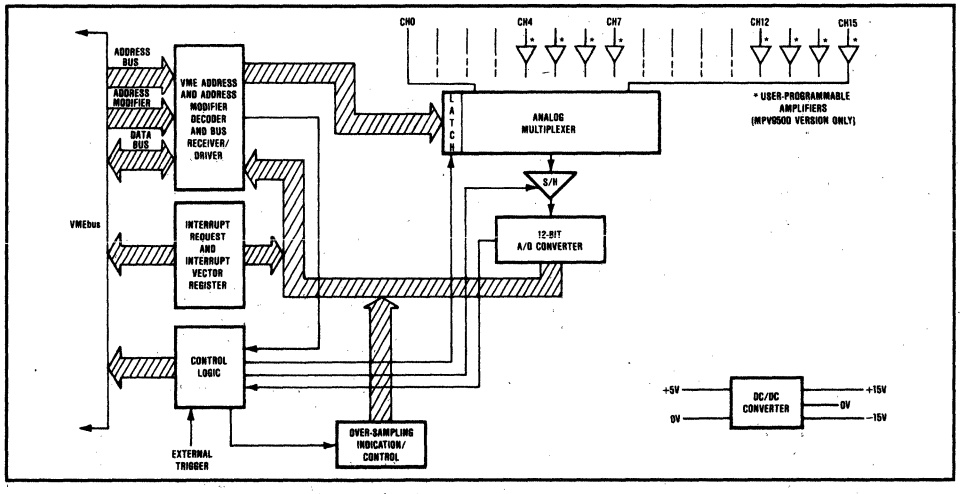
- THROUGHPUT RATES SUITABLE FOR DSP APPLICATIONS
- 3μsec TOTAL THROUGHPUT TIME
- 12-BIT RESOLUTION
- RESISTOR-PROGRAMMABLE-GAIN AMPLIFIER OPTION (MPV950D)
- HIGH AND LOW LEVEL INPUTS (±5V to ±500mV; 0 to +10V or 0 to +1V)
- ADDRESS-SELECTABLE IN WHOLE 16M BYTE MEMORY SPACE

DESCRIPTION

The MPV950 series of analog input/output boards are electrically and mechanically compatible with, and interface directly to, the VMEbus. The analog input section of the MPV950S includes 16 single-ended inputs with gain of 1; the MPV950 includes 8 single-ended inputs with fixed gain of 1 plus 8 inputs with uncommitted amplifiers whose function is user-definable with optional resistor-programmable gains of 1 to 10 (MPV950D), sample/hold amplifier, and 12-bit A/D converter.

An external trigger input is provided and includes an associated front panel indicator which illuminates when the trigger rate exceeds the conversion rate.

MPV950 series boards operate from a single +5V supply with an on-board DC/DC converter providing the remaining power requirements.



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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated power supplies unless otherwise specified.

ANALOG INPUT SECTION	
INPUT CHARACTERISTICS	
Number of channels	16
ADC Gain Ranges (jumper-selectable)[1]	0 to +10V, ±5V
Amplifier Gain Ranges, Resistor-Programmable[2] (MPV950D)	1 to 10
Maximum Input Voltage Without Damage	±25V (power off) ±35V (power on)
Input Impedance:	
MPV950S	>10MΩ
MPV950D, unconditioned inputs	>10MΩ
conditioned inputs	dependent upon amplifier configuration
Bias Current (+25°C), max:	
MPV950S	±30nA
MPV950D, unconditioned	±30nA
conditioned	±80nA
Amplifier Input Offset Voltage (MPV950D)	30μV
Amplifier Input Offset Voltage Drift	0.4μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Throughput Time, max: 12 bits	3μsec
10 bits	2.2μsec
8 bits	2μsec
ACCURACY	
System Error at +25°C, max[3]	
MPV950S	±0.06% FSR[4]
MPV950D, G = 1	±0.06% FSR
G = 10	±0.06% FSR
System Linearity:	
MPV950S	±0.025%
MPV950D, G = 1	±0.025%
G = 10	±0.025%
ADC Gain Error	Adjustable to zero
ADC Offsett Error	Adjustable to zero
Monotonicity[5]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE	
System Accuracy Drift	
MPV950S	±50ppm of FSR/°C
MPV950D	±55ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time, max	20nsec
Aperture Time Uncertainty	±100psec
Channel Crosstalk	75dB down at 1kHz for OFF channel to ON channel
POWER REQUIREMENTS	
MPV950S	+5V ±5% at 2.0A max
MPV950D	+5V ±5% at 2.0A max
ENVIRONMENTAL	
Operating Temperature	0°C to +60°C
Storage Temperature	−25°C to +85°C
Relative Humidity	90% noncondensing

NOTES: (1) Factory set for 0 to +10V operation. (2) Factory set for single-ended mode and Gain = 1. (3) Includes linearity errors with gain and offset errors adjustable to zero. (4) FSR means Full Scale Range. (5) No missing codes guaranteed.

MECHANICAL

Compatible with dougle-height VMEbus card-racking systems. Minimum card spacing 20.34mm (0.8") [VMEbus specification-compatible]. One 37-pin 'D' type analog connector on board for analog inputs/outputs. Use Cannon 'D' type connector part number DC37P/1A1N or equivalent.

OPERATING INSTRUCTIONS

INSTALLATION

The MPV950 is shipped from the factory calibrated and ready to use. Installation only requires plugging the card into an empty slot in the VMEbus card cage and wiring the front-panel connector.

PROGRAMMING

The board is programmed as 64 successive memory locations (word locations), switch-selectable in the whole 16M byte address range. The A/D converter output is a 12-bit word, therefore a data word access is required to read the converted data for each channel.

A minimum of instructions are needed to read an input channel. For example, a read instruction addressed to the next channel to be converted will acquire the converted data of the current channel, and upon completion of the data transfer, initiate a conversion at the new channel address just selected (if CPU triggering is selected) or await an external trigger input before conversion at the new address (if external triggering is selected).

All boards are jumpered at the factory with a base address of FFF780H. Each subsequent channel is two memory locations past the start of the last channel; consequently channel 0 is at location FFF780H, channel 1 is at location FFF782H.

The input system operates in the following modes:

Interrupt Mode—A read instruction or an external trigger to the board starts a conversion. An interrupt is generated at the end of the conversion. The interrupt can be connected to any one of seven interrupt request lines but may be disabled by software (Control Register D09=1 enables the board for Interrupt Mode).

Polling Mode—A read instruction or an external trigger to the board starts the conversion. The interrupt is disabled either by software or by setting all switches on the interrupt request lines to the OFF position. The CPU determines the end of conversion by reading the Status Register (Control Register D09=0 disables the interrupt for Polling Mode). When conversion is complete, the CPU reads the data. The read instruction is addressed to the next channel to be converted. The data from the last conversion is thus transferred to the CPU and either conversion is started for the next channel (CPU trigger selected), or an external trigger is awaited (external trigger selected).

During the Interrupt Mode of operation, the MPV950 supplies the interrupt vector on data lines D00-D07 when requested by the CPU. The vector is user-definable as listed in Table I. The MPV950 can also be selected to

interrupt on any one of seven interrupt request lines as shown in Table II. Interrupt capability can be disabled either by software (Control Register D09=0) or by hardware (no switches selected).

TABLE I. Interrupt Vector Selection

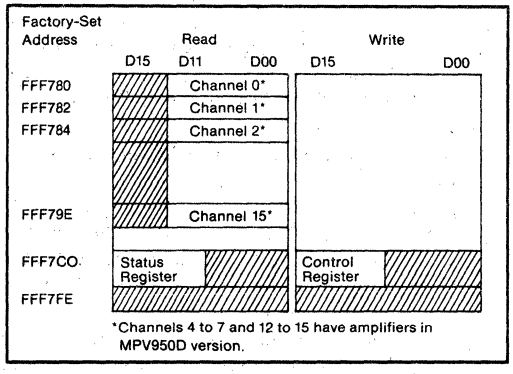
Data Line	Switch Position For "0"	Switch Position For "1"
D00	SW4 psn 1 ON	SW4 psn 1 OFF
D01	2 ON	2 OFF
D02	3 ON	3 OFF
D03	4 ON	4 OFF
D04	5 ON	5 OFF
D05	6 ON	6 OFF
D06	7 ON	7 OFF
D07	8 ON	8 OFF

TABLE II. Interrupt Line Selection

Request Interrupt On Line	Switch Combination (one only)
IRQ1*	SW1 psn 10, 3, 2 ON
IRQ2*	9, 3, 1 ON
IRQ3*	8, 3 ON
IRQ4*	7, 2, 1 ON
IRQ5*	6, 2 ON
IRQ6*	5, 1 ON
IRQ7*	4 ON

SW4 is used to set the interrupt vector while SW1 selects the interrupt line on which the request is to be made (Note that switch SW1 should be set to select interrupt capability on ONE line only).

MEMORY MAP



*Channels 4 to 7 and 12 to 15 have amplifiers in MPV950D version.

STATUS REGISTER

D15	D14	D13	D12	D11	D10	D09	D08
Over Samp	Over Samp	Over Samp	Over Samp	N/A	Conv Comp	Int En	Ext Trig

Over Samp —These bits are normally high. They go low when the external (or internal) trigger rate exceeds the maximum permissible rate.

Conv Comp —This bit is low during conversion. It goes high upon completion of conversion.

Int En —Status of interrupt enable.

Ext Trig —Status of external trigger enable.

CONTROL REGISTER

D15	D14	D13	D12	D11	D10	D09	D08
N/A	N/A	N/A	N/A	N/A	N/A	Int En	Ext Trig

Int En —A 1 enables interrupt, a 0 disables interrupt.

Ext Trig—A 0 enables external triggering, a 1 disables external triggering.

ADDRESS MODIFICATION

The base address of a board can be set to any value by properly setting its address selectors. The base address set at the factory is FFF780H. To change the sense of a bit simply change the position of the switch setting for that bit, (address line A07 is factory-set to a "1")—see Table III.

TABLE III. Address Switch Selection.

Address Line	Factory Set	Switch Position For "0"	Switch Position For "1"
A07	1		
A08	1	SW2 psn 1 ON	SW2 psn 1 OFF
A09	1	2 ON	2 OFF
A10	1	3 ON	3 OFF
A11	0	4 ON	4 OFF
A12	1	5 ON	5 OFF
A13	1	6 ON	6 OFF
A14	1	7 ON	7 OFF
A15	1	8 ON	8 OFF
A16	1	SW3 psn 8 ON	SW3 psn 8 OFF
A17	1	7 ON	7 OFF
A18	1	6 ON	6 OFF
A19	1	5 ON	5 OFF
A20	1	4 ON	4 OFF
A21	1	3 ON	3 OFF
A22	1	2 ON	2 OFF
A23	1	1 ON	1 OFF

ANALOG INPUT RANGE SELECTION

MPV950S

The analog input system can be set for either ±5V or 0 to +10V full scale. It is set for 0 to +10V at the factory (complementary straight binary coding). To set the inputs for the ±5V range, select the jumper links as shown in Table IV (before adding new jumpers, remove those indicated for the present range).

TABLE IV. Input Range Setting Jumpers.

Range	Insert Jumpers
0 to +10V	J6
±5V	J7

The MPV950S is factory-set for complementary straight binary coding. Table V shows the output codes for the analog input section.

TABLE V. Output Codes for Analog Input Section.

COMPLEMENTARY STRAIGHT BINARY

XXXX 1111 1111 1111	(X) FFFH	Negative Full Scale
XXXX 0111 1111 1111	(X) 7FFH	Midscale
XXXX 1000 0000 0000	(X) 000H	Positive Full Scale

Four MSB's are unused and set to 1111.

MPV950D

The analog input system can be set for any range between ±500mV to ±5V or 0 to +1V or 0 to +10V. It is

set for 0 to +10V at the factory (complementary straight binary coding). There are two gain determining elements in this system: the A/D converter and the amplifier associated with a channel. The A/D converter is factory set for a 0 to +10V range and the amplifiers for a gain of 1.

The A/D converter can be set for other ranges by simply changing the jumper links as shown in Table IV. (Before adding new jumpers, remove those indicated for the present range).

The amplifiers can be set to provide any gain value in the range 1 to 10 inclusive. The "uncommitted" amplifier configuration is shown in Figure 1.

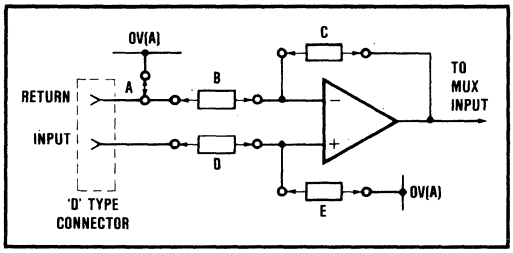


FIGURE 1. "Uncommitted" Amplifier Configuration.

TABLE VI. Circuit Components At Each Channel.

Component	CH7	CH6	CH5	CH4	CH15	CH14	CH13	CH12
A*	J9	J10	J11	J12	J13	J14	J15	J16
B	R33	R37	R41	R45	R49	R53	R57	R61
C*	R34	R38	R42	R46	R50	R54	R58	R62
D*	R35	R39	R43	R47	R51	R55	R59	R63
E	R36	R40	R44	R48	R52	R56	R60	R64

*Factory-fitted link for single-ended input and gain = 1. For other amplifier information, see data sheet on the OPA27 amplifier (PDS-466).

The above arrangement allows the amplifiers to be user connected in many of the standard operational amplifier configurations.

ANALOG INPUT CALIBRATION

If the input range of the A/D converter is to be changed, the following procedure can be used to adjust gain and offset errors. (MPV950 series boards are factory-calibrated on the 0 to +10V range).

Calibration is performed by connecting a voltage source capable of 0.002% accuracy to Channel 0. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a DVM capable of 0.002% accuracy). Offset and gain adjustments are made while applying the input voltages listed in Table VII.

TABLE VII. Analog Input Calibration Values.

Range	Offset Adjust	Gain Adjust
0 to +10V	1.221mV	+9.9963V
±5V	−4.9988V	+4.9963V

Before making the adjustments, allow the MPV950 to reach thermal equilibrium (about 20 minutes under power). The offset adjustment is made first by using the offset calibration voltage and the following procedure:

1. Set calibration voltage to appropriate value.
2. a. For 0 to +10V range: Adjust the on-board offset potentiometer (RV2) until the output code reads FFFEH.
   b. Adjust the offset potentiometer until the position where the output code makes the transition from FFFEH to FFFFH.
3. a. For ±5V range: Adjust the on-board offset potentiometer (RV2) until the output code reads F7FFH.
   b. Adjust the offset potentiometer until the position where the output code makes the transition from F7FFH to F800H.

To perform the gain adjustment, perform the following procedure:

1. Set input voltage to appropriate value.
2. Adjust the on-board gain potentiometer (RV1) until the output code reads F001H.
3. Adjust the gain potentiometer until the position where the output code makes the transition from F001H to F000H.

Calibration is now complete.

FREQUENCY RESPONSE

The ability of the MPV950 series to respond to an input signal of a given frequency is determined by the rate at which the system can acquire and convert signals and by the frequency response of the input amplifiers (MPV-950D).

For 12-bit operation using all 16 channels simultaneously, maximum recommended input frequency is 10kHz. Care should be taken to ensure that the input signal does not contain frequencies of a significant amplitude beyond this value.

For 10-bit resolution and 16-channel operation, the maximum recommended input frequency is 15kHz.

For 8-bit resolution and 16-channel operation, the maximum recommended input frequency is 16kHz.

If the number of channels used at any one time is reduced, then the input signal frequency can be increased accordingly. For example, for 12-bit operation but using only 8 channels, the maximum input frequency can be increased to 20kHz.

The input signal frequency and number of channels (for 12-bit operation) are related as shown below.

$$\text{Max input signal frequency (kHz)} = A/n$$

where A = 160 for 12-bit operation
= 240 for 10-bit operation
= 256 for 8-bit operation
n = number of channels in use

An external trigger input is provided. Details of the trigger signal are shown in Figure 2. A TTL compatible input signal can be used to trigger the board.

The maximum trigger signal repetition rate must not exceed the rate at which an input can be acquired and converted. For 12-bit operation, the maximum trigger frequency is typically 320kHz (not including CPU latency time); for 10-bit operation it is typically 480kHz, and for 8-bit operation it is typically 512kHz.

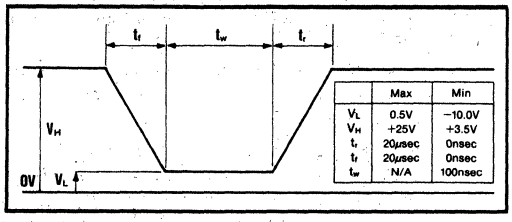


FIGURE 2. External Trigger Signal.

Should the trigger frequency exceed the maximum permissible rate, the front panel LED will illuminate. If this occurs, the trigger frequency should be reduced until the LED is extinguished. Exceeding the maximum trigger rate will also cause data bits D15, D14, D13, D12 (which are normally at a high level), to be driven to a low level, thus indicating the oversampling condition to the CPU.

SHORT CYCLE

If less than 12 bits of resolution is required, the cycle time of the A/D converter can be shortened to give the equivalent of a 10-bit converter with 670nsec conversion time or an 8-bit converter with 500nsec conversion time.

The procedure for obtaining short cycle performance is as follows:

1. Connect a frequency counter or oscilloscope probe to test point TP6.
2. Remove jumpers J1 and J5.
3. Insert jumpers J8, J4, and J3 for 10-bit operation or insert jumpers J8, J4, and J2 for 8-bit operation.
4. Adjust potentiometer RV3 until the pulse width at test point TP6 is 670nsec for 10-bit resolution or 500nsec for 8-bit resolution (see Figure 3).
5. Insert jumper J1.

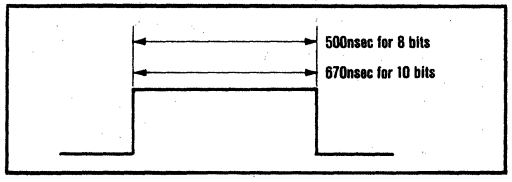


FIGURE 3. Waveform at TP6.

OPERATION SUMMARY

All boards are shipped from the factory ready for immediate use, however they do have a number of user-selectable options. These options, which have already been described, are summarized below.

1. Programming Mode

Units are factory set to the non-interrupt mode and default, on power-up, to the polling mode. Selection of the interrupt mode and interrupt vector is made as outlined earlier. Table I describes the selection of one of seven interrupt vectors.

2. Address/Address Modifier

The units are factory-set for a base address of FFF780H and to respond to short I/O addressing with no address modifier decoding. Table III describes the jumpers which allow the user to configure the units for any address. Address modifier code response can be altered by programming the PROM to suit user requirements (consult factory for details). Address/Address Modifier decoding options are shown in Table VIII.

TABLE VIII. Address and Address Modifier Decoding Options.

J20	J21	AM Codes	Address Decoding
*Insert	Insert	N/A	A01-A15
Insert	Remove	N/A	A01-A23
Remove	Remove	30,39	A01-A23

*Factory-set option.

3. Analog Input Range

Two input systems are available with the units—16 unconditioned inputs (MPV950S), and 8 unconditioned plus 8 conditioned inputs (MPV950D). In both cases the A/D converter may be set to one of two ranges. The amplifiers may be user-set as defined earlier.

4. Triggering

The unit defaults on power-up to the external triggering mode. Selection of internal triggering is as defined earlier (see Control Register).

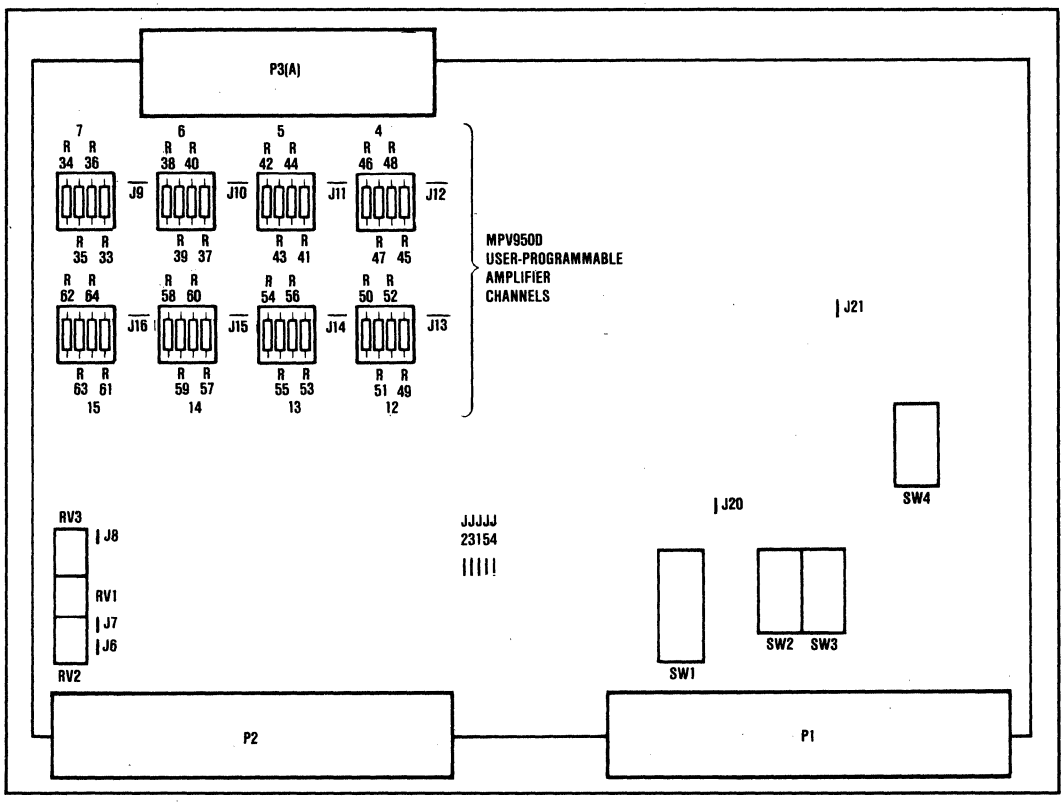


FIGURE 4. MPV950 Series Switch and Jumper Positions.

CONNECTOR PINOUT ("D" TYPE)

Pin No.	Description	Pin No.	Description
1	IN15	20	RET15
2	IN07	21	RET07
3	IN14	22	RET14
4	IN06	23	RET06
5	IN13	24	RET13
6	IN05	25	RET05
7	IN12	26	RET12
8	IN04	27	RET04
9	0V (ANALOG COMMON)	28	0V (ANALOG COMMON)
10	IN11	29	RET11
11	IN03	30	RET03
12	IN10	31	RET10
13	IN02	32	RET02
14	IN09	33	RET09
15	IN01	34	RET01
16	IN08	35	RET08
17	IN00	36	RET00
18	TRIGGER RETURN	37	EXTERNAL TRIGGER
19	TRIGGER RETURN		

NOTE: Unused analog inputs should be connected to 0V (Analog Common)

ORDERING INFORMATION

The following options are available when ordering MPV950 series boards.

Description	Model
16 channels single-ended, analog input	MPV950S
8 channels with user-programmable amplifiers	MPV950D

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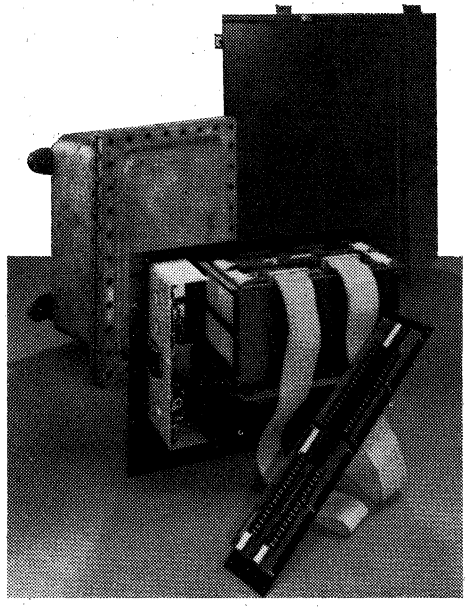
DATA ACQUISITION AND CONTROL SYSTEMS

REMOTE TERMINAL UNITS

Remote Terminal Units (RTUs) are microprocessor-based data acquisition and control packages that provide measurement signal conditioning, local control, and intelligence for complex production processes. These products are geographically distributed throughout the plant facility and communicate the data from many sensors to a central computer over a single cable, thus eliminating large bundles of costly wiring.

MCS Series

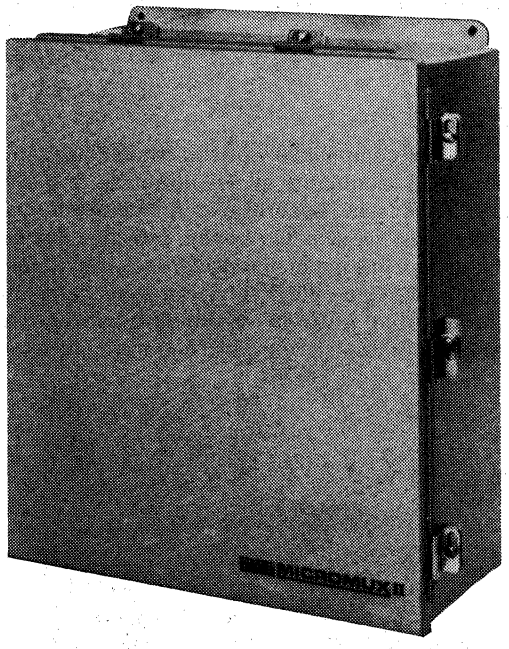
The MCS Series are competitively priced data acquisition and control systems RTU. MCS modularity allows purchase of a system configured for today's needs and assures expandability later with minimum problems and cost. This versatile system provides analog and digital signal conditioning while maintaining accruacy over ambient temperature ranges from −10°C to +60°C. A full range of analog and digital I/O functions are available. A variety of standard packages are available including rack mount chassis with card cage and NEMA enclosures.



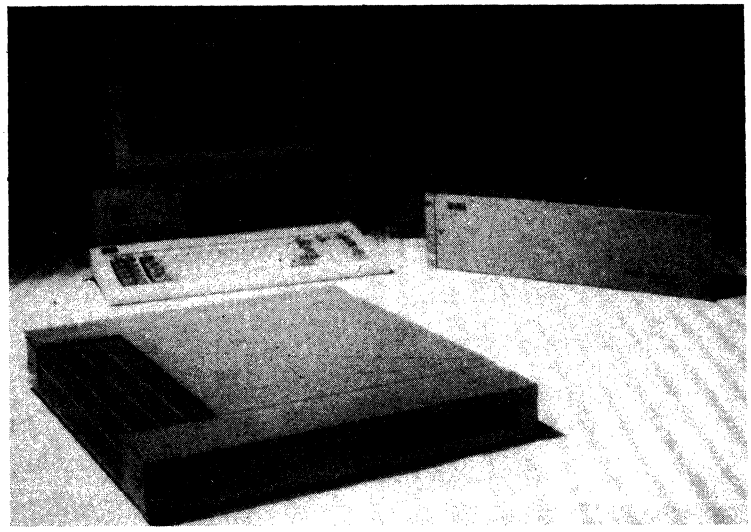
Micromux II

Low base cost makes this system ideal for low point count Supervisory Control and Data Acquisition (SCADA) applications. Multidrop expandability allows the system to grow as needs increase. Modern CMOS technology dramatically reduces power consumption while providing a wide −40°C to +60°C operating temperature range.

Analog and digital I/O options are combined with CPU intelligence on a single board. Each Micromux II board accommodates up to four I/O modules in any combination. I/O modules are available for high level analog input isolation, T/C and RTD linearization, analog outputs, digital I/O, and pulse accumulation. Communications are over a serial line. An onboard modem is optional. NEMA enclosure options protect Micromux II from harsh environments.



PERSONAL COMPUTER INSTRUMENTATION



INTELLIGENT INSTRUMENTATION TURNS PCs INTO LOW COST INDUSTRIAL OR LABORATORY CONTROL CENTERS

The new PCI-3000 System from Burr-Brown lets small personal computers perform test, measurement, data acquisition, signal processing, and control functions formerly requiring much larger and more expensive minicomputers and dedicated systems.

PCI-3000 acts as a front-end processor interfacing a variety of analog and digital data to the PC from industrial and laboratory transducers and signal sources. Compatible host computers include IBM PC and XT, Apple, Compaq, DEC, and HP, plus many minicomputers and mainframes.

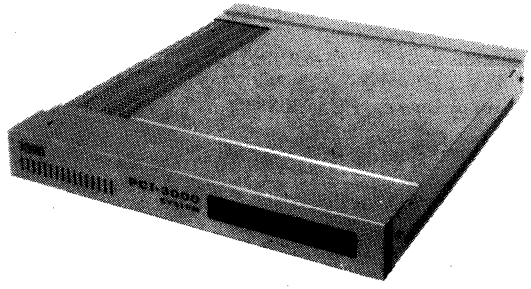
Modular design and a very wide selection of analog, digital, and special-function input/ouput (I/O) boards permit great flexibility in configuring systems to initial requirements and expansion to accommodate system growth and diversification. Added flexibility is provided by extensive internal firmware which accepts simple high level commands.

A basic PCI-3000 system consists of a master unit containing a power supply, Z80A microcomputer with up to 32k of user memory and up to three I/O boards selected for the application. As many as 192 analog or digital I/O points are available to the user from a single master unit. With expansion enclosures, a single master unit can provide up to 1024 I/O points, using 16 I/O boards. Thermocouple, frequency measurement, counting, and pulse-generating functions are also supported.

A family of termination panels are available in the PCI-3000 system. These panels provide convenient screw-terminal connections for both signal inputs and outputs from the real world. Two types of panel enclosures are provided. One panel enclosure is designed for industrial environments. Its panels contain mounting fixtures for auxiliary passive signal conditioning devices such as input filters, dropping resistors, protection diodes, and voltage dividers. A second panel enclosure adapts the PCI-3000 to the unique requirements of the laboratory. Its panel features 64 channels of analog input, 64 digital I/O points, 4 analog outputs, 7 counters, 2 pushbutton switches, and 4 optically-coupled outputs.

PCI-3000

INTELLIGENT INSTRUMENTATION
for Industry and Laboratory



CONFIGURATION GUIDE
AND
DATA BOOK

BURR-BROWN®

TABLE OF CONTENTS

INTRODUCTION

The PCI-3000 is an intelligent instrumentation front end designed to turn any personal computer into a powerful system for data acquisition, test, measurement and control. It interfaces to personal computers such as the IBM PC, IBM XT, DEC, HP, Compaq, Apple, and others. Communications with these computers (or with any other host) takes place through serial (RS-232 or RS-422) channels, or optionally, via IEEE-488.

The PCI-3000 is a very flexible system that offers extensive expansion capabilities. The basic or master unit is housed in a rugged, yet attractive, compact enclosure designed for either rack mounting or for tabletop integration with a personal computer. The master enclosure contains power supplies and a single-board microcomputer. Additionally, up to three I/O boards may be added within the master enclosure. This type of modular construction provides great flexibility in configuring a system. A very basic system could consist of the master enclosure (power supply and microcomputer) with only one I/O board added inside.

System capability can be expanded in the following two directions as shown in Figure 1:

1. A variety of I/O boards may be added along the PCI-3000 Interface Bus under master system control. Expansion-enclosure boxes are available to house four additional I/O boards each. By using multiple expansion chassis, systems of up to 16 I/O boards and over 1000 points may be controlled from a single master unit. The PCI-3000 Bus is designed to allow reliable communications between the expansion enclosures and the master enclosure at distances up to 10 meters (approximately 30 feet).
2. Up to 31 master systems may be networked together along a multidrop communications bus from a single host using RS-422, or IEEE-488 protocols. For applications where sensors or output devices are widely distributed, RS-422 communications can be used for direct wire connections over distances up to 1200 meters (approximately 4000 feet). For longer distances, modems may be used to communicate over various communications links.

The flexibility of the PCI-3000 System is a result of the internal firmware operating system. Stored in EPROM, the operating system is normally transparent to users who rely on the standard command functions. However, the operating system can be modified by those who want to create their own command functions or stand-alone programs for individualized applications. The choice to use these features is up to each user, but is facilitated by these internal PCI-3000 utilities:

Task scheduler
Allows regular or timed execution of user tasks

Drivers
Buffered access to all communications ports
Access to all input/output boards
Clock handling

Debug
Through the on-line debugger

System Library Routines for
Code conversions
Buffer handling
Number system conversion
Thermocouple linearization

The unique PCI-3000 firmware allows the user to access the system without modification or to tailor it to meet special needs. PCI-3000 systems can be programmed as complete data acquisition and control systems. Terminals and printers can be connected to meet individual system needs. User EPROM space is available so programs may be permanently added to PCI-3000 systems.

In addition to its sophisticated architecture and easy-to-use software, the PCI-3000 System offers a reliable and practical set of termination panels which provide a con-

TABLE I. PCI-3000 System Specifications.
(Read/write speeds correspond to 9600 baud communications.)

Communications Local Multidrop Remote	Two asynchronous serial channels, 300-9600 baud. RS-232-C signals on both channels. RS-422 signals on Channel A. (2-wire, half-duplex. Up to 4000 feet.) IEEE-488 (optional), controlled by host.
Memory	8k bytes of user RAM installed. Expandable to 32k bytes, RAM or EPROM.
Temperature Range	0°C to +50°C (I/O boards and enclosures). −25°C to +70°C (passive termination panels).
Mechanical Master or expansion Termination panel rack Lab panel	 2.4 × 17 × 19 inches (H, W, D) 5 × 19 × 2.5 inches (H, W, D) 15.8 × 19 × 2.5 inches (H, W, D)
Expandability	Up to 192 I/O channels per master enclosure. Up to 1024 channels using expansion enclosures. Up to 31 masters can be networked together on an RS-422 multidrop communications line supporting up to 31744 I/O channels.
Analog Inputs Single-ended or Differential	±10mV to ±10V direct inputs (higher with attenuation added to termination panel). Convertible to current input. 0.1% full scale accuracy. 12-bit resolution. 2000 readings/sec (into internal memory). Up to 30 readings/sec returned to host. Programmable gain (1 to 1000). Thermocouple inputs (J, K or T), 0.8°C repeatability.
Analog Output Voltage or current	±10V or 4 to 20mA. 12-bit resolution. 0.1% full scale accuracy. Write time, 20msec.
Counters	Maximum input frequency: 8MHz. Accumulation, gateable. Direct frequency measurements. 16-bit resolution. 0.005% stability.
Pulse Output	Programmable pulse width, period and number of pulses. Frequency range: 61Hz to 2MHz. 125nsec resolution. 0.005% stability.
Digital Input and output	TTL compatible. 24mA current sink, 15mA current source. Read/set bits, bytes or words at the rate of 30/sec. High voltage isolation (4000V DC/AC) and 3A switch capability with opto-isolation panels.
Power Supply	85VAC to 130VAC, 50Hz to 60Hz or 200VAC to 260VAC, 50Hz to 60Hz. 80W.
Termination Panels	Provides screw terminal connections and provisions for user-defined signal conditioning.

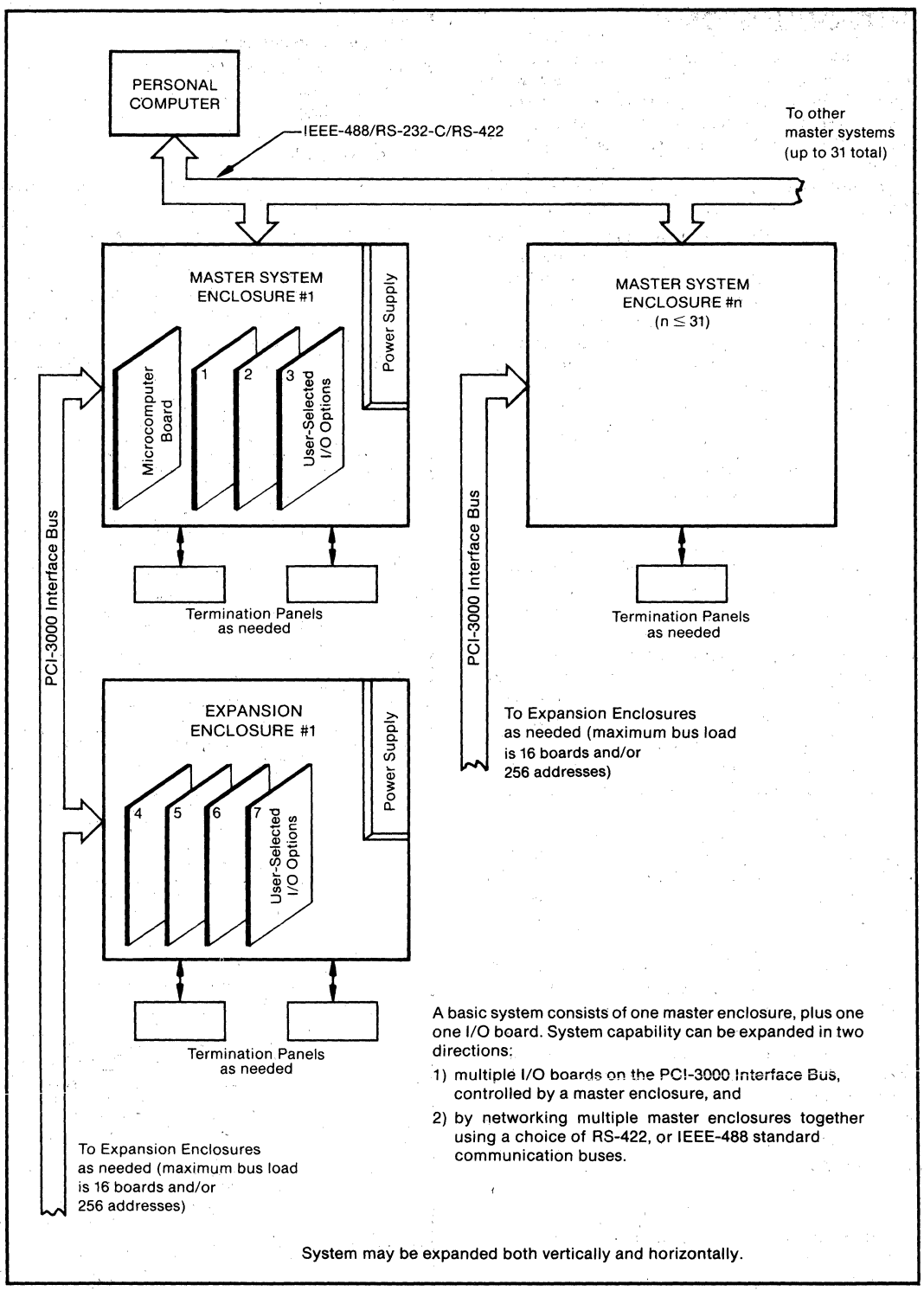


FIGURE 1. PCI-3000 System Expansion Capability.

venient means of connecting to sensors or to output devices. Two different termination panel enclosures are offered to provide an inexpensive and convenient method for housing the termination panels and the wiring leading from the real world into the system:

1. An industrial termination panel enclosure can house one of a number of different termination-panel options. Termination panels provide a neat, accessible method to interface between field wiring and cables leading to master or expansion enclosures. Each of the optional termination panels is designed for optimum interfacing with specific types of input/output devices (digital I/O, analog I/O, thermocouples, etc.)
2. A laboratory termination panel enclosure accepts 64 channels of analog input, 64 digital I/O points, four analog outputs, seven counters, two push-button switches, and provides four optically-coupled inputs. Both ±15V and +5V are brought to its panel along with a variable voltage source (±10 V).

Table I gives the PCI-3000 system specifications.

CONFIGURING A PCI-3000 SYSTEM

This section is an aid in configuring a system for a specific application. More detailed information about each specific product area appears in later sections of this brochure.

Starting with the Master System Enclosure with its power supply and microcomputer, there are three additional elements to consider in configuring a PCI-3000 System:

—the input/output boards for a specific application
—the termination panels for the I/O boards
—the Expansion Enclosures, if required.

The first step in configuring a system is to select the appropriate input/output boards and termination panels to meet the requirements of a given application. The function of a termination panel is to connect the application signals to the input/output boards. The function of an input/output board is to provide the necessary interfacing circuitry to convert real-world signals to a compatible digital format for signal processing.

The termination panel family includes a wide variety of analog, digital, combination analog/digital, thermocouple, laboratory, and optically-isolated terminations. If desired, the termination panels can be housed in a Burr-Brown Termination Panel Enclosure, or in other enclosures such as NEMA boxes for harsh-environment operation.

Input/output boards include digital input/outputs, analog input/outputs, thermocouple inputs, pulse inputs/outputs, as well as combination units.

After selecting the appropriate input/output boards and termination panels, the Master System Enclosure and Expansion Enclosures can be selected. Three input/output boards fit in one Master Enclosure. Each expansion enclosure can hold four input/output boards. Master Systems are listed under the PCI-3000 Series. Expansion Enclosures are needed only if more than three input/output boards are required in your application.

Figure 2 is a convenient diagram to aid in selecting the various I/O boards and termination panels in order to configure a system for any given application. Figure 2 carries the information in Figure 1 to the next lower level, showing which I/O boards will properly interface with termination panels in order to bring signals to and from the real world.

PCI-3000 MASTER AND EXPANSION ENCLOSURES

PCI-3000 Systems are housed in one or more slim-line enclosures that are equally attractive in either tabletop or rack-mounted applications. Each such enclosure houses power supplies and up to four printed-circuit boards. The heart of the PCI-3000 system, a single-board Z80A-based microcomputer, resides in the master enclosure along with as many as three I/O boards. Expansion enclosures accommodate up to four I/O boards. A system of up to 1024 points can be configured with one master enclosure and four expansion enclosures. Systems of up to 31,744 points can be constructed by networking 31 masters together on the RS-422 port. Multi-enclosure systems may be configured by stacking enclosures on top of one another, or by rack mounting the enclosures, using optional slides.

Interconnections between I/O boards and between enclosures are achieved via mass-terminated ribbon cables. Since each expansion enclosure contains its own power supplies, power requirements are automatically met as the system is expanded. Input/output cables exit the rear of the enclosure through a strain-relief slot and plug into screw terminal panels that may also be tabletop or rack mounted in termination panel enclosures.

The unique design of the enclosures allows cooling to occur by a combination of radiation from its metal skin and convection through vent holes. The power supply pod is separated from the printed-circuit boards by a metal thermal barrier. No fans are necessary. This fact considerably improves overall system reliability.

For very harsh environments, PCI-3000 systems can be mounted in NEMA enclosures that provides waterproofing and protection from dust and oil.

FEATURES AND CAPABILITIES

Some of the features and capabilities of the PCI-3000 System that reside in the Master Enclosure are summarized below.

Microprocessor

The PCI-3000 uses the Z80A microprocessor. It operates at a 4MHz rate.

Memory

The microcomputer board is equipped with eight memory sockets which allow a full memory expansion of 64k bytes. The bottom bank of four sockets is dedicated to

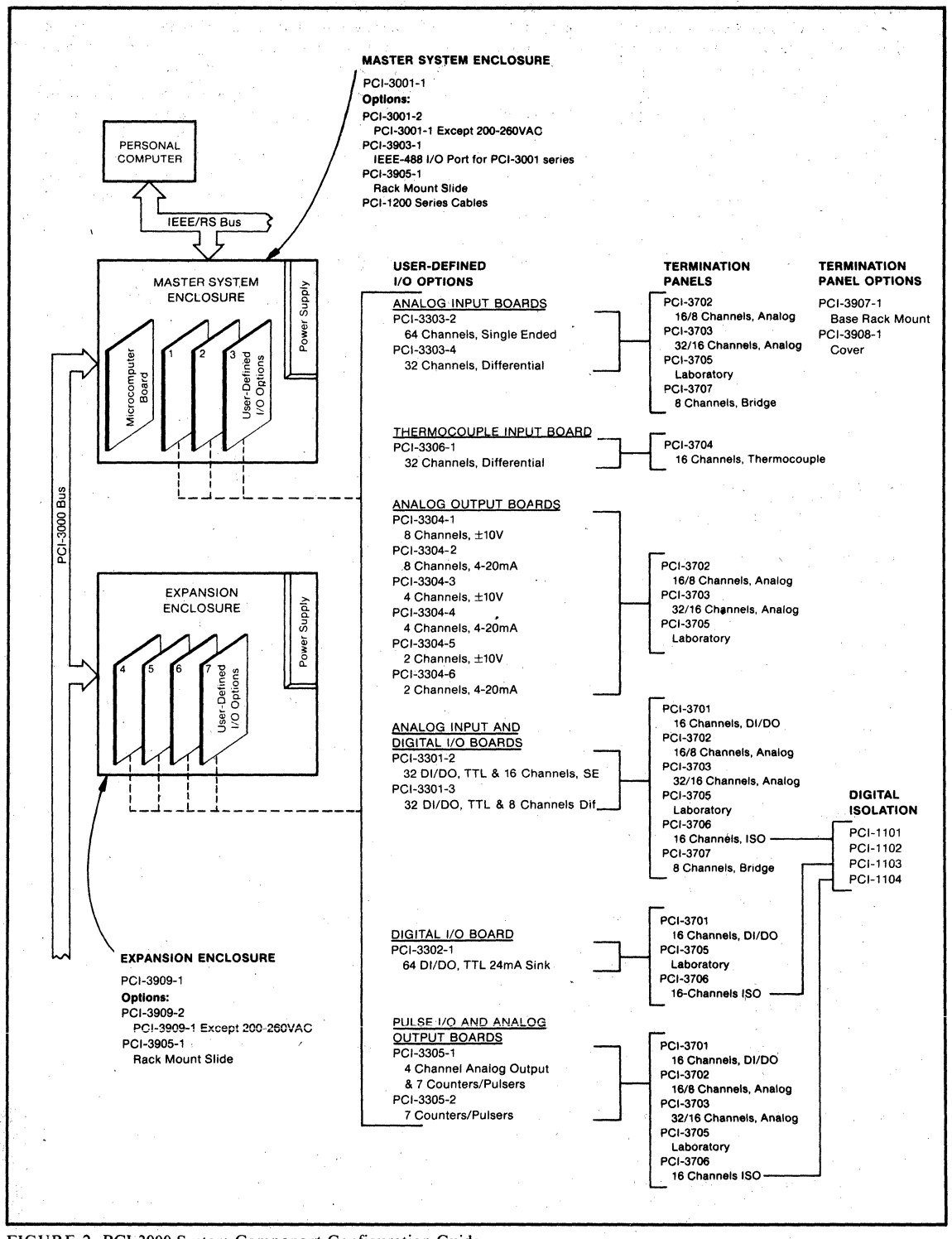


FIGURE 2. PCI-3000 System Component Configuration Guide.

firmware and system RAM. This leaves the top four sockets for RAM expansion or for user EPROM to accommodate special commands or programs. Each socket may be strapped to accept either a RAM or EPROM chip of the BYTEWIDE format. (32K bytes maximum.)

Watchdog Timer

This circuit ensures that the microcomputer will be reinitialized in the event that the processor halts or becomes caught in an infinite loop. A software routine "hits" the Watchdog timer (WDT) periodically. If this routine fails to run, the WDT times out and restarts the processor.

Switch Register

Sixteen on-board switches allow baud rate and mode selection for serial communications channels A and B, as well as unit identification for use in multidrop systems.

Indicators

Eight LED indicators are provided which are used as processor status indicators for both normal operation and during the execution of internal diagnostics.

INPUT/OUTPUT COMMUNICATIONS PORTS

The following descriptions provide an overview of the characteristics of each of the PCI-3000 input/output communications ports.

Channel A

Channel A is a serial, asynchronous, RS-232/422 channel for communication to a host computer or to a terminal. Line speeds of 300 baud to 9600 baud may be selected. When RS-232 is selected, modem control signals are provided. RS-422 drivers and receivers are available to provide two-wire, half-duplex communications. This technique permits reliable data transmission at high data rates without a modem over longer distances than are possible with RS-232 (up to 4000 feet). In addition, RS-422 supports multidrop capability of up to 31 master systems.

Channel B

Channel B provides only RS-232 communications.

PCI-3000 Bus

This bus is designed for simple and reliable interconnection of input/output boards. The PCI-3000 Bus is equipped with special line-transceivers that make it possible for the bus to extend through multiple expansion enclosures while maintaining reliable operation.

GPIB

This optional communications port is the IEEE-488 standard bus for instrument interconnection. It allows the host computer to communicate with both the PCI-3000 and to other instruments plugged into the GPIB.

SYSTEM ENCLOSURE OPTIONS

The following options for PCI-3000 Systems relate to the system enclosures.

PCI-3001-1 Master Enclosure

This enclosure contains the microcomputer, power supply, and cables necessary to begin using the PCI-3000 System with a personal computer equipped with an RS-422 or with RS-232-C communications port. Not included are the I/O interface boards or the termination panels required for a specific application. The PCI-3001-1 Base Unit operates on 85 to 130VAC, 50 to 60Hz.

PCI-3001-2 Master Enclosure

This system has the same features as the PCI-3001-1 except that the power supply operates on 200 to 260 VAC, 50 to 60 Hz.

PC-3909-1 Expansion Enclosure

This enclosure contains power supplies, cables, and mounting space for four I/O boards. Power supplies operate on 85 to 130 VAC, 50 to 60 Hz.

PCI-3909-2 Expansion Enclosure

Same as PCI-3909-1 except power supplies operate on 200 to 260 VAC, 50 to 60 Hz.

The following options are not necessary for the basic operation of the PCI-3001 and PCI-3909 series, but they may be purchased separately for spares, mounting, or for expansion of basic capability of the system.

PCI-3905-1 Rack-Mount Slides

For the PCI-3001 and PCI-3909 Series.

PCI-3903-1 IEEE-488 Port

Converts the PCI-3001 Series to provide IEEE-488 (GPIB) communications.

PCI-3901-1 Microcomputer Board

This board is supplied as part of a PCI-3001 Series Enclosure. This item is a separate listing for those who desire spares. Firmware EPROMs and RAM not included (see below).

PCI-3901-2 Microcomputer Board

This board is the same as the PCI-3901-1, except it does contain the latest revision of PCI-3000 System firmware (EPROMs and RAM).

PCI-3902-1 Firmware Integrated Circuits

The latest revision of PCI-3000 System firmware. Includes EPROMs and system RAM integrated circuits.

INPUT/OUTPUT BOARDS AND DATA SHEETS

Interfacing to real-world signals takes place through the various I/O boards that are available for the PCI-3000 System. Up to three of these I/O boards may be plugged into a Master Enclosure (PCI-3001 Series). This allows systems of up to 192 points to be configured in a single enclosure. For larger systems, Expansion Enclosures (PCI-3909 Series) may be used. Each Expansion Enclosure will accommodate up to four I/O boards, which allows interfacing as many as 256 additional points per expansion enclosure. See Table I for a summary of board specifications.

A list of I/O boards with brief summary descriptions follows. More detail is given in the data sheets at the end of this section.

DIGITAL INPUT/OUTPUT BOARD

PCI-3302-1

64 digital input/output lines, TTL-levels, 24mA sink current

COMBINATION INPUT/OUTPUT BOARDS

PCI-3301-2

32 digital input/outputs and 16 single-ended analog inputs, 12-bit resolution

PCI-3301-3

32 digital input/outputs and 8 differential analog inputs, 12-bit resolution

PCI-3305-1, Counter/Pulser/Analog Output Board

7 digital registers and 4 analog outputs

ANALOG INPUT BOARDS

PCI-3303-2

64 single-ended analog inputs, programmable gain, 12-bit resolution

PCI-3303-4

32 differential analog inputs, programmable gain, 12-bit resolution

THERMOCOUPLE INPUT BOARD

PCI-3306-1

32 channels for J, K, or T type thermocouple inputs, A/D conversion, 12-bit resolution, zero-point compensation, and linearization.

ANALOG OUTPUT BOARDS

PCI-3304-1, 8-Channel Analog Voltage Output Board

±10V analog outputs, 12-bit resolution

PCI-3304-2, 8-Channel Analog Current Output Board

4 to 20mA, analog outputs, 12-bit resolution

PCI-3304-3, 4-Channel Analog Voltage Output Board

±10V analog outputs, 12-bit resolution

PCI-3304-4, 4-Channel Analog Current Output Board

4 to 20mA, analog outputs, 12-bit resolution

PCI-3304-5, 2-Channel Analog Voltage Output Board

±10V analog outputs, 12-bit resolution

PCI-3304-6, 2-Channel Analog Current Output Board

4 to 20mA, analog outputs, 12-bit resolution

COUNTER INPUT/PULSER OUTPUT BOARDS

PCI-3305-1, Counter/Pulser/Analog Output Board

7 digital registers and 4 analog outputs

PCI-3305-2, Counter/Pulser Board

7 digital registers

BURR-BROWN®

PCI-3301 Series

32-POINT DIGITAL INPUT/OUTPUT, 16-CHANNEL ANALOG INPUT BOARDS

FEATURES

DIGITAL I/O SYSTEM

- 32 TTL level input/output points.
- Four 8-bit digital I/O registers each jumper configured for input or output.
- Contents of output registers may be read back.
- Input or output configuration may be read by software.
- Output registers provide 24mA of sink current and 15mA of source current
- Up to 30 read/writes per sec
- Compatible with both isolated and non-isolated termination panels

ANALOG INPUT SYSTEM

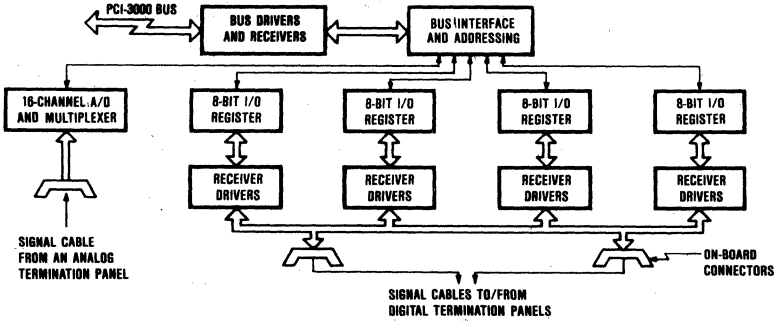
- 16 channels of single-ended input or 8 channels of differential input.
- 12-bit resolution.
- Up to 2000 readings per second (internal storage)
- Up to 30 readings per second (returned to host)
- Gain selection by installing precision resistor (G=1 to 250)
- 0.1% full-scale accuracy
- CMRR = 80dB at 60Hz
- $Z_{in} = 10^9\Omega$
- $I_{bias} = 25nA$
- Crosstalk $\geq -100dB$

DESCRIPTION

The PCI-3301 series of I/O boards provides a mixture of digital input/output points and analog input channels for PCI-3000 systems.

The 32 digital points may be jumper-strapped for input or output on a byte basis. The standard signal levels are TTL input and buffered TTL driver outputs. Input/output cables mate directly to digital isolation panels for handling high voltage AC or DC discrete signals.

Two versions of the PCI-3301 series are offered. The PCI-3301-2 has 16 single-ended analog inputs. The 3301-3 has 8 differential analog inputs. The input gain may be user-selected by insertion of a precision resistor.



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BURR-BROWN®

PCI-3302-1

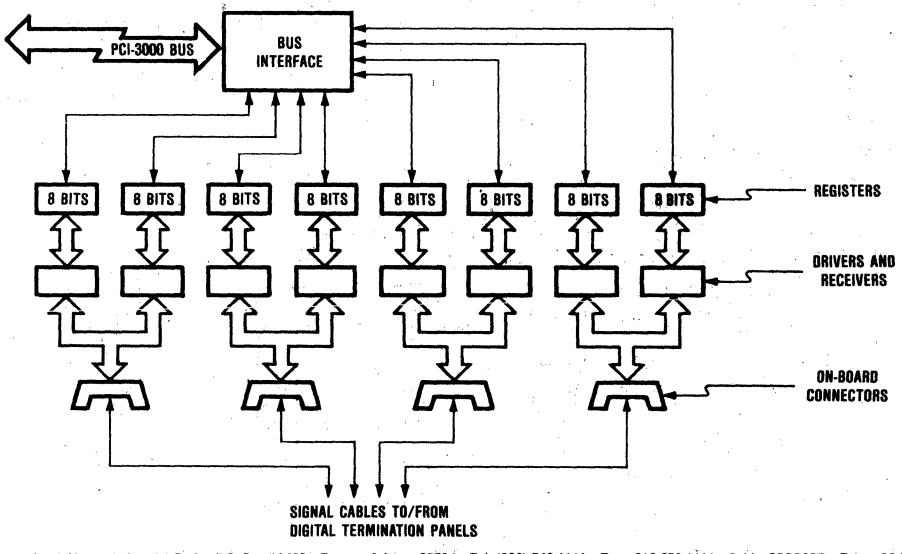
64-POINT DIGITAL INPUT/OUTPUT BOARD

FEATURES

- 64 TTL level input/output points.
- Eight 8-bit digital I/O registers, each jumper configured for input or output.
- Contents of output register may be read back.
- Input or Output configuration may be read by software.
- Output registers provide 24mA of sink current and 15mA of source current.
- Compatible with PCI-3701 signal conditioning/screw termination panels.
- Compatible with PCI-3706 high voltage/high current isolated signal conditioning panels.
- Read or set bits, bytes, or words at the rate of up to 30 per second.

DESCRIPTION

The PCI-3302-1 is an I/O board for the PCI-3000 System that provides 64 buffered TTL level digital inputs or outputs. These bits are organized into eight, 8-bit wide registers, each of which is jumper-selectable as an input or an output byte. However, higher voltage signals and high voltage isolation may be obtained by using external termination panels, such as the PCI-3706-1, along with the PCI-1100 Series Optoisolators.



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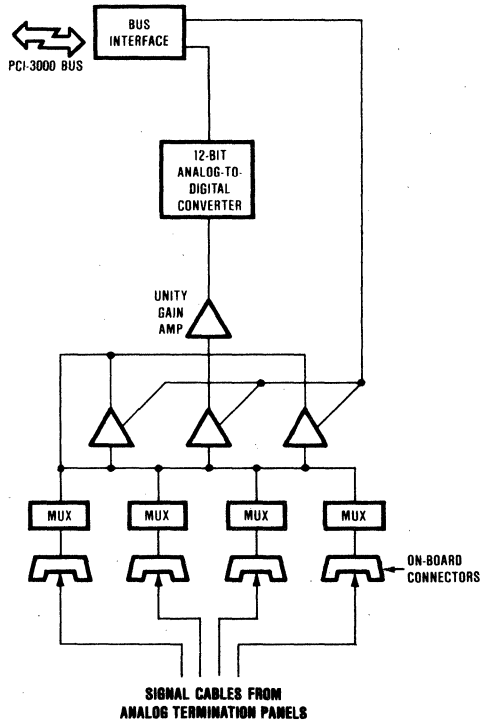
BURR-BROWN®

PCI-3303 Series

64-CHANNEL ANALOG INPUT BOARD

FEATURES

- 64 Channels of single-ended input or 32 channels of differential input.
- 12-bit resolution.
- System accuracy of 0.1% full scale.
- $Z_{in} = 10^{10}\Omega$
- $I_{bias} = 10nA$
- 4 programmable gains—1, 10, 100, 1000 (can be configured for other gains)
- Converter input range is ±10V.
- May be user jumpered for ±5V or 0 to 10V.
- Can be configured for current input
- Up to 2000 readings per second into internal memory
- Up to 30 readings per second returned to host
- Connects through cables to analog signal conditioning/screw termination panels. These panels provide capability for installation of signal filtering, current loop input, voltage division and surge suppression components.



DESCRIPTION

The PCI-3303 Series of I/O boards for the PCI-3000 System provide up to 64 channels of single-ended or 32 channels of differential analog input. Analog input is obtained by selecting one of the input channels using an analog multiplexer and converting the voltage to a digital value with a 12-bit, successive-approximation, analog-to-digital converter. One of four amplifier gains may be selected for each conversion, allowing a full scale input range of ±10mV to ±10V.

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BURR-BROWN®

PCI-3304 Series

8-, 4-, AND 2-CHANNEL DIGITAL-TO-ANALOG CONVERTER BOARDS

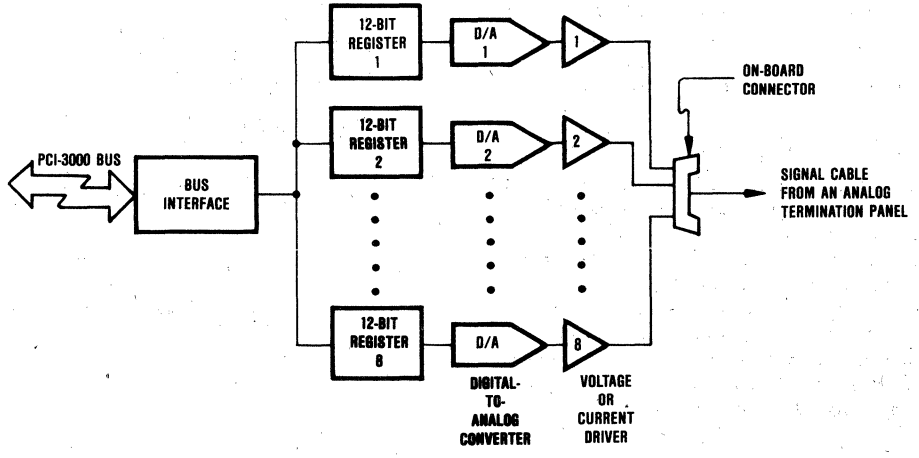
FEATURES

- 12-bit digital-to-analog converter.
- 0.1% full-scale accuracy.
- Output write time as short as 20msec.
- Two versions of output available—voltage (±10V) or current (4mA to 20mA).
- Voltage versions may be user-jumpered for ±5V, 0 to 5V, ±2.5V or 0 to 10V.
- Both output versions available in 2, 4 or 8 channels.

DESCRIPTION

The PCI-3304 series of digital-to-analog converter boards provide up to eight channels of analog output for PCI-3000 Systems. Each output is directly proportional to a corresponding value loaded into the 12-bit digital register on the interface bus. In addition, the board is available in two, four and eight channel versions.

PCI-3304-1, 8-Channel Voltage Output
PCI-3304-2, 8-Channel Current Output
PCI-3304-3, 4-Channel Voltage Output
PCI-3304-4, 4-Channel Current Output
PCI-3304-5, 2-Channel Voltage Output
PCI-3304-6, 2-Channel Current Output



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BURR-BROWN®

PCI-3305 Series

COUNTER/PULSER OUTPUT ANALOG OUTPUT

FEATURES

- Seven 16-bit counters.
- 8MHz input pulse rate.
- 2MHz pulse-generation rate.
- 125nsec resolution.
- ±0.005% stability.
- Four of seven counters may be set up to count events, measure frequency, output pulse streams.
- Four 12-bit digital-to-analog converters (PCI-3305-1 only).
- Counter functions are compatible with PCI-3706-1 high voltage/high current isolated signal conditioning/screw termination panels.

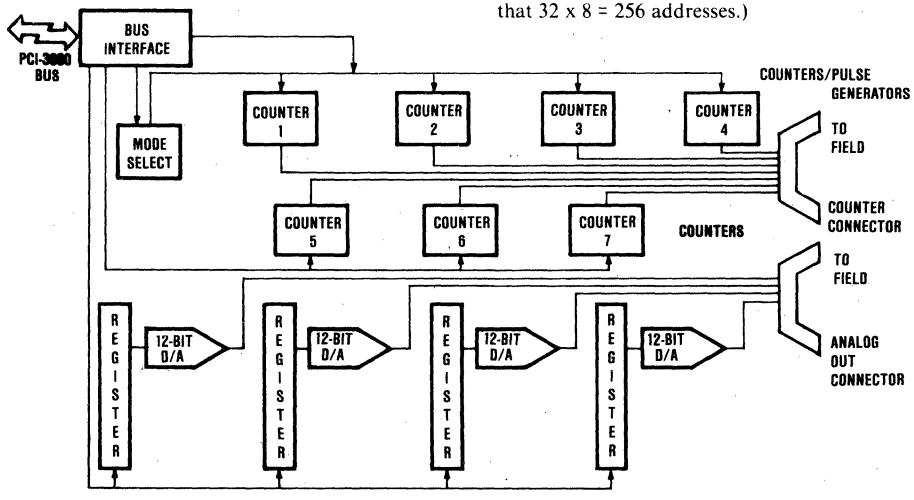
DESCRIPTION

The PCI-3305 series of I/O boards provide a mixture of pulse or event counting, frequency measurement, pulse output and analog output, for PCI-3000 Systems.

All boards in this series include seven 16-bit counter blocks. Three of these counters are used exclusively as event counters. The other four counters may be set up, through software commands, as counters to measure frequency, or as pulse output blocks (either finite or continuous pulse streams).

The PCI-3305-1 board includes four digital-to-analog converters, which provide four channels of analog output voltages.

This board requires 32 addresses. This limits a single master system to 56 counters if entirely configured with PCI-3305 series boards. (Note that 32 x 8 = 256 addresses.)



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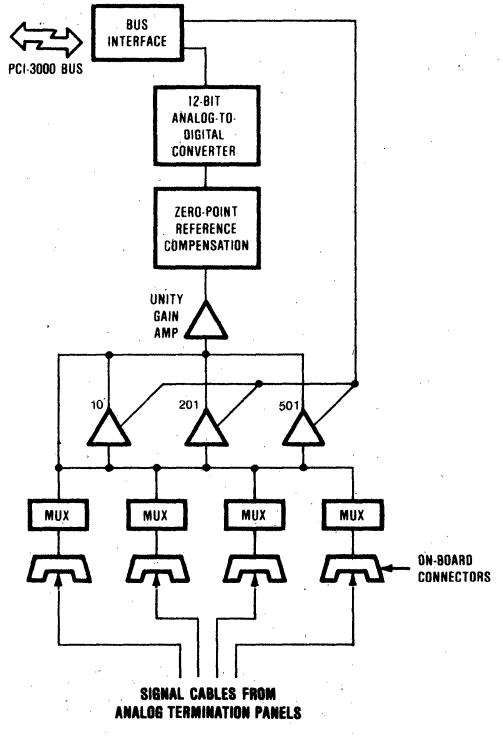
BURR-BROWN®

PCI-3306-1

32-CHANNEL DIRECT THERMOCOUPLE INPUT BOARD

FEATURES

- 32 channels of direct thermocouple input.
- Zero point referencing for J, K, and T types of thermocouples.
- Gain = 1 and 10, noncompensated, input available for nonthermocouple channels.
- ±0.8°C repeatability.
- $I_{bias} = \pm 10nA$
- Crosstalk ≥ −110dB
- CMRR = 92dB at 60Hz
- 12-bit analog-to-digital converter used to obtain reading.
- Firmware can provide linearized results in degrees centigrade.



DESCRIPTION

The PCI-3306-1 is a PCI-3000 System board which provides 32 channels of direct thermocouple inputs. The PCI-3306-1 in conjunction with the PCI-3704-1 termination panel includes a solid state junction compensation network which provides an output that is zero point referenced. Thermocouple types J, K, and T are supported. The PCI-3306-1 must be used with a PCI-3704-1 screw termination panel, which provides the screw terminals for the thermocouples as well as a terminal temperature sensor for the compensation network. The firmware has the capability of returning the values read from the PCI-3306-1 directly in degrees centigrade.

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PCI-3000 SYSTEM FIRMWARE

Command messages are sent to the PCI-3000 from its host computer through any of its three communications ports. These commands are interpreted by decoding programs within the PCI-3000 firmware. A decoded function command causes one of a number of data acquisition or control function programs to execute under the operating system. Each different function returns results to the host computer through the receiving communications port. A standard set of functions within the firmware allows reading or setting of all signal I/O. For most users, all that will ever be needed are the standard functions included in the PCI-3000 firmware. Simply send a command string with a high level statement like PRINT from BASIC and receive a data string back with an INPUT statement.

Since the internal firmware is indeed a small operating system, a user may write his own special-purpose functions that may be down-line loaded and become extensions to the standard firmware. Special functions may also be set up to run continually, or on a timed basis.

Other features of the PCI-3000 firmware include:

—On-line and off-line diagnostics for system trouble-shooting.

—A Console Emulator program which allows direct interaction with the PCI-3000 at the machine level for debugging user programs.

—A set of internal system utilities to allow easy programming of user functions.

The following describes how to work with the PCI-3000 Operating System.

HOW TO WORK WITH A PCI-3000

In the simplest mode of operation, there are basically two steps in using the PCI-3000 to acquire data or generate control signals. The first step is to tell the PCI-3000 what it is you want it to do, the second is to receive the desired data or command acknowledgement back from the PCI-3000. The PCI-3000 accepts command messages and returns data as a string of ASCII alpha-numeric characters. This is very convenient, since most personal and other computers have software that supports transmission and reception of ASCII characters through their communications ports. Once a PCI-3000 is plugged into an RS-232 or RS-422 communications port on your computer, you are ready to send commands and receive data. GPIB (IEEE-488) is a PCI-3000 communications option.

Probably the easiest method of learning how to program your personal computer to communicate with the PCI-3000 is by looking at some specific examples. Once you have worked through these examples, you can begin using the other PCI-3000 function commands summarized in Table II. The following examples are written in the BASIC language. However, the principles shown apply equally to any programming language that you may prefer to use.

Let's start by reading the value of a particular digital input port on the PCI-3000. The following BASIC program steps would achieve that result:

```
10  OPEN "COM:96ØØ" AS #1
20  PRINT #1, "$AØ,1,RD BT (Ø,7)"
30  LINE INPUT #1,A$
40  PRINT A$
```

Let's look at each of these commands in detail.

```
10  OPEN COM AS #1
```

STATEMENT 10 is a typical command to open a communications channel at 9600 baud and designate it as #1. Some operating systems include terms to define parity, etc.

```
20  PRINT #1, "$AØ,1,RD BT (Ø,7)"
```

STATEMENT 20 causes the message

$AØ,1,RD BT (Ø,7) <CR>

to be sent to the PCI-3000 as an ASCII character string, through com port #1. Let's examine each character segment:

$	Tells the PCI-3000 that a new message is starting.
AØ	Tells the PCI-3000 that the message is in the ASCII format, with no error checking.
1	Defines the PCI-3000 id number, which allows a number of PCI-3000s to be connected in a network. (This number could be 1-31).
RD	Tells the PCI-3000 that this function command is from the READ group of commands (RD is the abbreviation for ReaD).
BT	Tells the PCI-3000 that only one bit is to be read (BT is the abbreviation for BiT).
(Ø,7)	Tells the PCI-3000 that the bit to be read is bit number 7 at address number Ø. (More about addresses later.)
<CR>	This character, which is the same as "Carriage Return" or "Enter", is automatically transmitted by your computer. It tells the PCI-3000 that the message has ended and it should now execute the command it received.

```
30  LINE INPUT #1,A$
```

STATEMENT 30 captures the response from the PCI-3000 by using the LINE INPUT command. The actual response from the PCI-3000 might be:

TABLE II. Standard PCI-3000 Firmware Functions (Version 13.5)

Command (Parameters)	Function
Read Group	
RD BY (A)	ReaD BYte at PCI-3000 Bus Address A.
RD BT (A, bit n)	Read BiT n of BYte at PCI-3000 Bus Address A.
RD WD (A)	Read WorD at PCI-3000 Bus Address A (i.e., PCI-3000 Address A is low byte and Address A+1 is high byte).
RD AN (A, channel n)	Read ANalog Channel n at PCI-3000 Bus Address A.
RD ID (A)	Read register IDentification of PCI-3000 Bus Address A.
RD CF [A]	Read register identification of eight PCI-3000 Bus Addresses starting at A.
RD TJ	Read Thermocouple Channel n at PCI-3000 Bus Address A.
(A, channel n)	Thermocouple types—J, K, or T are read by entering TJ, TK or TT respectively.
Write Group	
WR BY (A, byte)	WRite BYte into PCI-3000 bus address A.
WR BS (A, bit n)	Set Bit n of byte at PCI-3000 Bus Address A.
WR BC (A, bit n)	Clear Bit n of byte at PCI-3000 Bus Address A.
WR WD (A, word)	Write WorD into PCI-3000 Bus Address A (low byte) and Address A+1 (high byte).
WR AN (A, byte)	Write Byte into PCI-3000 DAC at bus address A.
Downline Load Group	
LB BL (START, END, xx, xx, ...)	Downline LoaD BLock of data from memory address START to memory address END, xx are data bytes being loaded.
LD FN (CODE1, CODE2, 0, START, END, xx, xx, ...)	Downline LoaD new FuNction, CODE1 and CODE2 are ASCII codes of function command letters. Data bytes (xx) will be loaded in memory from START address to END address.
Continuous Function Control Group	
AC (xx, xx, ...)	Add to Continuous function buffer. xx are arguments and parameters required by function being added.
CC EN	ENable Continuous Function execution.
CC DS	DiSable Continuous Function execution.
CC CL	CLear Continuous Function execution buffer.
CC RP (ENTRY)	RePort on the next continuous function results starting from ENTRY number.
Diagnostic Group	
DR AN port (A, START CHANNEL, No. CHANNELS)	Dump a Diagnostic Report of ANalog channels on "port". These channels are at PCI-3000 Bus Address A beginning with START CHANNEL and continuing for No. CHANNELS)
DR BY port (A, NUMBER)	Dump a Diagnostic Report of digital BYtes on "port" starting with PCI-3000 Bus Address A and continuing for NUMBER bytes.
DL TB (OUT, IN)	Do a Digital Loop Back Test from OUT byte Address to IN byte Address.
High Speed Scan Group	
AS [CL] (A, START CHANNEL, No. CHANNEL {G. COMP.})	Set up for high speed scan. Add No. CHANNEL of consecutive channels beginning with START CHANNEL at Address A to Cycle Table. If so specified, conversions will be done with a gain of G and cold junction compensation specified by COMP. If the argument CL is included, the Cycle Table will be cleared before adding any channels.
TS (A, CHANNEL n, TRIG)	Set up a trigger for high-speed scan. A is the address for the TRIGger, CHANNEL n is a bit number or analog channel number. Analog channels will trigger on a change greater than TRIG. For digital channels TRIG defines a level or transition.
AR [NU] (No. of Channels)	Used to retrieve analog data stored in memory by the analog acquisition scan (AA) function. Data is retrieved using this function successively. No. of channels defines the number of analog channels to be returned. If NU is specified results will not be returned in engineering units.
AA [port] (CYCLE COUNT, DELAY [TRIG])	This will execute an analog acquisition scan of all channels in the Cycle Table defined by the AS command. CYCLE COUNT defines the number of such scans desired while delay defines the time—in milliseconds—between scans. If TRIG is present, the scan will take place only after the trigger (as defined by TS function) has occurred. If port is specified, data is dumped out on the port, otherwise data is saved in memory.
Counter Module Support	
EV EN (A, COUNTER n)	ENable EVent counting at COUNTER n at PCI-3000 Bus Address A.
EV RD [CL] (A, COUNTER n)	ReaD EVent COUNTER n at PCI-3000 Bus Address A. If CL is present then clear the counter after the read.
FR [NW] (A, COUNTER n, exp [m])	Read FRequency at COUNTER n at PCI-3000 Bus Address A, exp is a power of ten and along with M defines the units of frequency desired. If NW is present, the frequency measurement will be initiated by the function will not wait for completion.
FR RD [NW] (A, COUNTER n)	ReaD previously initiated FRequency at COUNTER n at PCI-3000 Bus Address A. if NW is present the function will not wait for the reading to complete.
PG FL (A, COUNTER n. WIDTH, PERIOD number)	Output a finite number of pulses from COUNTER n at PCI-3000 Bus Address A. WIDTH defines pulse width, PERIOD pulse period, number defines number of pulses.
PG ST (A, COUNTER n, WIDTH, PERIOD)	Output a continuous Pulse Stream from COUNTER n at PCI-3000 Bus Address A. Width defines pulse width, PERIOD pulse period.
PG SP (A, COUNTER n)	StoP Pulse stream from COUNTER n at PCI-3000 Bus Address A.

TABLE II. Standard PCI-3000 Firmware Functions (Version 1.35)(Cont)

Miscellaneous Control	
$/C	Puts port into console mode.
X	Removes port from console mode. (Console mode enables echo, and runs PCI-3000 on-line debug program to examine/change memory, etc.
IN	Initializes all modules on the PCI-3000 bus.

!7,O,1 <CR>

where:

!	Marks the beginning of a return message.
1	Means that the response came from master number 1.
O,	Means that the function executed OK (if an error had occurred, an "E" would have been transmitted along with an error code).
1	Means that the status of the digital line in the PCI-3000 that is being interrogated is low (where a "1" means low and a "0" means high).
<CR>	Message terminator.

```
40  PRINT A$
```

In STATEMENT 40, the command PRINT A$ will cause the returned data, to be displayed on the personal computer CRT.

Let's look at another example. We'll make a couple of assumptions to simplify things a little bit. First, assume that the communications channel is already open. Second, assume that the input to the analog input is half of the full-scale value in the positive direction. A command sequence to read an analog channel would be as follows:

```
      "
      "
      "
PRINT #1 "$A0,7,RD AN (4,15)"
LINE INPUT #1 A$
      "
      "
      "
```

The actual response string might be:

!7,O,+1024

The decimal number +1024 represents the analog signal level. The actual value of the response could have been any number in the range -2048 to +2047 which represents the plus and minus full-scale swing of a 12-bit analog-to-digital converter.

The (4,15) in the print statement tells the PCI-3000 that the reading should be taken on channel 15 of the analog-to-digital converter whose control register is at address 4.

You've now seen how to receive both digital and analog inputs from the PCI-3000 into your personal computer. How about the other direction—writing analog and digital data to the PCI-3000's output ports. Writing a byte of data out to a digital output would be accomplished with the following sequence:

```
      "
      "
      "
PRINT #1 "$A0,7,WR BY (1,255)"
LINE INPUT #1 A$
      "
      "
      "
```

The command sets all the bits (255 is the decimal equivalent of all 1's) at the PCI-3000 address 1.

The data string held in A$ contains the value of the output byte that the PCI-3000 has read back after executing the output byte function. This read back provides a check that the data was sent correctly.

As you can probably see, it is very easy to manipulate PCI-3000 inputs and outputs from any high level language without the need of special drivers or software extensions from your computer. It's possible to communicate with the PCI-3000 from any computer or terminal equipped with an RS-232, RS-422 or GPIB communications port.

If you want to write personal computer programs in an Assembler language in order to significantly improve system performance, the PCI-3000 also offers a BINARY protocol. The BINARY protocol is more efficient than the ASCII protocol used in the above examples, but does require a more detailed understanding of the operation of the PCI-3000 and the personal computer. All the function commands available in the ASCII protocol are also available in the BINARY protocol.

TERMINATION PANELS AND HARDWARE

All I/O boards connect to input signals or to output devices through ribbon cable connectors. A family of termination panels is offered to assure reliable, rugged, and convenient connection to the outside world. These termination panels connect directly to the (included) ribbon cables through compatible connectors. Also, these panels provide mounting

facilities for the addition of passive, signal conditioning components for input filters, dropping resistors, current-to-voltage resistors, voltage dividers, and light emitting diodes (LEDs).

All digital input/output boards are compatible with the optically isolated digital input/output signal conditioning panels. This panel supports high isolation (4000V) AC or DC, and high current (3A) drive operation. A selection of optically isolated, digital I/O modules (PCI-1100 Series) plug into these panels to provide a variety of needs. Functions provided by these modules are: DC input, AC input, DC switch output, AC switch output.

Also available are mounting boxes (enclosures) for the termination panels. These enclosures have been styled to match other PCI-3000 enclosures and provide an inexpensive way to make field wiring neat and easily accessible, yet protected.

The termination panel enclosure box mounts in a standard 19″ rack, contains wire troughing, and has access holes for PCI-3000 standard mass-terminated cables.

DIGITAL TERMINATION PANELS

Listed below are the various PCI-3000 termination panels.

PCI-3701-1 16-Channel Digital Termination Panel

Board area available for custom interface circuitry. 16-channel digital input/output with six-foot cable. Can be used with the PCI-3301 series, PCI-3302 series and PCI-3305 series I/O boards.

PCI—3701-2 16-Channel Digital Termination Panel

Same as PCI-3701-1 except straight-through jumpers installed.

PCI-3705-1 Laboratory Termination Panel

Includes 64 analog inputs, 64 digital input/outputs, provision for four analog outputs and seven counter inputs or seven pulse outputs, two push-button switches, four optically-coupled transistor outputs and a variable voltage source. Enclosure and cable assembly are included. Can be used with both the PCI-3302-1 and PCI-3303-3 I/O boards simultaneously. Can also be used with PCI-3301, PCI-3304, and PCI-3305 series boards.

OPTICALLY-ISOLATED TERMINATION PANEL AND ISOLATORS

PCI-3706-1 16-Channel Optically Isolated Digital Input/Output Termination Panel and six-foot cable

Each PCI-3706 panel accepts up to 16 PCI-1100 series digital input/output isolators. Can be used with the PCI-3301 series and PCI-3302 series I/O boards.

PCI-1101 Single DC Input Opto-Isolator

Accepts DC inputs of 10V to 32V and converts to TTL levels. Mounts on PCI-3706-1 Termination Panel.

PCI-1102 Single AC Input Opto-Isolator

Accepts AC inputs of 90V to 140V and converts to TTL levels. Mounts on PCI-3706-1 Termination Panel.

PCI-1103 Single DC Output Opto-Isolator

Switches DC voltages up to 60V at 3A controlled by TTL signals. Mounts on PCI-3706-1 Termination Panel.

PCI-1104 Single AC Output Opto-Isolator

Switches AC voltages of 12V to 140V at 3A controlled by TTL signals. Mounts on PCI-3706-1 Termination Panel.

ANALOG TERMINATION PANELS

PC-3702-1 Analog Input or Output Termination Panel

Board area available for custom interface circuitry. Sixteen single-ended or eight differential analog inputs or eight analog outputs with six-foot cable. Can be used with the PCI-3301-2, PCI-3301-3, PCI-3303 series, PCI-3305-2, and PCI-3304 series I/O boards.

PCI-3702-2 8- or 16-Channel Analog Termination Panel

Same as PCI-3702-1 except straight-through jumpers installed. Can be used with the PCI-3301-2, PCI-3301 series, PCI-3303 series, PCI-3305-2, and PCI-3304 series I/O boards.

PCI-3703-1 32- or 16-Channel Analog Termination Panel

Board area available for custom interface circuitry. 32 single-ended or 16 differential analog inputs with two six-foot cables. Can be used with the PCI-3301-2, PCI-3301-3, PCI—3303 series, PCI-3305-2, and PCI-3304 series I/O boards.

PCI-3703-2 32- or 16-Channel Analog Termination Panel

Same as PCI-3703-1 except straight-through jumpers installed. Can be used with PCI-3301-2, PCI-3301-3, PCI-3303 series, PCI-3305-2, and PCI-3304 series I/O boards.

PCI-3705-1 Laboratory Termination Panel

Includes 64 analog inputs, 64 digital input/outputs, provision for four analog outputs and seven counter inputs or seven pulse outputs, two push-button switches, four optically coupled transistor outputs and a variable voltage source. Enclosure and cable assembly are included. Can be used with both the PCI-3302-1 and PCI-3303-3 I/O board simultaneously. Can also be used with PCI-3301, PCI-3304, and PCI-3305 series boards.

PCI-3707-1 Bridge/Signal Conditioning Termination Panel

8 channel differential connections for Bridge circuits like strain gauges, pressure transducers and RTD's. Can be used with the PCI-3301 series and PCI-3303 series I/O boards.

THERMOCOUPLE TERMINATION PANEL

PCI-3704-1 16-Channel Thermocouple Termination Panel

Sixteen thermocouple inputs. Includes two six-foot cables and an enclosure. Must be used with the PCI-3306-1 I/O board.

COMMUNICATION PRODUCTS

The following products are offered to simplify the task of establishing a communications link between the PCI-3000 and your computer.

PCI-3903-1 IEEE-488 Port

Converts the PCI-3000 series to IEEE-488 (GPIB) communications.

PCI-3906-1 IEEE-488 Upgrade for an IBM PC/PCI-3000 System

This package includes everything necessary to upgrade an IBM PC or XT, Compaq or other IBM compatible personal computers, and a PCI-3000 System to IEEE-488 communications. Included are the PCI-3903-1 Communications Port for the PCI-3000; an IEEE-488 board and software to plug into an expansion slot in the IBM PC or XT; the PCI-1201-1 Cable; and complete documentation.

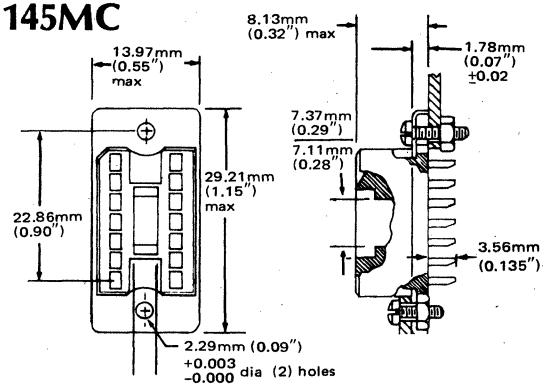
PCI-1201-1	IEEE-488 Cable, 6-foot length
PCI-1201-2	IEEE-488 Cable, 12-foot length
PCI-1202-1	RS-232-C Cable, 3-foot length
PCI-1201-2	RS-232-C Cable, 6-foot length
PCI-1202-3	RS-232-C Cable, 10-foot length
PCI-1202-4	RS-232-C Cable, 20-foot length

ACCESSORIES

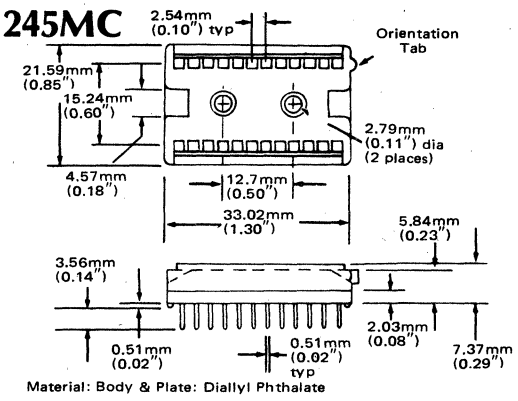
This section contains illustrations and information on the mating connectors and heat sinks available for use with various Burr-Brown products. The type of connector and/or heat sink required by the product is specified within the product data sheet. Prices are available from your nearest Burr-Brown representative.

MATING CONNECTORS

145MC

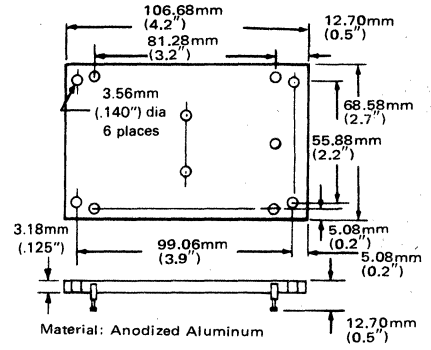


245MC



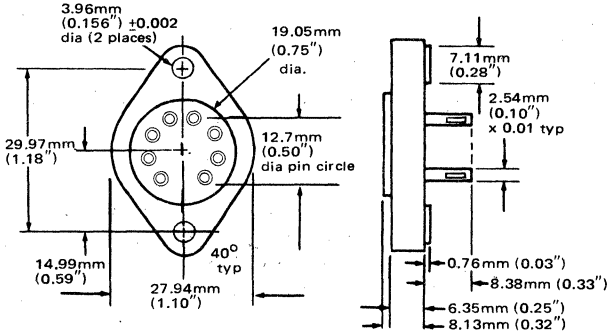
Material: Body & Plate: Diallyl Phthalate

548MC

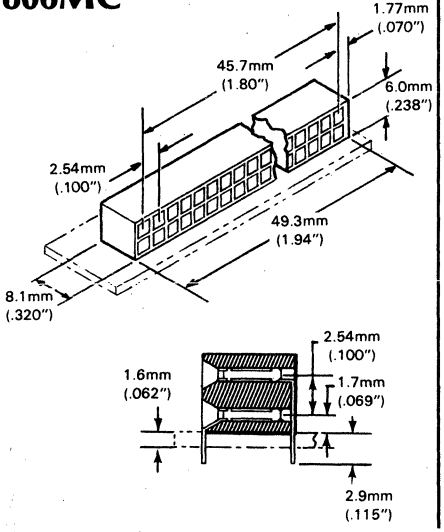


Material: Anodized Aluminum

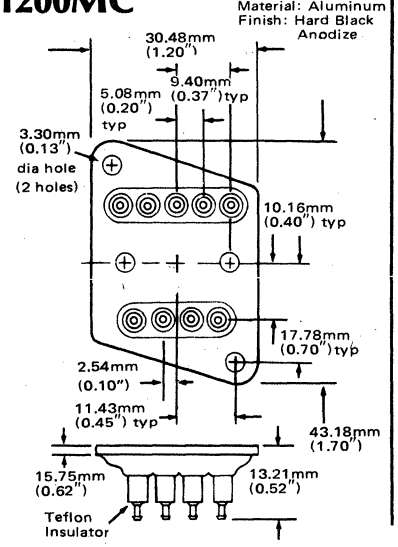
803MC



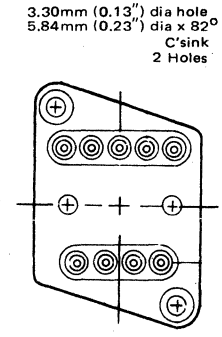
806MC



1200MC



1400MC*

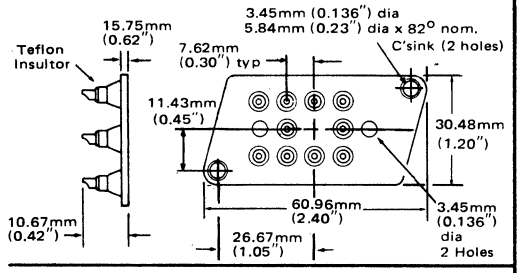


Material: Aluminum
Finish: Hard Black Anodize

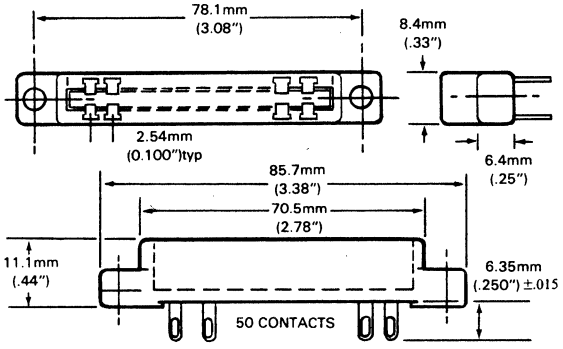
* Identical to 1200MC except for mounting holes.

1500MC

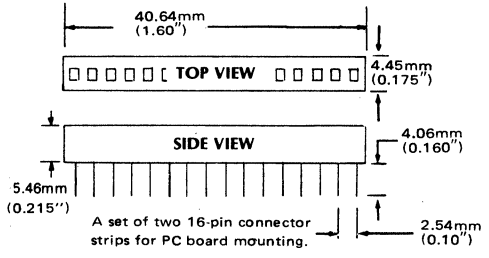
Material: Aluminum
Finish: Hard Black Anodize



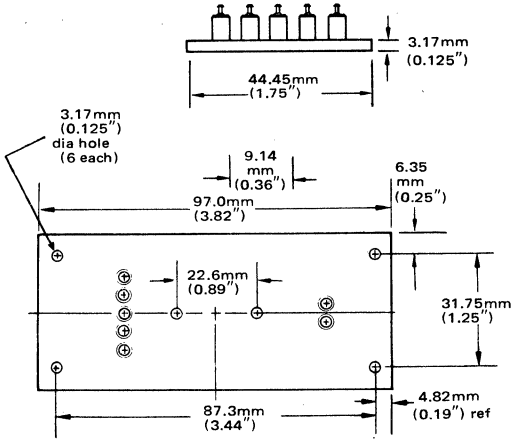
2250MC



2302MC



2800MC

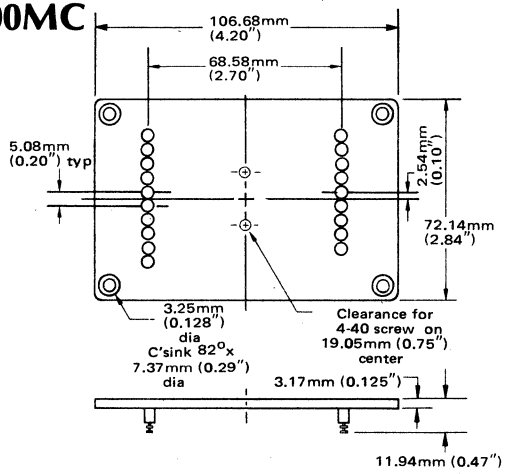


2401MC

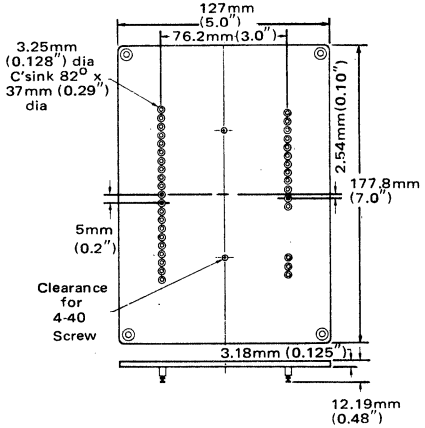
Identical to 2302MC except each connector strip length is 45.72mm (1.80")

A set of four 18-pin connector strips for PC board mounting.

4400MC



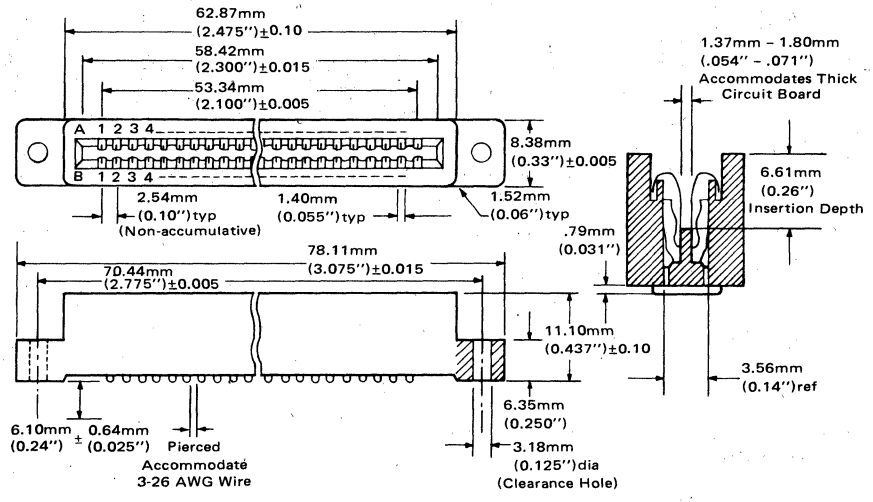
4800MC



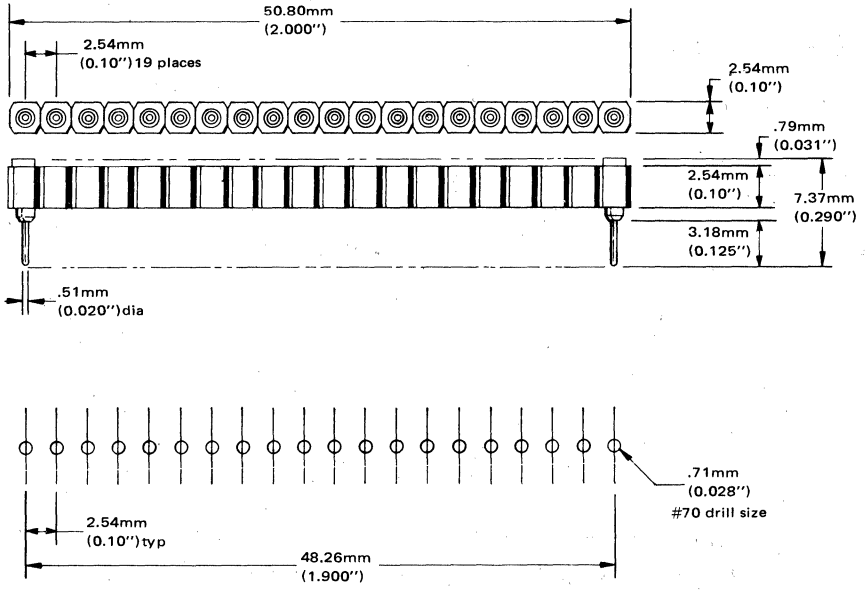
ACCESS

MATING CONNECTORS

2201MC

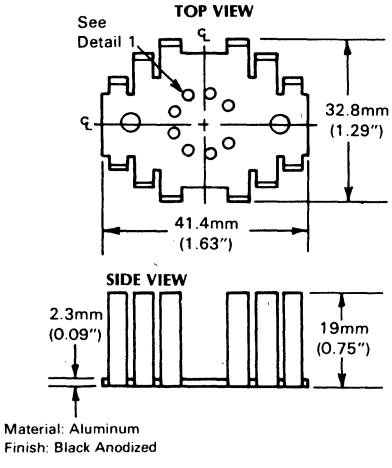


2350MC



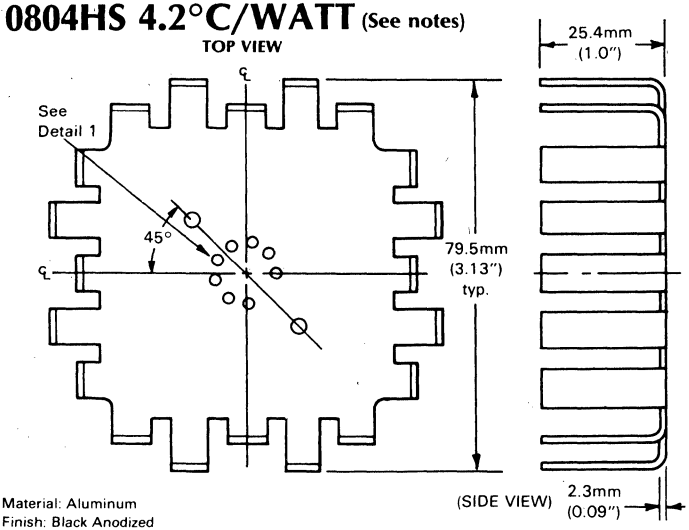
0803HS 12°C/WATT

(See notes)



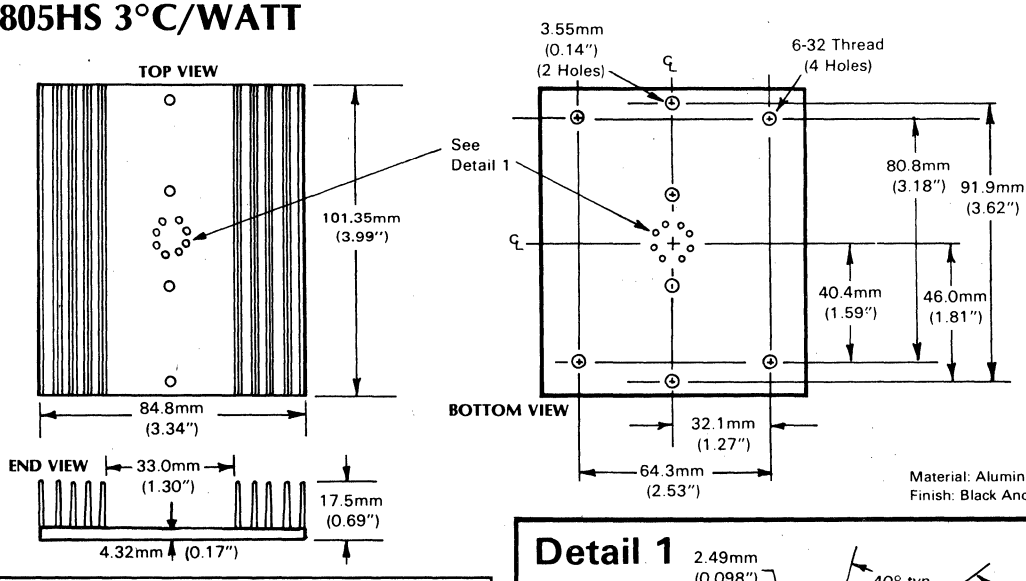
Material: Aluminum
Finish: Black Anodized

0804HS 4.2°C/WATT (See notes)



Material: Aluminum
Finish: Black Anodized

0805HS 3°C/WATT

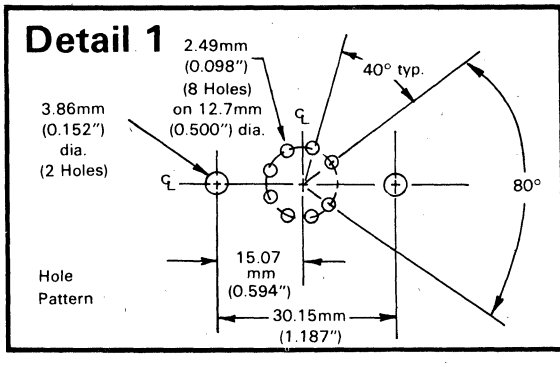


Material: Aluminum
Finish: Black Anodized

***NOTES**

1. Thermal resistance specified are for natural connection. Heatsinks 0803HS and 0804HS are mounted on 6" x 6" x 1/16" G-10 PC board.
2. A thin-film of heatsink compound (Dow Corning 340 or equivalent) between the heatsink and the TO-3 device is recommended.

Detail 1



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CUSTOMER PRICE LIST

Prices in U.S. dollars. F.O.B. Tucson, Arizona Quantity discounts available. **Effective September 1, 1984**

Model Number	1-9	10-24	25-99	100-249
0025MK	1.00	1.00	1.00	
0100MS	11.80	11.80	11.80	9.85
0145MC	4.65	4.10	3.60	
0432MC	8.00	8.00	6.00	5.20
0546	98.50	98.50	98.50	
0548MC	26.00	26.00	26.00	
0549	62.00	62.00	62.00	
0550	67.50	67.50	67.50	
0551	69.50	69.50	69.50	
0552	75.50	75.50	75.50	
0553	97.38	97.38	97.38	
0554	122.25	122.25	122.25	
0556	155.00	155.00	155.00	
0560	68.75	68.75	68.75	
0561	75.10	75.10	75.10	
0562	97.38	97.38	97.38	
0700	57.50	57.50	57.50	
M	60.00	60.00	60.00	
U	50.00	50.00	50.00	
UM	57.50	57.50	57.50	
0710	64.25	64.25	64.25	
0722	49.95	49.95	37.75	34.50
BG	60.35	60.35	49.20	44.85
MG	54.35	54.35	43.55	38.80
0724	66.65	66.65	52.65	48.55
0803HS	3.30	3.30	3.00	2.70
MC	4.95	4.95	4.10	4.10
0804HS	4.85	4.85	4.00	4.00
0805HS	16.50	16.50	16.50	
0806MC	19.00	19.00	19.00	
2014MC	15.00	15.00		
2020MC	8.00	8.00		
2026MC	25.00	25.00		
2201MC	28.00	28.00	28.00	
2220MC	8.00	8.00	8.00	
2240MC	15.00	15.00	15.00	
2250MC	18.00	18.00	18.00	
2302MC	7.75	7.75	7.75	
2350MC	13.00	13.00	13.00	
2360MC	9.00	9.00	9.00	
2525MC	25.50	25.50		
3271/25	195.00	195.00	195.00	
3291/14	113.00	113.00	113.00	
3292/14	113.00	113.00	113.00	
3293/14	99.00	99.00	99.00	
3329/03	38.60	38.60	33.00	24.00
3354/25	155.00	155.00	155.00	
3355/25	118.00	118.00	118.00	
3356/25	101.00	101.00	101.00	
3430J	123.00	123.00	123.00	
K	123.00	123.00	123.00	
3450	229.00	229.00	229.00	

Model Number		1-9	10-24	25-99	100-249
3451		217.00	217.00	217.00	
3452		217.00	217.00	217.00	
3455		217.00	217.00	217.00	
3500A		10.30	10.30	8.15	6.40
B		17.60	17.60	14.45	10.85
C		22.45	22.45	18.65	14.20
E		36.25	36.25	28.00	22.25
MP	*	36.25	36.25	28.00	22.25
R		21.25	21.25	16.60	12.50
R/883B		20.00	20.00	18.00	17.00
R/MIL	†	30.00	30.00	24.00	23.00
RQ		27.50	27.50	22.50	18.00
S		33.00	33.00	25.25	21.20
SQ		44.50	44.50	34.70	29.50
T		53.25	53.25	41.00	33.60
TQ		71.00	71.00	56.60	48.00
U/883B		15.00	15.00	13.00	12.00
3501A		5.95	5.95	4.85	3.85
AQ		9.25	9.25	7.30	6.10
B		12.20	12.20	10.10	7.95
BQ		15.75	15.75	13.40	11.10
C		15.95	15.95	13.25	11.20
CQ		20.60	20.60	17.50	14.45
R		17.50	17.50	15.60	11.70
S		25.50	25.50	20.75	16.95
3507J		12.95	12.95	10.75	9.25
JQ		17.35	17.35	13.95	12.35
3508J		10.75	10.75	8.65	7.75
3510AM		9.35	9.35	7.50	5.95
BM		11.85	11.85	9.40	7.45
CM		18.25	18.25	14.25	11.60
SM		18.25	18.25	14.25	11.60
VM/883B		30.00	25.00	21.00	16.00
VM/MIL	†	45.00	35.00	29.00	22.00
3521H		23.95	23.95	19.45	15.70
J		34.25	34.25	25.90	21.25
JQ		45.15	45.15	34.65	29.40
K		51.40	51.40	38.85	34.28
L		72.40	72.40	55.25	47.00
R		84.25	84.25	68.80	55.70
RQ		110.00	110.00	95.00	82.65
3522J		17.85	17.85	14.35	11.75
K		23.50	23.50	19.40	16.00
L		32.75	32.75	25.25	21.10
S		46.30	46.30	37.30	29.85
SQ		61.65	61.65	51.95	43.65
3523J		33.35	33.35	26.25	21.65
JQ		44.00	44.00	37.00	31.50
K		39.70	39.70	32.95	27.55
L		47.60	47.60	37.80	31.80
LQ		64.00	64.00	54.50	48.95
3527AM		16.25	16.25	12.70	10.95
AMQ		21.80	21.80	17.15	14.85
BM		21.75	21.75	16.50	14.65
BMQ		26.75	26.75	22.05	19.25
CM		33.15	33.15	26.75	23.30

* Prices for the 3500MP are for matched pairs.
† Qualification reports $40 each.
All prices subject to change without notice.
Minimum order $75.

CUSTOMER PRICE LIST

Prices in U.S. dollars. F.O.B. Tucson, Arizona Quantity discounts available. **Effective September 1, 1984**

Model Number	1-9	10-24	25-99	100-249
3528AM	20.25	20.25	15.85	12.95
AMQ	27.05	27.05	21.55	17.45
BM	24.85	24.85	19.35	17.55
BMQ	33.00	33.00	25.95	23.60
CM	30.25	30.25	24.15	21.90
CMQ	40.95	40.95	33.65	29.00
3542J	9.75	9.75	8.50	6.50
JQ	15.00	15.00	13.00	11.00
S	15.80	15.80	14.00	12.65
SQ	22.45	22.45	18.75	17.50
3550J	31.20	31.20	25.00	21.45
K	39.75	39.75	31.25	25.50
S	57.80	57.80	46.85	35.70
SQ	78.00	78.00	64.50	51.00
3551J	31.80	31.80	25.25	21.45
S	56.15	56.15	46.25	35.70
SQ	70.00	70.00	60.00	49.00
3553AM	36.00	36.00	28.90	22.45
AMQ	57.00	57.00	50.00	44.00
3554AM	73.20	73.20	57.70	47.70
AMQ	90.00	90.00	74.00	65.00
BM	83.80	83.80	69.30	56.15
BMQ	105.00	105.00	90.00	77.00
SM	97.60	97.60	78.80	66.30
SMQ	130.00	130.00	110.00	94.50
3571AM	72.45	72.45	54.00	48.00
AMQ	98.00	98.00	79.00	69.00
3572AM	83.00	83.00	64.00	54.50
3573AM	36.00	36.00	26.50	25.00
3580J	62.00	62.00	47.50	41.00
3581J	93.45	93.45	69.85	61.00
3582J	101.50	101.50	87.40	71.00
JQ	135.00	135.00	119.00	104.00
3583AM	100.00	100.00	85.00	70.00
AMQ	140.00	140.00	118.00	103.00
JM	95.00	95.00	80.00	65.00
3584JM	94.50	94.50	72.50	65.50
JMQ	129.50	129.50	109.00	98.00
3606AG	105.00	105.00	95.00	87.00
AM	121.00	121.00	110.00	98.50
BG	137.00	137.00	126.50	113.85
BM	167.00	167.00	153.65	137.00
3626AP	33.60	33.60	24.30	20.85
BP	35.91	35.91	27.20	22.65
CP	41.35	41.35	34.20	27.85
3627AM	12.50	12.50	9.85	9.15
BM	16.75	16.75	12.60	11.25
3629AM	32.65	32.65	26.15	23.05
AP	29.25	29.25	24.20	21.45
BM	39.60	39.60	31.00	26.35
BP	37.30	37.30	26.50	24.80
CM	46.35	46.35	36.75	30.60
CP	41.40	41.40	34.20	27.85
SM	46.35	46.35	36.75	30.60
3630AM	44.00	44.00	34.00	28.00
BM	62.25	62.25	48.70	41.15
CM	95.00	95.00	72.25	64.50
SM	95.00	95.00	72.25	64.50
3650HG	56.25	56.25	42.80	33.75
JG	73.15	73.15	55.15	46.70
KG	88.90	88.90	73.35	65.00
MG	50.40	50.40	36.60	32.00
3652HG	73.15	73.15	57.35	46.70
JG	88.90	88.90	69.70	64.00
MG	57.25	57.25	47.25	42.80

Model Number	1-9	10-24	25-99	100-249
3656AG	86.35	86.35	69.00	57.85
BG	106.75	106.75	85.35	77.85
HG	76.25	76.25	61.00	51.00
JG	81.30	81.30	65.00	54.50
KG	99.95	99.95	79.95	66.95
4084/25	167.00	167.00	167.00	
4085BM	82. 00	82.00	73.50	59.00
KG	71.00	71.00	60.65	49.50
SM	103.00	103.00	94.50	75.50
4115/04	66.30	66.30	52.50	48.75
4127JG	50.75	50.75	39.40	34.40
KG	58.45	58.45	49.45	43.90
4203J	36.25	36.25	26.00	19.60
K	49.65	49.65	42.75	34.80
S	77.00	77.00	59.00	53.00
SQ	102.50	102.50	82.00	74.00
4204J	68.00	68.00	59.95	51.00
K	88.75	88.75	79.55	64.50
S	101.00	101.00	94.00	82.00
SQ	134.00	134.00	129.00	116.00
4205J	31.95	31.95	26.00	19.95
K	46.50	46.50	37.85	30.25
S	66.45	66.45	52.00	40.00
SQ	88.35	88.35	71.85	56.65
4206J	48.45	48.45	39.95	30.25
K	68.80	68.80	56.65	42.25
4213AM	29.35	29.35	23.45	18.90
AMQ	36.70	36.70	30.60	25.50
BM	42.50	42.50	33.40	28.30
SM	55.00	55.00	46.90	37.75
UM	31.00	31.00	26.00	23.00
UM/883B	43.00	43.00	37.00	29.00
VM	45.00	45.00	39.00	29.00
VM/883B	60.00	60.00	49.00	38.00
VM/MIL †	65.00	65.00	53.00	42.00
WM	60.00	60.00	49.00	38.00
WM/883B	75.00	75.00	62.00	48.00
4214AP	25.25	25.25	21.25	16.80
BP	37.45	37.45	31.20	27.00
RM	30.50	30.50	24.95	23.35
SM	49.40	49.40	42.00	36.75
4301	90.75	90.75	74.50	64.70
4302	52.55	52.55	39.70	32.15
4340	90.75	90.75	71.40	64.20
4341	29.20	29.20	24.05	17.95
4423	24.20	24.20	19.50	16.65
ADC10HT	495.00	495.00	455.00	
HT-1	385.00	385.00	345.00	
ADC60-12	337.00	337.00	337.00	
ADC71JG	129.00	129.00	121.00	93.00
KG	161.00	161.00	151.00	116.00
ADC72AM	207.00	207.00	194.00	149.00
BM	258.00	258.00	242.00	186.00
JM	173.00	173.00	162.00	125.00
KM	216.00	216.00	202.00	155.00
ADC731J	556.00	556.00	556.00	
K	654.00	654.00	654.00	
ADC73J	456.00	456.00	456.00	
K	543.00	543.00	543.00	
ADC76JG	229.00	229.00	215.00	165.00
KG	265.00	265.00	244.00	199.00

† Qualification reports $40 each.
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Minimum order $75.

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Prices in U.S. dollars. F.O.B. Tucson, Arizona Quantity discounts available. **Effective September 1, 1984**

Model Number	1-9	10-24	25-99	100-249
ADC803BM	259.00	239.00	214.00	175.00
CM	299.00	278.00	249.00	199.00
ADC80AG-10	85.00	85.00	68.00	46.00
AG-12	87.00	87.00	69.00	48.00
AGZ-12	87.00	87.00	69.00	48.00
ADC82AG	65.00	65.00	52.00	44.00
AM	94.00	94.00	75.00	63.00
AMQ	127.00	127.00	110.00	
ADC84KG-10	105.00	105.00	84.00	70.00
KG-12	115.00	115.00	92.00	77.00
ADC85-10	143.00	143.00	115.00	
-12	150.00	150.00	120.00	
C-12	132.00	132.00	106.00	
CQ-12	193.00	193.00	159.00	
Q-10	172.00	172.00	139.00	
Q-12	206.00	206.00	165.00	
ADC87	240.00	240.00	225.00	216.00
/883B	335.00	335.00	294.00	270.00
/MIL †	415.00	415.00	415.00	390.00
U	172.00	172.00	160.00	150.00
U/883B	206.00	206.00	190.00	180.00
ADC87V	220.00	220.00	205.00	195.00
V/883B	270.00	270.00	250.00	230.00
V/MIL †	385.00	385.00	385.00	345.00
BOOK-01	33.50			
Operational Amplifiers—Design and Applications				
BOOK-02	33.50			
Applications of Operational Amplifiers—Third Generation Techniques				
BOOK-03	29.50			
Function Circuits—Theory and Applications				
BOOK-04	29.50			
Designing With Operational Amplifiers—Applications Alternatives				
DAC10HT	295.00	295.00	230.00	
HT-1	218.00	218.00	170.00	
DAC60-10	147.00	147.00	147.00	
-12	157.00	157.00	157.00	
DAC63BG	108.00	108.00	89.00	83.00
BM	126.00	126.00	107.00	97.00
CG	119.00	119.00	99.00	92.00
CM	139.00	139.00	119.00	107.00
SM	209.00	209.00	182.00	166.00
TM	229.00	229.00	203.00	184.00
DAC70-COB-I	186.00	186.00	154.00	129.00
-CSB-I	186.00	186.00	154.00	129.00
DAC700BH	58.00	58.00	46.00	39.00
KH	48.00	48.00	38.00	32.00
DAC701BH	58.00	58.00	46.00	39.00
KH	48.00	48.00	38.00	32.00
DAC702BH	58.00	58.00	46.00	39.00
KH	48.00	48.00	38.00	32.00
DAC703BH	58.00	58.00	46.00	39.00
KH	48.00	48.00	38.00	32.00
DAC706BH	73.00	73.00	69.00	54.00
KH	63.00	63.00	51.00	44.00
DAC707BH	73.00	73.00	69.00	54.00
KH	63.00	63.00	51.00	44.00
DAC708BH	73.00	73.00	69.00	54.00
KH	63.00	63.00	51.00	44.00
DAC709BH	73.00	73.00	69.00	54.00
KH	63.00	63.00	51.00	44.00

Model Number	1-9	10-24	25-99	100-249
DAC71-CCD-I	55.00	55.00	48.00	42.00
-CCD-V	58.00	58.00	52.00	48.00
-COB-I	55.00	55.00	48.00	42.00
-COB-V	58.00	58.00	52.00	48.00
-CSB-I	55.00	55.00	48.00	42.00
-CSB-V	58.00	58.00	52.00	48.00
DAC72-CCD-V	91.00	91.00	79.00	62.00
-COB-I	79.00	79.00	71.00	55.00
-COB-V	91.00	91.00	79.00	62.00
-CSB-I	79.00	79.00	71.00	55.00
-CSB-V	91.00	91.00	79.00	62.00
C-COB-V	77.00	77.00	67.00	53.00
DAC736J	357.00	357.00	357.00	
K	420.00	420.00	420.00	
DAC73J	357.00	357.00	357.00	
K	420.00	420.00	420.00	
DAC80-CBI-I	34.50	34.50	29.00	22.00
-CBI-V	36.50	36.50	29.00	22.95
-CCD-I	34.50	34.50	31.00	22.00
-CCD-V	36.50	36.50	32.50	22.95
DAC800-CBI-I	23.00	23.00	18.50	15.50
-CBI-V	25.00	25.00	20.00	16.75
P-CBI-V	22.00	22.00	17.60	14.75
DAC80Z-CBI-I	34.50	34.50	29.00	22.00
Z-CBI-V	36.50	36.50	29.00	22.95
Z-CCD-V	36.50	36.50	32.50	22.95
DAC811AH	22.50	22.50	17.90	14.90
BH	28.50	28.50	22.50	18.90
RH	79.00	79.00	63.00	53.00
SH	130.00	130.00	106.00	86.00
DAC812BM	119.00	105.00	95.00	86.00
CM	159.00	141.00	127.00	115.00
DAC82KG	34.00	34.00	27.00	23.00
DAC85-CBI-I	75.00	75.00	60.00	55.00
-CBI-V	78.00	78.00	63.00	58.00
DAC850-CBI-I	33.00	33.00	26.00	22.00
-CBI-V	35.00	35.00	28.00	23.50
DAC851-CBI-I	49.00	49.00	39.00	33.00
-CBI-V	53.00	53.00	42.50	35.50
DAC85C-CBI-V	76.00	76.00	61.00	56.00
LD-CBI-V	145.00	145.00	130.00	
Q-CBI-I	136.00	136.00	121.00	
Q-CBI-V	141.00	141.00	123.00	
DAC87-CBI-I	115.00	115.00	105.00	95.00
-CBI-I/B	125.00	125.00	115.00	105.00
-CBI-V	120.00	120.00	110.00	100.00
-CBI-V/B	130.00	130.00	120.00	110.00
-CBI-V/MIL†	140.00	140.00	130.00	120.00
-CBI-V/MIL† (8300201XC)	195.00	195.00	178.00	165.00
DAC870U	45.00	45.00	40.00	35.00
U/883B	65.00	65.00	60.00	55.00
UL	50.00	50.00	45.00	40.00
UL/883B	70.00	70.00	65.00	60.00
V	80.00	80.00	75.00	67.00
V/883B	90.00	90.00	85.00	75.00
V/MIL †	110.00	110.00	105.00	90.00
VL	85.00	85.00	80.00	72.00
VL/883B	95.00	95.00	90.00	80.00
VL/MIL †	115.00	115.00	110.00	95.00

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CUSTOMER PRICE LIST

Prices in U.S. dollars. F.O.B. Tucson, Arizona Quantity discounts available. **Effective September 1, 1984**

Model Number	1-9	10-24	25-99	100-249
DAC87U-CBI-I	90.00	90.00	80.00	70.00
U-CBI-I/B	100.00	100.00	90.00	80.00
U-CBI-V	95.00	95.00	85.00	75.00
U-CBI-V/BOY	105.00	105.00	95.00	85.00
DAC90BG	19.50	19.50	15.50	13.00
BGQ	26.00	26.00	21.00	17.50
SG	27.00	27.00	22.00	18.00
SGQ	36.00	36.00	29.00	25.00
DIV100HP	30.25	30.25	24.15	18.15
JP	42.25	42.25	36.25	27.75
KP	60.35	60.35	51.95	39.85
DTP-05	195.00	195.00	195.00	
E	195.00	195.00	195.00	
INA101AG	17.95	17.95	13.50	12.75
AM	14.00	14.00	10.50	8.50
CG	23.00	23.00	17.25	16.35
CM	18.40	18.40	13.80	12.85
SG	24.75	24.75	18.50	17.65
SM	19.50	19.50	14.65	13.95
INA104AM	24.25	24.25	19.25	17.95
BM	29.00	29.00	23.25	21.65
CM	37.45	37.45	29.85	27.85
HP	18.75	18.75	14.95	13.95
JP	22.50	22.50	17.95	16.75
KP	29.00	29.00	23.25	21.65
INA258UG	34.00	34.00	34.00	25.00
UG/883B	38.00	38.00	38.00	28.00
UL	37.00	37.00	37.00	27.00
UL/883B	41.00	41.00	41.00	31.00
VG	45.00	45.00	41.00	38.00
VG/883B	54.00	54.00	49.00	46.00
VG/MIL †	70.00	70.00	63.00	60.00
VL	49.00	49.00	45.00	42.00
VL/883B	59.00	59.00	53.00	51.00
VL/MIL †	77.00	77.00	69.00	66.00
WG	58.00	58.00	52.00	49.00
WG/883B	69.00	69.00	62.00	59.00
WG/MIL †	87.00	87.00	78.00	74.00
WL	64.00	64.00	57.00	53.00
WL/883B	76.00	76.00	68.00	64.00
WL/MIL †	96.00	96.00	86.00	81.00
ISO100AP	32.50	32.50	28.75	25.50
BP	35.40	35.40	31.60	28.65
CP	39.50	39.50	36.30	33.60
LOG100JP	43.00	43.00	35.00	30.00
MP10	169.00	169.00	135.00	
MP11	175.00	175.00	140.00	
MP20	336.00	336.00	269.00	
MP22BG	324.00	285.00	259.00	
MP32BG	324.00	280.00	259.00	
CG	405.00	405.00	324.00	
MPC16S	23.21	23.21	20.06	17.00
MPC4D	12.97	12.97	11.21	9.50
MPC800KG	27.86	27.86	23.06	19.22
SG	55.67	55.67	46.07	38.39
MPC801KG	14.50	14.50	12.00	10.00
SG	30.00	30.00	24.83	20.69
MPC8D	23.21	23.21	20.06	17.00
S	12.97	12.97	11.21	9.50
MPY100AG	13.85	13.85	12.45	11.25
AM	10.50	10.50	9.45	8.50
BG	22.45	22.45	20.45	18.65
BM	17.00	17.00	15.45	14.10
CG	33.70	33.70	31.00	28.65
CM	25.50	25.50	23.45	21.70
SG	50.55	50.55	46.50	43.00
SM	38.25	38.25	35.20	32.55
OPA100AM	11.00	11.00	9.00	7.95
BM	14.00	14.00	11.00	9.85
CM	20.00	20.00	16.00	12.00
OPA101AM	35.00	35.00	29.85	23.25
BM	43.50	43.50	37.50	32.75
OPA102AM	37.00	37.00	31.75	24.25
BM	45.00	45.00	38.65	33.50
OPA103AM	10.50	10.50	8.60	6.80
BM	14.20	14.20	11.45	8.95
CM	18.60	18.60	14.85	11.55
DM	29.85	29.85	23.85	18.50
OPA104AM	17.50	17.50	13.95	10.25
BM	23.65	23.65	18.95	14.50
CM	29.50	29.50	23.50	19.00
OPA105UM	25.00	25.00	23.50	22.00
UM/883B	30.00	30.00	28.00	25.00
VM	35.00	35.00	32.00	30.00
VM/883B	43.00	43.00	39.00	35.00
VM/MIL †	55.00	55.00	50.00	45.00
WM	47.00	47.00	42.00	40.00
WM/883B	57.00	57.00	51.00	45.00
WM/MIL †	75.00	75.00	67.00	60.00
OPA106UM	28.00	28.00	25.00	22.00
UM/883B	34.00	34.00	32.00	28.00
VM	38.00	38.00	35.00	32.00
VM/883B	47.00	47.00	43.00	38.00
VM/MIL †	60.00	60.00	55.00	50.00
WM	50.00	50.00	45.00	42.00
WM/883B	61.00	61.00	55.00	50.00
WM/MIL †	80.00	80.00	72.00	65.00
OPA111AM	9.75	9.75	7.95	6.35
BM	15.35	15.35	12.25	9.95
SM	16.85	16.85	13.95	11.95
OPA11HT	49.00	49.00	46.55	39.20
OPA201AG	11.25	11.25	9.25	6.95
BG	15.75	15.75	13.50	10.50
CG	18.35	18.35	15.75	12.35
RG	14.75	14.75	12.70	9.60
SG	21.35	21.35	18.45	14.35
OPA21AJ	20.35	20.35	16.35	13.50
AZ	17.75	17.75	14.45	11.95
BJ	14.85	14.85	11.95	9.95
BZ	12.85	12.85	9.95	8.45
EJ	10.95	10.95	8.85	7.20
EZ	9.40	9.40	7.50	6.25
FJ	8.65	8.65	6.90	5.75
FZ	6.90	6.90	5.55	4.60
GJ	6.25	6.25	5.00	4.15
GZ	4.95	4.95	4.00	3.30

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CUSTOMER PRICE LIST

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Model Number	1-9	10-24	25-99	100-249
OPA27AJ	20.95	20.95	16.70	12.95
AZ	22.25	22.25	17.80	13.80
BJ	14.95	14.95	11.95	9.25
BZ	15.95	15.95	12.80	9.90
CJ	10.95	10.95	8.75	7.00
CZ	11.80	11.80	9.45	7.55
EJ	16.00	16.00	12.80	9.90
EZ	17.00	17.00	13.65	10.60
FJ	10.70	10.70	8.55	6.85
FZ	11.25	11.25	9.00	7.25
GJ	8.20	8.20	6.55	5.25
GZ	8.65	8.65	6.90	5.50
OPA37AJ	20.95	20.95	16.70	12.95
AZ	22.25	22.25	17.80	13.80
BJ	14.95	14.95	11.95	9.25
BZ	15.95	15.95	12.80	9.90
CJ	10.95	10.95	8.75	7.00
CZ	11.80	11.80	9.45	7.55
EJ	16.00	16.00	12.80	9.90
EZ	17.00	17.00	13.65	10.60
FJ	10.70	10.70	8.55	6.85
FZ	11.25	11.25	9.00	7.25
GJ	8.20	8.20	6.55	5.25
GZ	8.65	8.65	6.90	5.50
OPA501AM	53.40	53.40	40.00	32.50
BM	63.00	63.00	47.85	37.85
RM	68.50	68.50	49.25	42.50
SM	82.00	82.00	59.85	49.95
OPA600UM	143.00	143.00	115.00	102.00
UM/883	165.00	165.00	145.00	118.00
VM	180.00	180.00	153.00	126.00
VM/883B	195.00	195.00	166.00	135.00
VM/MIL †	215.00	215.00	185.00	175.00
OPA605AM	64.00	64.00	54.50	48.00
CM	89.00	89.00	74.50	66.75
HG	51.50	51.50	45.00	40.50
KG	76.65	76.65	67.00	57.50
OPA8780	125.00	125.00	99.00	88.00
UM	102.00	102.00	81.00	72.00
UM/883B	135.00	135.00	106.00	95.00
VM/883B	190.00	190.00	151.00	134.00
VM/MIL †	240.00	240.00	190.00	170.00
PCM52JG-V	37.00	37.00	32.50	23.00
PCM53JG-I	37.00	37.00	32.50	23.00
JG-V	37.00	37.00	32.50	23.00
JP-V	29.00	29.00	26.00	19.00
PCM75JG	198.00	198.00	179.00	145.00
KG	249.00	249.00	235.00	189.00
PGA100AG	65.00	65.00	55.00	49.50
BG	72.00	72.00	62.00	54.00
PGA200AG	51.50	51.50	39.95	34.75
BG	57.85	57.85	46.75	41.00
PGA201AG	51.50	51.50	39.95	34.75
BG	57.85	57.85	46.75	41.00
PSX-24	35.00	35.00	35.00	
PWR70	40.00	40.00		20.00
REF101JM	30.90	30.90	27.80	22.50
KM	38.50	38.50	35.00	28.80
RM	33.75	33.75	30.70	25.20
SM	42.35	42.35	38.95	32.40
REF10JM	17.40	17.40	15.65	13.35
KM	21.85	21.85	19.65	16.75
RM	19.95	19.95	17.95	15.35
SM	29.40	29.40	26.35	22.50
RF-500-108	8.00	8.00	7.50	7.00
SDM853	329.00	329.00	329.00	
SDM854AG	210.00	210.00	168.00	
BG	233.00	233.00	187.00	
SDM856JG	181.00	181.00	145.00	
KG	219.00	219.00	175.00	
SDM857JG	194.00	194.00	155.00	
KG	232.00	232.00	186.00	
SHC298AM	6.95	6.95	5.50	4.50
SHC803BM	162.00	143.00	129.00	117.00
CM	184.00	163.00	146.00	133.00
SHC804BM	145.00	129.00	115.00	105.00
CM	159.00	141.00	126.00	115.00
SHC80KP	51.00	51.00	41.00	34.00
SHC85	85.00	79.00	68.00	57.00
ET	129.00	116.00	110.00	
ETQ	179.00	170.00	162.00	
Q	137.00	129.00	110.00	
SHM60	140.00	140.00	140.00	
UAF11	53.60	53.60	40.70	26.40
UAF21	85.50	85.50	78.65	53.35
UAF31	35.20	35.20	27.20	19.35
UAF41	20.85	20.85	14.10	11.50
VFC320BG	15.95	15.95	11.75	8.95
BM	15.60	15.60	11.40	8.75
CG	18.50	18.50	13.65	11.50
CM	16.60	16.60	12.45	10.45
SM	20.65	20.65	15.60	13.40
VFC32BM	14.90	14.90	10.85	8.35
BMQ	19.95	19.95	15.50	11.95
KP	10.15	10.15	8.65	6.15
SM	19.70	19.70	15.00	11.85
SMQ	26.00	26.00	20.00	16.40
UM	15.00	15.00	11.00	7.50
UM/883B	20.00	20.00	16.00	12.50
VM	26.00	26.00	21.00	18.00
VM/883B	35.00	35.00	29.00	23.00
VM/MIL †	66.00	66.00	54.00	43.00
WM	40.00	40.00	35.00	30.00
WM/883B	45.00	45.00	40.00	35.00
VFC42BM	29.65	29.65	25.15	21.95
BP	21.35	21.35	17.35	15.70
SM	36.00	36.00	30.00	24.65
VFC52BM	29.65	29.65	25.00	21.95
BP	21.35	21.35	17.35	15.70
SM	36.00	36.00	30.00	24.65
VFC62BG	15.95	15.95	11.75	8.95
BM	15.60	15.60	11.40	8.75
CG	18.50	18.50	13.65	11.50
CM	16.60	16.60	12.45	10.40
SM	20.65	20.65	15.60	13.40
XTR100AM	38.00	38.00	35.65	28.95
AP	30.00	30.00	27.80	23.85
BM	46.00	46.00	43.35	35.95
BP	36.00	36.00	33.95	29.25

† Qualification reports $40 each.
All prices subject to change without notice.
Minimum order $75.

CUSTOMER PRICE LIST

Prices in U.S. dollars. F.O.B. Tucson, Arizona **Effective September 1, 1984**

MICROCOMPUTER I/O BOARDS

Model Number	1-99
MP1104	895
MP1216	815
-PGA	925
MP6102-0	570
-1	570
MP6202-0	260
-1	175
-2	375
MP6303-8	550
-16	610
-24	660
-32	720
MP6304-0	230
MP6305-4	335
-8	430
MP6309-0	410
-1	290
MP6311-01	410
MP6394-0	320
MP6421-0	375
MP701	365
MP702	625
MP710	450
-NS	395
MP7104	825
MP7105	710
-NS	630
MP7208	885
MP7209	775
-NS	630
MP7216	885
MP7217	775
-NS	630
MP7218	560
MP7408	550
-AO	670
-NS-AO	620
-NS	495
MP7432	650
-AO	770
-NS-AO	720
-NS	595
MP7504	780
MP7608	795
-I	795
MP8001	90
MP8002	30
MP8003	110
MP8004	60
MP8005	40
MP801	365
MP802	625
MP810	450
-AC	450
-DB	495
-LV	395
-NS	395
MP820-05	475
-15	760

Model Number	1-99
MP821-05	575
-15	860
MP830-72	450
-72R	575
MP8304	775
MP8305	650
MP8305-NS	625
MP8316-I	785
-V	685
MP8408	840
MP8409	740
-NS	645
MP8416	910
MP8417	780
-NS	660
MP8418	820
-AO	955
-EXP	610
-ISOE	825
-PGA	950
-PGA-AO	1150
MP8430	950
MP8608	595
-AO	720
MP8616	595
-AO	720
MP8632	680
-AO	795
MPV901	1495
A	1720
P	2020
MPV950D	2840
S	2390
SM50123-001	50
-002	65
-003	75

MICROTERMINALS™

Model Number	1-49
TM25-300HM	325
HT	265
NM	325
NT	265
TM27	250
-12	250
TM70	495
TM71	595
-21	595
-IO	695
-IO-21	695
B-11	1495
B-12	1495
B-21	1495
B-22	1495
B-31	1495
B-32	1495
TM76	495
K	595
TM77	595
-21	595
-IO	695
-IO-21	695
B-11	1495
B-12	1495
B-21	1495
B-22	1495
B-31	1495
B-32	1495
K	695
K-21	695
K-IO	795
K-IO-21	795
TMT-01	18

All prices subject to change without notice.
Minimum order $75.

Prices in U.S. dollars. F.O.B. Tucson, Arizona Effective September 1, 1984

TM900 TRANSACTION PROCESSOR

Model #	Type	Type/Description	1-9
TM900	Base unit	32-terminal configuration: 19" rack mount, central processor PC board, host/console/ link ports, 1 peripheral processor PC board, 2 RS-422/20mA Microterminal™ ports (interface for 32 Microterminals™), standard 115VAC power supply.	7500
	Base unit	64-terminal configuration: same as above, with 1 peripheral processor PC board, and 4 RS-422/20mA Microterminal™ ports (interface for 64 Microterminals™).	8500
	Base unit	96-terminal configuration: same as above, with 2 peripheral processor PC boards, and 6 RS-422/20mA Microterminal™ ports (interface for 96 Microterminals™).	9500
	Base unit	128-terminal configuration: same as above, with 2 peripheral processor PC boards, and 8 RS-422/20mA Microterminal™ ports (interface for 128 Microterminals™).	10,500
PSB100	Option	24VDC battery backup power supply with internal batteries.	1500
TM910	Option	10MB Winchester disk drive.	7680
SM50196	Spare part	Termination assembly.	95
SM50226	Spare part	Peripheral processor board.	2300
SM50231	Spare part	Central processor board.	4250
SM50197	Spare part	Front panel display board.	125
SM50229	Spare part	Power supply.	1200
SM51170	Spare part	Battery backup power supply.	1800

CUSTOMER PRICE LIST

Prices in U.S. dollars. F.O.B. Tucson, Arizona Quantity discounts available. **Effective September 1, 1984**

PCI INTELLIGENT INSTRUMENTATION PRODUCTS

Model #	Type	Type/Description	1-9
PCI-1101	Isolator	DC input opto-isolator (10-32V).	25
PCI-1102	Isolator	AC input opto-isolator (90-140V).	25
PCI-1103	Isolator	DC output opto-isolator, switches up to 60V at 3A.	25
PCI-1104	Isolator	AC output opto-isolator, switches 12-140V at 3A.	25
PCI-1201-1	Cable	IEEE-488 cable, 6 feet long.	85
-2	Cable	IEEE-488 cable, 12 feet long.	95
PCI-1202-1	Cable	RS-232C cable, 3 feet long.	25
-2	Cable	RS-232C cable, 6 feet long.	35
-3	Cable	RS-232C cable, 10 feet long.	40
-4	Cable	RS-232C cable, 20 feet long.	45
PCI-3001-1	Master	System enclosure (85-130VAC) with user manual.	2995
PCI-3001-2	Master	System enclosure (200-260VAC) with user manual.	2995
PCI-3301-2	Board	32-channel digital I/O and 16-channel single-ended analog input.	1395
-3	Board	32-channel digital I/O and 8-channel differential analog input.	1395
PCI-3302-1	Board	64-channel digital I/O.	795
PCI-3303-2	Board	64-channel single-ended analog input.	1695
-4	Board	32-channel differential analog input.	1695
PCI-3304-1	Board	8-channel ±10V analog output.	1595
-2	Board	8-channel 4-20mA analog output.	1595
-3	Board	4-channel ±10V analog output.	1125
-4	Board	4-channel 4-20mA analog output.	1125
-5	Board	2-channel ±10V analog output.	870
-6	Board	2-channel 4-20mA analog output.	870
PCI-3305-1	Board	4-channel analog output and 7 counter input/pulse output.	1295
-2	Board	7 counter input/pulse output.	790
PCI-3306-1	Board	32-channel J, K, T thermocouple input.	2390
PCI-3701-1	Panel	16-channel digital termination with space for custom input circuits.	170
-2	Panel	16-channel digital termination with straight-through jumpers.	180
PCI-3702-1	Panel	8/16-channel analog termination with space for custom input circuits.	170
-2	Panel	8/16 channel analog termination with straight-through jumpers.	180
PCI-3703-1	Panel	32/16-channel analog termination with space for custom input circuits.	195
-2	Panel	32/16-channel analog termination with straight-through jumpers.	230
PCI-3704-1	Panel	16-channel thermocouple termination.	495
PCI-3705-1	Panel	Laboratory termination, with 64 analog in, 64 digital I/O, 4 analog out, 7 counter/pulse, controls and PS terminals.	1150
PCI-3706-1	Panel	16-channel opto-isolator digital I/O requires PCI-1100 series isolators.	160
PCI-3901-1	MPU	PC board microcomputer, without EPROM and RAM.	995
-2	MPU	PC board microcomputer, with latest revision EPROM and RAM.	1465
PCI-3902-1	Firmware	Latest revision firmware, with EPROMs and RAM IC's.	470
PCI-3903-1	IEEE	IEEE-488 communication port.	198
PCI-3904-1	Manual	Additional user's manual.	50
PCI-3905-1	Rack	Rack mount slide for master enclosure and expansion enclosure.	85
PCI-3906-1	IEEE	IEEE-488 upgrade for IBM PC, XT; includes PCI-3903 and PCI-1201-1 plus 488 board and software for PC, XT.	990
PCI-3907-1	Rack	Rack mount enclosure for termination panels.	49
PCI-3908-1	Cover	Cover for rack mount termination panel enclosure.	25
PCI-3909-1	Expansion	System enclosure (85-130V).	1495
-2	Expansion	System enclosure (200-260V).	1495
PCI-3910-1	8k RAM	Memory expansion IC's.	195

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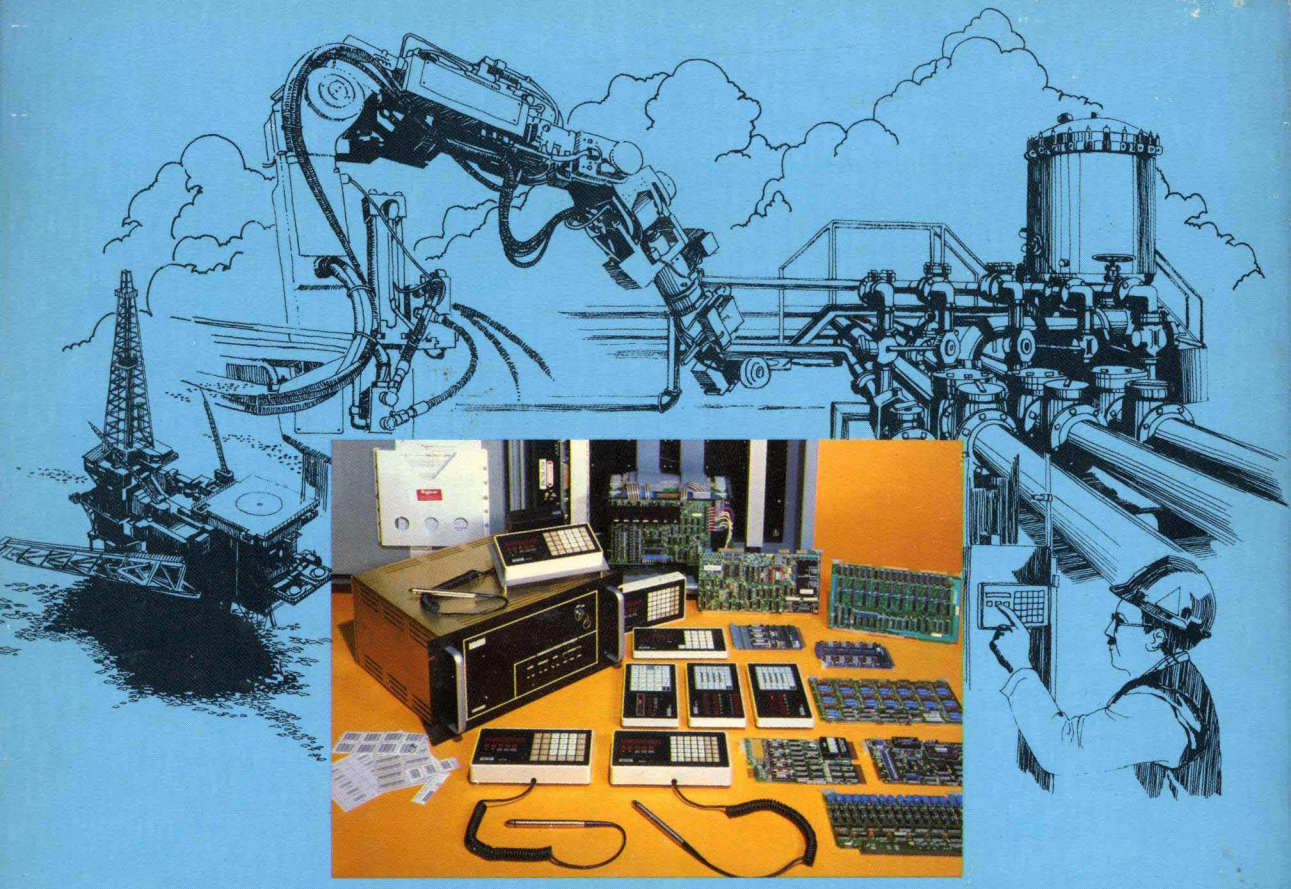

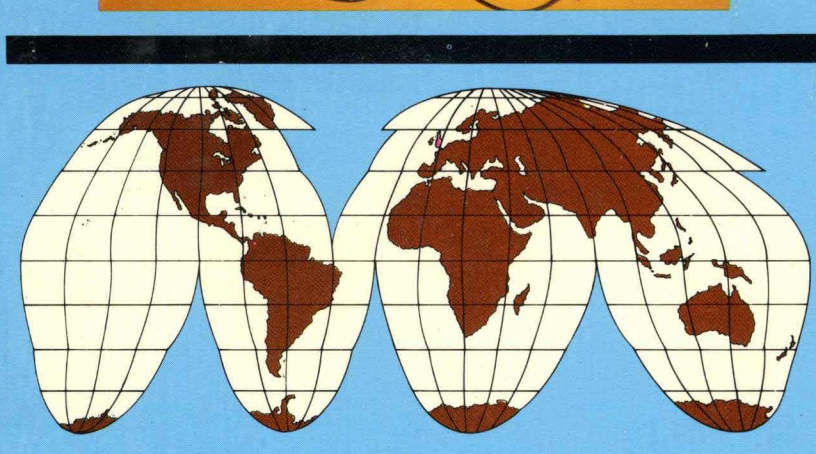

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