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Integrated Circuits Data Book Supplement

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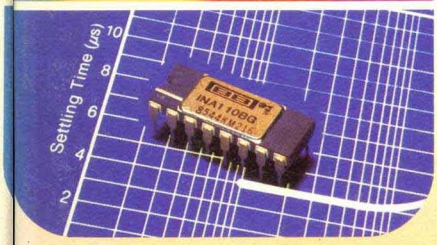

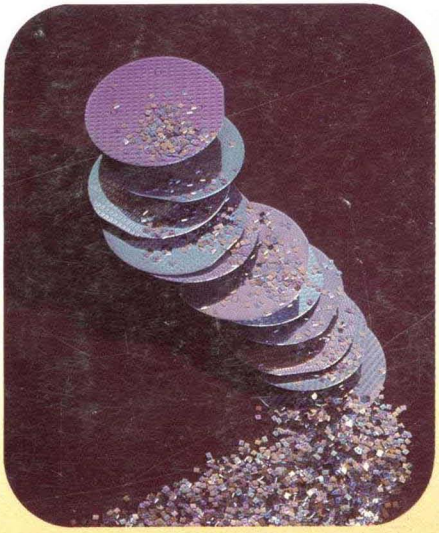

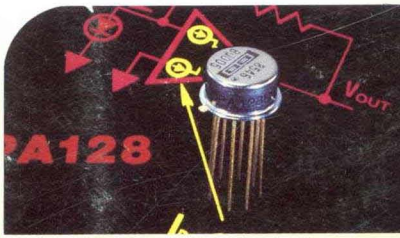

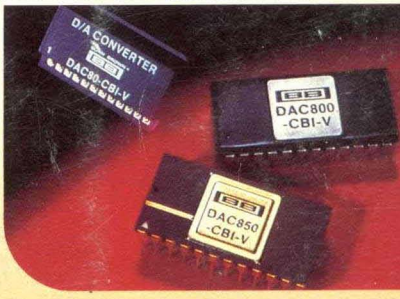

Operational Amplifiers
Instrumentation Amplifiers
Isolation Amplifiers
Analog Circuit Functions
Military Products

A/D Converters
D/A Converters
Sample/Hold Converters
Multiplexers
Power Supplies

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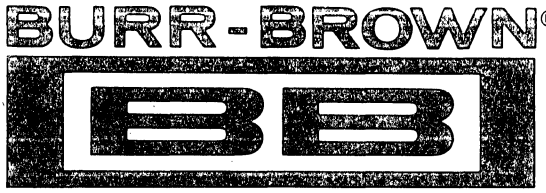
MODEL INDEX

DSPlay™ Burr-Brown Corp.

A complete price list for these products is located inside the back cover.



SUPPLEMENT TO
INTEGRATED CIRCUITS DATA BOOK

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LI-340

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INTRODUCTION

This supplement to the Burr-Brown Integrated Circuits Data Book contains product data sheets on new products that have been developed and introduced since the Data Book was published. Product lines such as Operational, Instrumentation, and Isolation Amplifiers, Analog-to-Digital and Digital-to-Analog Converters, Military Products, Modular Power Supplies, Data Entry and Display Terminals, Microcomputer I/O Systems, and Data Acquisition Components are represented.

The Model Index list on the inside of the front cover refers to models and page numbers in both the Data Book and this supplement. Products in this supplement are set in bold type.

A Selection Guide beginning on page iii contains a summary of performance characteristics of all products in both the Data Book and this supplement.

A complete list of all Burr-Brown offices and sales representatives can be found on the inside of the back cover. If you have questions on any of our products please contact the nearest Burr-Brown office or sales representative.

SELECTION GUIDE
HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

GENERAL PURPOSE

These moderately priced FET and bipolar op amps offer good performance over a wide range of parameters. These are good options when a special function op amp is not required. You can be confident that Burr-Brown's quality and reliability are inherent in their design.

GENERAL PURPOSE												
		Offset Voltage, max		Bias Current	Open Loop	Frequency Response		Rated Output, min				
Description	Model	At 25°C, (±mV)	Temp Drift, (±μV/°C)	(25°C), max (nA)	Gain, min (dB)	Unity Gain (MHz)	Slew Rate (V/μsec)	(±V)	(±mA)	Temp Range[1]	Package	Page
Low Power	OPA21GZ	0.5	5	50	114	0.3	0.2	13.6	1.3	Ind	DIP	1-13
	OPA21EZ	0.1	1	25	120	0.3	0.2	13.7	1.4	Ind	DIP	1-13
Switchable Input	OPA201AG	0.5	5	50	114	0.5	0.1	13.5	5	Com	DIP	1-87
	OPA201BG	0.2	2	40	114	0.5	0.1	13.5	5	Com	DIP	1-87
	OPA201CG	0.1	1	25	120	0.5	0.1	13.5	5	Com	DIP	1-87
	OPA201SG	0.2	2	40	114	0.5	0.1	13.5	5	MIL	DIP	1-87
Low Cost FET	OPA121KP*	3	10	±0.010	106	2	2	10	5	Com	DIP	1-67
	OPA121KM	2	10	±0.005	110	2	2	10	5	Com	TO-99	1-67
Wide Temp Range	OPA11HT	5	5[2]	±25	94	12.0	7.0	10	15	−55°C to +175°C	TO-99	1-9
	OPA27HT	0.05	0.25[2]	1μA	120	6	1.9	12	16[2]	−55°C to +200°C	TO-99	1-29
	OPA37HT	0.05	0.25[2]	1μA	120	36	11.9	12	16[2]	−55°C to +200°C	TO-99	1-29
	OPA111HT	0.5	8[2]	0.002	114	2	2	10	5	−55°C to +200°C	TO-99	1-63

NOTES: (1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. (2) Typical.

LOW DRIFT

Low offset voltage drift vs temperature performance in both FET and bipolar input types is obtained by our sophisticated drift compensation techniques. First, the drift is measured and then special laser trim techniques are used to minimize the drift and the initial offset voltage at 25°C. Finally, "max drift" performance is retested for conformance with specifications.

LOW DRIFT (≤5μV/°C)												
		Offset Voltage, max		Bias Current	Open Loop	Frequency Response		Rated Output, min				
Description	Model	At 25°C (±mV)	Temp Drift (±μV/°C)	(25°C), max (nA)	Gain, min (dB)	Unity Gain (MHz)	Slew Rate (V/μsec)	(±V)	(±mA)	Temp Range[1]	Package	Page
FET	OPA111AM*	0.5	5	±0.002	114	2	2	11	5	Ind	TO-99	1-53
	OPA111BM	0.25	1	±0.001	120	2	2	11	5	Ind	TO-99	1-53
	OPA111SM	0.5	5	±0.002	114	2	2	11	5	MIL	TO-99	1-53
Wideband	OPA156AM	2	5	0.05	94	6	14	10	5	MIL	TO-99	1-81
	OPA356AM	2	5	0.05	94	6	14	10	5	Com	TO-99	1-81
	OPA606LM	0.5	5	±0.01	100	13	35	12	5	Com	TO-99	1-135
Dual FET	OPA2111BM*	0.5	2.8	±0.004	114	2	2	11	5	Ind	TO-99	1-143
Bipolar	OPA27A*	0.025	0.6	±40	120	8	1.9	12	16.6	MIL	TO-99, DIP	1-17
	OPA37A*	0.025	0.6	±40	120	63[2]	11.9	12	16.6	MIL	TO-99, DIP	1-17
	OPA27B	0.060	1.3	±55	120	8	1.9	12	16.6	MIL	TO-99, DIP	1-17
	OPA37B	0.060	1.3	±55	120	63[2]	11.9	12	16.6	MIL	TO-99, DIP	1-17
	OPA27C	0.100	1.8	±80	117	8	1.9	12	16.6	MIL	TO-99, DIP	1-17
	OPA37C	0.100	1.8	±80	117	63[2]	11.9	12	16.6	MIL	TO-99, DIP	1-17
	OPA27E	0.025	0.6	±40	120	8	1.9	12	16.6	Ind	TO-99, DIP	1-17
	OPA37E	0.025	0.6	±40	120	63[2]	11.9	12	16.6	Ind	TO-99, DIP	1-17
	OPA27F	0.060	1.3	±55	120	8	1.9	12	16.6	Ind	TO-99, DIP	1-17
	OPA37F	0.060	1.3	±55	120	63[2]	11.9	12	16.6	Ind	TO-99, DIP	1-17
	OPA27G	0.100	1.8	±80	117	8	1.9	12	16.6	Ind	TO-99, DIP	1-17
	OPA37G	0.100	1.8	±80	117	63[2]	11.9	12	16.6	Ind	TO-99, DIP	1-17
	OPA27GP	0.100	1.8	±80	117	8	1.9	12	16.6	Com	DIP	1-17
	OPA37GP	0.100	1.8	±80	117	63[2]	11.9	12	16.6	Com	DIP	1-17
Low Power	OPA21EZ	0.1	1	25	120	0.3	0.2	13	5	Ind	DIP	1-13
	OPA21GZ	0.5	5	50	114	0.3	0.2	13	5	Ind	DIP	1-13

NOTES: (1) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (2) Gain-bandwidth product for OPA37. A_V = 5 minimum.
*Available in 20-pin ceramic leadless chip carriers.

LOW BIAS CURRENT

Our many years of experience in designing, manufacturing and testing FET amplifiers gives us unique abilities in providing low and ultra low bias current op amps. These amplifiers offer bias currents as low as 75fA (75×10^{-15} amps) and low voltage drift as low as $1\mu V/°C$. With offset voltage laser-trimmed to as low as $250\mu V$, the need for expensive trim pot adjustments is eliminated.

LOW BIAS CURRENT (≤50pA)													
		Offset Voltage, max		Bias Current	Open Loop	Frequency Response		Rated Output, min					
Description	Model[1]	At 25°C, (±mV)	Temp Drift, (±μV/°C)	(25°C), max (pA)	Gain, min (dB)	Unity Gain (MHz)	Slew Rate (V/μsec)	(±V)	(±mA)	Temp Range[2]	Package	Page
Premium Performance	OPA111AM*	0.5	5	±2	114	2	2	11	5	Ind	TO-99	1-53
	OPA111BM	0.25	1	±1	120	2	2	11	5	Ind	TO-99	1-53
	OPA111SM	0.5	5	±2	114	2	2	11	5	MIL	TO-99	1-53
Low Noise	OPA101AM	0.50	10	−15	94	10	6.5	12	12	Ind	TO-99	1-33
	OPA101BM	0.25	5	−10	94	10	6.5	12	12	Ind	TO-99	1-33
	OPA102AM	0.50	10	−15	94	40	14	12	12	Ind	TO-99	1-33
	OPA102BM	0.25	5	−10	94	40	14	12	12	Ind	TO-99	1-33
Ultra-Low Bias Current	OPA128JM*	1	20	±0.300	94	1	3	10	5	Com	TO-99	1-73
	OPA128KM	0.5	10	±0.150	110	1	3	10	5	Com	TO-99	1-73
	OPA128LM	0.5	5	±0.075	110	1	3	10	5	Com	TO-99	1-73
	OPA128SM	0.5	10	±0.150	110	1	3	10	5	MIL	TO-99	1-73
Dual FET	OPA2111AM*	0.75	6	±8	110	2	2	11	5	Ind	TO-99	1-143
	OPA2111BM	0.5	2.8	±4	114	2	2	11	5	Ind	TO-99	1-143
	OPA2111SM	0.75	6	±8	110	2	2	11	5	MIL	TO-99	1-143
	OPA2111KM	**2**	**15**	**±15**	**106**	**2**	**2**	**11**	**5**	**Com**	**TO-99**	**38**
	OPA2111KP	**2**	**15**	**±15**	**106**	**2**	**2**	**11**	**5**	**Com**	**DIP**	**38**
Quad FET	OPA404AG*	1	3[4]	±8	88	6.4	35	11.5	5	Ind	DIP	1-95
	OPA404BG	0.75	3[4]	±4	92	6.4	35	12	5	Ind	DIP	1-95
	OPA404SG	1	3[4]	±8	88	6.4	35	11.5	5	MIL	DIP	1-95
	OPA404KP	**2.5**	**5[4]**	**±12**	**88**	**6.4**	**35**	**11.5**	**5**	**Com**	**DIP**	**1**
Low Cost	OPA121KM*	2	10	±5	110	2	2	11	5	Com	TO-99	1-67
	OPA121KP	3	10	±10	106	2	2	11	5	Com	DIP	1-67
Wideband	**OPA602AM**	**1**	**15**	**10**	**75**	**6.5**	**20**	**10**	**15**	**Ind**	**TO-99**	**23**
	OPA602BM	**0.5**	**5**	**2**	**88**	**6.5**	**24**	**10**	**15**	**Ind**	**TO-99**	**23**
	OPA602CM	**0.25**	**2**	**1**	**92**	**6.5**	**28**	**10**	**15**	**Ind**	**TO-99**	**23**
	OPA602SM	**0.5**	**5**	**2**	**88**	**6.5**	**24**	**10**	**15**	**MIL**	**TO-99**	**23**
	OPA606KM	1.5	5[4]	±15	95	12.5	33	11	5	Com	TO-99	1-135
	OPA606LM	0.5	5	±10	100	13	35	12	5	Com	TO-99	1-135
	OPA606SM	1.5	5[4]	±15	95	12.5	33	11	5	MIL	TO-99	1-135
	OPA606KP	3	10[4]	±25	90	12	30	11	5	Com	DIP	1-135
Low Cost, Ultra-Low Bias Current	AD515JH	3	50	0.300	86	0.35	1	10	5	Com	TO-99	1-153
	AD515KH	1	15	0.150	92	0.35	1	10	5	Com	TO-99	1-153
	AD515LH	1	25	0.075	88	0.35	1	10	5	Com	TO-99	1-153

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) Typical.

LOW NOISE

Now both FET and bipolar input op amps are offered with guaranteed low noise specifications. Until now the designer had to rely on "typical" specs for his demanding low noise designs. These fully characterized parts allow a truly complete error budget calculation.

LOW NOISE (Guaranteed e_n)													
		Noise Voltage at 10kHz, max	Bias Current (25°C), max	Offset Voltage, max		Open Loop Gain, min	Frequency Response		Rated Output, min		Temp Range		
Description	Model	(nV/√Hz)	(pA)	At 25°C (±mV)	Temp Drift (±μV/°C)	(dB)	Gain Bandwidth (MHz)	Slew Rate, min (V/μsec)	(±V)	(±mA)	[1]	Package	Page
Bipolar	OPA27A*	3.8	±40nA	0.025	0.6	120	8	1.7	12	16.6	MIL	TO-99, DIP	1-17
	OPA37A*	3.8	±40nA	0.025	0.6	120	63	11	12	16.6	MIL	TO-99, DIP	1-17
	OPA27B	3.8	±55nA	0.060	1.3	120	8	1.7	12	16.6	MIL	TO-99, DIP	1-17
	OPA37B	3.8	±55nA	0.060	1.3	120	63	11	12	16.6	MIL	TO-99, DIP	1-17
	OPA27C	4.5	±80nA	0.100	1.8	117	8	1.7	12	16.6	MIL	TO-99, DIP	1-17
	OPA37C	4.5	±80nA	0.100	1.8	117	63	11	12	16.6	MIL	TO-99, DIP	1-17
	OPA27E	3.8	±40nA	0.025	0.6	120	8	11	12	16.6	Ind	TO-99, DIP	1-17
	OPA37E	3.8	±40nA	0.025	0.6	120	63	11	12	16.6	Ind	TO-99, DIP	1-17
	OPA27F	3.8	±55nA	0.060	1.3	120	8	1.7	12	16.6	Ind	TO-99, DIP	1-17
	OPA37F	3.8	±55nA	0.060	1.3	120	63	11	12	16.6	Ind	TO-99, DIP	1-17

*Available in 20-pin ceramic leadless chip carriers.

This table continued on next page.

Models in **boldface type** are found in this supplement; others are in the Burr-Brown *Integrated Circuits Data Book.*

LOW NOISE (Guaranteed e_n) (CONT)														
		Noise Voltage at 10kHz, max	Bias Current (25°C), max	Offset Voltage, max		Open Loop Gain, min	Frequency Response		Rated Output, min		Temp Range [1]			
Description	Model	(nV/√Hz)	(pA)	At 25°C (±mV)	Temp Drift (±μV/°C)	(dB)	Gain Bandwidth (MHz)	Slew Rate, min (V/μsec)	(±V)	(±mA)		Package	Page
Bipolar	OPA27G	4.5	±80nA	0.100	1.8	117	8	1.7	12	16.6	Ind	TO-99, DIP	1-17
	OPA37G	4.5	±80nA	0.100	1.8	117	63	11	12	16.6	Ind	TO-99, DIP	1-17
Wide Bandwidth	OPA101AM	8	−15	0.5	10	94	20	5	12	12	Ind	TO-99	1-33
	OPA101BM	8	−10	0.25	5	94	20	5	12	12	Ind	TO-99	1-33
	OPA102AM	8	−15	0.5	10	94	40	10	12	12	Ind	TO-99	1-33
	OPA102BM	8	−10	0.25	5	94	40	10	12	12	Ind	TO-99	1-33
FET	OPA111AM*	8	±2	0.5	5	114	2	1	11	5	Ind	TO-99	1-53
	OPA111BM	8	±1	0.25	1	120	2	1	11	5	Ind	TO-99	1-53
	OPA111SM	8	±2	0.5	5	114	2	1	11	5	MIL	TO-99	1-53
	OPA606LM	13	±10	0.5	5	100	13	25	12	5	Com	TO-99	1-135
Low Cost	OPA27GP	4.5	±80nA	0.100	1.8	117	8	1.9[2]	10	16.6	Com	DIP	1-17
	OPA37GP	4.5	±80nA	0.100	1.8	117	63	11.9[2]	10	16.6	Com	DIP	1-17
Dual FET	OPA2111AM*	8	±8	0.75	6	110	2	1	11	5	Ind	TO-99	1-143
	OPA2111BM	8	±4	0.5	2.8	114	2	1	11	5	Ind	TO-99	1-143
	OPA2111SM	8	±4	0.75	6	110	2	1	11	5	MIL	TO-99	1-143
	OPA2111KM	**6[2]**	**±15**	**2**	**15**	**106**	**2**	**1**	**11**	**5**	**Com**	**TO-99**	**38**
	OPA2111KP	**6[2]**	**±15**	**2**	**15**	**106**	**2**	**1**	**11**	**5**	**Com**	**DIP**	**38**

NOTES: (1) Ind = −25°C to +85°C, MIL = −55°C to +125°C, Com = 0°C to +70°C. (2) Typical.

UNITY-GAIN BUFFER (Power Booster)

These versatile amplifiers: boost the output current capability of another amplifier; buffer an impedance that might load a critical circuit; may be used inside the feedback loop of another op amp to form a current-boosted, composite amplifier. Currents as high as ±100mA are available with speeds of 2000V/μsec.

UNITY-GAIN BUFFER											
		Rated Output, min		Frequency Response			Gain	Input Impedance	Temp		
Description	Model	(±V)	(±mA)	−3dB (MHz)	Full Power BW (MHz)	Slew Rate (V/μsec)	(V/V)	(Ω)	Range[1]	Package	Page
High Performance	3553AM	10	200	300	32	2000	≈1	10^{11}	Ind	TO-3	1-184
Low Cost	**OPA633AH**	**10**	**80**	**275**	**65**	**1000**	**≈1**	**10^6**	**Ind**	**TO-8**	**29**
	OPA633SH	**10**	**80**	**275**	**65**	**1000**	**≈1**	**10^6**	**MIL**	**TO-8**	**29**
	OPA633KP	**10**	**80**	**275**	**65**	**1000**	**≈1**	**10^6**	**Com**	**DIP**	**29**

NOTES: (1) Ind = −25°C to +85°C, MIL = −55°C to +125°C, Com = 0°C to +70°C.

WIDE BANDWIDTH

Design expertise in wideband circuits combines with our fully developed technology to create cost effective wideband op amps. Burr-Brown high speed amplifiers also offer outstanding DC performance specifications.

WIDE BANDWIDTH (≥5MHz)													
		Frequency Response				Rated Output, min		Offset Voltage, max		Open Loop			
Description	Model[1]	Gain Bandwidth (MHz)	Slew Rate, min (V/μsec)	t_S ±0.1% (nsec)	Compensation	(±V)	(±mA)	At 25°C (±mV)	Temp Drift (±μV/°C)	Gain, min (dB)	Temp Range [2]	Package	Page
FET	3554AM, (Q)	1700, A = 1000	1000	120	ext.	10	100	2	50	100	Ind	TO-3	1-188
	3554BM, (Q)	1700, A = 1000	1000	120	ext.	10	100	1	15	100	Ind	TO-3	1-188
	3554SM, (Q)	1700, A = 1000	1000	120	ext.	10	100	1	25	100	MIL	TO-3	1-188
	3551J	50, A = 10	250	400	ext.	10	10	1	50[3]	88	Com	TO-99	1-180
	3551S, (Q)	50, A = 10	250	400	ext.	10	10	1	50[3]	88	MIL	TO-99	1-180
	3550J	10, A = 10	65	400	int.	10	10	1	50[3]	88	Com	TO-99	1-176
	3550K	20, A = 1	100	400	int.	10	10	1	50[3]	88	Com	TO-99	1-176
	3550S, (Q)	10, A = 1	65	400	int.	10	10	1	50[3]	88	MIL	TO-99	1-176
Bipolar	3508J	100, A = 100	0	—	ext.	10	10	5	30[3]	98	Com	TO-99	1-163
	3507J, (Q)	20, A = 10	80	200	ext.	10	10	10	30[3]	83	Com	TO-99	1-161

*Available in 20-pin ceramic leadless chip carriers.

This table continued on next page.

Models in **boldface type** are found in this supplement; others are in the Burr-Brown *Integrated Circuits Data Book*.

WIDE BANDWIDTH (≥5MHz) (CONT)														
		Frequency Response				Rated Output, min		Offset Voltage, max		Open Loop				
Description	Model[1]	Gain Bandwidth (MHz)	Slew Rate, min (V/μsec)	t_s ±0.1% (nsec)	Compensation	(±V)	(±mA)	At 25°C (±mV)	Temp Drift (±μV/°C)	Gain, min (dB)	Temp Range [2]	Package	Page
FET	OPA156AM	6, A = 1	10	1.5μsec	int.	10	5	2	5	94	MIL	TO-99	1-81
	OPA356AM	6, A = 1	10	1.5μsec	int.	10	5	2	5	94	Com	TO-99	1-81
Advance Information	**OPA602AM**	**6.5**	**20**	**600**	**Int.**	**10**	**15**	**1**	**15**	**75**	**Ind.**	**TO-99**	**23**
	OPA602BM	**6.5**	**24**	**600**	**Int.**	**10**	**15**	**0.5**	**5**	**88**	**Ind.**	**TO-99**	**23**
	OPA602CM	**6.5**	**28**	**600**	**Int.**	**10**	**15**	**0.25**	**2**	**92**	**Ind.**	**TO-99**	**23**
	OPA602SM	**6.5**	**24**	**600**	**Int.**	**10**	**15**	**0.5**	**5**	**88**	**MIL**	**TO-99**	**23**
	OPA605H	200, A=1000	300[3]	300	ext.	10	30	1	25	96[3]	Com	DIP	1-129
	OPA605A	200, A=1000	300[3]	300	ext.	10	30	1	25	96[3]	Ind	DIP	1-129
	OPA605K	200, A=1000	300[3]	300	ext.	10	30	0.5	5	96[3]	Com	DIP	1-129
	OPA605C	200, A=1000	300[3]	300	ext.	10	30	0.5	5	96[3]	Ind	DIP	1-129
	OPA606KM	12.5	22	1μsec	int.	11	5	1.5	5[3]	95	Com	TO-99	1-135
	OPA606LM	13	25	1μsec	int.	12	5	0.5	5	100	Com	TO-99	1-135
	OPA606SM	12.5	22	1μsec	int.	11	5	1.5	5[3]	95	MIL	TO-99	1-135
	OPA606KP	12	20	1μsec	int.	11	5	3	10[3]	90	Com	TO-99	1-135
Quad FET	OPA404AG	6.4	24	600	int.	11.5	5	1	3[3]	88	Ind	DIP	1-95
	OPA404BG	6.4	28	600	int.	11.5	5	0.75	3[3]	92	Ind	DIP	1-95
	OPA404SG	6.4	24	600	int.	11.5	5	1	3[3]	88	MIL	DIP	1-95
	OPA404KP	**6.4**	**24**	**600**	**Int.**	**11.5**	**5**	**2.5**	**5[3]**	**88**	**Com**	**DIP**	**1**
Low Noise Bipolar	OPA27A*	8, A = 1	1.7	—	int.[4]	12	16.6	0.025	0.6	120	MIL	TO-99, DIP	1-17
	OPA37A*	63, A = 5	11	—	int.[4]	12	16.6	0.025	0.6	120	MIL	TO-99, DIP	1-17
	OPA27B	8, A = 1	1.7	—	int.[4]	12	16.6	0.060	1.3	120	MIL	TO-99, DIP	1-17
	OPA37B	63, A = 5	11	—	int.[4]	12	16.6	0.060	1.3	120	MIL	TO-99, DIP	1-17
	OPA27C	8, A = 1	1.7	—	int.[4]	12	16.6	0.100	1.8	117	MIL	TO-99, DIP	1-17
	OPA37C	63, A = 5	11	—	int.[4]	12	16.6	0.100	1.8	117	MIL	TO-99, DIP	1-17
	OPA27E	8, A = 1	1.7	—	int.[4]	12	16.6	0.025	0.6	120	Ind	TO-99, DIP	1-17
	OPA37E	63, A = 5	11	—	int.[4]	12	16.6	0.025	0.6	120	Ind	TO-99, DIP	1-17
	OPA27F	8, A = 1	1.7	—	int.[4]	12	16.6	0.060	1.3	120	Ind	TO-99, DIP	1-17
	OPA37F	63, A = 5	11	—	int.[4]	12	16.6	0.060	1.3	120	Ind	TO-99, DIP	1-17
	OPA27G	8, A = 1	1.7	—	int.[4]	12	16.6	0.100	1.8	117	Ind	TO-99, DIP	1-17
	OPA37G	63, A = 5	11	—	int.[4]	12	16.6	0.100	1.8	117	Ind	TO-99, DIP	1-17
Low Noise FET	OPA101AM	20, A=100	5	2.5μsec	int.	12	12	0.5	10	94	Ind	TO-99	1-33
	OPA101BM	20, A=100	5	2.5μsec	int.	12	12	0.25	5	94	Ind	TO-99	1-33
	OPA102AM	40, A=100	10	1.5μsec	int.	12	12	0.5	10	94	Ind	TO-99	1-33
	OPA102BM	40, A=100	10	1.5μsec	int.	12	12	0.25	5	94	Ind	TO-99	1-33
Fast Settling	OPA600UM	6000, A=1000	500	80	ext.	9	180	5	100	86	MIL	DIP	12-94
	OPA600VM	6000, A=1000	500	80	ext.	9	180	4	20	86	MIL	DIP	12-94
	OPA600BM	5000, A = 1000	500	80	ext.	9	180	±5	±80	86	Ind	DIP	1-121
	OPA600CM	5000, A = 1000	500	80	ext.	9	180	±4	±40	86	Ind	DIP	1-121
	OPA600SM	5000, A = 1000	500	80	ext.	9	180	±5	±100	86	MIL	DIP	1-121
	OPA600TM	5000, A = 1000	500	80	ext.	9	180	±4	±80	86	MIL	DIP	1-121
Unity-Gain Buffer	3553AM, (Q)	32	2000	—	—	10	200	50	300[3]	NA	Ind	TO-3	1-184
Low Cost	OPA27GP	8, A = 1	1.9[3]	—	int.	12	16.6	0.100	1.8	117	Com	DIP	1-17
	OPA37GP	63, A = 5	11.9[3]	—	int.[4]	12	16.6	0.100	1.8	117	Com	DIP	1-17
Wide Temp Range	OPA27HT	6, A = 1	1.9	—	int.	12	16.6[3]	0.050	0.25[3]	120	−55°C to +200°C	TO-99	1-29
	OPA37HT	36, A = 5	11.9	—	int.[4]	12	16.6[3]	0.050	0.25[3]	120		TO-99	1-29
	OPA11HT	12, A=1	4	1.5μsec	ext.	10	15	5[3]	5	98	−55°C to +200°C	TO-99	1-9

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) Typical. (4) G = 5 min for OPA37.

*Available in 20-pin ceramic leadless chip carriers.

Models in **boldface type** are found in this supplement; others are in the Burr-Brown *Integrated Circuits Data Book.*

HIGH VOLTAGE—HIGH CURRENT												
		Rated Output, min		Offset Voltage, max		Bias Current	Frequency Response		Open Loop	Temp		
Description	Model[1]	(±V)	(±mA)	At 25°C, (±mV)	Temp Drift, (±μV/°C)	(25°C), max (pA)	Unity Gain (MHz)	Slew Rate (V/μsec)	Gain (dB)	Range [2]	Package	Page
High Power	OPA501AM	20	10A	10	65	40nA	1	1.35	94	Ind	TO-3	1-103
	OPA501BM	26	10A	5	40	20nA	1	1.35	98	Ind	TO-3	1-103
	OPA501RM	20	10A	10	65	40nA	1	1.35	94	MIL	TO-3	1-103
	OPA501SM	26	10A	5	40	20nA	1	1.35	98	MIL	TO-3	1-103
	OPA511AM	22	5A	10	65	40	1	1	91	Ind	TO-3	1-111
	OPA512BM	35	10A	6	65	30	4	2.5	110	Ind	TO-3	1-116
	OPA512SM	35	15A	3	40	20	4	2.5	110	MIL	TO-3	1-116
	OPA541AM	**30**	**5A**	**10**	**40**	**50**	**1.6**	**8**	**90**	**Ind.**	**TO-3**	**9**
	OPA541BM	**35**	**5A**	**1**	**30**	**50**	**1.6**	**8**	**90**	**Ind.**	**TO-3**	**9**
	OPA541SM	**35**	**5A**	**1**	**30**	**50**	**1.6**	**8**	**90**	**MIL**	**TO-3**	**9**
	3573AM	20	2A[5]	10	65	40nA	1	2.6	94	Ind	TO-3	1-202
	3572AM	30	2A[5]	2	40	−100	0.5	3	94	Ind	TO-3	1-196
	3571AM, (Q)	30	1A[4]	2	40	−100	0.5	3	94	Ind	TO-3	1-196
Wideband	3554AM, (Q)	10	100	2	50	−50	1700[3]	1200	100	Ind	TO-3	1-188
	3554BM, (Q)	10	100	1	15	−50	1700[3]	1200	100	Ind	TO-3	1-188
	3554SM, (Q)	10	100	1	25	−50	1700[3]	1200	100	MIL	TO-3	1-188
High Voltage	3584JM, (Q)	145	15	3	25	−20	20[3]	150	126	Com	TO-3	1-214
	3583AM	140	75	3	25	−20	5	30	118	Ind	TO-3	1-210
	3583JM	140	75	3	25	−20	5	30	118	Com	TO-3	1-210
	3582J	145	15	3	25	−20	5	20	118	Com	TO-3	1-206
	3581J	70	30	3	25	−20	5	20	112	Com	TO-3	1-206
	3580J	30	60	10	30	−50	5	15	106	Com	TO-3	1-206
Advance Information	**OPA445BM**	**35**	**15**	**3**	**10**	**50**	**2**	**10**	**100**	**Ind**	**TO-99**	**5**
	OPA445SM	**35**	**15**	**1**	**10**	**50**	**2**	**10**	**100**	**MIL**	**TO-99**	**5**
Booster	3553AM, (Q)	10	200	50	300[6]	−200	300	2000	NA	Ind	TO-3	1-184
	OPA633AH	**10**	**80**	**15**	**33**[6]	**35μA**	**275**[6]	**1000**	**NA**	**Ind**	**TO-8**	**29**
	OPA633SH	**10**	**80**	**15**	**33**[6]	**35μA**	**275**[6]	**1000**	**NA**	**MIL**	**TO-8**	**29**
	OPA633KP	**10**	**80**	**15**	**33**[6]	**35μA**	**275**[6]	**1000**	**NA**	**Com**	**DIP**	**29**

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) Gain-bandwidth product. (4) 2A peak. (5) 5A peak. (6) Typical.

INSTRUMENTATION AMPLIFIERS AND PROGRAMMABLE GAIN AMPLIFIERS

INSTRUMENTATION AMPLIFIERS											
						Input Parameters					
Description	Model	Gain Range	Gain Accuracy, G = 100, 25°C, max (%)	Gain Drift, G = 100 (ppm/°C)	Non-Linearity, G = 100, max (%)	CMR, DC to 60Hz, G = 10, 1kΩ Unbal., min (dB)	Offset Voltage vs Temp, max (μV/°C)	Dynamic Response, G = 100, ±3dB BW (kHz)	Temp Range [1]	Package	Page
Very-High Accuracy	INA104HP	1-1000[2]	0.15	22	±0.007	96	±(2 ± 20/G)	25	Com	DIP	2-26
	INA104JP	1-1000[2]	0.15	22	±0.003	96	±(0.25 ± 10/G)	25	Com	DIP	2-26
	INA104KP	1-1000[2]	0.15	22	±0.003	96	±(0.75 ± 10/G)	25	Com	DIP	2-26
	INA104AM	1-1000[2]	0.15	22[3]	±0.007	96	±(2 ± 20/G)	25	Ind	DIP	2-26
	INA104BM	1-1000[2]	0.15	22[3]	±0.003	96	±(0.75 ± 10/G)	25	Ind	DIP	2-26
	INA104CM	1-1000[2]	0.15	22[3]	±0.003	96	±(0.25 ± 10/G)	25	Ind	DIP	2-26
	INA104SM	1-1000[2]	0.15	22[3]	±0.003	96	±(0.75 ± 10/G)	25	MIL	DIP	2-26
	INA101AM*	1-1000[2]	0.03	22[4]	±0.007	96	±(2 + 20/G)	25	Ind	TO-100	2-7
	INA101CM	1-1000[2]	0.03	22[4]	±0.004	96	±(0.25 + 10/G)	25	Ind	TO-100	2-7
	INA101SM	1-1000[2]	0.03	22[4]	±0.004	96	±(0.25 + 10/G)	25	MIL	TO-100	2-7
	INA101AG	1-1000[2]	0.03	22[3]	±0.007	96	±(2 + 20/G)	25	Ind	DIP	2-7
	INA101CG	1-1000[2]	0.03	22[3]	±0.003	96	±(0.25 + 10/G)	25	Ind	DIP	2-7
	INA101SG	1-1000[2]	0.03	22[3]	±0.003	96	±(0.25 + 10/G)	25	MIL	DIP	2-7
	INA101HP	1-1000[2]	0.3	22[3]	±0.007	90	±(2 + 20/G) typ	25	Com	DIP	2-7
	INA101KU	**1-1000**[2]	**0.3**	**22**[3]	**±0.007**	**90**	**±(2 + 20/G) typ**	**25**	**Com**	**SOIC**	**xxiii**
Low Quiescent Power	INA102AG*	1, 10, 100, 1000	0.25	20	±0.05	80	±(5 + 10/G)	3	Ind	DIP	2-18
	INA102CG		0.15	15	±0.02	90	±(2 + 5/G)	3	Ind	DIP	2-18

*Available in 20-pin ceramic leadless chip carriers.

This table continued on next page.

Models in **boldface type** are found in this supplement; others are in the Burr-Brown *Integrated Circuits Data Book.*

INSTRUMENTATION AMPLIFIERS (CONT)											
						Input Parameters					
Description	Model	Gain Range	Gain Accuracy, G = 100, 25°C, max (%)	Gain Drift, G = 100 (ppm/°C)	Non-Linearity, G = 100, max (%)	CMR, DC to 60Hz, G = 10, 1kΩ Unbal., min (dB)	Offset Voltage vs Temp, max (μV/°C)	Dynamic Response, G = 100, ±3dB BW (kHz)	Temp Range [1]	Package	Page
Fast Settling FET Input	INA110AG*	1, 10, 100,	0.2	40	±0.02	87	±(5 + 100/G)	470	Ind	DIP	2-46
	INA110BG	200, 500	0.1	20	±0.01	96	±(2 + 50/G)	470	Ind	DIP	2-46
	INA110SG	**1, 10, 100**	**0.1**	**20**	**0.01**	**96**	**±(2 + 50/G)**	**470**	**MIL**	**DIP**	**53**
	INA110KP	**200,**	**0.2**	**6 typ**	**0.02**	**87**	**±(2 + 20/G) typ**	**470**	**Com**	**DIP**	**53**
	INA110KU	**500**	**0.2**	**6 typ**	**0.02**	**87**	**±(2 + 20/G) typ**	**470**	**Com**	**SOIC**	**53**
Buffer, Unity-Gain Differential	3627AM	1V/V, fixed	0.01	5	±0.001[3]	90	30	800[3]	Ind	TO-99	2-122
	3627BM	1V/V, fixed	0.01	5	±0.001[3]	100	20	800[3]	Ind	TO-99	2-122
	INA105AM*	1V/V, fixed	0.01	5	±0.001[3]	80[6]	20	1000[3]	Ind	TO-99	2-36
	INA105BM	1V/V, fixed	0.01	5	±0.001[3]	86[6]	10	1000[3]	Ind	TO-99	2-36
	INA105KP	1V/V, fixed	0.025	5	±0.001[3]	72[6]	5 typ	1000[3]	Com	DIP	2-36
	INA105KU	**1V/V, fixed**	**0.025**	**5**	**±0.001[3]**	**72[6]**	**5**	**1000[3]**	**Com**	**SOIC**	**xxiii**
Gain of 10 Differential	**INA106AM**	**10V/V fixed**	**0.01**	**10**	**0.001**	**94[6]**	**5**	**500[5]**	**Ind**	**DIP**	**45**
	INA106BM	**10V/V fixed**	**0.01**	**10**	**0.001**	**100[6]**	**2**	**500[5]**	**Ind**	**DIP**	**45**
	INA106KP	**10V/V fixed**	**0.025**	**4 typ**	**0.001**	**86[6]**	**0.2 typ**	**500[5]**	**Com**	**DIP**	**45**
High Common Mode Voltage Differential (200VDC CMV)	**INA117AG**	**1V/V fixed**	**0.05[3]**	**10[3]**	**0.001[3]**	**74[3,6]**	**40**	**200[3]**	**Ind**	**TO-99**	**57**
	INA117BG	**1V/V fixed**	**0.02[3]**	**10[3]**	**0.001[3]**	**86[3,6]**	**20**	**200[3]**	**Ind**	**TO-99**	**57**
	INA117P	**1V/V fixed**	**0.05[3]**	**10[3]**	**0.001[3]**	**74[3,6]**	**40**	**200[3]**	**Com**	**DIP**	**57**
PROGRAMMABLE GAIN AMPLIFIERS											
Noninverting Multiplexed Input	PGA100AG	Gain set	0.05	10	±0.01	NA	6 typ	5MHz	Ind	DIP	2-58
	PGA100BG	with 4-bit word 1, 2, 4, 8 . . . 128	0.02	10	±0.005	NA	6 typ	5MHz	Ind	DIP	2-58
	PGA102AG	Gain set	0.02	20	0.01	—	3, G = 100	250	Ind	DIP	2-66
	PGA102BG	with 2-bit	0.01	20	0.01	—	3, G = 100	250	Ind	DIP	2-66
	PGA102SG	word 1, 10	0.01	20	0.01	—	3, G = 100	250	Ind	DIP	2-66
	PGA102KP	100	0.02	50	0.01	—	3, G = 100	250	Com	DIP	2-66
Instrumentation Amplifier Input	PGA200AG	Gain set	0.05	20	±0.007	96	2, G = 100	30	Ind	DIP	2-76
	PGA200BG	with 2-bit word 1, 10, 100, 1000	0.02	10	±0.003	96	0.4, G = 100	30	Ind	DIP	2-76
Differential Input	3606AG	Gain set	0.05	10	0.004	90, G = 1	±(3 + 50/G)	40	Ind	DIP	2-114
	3606AM	with 3-bit	0.05	10	0.004	90, G = 1	±(3 + 50/G)	40	Ind	DIP	2-114
	3606BG	word 1, 2, 4	0.02	10	0.004	90, G = 1	±(1 + 20/G)	40	Ind	DIP	2-114
	3606BM	8 . . . 1024	0.02	10	0.004	90, G = 1	±(1 + 20/G)	40	Ind	DIP	2-114

NOTES: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (2) Set with external resistor. (3) Unity-gain. (4) With zero TC external resistor. (5) Gain = 10. (6) No source imbalance.

PRECISION TRANSMITTERS													
		Span			Input Parameters			Output Parameters					
Description	Model	Un-trimmed Error, max (%)	Non-Linearity, max (%)	Temp Drift[1] (ppm/°C)	Offset Voltage, max (μV)	Offset Voltage vs Temp, max (μV/°C)	CMR, DC, min (dB)	Current Range (mA)	Offset Current Error, max (μA)	FS Output Current Error, max (μA)	Temp Range [2]	Package	Page
Two-Wire	XTR100AM	−3	0.01	±100	±50	±1	90	4-20	±4	±20	Ind	DIP	2-82
	XTR100AP	−3	0.01	±100	±50	±1	90	4-20	±4	±20	Ind	DIP	2-82
	XTR100BM	−3	0.01	±100	±25	±0.5	90	4-20	±4	±20	Ind	DIP	2-82
	XTR100BP	−3	0.01	±100	±25	±0.5	90	4-20	±4	±20	Ind	DIP	2-82
	XTR101AG*	−5	0.01	±100	±60	±1.5	90	4-20	±10	±40	Ind	DIP	2-94
	XTR101BG	−5	0.01	±100	±30	±0.75	90	4-20	±6	±30	Ind	DIP	2-94
	XTR101AP	**−5**	**0.01**	**±100**	**±100**	**±1.5**	**90**	**4-20**	**±19**	**±60**	**Ind[3]**	**DIP**	**65**
	XTR101AU	**−5**	**0.01**	**±100**	**±100**	**±1.5**	**90**	**4-20**	**±19**	**±60**	**Ind[3]**	**SOIC**	**xxiii**
Three-Wire and Current Source	XTR110AG*	0.6	0.025	50	—	—	—	4-20,	±64	±96	Ind	DIP	2-104
	XTR110BG	0.2	0.005	30	—	—	—	0-20,	±16	±32	Ind	DIP	2-104
	XTR110KP	0.6	0.025	50	—	—	—	5-25	±64	±96	Com	DIP	2-104
	XTR110KU	**0.6**	**0.025**	**50**	—	—	—	[4]	**±64**	**±96**	**Com**	**SOIC**	**xxiii**

NOTES: (1) With zero TC span resistor. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) −40°C to +85°C. (4) Many more ranges with appropriate circuit.

*Available in 20-pin ceramic leadless chip carriers.

Models in **boldface type** are found in this supplement; others are in the Burr-Brown *Integrated Circuits Data Book.*

ISOLATION PRODUCTS

TRANSFORMER COUPLED AMPLIFIERS																	
		Isolation Voltage (V)		Isolation Mode Rejection, typ.		Leakage Current at Test Voltage	Isolation Impedance		Gain Nonlinearity		Voltage Drift,	Bias Current,	±3dB Freq.	External Isolation Power	Temp. Range		
Description	Model	Continuous, peak	Pulse/ Test, peak	DC (dB)	60Hz (dB)	(μA)	(Ω)	(pF)	max (%)	typ. (%)	(±μV/°C) max	max	(kHz)	Required	[1]	Package	Page
Low Drift[2]	3450	±500	±2000	160	120	1	10^{12}	16	±0.005	±0.0015	100	50nA	1.5	No	Com	Module	3-19
Low Bias FET	3451	±500	±2000	160	120	1	10^{12}	16	±0.025	±0.005	100	25pA	2.5	No	Com	Module	3-19
	3452	±2000	±5000	160	120	1	10^{12}	16	±0.025	±0.005	100	10pA	2.5	No[4]	Com	Module	3-19
	3455	[3]	[3]	160	120	[3]	10^{12}	16	±0.025	±0.005	100	20pA	2.5	No[4]	Com	Module	3-19
Highest Isolation Voltage	3656AG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	25 + (500/G_1)	100nA	30	No	Ind	DIP	3-29
	3656BG	±3500	±8000	160	125	0.5	10^{12}	6	±0.05	±0.03	5 + (1000/G_1)	100nA	30	No	Ind	DIP	3-29
	3656HG	±3500	±8000	160	125	0.5	10^{12}	6	±0.15	±0.03	200 + (1000/G_1)	100nA	30	No	Com	DIP	3-29
	3656JG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	50 + (750/G_1)	100nA	30	No	Com	DIP	3-29
	3656KG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	10 + (350/G_1)	100nA	30	No	Com	DIP	3-29
OPTICALLY COUPLED AMPLIFIERS																	
Balanced Current Input	3650HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	25	10nA	15	Yes[6]	Ind	DIP	3-21
	3650JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.03	10	10nA	15	Yes[6]	Ind	DIP	3-21
	3650KG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.05	±0.02	5	10nA	15	Yes[6]	Ind	DIP	3-21
	3650MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100	10nA	15	Yes[6]	Ind	DIP	3-21
Balanced FET Input	3652HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	50	50nA	15	Yes	Ind	DIP	3-21
	3652JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.05	25	50nA	15	Yes	Ind	DIP	3-21
	3652MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100	50nA	15	Yes	Ind	DIP	3-21
Low Drift Wide Bandwidth	ISO100AP	750	2500	146[6]	108[6]	0.3	10^{12}	2.5	0.4	0.1	$10^{(6)}$	10nA	60	Yes	Ind	DIP	3-6
	ISO100BP	750	2500	146[6]	108[6]	0.3	10^{12}	2.5	0.1	0.01	$4^{(6)}$	10nA	60	Yes	Ind	DIP	3-6
	ISO100CP	750	2500	146[6]	108[6]	0.3	10^{12}	2.5	0.07	0.02	$4^{(6)}$	10nA	60	Yes	Ind	DIP	3-6
CAPACITOR COUPLED, HERMETICALLY SEALED AMPLIFIERS																	
1500VAC Isolation	**ISO102**	**±2121**	**±4000**	**160**	**120**	**1.0**	10^{14}	**6**	**0.075**	**0.04**	**±500**	**100μA**	**70**	**Yes**	**Ind**	**DIP**	**68**
	ISO102B	**±2121**	**±4000**	**160**	**120**	**1.0**	10^{14}	**6**	**0.025**	**0.02**	**±250**	**100μA**	**70**	**Yes**	**Ind**	**DIP**	**68**
3500VAC Isolation	**ISO106**	**±4950**	**±8000**	**160**	**130**	**1.0**	10^{14}	**6**	**0.075**	**0.04**	**±500**	**100μA**	**70**	**Yes**	**Ind**	**DIP**	**68**
	ISO106B	**±4950**	**±8000**	**160**	**130**	**1.0**	10^{14}	**6**	**0.025**	**0.02**	**±250**	**100μA**	**70**	**Yes**	**Ind**	**DIP**	**68**

NOTES: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C. (2) Bipolar. (3) Isolation voltage tested at 2500V, rms, 60Hz; leakage current tested for 2μA max at 240V, rms, 60Hz. (4) ±15V at ±15mA isolated power available to power external circuitry. (5) At 240V/60Hz. (6) R_{IN} = 10k, Gain = 100.

ISOLATION POWER SUPPLIES[1]													
		Isolation Voltage (V)		Input Voltage (VDC)		Leakage Current, 240VAC, 60Hz	Isolation Impedance		Rated Current, Balanced Loads On All	Max Current,[1] Balanced Loads On All	Sensitivity To To Input Voltage	Temp Range		
Description	Model	Continuous Peak	Pulse/ Test Peak	Min	Max	(μA)	(Ω)	(pF)	Outputs (mA)	Outputs (mA)	Change (V/V)	[2]	Package	Page
Single ±15V Output	700	1500	4200	10	18	1	10^{10}	5	±3-30	±60	1.08	Ind	Module	14-35
	700U	2000	5000	10	18	1	10^{10}	3	±3-30	±60	1.08	Ind	Module	14-35
	725	**2121**	**4000**	**7**	**18**	**1.2**	10^{12}	**9**	**±15**	**±40**	**1.15**	**Ind**	**DIP**	**82**
	726	**4950**	**8000**	**7**	**18**	**1.2**	10^{12}	**9**	**±15**	**±40**	**1.15**	**Ind**	**DIP**	**82**
Dual ±15V Output	722	4950	8000	5	16	1	10^{10}	6	±3-40	±50	1.13	Ind	Module	14-41
Quad ±15V Output	710	1000	3100	10	18	1	10^{10}	8	±9.5	±60	1.08	Ind	Module	14-37
Quad ±8V Output	724	1000	3000	5	16	1	10^{10}	6	±3-16	±60	0.63	Ind	Module	14-45

NOTE: (1) See complete data sheet for full specifications, especially regarding output current capabilities. (2) Ind = −25°C to +85°C.

Models in **boldface type** are found in this supplement; others are in the Burr-Brown *Integrated Circuits Data Book.*

ANALOG CIRCUIT FUNCTIONS

MULTIPLIERS/DIVIDERS

You can select accuracy from 0.25% to 2% max from this complete line of integrated circuit multipliers. Most provide full four-quadrant multiplication. All are laser-trimmed for accuracy—no trim pots are needed to meet specified performance. These compact models bring the cost of high performance down to acceptable levels.

MULTIPLIERS/DIVIDERS									
Model	Transfer Function	Error at +25°C, max (%)	Temperature Coefficient (%/°C)	Feed-through (mV)	Offset Voltage (mV)	1% Band-width (kHz)	Temp Range (1)	Package	Page
MPY100A*	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$	±2	0.017	100	50	70	Ind	TO-100	4-23
MPY100B	‡	±1	0.008	30	10	70	Ind	TO-100	4-23
MPY100C	‡	±0.5	0.008	30	7	70	Ind	TO-100	4-23
MPY100S	‡	±0.5	0.025	30	7	70	MIL	TO-100	4-23
MPY534JH*	‡	±1.0	0.022	0.3%	5	3MHz	Com	TO-100	4-31
MPY534JD	‡	±1.0	0.022	0.3%	5	3MHz	Com	DIP	4-31
MPY534KH	‡	±0.5	0.015	0.15	2	3MHz	Com	TO-100	4-31
MPY534KD	‡	±0.5	0.015	0.15%	2	3MHz	Com	DIP	4-31
MPY534LH	‡	±0.25	0.008	0.05%	2	3MHz	Com	TO-100	4-31
MPY534LD	‡	±0.25	0.008	0.05%	2	3MHz	Com	DIP	4-31
MPY534SH	‡	±1.0	0.02	0.3%	5	3MHz	MIL	TO-100	4-31
MPY534SD	‡	±1.0	0.02	0.3%	5	3MHz	MIL	DIP	4-31
MPY534TH	‡	±0.5	0.01	0.15%	2	3MHz	MIL	TO-100	4-31
MPY534TD	‡	±0.5	0.01	0.15%	2	3MHz	MIL	DIP	4-31
MPY634AM*	‡	±1.0	0.022	0.3%	5	10MHz	Ind	TO-100	4-38
MPY634BM	‡	±0.5	0.015	0.15%	2	10MHz	Ind	TO-100	4-38
MPY634SM	‡	±1.0	0.02	0.3%	5	10MHz	MIL	TO-100	4-38
MPY634KP	‡	±2.0	0.03	0.3%	25	10MHz	Ind	DIP	4-38
MPY634KU	‡	**±2.0**	**0.03**	**0.3%**	**25**	**10MHz**	**Com**	**SOIC**	**xxiii**
AD632A	‡	1	0.02	0.3	30	50	Ind		
AD632B	‡	0.5	0.01	0.15	15	50	Ind	TO-100,	Advance
AD632S	‡	1	0.02	0.3	30	50	MIL	DIP	Information
AD632T	‡	0.5	0.01	0.15	15	50	MIL		

‡Same as model above.

NOTE: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C.

*Available in 20-pin ceramic leadless chip carriers.

SPECIAL FUNCTIONS

This group of models offers many different functions that are the quick, easy way to solve a wide variety of analog computational problems. Most are in integrated circuit packages and are laser-trimmed for excellent accuracy.

SPECIAL FUNCTIONS						
Function	Model	Description	Comments	Temp Range(1)	Package	Page
Multifunction Converter	4302	$Y\ (Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	Plastic package.	Ind	DIP	4-111
	LOG100JP	K Log (I_1/I_2)	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.	Com	DIP	4-15
Logarithmic Amplifier	4127JG 4127KP	K Log (I_1/I_{REF})	A more versatile part which contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com Com	DIP DIP	4-90 4-90
$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2\,(t)\,dt}$	4341	True rms-to-DC conversion based on a log-antilog occupational approach.	Some external trimming required. Lower cost in plastic package. Pin compatible with 4340.	Ind	DIP	4-119
Peak Detector	4085BM 4085KG 4085SM	These are analog memory circuits which hold and provide read-out of a DC voltage equal to peak value of a complex input waveform.	Digital mode control provides reset capability and allows selection of peaks within a desired time interval. May be used to make peak-to-peak detector.	Com Ind MIL	DIP DIP DIP	4-82 4-82 4-82

NOTE: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C.

Models in **boldface type** are found in this supplement; others are in the Burr-Brown *Integrated Circuits Data Book.*

DIVIDERS

The use of a special log/antilog commited divider design overcomes the major problem encountered when trying to use a multiplier in a divider circuit. Outstanding accuracy is maintained even at very low denominator voltages.

DIVIDERS									
Model	Transfer Function	Input Range	Accuracy, max D = 250mV (%)	Temperature Coefficient (%/°C)	0.5% Bandwidth (kHz)	Rated Output, min	Temp Range[1]	Package	Page
DIV100HP	N/D 10	250mV	1.0	0.2	15	±10V, ±5mA	Ind	DIP	4-7
DIV100JP	N/D 10	to	0.5	0.2	15	±10V, ±5mA	Ind	DIP	4-7
DIV100KP	N/D 10	10V	0.25	0.2	15	±10V, ±5mA	Ind	DIP	4-7

NOTE: (1) Ind = −25°C to +85°C.

FREQUENCY PRODUCTS

This group of products consists of precision oscillators and active filters for both signal generation and attenuation. Both fixed frequency and user-selected frequency units are available.

FREQUENCY PRODUCTS						
Function	Model	Description	Comments	Temp Range[1]	Package	Page
Oscillator	4423	Very-low cost in plastic package. Provides resistor programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP	4-123
Universal Active Filter	UAF41 UAF21	These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass and bandpass outputs are available.	Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.	Ind Ind	DIP DIP	4-68 4-60

NOTE: (1) Com = 0 to +70°C, Ind = −25°C to +85°C.

VOLTAGE REFERENCE

These products are precision voltage references which provide a +10V output. The output can be adjusted with minimal effect on drift or stability.

VOLTAGE REFERENCE								
				Power Supply				
Model	Output (V)	Minimum Output (mA)	Maximum Drift (ppm/°C)	(V)	(mA)	Temp Range[1]	Package	Page
REF10KM*	+10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	4-46
REF10JM	+10.00 ±0.005	10	2	+13.5/35	4.5	Com	TO-99	4-46
REF10SM	+10.00 ±0.005	10	3	+13.5/35	4.5	MIL	TO-99	4-46
REF10RM	+10.00 ±0.005	10	6	+13.5/35	4.5	MIL	TO-99	4-46
REF101KM*	+10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	4-52
REF101JM	+10.00 ±0.005	10	2	+13.5/35	4.5	Com	TO-99	4-52
REF101SM	+10.00 ±0.005	10	3	+13.5/35	4.5	MIL	TO-99	4-52
REF101RM	+10.00 ±0.005	10	6	+13.5/35	4.5	MIL	TO-99	4-52

*Available in 20-pin ceramic leadless chip carriers.
NOTE: (1) Com = 0 to +70°C, MIL = −55 to +125°C.

DATA CONVERSION AND DATA ACQUISITION

ANALOG-TO-DIGITAL CONVERTERS										
Description	Model	Q[1] Screen	Resolution (Bits)	Linearity Error (% FSR)	Conversion Time (μs)	Gain Tempco (ppm/°C)	Temp Range[2]	Input Range[3] (V)	Package	Page
Very High Speed	ADC803	Q	12	±0.012	1.5	30	MIL, Ind	10, 20, U/B	Hermetic Metal DIP	5-102
Ultra High Speed	**ADC600**		**12**	**±0.015**	**0.1**	**30**	**Com**	**1.25 B**	**Module**	**103**
Serial Out	ADC804	Q	12	±0.012	17	30	MIL, Com, Ind	5, 10, 20 U/B	Hermetic Ceramic DIP	5-114
Low Cost, Microprocessor Interface	ADC574	Q	12	±0.012	25	25	MIL,	10, 20 U/B	Hermetic Ceramic DIP	5-80
	ADC674	Q	12	±0.012	15	25	Com, Ind	10, 20 U/B	Hermetic Ceramic DIP	5-93
Low Cost	ADC80AG	Q	12	±0.012	25	30	Ind	5, 10, 20 U/B	Hermetic Ceramic DIP	5-56
	ADC80MAH	**QM**	**12**	**±0.012**	**25**	**30**	**Ind**	**5, 10, 20 U/B**	**Hermetic Ceramic DIP**	**87**
High Temp	ADC10HT		12	±0.012	50	35	−55°C to +200°C	10, 20, U/B	Hermetic Ceramic DIP	5-3
High Speed, Low Cost	**ADC84**	**Q**	**12**	**±0.012**	**10**	**30**	**Com**	**5, 10, 20 U/B**	**Hermetic Ceramic DIP**	**95**
High Speed, Wide Temp	**ADC85H**	**Q**	**12**	**±0.012**	**10**	**30**	**Ind**	**5, 10, 20 U/B**	**Hermetic Ceramic DIP**	**95**
	ADC87H	**Q**	**12**	**±0.012**	**10**	**30**	**MIL**	**5, 10, 20 U/B**	**Hermetic Ceramic DIP**	**95**
High Resolution	ADC71	Q	16	±0.003	50	15	Ind, Com	5, 10, 20 U/B	Ceramic DIP	5-13
	ADC72	Q	16	±0.003	50	15	Ind, Com	5, 10, 20 U/B	Hermetic Metal DIP	5-21
	ADC76	Q	16	±0.003	17	15	Ind, Com	5, 10, 20 U/B	Ceramic DIP	5-40
Audio	PCM75		16	0.006% THD	17	20	Com	5, 10, 20 U/B	Ceramic DIP	5-122

NOTES: (1) "Q" or "QM" indicates product available with screening for enhanced reliability. (2) Com = 0°C to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C. (3) U = Unipolar, B = Bipolar.

DIGITAL-TO-ANALOG CONVERTERS										
Description	Model	Q[1] Screen	Resolution (Bits)	Linearity Error (% FSR)	Settling Time (μs)	Gain Tempco (ppm/°C)	Temp Range[2]	Output Range[3]	Package	Page
Very High Resolution	**DAC729**	**Q**	**18**	**±0.00075**	**5**	**15**	**Com**	**10V, 20V U/B**	**Hermetic Ceramic DIP**	**141**
High Resolution	DAC700	QM	16	±0.0015	1	10	MIL, Com, Ind	−1mA	Hermetic	6-98
	DAC701	QM	16	±0.0015	8	10	MIL, Com, Ind	10V, 20V U/B	Ceramic DIP,	6-98
	DAC702	QM	16	±0.0015	1	10	MIL, Com, Ind	±1mA	Plastic DIP,	6-98
	DAC703	QM	16	±0.0015	8	10	MIL, Com, Ind	10V, 20V U/B	LCC, Die	6-98
Bus Interface, High Resolution	DAC705	QM	16	±0.003	8	15	MIL, Com, Ind	10V, 20V U/B	Hermetic Ceramic DIP	6-106
	DAC706	QM	16	±0.003	1	15	MIL, Com, Ind	±1mA	Hermetic Ceramic DIP	6-106
	DAC707	QM	16	±0.003	8	15	MIL, Com, Ind	10V, 20V U/B	Hermetic Ceramic DIP, Plastic DIP	6-106
	DAC708	QM	16	±0.003	1	15	MIL, Com, Ind	2mA, ±1mA	Hermetic Ceramic DIP	6-106
	DAC709	QM	16	±0.003	8	15	MIL, Com, Ind	10V, 20V U/B	Hermetic Ceramic DIP	6-106
High Resolution	DAC70BH	QM	16	±0.003	1, 10	20	Ind	10V, 20V, 2mA U/B	Hermetic Ceramic DIP	6-20
	DAC71	QM	16	±0.003	1, 10	20	Com	10V, 20V, 2mA U/B	Hermetic Ceramic DIP	6-28
	DAC72BH	QM	16	±0.003	1, 10	20	Ind	10V, 20V, 2mA U/B	Hermetic Ceramic DIP	6-20
Low Cost, High Resolution	DAC710		16	±0.003	1	50	Com	±1mA	Hermetic Ceramic	6-116
	DAC711		16	±0.003	8	50	Com	10V, 20V U/B	DIP, Plastic DIP	6-116
Low Cost, Bus Interface	DAC811	QM	12	±0.006	4	20	MIL, Com, Ind	10V, 20V U/B	Hermetic Ceramic DIP, Plastic DIP, SOIC, Die	6-130
CMOS	**DAC7541**	**QM**	**12**	**±0.012**	**2**	**5**	**MIL, Com, Ind**	**Multiplying**	**Hermetic Ceramic DIP, Plastic DIP, SOIC, Die**	**159**
CMOS, Bus Interface	**DAC7545**	**QM**	**12**	**±0.012**	**2**	**5**	**MIL, Com, Ind**	**Multiplying**	**Hermetic Ceramic DIP,**	**167**
	DAC8012	**QM**	**12**	**±0.012**	**1**	**5**	**MIL, Com, Ind**	**Multiplying**	**Plastic DIP, SOIC, Die**	**174**
Low Cost, Industry Standard	DAC80		12	±0.012	0.3, 3 typ	30	Com	10V, 20V, 2mA U/B	Hermetic Ceramic DIP, Plastic DIP, Die	6-64
	DAC85H	QM	12	±0.012	0.3, 3 typ	20	Ind	10V, 20V, 2mA U/B	Hermetic Ceramic DIP	6-85
Military Temp, Industry Standard	DAC87H	QM	12	±0.012	0.3, 3 typ	20	MIL	10V, 20V, 2mA U/B	Hermetic Ceramic DIP	6-85

This table continued on next page.

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DIGITAL-TO-ANALOG CONVERTERS (CONT)										
Description	Model	Q[1] Screen	Resolution (Bits)	Linearity Error (% FSR)	Settling Time (μs)	Gain Tempco (ppm/°C)	Temp Range[2]	Output Range[3]	Package	Page
Ultra High Speed ECL	DAC63	Q	12	±0.012	0.05	30	MIL, Ind	10mA, U/B	Ceramic DIP, Metal Can	6-12
Ultra High Speed TTL	DAC812	Q	12	±0.012	0.065	20	Ind	10mA, U/B	Ceramic DIP, Metal Can	6-138

NOTES: (1) "Q" or "QM" indicates product available with screening for enhanced reliability. (2) MIL = −55°C to +125°C, Com = 0°C to +70°C, Ind = −25°C to +85°C. (3) U = Unipolar, B = Bipolar.

VOLTAGE-TO-FREQUENCY CONVERTERS								
Description	Model[1]	Frequency Range (kHz)	V_{IN} Range (V)	Linearity, max (% of FSR)	Tempco, max (ppm of FSR/°C)	Temp Range[2]	Package	Page
Low Cost, Monolithic	VFC32KP*	User-selected, 500kHz, max	User-selected	±0.01 at 10kHz	75 typ	Com	DIP	10-3
	VFC32BM, (Q)			±0.05 at 100kHz	±100	Ind	TO-100	10-3
	VFC32SM, (Q)			±0.2 at 500kHz	±150	MIL	TO-100	10-3
Low Cost Complete	VFC42BP	0 to 10	0 to +10	±0.01	±100	Ind	DIP	10-11
	VFC42SM	0 to 10	0 to +10	±0.01	±100	MIL	DIP	10-11
	VFC52BP	0 to 100	0 to +10	±0.05	±150	Ind	DIP	10-11
	VFC52SM	0 to 100	0 to +10	±0.05	±150	MIL	DIP	10-11
Precision Monolithic	VFC62BG*	User-selected, 1MHz max	User-selected	±0.005 at 10kHz	±50	Ind	DIP	10-17
	VFC62BM			±0.005 at 10kHz	±50	Ind	TO-100	10-17
	VFC62SM			±0.005 at 10kHz	±50	MIL	TO-100	10-17
	VFC62CG			±0.002 at 10kHz	±20	Ind	DIP	10-17
	VFC62CM			±0.002 at 10kHz	±20	Ind	TO-100	10-17
	VFC320BG*	User-selected, 1MHz max	User-selected	±0.005 at 10kHz	±50	Ind	DIP	10-40
	VFC320BM			±0.005 at 10kHz	±50	Ind	TO-100	10-40
	VFC320SM			±0.005 at 10kHz	±50	MIL	TO-100	10-40
	VFC320CG			±0.002 at 10kHz	±20	Ind	DIP	10-40
	VFC320CM			±0.002 at 10kHz	±20	Ind	TO-100	10-40
Synchronized Monolithic	VFC100AG*	Clock Programmed, 2MHz max	0 to +10	0.025 at 100kHz	±100	Ind	DIP	10-25
	VFC100BG		0 to +10	0.1 at 1MHz	±50	Ind	DIP	10-25
	VFC100SG		0 to +10	0.025 at 100kHz	±100	MIL	DIP	10-25

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. (2) Com = 0 to +70°C, Ind = −25°C to +85°C, MIL = −55°C to +125°C.

*Available in 20-pin ceramic leadless chip carriers.

SAMPLE/HOLD AMPLIFIERS													
Description	Model	Q[1] Screen	Gain Error (% FSR)	Offset Error (mV)	Charge Offset (mV)	Amplifier Bandwidth, −3dB (MHz)	Hold Transient Settling (μs to 1mV)	Acquisition Time (μs) (0.01% FSR)	Aperture Time (ns)	Aperture Jitter (ns)	Input Range (Vp-p)	Package	Page
Ultra High Speed	SHC600	Q	0.1	5	10 max	70	0.015	0.05	8	0.009	2.5	Ceramic DIP	7-21
High Speed With Buffer	SHC803	Q	0.1	3	5 max	16	0.15	0.35	25	0.025	20	Hermetic Metal DIP	7-24
High Speed	SHC804	Q	0.1	3	5 max	16	0.15	0.35	25	0.025	20	Hermetic Metal DIP	7-24
Low Cost	SHC5320	Q		0.5	1 typ	1.5	0.25	1.5	25	0.3	20	Hermetic Ceramic DIP	7-30
	SHC85	Q	0.01	2	2 max		0.5	4.5	30	1.5	20	Hermetic Metal DIP	7-11
	SHC298		0.01	7	25 max		1.5	10	200	15	20	TO-99	7-15

NOTE: (1) "Q" indicates product available with screening for enhanced reliability.

MULTIPLEXERS								
Description	Model	Channels	Input Range (V)	On Resistance, max (Ω)	Crosstalk (% of Off Channel)	Settling Time (to 0.01%)	Package	Page
Protected Inputs	MPC8S	8 Single	±15	1.8k	0.005	5μs	DIP	9-3
	MPC4D	4 Differential	±15	1.8k	0.005	5μs	DIP	9-3
	MPC16S	16 Single	±15	1.8k	0.005	4μs	DIP	9-10
	MPC8D	8 Differential	±15	1.8k	0.005	4μs	DIP	9-10
High Speed	MPC800KG	16 Single or 8 Differential	±15	750	0.004	800ns	DIP	9-17
	MPC800SG	16 Single or 8 Differential	±15	750	0.004	800ns	DIP	9-17
	MPC801KG	8 Single or 4 Differential	±15	750	0.004	800ns	DIP	9-24
	MPC801SG	8 Single or 4 Differential	±15	750	0.004	800ns	DIP	9-24

MILITARY PRODUCTS

ANALOG-TO-DIGITAL CONVERTERS								
Model	Resolution (Bits)	Linearity, max (±LSB)	Conversion Time, max (μs)	Gain Drift, max (±ppm/°C)	Input Range (V)	Operating Temperature Range	Package	Page
ADC87/883B	12	1/2	10	15	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	32-pin DIP	12-8
ADC87	12	1/2	10	15		MIL	32-pin DIP	12-8
ADC87U/883B	12	1/2	10	15		MIL	32-pin DIP	12-8
ADC87U	12	1/2	10	15		MIL	32-pin DIP	12-8
ADC87V/883B	12	1/2	10	15		MIL	32-pin DIP	12-8
ADC87V	12	1/2	10	15		MIL	32-pin DIP	12-8

DIGITAL-TO-ANALOG CONVERTERS									
Model	Resolution (Bits)	Linearity, max (±LSB)	Monotonicity (°C)	Gain Drift, max (±ppm/°C)	Settling Time, max	Output Ranges (V)	Operating Temperature Range	Package	Page
DAC87-CBI-V/B	12	1/2	−55 to +125	20	7μsec	±2.5, ±5, ±10, +5, +10	MIL	24-pin DIP	12-24
DAC87-CBI-V	12	1/2	−55 to +125	20	7μsec		MIL	24-pin DIP	12-24
DAC87U-CBI-V/B	12	1/2	−25 to +85	20	7μsec		MIL	24-pin DIP	12-24
DAC87U-CBI-V	12	1/2	−25 to +85	20	7μsec		MIL	24-pin DIP	12-24
DAC87-CBI-I/B	12	1/2	−55 to +125	20	400nsec	0 to 2mA, ±1mA	MIL	24-pin DIP	12-24
DAC87-CBI-I	12	1/2	−55 to +125	20	400nsec		MIL	24-pin DIP	12-24
DAC87U-CBI-I/B	12	1/2	−25 to +85	20	400nsec		MIL	24-pin DIP	12-24
DAC87U-CBI-I	12	1/2	−25 to +85	20	400nsec		MIL	24-pin DIP	12-24
DAC870V/883B	12	1/2	−55 to +125	25	7μsec	±2.5, ±5, ±10, 0 to +5, 0 to +10	MIL	24-pin DIP	12-48
DAC870V	12	1/2	−55 to +125	25	7μsec		MIL		12-48
DAC870U/883B	12	1/2	−25 to +85	20	7μsec		MIL	ceramic	12-48
DAC870U	12	1/2	−25 to +85	20	7μsec		MIL		12-48
DAC870VL/883B	12	1/2	−55 to +125	25	7μsec		MIL	28-term.	12-48
DAC870VL	12	1/2	−55 to +125	25	7μsec		MIL	leadless	12-48
DAC870UL/883B	12	1/2	−25 to +85	20	7μsec		MIL	chip	12-48
DAC870UL	12	1/2	−25 to +85	20	7μsec		MIL	carrier	12-48
DAC703VG/883B	**16**	**±.003% FSR**	**−55 to +125[1]**	**20**	**8μsec**	**±10**	**MIL**	**24-pin DIP**	**191**
DAC703VG	**16**	**±.003% FSR**	**−55 to +125[1]**	**20**	**8μsec**	**±10**	**MIL**	**24-pin DIP**	**191**
DAC703VL/883B	**16**	**±.003% FSR**	**−55 to +125[1]**	**20**	**8μsec**	**±10**	**MIL**	**28-term.**	**191**
DAC703VL	**16**	**±.003% FSR**	**−55 to +125[1]**	**20**	**8μsec**	**±10**	**MIL**	**LCC**	**191**

NOTE: (1) Monotonicity to 14-bit accuracy.

VOLTAGE-TO-FREQUENCY CONVERTERS							
Model	V_{IN} Range (V)	F_{OUT} Range, max (kHz)	Linearity, max at 10kHz (% FSR)	Full Scale Drift, max (ppm FSR/°C)	Operating Temperature Range	Package	Page
VFC32WM/883B	±10	200	±0.006	±100 at 10kHz	MIL	TO-100	12-135
VFC32WM	±10	200	±0.006	±100 at 10kHz	MIL	TO-100	12-135
VFC32VM/883B	±10	200	±0.01	−400, +150 at 200kHz	MIL	TO-100	12-135
VFC32VM	±10	200	±0.01	−400, +150 at 200kHz	MIL	TO-100	12-135
VFC32UM/883B	±10	200	±0.01	±150 at 10kHz	MIL	TO-100	12-135
VFC32UM	±10	200	±0.01	±150 at 10kHz	MIL	TO-100	12-135

Models in **boldface type** are found in this supplement; others are in the Burr-Brown *Integrated Circuits Data Book.*

MULTIPLIERS								
Model	Accuracy at 25°C, max (±%)	Accuracy at 125°C, max (±%)	Feedthrough, max (±mV)	Output Offset, max (±mV)	Output, min (V, mA)	Operating Temperature Range	Package	Page
4213WM/883B	1/2	4	50	25	±10, ±5	MIL	TO-100	12-166
4213WM	1/2	4	50	25	±10, ±5	MIL	TO-100	12-166
4213VM/883B	1	4	100	30	±10, ±5	MIL	TO-100	12-166
4213VM	1	4	100	50	±10, ±5	MIL	TO-100	12-166
4213UM/883B	1	2[1]	100	50	±10, ±5	MIL	TO-100	12-166
4213UM	1	2[1]	100	50	±10, ±5	MIL	TO-100	12-166

NOTES: (1) At +85°C.

OPERATIONAL AMPLIFIERS												
		Offset Voltage										
Description	Model	At 25°C, max (±mV)	Drift, max (±μV/°C)	Bias Current, max (nA)	Bandwidth Unity Gain, min (MHz)	Slew Rate, min (V/μs)	t_s ±0.01% (ns)	Compensation	Output, min (V, mA)	Operating Temp. Range	Package	Page
Wideband	OPA600VM/883B	2	20	−100pA	5000,[1] A = 1000	400	125	external	±10, ±200	MIL	16-pin DIP	12-94
	OPA600VM	2	20	−100pA		400	125	external	±10, ±200	MIL		12-94
	OPA600UM/883B	5	80	−100pA		400	150	external	±10, ±200	MIL		12-94
	OPA600UM	5	80	−100pA		400	150	external	±10, ±200	MIL		12-94
General Purpose Bipolar	3500R/883B	5	20	±30	1	0.6	—	internal	±10, ±10	MIL	TO-99	12-147
	3500U/883B	5	20[2]	±30	1	0.6	—	internal	±10, ±10	MIL	TO-99	12-147
Precision Bipolar	3510VM/883B	0.12	2	±25	0.25	0.5	—	internal	±10, ±10	MIL	TO-99	12-158
Low Drift, Low Bias	OPA105WM/883B	0.250	2	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
	OPA105WM	0.250	2	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
	OPA105VM/883B	0.250	5	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
	OPA105VM	0.250	5	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
	OPA105UM/883B	0.250	15[2]	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
	OPA105UM	0.250	15[2]	−1pA	1	0.9	—	internal	±10, ±10	MIL	TO-99	12-74
Ultra Low Bias Current	OPA106WM/883B	0.250	5	−100fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
	OPA106WM	0.250	5	−100fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
	OPA106VM/883B	0.250	10	−150fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
	OPA106VM	0.250	10	−150fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
	OPA106UM/883B	0.250	20[2]	−300fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
	OPA106UM	0.250	20[2]	−300fA	1	1.2	—	internal	±10, ±5	MIL	TO-99	12-84
Low Drift, Low Bias, Low Noise	**OPA111VM/883B**	**0.500**	**10**	**±2pA**	**2**	**1**	—	**internal**	**±10, ±5**	**MIL**	**TO-99**	**210**
	OPA111UM	**0.500**	**10**	**±2pA**	**2**	**1**	—	**internal**	**±10, ±5**	**MIL**	**TO-99**	**210**
Power	**OPA501VM/883B**	**5**	**40**	**±20**	**1**	**1.35**	—	**internal**	**±26, ±10A**	**MIL**	**TO-3**	**222**
	OPA501VM	**5**	**40**	**±20**	**1**	**1.35**	—	**internal**	**±26, ±10A**	**MIL**	**TO-3**	**222**
	OPA501UM/883B	**10**	**65**	**±40**	**1**	**1.35**	—	**internal**	**±20, ±10A**	**MIL**	**TO-3**	**222**
	OPA501UM	**10**	**65**	**±40**	**1**	**1.35**	—	**internal**	**±20, ±10A**	**MIL**	**TO-3**	**222**
	OPA8780VM/883B	10	30	−0.05	5	15	—	internal	±30, ±60	MIL	TO-3	12-1110
	OPA8780VM	10	30	−0.05	5	15	—	internal	±30, ±60	MIL	TO-3	12-1110
	OPA8780UM/883B	10	50	−0.05	5	15	—	internal	±30, ±60	MIL	TO-3	12-1110
	OPA8780UM	10	50	−0.05	5	15	—	internal	±30, ±60	MIL	TO-3	12-1110

NOTES: (1) Gain-bandwidth product. (2) −25°C to +85°C.

INSTRUMENTATION AMPLIFIERS											
						Input Parameters					
Description	Model	Gain Range[1]	Gain Accuracy, G = 100, At 25°C, max (%FS)	Gain Drift, G = 100, typ (ppm/°C)	Non-linearity G = 100 max	CMR, DC to 60Hz, G = 10, min, 1kΩ Unbal. (dB)	Offset Voltage vs Temp, G = 1000, max (μV/°C)	Dynamic Response, G = 100, ±3dB BW (kHz)	Temp Range	Package	Page
Very High Accuracy	**INA101VG/883B**	**1-1000**	**0.10**	**22**	**0.007**	**96**	**1.75**	**25**	**MIL**	**DIP**	**200**
	INA101VG	**1-1000**	**0.10**	**22**	**0.007**	**96**	**1.75**	**25**	**MIL**	**DIP**	**200**
	INA101VM/883B	**1-1000**	**0.10**	**22**	**0.007**	**96**	**1.75**	**25**	**MIL**	**TO-100**	**200**
	INA101VM	**1-1000**	**0.10**	**22**	**0.007**	**96**	**1.75**	**25**	**MIL**	**TO-100**	**200**
	INA258WG/883B	1-1000	0.10	22	0.007	96	0.5	25	MIL	DIP	12-61
	INA258WG	1-1000	0.10	22	0.007	96	0.5	25	MIL	DIP	12-61
	INA258VG/883B	1-1000	0.10	22	0.007	96	1.0	25	MIL	DIP	12-61
	INA258VG	1-1000	0.10	22	0.007	96	1.0	25	MIL	DIP	12-61
	INA258UG/883B	1-1000	0.10	22	0.007	96	3.0	25	MIL	DIP	12-61
	INA258UG	1-1000	0.10	22	0.007	96	3.0	25	MIL	DIP	12-61
	INA258WL/883B	1-1000	0.10	22	0.007	96	0.5	25	MIL	20-terminal leadless chip carrier	12-61
	INA258WL	1-1000	0.10	22	0.007	96	0.5	25	MIL		12-61
	INA258VL/883B	1-1000	0.10	22	0.007	96	1.0	25	MIL		12-61
	INA258VL	1-1000	0.10	22	0.007	96	1.0	25	MIL		12-61
	INA258UL/883B	1-1000	0.10	22	0.007	96	3.0	25	MIL		12-61
	INA258UL	1-1000	0.10	22	0.007	96	3.0	25	MIL		12-61

NOTES: (1) Set with external resistor.

Models in **boldface type** are found in this supplement; others are in the Burr-Brown *Integrated Circuits Data Book.*

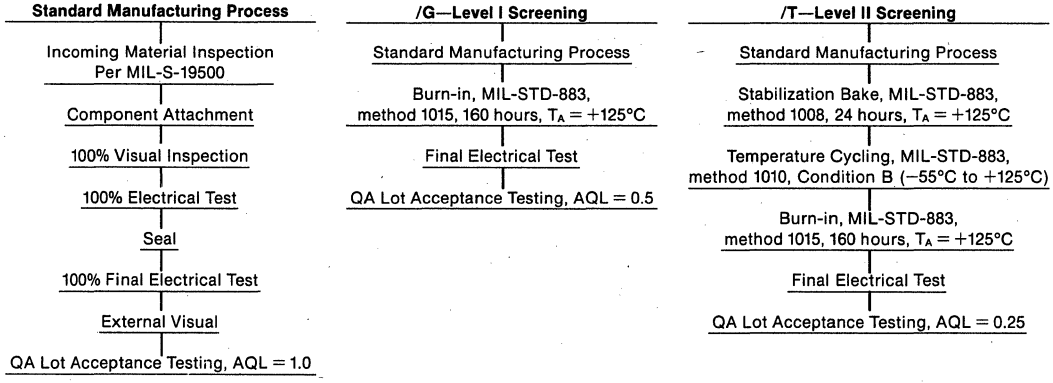
MODULAR POWER SUPPLIES

DC/DC CONVERTERS							
Description	Model	Input (VDC)	Output	Isolation (VDC)	Leakage Current, max (μA)	Package	Page
Unregulated	PWR1xx	5 to 48	450mW	1000	5	Module	14-9
Unregulated	PWR2xx	5 to 48	1.5W	1000	5	Module	14-11
Unregulated	PWR3xx	5 to 48	2W, dual channel	1000	5	Module	14-13
Unregulated	PWR4xx	5 to 48	3W	1000	5	Module	14-15
Unregulated	PWR5xx	5 to 48	4W	750	15	Module	14-17
Regulated	PWR6xx	5 to 48	2W	1000	20	Module	14-19
Regulated	**PWR7xx**	**5 to 48**	**5W**	**1000**	**25**	**Module**	**237**
Unregulated	PWR8xx	5 to 48	5W, triple output	1000	5	Module	14-25
Unregulated	PWR70	10 to 18	±15VDC, ±15mA	2000	2	Module	14-27
Unregulated	PWR71	10 to 18	±15VDC, ±25mA	1000	3	Module	14-29
Unregulated	PWR72	5 to 22	±15VDC, ±100mA	1000	3	Module	14-31
Unregulated	PWR74	10 to 20	±15VDC, ±25mA	1500	2	Module	14-33
Unregulated	**PWR1017**	**10 to 18**	**±15VDC, ±25mA, 4 channels**	**1000**	**3**	**Module**	**241**
Regulated	**PWR5038**	**4.75 to 5.25**	**2.75W, triple output**	**500**	**5**	**Module**	**245**
Regulated	**PWR5104**	**4.75 to 5.25**	**±12VDC, ±370mA**	**750**	**15**	**Module**	**247**
Regulated	**PWR5105**	**4.75 to 5.25**	**±15VDC, ±300mA**	**750**	**15**	**Module**	**247**

NOTES: (1) Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields. Models 700M and 700UM are similar to models 700 and 700U, but in addition, they are 100% screened to patient-connected circuit requirements for the leakage current (par. 27.5) and withstand voltage (par. 31.11) of UL544. Additional per-unit charge for 700M or 700UM. (2) Model 710 provides four channels (sets) of isolated outputs.

RELIABILITY

All Burr-Brown PWR Series DC/DC converters are manufactured using stringent in-process controls and quality inspections. The customer may also choose one of two additional levels of screening to meet specific requirements. The advanced reliability program is designed to reduce infant mortality, system rework, field failures, and equipment downtime.



BURR-BROWN—A WORLDWIDE LEADER IN MICROCIRCUITS AND MICROPROCESSOR-BASED SYSTEMS AND SUBSYSTEMS

Burr-Brown first introduced VMEbus products in 1983 and now manufactures a comprehensive line of specialized products for the industrial instrumentation, control, and automation markets. Utilizing Burr-Brown's high performance data conversion products (e.g. ADC803), Burr-Brown is able to offer products which set new performance standards in the VMEbus market. When these are operated with the digital signal processing boards, a wide range of applications can be addressed.

With over ten years experience in the design and manufacture of board-level products, you can rely on the market leaders for VMEbus data acquisition boards.

THE SYSTEMS APPROACH

A systems approach has been taken in the design of the bus interface. This ensures software compatibility between the boards as well as giving the system designer a wide range of VMEbus features.

- Configuration A24, D16, DTB slave
- Address block selectable within 16M bytes memory space
- Short addressing available if required (64 bytes)
- 150ns response to CPU interrogation
- 7-level interrupt priority selection
- Full interrupt vector selection—8 lines (256 options)
- Double Eurocard format, 160mm × 233mm

SUPPORT DOCUMENTATION

Each VMEbus board is fully supported with a comprehensive operating manual. In addition to detailed set-up and operating instructions, the manual includes schematics and assembly language software written for the 68000 processor.

TOP-QUALITY VMEbus PRODUCTS FROM BURR-BROWN

In addition to the full Q.C. inspection of incoming components, the boards are subjected to a comprehensive temperature-cycled burn-in (8 cycles between −20°C and +50°C).

Exhaustive tests before and after burn-in ensure that any problems are identified before the product leaves the factory.

VMEbus ANALOG I/O BOARDS

	Input			Output			
Product	Resolution (Bits)	Number of Channels	Sampling Rate (kHz)	Resolution (Bits)	Number of Channels	Sampling Rate (kHz)	Description
MPV901	12	32SE/16DIF	11	—	—	—	General purpose, analog input.
MPV901A	12	32SE/16DIF	11	12	2	200	As MPV901, with analog output.
MPV901P	12	32SE/16DIF	11	12	2	200	As MPV901A, with software-programmable gain.
MPV904	—	—	—	12	16	285Hz	Low-cost analog output (voltage output).
MPV905	—	—	—	12	8	285Hz	Current output.
MPV906	12	64SE/32DIF	33	—	—	—	High-density analog input, optically isolated, optional digital I/O.
ACX906	—	—	—	—	—	—	Digital I/O module for MPV906/907, 32 I/O lines.
MPV907	12	32SE/16DIF	33	—	—	—	Low-cost analog input, optional digital I/O.
MPV911	16	8SE	45	—	—	—	High resolution analog input, with on-board data buffer.
MPV950S	12	16SE	330	—	—	—	High speed analog input.
MPV950D	12	8SE + 8DIF	330	—	—	—	As MPV950S, with 8 user-configurable input amplifiers.
MPV952	12	8SE	330	—	—	—	High speed analog input, with on-board data buffer.
MPV954	—	—	—	12	8	858	High speed analog output, with on-board data buffer.
MPV940	—	—	—	—	—	—	Intelligent I/O controller—6800 CPU, optically isolated I/O expansion interface.
ACX945A	12	16SE/8DIF	33	—	—	—	Analog input module for MPV940.
ACX945B	12	16SE/8DIF	33	12	4	500	As ACX945A, with 12-bit analog output.
ACX945C	12	16SE/8DIF	33	16	4	83	As ACX945A, with 16-bit analog output.
ACX946	—	—	—	—	—	—	Digital I/O module for MPV940, 32 programmable I/O lines.

VMEbus DIGITAL I/O			
Product	Number of Channels	Type	Description
MPV902	32	Relay contact output	28VDC at 0.5A, 10W max output rating.
MPV910	32	Optical isolated input	
MPV910NS	32	Optical isolated input	As MPV910 without power supply.
MPV910LV	32	Optical isolated input	As MPV910NS for low voltage inputs.
MPV930	48	TTL level I/O	Lines programmable as input or output in groups of eight.

VMEbus DIGITAL SIGNAL PROCESSING BOARDS	
Product	Description
SPV100	A VMEbus board for general purpose DSP, based on the Texas Instruments TMS32010. Swinging buffer data memory for pipelining of data input/output and processing. Program ROM and RAM for user programming.
FFT100[1]	Fast Fourier Transform firmware for the SPV100. FFT-1 64 points, -3 256 points, -4 512 point, -5 1024 point transform.
FIL100[1]	Digital filter firmware for the SPV100. From 5 to 89 taps.
COR100[1]	Correlation firmware for the SPV100. Auto-and cross-correlation.
ASM310V	TMS32010 cross-assembler. Runs under VERSAdos.
MON100V	Monitor/debugger software for SPV100. Runs under VERSAdos.
APS100V[1]	DSP applications software library for SPV100. Includes vector operations, correlation, trigonometric functions, interpolation and decimation, filtering, windowing and FFTs. Routines are called from FORTRAN running under VERSAdos.
SPV120	Second generation DSP board based on TMS32020. Two RS-232 ports, auxiliary input and output ports, DMA controller for faster I/O concurrent with processing. Program RAM, bipolar ROM and EPROM. Supplied with EPROM-based debug monitor.
ACX120A	Add-on program RAM module for SPV120—16k × 16 bits.
ACX120B	Add-on program RAM module for SPV120—80k × 16 bits.
ASM320V	TMS32020 cross-assembler for SPV120. Runs under VERSAdos.
MON120V	Monitor/debugger software for SPV120. Runs under VERSAdos.
APS120V[1]	DSP applications software library for SPV120. Includes vector operations, correlation, trigonometric functions, interpolation and decimation, filtering, windowing and FFTs. All routines are callable from FORTRAN running under VERSAdos.
MPV960	Analog input and DSP. Four channels of simultaneously sampled analog input (at 100kHz sampling rate) plus TMS32010 processor. Applications in digital filtering, signal averaging, etc.
ACX960	Add-on program RAM/ROM module for MPV960. Includes debug monitor and basic data acquisition routines.
MPV990	Anti-aliasing filter board. Four independent programmable filters, with user-configurable front ends. Ideal for use with MPV960.

NOTE: (1) This software is also available as source code. To order, add S suffix to product code; e.g., APS100VS.

SOFTWARE DRIVERS FOR VMEbus BOARDS	
Product	Description
PSOA	pSOS drivers for MPV901, MPV904, MPV905, MPV950, MPV952. Distributed in UNIX format 5-1/4" floppy disks.
PSOA-P	As PSOA, but distributed in MS-DOS format disks.
PSOB	pSOS drivers for MPV960, SPV100. Distributed in UNIX format 5-1/4" floppy disks.
PSOB-P	As PSOB, but distributed in MS-DOS format disks.
VDR100	VERSAdos driver for SPV100.
VDR120	VERSAdos driver for SPV120.

SURFACE MOUNT MICROCIRCUITS

Burr-Brown is the first manufacturer to offer high performance microcircuits in a wide variety of surface mount packages. These packages permit denser layouts on one or both sides of a PC board, often saving 50% or more of the space normally required for these analog circuits. Many of these miniature devices also fit inside transducer cavities and may be used on modules or even hybrid circuits. Packages currently available are:

- **SOIC**—Plastic small-outline package, gull-wing leads on 1.27mm centers. Example: SOIC-8 has 8 leads.
- **LCC**—Ceramic leadless chip carrier, terminals on 1.27mm centers. Example: LCC-20 has 20 terminals.

SURFACE MOUNT DEVICES					
Device Type	Description	Model	Package	Dimensions (mm)	Product Data Sheet
Analog Multipliers/Dividers	Low Cost	MPY100L	LCC-20	9.0 × 9.0	LCC Short Form
	Precision	4213L	LCC-20	9.0 × 9.0	LCC Short Form
Current Transmitters/Converters	Two-Wire, 4-20mA	XTR101L	LCC-20	9.0 × 9.0	LCC Short Form
		XTR101U	SOIC-16	10.4 × 7.5	PDS-734
	Voltage-to-Current Converters	XTR110L	LCC-20	9.0 × 9.0	LCC Short Form
		XTR110U	SOIC-16	10.4 × 7.5	PDS-731
Digital-to-Analog Converters	16-Bit, Monolithic	DAC700-703BL	LCC-28	11.4 × 11.4	PDS-494
	16-Bit, Monolithic, Military	DAC703L	LCC-28	11.4 × 11.4	PDS-751
	12-Bit, μP-Compatible	DAC811U	LCC-28	11.4 × 11.4	PDS-503
	12-Bit, Monolithic	DAC850L	LCC-28	11.4 × 11.4	PDS-453
	12-Bit, MIL Temp	DAC851L	LCC-28	11.4 × 11.4	PDS-453
	12-Bit, Military	DAC870L	LCC-28	11.4 × 11.4	PDS-511
	12-Bit, CMOS	DAC7541AU	SOIC-18	11.6 × 7.5	PDS-639
	16-Bit, Digital Audio	PCM55	SOIC-24	15.8 × 9.0	PDS-619
Instrumentation Amplifiers	Precision, Monolithic	INA101L	LCC-20	9.0 × 9.0	LCC Short Form
		INA101U	SOIC-16	10.4 × 7.5	PDS-730
	Low Power	INA102L	LCC-20	9.0 × 9.0	LCC Short Form
	Unity Gain, Differential	INA105L	LCC-20	9.0 × 9.0	LCC Short Form
		INA105U	SOIC-8	4.9 × 3.9	PDS-693
	Fast, FET Input	INA110L	LCC-20	9.0 × 9.0	LCC Short Form
		INA110U	SOIC-16	10.4 × 7.5	PDS-733
	Precision, Military	INA258L	LCC-20	8.9 × 8.9	PDS-501
Operational Amplifiers	Electrometer	AD515L	LCC-20	9.0 × 9.0	LCC Short Form
	Ultra-Low Noise	OPA27/37L	LCC-20	9.0 × 9.0	LCC Short Form
		OPA27/37U	SOIC-8	4.9 × 3.9	PDS-691
	Precision, *Difet*®	OPA111L	LCC-20	9.0 × 9.0	LCC Short Form
	Low Cost, *Difet*	OPA121L	LCC-20	9.0 × 9.0	LCC Short Form
		OPA121U	SOIC-8	4.9 × 4.9	PDS-692
	Electrometer Grade	OPA128L	LCC-20	9.0 × 9.0	LCC Short Form
	High Speed, Quad	OPA404L	LCC-20	9.0 × 9.0	LCC Short Form
	Precision, Dual	OPA2111L	LCC-20	9.0 × 9.0	LCC Short Form
Precision Analog Multipliers	Low Cost, Monolithic	MPY534L	LCC-20	9.0 × 9.0	LCC Short Form
	Wide Bandwidth	MPY634L	LCC-20	9.0 × 9.0	LCC Short Form
Precision Voltage References	Ultra-Stable	REF10L	LCC-20	9.0 × 9.0	LCC Short Form
	Low Drift	REF101L	LCC-20	9.0 × 9.0	LCC Short Form
Voltage-to-Frequency and Frequency-to-Voltage Converters	Low Cost, Monolithic	VFC32L	LCC-20	9.0 × 9.0	LCC Short Form
	Precision, Monolithic	VFC62L	LCC-20	9.0 × 9.0	LCC Short Form
	Synchronized	VFC100L	LCC-20	9.0 × 9.0	LCC Short Form
	Precision, Monolithic	VFC320L	LCC-20	9.0 × 9.0	LCC Short Form
Data Acquisition System	12-Bit, 16-Channel	SDM862/863L	LCC-68	24.3 × 24.3	PDS-686

Difet® Burr-Brown Corp.

HIGH PERFORMANCE CHIPS

HIGH PERFORMANCE DICE BACKED BY BURR-BROWN'S TRADITION OF QUALITY

Many of Burr-Brown's high-performance monolithic products are available in die form, including D/A converters, precision operational and instrumentation amplifiers, current transmitters, voltage/frequency converters, and many more.

All Burr-Brown dice products are the same as those used in our high quality, high performance monolithic and hybrid devices and are proven in demanding applications throughout the world. The dice are manufactured and tested at our Tucson Microtechnology facility using the most advanced equipment and methods available, assuring total control of quality and reliability for every product.

The state-of-the-art performance achieved by these precision monolithic products reflects Burr-Brown's unmatched technical capabilities in low noise processing, high stability nichrome thin-film resistors, active laser trimming, dielectric isolation, and patented circuit design.

At Burr-Brown concern for quality is a fundamental part of wafer processing. Dice are 100% visually inspected according to MIL-STD-883, Method 2010, Condition B. All wafers are 100% probe tested to specified electrical test limits.

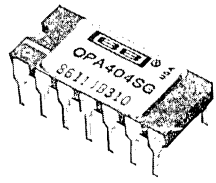
Our newest products are described below. See also our current *Integrated Circuits Data Book* for additional product information.

HIGH PERFORMANCE CHIPS

Description	Model	Die Size (mils)	Key Specifications*	Product Data Sheet	
				Die	Packaged
Unity-Gain Differential Amplifier	INA105AD	83 × 63	±0.01% max DC Gain Error	PDS-703	PDS-617
Precision Instrumentation Amplifier	INA110AD	139 × 89	±0.01%FS max Nonlinearity	PDS-702	PDS-645
Precision Analog Multiplier	MPY534AD	100 × 92	$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$	PDS-711	PDS-614
Difet® Electrometer-Grade Operational Amplifier	OPA128JD	96 × 71	±40pA max Bias Current	PDS-704	PDS-653
High Speed *Difet* Operational Amplifier	OPA606KD	65 × 54	±2mV max Offset Voltage	PDS-660	PDS-598
Precision Two-Wire Transmitter	XTR101AD	150 × 105	4-20mA Operating Range		PDS-708
Voltage-to-Current Converter/Transmitter	XTR110AD	109 × 78	±0.025% of Span max Nonlinearity		PDS-605A

*These specifications are probed at the wafer level. Consult the product data sheet for the packaged device for complete characterization.
Difet® Burr-Brown Corp.

BURR-BROWN®



OPA404

NEW PACKAGE
NOW AVAILABLE

Quad High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±750μV max
- LOW BIAS CURRENT: ±4pA max
- FAST SETTLING: 1.5μs to 0.01%
- STANDARD QUAD PINOUT

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

The OPA404 is a high performance monolithic *Difet*® (dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias current together with wide bandwidth and fast slew rate.

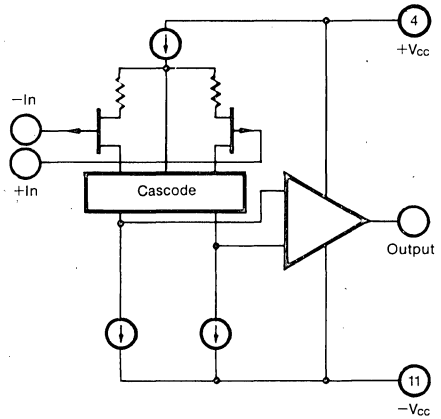
Noise, bias current, voltage offset, drift, and speed are superior to BIFET® amplifiers.

Laser trimming of thin-film resistors gives very-low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.

Difet® Burr-Brown Corp., BIFET® National Semiconductor Corp.



OPA404 Simplified Circuit
(Each Amplifier)

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE[1]											
Voltage: f_O = 10Hz			32			*			*		nV/√Hz
f_O = 100Hz			19			*			*		nV/√Hz
f_O = 1kHz			15			*			*		nV/√Hz
f_O = 10kHz			12			*			*		nV/√Hz
f_B = 10Hz to 10kHz			1.4			*			*		µV, rms
f_B = 0.1Hz to 10Hz			0.95			*			*		µV, p-p
Current: f_B = 0.1Hz to 10Hz			12			*			*		fA, p-p
f_O = 0.1Hz to 20kHz			0.6			*			*		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage	V_{CM} = 0VDC		±260	±1mV		*	±750		*	*	µV
KP			±750	±2.5mV							µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3			*			*		µV/°C
KP			±5								µV/°C
Supply Rejection	±V_{CC} = 12V to 18V	80	100		86	*		*	*		dB
KP		76	100								dB
			10	100		*	50		*	*	µV/V
KP			10	200							µV/V
Channel Separation	100Hz, R_L = 2kΩ		125			*			*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±1	±8		*	±4		*	*	pA
KP			±1	±12							pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.5	8		*	4		*	*	pA
KP			0.5	12							pA
IMPEDANCE											
Differential			10^{13} ‖ 1			*			*		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			*			*		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10.5	+13, −11		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	88	100		92	*		*	*		dB
KP		84	100								dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq$ 2kΩ	88	100		92	*		*	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	4	6.4		5	*		*	*		MHz
Full Power Response	20V p-p, R_L = 2kΩ		570			*			*		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	24	35		28	*		*	*		V/µs
Settling Time: 0.1%	Gain = −1, R_L = 2kΩ		0.6			*			*		µs
0.01%	C_L = 100pF, 10V step		1.5			*			*		µs
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11.5	+13.2, −13.8		*	*		*	*		V
Current Output	V_O = ±10VDC	±5	±10		*	*		*	*		mA
Output Resistance	1MHz, open loop		80			*			*		Ω
Load Capacitance Stability	Gain = +1		1000			*			*		pF
Short Circuit Current		±10	±18	±20	*	*	*	*	*	*	mA
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range,											
Derated Performance		±5		±18	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		9	10		*	*		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient temp.	−25		+85	*		*	−55		+125	°C
KP		0		+70							°C
Operating	Ambient temp.	−55		+125	*		*	*		*	°C
KP		−25		+85							°C
Storage	Ambient temp.	−65		+150	*		*	*		*	°C
θ Junction-Ambient			100			*			*		°C/W
KP			120								°C/W

*Specification same as OPA404AG.

NOTES: (1) Noise testing available—inquire.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient temp.	−25		+85	*		*	−55		+125	°C
KP		0		+70							°C
INPUT											
OFFSET VOLTAGE											
Input Offset Voltage	V_{CM} = 0VDC		±450	2mV		*	±1.5mV		±550	±2.5mV	µV
KP			±1	±3.5							mV
Average Drift			±3			*			*		µV/°C
KP			±5								µv/°C
Supply Rejection		75	96		80	*		70	93		dB
			16	178		*	100		22	316	µV/V
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±32	±200		*	±100		±500	±5nA	pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		17	100		*	50		260	2.5nA	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10.2	+12.7,−10.6		*	*		±10	+12.6,−10.5		V
Common-Mode Rejection	V_{IN} = ±10VDC	82	99		86	*		80	88		dB
KP		80	99								dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	82	94		86	*		80	88		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11.5	+12.9,−13.8		*	*		±11	+12.7,−13.8		V
Current Output	V_O = ±10VDC	±5	±9		*	*		*	±8		mA
Short Circuit Current	V_O = 0VDC	±5	±12	±30	*	*	*	±8	±10	*	mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		9.3	10.5		*	*		9.4	11	mA

*Specification same as OPA404AG.

ORDERING INFORMATION

OPA404 X X

- Basic model number
- Performance grade
  - K = 0°C to +70°C
  - A, B = −25°C to +85°C
  - S = −55°C to +125°C
- Package code
  - G = 14-pin ceramic DIP
  - P = 14-pin plastic DIP

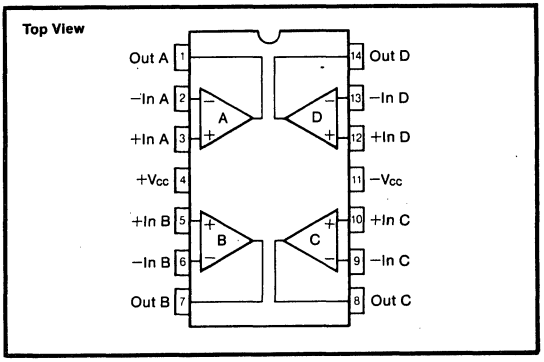
NOTE:
Refer to complete data sheet PDS-677 for complete typical curves and applications information.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	1000mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	P = −40/+85°C, G = −65/+150°C
Operating Temperature Range	P = −25/+85°C, G = −55/+125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES:
(1) Packages must be derated based on θ_{JC} = 30°C/W or θ_{JA} = 120°C/W.
(2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to: 18V > V_{IN} > $-V_{CC}$ − 8V. See Figure 2.
(3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

CONNECTION DIAGRAM

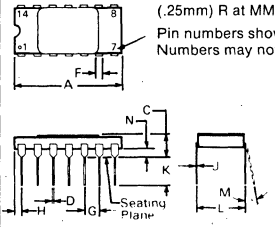


MECHANICAL

"G" Package

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

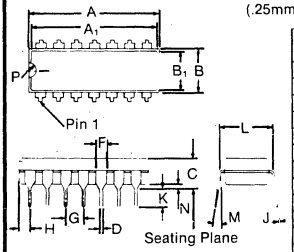


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	.10°	—	10°
N	.009	.060	0.23	1.52

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

"P" Package 14-pin plastic DIP

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.



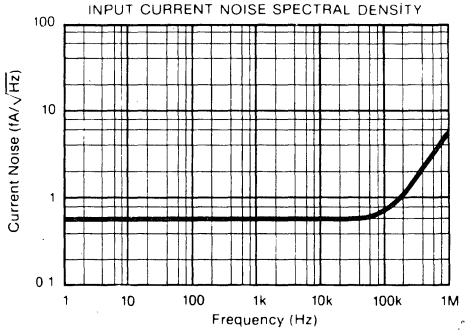
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.700	.800	17.78	20.32
A_1	.685	.785	17.40	19.94
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.050	.100	1.27	2.54
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

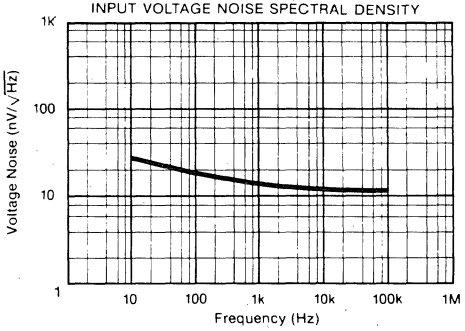
TYPICAL PERFORMANCE CURVES

T_A +25°C, V_{CC} = ±15VDC unless otherwise noted

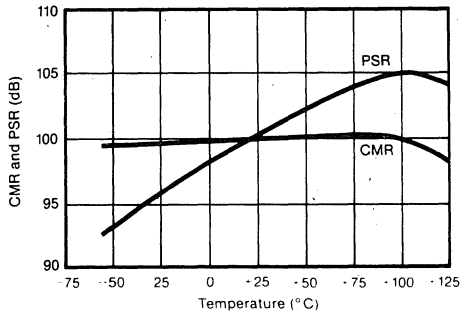
INPUT CURRENT NOISE SPECTRAL DENSITY



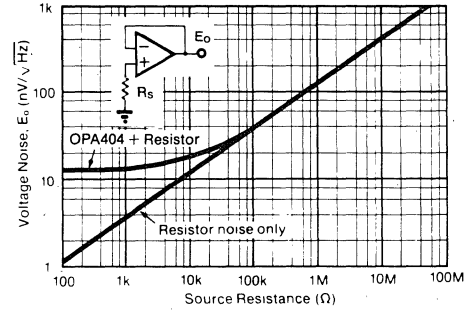
INPUT VOLTAGE NOISE SPECTRAL DENSITY



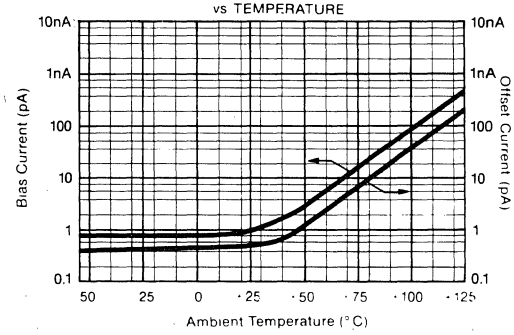
POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



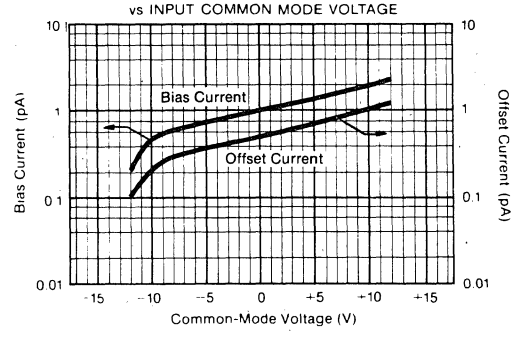
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



BIAS AND OFFSET CURRENT vs TEMPERATURE



BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



BURR-BROWN®

OPA445

ADVANCE INFORMATION
Subject to Change

High Voltage FET-Input OPERATIONAL AMPLIFIER

FEATURES

- WIDE POWER SUPPLY RANGE: ±10V to ±50V
- HIGH SLEW RATE: 10V/μs
- LOW INPUT BIAS CURRENT: 50pA max
- STANDARD-PINOUT TO-99 PACKAGE

APPLICATIONS

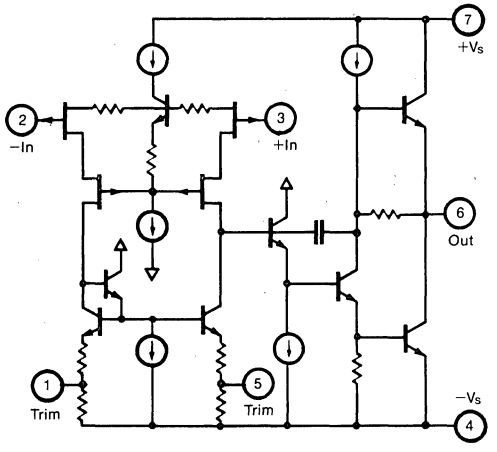
- TEST EQUIPMENT
- HIGH VOLTAGE REGULATORS
- POWER AMPLIFIERS
- DATA ACQUISITION
- SIGNAL CONDITIONING

DESCRIPTION

The OPA445 is a monolithic operational amplifier capable of operation from power supplies up to ±50V and output currents of 15mA. It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings.

The OPA445's high slew rate provides wide power-bandwidth response, which is often required for high voltage applications. FET input circuitry allows the use of high impedance feedback networks, thus minimizing their output loading effects. Laser trimming of the input circuitry yields low input offset voltage and drift.

The OPA445 is unity-gain stable and requires no external compensation components. It is available in both industrial (−25°C to +85°C) and military (−55°C to +125°C) temperature ranges.



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SPECIFICATIONS

ELECTRICAL

At $V_S = \pm 40V$ and $T_A = +25°C$ unless otherwise specified.

		OPA445SM			OPA445BM			ADVANCE INFORMATION OPA445AP			
PARAMETER		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT											
OFFSET VOLTAGE											
Input Offset Voltage	$V_{CM} = 0V$		0.5	1.0		1.0	3.0		2.0	5.0	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		*			10			15		µV/°C
Supply Rejection	$V_S = \pm 10V$ to $\pm 50V$	*	*		80	110		*	*		dB
BIAS CURRENT											
Input Bias Current	$V_{CM} = 0V$		*	*		20	50		50	100	pA
Over Temperature				100			10			20	nA
OFFSET CURRENT											
Input Offset Current	$V_{CM} = 0V$		*	*		4	10		20	40	pA
Over Temperature				50			5			10	nA
IMPEDANCE											
Differential			*			$10^{13} \parallel 1$			*		Ω || pF
Common-Mode			*			$10^{14} \parallel 3$			*		Ω || pF
VOLTAGE RANGE											
Common-Mode Input Range		*			±35			*			V
Common-Mode Rejection	$V_{IN} = \pm 30V$,										
	Over temp.	*	*		80	95		*	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L = 5k\Omega$	*	*		100	105		*	*		dB
Over Temperature		*			97			*			dB
FREQUENCY RESPONSE											
Gain Bandwidth	Small signal		*			2			*		MHz
Full Power Response	35Vp-p, $R_L = 5k\Omega$	*	*		45	55		*	*		kHz
DYNAMIC RESPONSE											
Slew Rate	$V_O = \pm 35V$,										
	$R_L = 5k\Omega$	*	*		5	10		*	*		V/µs
Rise Time	$V_O = \pm 200mV$		*			60			*		ns
Overshoot	$A_V = +1$										
	$Z_L = 5k\Omega \parallel 50pF$		*			30			*		%
RATED OUTPUT											
Voltage Output, over temp.	$R_L = 5k\Omega$	*			±35			*			V
Current Output	$V_O = \pm 28V$	*			±15			*			mA
Output Resistance	DC, open loop		*			220			*		Ω
Short Circuit Current			*			±26			*		mA
POWER SUPPLY											
Rated Voltage, $\pm V_S$			*			±40			*		V
Voltage Range, $\pm V_S$											
Derated Performance	Over temp.	*		*	±10		±50	*		*	V
Current, Quiescent	$I_O = 0mA$		*	*		3.8	4.5		*	*	mA
TEMPERATURE RANGE											
Specification		−55		+125	−25		+85	*		*	°C
Operating	Ambient temp.	*		*	−55		+125	−25		+85	°C
θ Junction-Ambient			*			200			90		°C/W

*Specification same as OPA445BM.

ORDERING INFORMATION

OPA445 ( ) ( )

Basic model number

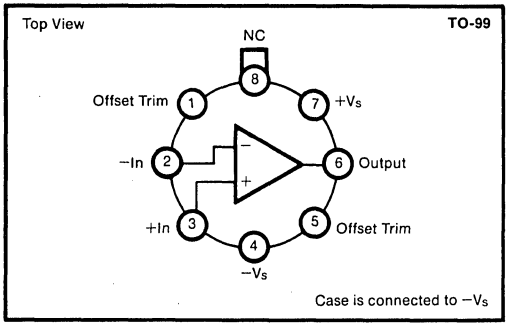
Performance grade (blank indicates A grade)
- A: −25°C to +85°C
- B: −25°C to +85°C
- S: −55°C to +125°C

Package code
- M: 8-pin TO-99
- P: 8-pin plastic DIP

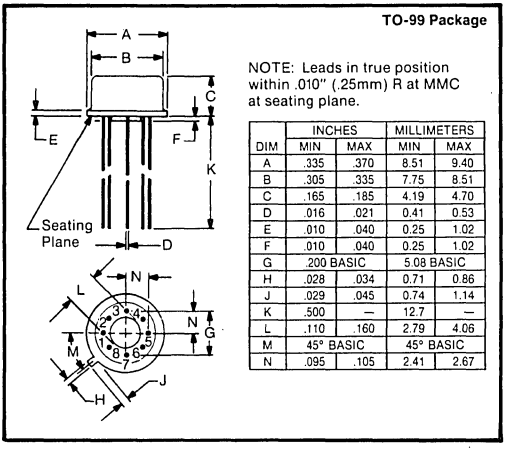
ABSOLUTE MAXIMUM RATINGS

Power Supply	±55V
Internal Power Dissipation	680mW
Differential Input Voltage	±80V
Input Voltage Range	$\|\pm V_S\| - 3V$
Storage Temperature Range: M	−65°C to +150°C
P	−40°C to +85°C
Operating Temperature Range: M	−55°C to +125°C
P	−40°C to +85°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit to Ground ($T_A = +25°C$)	Continuous
Junction Temperature	+175°C

CONNECTION DIAGRAM



MECHANICAL

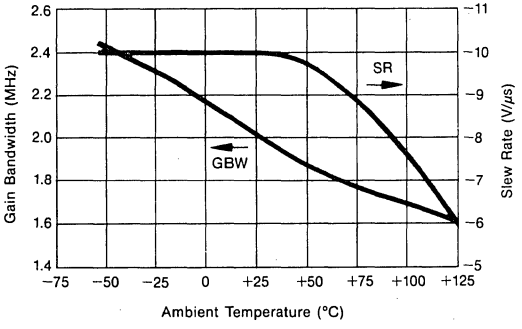


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

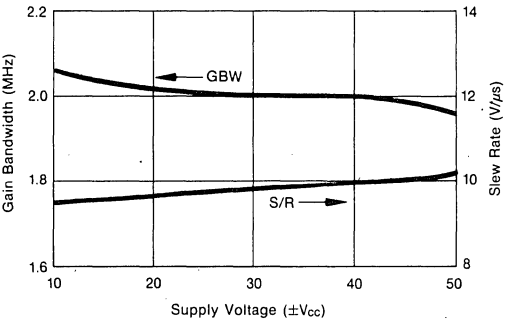
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

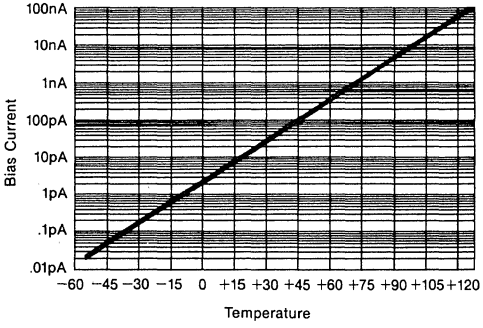
GAIN BANDWIDTH AND SLEW RATE VS TEMPERATURE



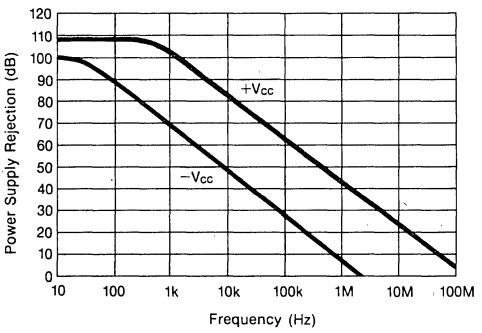
GAIN BANDWIDTH AND SLEW RATE VS SUPPLY VOLTAGE



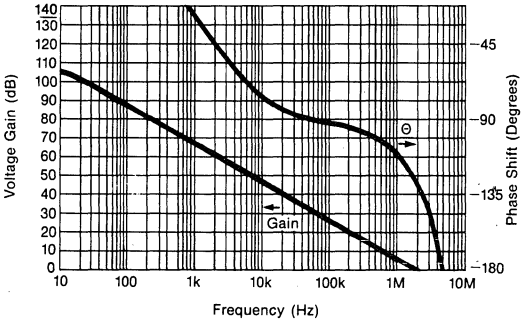
INPUT BIAS CURRENT VS TEMPERATURE



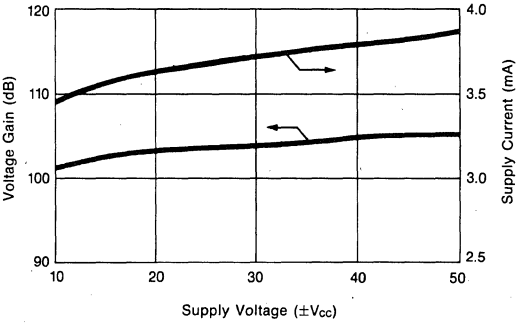
POWER SUPPLY REJECTION VS FREQUENCY



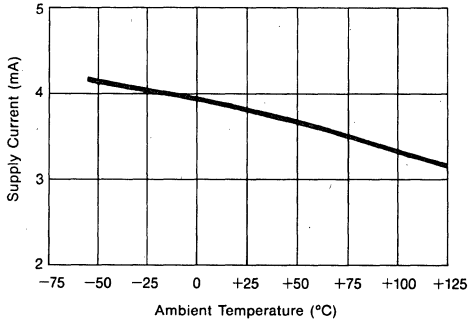
OPEN-LOOP
FREQUENCY RESPONSE



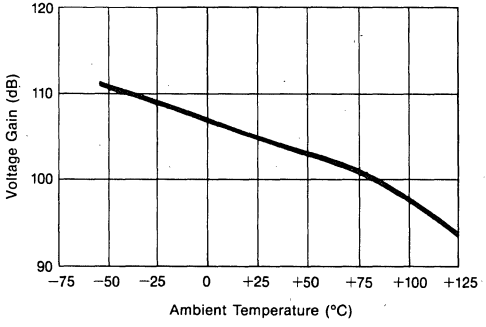
OPEN-LOOP GAIN AND SUPPLY CURRENT
VS SUPPLY VOLTAGE



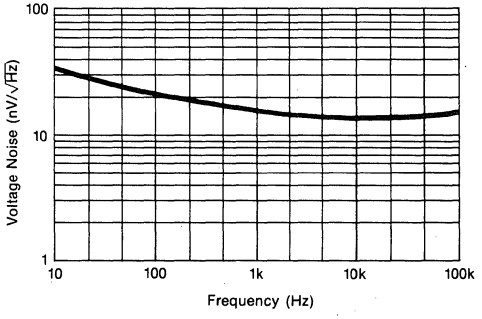
SUPPLY CURRENT VS TEMPERATURE



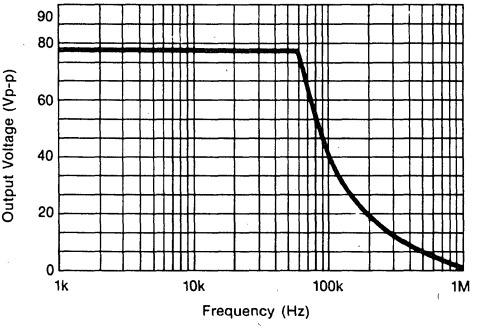
OPEN-LOOP GAIN VS TEMPERATURE



INPUT VOLTAGE NOISE SPECTRAL DENSITY



MAXIMUM OUTPUT VOLTAGE SWING
VS FREQUENCY



BURR-BROWN®

OPA541

ADVANCE INFORMATION
Subject to Change

High Power Monolithic OPERATIONAL AMPLIFIER

FEATURES

- POWER SUPPLIES TO ±40V
- OUTPUT CURRENT TO 10A PEAK
- PROGRAMMABLE CURRENT LIMIT
- INDUSTRY-STANDARD PINOUT
- FET INPUT

APPLICATIONS

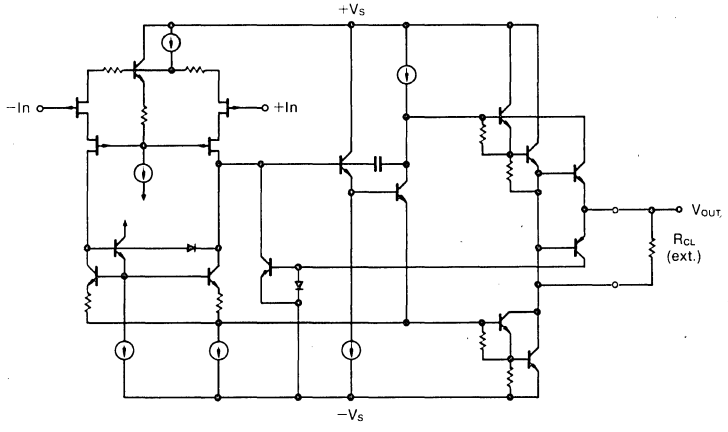
- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCHRO EXCITATION
- AUDIO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY

DESCRIPTION

The OPA541 is a monolithic power amplifier capable of operation from power supplies up to ±40V and continuous output currents up to 5A. Internal current limit circuitry can be user-programmed with a single external resistor, protecting the amplifier and load from fault conditions. The OPA541 is fabricated using a proprietary bipolar/FET process.

Pinout is compatible with popular hybrid power amplifiers such as the OPA511, OPA512 and the 3573. The OPA541 uses a single current-limit resistor to set both the positive and negative current limits. Applications currently using hybrid power amplifiers requiring two current-limit resistors need not be modified.

The OPA541 is available in an industry-standard 8-pin TO-3 hermetic package. The case is isolated from all circuitry, thus allowing it to be mounted directly to a heat sink without special insulators which degrade thermal performance.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

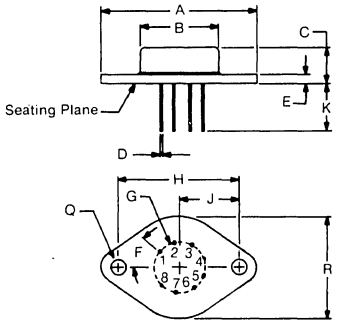
ELECTRICAL

At T_C = +25°C and V_S = ±35VDC unless otherwise noted.

PARAMETER	CONDITIONS	OPA541AM			OPA541BM/SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT OFFSET VOLTAGE								
V_{OS}			±2	±10		±0.1	±1	mV
vs Temperature	Specified temperature range		±20	±40		±15	±30	µV/°C
vs Supply Voltage	V_S = ±10V to ±V_{MAX}		±2.5	±10		*	*	µV/V
vs Power			±20	±60		*	*	µV/W
INPUT BIAS CURRENT								
I_B			4	50		*	*	pA
vs Supply Voltage			±10			*	*	pA/V
INPUT OFFSET CURRENT								
I_{OS}			±1	±30		*	*	pA
	Specified temperature range			5			*	nA
INPUT CHARACTERISTICS								
Common-Mode Voltage Range	Specified temperature range	±(|V_S|−6)	±(|V_S|−3)		*	*		V
Common-Mode Rejection	V_{CM} = (|±V_S|−6V)	95	113		*	*		dB
Input Capacitance			5			*		pF
Input Impedance, DC			1			*		TΩ
GAIN CHARACTERISTICS								
Open Loop Gain at 10Hz	R_L = 6Ω	90	97		*	*		dB
Gain-Bandwidth Product			1.6			*		MHz
OUTPUT								
Voltage Swing	I_O = 5A, Continuous	±(|V_S|−5.5)	±(|V_S|−4.5)		*	*		V
	I_O = 2A	±(|V_S|−4)	±(|V_S|−3.6)		*	*		V
	I_O = 0.5A	±(|V_S|−4)	±(|V_S|−3.2)		*	*		V
Current, Peak		9	10		*	*		A
AC PERFORMANCE								
Slew Rate		8	10		*	*		V/µs
Power Bandwidth	R_L = 8Ω, V_O = 20Vrms	45	55		*	*		kHz
Settling Time to 0.1%	2V Step		2				*	µs
Capacitive Load	Specified temperature range, G = 1	3.3					*	nF
	Specified temperature range, G > 10			SOA			*	
Phase Margin	Specified temperature range, R_L = 8Ω		40			*		Degrees
POWER SUPPLY								
Power Supply Voltage, ±V_S	Specified temperature range	±10	±30	±35	*	±35	±40	V
Current, Quiescent			20	25		*	*	mA
THERMAL RESISTANCE								
θ_{JC}, (junction to case)	AC output f > 60Hz		1.25	1.5		*	*	°C/W
θ_{JC}	DC output		1.4	1.9		*	*	°C/W
θ_{JA}, (junction to ambient)	No heat sink		30			*		°C/W
TEMPERATURE RANGE								
T_{CASE}	AM, BM	−25		+85	*		*	°C
	SM				−55		+125	°C

*Specification same as OPA541AM

MECHANICAL



NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

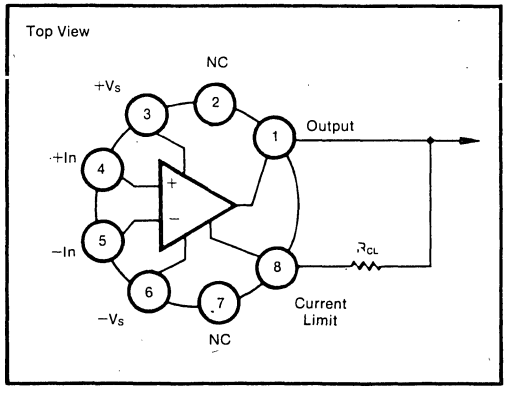
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.240	.290	6.10	7.37
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 90V
Output Current ..... see SOA
Power Dissipation, Internal[1] 125W
Input Voltage: Differential ..... $\pm V_S$
Common-mode ..... $\pm V_S$
Temperature: Pin solder, 10s ..... +300°C
Junction[1] ..... +150°C
Temperature Range:
Storage ..... −65°C to +150°C
Operating (case) ..... −55°C to +125°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

CONNECTION DIAGRAM



ORDERING INFORMATION

OPA541 ( ) M

Basic Model Number

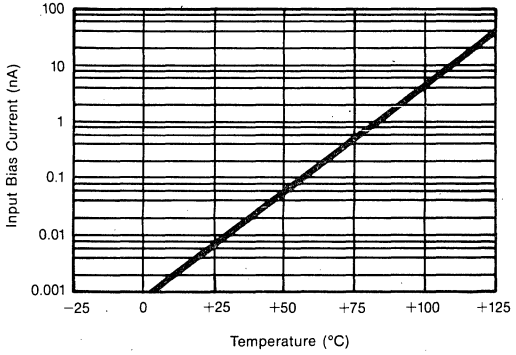
Performance Grade Code
A: −25°C to +85°C
B: −25°C to +85°C
S: −55°C to +125°C

Package Code
M = TO-3

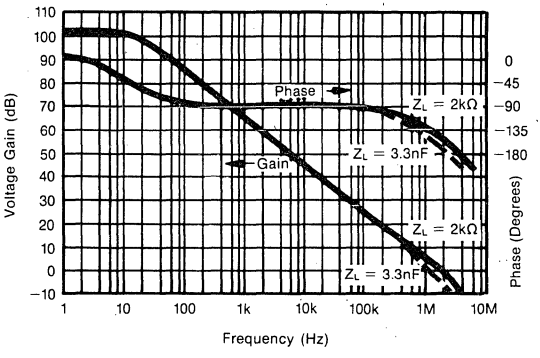
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±35VDC unless otherwise noted.

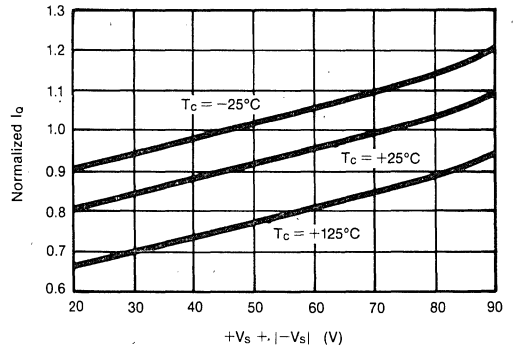
INPUT BIAS CURRENT
VS TEMPERATURE



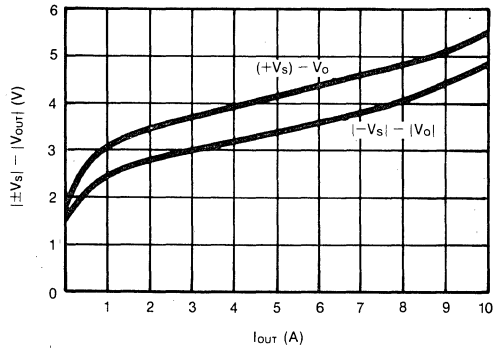
OPEN-LOOP GAIN AND
PHASE VS FREQUENCY



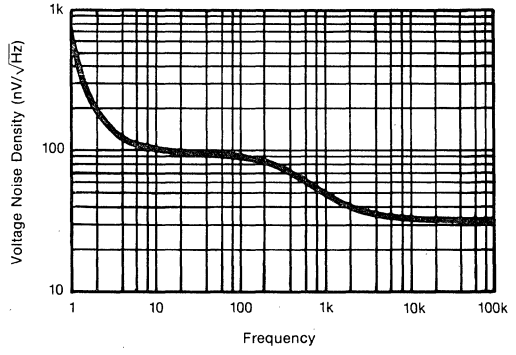
NORMALIZED QUIESCENT CURRENT VS
TOTAL POWER SUPPLY VOLTAGE



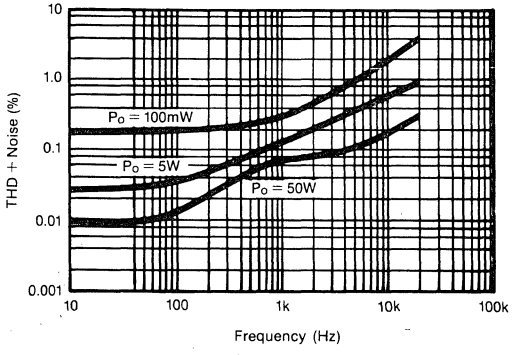
OUTPUT VOLTAGE SWING
VS OUTPUT CURRENT



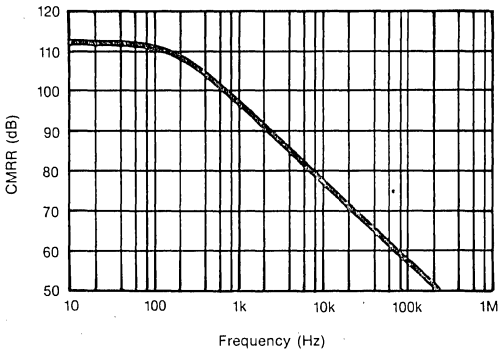
VOLTAGE NOISE DENSITY
VS FREQUENCY



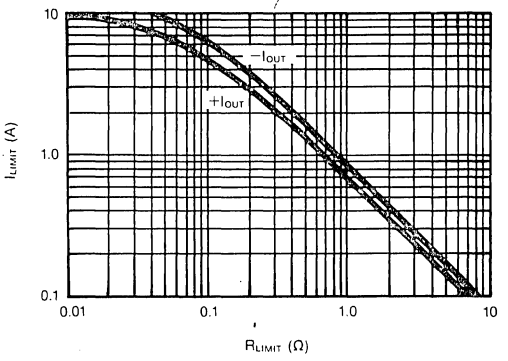
TOTAL HARMONIC DISTORTION
VS FREQUENCY



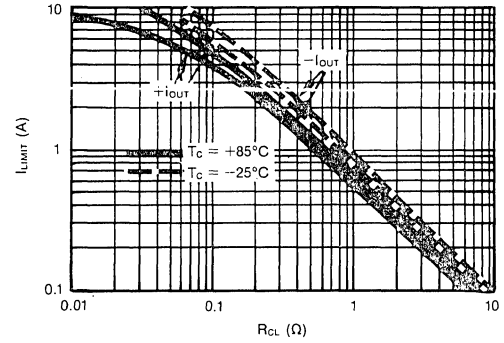
COMMON-MODE REJECTION VS FREQUENCY



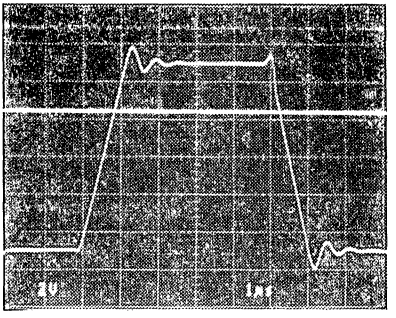
CURRENT LIMIT VS RESISTANCE LIMIT



CURRENT LIMIT VS RESISTANCE LIMIT VS TEMPERATURE



DYNAMIC RESPONSE



G = 1, C_L = 4.7nF

INSTALLATION INSTRUCTIONS

POWER SUPPLIES

The OPA541 is specified for operation from power supplies up to ±40V. It can also be operated from unbalanced or single power supply as long as the total power supply voltage does not exceed 80V. The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier's power supply pins. Good power amplifier circuit layout is, in general, like good high frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and oscillations.

CURRENT LIMIT

Internal current limit circuitry is controlled by a single external resistor, R_{CL}. Output load current flows through this external resistor. The current limit is activated when the voltage across this resistor is approximately a base-emitter turn-on voltage. The value of the current limit resistor is approximately:

$$R_{CL} = \frac{0.809}{|I_{LIM}|} - 0.057$$

The current limit value decreases with increasing temperature due to the temperature coefficient of a base-emitter junction voltage. Similarly, the current limit value increases at low temperatures. Current limit versus resistor value and temperature effects are shown in the Typical Performance Curves.

The adjustable current limit can be set to provide protection from short circuits. The safe short-circuit current depends on power supply voltage. See the discussion on Safe Operating Area to determine the proper current limit value.

Since the full load current flows through R_{CL}, it must be selected for sufficient power dissipation. For a 5A current limit, the dissipation of R_{CL} will be 3.25W for 5A continuous currents. Sinusoidal output will create dissipation according to the rms load current. Thus for the same 5A current limit, AC peaks would be limited to 5A, but the rms current would be 3.5A and a resistor with a lower power rating could be used. Some applications

(such as voice amplification) are assured of signals with much lower duty cycles, allowing a current resistor with a lower power rating. Wire-wound resistors may be used for R_{CL}. Some wire-wound resistors, however, have excessive inductance and may cause loop-stability problems. Be sure to evaluate circuit performance with resistor type planned for production to assure proper circuit operation.

HEAT SINKING

Power amplifiers are rated by case temperature, not ambient temperature as with signal op amps. The maximum allowable power dissipation is a function of the case temperature as shown on the power derating curve. All points on the power derating slope produce a maximum internal junction temperature of +150°C. Sufficient heat sinking must be provided to keep the case temperature within safe bounds for the maximum ambient temperature and power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{HS} = \frac{T_{CASE} - T_{AMBIENT}}{P_D \text{ (max)}}$$

Commercially available heat sinks often specify their thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the TO-3 package. Since mica and other similar insulators typically add approximately 0.7°C/W thermal resistance, their elimination significantly improves thermal performance. See Burr-Brown Application Note AN-83 for further details on heat sinking.

SAFE OPERATING AREA

The safe operating area (SOA) plot provides comprehensive information on the power handling abilities of the OPA541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

Short circuit protection requires evaluation of SOA. When the amplifier output is shorted to ground, the full power supply voltage is impressed across the conducting output transistor. The current limit must be set to a value which is safe for the power supply voltage used. For instance, with V_S ±35V, a short to ground would force 35V across the conducting power transistor. A current limit of 1.8A would be safe.

Reactive, or EMF-generating, loads such as DC motors can present difficult SOA requirements. With a purely reactive load, output voltage and load current are 90° out of phase. Thus, peak output current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Note AN-123 for further information on evaluating SOA.

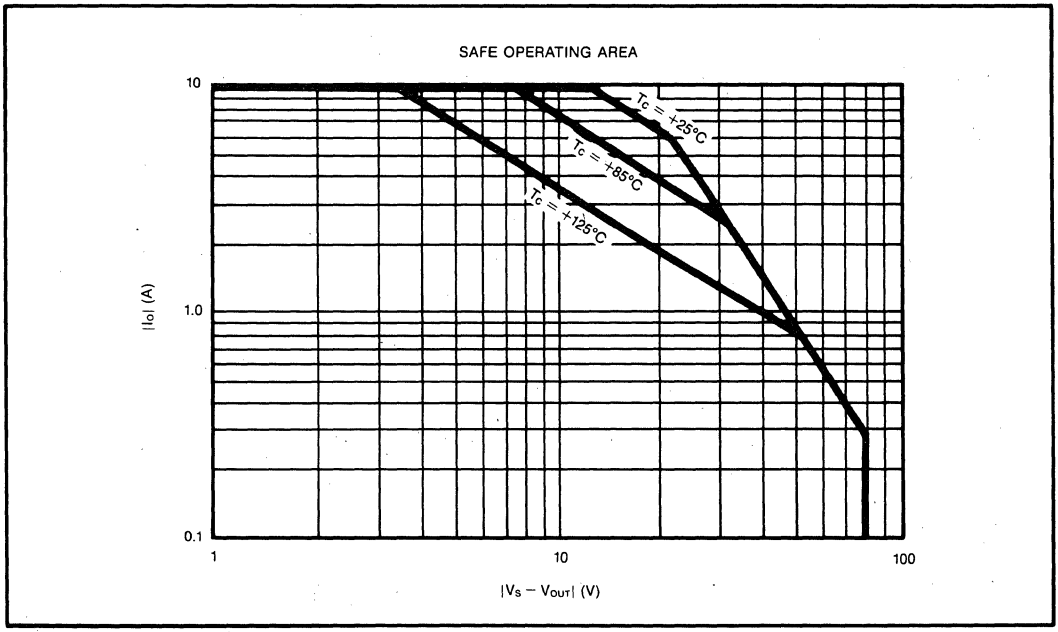


FIGURE 1. Safe Operating Area.

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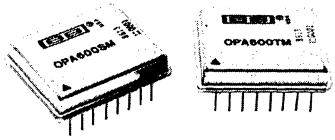


OPA600

Fast-Settling Wideband OPERATIONAL AMPLIFIER

FEATURES

- GAIN BANDWIDTH PRODUCT: 5GHz
- FAST SETTLING: 80ns to ±0.1%
  100ns to ±0.01%
- −25°C to +85°C AND
  −55°C to +125°C TEMPERATURE RANGES
- ±10V OUTPUT: 200mA

APPLICATIONS

- FAST VCO
- HIGH-SPEED D/A CONVERTER OUTPUT AMPLIFIER
- VIDEO AMPLIFIER
- HIGH-SPEED ADC DRIVER
- LOW-DISTORTION AMPLIFIER
- TRANSMISSION LINE BUFFER

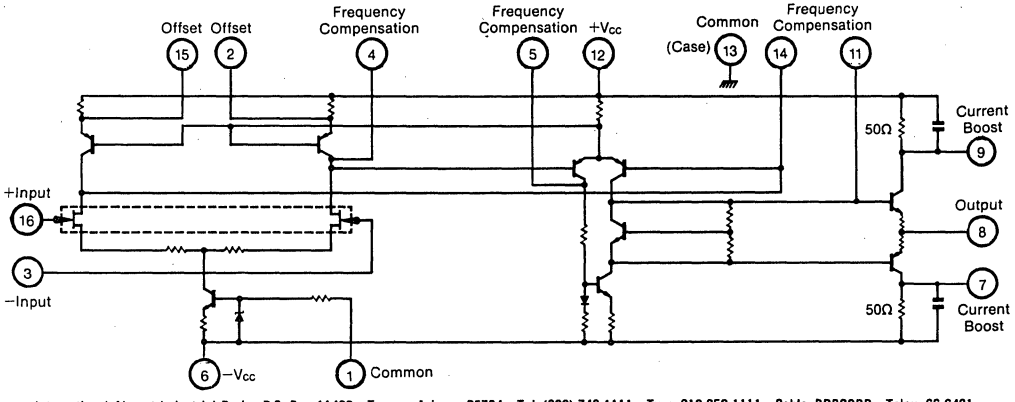
DESCRIPTION

The OPA600 is a wideband operational amplifier specifically designed for fast settling to ±0.01% accuracy. It is stable, easy to use, has good phase margin with minimum overshoot, and it has excellent DC performance. It utilizes an FET input stage to give low input bias current. Its DC stability over temperature is outstanding. The slew rate exceeds 400V/μs. All of this combines to form an outstanding amplifier for large and small signals.

High accuracy with fast settling time is achieved by using a high open-loop gain which provides the accuracy at high frequencies. The thermally balanced design maintains this accuracy without droop or thermal tail. External frequency compensation allows the user to optimize the settling time for various gains and load conditions.

The OPA600 is useful in a broad range of video, high speed test circuits and ECM applications. It is particularly well suited to operate as a voltage controlled oscillator (VCO) driver. It makes an excellent digital-to-analog converter output amplifier. It is a workhorse in test equipment where fast pulses, large signals, and 50Ω drive are important. It is a good choice for sample/holds, integrators, fast waveform generators, and multiplexers.

The OPA600 is specified over the industrial temperature range (OPA600BM, CM) and military temperature range (OPA600SM, TM). The OPA600 is housed in a welded, hermetic metal package.



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SPECIFICATIONS

ELECTRICAL

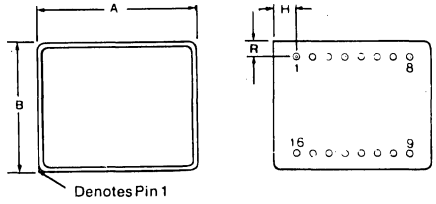
At V_{CC} = ±15VDC and T_A = +25°C unless otherwise specified.

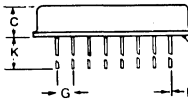
PARAMETER	CONDITIONS	OPA600CM, TM[1] MIN	OPA600CM, TM[1] TYP	OPA600CM, TM[1] MAX	OPA600BM, SM MIN	OPA600BM, SM TYP	OPA600BM, SM MAX	UNITS
OUTPUT								
Voltage	R_L = 2kΩ	±10			*			V
	R_L = 50Ω[2]	±9			*			V
Current	R_L = 50Ω[2]	±180	±200		*	*		mA
Current Pulse	R_L = 50Ω[3]	±180	±200		*	*		mA
Resistance	Open loop DC		75			*		Ω
Short-Circuit Current	To COMMON only, t_{MAX} = 1s[4]		250	300		*	*	mA
DYNAMIC RESPONSE								
Settling Time[5]: to ±0.01% (±1mV)	ΔV_{OUT} = 10V		100	125		*	*	ns
to ±0.1% (±10mV)	ΔV_{OUT} = 10V		80	105		*	*	ns
to ±1% (±100mV)	ΔV_{OUT} = 10V		70	95		*	*	ns
Gain-Bandwidth Product (open-loop)	C_C = 0pF, G = 1V/V		150			*		MHz
	C_C = 0pF, G = 10V/V		500			*		MHz
	C_C = 0pF, G = 100V/V		1.5			*		GHz
	C_C = 0pF, G = 1000V/V		5			*		GHz
	C_C = 0pF, G = 10,000V/V		10			*		GHz
Bandwidth (−3dB small signal)[6]	G = +1V/V		125			*		MHz
	G = −1V/V		90			*		MHz
	G = −10V/V		95			*		MHz
	G = −100V/V		20			*		MHz
	G = −1000V/V		6			*		MHz
Full Power Bandwidth	V_{OUT} = ±5V, G = −1V/V, C_C = 3.3pF, R_L = 100Ω		16			*		MHz
Slew Rate	V_{OUT} = ±5V, G = −1000V/V, C_C = 0pF, R_L = 100Ω		500			*		V/μs
	V_{OUT} = ±5V, G = −1V/V[4]	400	440		*	*		V/μs
Phase Margin	G = −1V/V, C_C = 3.3pF		40			*		Degrees
GAIN								
Open-Loop Voltage Gain	f = DC, R_L = 2kΩ, T_A = +25°C	86	94		*	*		dB
INPUT								
Offset Voltage[7]	T_A = +25°C		±1	±4		±2	±5	mV
	T_A = −25°C to +85°C			±5			±10	mV
	T_A = −55°C to +125°C			±6			±15	mV
Offset Voltage Drift	T_A = −25°C to +85°C			±20			±80	μV/°C
	T_A = −55°C to +125°C			±20			±100	μV/°C
Bias Current	T_A = +25°C		−20	−100		*	*	pA
	T_A = −25°C to +125°C		−20	−100		*	*	nA
Offset Current	T_A = +25°C		20			*		pA
	T_A = −55°C to +125°C		20			*		nA
Power Supply Rejection Ratio	V_{CC} = ±15V, ±1V		200	500		*	*	μV/V
Common-Mode Voltage Range		−10		+7	*		*	V
Common-Mode Rejection Ratio	V_{CM} = −5V to +5V	60	80		*	*		dB
Impedance	Differential and Common-Mode		10^{11}‖2			*		Ω‖pF
Voltage Noise	10kHz Bandwidth		20			*		nV/√Hz
POWER SUPPLY								
Rated (V_{CC})			±15			*		VDC
Operating Range		±9		±16	*		*	VDC
Quiescent Current			±30	±38		*	*	mA
TEMPERATURE RANGE (Ambient)[8]								
Operating: BM, CM		−25		+85	*		*	°C
SM, TM		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C
θ_{JC}, (junction to case)			30			*		°C/W
θ_{CA}, (case to ambient			35			*		°C/W

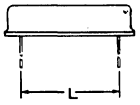
*Specification same as OPA600CM, TM.

NOTES: (1) BM, CM grades: −25°C to +85°C. SM, TM grades: −55°C to +125°C. (2) Pin 9 connected to $+V_{CC}$, pin 7 connected to $-V_{CC}$. Observe power dissipation ratings. (3) Pin 9 and pin 7 open. Single pulse t = 100ns. Observe power dissipation ratings. (4) Pin 9 and pin 7 open. See section on Current Boost. (5) G = −1V/V. Optimum settling time and slew rate achieved by individually compensating each device. Refer to section on Compensation. (6) Frequency compensation as discussed in section on Compensation. (7) Adjustable to zero. (8) Heat Sink (optional): IERC LBOCI-72CB with 2 each DCV-1B Clamps.

MECHANICAL



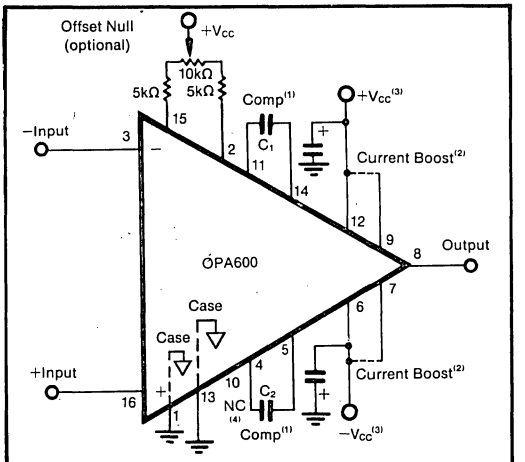




DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.963	.980	24.46	24.89
B	.760	.805	19.30	20.45
C	.175	.190	4.45	4.83
D	.014	.022	0.36	0.56
G	.100 BASIC		2.54 BASIC	
H	.135	.155	3.43	3.94
K	.230	.270	5.84	6.86
L	.600 BASIC		15.24 BASIC	
R	.095	.115	2.41	2.92

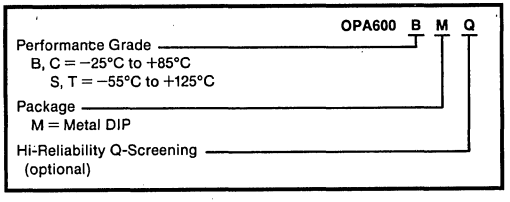
NOTES:
1. Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
2. Pin numbers shown for reference only.

CONNECTION DIAGRAM



NOTES: (1) Refer to Figure 4 for recommended frequency compensation. (2) Connect pin 9 to pin 12 and connect pin 7 to pin 6 for maximum output current. See Application Information for further information. (3) Bypass each power supply lead as close as possible to the amplifier pins. A 1μF CS13 tantalum capacitor is recommended. (4) There is no internal connection. An external connection may be made. (5) It is recommended that the amplifier be mounted with the case in contact with a ground plane for good thermal transfer and optimum AC performance.

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS(1)

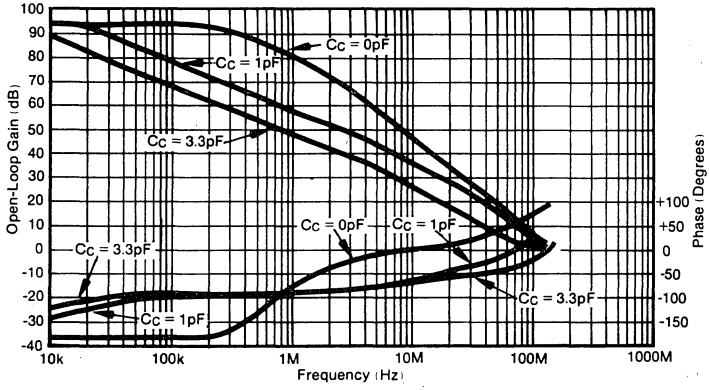
Supply Voltage, +Vcc to −Vcc	±17V
Power Dissipation, At TCASE +125°C(2)	1.6W
Input Voltage: Differential	±Vcc
Common-Mode	±Vcc
Output Short Circuit Duration to Common	<5sec
Temperature: Pin (soldering, 20sec)	+300°C
Junction(1), TJ	+175°C
Temperature Range: Storage	−65°C to +150°C
Operating (case)	−55°C to +125°C

NOTES: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability. (2) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

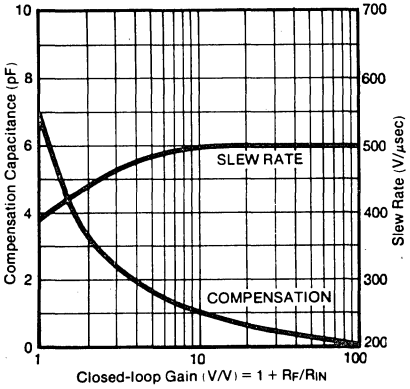
TYPICAL PERFORMANCE CURVES

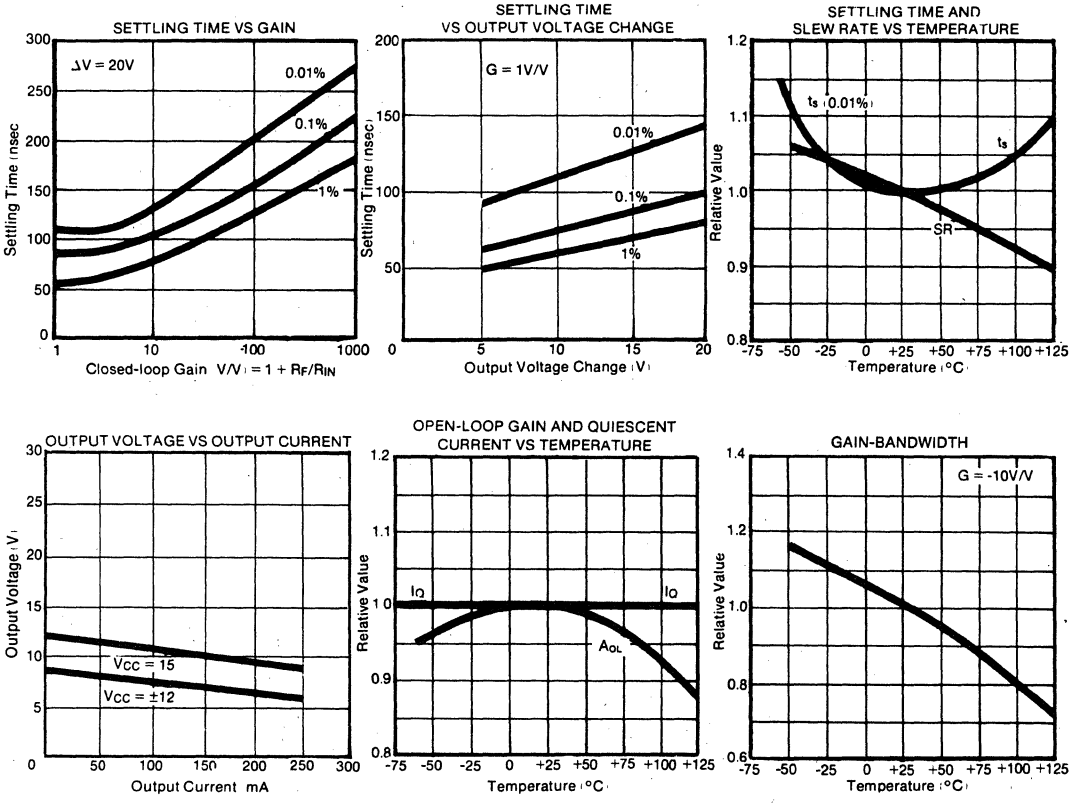
(Typical at T_A = +25°C and ±V_{CC} = 15VDC, unless otherwise specified.)

BODE PLOT



COMPENSATION AND SLEW RATE VS GAIN





INSTALLATION AND OPERATION

WIRING PRECAUTIONS

The OPA600 is a wideband, high frequency operational amplifier with a gain-bandwidth product exceeding 5GHz. This capability can be realized by observing a few wiring precautions and using high frequency layout techniques. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths and should be as short as possible. The entire physical circuit should be as small as is practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the input terminals of the amplifier and compensation pins. Stray signal coupling from the output to the input should be minimized. All circuit element leads should be as short as possible and low values of resistance should be used. This will give the best circuit performance as it will minimize the time constants formed with the circuit capacitances and will eliminate stray, unwanted tuned circuits.

Grounding is the most important application consideration for the OPA600, as it is with all high frequency circuits. Ultra-high frequency transistors are used in the design of the OPA600 and oscillations at frequencies of 500MHz and above can be stimulated if good grounding techniques are not used. A ground plane is highly recommended. It should connect all areas of the pattern side of the printed circuit that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pickup.

Point-to-point wiring is not recommended. However, if point-to-point wiring is used, a single-point ground should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This eliminates common current paths or ground loops which can cause unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A 1μF CS13 tantalum capacitor is recommended. A parallel 0.01μF ceramic may be added if desired. This is especially important when driving high current loads. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

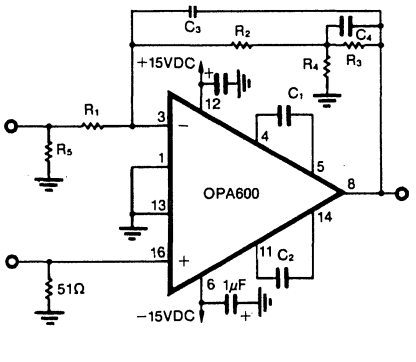
OPA600 circuit common is connected to pins 1 and 13; these pins should be connected to the ground plane. The input signal return, load return, and power supply commmon should also be connected to the ground plane.

The case of the OPA600 is internally connected to circuit common, and as indicated above, pins 1 and 13 should be connected to the ground plane. Ideally, the case should be mechanically connected to the ground plane for good thermal transfer, but because this is difficult in practice, the OPA600 should be fully inserted into the printed circuit board with the case very close to the ground plane to make the best possible thermal connection. If the case and ground plane are physically connected or are in close thermal proximity, the ground plane will provide heat sinking which will reduce the case temperature rise. The minimum OPA600 pin length will minimize lead inductance, thereby maximizing performance.

COMPENSATION

The OPA600 uses external frequency compensation so that the user may optimize the bandwidth or settling time for his particular application. Several performance curves aid in the selection of the correct compensations capacitance value. The Bode plot shows amplitude and phase versus frequency for several values of compensation. A related curve shows the recommended compensation capacitance versus closed-loop gain.

Figure 1 shows a recommended circuit schematic. Component values and compensation for amplifiers with several different closed-loop gains are shown. This circuit will yield the specified settling time. Because each device is unique and slightly different, as is each user's circuit, optimum settling time will be achieved by individually compensating each device in its own circuit, if desired. A 10% to 20% improvement in settling time has been experienced from the values indicated in the Electrical Specifications table.



Closed Loop Gain	R_1	R_2	R_3	R_4	C_1, C_2	C_3	C_4	R_5
+1	open	100	short	open	6.8	0	0	--
−1	620	620	short	open	3.3	4.7	0	56
−10	100	1k	short	open	1	2.2	0	100
−100	100	3.3k	3.3k	3.2k	0	1	0	100
−1000	100	3.3k	3.3k	116	0	0	4.7	100

FIGURE 1. Recommended Amplifier Circuits and Frequency Compensation.

The primary compensation capacitors are C_1 and C_2 (see Figure 1). They are connected between pins 4 and 5 and between pins 11 and 14. Both C_1 and C_2 should be the same value. As Figure 1 and the performance curves show, larger closed-loop configurations require less capacitance and improved gain-bandwidth product can be realized. Note that no compensation capacitor is required for closed-loop gains equal to or above 100V/V. If upon initial application the user's circuit is unstable, and remains so after checking for proper bypassing, grounding, etc., it may be necessary to increase the compensation slightly to eliminate oscillations. Do not over compensate. It should not be necesary to increase C_1 and C_2 beyond 10pF to 15pF. It may also be necessary to individually optimize C_1 and C_2 for improved performance.

The flat high frequency response of the OPA600 is preserved and high frequency peaking is minimized by connecting a small capacitor in parallel with the feedback resistor (see Figure 1). This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1kΩ) and up to 10pF for circuits using larger resitances. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator is recommended to avoid using a large value resistor with its long time constant.

CAPACITIVE LOADS

The OPA600 will drive large capacitive loads (up to 100pF) when properly compensated and settling times of under 150ns are achievable. The effect of a capacitive load is to decrease the phase margin of the amplifier, which may cause high frequency peaking or oscillations. A solution is to increase the compensation capacitance, somewhat slowing the amplifier's ability to respond. The recommended compensation capacitance value as a function of load capacitance is shown in Figure 2. (Use two capcitors, each with the value indicated.) Alternately, without increasing the OPA600's compensation capacitance, the capacitive load may be buffered by connecting a small resistance, usually 5Ω to 50Ω, in series with the Output, pin 8.

For very-large capacitive loads, greater than 100pF, it will be necessary to use doublet compensation. Refer to Figure 3 and discussion on slew rate. This places the dominant pole at the input stage. Settling time will be approximately 50% slower; slew rate should increase. Load capacitance should be minimized for optimum high frequency performance.

Because of its large output capability, the OPA600 is particularly well suited for driving loads via coaxial

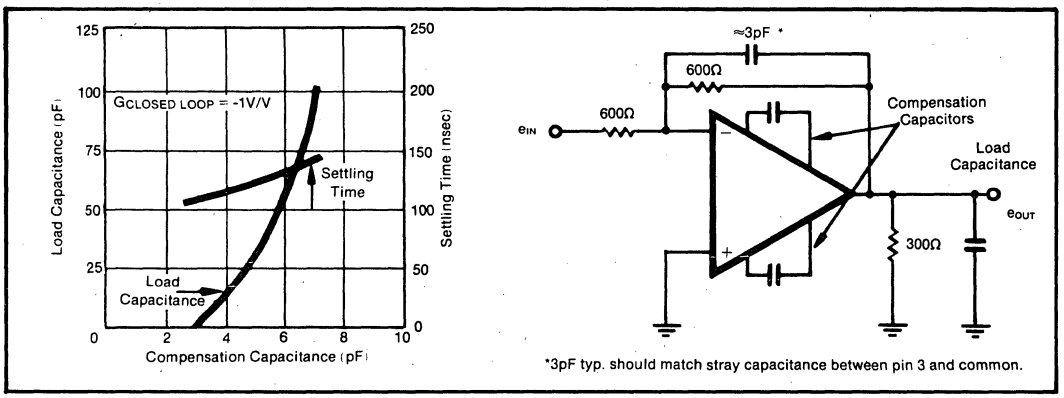


FIGURE 2. Capacitive Load Compensation and Response.

cables. Note that the capacitance of coaxial cable (29pF/foot of length for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition, a 10V step.

Settling time is a complete dynamic measure of the OPA600's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open-loop gain. Performance curves show the OPA600 settling time to ±1%, ±0.1%, and ±0.01%. The best settling time is achieved in low closed-loop gain circuits.

Settling time is dependent upon compensation. Undercompensation will result in small phase margin, overshoot or instability. Over-compensation will result in poor settling time.

Figure 1 shows the recommended compensation to yield the specified settling time. Improved or optimum settling time may be achieved by individually compensating each device in the user's circuit since individual devices vary slightly from one to another, as do user's circuits.

SLEW RATE

Slew rate is primarly an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or small signal bandwidth. Slew rate is dependent upon compensation and decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve.

The OPA600 slew rate may be increased by using an alternate compensation as shown in Figure 3. The slew rate will increase between 700 and 800V/μs typical, with 0.01% settling time increasing to between 175 and 190ns typical, and 0.1% settling time increasing to between 110 and 120ns typical.

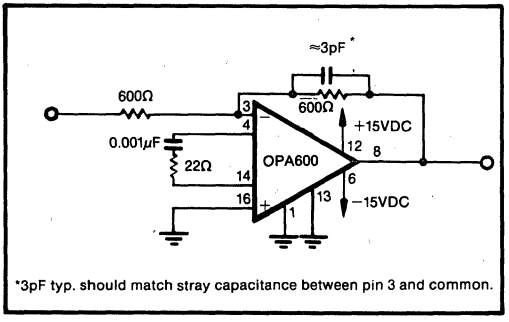


FIGURE 3. Amplifier Circuit for Increased Slew Rate.

For alternate doublet compensation refer to Figure 3. For a closed-loop gain equal to −1, delete C_1 and C_2 and add a series RC circuit (R = 22Ω, C = 0.01μF) between pins 14 and 4. Make no connections to pins 11 and 5. Absolutely minimze the capacitance to these pins. If a connector is used for the OPA600, it is recommended that sockets for pins 11 and 5 be removed. For a PC board mount, it is recommended that the PC board holes be overdrilled for pins 11 and 5 and adjacent ground plane copper be removed. Effectively this compensation places the dominant pole at the input stage, allowing the output stage to have no compensation and to slew as fast as possible. Bandwidth and settling time are impaired only slightly. For closed-loop gains other than −1, different values of R and C may be required.

OFFSET ADJUSTMENT

The offset voltage of the OPA600 may be adjusted to zero by connecting a 5kΩ resistor in series with a 10kΩ linear potentiometer in series with another 5kΩ resistor between pins 2 and 15, as shown in Figure 4. It is important that one end of each of the two resistors be located very close to pins 2 and 15 to isolate and avoid loading these sensitive terminals. The potentiometer should be a small noninductive type with the wiper connected to the positive supply. The leads connecting these components should be short, no longer than 0.5-inch, to avoid stray capacitance and stray signal pick-up. If the potentiometer must be located away from the immediate vicin-

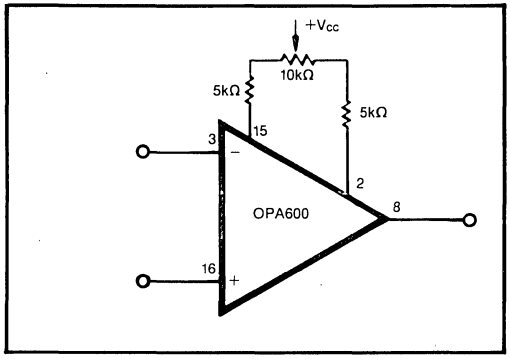


FIGURE 4. Offset Null Circuit.

ity of the OPA600, extreme care must be observed with the sensitive leads. Locate the two 5kΩ resistors very close to pins 2 and 15.

Never connect $+V_{CC}$ directly to pin 2 or 15. Do not attempt to eliminate the 5kΩ resistors because at extreme rotation, the potentiometer will directly connect $+V_{CC}$ to pin 2 or 15 and permanent damage will result.

Offset voltage adjustment is optional. The potentiometer and two resistors are omitted when the offset voltage is considered sufficiently low for the particular application. For each microvolt of offset voltage adjusted, the offset voltage temperature sensitivity will change by $\pm 0.004\mu V/°C$.

CURRENT BOOST

External ability to bypass the internal current limiting resistors has been provided in the OPA600. This is referred to as current boost. Current boost enables the OPA600 to deliver large currents into heavy loads (±200mA at ±10V). To bypass the resistors and activate the current boost, connect pin 7 to $-V_{CC}$ at pin 6 with a short lead to minimize lead inductance and connect pin 9 to $+V_{CC}$ at pin 12 with a short lead.

CAUTION—Activating current boost by bypassing the internal current limiting resistors can permanently damage the OPA600 under fault conditions. See section on short circuit protection.

Not activating current boost is especially useful for initial breadboarding. The 50Ω (±5%) current limiting resistor in the collector circuit of each of the output transistors causes the output transistors to saturate; this limits the power dissipation in the output stage in case of a fault. Operating with the current boost not activated may also be desirable with small-signal outputs (i.e., ±1V) or when the load current is small.

Each resistor is internally capacitively-bypassed (0.01μF, ±20%) to allow the amplifier to deliver large pulses of current, such as to charge diode junctions or circuit capacitance and still respond quickly. The length of time that the OPA600 can deliver these current pulses is limited by the RC time constant.

The internal voltage drops, output voltage available, power dissipation, and maximum output current can be determined for the user's application by knowing the load resistance and computing:

$$V_{OUT} = 14\,[R_{LOAD} \div (50 + R_{LOAD})]$$

This applies for R_{LOAD} less than 100Ω and the current boost not activated. When R_{LOAD} is large, the peak output voltage is typically ±11V, which is determined by other factors within the OPA600.

SHORT-CIRCUIT PROTECTION

The OPA600 is short-circuit-protected for momentary short to common (<5s), typical of those enountered when probing a circuit during experimental breadboarding or troubleshooting. This is true only if pins 7 and 9 are open (current boost not activated). An internal 50Ω resistor is in series with the collector of each of the output transistors, which under fault conditions will cause the output transistors to saturate and limit the power dissipation in the output stage. Extended application of an output short can damage the amplifier due to excessive power dissipation.

The OPA600 is not short-circuit-protected when the current boost is activated. The large output current capability of the OPA600 will cause excessive power dissipation and permanent damage will result even for momentary shorts to ground.

Output shorts to either supply will destroy the OPA600 whether the current boost is activated or not.

HEAT SINKING AND POWER DISSIPATION

The OPA600 is intended as a printed circuit board mounted device, and as such does not require a heat sink. It is specified for ambient temperature operation from −55°C to +125°C. However, the power dissipation must be kept within safe limits. At extreme temperature and under full load conditions, some form of heat sinking will be necessary. The use of a heat sink, or other heat dissipating means such as proximity to the ground plane, will result in cooler operating temperatures, better temperature performance, and improved reliability.

It may be necessary to physically connect the OPA600 to the printed circuit board ground plane, attach fins, tabs, etc., to dissipate the generated heat. Because of the wide variety of possibilities, this task is left to the user. For all applications it is recommended that the OPA600 be fully inserted into the printed circuit board and that the pin length be short. Heat will be dissipated through the ground plane and the AC performance will be its best.

With a maximum case temperature of +125°C and not exceeding the maximum junction of +175°C, a maximum power dissipation of 600mW is allowed in either output transistor.

TESTING

For static and low frequency dynamic measurements, the OPA600 may be tested in conventional operational amplifier test circuits, provided proper ground techniques are observed, excessive lead lengths are avoided, and care is maintained to avoid parasitic oscillations. The circuit in Figure 3 is recommended for low frequency functional testing, incoming inspection, etc. This circuit is less susceptible to stray capacitance, excessive lead length, parasitic tuned circuits, changing capacitive loads, etc. It does not yield optimum settling time. We recommend placing a resistor (approximately 300Ω) in series with each piece of test equipment, such as a DVM, to isolate loading effects on the OPA600.

To realize the full performance capabilities of the OPA600, high frequency techniques must be employed and the test fixture must not limit the amplifier. Settling time is the most critical dynamic test and Figure 5 shows a recommended OPA600 settling time test circuit schematic. Good grounding, truly square drive signals, minimum stray coupling, and small physical size are important.

The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. A circuit that generates a ±5V flat topped pulse is shown in Figure 6.

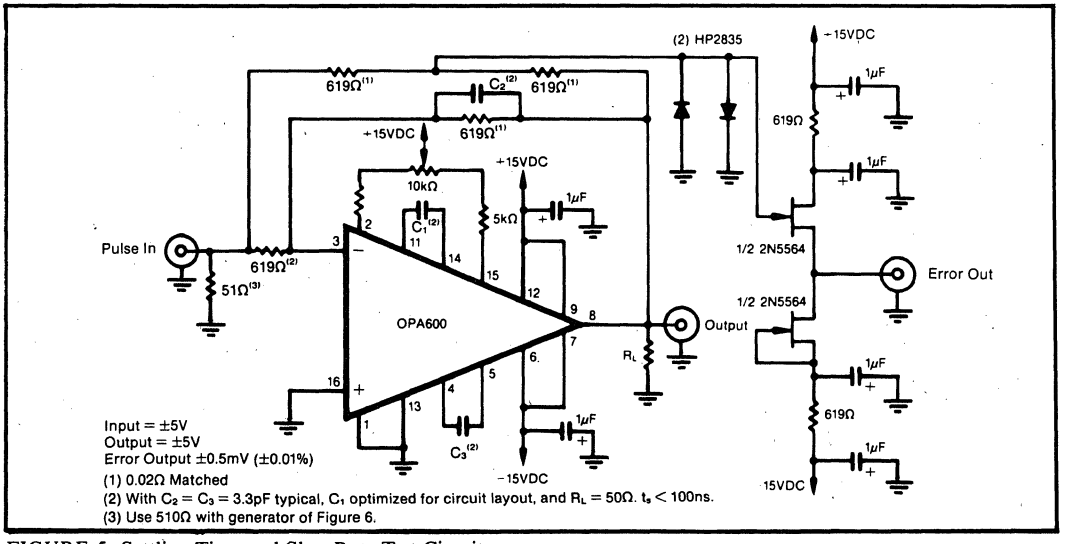


FIGURE 5. Settling Time and Slew Rate Test Circuit.

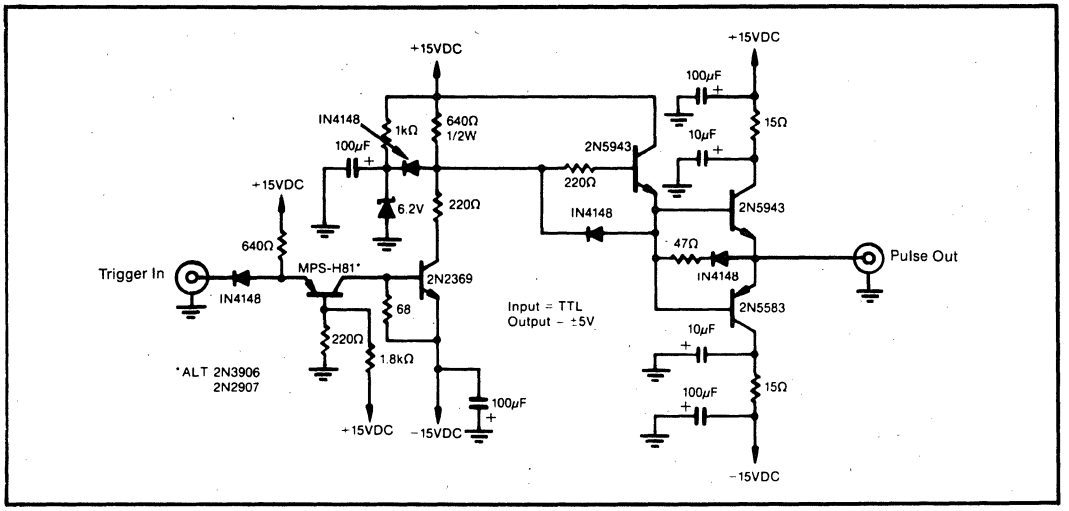


FIGURE 6. Flat Top Pulse Generator.

BURR-BROWN®

OPA602

ADVANCE INFORMATION
Subject to Change

High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 0.4MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±250μV max
- LOW BIAS CURRENT: ±1pA max
- FAST SETTLING: 1μs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION

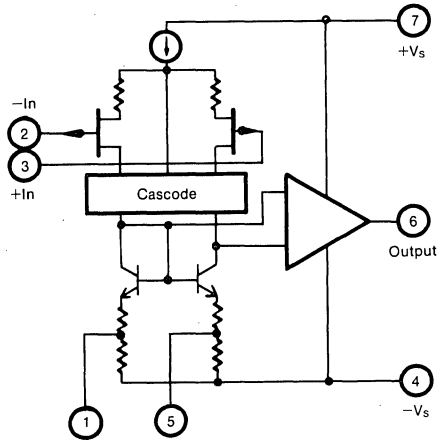
DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic *Difet* (dielectrically isolated FET) construction provides an unusual combination of high speed and accuracy.

Its wide bandwidth design minimizes dynamic errors. High slew rate and fast-settling behavior allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion characteristics provide high performance in frequency-domain circuitry. All dynamic and DC specifications are rated with a 1kΩ resistor in parallel with 500pF load impedance. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. *Difet* construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.



Difet® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_S = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA602AM			OPA602BM/SM			OPA602CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE											
Voltage: f_O = 10Hz			*			23			*		nV/√Hz
f_O = 100Hz			*			19			*		nV/√Hz
f_O = 1kHz			*			13			*		nV/√Hz
f_O = 10kHz			*			12			*		nV/√Hz
f_B = 10Hz to 10kHz			*			1.4			*		μVrms
f_B = 0.1Hz to 10Hz			*			0.95			*		μVp-p
Current: f_B = 0.1Hz to 10Hz			*			12			*		fAp-p
f_O = 0.1Hz to 20kHz			*			0.6			*		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage	V_{CM} = 0VDC		±300	±1000		±150	±500		±100	±250	μV
Over Specified Temp.			±550			±250	±1000		±200	±500	μV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		*	±15		±3	±5		±1	±2	μV/°C
Supply Rejection	$\pm V_S$ = 12V to 18V	70	*		80	100		86	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±2	±10		±1	±2		±0.5	±1	pA
Over Specified Temp.			±20	±500		±20	±200		±10	±100	pA
SM Grade						±200	±2000				pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		1	10		0.5	2		0.5	1	pA
Over Specified Temp.			20	500		20	200		10	100	pA
SM Grade						200	1000				pA
INPUT IMPEDANCE											
Differential			*			10^{13}‖1			*		Ω‖pF
Common-Mode			*			10^{14}‖3			*		Ω‖pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		*	*		±10.2	+13, −11		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	75	*		88	100		92	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq$ 1kΩ	75	*		88	100		92	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	3.5	*		4	6.5		5	*		MHz
Full Power Response	20Vp-p, R_L = 1kΩ		*			570			*		kHz
Slew Rate	V_O = ±10V, R_L = 1kΩ	20	*		24	35		28	*		V/μs
Settling Time: 0.1%	Gain = −1, R_L = 1kΩ		*			0.7			*		μs
0.01%	C_L = 500pF, 10V step		*			1.0			*		μs
RATED OUTPUT											
Voltage Output	R_L = 1kΩ	±11	*		±11.5	+12.9, −13.8			*	*	V
Current Output	V_O = ±10VDC	*	*		±15	±20		*	*		mA
Output Resistance	1MHz, open loop		*			80			*		Ω
Load Capacitance Stability	Gain = +1		*			1500			*		pF
Short Circuit Current		±25	*		±30	±50		*	*		mA
POWER SUPPLY											
Rated Voltage			*			±15			*		VDC
Voltage Range, Derated Performance		*		*	±5		±18	*		*	VDC
Current, Quiescent	I_O = 0mADC		*	*		3	4		*	*	mA
Over Specified Temp.			*	*		3.5	4.5		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient temp.	*		*	−25		+85	*		*	°C
SM Grade					−55		±125				°C
Operating	Ambient temp.	*		*	−55		+125	*		*	°C
Storage	Ambient temp.	*		*	−65		+150	*		*	°C
θ Junction-Ambient			*			200			*		°C/W

*Specification same as OPA602BM

ORDERING INFORMATION

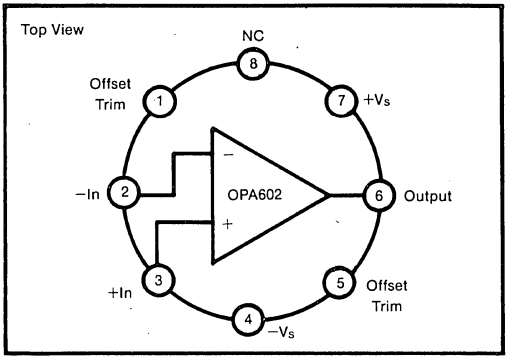
OPA602 ( ) ( )

Basic model number

Performance grade code
- A, B, C: −25°C to +85°C
- S: −55°C to +125°C

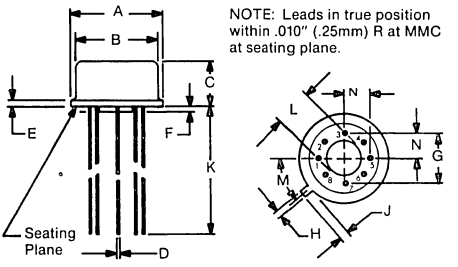
Package Code
- M: TO-99 Metal Package

CONNECTION DIAGRAM



MECHANICAL

TO-99 Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

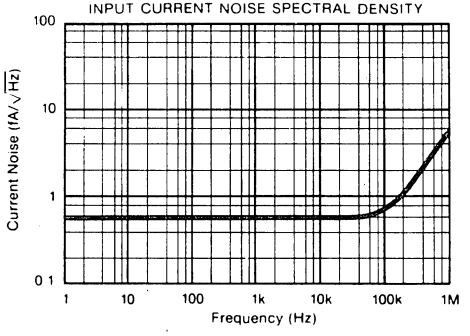
ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation ($T_J \leq +175°C$)	+1000mW
Differential Input Voltage	Total V_S
Input Voltage Range	$\pm V_S$
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit to ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

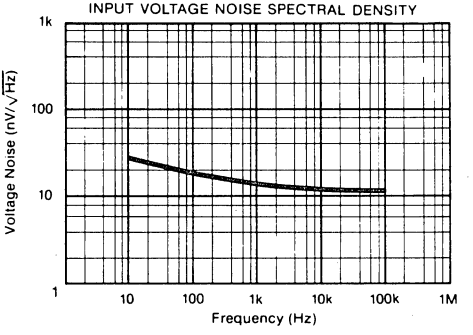
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = \pm 15VDC$ unless otherwise noted.

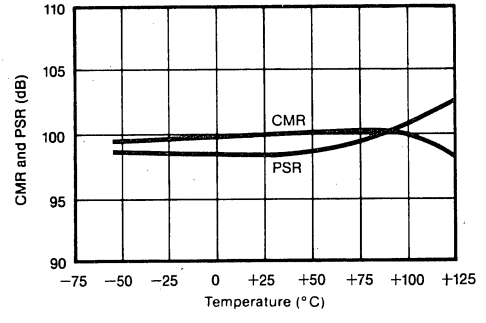
INPUT CURRENT NOISE SPECTRAL DENSITY



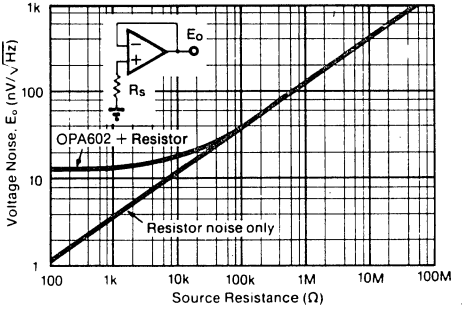
INPUT VOLTAGE NOISE SPECTRAL DENSITY



POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



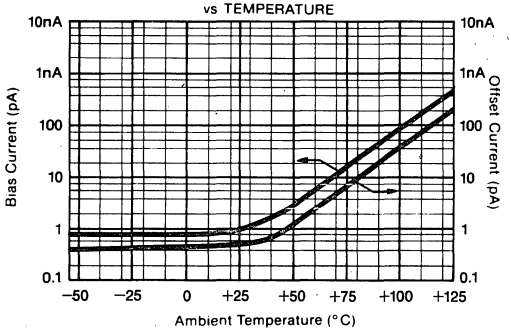
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



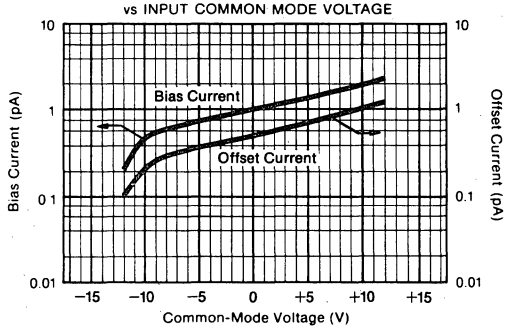
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = \pm 15VDC$ unless otherwise noted.

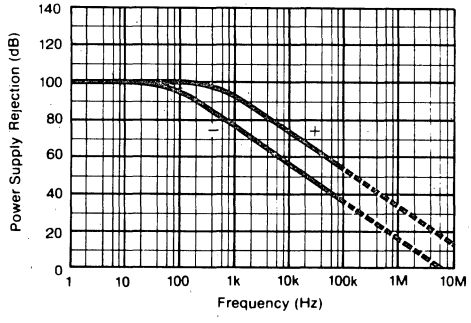
BIAS AND OFFSET CURRENT vs TEMPERATURE



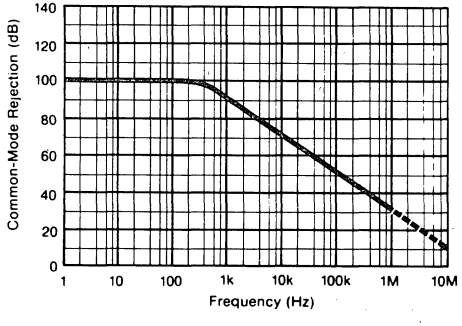
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



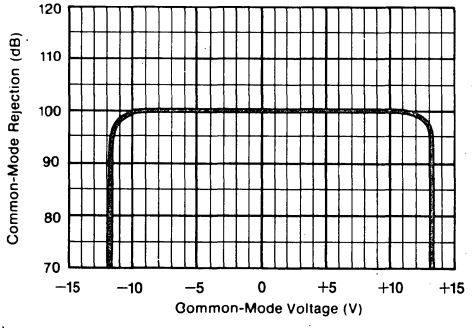
POWER SUPPLY REJECTION vs FREQUENCY



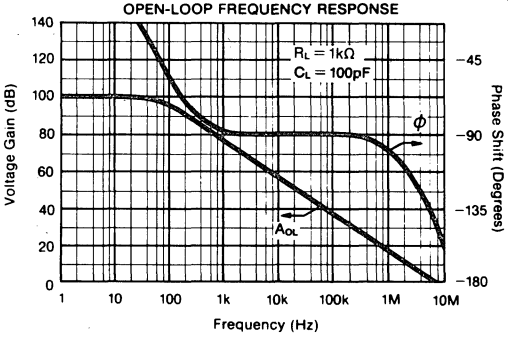
COMMON-MODE REJECTION vs FREQUENCY



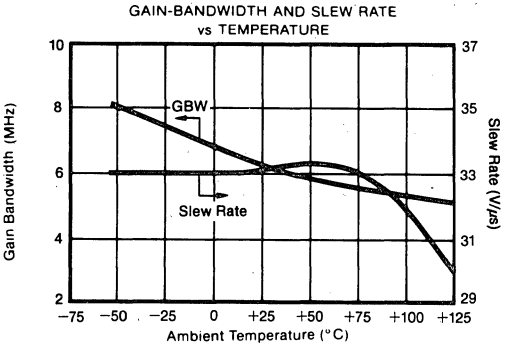
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



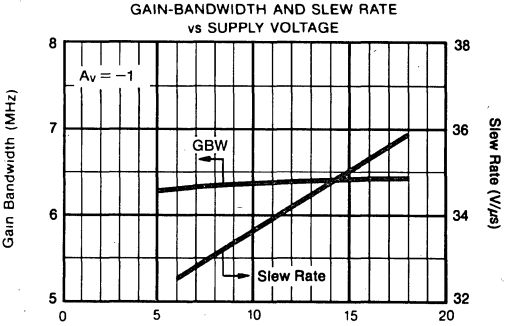
OPEN-LOOP FREQUENCY RESPONSE



GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



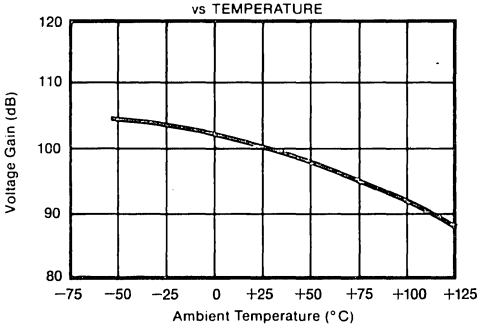
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



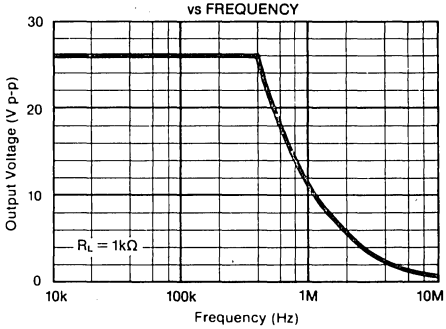
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

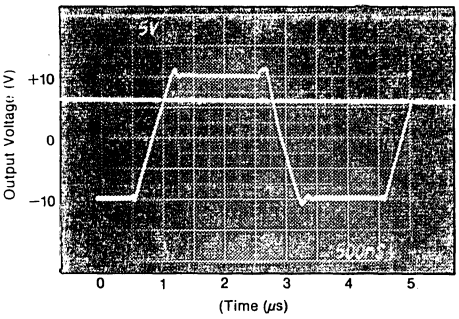
OPEN-LOOP GAIN vs TEMPERATURE



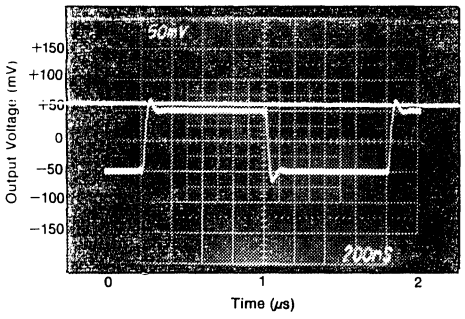
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



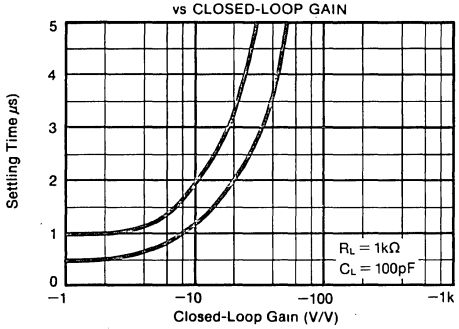
LARGE SIGNAL TRANSIENT RESPONSE



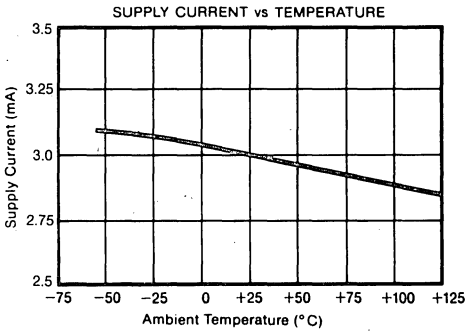
SMALL SIGNAL TRANSIENT RESPONSE



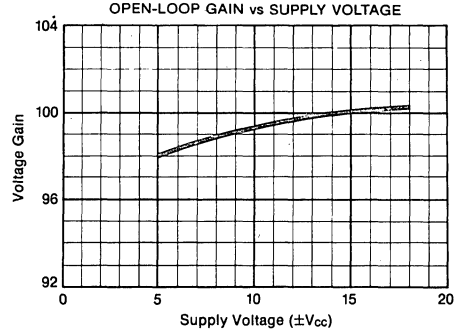
SETTLING TIME vs CLOSED-LOOP GAIN



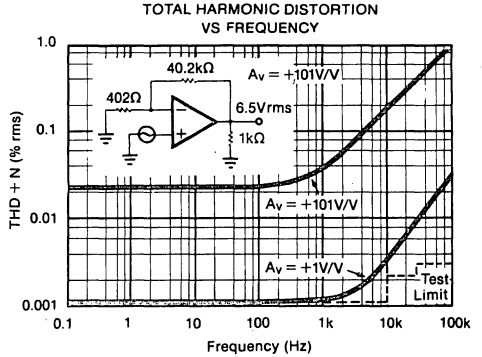
SUPPLY CURRENT vs TEMPERATURE



OPEN-LOOP GAIN vs SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION VS FREQUENCY



APPLICATIONS INFORMATION

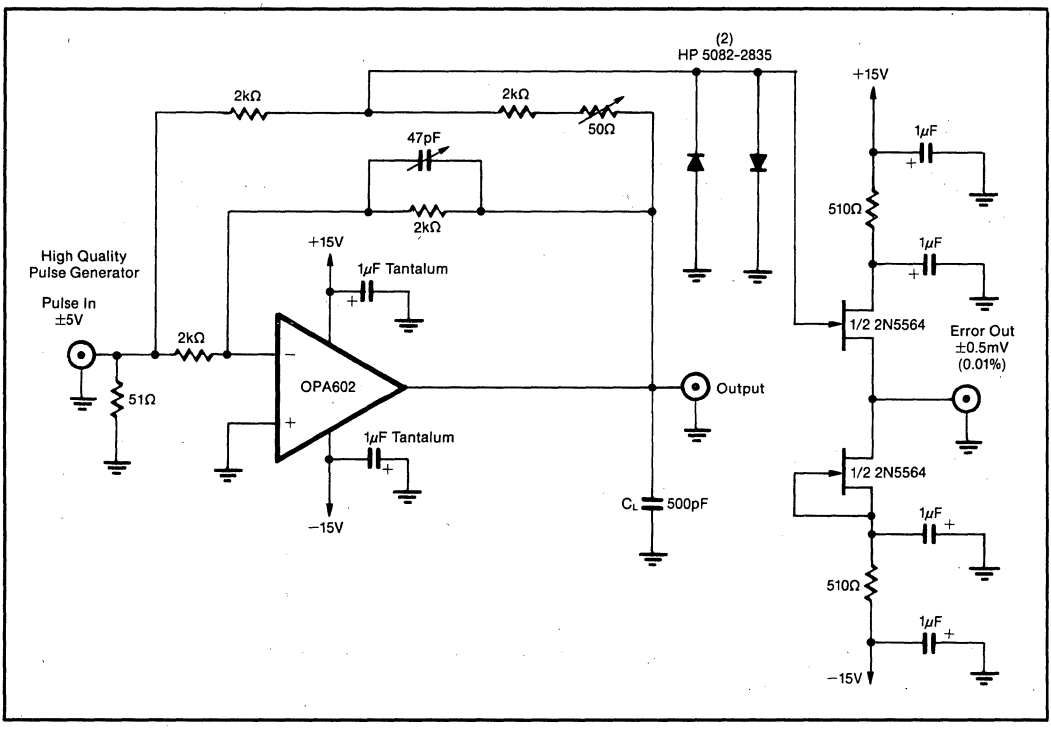


FIGURE 1. Settling Time and Slew Rate Test Circuit.

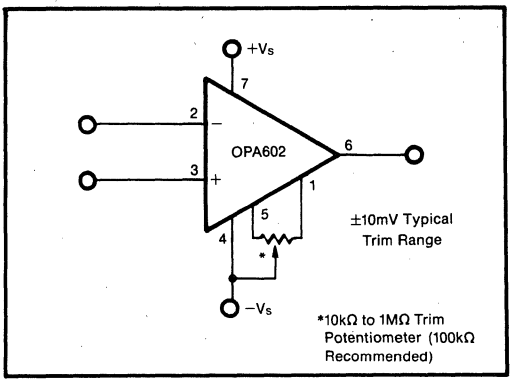
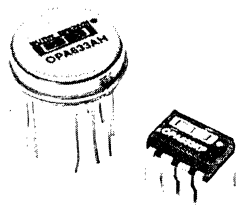


FIGURE 2. Offset Voltage Trim.

BURR-BROWN®



OPA633

High Speed BUFFER AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 275MHz
- HIGH SLEW RATE: 2500V/μs
- HIGH OUTPUT CURRENT: 100mA
- LOW OFFSET VOLTAGE: 1.5mV
- REPLACES HA-5033
- IMPROVED PERFORMANCE/PRICE: LH0033, LTC1010, HOS200

APPLICATIONS

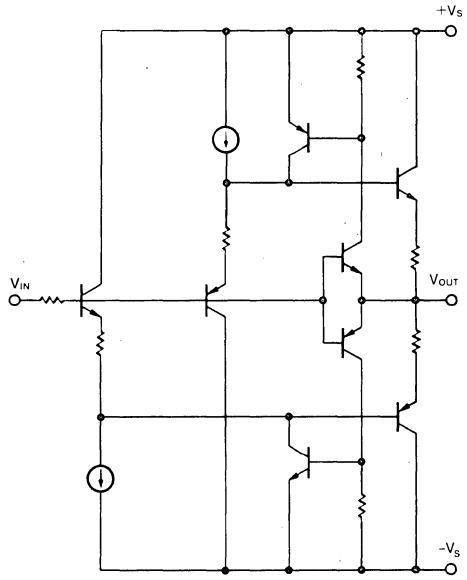
- OP AMP CURRENT BOOSTER
- VIDEO BUFFER
- LINE DRIVER
- A/D CONVERTER INPUT BUFFER

DESCRIPTION

The OPA633 is a monolithic unity-gain buffer amplifier featuring very wide bandwidth and high slew rate. A dielectric isolation process incorporating both NPN and PNP high frequency transistors achieves performance unattainable with conventional integrated circuit technology. Laser trimming provides low input offset voltage.

High output current capability allows the OPA633 to drive 50Ω and 75Ω lines, making it ideal for RF, IF and video applications. Low phase shift allows the OPA633 to be used inside amplifier feedback loops thus bringing high current output and ability to drive capacitive loads to many circuit applications.

The OPA633 is available in the 12-pin TO-8 hermetic metal package with −25°C to +85°C and −55°C to +125°C temperature ranges and a low cost plastic DIP package specified for operation from 0°C to +75°C.



International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

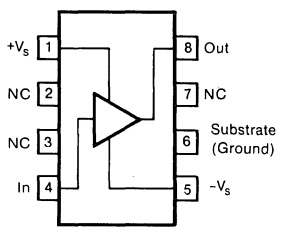
At +25°C, $V_S = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $C_L = 10pF$ unless otherwise noted.

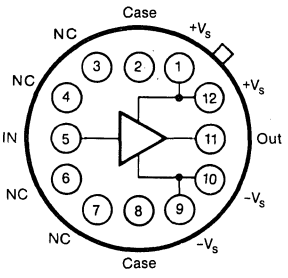
PARAMETER	CONDITIONS	OPA633AH			OPA633SH			OPA633KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE											
Small Signal Bandwidth			275			*			260		MHz
Full Power Bandwidth	V_O = 1Vrms, $R_L = 1k\Omega$		65			*			40		MHz
Slew Rate	V_O = 10V, $V_S = \pm 15V$, $R_L = 1k\Omega$	1000	2500		*	*		*	*		V/μs
Rise Time, 10% to 90%	V_O = 500mV		2.5			*			*		ns
Propagation Delay			1			*			*		ns
Overshoot			10			*			*		%
Settling Time, 0.1%			50			*			*		ns
Differential Phase Error[1]			0.1			*			*		Degrees
Differential Gain Error[1]			0.1			*			*		%
Total Harmonic Distortion	V_O = 1Vrms, $R_L = 1k\Omega$, f = 100kHz		0.005			*			*		%
	V_O = 1Vrms, $R_L = 100\Omega$, f = 100kHz		0.02								%
OUTPUT CHARACTERISTICS											
Voltage	$T_A = T_{MIN}$ to T_{MAX}	±8.0	±10		*	*		*	*		V
	$R_L = 1k\Omega$, $V_S = \pm 15V$	±11	±13		*	*		*	*		V
Current		±80	±100		*	*		*	*		mA
Resistance			5			*			*		Ω
TRANSFER CHARACTERISTICS											
Gain		0.93	0.95		*	*		*	*		V/V
	$R_L = 1k\Omega$		0.99			*			*		V/V
	$T_A = T_{MIN}$ to T_{MAX}	0.92	0.95		*	*		*	*		V/V
INPUT											
Offset Voltage	T_A = +25°C		±1.5	±15		*	*		±5	*	mV
	$T_A = T_{MIN}$ to T_{MAX}		±5	±25		*	*		±6	*	mV
vs Temperature			±33			*			*		μV/°C
vs Supply	$T_A = T_{MIN}$ to T_{MAX}	54	72		*	*		*	*		dB
Bias Current	T_A = +25°C		±15	±35		*	*		*	*	μA
	$T_A = T_{MIN}$ to T_{MAX}		±20	±50		*	*		*	*	μA
Noise Voltage	10Hz to 1MHz		20			*			*		μVp-p
Resistance			1.5			*			*		MΩ
Capacitance			1.6			*			*		pF
POWER SUPPLY											
Rated Supply Voltage	Specified performance		±12			*			*		V
Operating Supply Voltage	Derated performance	±5		±16	*		*	*		*	V
Current, Quiescent	$I_O = 0$		21	25		*	*		*	*	mA
	$I_O = 0$, $T_A = T_{MIN}$ to T_{MAX}		21	30		*	*		*	*	mA
TEMPERATURE RANGE											
Specification, Ambient		−25		+85	−55		+125	0		+75	°C
Operating, Ambient		−55		+125	*		*	−25		+85	°C
θ Junction, Ambient[2]			99			*			90		°C/W
θ Junction, Case[2]			31			*			27		°C/W

* Specification same as OPA633AH.

NOTES: (1) Differential phase error in video transmission systems is the change in phase of a color subcarrier resulting from a change in picture signal from blanked to white. Differential gain error is the change in amplitude at the color subcarrier frequency resulting from a change in picture signal from blanked to white. (2) Recommended heat sinks for the TO-8 package are: Thermalloy 2204A with θ_{SA} = 27°C/W and IERC Up TO-8-48CB, θ_{SA} = 10°C/W.

CONNECTION DIAGRAMS



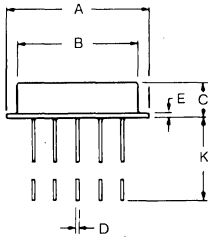


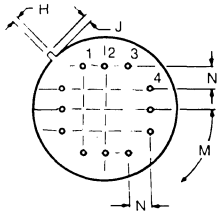
ABSOLUTE MAXIMUM RATINGS

Power Supply, $\pm V_S$	±20V
Input Voltage V_{IN}	$+V_S + 2$ to $-V_S - 2$
Output Current (peak)	±200mA
Internal Power Dissipation (25°C): TO-8 (H)	1.75W
DIP (P)	1.95W
Junction Temperature	200°C
Storage Temperature Range: TO-8	−65°C to +150°C
DIP	−40°C to +85°C
Lead Temperature (soldering, 60s)	300°C

MECHANICAL

TO-8



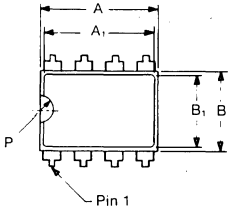


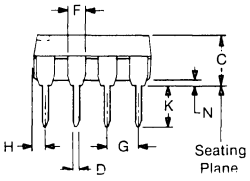
NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

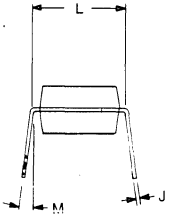
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.593	.603	15.06	15.32
B	.547	.553	13.89	14.05
C	.130	.150	3.30	3.81
D	.016	.019	0.41	0.48
E	.010	.040	0.25	1.02
H	.026	.036	0.66	0.91
J	.026	.036	0.66	0.91
K	.500	.562	12.70	14.27
M	45° BASIC		45° BASIC	
N	.100 BASIC		2.54 BASIC	

"P" Package, 8-Pin Plastic

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.



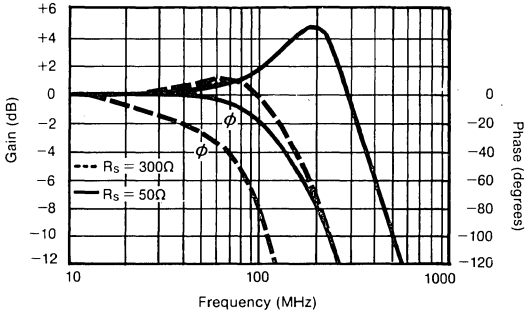




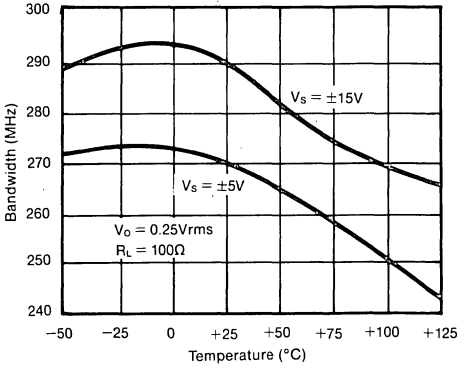
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.355	.400	9.03	10.16
A_1	.340	.385	8.65	9.80
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

TYPICAL PERFORMANCE CURVES

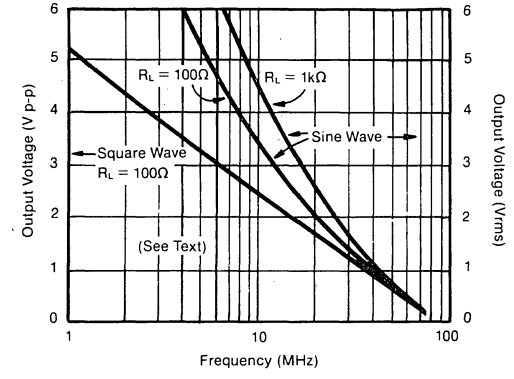
GAIN/PHASE VS FREQUENCY



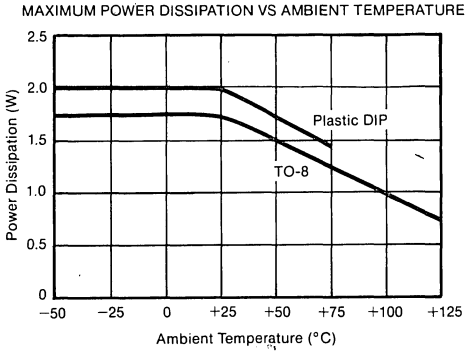
SMALL SIGNAL BANDWIDTH VS TEMPERATURE



SAFE INPUT VOLTAGE VS FREQUENCY

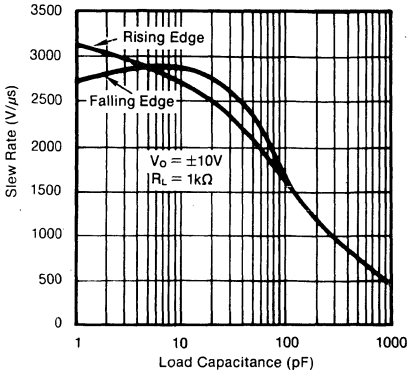


MAXIMUM POWER DISSIPATION VS AMBIENT TEMPERATURE

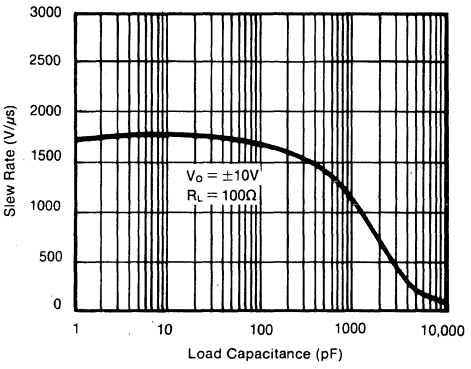


TYPICAL PERFORMANCE CURVES (CONT)

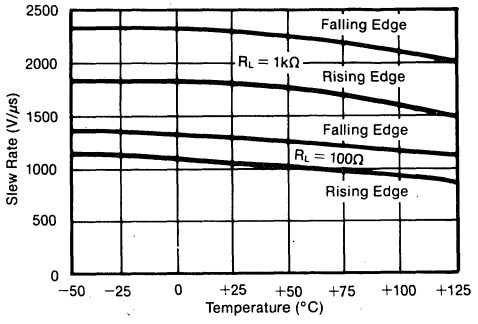
SLEW RATE VS LOAD CAPACITANCE



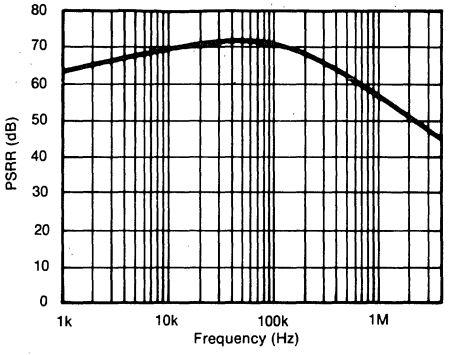
SLEW RATE VS LOAD CAPACITANCE



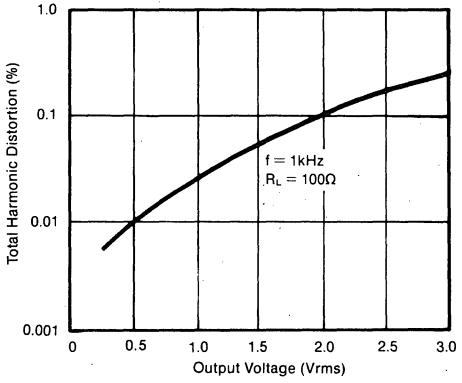
SLEW RATE VS TEMPERATURE



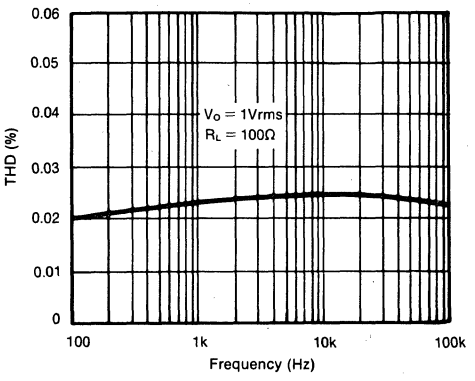
POWER SUPPLY REJECTION VS FREQUENCY



TOTAL HARMONIC DISTORTION VS OUTPUT VOLTAGE

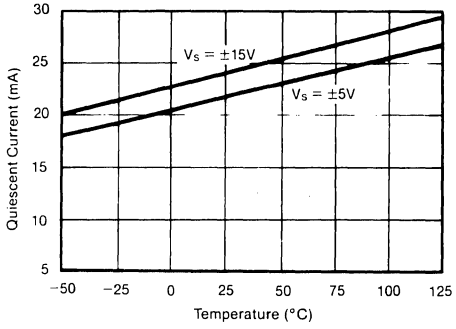


TOTAL HARMONIC DISTORTION VS FREQUENCY

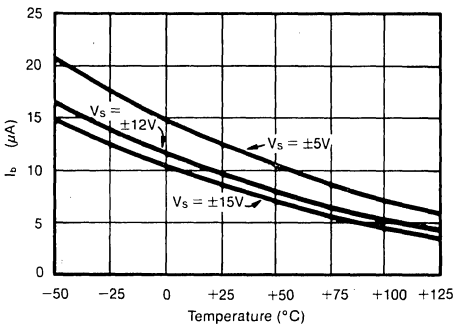


TYPICAL PERFORMANCE CURVES (CONT)

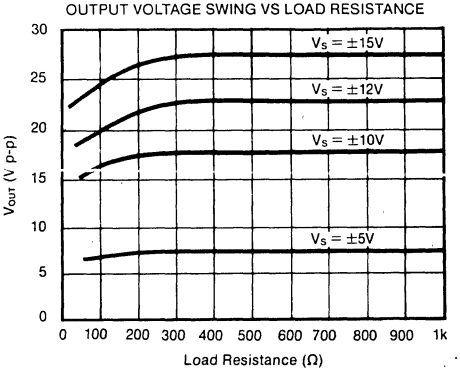
QUIESCENT CURRENT VS TEMPERATURE



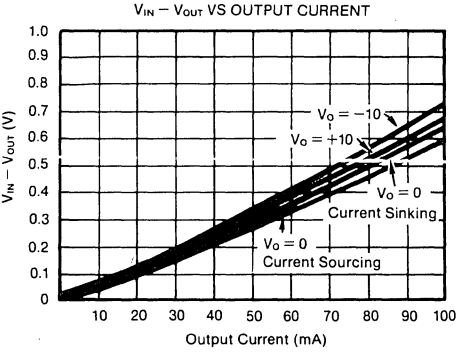
INPUT BIAS CURRENT VS TEMPERATURE



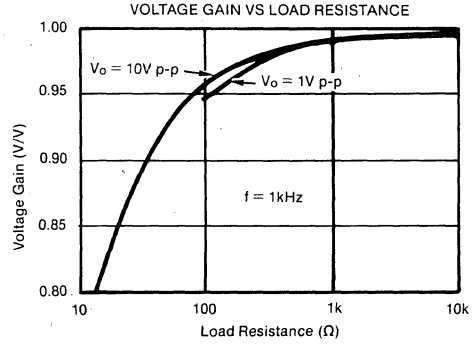
OUTPUT VOLTAGE SWING VS LOAD RESISTANCE



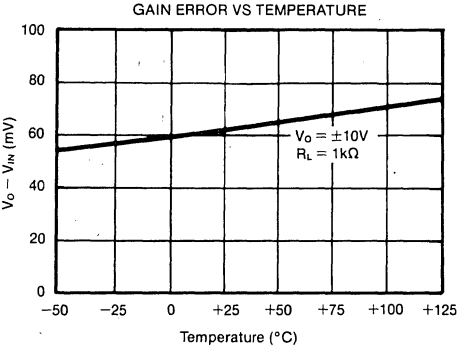
$V_{IN} - V_{OUT}$ VS OUTPUT CURRENT



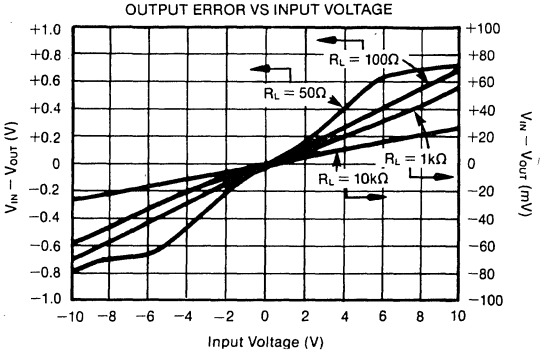
VOLTAGE GAIN VS LOAD RESISTANCE



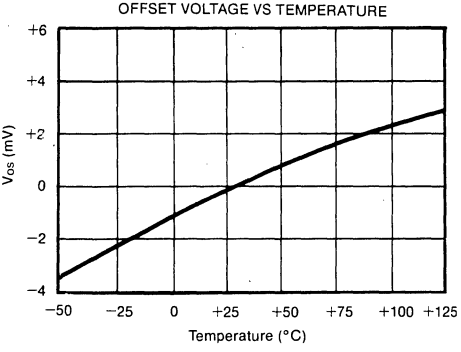
GAIN ERROR VS TEMPERATURE



OUTPUT ERROR VS INPUT VOLTAGE



OFFSET VOLTAGE VS TEMPERATURE



INSTALLATION AND OPERATION

CIRCUIT LAYOUT

As with any high frequency circuitry, good circuit layout technique must be used to achieve optimum performance. A circuit-board layout is provided which demonstrates the principles of good layout. Most of the applications circuits shown can be evaluated using this circuit board.

Pinout of the TO-8 package version has been designed for maximum compatibility with other buffer amplifiers. Pins 1 and 12 are internally connected to $+V_S$. Pins 9 and 10 are internally connected to $-V_S$. This allows the OPA633 to be used in applications presently using the LH0033 buffer amplifier. Only one of the power supply connections for $+V_S$ and $-V_S$ must be connected for proper operation.

Power supply connections must be bypassed with high frequency capacitors. Many applications benefit from the use of two capacitors on each power supply—a ceramic capacitor for good high frequency decoupling and a tantalum type for lower frequencies. They should be located as close as possible to the buffer's power supply pins. A large ground plane is used to minimize high frequency ground drops and stray coupling.

The case of the TO-8 package is connected to pin 2, which should be grounded. Pin 6 of the DIP package connects to the substrate of the integrated circuit and should be connected to ground. In principle it could also be connected to $+V_S$ or $-V_S$, but ground is preferable. The additional lead length and capacitance associated with sockets may present problems in applications requiring the highest fidelity of high speed pulses.

Depending on the nature of the input source impedance, a series input resistor may be required for best stability. This behavior is influenced somewhat by the load impedance (including any reactive effects). A value of 50Ω to 200Ω is typical. This resistor should be located close to the OPA633's input pin to avoid stray capacitance at the input which could reduce bandwidth (see Gain and Phase Versus Frequency curve).

OVERLOAD CONDITIONS

The input and output circuitry of the OPA633 are not protected from overload. When the input signal and load characteristics are within the device's capabilities, no protection circuitry is required. Exceeding device limits can result in permanent damage.

The OPA633's small package and high output current capability can lead to overheating. The internal junction temperature should not be allowed to exceed 150°C. Although failure is unlikely to occur until junction temperature exceeds 200°C, reliability of the part will be degraded significantly at such high temperatures. External heat sinks can be used to reduce the temperature rise. Since significant heat transfer takes place through the package leads, wide printed circuit traces to all leads will improve heat sinking. Sockets can reduce heat sinking significantly and thus are not recommended.

Junction temperature rise is proportional to internal power dissipation. This can be reduced by using the minimum supply voltage necessary to produce the required output voltage swing. For instance, 1V video signals can be easily handled with ±5V power supplies thus minimizing the internal power dissipation.

Output overloads or short circuits can result in permanent damage by causing excessive output current. The 50Ω or 75Ω series output resistor used to match line impedance will, in most cases, provide adequate protection. When this resistor is not used, the device can be protected by limiting the power supply current. See "Protection Circuits."

Excessive input levels at high frequency can cause increased internal dissipation and permanent damage. See the safe input voltage versus frequency curves. When used to buffer an op amp's output, the input to the OPA633 is limited, in most cases, by the op amp. When high frequency inputs can exceed safe levels, the device must be protected by limiting the power supply current.

PROTECTION CIRCUITS

The OPA633 can be protected from damage, due to excessive currents, by the simple addition of resistors in series with the power supply pins (Figure 5a). While this limits output current, it also limits voltage swing with low impedance loads. This reduction in voltage swing is minimal for AC or high crest factor signals since only the average current from the power supply causes a voltage drop across the series resistor. Short duration load-current peaks are supplied by the bypass capacitors.

The circuit of Figure 5b overcomes the limitations of the previous circuit with DC loads. It allows nearly full output voltage swing up to its current limit of approximately 140mA. Both circuits require good high frequency capacitors (e.g., tantalum) to bypass the buffer's power supply connections.

CAPACITIVE LOADS

The OPA633 is designed to safely drive capacitive loads up to 0.01μF. It must be understood, however, that rapidly changing voltages demand large output load currents:

$$I_{LOAD} = (C_{LOAD})\, dV/dt$$

Thus a signal slew rate of 1000V/μs and load capacitance of 0.01μF demands a load current of 10A. Clearly maximum slew rates cannot be combined with large capacitive loads. Load current should be kept less than 100mA continuous (200mA peak) by limiting the rate of change of the input signal or reducing the load capacitance.

USE INSIDE A FEEDBACK LOOP

The OPA633 may be used inside the feedback path of an op amp such as the OPA606. Higher output current is achieved without degradation in accuracy. This approach may actually improve performance in precision applications by removing load-dependent dissipation from a precision op amp. All vestiges of load-dependent offset voltage and temperature drift can be eliminated with this technique. Since the buffer is placed within the feedback loop of the op amp, its DC errors will have a negligible effect on overall accuracy. Any DC errors contributed by the buffer are divided by the loop gain of the op amp.

The low phase shift of the OPA633 allows its use inside the feedback loop of a wide variety of op amps. To assure stability, the buffer must not add significant phase shift to the loop at the gain crossing frequency of the circuit—the frequency at which the open loop gain of the op amp is equal to the closed loop gain of the application. The OPA633 has a typical phase shift of less than 10° up to 70MHz, thus making it useful even with wideband op amps.

APPLICATIONS CIRCUITS

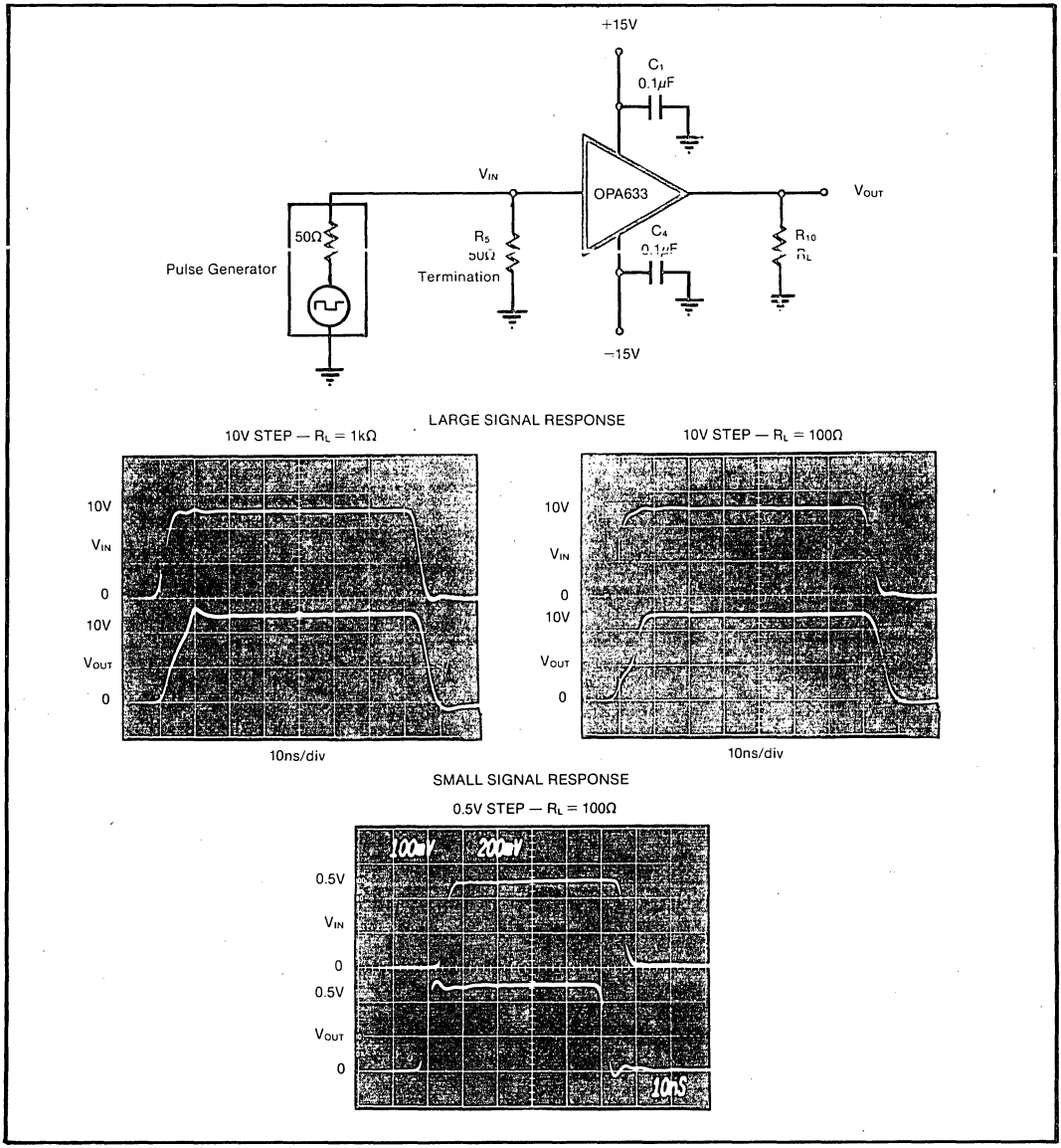


FIGURE 1. Dynamic Response Test Circuit.

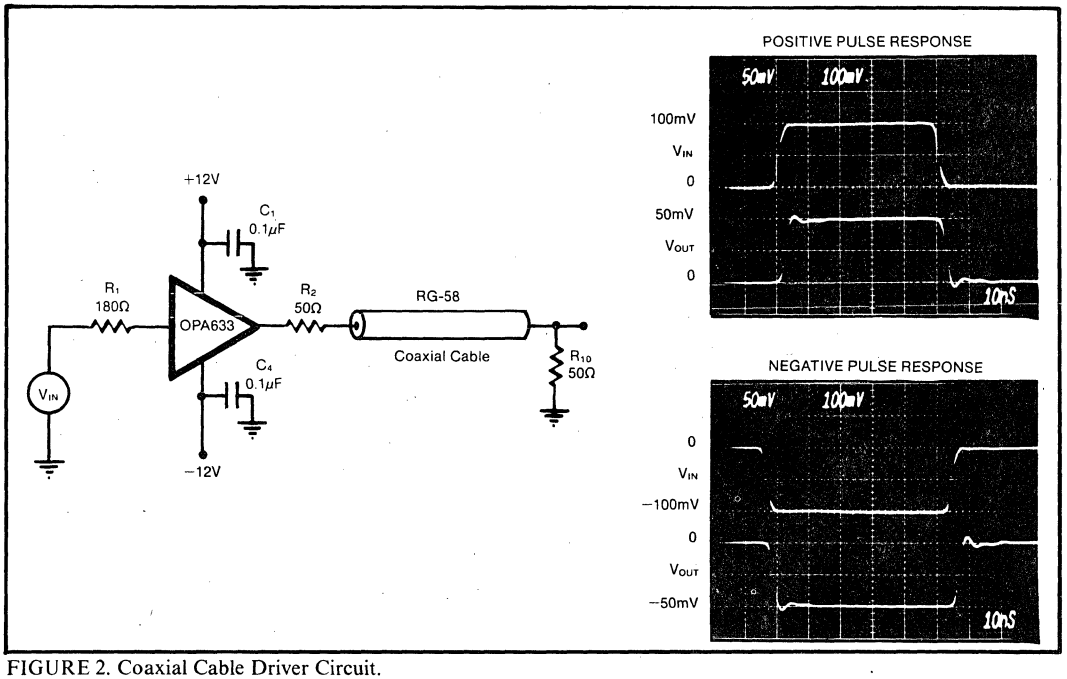


FIGURE 2. Coaxial Cable Driver Circuit.

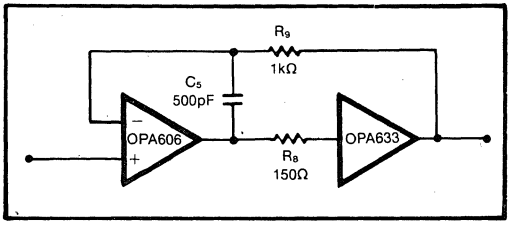


FIGURE 3. Precision High Current Buffer.

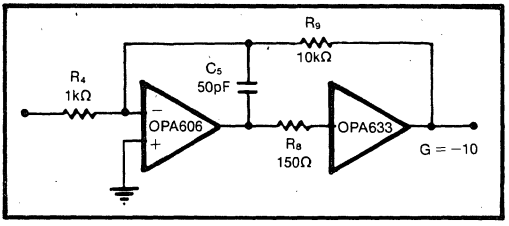


FIGURE 4. Buffered Inverting Amplifier.

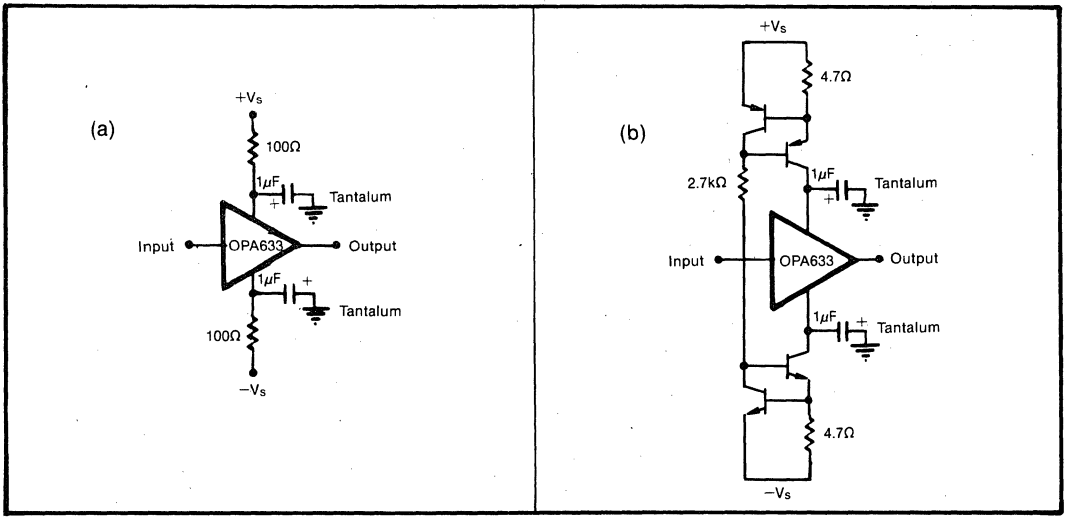
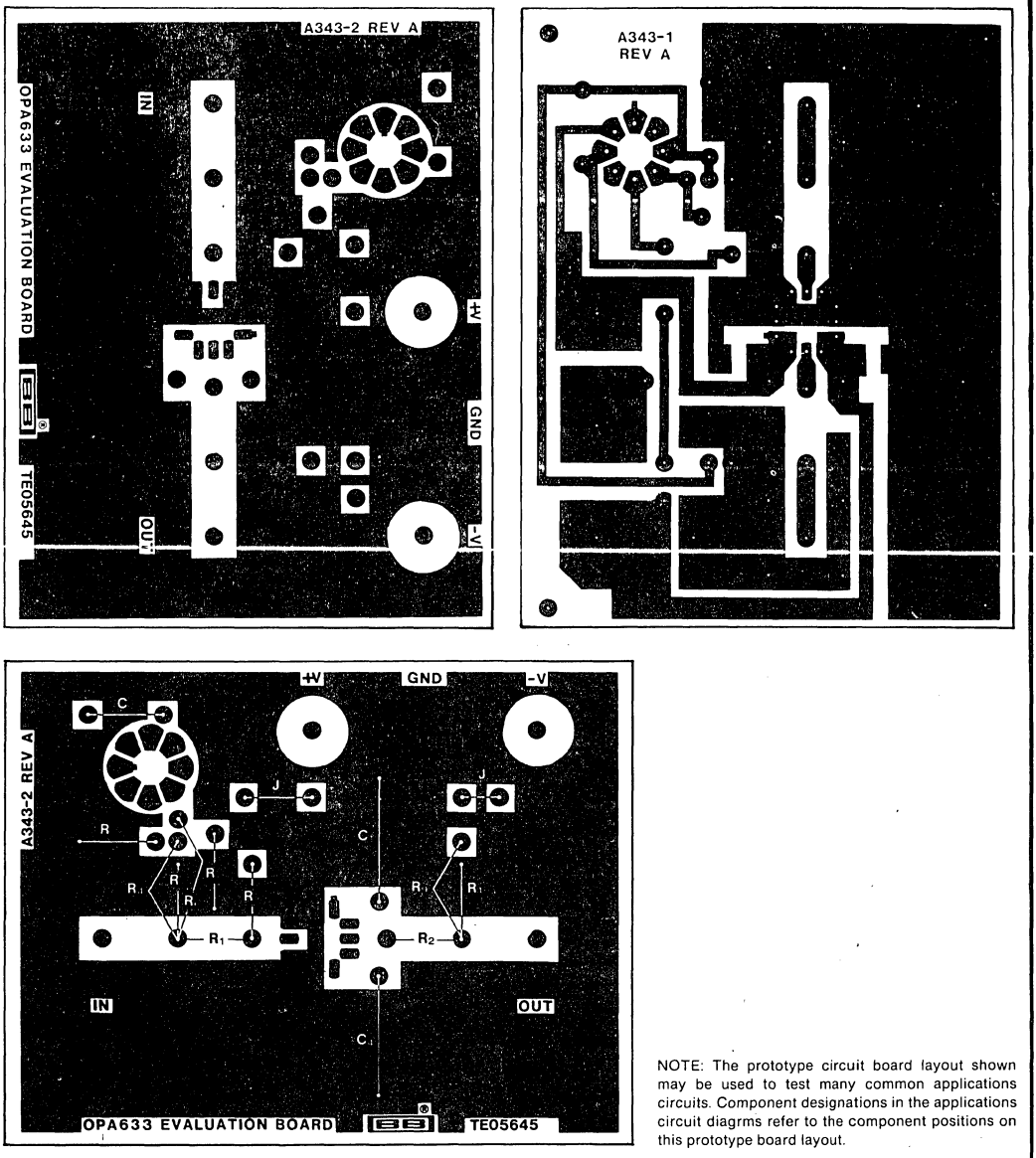


FIGURE 5. Output Protection Circuits.



NOTE: The prototype circuit board layout shown may be used to test many common applications circuits. Component designations in the applications circuit diagrms refer to the component positions on this prototype board layout.

FIGURE 6. Prototype Circuit Board Layout.

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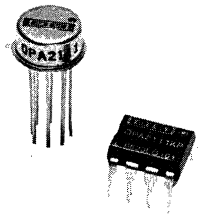


OPA2111

NEW PACKAGE NOW AVAILABLE

Dual Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% tested: 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW BIAS CURRENT: 4pA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 2.8μV/°C
- HIGH OPEN LOOP GAIN: 114dB min
- HIGH COMMON-MODE REJECTION: 96dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

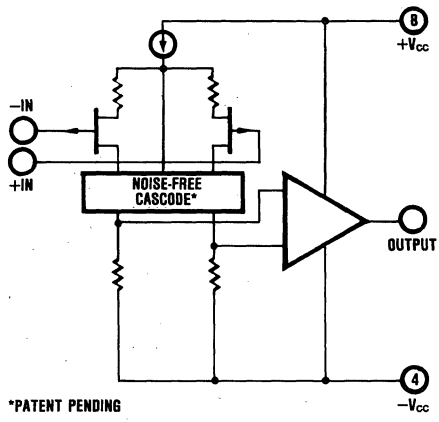
The OPA2111 is a high precision monolithic *Difet* (dielectrically isolated FET) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patent pending). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op-amp pin configuration allows upgrading of existing designs to higher performance levels.



OPA2111 SIMPLIFIED CIRCUIT (EACH AMPLIFIER)

BIFET® National Semiconductor Corp., *Difet*® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM/KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT														
NOISE														
Voltage, f_O = 10Hz	Max: 100% tested		40	80		30	60		40	80		40		nV/√Hz
f_O = 100Hz	Max: 100% tested		15	40		11	30		15	40		15		nV/√Hz
f_O = 1kHz	Max: 100% tested		8	15		7	12		8	15		8		nV/√Hz
f_O = 10kHz	(1)		6	8		6	8		6	8		6		nV/√Hz
f_B = 10Hz to 10kHz	(1)		0.7	1.2		0.6	1.0		0.7	1.2		0.7		µV, rms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3		1.6		µV, p-p
Current, f_B = 0.1Hz to 10Hz	(1)		15	24		12	19		15	24		15		fA, p-p
f_O = 0.1Hz to 20kHz	(1)		0.8	1.3		0.6	1.0		0.8	1.0		0.8		fA/√Hz
OFFSET VOLTAGE[2]														
Input Offset Voltage	V_{CM} = 0VDC		±0.1	±0.75		±0.05	±0.5		±0.1	±0.75		±0.3	±2	mV
Average Drift	T_A = T_{MIN} to T_{MAX}		±2	±6		±0.5	±2.8		±2	±6		±8	±15	µV/°C
Match			±1			±0.5			2			2		µV/°C
Supply Rejection		90	110		96	110		90	110		86	110		dB
			±3	±31		±3	±16		±3	±31		±3	±50	µV/V
Channel Separation	100Hz, R_L = 2kΩ		136			136			136			136		dB
BIAS CURRENT[2]														
Initial Bias Current	V_{CM} = 0VDC		±2	±8		±1.2	±4		±2	±8		±3	±15	pA
Match			±1			±0.5			±1			2		pA
OFFSET CURRENT[2]														
Input Offset Current	V_{CM} = 0VDC		±1.2	±6		±0.6	±3		±1.2	±6		±3	±12	pA
IMPEDANCE														
Differential			10^{13} || 1			10^{13} || 1			10^{13} || 1			10^{13} || 1		Ω || pF
Common-Mode			10^{14} || 3			10^{14} || 3			10^{14} || 3			10^{14} || 3		Ω || pF
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11	±10	±11		±10	±11			±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		96	110		90	110		82	110		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	R_L ≥ 2kΩ	110	125		114	125		110	125		106	125		dB
Match			3			2			3			3		dB
FREQUENCY RESPONSE														
Unity Gain, Small Signal			2			2			2			2		MHz
Full Power Response	20V p-p, R_L = 2kΩ	16	32		16	32		16	32			32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2		1	2		1	2			2		V/µs
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		6			6			6			6		µs
0.01%	10V step		10			10			10			10		µs
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5			5			5		µs
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		±11	±12		±11	±12		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		100			100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Rated Voltage			±15			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		5	7		5	7		5	7		5	9	mA
TEMPERATURE RANGE														
Specification	Ambient temp.	−25		+85	−25		+85	−55		+125	0		+70	°C
Operating	Ambient temp.	−55		+125	−40		+85	−55		+125	−40		+85	°C
Storage	Ambient temp.	−65		+150	−65		+150	−65		+150	−40		+85	°C
θ Junction-Ambient			200			200			200			200[4]		°C/W

NOTES: (1) Sample tested—maximum parameters are guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Typical θ_{J-A} = 150°C/W for plastic DIP.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM/KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE														
Specification Range	Ambient temp.	−25		+85	−25		+85	−55		+125	0		+70	°C
INPUT														
OFFSET VOLTAGE[1]														
Input Offset Voltage	V_{CM} = 0VDC		±0.22	±1.2		±0.08	±0.75		±0.3	±1.5		±0.9	±5	mV
Average Drift			±2	±6		±0.5	±2.8		±2	±6		±8	±15	µV/°C
Match			1			0.5			2			2		µV/°C
Supply Rejection		86	100		90	100		86	100		82	100		dB
			±10	±50		±10	±32		±10	±50		±10	±80	µV/V
BIAS CURRENT[1]														
Initial Bias Current	V_{CM} = 0VDC		±125	±1nA		±75	±500		±2.0nA	±16.3nA		±125	±500	pA
Match			60			30			1nA					pA
OFFSET CURRENT[1]														
Input Offset Current	V_{CM} = 0VDC		±75	±750		±38	±375		±1.3nA	±12nA		±75	±375	pA
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		80	100		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	120		110	120		106	120		100	120		dB
Match			5			3			5			5		dB
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10.5	±11		±10.5	±11		±10.5	±11		±10.5	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Current, Quiescent	I_O = 0mADC		5	8		5	8		5	8		5	10	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ORDERING INFORMATION

OPA2111 ( ) ( )

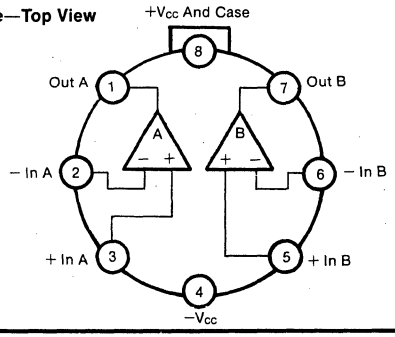
- Basic model number
- Performance grade
  - A, B = −25°C to +85°C
  - S = −55°C to +125°C
  - K = 0°C to +70°C
- Package Code
  - M = TO-99 metal can
  - P = Plastic DIP

ABSOLUTE MAXIMUM RATINGS

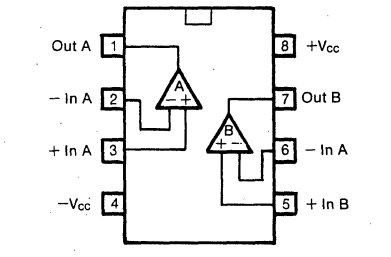
Supply	±18VDC
Internal Power Dissipation ($T_J \leq$ +175°C)	500mW
Differential Input Voltage	Total V_{CC}
Input Voltage Range	±V_{CC}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit to ground (+25°C)	Continuous
Junction Temperature	+175°C

CONNECTION DIAGRAMS

'M' Package—Top View

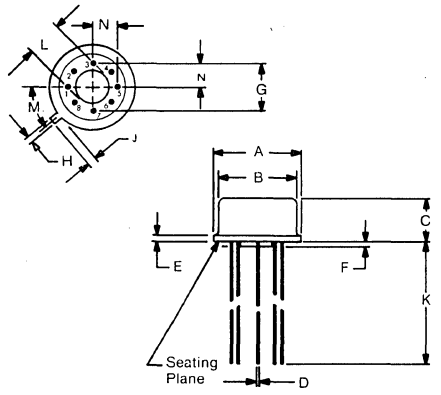


'P' Package—Top View



MECHANICAL

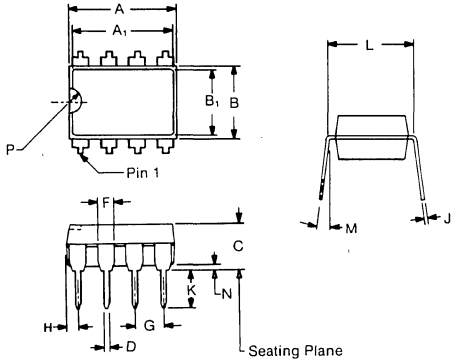
'M' Package—TO-99 (Hermetic)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

'P' Package—Plastic DIP



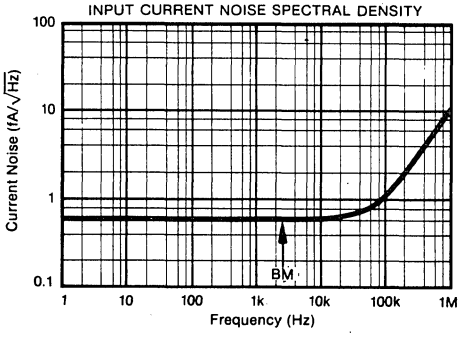
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.355	.400	9.02	10.16
A_1	.340	.385	8.65	9.80
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.39	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

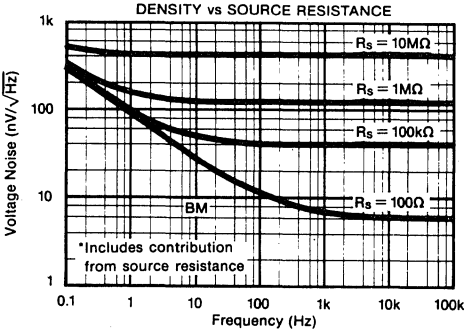
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

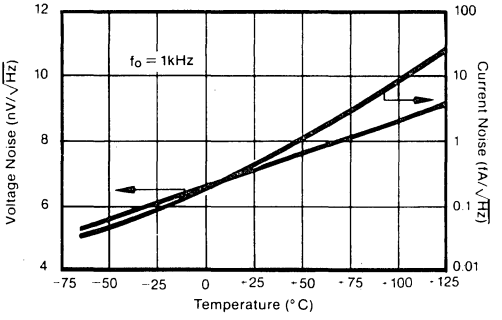
INPUT CURRENT NOISE SPECTRAL DENSITY



TOTAL* INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



NOTE:
Refer to complete data sheet PDS-540 for complete typical curves and applications information.

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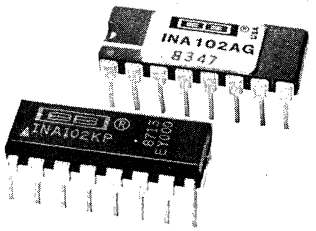


INA102

Low Power
High Accuracy
INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 750μA, max
- INTERNAL GAINS: X 1, 10, 100, 1000
- LOW GAIN DRIFT: 5ppm/°C, max
- HIGH CMR: 90dB, min
- LOW OFFSET VOLTAGE DRIFT: 2μV/°C, max
- LOW OFFSET VOLTAGE: 100μV, max
- LOW NONLINEARITY: 0.01%, max
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$
- LOW COST

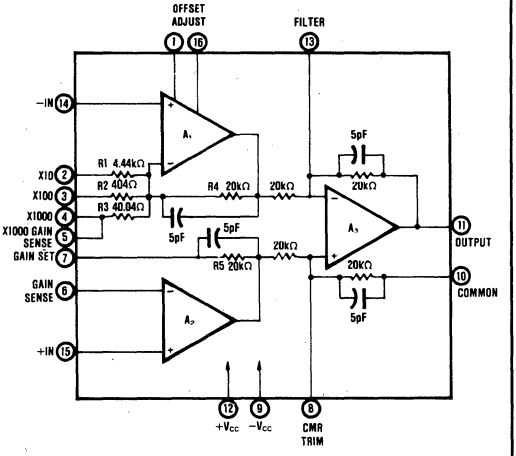
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gauges
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCER AMPLIFIER
- LOW LEVEL SIGNAL AMPLIFIER
- MEDICAL INSTRUMENTATION
- MULTICHANNEL SYSTEMS
- BATTERY POWERED EQUIPMENT

DESCRIPTION

The INA102 is a high-accuracy monolithic instrumentation amplifier designed for signal conditioning applications where low quiescent power is desired. On-chip thin-film resistors provide excellent temperature and stability performance. State-of-the-art laser trimming technology insures high gain accuracy and common-mode rejection while avoiding expensive external components. These features make the INA102 ideally suited for battery powered and high volume applications.

The INA102 is also convenient to use. A gain of 1, 10, 100, or 1000 may be selected by simply strapping the appropriate pins together. 5ppm/°C gain drift in low gains can then be achieved without external adjustment. When higher than specified CMR is required, CMR can be trimmed using the pins provided. In addition, balanced filtering can be accomplished in the output stage.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

MODEL		INA102AG			INA102CG			INA102KP			
	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN											
Range of Gain		1		1000	*		*	*		1000	V/V
Gain Equation			G = 1 + (40k/R_G)[1]			*			*		V/V
Error, DC: G = 1	T_A = +25°C			0.1			0.05			0.15	%
G = 10	T_A = +25°C			0.1			0.05			0.35	%
G = 100	T_A = +25°C			0.25			0.15			0.4	%
G = 1000	T_A = +25°C			0.75			0.5			0.9	%
G = 1	T_A = T_{MIN} to T_{MAX}			0.16			0.08			0.21	%
G = 10	T_A = T_{MIN} to T_{MAX}			0.19			0.11			0.44	%
G = 100	T_A = T_{MIN} to T_{MAX}			0.37			0.21			0.52	%
G = 1000	T_A = T_{MIN} to T_{MAX}			0.93			0.62			1.08	%
Gain Temp. Coefficient											
G = 1				10			5			*	ppm/°C
G = 10				15			10			*	ppm/°C
G = 100				20			15			*	ppm/°C
G = 1000				30			20			*	ppm/°C
Nonlinearity, DC: G = 1	T_A = +25°C			0.03			0.01			*	% of FS
G = 10	T_A = +25°C			0.03			0.01			*	% of FS
G = 100	T_A = +25°C			0.05			0.02			*	% of FS
G = 1000	T_A = +25°C			0.1			0.05			*	% of FS
G = 1	T_A = T_{MIN} to T_{MAX}			0.045			0.015			*	% of FS
G = 10	T_A = T_{MIN} to T_{MAX}			0.045			0.015			*	% of FS
G = 100	T_A = T_{MIN} to T_{MAX}			0.075			0.03			*	% of FS
G = 1000	T_A = T_{MIN} to T_{MAX}			0.15			0.1			*	% of FS
RATED OUTPUT											
Voltage	R_L = 10kΩ	±(|V_{CC}| − 3.5)			*	*		±(|V_{CC}| − 2.5)			V
Current		±1			*			*			mA
Short-Circuit Current			2			*			*		mA
Output Impedance: G = 1000			0.1			*			*		Ω
INPUT											
OFFSET VOLTAGE											
Initial Offset[2]	T_A = +25°C			±300 ±300/G			±100 ±200/G			±400 ±700/G	μV
vs Temperature				±5, ±10/G			±2 ±5/G			*	μV/°C
vs Supply				±40 ±50/G			±10 ±20/G			*	μV/V
vs Time			±(20 + 30/G)			*			*		μV/mo
BIAS CURRENT											
Initial Bias Current (each input)	T_A = T_{MIN} to T_{MAX}			50		6	30		*	*	nA
vs Temperature			±0.1			*			*		nA/°C
vs Supply			±0.1			*			*		nA/V
Initial Offset Current	T_A = T_{MIN} to T_{MAX}		±2.5	±15		±2.5	±10		*	*	nA
vs Temperature			±0.1			*			*		nA/°C
IMPEDANCE											
Differential			10^{10} || 2			*			*		Ω || pF
Common-mode			10^{10} || 2			*			*		Ω || pF
VOLTAGE RANGE											
Range, Linear Response	T_A = T_{MIN} to T_{MAX}	±(|V_{CC}| − 3.5)			*			±(|V_{CC}| − 2.5)			V
CMR with 1kΩ Source Imbalance											
G = 1	DC to 60Hz	80	94		90	94		60	84		dB
G = 10	DC to 60Hz	80	100		90	*		*	*		dB
G = 10 to 1000	DC to 60Hz	80	100		90	100		*	*		dB
NOISE											
Input Voltage Noise											
f_B = 0.01Hz to 10Hz			0.1			*			*		μV, p-p
Density, G = 1000											
f_O = 10Hz			30			*			*		nV/√Hz
f_O = 100Hz			25			*			*		nV/√Hz
f_O = 1kHz			25			*			*		nV/√Hz
Input Current Noise											
f_B = 0.01Hz to 10Hz			25			*			*		pA, p-p
Density: f_O = 10Hz			0.3			*			*		pA/√Hz
f_O = 100Hz			0.2			*			*		pA/√Hz
f_O = 1kHz			0.15			*			*		pA/√Hz
DYNAMIC RESPONSE											
Small Signal, ±3dB Flatness	V_{OUT} = 0.1Vrms										
G = 1			300			*			*		kHz
G = 10			30			*			*		kHz
G = 100			3			*			*		kHz
G = 1000			0.3			*			*		kHz
Small Signal, ±1% Flatness	V_{OUT} = 0.1Vrms										
G = 1			30			*			*		kHz
G = 10			3			*			*		kHz
G = 100			0.3			*			*		kHz
G = 1000			0.03			*			*		kHz
Full Power, G = 1 to 100	V_{OUT} = 10V, R_L = 10kΩ	1.7	2.5		*	*		*	*		kHz
Slew Rate, G = 1 to 100	V_{OUT} = 10V, R_L = 10kΩ	0.1	0.15		*	*		*	*		V/μsec
Settling Time, 0.1%:	R_L = 10kΩ, C_L = 100pF										
G = 1	10V step		50			*			*		μsec
G = 100			360			*			*		μsec
G = 1000			3300			*			*		μsec
Settling Time, 0.01%: G = 1	10V step		60			*			*		μsec
G = 100			500			*			*		μsec
G = 1000			4500			*			*		μsec

ELECTRICAL (CONT)

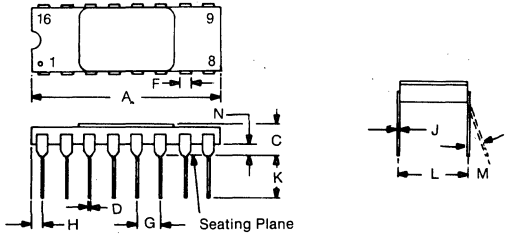
MODEL	CONDITIONS	INA102AG			INA102CG			INA102KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±3.5		±18	*		*	*		*	V
Quiescent Current[3]	V_O = 0V, $T_A = T_{MIN}$ to T_{MAX}		±500	±750		*	*		*	*	µA
TEMPERATURE RANGE											
Specification		−25		+85	*		*	0		+70	°C
Operation		−25		+85	*		*	*		*	°C
Storage		−65		+150	*		*	−55		+125	°C

*Specifications same as for INA102AG.

NOTES: (1) The internal gain set resistors have an absolute tolerance of ±20%; however, their tracking is 50ppm/°C. R_G will add to the gain error if gains other than 1, 10, 100 or 1000 are set externally. (2) Adjustable to zero at any one time.

MECHANICAL

Hermetic

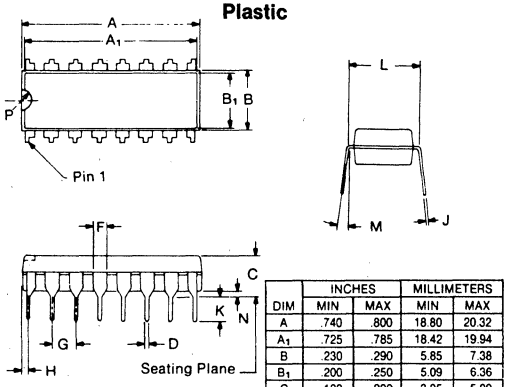


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within .010" (.25mm) R at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

Plastic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.740	.800	18.80	20.32
A_1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.02	0.05	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

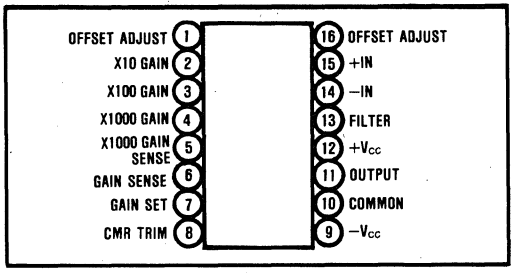
PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CASE: Plastic

ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Voltage Range	±V_{CC}
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range: Ceramic	−65°C to +150°C
Plastic	−55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration	Continuous to ground

PIN CONFIGURATION



ORDERING INFORMATION

INA102 X G

Basic Model Number

Performance Grade Code
A, C: −25°C to +85°C
K: 0°C to +70°C

Package Code
G: 16-pin Hermetic DIP
P: 16-pin Plastic DIP

INA102AG, INA102CG, INA102KP

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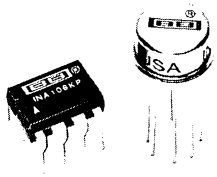


INA106

Precision Fixed-Gain DIFFERENTIAL AMPLIFIER

FEATURES

- FIXED GAIN, A = 10
- CMR 100dB min over temp
- NONLINEARITY 0.001% max
- NO EXTERNAL ADJUSTMENTS REQUIRED
- EASY TO USE
- COMPLETE SOLUTION
- HIGHLY VERSATILE
- LOW COST
- TO-99 HERMETIC METAL AND LOW COST PLASTIC PACKAGES

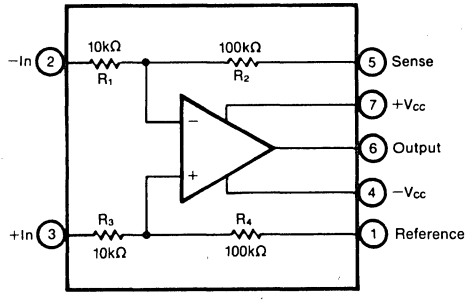
APPLICATIONS

- DIFFERENTIAL AMPLIFIER, A = 10
- BASIC INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- INVERTING AMPLIFIER, A = −10
- NONINVERTING AMPLIFIER, A = 10
- SUMMING AMPLIFIER, WEIGHTED
- ±100V CM RANGE DIFFERENTIAL AMPLIFIER

DESCRIPTION

The INA106 is a precision fixed-gain differential amplifier. As a monolithic circuit, it offers high reliability at low cost. It consists of a premium grade operational amplifier and an on-chip precision resistor network.

The INA106 is completely self-contained and offers the user a highly versatile function. No adjustments to gain, offset, and CMR are necessary. This provides three important advantages: (1) lower initial design engineering time, (2) lower manufacturing assembly time and cost, and (3) easy cost-effective field repair of a precision circuit.



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SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted.

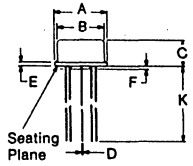
PARAMETER	CONDITIONS	INA106AM MIN	INA106AM TYP	INA106AM MAX	INA106BM MIN	INA106BM TYP	INA106BM MAX	INA106KP MIN	INA106KP TYP	INA106KP MAX	UNITS
GAIN											
Initial[1]			10			*			*		V/V
Error			0.005	0.01		*	*		0.01	0.025	%
vs Temperature			−4	±10		*	*		*		ppm/°C
Nonlinearity[2]			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, −5mA	10	12		*	*		*	*		V
Rated Current	E_O = 10V	+20, −5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To common		+40/−10			*			*		mA
Capacitive Load	Stable operation		1000			*			*		pF
INPUT											
Impedance	Differential		10			*			*		kΩ
	Common-mode		110			*			*		kΩ
Voltage Range	Differential	±1			*			*			V
	Common-mode	±11			*			*			V
Common-mode Rejection[3]	$T_A = T_{MIN}$ to T_{MAX}	94	100		100	106		86	*		dB
OFFSET VOLTAGE	RTI[4]										
Initial			50	100		*	*		*	200	µV
vs Temperature			0.2	5		*	2		*		µV/°C
vs Supply	±V_{CC} = 6V to 18V		1	10		*	*		*	*	µV/V
vs Time			10			*			*		µV/mo
OUTPUT NOISE VOLTAGE	RTI[5]										
F_B = 0.01Hz to 10Hz			1			*			*		µV p-p
F_O = 10kHz			30			*			*		nV/√Hz
DYNAMIC RESPONSE											
Gain Bandwidth	−3dB		5			*			*		MHz
Full Power BW	V_O = 20V p-p	30	50		*	*		*	*		kHz
Slew Rate		2	3		*	*		*	*		V/µs
Settling Time: 0.1%	V_O = 10V step		5			*			*		µs
0.01%	V_O = 10V step		10			*			*		µs
0.01%	V_{CM} = 10V step, V_{DIFF} = 0V		5			*			*		µs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated performance	±5		±18	*		*	*		*	V
Quiescent Current	V_{OUT} = 0V		±1.5	±2		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		−25		+85	*		*	0		+70	°C
Operation		−55		+125	*		*	−25		+85	°C
Storage		−65		+150	*		*	−40		+85	°C

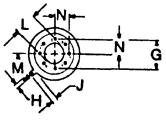
* Specification same as for INA106AM.

NOTES: (1) Connected as difference amplifier (see Figure 4). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see Maintaining CMR section). (4) Includes effects of amplifier's input bias and offset currents. (5) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

MECHANICAL

TO-99 Package



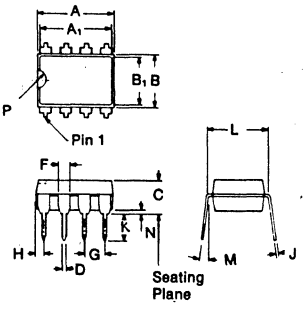


NOTE: Leads in true position within 0.01" (0.25 mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

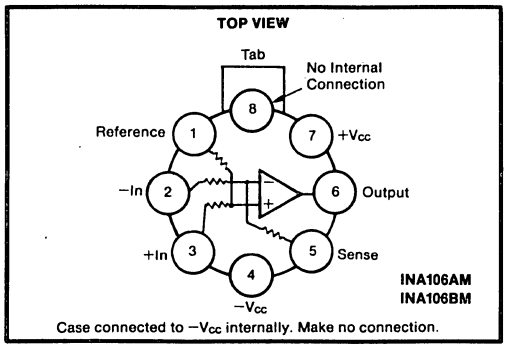
"P" Package—Plastic DIP



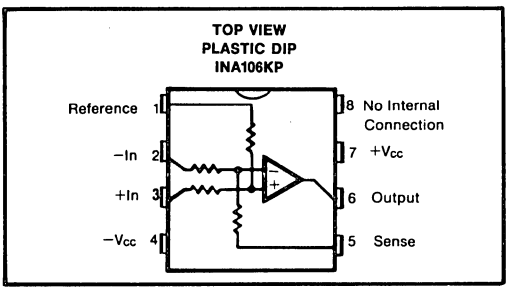
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.355	.400	9.02	10.16
A_1	.340	.385	8.64	9.78
B	.230	.290	5.84	7.37
B_1	.200	.250	5.08	6.35
C	.120	.200	3.05	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.81
L	.300 BASIC		7.63 BASIC	
M	.0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

PIN DESIGNATIONS



PIN DESIGNATIONS



ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Voltage Range	±Vcc
Operating Temperature Range: M	−55°C to +125°C
P	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short Circuit to Common	Continuous

ORDERING INFORMATION

INA106 X X

Basic Model Number

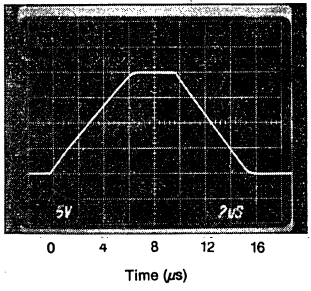
Performance Grade
- A, B: −25°C to +85°C
- K: 0°C to +70°C

Package Code
- M: TO-99 metal can
- P: 8-pin mini plastic DIP

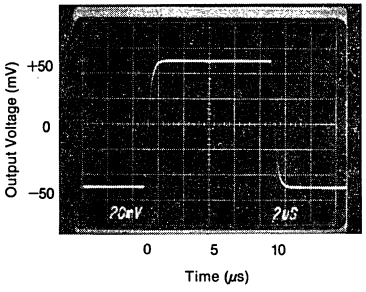
TYPICAL PERFORMANCE CURVES

T_A = 25°C, ±V_{CC} = 15V unless otherwise noted.

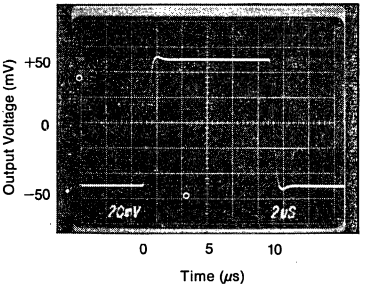
STEP RESPONSE



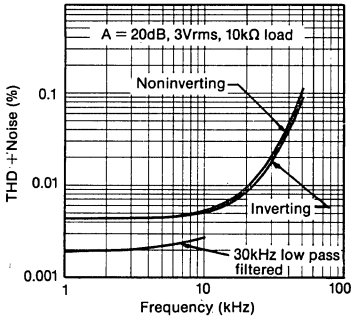
SMALL SIGNAL RESPONSE
(No Load)



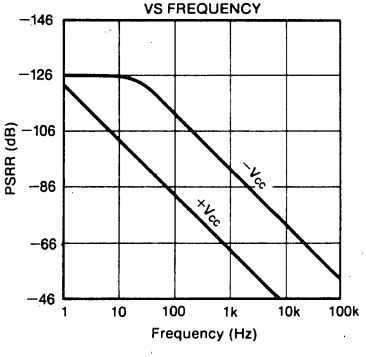
SMALL SIGNAL RESPONSE
(R_{LOAD} = ∞Ω, C_{LOAD} = 1000pF)



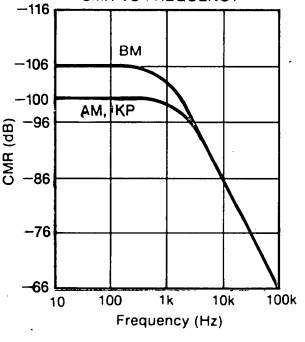
TOTAL HARMONIC DISTORTION AND NOISE VS FREQUENCY



POWER SUPPLY REJECTION VS FREQUENCY

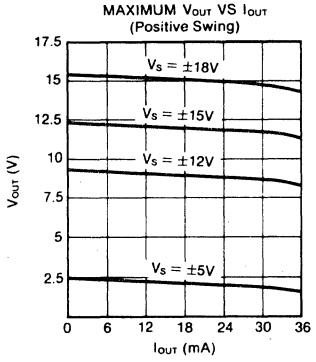


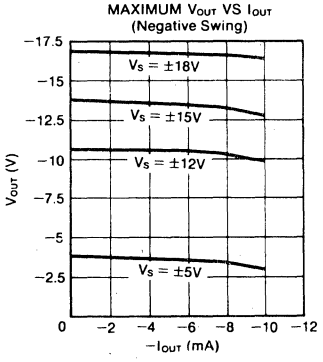
CMR VS FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.





DISCUSSION OF PERFORMANCE

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1μF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance.

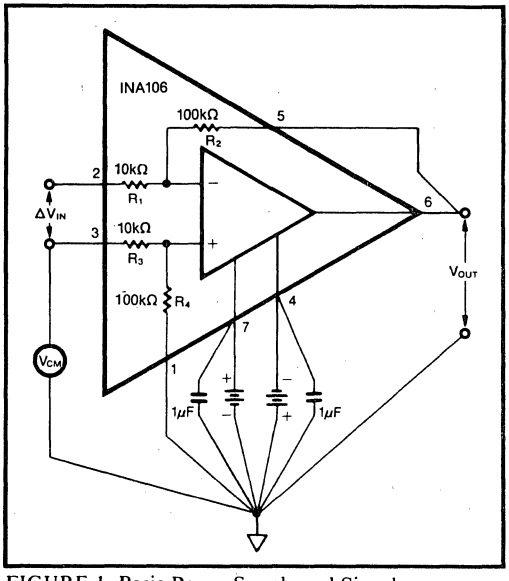


FIGURE 1. Basic Power Supply and Signal Connections.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuit for the INA106. This circuit will allow ±3mV of adjustment and will not affect the gain accuracy or CMR.

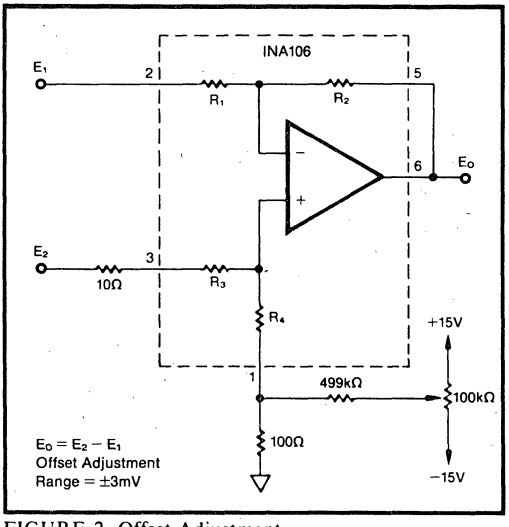


FIGURE 2. Offset Adjustment.

MAINTAINING COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: (1) resistor matching and tracking (the internal INA106 circuitry does this for the user) and (2) source impedance including its imbalance.

Referring to Figure 1, the CMR depends upon the match of the internal R_4/R_3 ratio to the R_1/R_2 ratio. A CMR of 106dB requires resistor matching of 0.005%. To maintain 100dB, minimum CMR to +85°C, the resistor TCR tracking must be better than 2ppm/°C. These accuracies are difficult and expensive to reliably achieve with discrete components.

Any source impedance adds directly to the input resistors, R_1 and R_3, and will degrade DC and AC CMR. Likewise any wiring resistance adds directly to any of the precision difference resistors. A resistance of 0.5Ω (0.005% of 10kΩ) will degrade the 106dB CMR of the INA106; 5Ω will degrade the CMR to 86dB.

When input filters are used preceding an instrumentation amplifier, care should also be taken to match RCs on the two input lines. For example, mismatched input filters for high frequencies will reduce the CMR at lower frequencies, e.g, 60Hz. Differential filters will not degrade AC CMR.

RESISTOR NOISE IN THE INA106

Figure 3 shows the model for calculating resistor noise in the INA106. Resistors have Johnson noise resulting from thermal agitation. The expression for this noise is:

$$E_{RMS} = \sqrt{4KTRB}$$

Where: K = Boltzman's constant (J/°K)
T = Absolute temperature (°K)
R = Resistance (Ω)
B = Bandwidth (Hz)

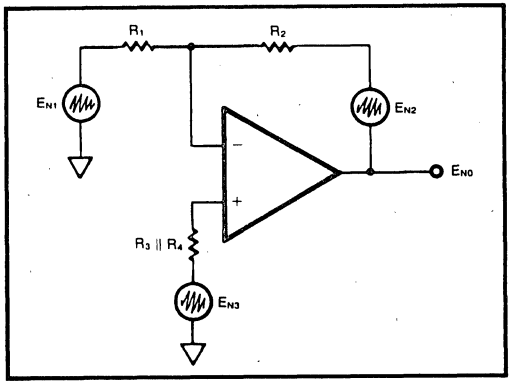


FIGURE 3. Resistor Noise Model.

At room temperature, this noise becomes:

$$E_N = 1.3^{-10}\sqrt{R} \qquad (V/\sqrt{Hz})$$

The three noise sources in Figure 2 are:

$$E_{N1} = 1.3^{-10}\,(R_2/R_1)\,\sqrt{R_1}$$
$$E_{N2} = 1.3^{-10}\,\sqrt{R_2}$$
$$E_{N3} = 1.3^{-10}\,(1 + R_2/R_1)\,\sqrt{R_3 \| R_4}$$

Adding as the root of the sums squared,

$$E_{NO} = 193nV\,\sqrt{Hz}$$

RTI, with A = 10,

$$E_{NI} = 19.3nV/\sqrt{Hz}$$

For example,

E_{NO} within a
600kHz BW = $0.15mV_{RMS}$
= 0.9mVp-p with a crest factor of 6 (statistically includes 99.7% of all noise peak occurrences)

This is the noise due to the resistors alone. It is included in the noise specification of the INA106.

APPLICATIONS CIRCUITS

The INA106 is ideally suited for a wide range of circuit functions. The following figures show many applications circuits.

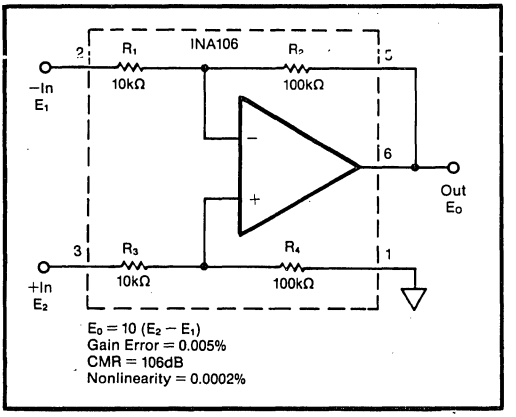


FIGURE 4A. Precision Difference Amplifier.

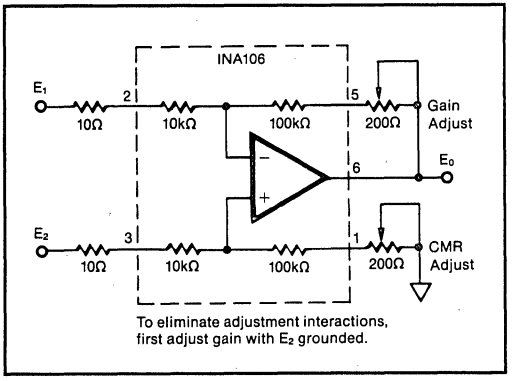
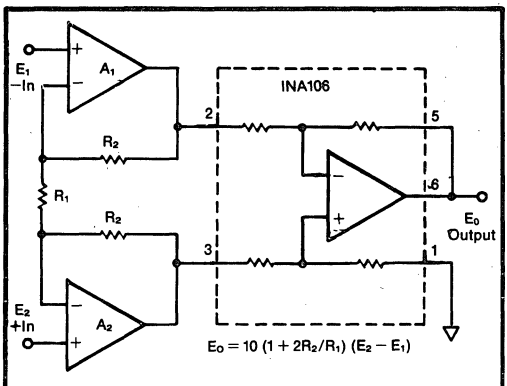


FIGURE 4B. Difference Amplifier With Gain And CMR Adjust.



For the ultimate performance high gain instrumentation amplifier, the INA106 can be combined with state-of-the-art op amps. For low source impedance applications, an input stage using OPA37s will give the best low noise, offset, and temperature drift. At source impedances above about 10kΩ, the bias current noise of the OPA37 reacting with the input impedance begins to dominate the noise. For these applications, using an OPA111 or a dual OPA2111 FET input op amp will provide lower noise. For an electrometer grade IA, use the OPA128. (See table below.)

Using the INA106 for the difference amplifier also extends the input common-mode range of the instrumentation amplifier to ±10V. A conventional IA with a unity-gain difference amplifier has an input common-mode range limited to ±5V for an output swing of ±10V. This is because a unity-gain difference amp needs ±5V at the input for 10V at the output, allowing only 5V additional for common mode.

A_1, A_2	R_1 (Ω)	R_2 (kΩ)	Gain (V/V)	CMRR (dB)	I_b (pA)	Noise at 1kHz (nV/√Hz)
OPA37A	50.5	2.5	1000	128	40000	4
OPA111B	202	10	1000	110	1	10
OPA128LM	202	10	1000	118	0.075	38

FIGURE 5. Precision Instrumentation Amplifier.

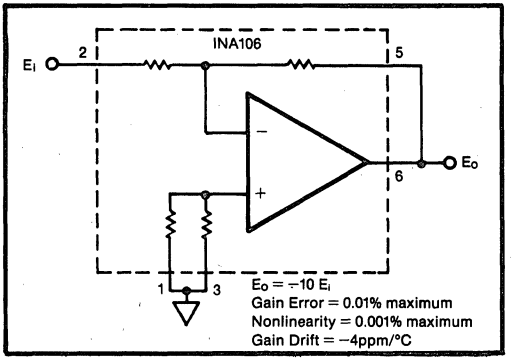


FIGURE 6. Precision Inverting Amplifier with Gain of −10.

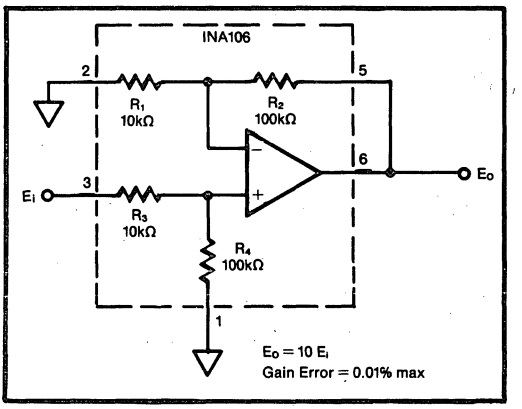


FIGURE 7. Precision Noninverting Amplifier with Gain of 10.

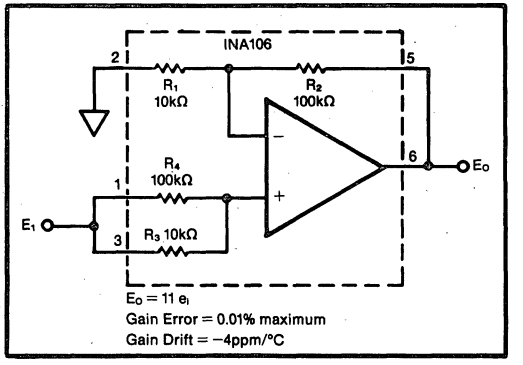


FIGURE 8. Precision Noninverting Amplifier with Gain of 11.

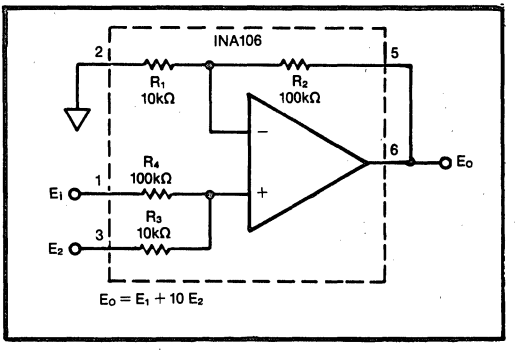
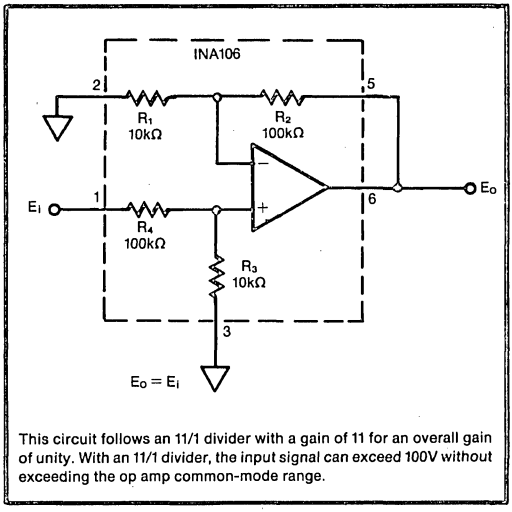


FIGURE 9. Precision Summing Amplifier with Weighted Inputs.



This circuit follows an 11/1 divider with a gain of 11 for an overall gain of unity. With an 11/1 divider, the input signal can exceed 100V without exceeding the op amp common-mode range.

FIGURE 10. Voltage Follower with Input Protection.

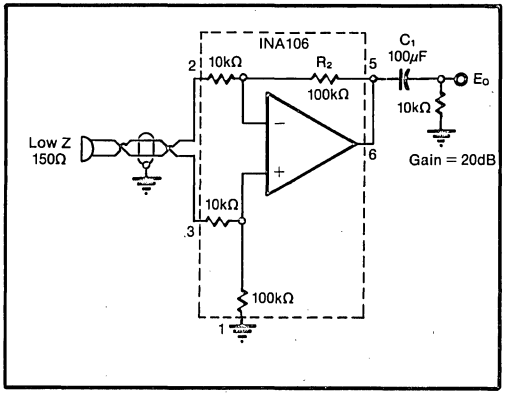
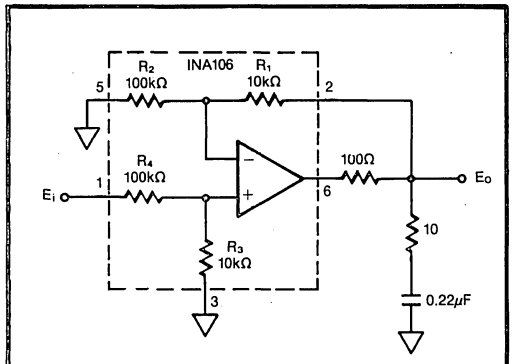


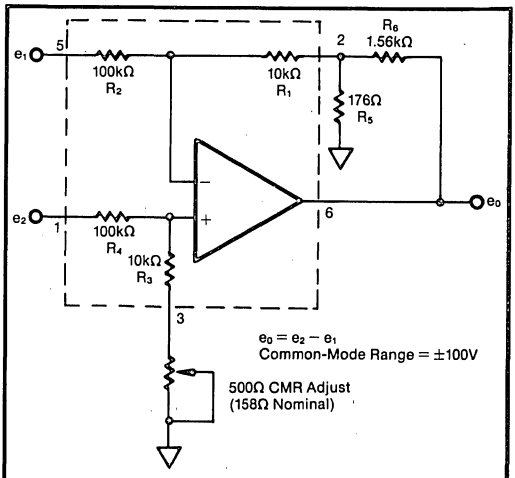
FIGURE 11. Differential-Input, Low-Impedance, Microphone Preamplifier (20dB gain).



Gain = 1/10
Also: Gain = −1/10 by grounding R_4 and driving R_2
Gain = 1/10 differential driving both R_2 and R_4.

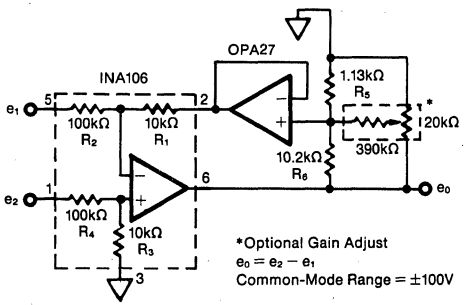
The 100Ω, 10Ω, 0.22µF network on the output assures stability by inserting a 70kHz zero and 700kHz pole to decrease the loop gain by 10 at 700kHz. With the output taken at the junction of the 100Ω and 10Ω resistors, gain accuracy is maintained, and noise gain at the output remains at unity. For a 10V output swing, the load should be limited to 10kΩ since the 100Ω resistor acts as a voltage divider with the load. Also the large signal bandwidth will be limited by the ability of the amplifier to slew into the 0.22µF capacitor. Assuming 10mA output current and a 20Vp-p output signal, the full power bandwidth will be 1.0kHz. Since the circuit is a 10/1 attenuator, this would assume a 200Vp-p input signal. With a 20Vp-p input signal, the bandwidth would be 10kHz.

FIGURE 12. Precision Attenuator.



The addition of two external resistors and a pot turns the INA106 into a unity-gain difference amplifier with input common-mode range exceeding ±100V. The circuit requires CMR adjustment and has a 2% gain accuracy. Better gain accuracy is difficult to obtain, since CMR and gain adjustments interact. See Figure 14.

FIGURE 13. ±100V Common-Mode Range Difference Amplifier.



The addition of an op amp to circuit of Figure 13 can eliminate the need for CMR and gain adjustments. CMR will be 20dB lower than that of the INA106, which is specified in a gain of 10. Gain accuracy is set strictly by the R_5, R_6 ratio and the initial gain accuracy of the INA106 ($A = 1 + R_6/R_5 \pm .01\%$). CMR can be adjusted by adding a 10Ω resistor in series with R_1 (pin 2) and a 20Ω pot in series with R_3 (pin 2). Gain and CMR adjustments do not interact.

FIGURE 14. ±100V Common-Mode Range Difference Amplifier Requiring No Adjustments.

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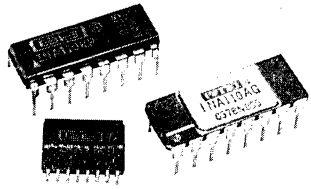


INA110

Fast-Settling FET-Input Very High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- LOW BIAS CURRENT: 50pA, max
- FAST SETTLING: 4μs to 0.01%
- HIGH CMR: 106dB, min; 90dB at 10kHz
- CONVENIENT INTERNAL GAINS: 1, 10, 100, 200, 500
- VERY-LOW GAIN DRIFT: 10 to 50ppm/°C
- LOW OFFSET DRIFT: 2μV/°C
- LOW COST
- PINOUT COMPATIBLE WITH AD524 AND AD624, allowing upgrading of many existing applications

APPLICATIONS

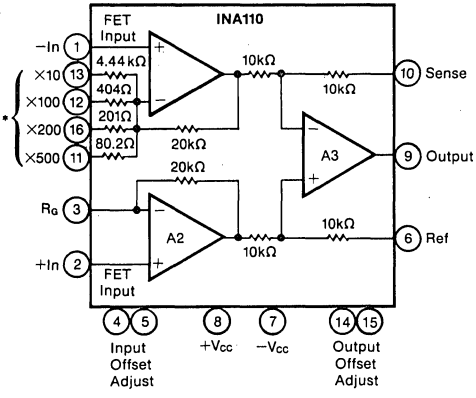
- Fast scanning rate multiplexed input data acquisition system amplifier
- Fast differential pulse amplifier
- High speed, low drift gain block
- Amplification of low level signals from high impedance sources and sensors
- Instrumentation amplifier with input low pass filtering using large series resistors
- Instrumentation amplifier with overvoltage input protection using large series resistors
- Amplification of signals from strain gauges, thermocouples, and RTDs

DESCRIPTION

The INA110 is a monolithic FET input instrumentation amplifier with a maximum bias current of 50pA. The circuit provides fast settling of 4μs to 0.01%. Laser trimming guarantees exceptionally good DC performance. Voltage noise is low, and current noise is virtually zero. Internal gain set resistors guarantee high gain accuracy and low gain drift. Gains of 1, 10, 100, 200, and 500 are provided.

The inputs are inherently protected by P-channel FETs on each input. Differential and common-mode voltages should be limited to ±Vcc. When severe overvoltage exists, use diode clamps as shown in the application section.

The INA110 is ideally suited for applications requiring large input resistors for overvoltage protection or filtering. Input signals from high source impedances can easily be handled without degrading DC performance. Fast settling for rapid scanning data acquisition systems is now achievable with one component, the INA110.



* Connect to Rg for desired gain.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC, R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	INA110AG			INA110BG/SG			INA110KP/KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Range of Gain		1		800	*		*	*		*	V/V
Gain Equation[1]						G = 1 + [40K/(R_G + 50Ω)]					V/V
Gain Error, DC: G = 1			0.002	0.04		*	0.02		*	*	%
G = 10			0.01	0.1		0.005	0.05		*	*	%
G = 100			0.02	0.2		0.01	0.1		*	*	%
G = 200			0.04	0.4		0.02	0.2		*	*	%
G = 500			0.1	1.0		0.05	0.5		*	*	%
Gain Temp. Coefficient: G = 1			±3	±20		*	±10		*		ppm/°C
G = 10			±4	±20		±2	±10		*		ppm/°C
G = 100			±6	±40		±3	±20		*		ppm/°C
G = 200			±10	±60		±5	±30		*		ppm/°C
G = 500			±25	±100		±10	±50		*		ppm/°C
Nonlinearity, DC: G = 1			±0.001	±0.01		±0.0005	±0.005		*	*	% of FS
G = 10			±0.002	±0.01		±0.001	±0.005		*	*	% of FS
G = 100			±0.004	±0.02		±0.002	±0.01		*	*	% of FS
G = 200			±0.006	±0.02		±0.003	±0.01		*	*	% of FS
G = 500			±0.01	±0.04		±0.005	±0.02		*	*	% of FS
OUTPUT											
Voltage, R_L = 2kΩ	Over temp	±10	±12.7		*	*		*	*		V
Current	Over temp	±5	±25		*	*		*	*		mA
Short-Circuit Current			±25			*			*		mA
Capacitive Load	Stability		5000			*			*		pF
INPUT											
OFFSET VOLTAGE[2]											
Initial Offset: G, P			±(100 + 1000/G)	±(500 + 5000/G)		±(50 + 600/G)	±(250 + 3000/G)		*	*	μV
U									±(200 + 2000/G)	±(1000+ 5000/G)	μV
vs Temperature			±(2 + 20/G)	±(5 + 100/G)		±(1 + 10/G)	±(2 + 50/G)		*		μV/°C
vs Supply	V_{CC} = ±6V to ±18V		±(4 + 60/G)	±(30 + 300/G)		±(2 + 30/G)	±(10 + 180/G)		*	*	μV/V
BIAS CURRENT											
Initial Bias Current	Each input		20	100		10	50		*	*	pA
Initial Offset Current			2	50		1	25		*	*	pA
Impedance: Differential			5×10^{12}||6			*			*		Ω||pF
Common-Mode			2×10^{12}||1			*			*		Ω||pF
VOLTAGE RANGE	V_{IN} Diff. = 0V[3]										
Range, Linear Response		±10	±12					*	*		V
CMR with 1kΩ Source Imbalance:											
G = 1	DC	70	90		80	100		*	*		dB
G = 10	DC	87	104		96	112		*	*		dB
G = 100	DC	100	110		106	116		*	*		dB
G = 200	DC	100	110		106	116		*	*		dB
G = 500	DC	100	110		106	116		*	*		dB
NOISE, Input[4]											
Voltage, f_O = 10kHz			10			*			*		nV/√Hz
f_B = 0.1Hz to 10Hz			1			*			*		μVp-p
Current, f_O = 10kHz			1.8			*			*		fA/√Hz
NOISE, Output[4]											
Voltage, f_O = 10kHz			65			*			*		nV/√Hz
f_B = 0.1Hz to 10Hz			8			*			*		μVp-p
DYNAMIC RESPONSE											
Small Signal: G = 1	−3dB		2.5			*			*		MHz
G = 10			2.5			*			*		MHz
G = 100			470			*			*		kHz
G = 200			240			*			*		kHz
G = 500			100			*			*		kHz
Full Power	V_{OUT} = ±10V, R_L = 2kΩ	190	270		*	*			*		kHz
Slew Rate	G = 1 to 100	12	17		*	*			*		V/μs
Settling Time:											
0.1%, G = 1	V_O = 20V step		4			*			*		μs
G = 10			2			*			*		μs
G = 100			3			*			*		μs
G = 200			5			*			*		μs
G = 500			11			*			*		μs

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	INA110AG MIN	INA110AG TYP	INA110AG MAX	INA110BG/SG MIN	INA110BG/SG TYP	INA110BG/SG MAX	INA110KP/KU MIN	INA110KP/KU TYP	INA110KP/KU MAX	UNITS
Settling Time:											
0.01%, G = 1	V_O = 20V step		5	12.5		*	*		*		µs
G = 10			3	7.5		*	*		*		µs
G = 100			4	7.5		*	*		*		µs
G = 200			7	12.5		*	*		*		µs
G = 500			16	25		*	*		*		µs
Overload Recovery[5]	50% overdrive		1			*			*		µs
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±6		±18	*		*	*		*	V
Quiescent Current	V_O = 0V		±3.0	±4.5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: A, B, K		−25		+85	*		*	0		+70	°C
S					−55		+125				°C
Operation		−55		+125	*		*	−25		+85	°C
Storage		−65		+150	*		*	−40		+85	°C
θ_{JA}			100			*			*		°C/W

* Same as INA110AG.

NOTES: (1) Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 11, 12, and 16. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. (2) Adjustable to zero. (3) For differential input voltage other than zero, see Typical Performance Curves. (4) $V_{NOISE\ RTI} = \sqrt{V_{N\ INPUT}^2 + (V_{N\ OUTPUT}/Gain)^2}$. (5). Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

ORDERING INFORMATION

INA110 X X

Basic Model Number

Performance Grade Code
- A, B: −25°C to +85°C
- S: −55°C to +125°C
- K: 0°C to +70°C

Package Code
- G: 16-Pin Hermetic DIP
- P: 16-Pin Plastic DIP
- U: 16-Pin Small Outline Surface Mount

PIN CONFIGURATION

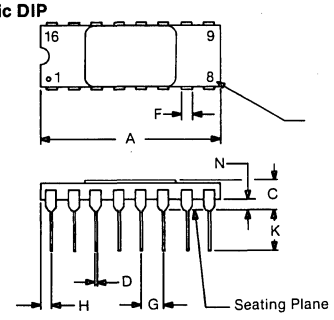
−In	1	16	×200
+In	2	15	Output Offset Adjust
RG	3	14	Output Offset Adjust
Input Offset Adjust	4	13	×10
Input Offset Adjust	5	12	×100
Reference	6	11	×500
−Vcc	7	10	Output Sense
+Vcc	8	9	Output

ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18V
Input voltage Range ..... ±Vcc
Operating Temperature Range: G..... −55°C to +125°C
P, U..... −25°C to +85°C
Storage Temperature Range: G ..... −65°C to +150°C
P, U ..... −40°C to +85°C
Lead Temperature (soldering 10s): G, P..... +300°C
(soldering 3s): U..... +260°C
Output Short-Circuit Duration ..... Continuous to Common

MECHANICAL

Hermetic DIP

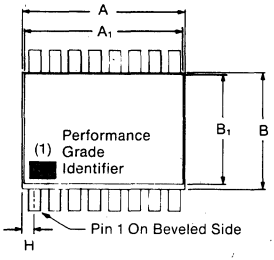


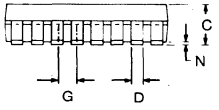
NOTE: Leads in true position within .010" (.25mm) R at seating plane.

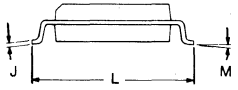
Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

Small Outline Surface Mount





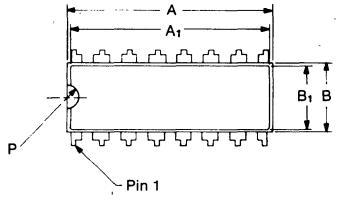


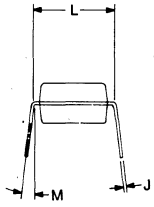
NOTE: Leads in true position within 0.010" (.25mm) R at MMC at seating plane.

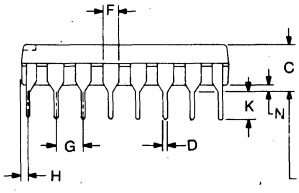
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.400	.416	10.16	10.57
A_1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B_1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

(1) Performance grade identifier box for small outline surface mount. Blank indicates K grade. Part is marked INA110U.

Plastic DIP







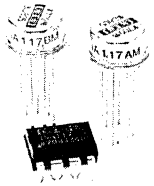
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CASE: Plastic

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.740	.800	18.80	20.32
A_1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.02	0.05	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

BURR-BROWN®



INA117

ADVANCE INFORMATION
Subject to Change

Precision High Common-Mode Voltage Unity-Gain DIFFERENTIAL AMPLIFIER

FEATURES

- HIGH COMMON-MODE RANGE: ±200VDC OR AC PEAK, continuous
- UNITY GAIN: 0.02% GAIN ERROR, max
- EXCELLENT NONLINEARITY: 0.001% max
- HIGH CMR: 86dB, min
- 8-PIN TO-99 OR PLASTIC DIP
- LOW COST

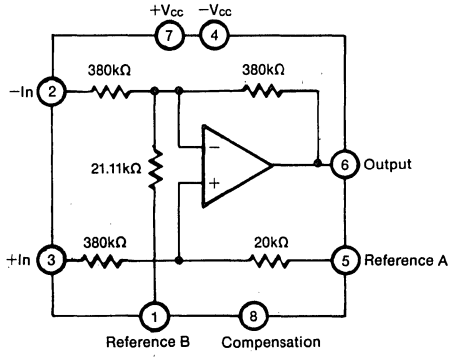
APPLICATIONS

- AC OR DC POWER LINE MONITORING
- TEST EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- GROUND BREAKER
- INDUSTRIAL DATA ACQUISITION SYSTEMS—INPUT BUFFER WITH OVER-VOLTAGE PROTECTION

DESCRIPTION

The INA117 is a precision unity-gain differential amplifier offering an extremely high common-mode input voltage range. As a monolithic circuit, it offers high reliability at low cost. The INA117 consists of a premium grade operational amplifier with an on-chip precision resistor network. In instances where an isolation amplifier is used for its inherent high common-mode capabilities and not for galvanic isolation, the INA117 may be substituted at substantially lower cost, especially since no costly isolation power supply is needed.

The INA117 is completely self-contained and offers the user a highly versatile function. No adjustments to gain, offset or CMR are needed. This provides three important advantages: lower initial design engineering time, lower manufacturing assembly time and cost, and easy, cost-effective field repair of a precision circuit.



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SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted.

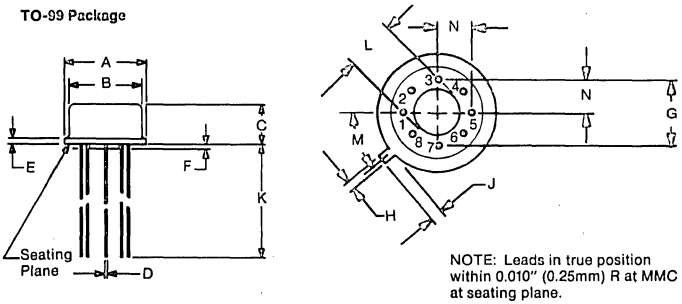
PARAMETER	CONDITIONS	INA117AM			INA117BM			INA117P			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Initial[1]			1			*			*		V/V
Error			0.01	0.05		*	0.02		*	*	%
vs Temperature			2	10			*		*		ppm/°C
Nonlinearity[2]			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, −5mA	10.0	12		*	*		*	*		V
Rated Current	E_O = 10V	+20, −5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To common		+49,								
			−13			*			*		mA
Capacitive Load	Stable operation		1000			*			*		pF
INPUT											
Impedance	Differential		800			*			*		kΩ
	Common-mode		400			*			*		kΩ
Voltage Range	Differential	±10				*			*		V
	Common-mode, continuous	±200			*			*			VDC, ACpk
Common-mode Rejection[3]		74	80		86	94		*	*		dB
vs Temperature: DC	$T_A = T_{MIN}$ to T_{MAX}	66	75		80	90			*		dB
AC, 60Hz		66	80		*	94			*		dB
OFFSET VOLTAGE	RTO[4]										
Initial			120	1000		*	500		*	*	μV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		8.5	40		*	20		*		μV/°C
vs Supply	$\pm V_{CC}$ = 5V to 18V	74	90		80	*		*	*		μV/V
vs Time			200			*			*		μV/mo
OUTPUT NOISE VOLTAGE	RTO[5]										
F_B = 0.01Hz to 10Hz			25			*			*		μV p-p
F_O = 10kHz			550			*			*		nV/√Hz
DYNAMIC RESPONSE											
Gain Bandwidth	−3dB		200			*			*		kHz
Full Power Bandwidth	V_O = 20Vp-p	30			*			*			kHz
Slew Rate		2	2.6		*	*		*	*		V/μs
Settling Time: 0.1%	V_O = 10V step		6.5			*			*		μs
0.01%	V_O = 10V step		10			*			*		μs
0.01%	V_{CM} = 10V step, V_{DIFF} = 0V		4.5			*			*		μs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated performance	±5		±18	*		*	*		*	V
Quiescent Current	V_{OUT} = 0V		1.5	2.0		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		−25		+85	*		*	0		+70	°C
Operation		−55		+125	*		*	−25		+85	°C
Storage		−65		+150	*		*	−40		+85	°C

*Specification same as for INA117AM.

NOTES: (1) Connected as difference amplifier. (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see Offset and CMR section). (4) Includes effects of amplifier's input bias and offset currents. (5) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

MECHANICAL

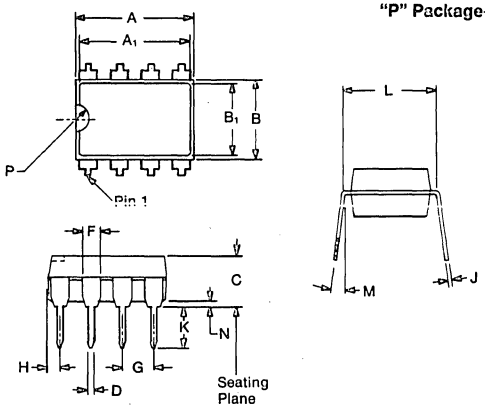
TO-99 Package



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

"P" Package—Plastic DIP

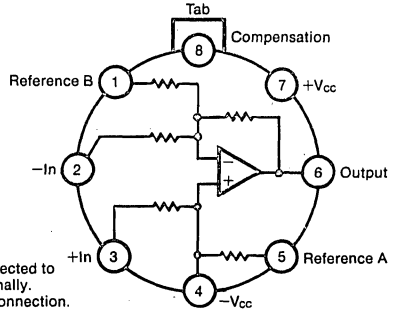


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.355	.400	9.02	10.16
A1	.340	.385	8.64	9.78
B	.230	.290	5.84	7.37
B1	.200	.250	5.08	6.35
C	.120	.200	3.05	5.08
D	.015	.023	0.38	0.58
F	.050	.070	1.27	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.81
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

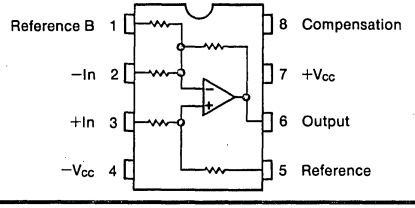
PIN DESIGNATIONS

Top View — Metal TO-99—INA117AM, BM



Case connected to −Vcc internally.
Make no connection.

Top View — Plastic DIP—INA117P



ORDERING INFORMATION

INA117 X X

Basic Model Number

Performance Grade
- A, B: −25°C to +85°C
- None: 0°C to +70°C

Package Code
- M: TO-99 metal can
- P: 8-pin mini plastic DIP

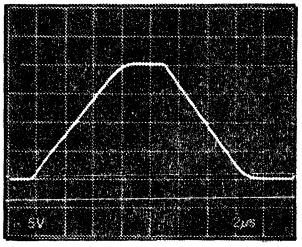
ABSOLUTE MAXIMUM RATINGS

Supply	±22V
Input Voltage Range, Continuous	±200V
Common and Differential, Momentary, 10s	±500V
Operating Temperature Range: M	−55°C to +125°C
P	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (soldering 10s)	+300°C
Output Short Circuit to Common	Continuous

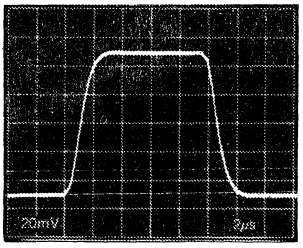
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $\pm V_{CC} = 15V$ unless otherwise noted.

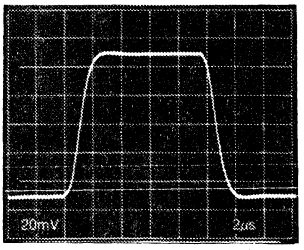
STEP RESPONSE
Pin 8 Grounded, No Load



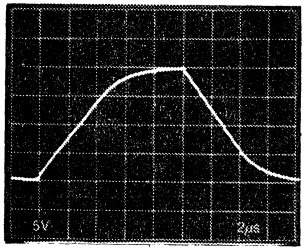
SMALL SIGNAL RESPONSE
No Load



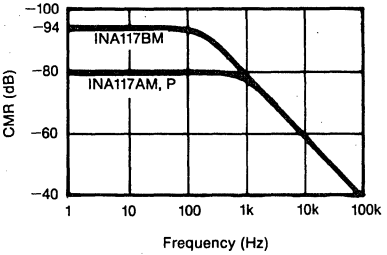
SMALL SIGNAL RESPONSE
$R_L = \infty$, $C_L = 1000pF$



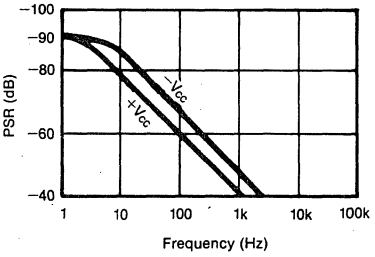
STEP RESPONSE
Pin 8 Ungrounded, No Load



COMMON-MODE REJECTION
VS FREQUENCY



POWER-SUPPLY REJECTION
VS FREQUENCY



DISCUSSION OF SPECIFICATIONS

Refer to Figure 1. Resistor networks at the amplifier input divide the input voltages down to levels suitable for the operational amplifier's common-mode and differential signal capabilities. Feedback around the operational amplifier then restores overall circuit gain to unity for differential signals, while preserving high common-mode rejection.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 also shows the proper connections for power supply and signal. Supplies should be decoupled with 1µF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance.

OFFSET AND COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: resistor matching and tracking (already trimmed in the INA117 for the user) and source impedance.

CMR depends on the accurate matching of several resistor ratios. High accuracies needed to maintain the specified CMR and CMR temperature coefficient are difficult and expensive to reliably achieve with discrete components.

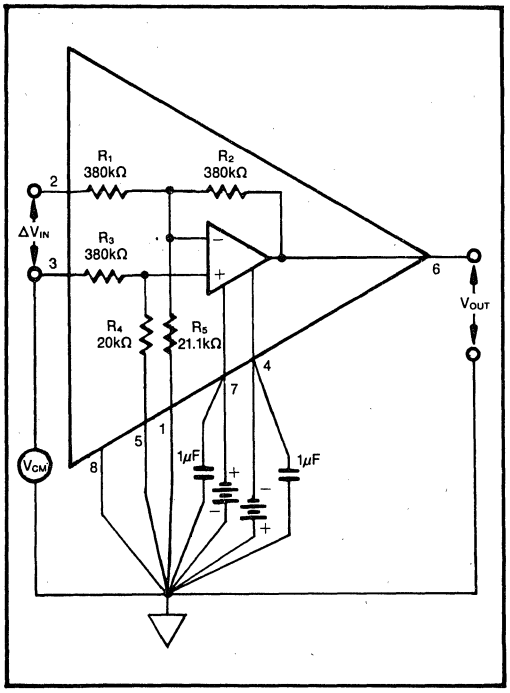


FIGURE 1. Basic Power Supply and Signal Connections.

Any external resistance imbalance adds directly to these resistor ratios. These imbalances can occur either directly in series with R_1 or R_3 or in series with R_4 or R_5. For example, 4Ω added in series with pin 1 or 76Ω in series with pin 2 will degrade CMR from 86dB to 72dB.

When input filters are used preceding an instrumentation amplifier, care should also be taken to match RCs on the two input lines. For example, mismatched input filters for high frequencies will reduce the CMR at lower frequencies, e.g., 60Hz. Differential filters will not degrade AC CMR.

Figures 2a, b, and c show circuitry to allow trim of both CMR and DC offset. Use of these circuits will affect gain accuracy slightly.

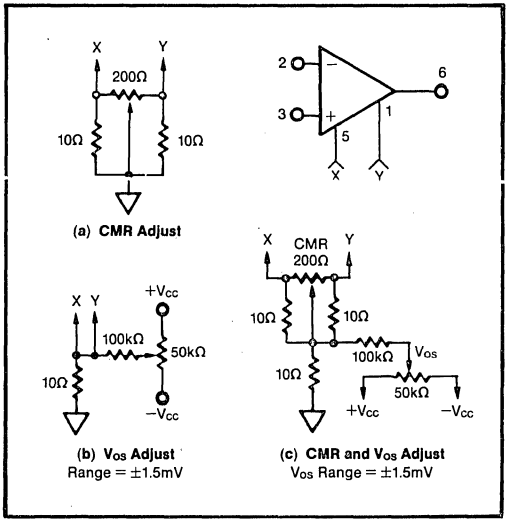


FIGURE 2. CMR and V_{OS} Adjustment.

RESISTOR NOISE IN THE INA117

Figure 3 shows the model for calculating resistor noise in the INA117. Resistors have Johnson noise resulting from thermal agitation. The expression for this noise is:

$$E_{RMS} = \sqrt{2\pi KTRB}$$

Where: K = Boltzman's constant (J/°K)
T = Absolute temperature (°K)
R = Resistance (Ω)
B = Bandwidth (Hz)

At room temperature, this noise becomes:

$$E_N = 1.3 \times 10^{-10} \sqrt{R} \quad (V/\sqrt{Hz})$$

The two noise sources in Figure 3 are:

$$E_{N1} = 1.3 \times 10^{-10} \sqrt{R_5} \quad (V/\sqrt{Hz})$$
$$E_{N2} = 1.3 \times 10^{-10} \sqrt{R_4} \quad (V/\sqrt{Hz})$$

Referred to output,

$$E_{NO1} = E_{N1} (R_2/R_5)$$
$$E_{NO2} = E_{N2} [(R_2/R_1 \parallel R_5) + 1]$$

Adding as the root of the sums squared:

$$E_{NO} = \sqrt{E_{NO1}^2 + E_{NO2}^2} \quad (V/\sqrt{Hz})$$

E_{NO} at a 200kHz bandwidth
= 0.27mVrms
= 1.6mVp-p with a crest factor of 6 (statistically includes 99.7% of all noise peak occurrences)

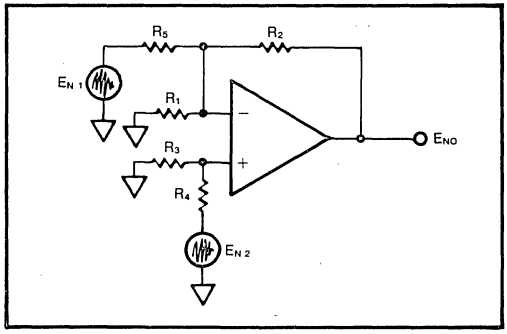


FIGURE 3. Resistor Noise Model.

USE OF THE COMPENSATION TERMINAL (Pin 8)

The design of the INA117 involves use of large-area resistors, resulting in relatively large distributed capacitances between the resistors and the underlying epitaxial layer. To preserve circuit stability, it is necessary to minimize this capacitive effect on R_2. Figure 4 shows a simplified equivalent circuit diagram. Careful layout of the epitaxial layer matches the voltage gradients across R_2 and the epitaxial layer when pin 8 is grounded, minimizing the distributed capacitive effects. The epitaxial bulk resistance represents a DC load of about 15kΩ on the amplifier output when pin 8 is grounded. If pin 8 is left ungrounded, distributed capacitance to AC ground is still reduced, but a net shunt capacitance remains. This effect can be used to advantage in some circuits; the bandwidth of the INA117 in the unity-gain differential amplifier configuration is reduced from 200kHz to 80kHz typically, and results in an output noise voltage reduction by a factor of 1.6. If the INA117 is used in other circuit configurations, the effects of the shunt capacitance should be carefully evaluated.

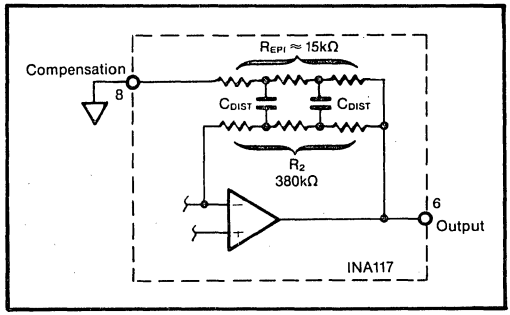


FIGURE 4. Simplified Equivalent Circuit Diagram.

APPLICATIONS CIRCUITS

The INA117 is ideally suited for a wide range of circuit functions. The following figures show many applications circuits.

BATTERY CELL MONITOR

Batteries are often charged in series. The INA117 is ideal for directly monitoring the condition of each cell. Operating range is up to ±200V, and differential fault conditions in this range will not damage the amplifier. Since the INA117 requires no isolated front-end power, cost per cell is very low.

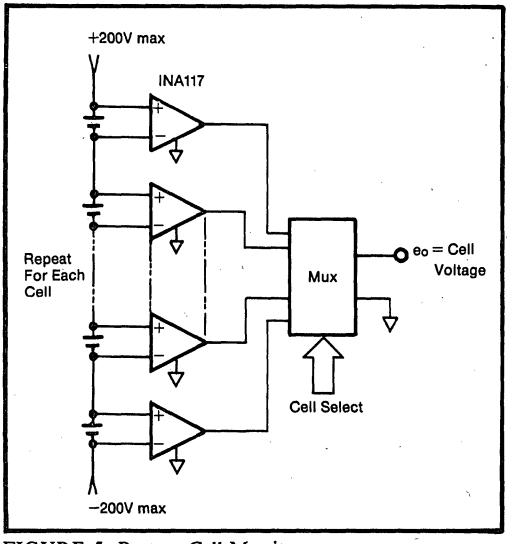


FIGURE 5. Battery Cell Monitor.

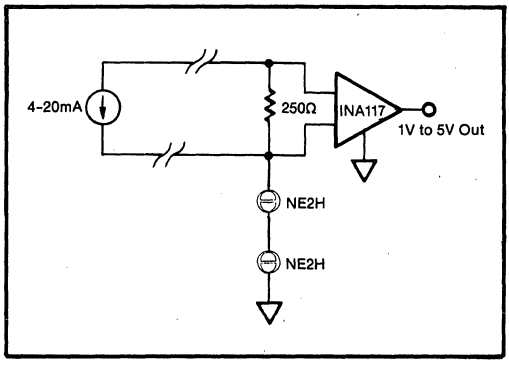


FIGURE 6. 4–20mA Current Receiver.

LEAKAGE CURRENT TEST MONITOR

When the return path is not independently available, leakage current must be measured in series with the input. When the 400kΩ input impedance of the INA117 is too low, a buffer amplifier may be added to the front end. In this example, an OPA128 electrometer-grade operational amplifier is used. The 1kΩ and 9kΩ feedback resistors set a noninverting gain of 10. Bias current of the amplifier is less than 75fA. The diodes and 100kΩ resistor protect the amplifier from 200V short circuit fault conditions.

Since common-mode rejection is the ratio of common-mode gain to differential gain, CMR is boosted. The 20dB gain of the OPA128 added to the 86dB CMR of the INA117 results in a total CMR of 106dB minimum.

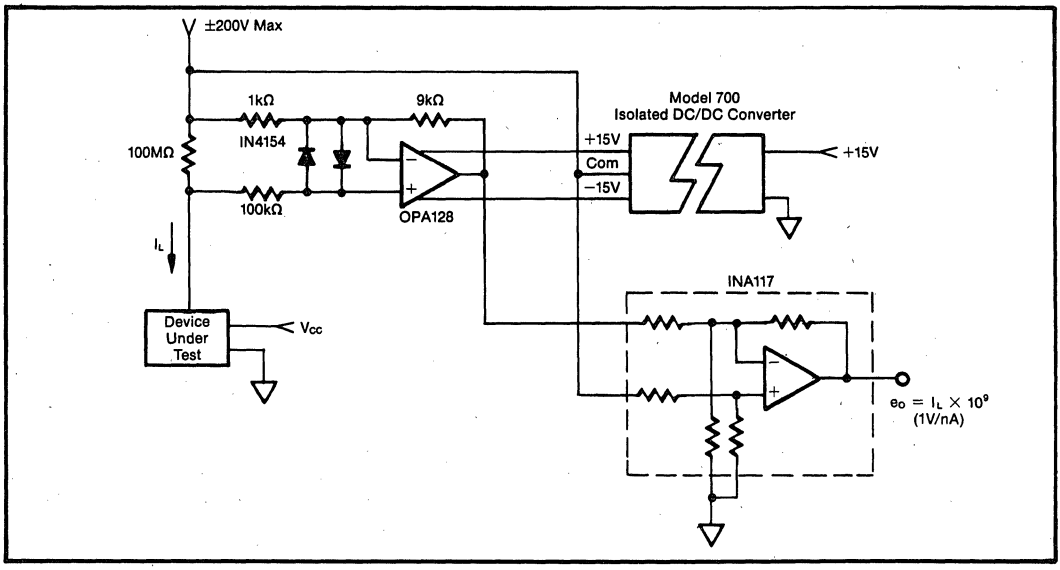


FIGURE 7. Leakage Current Monitor.

BRIDGE AMPLIFIER LOAD CURRENT MONITOR

Bridge amplifiers are popular because they double the voltage swing possible across the load with any given power supply. In this circuit A_1 and A_2 form a bridge amplifier driving a load. A_1 is connected as a follower and A_2 as an inverter.

At low frequencies, a sense resistor could be inserted in series with the load and an instrumentation amplifier used to directly monitor the load current. Under high frequency or transient conditions, CMR errors limit the accuracy of this approach. An alternate approach is to measure the power amplifier supply currents. To understand how it works, notice that since essentially no current flows in the amplifier inputs, $I_{LOAD} = I_1 - I_2$.

A_3 and A_4 are INA117s used to monitor A_1 supply currents I_1 and I_2 across sense resistors R_1 and R_2. Since the INA117 has a ±200V CMV range, the inputs (pins 2 and 3) can be tied to $\pm V_{CC}$ as long as the differential input is less than 10V.

If $R_1 = R_2 = R$
then $e_1 = I_1 \times R$
$e_2 = -I_2 \times R$
and $e_1 + e_2 = I_{LOAD} \times R$

A_5 is an INA105 difference amplifier connected as a noninverting summing amplifier with a gain of 5. The accurate matching of the two 25kΩ input resistors makes a very accurate summing amplifier.

$e_O = 5\ (e_1 + e_2) = 5\ (I_{LOAD} \times R)$
since $R = 0.2\Omega$
$e_O = I_{LOAD}\ (1V/A)$

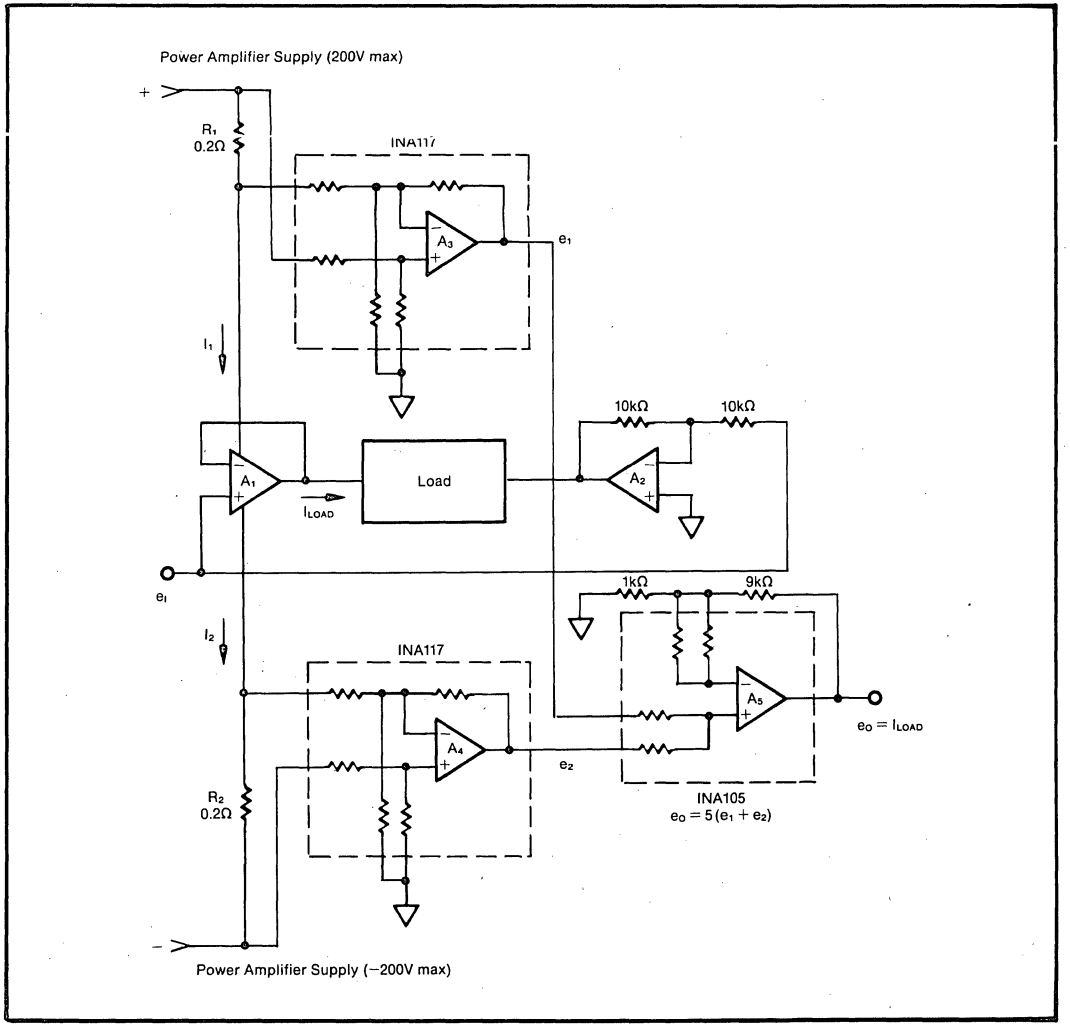


FIGURE 8. Bridge Amplifier Load Current Monitor.

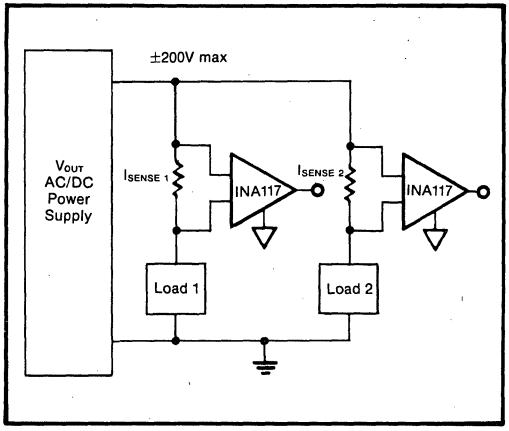


FIGURE 9. Power Supply Current Monitor.

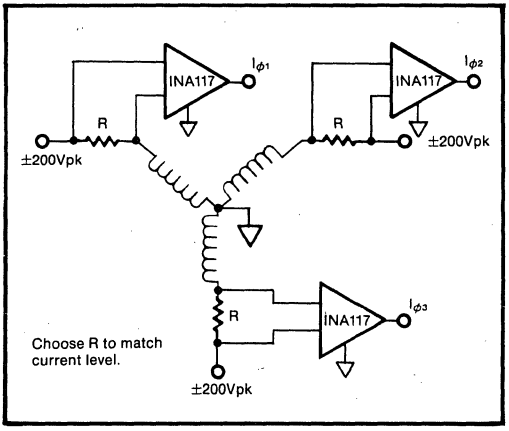


FIGURE 11. Three-Phase Current Monitor.

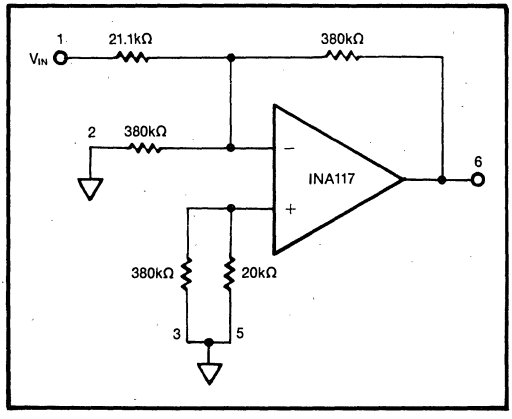


FIGURE 10. Inverting Amplifier, Gain = 18.

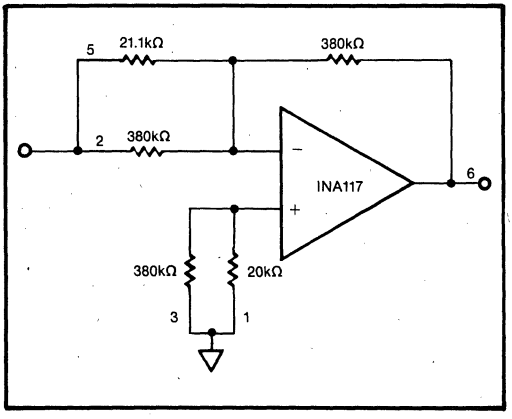


FIGURE 12. Inverting Amplifier, Gain = 19.

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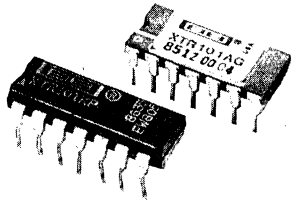


XTR101

Precision, Low Drift 4mA to 20mA TWO-WIRE TRANSMITTER

FEATURES

- INSTRUMENTATION AMPLIFIER INPUT
  - Low Offset Voltage, 30μV max
  - Low Voltage Drift, 0.75μV/°C max
  - Low Nonlinearity, 0.01% max
- TRUE TWO-WIRE OPERATION
  - Power and Signal on One Wire Pair
  - Current Mode Signal Transmission
  - High Noise Immunity
- DUAL MATCHED CURRENT SOURCES
- WIDE SUPPLY RANGE, 11.6V to 40V
- −40°C to +85°C SPECIFICATION RANGE
- SMALL 14-PIN DIP PACKAGE, CERAMIC AND PLASTIC

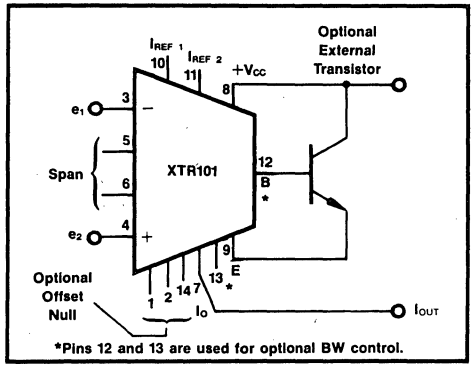
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  - Pressure Transmitters
  - Temperature Transmitters
  - Millivolt Transmitters
- RESISTANCE BRIDGE INPUTS
- THERMOCOUPLE INPUTS
- RTD INPUTS
- CURRENT SHUNT (mV) INPUTS
- PRECISION DUAL CURRENT SOURCES
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR101 is a microcircuit, 4mA to 20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, and dual-matched precision current reference. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTDs, thermistors, and strain gauge bridges. State-of-the-art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications. In addition the optional external transistor allows even higher precision.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers. Also, the XTR101 is generally very useful for low-noise, current-mode signal transmission.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, +V_{CC} = 24VDC, R_L = 100Ω with external transistor connected unless otherwise noted.

PARAMETER	CONDITIONS/DESIGNATION	XTR101AG MIN	XTR101AG TYP	XTR101AG MAX	XTR101BG MIN	XTR101BG TYP	XTR101BG MAX	XTR101AP MIN	XTR101AP TYP	XTR101AP MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS											
Current	Linear Operating Region	4		20	*		*	*		*	mA
	Derated Performance	3.8		22	*		*	*		*	mA
Current Limit			28	38		*	*		31	*	mA
Offset Current Error	I_{OS}, I_O = 4mA		±3.9	±10		±2.5	±6		±8.5	±19	μA
vs Temperature	$\Delta I_{OS}/\Delta T$		±10.5	±20		±8	±15		±10.5	±20	ppm, FS/°C
Full Scale Output Current Error	Full Scale = 20mA		±20	±40		±15	±30		±30	±60	μA
Power Supply Rejection		110	125		*	*		*	122		dB
Power Supply Voltage	V_{CC}, pins 7 and 8, compliance[1]	+11.6		+40	*		*	*		*	VDC
Load Resistance	At V_{CC} = +24V, I_O = 20mA			600			*			600	Ω
	At V_{CC} = +40V, I_O = 20mA			1400			*			1400	Ω
SPAN											
Output Current Equation	R_S in Ω, e_1 and e_2 in V			$i_O = 4mA + [0.016\text{Ω} + (40/R_S)] (e_2 - e_1)$							
Span Equation	R_S in Ω			$S = [0.016\text{Ω} + (40/R_S)]$							A/V
vs Temperature	Excluding TCR of R_S		±30	±100		*	*		*	*	ppm/°C
Untrimmed Error[2]	ε_{SPAN}	−5	−2.5	0	*	*	*	*	*	*	%
Nonlinearity	$\varepsilon_{NONLINEARITY}$			0.01			*			*	%
Hysteresis			0			*			*		%
Dead Band			0			*			*		%
INPUT CHARACTERISTICS											
Impedance: Differential			0.4 ‖ 3			*			*		GΩ ‖ pF
Common-Mode			10 ‖ 3			*			*		GΩ ‖ pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)$ [3]	0		1	*		*	*		*	V
Offset Voltage	V_{OS}		±30	±60		±20	±30		*	±100	μV
vs Temperature	$\Delta V_{OS}/\Delta T$		±0.75	±1.5		±0.35	±0.75		*	*	μV/°C
Bias Current	I_B		60	150		*	*		*	*	nA
vs Temperature	$\Delta I_B/\Delta T$		0.30	1		*	*		*	*	nA/°C
Offset Current	I_{OSI}		10	±30		*	±20		*	*	nA
vs Temperature	$\Delta I_{OSI}/\Delta T$		0.1	0.3		*	*		*	*	nA/°C
Common-Mode Rejection[4]	DC	90	100		*	*		*	*		dB
Common-Mode Range	e_1 and e_2 with respect to pin 7	4		6	*		*	*		*	V
CURRENT SOURCES											
Magnitude			1			*			*		mA
Accuracy	V_{CC} = 24V, $V_{PIN\ 8} - V_{PIN\ 10, 11}$ = 19V, R_2 = 5kΩ, Figure 5		±0.06	±0.17		±0.025	±0.075		±0.2	±0.37	%
vs Temperature			±50	±80		±30	±50		*	*	ppm/°C
vs V_{CC}			±3			*			*		ppm/V
vs Time			±8			*			*		ppm/month
Compliance Voltage	With respect to pin 7	0		V_{CC} − 3.5				*		*	V
Ratio Match	Tracking										
Accuracy	$1 - I_{REF\ 1}/I_{REF\ 2}$		±0.014	±0.06		±0.009	±0.04		±0.031	±0.088	%
vs Temperature				±15			10			*	ppm/°C
vs V_{CC}			±10			*			*		ppm/V
vs Time			±1			*			*		ppm/month
Output Impedance		10	20		*	*		*	15		MΩ
TEMPERATURE RANGE											
Specification		−40		+85	*		*	−40		+85	°C
Operating		−55		+125	*		*	−40		+85	°C
Storage		−55		+165	*		*	−55		+125	°C

*Same as XTR101AG.

NOTES: (1) See Typical Performance Curves. (2) Span error shown is untrimmed and may be adjusted to zero. (3) e_1 and e_2 are signals on the −IN and +IN terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR101A and XTR101B grades respectively. 2mV FS is also possible with the B grade, but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise. (4) Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Application Information section in PDS627.

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} 40V

Input Voltage, e_1 or e_2 ..... $\geq V_{OUT}, \leq +V_{CC}$

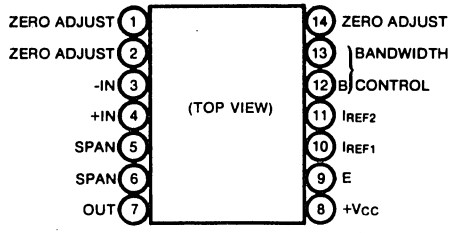
Storage Temperature Range: Ceramic... −55°C to +165°C
Plastic..... −55 to +125°C

Lead Temperature (soldering 10 seconds)..... +300°C

Output Short-Circuit Duration.... Continuous $+V_{CC}$ to I_{OUT}

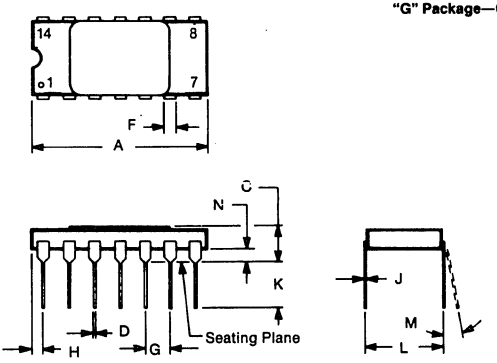
Junction Temperature ..... +165°C

PIN DESIGNATIONS



MECHANICAL

"G" Package—Ceramic DIP

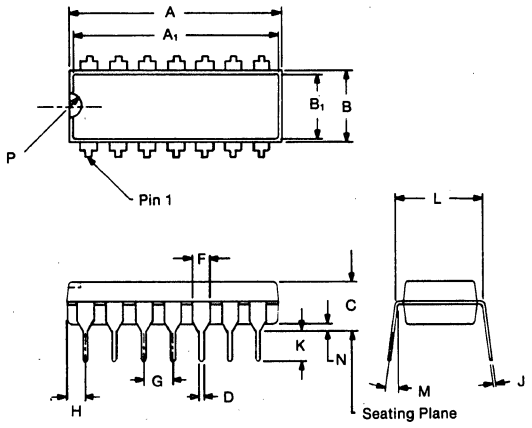


NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

"P" Package—Plastic DIP



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.700	.800	17.78	20.32
A_1	.685	.785	17.40	19.94
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.050	.100	1.27	2.54
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

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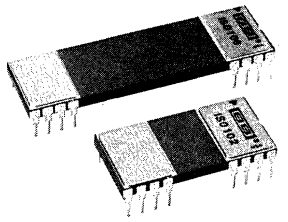


ISO102
ISO106

Low Cost, High Voltage, Wide Bandwidth Standard Hermetic DIP SIGNAL ISOLATION BUFFER AMPLIFIERS

FEATURES

- INDUSTRY'S FIRST HERMETIC ISOLATION AMPLIFIERS AT LOW COST
- EASY-TO-USE COMPLETE CIRCUIT
- RUGGED BARRIER, HV CERAMIC CAPACITORS
- 100% TESTED FOR HIGH VOLTAGE BREAKDOWN
  ISO102: 4000Vrms/10s, 1500Vrms/1min
  ISO106: 8000Vpk/10s, 3500Vrms/1min
- ULTRA HIGH IMR: 125dB min at 60Hz, ISO106
- WIDE INPUT RANGE: −10V to +10V
- WIDE BANDWIDTH: 70kHz
- VOLTAGE REFERENCE OUTPUT: 5VDC

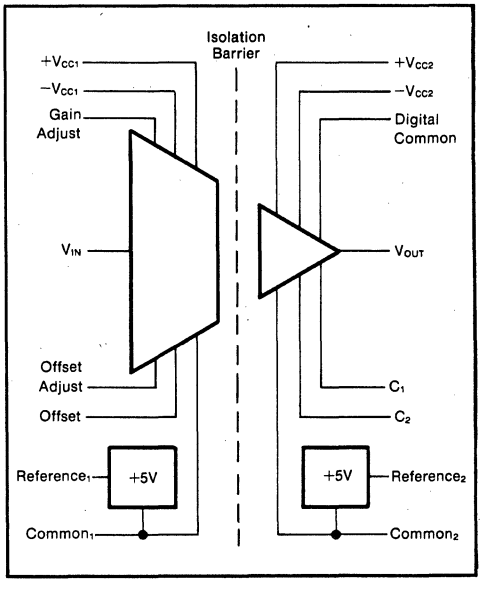
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer channel isolator for thermocouples, RTDs, pressure bridges, flow meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- BIOMEDICAL/ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MILITARY EQUIPMENT

DESCRIPTION

The ISO102 and ISO106 isolation buffer amplifiers are two members of a new series of low cost isolation products from Burr-Brown. They have the same electrical performance and differ only in continuous isolation voltage rating and package length. The ISO102 is rated for 1500Vrms in a 24-pin DIP. The ISO106 is rated for 3500Vrms in a 40-pin DIP. Both side-braze DIPs are 600 mil wide and have industry standard package dimensions with the exception of missing pins between input and output stages. This permits utilization of automatic insertion techniques in production. The three-chip hybrid with its generous high voltage spacing is easy to use (no external components are required).

Each buffer accurately isolates ±10V analog signals by digitally encoding the input voltage and uniquely coupling across a differential ceramic capacitive barrier. This design is nearly immune to variations in the barrier voltage. All elements necessary for operation are contained within the DIP. This provides low cost compact signal isolation in a hermetic package.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC1} = V_{CC2} = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	ISO102, ISO106 MIN	ISO102, ISO106 TYP	ISO102, ISO106 MAX	ISO102B, ISO106B MIN	ISO102B, ISO106B TYP	ISO102B, ISO106B MAX	UNITS
ISOLATION								
Voltage								
Rated Continuous[1]								
ISO102: AC, 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
ISO106: AC, 60Hz	T_{MIN} to T_{MAX}	3500			*			Vrms
DC	T_{MIN} to T_{MAX}	4950			*			VDC
Test Breakdown, AC, 60Hz								
ISO102	10 seconds	4000			*			Vrms
ISO106	10 seconds	8000			*			Vpk
Isolation-Mode Rejection[2]	V_{ISO} = Rated Continuous, 60Hz							
AC: ISO102		115	120		*	*		dB
			1	2		*	*	µVrms/V
ISO106		125	130		*	*		dB
			0.3	0.6		*		µVrms/V
DC		140	160		*	*		dB
			0.01	0.10		*	*	µVDC/V
Barrier Resistance			10^{14}			*		Ω
Barrier Capacitance			6			*		pF
Leakage Current	V_{ISO} = 240Vrms, 60Hz		0.5	1.0		*	*	µArms
GAIN								
Nominal Gain			1			*		V/V
Initial Error[3]			±0.1	±0.25		*	*	% FSR
Gain vs Temperature			±20	±50		±12	±25	ppm FSR/°C
Nonlinearity[4]	V_O = 10V to +10V		±0.04	±0.075		±0.02	±0.025	% FSR
INPUT OFFSET VOLTAGE								
Initial Offset	V_{IN} = 0V		±20	±70		*	*	mV
vs Temperature			±250	±500		±150	±250	µV/°C
vs Power Supplies[5]	Input Stage, V_{CC1} = ±10V to ±20V		3.7			*		mV/V
	Output Stage, V_{CC2} = ±10V to ±20V		−3.7			*		mV/V
INPUT								
Voltage Range	Rated Operation	−10		+10	*		*	V
Resistance		75	100		*	*		kΩ
Capacitive			5			*		pF
OUTPUT								
Voltage Range	Rated Operation	−10		+10	*		*	V
	Derated Operation	−12		+12	*		*	V
Current Drive		±5			*			mA
Short Circuit Current		9	20	50	*	*	*	mA
Ripple Voltage[6]	f = 0.5MHz to 1.5MHz		3			*		mVp-p
Resistance			0.3	1		*	*	Ω
Capacitive Load Drive Capability		10000			*			pF
Overload Recovery Time, 0.1%	$\|V_O\| > 12V$		30			*		µs
OUTPUT VOLTAGE NOISE								
Voltage: f = 0.1Hz to 10Hz			50			*		µVp-p
f = 0.1Hz to 70kHz			16			*		$\mu V/\sqrt{Hz}$
Dynamic Range[7]: f = 0.1Hz to 70kHz	12-bit resolution, 1LSB, 20VFS		74			*		dB
f = 0.1Hz to 280Hz	16-bit resolution, 1LSB, 20VFS		96			*		dB
FREQUENCY RESPONSE								
Small Signal Bandwidth			70			*		kHz
Full Power Bandwidth, 0.1% THD	V_O = ±10V		5			*		kHz
Slew Rate	V_O = ±10V		0.5			*		V/µs
Settling Time, 0.1%	V_O = −10V to +10V		100			*		µs
Overshoot, Small Signal[8]	$C_1 = C_2 = 0$		40			*		%
VOLTAGE REFERENCES								
Voltage Output, Ref1, Ref2	No Load	+4.995	+5.00	+5.005	*	*	*	VDC
vs Temperature			±5	20		*	*	ppm/°C
vs Supplies			10			*		µV/V
vs Load			400	1000		*		µV/mA
Current Output		−0.1		+5	*		*	mA
Short Circuit Current		6	14	30	*	*	*	mA

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	ISO102, ISO106			ISO102B, ISO106B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Rated Voltage, $\pm V_{CC1}$, $\pm V_{CC2}$	Rated Performance		±15			*		V
Voltage Range		±10		±20	*		*	V
Quiescent Current: $+V_{CC1}$	No Load		+11	+15		*	*	mA
$-V_{CC1}$			−9	−12		*	*	mA
$+V_{CC2}$			+25	+33		*	*	mA
$-V_{CC2}$			−15	−20		*	*	mA
Power Dissipation: $\pm V_{CC1}$			300	400		*	*	mW
$\pm V_{CC2}$			600	800		*	*	mW
TEMPERATURE RANGE								
Specification		−25		+85	*		*	°C
Operating[9]		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C
Thermal Resistance, θ_{JA}			40			*		°C/W

* Same as ISO102, ISO106.

NOTES: (1) 100% tested at rated continuous for 1 minute. (2) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. It is a function of frequency as shown in the Typical Performance Curves. This is specified for barrier voltage slew rates not exceeding 100V/μs. (3) Adjustable to zero. FSR = Full Scale Range = 20V. (4) Nonlinearity is the peak deviation of the output voltage from the best fit straight line. It is expressed as the ratio of deviation to FSR. (5) Power Supply Rejection = change in V_{OS}/20V supply change. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Dynamic Range = FSR/(Voltage Spectral Noise Density × square root of User Bandwidth). (8) Overshoot can be eliminated by band-limiting. (9) See Typical Performance Curve E for limitations.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage ..... ±20V
Input Voltage Range ..... ±50V
Continuous Isolation Voltage Across Barrier
ISO102 ..... 1500Vrms
ISO106 ..... 3500Vrms
Junction Temperature..... +160°C
Storage Temperature Range..... −65°C to +150°C
Lead Temperature (soldering 10 seconds) ..... +300°C
Amplifier and Reference Output
Short Circuit Duration ..... Continuous to Common

ORDERING INFORMATION

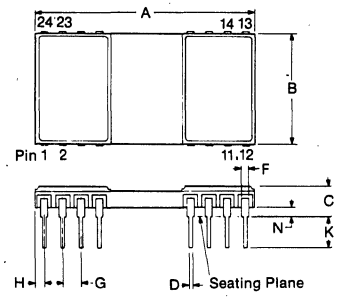
ISO10X X

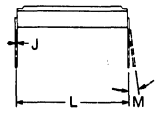
Basic model number
ISO102, ISO106

Performance grade
No designation, B: −25°C to +85°C

MECHANICAL

24-Pin Double-Wide Hermetic DIP **ISO102**





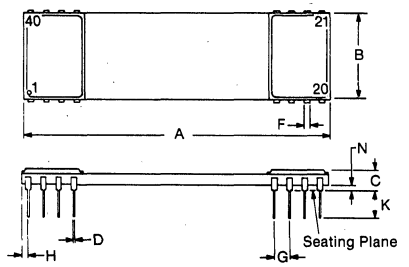
Pin numbers shown for reference only. Numbers may not be marked on package.

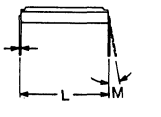
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.190	1.210	30.23	30.73
B	.580	.600	14.73	15.24
C	.140	.185	3.56	4.70
D	.015	.021	0.38	0.53
F	.030	.060	0.76	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

CASE: Ceramic
WEIGHT: 3.7g (0.13oz)

40-Pin Double-Wide Hermetic DIP **ISO106**





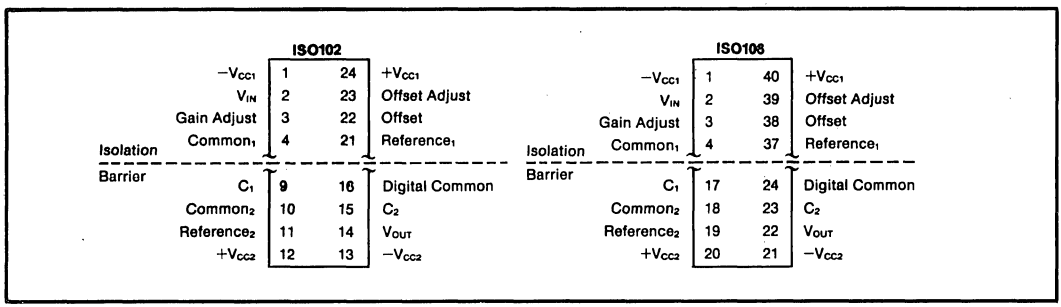
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.980	2.020	50.29	51.31
B	.580	.600	14.73	15.24
C	.140	.185	3.56	4.70
D	.015	.021	0.38	0.53
F	.030	.060	0.76	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

CASE: Ceramic
WEIGHT: 6.2g (0.22oz)

PIN CONFIGURATION



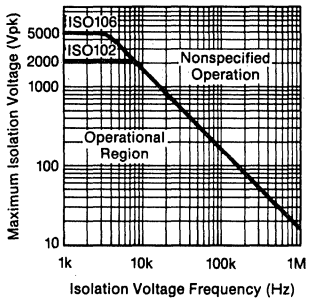
PIN DESCRIPTIONS

$\pm V_{CC1}$, $Common_1$	Positive and negative power supply voltages and common (or ground) for the input stage. $Common_1$ is the analog reference voltage for input signals.
$\pm V_{CC2}$, $Common_2$	Positive and negative power supply voltages and common (or ground) for the ouptut stage. $Common_2$ is the analog reference voltage for output signals. The voltage between $Common_1$ and $Common_2$ is the isolation voltage and appears across the internal high voltage barrier.
V_{IN}	Signal input pin. Input impedance is typically 100kΩ. The input range is rated for ±10V. The input level can actually exceed the input stage supplies. Output signal swing is limited only by the output supply voltages.
Gain Adjust	This pin is an optional signal input. A series 5kΩ potentiometer between this pin and the input signal allows a guaranteed ±1.5% gain adjustment range. When gain adjustment is not required, the Gain Adjust should be left open. Figure 4 illustrates the gain adjustment connection.
$Reference_1$	+5V reference output. This low drift zener voltage reference is necessary for setting the bipolar offset point of the input stage. **This pin must be strapped to either Offset or Offset Adjust to allow the isolation amplifier to function.** The reference is often useful for input signal conditioning circuits. See Typical Performance Curve K for the effect of offset voltage change with reference loading. $Reference_1$ is identical to, but independent of, $Reference_2$. This output is short circuit protected.
$Reference_2$	+5V reference output. This reference circuit is identical to, but independent of, $Reference_1$. It controls the bipolar offset of the output stage through an internal connection. This output is short circuit protected.
Offset	Offset input. **This input must be strapped to $Reference_1$** unless user adjustment of bipolar offset is required.
Offset Adjust	This pin is for optional offset control. When connected to the $Reference_1$ pin through a 1kΩ potentiometer, ±150mV of adjustment range is guaranteed. Under this condition, the Offset pin should be connected to the Offset Adjust pin. When offset adjustment is not required, the Offset Adjust pin is left open. See Figure 4.
Digital Common	Digital common or ground. This separate ground carries currents from the digital portions of the output stage circuit. The best grounding practices require that digital common current does not flow in analog common connections. In most systems the physical connection between analog and digital commons must be at the system power supplies terminal to insure digital noise is kept out of the analog signal. Difference in potentials between the $Common_2$ and Digital Common pins can be ±1V. See Figure 2.
V_{OUT}	Signal output. Because the isolation amplifier has unity gain, the output signal is ideally identical to the input signal. The output is low impedance and is short-circuit-protected.
C_1, C_2	Capacitors for small signal bandwidth control. These pins connect to the internal rolloff frequency controlling nodes of the output low-pass filter. Additional capacitance added to these pins will modify the bandwidth of the buffer. C_2 is always twice the value of C_1. See Typical Performance Curve B for the relationship between bandwidth and C_1 and C_2. When no connections are made to these pins, the full small signal bandwidth is maintained. Be sure to shield C_1 and C_2 pins from high electric fields on the PC board. This preserves AC Isolation Mode Rejection by reducing capacitive coupling effects.

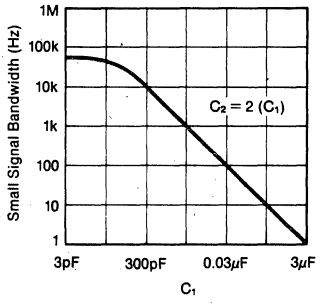
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

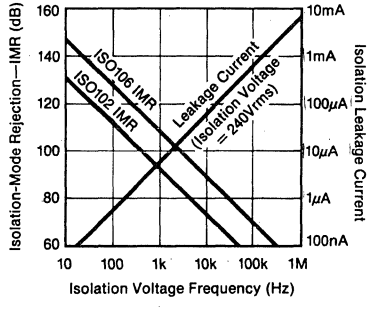
A. RECOMMENDED RANGE OF ISOLATION VOLTAGE



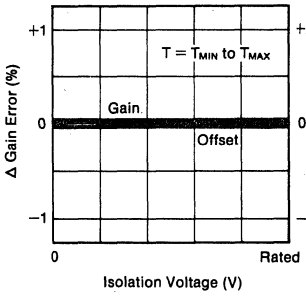
B. BANDWIDTH CONTROL



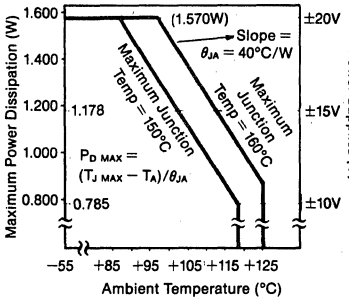
C. IMR/LEAKAGE VS FREQUENCY



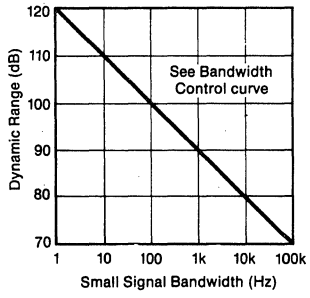
D. GAIN ERROR/OFFSET ISOLATION VOLTAGE



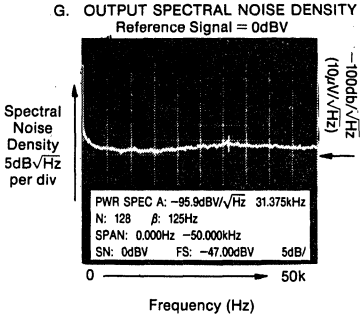
E. POWER DISSIPATION VS TEMPERATURE



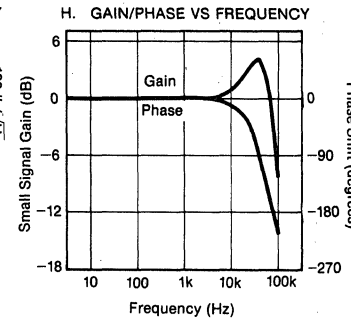
F. DYNAMIC RANGE VS BANDWIDTH



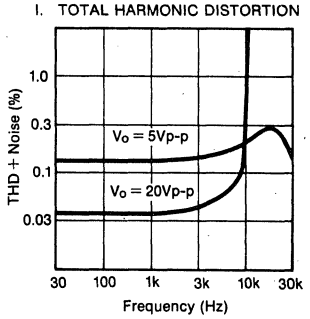
G. OUTPUT SPECTRAL NOISE DENSITY



H. GAIN/PHASE VS FREQUENCY



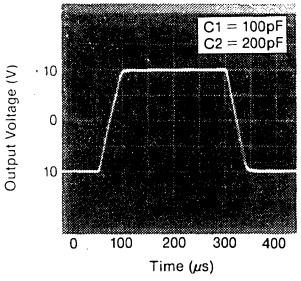
I. TOTAL HARMONIC DISTORTION



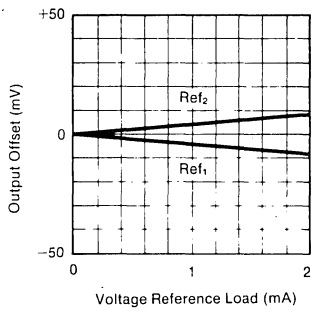
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

J. LARGE SIGNAL TRANSIENT RESPONSE



K. EFFECT OF REFERENCE LOADING ON OFFSET



THEORY OF OPERATION

The ISO102 and ISO106 have no galvanic connection between the input and output. The analog input signal referenced to the input common is accurately duplicated at the output referenced to the output common. Because the barrier information is digital, potentials between the two commons can assume a wide range of voltages and frequencies without influencing the output signal. Signal information remains undisturbed until the slew rate of the barrier voltage exceeds 100V/μs. The amplifier is protected from damage for slew rates up to 100,000V/μs.

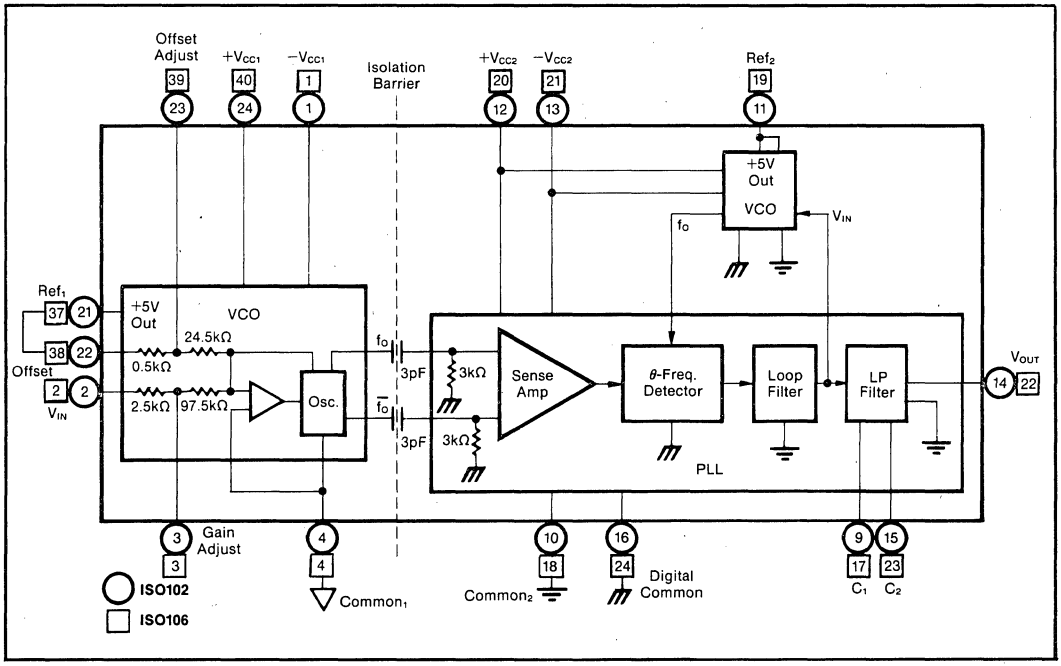


FIGURE 1. Simplified Diagram of ISO102 and ISO106.

A simplified diagram of the ISO102 and ISO106 is shown in Figure 1. The design consists of an input voltage-controlled oscillator (VCO) also known as a voltage-to-frequency converter (VFC), differential capacitors, and output phase lock loop (PLL). The input VCO drives digital levels directly into the two 3pF barrier capacitors. The digital signal is frequency modulated and appears differentially across the barrier while the externally applied isolation voltage appears common-mode.

A sense amplifier detects only the differential information. The output stage decodes the frequency modulated signal by the means of a PLL. The feedback of the PLL employs a second VCO that is identical to the encoder VCO. The PLL forces the second VCO to operate at the same frequency (and phase) as the encoder VCO; therefore, the two VCOs have the same input voltage. The input voltage of the decoder VCO serves as the isolation buffer's output signal after passing through a 100kHz second order active filter.

ABOUT THE BARRIER

For any isolation product, barrier composition is of paramount importance in achieving high reliability. Both the ISO102 and ISO106 utilize two 3pF high voltage ceramic coupling capacitors. They are constructed of tungsten thick film deposited in a spiral pattern on a ceramic substrate. Capacitor plates are buried in the package, making the barrier very rugged and hermetically sealed. Capacitance results from the fringing electric fields of adjacent metal runs. Dielectric strength exceeds 10kV and resistance is typically $10^{14}\Omega$. Input and output circuitry are contained in separate solder-sealed cavities, resulting in the industry's first fully hermetic hybrid isolation amplifier.

The ISO102 and ISO106 are free from partial discharge at rated voltages. Partial discharge is a form of localized breakdown that degrades the barrier over time. Since it does not bridge the space across the barrier, it is difficult to detect. Both isolation amplifiers have been extensively evaluated at high temperature and high voltage.

POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 2 shows the proper power supply and signal connections. Each supply should be AC-bypassed to Analog Common with 0.1μF ceramic capacitors as close to the amplifier as possible. Short leads will minimize lead inductance. A ground plane will also reduce noise problems. Signal common lines should tie directly to the common pin if a low impedance ground plane is not used. Refer to Digital Common in the Pin Descriptions table.

To avoid gain and isolation-mode rejection (IMR) errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Any capacitance across the barrier will increase AC leakage current and may degrade high frequency IMR. The schematic in Figure 3 shows the proper technique for wiring analog and digital commons together.

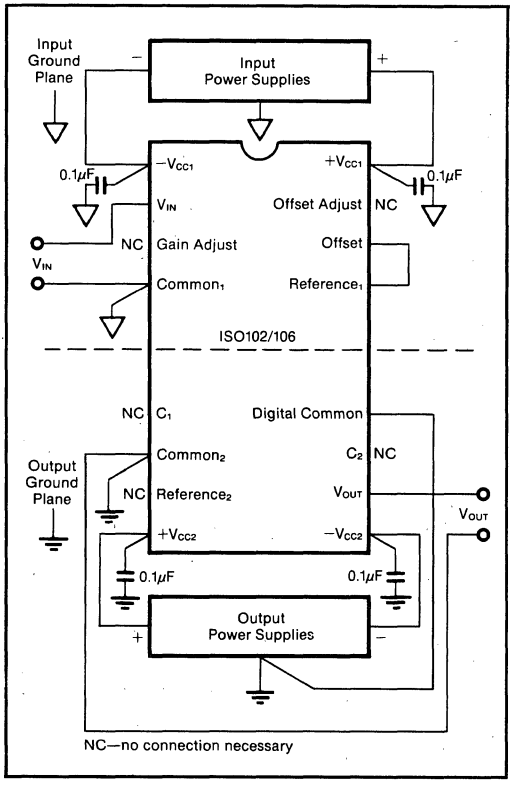


FIGURE 2. Power Supply and Signal Connection for ISO102 and ISO106.

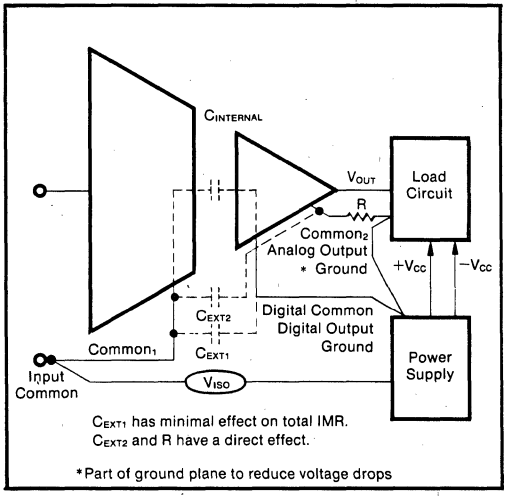


FIGURE 3. Technique for Wiring Analog and Digital Commons Together in the ISO102 and ISO106.

DISCUSSION OF SPECIFICATIONS

The ISO102 and ISO106 are unity gain buffer isolation amplifiers primarily intended for high level input voltages on the order of 1V to 10V. They may be preceded by operational, differential, or instrumentation amplifiers that precondition a low level signal on the order of millivolts and translate it to a high level.

ISOLATION-MODE REJECTION

The ISO102 and ISO106 provide exceptionally high isolation-mode rejection over a wide range of isolation-mode voltages and frequencies. The typical performance curves should be used to insure operation within the recommended range. The maximum barrier voltage allowed decreases as the frequency of the voltage increases. As with all isolation amplifiers, a change of voltage across the barrier will induce leakage current across the barrier. In the case of the ISO102 and ISO106, there exists a threshold of leakage current through the signal capacitors that can cause over-drive of the decoder's sense amplifier. This occurs when the slew rate of the isolation voltage reaches 100V/μs. The output will recover in about 50μs from transients exceeding 100V/μs.

Typical Performance Curve C indicates the expected isolation-mode rejection over a wide range of isolation voltage frequencies. Also plotted is the typical leakage current across the barrier at 240Vrms. The majority of the leakage current is between the input common pin and the output digital ground pin.

The ISO102 and ISO106 are intended to be continuously operated with fully rated isolation voltage and temperature without significant drift of gain and offset. See performance curve D for changes in gain and offset with isolation voltage.

SUPPLY AND TEMPERATURE RANGE

The ISO102 and ISO106 are rated for ±15V supplies; however, they are guaranteed to operate from ±10V to ±20V. Performance is also rated for an ambient temperature range of −25°C to +85°C. For operation outside this temperature range, refer to performance curve E to establish the maximum allowed supply voltage. Supply currents are fairly insensitive to changes in supply voltage or temperature. Therefore, the maximum current limits can be used in computing the maximum junction temperature under nonrated conditions.

OPTIONAL BANDWIDTH CONTROL

The following discussion relates optimum dynamic range performance to bandwidth, noise, and settling time.

The outputs of the ISO102 and ISO106 are the outputs of a second order low-pass Butterworth filter. Its low impedance output is rated for ±5mA drive and ±12V range with 10,000pF loads. The closed-loop bandwidth of the PLL is 70kHz, while the output filter is internally set at 100kHz. The output filter lowers the residual voltage of the barrier FM signal to below the noise floor of the output signal.

Two pins are available for optional modification of the filter's bandwidth. Only two capacitors are required. Performance curve B gives the value of C_1 (C_2 is equal to twice C_1) for the desired bandwidth. Figure 4 illustrates the optional connection of both capacitors.

A tradeoff can be achieved between the required signal bandwidth and system dynamic range. The noise floor of the output limits the dynamic range of the output signal. The noise power varies with the square root of the bandwidth of the buffer. It is recommended that the bandwidth be reduced to about twice the maximum signal bandwidth for optimum dynamic range as shown in performance curve F. The output spectral noise density measurement is displayed in performance curve G. The noise is flat to within 5dB$\sqrt{\text{Hz}}$ between 0.1Hz to 70kHz.

The overall small signal gain of the buffer amplifiers is shown in performance curve H. This assumes no external band-limiting capacitors. The total harmonic distortion for large signal sine wave outputs is plotted in performance curve I. The phase-lock-loop displays slightly nonuniform rise and fall edges under maximum slew conditions. Reducing the output filter bandwidth to below 70kHz smoothes the output signal and eliminates any overshoot. See the settling time performance curve J.

OPTIONAL OFFSET AND GAIN ADJUSTMENT

In many applications the factory-trimmed offset is adequate. For situations where reduced or modified gain and offset are required, adjustment of each is easy. The addition of two potentiometers as shown in Figure 4 provides for a two step calibration.

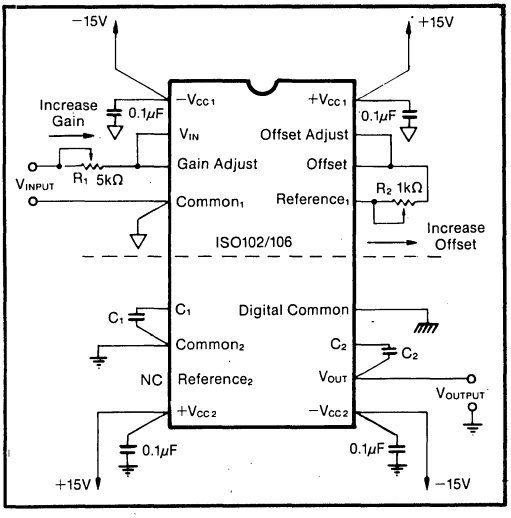


FIGURE 4. Optional Gain Adjust, Offset Adjust, and Bandwidth Control.

Offset should be adjusted first. Gain adjustment does not interfere with offset. The potentiometer's TCR adds only 2% to overall temperature drift.

The offset and gain adjustment procedures are as follows:

1. Set V_{IN} to 0V and adjust R_1 to desired offset at the output.
2. Set V_{IN} to full scale (not zero). Adjust R_2 for desired gain.

PRINTED CIRCUIT BOARD LAYOUT

The distance across the isolation barrier, between external components, and conductor patterns, should be maximized to reduce leakage and arcing at high voltages. Good layout techniques that reduce stray capacitance will assure low leakage current and high AC IMR. For some applications, applying conformal coating compound such as urethane is useful in maintaining good performance. This is especially true where dirt, grease or moisture can collect on the PC board surface, component surface, or component pins. Following this industry-accepted practice will give best results, particularly when circuits are operated or tested in a moisture-condensing environment. Optimum coating can be achieved by administering urethane under vacuum conditions. This allows complete coverage of all areas.

Figure 5 shows the recommended layout of the DEM102 demonstration board. This board contains the ISO102 and PWS725. The PWS725 is a DC-to-DC converter with a rated barrier voltage of 1500Vrms. It provides isolated power for the ISO102's input stage and other input circuitry that may be used. The DEM102 board illustrates the ease of use of these components. Notice that the ISO102's external high voltage spacing is maintained on both sides of the PC board layout. The placement of bypass capacitors, gain and offset potentiometers, and the PWS725's input ripple filter components are shown. The DEM106 layout in Figure 6 is similar to the DEM102. It contains the ISO106 and PWS726, which is rated for 3500Vrms. The schematic of both demonstration boards appears in Figure 7. Boards are available from Burr-Brown to facilitate fast, easy evaluation of electrical and isolation performance.

Isolation-mode rejection can be affected by the PC board layout. The most critical pins for obtaining maximum IMR are C_1 and C_2. These are the only high impedance nodes under normal operation and can be influenced by the barrier's voltage if not shielded. Grounded rings around the C_1 and C_2 contacts on the board greatly reduce high voltage electric fields at these pins. Maximum IMR is achieved when a ground plane is provided on both sides of the C_1, C_2 interconnect.

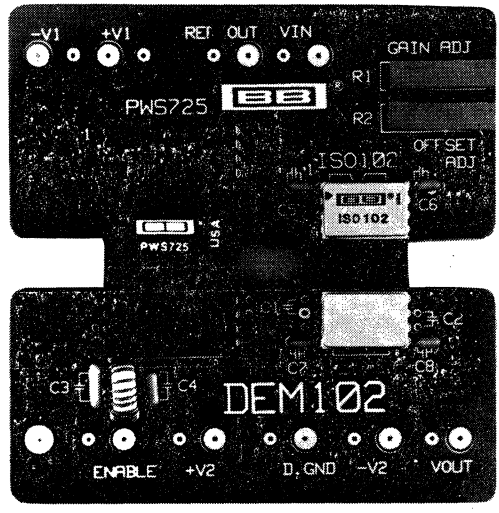


FIGURE 5. Recommended Layout for ISO102 and PWS725 (Demonstration Board DEM102).

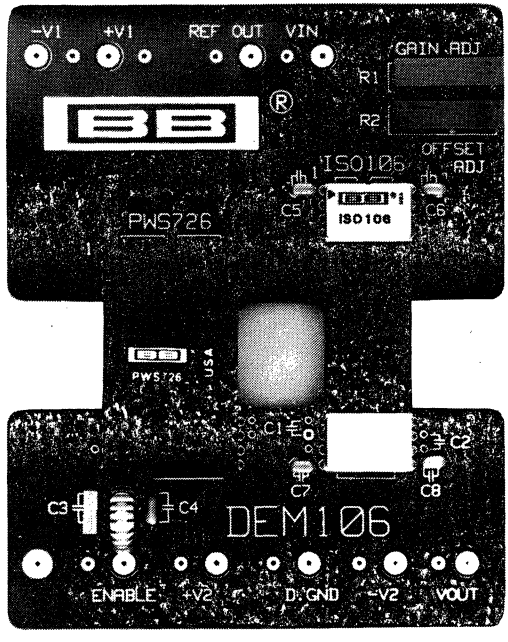


FIGURE 6. Recommended Layout for ISO106 and PWS726 (Demonstration Board DEM106).

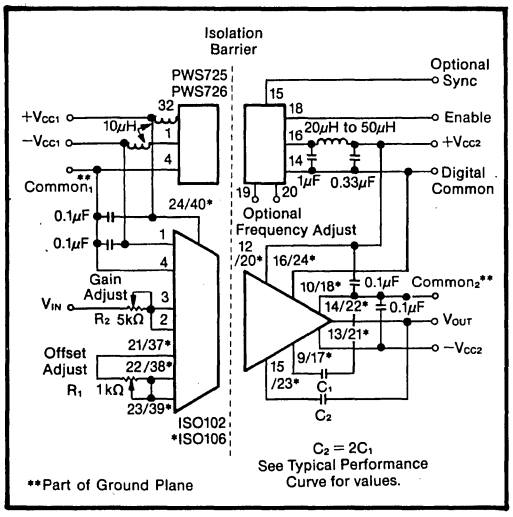


FIGURE 7. Schematic for Layout in Figures 5 and 6.

APPLICATIONS

The ISO102 and ISO106 isolation amplifiers are used in three categories of applications:

1. accurate isolation of signals from high voltage ground potentials,
2. accurate isolation of signals from severe ground noise, and
3. fault protection from high voltages in analog measurement systems.

Figures 8 through 18 show a variety of application circuits.

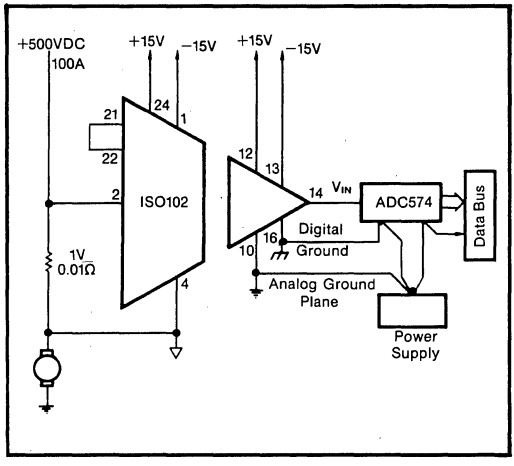


FIGURE 8. Isolated Power Current Monitor for Motor Circuit. (The ISO102 allows reliable safe measurement at high voltages.)

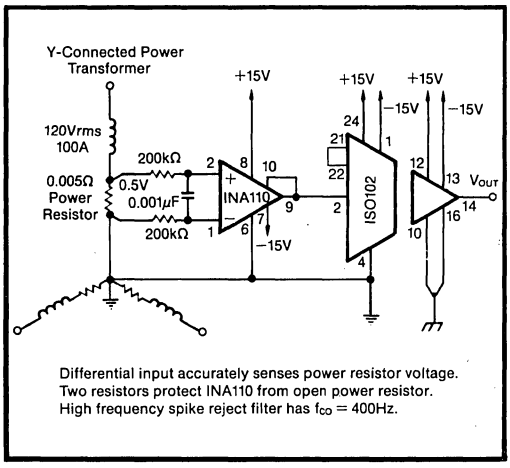


FIGURE 9. Isolated Power Line Monitor (0.5μA leakage current at 120Vrms.)

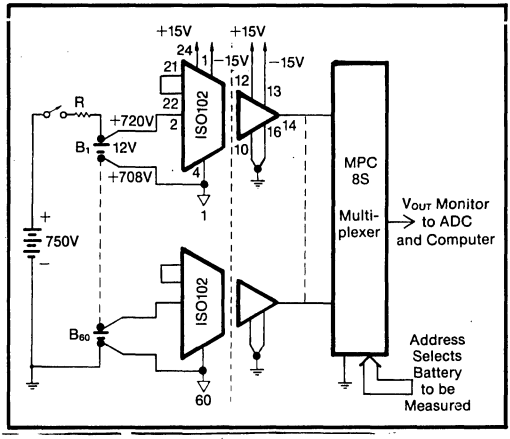


FIGURE 10. Battery Monitor for High Voltage Charging Circuit.

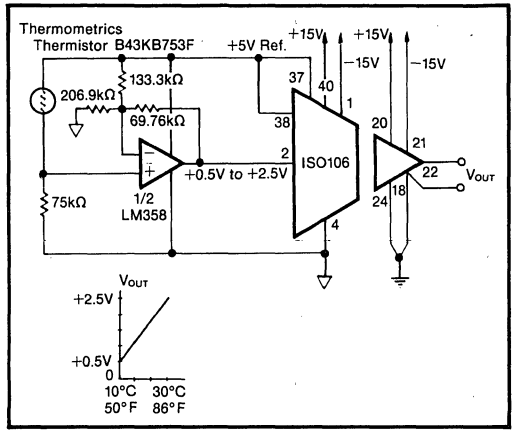


FIGURE 11. Isolated RTD Temperature Amplifier.

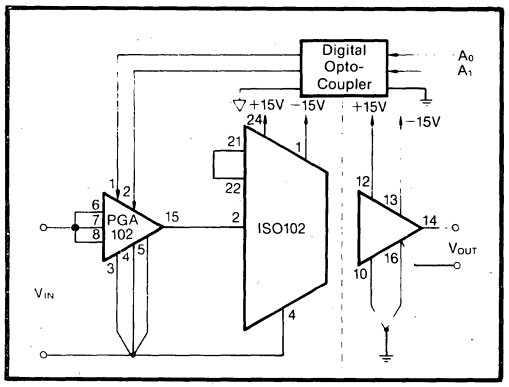


FIGURE 12. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

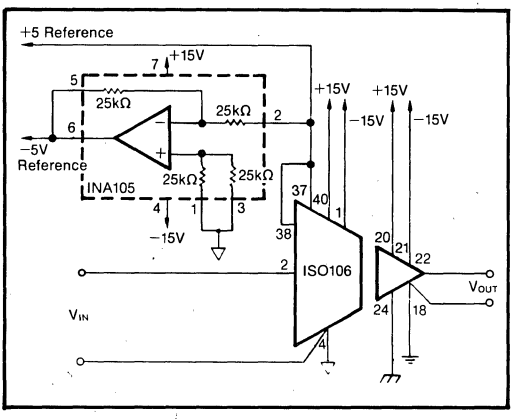


FIGURE 13. Isolation Amplifier with Isolated Bipolar Input Reference.

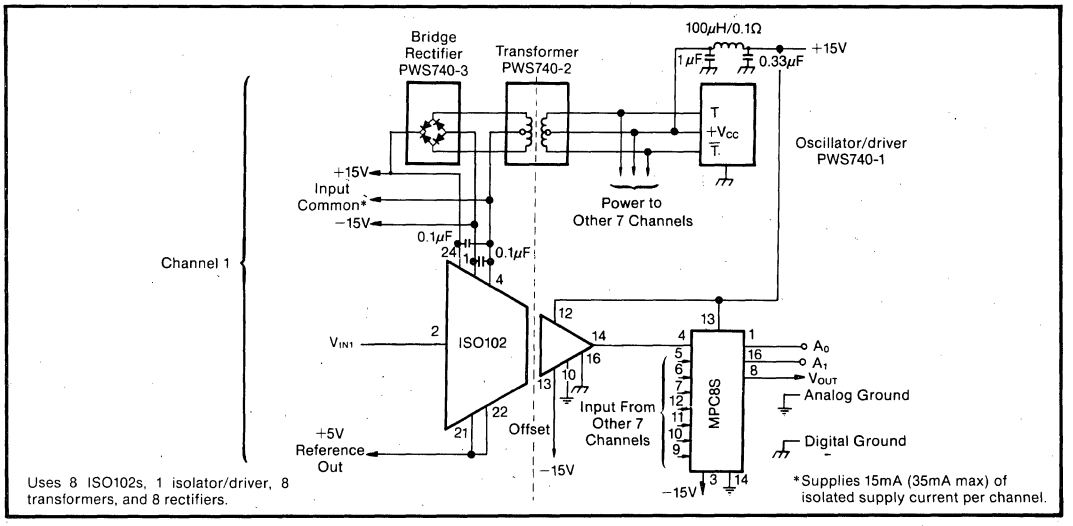


FIGURE 14. Low Cost Eight-Channel Isolation Amplifier Block with Channel-to-Channel Isolation.

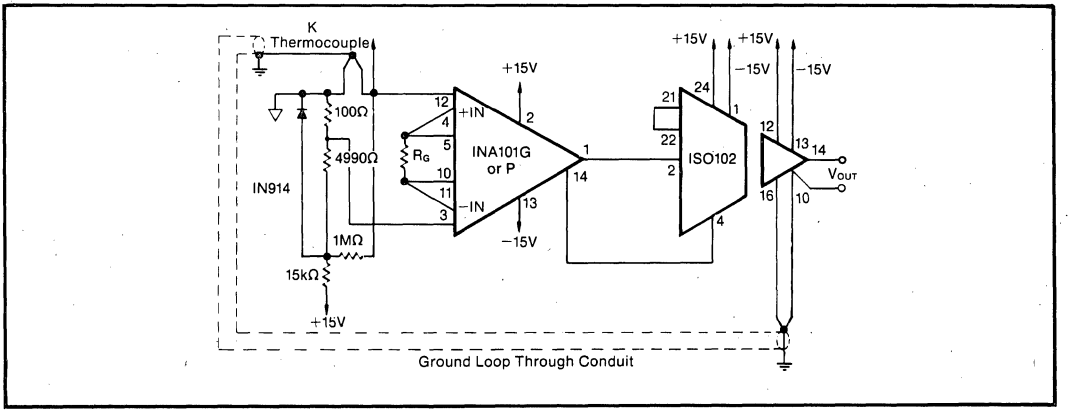


FIGURE 15. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Upscale Burn-out.

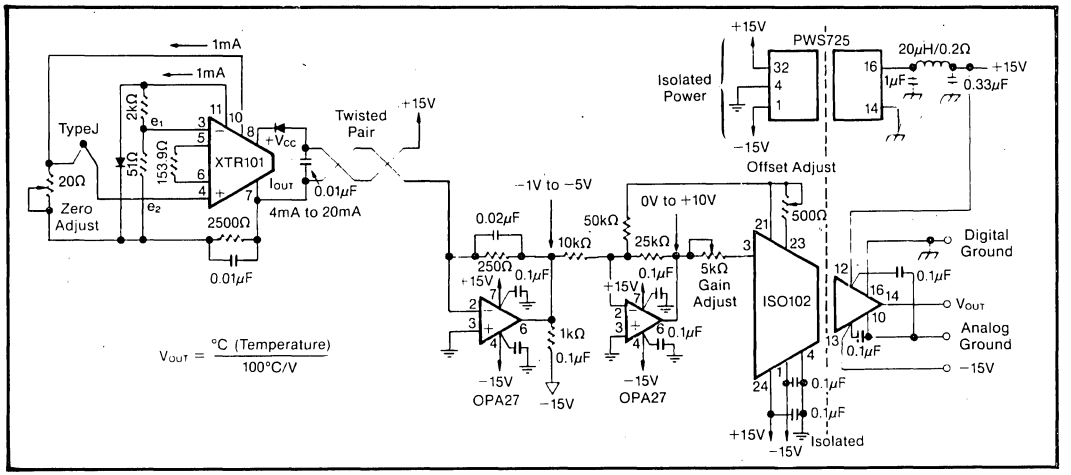


FIGURE 16. Remote Isolated Thermocouple Transmitter with Cold Junction Compensation.

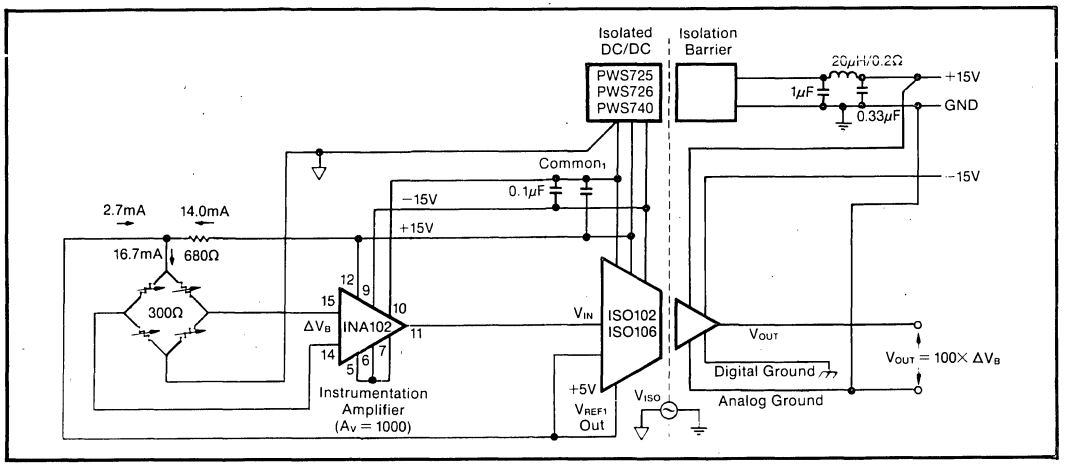


FIGURE 17. Isolated Instrumentation Amplifier for 300Ω Bridge. (Reference voltage from isolation amplifier is used to excite bridge.)

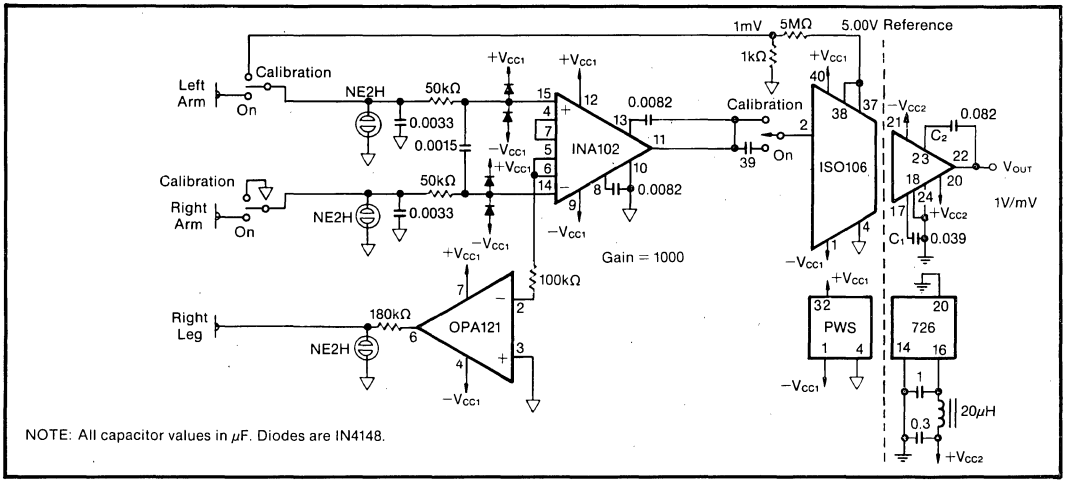


FIGURE 18. Right-Leg Driven ECG Amplifier (with defibrillator protection and calibrator).

AN ERROR ANALYSIS OF THE ISO102 IN A SMALL SIGNAL MEASURING APPLICATION

High accuracy measurements of low-level signals in the presence of high isolation mode voltages can be difficult due to the errors of the isolation amplifiers themselves.

This error analysis shows that when a low drift operational amplifier is used to preamplify the low-level source signal, a low cost, simple and accurate solution is possible.

In the circuit shown in Figure 1, a 50mV shunt is used to measure the current in a 500VDC motor. The OPA27 amplifies the 50mV by 200 × to 10V full scale. The output of the OPA27 is fed to the input of the ISO102, which is a unity-gain isolation amplifier. The 5kΩ and 1kΩ potentiometers connected to the ISO102 are used to adjust the gain and offset errors to zero as described in the ISO102 data sheet.

SOME OBSERVATIONS

The total errors of the op amp and the iso amp combined are approximately 0.6% of full-scale range. If the op amp had not been used to preamplify the signal, the errors would have been 74.4% of FSR. Clearly, the small cost of adding the op amp buys a large performance improvement.

After gain and offset nulling, the dominant errors of the iso amp are gain nonlinearity and power supply rejection. Thus, well regulated supplies will reduce the errors even further.

The RMS noise of the ISO102 with a 120Hz bandwidth is only 0.18mVrms, which is only 0.0018% of the 10V full-scale output. Therefore, even though the $16\mu V/\sqrt{Hz}$ noise spectral density specification may appear large compared to other isolation amplifiers, it does not turn out to be a significant error term. It is worth noting that even if the bandwidth is increased to 10kHz, the noise of the iso amp would only contribute 0.016%FSR error.

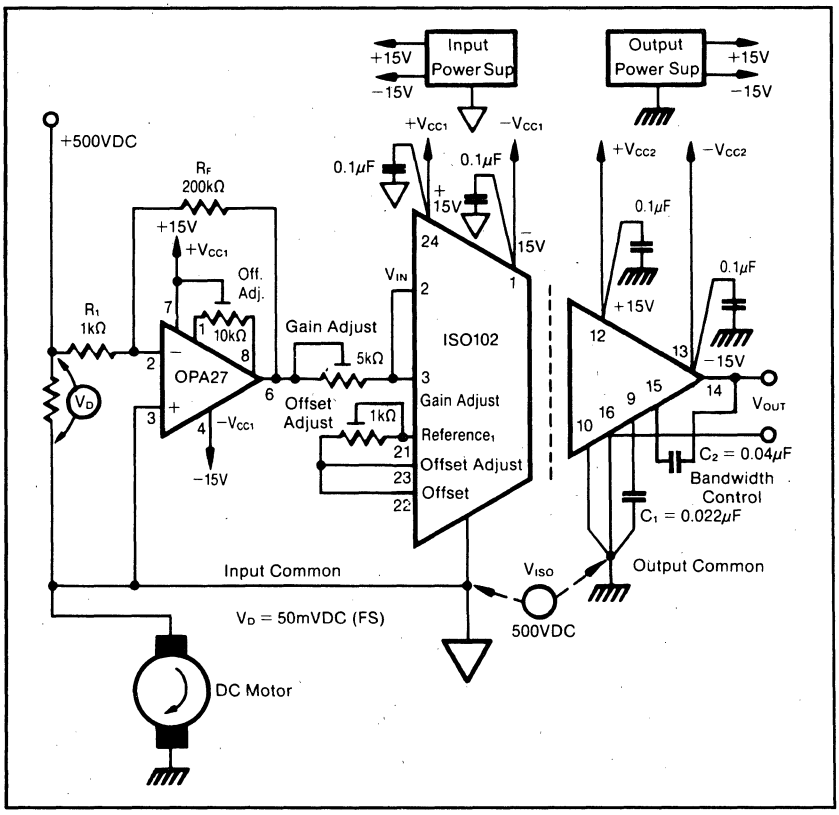


FIGURE 1. 50mV Shunt Measures Current In A 500VDC Motor.

The Errors Of The Op Amp At 25°C (Referred To Input, RTI)

$$V_{E\,(OPA)} = V_D \left[1 - \frac{1}{1 + \frac{1}{\beta A_{VOL}}}\right] + V_{OS}\left[1 + \frac{R_1}{R_F}\right] + I_B R_1 + \text{P.S.R.} + \text{Noise}$$

$V_{E\,(OPA)}$ = Total Op Amp Error (RTI)

V_D = Differential Voltage (Full Scale) Across Shunt

$\left[1 - \frac{1}{1 + \frac{1}{\beta A_{VOL}}}\right]$ = Gain Error Due to Finite Open Loop Gain

β = Feedback Factor

A_{VOL} = Open Loop Gain at Signal Frequency

V_{OS} = Input Offset Voltage

I_B = Input Bias Current

P.S.R. = Power Supply Rejection (μV/V) [Assuming a 20% change with ±15V supplies. Total error is twice that due to one supply]

Noise = $5nV\sqrt{Hz}$ (for 1kΩ source resistance and 1kHz bandwidth)

$ERROR_{(OPA)}$ (RTI)		GAIN ERROR		OFFSET		P.S.R.		NOISE
$V_{E\,(OPA)}$	=	$50mV\left[1 - \frac{1}{1 + \frac{1}{10^6/200}}\right]$		$\left[0{,}025mV\left(1 + \frac{1}{200}\right) + 40 \times 10^{-9} \times 10^3\right]$		[20μV/V × 3V × 2]		[$5nV\sqrt{120}$ (nVrms)]
	=	0.01mV		[0,0251mV + 0,04mV]	+	0.12mV	+	$0{,}055 \times 10^{-3}$mVrms
Error as % of FSR	=	0.02%	+	[0.05% + 0.08%]	+	0.24%	+	0.00011%
After Nulling								
	=	0.01mV	+	[0mV + 0mV]	+	0.12mV	+	0.055×10^{-3}mVrms
	=	0.13mV						
Error as % of FSR*	=	0.02%	+	[0% + 0%]	+	0.24%	+	0.00011%
	=	0.26% of 50mV						

*FSR = Full-Scale Range. 50mV at input to op amp, or 10V at input (and output) of ISO amp.

The Errors Of The ISO Amp At 25°C (RTI)

$$V_{E\,(ISO)} = \frac{1}{200}\left[\frac{V_{ISO}}{IMR} + V_{OS} + \text{G.E.} + \text{Nonlinearity} + \text{P.S.R.} + \text{Noise}\right]$$

$V_{E\,(ISO)}$ = Total ISO Amp Error

IMR = Isolation Mode Rejection

V_{OS} = Input Offset Voltage

$V_{ISO} = V_{IMV}$ = Isolation Voltage = Isolation Mode Voltage

G.E. = Gain Error (% of FSR)

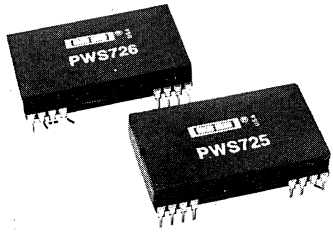
Nonlinearity = Peak-to-peak deviation of output voltage from best-fit straight line. It is expressed as ratio based on full-scale range.

P.S.R. = Change in V_{OS}/10V × Supply Change

Noise = Spectral noise density × $\sqrt{\text{bandwidth}}$. It is recommended that bandwidth be limited to twice maximum signal bandwidth for optimum dynamic range.

$ERROR_{(ISO)}$ (RTI)		IMR		V_{OS}		G.E.		NONLINEARITY		P.S.R.		NOISE
$V_{E\,(ISO)}$	=	$\frac{1}{200}\left[\frac{500VDC}{140dB}\right.$	+	70mV	+	$20V \times \frac{0.25}{100}$	+	$\frac{0.75}{100} \times 20V$	+	$3.7mV \times 3V \times 2$	+	$16\mu V\sqrt{120}$ (rms)$\left.\right]$
	=	$\frac{1}{200}$ [0.05mV	+	70mV	+	50mV	+	15mV	+	22.2mV	+	0.175mVrms]
Error as % of FSR	=	0.0005%	+	0.7%	+	0.5%	+	0.15%	+	0.22%	+	0.00175%
After Nulling												
$V_{E\,(ISO)}$	=	$\frac{1}{200}$ [0.05mV	+	0mV	+	0mV	+	15mV	+	22.2mV	+	0.175mVrms]
	=	$\frac{1}{200}$ [37.2mV]										
	=	0.19mV										
Error as % of FSR	=	0.0005%	+	0%	+	0%	+	0.15%	+	0.22%	+	0.00175%
	=	0.37% of 50mV										
Total Error	=	$V_{E\,(OPA)}$	+	$V_{E\,(ISO)}$								
	=	0.13mV	+	0.19mV								
	=	0.32mV										
	=	0.64% of 50mV										

BURR-BROWN®



PWS725
PWS726

ADVANCE INFORMATION
Subject to Change

Isolated, Unregulated DC/DC CONVERTERS

FEATURES

- ISOLATED ±7 TO ±18VDC OUTPUT FROM SINGLE 7 TO 18VDC SUPPLY
- ±15mA OUTPUT AT RATED VOLTAGE ACCURACY
- HIGH ISOLATION VOLTAGE
  PWS725: 1500Vrms
  PWS726: 3500Vrms
- LOW LEAKAGE CAPACITANCE: 9pF
- LOW LEAKAGE CURRENT: 2μA, max, at 240VAC 50/60Hz
- HIGH RELIABILITY DESIGN
- COMPACT
- LOW COST
- EASY TO APPLY—FEW EXTERNAL PARTS

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS EQUIPMENT
- TEST EQUIPMENT
- DATA ACQUISITION

DESCRIPTION

The PWS725 and PWS726 convert a single 7 to 18VDC input to bipolar voltages of the same value as the input voltage. The converters are capable of providing ±15mA at rated voltage accuracy and up to ±40mA without damage. (See Output Current Rating.)

The PWS725 and PWS726 converters provide reliable, engineered solutions where isolated power is required in critical applications. The high isolation voltage rating is achieved through use of a specially-designed transformer and physical spacing. An additional high dielectric-strength, low leakage transformer coating increases the isolation rating of the PWS726.

Reliability and performance are designed in. The bifilar wound, wirebonded transformer simultaneously provides lower output ripple than competing designs, and a higher performance/cost ratio. The soft-start oscillator/driver design assures full operation of the oscillator before either MOSFET driver turns on, protects the switches, and eliminates high inrush currents during turn-on. Input current sensing protects both the converter and the load from possible thermal damage during a fault condition.

Special design features make these converters especially easy to apply. The compact size allows dense circuit layout while maintaining critical isolation requirements. The Sync connection allows frequency synchronization of up to eight converters. The Enable input allows control over output power in instances where shutdown is desired to conserve power, such as in battery-powered equipment, or where sequencing of power turn-on/turn-off is desired.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

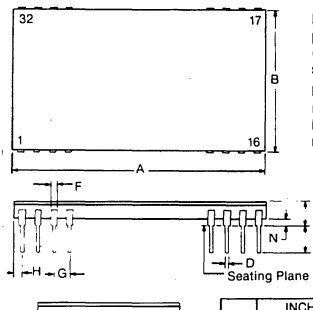
ELECTRICAL

T_A = +25°C, C_L = 1.0μF ceramic, V_{IN} = 15VDC, operating frequency = 400kHz, V_{OUT} = ±15VDC, C_{IN} = 1.0μF ceramic, I_{OUT} = ±15mA, unless otherwise noted.

					ADVANCE INFORMATION			
		PWS725			PWS726			
PARAMETERS	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT								
Rated Voltage			15			*		VDC
Input Voltage Range		7		18	*		*	VDC
Input Current	I_O = ±15mA		82			*		mA
Input Current Ripple	No external filtering		150			*		mAp-p
	L-C input filter, L_{IN} = 100μH, C_{IN} = 1μF[1]		5			*		mAp-p
	C only, C_{IN} = 1μF		60					mAp-p
ISOLATION								
Test Voltages	Input to output, 10 seconds	4000			8000			VDC
	Input to output, 60 seconds, minimum	1500			3500			Vrms
Rated Voltage	Input to output, continuous, AC 60Hz			1500			3500	Vrms
	Input to output, continuous DC			2121			4949	VDC
Isolation Impedance	Input to output		$10^{12}\|\|9$			*		Ω||pF
Leakage Current	Input to output, 240Vrms, 60Hz		1.2	2.0		*	*	μA
OUTPUT								
Rated Output Voltage		14.25	15.00	15.75	*	*	*	VDC
Output Current	Balanced loads		15.0	40		*	*	mA
	Single-ended			80			*	mA
Load Regulation	Balanced loads, ±10mA < I_{OUT} < ±40mA			0.4			*	%/mA
Ripple Voltage (400kHz)	No external capacitor		60			*		mVp-p
	L_O = 10μH, C_O = 1μF (Figure 1)		10			*		mVp-p
	L_O = 0μH, C_O filter only		See Performance Curves					
Output Switching Noise	L_O = 10μH, C_O = 1.0μF		1			*		mVp-p
Output Capacitive Load	L_O = 100μH, C filter			10			*	μF
	C filter only			1			*	μF
Voltage Balance, V+, V−			0.04					%
Sensitivity to ΔV_{IN}			1.15					V/V
Output Voltage Temp. Coefficient			10					mV/°C
TEMPERATURE								
Specification		−25		+85	*		*	°C
Operating		−25		+85	*		*	°C
Storage		−25		+125	*		*	°C

*Specification same as PWS725. NOTE: (1) See Figure 1.

MECHANICAL

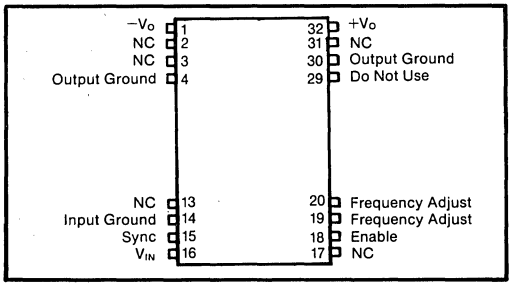


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.150	.185	3.81	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

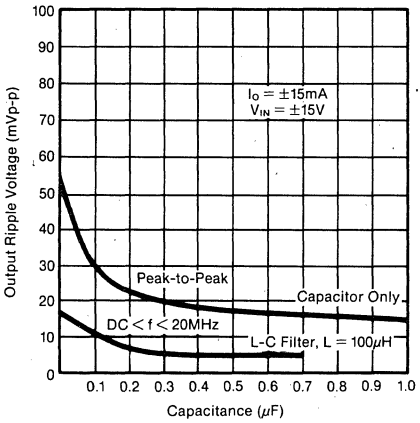
PIN CONFIGURATION



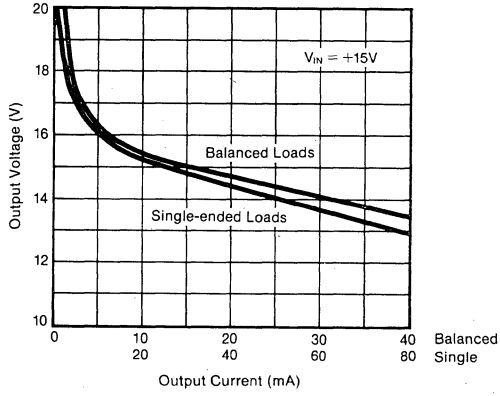
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

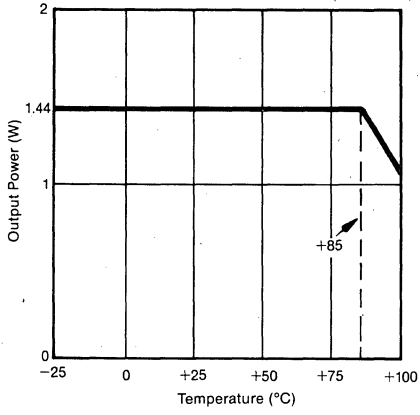
OUTPUT CAPACITANCE vs RIPPLE VOLTAGE



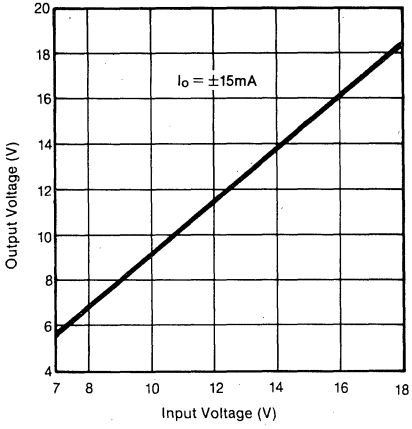
LOAD REGULATION



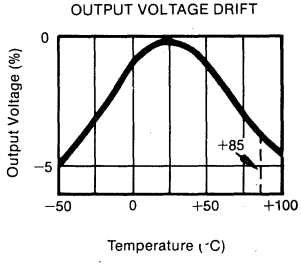
MAXIMUM POWER DISSIPATION



LINE REGULATION



OUTPUT VOLTAGE DRIFT



THEORY OF OPERATION

The PWS725 and the PWS726 DC-to-DC converters consist of a free-running oscillator, control and switch driver circuitry, MOSFET switches, a transformer, a bridge rectifier, and filter capacitors together in a 32-pin DIP (0.900 inches nominal) package. The control circuitry consists of current limiting, soft start, frequency adjust, enable, and synchronization features.

In instances where several converters are used in a system, beat frequencies developed between the converters are a potential source of low frequency noise in the supply and ground paths. This noise may couple into signal paths. By connecting the SYNC pins together, up to eight converters can be synchronized and these beat frequencies avoided. The unit with the highest natural

frequency will determine the synchronized running frequency. To avoid excess stray capacitance, the SYNC pin should not be loaded with more than 50pF. If unused, the SYNC pin must be left open.

Soft start circuitry protects the MOSFET switches during start up. This is accomplished by holding the gate-to-source voltage of both MOSFET switches low until the free-running oscillator is fully operational. In addition to the soft start circuitry, input current sensing also protects the MOSFET switches. This current limiting keeps the FET switches operating in their safe operating area under fault conditions or excessive loads. When either of these conditions occur, the peak input current exceeds a safe limit. The result is an approximate 5% duty cycle, 300μs drive period to the MOSFET switches. This protects the internal MOSFET switches as well as the external load from any thermal damage. When the fault or excessive load is removed, the converter resumes normal operation. A delay period of approximately 50μs incorporated in the current sensing circuitry allows the output filter capacitors to fully charge after a fault is removed. This delay period corresponds to a filter capacitance of no more than 1μF at either of the output pins. This provides full protection of the MOSFET switches and also sufficiently filters the output ripple voltage (see specification table). The current sensing circuitry is designed to provide thermal protection for the MOSFET switches over the operating temperature range as well. The low thermal resistance of the package (θ_{JC} = 10°C/W) ensures safe operation under rated conditions. When these rated conditions are exceeded, the unit will go into its shutdown mode.

An optional potentiometer can be connected between the two FREQUENCY ADJUST pins to trim the oscillator operating frequency ±10% (see Figure 1). Care should be taken when trimming the frequency near the low frequency range. If the frequency is trimmed too low, the peak inductive currents in the primary will trip the input current sensing circuitry to protect the MOSFET switches from these peak inductive currents.

The ENABLE pin allows external control of output power. When this pin is pulled low, output power is disabled. Logic thresholds are TTL compatible. When not used, the Enable input may be left open or tied to V_{IN} (pin 16).

OUTPUT CURRENT RATING

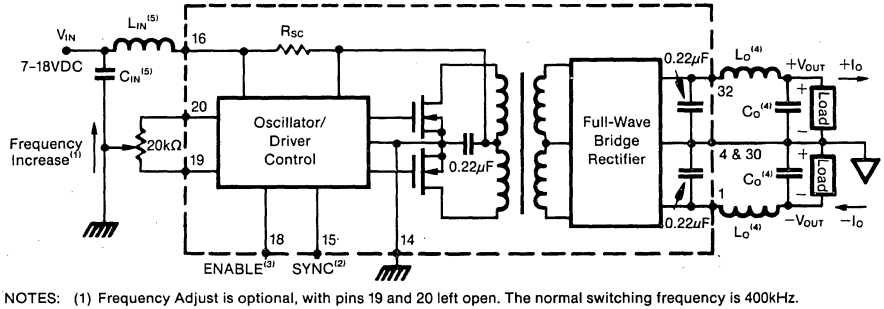
The total current which can be drawn from the PWS725 or PWS726 is a function of total power being drawn from both outputs (see Functional Diagram). If one output is not used, then maximum current can be drawn from the other output. If both outputs are loaded, the total current must be limited such that:

$$|I_L+| + |I_L-| \leq 80mA$$

It should be noted that many analog circuit functions do not simultaneously draw full rated current from both the positive and negative supplies. For example, an operational amplifier may draw 13mA from the positive supply under full load while drawing only 3mA from the negative supply. Under these conditions, the PWS725/726 could supply power for up to five devices (80mA ÷ 16mA ≈ 5). Thus, the PWS725/726 can power more circuits than is at first apparent.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter period of time. The relationship between actual test conditions and the continuous derated maximum specification is an important one. Burr-Brown has chosen a deliberately conservative one: VDC_{TEST} = (2 × VACrms CONTINUOUS RATING) + 1000V for ten seconds. This choice is appropriate for conditions where system transient voltages are not well defined.* Where the real voltages are well-defined or where the isolation voltage is not continuous, the user may choose a less conservative derating to establish a specification from the test voltage.



NOTES: (1) Frequency Adjust is optional, with pins 19 and 20 left open. The normal switching frequency is 400kHz.
(2) Leave SYNC pin open if unused, limit stray capacitance on SYNC pin to less than 50pF.
(3) Leave ENABLE pin open or connect to V_{IN} if not used.
(4) Optional output filtering, with L_O = 0, limit $C_O \leq 1\mu F$, with L_O = 100μH, limit $C_O \leq 10\mu F$, See Performance Curves for L_O = 0.
(5) Optional input filtering, see Performance Curves for L_{IN} = 0.

FIGURE 1. PWS725/726 Functional Diagram.

*Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS I-109 and ICS I-111.

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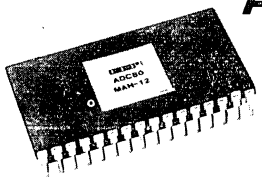
BURR-BROWN®

ADC80MAH-12



Monolithic 12-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- INDUSTRY-STANDARD 12-BIT ADC
- MONOLITHIC CONSTRUCTION
- LOW COST
- ±0.012% LINEARITY
- 25μs MAX CONVERSION TIME
- ±12V or ±15V OPERATION
- NO MISSING CODES −25°C to +85°C
- HERMETIC 32-PIN PACKAGE
- PARALLEL OR SERIAL OUTPUTS
- 705mW MAX DISSIPATION

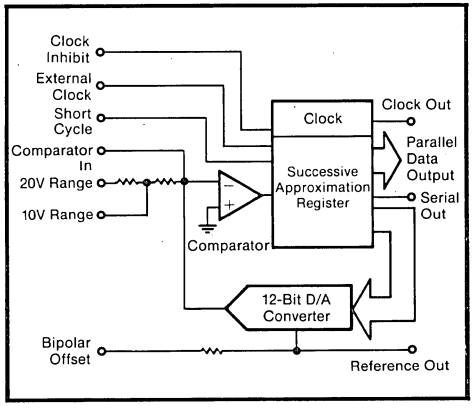
DESCRIPTION

The ADC80MAH-12 is a 12-bit single-chip successive-approximation analog-to-digital converter for low cost converter applications. It is complete with a comparator, a 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, a successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25μs makes the ADC80MAH-12 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, this A/D converter may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation. The convert command circuits have been redesigned to allow simplified free-running operation with internal or external clock.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80MAH-12 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike many ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified.

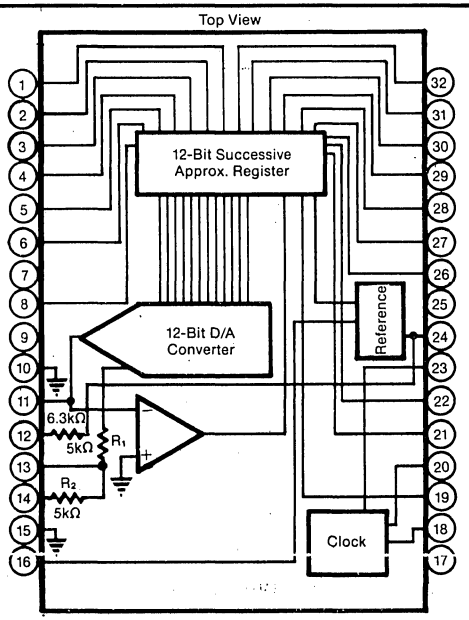
MODEL	ADC80MAH-12			UNITS
	MIN	TYP	MAX	
RESOLUTION			12	Bits
INPUT				
ANALOG				
Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
Bipolar		±2.5, ±5, ±10		V
Impedance: 0 to +5V, ±2.5V	2.45	2.5	2.55	kΩ
0 to +10V, ±5V	4.9	5	5.1	kΩ
±10V	9.8	10	10.2	kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2.0		5.5	V
V_{IL} (Logic "0")	−0.3		+0.8	V
I_{IH} (V_{IN} = +2.7V)			20	μA
I_{IL} (V_{IN} = +0.4V)	−20			μA
Convert Command Pulse Width[1]	100ns		20	μs
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[2]		±0.1	±0.3	% of FSR[3]
Offset Error[2]: Unipolar		±0.05	±0.2	% of FSR
Bipolar		±0.1	±0.3	% of FSR
Linearity Error			±0.012	% of FSR
Differential Linearity Error		±1/2	±3/4	LSB
Inherent Quantization Error		±1/2		LSB
POWER SUPPLY SENSITIVITY				
11.4V ≤ ± V_{CC} ≤ 16.5V		±0.003	±0.009	% of FSR/%V_{CC}
+4.5V ≤ V_{DD} ≤ +5.5V		±0.002	±0.005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[4]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset: Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	−25		+85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[5]		22	25	μs
OUTPUT				
DIGITAL (Bits 1-12, Clock Out, Status, Serial Out)				
Output Codes[6]				
Parallel: Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[7]		CSB, COB		
Logic Levels: Logic 0 (I_{SINK} ≤ 3.2mA)			+0.4	V
Logic 1 (I_{SOURCE} ≤ 80μA)	+2.4			V
Internal Clock Frequency		520		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6.28	+6.3	+6.32	V
Source Current Available for External Loads[8]	200			μA
Temperature Coefficient		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
Rated Supply Voltages		+5, ±12 or ±15		V
Supply Ranges: ±V_{CC}	±11.4		±16.5	V
V_{DD}	+4.5		+5.5	V
Supply Drain: +I_{CC} (+V_{CC} = 15V)		8.5	11	mA
−I_{CC} (−V_{CC} = 15V)		21	24	mA
I_{DD} (V_{CC} = 5V)		30	36	mA
Power Dissipation (±V_{CC} = 15V, V_{DD} = 5V)		593	705	mW
Thermal Resistance, θ_{JA}		50		°C/W
TEMPERATURE RANGE (Ambient)				
Specification	−25		+85	°C
Operating (derated specs)	−55		+125	°C
Storage	−65		+150	°C

NOTES: (1) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns; however, it must be limited to 20μs (max) to assure the specified conversion time. (2) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (4) Includes drift due to linearity, gain, and offset drifts. (5) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time; see "Short Cycle Feature" section. (6) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table I for additional information. (7) NRZ means Non-Return-to-Zero coding. (8) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specification.

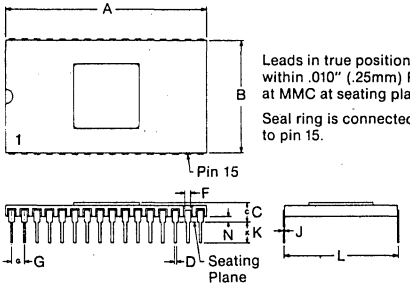
CONNECTION DIAGRAM

Pin 1	Bit 6	Pin 32	Bit 7
Pin 2	Bit 5	Pin 31	Bit 8
Pin 3	Bit 4	Pin 30	Bit 9
Pin 4	Bit 3	Pin 29	Bit 10 (LSB—10 Bits)
Pin 5	Bit 2	Pin 28	Bit 11
Pin 6	Bit 1 (MSB)	Pin 27	Bit 12 (LSB—12 Bits)
Pin 7	N/C*	Pin 26	Serial Out
Pin 8	Bit 1 (MSB)	Pin 25	$-V_{CC}$
Pin 9	+5V Digital Supply	Pin 24	Reference Out (+6.3V)
Pin 10	Digital Common	Pin 23	Clock Out
Pin 11	Comparator In	Pin 22	Status
Pin 12	Bipolar Offset	Pin 21	Short Cycle
Pin 13	R1 10V Range	Pin 20	Clock Inhibit
Pin 14	R2 20V Range	Pin 19	External Clock
Pin 15	Analog Common	Pin 18	Convert Command
Pin 16	Gain Adjust	Pin 17	$+V_{CC}$

* +5V applied to pin 7 has no effect on circuit.



MECHANICAL



Leads in true position within .010" (.25mm) R at MMC at seating plane.

Seal ring is connected to pin 15.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.584	1.616	40.23	41.05
B	.885	.905	22.48	22.99
C	.124	.166	3.15	4.22
D	.016	.020	0.41	0.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
J	.009	.012	0.23	0.30
K	.165	.175	4.19	4.45
L	.900 BASIC		22.86 BASIC	
N	.040	.060	1.02	1.52

CASE: Ceramic, hermetic
MATING CONNECTOR: 2302MC
WEIGHT: 8.4gm (0.29oz)

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common	0 to +16.5V
$-V_{CC}$ to Analog Common	0 to −16.5V
V_{DD} to Digital Common	0 to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs (Convert Command, Clock In) to Digital Common	−0.3V to $+V_{CC}$
Analog Inputs (Analog In, Bipolar Offset) to Analog Common	±16.5V
Reference Output	Indefinite Short to Common, Momentary Short to V_{CC}
Lead Temperature, Soldering	+300°C, 10s
Maximum Junction Temperature	+160°C

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

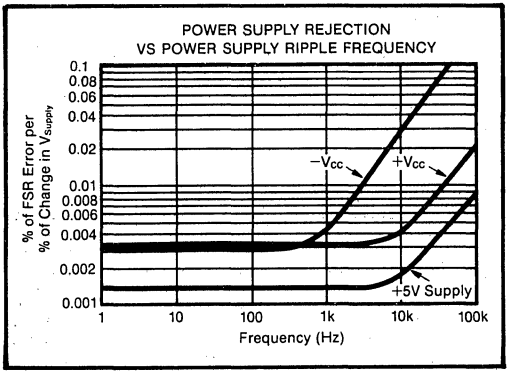
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

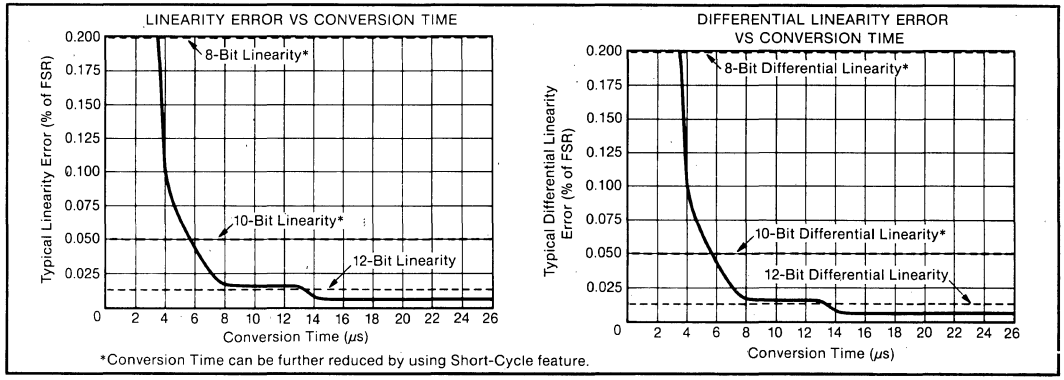
ORDERING INFORMATION

Model	Resolution (bits)
ADC80MAH-12	12
ADC80MAH-12/QM[1]	12

NOTE: (1) /QM suffix indicates Environmental Screening; see Table IV for details.

TYPICAL PERFORMANCE CURVES





DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers.

The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1 which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

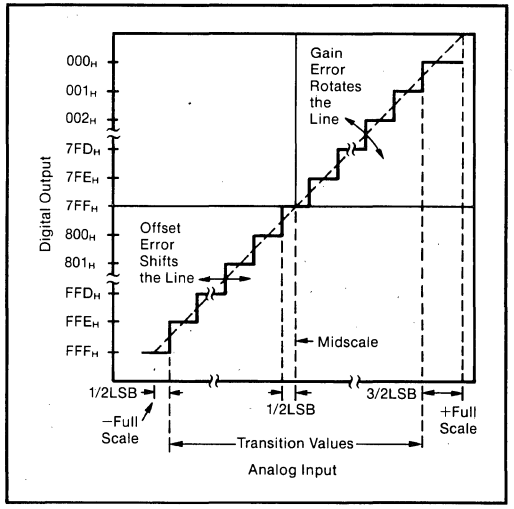


FIGURE 1. Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC80 analog input signal range are described in Table I.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB[1] or CTC[2]	COB or CTC	COB or CTC	CSB[3]	CSB
One Least Significant Bit (LSB)	$FSR/2^n$ n = 8 n = 10 n = 12	$20V/2^n$ 78.13mV 19.53mV 4.88mV	$10V/2^n$ 39.06mV 9.77mV 2.44mV	$5V/2^n$ 19.53mV 4.88mV 1.22mV	$10V/2^n$ 39.06mV 9.77mV 2.44mV	$5V/2^n$ 19.53mV 4.88mV 1.22mV
Transition Values MSB LSB 001_H to 000_H 800_H to $7FF_H$ FFF_H to FFE_H	 + Full Scale Midscale − Full Scale	 +10V − 3/2LSB 0 −10V + 1/2LSB	 +5V − 3/2LSB 0 −5V + 1/2LSB	 +2.5V − 3/2LSB 0 −2.5V + 1/2LSB	 +10V − 3/2LSB +5V 0 + 1/2LSB	 +5V − 3/2LSB +2.5V 0 + 1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) CTC = Complementary Two's Complement—obtained by using the complement of the most significant bit (MSB). $\overline{MSB}$ is available on pin 8. (3) CSB = Complementary Straight Binary.

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC80 input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. ADC80 is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC80 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC80 follows this convention. Thus, bipolar offset error for the ADC80 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the Specification temperature range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC80 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

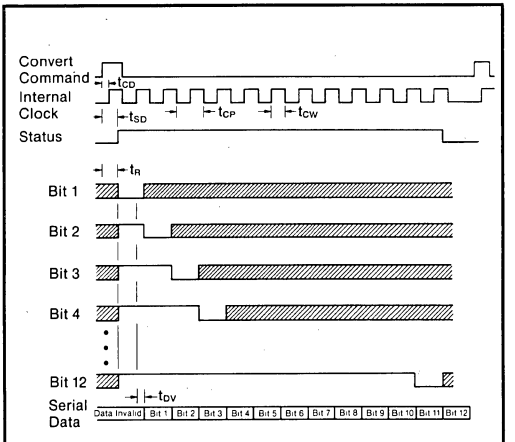
TIMING CONSIDERATIONS

Timing relationships of the ADC80 are shown in Figure 2.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the falling edge of the 13th clock pulse, and with valid output data ready to be read at that time.

Additional convert commands applied during conversion will be ignored.

Status remains high until after the falling edge of the 13th clock pulse. This allows direct use of status for latching parallel data.



Symbol	Parameter	Typ.	Units
t_{CD}	Clock delay from convert command	153	ns
t_{CP}	Nominal clock period	1.81	µs
t_{CW}	Nominal clock pulse width	0.87	µs
t_{SD}	Status delay from convert command	186	ns
t_R	All bits reset delay from convert command	141	ns
t_{DV}	Data valid time from clock pulse high	−15	ns

FIGURE 2. Timing Diagram (nominal values at +25°C with internal clock).

DEFINITION OF DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC80 parallel output; all three are complementary codes, meaning that logic "0" is true. The available codes are complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) and complementary two's complement (CTC) for bipolar input signal ranges. CTC coding is obtained by complementing bit 1 (the MSB) relative to its normal state for CSB or COB coding; the complement of bit 1 is available on pin 8.

Serial Data

Two (complementary) straight binary codes are available on the serial output of the ADC80; as in the parallel case, they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values of Table I also apply to the serial data output, except that the CTC code is not available. All clock pulses available from the ADC80 have equal pulse widths to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC80, but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC80 as possible. Capacitive loading on comparator and input pins should be kept to a minimum to maintain converter performance.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC80 will be driving into a nominal DC input impedance of 2.3kΩ to 9.2kΩ depending upon the range selected. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC80 offers five standard input ranges: 0V to +5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. External padding resistors can be added to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range). Alternatively, the gain range of the converter may easily be increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by decreasing the value of the gain adjust series resistor in Figure 5.

TABLE II. Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

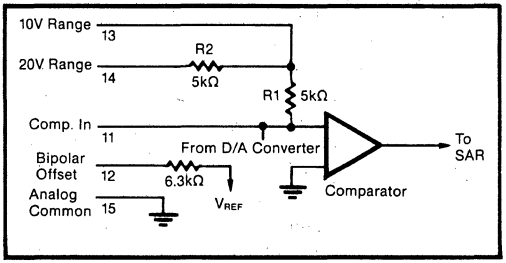


FIGURE 3. Input Scaling Circuit.

CALIBRATION

Optional External Gain And Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC80 as shown in Figures 4 and 5 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These pots may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 16 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

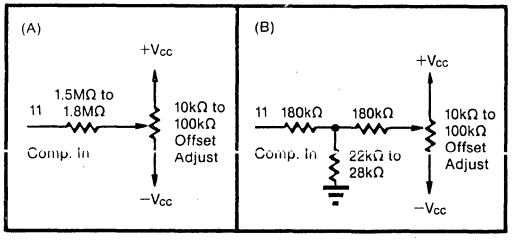


FIGURE 4. Two Methods of Connecting Optional Offset Adjust.

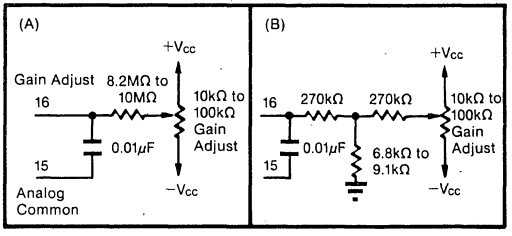


FIGURE 5. Two Methods of Connecting Optional Gain Adjust.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 4. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V +2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurrence of each of the two codes. In other words, the potentiometer is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 5. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V −7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transitions to a precisely known value.

CLOCK OPTIONS AND SHORT CYCLE FEATURE

The ADC80 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with inexpensive TTL logic as shown in Figures 6 through 9. Pin 20 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 19.

A short-cycle input (pin 21) permits the conversion to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applications not requiring full 12-bit resolution. In these situations, the short-cycle pin should be connected to the bit output pin of the next bit after the desired resolution. For example, when 10-bit resolution is desired, pin 21 is connected to pin 28 (bit 11). In this example, the conversion cycle terminates and status is reset after the bit 10 decision. Short-cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times (with internal clock) are shown in Table III. Shorter conversion times are possible with an external clock applied to pin 19. With increasing clock speed, linearity performance will begin to degrade as indicated in the Typical Performance Curves. These curves should be used only as guidelines because guaranteed performance is specified and tested only with the internal clock.

TABLE III. Short-Cycle Connections and Conversion Times for 8-, 10-, and 12-Bit Resolutions—ADC80MAH-12.

Resolution (Bits)	12	10	8
Connect pin 21 to	Pin 9 or NC	Pin 28	Pin 30
Maximum Conversion Time[1] Internal Clock (μs)	25	22	18
Maximum Linearity Error at +25°C (% of FSR)	0.012	0.048	0.20

NOTE: (1) Conversion time to maintain ±1/2LSB linearity error.

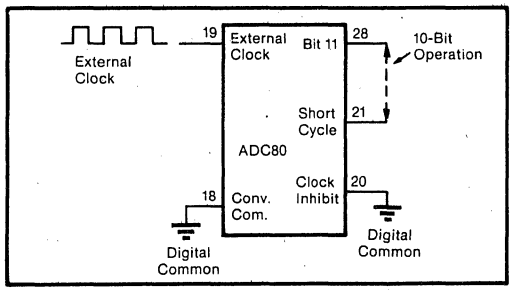


FIGURE 6. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

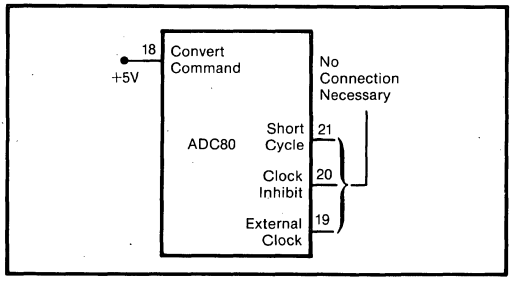


FIGURE 7. Continuous Conversion.

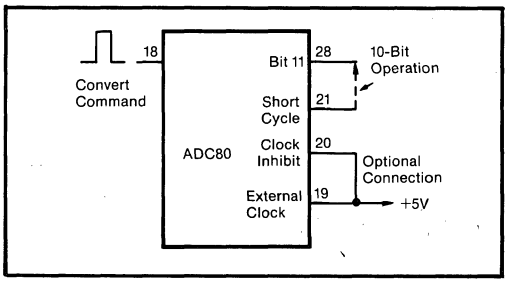


FIGURE 8. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

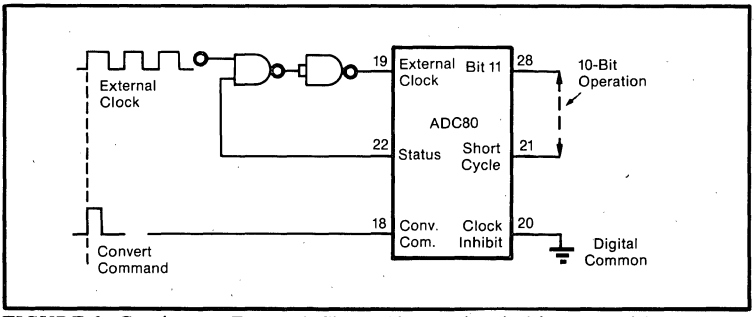


FIGURE 9. Continuous External Clock. (Conversion intitiated by rising edge of convert command. The convert command must be synchronized with clock.)

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table IV is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE IV. Screening Flow for ADC80MAH-12/QM.

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	2010	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady state
Hermeticity: Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/s bubble test only, pre-conditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	2009	

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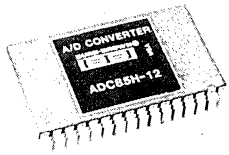


ADC84
ADC85H
ADC87H

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- INDUSTRY STANDARD 12-BIT A/D CONVERTERS
- COMPLETE WITH CLOCK AND INPUT BUFFER
- HIGH SPEED CONVERSION: 10μs (max)
- REDUCED CHIP COUNT—HIGH RELIABILITY
- LOWER POWER DISSIPATION: 450mW (typ)
- ±0.012% MAX LINEARITY
- THREE TEMPERATURE RANGES:
  0°C to +70°C
  −25°C to +85°C
  −55°C to +125°C
- NO MISSING CODES OVER FULL TEMPERATURE RANGE
- PARALLEL AND SERIAL OUTPUTS
- ±12V or ±15V POWER SUPPLY OPERATION
- HERMETIC 32-PIN CERAMIC SIDE-BRAZED DIP

DESCRIPTION

The ADC85H Series of analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a 32-pin hermetic side-brazed package.

Complete with internal reference and input buffer amplifier, they offer versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.012% (±1/2LSB).

The fast 10μs conversion speed for 12-bit resolution makes these ADCs excellent for a wide range of applications where system throughput sampling rates of 100kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at lower resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are CMOS/TTL-compatible. Power supply voltages are ±12VDC or ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

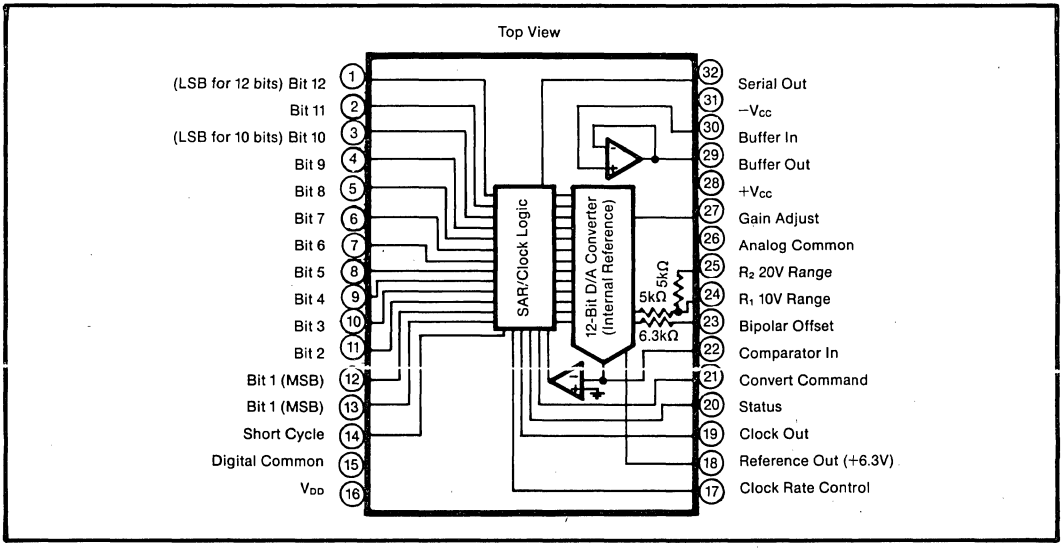
Specified at +25°C and rated supplies unless otherwise noted.

MODEL	ADC84KG-12[1]			ADC85H-12			ADC87H-12			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			*			*	Bits
INPUTS										
ANALOG										
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*			*		V
Unipolar		0 to +5, 0 to +10			*			*		V
Impedance (Direct Input): 0 to +5V, ±2.5V	2.45	2.5	2.55	*	*	*	*	*	*	kΩ
0 to +10V, ±5V	4.9	5	5.1	*	*	*	*	*	*	kΩ
±10V	9.8	10	10.2	*	*	*	*	*	*	kΩ
Buffer Amplifier: Impedance	100			*			*			MΩ
Bias Current		50			*			*		nA
Settling Time to 0.01% for 20V step[2]		2			*			*		µs
DIGITAL[3]										
Convert Command		Positive pulse 50ns (min), trailing edge initiates conversion								
Logic Loading		1			*			*		TTL Load
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error[4]		±0.1	±0.25		*	*		*	*	%
Offset Error[4]: Unipolar		±0.05	±0.2		*	*		*	*	% of FSR[5]
Bipolar		±0.1	±0.25		*	*		*	*	% of FSR
Linearity Error[6]			±0.012			*			*	% of FSR
Inherent Quantization Error		±0.5			*			*		LSB
Differential Linearity Error		±0.5			*			*		LSB
No Missing Codes Temperature Range	0		+70	−25		+85	−55		+125	°C
POWER SUPPLY SENSITIVITY										
Gain and Offset: ±15V		±0.004			*			*		% of FSR/%V_S
+5V		±0.001			*			*		% of FSR/%V_S
DRIFT										
Gain			±30			±15			±15	ppm/°C
Offset: Unipolar		±3			±3				±5	ppm of FSR/°C
Bipolar			±15			±7			±10	ppm of FSR/°C
Linearity			±3			±2			±2	ppm of FSR/°C
Monotonicity		Guaranteed			*			*		
CONVERSION TIME			10			*			*	µs
DIGITAL OUTPUT[3]										
(All Codes Complementary)										
Parallel Output Codes: Unipolar		CSB			*			*		
Bipolar		COB, CTC			*			*		
Output Drive		2			*			*		TTL Loads
Serial Data Codes (NRZ)		CSB, COB			*			*		
Output Drive		2			*			*		TTL Loads
Status		Logic "1" during conversion			*			*		
Output Drive		2			*			*		TTL Loads
Internal Clock: Output Drive		2			*			*		TTL Loads
Frequency[7]		1.35			*			*		MHz
INTERNAL REFERENCE VOLTAGE										
Reference Output	+6.2	+6.3	+6.4	*	*	*	*	*	*	V
Max. External Current With No Degradation			200			*			*	µA
Tempco of Drift			±20		±5	±10		±5	±10	ppm/°C
POWER SUPPLY REQUIREMENTS										
Rated Supply Voltages		+5, ±12 or ±15			*			*		V
Supply Ranges: V_{DD}	+4.75		+5.25	*		*	*		*	V
$\pm V_{CC}$	±11.4		±16.5	*		*	*		*	V
Supply Drain: $+I_{CC}$			20			*			*	mA
$-I_{CC}$			25			*			*	mA
I_{DD}			10			*			*	mA
Total Power Dissipation		450	725		*	*		*	*	mW
TEMPERATURE RANGE										
Specification	0		+70	−25		+85	−55		+125	°C
Operating (with Derated Specs)	−25		+85	−55		+125				°C
Storage	−65		+150	*		*	*		*	°C
PACKAGE	Hermetic Ceramic				*			*		

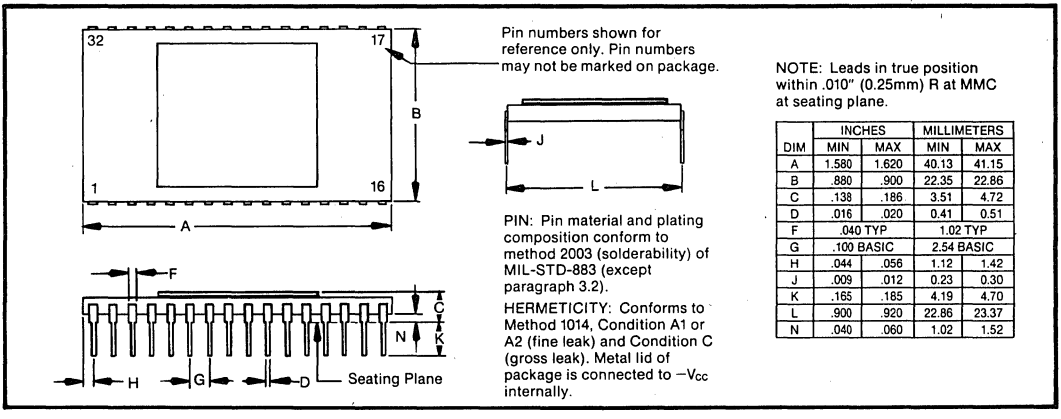
*Specification is the same as ADC84KG-12.

NOTES: (1) Model ADC84KG-10 is the same as model ADC84KG-12 except for the following: (a) Resolution: 10 bits (max), (b) Linearity Error: ±0.048% of FSR (max), (c) Conversion Time: 6μs (max), (d) Internal Clock Frequency: 1.9MHz (typ). (2) If the buffer is used, delay Convert Command until amplifier settles. (3) DTL/TTL compatible. For digital inputs Logic "0" = 0.8V (max) and Logic "1" = 2.0V min. For digital outputs Logic "0" = 0.4V (max) and Logic "1" = 2.4V (min). (4) Adjustable to zero. (5) FSR means Full Scale Range. (6) The error shown is the same as ±1/2LSB max linearity error in % of FSR. (7) Internal clock is externally adjustable.

CONNECTION DIAGRAM—ADC85H SERIES



MECHANICAL



Pin numbers shown for reference only. Pin numbers may not be marked on package.

PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

HERMETICITY: Conforms to Method 1014, Condition A1 or A2 (fine leak) and Condition C (gross leak). Metal lid of package is connected to −Vcc internally.

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

ORDERING INFORMATION

Model	Resolution (Bits)	Temp Range (°C)
ADC84KG-10	10	0 to +70
ADC84KG-12	12	0 to +70
ADC85H-12	12	−25 to +85
ADC85HQ-12*	12	−25 to +85
ADC87H-12	12	−55 to +125
ADC87HQ-12*	12	−55 to +125

* Q suffix indicates environmental screening; see Table II for details.

THEORY OF OPERATION

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC84, ADC85H and ADC87H are also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperature range. Figure 2 is the timing diagram.

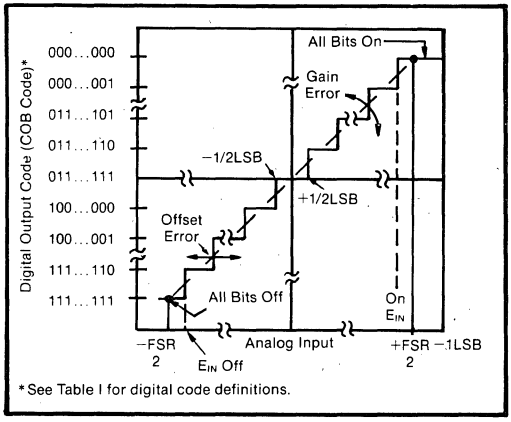


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

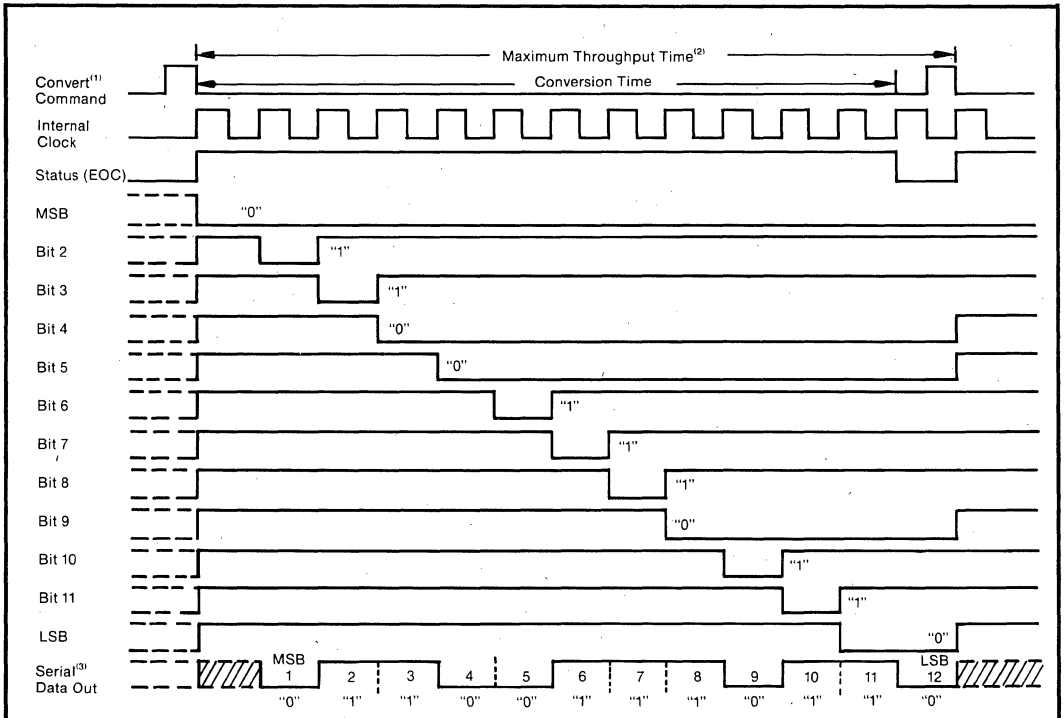


FIGURE 2. Timing Diagram.

DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC85H series parallel output:

- complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges;
- complementary two's complement (CTC) for bipolar input signal ranges;
- complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible analog input signal range for 8-, 10-, and 12-bit resolutions.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary Output	Input Voltage Range and LSB Values					
Analog Input Voltage Ranges	Defined As	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	FSR/2^n n = 8 n = 10 n = 12	20V/2^n 78.13mV 19.53mV 4.88mV	10V/2^n 39.06mV 9.77mV 2.44mV	5V/2^n 19.53mV 4.88mV 1.22mV	10V/2^n 39.06mV 9.77mV 2.44mV	5V/2^n 19.53mV 4.88mV 1.22mV
Transition Values MSB LSB 000...000[4] 011...111 111...110	 +Full Scale Mid Scale −Full Scale	 +10V − 3/2LSB 0 −10V + 1/2LSB	 +5V − 3/2LSB 0 −5V + 1/2LSB	 +2.5V − 3/2LSB 0 −2.5V + 1/2LSB	 +10V − 3/2LSB +5V 0 + 1/2LSB	 +5V − 3/2LSB +2.5V 0 + 1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) CTC = Complementary Two's Complement—obtained by using the complement of the most-significant bit (MSB). MSB is available on pin 13. (3) Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table II is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE II. Screening for ADC85HQ-12 and ADC87HQ-12.

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118*	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Burn-in	1015, B	160 hour, +125°C steady-state
Electrical Test	Burr-Brown test procedure	
Hermeticity: Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/s bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	QC5150*	

* Available upon request.

DISCUSSION OF SPECIFICATIONS

The ADC85H series is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. These ADCs are factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature: gain, offset and linearity drift. The worst-case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or Iσ errors as follows:

$$RSS = \sqrt{\epsilon g^2 + \epsilon o^2 + \epsilon e^2}$$

where ϵg = gain drift error (ppm /°C)
ϵo = offset drift error (ppm of FSR/°C)
ϵe = linearity error (ppm of FSR/°C)

For the ADC85H-12 operating in the unipolar mode, the total RSS drift is ±15.42ppm/°C and for bipolar operation the total RSS drift is ±16.7ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. The power supply sensitivity specification is a measure of how much the plus full-scale value will change from the initial value for independent changes in each power supply. This change results in a proportional change in all code transition values (i.e., a gain error).

The conversion speeds are specified for a maximum linearity error of ±1/2LSB with the internal clock. Faster conversion speeds are possible but at a sacrifice in linearity (see Clock Rate Control Alternate Connections).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. Normally, regulated power supplies with 1% or less ripple are recommended for use with these ADCs. See Layout Precautions and Power Supply Decoupling.

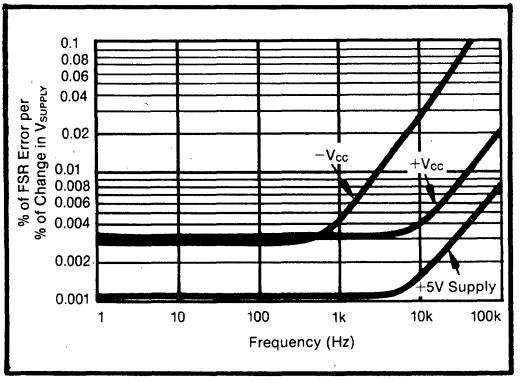


FIGURE 3. Power Supply Rejection vs Power Supply Ripple Frequency.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC85H series, but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. If these grounds must be run separately, use a wide conductor pattern and a 0.01μF to 0.1μF nonpolarizaed bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 4 to reduce noise during operation. These capacitors should be located close to the ADC. 1μF electrolytic type capacitors should by bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

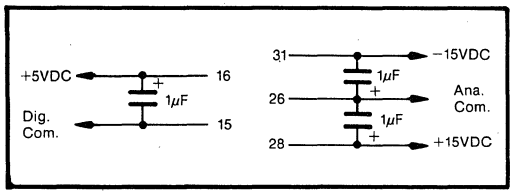


FIGURE 4. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table III. See Figure 5 for circuit details.

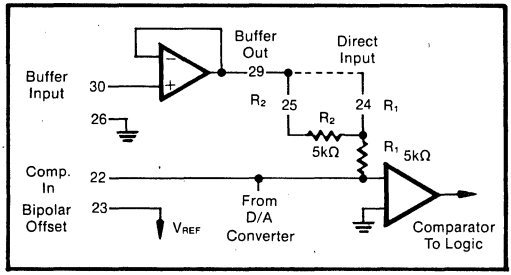


FIGURE 5. Input Scaling Circuit.

TABLE III. Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Buffered Input[1] Connect Pin 29 To Pin	For Direct Input[2] Connect Input Signal To Pin
±10V	COB or CTC	22	Input Signal[3]	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0 to +5V	CSB	26	Pin 22	24	24
0 to +10V	CSB	26	Open	24	24

NOTES: (1) Connect to pin 29 or input signal as shown in next two columns. (2) **If the buffer amplifier is not used, pin 30 must be connected to ground (pin 26).** (3) The input signal is connected to pin 30 if the buffer amplifier is used.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 27 (Gain Adjust) should be bypassed with 0.01μF to reduce noise pickup and Pin 22 (Offset Adjust) may be left open if no external adjustment is required.

Adjustment Procedure

OFFSET—Connect the Offset potentiometer as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

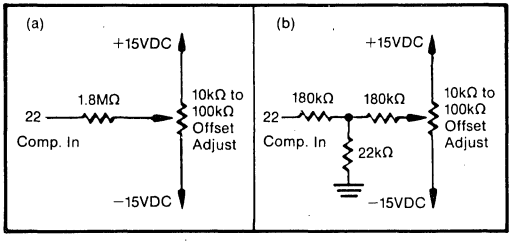


FIGURE 6. Two Methods of Connecting Optional Offset Adjust.

GAIN—Connect the Gain adjust potentiometers as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition voltage to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

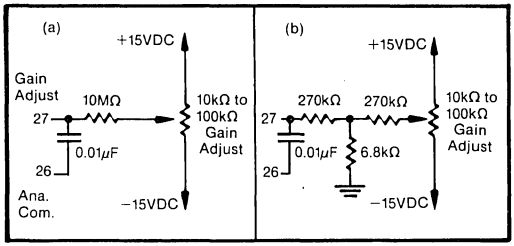


FIGURE 7. Two Methods of Connecting Optional Gain Adjust.

Clock Rate Control Alternate Connections

If adjustment of the Clock Rate is desired for faster conversion speeds, the Clock Rate Control may be connected to an external multiturn trim potentiometer with TCR of ±100ppm/°C or less as shown in Figure 8. If the potentiometer is connected to −15VDC, conversion time can be increased as shown in Figure 8. If these adjustments are used, delete the connections shown in Table IV for pin 17. See Typical Performance Curves for nonlinearity error vs. clock frequency, and Figure 9 for the effect of the control voltage on clock speed. Operation with clock rate control voltage of less than −1VDC is not recommended.

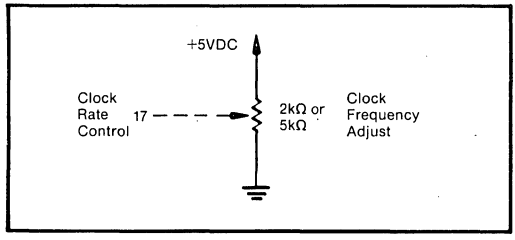


FIGURE 8. 12-Bit Clock Rate Control Optional Fine Adjust.

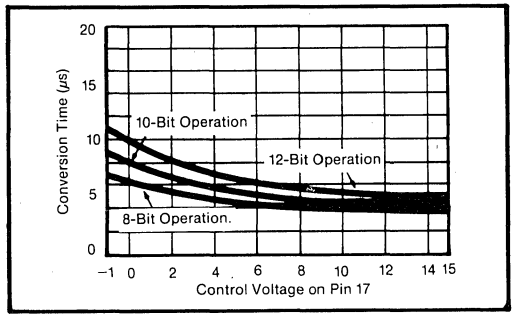


FIGURE 9. Conversion Time vs Clock Speed Control.

Additional Connections Required

The ADC85H series may be operated at faster speeds for resolutions less than 12 bits by connecting the Short Cycle input, pin 14, as shown in Table IV. Conversion

speeds, linearity and resolution are shown for reference. Specifications for 10-bit units assume connections as shown below.

TABLE IV. Short Cycle Connections and Specifications for 8- to 12-Bit Resolution.

Resolution (Bits)	12	10	8
Connect Pin 17 to [1]	Pin 15	Pin 16	Pin 28
Connect Pin 14 to	Pin 16	Pin 2	Pin 4
Maximum Conversion Speed (μs)[2]	10	6	4
Maximum Nonlinearity at 25°C (% of FSR)	0.012[3]	0.048[4]	0.20[4]

NOTES: (1) Connect only if clock rate control is not used. (2) Maximum conversion speeds to maintain ±1/2LSB nonlinearity error. (3) 12-bit models only. (4) 10- or 12-bit models.

Converter Initialization

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

Output Drive

Normally all ADC84, ADC85H, and ADC87H logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

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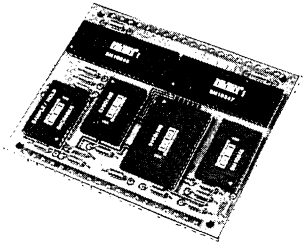


ADC600

12-BIT
ULTRA-HIGH SPEED A/D CONVERTER

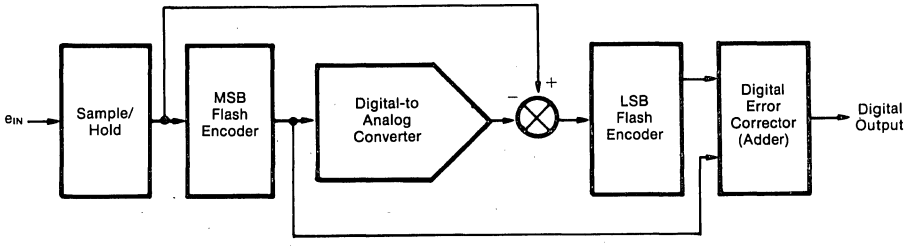
FEATURES

- HIGH RESOLUTION: 12 bits
- SAMPLE RATE: DC to 10MHz
- HIGH SINAD RATIO: 67dB
- LOW HARMONIC DISTORTION: −71dB
- LOW INTERMODULATION DISTORTION: −70dB
- INPUT RANGE: ±1.25V
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- LOW DISSIPATION: 8.5W
- 0°C TO +70°C AND −40°C TO +85°C
- DIGITAL SIGNAL PROCESSING
- RADAR SIGNAL ANALYSIS
- TRANSIENT SIGNAL RECORDING
- FFT SPECTRUM ANALYSIS
- HIGH-SPEED DATA ACQUISITION
- JAM-RESISTANT SYSTEMS
- SIGINT, ECM, AND EW SYSTEMS
- DIGITAL COMMUNICATIONS
- DIGITAL OSCILLOSCOPES

DESCRIPTION

The ADC600 is an ultra-high speed analog-to-digital converter capable of digitizing signals at any rate from DC to 10 megasamples per second. Outstanding dynamic range has been achieved by minimizing noise and distortion.

The ADC600 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry. Laser-trimmed ceramic submodules are mounted on a 17-square-inch multilayer PC motherboard. Logic is ECL.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, 10MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = 15V, V_{DD1} = +5V, V_{DD2} = −5.2V, and 15-minute warmup in normal convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC600K MIN	ADC600K TYP	ADC600K MAX	ADC600B MIN	ADC600B TYP	ADC600B MAX	UNITS
RESOLUTION				12			*	Bits
INPUTS								
ANALOG								
Input Range	Full scale	−1.25		+1.25	*		*	V
Input Impedance			1.5			*		MΩ
Input Capacitance			5			*		pF
DIGITAL								
Logic Family			ECL 10k-Compatible			*		
Convert Command			Negative Edge			*		
Pulse Width		10			*			ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	F = 200Hz		±0.1	±0.5		*	*	% FSR
Input Offset	DC		±0.1	±0.5		*	*	% FSR[1]
Integral Linearity Error	F = 200Hz			1.25			*	LSB
Differential Linearity Error	F = 200Hz: 68.3% of all codes			0.25			*	LSB
	99.7% of all codes			1.00			*	LSB
	100% of all codes			+1.25			*	LSB
				−1.00			*	LSB
Missing Codes				none			*	
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	*		*	Samples/s
Conversion Time	First conversion		140	150		*	*	ns
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	F = 4.9MHz: 68.3% of all codes			0.5			*	LSB
	99.7% of all codes			1.5			*	LSB
	100% of all codes			2.0			*	LSB
Total Harmonic Distortion[2]								
F = 4.8MHz (0dB)	F_S = 10MHz		−71			*		dBC[3]
F = 0.58MHz (0dB)			−74			*		dBC
F = 2.4MHz (0dB)	F_S = 5MHz		−73			*		dBC
F = 0.58MHz (0dB)			−74.5			*		dBC
Two-Tone Intermodulation Distortion[2][4]								
F = 4.88MHz (−6dB) 4.65MHz (−6dB)	F_S = 10MHz		−70.5			*		dBC
F = 2.40MHz (−6dB) 2.25MHz (−6dB)	F_S = 5MHz		−74.5			*		dBC
Signal-to-Noise and Distortion (SINAD) Ratio								
F = 4.8MHz (0dB)	F_S = 10MHz		66.8			*		dB
F = 0.58MHz (0dB)			68.6			*		dB
F = 2.4MHz (0dB)	F_S = 5MHz		67.2			*		dB
F = 0.58MHz (0dB)			69			*		dB
Aperture Time			6			*		ns
Aperture Jitter			±5			*		ps
Analog Input Bandwidth								
Small Signal	−20dB input		70			*		MHz
Full Power	0dB input		40			*		MHz
OUTPUTS								
Logic Family			ECL with pull-down to $-V_{DD2}$ (see text)					
Logic Coding			Offset Binary, Twos Complement					
Logic Levels	Logic "LO"		−1.7			*		V
	Logic "HI"		−0.9			*		V
EOC Delay Time	Data Out to DV	5	35		*	*		ns
Tr and Tf	20% to 80%		5			*		ns
Data Valid Pulse Width	50%	5	8		*	*		ns
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
V_{DD1}		+4.75	+5	+5.25	*	*	*	V
V_{DD2}		−4.95	−5.2	−5.46	*	*	*	V
Supply Currents: $+V_{CC}$	Operating		75			*		mA
$-V_{CC}$			45			*		mA
V_{DD1}			400			*		mA
V_{DD2}			900			*		mA
Power Consumption	Operating		8.5			*		W

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

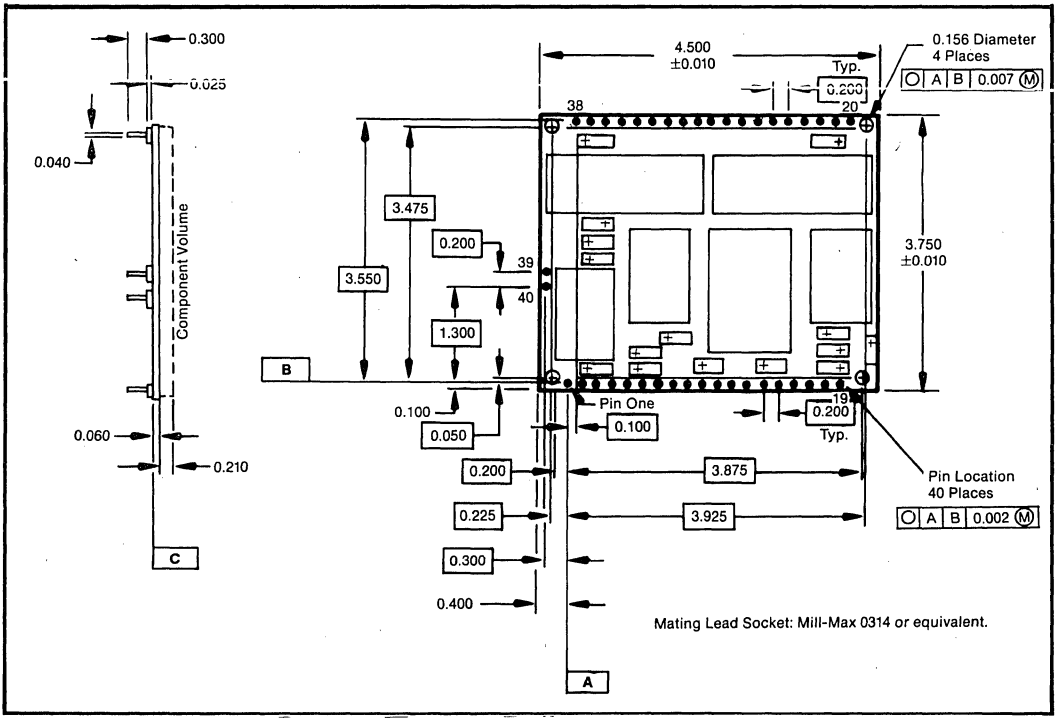
$\pm V_{CC}$ = 15V, V_{DD1} = +5V, V_{DD2} = −5.2V, R_S = 50Ω, 15-minute warmup, and $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	ADC600K MIN	ADC600K TYP	ADC600K MAX	ADC600B MIN	ADC600B TYP	ADC600B MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE} max	0		+70	−40		+85	°C
Storage	$T_{AMBIENT}$	−40		+100	*		*	°C
ACCURACY								
Gain Error	F = 200Hz		±30			*		ppm/°C
Input Offset	DC		±50			*		µV/°C
Integral Linearity Error	F = 200Hz			1.5			*	LSB
Differential Linearity Error	F = 200Hz							
	63% of all codes			0.5			*	LSB
	98% of all codes			1.25			*	LSB
	100% of all codes			1.5			*	LSB
Sample Rate		DC		10	*		*	MHz

*Same as ADC600K

NOTE: (1) FSR: full-scale range = 2.5Vp-p. (2) Units with tested and guaranteed distortion specifications are available on special order—inquire. (3) dBC = level referred to carrier (input signal ≈ 0dB); F = input signal frequency; F_S = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (≈ 0dB), the intermodulation products will be 6dB lower.

MECHANICAL



ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±16.5V
V_{DD1}	+7.0V
V_{DD2}	−7.0V
Analog Input	±5.0V
Logic Input	V_{DD2} to +0.5V
Case Temperature	100°C
Junction Temperature(1)	150°C
Storage Temperature	−40°C to +100°C

Stresses above these ratings may cause permanent damage to the device.

(1). See Table I for thermal resistance data.

ORDERING INFORMATION

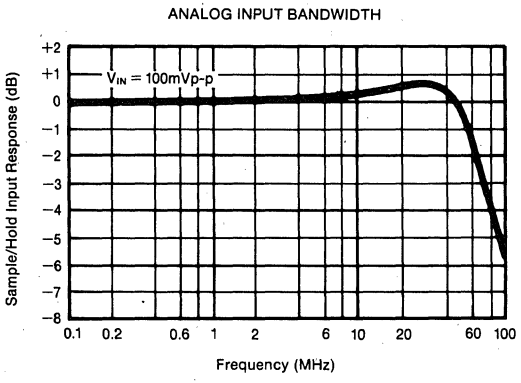
ADC600 X Q

- Basic Model Number
- Performance Grade Code
  - K = 0°C to +70°C
  - B = −40 to +85°C
- Reliability Screening
  - Q = Q-Screened

PIN ASSIGNMENTS

1	Common	21	Common
2	$-V_{CC}$ (−15V)	22	Data Valid
3	V_{DD2} (−5.2V)	23	Bit 12 (LSB)
4	V_{DD1} (+5V)	24	Bit 11
5	$+V_{CC}$ (+15V)	25	Bit 10
6	Common	26	Bit 9
7	V_{DD2} (−5.2V)	27	Bit 8
8	V_{DD1} (+5V)	28	Bit 7
9	Common	29	Bit 6
10	V_{DD2} (−5.2V)	30	Bit 5
11	Common	31	Bit 4
12	Common	32	Bit 3
13	$+V_{CC}$ (+15V)	33	Bit 2
14	$-V_{CC}$ (−15V)	34	Bit 1 (MSB)
15	V_{DD2} (−5.2V)	35	$\overline{\text{Bit 1 (MSB)}}$
16	V_{DD1} (+5V)	36	V_{DD2} (−5.2V)
17	Common	37	Common
18	V_{DD2} (−5.2V)	38	Convert Command
19	V_{DD1} (+5V)	39	Analog Input
20	V_{DD2} (−5.2V)	40	Analog Input Return

TYPICAL PERFORMANCE CURVE



THEORY OF OPERATION

The ADC600 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: Sample/Hold Amplifier, MSB Flash encoder, DAC and Error Amplifier, LSB Flash Encoder, Digital Error Corrector, and Timing Circuits. The ADC600 uses individually tested and laser-trimmed submodules mounted on a four-layer motherboard to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer the capacitor can acquire the signal in 25ns. The low-bias-current output buffer is then required to settle to only the resolution (7 bits) of the first (MSB) flash encoder in 25ns while an additional 60ns is allowed for settling to the resolution (12 bits) of the second (LSB) flash encoder. Sample/hold droop appears as only an offset error and does not affect linearity.

Both the MSB and the LSB flash encoder (ADC) are high-speed 7-bit resolution converters formed by parallel-connecting two 6-bit flash ADCs as shown in Figure 2. The DAC +10V reference is also used to generate reference voltages for the MSB and LSB encoders to compensate drift errors. Buffering and scaling are performed by I_{C1} and I_{C2}. Laser-trimming is used to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 7-bit resolution DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome resistors on sapphire and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 25ns.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, a high-speed FET switch blanks the amplifier input from the beginning of the S/H acquisition time to end of the MSB encoder update time.

The timing circuits shown in Figure 3 supply all the critical timing signals necessary for proper operation of the ADC600. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. The ECL logic timing delay is stable over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated by IC_1 to allow triggering by pulses from as narrow as 5ns to as wide as 75% duty cycle. This differentiated signal sets flip-flop IC_2, placing the S/H back into its sample mode.

The output of the third stage of the shift register is also differentiated by IC_8 and used to generate a strobe for the LSB flash encoder. R_1 is laser-trimmed to generate a precise 8ns pulse while the oscillator frequency is adjusted to trim the strobe pulse delay. IC_4 and IC_5 comprise the

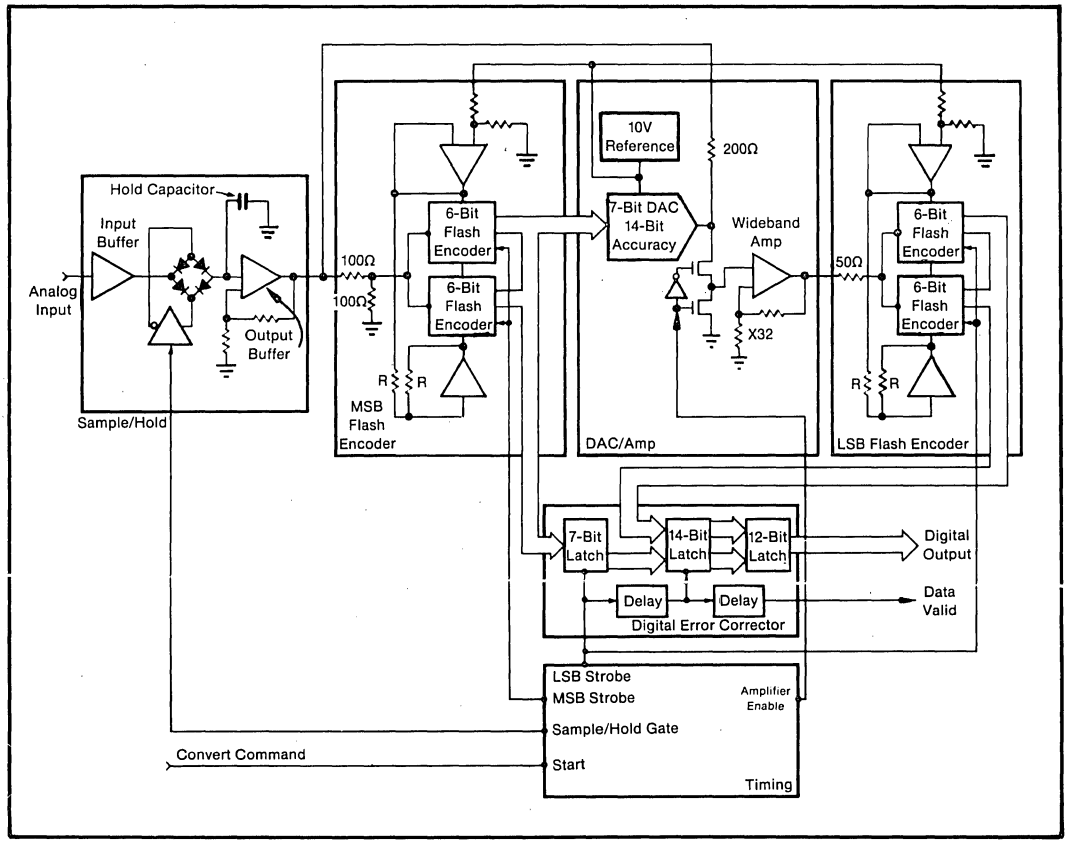


FIGURE 1. Block Diagram of 12-Bit 10MHz ADC600.

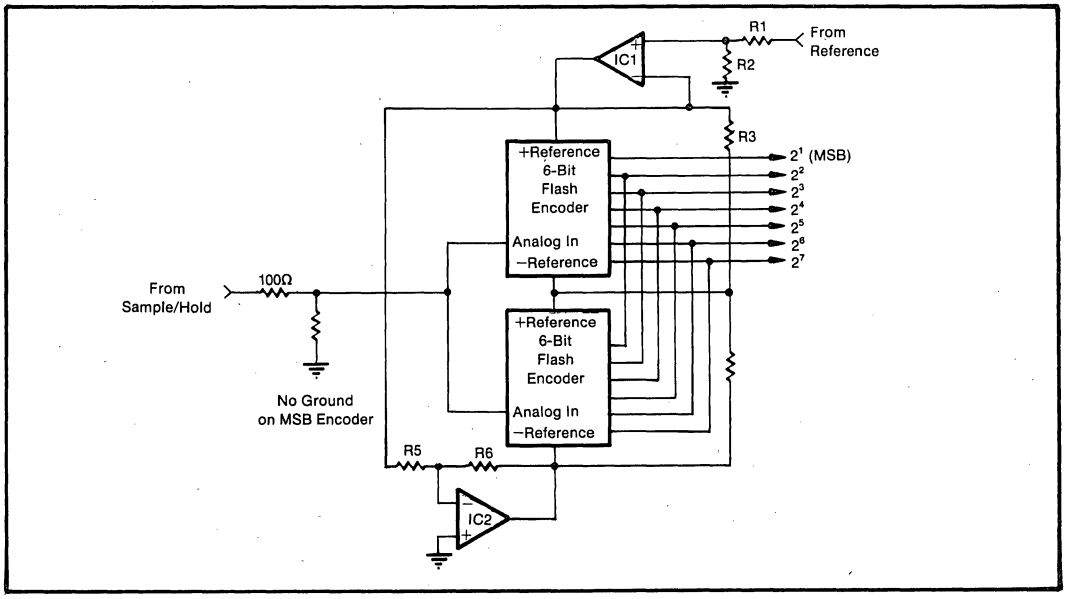


FIGURE 2. 7-Bit Flash Encoder.

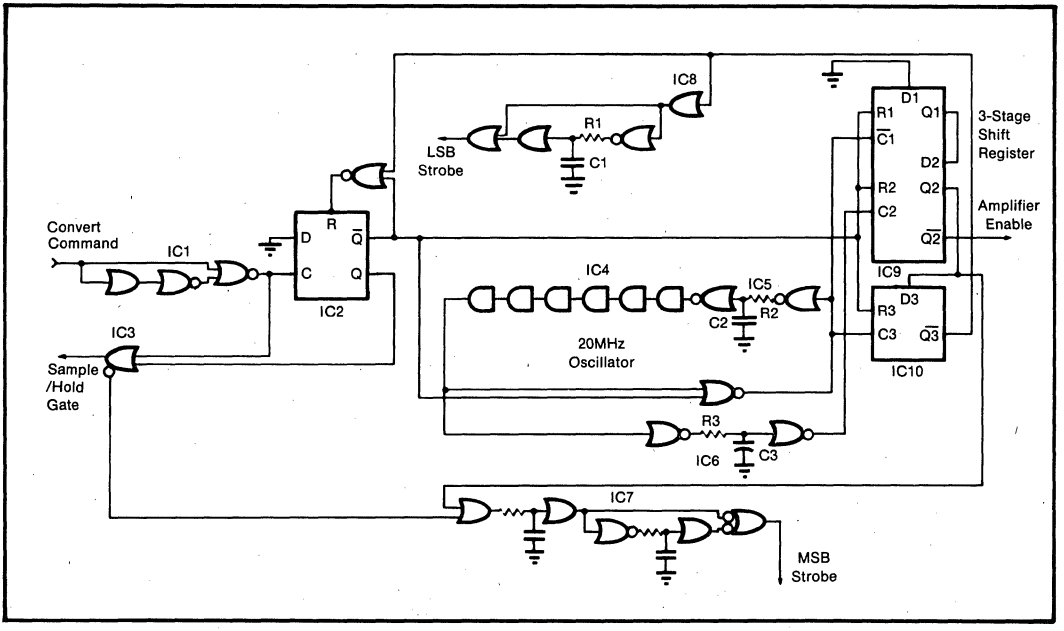


FIGURE 3. Schematic of Timing Module.

principal elements of a 20MHz ring oscillator. R_2 and C_2 add additional delay and allow laser-trimming for the LSB delay. A blanking pulse to prevent error amplifier overload is generated by the second stage of the shift register. Proper timing is generated by laser-trimming R_3 which, along with C_3 forms a delay element along with two gates of IC_6.

A strobe pulse of the MSB flash encoder is generated and trimmed in a similar circuit using IC_7. This technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus the fixed 67ns ADC conversion time ADC600 conversion rates are therefore possible above the 10MHz specification but S/H acquisition time is sacrificed and accuracy is rapidly degraded.

The output of the MSB encoder is read into a separate 7-bit latch at the same time the LSB encoder is being strobed. The latched MSB data, along with the LSB data, is then read into a 14-bit latch 30ns after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. This latch eliminates any critical timing problems that would result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry (Figure 4) is to assemble the 7-bit words from the two flash encoders into a 12-bit output word. In addition, the circuit uses the LSB flash encoder strobe to generate timing strobes for both data registers. A data valid (DV) pulse is also generated which is used to indicate when output data can be latched into an external register. This DV pulse is delayed 5ns after the output data has settled to allow a sufficient set-up time for an external ECL data latch.

The 14-bit register output is then sent to a 12-bit adder where the final data output word is created. The MSB data forms the most significant seven bits of a 12-bit word, with the last five bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits form the other input to the adder with the first five bits being assigned zeros. As two 12-bit words are being added, the output of the adder could exceed 12 bits in range; however, the final data output is only a 12-bit word, so a means of detecting an overrange is included.

To prevent reading erroneous data, the converter data output reads all ones for a full-scale positive input or overrange and reads all zeros for a negative full-scale input or overrange. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±1.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADC600 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a Fast Fourier Transform (FFT) to the ADC digitial output will provide data on all important dynamic performance parameters: total harmonic distortion (THD), signal-to-noise raito (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), total noise and distortion (TND), and intermodulation distortion (IMD).

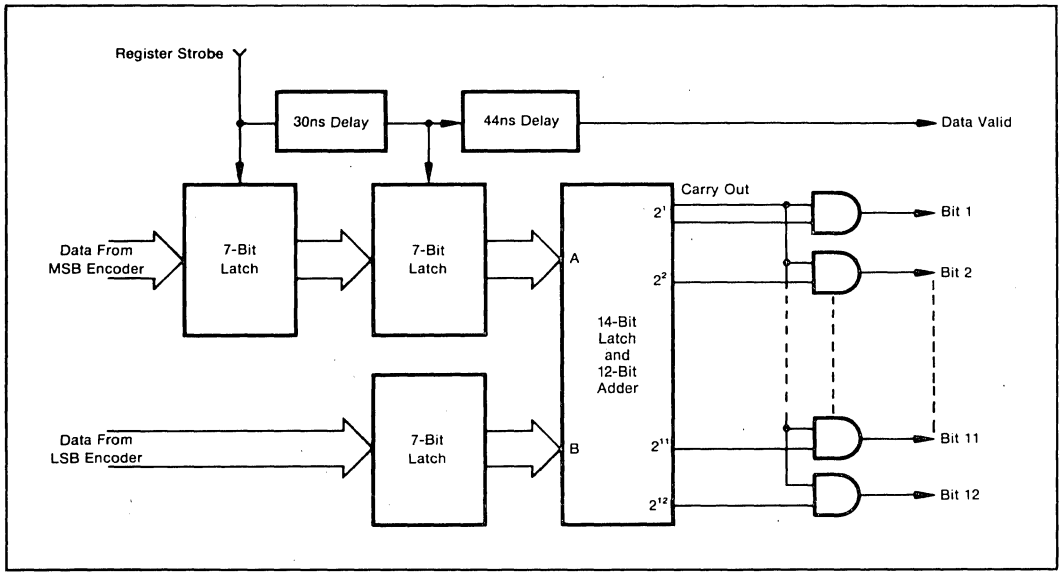


FIGURE 4. Block Diagram of Digital Error Corrector.

A test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 5. This was used to generate the typical FFT performance curves shown on pages 112 through 115.

To preserve measurement accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To assure that the majority of codes are exercised in the ADC600 (12 bits), a ten-sample average of 512-point FFTs is taken.

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion[2] Ratio (SINAD):
$$10 \log \frac{\text{sine wave signal power}}{\text{noise + harmonic power}}$$
2. Total Harmonic Distortion (THD):
$$10 \log \frac{\text{harmonic power (first nine harmonics)}}{\text{sinewave signal power}}$$
3. Total Noise Distortion (TND):
$$10 \log \frac{\text{noise power}}{\text{sinewave signal power}}$$
4. Intermodulation Distortion (IMD):
$$10 \log \frac{\text{IMD product power}}{\text{sinewave signal power}}$$

IMD is referenced[3] to the larger of the test signals f_1 or f_2.

Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

Attention to test set-up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise will not overrange the ADC and "hard limit" on signal peaks.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than −6dB to prevent "hard limiting" on peaks.
3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 6) will eliminate harmonics from the test signal generator.
4. Test signal generators must have exceptional noise performance (better than −155dBC) to achieve accurate SNR measurements[4]. Good generators together with fifth-order elliptical bandpass filters are recommended for SNR and SINAD tests.
5. The analog input of the ADC600 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω) or it should be driven by an OPA600 buffer. Short leads are necessary to prevent digital noise pickup.
6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A recommended interface circuit is shown in Figure 7. Short leads are necessary to preserve fast ECL rise times.
7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. An active summing amplifier using an OPA600 is shown in Figure 8. This circuit will provide excellent performance from DC to

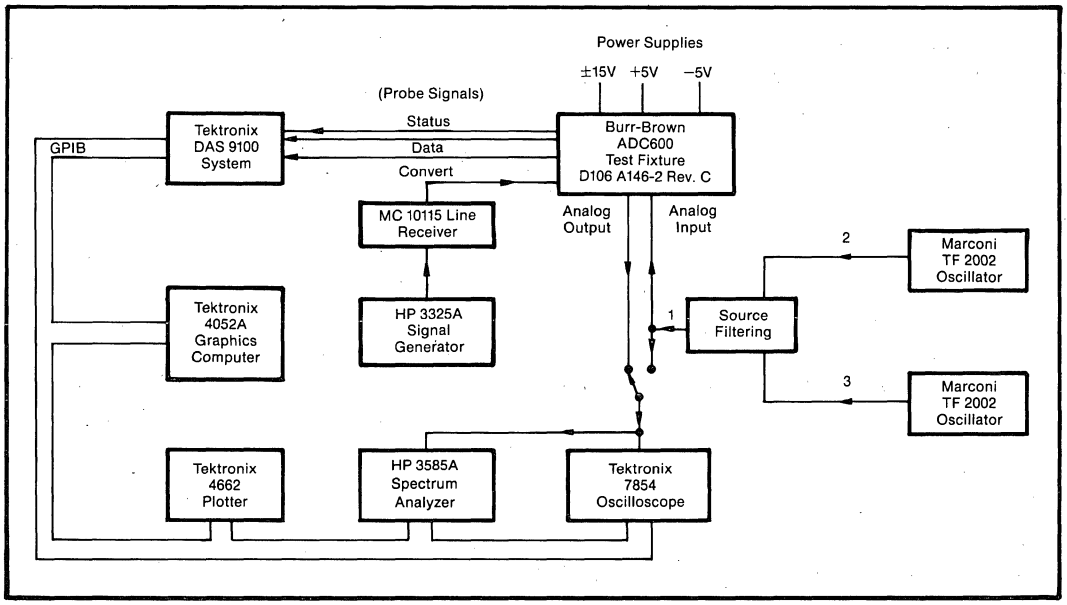


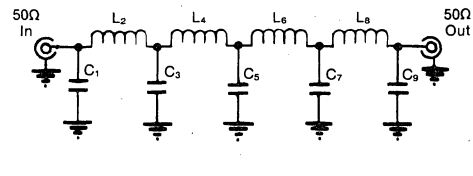
FIGURE 5. Test Setup for High Speed FFT Testing.

5MHz with harmonic and intermodulation distortion products typically better than −70dBC. A passive hybrid transformer signal combiner can also be used (Figure 9) over a range of about 1MHz to 30MHz. The port-to-port isolation will be ≈ 45dB between signal generators and the input-output insertion loss will be ≈ 6dB.

8. A very low side-lobe window must be used for FFT calculation. A minimum four-sample Blackman-Harris window function is recommended.[1]
9. Digital data must be latched into an external ECL 12-bit register only by the Data Valid output pulse. Due to the possibility of improper timing, output data **cannot** be latched by using the convert command!
10. Do not overload the data output logic. These outputs are already provided with internal 68Ω pull-down resistors tied to −5.2V.
11. A well-designed, clean PC board layout will assure proper operation and clean spectral response[5][6]. Proper grounding and bypassing, short lead lengths and separation of analog and digital signals and ground returns are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (2oz-foil) ground planes can give excellent results, if carefully designed.

    Prototyping "plug-boards" or wire-wrap boards will not be satisfactory.

NOTES:
1. *On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform*, Fredric J. Harris. Proceedings of the IEEE, Vol. 66, No. 1, January 1978, pp 51-83.
2. SINAD test includes harmonics whereas SNR does not include these important spurious products.
3. If IMD is referenced to peak envelope power, an improvement of 6dB.
4. *Test Report: FFT Characterization of Burr-Brown ADC600K*, Signal Conversion Ltd., Swansea, Wales, U.K.
5. MECL System Design Handbook, 3rd Edition, Motorola Corp.
6. Motorola MECL, Motorola Corp.



9th Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2× cutoff frequency = 90dB.

Cutoff frequency = −3dB frequency; to convert cutoff frequency to −0.5dB frequency, multiply all LC values by 0.9897.

Cutoff Freq. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_2 (μH)	L_4 (μH)	L_6 (μH)	L_8 (μH)
5.0	1134.6	1729.2	1765.6	1729.2	1134.6	2.056	2.216	2.216	2.056
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45

FIGURE 6. Ninth-Order Harmonic Filter.

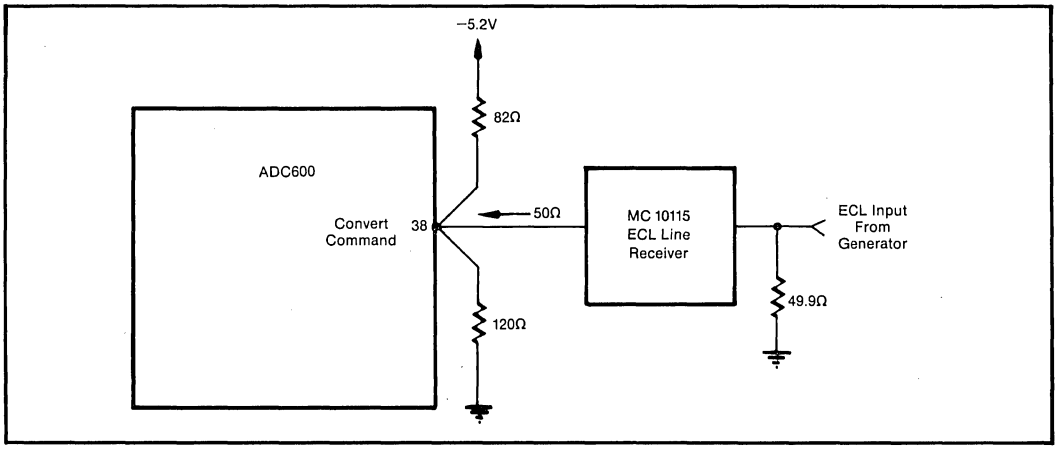


FIGURE 7. Optional Convert Command Interface Circuit.

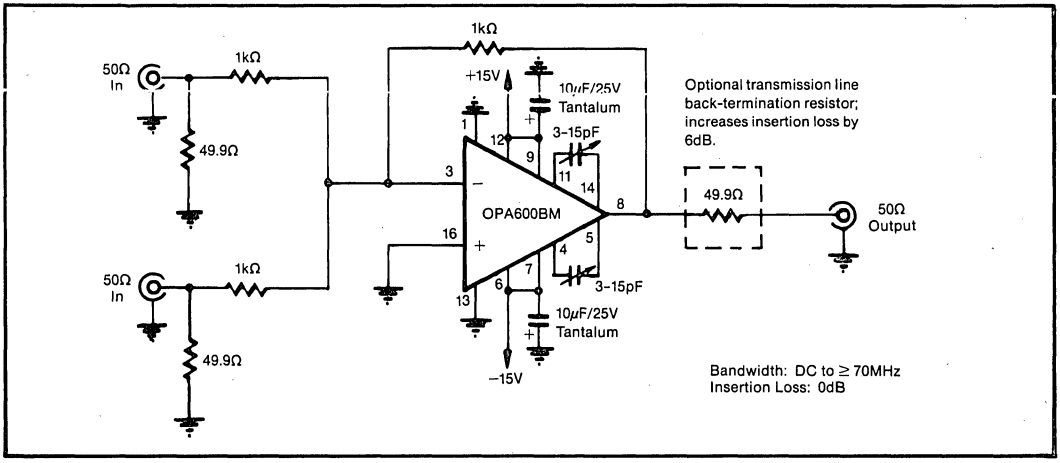


FIGURE 8. Active Signal Combiner.

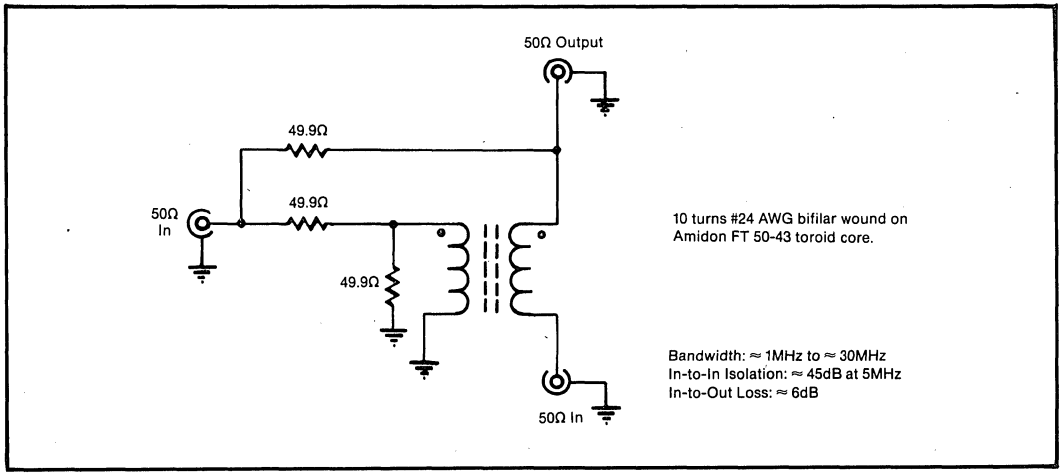
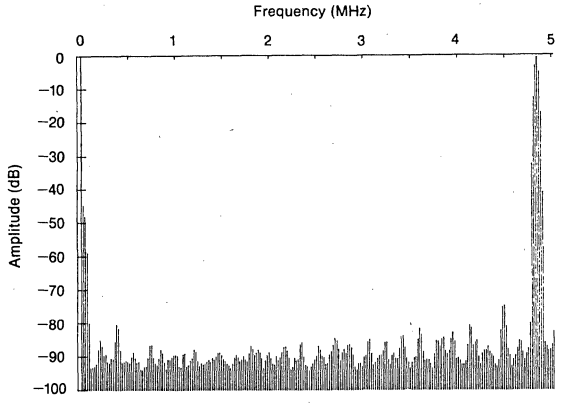


FIGURE 9. Passive Signal Combiner.

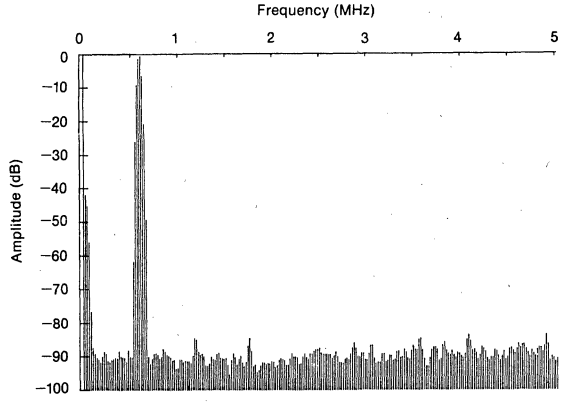
TYPICAL FFT SPECTRAL PERFORMANCE

All FFT data: 512-point FFT, 10-sample average; minimum 4-sample Blackman-Harris Window.

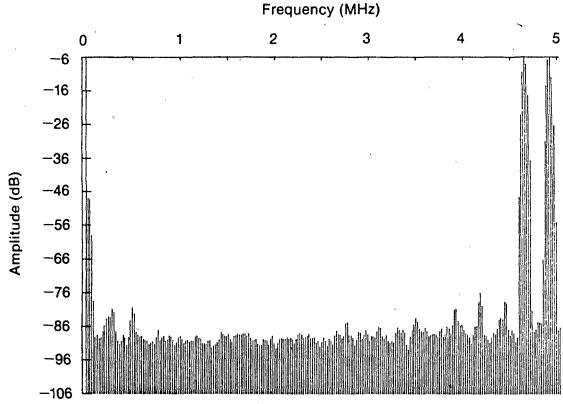
Sample Rate = 10MHz, Input Voltage = Full-Scale (0dB)



	Level re: Full-Scale (dB)
4.8438MHz Fundamental	−0.7
Harmonics: 2f	−80.5
3f	−74.7
4f	−86.6
SINAD	67.2dB
TND	−69.5dBC
THD	−71.0dBC



	Level re: Full-Scale (dB)
0.6055MHz Fundamental	−0.6
Harmonics: 2f	−84.7
3f	−84.6
4f	−87.5
SINAD	69.6dB
TND	−70.7dBC
THD	−76.4dBC

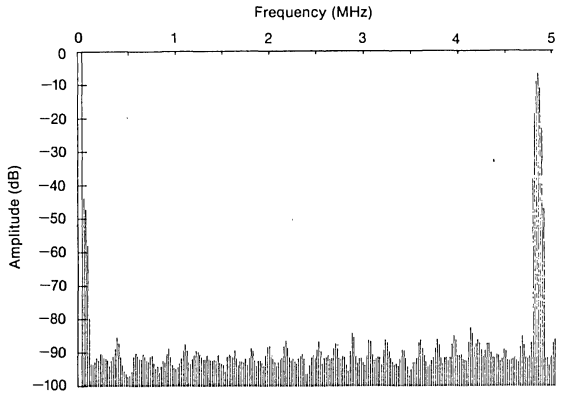


	Level re: Full-Scale (dB)
F_1: 4.9219MHz	−6.3
F_2: 4.6484MHz	−6.3
Peak Envelope	−0.6
IMD: 0.4883MHz	−80.8
4.1797MHz	−76.3
4.4336MHz	−78.9

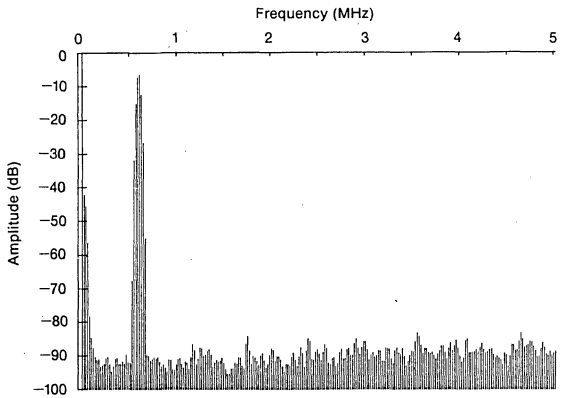
TYPICAL FFT SPECTRAL PERFORMANCE (CONT)

All FFT data: 512-point FFT, 10-sample average; minimum 4-sample Blackman-Harris Window.

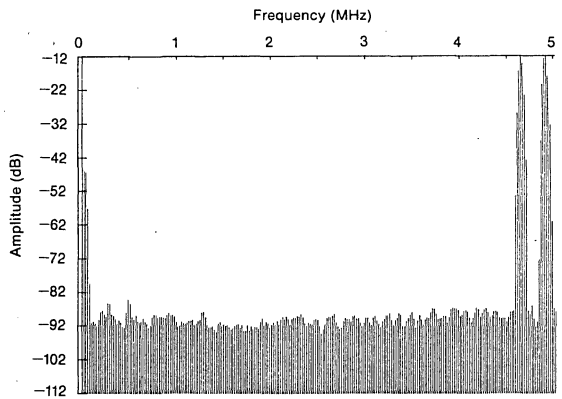
Sample Rate = 10MHz, Input Voltage = Half-Scale (−6dB)



	Level re: Full-Scale (dB)
4.8438MHz Fundamental =	−6.8
Harmonics: 2f =	−85.4
3f =	−89.1
4f =	−90.1
SINAD =	64.0dB
TND =	−65.2dBC
THD =	−70.2dBC



	Level re: Full-Scale (dB)
0.6055MHz Fundamental =	−6.5
Harmonics: 2f =	−86.6
3f =	−84.2
4f =	−84.9
SINAD =	63.7dB
TND =	−65.1dBC
THD =	−69.2dBC

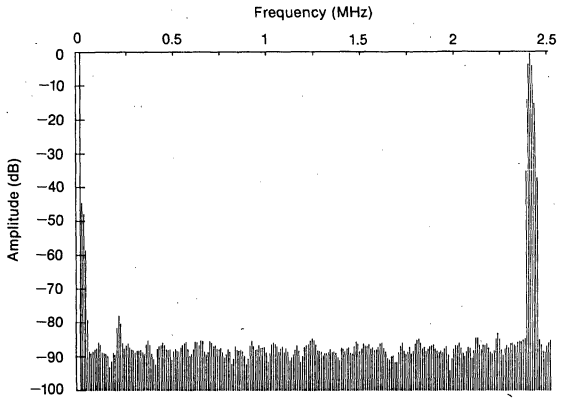


	Level re: Full-Scale (dB)
F_1: 4.9219MHz =	−12.35
F_2: 4.6484MHz =	−12.45
Peak Envelope =	−6.7
IMD: 0.2734MHz =	−85.5
0.4883MHz =	−84.5
4.7656MHz =	−86.3

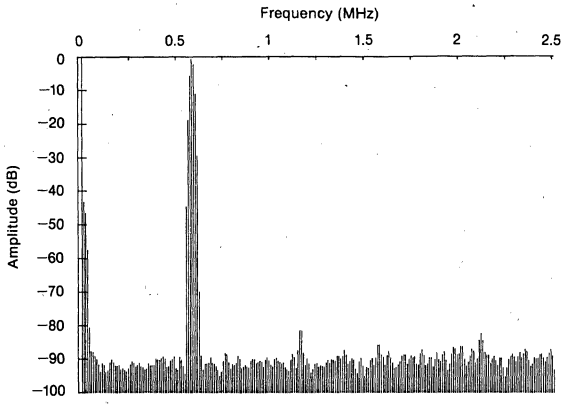
TYPICAL FFT SPECTRAL PERFORMANCE (CONT)

All FFT data: 512-point FFT, 10-sample average; minimum 4-sample Blackman-Harris Window.

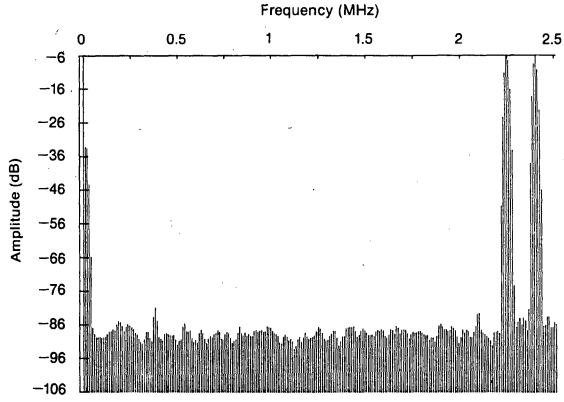
Sample Rate = 5MHz, Input Voltage = Full-Scale (0dB)



	Level re: Full-Scale (dB)
2.4121MHz Fundamental =	−0.6
Harmonics: 2f =	−77.9
3f =	−83.1
4f =	−85.3
SINAD =	67.3dB
TND =	−68.5dBC
THD =	−73.3dBC



	Level re: Full-Scale (dB)
0.5859MHz Fundamental =	−0.7
Harmonics: 2f =	−81.4
3f =	−87.2
4f =	−87.0
SINAD =	69.6dB
TND =	−70.7dBC
THD =	−76.1dBC

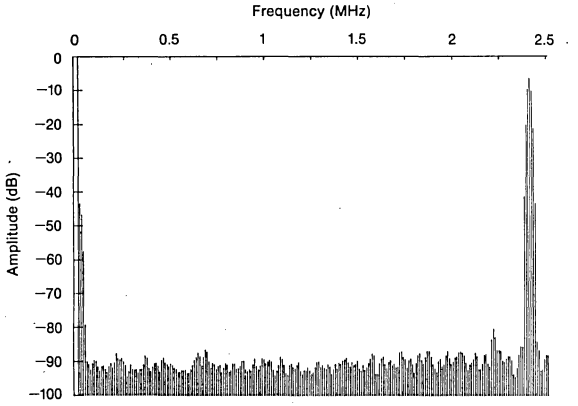


	Level re: Full-Scale (dB)
F_1: 2.2461MHz =	−6.3
F_2: 2.4023MHz =	−6.4
Peak Envelope =	−0.7
IMD: 0.3809MHz =	−81.2
2.0996MHz =	−82.9
2.4707MHz =	−83.9

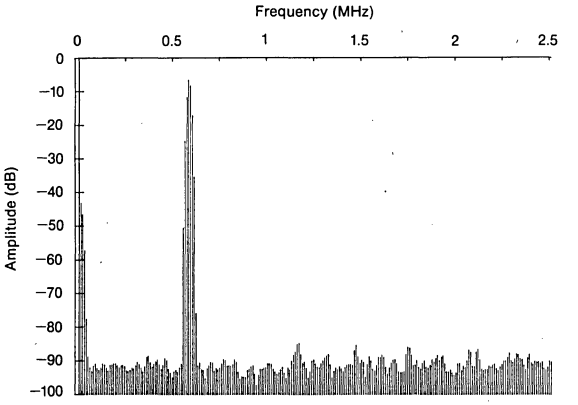
TYPICAL FFT SPECTRAL PERFORMANCE (CONT)

All FFT data: 512-point FFT, 10-sample average; minimum 4-sample Blackman-Harris Window.

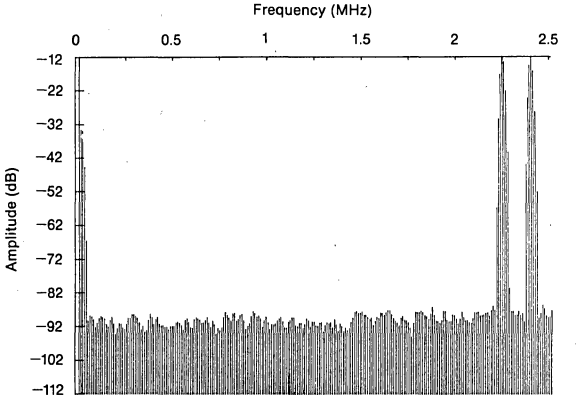
Sample Rate = 5MHz, Input Voltage = Half-Scale (−6dB)



	Level re: Full-Scale (dB)
2.4121MHz Fundamental =	−6.6
Harmonics: 2f =	−87.6
3f =	−80.4
4f =	−88.3
SINAD =	64.3dB
TND =	−65.7dBC
THD =	−69.9dBC



	Level re: Full-Scale (dB)
0.5859MHz Fundamental =	−6.6
Harmonics: 2f =	−84.6
3f =	−85.9
4f =	−87.8
SINAD =	64.8dB
TND =	−65.9dBC
THD =	−71.3dBC



	Level re: Full-Scale (dB)
F_1: 2.2461MHz =	−12.4
F_2: 2.4023MHz =	−12.4
Peak Envelope =	−6.8
IMD: 1.6406MHz =	−87.5
1.8750MHz =	−86.7
2.4609MHz =	−86.0

DIGITIZING INPUT WAVEFORMS

The response of the ADC600 is illustrated by the digitized waveforms of Figure 10. The 4.99MHz sine wave near the Nyquist limit is virtually identical to much lower frequency sine wave input. The under-sampled 19.999MHz sine wave illustrates the ADC600's excellent analog input full-power bandwidth. Figure 11 shows a block diagram of this high-speed digitizer.

HISTOGRAM TESTING

Histogram testing is used to test differential nonlinearity of the ADC600. This system block diagram is shown in Figure 12 and histogram test results for a typical converter are shown in Figure 13. Note that differential nonlinearity is 1/2LSB at 200Hz and it shows virtually no degradation near the Nyquist limit of 5MHz; there are no missing codes present and the peak nonlinearity does not exceed 1LSB. Histogram testing is a useful performance indicator as the width of all codes can be determined.

SPECTRUM ANALYZER TESTING

A beat-frequency technique (Figure 14) can be used to view digitized waveforms on an oscilloscope and, with care, this technique can also be used for testing high-speed ADC dynamic characteristics with an analog spectrum analyzer.

In this method a test signal is digitized by the ADC600 and the output digital data is latched into an external ECL latch by the converter Data Valid output pulse driving a divide-by-N counter. The holding register drives a 12-bit video-speed DAC which reconstructs the digital signal back into an analog replica of the ADC600 input. This analog signal also includes distortion products and noise resulting from the digitization, which can be viewed on an ordinary RF spectrum analyzer. Typical results are shown in Figures 15 and 16.

It is important to realize that the distortion and noise measured by this technique include not only that from the ADC600, but also the entire analog-to-analog test

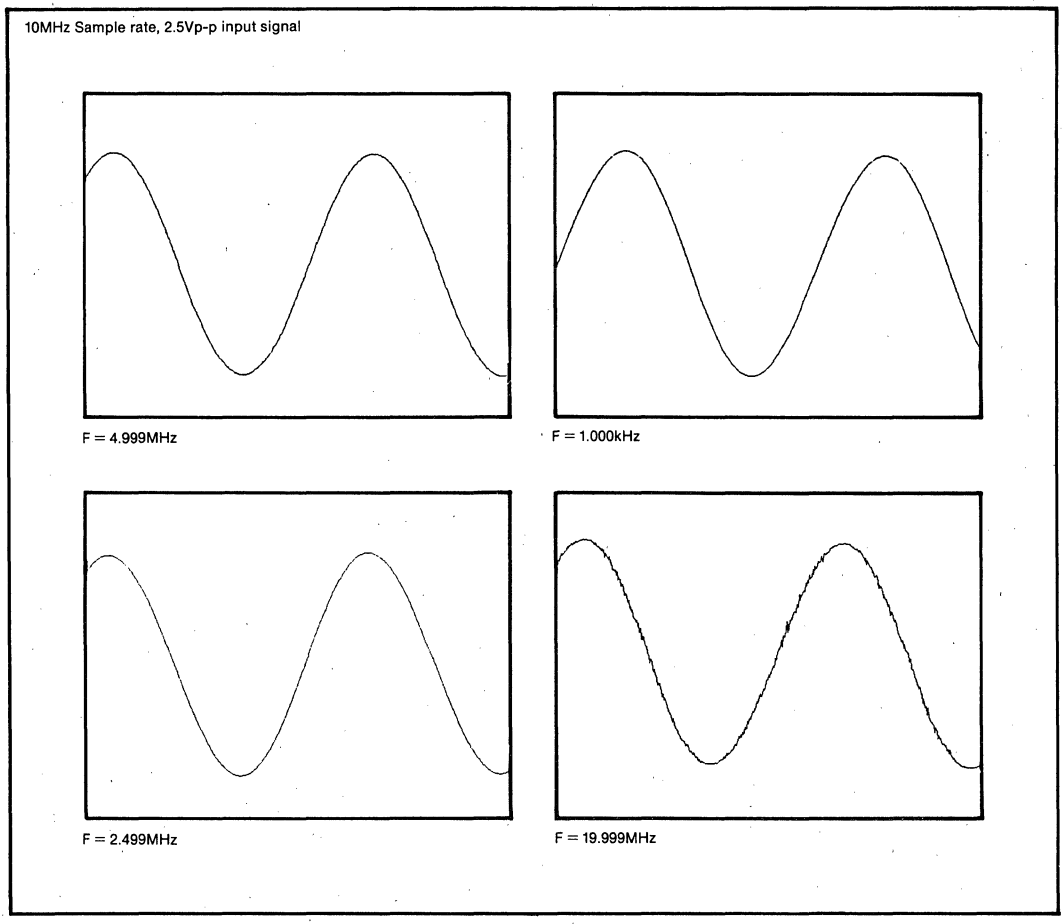


FIGURE 10. Digitized Waveforms (512 points).

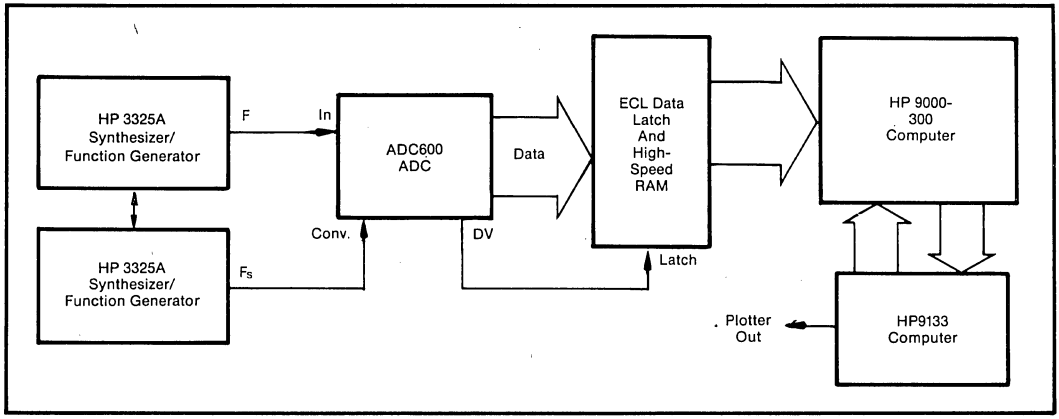


FIGURE 11. High-Speed Digitizer.

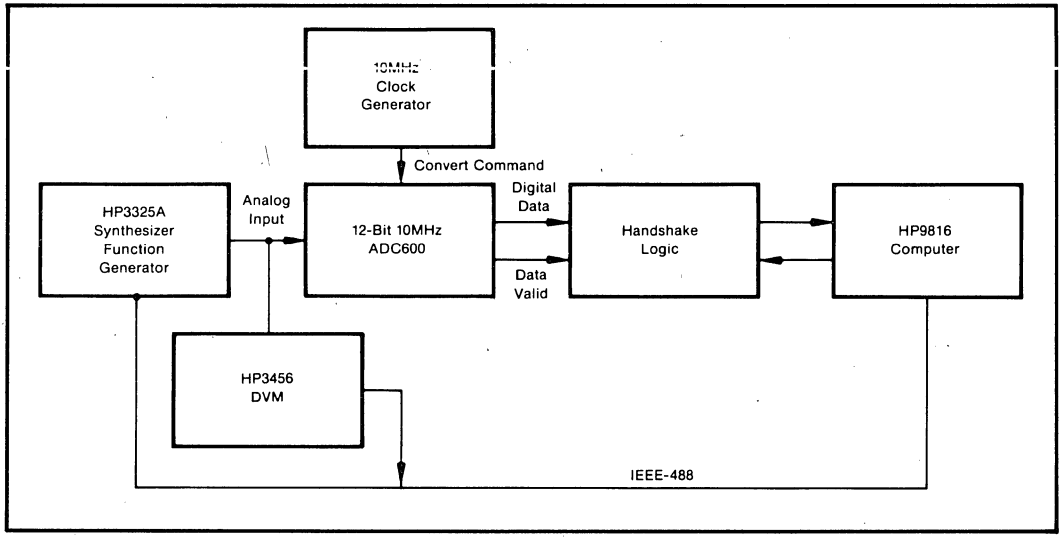


FIGURE 12. Block Diagram of Histogram Test.

system. Nonlinearity of the reconstruction circuit must be very low to measure a high performance ADC, and this places severe requirements on the DAC, deglitcher, and buffer amplifiers.

Using the high-speed video DAC63 in the analog reconstruction circuit allows excellent test circuit linearity to be achieved. Clocking the DAC (demodulating) at f_C/N allows a longer settling time and keeps linearity high in the digital-to-analog portion of the test circuit. Spectrum analyzer dynamic range can be a limiting factor in this method and a sharp notch filter can be used to attenuate the high-level fundamental frequency. Attenuating the fundamental allows the spectrum analyzer to be used on a more sensitive range without generating distortion products within the input of the analyzer.

Note that even though the signal is demodulated at a frequency of sample rate/N (here N = 2 or 4), the distortion products still maintain a correct frequency relationship to the fundamental. While this analog technique shows excellent performance, it cannot exclude some distortion products unavoidably generated within the analog reconstruction portion of the test system. For this reason, the digital FFT technique is capable of more accurate high-speed analog/digital converter dynamic performance measurements.

TIMING

The ADC600 generates all necessary timing signals in laser-trimmed submodules. Only the timing between Convert Command, Output Data, and Data Valid must

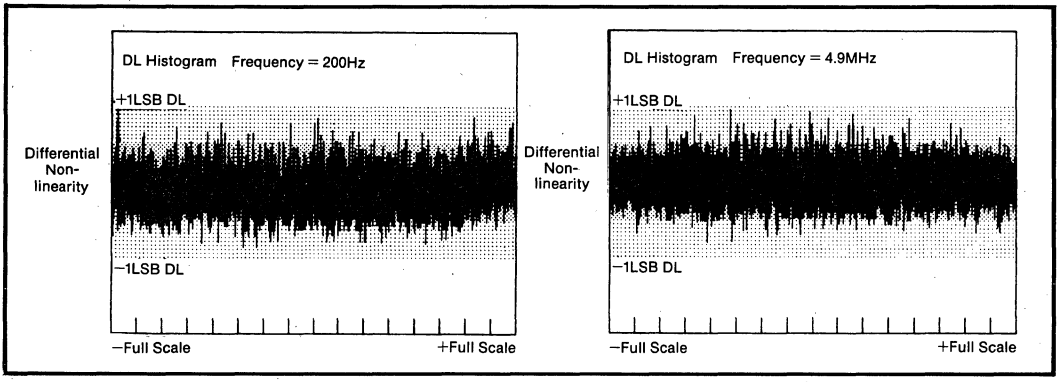


FIGURE 13. Histogram Test Results (10MHz Sample Rate).

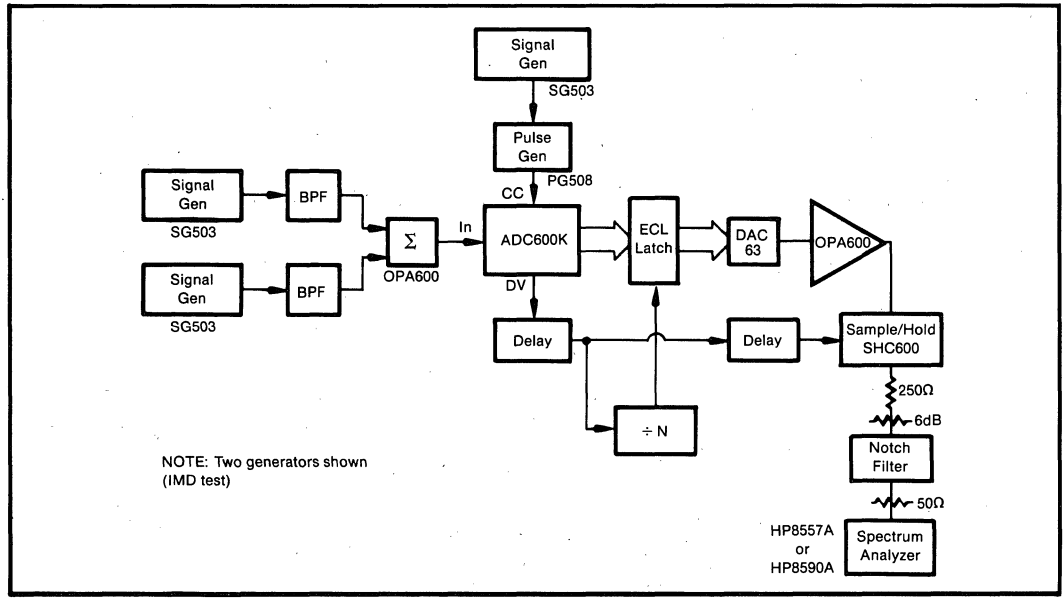


FIGURE 14. Analog-to-Analog Spectral Analysis by Beat-Frequency Techniques.

be considered. Proper timing is shown in Figure 17. The output data **cannot** be timed by the conversion clock, since the data from the 12-bit adder is not guaranteed until the Data Valid pulse is generated.

Data should be latched into an external 12-bit ECL register that can operate reliably with a set-up time of 5ns minimum (Figure 18).

Logic conversion to TTL can be accomplished by logic level translator ICs (such as 10125 or 10124), but care must be exercised, since TTL is very noisy and maintaining a clean analog signal can be difficult. To preserve the low noise of ECL logic, any conversion to TTL should be done on a separate circuit board which is driven by differential ECL drivers.

1. FAST™ Applications Handbook, 1987. Fairchild Semiconductor Corp.
2. *Fairchild Advanced CMOS Technology*, Technology Seminar Notes, 1985.
3. *Impedance Matching Tweaks Advance CMOS IC Testing*, Gerald C. Cox, Electronic Design, April, 1987.
4. *Grounding for Electromagnetic Compatibility*, Jerry H. Bogar, Design News, 23 February, 1987.

THERMAL REQUIREMENTS

The ADC600 is tested and specified over a temperature range of 0°C to +70°C (K grade) and −40°C to +85°C (B grade). The converters are tested in a forced-air environment with a 10 SCFM air flow. The ADC600 can be operated in a normal convection ambient-air environment if submodule case temperature does not exceed the upper limit of its specification.[1]

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient temperatures. Worst-case junction temperature (θ_{JC}) and top-surface submodule (θ_{CA}) are presented in Table I to aid the designer in determining cooling requirements.

1. *Maximizing Heat Transfer from PCBs*, Machine Design, March 26, 1987, Jeilong Chung.

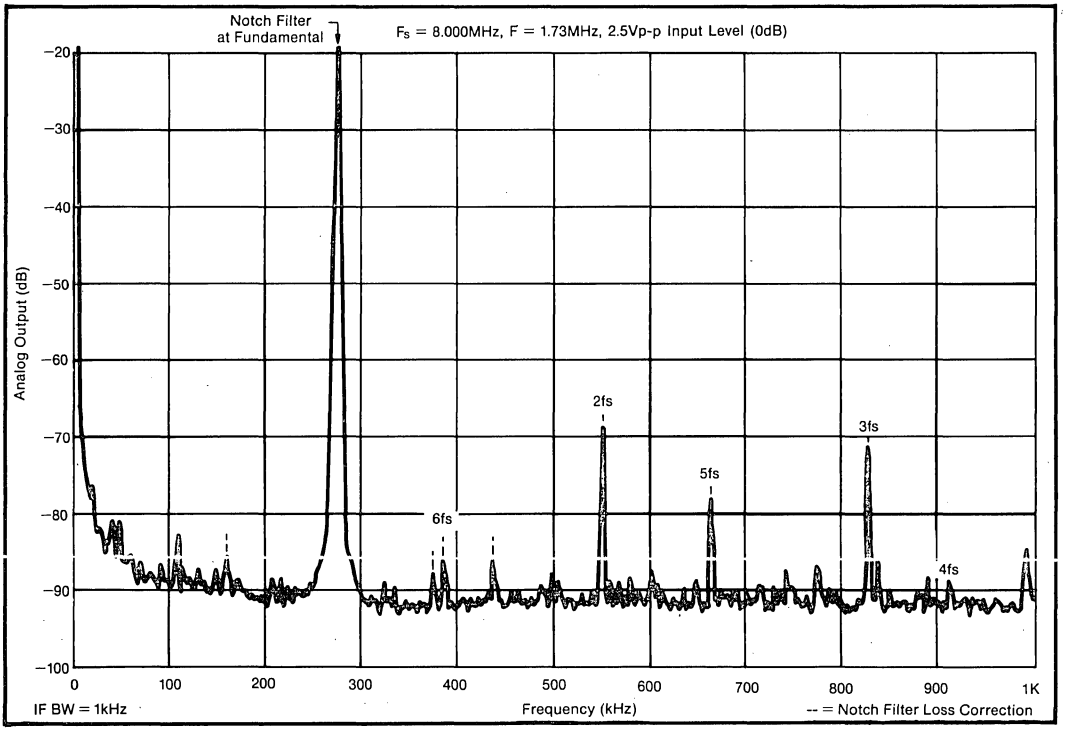


FIGURE 15. Analog-to-Analog Harmonic Distortion.

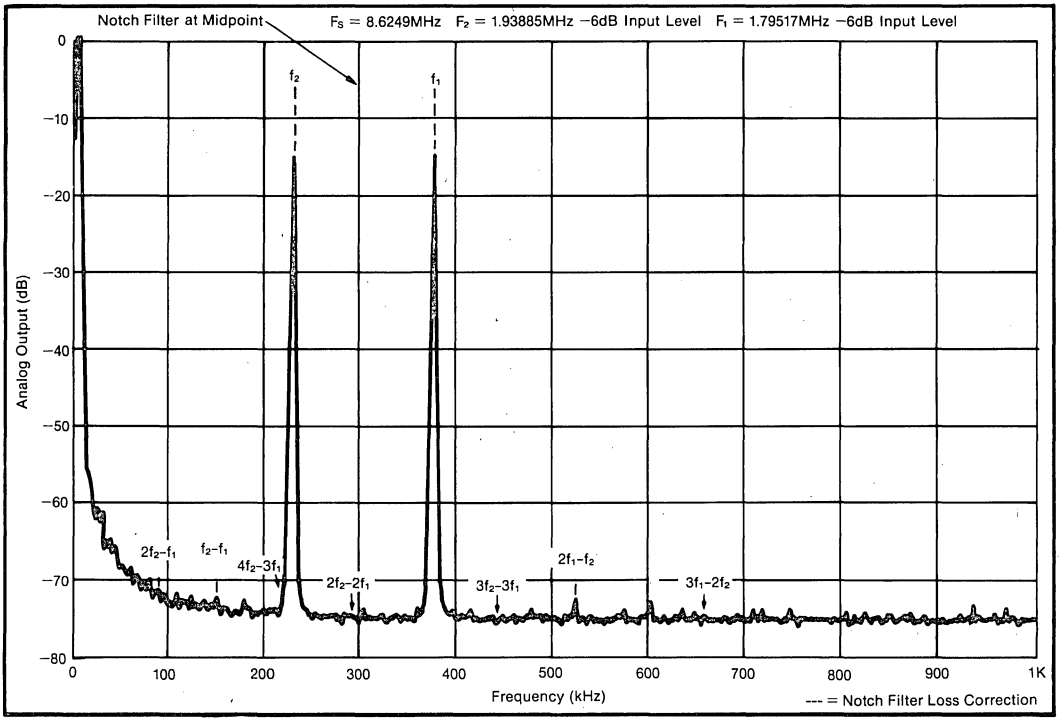


FIGURE 16. Analog-to-Analog Two-Tone IMD.

TABLE I. Cooling Requirement Factors.

Submodule	Power Dissipation (W)	25°C Ambient Air Normal Convection θ_{JC} (°C/W)	θ_{CA} (°C/W)	DIP Package Type
SHC600	1.5	28.7	23.3	24-pin
SM10343	1.6	17.5	24.4	24-pin
SM10344	1.6	10.6	21.3	32-pin
SM10345	1.6	17.5	21.9	24-pin
SM10346	2.1	8.6	16.7	40-pin
SM10347	1.1	17.3	28.2	40-pin

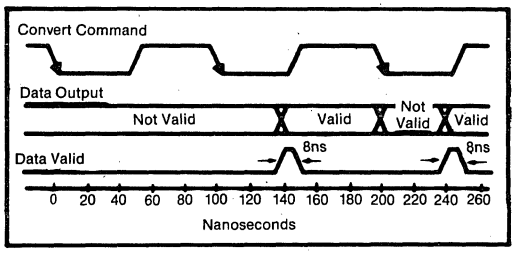


FIGURE 17. ADC600 Timing Diagram.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table II is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883. Table III shows the board-level screening flow for ADC600Q.

TABLE II. Screening Flow for ADC600Q (active components).

Screen	MIL-STD-883, Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
Electrical Test	Burr-Brown test procedure	
High Temperature Storage (Stabilization Bake)	1008	24 hour, +125°C
Temperature Cycling	1010	10 cycles, −55°C to −125°C
Constant Acceleration	2001, A	2000 G; Y Axis only
Burn-In	1015, D	160 hour, +85 or +70°C, steady-state
Hermeticity: Fine Leak Gross Leak	1014, C	bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
External Visual	Burr-Brown QC5150	

TABLE III. Screening Flow for ADC600Q (board level).

Screen	MIL-STD-883, Method, Condition	Screening Level
External Visual	Burr-Brown QC Specification	
Electrical Test	Burr-Brown Data Sheet	
Stablilization Bake	1008	24 hour, +125°C
Burn-In	1015, D	160 hour, +85°C or +70°C steady-state
Final Electrical	Burr-Brown Data Sheet	
Final External Visual	Burr-Brown QC Specification	

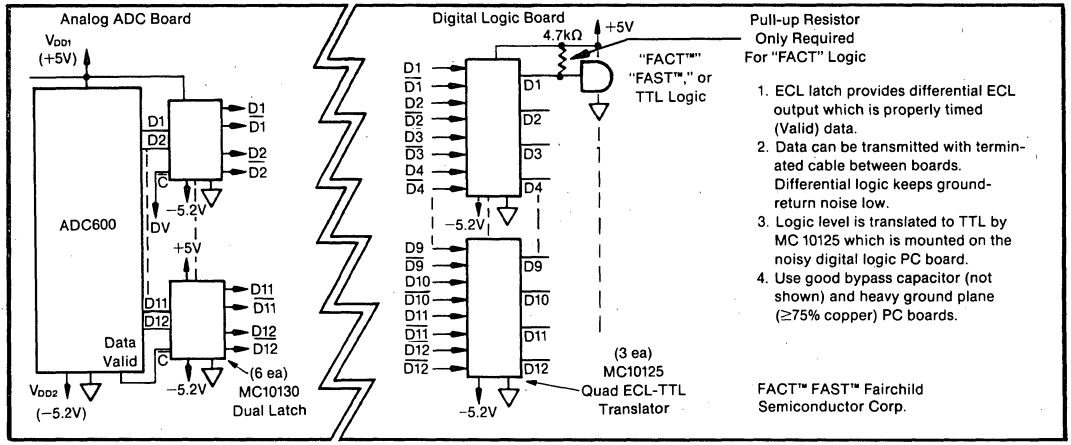


FIGURE 18. ECL/TTL Logic Interface.

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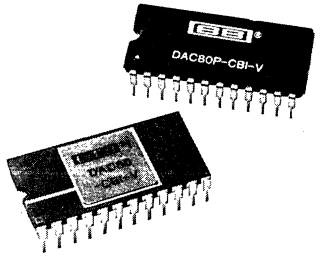
BURR-BROWN®



DAC80
DAC80P

Monolithic 12-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- INDUSTRY STANDARD PINOUT
- LOW POWER DISSIPATION: 345mW
- FULL ±10V SWING WITH V_{CC} = ±12VDC
- DIGITAL INPUTS ARE TTL- AND CMOS-COMPATIBLE
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES
- SINGLE-CHIP DESIGN
- ±1/2LSB MAXIMUM NONLINEARITY, 0°C to +70°C
- GUARANTEED MONOTONICITY, 0°C to +70°C
- TWO PACKAGE OPTIONS: Hermetic side-brazed ceramic and low-cost molded plastic
- SETTLING TIME: 4μs max to ±0.01% of Full Scale

DESCRIPTION

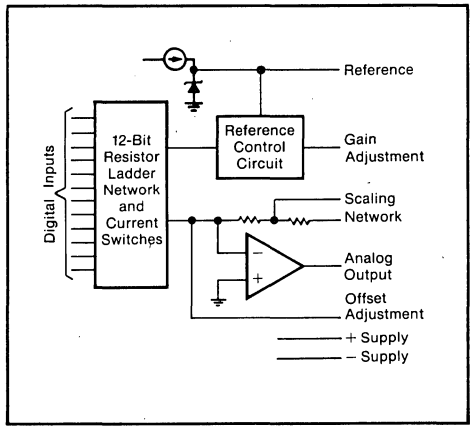
This monolithic digital-to-analog converter is pin-for-pin equivalent to the industry standard DAC80, first introduced by Burr-Brown. Its single-chip design includes the output amplifier and provides a highly stable reference capable of supplying up to 2.5mA to an external load without degradation of D/A performance.

This converter uses proven circuit techniques to provide accurate and reliable performance over temperature and power supply variations. The use of a buried zener diode as the basis for the internal reference contributes to the high stability and low noise of the device. Advanced methods of laser trimming result in precision output current and output amplifier feedback resistors, as well as low integral and differential linearity errors. Innovative circuit design enables the DAC80 to operate at supply voltages as low as ±11.4V with no loss in performance or accuracy over any range of output voltage. The lower power dissipation of this 118-mil by 121-mil chip results in higher reliability and greater long term stability.

Burr-Brown has further enhanced the reliability of the monolithic DAC80 by offering a hermetic, side-brazed, ceramic package. In addition, ease of use has been enhanced by eliminating the need for a +5V logic power supply.

For applications requiring both reliability and low cost, the DAC80P in a molded plastic package offers the same electrical performance over temperature as the ceramic model. The DAC80P is available with either voltage or current output.

For designs that require a wider temperature range, see Burr-Brown models DAC85H and DAC87H. For designs that require complementary coded decimal inputs, see Burr-Brown model DAC80-CCD-V (-I).



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SPECIFICATIONS

ELECTRICAL

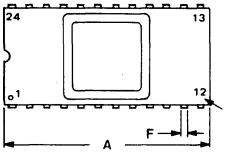
Typical at +25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

MODEL	DAC80			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT				
Resolution			12	Bits
Logic Levels (0°C to +70°C)[1]:				
V_{IH} (Logic "1")	+2		+16.5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IN} = +2.4V)			+20	µA
I_{IL} (V_{IN} = +0.4V)			−180	µA
ACCURACY (at +25°C)				
Linearity Error		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	±3/4	LSB
Gain Error[2]		±0.1	±0.3	%
Offset Error[2]		±0.05	±0.15	% of FSR[3]
DRIFT (0°C to +70°C)[4]				
Total bipolar drift (includes gain, offset, and linearity drifts)		±10	±25	ppm of FSR/°C
Total Error Over 0°C to +70°C[5]				
Unipolar		±0.06	±0.15	% of FSR
Bipolar		±0.06	±0.12	% of FSR
Gain: Including Internal Reference		±10	±30	ppm/°C
Excluding Internal Reference		±5	±10	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	±3/4	LSB
Linearity Error 0°C to +70°C		±1/4	±1/2	LSB
Monotonicity Guaranteed	0		+70	°C
CONVERSION SPEED, V_{OUT} models				
Settling Time to ±0.01% of FSR				
For FSR change (2kΩ ‖ 500pF load)				
with 10kΩ Feedback		3	4	µs
with 5kΩ Feedback		2	3	µs
For 1LSB Change		1		µs
Slew Rate	10			V/µs
CONVERSION SPEED, I_{OUT} models				
Settling Time to ±0.01% of FSR				
For FSR change: 10Ω to 100Ω load		300		ns
1kΩ load		1		µs
ANALOG OUTPUT, V_{OUT} models				
Ranges	±2.5, ±5, ±10, +5, +10			V
Output Current[6]	±5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit to Common, Duration[7]		Indefinite		
ANALOG OUTPUT, I_{OUT} models				
Ranges: Bipolar	±0.96	±1.0	±1.04	mA
Unipolar	−1.96	−2.0	−2.04	mA
Output Impedance: Bipolar	2.6	3.2	3.7	kΩ
Unipolar	4.6	6.6	8.6	kΩ
Compliance	−2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	V
External Current (constant load)			2.5	mA
Drift vs Temperature		±10	±20	ppm/°C
Output Impedance		1		Ω
POWER SUPPLY SENSITIVITY				
V_{CC} = ±12VDC or ±15VDC		±0.002	±0.006	% FSR/ % V_{CC}
POWER SUPPLY REQUIREMENTS				
±V_{CC}	±11.4		±16.5	VDC
Supply Drain (no load): +V_{CC}		8	12	mA
−V_{CC}		15	20	mA
Power Dissipation (V_{CC} = ±15VDC)		345	480	mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	−25		+85	°C
Storage: Plastic DIP	−60		+100	°C
Ceramic DIP	−65		+150	°C

NOTES: (1) Refer to "Logic Input Compatibility" section. (2) Adjustable to zero with external trim potentiometer. (3) FSR means full scale range and is 20V for ±10V range, 10V for ±5V range for V_{OUT} models; 2mA for I_{OUT} models. (4) To maintain drift spec, internal feedback resistors must be used. (5) Includes the effects of gain, offset and linearity drift. Gain and offset errors externally adjusted to zero at +25°C. (6) For ±V_{CC} less than ±12VDC, limit output current load to ±2.5mA to maintain ±10V full scale output voltage swing. For output range of ±5V or less, the output current is ±5mA over entire ±V_{CC} range. (7) Short circuit current is 40mA, max.

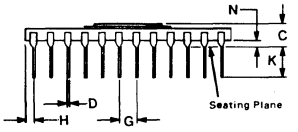
MECHANICAL

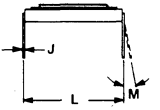
Hermetic Ceramic 24-Lead DIP



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.





PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

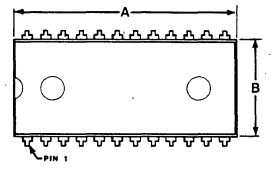
HERMETICITY: Conforms to Method 1014, Condition A1 or A2 (fine leak) and Condition C (gross leak). Metal lid of package is connected to −V_{CC} internally.

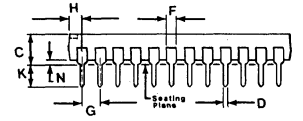
CASE: Ceramic

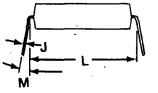
MATING CONNECTOR: 0245MC
WEIGHT: 4.1 grams (0.15 oz.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

Molded Plastic 24-Lead DIP







NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

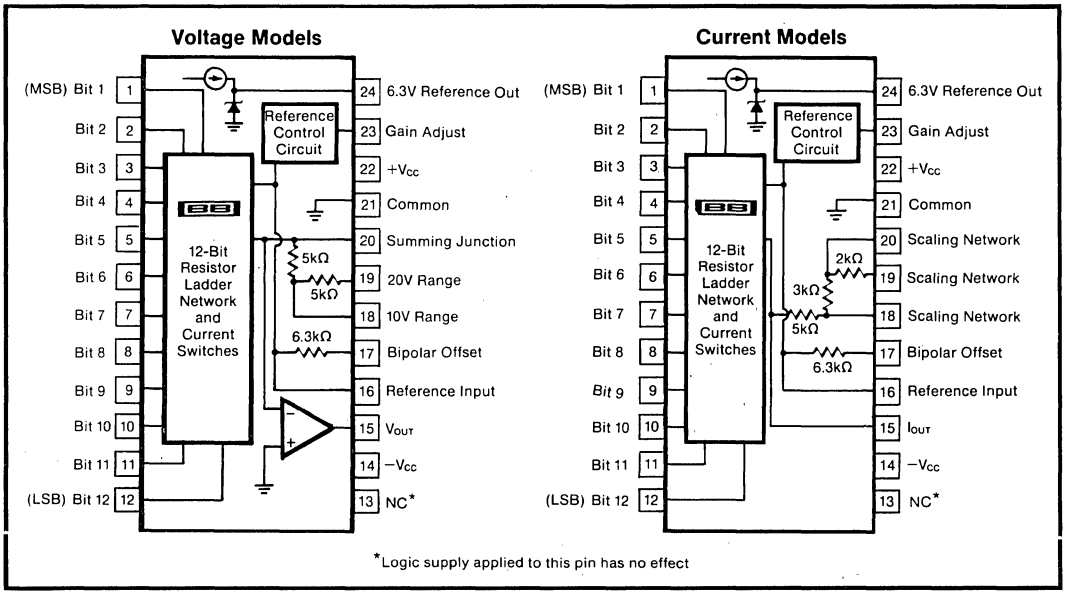
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CASE: Plastic

MATING CONNECTOR: 0245MC
WEIGHT: 3.7 grams (0.13 oz.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.238	1.283	31.32	32.69
B	.538	.578	13.67	14.61
C	.169	.224	4.29	5.70
D	.016	.023	0.36	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.016	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

FUNCTIONAL DIAGRAM AND PIN ASSIGNMENTS



*Logic supply applied to this pin has no effect

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC80 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB, or CTC (see Table I).

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB ↓ ↓	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-1LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	1/2 Full Scale -1LSB	-1LSB	-Full Scale
111111111111	Zero	-Full Scale	Zero

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

ORDERING INFORMATION

Model	Output	Package
DAC80-CBI-I	Current	Ceramic
DAC80-CBI-V	Voltage	Ceramic
DAC80P-CBI-I	Current	Plastic
DAC80P-CBI-V	Voltage	Plastic
DAC80Z-CBI-I*	Current	Ceramic
DAC80Z-CBI-V*	Voltage	Ceramic

*DAC80Z is not recommended for new designs; both standard DAC80 and DAC80P now operate over extended power supply range.

ABSOLUTE MAXIMUM RATINGS

+Vcc to Common	0V to +18V
−Vcc to Common	0V to −18V
Digital Data Inputs to Common	−1V to +18V
Reference Output to Common	±Vcc
Reference Input to Common	±Vcc
Bipolar Offset to Common	±Vcc
10V Range R to Common	±Vcc
20V Range R to Common	±Vcc
External Voltage to DAC Output	−5V to +5V
Lead Temperature, Soldering	+300°C, 10s
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}: Plastic DIP	100°C/W
Ceramic DIP	65°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C and +70°C; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

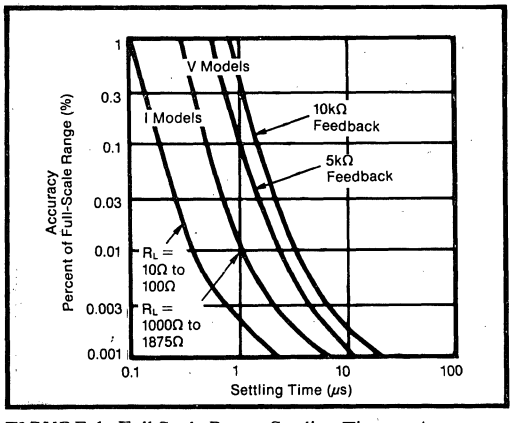


FIGURE 1. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111 . . . 11 to 1000 . . . 00), the point at which the worst case settling time occurs.

Current Output Models

Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to −2V (see Figures 11 and 12).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage range of ±1V and 0 to −2V. (See Figures 11 and 12).

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages (see Figure 2).

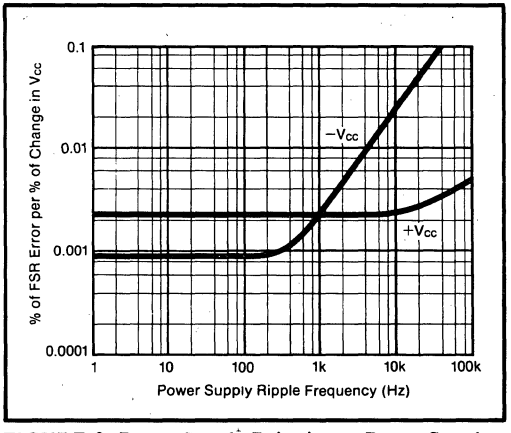


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 2.5mA.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

LOGIC INPUT COMPATIBILITY

DAC80 digital inputs are TTL, LSTTL and 4000B, 54/74HC CMOS compatible. The input switching threshold remains at the TTL threshold over the entire supply range.

Logic "0" input current over temperature is low enough to permit driving DAC80 directly from outputs of 4000B and 54/74C CMOS devices.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Connect power supply voltages as shown in Figure 3. For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown. These capacitors (1μF tantalum) should be located close to the DAC80.

±12V OPERATION

All DAC80 models can operate over the entire power supply range of ±11.4V to ±16.5V. Even with supply levels dropping to ±11.4V, the DAC80 can swing a full ±10V range, provided the load current is limited to ±2.5mA. With power supplies greater than ±12V, the DAC80 output can be loaded up to ±5mA. For output swing of ±5V or less, the output current is ±5mA, min. over the entire V_{CC} range.

No bleed resistor is needed from $+V_{CC}$ to pin 24, as was needed with prior hybrid Z versions of DAC80. Existing ±12V applications that are being converted to the monolithic DAC80 must omit the resistor to pin 24 to insure proper operation.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted.

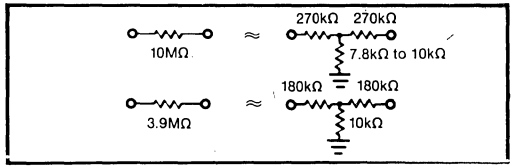


FIGURE 4. Equivalent Resistances.

Existing applications that are converting to the monolithic DAC80 must change the gain trim resistor on pin 23 from 33MΩ to 10MΩ to insure sufficient adjustment range. Pin 23 is a high impedance point and a 0.001μ1F to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figure 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A operation.

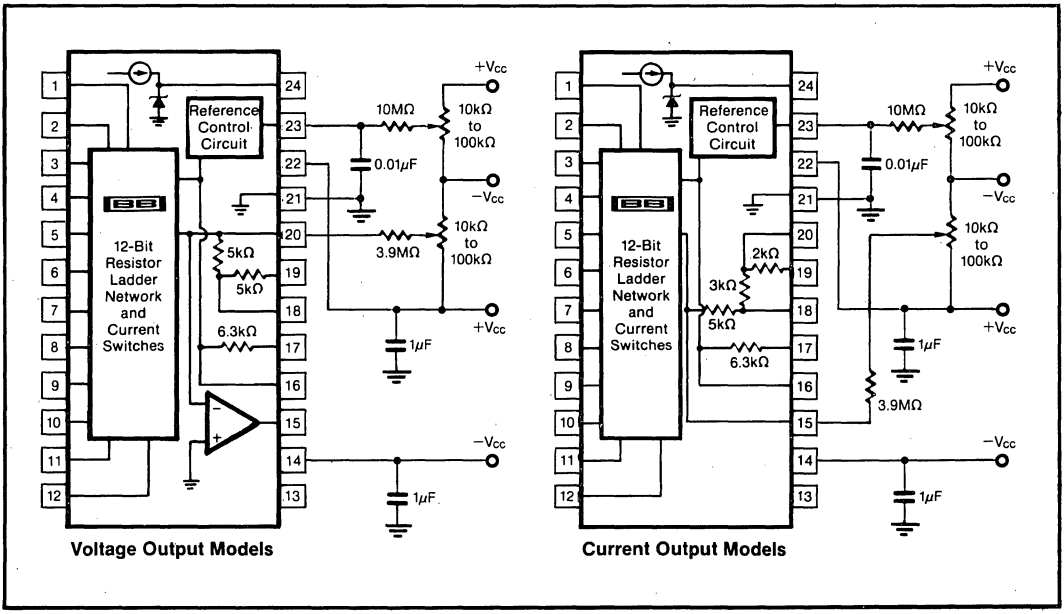


FIGURE 3. Power Supply and External Adjustment Connection Diagrams

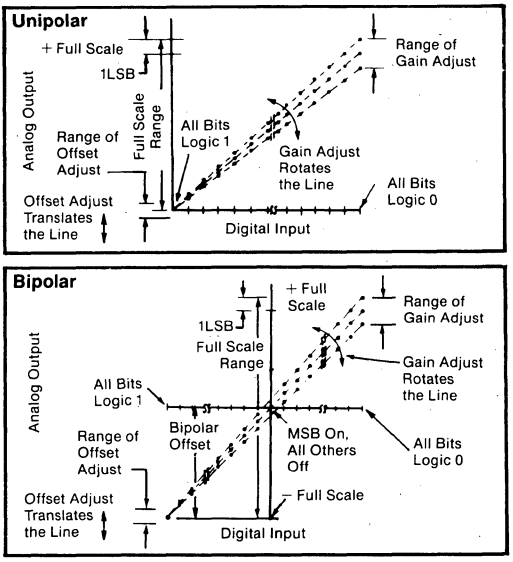


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar and Bipolar D/A Converter.

Offset Adjustment

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.

TABLE II. Digital Input/Analog Output.

DIGITAL INPUT	ANALOG OUTPUT			
	VOLTAGE *		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output. Adjust the Gain potentiometer for this positive full scale output. See Table II for positive full scale voltages and currents.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

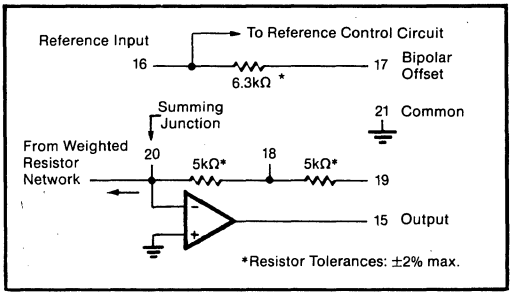


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other internal device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 4μs for the 20V range and 3μs for the 10V range.

TABLE III. Output Voltage Range Connections for Voltage Models.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

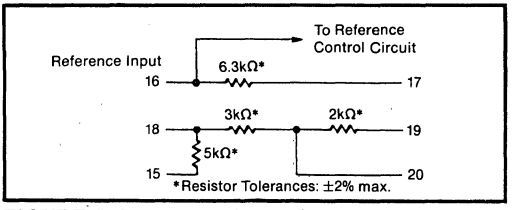


FIGURE 7. Internal Scaling Resistors.

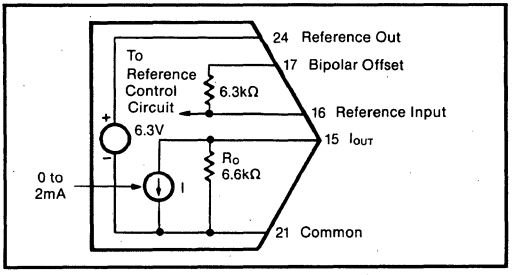


FIGURE 8. Current Output Model Equivalent Output Circuit.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving An External Op Amp

The current output model DAC80 will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage. See Figure 9.

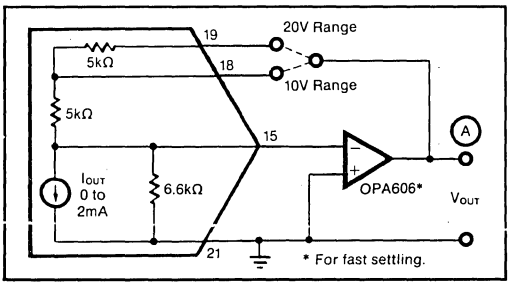


FIGURE 9. External Op-Amp—Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges. See Figure 10. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C plus R_F drift to total drift.

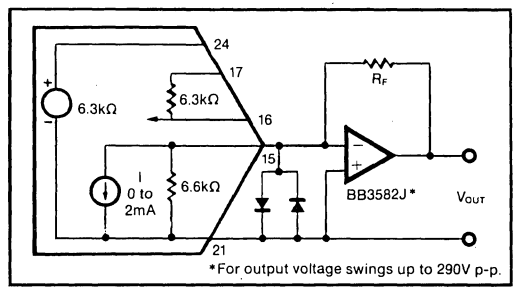


FIGURE 10. External Op-Amp—Using External Feedback Resistors.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 11 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA\ [(R_L \times R_O) \div (R_L + R_O)]$$

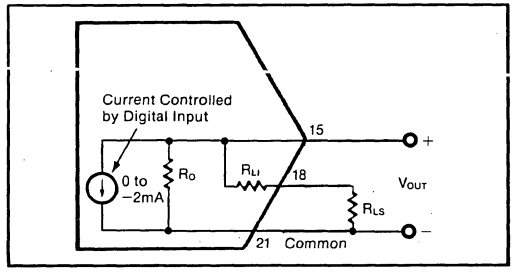


FIGURE 11. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

The unipolar output impedance R_O equals 6.6kΩ (typ) and R_{LI} is the internal load resistance of 968Ω (derived by connecting pin 15 to pin 20 and pin 18 to 19). By choosing $R_{LS} = 210Ω$, $R_L = 1178Ω$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of 0 to −2V. Since R_O is not exact, initial trimming per Figure 3 may be necessary; also R_{LS} may be trimmed.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA\ [(R_O \times R_L) \div (R_O + R_L)]$$

By connecting pin 17 to 15, the output current becomes bipolar (±1mA) and the output impedance R_O becomes 3.2kΩ (6.6kΩ in parallel with 6.3kΩ). R_{LI} is 1200Ω (derived by connecting pin 15 to 18 and pin 18 to 19). By choosing $R_{LS} = 255Ω$, $R_L = 1455Ω$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of ±1V. As indicated above, trimming may be necessary.

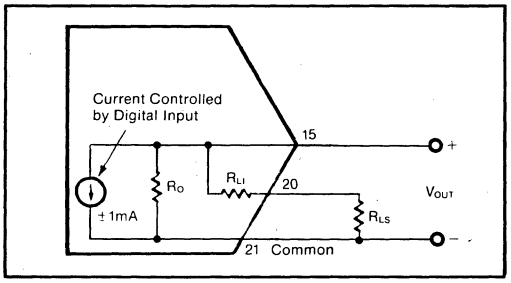
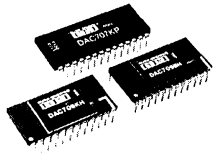


FIGURE 12. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

BURR-BROWN®



DAC705/706/707
DAC708/709

Microprocessor-Compatible 16-BIT DIGITAL-TO-ANALOG CONVERTERS

FEATURES

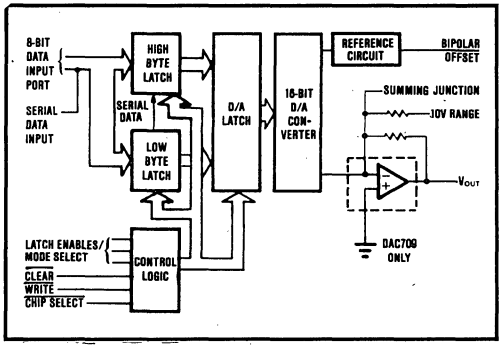
- TWO-CHIP CONSTRUCTION
- HIGH-SPEED 16-BIT PARALLEL, 8-BIT (BYTE) PARALLEL, AND SERIAL INPUT MODES
- DOUBLE-BUFFERED INPUT REGISTER CONFIGURATION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY:
  Linearity Error ±0.003% of FSR max
  Differential Linearity Error ±0.006% of FSR max
- MONOTONIC (TO 14 BITS) OVER SPECIFIED TEMPERATURE RANGE
- HERMETICALLY SEALED
- LOW COST PLASTIC VERSIONS AVAILABLE (DAC707JP/KP)

DESCRIPTION

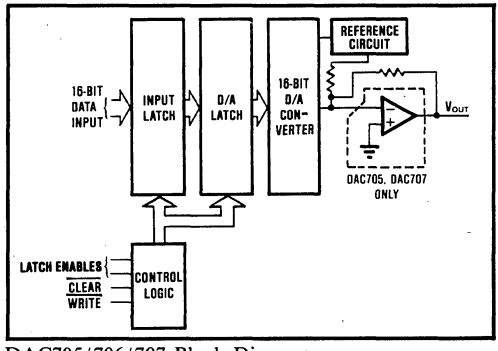
The DAC708 and DAC709 are 16-bit converters designed to interface to an 8-bit microprocessor bus. 16-bit data is loaded in two successive 8-bit bytes into parallel 8-bit latches before being transferred into the D/A latch. The DAC708 and DAC709 are current and voltage output models respectively and are in 24-pin hermetic DIPs. Input coding is Binary Two's Complement (bipolar) or Unipolar Straight Binary (unipolar, when an external logic inverter is used to invert the MSB). In addition, the DAC708/-709 can be loaded serially (MSB first).

The DAC705, DAC706, and DAC707 are designed to interface to a 16-bit bus. Data is written into a 16-bit latch and subsequently the D/A latch. The DAC705 and DAC707 are voltage output models. DAC706 is a current output model. Outputs are bipolar only (current or voltage) and input coding is Binary Two's Complement (BTC).

All models have Write and Clear control lines as well as input latch enable lines. In addition, DAC708 and DAC709 have Chip Select control lines. In the bipolar mode, the Clear input sets the D/A latch to give zero voltage or current output. They are all 14-bit accurate and are complete with reference, and, for the DAC705, DAC707, and DAC709, a voltage output amplifier.



DAC708/709 Block Diagram



DAC705/706/707 Block Diagram

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up unless otherwise noted.

MODEL	DAC707JP			DAC705/706/707/708/709KH, DAC707KP			DAC705/706/707/708/ 709BH, SH			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT										
DIGITAL INPUT										
Resolution			16			*			*	Bits
Bipolar Input Code (all models)		Binary Two's Complement			*			*		
Unipolar Input Code[1] (DAC708/709 only)					Unipolar Straight Binary			*		
Logic Levels[2]: V_{IH}	+2.0		+5.5	*		*	*		*	V
V_{IL}	−1.0		+0.8	*		*	*		*	V
I_{IH} (V_I = +2.7V)			1			*			*	μA
I_{IL} (V_I = +0.4V)			1			*			*	μA
TRANSFER CHARACTERISTICS										
ACCURACY[3]										
Linearity Error		±0.003	±0.006		±0.0015	±0.003		*	*	% of FSR[4]
Differential Linearity Error[5]		±0.0045	±0.012		±0.003	±0.006		*	*	% of FSR
at Bipolar Zero[5, 6]					±0.003	±0.006		±0.0015	±0.003	% of FSR
Gain Error[7]		±0.07	±0.30		*	±0.15		±0.05	±0.10	%
Zero Error[7]		±0.05	±0.1		*	*		*	*	% of FSR
Monotonicity Over Spec Temp Range	13			14			14			Bits
Power Supply Sensitivity: +V_{CC}, −V_{CC}		±0.0015	±0.006		*	*		*	±0.003	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*		*	*	% of FSR/%V_{DD}
DRIFT (over Spec Temp range[3])										
Total Error over Temp Range[8]		±0.08			*	±0.15		*	±0.10	% of FSR
Total Full Scale Drift		±10			*	±25		*	±15	ppm of FSR/°C
Gain Drift		±10	±30		*	±25		±7	±15	ppm/°C
Zero Drift: Unipolar (DAC708/709 only)					±2.5	±5		±1.5	±3	ppm of FSR/°C
Bipolar (all models)		±5	±15		*	±12		±4	±10	ppm of FSR/°C
Differential Linearity Over Temp[5]			±0.012			+0.009, −0.006			*	% of FSR
Linearity Error Over Temp[5]			±0.012			±0.006			*	% of FSR
SETTLING TIME (to ±0.003% of FSR)[9]										
Voltage Output Models										
Full Scale Step (2kΩ load)		4			*	8		*	8	μs
1LSB Step at Worst Case Code[10]		2.5			*	4		*	4	μs
Slew Rate		10			*			*		V/μs
Current Output Models										
Full Scale Step (2mA): 10 to 100Ω load					350			*		ns
1kΩ load					1			*		μs
OUTPUT										
VOLTAGE OUTPUT MODELS										
Output Voltage Range										
DAC709: Unipolar (USB Code)					0 to +10			*		V
Bipolar (BTC Code)					±5, ±10			*		V
DAC707 Bipolar (BTC Code)		±10			*			*		V
DAC705 Bipolar (BTC Code)					±5			*		V
Output Current	±5			*						mA
Output Impedance		0.15			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*		
CURRENT OUTPUT MODELS										
Output Current Range (±30% typ)										
DAC708: Unipolar (USB Code)					0 to −2			*		mA
Bipolar (BTC Code)					±1			*		mA
DAC706 Bipolar (BTC Code)					±1					mA
Unipolar Output Impedance (±30% typ)					4.0			*		kΩ
Bipolar Output Impedance (±30% typ)					2.45			*		kΩ
Compliance Voltage					±2.5			*		V
POWER SUPPLY REQUIREMENTS										
Voltage (all models): +V_{CC}	+13.5	+15	+16.5	*	*	*	*	*	*	V
−V_{CC}	−13.5	−15	−16.5	*	*	*	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	*	*	*	V
Current (No load, +15V supplies)										
Current Output Models: +V_{CC}					+10	+25		*	*	mA
−V_{CC}					−13	−25		*	*	mA
V_{DD}					+5	+10		*	*	mA
Voltage Ouptut Models: +V_{CC}		+16	+30		*	*		*	*	mA
−V_{CC}		−18	−30		*	*		*	*	mA
V_{DD}		+5	+10		*	*		*	*	mA

ELECTRICAL (CONT)

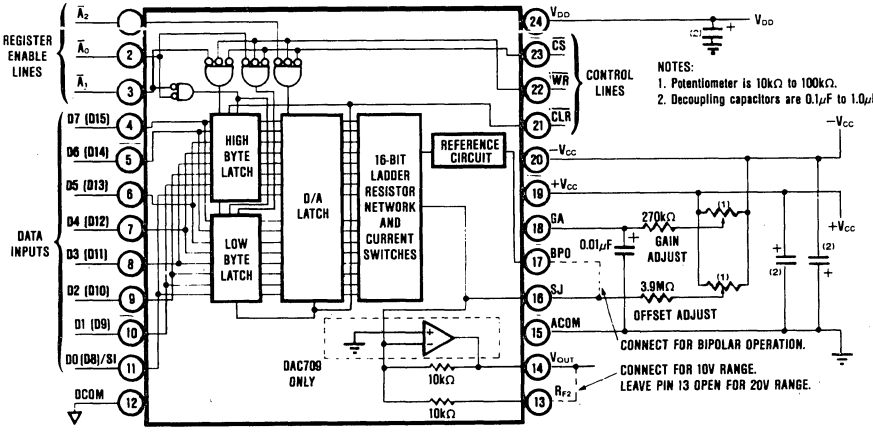
MODEL	DAC707JP			DAC705/706/707/708/709KH, DAC707KP			DAC705/706/707/708/ 709BH, SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS (CONT)										
Power Dissipation (±15V supplies)										
Current Output Models					370	800		*	*	mW
Voltage Output Models		535			*	950		*	*	mW
TEMPERATURE RANGE										
Specification: BH grades							−25		+85	°C
JP, KP, KH grades	0		+70	*		*				°C
SH grades							−55		+125	°C
Storage: Ceramic				−65		+150	−65		+150	°C
Plastic	−60		+100	*		*				°C

*Specification same as for models in column to the left.

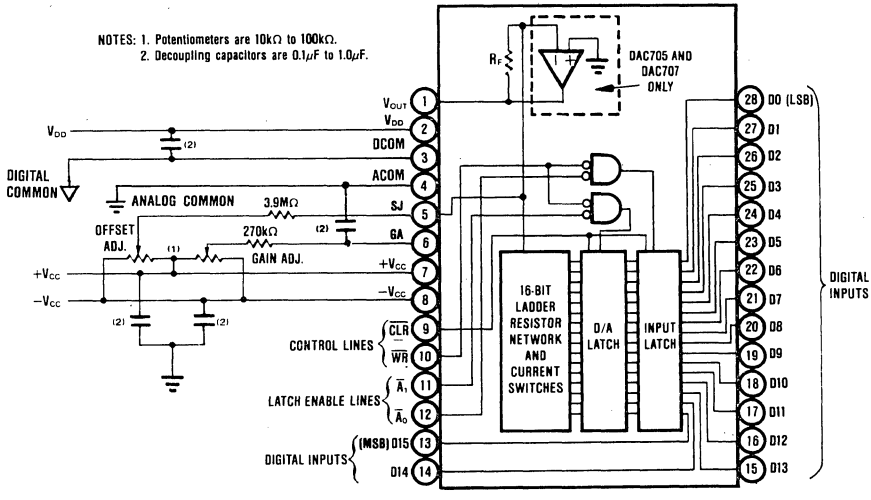
NOTES: (1) MSB must be inverted externally prior to DAC708/709 input. (2) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specified temperature range. (3) DAC706 and DAC708 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all tests. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) ±0.0015% of Full Scale Range is equal to 1 LSB in 16-bit resolution. ±0.003% of Full Scale Range is equal to 1 LSB in 15-bit resolution. ±0.006% of Full Scale Range is equal to 1 LSB in 14-bit resolution. (6) Error at input code 0000_H. (For unipolar connection on DAC708/709, the MSB must be inverted externally prior to D/A input.) (7) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (8) With gain and zero errors adjusted to zero at +25°C. (9) Maximum represents the 3σ limit. Not 100% tested for this parameter. (10) The bipolar worst-case code change is $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$. For unipolar (DAC708/709 only) it is $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.

CONNECTION DIAGRAMS

DAC708/709



DAC705/706/707

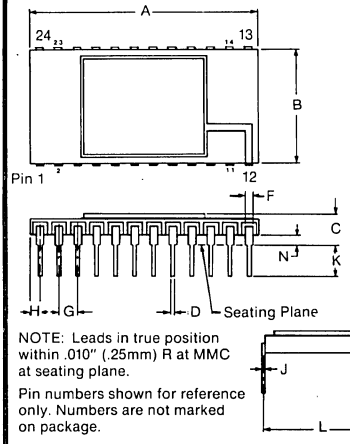


DESCRIPTION OF PIN FUNCTIONS

DAC705/706/707		Pin	DAC708/709	
Designator	Description	#	Designator	Description
V_{OUT} (DAC707 and DAC705) R_F (DAC706)	Voltage output for DAC707 (±10V) and DAC705 (±5V) or an internal feedback resistor for use with an external output op amp for the DAC706.	1	A_2	Latch enable for D/A latch (Active low)
V_{DD}	Logic supply (+5V)	2	A_0	Latch enable for "low byte" input (Active low). When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled.
DCOM	Digital common	3	A_1	Latch enable for "high byte" input (Active low). When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled.
ACOM	Analog common	4	D7 (D15)	Input for data bit 7 if enabling low byte (LB) latch or data bit 15 if enabling the high byte (HB) latch.
SJ (DAC705 and DAC707) I_{OUT} (DAC706)	Summing junction of the internal output op amp for the DAC705 and DAC707, or the current output for the DAC706. Offset adjust circuit is connected to the summing junction of the output amplifier. Refer to Block Diagram.	5	D6 (D14)	Input for data bit 6 if enabling LB latch or data bit 14 if enabling the HB latch.
GA	Gain adjust pin. Refer to Connection Diagram for gain adjust circuit.	6	D5 (D13)	Data bit 5 (LB) or data bit 13 (HB)
$+V_{CC}$	Positive supply voltage (+15V)	7	D4 (D12)	Data bit 4 (LB) or data bit 12 (HB)
$-V_{CC}$	Negative supply voltage (−15V)	8	D3 (D11)	Data bit 3 (LB) or data bit 11 (HB)
CLR	Clear line. Sets the input latch to zero and sets the D/A latch to the input code that gives bipolar zero on the D/A output (Active low)	9	D2 (D10)	Data bit 2 (LB) or data bit 10 (HB)
WR	Write control line (Active low)	10	D1 (D9)	Data bit 1 (LB) or data bit 9 (HB)
A_1	Enable for D/A converter latch (Active low)	11	D0 (D8)/SI	Data bit 0 (LB) or data bit 8 (HB). Serial input when serial mode is selected.
A_0	Enable for input latch (Active low)	12	DCOM	Digital common
D15 (MSB)	Data bit 15 (Most Significant Bit)	13	R_{F2}	Feedback resistor for internal or external operational amplifier. Connect to pin 14 when a 10V output range is desired. Leave open for a 20V output range.
D14	Data bit 14	14	V_{OUT} R_{F1} (DAC708)	Voltage output for DAC709 or feedback resistor for use with an external output op amp for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D13	Data bit 13	15	ACOM	Analog common
D12	Data bit 12	16	SJ (DAC709) I_{OUT} (DAC708)	Summing junction of the internal output op amp for the DAC709, or the current output for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D11	Data bit 11	17	BPO	Bipolar offset. Connect to pin 16 when operating in the bipolar mode. Leave open for unipolar mode.
D10	Data bit 10	18	GA	Gain adjust pin
D9	Data bit 9	19	$+V_{CC}$	Positive supply voltage (+15V)
D8	Data bit 8	20	$-V_{CC}$	Negative supply voltage (−15V)
D7	Data bit 7	21	CLR	Clear line. Sets the high and low byte input registers to zero and, for bipolar operation, sets the D/A register to the input code that gives bipolar zero on the D/A output. (In the unipolar mode, invert the MSB prior to the D/A.)
D6	Data bit 6	22	WR	Write control line
D5	Data bit 5	23	CS	Chip select control line
D4	Data bit 4	24	V_{DD}	Logic supply (+5V)
D3	Data bit 3	25	No pin	
D2	Data bit 2	26	No pin	(The DAC708 and DAC709 are in 24-pin packages)
D1	Data bit 1	27	No pin	
D0 (LSB)	Data bit 0 (Least Significant Bit)	28	No pin	

MECHANICAL

DAC708/709

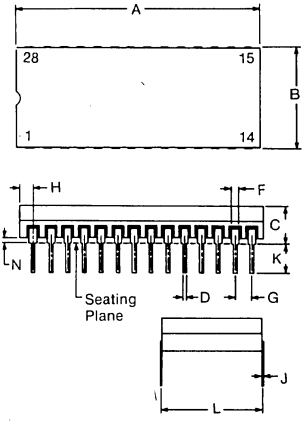


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

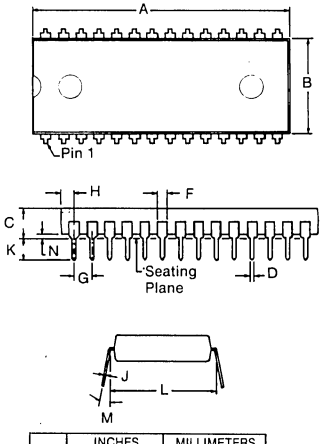
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.190	1.210	30.23	30.73
B	.580	.600	14.73	15.24
C	.140	.185	3.56	4.70
D	.016	.020	0.41	0.51
F	.030	.050	0.76	1.27
G	.100 BASIC		2.54 BASIC	
H	.035	.065	0.89	1.65
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

DAC705/706/707



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.465	35.20	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	.38	.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.035	.095	.89	2.41
J	.009	.012	.23	.30
K	.155	.195	3.94	4.05
L	.600 BASIC		15.42 BASIC	
N	.020	.060	.51	1.52

DAC707JP/KP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.440	1.500	36.58	38.10
B	0.475	0.520	12.07	13.20
C	0.170	0.225	4.32	5.72
D	0.016	0.024	0.40	0.60
F	0.047	0.065	1.20	1.65
G	0.100 BASIC		2.54 BASIC	
H	0.050	0.100	1.27	2.54
J	0.008	0.014	0.20	0.35
K	0.130	0.154	3.30	3.90
L	0.600 BASIC		15.24 BASIC	
M	0°C	15°C	0°C	15°C
N	0.020	0.024	0.51	0.61

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON ..... 0V, +15V
$+V_{CC}$ to COMMON ..... 0V, +18V
$-V_{CC}$ to COMMON ..... 0V, −18V
Digital Data Inputs to COMMON ..... −0.5V, V_{DD} +0.5
DC Current any Input ..... ±10mA
Reference Out to COMMON .. Indefinite Short to COMMON
V_{OUT} (DAC707, DAC709) ..... Indefinite Short to COMMON

External Voltage Applied to R_F (pin 1, DAC706; pin 13 or 14, DAC708) ..... ±18V
External Voltage Applied to D/A Output (pin 1, DAC707; pin 14, DAC708) ..... ±5V
Power Dissipation 1000mW
Storage Temperature ..... −60°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Model	Temperature Range	Input Configuration	Output Configuration
DAC705KH	0 to +70°C	16-bit port	±5V output
BH	−25 to +85°C	16-bit port	±5V output
BH/QM	−25 to +85°C	16-bit port	±5V output
SH	−55 to +125°C	16-bit port	±5V output
SH/QM	−55 to +125°C	16-bit port	±5V output
DAC706KH	0 to +70°C	16-bit port	±1mA output
BH	−25 to +85°C	16-bit port	±1mA output
BH/QM	−25 to +85°C	16-bit port	±1mA output
SH	−55 to +125°C	16-bit port	±1mA output
SH/QM	−55 to +125°C	16-bit port	±1mA output
DAC707JP	0 to +70°C	16-bit port	±10V output
KP	0 to +70°C	16-bit port	±10V output
KH	0 to +70°C	16-bit port	±10V output
BH	−25 to +85°C	16-bit port	±10V output
BH/QM	−25 to +85°C	16-bit port	±10V output
SH	−55 to +125°C	16-bit port	±10V output
SH/QM	−55 to +125°C	16-bit port	±10V output
DAC708KH	0 to +70°C	8-bit port	±1mA output
BH	−25 to +85°C	8-bit port	±1mA output
BH/QM	−25 to +85°C	8-bit port	±1mA output
SH	−55 to +125°C	8-bit port	±1mA output
SH/QM	−55 to +125°C	8-bit port	±1mA output
DAC709KH	0 to +70°C	8-bit port	±10V output
BH	−25 to +85°C	8-bit port	±10V output
BH/QM	−25 to +85°C	8-bit port	±10V output
SH	−55 to +125°C	8-bit port	±10V output
SH/QM	−55 to +125°C	8-bit port	±10V output

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

For bipolar operation, the DAC705/706/707/708/709 accept positive-true binary two's complement input code. For unipolar operation (DAC708/709 only) the input code is positive-true straight-binary provided that the MSB input is inverted with an external inverter. See Table I.

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output	
	Unipolar Straight Binary[1] (DAC708/709 only; connected for Unipolar operation)	Binary Two's Complement (Bipolar operation; all models)
$7FFF_H$	+1/2 Full Scale −1 LSB[2]	+Full Scale
0000_H	Zero	Zero
$FFFF_H$	+Full Scale	−1LSB
8000_H	+1/2 Full Scale	−Full Scale

(1) MSB must be inverted externally. (2) Assumes MSB is inverted externally.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (−Full Scale point and +Full Scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of −1LSB maximum (−0.0006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC705/706/707/708/709 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences at t_{min}, +25°C and t_{max}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. (For the DAC708/709 in unipolar mode, the MSB must be inverted.) This code corresponds to zero volts (DAC705/707 and DAC709) or zero milliamps (DAC706 and DAC708) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

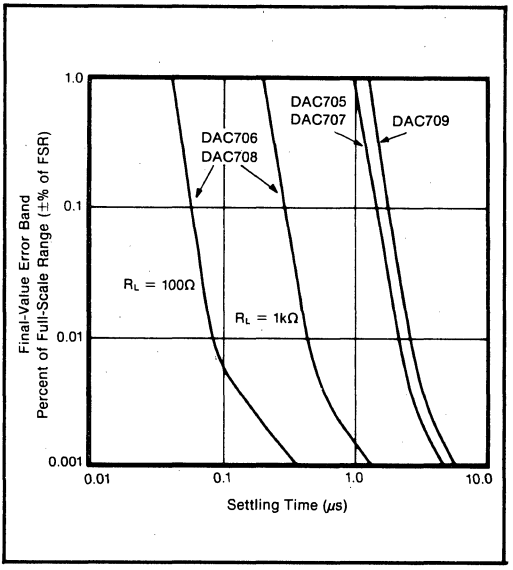


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2 LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V) or 10V (±5V or 0 to 10V) and a 1LSB change at the "major carry", the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

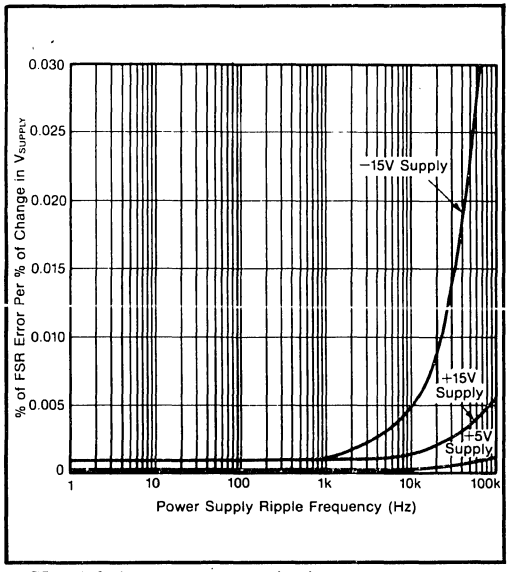


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001μF to 0.01μF ceramic capacitor should be connected from GAIN ADJUST to ANALOG COMMON to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar D/A converters.

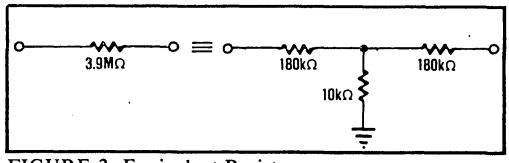


FIGURE 3. Equivalent Resistances.

Zero Adjustment

For unipolar (USB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (BTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and connection diagrams for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

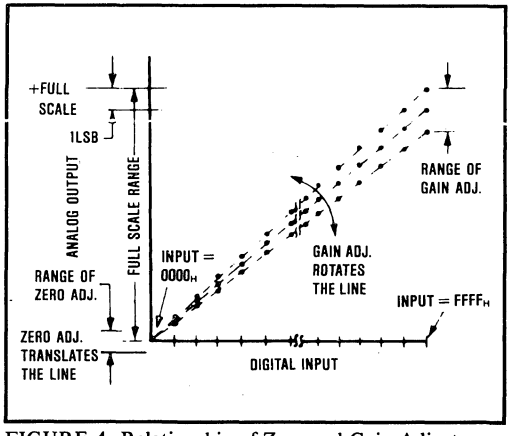


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC708 and DAC709.

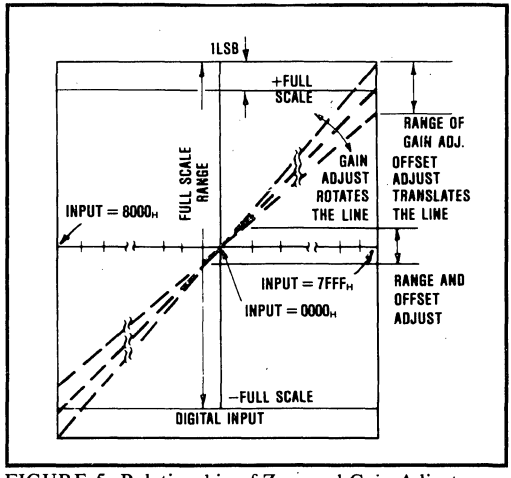


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC705/706/707 and DAC708/709.

TABLE II. Digital Input And Analog Output Voltage/Current Relationships.

VOLTAGE OUTPUT MODELS												
Digital Input Code	Analog Output *Unipolar, 0 to +10V			Units	Digital Input Code	Analog Output Bipolar, ±10V			Analog Output Bipolar, ±5V			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	16-Bit	15-Bit	14-Bit	
One LSB	153	305	610	μV	One LSB	305	610	1224	153	305	610	μV
$FFFF_H$	+9.99985	+9.99969	+9.99939	V	$7FFF_H$	+9.99960	+9.99939	+9.99878	+4.99980	+4.99970	+4.99939	V
0000_H	0	0	0	V	8000_H	−10.0000	−10.0000	−10.0000	−5.0000	−5.0000	−5.0000	V

CURRENT OUTPUT MODELS									
Digital Input Code	Analog Output *Unipolar, 0 to −2mA			Units	Digital Input Code	Analog Output Bipolar, ±1mA			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	
One LSB	0.031	0.061	0.122	μA	One LSB	0.031	0.061	0.122	μA
$FFFF_H$	−1.99997	−1.99994	−1.99988	mA	$7FFF_H$	−0.99997	−0.99994	−0.99988	mA
0000_H	0	0	0	mA	8000_H	+1.00000	+1.00000	+1.00000	mA

*MSB assumed to be inverted externally.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagrams for gain adjustment circuit connections.

INTERFACE LOGIC AND TIMING

DAC708/709

The signals CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), register enables ($\overline{A_0}$, $\overline{A_1}$, and $\overline{A_2}$) and CLEAR ($\overline{CLR}$), provide the control functions for the microprocessor interface. They are all active in the "low" or logic "0" state. $\overline{CS}$ must be low to access any of the registers. $\overline{A_0}$ and $\overline{A_1}$ steer the input 8-bit data byte to the low- or high-byte input latch respectively. $\overline{A_2}$ gates the contents of the two input latches through to the D/A latch in parallel. The contents are then applied to the input of the D/A converter. When $\overline{WR}$ goes low, data is strobed into the latch or latches which have been enabled.

The serial input mode is activated when both $\overline{A_0}$ and $\overline{A_1}$ are logic "0" simultaneously. The D0 (D8)/SI input data line accepts the serial data MSB first. Each bit is clocked in by a $\overline{WR}$ pulse. Data is strobed through to the D/A latch by $\overline{A_2}$ going to logic "0" the same as in the parallel input mode.

Each of the latches can be made "transparent" by maintaining its enable signal at logic "0". However, as stated above, when both $\overline{A_0}$ and $\overline{A_1}$ are logic "0" at the same time, the serial mode is selected.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the D/A latch to 0000_H. This is the binary code that gives a null, or zero, at the output of the D/A in the bipolar mode. In the unipolar mode, activating $\overline{CLR}$ will cause the output to go to one-half of full scale.

The maximum clock rate of the latches is 10MHz. The minimum time between write (WR) pulses for successive enables is 20ns. In the serial input mode (DAC708 and DAC709), the maximum rate at which data can be clocked into the input shift register is 10MHz.

The timing of the control signals is given in Figure 6.

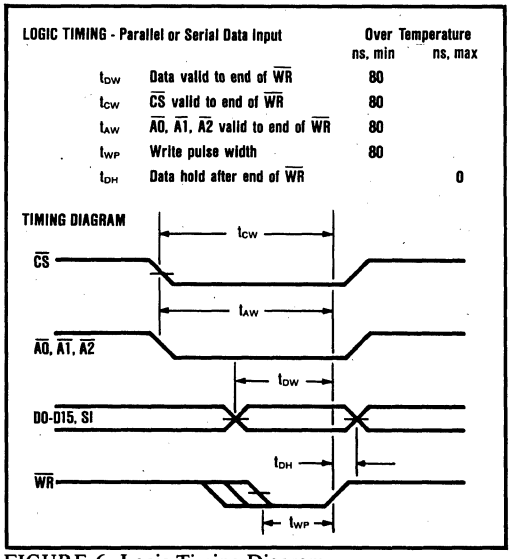


FIGURE 6. Logic Timing Diagram.

DAC706/707

The DAC705/706/707 interface timing is the same as that described above except instead of two 8-bit separately-enabled input latches, it has a single 16-bit input latch enabled by $\overline{A_0}$. The D/A latch is enabled by $\overline{A_1}$. Also, there is no serial-input mode and no CHIP SELECT ($\overline{CS}$) line.

INSTALLATION CONSIDERATIONS

Due to the extremely-high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms

of a system layout, the resistance of typical 1 ounce copper-clad printed circuit board material is approximately 1/2mΩ per square. In the example above, a 10 milliinch-wide conductor 60 milliinches long would cause a 1LSB error.

In Figures 7 and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed with gain calibration. R_3 is part of R_L if the output voltage is sensed at ANALOG COMMON.

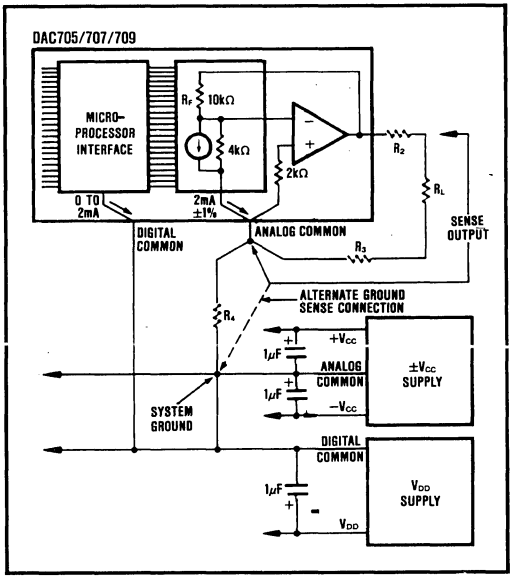


FIGURE 7. DAC705/707/709 Bipolar Output Circuit (Voltage Out).

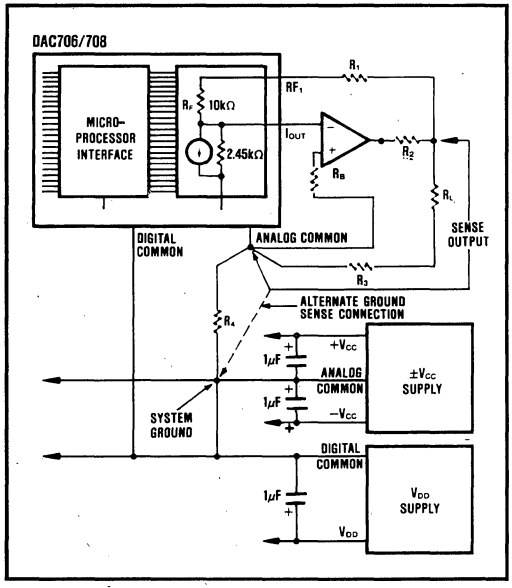


FIGURE 8. DAC706/708 Bipolar Output Circuit (with External Op Amp).

Figures 8 and 9 show two methods of connecting the currrent output model with an external precision output op amp. By sensing the output voltage at the load resistor (connecting R_F to the output of the amplifier at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

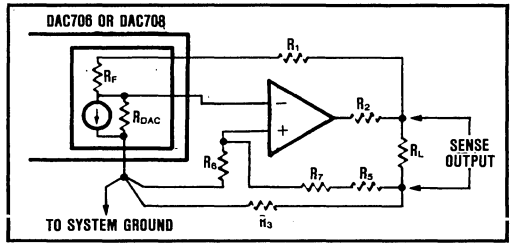


FIGURE 9. Alternate Connection for Ground Sensing at the Load (Current Output Models).

In many applications it is impractical to sense the output voltage at ANALOG COMMON. Sensing the output voltage at the system ground point is permissible because these converters have separate analog and digital common lines and the analog return current is a near-constant 2mA and varies by only 10μA to 20μA over the entire input code range. R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 is constant and appears as a zero error that can be nulled with the zero calibration adjustment.

Another approach senses the output at the load as shown in Figure 9. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection across R_L. The effect of R_4 is negligible as explained previously.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small flux-capture cross section for any external field.

ENVIRONMENTAL SCREENING

/QM Screening

All BH and SH models are available with Burr-Brown's /QM environmental screening for enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the

screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

SCREENING FLOW FOR /QM MODELS

Screen	MIL-STD-883 Method	Condition	Comments
Internal Visual	2017	B	
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24hrs
Temperature Cycling	1010	C	−65 to +150°C, 10 cycles
Burn-in	1015	B	+125°C, 160hrs
Constant Acceleration	2001		
28-pin pkg.		B	10,000G
24-pin pkg.		E	30,000G
Hermeticity			
Fine Leak	1014	A1 or A2	
28-pin pkg.			2×10^{-7} atmcc/sec
24-pin pkg.			5×10^{-8} atmcc/sec
Gross Leak	1014	C	60psig, 2hr
External Visual	2009		

APPLICATIONS

LOADING THE DAC709 SERIALLY ACROSS AN ISOLATION BARRIER

A very useful application of the DAC709 is in achieving low-cost isolation that preserves high accuracy. Using the serial input feature of the input register pair, only three signal lines need to be isolated. The data is applied to pin 11 in a serial bit stream, MSB first. The WR input is used as a data strobe, clocking in each data bit. A RESET signal is provided for system startup and reset. These three signals are each optically isolated. Once the 16 bits of serial data have been strobed into the input register pair, the data is strobed through to the D/A register by the "carry" signal out of a 4-bit binary synchronous counter that has counted the 16 WR pulses used to clock in the data. The circuit diagram is given in Figure 10.

CONNECTING MULTIPLE DAC707s TO A 16-BIT MICROPROCESSOR BUS

Figure 11 illustrates the method of connecting multiple DAC707s to a 16-bit microprocessor bus. The circuit shown has two DAC707s and uses only one address line to select either the input register or the D/A register. An external address decoder selects the desired converter.

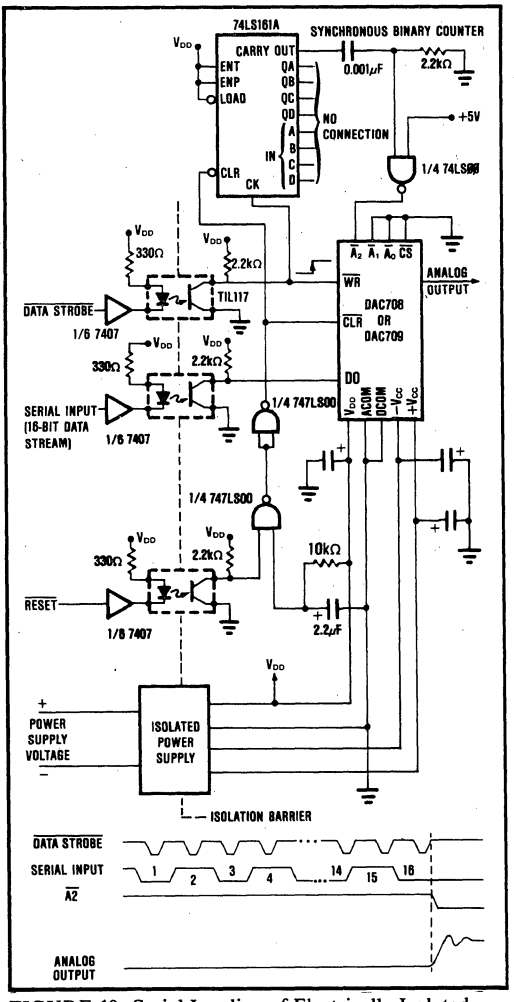


FIGURE 10. Serial Loading of Electrically Isolated DAC708/709.

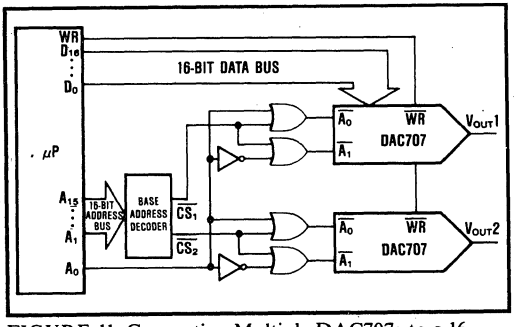
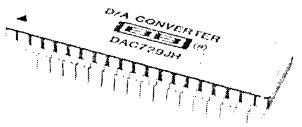


FIGURE 11. Connecting Multiple DAC707s to a 16-Bit Microprocessor.

BURR-BROWN®



DAC729

ADVANCE INFORMATION
Subject to Change

Ultra-High Resolution 18-Bit DIGITAL-TO-ANALOG CONVERTER

FEATURES

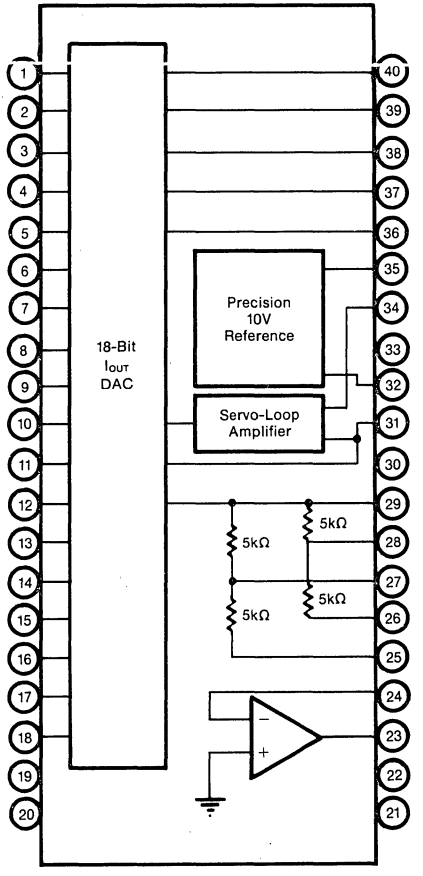
- 16-BIT LINEARITY GUARANTEED (K GRADE)
- USER ADJUSTABLE TO 18-BIT LINEARITY (K GRADE)
- PRECISION INTERNAL REFERENCE NOT DEDICATED
- FAST SETTLING, LOW NOISE INTERNAL OP AMP NOT DEDICATED
- LOW TEMPERATURE DRIFT
- HERMETIC 40-PIN CERAMIC PACKAGE
- I_{OUT} OR V_{OUT} OPERATION

DESCRIPTION

The DAC729 sets the standard in very high accuracy digital-to-analog conversion. It is supplied from the factory at a guaranteed linearity of 16 bits, and is user-adjustable to 18-bit linearity (1LSB = FSR/262144).

To attain this high level of accuracy, the design takes advantage of Burr-Brown's thin-film monolithic DAC process, dielectric op amp process, hybrid capabilities, and advanced test and laser-trim techniques.

The DAC729 hybrid layout is specifically partitioned to minimize the effect of external load-current-induced thermal errors. The op amp design consists of a fast settling precision op amp with a current buffer within the feedback loop. This architecture isolates the load from the op amp, which results in a fast settling (15μs to 18 bits) op amp that boasts an open-loop gain of over 500k. The standard 40-pin package offers full hermeticity, contributing to the excellent reliability of the DAC729.



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SPECIFICATIONS

ELECTRICAL

Typical at 25°C, $\pm V_{CC}$ = 15VDC.

MODEL	DAC729JH			DAC729KH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT							
DIGITAL INPUT							
Resolution		18			*		Bits
Digital Inputs[1]: V_{IH}	+2.4		$+V_L$	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH}, V_{IN} = 2.7V			+5.0			*	μA
I_{IL}, V_{IN} = 0.4V			−300			*	μA
TRANSFER CHARACTERISTICS							
ACCURACY[2]							
Linearity Error[3]			±0.0015			±0.0007	% of FSR[4]
Differential Linearity Error			±0.003			±0.0015	% of FSR
Gain Error [5]		±0.05	±0.10		*	*	%
Offset Error[5]: Voltage, COB[6]		±5	±10		*	*	mV
CSB[6]		±0.5	±0.8		*	*	mV
Current, COB			±5			*	μA
CSB			±1			*	μA
Monotonicity (0°C to 70°C)	15	16			17		Bits
Differential Linearity Adjustment Resolution[7]		17			18		Bits
DRIFT (Over Specification Temperature Range)							
Total Voltage Error Over Temperature (0°C to +70°C)[8]		±0.050	±0.100		*	*	% of FSR
Total Full-Scale Drift		±9	±0.18		±7	±15	ppm of FSR/°C
Gain Drift (Excluding Reference Drift)		±1	±3.0		*	*	ppm/°C
Offset Drift (Excluding Reference Drift): COB		±2.0	±5.0		*	*	ppm of FSR/°C
CSB		±0.5	±2.0		*	*	ppm of FSR/°C
Linearity Error Over Temperature		±0.5	±1.0		±0.25	±0.50	ppm of FSR/°C
Differential Linearity Error Over Temperature		±0.5	±1.0		±0.25	±0.50	ppm of FSR/°C
OUTPUT							
VOLTAGE OUTPUT MODE							
Ranges: COB		±2.5, ±5, ±10			*		V
CSB		0 to 10, 0 to 5			*		V
Output Current	±5			*			mA
Output Impedance		0.15			*		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
CURRENT OUTPUT MODE							
COB Ranges		±1.0			*		mA
Output Impedance		2.86			*		kΩ
CSB Ranges		0 to −2			*		mA
Output Impedance		4.0			*		kΩ
Output Current Tolerance			±0.1			*	% of FSR
Compliance Voltage		−1 to +5			*		V
SETTLING TIME (To ±0.00038% of FSR)[9]							
Voltage (Load = 2kΩ ‖ 100pF):							
Full-Scale Step		5	8		*	*	μs
1LSB Step (Major Carry)[10]		4	7		*	*	μs
Slew Rate		20			*		V/μs
Switching Transient Peak		500			*		mV
Switching Transient Energy		0.45			*		V-μs
Current Full-Scale Step (2mA × 10Ω)		300			*		ns
REFERENCE							
Output (pin 32): Voltage	+9.990	10.000	10.010	*	*	*	V
Source Current[11]			+4.0			*	mA
Temperature Coefficient		±1.0	±2.5		*	*	ppm/°C
Short-Circuit Duration		Indefinite to Common			Indefinite to Common		
Input Voltage Tolerance (external)	+9.990	10	10.010	*	*	*	V
Reference Load: Unipolar Mode			−1.0			*	mA
Bipolar Mode			−2.0			*	mA

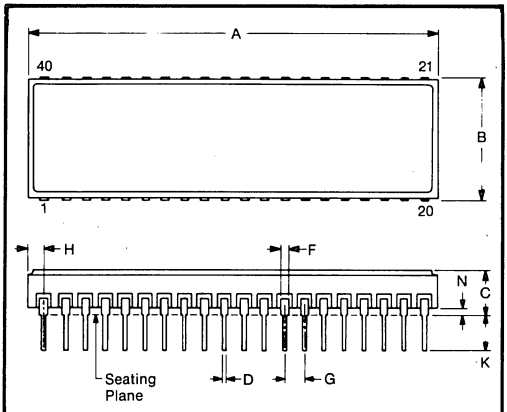
ELECTRICAL (CONT)

MODEL	DAC729JH			DAC729KH			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+13.5	+15	+16.5	*	*	*	V
$-V_{CC}$	−16.5	−15	−13.5	*	*	*	V
$+V_L$	+4.75	+5	+5.25	*	*	*	V
Current: $+V_{CC}$		+30	+40		*	*	mA
$-V_{CC}$		−40	−55		*	*	mA
$+V_L$		+18	+25		*	*	mA
Power Dissipation (Typical Supplies)		1.14	1.55		*	*	W
Power Supply Sensitivity, Unipolar: ±15VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
+5VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
Bipolar: ±15VDC		±0.0004	±0.0015		*	*	% of FSR/%V_S
+5VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
Gain: ±15VDC		±0.0005	±0.0015		*	*	% of FSR/%V_S
+5VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
ENVIRONMENTAL SPECIFICATIONS							
Temperature Range: Specification	0		+70	*		*	°C
Storage	−60		+150	*		*	°C

*Specification same as DAC729JH.

NOTES: (1) TTL and CMOS compatible. (2) Specified for V_{OUT} mode using the internal op amp. (3) ±0.00076% of full-scale range is 1/2LSB of 16-bit resolution. (4) FSR means full-scale range, 20V for ±10V range, etc. (5) Adjustable to zero error with an external potentiometer. (6) COB is complementary offset binary (bipolar); CSB is complementary straight binary (unipolar). (7) Using the MSB adjustment circuit, the user may improve the DAC linearity to 1/2LSB of this specification. (8) With gain and offset errors adjusted to zero at 25°C. (9) Maximum represents 3 sigma limit, not 100% production tested. (10) At the major carry; 20000 to 1FFFF Hex and from 1FFFF to 20000 Hex. (11) Maximum with no degradation in specifications. External loads must be constant.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.980	2.040	50.29	51.82
B	.610	.630	15.49	16.00
C	.150	.200	3.81	5.08
D	.016	.020	0.41	0.51
F	.050 TYP		1.27 TYP	
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.009	.012	0.23	0.30
K	.155	.195	3.94	4.95
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (.025mm) R at MMC at seating plane.

Pin numbers are shown for reference only. Numbers may not be marked on package.

ABSOLUTE MAXIMUM RATINGS

$+V_{DD}$ to Common	0V to +7V
$+V_{CC}$ to Common	0V to +18V
$-V_{CC}$ to Common	0V to −18V
Digital Data Inputs (pins 1-18) to Common	+0.5V to +18V
Reference out (pin 32) to Common	Indefinite Short to Common
External Voltage Applied to D/A Output (pin 29)	−5V to +5V
V_{OUT} (pin 23)	Indefinite Short to Common
Power Dissipation	3000mW
Storage Temperature	−60°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN CONNECTIONS

DAC729

Bit 1	1	40	V_{POT}
Bit 2	2	39	Bit 1 Adjust
Bit 3	3	38	Bit 2 Adjust
Bit 4	4	37	Bit 3 Adjust
Bit 5	5	36	Bit 4 Adjust
Bit 6	6	35	Reference Adjust
Bit 7	7	34	Gain Adjust
Bit 8	8	33	Reference Common
Bit 9	9	32	Reference Out
Bit 10	10	31	Reference In
Bit 11	11	30	Analog Common
Bit 12	12	29	I_{OUT}
Bit 13	13	28	5kΩ Feedback
Bit 14	14	27	5kΩ Feedback
Bit 15	15	26	10kΩ Feedback
Bit 16	16	25	10kΩ Feedback
Bit 17	17	24	Summing Junction
Bit 18	18	23	V_{OUT}
$+V_L$ (5V)	19	22	$+V_{CC}$ (15V)
Power Ground	20	21	$-V_{CC}$ (15V)

THEORY OF OPERATION

The DAC729 is an 18-bit digital-to-analog converter system, including a precision reference, low noise, fast settling operational amplifier, and the 18-bit current source/DAC chip contained in a hermetic 40-pin ceramic dual-in-line package.

THE INTERNAL REFERENCE

The reference consists of a very low temperature coefficient closed-loop reference zener circuit that has been slope-compensated by laser-trimming current-setting resistors to a zener current to achieve less than 1ppm/°C temperature drift of V_{REF}.

By strapping pin 32 (Reference Out) to pin 31 (Reference In), the DAC will be properly biased from the internal reference. The internal reference may be fine adjusted using pin 35 as shown in Figure 7. The reference has an output buffer that will supply 4mA for use external to the DAC729. This load must remain constant because changing load on the reference may change the reference current to the DAC.

In systems where several components need to track the same system reference, the DAC729 may be used with an external 10V reference, however, the internal reference has lower noise (6μVp-p) and better stability than other references available.

THE OPERATIONAL AMPLIFIER

To support a DAC of this accuracy, the operational amplifier must have a maximum gain-induced error of less than 1/3LSB, independent of output swing (the op amp must be linear!). To support 15 bits (1/2-bit linearity) the op amp must have a gain of 130,000V/V. For 18 bits, the minimum gain is well over 500,000V/V. Since thermal feedback is the major limitation of gain for mono op amps, the amplifier was designed as a high gain, fast settling mono op amp, followed by a monolithic, unity gain current buffer to isolate the thermal effects of external loads from the input stages of the gain transistors. The op amp and buffer are separated from the DAC chip, minimizing thermally-induced linearity errors in the DAC circuit. The op amp, like the reference, is not dedicated to the DAC729. The user may want to add a network, or select a different amplifier. The DAC729 internal op amp is intended to be the best choice for settling, speed, and noise.

THE DAC CHIP

The heart of the DAC729 is a monolithic current source and switch integrated circuit. The absolute linearity, differential linearity, and the temperature performance of the DAC729 are the result of the design, which utilizes the excellent element matching of the current sources and switch transistors to each other, and the tracking of the current setting resistors to the feedback resistors. Older, more discrete designs cannot achieve the performance of this monolithic DAC design.

The two most significant bits are binarily weighted inner-digitized current sources. The currents for bits 3 through 18 are scaled with both current sources weighting and an R-2R ladder. The circuit design is optimized for low noise and low superposition error, with the current sources arranged to minimize both code-dependent thermal errors and IR drop errors. As a result, the superposition errors are typically less than 20μV.

The DAC chip is biased from a servo amplifier feeding into the base line of the current sources. This servo amplifier sets the collector current to be mirrored and scaled in the DAC chip current sources. The reference current for the servo is established by the reference voltage applied to pin 31 feeding an internal resistor (10kΩ) to the virtual ground of the servo amplifier.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC729 accepts complementary digital input codes in either binary format (CSB, Unipolar or COB, Bipolar; see Table I).

TABLE I. Digital Input Coding.

	DAC Analog Output			
Digital Input	COB	20V FSR	CSB	10V FSR
00 0000 0000 0000 0000	+ Full Scale	9.999924V	+ Full Scale	9.999962V
11 1111 1111 1111 1111	− Full Scale	−10V	− Full Scale	0V

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.0015% for 16-bit resolution) insures monotonicity

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC729 is specified to be monotonic to 16 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale

range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is measured by: (1) testing the end point differences for each D/A at t_{MIN}, +25°C and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Offset Drift

Offset drift is a measure of the change in the output with $3FFFF_H$ applied to the digital inputs over the specified temperature range. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the offset error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full-scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input.

Voltage Output

Settling times are specified to ±0.00075% of FSR (±1/2LSB for 16 bits) for two input conditions: a full-scale range change of 20V (COB) or 10V (CSB) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to ±0.00075% of FSR for a full-scale range change with an output load resistance of 10Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified linearity.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_L) about the nominal power supply voltages (see Figure 1). It is specified for DC or low frequency changes. The typical performance curve in Figure 1 shows the effect of high frequency changes in power supply voltages using internal reference, DAC, and op amp.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in

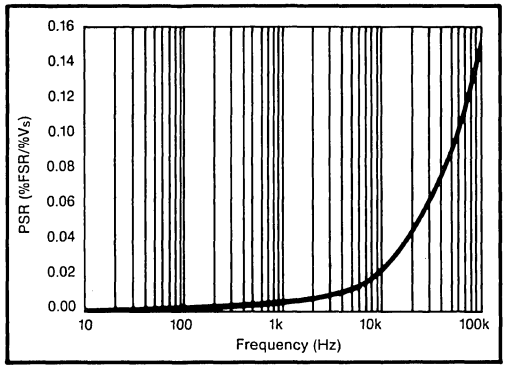


FIGURE 1. Power Supply Rejection vs Frequency Using Internal Reference and Op Amp.

Figure 2. These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC729. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

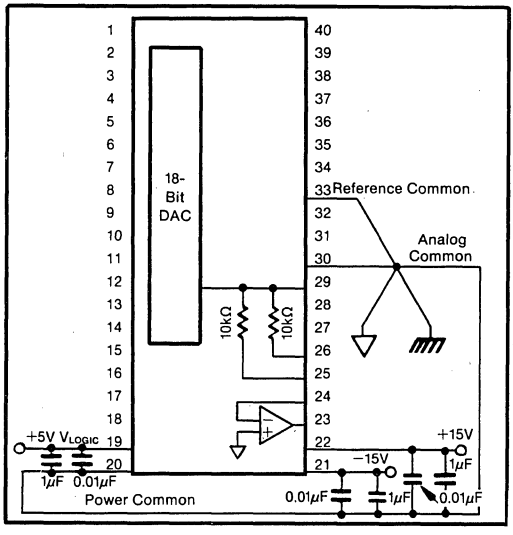


FIGURE 2. Ground Connections and Supply Bypass.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC729 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust (pin 34) to common to shunt noise pickup. Refer

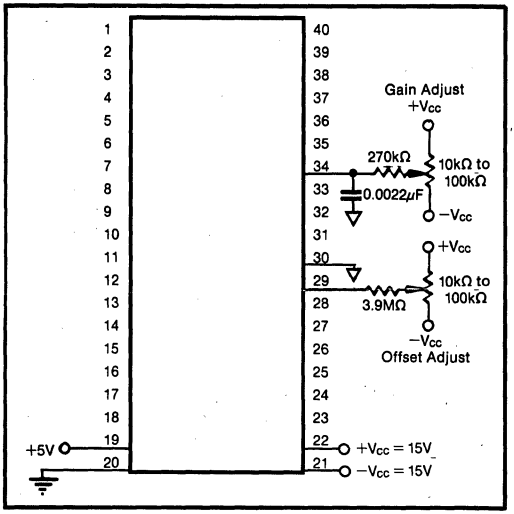


FIGURE 3. Typical Gain and Offset Adjust Hook-Up.

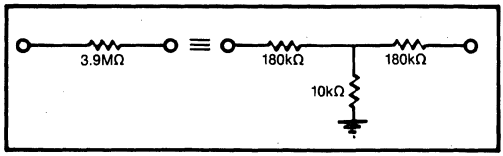


FIGURE 4. Equivalent Resistances.

to Figures 5 and 6 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

OFFSET ADJUSTMENT

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

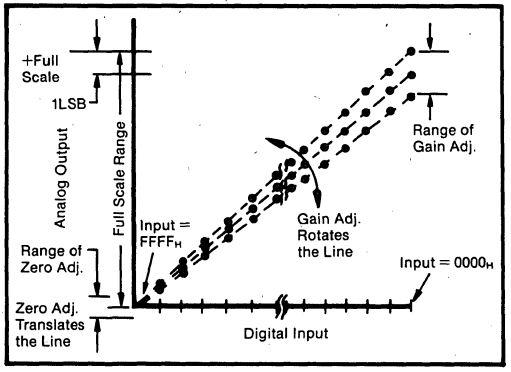


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

For bipolar (COB) configurations, apply the digital input code that should produce the maximum negative output voltage. See Table II for corresponding codes and Figures 2 and 3 for offset adjustment connections. Offset adjust

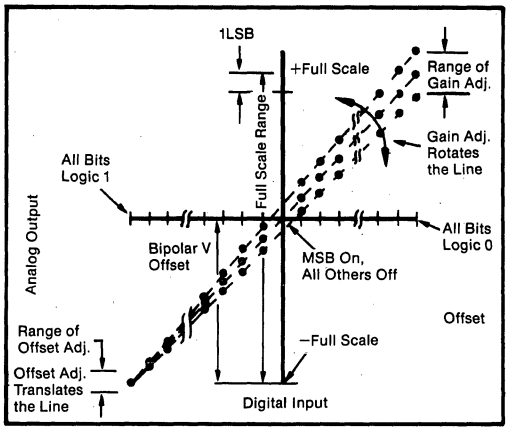


FIGURE 6. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

should be made prior to gain adjust.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and Figure 3 for gain adjustment connections.

TABLE II. Output Range Connections.

Output Range	Code	Connect Pin 23	Connect Pin 31	Connect Pin 24
±10V	COB	to Pin 25	to Pin 26	to Pin 29
±5V	COB	to Pin 27	to Pin 26	to Pin 29
±2.5V	COB	to Pin 27	to Pin 26	to Pins 29 & 25
0 to 10V	CSB	to Pin 27	N/C	to Pin 29
0 to 5V	CSB	to Pins 27 & 28	N/C	to Pin 29

REFERENCE ADJUSTMENT

The internal reference may be fine adjusted using pin 35 as shown in Figure 7. Adjusting the reference has a similar effect on the DAC as gain adjust, except the transfer function rotates around bipolar zero for a bipolar hookup. The transfer function is shown in Figure 8.

The value of the setting resistor may be selected from the graph. The range of adjustment should be minimized to limit the effects of drift and noise from the external resistor and potentiometer.

LAYOUT/APPLICATIONS SUGGESTIONS

Obviously, the management of IR drops, power supply noise, thermal stability, and environmental noise becomes much more critical as the accuracy of the system increases. The DAC729 has been designed to minimize these applications problems to a large degree. The basics of "Kelvin sensing" and "holy point" grounding will be the most important considerations in optimizing the absolute accuracy of the system. Figure 9 shows the proper connection of the DAC with the holy-point ground and

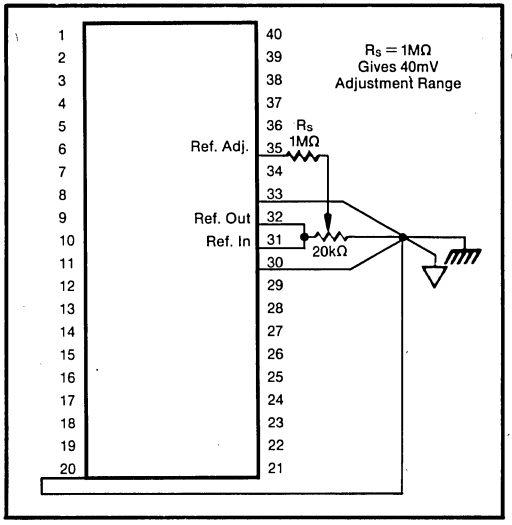


FIGURE 7. V_{REF} Adjust.

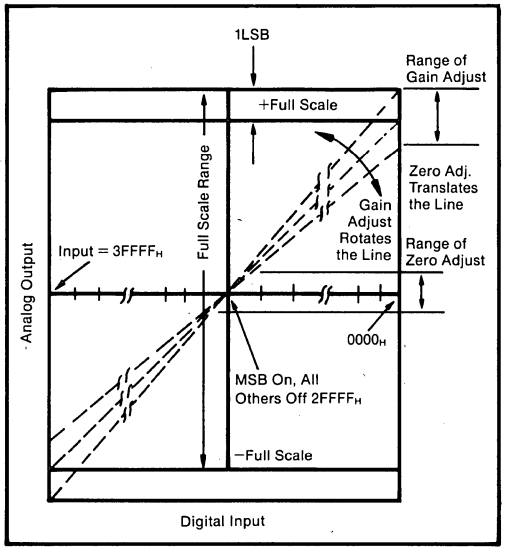


FIGURE 8. Effect of V_{REF} Adjust on a COB Connected Device.

the Kelvin-voltage-output connection at the load.

The DAC729 has three separate supply common (ground) pins. Reference common (pin 33) carries the return current from the internal reference and the output I/V converter common. The current in pin 33 is stable and independent of code or load. Power common (pin 20) carries the variable currents of the biasing circuits. Analog common (pin 30) is the termination of the R-2R ladder and also carries the "waste current" from the off side of the current switches. These three ground pins must be star connected to system ground for the DAC to bias properly and accurately. Good ground connections are essential,

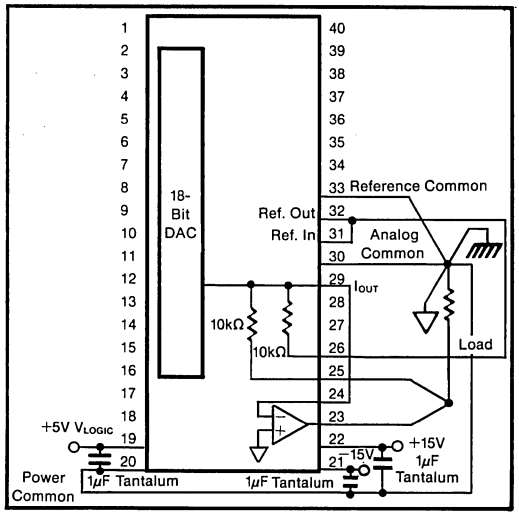


FIGURE 9. Typical Hook-Up Diagram with "Holy Point" Ground and Kelvin Sense Load, Using Internal Op Amp and Reference.

because an IR drop of just 39μV completely swamps out a 10V FSR 18-bit LSB.

Temperature variations of the part may cause accuracy errors. Careful attention must be paid to the effects of the load that the DAC is driving. Although the internal current buffer will drive substantial loads (25mA or more typically), the thermals produced internally will affect the individual current sources of the DAC. The package has a thermal resistance of about 25°C/W. This thermal resistance will show up as a thermal gradient across the DAC chip and could cause linearity problems. These problems may appear as a code dependent error for DC or slow data rates. To overcome the problems of a heavy load, it is suggested that an external current buffer be used (Figure 10), and located so as not to affect the DAC temperature.

TRUE 18-BIT PERFORMANCE (LINEARITY ADJUSTMENT)

To take full advantage of the DAC729's accuracy, the four MSBs have adjustment capabilities. A simplified schematic (Figure 11) shows the internal structure of the DAC current source and the adjustment input terminal. The suggested network for adjusting the linearity is shown in Figure 12. This circuit has nearly twice the range that is required for the DAC729JH. The range is intentionally narrow so as to minimize the effect of temperature drift or stability problems in the potentiometers. The potentiometers are biased in an identical fashion to the internal DAC current sources to minimize power supply rejection problems and temperature drift problems.

The linearity adjustment requires a digital voltmeter with 7 digits of resolution on the 10V range (1μV resolution) and excellent linearity. For the DAC, 1LSB of the 0V to 10V scale (10 FSR) is 38μV. To be 1/2LSB linear, the

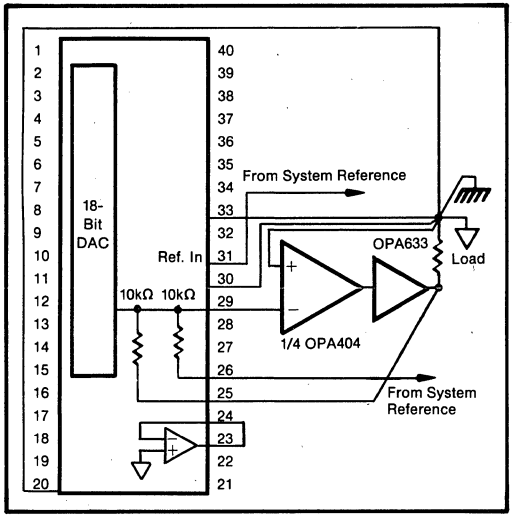


FIGURE 10. Using an External Op Amp with Buffer and External Reference for ±10V Output.

measurement must resolve 19μV. The meter must be properly calibrated and linear to 1ppm of range.

With the DAC connected for 0 to 10V output (Figure 13), the adjustment procedure is to set the DAC code and measure as follows.

FOURTH MSB ADJUSTMENT
1. Code = 11 1100 0000 0000 0000
2. Measure
3. Code = 11 1011 1111 1111 1111
4. Measure and difference.
5. Adjust 4th MSB potentiometer to make difference +38μV.
6. Repeat steps 1 through 5 to confirm.

THIRD MSB ADJUSTMENT
1. Code = 11 1000 0000 0000 0000
2. Measure
3. Code = 11 0111 1111 1111 1111
4. Measure and difference.
5. Adjust 3rd MSB potentiometer to make difference +38μV.
6. Repeat steps 1 through 5 to confirm.

SECOND MSB ADJUSTMENT
1. Code = 11 0000 0000 0000 0000
2. Measure
3. Code = 10 1111 1111 1111 1111
4. Measure and difference.
5. Adjust 2nd MSB potentiometer to make difference +38μV.
6. Repeat steps 1 through 5 to confirm.

MSB ADJUSTMENT
1. Code = 10 0000 0000 0000 0000
2. Measure
3. Code = 01 1111 1111 1111 1111
4. Measure and difference.
5. Adjust the MSB potentiometer to make difference +38μV.
6. Repeat steps 1 through 5 to confirm.

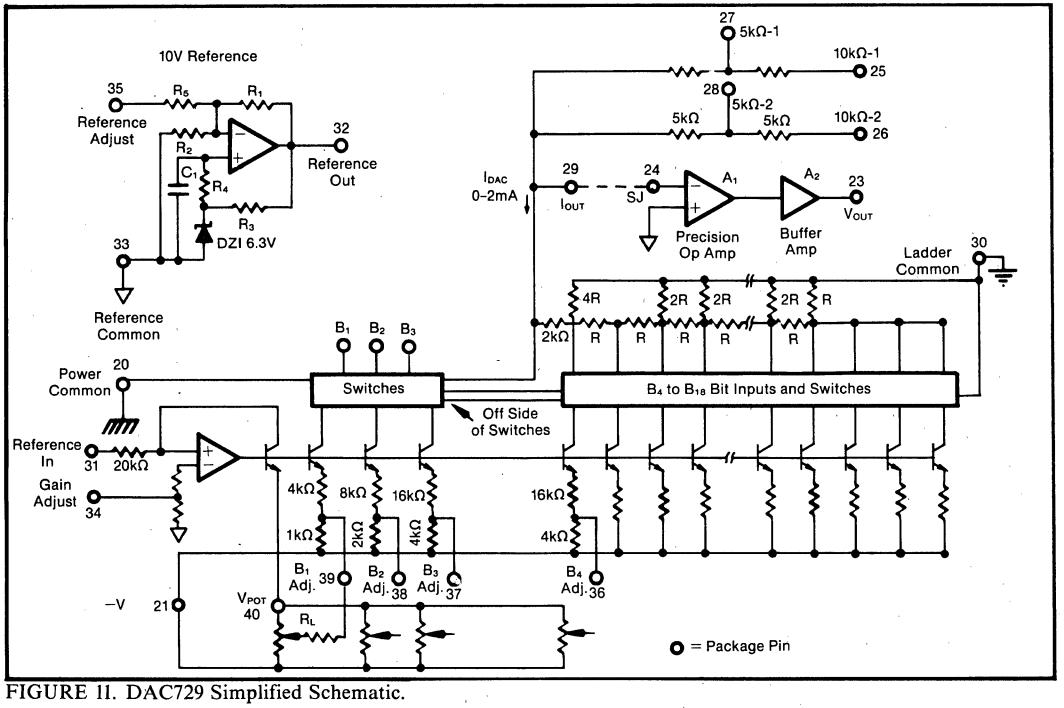


FIGURE 11. DAC729 Simplified Schematic.

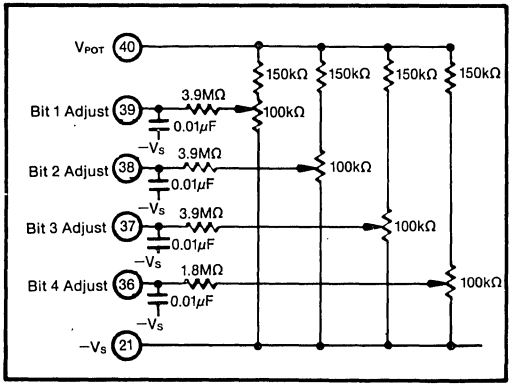


FIGURE 12. Differential Linearity Adjustment Circuit for the 4MSBs.

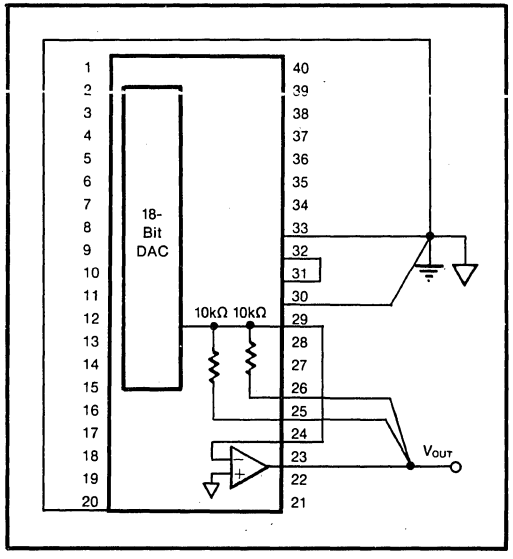


FIGURE 13. 0 to 10V FSR.

APPLICATIONS

The DAC729 is the DAC of choice for applications requiring very high resolution, accuracy, and wide dynamic range.

DIGITAL AUDIO

The excellent linearity and differential linearity are ideal for PCM professional audio and waveform generation applications.

The DAC729 offers superb dynamic range. Dynamic range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range, usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6dB per bit. For the DAC729 the theoretical range is 108dB! The actual dynamic range is limited by noise (signal-to-noise) and linearity errors. The DAC729's 6μV typical noise floor, fast settling op amp, and adjustable 18-bit linearity minimize the limitation.

Total harmonic distortion (THD) is the measure of the magnitude and distribution of the linearity error, differential linearity error, noise, and quantization error. The THD is defined as the ratio of the square root of the sum of the squares of the harmonics to the values of the input fundamental frequency. The RMS value of a DAC error can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the DAC729 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \quad (2)$$

where E rms is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

The DAC729 has demonstrated THD of better than 0.0009% of full scale (at 1kHz). This is the level of distortion that is desired to test other professional audio products, making the DAC729 ideal for professional audio test equipment.

The ability to adjust the linearity of the 4MSBs, the 18-bit resolution, fast settling and low noise give the DAC729 unmatched performance.

AUTOMATIC TEST EQUIPMENT

The ability to adjust the absolute linearity and the ability to run several DACs from the same reference make the DAC729 ideal as the reference DAC for an entire data conversion system. Since the feedback resistors are absolute value (±0.1%), the addition of a 240Ω resistor makes the output 10.24V.This feature makes discrete 10mV steps easy to create with a resolution of 39μV for 10.24V FSR. Figure 14 shows the DAC729 connected for 0V to 10.24V operation and using an external reference. The two 240Ω resistors are in series with the parallel 10kΩ internal resistors, resulting in 10.24V out. This hook-up minimizes the thermal coefficient of resistance problems associated with this accuracy.

The low superposition error of the DAC729 makes the system calibration routines become much less complicated. There is seldom a need to iterate through the calibration routine. Repeatability of the DAC output voltage is many times better than competitive products. This feature cuts system overhead time, improves accuracy, and cuts guardbands for the user. The entire set of test head DACs could be upgraded from 16 bits to 18 bits by replacing the existing 16-bit DACs.

THE HEART OF AN 18-BIT ADC

The DAC729 makes a good building block in ADC applications. The key to ADC accuracy is differential linearity of the DAC. The ability to adjust to 18-bit linearity, coupled with the fast settling time of the DAC729 makes the design cycle for an 18-bit successive approximation ADC much faster, and the production more consistent. Figure 15 shows the DAC as the heart of a successive approximation ADC. The clock and successive approximation register could be implemented in 7400 series TTL, as a simple gate-array or standard cell, or part of a local processor.

With the DAC out of the way, the comparator is the toughest part of the ADC design. To resolve an 18-bit LSB, and interface to a TTL logic device, the comparator must have a gain of 500kV/V (5X actual) as well as low hysteresis, low noise, and low thermally-induced offsets. With this much gain, a slow comparator may be desired to reduce the risk of instability.

The feedback resistors of the DAC are the input scaling resistors of the ADC. An OPA404 and an OPA633 make an excellent buffer for the input signal, giving a very high input impedance to the signal (minimizing IR drop) while maintaining the linearity.

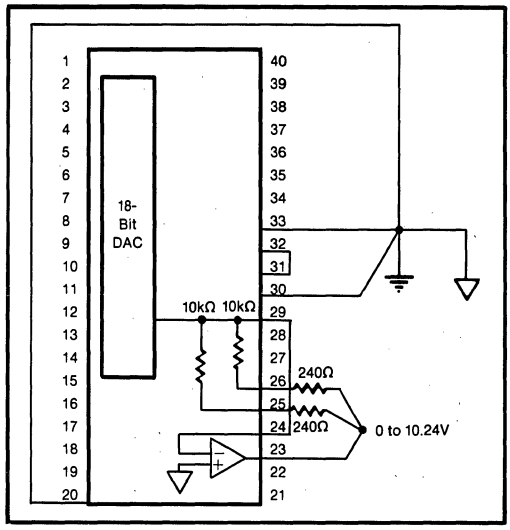


FIGURE 14. 0V to 10.24V Using Internal Op Amp and Internal References.

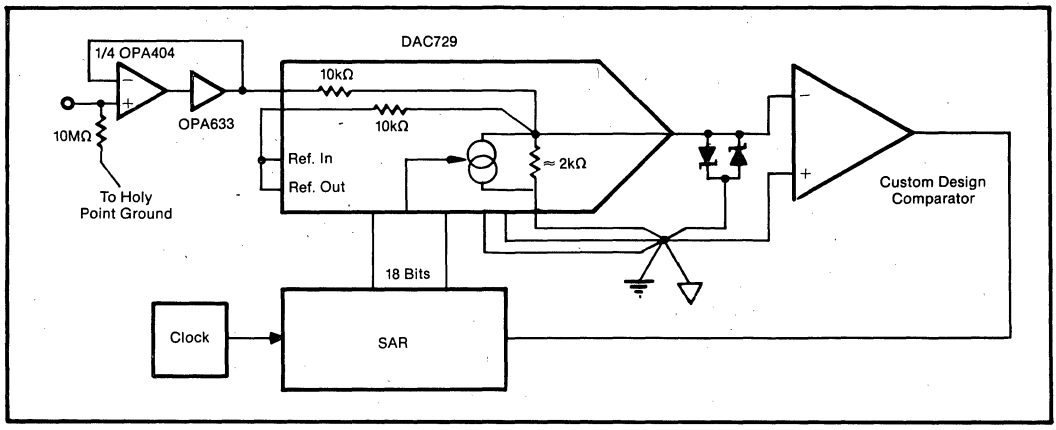


FIGURE 15. Block Diagram of an 18-Bit $\pm 10V_{IN}$ ADC.

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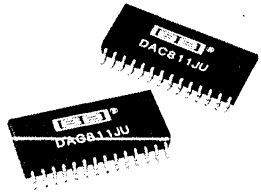


DAC811JU
DAC811KU

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER (Small-Outline Surface-Mount Package)

FEATURES

- SINGLE INTEGRATED CIRCUIT CHIP
- MICROCOMPUTER INTERFACE: DOUBLE-BUFFERED LATCH
- VOLTAGE OUTPUT: ±10V, ±5V, +10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- ±3/4LSB MAXIMUM NONLINEARITY OVER TEMPERATURE
- GUARANTEED SPECIFICATIONS AT ±12V AND ±15V SUPPLIES
- TTL/5V CMOS-COMPATIBLE LOGIC INPUTS

DESCRIPTION

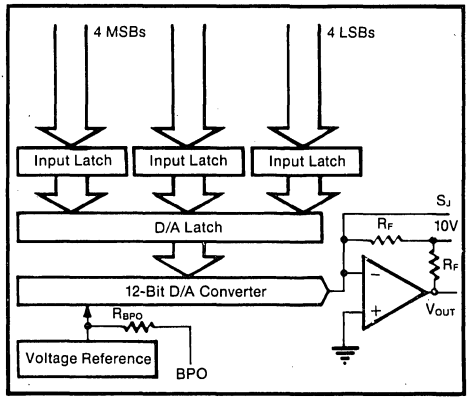
The DAC811U is a complete single-chip integrated-circuit microcomputer-compatible 12-bit digital-to-analog converter packaged in a 28-lead plastic SOIC. The chip includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches with laser-trimmed thin-film resistors provide a highly accurate and fast D/A converter.

Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nybbles to permit interfacing to 4-, 8-, 12- or 16-bit buses and to handle right- or left-justified data. The 12-bit data in the input latches is transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values and saves computer instructions.

The DAC811 is laser trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (K grade) at 25°C and ±3/4LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range.

DAC811JU and KU are specified over the temperature range of 0°C to +70°C.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C. $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

MODEL	DAC811JU			DAC811KU			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT							
Resolution			12			*	Bits
Codes[1]		USB, BOB			*		
Digital Inputs Over Temperature Range[2]							
V_{IH}	+2.0		+15	*		*	VDC
V_{IL}	0.0		+0.8	*		*	VDC
I_{IH}, V_I = +2.7V			+10			*	µA
I_{IL}, V_I = +0.4V			±20			*	µA
Digital Interface Timing Over Temperature Range[3]							
t_{WP}, $\overline{WR}$ pulse width	50			*			ns
$t_{AW}1$, $\overline{Nx}$ and $\overline{LDAC}$ valid to end of $\overline{WR}$	50			*			ns
t_{DW}, data valid to end of $\overline{WR}$	80			*			ns
t_{DH}, data valid hold time	0			*			ns
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[4]		±0.1	±0.2		*	*	%
Offset Error[4,5]		±0.05	±0.15		*	*	% of FSR[6]
Monotonicity		Guaranteed			*		
Power Supply Sensitivity: $+V_{CC}$		±0.001	±0.003		*	*	% of FSR/%V_{CC}
$-V_{CC}$		±0.002	±0.006		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0005	±0.0015		*	*	% of FSR/%V_{DD}
DRIFT (0°C to +70°C)							
Gain		±10	±30		*	*	ppm/°C
Unipolar Offset		±5	±10		*	*	ppm of FSR/°C
Bipolar Zero		±5	±10		*	*	ppm of FSR/°C
Linearity Error Over Temperature Range		±1/2	±3/4		±1/4	*	LSB
Monotonicity Over Temperature Range		Guaranteed			*		
CONVERSION SPEED							
SETTLING TIME[7] (to within ±0.01% of FSR of final value, 2kΩ load)							
For Full-Scale Range Change: 20V Range		3	4		*	*	µs
10V Range		3	4		*	*	µs
For 1LSB Change at Major Carry[8]		1			*		µs
Slew Rate[7]	8	12		*	*		V/µs
OUTPUT							
ANALOG OUTPUT							
Voltage Range ($\pm V_{CC}$ = 15V)[9]: Unipolar		0 to +10			*		V
Bipolar		±5, ±10			*		V
Output Current	±5			*			mA
Output Impedance (at DC)		0.2			*		Ω
Short Circuit to Common Duration		Indefinite			*		
REFERENCE VOLTAGE							
Voltage	+6.2	+6.3	+6.4	*	*	*	V
Source Current Available for External Loads	+2.0			*			mA
Temperature Coefficient		±10	±30		*	*	ppm/°C
Short Circuit to Common Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	VDC
$-V_{CC}$	−11.4	−15	−16.5	*	*	*	VDC
V_{DD}	+4.5	+5	+5.5	*	*	*	VDC
Current (no load): $+V_{CC}$		+16	+25		*	*	mA
$-V_{CC}$		−23	−35		*	*	mA
V_{DD}		+8	+15		*	*	mA
Potential at DCOM with Respect to ACOM[10]			±0.5			*	V
Power Dissipation		625	800		*	*	mW
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Storage	−60		+100	*		*	°C

*Same as DAC811JU.

NOTES: (1) USB = Unipolar Straight Binary, BOB = Bipolar Offset Binary. (2) TTL-, LSTTL-, 74HC CMOS-compatible. (3) Refer to Figures 6 and 7. (4) Adjustable to zero with external trim potentiometer. (5) Error at input code 000_{16} for both unipolar and bipolar ranges. (6) FSR means Full Scale Range and is 20V for the ±10V range. (7) Maximum represents the 3σ limit. Not 100% tested for this parameter. (8) At the major carry, $7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$. (9) Minimum supply voltage required for ±10V output swing is ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V with no external load. (10) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

ORDERING INFORMATION

DAC811 X U

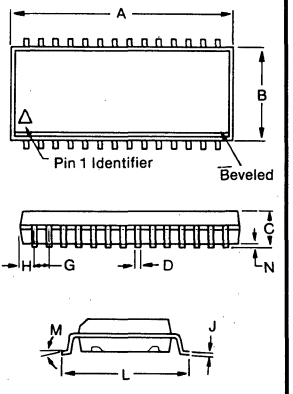
- Basic Model
- Grade
- Package Type

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$ to ACOM	0 to ±18V
V_{DD} to DCOM	0 to +7V
Input Voltage Range	$\pm V_{CC}$
Digital Inputs	−0.4V to V_{CC}
Lead Temp, Wave Soldering (3 seconds max)	+260°C
Output Short Circuit to Common	Continuous
Power Dissipation	1W

NOTE: Stresses above those listed may cause permanent damage to the device. Exposures to absolute maximum conditions for extended periods may effect device reliability.

MECHANICAL



NOTE: Leads in true position within 0.010" (.25mm) R at MMC at seating plane.

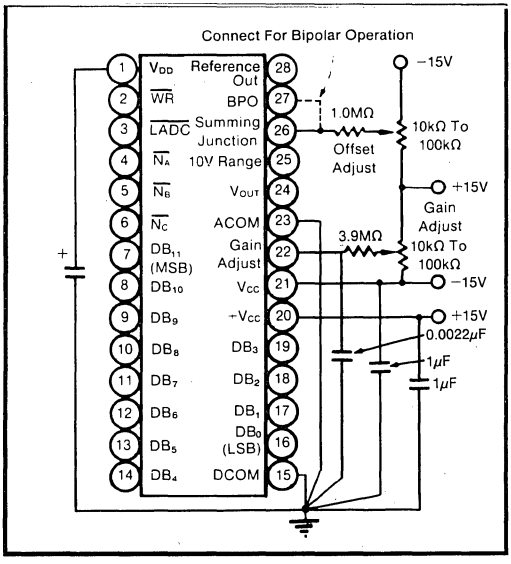
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.700	.716	17.78	18.19
B	.286	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.281	.309	7.14	7.85
M	5° TYP		5° TYP	
N	.007	.011	0.18	0.28

PIN NOMENCLATURE

PIN	NAME	FUNCTION
1	V_{DD}	Logic Supply, +5V
2	$\overline{WR}$	WRITE, command signal to load latches, Logic low loads latches.
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	NYBBLE A, enables $\overline{WR}$ to load input latch A (the most significant nybble). Logic low enables.
5	$\overline{N_B}$	NYBBLE B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	NYBBLE C, enables $\overline{WR}$ to load input latch C (the least significant nybble). Logic low enables.
7	D_{11}	DATA, Bit 12, MSB, positive true.
8	D_{10}	DATA, Bit 11
9	D_9	DATA, Bit 10
10	D_8	DATA, Bit 9
11	D_7	DATA, Bit 8
12	D_6	DATA, Bit 7
13	D_5	DATA, Bit 6
14	D_4	DATA, Bit 5

PIN	NAME	FUNCTION
15	DCOM	DIGITAL COMMON, V_{DD} supply return
16	D_0	DATA, Bit 1, LSB
17	D_1	DATA, Bit 2
18	D_2	DATA, Bit 3
19	D_3	DATA, Bit 4
20	$+V_{CC}$	Analog Supply Input, +15V or +12V
21	$-V_{CC}$	Analog Supply Input, −15V or −12V
22	GAIN ADJ	To externally adjust gain
23	ACOM	ANALOG COMMON, $\pm V_{CC}$ supply return
24	V_{OUT}	D/A converter voltage output
25	10V RANGE	Connect to pin 24 for 10V Range
26	SJ	SUMMING JUNCTION of output amplifier
27	BPO	BIPOLAR OFFSET. Connect to pin 26 for Bipolar Operation
28	REF OUT	6.3V reference output

CONNECTION DIAGRAM



DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC811 accepts positive true binary input codes. It may be connected by the user for any one of the following codes: USB (unipolar straight binary), BOB (bipolar offset binary) or, using an external inverter on the MSB line, BTC (binary two's complement). See Table I.

TABLE I. Digital Input Codes.

DIGITAL INPUT		ANALOG OUTPUT		
MSB ↓	LSB ↓	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
111111111111		+Full Scale	+Full Scale	−1LSB
100000000000		+1/2 Full Scale	Zero	−Full Scale
011111111111		1/2 Full Scale −1LSB	−1LSB	+Full Scale
000000000000		Zero	−Full Scale	Zero

*Invert the MSB of the BOB code with external inverter to obatin BTC code.

LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1's" and all "0's"). The DAC811 linearity error is specified at ±1/4LSB (max) at +25°C for the K grade and ±1/2LSB (max) for the J grade.

DIFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. The DAC811 is monotonic over the entire specification temperature range.

DRIFT

Gain drift is a measure of the change of the full-scale range output over the specification temperature range. Drift is expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by testing the full-scale range value (e.g., +FS minus −FS) at high temperature, +25°C, and low temperature; calculating the error with respect to the +25°C value and dividing by the temperature change.

Unipolar offset drift is a measure of the change in output with all 0's on the input over the specification temperature range. Offset is measured at high temperature, +25°C, and low temperature. The maximum change in offset referred to the +25°C value divided by the temperature change is the offset drift. It is expressed in parts per million of full-scale range per degree centigrade (ppm of FSR/°C).

Bipolar zero drift is measured at a digital input of 800_{16}, the code that gives zero volts output for bipolar operation.

SETTLING TIME

Settling time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of full-scale range (FSR): two for maximum full-scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC811 contains an on-chip 6.3V reference. This voltage (pin 28) has a tolerance of ±0.1V. The reference output may be used to drive external loads, sourcing at least 2.0mA. This current should be constant for best performance of the D/A converter.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A coonverter output. It is defined as a percent of FSR output change per percent of change in either the positive, negative, or logic supply voltages about the nominal voltages. Figure 1 shows typical power supply rejection versus power supply ripple frequency.

OFFSET AND GAIN ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

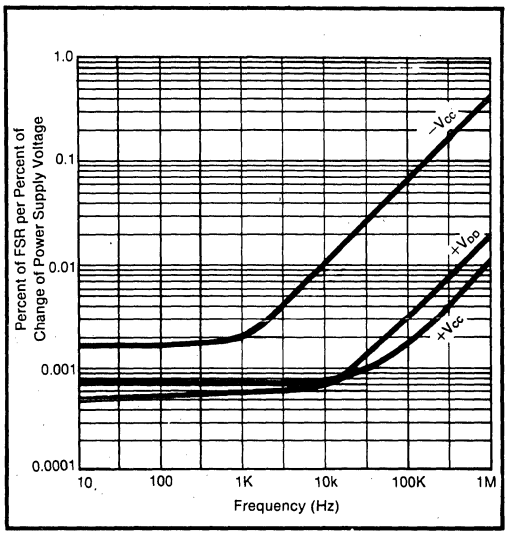


FIGURE 1. Power Supply Rejection versus Power Supply Ripple Frequency.

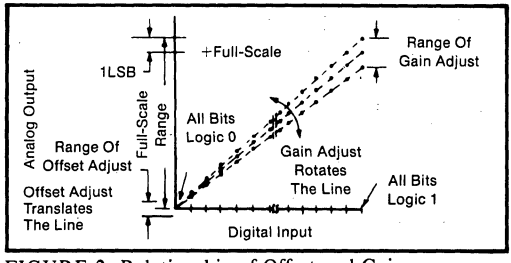


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

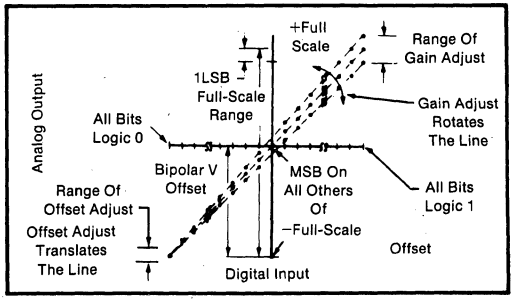


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

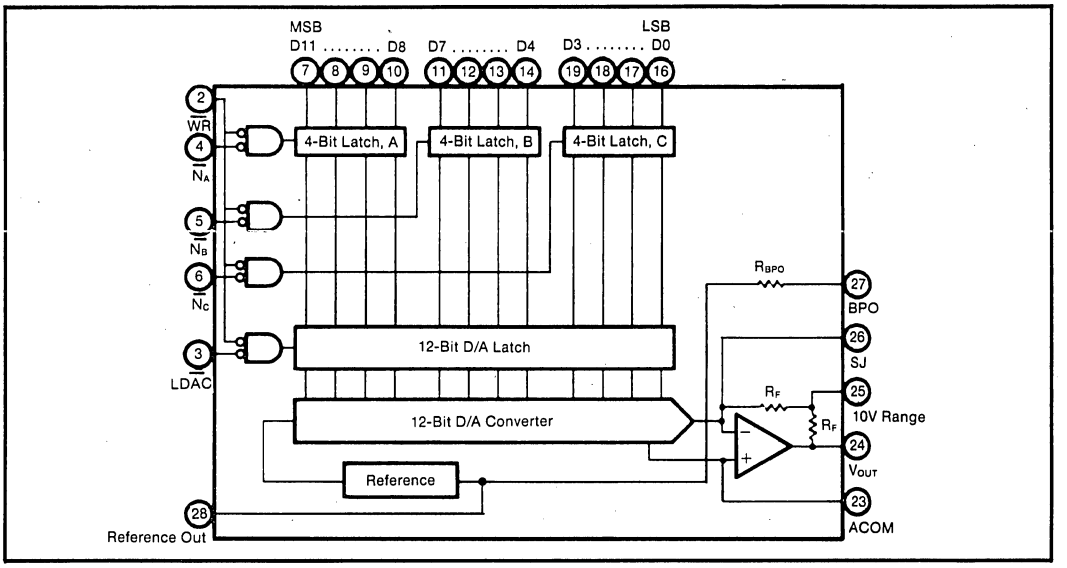


FIGURE 4. DAC811 Block Diagram.

OPERATION

DAC811 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 4.

±12V OPERATION

The DAC811 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10, the power supplies must be ±13.5V or greater. When operating with ±12V supplies, the output swing is restricted to approximately ±8V.

LOGIC INPUT COMPATIBILITY

The DAC811 digital inputs are TTL, LSTTL, and 54/74HC CMOS-compatible over the operating range of V_{DD}. The input switching threshold remains at the TTL threshold over the supply range.

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic "0." When either $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic "1," the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic "0."

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic "0." When either $\overline{LDAC}$ or $\overline{WR}$ are at logic "1," the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic "0."

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1," the data is latched. A truth table for all latches is given in Table II and Relatative Timing Diagrams are shown in Figures 5 and 6.

TABLE II. DAC811 Interface Logic Truth Table.

$\overline{WR}$	$\overline{N_A}$	$\overline{N_B}$	$\overline{N_C}$	$\overline{LDAC}$	OPERATION
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4MSBs
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4LSBs
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care

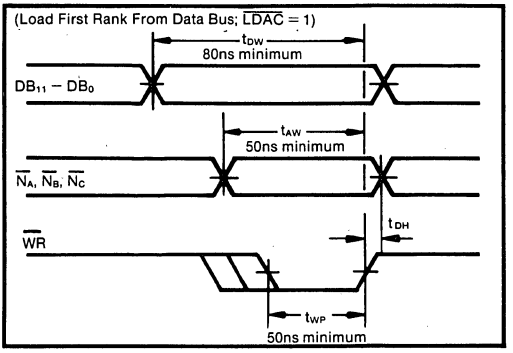


FIGURE 5. Write Cycle #1 (Data Latched from Data Bus).

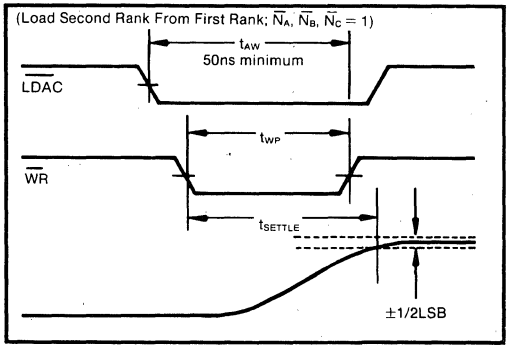


FIGURE 6. Write Cycle #2 (Data Transferred to DAC).

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram. TCR of the potentiometers should be 100ppmm/°C or less. The 1.0MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the DAC811 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 7, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.0022μF ceramic capacitor should be connnected from this pin to analog common to reduce noise pickup in all applications, including those not employing external gain adjustment.

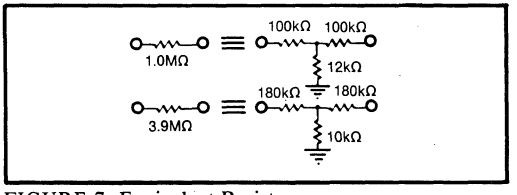


FIGURE 7. Equivalent Resistances.

Offset Adjustment

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full-scale voltage. Example: If the full-scale range is connected for 20V, the maximum negative output voltage is −10V. See Table III for corresponding codes.

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full-scale voltage. See Table III for positive full-scale voltages.

TABLE III. Digital Input/Analog Output, $\pm V_{CC} = \pm 15V$.

DIGITAL INPUT	ANALOG OUTPUT VOLTAGE		
	0 to 10V	±5V	±10V
12-Bit Resolution MSB LSB			
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5.0000V	0.0000V	0.0000V
011111111111	+4.9976V	−0.0024V	−0.0049V
000000000000	0.0000V	−5.0000V	−10.0000V
1LSB	2.44mV	2.44mV	4.88mV

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC811 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 8. Connections for the output ranges are listed in Table IV.

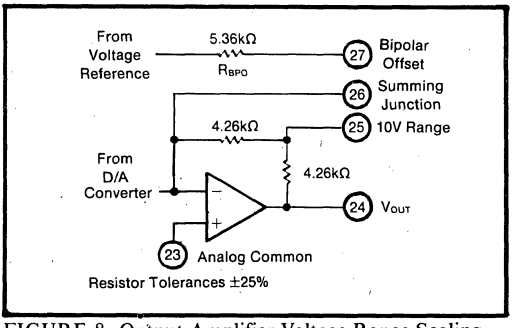


FIGURE 8. Output Amplifier Voltage Range Scaling Circuit.

TABLE IV. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 25 To	Connect Pin 27 To
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

INSTALLATION

POWER SUPPLY CONECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram.

These capacitors (1μF tantalum recommended) should be located close to the DAC811.

The DAC811 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The analog common (pin 23) and digital common (pin 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected.

Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may cause noise to be coupled through to the analog output, therefore, some caution is requried in applying these common connections.

The analog common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the analog common.

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC811 interface logic allows easy interface to microcomputer bus structures. The control signal $\overline{WR}$ is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{N}_S$ A, $\overline{N}_B$, $\overline{N}_C$, and $\overline{LDAC}$ determine which of the latches are enabled. It is permissible to enable two or more latches simultaneously as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC811s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are unused, the base address decoder can be simplified or eliminated altogether. For instance if half the memory space is unused, address line A_{15} of the microcomputer can be used as the chip select control.

4-BIT INTERFACE

An interface to a 4-bit microcomputer is shown in Figure 9. Each DAC811 occupies four address locations. A 74LS139 provides the two to four decoder and selects these with the base address. Memory Write ($\overline{WR}$) of the microcomputer is connected directly to the $\overline{WR}$ pin of the DAC811. An 8205 decoder is an alternative device to use instead of the 74LS139.

8-BIT INTERFACE

The control logic of DAC811 permits interfacing to right- or left-justified data formats illustrated in Figure 10. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figures 11 and 12 show an addressing scheme for right-justified and left-justified data respectively. The base address is decoded from the high-order address bits. A_0 and A_1 address the appropriate latches. Note that adjacent addresses are used. For the right-justified format $X10_{16}$ loads the 8LSBs and $X01_{16}$ loads the 4MSBs and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{16}$ and $X11_{16}$ are not used.

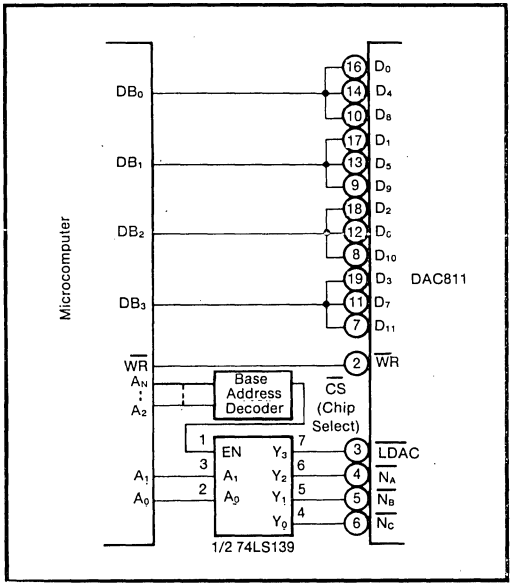


FIGURE 9. Addressing and Control for 4-Bit Microcomputer Interface.

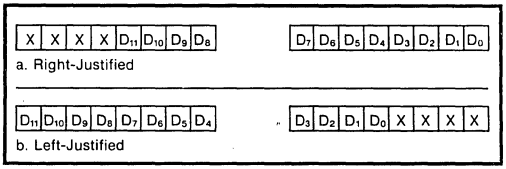


FIGURE 10. 12-Bit Data Formats for 8-Bit Systems.

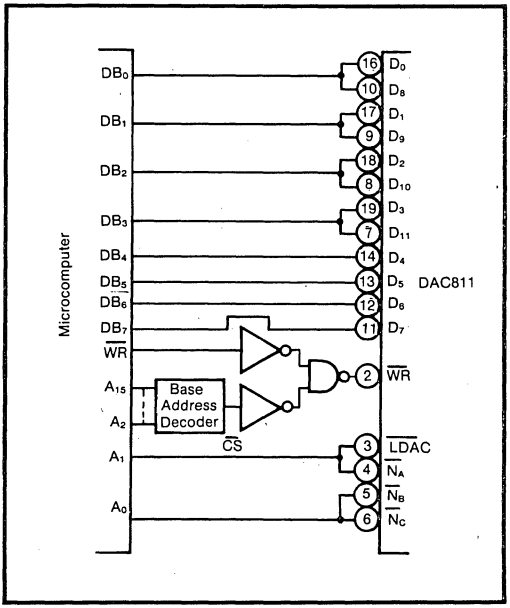


FIGURE 11. Right-Justified Data Bus Interface.

Left-justified data is handled in a similar manner, shown in Figure 12. The DAC811 still occupies two adjacent locations in the microcomputer's memory map.

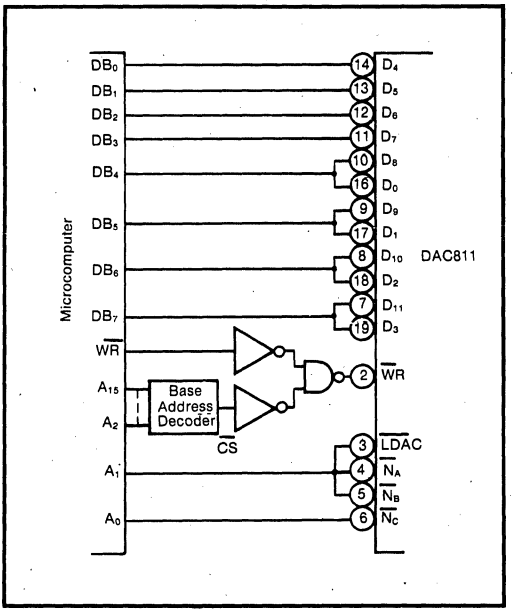


FIGURE 12. Left-Justified Data Bus Interface

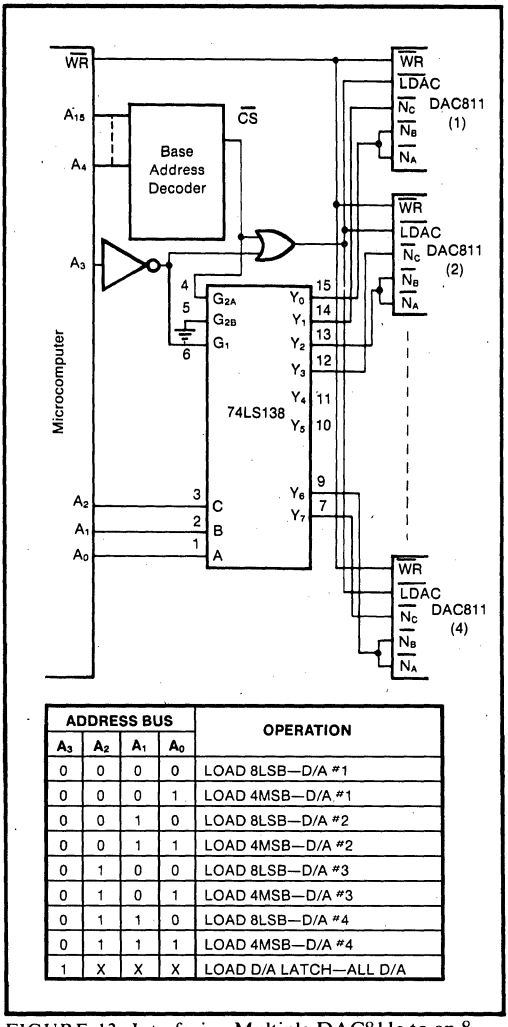
INTERFACING MULTIPLE DAC811s IN 8-BIT SYSTEMS

Many applications require that the outputs of several D/A converters be updated simultaneously such as automatic test systems. The interface shown in Figure 13 uses a 74LS138 decoder to decode a set of eight adjacent addresses to load the input latches of four DAC811s. The example shows a right-justified data format.

A ninth address using A_3 causes all DAC811s to be updated simultaneously. If a particular DAC811 is always loaded last, for instance, D/A #4, A_3 is not needed, thus saving eight address spaces for other uses. Incorporate A_3 into the Base Address Decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{N_C}$ of D/A #4, and connect G_1 of the 74LS138 to +5.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines, $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC811, is selected by the address decoder and strobed by $\overline{WR}$.



ADDRESS BUS				OPERATION
A_3	A_2	A_1	A_0	
0	0	0	0	LOAD 8LSB—D/A #1
0	0	0	1	LOAD 4MSB—D/A #1
0	0	1	0	LOAD 8LSB—D/A #2
0	0	1	1	LOAD 4MSB—D/A #2
0	1	0	0	LOAD 8LSB—D/A #3
0	1	0	1	LOAD 4MSB—D/A #3
0	1	1	0	LOAD 8LSB—D/A #4
0	1	1	1	LOAD 4MSB—D/A #4
1	X	X	X	LOAD D/A LATCH—ALL D/A

FIGURE 13. Interfacing Multiple DAC811s to an 8-Bit Bus.

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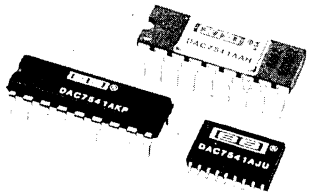


DAC7541A

Low Cost 12-Bit CMOS Four-Quadrant Multiplying DIGITAL-TO-ANALOG CONVERTER

FEATURES

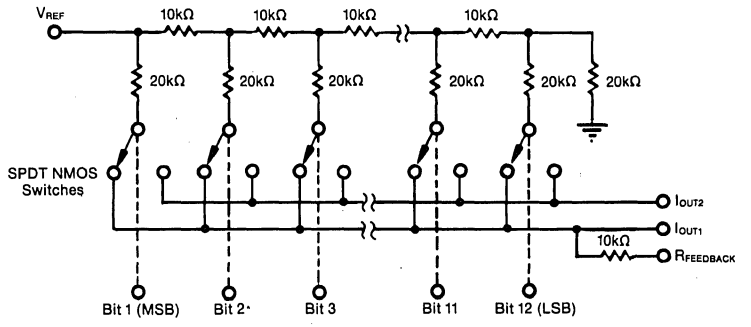
- FULL FOUR-QUADRANT MULTIPLICATION
- 12-BIT END-POINT LINEARITY
- DIFFERENTIAL LINEARITY ±1/2LSB MAX OVER TEMPERATURE (K/B/T GRADES)
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- TTL-/CMOS-COMPATIBLE
- SINGLE +5V TO +15V SUPPLY
- LATCH-UP RESISTANT
- 7521/7541/7541A REPLACEMENT
- PACKAGES: HERMETIC DIP, PLASTIC DIP, PLASTIC SOIC
- LOW COST

DESCRIPTION

The Burr-Brown DAC7541A is a low cost 12-bit, four-quadrant multiplying digital-to-analog converter. Laser-trimmed thin-film resistors on a monolithic CMOS circuit provide true 12-bit integral and differential linearity over the full specified temperature ranges.

The DAC7541A is a direct, improved pin-for-pin replacement for 7521, 7541, and 7541A industry standard parts. In addition to standard 18-pin plastic and hermetic ceramic packages, the DAC7541A is also available in a surface-mount plastic 18-pin SOIC.

FUNCTIONAL DIAGRAM



Digital Inputs (DTL/TTL/CMOS compatible)
Logic: A switch is closed to I_{OUT1} for its digital input in a "high" state.

Switches shown for digital inputs "high".

International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, $+V_{DD}$ = +12V or +15V, V_{REF} = +10V, $V_{PIN\ 1} = V_{PIN\ 2}$ = 0V unless otherwise specified.

MODEL	DAC7541A				
PARAMETER	**GRADE**	**T_A = +25°C**	**$T_A = T_{MIN}, T_{MAX}$[1]**	**UNITS**	**TEST CONDITIONS/COMMENTS**
ACCURACY					
Resolution	All	12	12	Bits	
Relative Accuracy	J, A, S	±1	±1	LSB max	±1LSB = ±0.024% of FSR.
	K, B, T	±1/2	±1/2	LSB max	±1/2LSB = ±0.012% of FSR.
Differential Non-linearity	J, A, S	±1	±1	LSB max	All grades guaranteed monotonic to
	K, B, T	±1/2	±1/2	LSB max	12 bits, T_{MIN} to T_{MAX}.
Gain Error	J, A, S	±6	±8	LSB max	Measured using internal R_{FB} and includes
	K, B, T	±1	±3	LSB max	effect of leakage current and gain T.C. Gain error can be trimmed to zero.
Gain Temperature Coefficient (ΔGain/ΔTemperature)	All		5	ppm/°C max	Typical value is 2ppm/°C.
Output Leakage Current: Out_1 (Pin 1)	J, K	±5	±10	nA max	All digital inputs = 0V.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
Out_2 (Pin 2)	J, K	±5	±10	nA max	All digital inputs = V_{DD}.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
REFERENCE INPUT					
Voltage (Pin 17 to GND)	All	−10/+10	−10/+10	V min/max	
Input Resistance (Pin 17 to GND)	All	7-18	7-18	kΩ min/max	Typical input resistance = 11kΩ. Typical input resistance temperature coefficient is −50ppm/°C.
DIGITAL INPUTS					
V_{IH} (Input **High** Voltage)	All	2.4	2.4	V min	
V_{IL} (Input **Low** Voltage)	All	0.8	0.8	V max	
I_{IN} (Input Current)	All	±1	±1	μA max	Logic inputs are MOS gates. I_{IN} typ (25°C) = 1nA.
C_{IN} (Input Capacitance)[2]	All	8	8	pF max	V_{IN} = 0V
POWER SUPPLY REJECTION					
$\Delta Gain/\Delta V_{DD}$	All	±0.01	±0.02	% per % max	V_{DD} = +11.4V to +16V
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min to V max	Accuracy is not guaranteed over this range.
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IH}.
		100	500	μA max	All digital inputs 0V or V_{DD}.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not production tested.
V_{DD} = +15V, V_{REF} = +10V except where stated, $V_{PIN\ 1} = V_{PIN\ 2}$ = 0V, output amp is OPA606 except where stated.

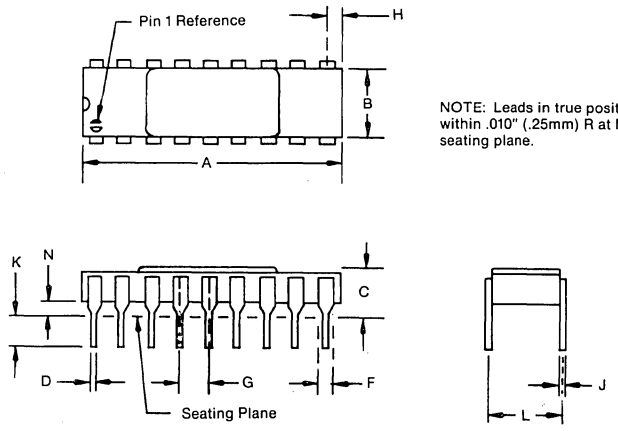
PROPAGATION DELAY (from Digital Input change to 90% of Final Analog Output)	All	100	—	ns typ	Out_1 Load = 100Ω, C_{EXT} = 13pF. Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
DIGITAL-TO-ANALOG GLITCH IMPULSE	All	1000	—	nV-s typ	V_{REF} = 0V, all digital inputs 0V to V_{DD} or V_{DD} to 0V. Measured using OPA606 as output amplifier.
MULTIPLYING FEEDTHROUGH ERROR (V_{REF} to Out_1)	All	1.0	—	mVp-p max	V_{REF} = ±10V, 10kHz sine wave.
OUTPUT CURRENT SETTLING TIME	All	0.6	—	μs typ	To 0.01% of Full Scale Range. Out_1 load = 100Ω, C_{EXT} = 13pF.
	All	1.0	—	μs max	Digital inputs: 0V to V_{DD} or V_{DD} to 0V.
OUTPUT CAPACITANCE					
$C_{OUT\ 1}$ (Pin 1)	All	100	100	pF max	Digital Inputs = V_{IH}
$C_{OUT\ 2}$ (Pin 2)	All	60	60	pF max	Digital Inputs = V_{IH}
$C_{OUT\ 1}$ (Pin 1)	All	70	70	pF max	Digital Inputs = V_{IL}
$C_{OUT\ 2}$ (Pin 2)	All	100	100	pF max	Digital Inputs = V_{IL}

NOTES: (1) Temperature ranges are: 0 to +70°C for JP, KP, JU and KU versions; −25°C to +85°C for AH, BH versions; −55°C to +125°C for SH, TH versions. (2) Guaranteed by design but not production tested.

MECHANICAL

Hermetic DIP

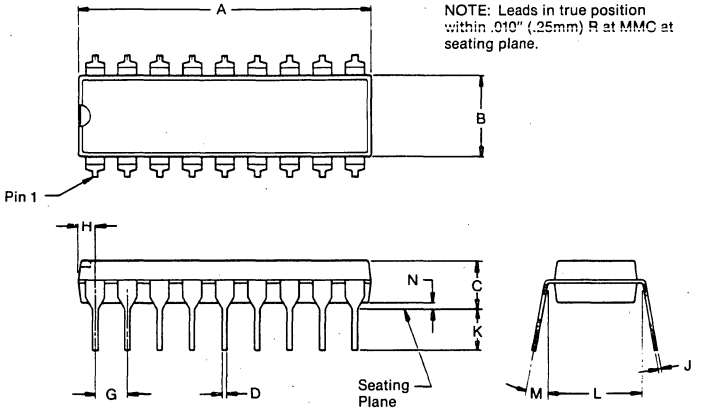
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	.960	—	24.38
B	.220	.310	5.59	7.87
C	—	.200	—	5.08
D	.014	.023	0.36	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.015	0.20	0.38
K	.125	.200	3.18	5.08
L	.290	.320	7.37	8.13
N	.015	.080	0.38	2.03



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Plastic DIP

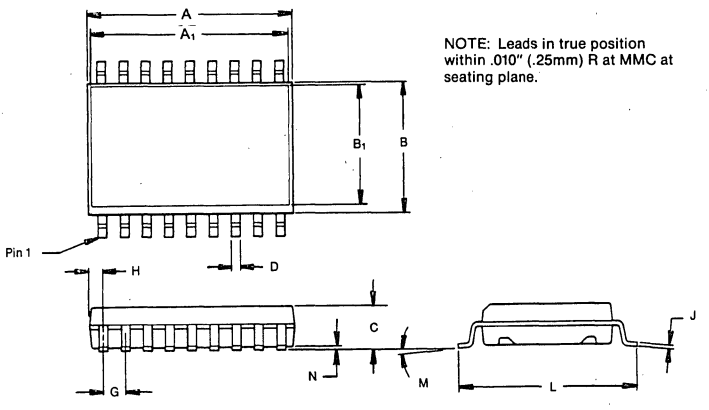
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.840	.940	21.34	23.88
B	.240	.280	6.10	7.11
C	—	.210	—	5.33
D	.014	.022	0.36	0.56
G	.100 BASIC		2.54 BASIC	
H	.040	.060	1.02	1.52
J	.008	.015	0.20	0.38
K	.115	.150	2.92	3.81
L	.280	.300	7.11	7.62
M	0°	10°	0°	10°
N	0.020	0.050	0.51	1.27



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Plastic SOIC

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.450	.466	11.43	11.84
A_1	.443	.446	11.25	11.33
B	.286	.302	7.26	7.67
B_1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30



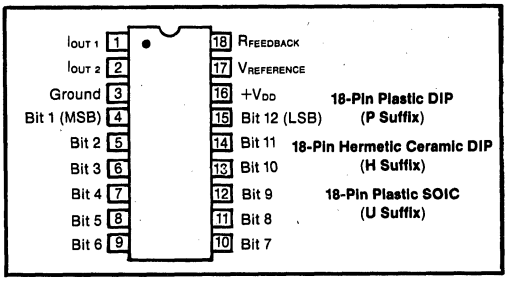
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} (pin 16) to Ground	+17V
V_{REF} (pin 17) to Ground	±25V
V_{RFB} (pin 18) to Ground	±25V
Digital Input Voltage (pins 4-15) to Ground	−0.4V, V_{DD}
$V_{PIN\ 1}$, $V_{PIN\ 2}$ to Ground	−0.4V, V_{DD}
Power Dissipation (any package):	
To +75°C	450mW
Derates above +75°C	−6mW/°C
Lead Temperature (soldering, 10s)	+300°C
Storage Temperature: Ceramic Package	+150°C
Plastic Package	+125°C

*Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS



CAUTION

The DAC7541A is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ENVIRONMENTAL SCREENING (QM SCREENING)

Burr-Brown /QM models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. All of the DAC7541xH grades are available with /QM screening.

/QM Screening (hermetic packages only)

Screen	MIL-STD-883 Method, Condition	Comments
Internal Visual	2010, B	
High Temperature Storage	1008, C	150°C, 24hrs
Temperature Cycle	1010, C	−65 to +150°C, 10 cycles
Burn-in	1015, B	+125°C
Constant Acceleration	2001, E	30,000G
Hermeticity: Fine Leak	1014, A1 or A2	5×10^{-8} atm cc/s
Gross Leak	1014, C	60psig, 2hrs
External Visual	2009	

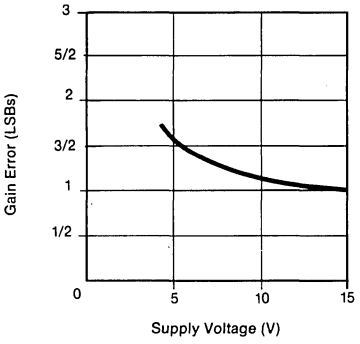
ORDERING INFORMATION

Model	Relative Accuracy (LSB)	Gain Error (LSB)	Package	Temperature Range (°C)
DAC7541AJP	±1	±6	Plastic DIP	0 to +70
DAC7541AKP	±1/2	±1	Plastic DIP	0 to +70
DAC7541AJU	±1	±6	Plastic SOIC	0 to +70
DAC7541AKU	±1/2	±1	Plastic SOIC	0 to +70
DAC7541AAH	±1	±6	Hermetic DIP	−25 to +85
DAC7541ABH	±1/2	±1	Hermetic DIP	−25 to +85
DAC7541ASH	±1	±6	Hermetic DIP	−55 to +125
DAC7541ATH	±1/2	±1	Hermetic DIP	−55 to +125

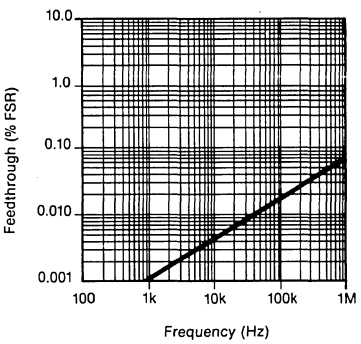
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V unless otherwise noted.

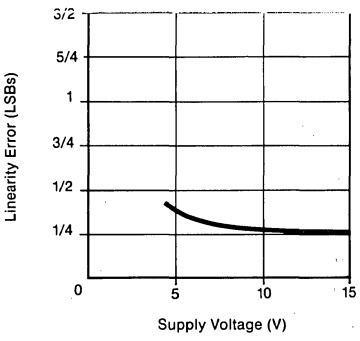
GAIN ERROR VS SUPPLY VOLTAGE



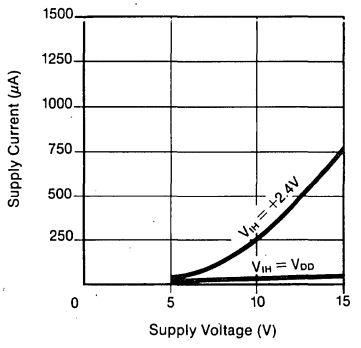
FEEDTHROUGH ERROR VS FREQUENCY



LINEARITY VS SUPPLY VOLTAGE



SUPPLY CURRENT VS SUPPLY VOLTAGE



DISCUSSION OF SPECIFICATIONS

Relative Accuracy

This term (also known as linearity) describes the transfer function of analog output to digital input code. The linearity error describes the deviation from a straight line between zero and full scale.

Differential Nonlinearity

Differential Nonlinearity is the deviation from an ideal 1LSB change in the output, from one adjacent output state to the next. A differential nonlinearity specification of ±1.0LSB guarantees monotonicity.

Gain Error

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC7541A is $-(4095/4096) \times (V_{REF})$. Gain error may be adjusted to zero using external trims.

Output Leakage Current

The measure of current which appears at Out_1 with the DAC loaded with all zeros, or at Out_2 with the DAC loaded to all ones.

Multiplying Feedthrough Error

This is the AC error output due to capacitive feedthrough from $V_{REFERENCE}$ to Out_1 with the DAC loaded to all zeros. This test is performed at 10kHz.

Output Current Settling Time

This is the time required for the output to settle to a tolerance of ±0.5LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

Propagation Delay

This is the measure of the delay of the internal circuitry and is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

Digital-to-Analog Glitch Impulse

This is the measure of the area of the glitch energy measured in nV-seconds. Key contributions to glitch energy are digital word-bit timing differences, internal circuitry timing differences, and charge injected from digital logic.

The measurement is performed with $V_{REFERENCE}$ = Ground, an OPA606 as the output op amp, and C_1 (phase compensation) = 0pF.

Monotonicity

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC7541A is guaranteed monotonic to 12 bits.

Power Supply Rejection

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

The DAC7541A is a 12-bit multiplying D/A converter consisting of a highly stable thin-film R-2R ladder network and 12 pairs of current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifer.

A simplified circuit of the DAC7541A is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\ 1}$ and $I_{OUT\ 2}$ bus lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The input resistance at $V_{REFERENCE}$ (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the $V_{REFERENCE}$ pin is constant, the reference terminal can be driven by a reference voltage or a reference current, AC or DC, of positive or negative polarity.

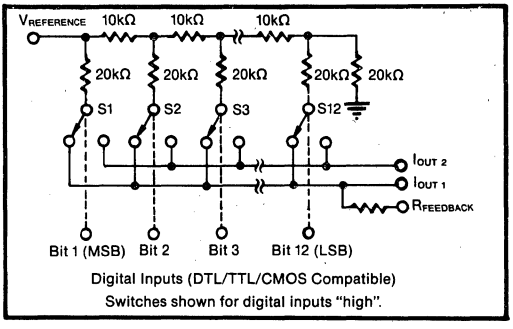


FIGURE 1. Simplified DAC Circuit.

EQUIVALENT CIRCUIT ANALYSIS

Figures 2 and 3 show the equivalent circuits for all digital inputs low and high respectively. The reference current is switched to $I_{OUT\ 2}$ when all inputs are low and $I_{OUT\ 1}$ when inputs are high. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant one-bit current drain through the ladder terminating resistor. The output capacitance is dependent upon the digital input code, and is therefore modulated between the low and high values.

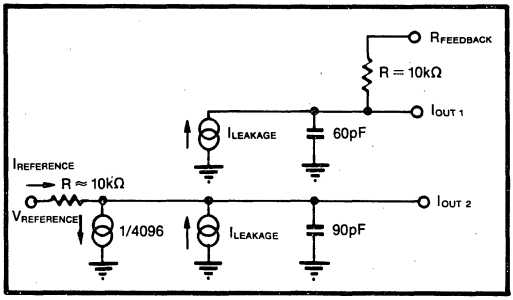


FIGURE 2. DAC7541A Equivalent Circuit (All Inputs Low).

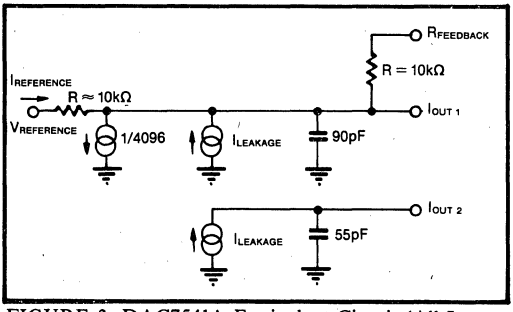


FIGURE 3. DAC7541A Equivalent Circuit (All Inputs High).

DYNAMIC PERFORMANCE

Output Impedance

The output resistance, as in the case of the output capacitance, is also modulated by the digital input code. The resistance looking back into the $I_{OUT\ 1}$ terminal may be anywhere between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high).The static accuracy and dynamic performance will be affected by this modulation. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the DAC7541A. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically dampen the output. See Figures 4 and 6.

APPLICATIONS

OP AMP CONSIDERATIONS

The input bias current of the op amp flows through the feedback resistor, creating an error voltage at the output of the op amp. This will show up as an offset through all

codes of the transfer characteristics. A low bias current op amp such as the OPA606 is recommended.

Low offset voltage and V_{OS} drift are also important. The output impedance of the DAC is modulated with the digital code. This impedance change (approximately 10kΩ to 30kΩ) is a change in closed-loop gain to the op amp. The result is that V_{OS} will be multiplied by a factor of one to two depending on the code. This shows up as a linearity error. Offset can be adjusted out using Figure 4. Gain may be adjusted using Figure 5.

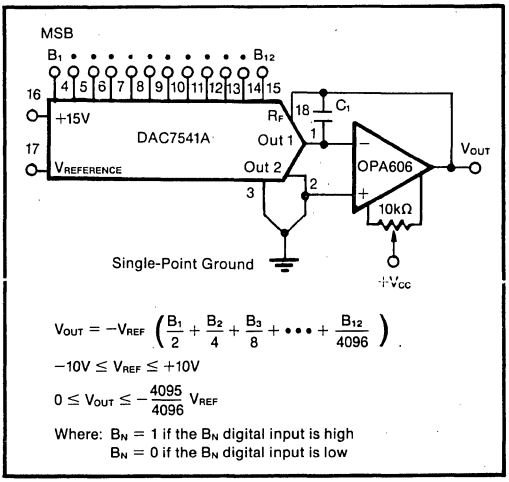


FIGURE 4. Basic Connection With Op Amp V_{OS} Adjust: Unipolar (two-quadrant) Multiplying Configuration.

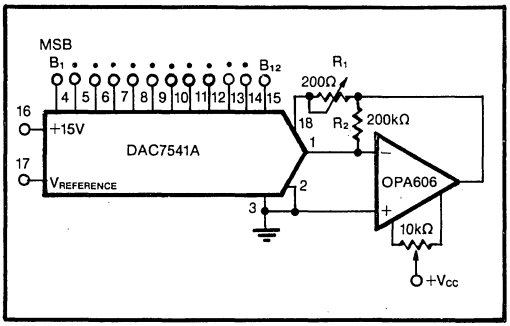


FIGURE 5. Basic Connection with Gain Adjust (allows adjustment up or down).

UNIPOLAR BINARY OPERATION (TWO-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (two-quadrant multiplication) operation. With a DC reference voltage or current (positive or negative polarity) applied at pin 17, the circuit is a unipolar D/A converter. With an AC reference voltage or current, the circuit provides two-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table I.

C_1 phase compensation (10 to 25pF) in Figure 4 may be required for stability when using high speed amplifiers. C_1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at Out_1.

TABLE I. Unipolar Codes.

Binary Input	Analog Output
MSB LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096)
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

R_1 in Figure 5 provides full scale trim capability—load the DAC register to 1111 1111 1111, adjust R_1 for $V_{OUT} = -V_{REF}$ (4095/4096). Alternatively, full scale can be adjusted by omitting R_1 and R_2 and trimming the reference voltage magnitude.

BIPOLAR FOUR-QUADRANT OPERATION

Figure 6 shows the connections for bipolar four-quadrant operation. Offset can be adjusted with the A_1 to A_2 summing resistor, with the input code set to 1000 0000 0000. Gain may be adjusted by varying the feedback resistor of A_2. The input/output relationship is shown in Table II.

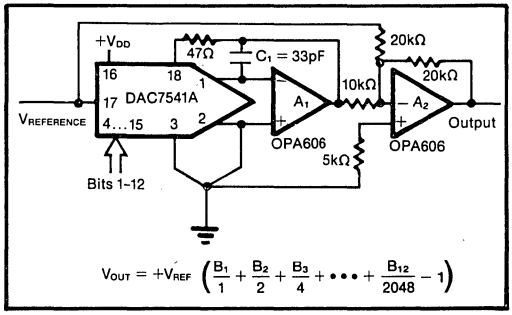


FIGURE 6. Bipolar Four-Quadrant Multiplier.

TABLE II. Bipolar Codes.

Binary Input	Analog Output
MSB LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

DIGITALLY CONTROLLED GAIN BLOCK

The 7541A may be used in a digitally controlled gain block as shown in Figure 7. This circuit gives a range of gain from one (all bits = one) to 4096 (LSB = one). The transfer function is:

$$V_{OUT} = \frac{-V_{IN}}{\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \bullet\bullet\bullet + \frac{B_{12}}{4096}\right)}$$

All bits off is an illegal state, as division by zero is impossible (no op amp feedback). Also, errors increase as gain increases, and errors are minimized at major carries (only one bit on at a time).

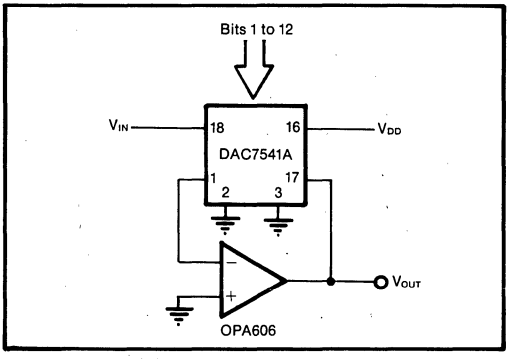


FIGURE 7. Digitally Programmable Gain Block.

BURR-BROWN®

DAC7545

ADVANCE INFORMATION
Subject to Change

Low-Cost 12-Bit CMOS Buffered Multiplying DIGITAL-TO-ANALOG CONVERTER

FEATURES

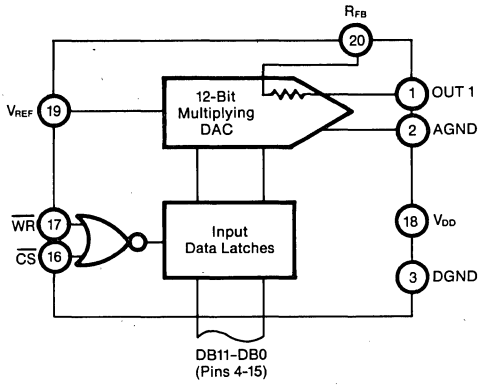
- FOUR-QUADRANT MULTIPLICATION
- LOW GAIN TC: 2PPM/°C typ
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- SINGLE 5V TO 15V SUPPLY
- TTL/CMOS LOGIC COMPATIBLE
- VERY LOW OUTPUT LEAKAGE: 10nA max
- VERY LOW OUTPUT CAPACITANCE: 70pF max
- VERY LOW GLITCH ENERGY: 250nV-s typ
- PROTECTION SCHOTTKY NOT REQUIRED
- DIRECT REPLACEMENT FOR AD7545, PM7545A

DESCRIPTION

The DAC7545 is a low-cost CMOS, 12-bit four-quadrant multiplying, digital-to-analog converter with input data latches. The input data is loaded into the DAC as a 12-bit data word. The data flows through to the DAC when both the chip select ($\overline{CS}$) and the write ($\overline{WR}$) pins are at a logic low.

Laser-trimmmed thin-film resistors and excellent CMOS current switches provide true 12-bit integral and differential linearity. The device operates on a single +5V to +15V supply and is available in 20-pin side-brazed DIP, 20-pin plastic DIP or a 20-lead plastic SOIC package. Devices are specified over the commercial, industrial, and military temperature ranges and are available with additional reliability screening.

The DAC7545 is well suited for battery or other low power applications because the power dissipation is less than 0.5mW when used with CMOS logic inputs and V_{DD} = 5V.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

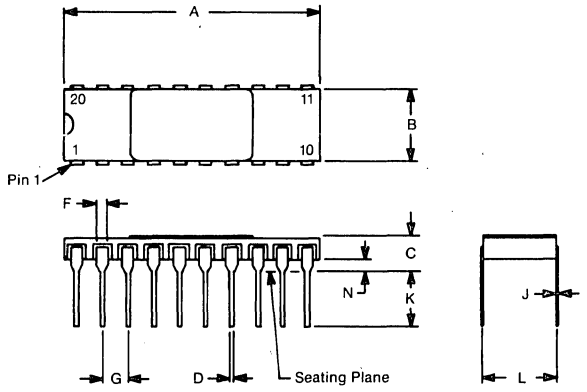
V_{REF} = +10V, $V_{OUT\,1}$ = 0V, ACOM = DCOM unless otherwise specified.

MODEL		DAC7545					
		V_{DD} = +5V		V_{DD} = +15V		UNITS	
PARAMETER	GRADE	T_A = +25°C	T_{MIN}-T_{MAX}[1]	T_A = +25°C	T_{MIN}-T_{MAX}[1]	(max)	TEST CONDITIONS/COMMENTS
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Relative Accuracy	J, A, S	±2	±2	±2	±2	LSB	
	K, B, T	±1	±1	±1	±1	LSB	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB	
	GL, GC, GU	±1/2	±1/2	±1/2	±1/2	LSB	
Differential Nonlinearity	J, A, S	±4	±4	±4	±4	LSB	10-bit monotonic, T_{MIN} to T_{MAX}.
	K, B, T	±1	±1	±1	±1	LSB	12-bit monotonic, T_{MIN} to T_{MAX}.
	L, C, U	±1	±1	±1	±1	LSB	12-bit monotonic, T_{MIN} to T_{MAX}.
	GL, GC, GU	±1	±1	±1	±1	LSB	12-bit monotonic, T_{MIN} to T_{MAX}.
Gain Error (with internal R_{FB})[2]	J, A, S	±20	±20	±25	±25	LSB	D/A register loaded with FFF_H. Gain error is adjustable using the circuits in Figures 4 and 5. Typical value is 2ppm/°C for V_{DD} = +5V.
	K, B, T	±10	±10	±15	±15	LSB	
	L, C, U	±5	±6	±10	±10	LSB	
	GL, GC, GU	±1	±2	±6	±7	LSB	
Gain Temperature Coefficient[3] (ΔGain/ΔTemperature)	All	±5	±5	±10	±10	ppm/°C	
DC Supply Rejection[3] (ΔGain/ΔV_{DD})	All	0.015	0.03	0.01	0.02	%/%	ΔV_{DD} = ±5%.
Output Leakage Current at Out 1	J, K, L, GL	±10	50	10	50	nA	DB_0-DB_{11} = 0V; $\overline{WR}$, $\overline{CS}$ = 0V.
	A, B, C, GC	±10	50	10	50	nA	
	S, T, U, GU	±10	200	10	200	nA	
DYNAMIC PERFORMANCE							
Current Settling Time[3]	All	2	2	2	2	μs	To 1/2LSB. Out_1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V.
Propagation Delay[3] (from digital input change to 90% of final analog output)	All	300		250		ns	Out_1 load = 100Ω. C_{EXT} = 13pF[4].
Glitch Energy	All	400		250		nV-s[5]	V_{REF} = ACOM.
AC Feedthrough at $I_{OUT\,1}$[6]	All	5	5	5	5	mVp-p[5]	V_{REF} = ±10V, 10kHz sine wave.
REFERENCE INPUT							
Input Resistance (pin 19 to ACOM)	All	7 25	7 25	7 25	7 25	kΩ[7] kΩ	Input resistance TC = 300ppm/°C[5].
AC OUTPUTS							
Output Capacitance[3]: $C_{OUT\,1}$	All	70	70	70	70	pF	DB_0-DB_{11} = 0V; $\overline{WR}$, $\overline{CS}$ = 0V.
$C_{OUT\,2}$	All	200	200	200	200	pF	DB_0-DB_{11} = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V.
DIGITAL INPUTS							
V_{IH} (Input **High** Voltage)	All	2.4	2.4	13.5	13.5	V[7]	
V_{IL} (Input **Low** Voltage)	All	0.8	0.8	1.5	1.5	V	
I_{IN} (Input Current)[8]	All	±1	±10	±1	±10	μA	V_{IN} = 0 or V_{DD}.
Input Capacitance[3]: DB_0-DB_{11}	All	5	5	5	5	pF	V_{IN} = 0V.
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF	V_{IN} = 0V.
SWITCHING CHARACTERISTICS[9]							
Chip Select to Write Setup Time t_{CS}	All	280 200	380 270	180 120	200 150	ns[7] ns[5]	See Figure 1.
Chip Select to Write Hold Time, t_{CH}	All	0	0	0	0	ns[7]	
Write Pulse Width, t_{WR}	All	250 175	400 280	160 100	240 170	ns[7] ns[5]	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$.
Data Setup Time, t_{DS}	All	140 100	210 150	90 60	120 80	ns[7] ns[5]	
Data Hold Time, t_{DH}	All	10	10	10	10	ns[7]	
POWER SUPPLY, I_{DD}	All	2	2	2	2	mA	All digital inputs V_{IL} or V_{IH}.
	All	100	500	100	100	μA	All digital inputs 0V or V_{DD}.
	All	10	10	10	10	μA[5]	All digital inputs 0V or V_{DD}.

NOTES: (1) Temperature ranges—JP, KP, LP, GLP: 0°C to 70°C. AH, BH, CH, GCH: −25°C to +85°C. SH, TH, UH, GUH: −55°C to +125°C. (2) This includes the effect of 5ppm max gain TC. (3) Guaranteed but not tested. (4) DB_0-DB_{11} = 0V to V_{DD} or V_{DD} to 0V. (5) Typical. (6) Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix H) to DCOM. (7) Minimum. (8) Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA. (9) Sample tested at +25°C to ensure compliance.

MECHANICAL

20-Pin Hermetic DIP (H Suffix)

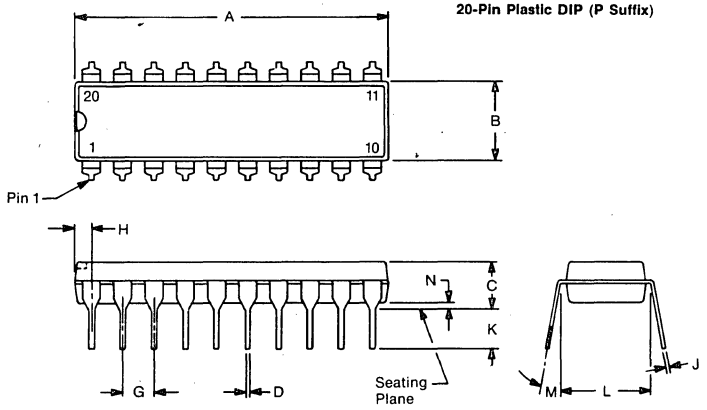


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.990	1.010	25.15	25.65
B	.285	.305	7.24	7.75
C	.100	.140	2.54	3.56
D	.016	.020	0.41	0.51
F	.054 TYP		1.37 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.31
K	.170 BASIC		4.32 BASIC	
L	.300	.320	7.62	8.13
N	.025	.045	0.64	1.14

20-Pin Plastic DIP (P Suffix)

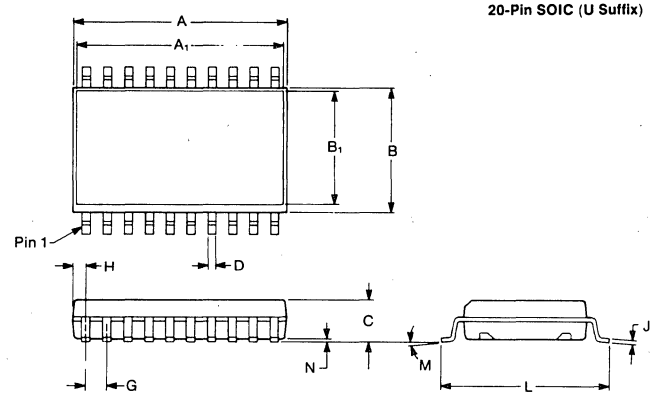


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.980	1.020	24.89	25.91
B	.240	.280	6.10	7.11
C	—	.210	—	5.33
D	.014	.022	0.36	0.59
G	.100 BASIC		2.54 BASIC	
H	.040	.060	1.02	1.52
J	.008	.015	0.20	0.38
K	.115	.150	2.92	3.81
L	.280	.300	7.11	7.62
M	0°	10°	0°	10°
N	.000	.020	0.00	0.51

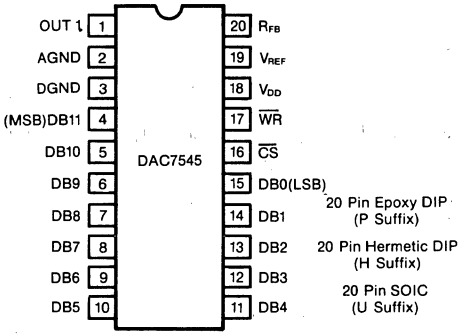
20-Pin SOIC (U Suffix)



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.502	.518	12.75	13.16
A_1	.495	.518	12.57	13.16
B	.286	.302	7.26	7.67
B_1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

PIN DESIGNATIONS



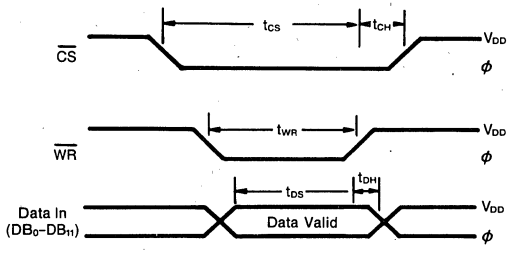
ABSOLUTE MAXIMUM RATINGS*

T_A = +25°C unless otherwise noted.

V_{DD} to DCOM ..... −0.3V, +17
Digital Input to DCOM..... −0.3V, V_{DD}
V_{RFB}, V_{REF}, to DCOM ..... ±25V
$V_{PIN\ 1}$ to DCOM ..... −0.3V, V_{DD}
ACOM to DCOM ..... −0.3V, V_{DD}
Power Dissipation: Any Package to +75°C 450mW
Derates above +75°C by... 6mW/°C
Operating Temperature:
Commercial—JP, KP, LP, GLP ..... 0°C to +70°C
Industrial—AH, BH, CH, GCH ..... −25°C to +85°C
Military—SH, TH, UH, GUH ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

***NOTE:** Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

WRITE CYCLE TIMING DIAGRAM



Mode Selection

Write Mode	Hold Mode
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB_0-DB_{11}) inputs	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB_0-DB_{11}) is locked out; DAC holds last data present when $\overline{CS}$ or $\overline{WR}$ assumed high state.

NOTES: V_{DD} = 5V; $t_R = t_F$ = 20ns.
V_{DD} = 15V; $t_R = t_F$ = 40ns.
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference is $V_{IH} + V_{IL\ 2}$

ENVIRONMENTAL SCREENING (QM SCREENING)

Burr-Brown /QM models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified.

	MIL-STD-883		
Screen	Method	Condition	Comments
Internal Visual	2010	B	
High Temperature Storage	1008	C	+150°C, 24hrs
Temperature Cycle	1010	C	−65 to +150°C, 10 Cycles
Burn-In	1015	B	+125°C, Figure 1
Constant Acceleration	2001	E	30,000G
Hermeticity: Fine Leak Gross Leak	1014 1014	A1 or A2 C	5×10^{-8} atm cc/s 60psig, 2hrs
External Visual	2009		

DISCUSSION OF SPECIFICATIONS

Relative Accuracy

This term (also known as linearity) describes the transfer function of analog output to digital input code. The linearity error describes the deviation from a straight line from zero to full scale (zero- and full-scale adjusted).

Differential Nonlinearity

Differential nonlinearity is the deviation from an ideal 1LSB change in the output, for adjacent input code changes. A differential nonlinearity specification of ±1.0LSB guarantees monotonicity.

Gain Error

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC7545 is −(4095/4096) (V_{REF}). Gain error may be adjusted to zero using external trims as shown in the applications section.

Output Leakage Current

The measure of current which appears at OUT 1 with the DAC loaded with all zeros.

Multiplying Feedthrough Error

This is the AC error output due to capacitive feedthrough from V_{REF} to OUT 1 with the DAC loaded to all zeros. This test is performed at 10kHz.

Output Current Settling Time

This is the time required for the output to settle to a tolerance of ±0.5LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

Propagation Delay

This is the measure of the delay of the internal circuitry and is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

Digital-To-Analog Glitch Impulse

This is the measure of the area of the glitch energy measured in nanovoit-seconds. Key contributions to glitch energy are internal circuitry timing differences and charge injected from digital logic. The measurement is performed with V_{REF} = GND and an OPA600 as the output op amp and C_1 (phase compensation) = 0pF.

Monotonicity

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC7545 is guaranteed monotonic to 12-bit accuracy, except the J, A, S grades are specified to be 10-bit monotonic.

Power Supply Rejection

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

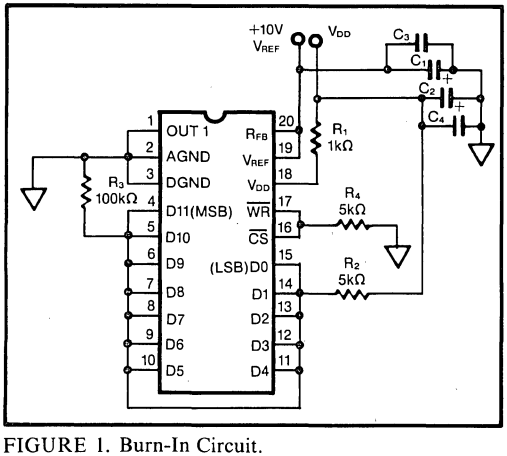


FIGURE 1. Burn-In Circuit.

Propogation Delay

This is the measure of the time that is required for the analog output to reach 90% of its final value for a change in digital input code.

CIRCUIT DESCRIPTION

Figure 2 shows a simplified schematic of the digital-to-analog converter portion of the DAC7545. The current from the V_{REF} pin is switched from $I_{OUT\ 1}$ to AGND by the FET switch. This circuit architecture keeps the resistance at the reference pin constant and equal to R_{LDR}, so the reference could be provided by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V even with V_{DD} = 5V. The R_{LDR} is equal to "R" and is typically 11kΩ. The output capacitance of the DAC7545 is code dependent and varies from a minimum value (70pF) at code 000_H to a maximum (200pF) at code FFF_H.

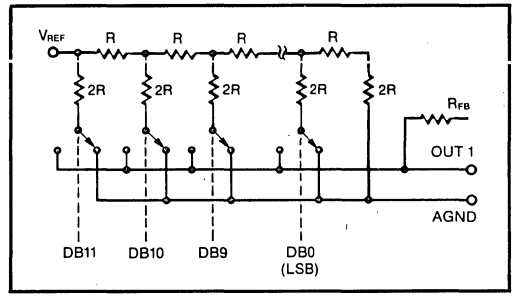


FIGURE 2. Simplified DAC Circuit of the DAC 7545.

The input buffers are CMOS inverters, designed so that when the DAC7545 is operated from a 5V supply (V_{DD}), the logic threshold is TTL-compatible. Being simple CMOS inverters, there is a range of operation where the inverters operate in the linear region and thus draw more supply current than normal. Minimizing this transition time and insuring that the digital inputs are operated as close to the rails as possible will minimize the supply drain current.

APPLICATIONS

Figure 3 shows the DAC7545 connected for unipolar operation. The high-grade DAC7545 is specified for a 1LSB gain error, so gain adjust is typically not needed. However, the resistors shown are for adjusting full-scale errors. The value of R_1 should be minimized to reduce the effects of mismatching temperature coefficients between the internal and external resistors. A range of adjustment of 1.5 times the desired range will be adequate. For example, for a DAC7545JP, the gain error is specified to be ±25LSB. A range of adjustment of

±37LSB will be adequate. The equation below results in a value of 458Ω for the potentiometer (use 500Ω).

$$R_1 = \frac{R_{LADDER}}{4096} \ (3 \times \text{Gain Error})$$

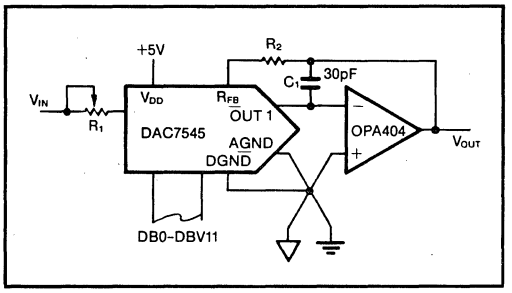


FIGURE 3. Unipolar Binary Operation.

The addition of R_1 will cause a negative gain error. To compensate for this error, R_2 must be added. The value of R_2 should be one-third the value of R_1.

The capacitor across the feedback resistor is used to compensate for the phase shift due to stray capacitances of the circuit board, the DAC output capacitance, and op amp input capacitance. Eliminating this capacitor will result in excessive ringing and an increase in glitch energy. This capacitor should be as small as possible to minimize settling time.

The circuit of Figure 3 may be used with input voltages up to ±20V as long as the output amplifier is biased to handle the excursions. Table I represents the analog output for four codes into the DAC for Figure 3.

TABLE I. Unipolar Codes.

Binary Code	Analog Output
MSB LSB	
1111 1111 1111	$-V_{IN}$ (4095/4096)
1000 0000 0000	$-V_{IN}$ (2048/4096) = 1/2V_{IN}
0000 0000 0001	$-V_{IN}$ (1/4096)
0000 0000 0000	0 Volts

Figure 4 shows the connections for bipolar four-quadrant operation. Offset can be adjusted with the A_1 to A_2 summing resistor, with the input code set to 1000 0000 0000. Gain may be adjusted by varying the feedback resistor of A_2. The input/output relationship is shown in Table II.

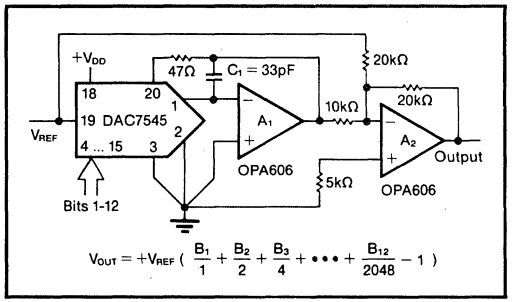


FIGURE 4. Bipolar Four-Quadrant Multiplier.

TABLE II. Bipolar Codes.

Binary Code	Analog Output
MSB LSB	
1111 1111 1111	+V_{REF} (2047/2048)
1000 0000 0000	0 Volts
0111 1111 1111	−V_{REF} (1/2048)
0000 0000 0000	−V_{REF} (2048/2048)

Figure 5 shows a hook-up for a digitally-controlled gain block. The feedback for the op amp is made up of the FET switch and the R-2R ladder. The input resistor to the gain block is the R_{FB} of the DAC7545. Since the FET switch is in the feedback loop, a "zero code" into the DAC will result in the op amp having no feedback, and a saturated op amp output.

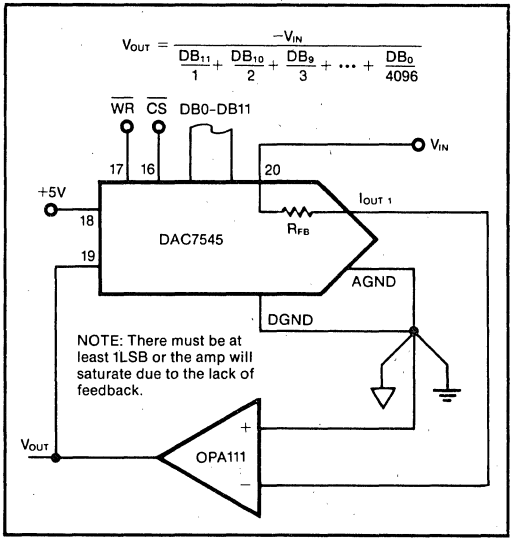


FIGURE 5. Digitally-Controlled Gain Block.

APPLICATIONS HINTS

CMOS DACS such as the DAC7545 exhibit a code-dependent output resistance. This resistance and the V_{OS} of the op amp cause error currents to flow that look like linearity and superposition errors. To minimize these errors, an op amp with a V_{OS} of less than 0.1LSB should be selected. Also, the op amp should have a gain that is sufficient to keep V_{OS} below 0.1LSB for the desired swing and load at the op amp output.

As with all analog circuits, the care in designing the ground system is critical to system accuracy. Static (DC) errors should be held to less than 0.1LSB for any point in the analog ground path. Holy point sensing is encouraged, so that all analog circuits are referenced to the same potential.

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BURR-BROWN®

DAC8012

ADVANCE INFORMATION
Subject to Change

Low Cost 12-Bit CMOS Latched-Readback Multiplying DIGITAL-TO-ANALOG CONVERTER

FEATURES

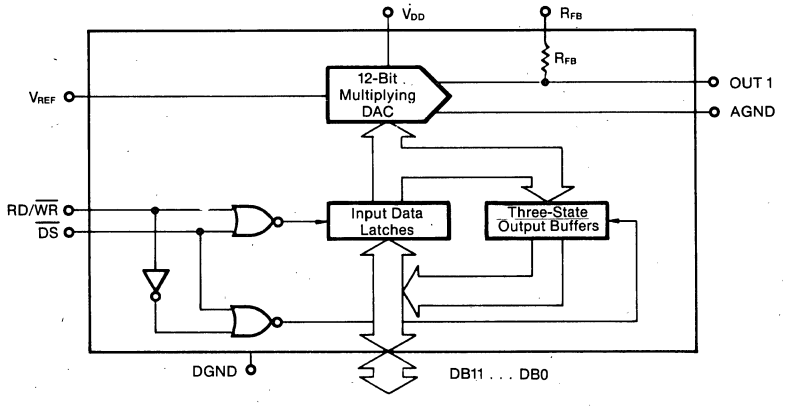
- DATA READBACK CAPABILITY
- FOUR-QUADRANT MULTIPLICATION
- LOW-GAIN TC: 2PPM/°C typ
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- SINGLE 5V TO 15V SUPPLY
- VERY LOW OUTPUT LEAKAGE (10nA max)
- VERY LOW OUTPUT CAPACITANCE (70pF max)
- VERY LOW GLITCH ENERGY (400nVs max)
- PROTECTION SCHOTTKY NOT REQUIRED
- DIRECT REPLACEMENT FOR PMI DAC8012

DESCRIPTION

The DAC8012 is a low-cost CMOS, 12-bit, four-quadrant multiplying, digital-to-analog converter with input data latches and readback capabilities. The input data is loaded into the DAC as a 12-bit data word. The data is loaded into the DAC from the bus when both the data strobe ($\overline{DS}$) and the read/write (RD/$\overline{WR}$) pins are held low. Data may be read back from the DAC by holding $\overline{DS}$ low and (RD/$\overline{WR}$) high. This readback feature enables the user to monitor the state of multiple DACs on a single bi-directional bus.

Laser-trimmed thin-film resistors and excellent CMOS current switches provide true 12-bit integral and differential linearity. The device operates on a single +5V to +15V supply and is available in 20-pin side-brazed DIP, 20-pin plastic DIP or a 20-lead plastic SOIC package. Devices are specified over the commercial, industrial, and military temperature ranges and are available with additional reliability screening.

The DAC8012 is well suited for battery or other low-power applications because the power dissipation is less than 0.5mW when used with CMOS logic inputs and $V_{DD} = 5V$.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{REF} = +10V, $V_{OUT\,1}$ = 0V, AGND = DGND = 0V unless otherwise noted.

PARAMETER	CONDITIONS	DAC8012B, K, T[1] MIN	DAC8012B, K, T[1] TYP	DAC8012B, K, T[1] MAX	DAC8012A, J, S[1] MIN	DAC8012A, J, S[1] TYP	DAC8012A, J, S[1] MAX	UNITS
V_{DD} = +5V or +15V								
STATIC ACCURACY								
Resolution		12			12			Bits
Relative Accuracy	T_A = Full temperature range			±1/2			±1	LSB
Differential Nonlinearity[2]	T_A = Full temperature range			±1			±1	LSB
Gain Error[3][4]	T_A = +25°C			±1			±3	LSB
	T_A = Full temperature Range			±2			±4	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature[5][6]				±5			±5	ppm/°C
DC Supply Rejection	T_A = +25°C (ΔV_{DD} = ±5%)			0.002			0.002	%/%
ΔGain/ΔV_{DD}[5]	T_A = Full temperature range (ΔV_{DD} = ±5%)			0.004			0.004	%/%
Output Leakage Current at OUT 1	T_A = +25°C, RD/$\overline{WR}$ = $\overline{DS}$ = 0V, all digital inputs = 0V			10			10	nA
	T_A = Full temperature range S, T versions			200			200	nA
	J, K, A, B versions			25			25	nA
DYNAMIC PERFORMANCE								
Propagation Delay[5][7][8]	T_A = +25°C (OUT 1 Load = 100Ω, C_{EXT} = 13pF)			300			300	ns
Current Settling Time[5][8]	T_A = Full temperature range (to 1/2 LSB) $I_{OUT\,1}$ Load = 100Ω			1			1	μs
Glitch Energy[5], V_{REF} = AGND	T_A = +25°C			400			400	nVs
	T_A = Full temperature range			500			500	nVs
AC Feedthrough at $I_{OUT\,1}$[5][11]	T_A = Full temperature range, V_{REF} = ±10V, f = 10kHz			5			5	mVp-p
REFERENCE INPUT								
Input Resistance (Pin 19 to GND)[12]	T_A = Full temperature range	7	11	15	7	11	15	kΩ
ANALOG OUTPUTS								
Output Capacitance[5]	T_A = Full temperature range							
$C_{OUT\,2}$	DB0-DB11 = 0V, RD/$\overline{WR}$ = $\overline{DS}$ = 0V			70			70	pF
$C_{OUT\,1}$	DB0-DB11 = V_{DD}, RD/$\overline{WR}$ = $\overline{DS}$ = 0V			150			150	pF
V_{DD} = +5V								
DIGITAL INPUTS								
Input High Voltage	T_A = Full temperature range	2.4			2.4			V
Input Low Voltage	T_A = Full temperature range			0.8			0.8	V
Input Current[9]	T_A = +25°C			1			1	μA
	T_A = Full temperature range			10			10	μA
Input Capacitance[5]: DB0-DB11	T_A = Full temperature range			12			12	pF
RD/$\overline{WR}$, $\overline{DS}$	T_A = Full temperature range			6			6	pF
DIGITAL OUTPUTS								
Output High Voltage	I_O = 400μA	4.0			4.0			V
Output Low Voltage	I_O = −1.6mA			0.4			0.4	V
Three-State Output Leakage Current				10			10	μA
SWITCHING CHARACTERISTICS[10]	See timing diagram							
Write to Data Stobe Setup Time	T_A = +25°C	0			0			ns
	T_A =Full temperature range	0			0			ns
Data Strobe to Write Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Read to Data Strobe Setup Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Read Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Write Mode Data Strobe Width	T_A = +25°C	180			180			ns
	T_A = Full temperature range	250			250			ns
Read Mode Data Strobe Width	T_A = +25°C	220			220			ns
	T_A = Full temperature range	290			290			ns
Data Setup Time	T_A = +25°C	210			210			ns
	T_A = Full temperature range	250			250			ns
Data Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Output Valid Time[13]	T_A = +25°C			300			300	ns
	T_A = Full temperature range			400			400	ns
Output Active Time from Deselection	T_A = +25°C			215			215	ns
	T_A = Full temperature range			375			375	ns
POWER SUPPLY	T_A = Full temperature range (all digital inputs V_{INL} or V_{INH})			2			2	mA
Supply Current	T_A = Full temperature range (all digital inputs 0V or V_{DD})		10	100		10	100	μA

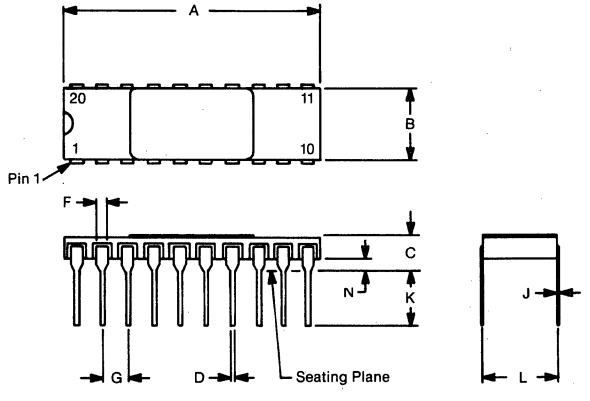
ELECTRICAL CHARACTERISTICS (CONT)

PARAMETER	CONDITIONS	DAC8012B, K, T[1] MIN	DAC8012B, K, T[1] TYP	DAC8012B, K, T[1] MAX	DAC8012A, J, S[1] MIN	DAC8012A, J, S[1] TYP	DAC8012A, J, S[1] MAX	UNITS
	V_{DD} = +15V							
DIGITAL INPUTS								
Input High Voltage	T_A = Full temperature range	13.5			13.5			V
Input Low Voltage	T_A = Full temperature range			1.5			1.5	V
Input Current[9]	T_A = +25°C			1			1	µA
	T_A = Full temperature range			10			10	µA
Input Capacitance[5]: DB0–DB11	T_A = Full temperature range			12			12	pF
RD/$\overline{WR}$, $\overline{DS}$	T_A = Full temperature range			10			10	pF
DIGITAL OUTPUTS								
Output High Voltage	I_O = 3mA	13.5			13.5			V
Output Low Voltage	I_O = −3mA			1.5			1.5	V
Three-State Output Leakage Current				10			10	µA
SWITCHING CHARACTERISTICS[10]	See Timing Diagram							
Write to Data Strobe Setup Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Write Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Read to Data Strobe Setup Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Read Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Write Mode Data Strobe Width	T_A = +25°C	100			100			ns
	T_A = Full temperature range	120			120			ns
Read Mode Data Strobe Width	T_A = +25°C	110			110			ns
	T_A = Full temperature range	150			150			ns
Data Setup Time	T_A = +25°C	90			90			ns
	T_A = Full temperature range	120			120			ns
Data Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Output Valid Time	T_A = +25°C			180			180	ns
	T_A = Full temperature range			220			220	ns
Output Active Time for Deselection	T_A = +25°C			180			180	ns
	T_A = Full temperature range			250			250	ns
POWER SUPPLY								
Supply Current	T_A = Full temperature range (all digital inputs V_{INL} or V_{INH})			2			2	mA
	T_A = Full temperature range (all digital inputs 0V or V_{DD})		10	100		10	100	µA

NOTES: (1) T_A = −55°C to +125°C for S, T grades. T_A = −25°C to +85°C for A, B grades. T_A = 0°C to +70°C for J, K grades. (2) 12-bit monotonic over full temperature range. (3) Includes the effects of 5ppm max gain T.C. (4) Using internal R_{FB}. DAC register loaded with 1111 1111 1111. (5) **Guaranteed** but **not tested**. (6) Typical value is 2ppm/°C for V_{DD} = +5V. (7) From digital input change to 90% of final analog output. (8) All digital inputs = 0V to V_{DD}; or V_{DD} to 0V. (9) Logic inputs are MOS gates, typical input current (at +25°C) is less than 1nA. (10) Sample tested at +25°C to ensure compliance. (11) Feedthrough can further be reduced by connecting the metal lid on the sidebraze package (Suffix H) to DGND. (12) Resistor T.C. = +100ppm/°C max. (13) C_L = 100pF.

MECHANICAL

20-Pin Hermetic DIP (H Suffix)

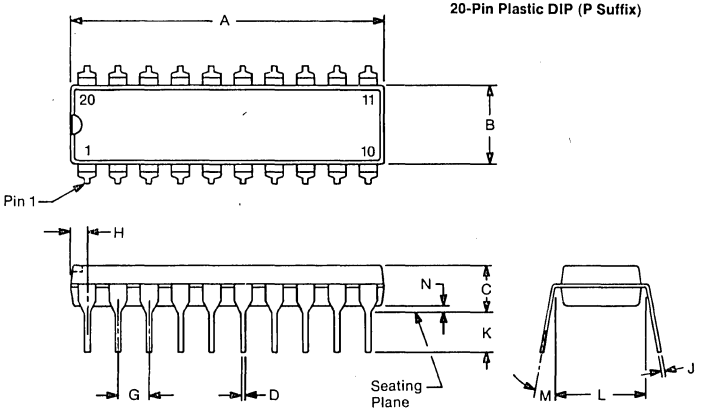


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.990	1.010	25.15	25.65
B	.285	.305	7.24	7.75
C	.100	.140	2.54	3.56
D	.016	.020	0.41	0.51
F	.054 TYP		1.37 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.31
K	.170 BASIC		4.32 BASIC	
L	.300	.320	7.62	8.13
N	.025	.045	0.64	1.14

20-Pin Plastic DIP (P Suffix)

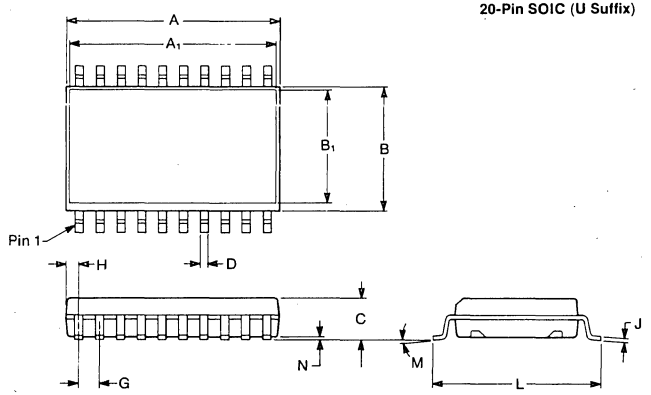


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.980	1.020	24.89	25.91
B	.240	.280	6.10	7.11
C	—	.210	—	5.33
D	.014	.022	0.36	0.59
G	.100 BASIC		2.54 BASIC	
H	.040	.060	1.02	1.52
J	.008	.015	0.20	0.38
K	.115	.150	2.92	3.81
L	.280	.300	7.11	7.62
M	0°	10°	0°	10°
N	.000	.020	0.00	0.51

20-Pin SOIC (U Suffix)

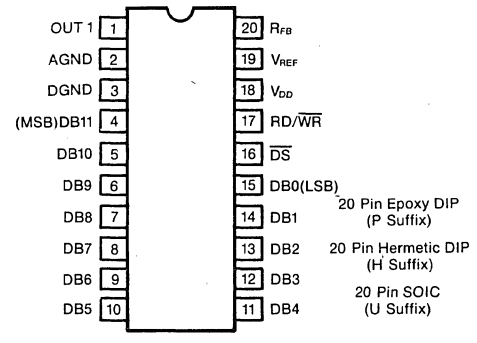


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.502	.518	12.75	13.16
A_1	.495	.518	12.57	13.16
B	.286	.302	7.26	7.67
B_1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

PIN DESIGNATIONS



ABSOLUTE MAXIMUM RATINGS

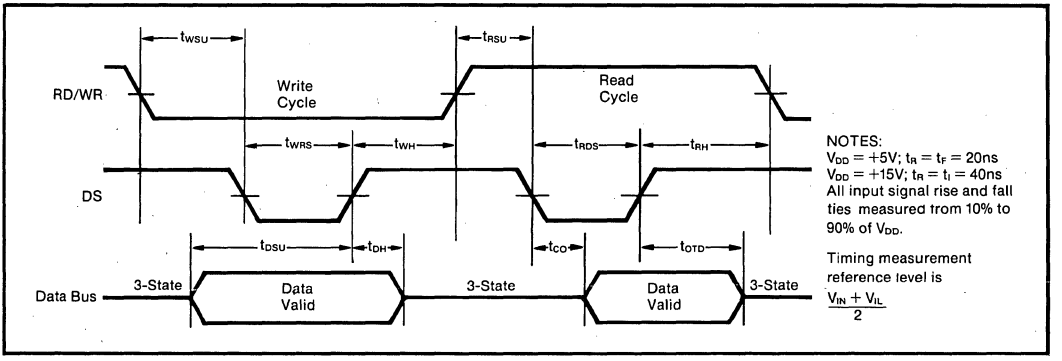
(T_A = +25°C, unless otherwise noted.)

V_{DD} to DGND ..... −.03V, +17V
Digital Input Voltage to DGND ..... −0.3V, V_{DD}
AGND to DGND ..... −0.3V, V_{DD}
V_{RFB}, V_{REF} to DGND ..... ±25V
$V_{PIN\ 1}$ to DGND ..... −0.3V, V_{DD}
Power Dissipation (any package) to +75°C 450mW
Derates Above +75°C by ..... 6mW/°C
Operating Temperature Range
Military Grades ..... −55°C to +125°C
Industrial Grades ..... −25°C to +85°C
Commercial Grades ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 60s) ..... +300°C

CAUTION

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
3. The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper antistatic handling procedures.
4. Remove power before inserting or removing units from their sockets.

TIMING DIAGRAM



ENVIRONMENTAL SCREENING (QM SCREENING)

Burr-Brown /QM models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and procedures employed; it does not imply conformance to any other military standards or to any method of MIL-STD-883 other than those specified.

Screen	MIL-STD-883 Method, Condition	Comments
Internal Visual	2010, B	
High Temperature Storage	1008, C	150°C, 24hrs
Temperature Cycle	1010, C	−65°C to +150°C, 10 Cycles
Burn-In	1015, B	+125°C, Figure 1
Constant Acceleration	2001, E	30,000G
Hermeticity: Fine Leak	1014, A1 or A2	5×10^{-8} atm cc/s
Gross Leak	1014, C	60psig, 2hrs
External Visual	2009	

DISCUSSION OF SPECIFICATIONS

Relative Accuracy

This term (also known as linearity) describes the transfer function of analog output to digital input code. The linearity error describes the deviation from a straight line from zero to full scale (zero and full scale adjusted).

Differential Nonlinearity

Differential nonlinearity is the deviation from an ideal 1LSB change in the output, for adjacent input code changes. A differential nonlinearity specification of ±1LSB guarantees monotonicity.

Gain Error

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC8012 is −(4095/4096) (V_{REF}). Gain error may be adjusted to zero using external trims as shown in the applications section.

Output Leakage Current

The measure of current which appears at OUT_I with the DAC loaded with all zeros.

Multiplying Feedthrough Error

This is the AC error output due to capacitive feedthrough from V_{REF} to OUT_I with the DAC loaded to all zeros. This test is performed at 10kHz.

Output Current Settling Time

This is the time required for the output to settle a tolerance of ±1/2LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

Propagation Delay

This is the measure of the delay of the internal circuitry and is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

Digital-To-Analog Glitch Impulse

This is the measure of the area of the glitch energy measured in nanovolt-seconds. Key contributions to glitch energy are internal circuitry timing differences and charge injected from digital logic. The measurement is performed with V_{REF} = GND.

Monotonicity

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC8012 is guaranteed monotonic to 12-bit accuracy except the J, A, S grades are specified 10-bit monotonic.

Power Supply Rejection

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

Propogation Delay

This is the measure of the time that is required for the analog output to reach 90% of its final value for a change in digital input code.

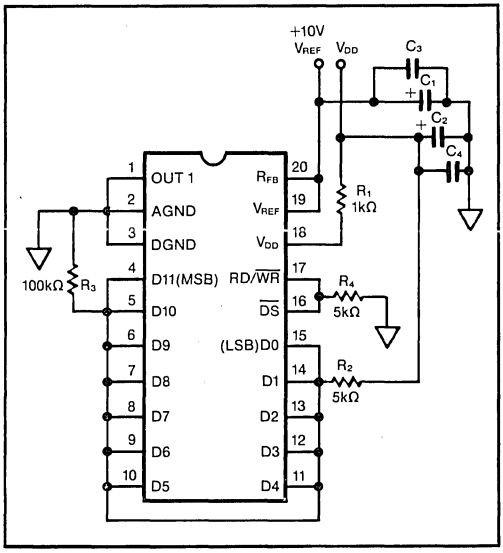


FIGURE 1. Burn-In Circuit.

CIRCUIT DESCRIPTION

DIGITAL-TO-ANALOG SECTION

Figure 2 shows a simplified schematic of the digital-to-analog portion of the DAC8012. The current from the V_{REF} pin is switched from $I_{OUT\ 1}$ to AGND by the FET switch for that bit. This circuit architecture keeps the resistance at the reference pin constant and equal to R_{LDR}, so the reference could be provided by either a voltage or

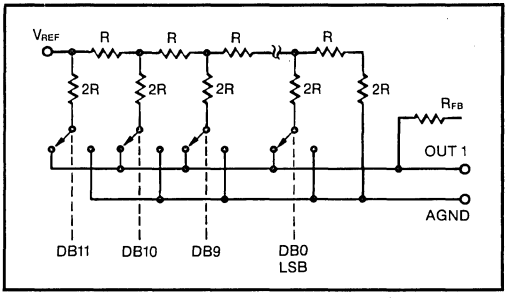


FIGURE 2. Simplified Circuit of the DAC8012.

current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V even with V_{DD} = 5V. The R_{LDR} is equal to "R" and is typically 11kΩ.

The output capacitance of the DAC8012 is code dependent and varies from a minimum value (70pF) at code 000_H to a maximum (200pF) at code FFF_H.

The input buffers are CMOS inverters, designed so that when the DAC8012 is operated from a 5V supply (V_{DD}), the logic threshold is TTL compatible. Being simple CMOS inverters, there is a range of operation where the inverters operated in the linear region and thus draw more supply current than normal. Minimizing the transition time and insuring that the digital inputs are operated as close to the rails as possible will minimize the supply drain current.

DIGITAL SECTION

Figure 3 shows the basic current switch. Figure 4 shows the schematic of the input/output buffers. When the $\overline{DS}$ and the RD/$\overline{WR}$ are held low the latches are transparent and pass data from the data bus to the DAC. When the $\overline{DS}$ is held low and the RD/$\overline{WR}$ line is held high, the three-state buffer becomes active and the data at the DAC is presented to the digital input/output lines for data readback.

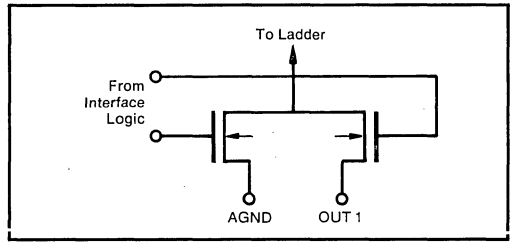


FIGURE 3. N-Channel Current Steering Switch.

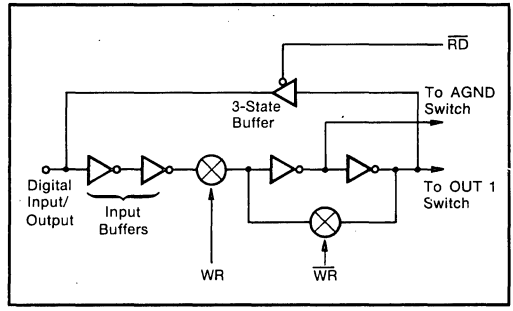


FIGURE 4. Digital Input/Output Structure.

APPLICATIONS

Figure 5 shows the DAC8012 connected for unipolar operation. The high-grade DAC8012 is specified for a 1LSB gain error, so gain adjust is typically not needed. However, the resistors shown are for adjusting full-scale errors. The value of R_1 should be minimized to reduce the effects of mismatching temperature coefficients

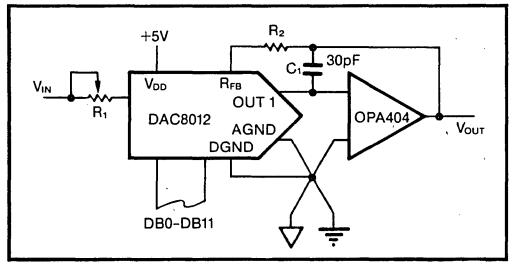


FIGURE 5. Unipolar Binary Operation.

between the internal and external resistors. A range of adjustment of 1.5 times the desired range will be adequate. For example, for a DAC8012JP, the gain error is specified to be ±3LSB. A range of adjustment of ±4.5LSB will be adequate. The equation shows a minimum value of 33Ω for the pot.

$$R_1 = (R_{LADDER}/4096) \times (3 \times \text{Gain Error})$$

The addition of R_1 will cause a negative gain error. To compensate for this error, R_2 must be added. The value of R_2 should be one third the value of R_1.

The capacitor across the feedback resistor is used to compensate for the phase shift due to stray capacitances of the circuit board, the DAC output capacitance, and op amp input capacitance. Eliminating this capacitor will result in excessive ringing and an increase in glitch energy in higher speed applications. This capacitor should be as small as possible to minimize settling time.

The circuit of Figure 5 may be used with input voltages of up to ±20V as long as the output amplifier is biased to handle the excursions. Table I presents the analog ouput for four codes into the DAC for Figure 5.

TABLE I. Unipolar Output Code for Figure 5.

Binary Code	Analog Output
MSB↓ ↓LSB	
1111 1111 1111	$-V_{IN}$ (4095/4096)
1000 0000 0000	$-V_{IN}$ (2048/4096) = 1/2V_{IN}
0000 0000 0001	$-V_{IN}$ (1/4096)
0000 0000 0000	0 Volts

BIPOLAR FOUR-QUADRANT OPERATION

Figure 6 shows the connections for bipolar four-quadrant operation. Offset can be adjusted with the A_1 to A_2 summing resistor, with the input code set to 1000 0000 0000. Gain may be adjusted by varying the feedback resistor of A_2. The input/output relationship is shown in Table II.

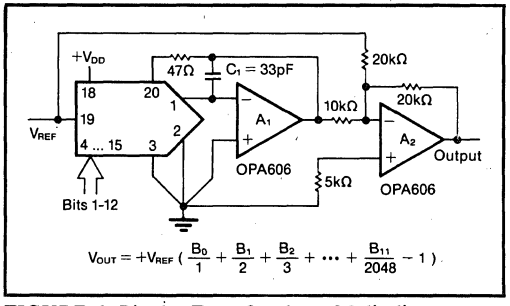


FIGURE 6. Bipolar Four-Quadrant Mulitplier.

TABLE II. Bipolar Codes and Analog Output for Figure 6.

Binary	Analog Output
MSB↓ ↓LSB	
1111 1111 1111	+V_{REF} (2047/2048)
1000 0000 0000	0 Volts
0111 1111 1111	−V_{REF} (1/2048)
0000 0000 0000	−V_{REF} (2048/2048)

Figure 7 shows a hook-up for a digitally-controlled gain block. The feedback for the op amp is made up of the FET switch and the R-2R ladder. The input resistor to the gain block is the R_{FB} of the DAC8012. Since the FET switch is in the feedback loop, a "zero code" into the DAC will result in the op amp having no feedback and a saturated op amp output. The DAC8012 readback feature makes the DAC8012 especially good for this configuration

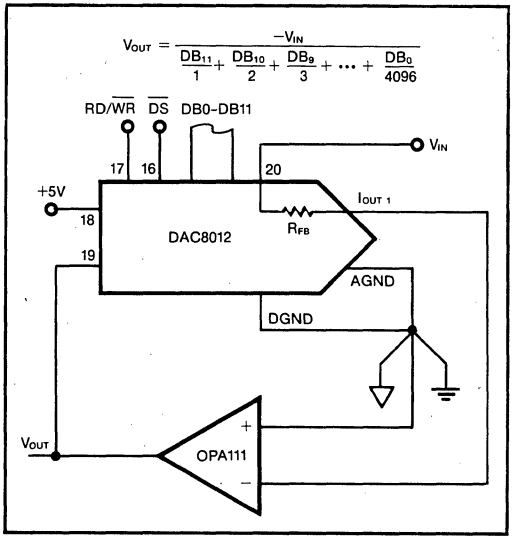


FIGURE 7. Digitally-Controlled Gain Block.

when an automatic gain or automatic calibration routine is used. If the logic were set up to calibrate a value via logic external to the processor (successive approximation register), then when the calibration is done, the processor could read the DAC8012 to store away the calibration code.

Figure 8 shows the DAC8012 interfaced to a 16-bit

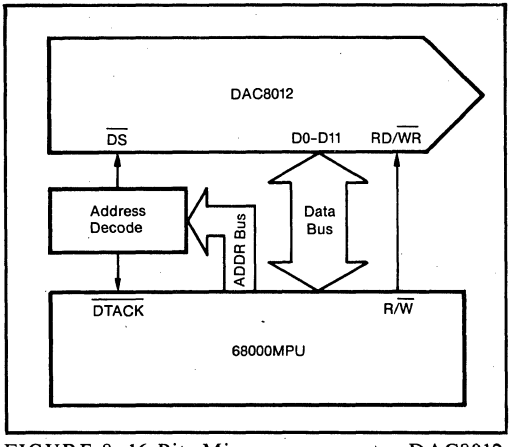


FIGURE 8. 16-Bit Microprocessor to DAC8012 Interface.

microprocessor. The interface requires only address decoding to select the DAC to be written to or read from.

Figure 9 shows an interface scheme for using the DAC8012 with an 8-bit microprocessor. The data for the first 4 bits are written and latched into the external write latch and the next 8 bits are presented on the bus. The DAC8012 is then instructed to pass the data through the internal DAC latch ($\overline{WR} + \overline{DS}$) and all 8 bits are transferred into the DAC. Reading data back is done in the same manner.

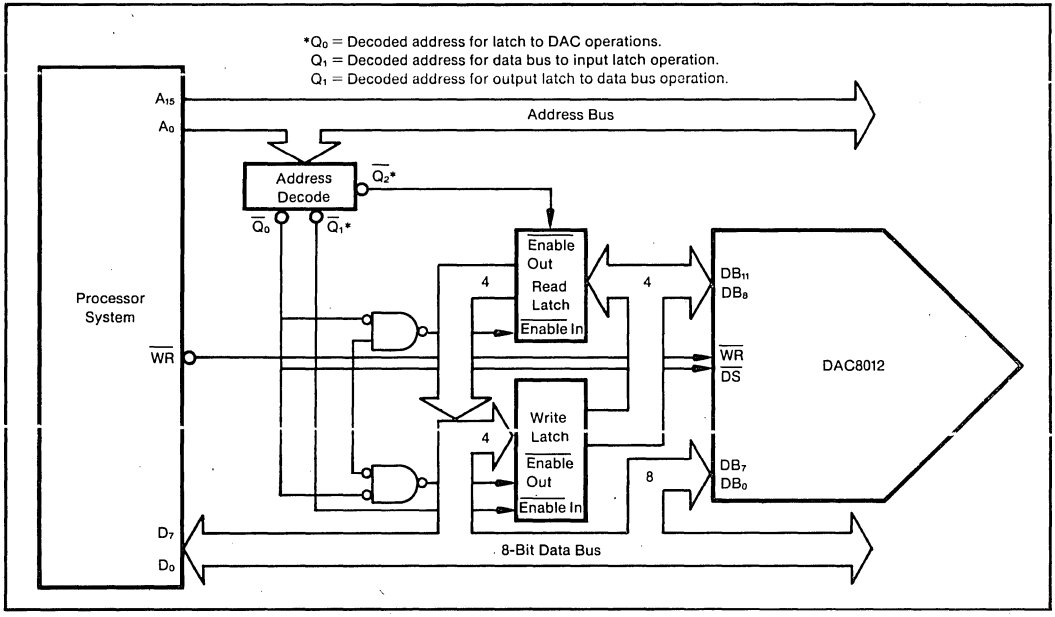
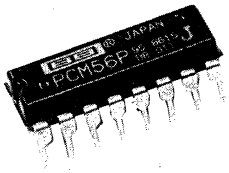


FIGURE 9. 8-Bit Processor to DAC8012 Interface.

BURR-BROWN®



PCM56P

DESIGNED FOR AUDIO

Serial Input 16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

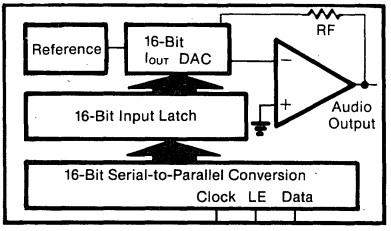
- SERIAL INPUT
- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 15-BIT MONOTONICITY, TYP
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.0025% MAX THD (FS Input, K Grade, 16 Bits)
- 0.02% MAX THD (–20dB Input, K Grade, 16 Bits)
- 1.5μs SETTLING TIME, TYP (Voltage Out)
- 96dB DYNAMIC RANGE
- ±3V or ±1mA AUDIO OUTPUT
- EIAJ STC-007-COMPATIBLE
- OPERATES ON ±5V to ±12V SUPPLIES
- PINOUT ALLOWS I_{OUT} OPTION
- PLASTIC DIP PACKAGE

DESCRIPTION

The PCM56P is a state-of-the-art, fully monotonic, digital-to-analog converter that is designed and specified for digital audio applications. This device employs ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

This converter is completely self-contained with a stable, low noise, internal zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V to ±12V. Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero) to further improve total harmonic distortion (THD) specifications if desired. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps assure the user of high system reliability and outstanding overall system performance.

The PCM56P is packaged in a high-quality 16-pin molded plastic DIP package and has passed operating life tests under simultaneous high-pressure, high-temperature, and high-humidity conditions.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

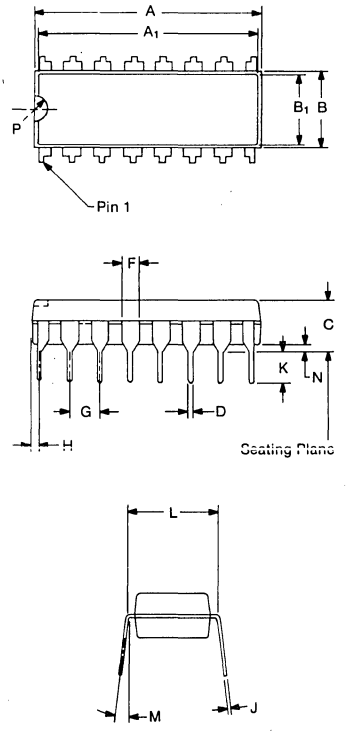
ELECTRICAL

Typical at +25°C and nominal power supply voltages of ±5V unless otherwise noted.

MODEL	PCM56P/-J/-K			
	MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Digital Inputs[1]: V_{IH}	+2.4		$+V_L$	V
V_{IL}	0		+0.8	V
I_{IH}, V_{IN} = +2.7V			+1.0	µA
I_{IL}, V_{IN} = +0.4V			−50	µA
Input Clock Frequency	10.0			MHz
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error		±2.0		%
Bipolar Zero Error		±30		mV
Differential Linearity Error		±0.001		% of FSR[2]
Noise (rms, 20Hz to 20kHz) at Bipolar Zero (V_{OUT} models)		6		µV
TOTAL HARMONIC DISTORTION				
V_O = ±FS at f = 991Hz: PCM56P-K		0.002	0.0025	%
PCM56P-J		0.002	0.004	%
PCM56P		0.002	0.008	%
V_O = −20dB at f = 991Hz: PCM56P-K		0.018	0.020	%
PCM56P-J		0.018	0.040	%
PCM56P		0.018	0.040	%
V_O = −60dB at f = 991Hz: PCM56P-K		1.8	2.0	%
PCM56P-J		1.8	4.0	%
PCM56P		1.8	4.0	%
MONOTONICITY		15		Bits
DRIFT (0°C to +70°C)				
Total Drift[3]		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)				
Voltage Output: 6V Step		1.5		µs
1LSB		1.0		µs
Slew Rate		12		V/µs
Current Output, 1mA Step: 10Ω to 100Ω load		350		ns
1kΩ load[4]		350		ns
WARM-UP TIME	1			Min
OUTPUT				
Voltage Output Configuration: Bipolar Range		±3.0		V
Output Current	±8.0			mA
Output Impedance		0.10		Ω
Short Circuit Duration	Indefinite to Common			
Current Output Configuration:				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.2		kΩ
POWER SUPPLY REQUIREMENTS[5]				
Voltage: $+V_S$ and $+V_L$	+4.75	+5.00	+13.2	V
$-V_S$ and $-V_L$	−4.75	−5.00	−13.2	V
Supply Drain (No Load): +V ($+V_S$ and $+V_L$ = +5V)		+10.0	+17.0	mA
−V ($-V_S$ and $-V_L$ = −5V)		−25.0	−35.0	mA
+V ($+V_S$ and $+V_L$ = +12V)		+12.0		mA
−V ($-V_S$ and $-V_L$ = −12V)		−27.0		mA
Power Dissipation: V_S and V_L = ±5V		175	260	mW
V_S and V_L = ±12V		468		mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C

NOTES: (1) Logic input levels are TTL/CMOS-compatible. (2) FSR means full-scale range and is equivalent to 6V (±3V) for PCM56 in the V_{OUT} mode. (3) This is the combined drift error due to gain, offset, and linearity over temperature. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) All specifications assume $+V_S$ connected to $+V_L$ and $-V_S$ connected to $-V_L$. If supplies are connected separately, $-V_L$ must not be more negative than $-V_S$ supply voltage to assure proper operation. No similar restriction applies to the value of $+V_L$ with respect to $+V_S$.

MECHANICAL



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragrah 3.2).

CASE: Plastic

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.740	.800	18.80	20.32
A_1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.02	0.05	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

ORDERING INFORMATION

Model	THD at FS (%)
PCM56P	0.008 Max
PCM56P-J	0.004
PCM56P-K	0.0025

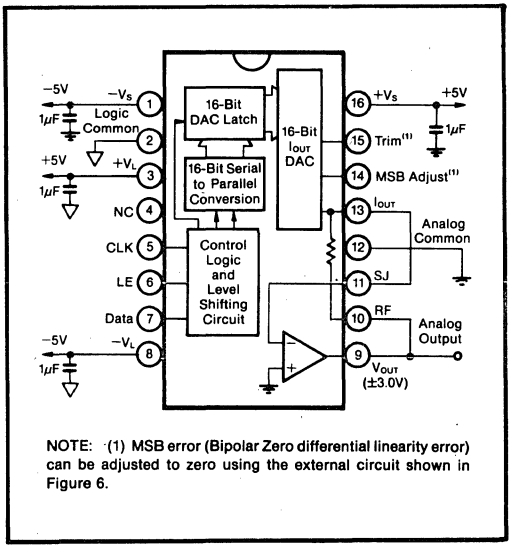
PIN ASSIGNMENTS

1	$-V_S$	Analog Negative Supply
2	LOG COM	Logic Common
3	$+V_L$	Logic Positive Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Supply
9	V_{OUT}	Voltage Output
10	RF	Feedback Resistor
11	SJ	Summing Junction
12	ANA COM	Analog Common
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trim-pot Terminal
16	$+V_S$	Analog Positive Supply

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±16VDC
Input Logic Voltage	$-1V$ to $+V_S/+V_L$
Power Dissipation	850mW
Operating Temperature	−25°C to +70°C
Storage Temperature	−60°C to +100°C
Lead Temperature During Soldering	10s at 300°C

CONNECTION DIAGRAM



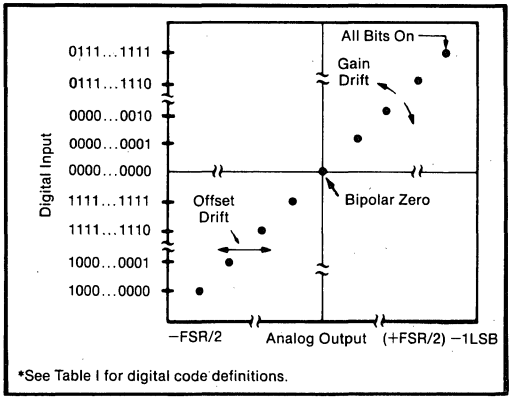
NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 6.

DISCUSSION OF SPECIFICATIONS

The PCM56P is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature, and settling time effects on accuracy.

The PCM56P is factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. Digital input to analog output relationship is shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.



*See Table I for digital code definitions.

FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

TABLE I. Digital Input to Analog Output Relationship.

Digital Input	Analog Output		
Binary Twos Complement (BTC)	DAC Output	Voltage (V), V_{OUT} Mode	Current (mA), I_{OUT} Mode
7FFF Hex	+ Full Scale	+2.999908	−0.999970
8000 Hex	− Full Scale	−3.000000	+1.000000
0000 Hex	Bipolar Zero	0.000000	0.000000
FFFF Hex	Zero − 1LSB	−0.000092	+0.030500µA

DIGITAL INPUT CODES

The PCM56P accepts serial input data (MSB first) in the Binary Twos Complement (BTC) form. Refer to Table I for input/output relationships.

BIPOLAR ZERO ERROR

Initial Bipolar Zero Error (Bit 1 "on" and all other bits "off") is the deviation from 0V out and is factory-trimmed to typically ±30mV at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM56P is factory trimmed to typically ±0.001% of FSR. The MSB DLE is adjustable to zero using the circuit shown in Figure 6.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy.

The PCM56P power supply sensitivity is shown by Figure 2. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

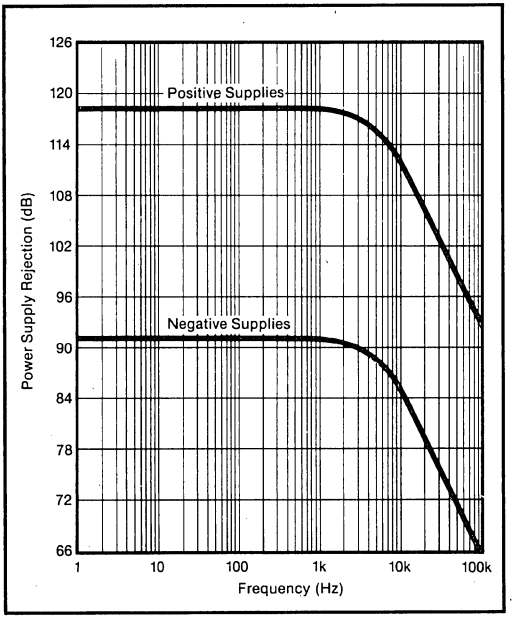


FIGURE 2. Power Supply Sensitivity.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 3).

Settling times are specified to ±0.006% of FSR: one for a large output voltage change of 6V and one for a 1LSB change. The 1LSB change is measured at the major carry (0000 hex to ffff hex), the point at which the worst-case settling time occurs.

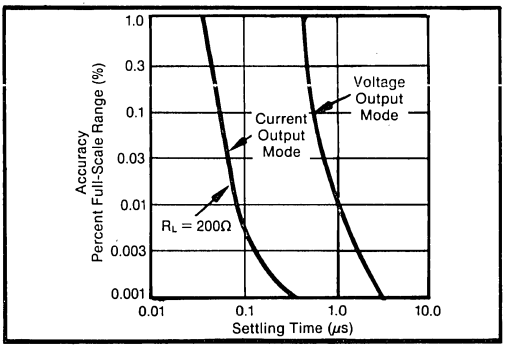


FIGURE 3. Full Scale Range Settling Time vs Accuracy.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM56P is designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM56P was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately $6 \times n$, or about 96dB of a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion.

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error,

Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM56P error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{1/n \sum_{i=1}^{n} [E_L(i) + E_Q(i)]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM56P at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \epsilon_{rms}/E_{rms} \qquad (2)$$

$$= \frac{\sqrt{1/n \sum_{i=1}^{n} [E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\%$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM56P the test period was chosen to be 22.7μs (44.1kHz), which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 991Hz and the amplitude of the input signal is 0dB, −20dB, and −60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

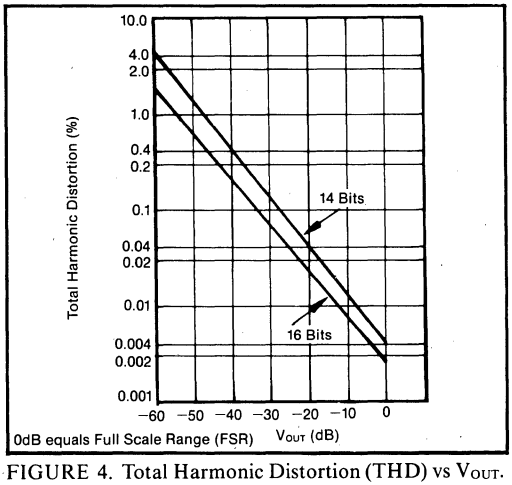


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

Figure 5 shows typical THD as a function of frequency.

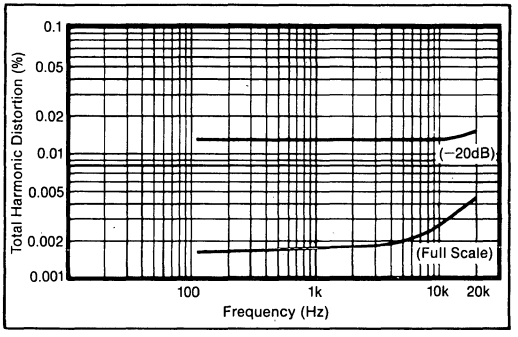


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the converter.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM56P can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

Differential linearity error at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ. Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 6 or the PCM56 connection diagram.

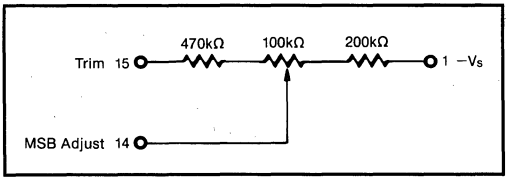


FIGURE 6. MSB Adjustment Circuit.

After allowing ample warm-up time (5–10 minutes) to assure stable operation of the PCM56, select input code FFFF hexadecimal (all bits on except the MSB). Measure the audio output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 0000 hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the audio output read 92μV more than the voltage reading of the previous code (a 1LSB step = 92μV).

A much simpler method is to dynamically adjust the DLE at BPZ. Again, refer to Figure 6 for circuitry and component values. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a −80dB level sinusoidal output. While measuring the THD of the audio circuit output, adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

INPUT TIMING CONSIDERATIONS

Figures 7 and 8 refer to the input timing required to interface the inputs of PCM56P to a serial input data stream. Serial data is accepted in Binary Twos Complement (BTC) with the MSB being loaded first. Data is clocked in on positive going clock (CLK) edges and is latched into the DAC input register on negative going latch enable (LE) edges.

The latch enable input must be high for at least one clock cycle before going low, and then must be held low for at least one clock cycle. The last 16 data bits clocked into the serial input register are the ones that are transferred to the DAC input register when latch enable goes low. In other words, when more than 16 clock cycles occur between a latch enable, only the data present during the last 16 clocks will be transferred to the DAC input register.

One requirement for clocking in all 16 bits is the necessity for a "17th" clock pulse. This automatically occurs when the clock is continuous (last bit shifts in on the first bit of the next data word). When the clock is stopped before the "17th" clock cycle occurs, however, the last serial input shift will not occur (the MSB will be in the bit 2 position). In any application where clock is noncontinuous, attention must be given to providing enough clocks to fully input the data word.

Figure 7 refers to the general input format required for the PCM56P. Figure 8 shows the specific relationships between the various signals and their timing constraints.

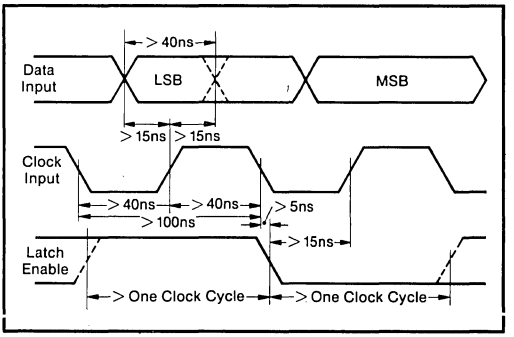
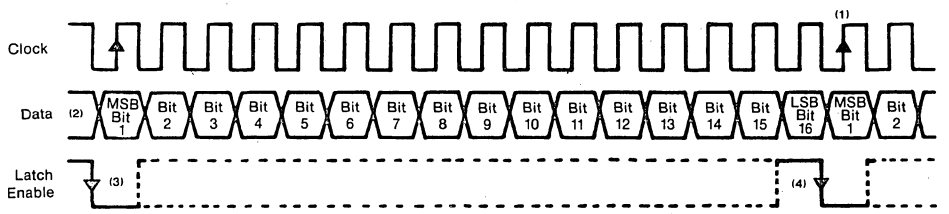


FIGURE 8. Input Timing Relationships.

INSTALLATION CONSIDERATIONS

If the optional external MSB error circuitry is used, a potentiometer with adequate resolution and a TCR of 100ppm/°C or less is required. Also, extra care must be taken to insure that no leakage path (either AC or DC) exists to pin 14. If the circuit is not used, pins 14 and 15 should be left open.

The PCM converter and the wiring to its connectors should be located to provide the optimum isolation from sources of RFI and EMI. The important consideration in the elimination of RF radiation or pickup is loop area;



NOTES: (1) If clock is stopped between input of 16-bit data words, latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 7. Input Timing Diagram.

therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together, they represent a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

Figures 9 and 10 show a circuit and timing diagram for a single PCM56P used to obtain both left- and right-channel output in a typical digital audio system. The audio output of the PCM56P is alternately time-shared between the left and right channels. The design is greatly simplified because the PCM56P is a complete D/A converter requiring no external reference or output op amp.

A sample/hold (S/H) amplifier, or "deglitcher" is required at the output of the D/A for both the left and right channel, as shown in Figure 9. The S/H amplifier for the left channel is composed of A_1, SW_1, and associated circuitry. A_1 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET swtich operate at a virtual ground when "C" and "B" are connected in the sample mode, there is no increase in distortion caused by the modulation effect of R_{ON} by the audio signal.

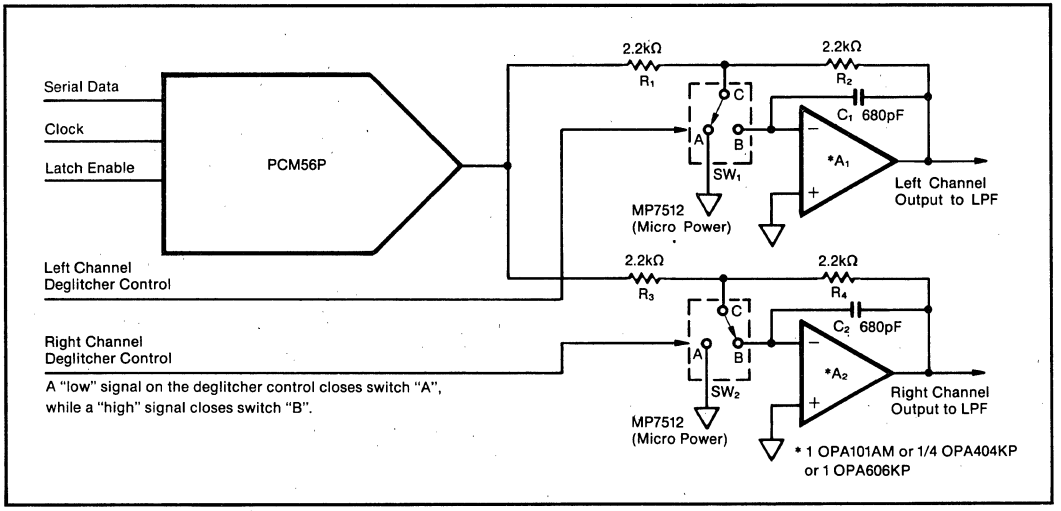


FIGURE 9. A Sample/Hold Amplifier (Deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.

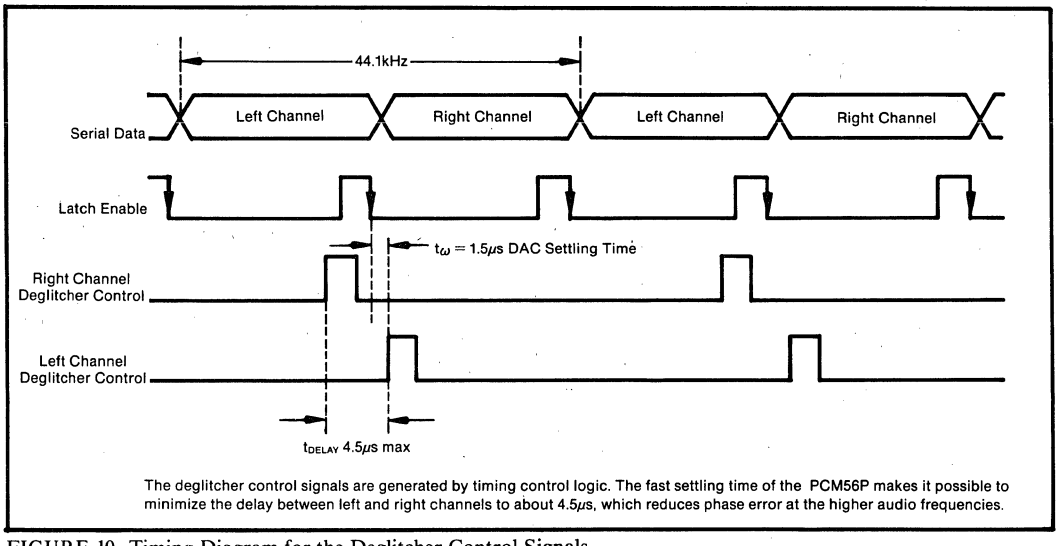


FIGURE 10. Timing Diagram for the Deglitcher Control Signals.

Figure 10 shows the deglitcher controls for both left and right channels which are produced by timing control logic. A delay of 1.5μs ($t\omega$) is provided to allow the output of the PCM56P to settle within a small error band around its final value before connecting it to the channel output. Due to the fast settling time of the PCM56P it is possible to minimize the delay between the left- and right-channel outputs when using a single D/A converter for both channels. This is important because the right- and left-channel data are recorded in-phase and the use of a slower D/A converter would result in significant phase error at higher frequencies.

The obvious solution to the phase shift problem in a two-channel system would be to use two D/A converters (one per channel) and time the outputs to change simultaneously. Figure 11 shows a block diagram of the final test circuitry used for PCM56P. It should be noted that no deglitching circuitry is required on the DAC output to meet specified THD performance. This means that when one PCM56P is used per channel, the need for all the sample/hold and controls circuitry associated with a single DAC (two-channel) design is effectively eliminated. The PCM56P is tested to meet its THD specifications without the need for output deglitching.

A low-pass filter is required after the PCM56P to remove all unwanted frequency components caused by the sampling frequency as well as those resulting from the discrete nature of the D/A output. This filter must have a flat frequency response over the entire audio band (0–20kHz) and a very high attenuation above 20kHz. Most previous digital audio circuits used a higher order (9–13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristic transients contained in music.

SECOND GENERATION SYSTEMS

One method of avoiding the problems associated with a higher order analog filter would be to use digital filter oversampling techniques. Oversampling by a factor of two would move the sampling frequency (88.2kHz) out to a point where only a simple low-order phase-linear analog filter is required after the deglitcher output to remove unwanted intermodulation products. In a digital compact disc application, various VLSI chips perform the functions of error detection/correction, digital filtering, and formatting of the digital information to provide the clock, latch enable, and serial input to the PCM56P. These VLSI chips are available from several sources (Sony, Yamaha, Signetics, etc.) and are specifically optimized for digital audio applications.

Oversampled circuitry requires a very fast D/A converter since the sampling freuqency is multiplied by a factor of two or more (for each output channel). A single PCM56P can provide two-channel oversampling at a 4X rate (176.4kHz/channel) and still remain well within the settling time requirements for maintaining specified THD performance. This would reduce the complexities of the analog filter even further from that used in 2X oversampling circuitry.

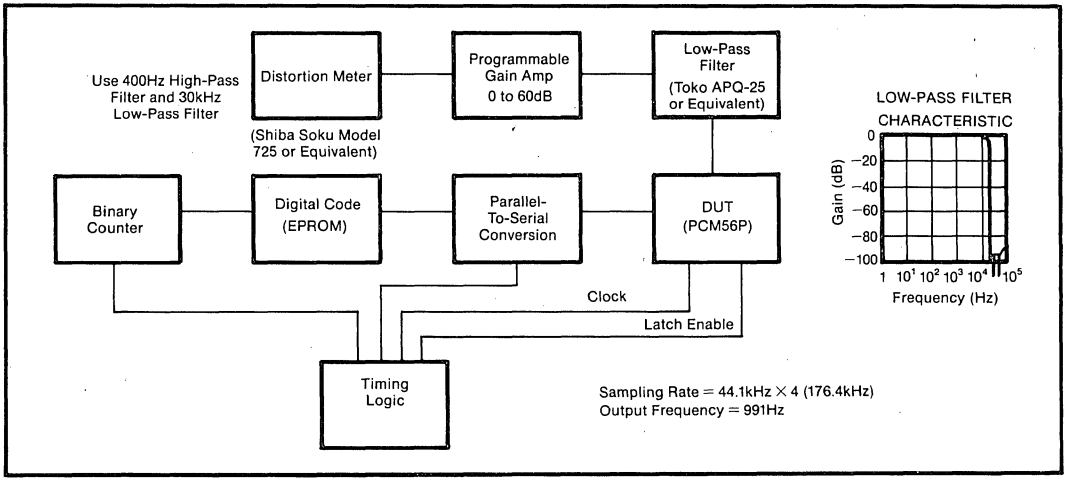


FIGURE 11. Block Diagram of Distortion Test Circuit.

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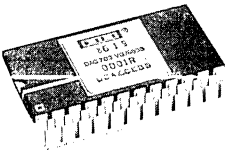
BURR-BROWN®

DAC703/883B SERIES



DAC703VG/883B DAC703VL/883B
DAC703VG DAC703VL

REVISION NONE
APRIL, 1987

Monolithic 16-Bit Military DIGITAL-TO-ANALOG CONVERTER

FEATURES

- FULLY COMPLIANT MIL-STD-883 PROCESSING
- MONOLITHIC CONSTRUCTION
- HIGH ACCURACY:
  Linearity Error ±0.003% of FSR max
  Differential Linearity Error ±0.006% of FSR max
- MONOTONIC (at 14 bits) OVER FULL MILITARY TEMPERATURE RANGE
- PIN-COMPATIBLE WITH DAC72 (COB model)
- DUAL-IN-LINE AND LCC PACKAGES

DESCRIPTION

This is a complete 16-bit bipolar output (±10V) digital-to-analog converter that includes a precision buried-zener voltage reference and a low-noise, fast-settling output operational amplifier, all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the military operating temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range (at +25°C). Differential linearity at +25°C is 0.006% of FSR.

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range.

Two product assurance levels are available: Standard and /883B. The Standard product assurance level offers Hi-Rel manufacturing where many MIL-STD-883 screens are performed routinely. The /883B product assurance level, /883B suffix, offers Hi-Rel manufacturing, 100% screening per MIL-STD-883 method 5004 and 5% PDA. Quality assurance further processes /883B devices, by performing group A and B inspections on each inspection lot and group C and D inspections as required by MIL-STD-883. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
DIGITAL-TO-ANALOG CONVERTER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a 16-bit, voltage output, digital-to-analog converter monolithic microcircuit.

1.2 Part number. The complete part number is as shown below.

DAC703	V	G	/883B
Basic Model Number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel Product Designator (see 1.2.2)

1.2.1 Device type. The device is a single 16-bit bipolar voltage output digital-to-analog converter. The input coding is complementary offset binary (COB). There is one electrical performance grade (V grade). This grade features specifications and testing over the Military temperature range (−55°C to +125°C). Electrical specifications and tests are shown in Tables I and II.

1.2.2 Device class. The device class is similar to the class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

Hi-Rel product designator	Requirements
/883B	Standard model plus 100% MIL-STD-883B class B screening, with 5% PDA, plus Quality Conformance Inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. Two case outlines are available.

1.2.3.1 24-pin ceramic side-brazed (DIP). The "G" package identifier is utilized to specify the 24-pin ceramic side-brazed package, which is MIL-M-38510, Appendix C, designator D-3, configuration 3. Figure 1 depicts the case outline for this package type.

1.2.3.2 28-terminal leadless chip carrier (LCC). The "L" package identifier is utilized to specify the 28-terminal square leadless chip carrier package, which is MIL-M-38510, Appendix C, designator C-4. Figure 1 depicts the case outline for this package type.

1.2.4 Absolute maximum ratings.

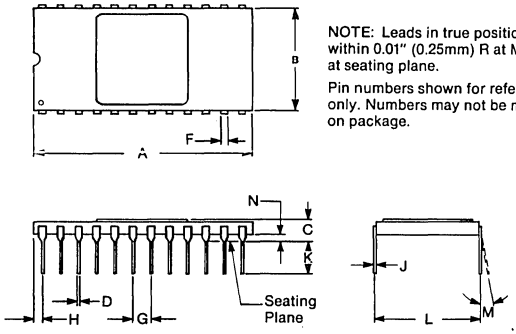
Supply voltage, V_{CC} to common	±18VDC
Supply voltage, V_{DD} to common	0VDC to +18VDC
Digital data input voltage to common	−1VDC to +7VDC
Short circuit duration:	
Reference output to common	Continuous
D/A voltage out to common	Continuous
External voltage applied to D/A output	−5V to +5V
Storage temperature range	−65°C to +165°C
Temperature (soldering 10s)	+300°C
Junction temperature	t_J = +175°C

1.2.5 Recommended operating conditions.

Supply voltage, $\pm V_{CC}$	±15VDC
Supply voltage, $\pm V_{DD}$	+5VDC
Ambient temperature range	−55°C to +125°C

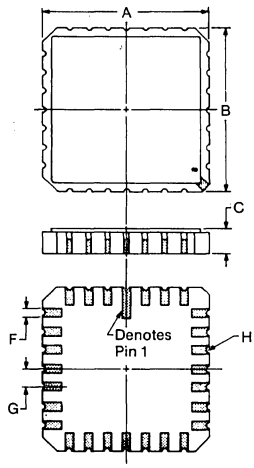
1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θJ-C
24-lead DIP	Figure 1	1000mW	25°C/W
28-terminal LCC	Figure 1	1000mW	48°C/W



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
B	.600	.620	15.24	15.75
C	.125	.171	3.18	4.34
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	2.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

(a) 24-pin side braze; package ID: "G".



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.442	.458	11.23	11.63
B	.442	.458	11.23	11.63
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
H	.008R TYP		0.20R TYP	

(b) 28-terminal LCC; package ID: "L"

FIGURE 1. Case Outlines.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specifications and standards form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510—Microcircuits, general specification for.

STANDARD
MILITARY
MIL-STD-883—Test methods and procedures for microcircuits.

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 General. Burr-Brown used production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

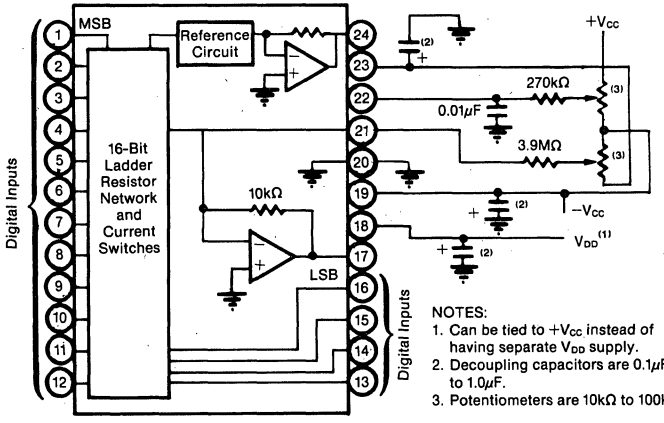
3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein and are shown in Figure 1.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figures 2 and 3.

3.2.8 Glassivation. The microcircuit dice are glassivated.

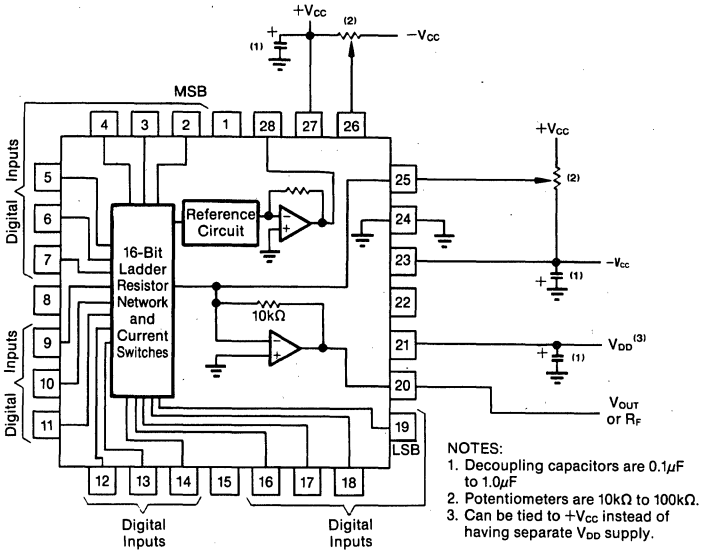
3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

3.4 Electrical test requirements. Electrical test requirements are shown in Table II. The subgroups of Table I, which constitute the minimum electrical test requirements for screening, qualification, and quality conformance inspection, are specified in Table II.



PIN #	"G" PACKAGE
1	Bit 1 (MSB)
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7
8	Bit 8
9	Bit 9
10	Bit 12
11	Bit 11
12	Bit 12
13	Bit 13
14	Bit 14
15	Bit 15
16	Bit 16 (LSB)
17	VOUT
18	VDD
19	−Vcc
20	Common
21	Summing Junction (Zero Adjust)
22	Gain Adjust
23	+Vcc
24	+6.3V Reference Output

FIGURE 2. "G" Package Circuit Diagram and Terminal Connections.



PIN #	"L" PACKAGE
1	No connection
2	Bit 1 (MSB)
3	Bit 2
4	Bit 3
5	Bit 4
6	Bit 5
7	Bit 6
8	No connection
9	Bit 7
10	Bit 8
11	Bit 9
12	Bit 10
13	Bit 11
14	Bit 12
15	No connection
16	Bit 13
17	Bit 14
18	Bit 15
19	Bit 16 (LSB)
20	VOUT
21	VDD
22	No connection
23	−Vcc
24	Common
25	Summing Junction
26	Gain Adjust
27	+Vcc
28	+6.3V Reference Output

FIGURE 3. "L" Package Circuit Diagram and Terminal Connections.

TABLE I. Electrical Performance Characteristics.

(T_A = −55°C to +125°C, Supply Voltages: $\pm V_{CC}$ = ±15VDC, V_{DD} = +5VDC)

CHARACTERISTICS	CONDITIONS	GROUP A SUBGROUPS	DAC703 "V" GRADE MIN	DAC703 "V" GRADE TYP	DAC703 "V" GRADE MAX	UNITS
INPUT						
DIGITAL INPUT						
Resolution 1/					16	Bits
Digital Inputs 2/						
V_{IH}		1	+2.4		$+V_{CC}$	V
V_{IL}		1	−1.0		+0.8	V
I_{IH}	V_I = +2.7V	1			+40	μA
I_{IL}	V_I = +0.4V	1			−0.5	mA
TRANSFER CHARACTERISTICS						
ACCURACY						
Linearity Error	T_A = +25°C	1	−0.003		+0.003	% of FSR 3/
	−55°C ≤ T_A ≤ +125°C	2, 3	−0.006		+0.006	% of FSR
Differential Linearity Error	T_A = +25°C	1	−0.006		+0.006	% of FSR
	−55°C ≤ T_A ≤ +125°C	2, 3	−0.006		+0.009	% of FSR
Gain Error 4/	T_A = +25°C	1	−0.1		+0.1	% of FSR
Zero Error 4/	T_A = +25°C	1	−0.1		+0.1	% of FSR
Monotonicity over Temp. Range 1/		1, 2, 3	14			Bits
DRIFT						
Gain Drift		2, 3	−20		+20	ppm/°C
Zero Drift		2, 3	−15		+15	ppm/°C
Total Error over Temperature			−0.1		+0.1	% of FSR
DYNAMIC CHARACTERISTICS						
Settling Time	to ±0.003%, R_L = 2kΩ Full-Scale Output Step	9		4	8	μs
Slew Rate	R_I = 2kΩ	9	10			V/μs
OUTPUT						
Output Voltage				±10		V
Output Current		1	±5			mA
Output Impedance				0.15		Ω
Reference Voltage		1, 2, 3	+6.0	+6.3	+6.6	V
Source Current	For external loads			+2.5		mA
Temperature Coefficient		1, 2, 3	−15		+15	ppm/°C
POWER SUPPLY REQUIREMENTS						
Suply Voltage, $+V_{CC}$			+13.5	+15	+16.5	V
$-V_{CC}$			−13.5	−15	−16.5	V
V_{DD}			+4.5	+5	+16.5	V
Supply Currents, $-I_{CC}$		1			+30	mA
$-I_{CC}$		1			−30	mA
I_{DD}		1			+8	mA
Power Supply Rejection	Delta $+V_{CC}$ = ±1V T_A = 25°C	1			4	mV/V
	Delta $-V_{CC}$ = ±1V T_A = 25°C	1			4	mV/V
	Delta V_{DD} = ±1V T_A = 25°C	1			4	mV/V

NOTES:

1/ 1LSB = 0.305mV.

2/ Digital Inputs are TTL-, LSTTL-, 54/74C-, 54/74HC-, and 54/74HTC-compatible over the operating voltage range of V_{DD} = +5V to +15V and over the operating temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. As logic "0" and "1" inputs vary over 0V to +0.8V and +2.4V to +10V respectively, the change in the D/A converter output voltage will not exceed ±0.003% of FSR.

3/ FSR = full-scale range = 20V.

4/ Adjustable to zero.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table I)

MIL-STD-883 TEST REQUIREMENTS \ MODELS	DAC703VG/883B DAC703VL/883B	DAC703GL DAC703VL
	Subgroups (see table I)	
Interim electrical parameters (preburn-in) (method 5005)	1	1
Final electrical test parameters (method 5005)	1*, 2, 3	1, 2, 3
Group A test requirements (method 5005)	1, 2, 3	N/A
Group C and D end point electrical parameters (method 5005)	1 and Table III	N/A
Additional electrical subgroups performed in addition to Group C inspection	9**	N/A

**PDA applies to subgroup 1. **Performed to an LTPD of 5.

TABLE III. Additional End-Point Limits (after 1000Hr Life Test).

PARAMETER	LIMIT
Gain Error	±0.2% of FSR*
Linearity Error	±5LSB**
Differential Linearity Error	±8LSB

*FSR = full-scale range. **1LSB = 0.305mV

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum:

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin
f. Electrostatic sensitivity identifier(Δ)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the "/883B" product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the "/883B" product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for the "/833B" Hi-Rel product designation is in accordance with MIL-STD-883B, method 5004, class B, and as specified herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, constant acceleration (condition A), temperature cycle (condition C), and external visual per MIL-STD-883B method 2009.

For the "/883B" product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection (QCI), for the "/883B" product designation, is in accordance with MIL-STD-883, and as specified in paragraph 4.4 herein. The microcircuit inpsection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510. The inspections to be performed are those specified herein for Groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4 herein.).

4.3 Screening. Screening for the "/883B" Hi-Rel product designation is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.
b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B.
   (2) Test circuit is Figure 4.
   (3) $T_A = +125°C$.
   (4) Test duration is 160 hours minimum.

1/A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

c. Percent defective allowable (PDA). The PDA, for "/883B" product designation only, is five percent and includes both parametric and catastrophic failures from Group A, Subgroub 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5005, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of Group A, Subgroup 1, after burn-in are used to determine the Percent Defective for each manufacturing lot, and the lot is accepted or rejected based on PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, class B, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5005, class B are performed as required by MIL-STD-883.

A report of the most recent Group C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, class B.

4.4.3 Group C inspection. Group C inspection consists of the subgroups and LTPD values shown in MIL-STD-883, method 5005, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B.
   (2) Test circuit is Figure 4.
   (3) $T_A = +125°C$ minimum.
   (4) Test duration is 1000 hours minimum.

b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005. End point electrical parameters are specified in Table II herein.

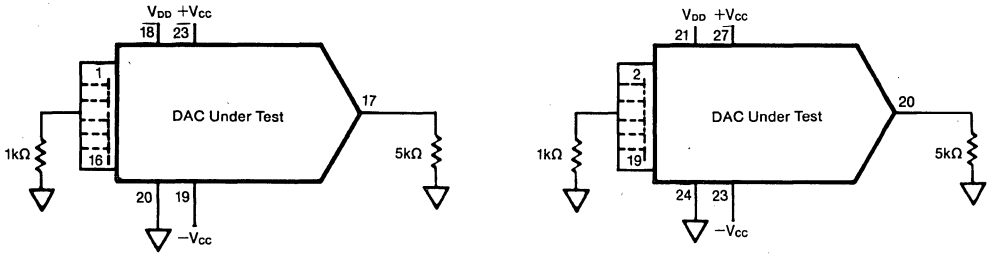
4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.



(a) 24-Pin Side-Brazed "G" Package

(b) 28-Terminal LCC "L" Package

FIGURE 4. Test Circuit for Burn-In and Operating Life Test.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering Data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

6.4 Microcircuit group assignment. These microcircuits are assigned to technology group D with a microcircuit group number of 56 as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. Caution—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

6.6 Definitions.

6.6.1 Linearity. This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

6.6.2 Differential linearity error. Differential linearity error (DLE) of a D/A converter is the deviation from its ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.006%FSR for 14-bit resolution) insures monotonicity.

6.6.3 Monotonicity. Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC703 is specified to be monotonic to 14 bits over the entire specification temperature range.

6.6.4 Gain error. Gain error is the difference between the ideal full-scale output and the actual output of the D/A converter. For the DAC703 this is at 0000H and FFFFH.

6.6.5 Zero error. Zero error is the difference between zero volts and the actual D/A converter output at the zero output code (7FFFH).

7. APPLICATION INFORMATION.

7.1 Power supply decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum or electrolytic capacitors, is used, should be parralleled with 0.01μF ceramic capacitors for best high-frequency performance.

7.2 Power-supply sensitivity. Power-supply sensitivity is specified in Table I. Power-supply sensitivity versus ripple frequency is shown in Figure 5.

7.3 External zero and gain error adjustment. The untrimmed accuracy of the DAC can be adjusted using the circuitry shown in Figures 2 and 3.

7.3.1 Zero adjustment. Apply the digital input code 7FFFH, which should produce zero volts output. Adjust the offset potentiometer until the output is zero volts.

7.3.2 Gain adjustment. Apply the digital input code 0000H, which should produce 9.99969 volts output. Adjust the gain potentiometer to produce 9.99969 volts.

7.4 Further information. Further application information can be found in Burr-Brown's commercial data sheet for the DAC700/702, DAC701/703.

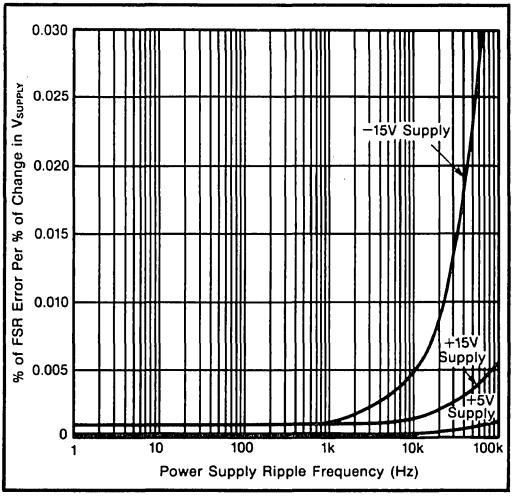
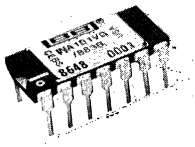


FIGURE 5. Power Supply Rejection Versus Power Supply Ripple Frequency.

BURR-BROWN®

INA101/883B SERIES



INA101VM/883B INA101VG/883B
INA101VM INA101VG

REVISION NONE
APRIL, 1987

Very High Accuracy Military INSTRUMENTATION AMPLIFIER

FEATURES

- FULLY COMPLIANT MIL-STD-883 PROCESSING
- ULTRA-LOW VOLTAGE DRIFT: 1.75μV/°C (A = 1000)
- LOW OFFSET VOLTAGE: 50μV
- LOW NONLINEARITY: 0.005%
- LOW NOISE: 13nV/$\sqrt{Hz}$ at f_o = 1kHz
- HIGH CMR: 106dB at 60Hz
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gauges
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS

DESCRIPTION

The INA101 is a high-accuracy, multistage, military-grade, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very high performance is desired. All circuits, including the interconnected laser-trimmed thin-film resistors, are integrated on a single monolithic substrate.

A multiamplifier design is used to provide the highest performance and maximum versatility with monolithic construction for low cost. The input stage uses Burr-Brown's ultra-low drift, low-noise technology to provide exceptional input characteristics.

Two product assurance levels are available: Standard and /883B. The Standard product assurance level offers Hi-Rel manufacturing where many MIL-STD-883 screens are performed routinely. The /883B product assurace level, /883B suffix, offers Hi-Rel manufacturing, 100% screening per MIL-STD-883 method 5004 and 5% PDA. Quality assurance further processes /883 devices, by performing lot and group C and D inspections as required by MIL-STD-883. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

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DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
INSTRUMENTATION AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a very high accuracy instrumentation amplifier. For description of operation see paragraph 8.

1.2 Part Number. The complete part number is as shown below.

INA101	V	M	/883B
Basic model number	Grade designator (see 1.2.1)	Package designator (see 1.2.3)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single instrumentation amplifier. One electrical performance grade ("V") is provided. The "V" grade offers specifications and operation over the Military temperature range (−55°C to +125°C). Electrical performance characteristics are shown in Table I, and Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the product assurance level B, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level as follows:

Hi-Rel product designator	Requirements
/883B	Standard model, plus 100% MIL-STD-883 class B screening, with 5% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and annually thereafter.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. Two package options are available ("G" and "M").

a. The "G" package is a 14-terminal ceramic side braze DIP and is case outline D-1, configuration 3, as defined in MIL-M-38510, Appendix C (see Figure 1a).

b. The "M" package is a 10-lead can, TO-100, and is case outline D-1 as defined in MIL-M-38510, Appendix C (see Figure 1b).

1.2.4 Absolute maximum ratings.

Positive supply voltage ($+V_{CC}$)	0 to +20VDC
Negative supply voltage ($-V_{CC}$)	0 to −20VDC
Duration output short circuit to ground	Continuous
Lead temperature (soldering, 10s)	+300°C
Junction temperature	+175°C
Storage temperature range	−65°C to +150°C

1.2.5 Recommended operating conditions.

Positive supply voltage ($+V_{CC}$)	+11VDC to +20VDC
Negative supply voltage ($-V_{CC}$)	−11VDC to −20VDC
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{JC}
10-lead TO-100	Figure 1	600mW	60°C/W
14-lead DIP	Figure 1	600mW	50°C/W

2. APPLICABLE DOCUMENTS

2.1 The following form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510—Microcircuits, general specification for.

STANDARD
MILITARY
MIL-STD-883—Test methods and procedures for microcircuits.

TABLE I. Electrical Performance Characteristics.

All characteristics at $-55°C \leq T_A \leq +125°C$, $\pm V_{CC} = 15VDC$, unless otherwise specified.

CHARACTERISTICS	SYMBOL	CONDITIONS	INA101VM/883B INA101VM INA101VG/883B INA101VG MIN	TYP	MAX	UNITS
GAIN						
Range of Gain	A_V	$A_V = 1 + (40k/R_G)$ 1/	1		1000	V/V
Gain Equation Error	E_{AV}	$A_V = 1$, $T_A = +25°C$			0.05	% FS
		$A_V = 10$, $T_A = +25°C$			0.10	% FS
		$A_V = 100$, $T_A = +25°C$			0.10	% FS
		$A_V = 1000$, $T_A = +25°C$			0.40	% FS
Gain Tempco 2/	$\Delta A_V/\Delta T$	$A_V = 1$		2		ppm/°C
		$A_V = 10$		20		ppm/°C
		$A_V = 100$		22		ppm/°C
		$A_V = 1000$		22		ppm/°C
DC Nonlinearity	NL	$A_V = 1$, $T_A = +25°C$			0.005	%
		$A_V = 10$, $T_A = +25°C$			0.005	%
		$A_V = 100$, $T_A = +25°C$			0.007	%
		$A_V = 1000$, $T_A = +25°C$			0.025	%
RATED OUTPUT						
Voltage	V_{OP}	$R_L = 2k\Omega$, $T_A = +25°C$	±10			V
Current	I_O		±5			mA
Impedance	Z_O			0.2		Ω
INPUT OFFSET VOLTAGE						
Initial 3/	V_{IO}	$A_V = 10$, $T_A = +25°C$			±75	μV
	V_{IO}	$A_V = 1000$, $T_A = +25°C$			±50	μV
vs Temperature	$\Delta V_{IO}/\Delta T$	$A_V = 10$, $-55°C \leq T_A \leq +125°C$			±2.5	μV/°C
		$A_V = 1000$, $-55°C \leq T_A \leq +125°C$			±1.75	μV/°C
vs Supply	PSRR	$A_V = 1$, $\Delta V_{CC} = \pm 5VDC$, $T_A = +25°C$			35	μV/V
		$A_V = 1000$, $\Delta V_{CC} = \pm 5VDC$, $T_A = +25°C$			2	μV/V
INPUT BIAS CURRENT						
Initial	I_{IB}	$T_A = +25°C$			±30	nA
Tempco	$\Delta I_{IB}/\Delta T$			±0.2		nA/°C
INPUT OFFSET CURRENT						
Initial	I_{IO}	$T_A = +25°C$			±30	nA
Tempco	$\Delta I_{IO}/\Delta T$			±0.5		nA/°C
INPUT IMPEDANCE						
Differential	Z_{ID}	$T_A = +25°C$		$10^{10}\|\|3$		Ω || pF
Common Mode	Z_{ICM}	$T_A = +25°C$		$10^{10}\|\|3$		Ω || pF
INPUT VOLTAGE						
Linear Response Range	V_{IN}		±10			V
Common-Mode Rejection	CMR	DC-60Hz, $A_V = 1k\Omega$ Source Imbalance				
		$T_A = +25°C$	80			dB
		DC-60Hz, $A_V = 10$, $1k\Omega$ Source Imbalance				
		$T_A = +25°C$	96			dB
		DC-60Hz, $A_V = 100$-1000.				
		$1k\Omega$ Source Imbalance, $T_A = +25°C$	106			dB
INPUT NOISE						
Input Voltage Noise	E_{NPP}	$f_B = 0.01$ to 10Hz, $T_A = +25°C$		0.8		μV, p-p
	E_N	$A_V = 1000$, $f_O = 10Hz$, $T_A = +25°C$		18		nV/√Hz
		$A_V = 1000$, $f_O = 100Hz$, $T_A = +25°C$		15		nV/√Hz
		$A_V = 1000$, $f_O = 1kHz$, $T_A = +25°C$		13		nV/√Hz
Input Current Noise	I_{NPP}	$f_B = 0.01Hz$ to 10Hz, $T_A = +25°C$		50		pA, p-p
	I_N	$f_O = 10Hz$, $T_A = +25°C$		0.8		pA/√Hz
		$f_O = 100Hz$, $T_A = +25°C$		0.46		pA/√Hz
		$f_O = 1kHz$, $T_A = +25°C$		0.35		pA/√Hz
DYNAMIC RESPONSE						
Slew Rate	SR	$A_V = 1$ to 100, $R_L = 2k\Omega$, $T_A = +25°C$	0.2			V/μs
Bandwidth	BW	3dB small signal, $A_V = 1$, $T_A = +25°C$		300		kHz
		$A_V = 10$, $T_A = +25°C$		140		kHz
		$A_V = 100$, $T_A = +25°C$		25		kHz
		$A_V = 1000$, $T_A = +25°C$		2.5		kHz
	BW	Full power $A_V = 1$ to 1000, $T_A = +25°C$		6.4		kHz
Settling Time	T_S	0.01%, $A_V = 1$, $T_A = +25°C$		30		μs
		$A_V = 100$, $T_A = +25°C$		50		μs
		$A_V = 1000$, $T_A = +25°C$		500		μs
POWER SUPPLY						
Rated Voltage	$\pm V_{CC}$		±5	±15	±20	V
Quiescent Current	I_O	$T_A = +25°C$			±8.5	mA

NOTES:
1/ Typically the tolerance of R_G will be the major source of gain error.
2/ Not including TCR of R_G.
3/ Adjustable to zero at any one gain.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883 REQUIREMENTS (Class B)	INA101VM/883B INA101VG/883B	INA101VM INA101VG
Interim electrical parameters (preburn-in) (method 5004)	1	
Final electrical test parameters (method 5004)	1*, 2, 3, 4	1, 2, 3, 4
Group A test requirements (method 5005)	1, 2, 3, 4	—
Group C and D end point electrical parameters (method 5005)	1	—

*PDA applies to subgroup 1 (see 4.3.c).

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS ($\pm V_{CC}$ = 15VDC unless otherwise specified)	LIMITS INA101VM/883B INA101VM INA101VG/883B INA101VG MIN	LIMITS MAX	UNITS
1 T_A = 25°C	V_{IO}	4001	A_V = 10		±75	µV
			A_V = 1000		±50	µV
	I_{IB}	4001			±20	nA
	I_{IO}	4001			±20	nA
	I_Q	4005			±6.5	mA
	PSRR	4003	A_V = 1, ΔV_{CC} = ±5VDC		±35	µV/V
			A_V = 1000, ΔV_{CC} = ±5VDC		±2	µV/V
	CMR	4003	DC, A_V = 1, 1kΩ Source Imbalance	80		dB
			DC, A_V = 10, 1kΩ Source Imbalance	96		dB
			DC, A_V = 100-1000, 1kΩ Source Imbalance	106		dB
2 T_A = 125°C	$\Delta V_{IO}/\Delta T$	4001	A_V = 10 [V_{IO} (125°C) − V_{IO} (25°C)] ÷ 100		±2.5	µV/°C
			A_V = 1000 [V_{IO} (125°C) − V_{IO} (25°C)] ÷ 100		±1.75	µV/°C
3 T_A = −55°C	$\Delta V_{IO}/\Delta T$	4001	A_V = 10 [V_{IO} (25°C) − V_{IO} (−55°C)] ÷ 80		±25	µV/°C
			A_V = 1000 [V_{IO} (25°C) − V_{IO} (−55°C)] ÷ 80		±1.75	µV/°C
4 T_A = 25°C	E_{AV}		Gain Equation Error: A_V = 1		0.05	%FS
			A_V = 10		0.10	%FS
			A_V = 100		0.10	%FS
			A_V = 1000		0.40	%FS
	V_{OP}	4004	R_L = 2kΩ	±10		V
	SR		R_L = 2kΩ	0.2		V/µs
	NL 1/	Figure 4	A_V = 1		0.005	%
			A_V = 10		0.005	%
			A_V = 100		0.007	%
			A_V = 1000		0.025	%

NOTES:

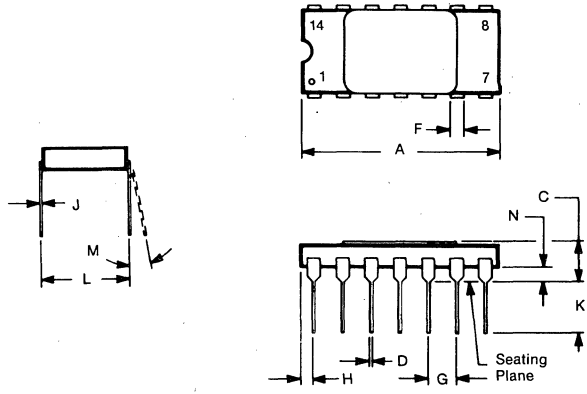
1/ E_1 = 0V and E_2 is varied to enable nonlinearity error to be measured by sampling 21 points between $-10V \leq E_{OUT} \leq +10V$ and determining worst case deviation from straight line connecting these end points at each gain setting.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

(a) 14-Pin Ceramic Side Braze—Package ID: "G"



NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

(b) TO-100 Metal Can—Package ID: "M"

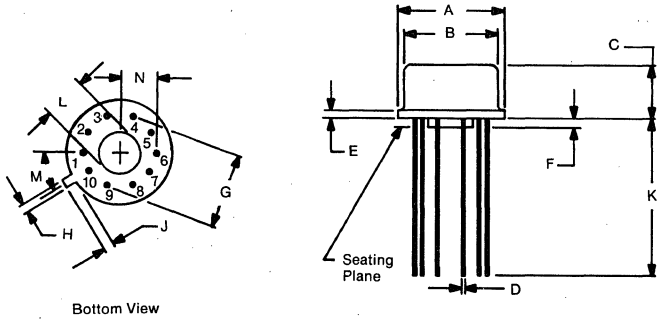


FIGURE 1. Case Outlines.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction and physical dimensions.

3.2.1 Package, metals, and other materials. The package, metal surfaces, and other materials are in accordance with MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

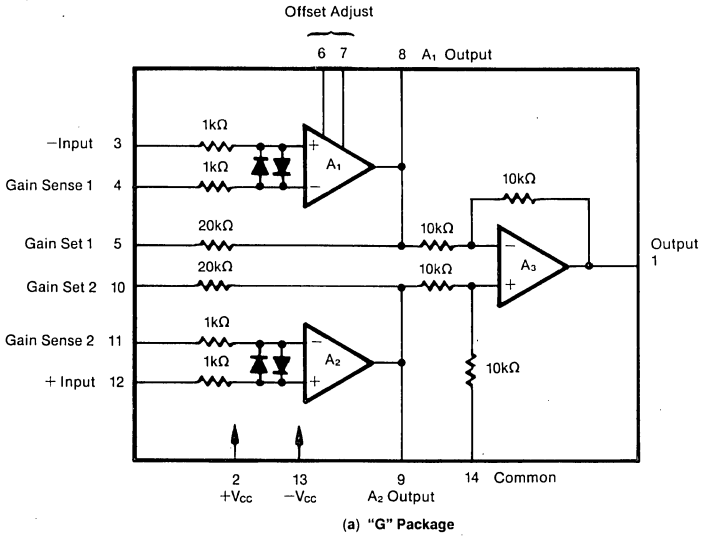
3.2.3. Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4. Lead material and finish. The lead material and finish (gold plate) are in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

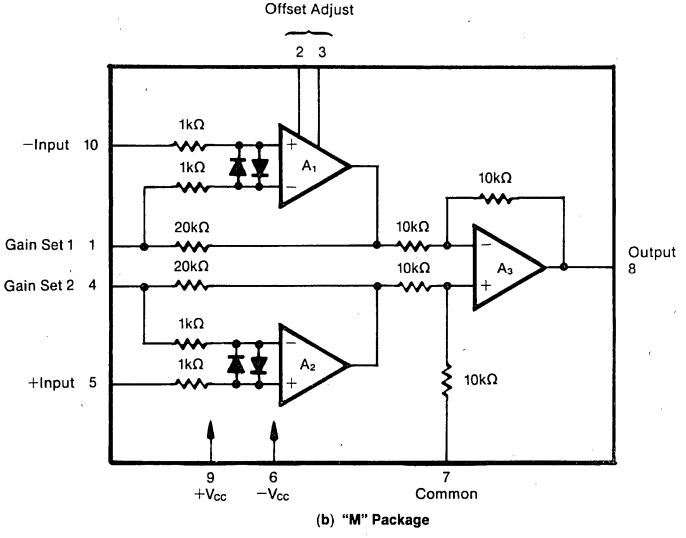
3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.



(a) "G" Package



(b) "M" Package

FIGURE 2. Circuit Diagram and Terminal Connections.

3.2.8 Glassivation. The microcircuit die is glassivated.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

3.4 Electrical test requirements. Electrical test requirements are shown in Table II. The subgroups of Table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.

3.5 Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum:

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin
f. Electrostatic sensitivity identifier(Δ)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures, and training prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1. Rework provisions. Rework provisions, including rebonding for the "/883B" Hi-Rel product designation are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the "/883B" Hi-Rel product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality, or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening.

a. Screening for the "/883B" Hi-Rel product designation is in accordance with MIL-STD-883, method 5004, class B, except as modified in paragraph 4.3 herein. All microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.
b. Screening for the standard model (no Hi-Rel product designation) includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, constant acceleration (condition E), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the "/883B" Hi-Rel product designation is in accordance with MIL-STD-883 and MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

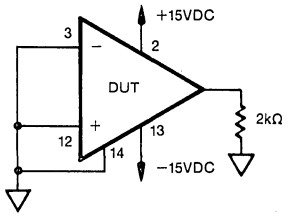
4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for Groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4). Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

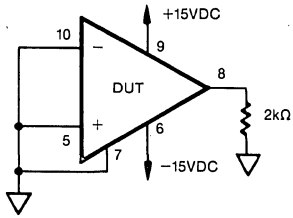
4.3 Screening. Screening for the "/883B" Hi-Rel product designation is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.
b. Burn-In test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B.
   (2) Test circuit is shown in Figure 3.
   (3) $T_A = +125°C$ minimum.
   (4) Test duration 160 hours minimum.
c. Percent defective allowable (PDA). The PDA, for the "/883B" Hi-Rel product designation only, is 5% based on failures from Group A, subgroup 1 test after cool-down as final electrical in accordance with MIL-STD-883, method 5004, and with no intervening electrical measurements. If interim electrical parameter tests performed prior to burn-in are omitted, all screening failures shall be included in the PDA calculation. The verified failures of group A, subgroup 1 after burn-in for each manufacturing lot are used to determine the percent defective for that lot. Each lot is accepted or rejected based on the PDA.
d. External visual inspection does not include measurement of case and lead dimensions.

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.



(a) "G" Package



(b) "M" Package

FIGURE 3. Test Circuit—Burn-In and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspection of MIL-STD-883, method 5005, class B, are performed on each inspection lot. Group C and D inspections of MIL-STD-883, method 5005, class B are performed as required by MIL-STD-883. A report of the most recent group C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B.
   (2) Test circuit is shown in Figure 3.
   (3) $T_A = +125°C$ minimum.
   (4) Test duration is 1000 hours minimum.
b. End point electrical parameters are specified in Table II.

4.4.4 Group D. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, end point electrical parameters.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering Data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

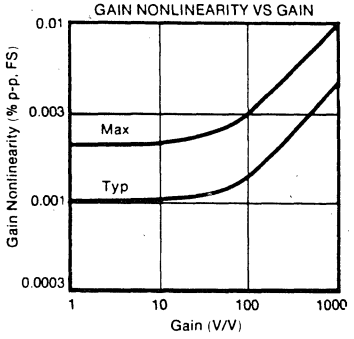
6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group D as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

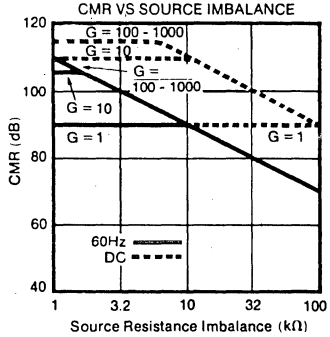
7.0 ELECTRICAL PERFORMANCE CURVES

(Typical at +25°C unless otherwise specified.)

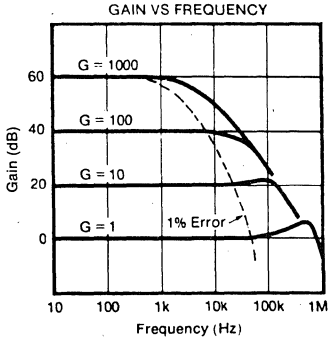
GAIN NONLINEARITY VS GAIN



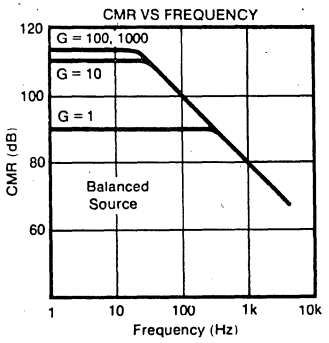
CMR VS SOURCE IMBALANCE



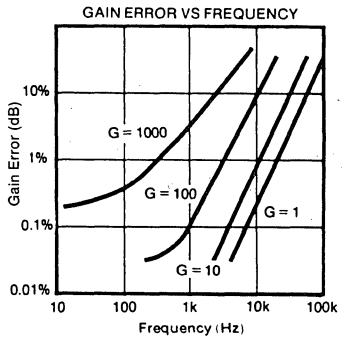
GAIN VS FREQUENCY



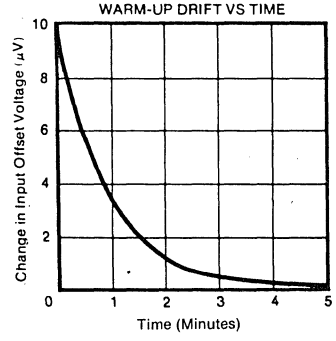
CMR VS FREQUENCY



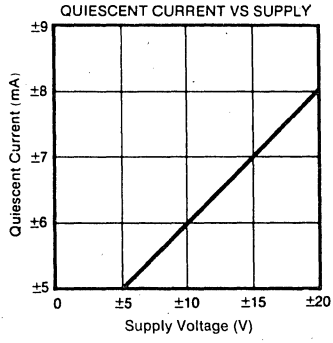
GAIN ERROR VS FREQUENCY



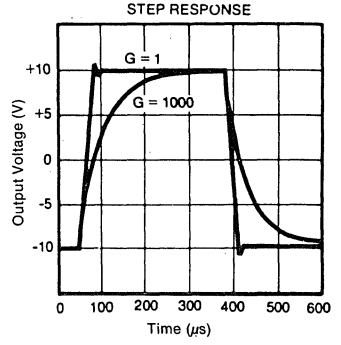
WARM-UP DRIFT VS TIME



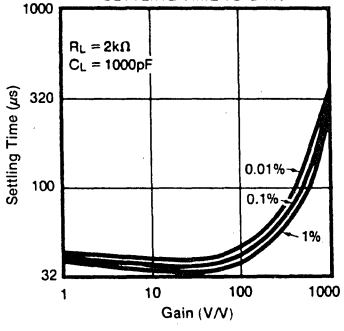
QUIESCENT CURRENT VS SUPPLY



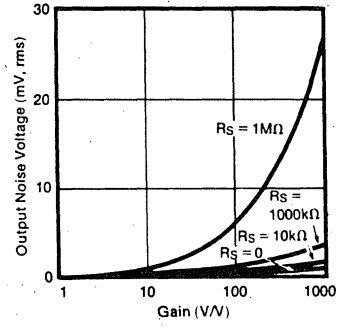
STEP RESPONSE



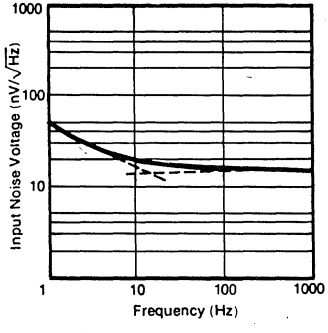
SETTLING TIME VS GAIN



OUTPUT NOISE VS GAIN



INPUT NOISE VOLTAGE VS FREQUENCY (100 ≤ GAIN ≤ 1000)



8. APPLICATION INFORMATION

8.1 Description. The INA101 is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers. See simplified schematics in Figure 2.

The input section (A_1 and A_2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature are low due to the monolithic design, and are improved even further by state-of-the-art laser-trimming techniques.

The output section (A_3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection.

8.2 Using the INA101. Figure 4 shows the simplest configuration of the INA101. The gain is set by the external resistor, R_G, with a gain equation of $G = 1 + (40k/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

8.3 Typical applications. Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gauges, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA101 accomplishes all these with high precision.

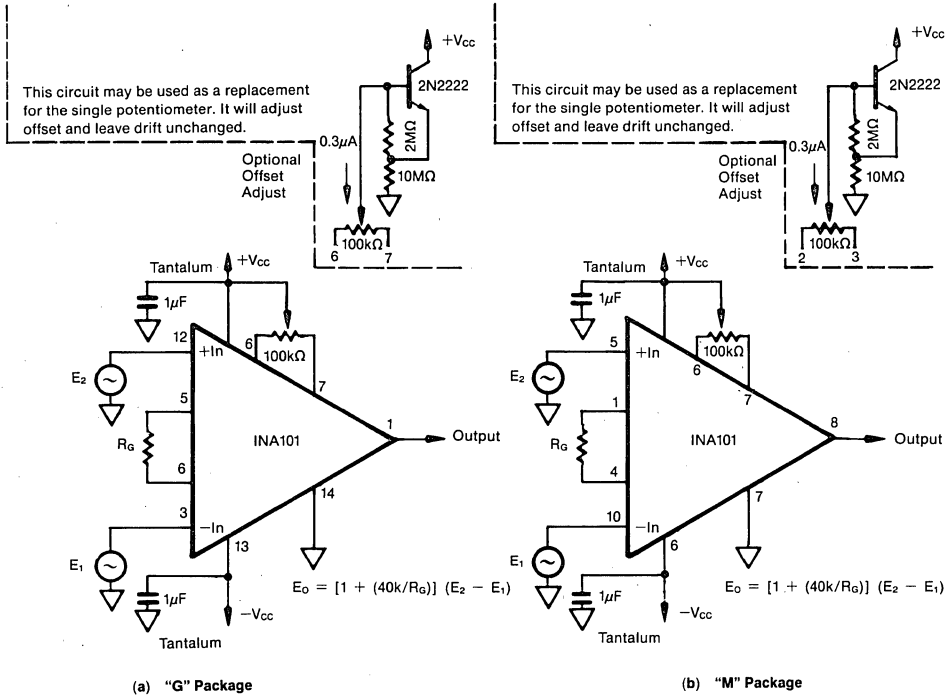
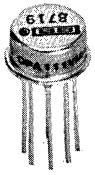


FIGURE 4. Basic Circuit Configuration.

BURR-BROWN®

OPA111/883B SERIES



OPA111VM/883B OPA111VM

REVISION NONE
APRIL, 1987

Low Noise Precision *Difet*® Military OPERATIONAL AMPLIFIER

FEATURES

- FULLY COMPLIANT MIL-STD-883 PROCESSING
- LOW NOISE: 100% tested, 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW BIAS CURRENT: 2pA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 10μV/°C max
- HIGH OPEN-LOOP GAIN: 114dB min
- HIGH COMMON-MODE REJECTION: 90dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- OPTOELECTRONICS
- RADIATION-HARD EQUIPMENT

DESCRIPTION

The OPA111/883B is a precision monolithic dielectrically-isolated FET (*Difet*) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications. The /883B versions are fully compliant to the requirements of MIL-STD-883.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.

Difet® Burr-Brown Corp., BIFET® National Semiconductor Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
LOW NOISE PRECISION *Difet*® OPERATIONAL AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a precision low noise dielectrically-isolated (*Difet*) operational amplifier

1.2 Part Number. The complete part number is as shown below.

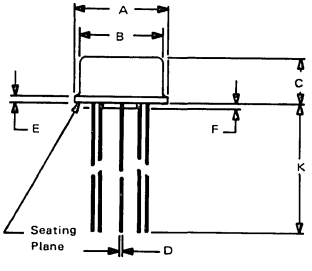
OPA111	V	M	/883B
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.2)

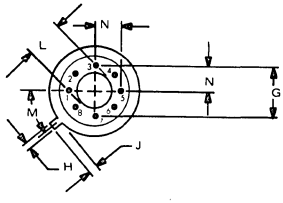
1.2.1 Device type. The device is a single precision dielectrically-isolated (*Difet*) low noise operational amplifier. One electrical performance grade (V) is provided. The V grade offers specifications and operation over the "MIL" temperature range (−55°C to +125°C). Electrical specifications are shown in Table I, and electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level as follows:

Hi-Rel product designator	Requirements
/883B	Standard model, plus 100% MIL-STD-883 class B screening, with 5% PDA, plus quality conformance inspection (QCI) consisting of groups A and B performed on each inspection lot, plus groups C and D performed as required by MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is A-1 (8-lead, TO-99) as defined in MIL-M-38510, Appendix C and is shown in Figure 1. The case is metal and is conductive.





NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 1. Case Outline (TO-99) Package Configuration.

1.2.4 Absolute maximum ratings:

Supply voltage $+V_{CC}$	±18VDC
Input voltage range	±18VDC 1/
Differential input voltage	±36VDC 1/
Internal power dissipation	500mW
Output short circuit duration	continuous to power supply common only
Storage temperature range	−65°C to +165°C
Temperature (soldering 10s)	+300°C
Junction temperature	T_J = +175°C

1.2.5 Recommended operating conditions.

Supply voltage	±15VDC
Ambient temperature range	−55°C to +125°C

1/ For supply voltages less than ±18VDC the absolute maximum input voltage is equal to $+18V > V_{IN} > -V_{CC} - 6V$.

1.2.6 Power and thermal characteristics

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{JC}
8-lead can	Figure 1	500mW	60°C/W

2. APPLICABLE DOCUMENTS

2.1 The following form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510—Microcircuits, general specification for.

STANDARD
MILITARY
MIL-STD-883—Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to ensure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction and physical dimensions.

3.2.1 Package, metals, and other materials. The package, metal surfaces, and other materials are in accordance with MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3. Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4. Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein and are shown in Figure 1.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

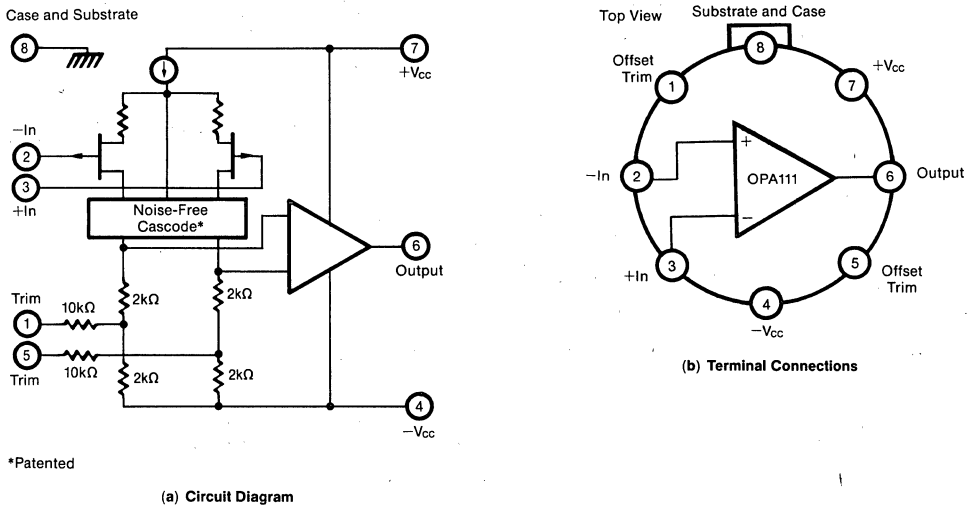


FIGURE 2. Circuit Diagram and Terminal Connections.

3.2.8 Glassivation. The microcircuit dice are glassivated.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

TABLE I. Electrical Performance Characteristics.

All characteristics at $-55°C \le T_A \le +125°C$, $\pm V_{CC}$ = 15VDC, pin 8 connected to ground unless otherwise specified.

CHARACTERISTICS	SYMBOL	CONDITIONS 1/		OPA111VM/883B OPA111VM MIN	TYP	MAX	UNITS
GAIN							
Open-Loop Voltage Gain	A_{VS}	R_L = 2kΩ, V_O = ±10V, F = 0Hz	T_A = +25°C	114			dB
			−55°C ≤ T_A ≤ +125°C	110			dB
RATED OUTPUT							
Voltage	V_{OP}	R_L = 2kΩ		±10			V
Current	I_O			±5			mA
Output Resistance	R_O	DC, Open Loop	T_A = +25°C		100		Ω
Load Capacitance Stability	C_L	Gain = +1	T_A = +25°C		1000		pF
Short Circuit Current	I_{OS}	To Ground		±10			mA
DYNAMIC RESPONSE							
Bandwidth	BW	Unity Gain-Small Signal	T_A = +25°C		2		MHz
Bandwidth	BW	Full Power	T_A = +25°C	16			kHz
Slew Rate	SR	R_L = 2kΩ, V_O = ±10V	T_A = +25°C	1			V/µs
Settling Time (0.1%)	T_S	G = −1, R_L = 2kΩ, 10V step	T_A = +25°C		6		µs
Settling Time (0.01%)	T_S	G = −1, R_L = 2kΩ, 10V step	T_A = +25°C		10		µs
Overload Recovery 2/	T_R	Gain = −1	T_A = +25°C		5		µs
INPUT OFFSET VOLTAGE 3/							
Initial Offset	V_{IO}	V_{CM} = 0VDC	T_A = +25°C	−500		+500	µV
Temperature Sensitivity	DV_{IO}	$\frac{V_{IO}(T_A) - V_{IO}(+25°C)}{\Delta T}$	−55 ≤ T_A ≤ +125°C	−10		+10	µV/°C
vs Power Supply	PSRR	V_{CC} = ±10V_{CC} = ±18VDC	T_A = +25°C	−31		+31	µV/V
			−55 ≤ T_A ≤ +125°C	−50		+50	µV/V
INPUT BIAS CURRENT 3/							
Initial Bias	I_{IB}	V_{CM} = 0	T_A = +25°C	−2		+2	pA
vs Supply Voltage			−55°C ≤ T_A ≤ +125°C	−4100		+4100	pA
INPUT OFFSET CURRENT 3/							
Initial Offset	I_{IO}	V_{CM} = 0	T_A = +25°C	−1.5		+1.5	pA
			−55°C ≤ T_A ≤ +125°C	−3100		+3100	pA
INPUT IMPEDANCE							
Differential	Z_{ID}		T_A = +25°C	10^{13} || 1			Ω || pF
Common-Mode	Z_{ICM}		T_A = +25°C	10^{14} || 3			Ω || pF
INPUT NOISE							
Voltage	e_N	f_O = 10Hz	T_A = +25°C			80	nV/√Hz
		f_O = 100Hz	T_A = +25°C			40	nV/√Hz
		f_O = 1kHz	T_A = +25°C			1.5	nV/√Hz
		f_O = 10kHz	T_A = +25°C			8	nV/√Hz
		f_B = 10Hz to 10kHz	T_A = +25°C			1.2	µVrms
Current	i_N	f_B = 0.1Hz to 10Hz	T_A = +25°C		7.5		fA, p-p
		f_O = 0.1Hz thru 20kHz	T_A = +25°C		0.4		fA/√Hz
INPUT VOLTAGE RANGE							
Common-Mode	V_{ICM}		T_A = +25°C	±10			V
Common-Mode Rejection	CMRR	V_{IN} = ±10V	T_A = +25°C	90			dB
			−55°C ≤ T_A ≤ +125°C	86			dB
POWER SUPPLY							
Rated Voltage	V_{CC}				±15		VDC
Voltage Range				±5		±18	VDC
Quiescent Current	I_Q					±3.5	mA
TEMPERATURE RANGE (ambient)							
Operating				−55		+125	°C
Storage				−65		+150	°C

1/ Optimum device performance is characterized in a reduced ambient light environment.

2/ Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.

3/ Offset voltage, offset current, and bias current are measured with units fully warmed up.

3.4 Electrical test requirements. Electrical test requirements are shown in Table II. The subgroups of Table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance inspection, are specified in Table II.

TABLE II. Electrical Test Requirements.

The individual tests within the subgroups appear in Table III.

MIL-STD-883 REQUIREMENTS	MODELS	
	OPA111VM/883B	OPA111VM
Interim electrical parameters (pre burn-in, method 5004)	1*	1
Final electrical test parameters (method 5004)	1, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 7	—
Group C and D end point electrical parameters (method 5005)	1	—

*PDA applies to subgroup 1 (see 4.3d).

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC} = \pm 15VDC$ unless otherwise specified	LIMITS OPA111VM/883B OPA111VM MIN	LIMITS OPA111VM/883B OPA111VM MAX	UNITS
1	V_{IO}	4001	$V_{CM} = 0VDC$	−500	+500	μV
$T_A = +25°C$	I_{IB}	4001		−2	+2	pA
	I_{IO}	4001		−1.5	+1.5	pA
	PSRR		$V_{CC} = \pm 10VDC$ to $\pm 18VDC$	−31	+31	μV/V
	CMRR	4003	$V_{IN} = \pm 10V$	90		dB
	$\pm I_{CC}$		$I_O = 0mA$		±3.5	mA
	I_{OS}			±10		mA
2	DV_{IO}	4001	$V_{CM} = 0VDC$	−10	+10	μV/°C
$T_A = +125°C$	I_{IB}	4001		−4100	+4100	pA
	I_{IO}	4001		−3100	+3100	pA
	PSRR		$V_{CC} = \pm 10VDC$ to $\pm 18VDC$	−50	+50	μV/V
	CMRR	4003	$V_{IN} = \pm 10V$	86		dB
	$\pm I_{CC}$		$I_O = 0mA$		±3.5	mA
	I_{OS}			±10		mA
3	DV_{IO}	4001	$V_{CM} = 0VDC$	−10	+10	μV/°C
$T_A = -55°C$	I_{IB}	4001		−4100	+4100	pA
	I_{IO}	4001		−3100	+3100	pA
	PSRR		$V_{CC} = \pm 10VDC$ to $\pm 18VDC$		±50	μV/V
	CMRR	4003	$V_{IN} = \pm 10V$	86		dB
	$\pm I_{CC}$		$I_O = 0mA$		±3.5	mA
	I_{OS}			±10		mA
4	$\pm V_{OP}$		$R_L = 2k\Omega$		±10	V
$T_A = +25°C$	A_{VS}	4004	$R_L \geq 2k\Omega$	114		dB
5	$\pm V_{OP}$		$R_L = 2k\Omega$		±10	V
$T_A = +125°C$	A_{VS}	4004	$R_L \geq 2k\Omega$	110		dB
6	$\pm V_{OP}$		$R_L = 2k\Omega$		+10	V
$T_A = -55°C$	A_{VS}	4004	$R_L \geq 2k\Omega$	110		dB
7	SR	4002	$V_O = \pm 10V$, $R_L = 2k\Omega$	1		V/μs
$T_A = +25°C$	e_N		$f_O = 10Hz$		80	$nV/\sqrt{Hz}$
			$f_O = 100Hz$		40	$nV/\sqrt{Hz}$
			$f_O = 1kHz$		15	$nV/\sqrt{Hz}$
			$f_O = 10kHz$		8	$nV/\sqrt{Hz}$
			$f_B = 10Hz$ to 10kHz		1.2	μVrms
	BW_{FP}			16		kHz

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum:

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

d. Manufacturer's designating symbol (CEBS)
e. Country of origin
f. Electrostatic sensitivity identifier (Δ)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the "/883B" product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the "/883B" product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality, or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for the "/883B" Hi-Rel product designation is in accordance with MIL-STD-883, method 5004, class B, except as modified herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, constant acceleration (condition A), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

For the "/883B" product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the "/883B" product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspections as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the "/883B" Hi-Rel product designation is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.
b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B.
   (2) Test circuit is Figure 3.
   (3) $T_A = +125°C$ minimum.
   (4) Test duration is 160 hours minimum.
c. Percent defective allowable (PDA). The PDA, for "/883B" product designation only, is five percent and includes both parametric and catastrophic failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5005, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on PDA.
d. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, class B, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5005, class B are performed as required by MIL-STD-883.

A report of the most recent group C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, class B.

4.4.3 Group C inspection. Group C inspection consists of the subgroups and LTPD values shown in MIL-STD-883, method 1005, class B, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B.
   (b) Test circuit is Figure 3.
   (3) $T_A = +125°C$ minimum.
   (4) Test duration is 1000 hours minimum.

b. End point electrical parameters are specified in Table II herein.

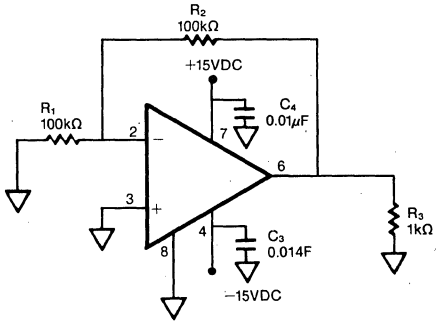


FIGURE 3. Test Circuit, Burn-In and Operating Life Test.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

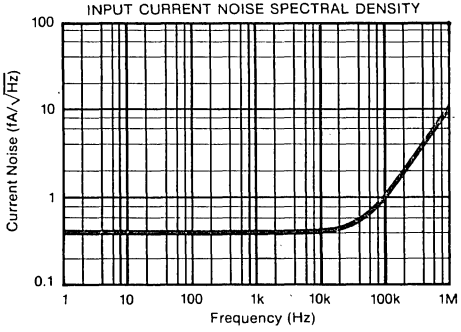
6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group E with a microcircuit group number of 61 as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

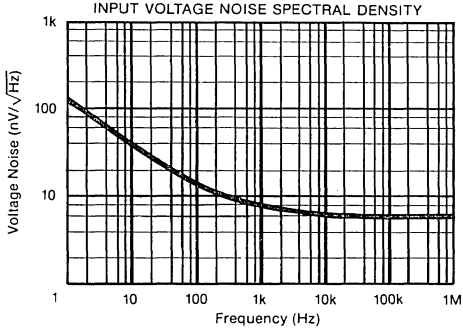
7. ELECTRICAL PERFORMANCE CURVES.

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

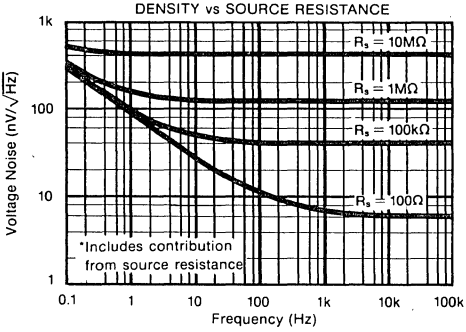
INPUT CURRENT NOISE SPECTRAL DENSITY



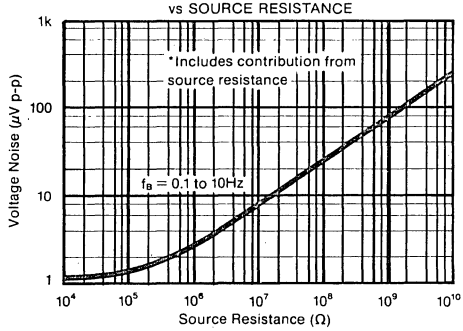
INPUT VOLTAGE NOISE SPECTRAL DENSITY



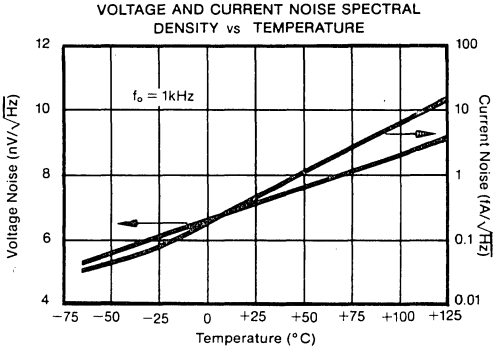
TOTAL* INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



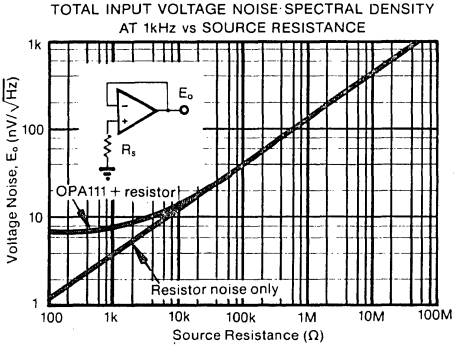
TOTAL* INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



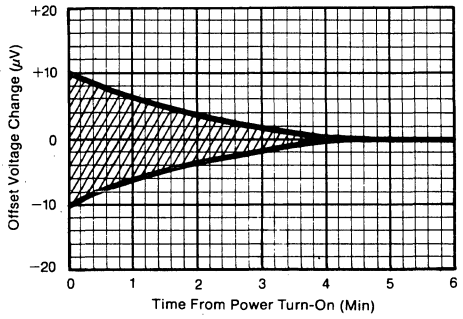
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



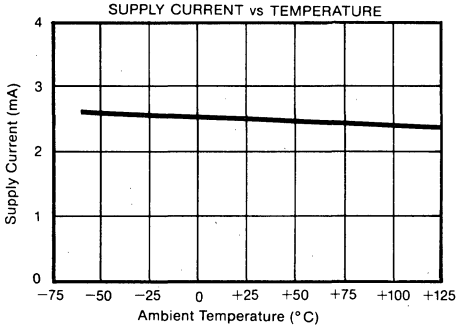
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



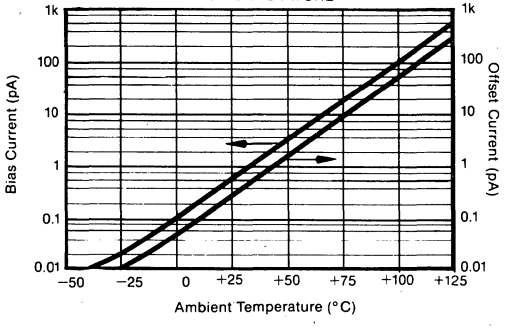
INPUT OFFSET VOLTAGE WARM-UP DRIFT



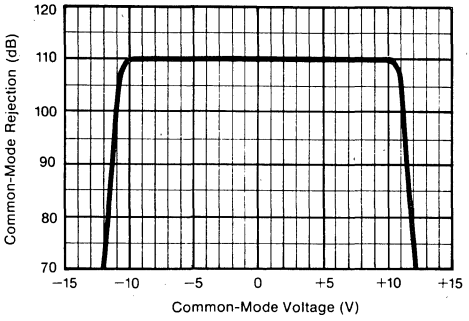
SUPPLY CURRENT vs TEMPERATURE



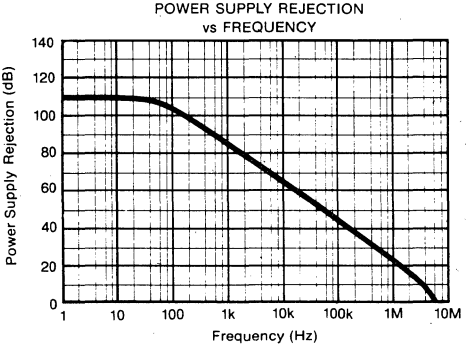
BIAS AND OFFSET CURRENT
vs TEMPERATURE



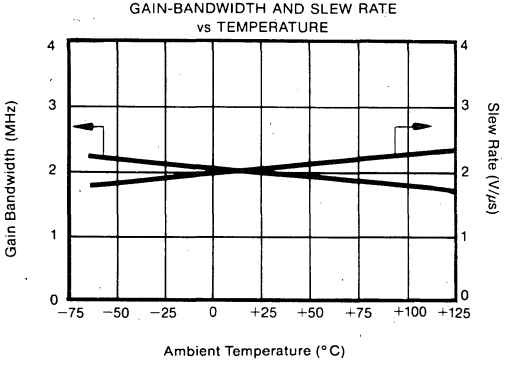
COMMON-MODE REJECTION
vs INPUT COMMON MODE VOLTAGE



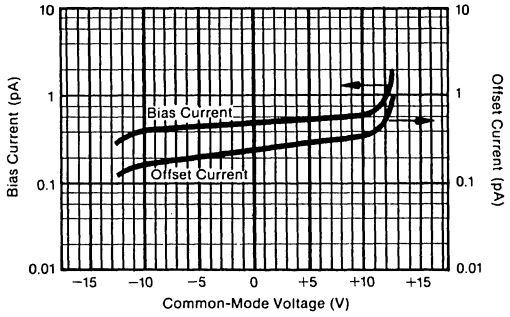
POWER SUPPLY REJECTION
vs FREQUENCY



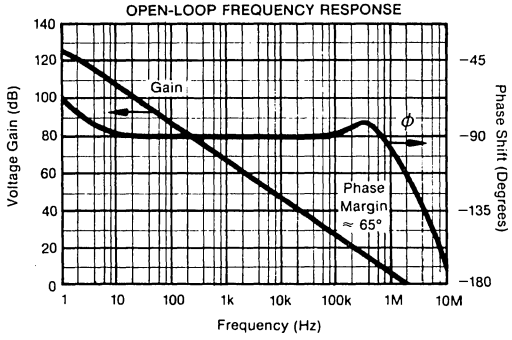
GAIN-BANDWIDTH AND SLEW RATE
vs TEMPERATURE



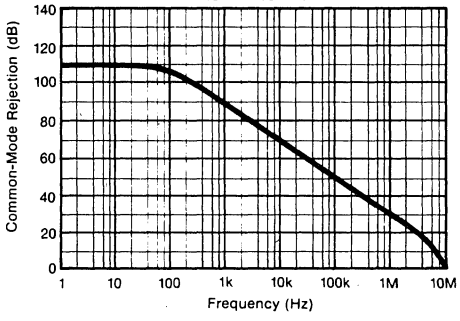
BIAS AND OFFSET CURRENT
vs INPUT COMMON MODE VOLTAGE



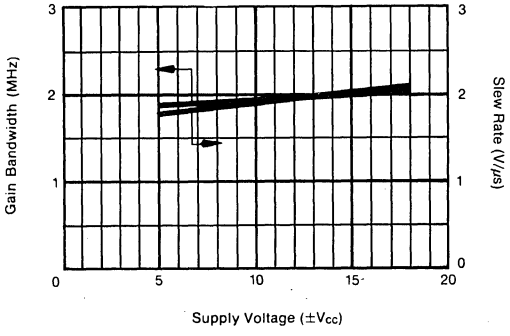
OPEN-LOOP FREQUENCY RESPONSE



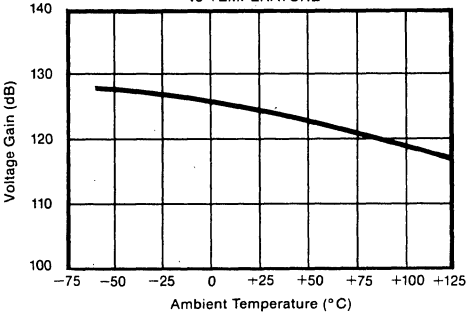
COMMON-MODE REJECTION
vs FREQUENCY



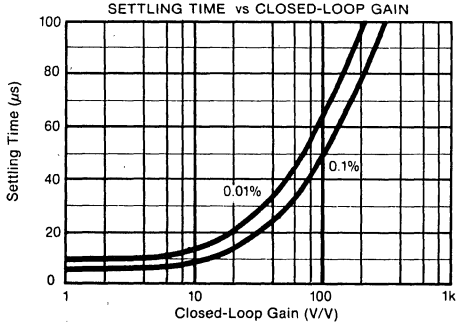
GAIN-BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE

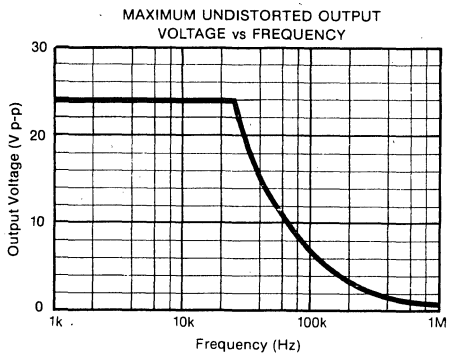


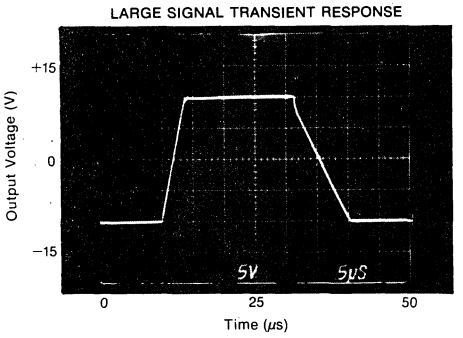
OPEN-LOOP GAIN
vs TEMPERATURE

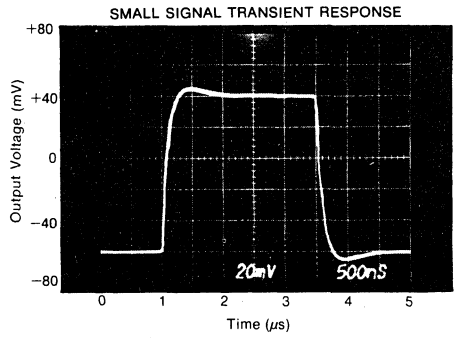


SETTLING TIME vs CLOSED-LOOP GAIN









8. APPLICATION INFORMATION

8.1 Offset voltage adjustment. Although the OPA111/883B Series has a low initial offset voltage (500μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser-adjusted offset-voltage temperature drift slightly. The drift will change approximately 0.3μV/°C for every 100μV of offset adjustment.

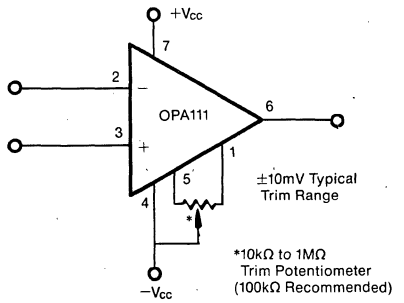


FIGURE 4. Offset Voltage Trim.

8.2 Guarding and shielding. The ultra-low bias current and high input impedance of the OPA111/883B Series are well-suited to a number of stringent applications; however, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA111/883B Series.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the amplifier's bias current of the OPA111/883B Series. To avoid leakage problems, it is recommended that the signal input lead of the OPA111/883B Series be wired to a Teflon™ standoff. If the OPA111/883B Series is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low input impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 5 illustrates the use of the guard. The resistor R_3 shown in Figure 5 is optional. It may be used to compensate effects of very large source resistances. However, note that its use would also increase the noise due to the thermal noise of R_3.

8.3 Additional application information. Additional application information is presented in the commercial OPA111 data sheet.

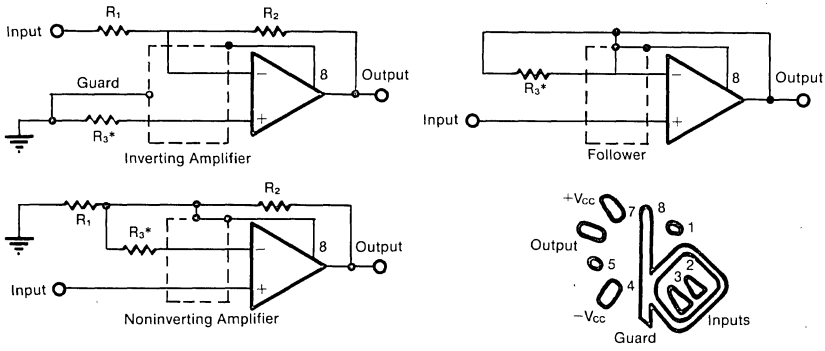
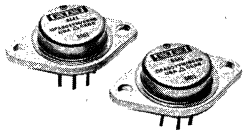


FIGURE 5. Connection of Input Guard.

Teflon™ E.I. du Pont de Nemours and Company.

BURR-BROWN®

OPA501/883B SERIES



OPA501VM/883B **OPA501UM/883B**
OPA501VM **OPA501UM**

High Current, High Power Military OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE, ±10V to ±40V
- HIGH OUTPUT CURRENT, ±10A Peak
- HIGH OUTPUT POWER, 260W Peak
- LOW DC THERMAL IMPEDANCE: 2.2°C/W
- MIL-STD-883 SCREENING

DESCRIPTION

The OPA501 is a high power operational amplifier. Its high current output stage delivers ±10A, yet the amplifier is unity-gain stable and it can be used in any operational amplifier configuration. The 260W peak output capability allows the OPA501 to drive loads (such as motors) with a greater safety margin.

Safe operating area is fully specified and output current limiting is provided to protect both the amplifier and the load from excessive current.

This hybrid IC is housed in an 8-pin hermetic TO-3 package. The electrically-isolated package allows direct mounting to chassis or heat sink without an insulating washer or spacer which would increase thermal resistance.

Two electrical performance grades are available. The premium grade operates from −55°C to +125°C and is designed for military, aerospace, and demanding industrial applications. The U grade has specifications for operation from −25°C to +85°C and from −55°C to +125°C. Applications include test equipment, shipboard, and ground support equipment where operation is normally between −25°C and +85°C and full temperature range operation must be assured.

The OPA501/883B Series is manufactured on a separate Hi-Rel manufacturing line with impeccable clean room conditions, which assures inherent quality and provides for long product life.

Two product assurance levels are available: Standard and /883B. The Standard product assurance level offers Hi-Rel manufacturing where many MIL-STD-883 screens are performed routinely. The /883B product assurance level, /883B suffix, offers Hi-Rel manufacturing, 100% screening per MIL-STD-883 method 5008 and 10% PDA. Quality assurance further processes /883B devices, by performing group A and B inspections on each inspection lot and group C and D inspections as required by MIL-STD-883. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

NOTE: This device was previously identified as OPA8785/883B Series.

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DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
HIGH CURRENT, HIGH POWER OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a high current, high power operational amplifier.

1.2 Part Number. The complete part number is as shown below.

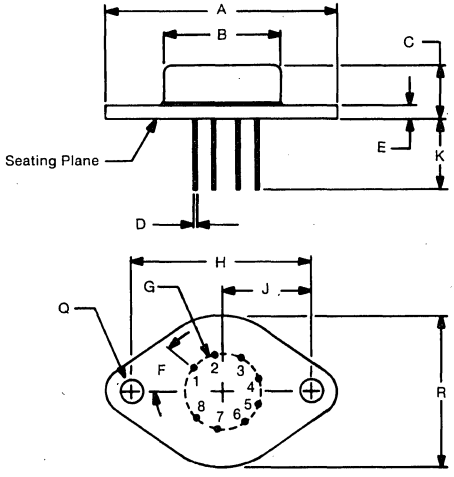
OPA501	V	M	/883B
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.1)

1.2.1 Device type. The device is a single operational amplifier. Two electrical performance grades are provided. The V grade offers performance specifications over the MIL temperature range (−55°C to +125°C) and the U grade is specified over the industrial temperature range (−25°C to +85°C). Electrical specifications are shown in Table I and electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

Hi-Rel Product Designator	Requirements
/883B	Standard model plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(none)	Standard model including 100% electrical testing.

1.2.3 Case Outline. The case outline is an 8-pin TO-3 package and is depicted in Figure 1.



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.340	6.60	8.64
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

FIGURE 1. Case Outline (TO-3) Package Configuration.

1.2.4 Absolute maximum ratings.

Supply Voltage V_{CC}	±40VDC
Differential input voltage	$\pm V_{CC} - 3$
DC internal power dissipation	80W 1/
AC internal power dissipation (10kHz, 50% duty cycle)	160W 1/
Output short circuit duration	Continuous to ground
Storage temperature range	−65°C to +165°C
Lead temperature (soldering, 60sec)	300°C
Junction temperature	$T_j = 200°C$
Common-mode input voltage	$\pm V_{CC}$

1.2.5 Recommended operating conditions.

Supply voltage Range	±34VDC (see Table I)
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θJ-C
8-lead TO-3	Figure 1	80W with heat sink	2.2°C/W with heat sink

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510—Microcircuits, general specifications for.

STANDARD
MILITARY
MIL-STD-883—Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.

3.2.2 Design Documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

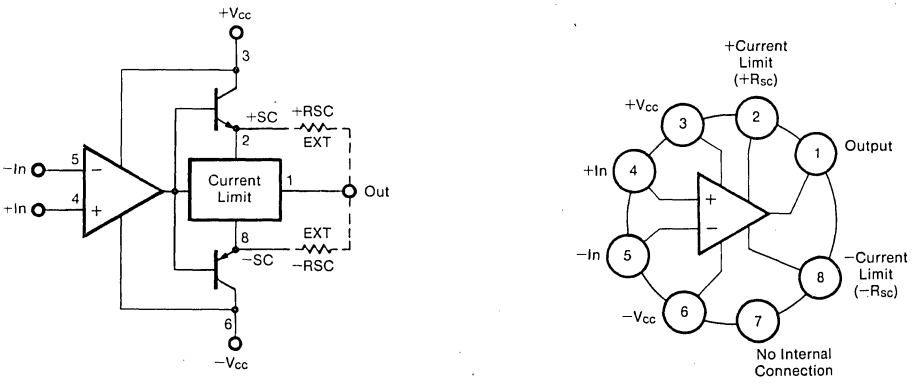
3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. The microcircuit dice are glassivated.

3.3 Electrical performance characteristics. The electrical performance charactersitics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

1/ $T_A \leq +25°C$.



(a) **Circuit Diagram** (b) **Terminal Connections—Top View**

FIGURE 2. Circuit Diagram and Terminal Connections.

TABLE I. Electrical Performance Characteristics.

All characteristics at $-55°C \leq T_A \leq +125°C$, $\pm V_{CC} = 34VDC$ unless otherwise specified.

CHARACTERISTICS	SYMBOL	CONDITIONS	OPA501VM/883B OPA501VM			OPA501UM/883B OPA501UM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
RATED OUTPUT 1/ 2/									
Output Current	I_{OP}	$R_L = 2.6\Omega$, $T_A = +25°C$	−10		+10	*		*	A
Continuous 3/	V_{OP}	$R_L = 10k\Omega$	−30		+30	*		*	V
Output Voltage 3/	V_{OP}	$I_O = 10A$ peak, 10kHz sine wave, $T_A = +25°C$	−26		+26	−20		+20	V
DYNAMIC RESPONSE									
Bandwidth	BW	Unity Gain, Small Signal $T_A = +25°C$		1			*		MHz
Bandwidth	BW	Full Power $V_O = 40Vp\text{-}p$, $R_L = 8\Omega$, $T_A = +25°C$	10			*			kHz
Slew Rate	SR	$R_L = 6.5\Omega$	1.35			*			V/μs
INPUT OFFSET VOLTAGE									
Initial Offset	V_{IO}	$T_A = +25°C$	−5		+5	−10		+10	mV
Tempco	DV_{IO}	$[V_{IO}(T_A) - V_{IO}(+25°C)] \div \Delta T$							
		$-55°C \leq T_A \leq +125°C$	−40		+40				μV/°C
		$-25°C \leq T_A \leq +85°C$				−65		+65	μV/°C
Vs Supply Voltage	PSRR	$V_{CC} = \pm 10$, $V_{CC} = \pm 40$, $T_A = +25°C$	−100		+100	*		*	μV/V
		$-55°C \leq T_A \leq +125°C$	−200		+200	*		*	μV/V
INPUT BIAS CURRENT									
Initial	I_{IB}	$T_A = +25°C$			±20			±40	nA
		$-55°C \leq T_A \leq +125°C$			±35				nA
		$-25°C \leq T_A \leq +85°C$						±50	nA
Vs Supply				±0.02			±0.02		nA/V
INPUT DIFFERENCE CURRENT									
Initial	I_{OS}	$T_A = +25°C$			±3			±10	nA
		$-55°C \leq T_A \leq +125°C$			±7				nA
		$-25°C \leq T_A \leq +85°C$						±7	nA
OPEN LOOP GAIN, DC	A_{VS}	$R_L = 10k\Omega$	94			90			dB
INPUT IMPEDANCE	Z_{IO}			10			*		MΩ
	Z_{ICM}			250			*		MΩ

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	SYMBOL	CONDITIONS	OPA501VM/883B OPA501VM MIN	OPA501VM/883B OPA501VM TYP	OPA501VM/883B OPA501VM MAX	OPA501UM/883B OPA501UM MIN	OPA501UM/883B OPA501UM TYP	OPA501UM/883B OPA501UM MAX	UNITS
INPUT NOISE									
Voltage Noise	e_n	f_n = 0.3Hz to 10Hz		3			*		μV, p-p
		f_n = 10Hz to 10kHz		5			*		μV, rms
Current Noise	i_n	f_n = 0.3Hz to 10Hz		20			*		pA, p-p
		f_n = 10Hz to 10kHz		4.5			*		pA, rms*
INPUT VOLTAGE RANGE									
Common-mode	V_{ICM}	Linear Operation	±(|V_{CC}| − 6)			*			V
Common-mode Rejection	CMRR	F = DC, V_{ICM} = ±22V	76			70			dB
		T_A = +25°C	80			70			dB
POWER SUPPLY									
Rated Voltage	V_{CC}			±34			*		V
Operating Voltage Range			±10		±40	*		*	V
Current, Quiescent	I_Q				±10			*	mA
TEMPERATURE RANGE									
Specification			−55		+125	−25		+85	°C
Storage			−65		+150	*		*	°C

*Specification same as OPA501 "V" grade.

NOTES:

1/ Package must be derated based on a junction-to-case thermal resistance of 2.2°C/W or a junction-to-ambient thermal resistance of 30°C/W.

2/ Safe Operating Area and Power Derating Curves must be observed.

3/ With ±R_{SC} = 0. Peak output current is typically greater than 10A if duty cycle and pulse width limitations are observed. Output current greater than 10A is not guaranteed.

3.4 Electrical test requirements. Electrical test requirements are shown in Table II. The subgroups of Table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance are specified in Table II.

TABLE II. Electrical Test Requirements.

MIL-STD-883 REQUIREMENTS (HYBRID CLASS)	MODELS OPA501VM/883B	MODELS OPA501VM	MODELS OPA501UM/883B	MODELS OPA501UM
Interim electrical parameters (Preburn-in) (method 5008)	1	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7	1*, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7
Group A test requirements (method 5008)	1, 2, 3, 4, 5, 6, 7	—	1, 2, 3, 4, 5, 6, 7	—
Group C end point electrical parameters (method 5008)	1	—	1	—

*PDA applies to subgroup 1 for /883B Hi-Rel designator (see 4.3c).

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS ±V_{CC} = ±34VDC unless otherwise specified	LIMITS OPA501VM/883B OPA501VM MIN	LIMITS OPA501VM/883B OPA501VM MAX	LIMITS OPA501UM/883B OPA501UM MIN	LIMITS OPA501UM/883B OPA501UM MAX	UNITS
1	V_{IO}	4001		−5	+5	−10	+10	mV
T_A = +25°C	I_{IB+}	4001		−20	+20	−40	+40	nA
	I_{IB-}	4001		−20	+20	−40	+40	nA
	I_{IO}	4001		−3	+3	−10	+10	nA
	+PSRR	4003	−V_{CC} = 34VDC, +V_{CC} = 10 to 40VDC	−100	+100	*	*	μV/V
	−PSRR	4003	+V_{CC} = 34VDC, −V_{CC} = 10 to 40VDC	−100	+100	*	*	μV/V
	CMRR	4003	V_{CM} = ±22V, F = DC	80		70		dB
	I_{CC+}	4005	V_{CM} = 0, no load condition		+10		*	mA
	I_{CC-}	4005	V_{CM} = 0, no load condition	−10		*		mA

TABLE III. Group A Inspection (cont).

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC} = \pm 34VDC$ unless otherwise specified	LIMITS OPA501VM/883B OPA501VM MIN	LIMITS OPA501VM/883B OPA501VM MAX	LIMITS OPA501UM/883B OPA501UM MIN	LIMITS OPA501UM/883B OPA501UM MAX	UNITS
2	DV_{IO}	4001	$[V_{IO}(+125°C) - V_{IO}(+25°C)] \div 100$	−40	+40	−65	+65	µV/°C
$T_A = +125°C$	I_{IB+}	4001		−35	+35	−60	+60	nA
	I_{IB-}	4001		−35	+35	−60	+60	nA
	I_{IO}	4001		−7	+7	−20	+20	nA
	+PSRR	4003	$-V_{CC} = 34VDC, +V_{CC} = 10$ to 40VDC	−200	+200	*	*	µV/V
	−PSRR	4003	$+V_{CC} = 34VDC, -V_{CC} = 10$ to 40VDC	−200	+200	*	*	µV/V
	CMRR	4003	$V_{CM} = \pm 22V$, F = DC	76		70		dB
	I_{CC+}	4005	$V_{CM} = 0$, no load condition		+10		*	mA
	I_{CC-}	4005	$V_{CM} = 0$, no load condition	−10		*		mA
3	DV_{IO}	4001	$[V_{IO}(+25°C) - V_{IO}(-55°C)] \div 80$	−40	+40	−65	+65	µV/°C
$T_A = -55°C$	I_{IB+}	4001		−35	+35	−60	+60	nA
	I_{IB-}	4001		−35	+35	−60	+60	nA
	I_{IO}	4001		−7	+7	−20	+20	nA
	+PSRR	4003	$-V_{CC} = 34VDC, +V_{CC} = 10$ to +40VDC	−200	+200	*	*	µV/V
	−PSRR	4003	$+V_{CC} = 34VDC, -V_{CC} = 10$ to 40VDC	−200	+200	*	*	µV/V
	CMRR	4003	$V_{CM} = \pm 22V$, F = DC	76		70		dB
	I_{CC+}	4005	$V_{CM} = 0$, no load condition		+10		*	mA
	I_{CC-}	4005	$V_{CM} = 0$, no load condition	−10		*		mA
4	V_{OP}**	4004	$I_O = 10A$ peak, 10kHz sine wave	−26	+26	−20	+20	V
$T_A = +25°C$	I_{OP}**	4004	$R_L = 2.6\Omega$, 10kHz sine wave	−10	+10	*	*	A
	A_{VS}	4004	$R_L = 10k\Omega$	94		90		dB
5	V_{OP}	4004	$R_L = 10k\Omega$	−30	+30	*	*	V
$T_A = +125°C$	A_{VS}	4004	$R_L = 10k\Omega$	94		90		dB
6	V_{OP}	4004	$R_L = 10k\Omega$	−30	+30	*	*	V
$T_A = -55°C$	A_{VS}	4004	$R_L = 10k\Omega$	94		90		dB
7	SR	4002	$R_L = 6.5\Omega$	1.35		*		V/µs
$T_A = +25°C$								

* Specification same as OPA501 "V" grade.
** Performed in final electrical only.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum:

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin
f. Electrostatic sensitivity identifier (Δ)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the /883B product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for /883B Hi-Rel product designation is in accordance with MIL-STD-883, method 5008, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, constant acceleration (condition A), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

For the /883B product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /883B product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the /883B Hi-Rel product designation is in accordance with MIL-STD-883, method 5008, class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.

b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B or D
   (2) Test circuit is Figure 3 herein for condition B
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

c. Percent defective allowable (PDA). The PDA, for /883B product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

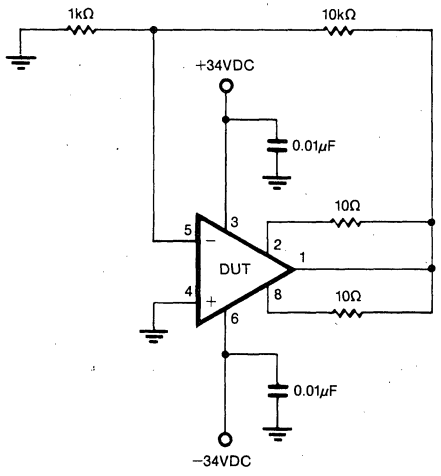


FIGURE 3. Test Circuit—Burn-in and Operating Life Test (Condition B).

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, class B, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5008, class B are performed as required by MIL-STD-883. A report of the most recent group C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, class B and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B or D
   (2) Test circuit is Figure 3 herein for condition B
   (3) $T_A = +125°C$ minimum
   (4) Test condition is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008 and as follows:

a. End point electrical parameters are specified in Table II herein.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirments for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

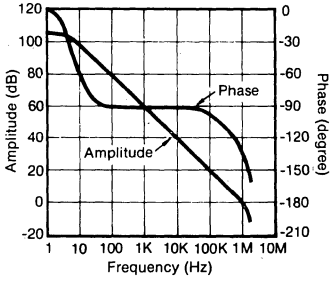
6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group I as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

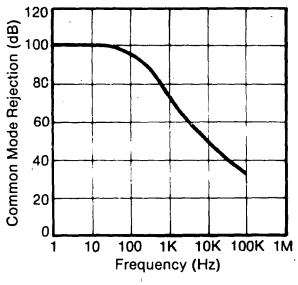
7. ELECTRICAL PERFORMANCE CURVES

Typical at +25°C case and $\pm V_{CC}$ = 28VDC unless otherwise noted.

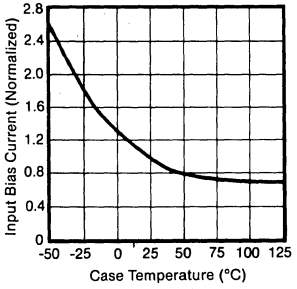
OPEN-LOOP FREQUENCY RESPONSE



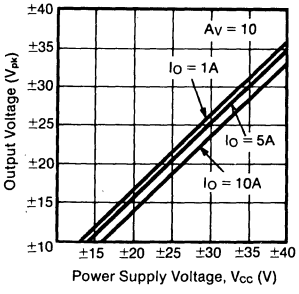
COMMON MODE REJECTION VS FREQUENCY



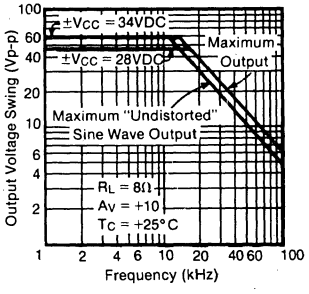
INPUT BIAS CURRENT VS TEMPERATURE



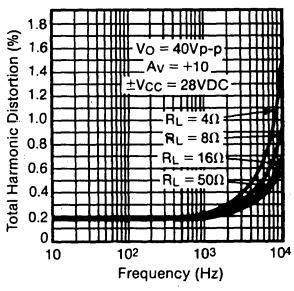
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE



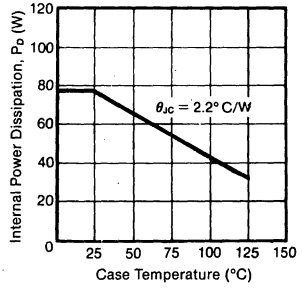
FULL POWER RESPONSE



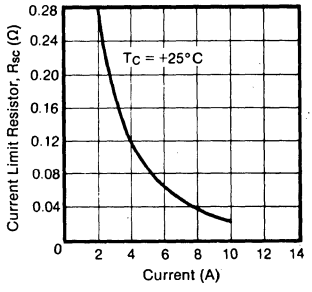
HARMONIC DISTORTION



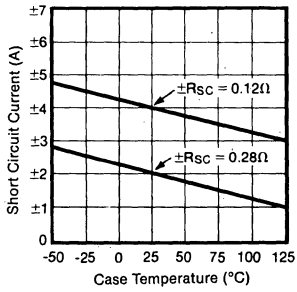
POWER DERATING CURVE



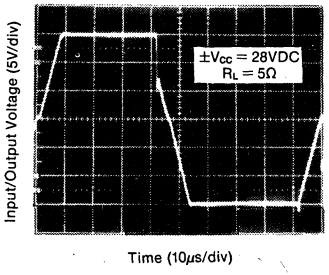
CURRENT LIMITING



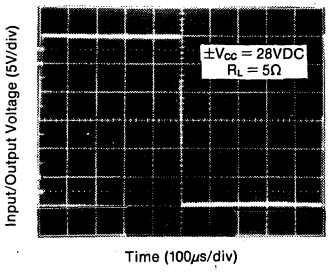
CURRENT LIMITING



PULSE RESPONSE, A_V = +1



PULSE RESPONSE, A_V = +1



8. APPLICATION INFORMATION

8.1 Grounding. Because of the high output current capability of the OPA501/883B Series, the user is cautioned to observe proper grounding techniques. Figure 4 illustrates a recommended technique.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

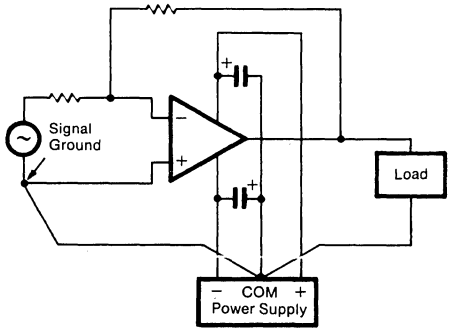


FIGURE 4. Proper Power Supply Connections.

8.2 Supply bypassing. The OPA501 power supplies should be bypassed with 50μF tantalum capacitors connected as close as possible to pins 3 and 6. These bypass capacitors should be connected to the load ground rather than the signal ground.

8.3 Current limits. OPA501 amplifier is designed so that both positive and negative load current limits can be set independently with external resistors $+R_{SC}$ and $-R_{SC}$ respectively. The approximate value of these resistors is given by the equation:

$$R_{SC} = [(0.65 \div I_{LIMIT}) - 0.0437] \text{ ohms}$$

I_{LIMIT} is the desired maximum current in amperes. The power dissipation of the current limit resistor is:

$$P_{max} = R_{SC} (I_{LIMIT})^2 \text{ watts}$$

R_{SC} is in ohms and I_{LIMIT} is in amperes.

Current limit resistors carry the full amplifier output current so lead lengths should be minimized. Highly inductive resistors can cause loop instability. Variation in limit with case temperature is shown in the Typical Performance Curves, paragraph 7.

The amplifier should be used with as low a current limit as possible for its particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and will increase reliability by limiting internal power dissipation.

The current limits may be used to generate other functions such as constant current supplies and torque or stall current limits for servomotor applications.

8.4 Heat sinking. The OPA501 requires a heat sink to limit output transistor junction temperature (T_J) to an absolute maximum of +200°C. The steady-state thermal circuit is illustrated in Figure 5.

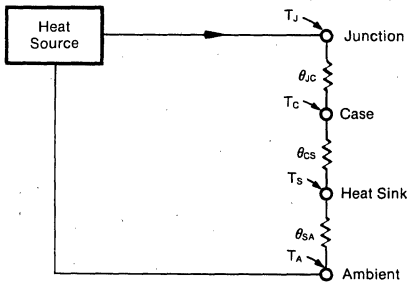


FIGURE 5. Simplified Steady-State Heat Flow Model.

Junction temperature (T_J) is found from the equation:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

where P_D = average amplifier power dissipation (W)
θ_{JC} = junction-to-case thermal resistance (°C/W)
θ_{CS} = case-to-sink thermal resistance (°C/W)
θ_{SA} = sink-to-ambient thermal resistance (°C/W)
T_A = ambient temperature (°C)

For most heat sink calculations the quiescent power dissipation is very low (<1W) and can be disregarded with only a small error.

The maximum size heat sink can be found as follows:

Example: Find the maximum thermal resistance (smallest heat sink) that can be used for an OPA501 with $\pm V_{CC}$ = 28VDC. Output voltage is +10VDC across a 10Ω resistor and ambient temperature is +50°C:

$$\theta_{SA} = [(T_J - T_A) \div PD] - \theta_{CS} - \theta_{JC}$$

As large a heat sink as possible should be used. θ_{CS} depends on the flatness of the heat sink, the thermal compound used, and the roughness of the mating surfaces. Typical values are between 0.1°C/W and 0.3°C/W for TO-3 package properly mounted on a heat sink.

The OPA501 mounting flange is electrically-isolated and can be mounted directly to a heat sink without insulating washers or spacers.

The output transistor thermal resistance (θ_{JC}) is a function of the output current pulse width, pulse shape, and duty cycle. Long duration pulses allow the junction temperature to approach its steady state value while shorter pulses cause a lower peak junction temperature due to the junction's thermal time constant. Heat is conducted away from the junction rapidly so that as the duty cycle decreases, junction temperature decreases.

Steady state θ_{JC} is rated at 2.2°C/W maximum. In applications where the amplifier's output current alternates between output transistors—for example, an AC amplifier—the transistor θ_{JC} will depend on frequency as shown in Figure 6.

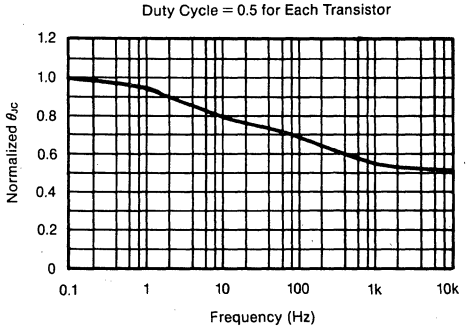


FIGURE 6. Effective θ_{JC} for Applications Where Output Current Alternates Between Output Transistors.

8.5 Safe operating area (SOA). In addition to the limits imposed by power dissipation, the amplifier's output transistors are also limited by a second breakdown region. This occurs because of increased emitter current density due to current crowding at higher operating voltages. Both the dissipation and second breakdown limits depend on time and temperature. Figure 7 shows each output transistor's SOA at a case temperature of +25°C.

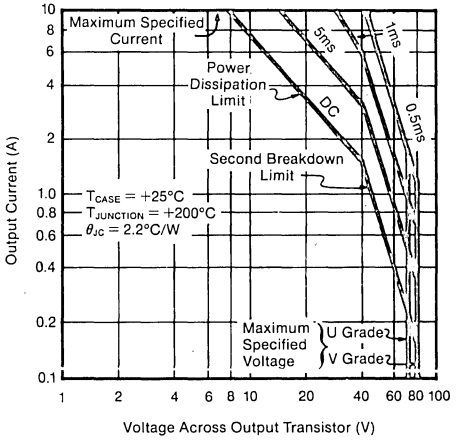


FIGURE 7. Transistor Safe Operating Area at +25°C Case Temperature.

Limits for short pulse widths are substantially greater than for steady state (DC). At a case temperature of +125°C the SOA limits are reduced (see Figure 8). The SOA shown in these curves is based on a conservative linear derating of both the power dissipation and the second breakdown region.

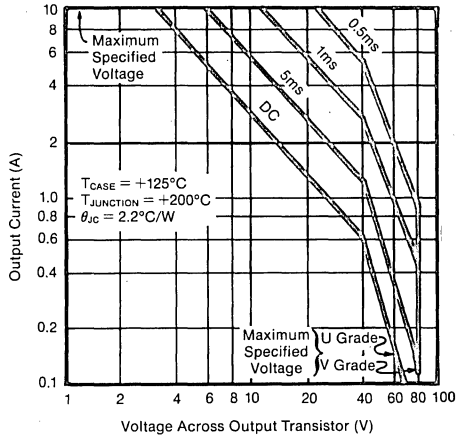


FIGURE 8. Transistor Safe Operating Area at +125°C Case Temperature.

Resistive loads are easy to analyze by simply plotting load lines on the SOA curve. If the curve representing the load line stays within the OPA501 output transistor's SOA curve and all other parameters are observed, such as case temperature, etc., the amplifier will be safe. The load line can swing through the larger SOA limits if their time duration constraints are strictly observed.

Reactive loads present a more complex problem since the output voltage and current are not in phase. This results in the reactive load line becoming elliptical (when plotted on linear axes) which requires a larger SOA for safe operation.

Although detailed analysis is beyond the scope of this data sheet, the load line can be viewed on an oscilloscope as shown in Figure 9. The X-Y display is driven by the voltage across the load and by the current into the load. This setup can also display voltage and current stress across the OPA501 output transistors as shown in Figure 10. This data can then be compared to the SOA limits.

The amplifier is designed to operate with electromotive force generating loads such as servomotors, relays, and actuators. Careful attention must be paid to both the load characteristics and the amplifier's SOA to ensure safe operation.

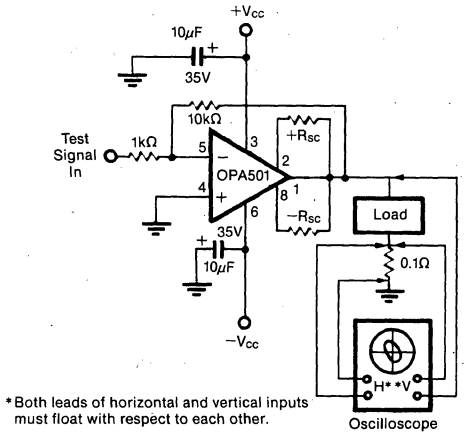


FIGURE 9. Loadline Display.

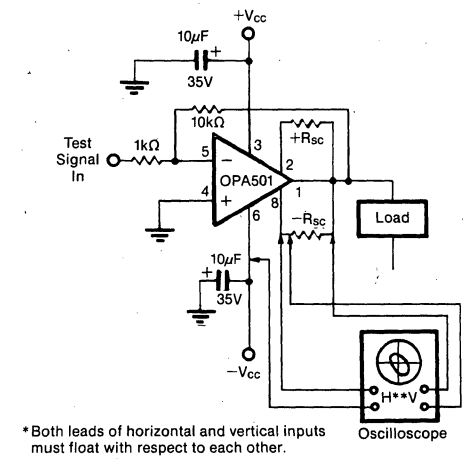


FIGURE 10. Output Transistor Safe Operating Area Stress Display.

Figure 11 shows the OPA501 configured as a DC permanent magnet motor driver. The armature current (I_A) and motor voltage (V_M) are monitored by an oscilloscope in the X-Y mode. Slewing the motor with a 4Hz sine wave results in the motor power ellipse of Figure 12. The input level has been adjusted to give ±20V, peak across the motor. An examination of the power ellipse indicates that the instantaneous power delivered to the motor exceeds the amplifier's output transistors safe operating area at a case temperature of +25°C. The point at which the motor shows 0V at −6.9A is a problem. The voltage across the output is 28V − 0V = 28V. Checking the SOA curve shows that the amplifier can safely withstand this condition for slightly under 5msec. At 4Hz this transient swing outside the DC SOA region is exceeded for much longer than 5msec. Continued operation under these conditions will result in device failure. Peak junction temperatures should not exceed +200°C. Perhaps a motor with a higher impedance winding should be considered for this application. Current limiting and lower supply voltage can also reduce dissipation.

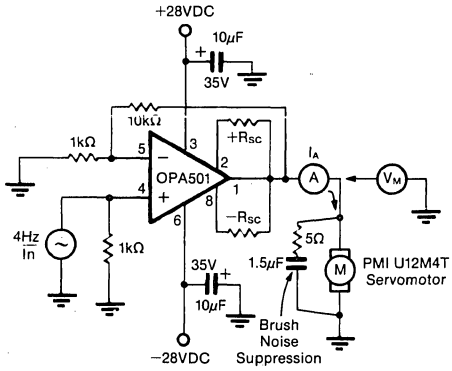


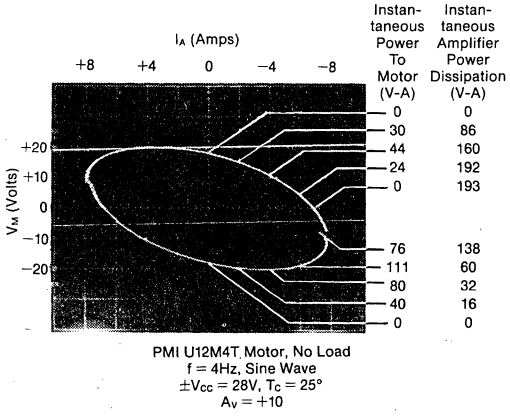
FIGURE 11. Servomotor Amplifier.

Motors used in servo applications often require a surprisingly large current to accelerate quickly. Worst-case conditions occur when the motor is operating at full speed and is suddenly slammed into reverse ("plugging"). This condition is illustrated in Figure 13 when a DC servomotor is driven by a bipolar square wave. As the motor reverses direction, a large surge current flows, causing very-high peak power dissipation in the amplifier. After several time constants (determined by the inertia moment) the current drops to a lower steady-state value. Loading the motor increases the motor average power and amplifier dissipation. SOA curves should be checked for safe operation under these surge conditions.

The OPA501 current limits may be set to clip the high surge currents to a safe level. This is shown in Figure 14. Note that the current limit does limit the servomotor peak acceleration.

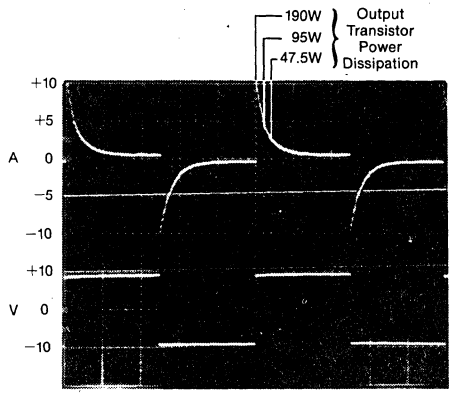
Inductive loads should be investigated for high peak transients generated by a collapsing magnetic field. Resistive damping can reduce this problem and although the amplifier has a substrate as part of the Darlington output transistor structure, external diodes are recommended for heavy clamping.

Fast diodes such as those normally used as rectifiers in switching power supplies are suitable.



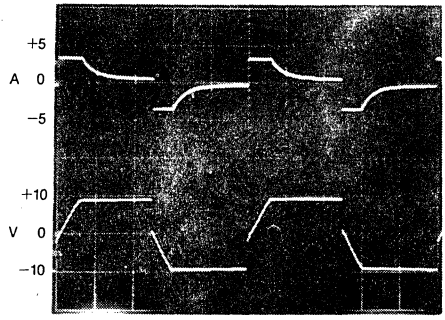
PMI U12M4T Motor, No Load
f = 4Hz, Sine Wave
$\pm V_{CC}$ = 28V, T_C = 25°
A_V = +10

FIGURE 12. DC Servomotor Load Line.



PMI U12M4T Motor, No Load
f = 4Hz, Square Wave
$\pm V_{CC}$ = 28V, T_C = 25°
A_V = +10

FIGURE 13. Servomotor Drive—"Plugging".



PMI U12M4T Motor, No Load
f = 4Hz, Sine Wave
$\pm V_{CC}$ = 28VDC, $\pm R_{SC}$ = 0.15Ω
T_C = 25°, A_V = +10

FIGURE 14. Servomotor Drive With Current Limit.

BURR-BROWN®

PWR7XX Series

5W Rated Output Power
REGULATED DC/DC CONVERTER SERIES

FEATURES

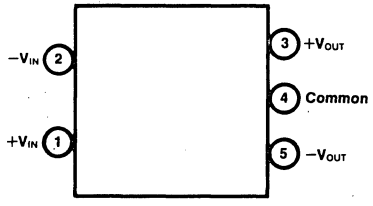
- Isolation Voltage Tested per UL544, VDE750, and CSAC22.2 Dielectric Withstand Requirement
- Barrier Leakage Current 100% Tested at 240VAC
- Single Channel
- Single or Dual Regulated Outputs
- Linear Output Regulation
- Wide Operating Temperature Range: −40°C to +100°C
- Input and Output Filtering
- Six-Sided Shielding

DESCRIPTION

The PWR7XX Series offers a large selection of regulated 5W DC/DC converters for use in such diverse applications as process control, telecommunications, portable equipment, medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

Thirty-six models allow the user to select input voltages ranging from +5VDC to +48VDC and output voltages of +5, +12, +15, ±5, ±12, or ±15V. Surface-mounted devices and manufacturing processes are used in the PWR7XX Series to give the user a device which is more environmentally rugged than most DC/DC converters. The use of surface-mount technologies also gives the PWR7XX Series superior isolation voltage. Each PWR7XX Series unit is tested in compliance with the dielectric withstand voltage requirements of UL544, VDC750, and CSAC22.2.

CONNECTION DIAGRAM



ORDERING INFORMATION

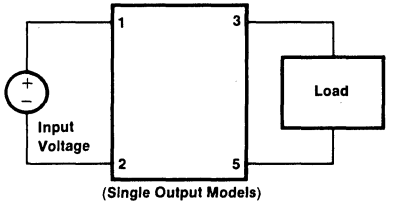
PWR 7XX /G

Device Family
PWR indicates DC/DC converter

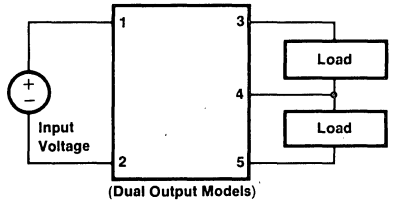
Model Number
Selected from table of Electrical Characteristics

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

TYPICAL APPLICATIONS



(Single Output Models)



(Dual Output Models)

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS[1]

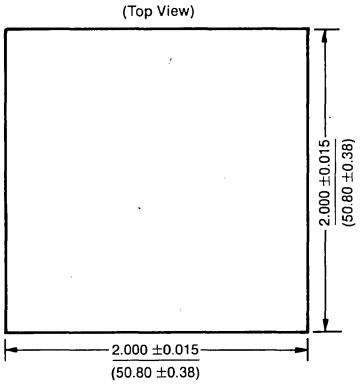
Model	Nominal Input Voltage (VDC)	Rated Output Voltage (VDC)	Rated Output Current (mA)	Input Current		Reflected Ripple Current, typ (mA) p-p	Regulation		Efficiency, min (%)
				No Load, typ (mA)	Rated Load, typ (mA)		Line, typ (%)	Load, typ (%)	
PWR700	5	5	1000	168	1600	30	.02	.04	61
PWR701		12	417	168	1535	30	.02	.04	63
PWR702		15	334	168	1490	30	.02	.04	65
PWR703		±5	±500	168	1560	30	.02	.04	62
PWR704		±12	±209	168	1490	30	.02	.04	65
PWR705		±15	±167	168	1450	30	.02	.04	67
PWR706	12	5	1000	38	620	10	.02	.04	61
PWR707		12	417	38	550	10	.02	.04	63
PWR708		15	334	38	535	10	.02	.04	65
PWR709		±5	±500	38	640	10	.02	.04	62
PWR710		±12	±209	38	550	10	.02	.04	65
PWR711		±15	±167	38	535	10	.02	.04	67
PWR712	15	5	1000	35	510	10	.02	.04	61
PWR713		12	417	35	490	10	.02	.04	63
PWR714		15	334	35	470	10	.02	.04	65
PWR715		±5	±500	35	520	10	.02	.04	62
PWR716		±12	±209	35	480	10	.02	.04	65
PWR717		±15	±167	35	455	10	.02	.04	67
PWR718	24	5	1000	33	320	20	.02	.04	61
PWR719		12	417	33	305	20	.02	.04	63
PWR720		15	334	33	300	20	.02	.04	65
PWR721		±5	±500	33	330	20	.02	.04	62
PWR722		±12	±209	33	310	20	.02	.04	65
PWR723		±15	±167	33	305	20	.02	.04	67
PWR724	28	5	1000	33	280	20	.02	.04	61
PWR725		12	417	33	270	20	.02	.04	63
PWR726		15	334	33	260	20	.02	.04	65
PWR727		±5	±500	33	280	20	.02	.04	62
PWR728		±12	±209	33	270	20	.02	.04	65
PWR729		±15	±167	33	260	20	.02	.04	67
PWR730	48	5	1000	31	165	10	.02	.04	61
PWR731		12	417	31	160	10	.02	.04	63
PWR732		15	334	31	155	10	.02	.04	65
PWR733		±5	±500	31	165	10	.02	.04	62
PWR734		±12	±209	31	155	10	.02	.04	65
PWR735		±15	±167	31	155	10	.02	.04	67

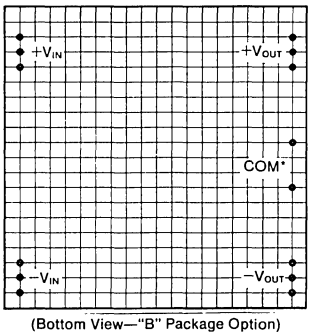
COMMON SPECIFICATIONS[1]

Parameter	Conditions	Min	Typ	Max	Units
INPUT					
Voltage Range	V_{IN} = 5V Models	4.65		6	VDC
	V_{IN} = 12V Models	11.00		15	VDC
	V_{IN} = 15V Models	13.70		17	VDC
	V_{IN} = 24V Models	21.00		27	VDC
	V_{IN} = 28V Models	25.00		31	VDC
	V_{IN} = 48V Models	44.50		53	VDC
ISOLATION					
Rated Voltage		1000			VDC
Test Voltage	60 Seconds, 60Hz	3000			V_{PK}
Resistance			10		GΩ
Capacitance			170		pF
Leakage Current	240V rms, 60Hz			25	μA, rms
OUTPUT					
Voltage Accuracy			±0.5	±1	%
Voltage Balance	Dual Output Units Only		±0.3		%
Temperature Coefficient	−25°C ≤ T_A ≤ +85°C		±0.01		%/°C
Ripple and Noise	BW = DC to 10MHz		30		mV, p-p
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+100	°C
Storage		−55		+125	°C

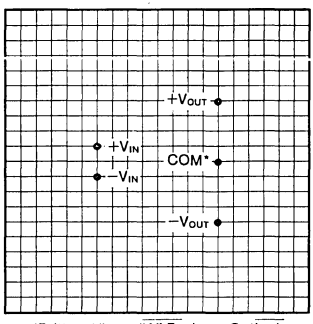
NOTE: (1) Specifications typical at T_A = +25°C, nominal input voltage, and rated output current unless otherwise noted.

MECHANICAL

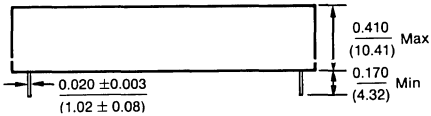




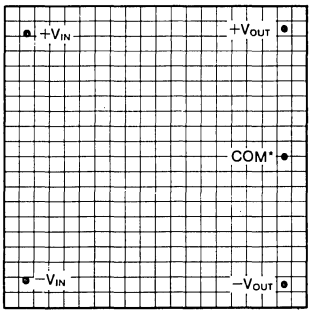
(Bottom View—"B" Package Option)



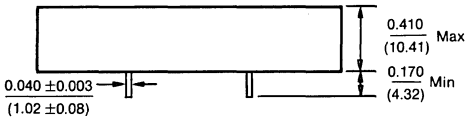
(Bottom View—"A" Package Option)



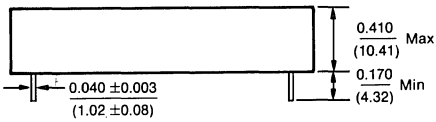
(Side View—"B" Package Option)



(Bottom View—"C" Package Option)



(Side View—"A" Package Option)



(Side View—"C" Package Option)

NOTES:

All dimensions are in inches (millimeters)

GRID: 0.100 inches (2.54 millimeters)

*Common pins are missing on single output models.

MATERIAL: Units are encapsulated in a low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range, and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	120% of nominal
Output Short-Circuit Duration	5 seconds
Internal Power Dissipation	3.5W
Lead Temperature (soldering, 10 seconds)	+300°C
Junction Temperature	+150°C
Package Thermal Resistance, Junction-to-Ambient, θ_{JA}	15°C/W

APPLICATION NOTES

TESTING ISOLATION BARRIER CHARACTERISTICS

The insulation and spacings of the PWR7XX Series are 100% tested to meet the dielectric withstand requirements of UL544, paragraph 31. A 60Hz essentially sinusoidal potential is applied between the primary and secondary for a period of one minute. The potential used for this test is twice the maximum rated voltage plus 1000V. For the PWR7XX Series the test voltage is 3000V peak.

Dielectric withstand testing is intended to be done at the manufacturer's site only. This test will not be repeated. Exposing the dielectric material of the isolation barrier to repeated testing causes microscopic carbonizing of the dielectric, resulting in a weakened barrier. A low resistance path will eventually be created across the barrier.

PRESERVING ISOLATION CHARACTERISTICS

If intrinsic safety is required, care should be taken in the layout and assembly of the printed wiring board (PWB) to avoid degrading the isolation barrier of the PWR7XX. Precautionary measures include cleaning the PWB prior to installing the PWR7XX to prevent trapping contaminates under the unit. Use nonconductive spacers to keep the PWR7XX off the PWB. Use epoxy solder mask to isolate PWB conductive traces which must run under or close to the PWR7XX. In the layout of the PWB, avoid placing PWB traces under the unit. Do not use conductive inks on the PWB under the unit; e.g., inks used in inspection stamps or component identification marking.

OUTPUT POWER DISTRIBUTION

Figure 1 shows the recommended method of connecting multiple loads to the PWR7XX. Single-point power distribution prevents ground loops and interaction between parallel load circuits.

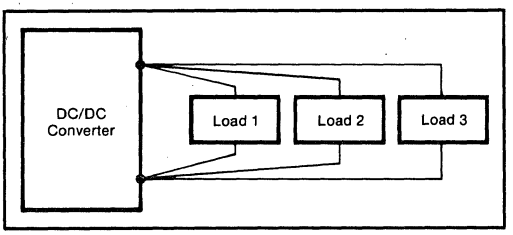


FIGURE 1. Recommended Power Distribution.

MEASURING NOISE

Measuring the input and output noise performance of a DC/DC converter is a very difficult task that should be attempted only in a controlled laboratory test environment due to extraneous noise sources.

Figure 2 illustrates two recommended methods for testing output voltage ripple and noise. Reflected input current ripple and noise should be measured with a high performance current probe. Measuring input current and noise into a "known" impedance with a voltage probe should be avoided.

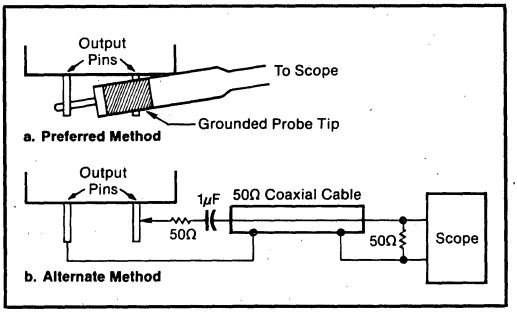


FIGURE 2. Recommended Noise Measurement Methods.

BURR-BROWN®

PWR1017

Four-Channel, Dual-Output, Synchronizable UNREGULATED DC/DC CONVERTER

FEATURES

- Synchronizable
- All Outputs Isolated
- Output Power to 3W
- High Isolation Voltage—1000Vpk
- Six-Sided Shielding
- Input and Output Filtering
- Low Profile Package—0.4" High

APPLICATIONS

- Power for High Resolution Data Acquisition
- Precision Test Equipment
- Spot Regulator
- Process Control
- Portable Equipment
- Multiple Power Supplies

DESCRIPTION

The PWR1017 is a four-channel, dual-output unregulated DC/DC converter designed for low noise applications where high efficiency and switching synchronization are required.

Any unit whose slave pin is connected to another unit's master pin will cause the oscillators to lock together. The PWR1017 may also be driven from a system master clock. The free running switching frequency is 250kHz.

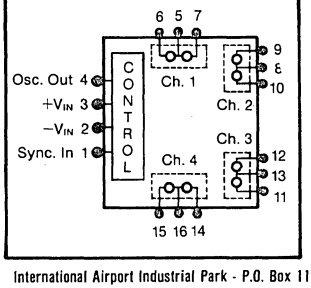
The PWR1017 has four isolated plus and minus output voltages approximately equal to the magnitude of the input voltage. It operates over an input voltage range of 10VDC to 18VDC. Rated output current for the PWR1017 is 25mA for all outputs.

Isolation voltage between the input and any of the four output circuits is 1000Vpk continuous. The same isolation specification applies between any of the four dual outputs.

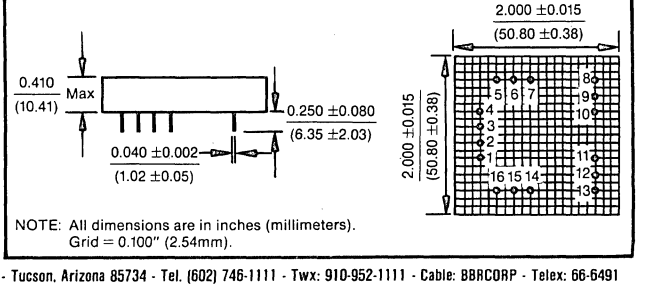
Six-sided shielding suppresses electromagnetic radiation which could disturb sensitive analog measurements or interfere with system timing signals. Filtering the PWR1017 input and outputs minimizes the effects of electrical noise on the source and loads of the converter.

Each PWR1017 is tested in compliance with UL544, VDE750, and CSA C22.2 dielectric withstand specifications. In addition, barrier leakage current is 100% tested.

CONNECTION DIAGRAM



MECHANICAL



NOTE: All dimensions are in inches (millimeters).
Grid = 0.100" (2.54mm).

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SPECIFICATIONS

ELECTRICAL

At T_A = 25°C, V_{IN} = 15VDC, I_{LOAD} = ±25mA and in free running mode unless otherwise noted.

PARAMETER	CONDITIONS	PWR1017 MIN	PWR1017 NORM	PWR1017 MAX	UNITS
INPUT					
Rated Voltage[1]			15		VDC
Voltage Range		10		18	VDC
Input Current	I_{LOAD} = 0		70		mA
	I_{LOAD} = Rated Load		285	350	mA
Ripple Current	I_{LOAD} = Rated Load		80		mA, p-p
ISOLATION	Ratings apply input-to-output and channel-to-channel				
Rated Voltage	Test: 60sec, 60Hz, 3000V, pk	1000			VDC
Resistance			10		GΩ
Capacitance			15		pF
Leakage Current	V_{ISO} = 240VAC, 60Hz		0.9	3	μA
OUTPUT					
Rated Voltage			±15		VDC
Voltage Range	I_{LOAD} = 0mA	±16	±16.5	±18	VDC
	I_{LOAD} = Rated Load	±14.25		±15.75	VDC
Rated Current	Each output	±25			mA
	Total of all outputs	200			mA
Current Range	Each output	0		±40	mA
	Total of all outputs	0		500	mA
Line Regulation	10VDC < V_{IN} < 18VDC		1.16		mV/mV
Load Regulation	0 > I_{LOAD} > 25mA		12.5		mV/mA
Ripple Voltage	I_{LOAD} = 0		±10		mV, pk
	I_{LOAD} = Rated Load			±100	mV, pk
SYNCHRONIZATION[2]					
f_{SYNC} Range	V_{SYNC} > 6.4Vp-p	400		700	kHz
V_{SYNC} Range	400kHz < f_{SYNC} < 700kHz	6.4		36	V, p-p
Oscillator Output Fanout				2	Synch Inputs
V_{SYNC}, max	Max deviation from $-V_{IN}$			50	V
V_{SYNC} Duty Cycle		5	50	60	%
TEMPERATURE					
Specification		−25		+85	°C
Operating		−40		+100	°C
Storage		−55		+125	°C

NOTE: (1) Other voltages available on request. (2) Operating frequency (in sync mode) = $f_{SYNC}/2$. Oscillator frequency (pin 4, free running) = 2 (f operation). Oscillator frequency (pin 4, sync mode) = f_{SYNC}.

ABSOLUTE MAXIMUM RATINGS

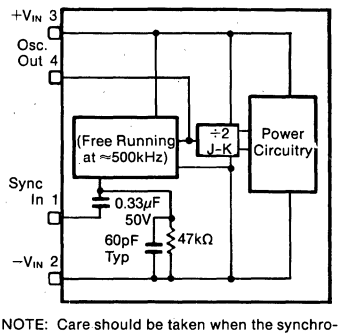
Input Voltage 18VDC
Output Current 500mA
Output Short Circuit
Duration ..... Momentary

ORDERING INFORMATION

PWR 1017 X

Device Family
PWR indicates DC/DC converter
Model Number
Reliability Screening
No designator indicates standard manufacturing process
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

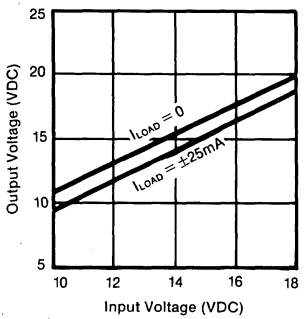
Control Circuitry Block Diagram



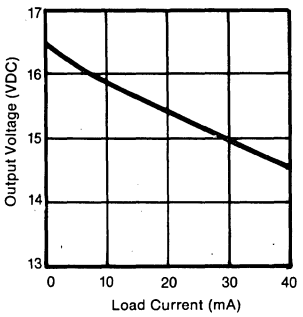
NOTE: Care should be taken when the synchronization input pin is not used, in order to avoid the possibility of noise pick-up and false PLL locking. This could destroy the unit and/or any other units that are coupled to its synchronization output (pin 4). This protection may be accomplished by either tying the synchronization pin to $-V_{IN}$, or clipping pin 1 off flush with the module surface. Tying pin 1 to $-V_{IN}$ is preferred.

TYPICAL PERFORMANCE CURVES

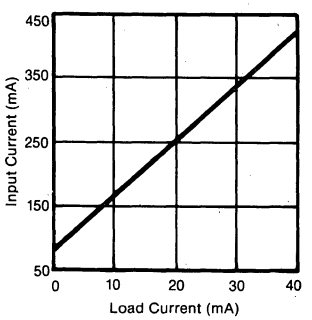
INPUT VOLTAGE VS OUTPUT VOLTAGE
T_A = +25°C



OUTPUT VOLTAGE VS LOAD CURRENT
T_A = +25°C, V_{IN} = 15V; each output loaded to indicated value.



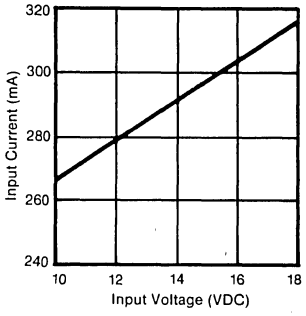
INPUT CURRENT VS OUTPUT CURRENT
T_A = +25°C, V_{IN} = 15VDC; each output loaded to indicated value.



TYPICAL PERFORMANCE CURVES (CONT)

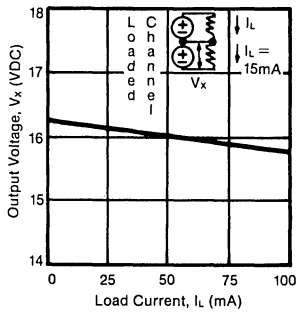
INPUT CURRENT VS INPUT VOLTAGE

T_A = +25°C, I_L = ±25mA



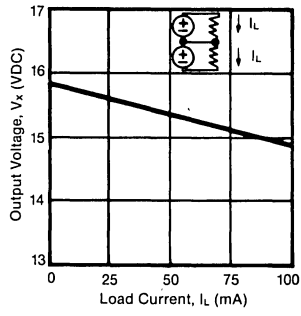
OUTPUT-TO-OUTPUT INTERACTION

T_A = +25°C, V_{IN} = 15V, free running, three outputs unloaded.



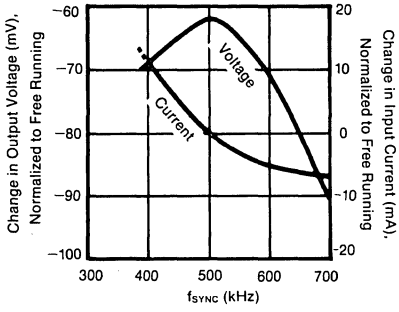
CHANNEL-TO-CHANNEL INTERACTION

T_A = +25°C, V_{IN} = 15VDC, free running, three outputs loaded to ±15mA

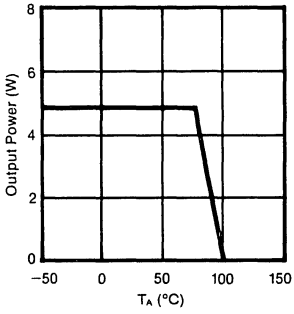


f_{SYNC} VS OUTPUT VOLTAGE AND INPUT CURRENT

T_A = +25°C, V_{IN} = 15VDC, I_L = ±25mA, V_{SYNC} = 15V p-p

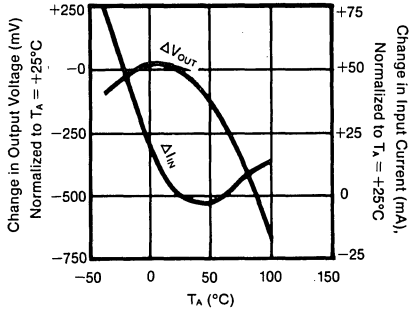


OUTPUT POWER DERATING



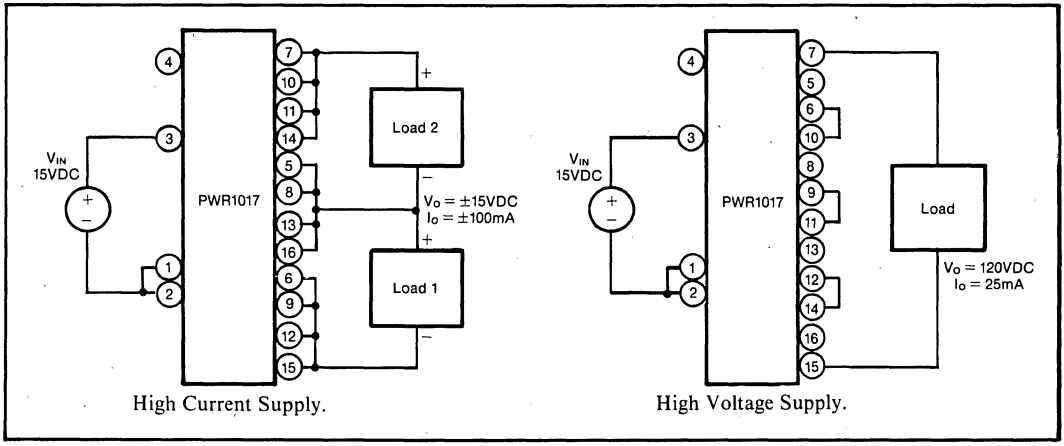
TEMPERATURE CHARACTERISTICS

V_{IN} = +15V, I_{LOAD} = ±25mA, free running.



APPLICATIONS

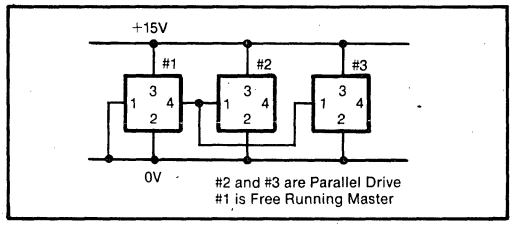
TYPICAL OUTPUT CONNECTIONS



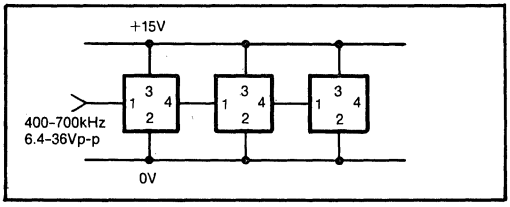
TYPICAL INPUT CONNECTIONS

Single Rail Input Supply

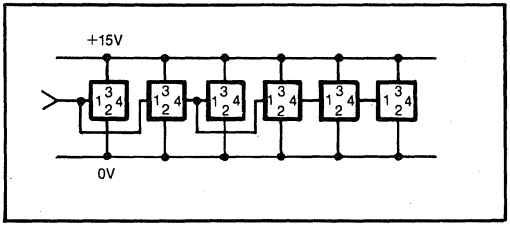
The PWR1017 can be hooked up in a number of configurations for single input voltages. Each unit may become either a master or a slave. The most common configuration is with a single master and multiple slave units.



The PWR1017 may also be connected in series where the first unit can either be a master or a slave driven by the system clock.

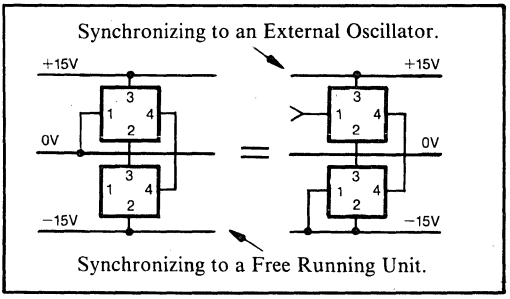


Any combination of serial or parallel may be used.

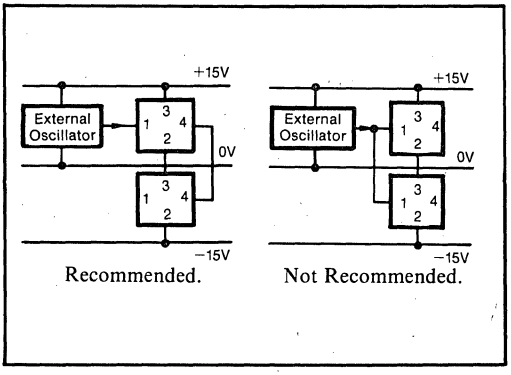


Split Rail Input Supply

PWR1017s may be driven by a differential supply and still be synchronized together. Care should be taken not to exceed the 50V maximum deviation from any $-V_{IN}$.



Tha master pin is a buffered output designed to drive other slave inputs. In split rail applications it is recommended that the external oscillator drive only one unit and all others be driven from the master outputs of other PWR1017s.



APPLICATION NOTES

TESTING ISOLATION BARRIER CHARACTERISTICS

The insulation and spacings of the PWR1017 are 100% tested to meet the dielectric withstand requirements of UL544, paragraph 31. A 60Hz essentially sinusoidal potential is applied between the primary and secondary for a period of one minute. The potential used for this test is twice the maximum rated voltage plus 1000V. For the PWR1017 the test voltage is 3000V peak.

Dielectric withstand testing is intended to be done at the manufacturer's site only. This test will not be repeated. Exposing the dielectric material of the isolation barrier to repeated testing causes mciroscopic carbonizing of the dielectric, resulting in a weakened barrier. A low resistance path will eventually be created across the barrier.

PRESERVING ISOLATION CHARACTERISTICS

If intrinsic safety is required, care should be taken in the layout and assembly of the printed wiring board (PWB) to avoid degrading the isolation barrier of the PWR1017. Precautionary measures include cleaning the PWB prior to installing the PWR1017 to prevent trapping contaminates under the unit. Use nonconductive spacers to keep the PWR1017 off the PWB. Use epoxy solder mask to isolate PWB conductive traces which must run under or close to the PWR1017. In the layout of the PWB, avoid placing PWB traces under the unit. Do not use conductive inks on the PWB under the unit; e.g., inks used in inspection stamps or component identification marking.

BURR-BROWN®

PWR5038

2.75 Watts—Triple-Output DC/DC CONVERTER

FEATURES

- Isolation Voltage 500 VDC
- Barrier Leakage Current 100% Tested at 240VAC
- Low Cost
- Wide Operating Temperature Range
- Input and Output Filtering
- Six-Sided Shielding

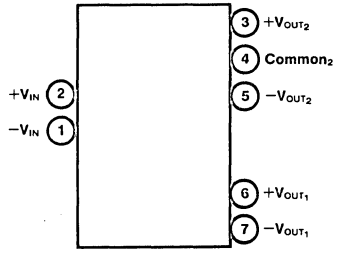
DESCRIPTION

The PWR5038 offers a triple output 2.75W DC to DC converter for use in such diverse applications as process control, telecommunications, portable equipment medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

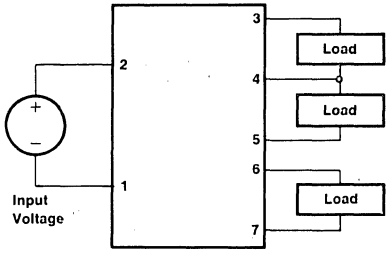
This model gives the user an output voltage of +5 and ±15VDC with an input voltage of +5VDC.

Surface-mounted devices and manufacturing processes are used in the PWR5038 to give the user a device which is more environmentally rugged than most DC to DC converters. The use of surface-mount technology also gives the PWR5038 a low cost reflected in our low prices.

CONNECTION DIAGRAM



TYPICAL APPLICATION



ORDERING INFORMATION

PWR 5038 /G

Device Family
PWR indicates DC/DC converter

Model Number

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

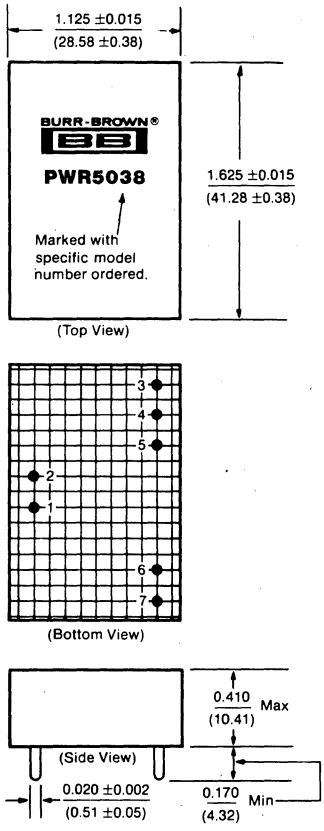
Specifications Typical at Ta = +25 deg C., nominal input voltage and rated output current unless otherwise noted.

PARAMETER	CONDITION	MIN	TYP	MSX	UNT
INPUT					
VOLTAGE			5.00		VDC
RANGE		4.75		5.25	VDC
CURRENT	NO LOAD		150		mA
	FULL LOAD			1.0	A
RIPPLE					mA
CURRENT	FULL LOAD		60		p-p
OUTPUT 1					
VOLTAGE			5		VDC
CURRENT				150	mA
ACCURACY	-25 to + 85 DEG C I LOAD 50 mA to 150 mA INPUT VOLTAGE 4.75 to 5.25 V	4.75		5.25	
RIPPLE	DC to 10 MHz		20		mV p-p
OUTPUT 2					
VOLTAGE			±15		VDC
CURRENT				67	mA
ACCURACY	-25 to +85 DEG C I LOAD 33 mA to 67 mA INPUT VOLTAGE 4.75 to 5.25 V	13.5		16.5	
RIPPLE	DC to 10 MHz		300		mV p-p
ISOLATION					
VOLTAGE		500			VDC
RESISTANCE			10		MΩ
CAPACITANCE			45		pF
LEAKAGE					
CURRENT	Viso = 240 VAC			5	μA
TEMPERATURE					
SPECIFICATION		-25		+85	°C
OPERATION		-40		+100	°C
STORAGE		-55		+125	°C

ABSOLUTE MAXIMUM RATINGS

Input Voltage	120% × rated voltage
Output Short-Circuit Duration	Momentary
Internal Power Dissipation	4W
Junction Temperature	2W
Package Thermal Resistance	+150°C
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL



NOTES:

All dimensions are in inches (millimeters)

GRID: 0.100 inches (2.54 millimeters)

MATERIAL: Low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

BURR-BROWN®

PWR5104
PWR5105

9W Rated Output Power
REGULATED DC-TO-DC CONVERTER

FEATURES

- LOW COST
- LOW NOISE
- LINEAR OUTPUT REGULATION
- WIDE OPERATING TEMPERATURE RANGE: −40°C TO +100°C
- ±12VDC AND ±15VDC OUTPUTS
- INPUT AND OUTPUT FILTERING
- SIX-SIDED SHIELDING
- BARRIER LEAKAGE CURRENT 100% TESTED AT 240VAC

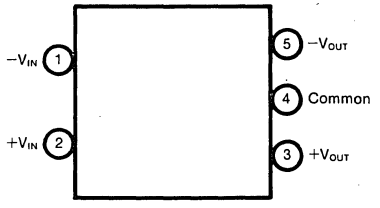
DESCRIPTION

The PWR5104 and PWR5105 offer respectively ±12VDC and ±15VDC ouputs of regulated 9W power driven from your +5V system bus. These units are designed for use in such diverse applications as process control, telecommunications, portable equipment, medical systems, airborne and shipboard electronic circuits, and automatic test equipment.

The PWR5104 and PWR5105 offer a low cost alternative to the models currently in the market. In addition these models utilize high frequency switching in order to maintain a low EMI and RFI environment. Both models incorporate input and output filtering along with six-sided shielding to keep unwanted noise from your circuit.

Surface-mounted devices and manufacturing processes are used in the PWR5104 and PWR5105 to give you a device which is more environmentally rugged than most DC-to-DC converters. These manufacturing and design technologies also give superior isolation voltage. The PWR5104 and PWR5105 are tested in compliance with the dielectric withstand voltage requirements of UL544, VDC750, and CSAC22.2.

CONNECTION DIAGRAM



ORDERING INFORMATION

PWR 510X/G

Device Family
PWR indicates DC/DC converter

Model Number
Selected from table of Electrical Characteristics

Reliability Screening
No designator indicates standard manufacturing processing
/G indicates Level I screening—burn-in only
/T indicates Level II screening—stabilization bake, temperature cycling, and burn-in

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SPECIFICATIONS

ELECTRICAL

Specifications typical at T_A = +25°C, nominal input voltage and rated output current unless otherwise noted.

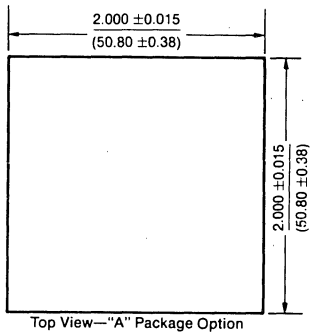
PARAMETER	CONDITIONS	PWR5104/5105 MIN	TYP	MAX	UNITS
INPUT					
Nominal Voltage			5.00		VDC
Voltage Range[1]		4.75		5.25	VDC
Input Current	No load		60		mA
Input Current	Rated load		2400	2570	mA
Ripple Current	At rated load		5		mA,p-p
OUTPUT					
PWR5104 Rated Voltage			±12		VDC
PWR5105 Rated Voltage			±15		VDC
Accuracy			±0.5	±1.0	%
Voltage Balance			±0.3		%
Temperature Coefficient	−25°C to +85°C		±0.01		%/°C
PWR5104 Rated Current		±375			mA
PWR5105 Rated Current		±300			mA
Ripple and Noise	BW = DC to 10MHz		6	35	mV,p-p
Line Regualtion			0.02		%
Load Regulation			0.04		%
Efficiency		70	75		%
ISOLATION					
Rated Voltage		750			VDC
Resistance			10		GΩ
Capacitance			50		pF
Leakage Current	240Vrms, 60Hz			15	μA, rms
GENERAL					
Switching Frequency			50		kHz
TEMPERATURE					
Specification		−25		+85	°C
Operation		−40		+100	°C
Storage		−55		+125	°C

NOTE: (1) Other voltage ranges available. Contact factory.

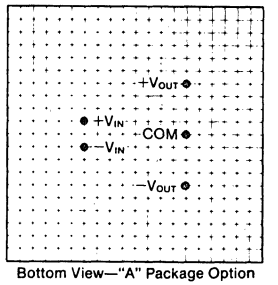
ABSOLUTE MAXIMUM RATINGS

Input Voltage..... 110% of nominal
Output Short-Circuit Duration ..... 15 seconds
Internal Power Dissipation 4.0W
Lead Temperature (soldering, 10 seconds)..... +300°C
Junction Temperature..... +150°C
Package Thermal Resistance,
Junction-to-Ambient, θ_{JA} ..... 15°C/W

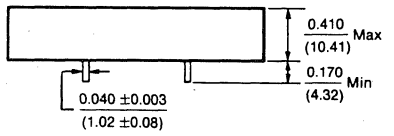
MECHANICAL



Top View—"A" Package Option



Bottom View—"A" Package Option



Side View—"A" Package Option

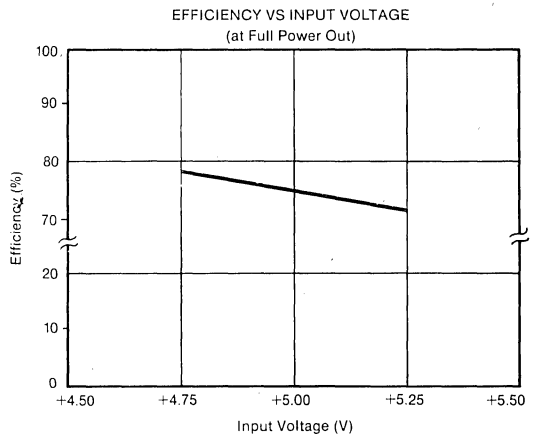
NOTES:

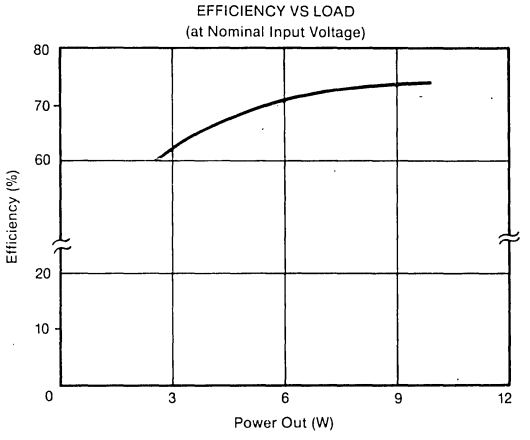
All dimensions are in inches (millimeters)

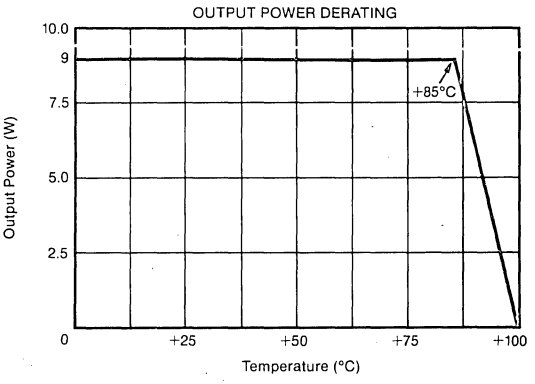
GRID: 0.100 inches (2.54 millimeters)

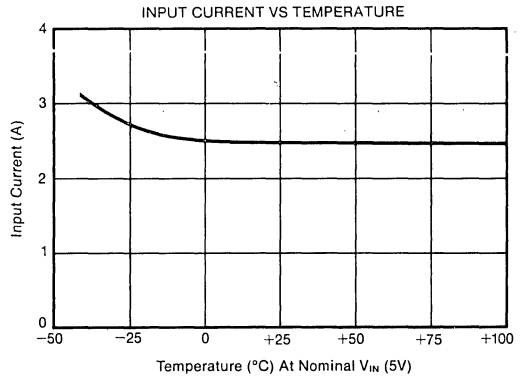
MATERIAL: Units are encapsulated in a low thermal resistance molding compound which has excellent chemical resistance, wide operating temperature range, and good electrical properties under high humidity environments. Lead material is brass with a hot-solder-dipped surface to allow ease of solderability.

TYPICAL PERFORMANCE CURVES









RELIABILITY

All Burr-Brown DC/DC converters are manufactured using stringent in-process controls and quality inspections. The customer may also choose one of two additional levels of screening to meet specific requirements.

The advanced reliability program is designed to reduce infant mortality, system rework, field failures, and equipment downtime.

Standard Manufacturing Process

Incoming Material Inspection
Per MIL-S-19500
↓
Component Attachment
↓
100% Internal Visual Inspection
↓
100% Electrical Test
↓
Seal
↓
100% Final Electrical Test
↓
External Visual
↓
QA Lot Acceptance Testing, AQL = 1.0

/G—Level I Screening

Standard Manufacturing Process
↓
Burn-in, MIL-STD-883,
method 1015, 160 hours, $T_A = +125°C$
↓
Final Electrical Test
↓
QA Lot Acceptance Testing, AQL = 0.5

/T—Level II Screening

Standard Manufacturing Process
↓
Stabilization Bake, MIL-STD-883,
method 1008, 24 hours, $T_A = +125°C$
↓
Temperature Cycling, MIL-STD-883,
method 1010, Condition B (−55°C to +125°C)
↓
Burn-in, MIL-STD-883,
method 1015, 160 hours, $T_A = +125°C$
↓
Final Electrical Test
↓
QA Lot Acceptance Testing, AQL = 0.25

APPLICATION NOTES

PRESERVING ISOLATION CHARACTERISTICS

If intrinsic safety is required, care should be taken in the layout and assembly of the printed wiring board (PWB) to avoid degrading the isolation barrier of the PWR510X. Precautionary measures include cleaning the 510X prior to installing the PWR510X to prevent trapping contaminates under the unit. Use nonconductive spacers to keep the PWR510X off the PWB. Use epoxy solder mask to isolate PWB conductive traces which must run under or close to the PWR510X. In the layout of the PWB, avoid placing PWB traces under the unit. Do not use conductive inks on the PWB under the unit; e.g., inks used in inspection stamps or component identification marking.

OUTPUT POWER DISTRIBUTION

Figure 1 shows the recommended method of connecting multiple loads to the PWR510X. Single-point power distribution prevents ground loops and interaction between parallel load circuits.

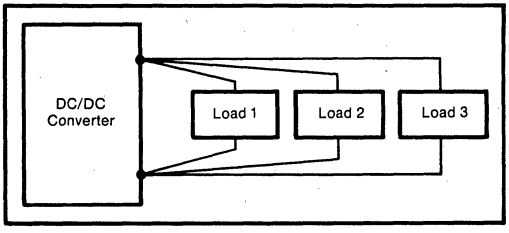


FIGURE 1. Recommended Power Distribution.

MEASURING NOISE

Measuring the input and output noise performance of a DC/DC converter is a very difficult task that should be attempted only in a controlled laboratory test environment due to extraneous noise sources.

Figure 2 illustrates two recommended methods for testing output voltage ripple and noise. Reflected input current ripple and noise should be measured with a high performance current probe. Measuring input current and noise into a "known" impedance with a voltage probe should be avoided.

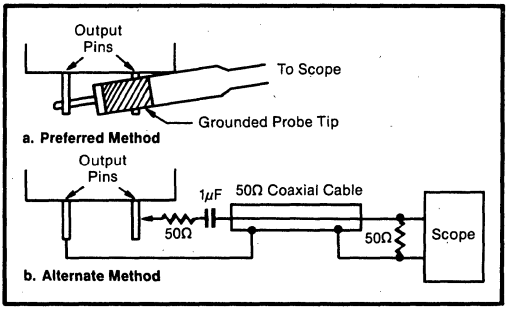
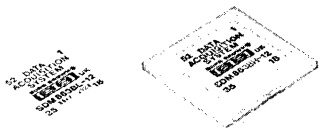


FIGURE 2. Recommended Noise Measurement Methods.

BURR-BROWN®

SDM862
SDM863



16 Single Ended / 8 Differential Input
12-BIT DATA ACQUISITION SYSTEMS

FEATURES

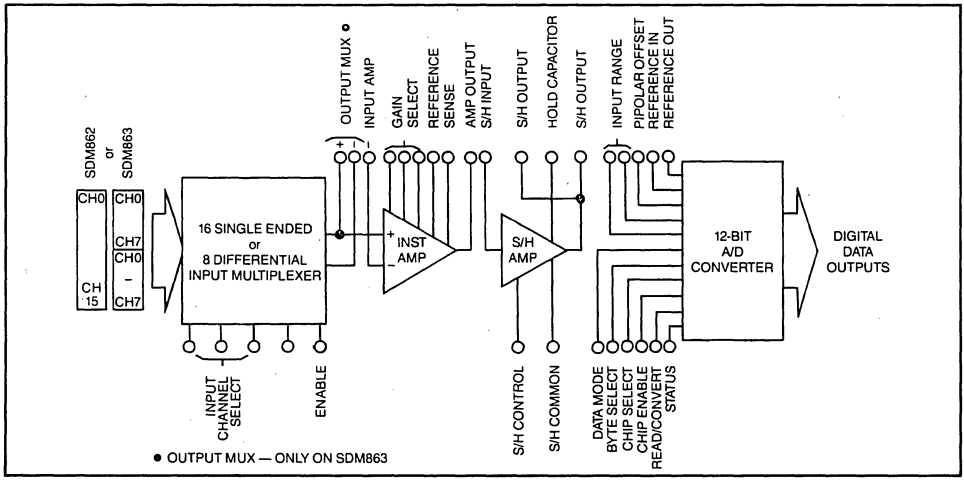
- COMPLETE 12-BIT DATA ACQUISITION SYSTEM IN A MINIATURE PACKAGE
- INPUT RANGES SELECTABLE FOR UNIPOLAR OR BIPOLAR OPERATION
- THROUGHPUT RATES
  - 8-BIT ACCURACY — 45KHz
  - 12-BIT ACCURACY — 33KHz
- SELECTABLE GAINS OF 1, 10 and 100
- FULL MICROPROCESSOR COMPATIBLE INTERFACE
- GUARANTEED NO MISSING CODES OVER TEMPERATURE
- SURFACE MOUNT OR PIN GRID ARRAY PACKAGE OPTIONS
- FULL SPECIFICATION OVER 3 TEMPERATURE RANGES
  - 0 to +70°C
  - −25 to +85°C
  - −55 to +125°C

DESCRIPTION

The SDM862 and SDM863 are complete data acquisition systems housed in a hermetically sealed 1″ square leadless chip carrier or a 1.1″ square pin grid array. The small package outlines and low power consumption provide an ideal data acquisition solution where space is at a premium.

The devices comprise of an input multiplexer (SDM862 16 single-ended inputs, SDM863 8 differential inputs), instrumentation amplifier with selectable gains, sample/hold amplifier and A/D converter with microprocessor interface and 3-state buffers.

The SDM862 and SDM863 will accept unipolar or bipolar voltage inputs in the range 0 to +10V, ±5V and ±10V. For low level signals jumper-selectable gains of 10 or 100 can be applied. The number of input channels can be expanded by the addition of multiplexers. The microprocessor interface and the facility of the sample/hold amplifier being controlled directly by the A/D converter simplifies system integration.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL **At 25 °C,** V_{CC} = ± 15V, V_{DD} =5V, external sample/hold capacitor of 4700pF.

MODEL	SDM862/SDM863 J, A, R			SDM862/SDM863 K, B, S			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			★	BITS
INPUT							
ANALOG							
VOLTAGE RANGES — Bipolar			±5, ±10				V
— Unipolar			0-10				V
INPUT IMPEDANCE — On Channel		10^{10}			★		Ω
— Off Channel		10^{10}			★		Ω
INPUT CAPACITANCE — On Channel		20			★		pF
— Off Channel		20			★		pF
CMRR (20V, DC to 1KHz)	80	85		★	★		dB
CROSSTALK (20Vp-p, 1KHz) [1]		−85	−80		★	★	dB
FEED THROUGH (AT 1KHz) [1]		−85	−80		★	★	dB
OFFSET (channel to channel) G=1 [2]		30	100		★	★	μV
INPUT BIAS CURRENT/CHANNEL		1	5		★	★	nA
INPUT VOLTAGE RANGE [3]	+10	+11		★	★		V
	−10	−15		★	★		V
DIGITAL							
MULTIPLEXER INPUT CHANNEL SELECT — Logic '1' (2V)		5	30		★	★	μA
— Logic '0' (0.8V)		5	30		★	★	μA
S/H COMMAND — Logic '1' (2V)		0.2			★		nA
— Logic '0' (0.8V)		5	30		★	★	μA
ADC SECTION — Logic '1' (2.4V)			10			★	μA
— Logic '0' (0.8V)			10			★	μA
TRANSFER CHARACTERISTICS							
ACCURACY							
INTEGRAL LINEARITY [4]			±0.024			±0.012	% of FSR
DIFFERENTIAL LINEARITY [4]			±0.024			±0.012	% of FSR
GAIN ERROR [5] — G = 1		0.7			★		%
—G = 100		0.9			★		%
UNIPOLAR OFFSET ERROR [5]		16			★		mV
BIPOLAR OFFSET ERROR [5]		50			★		mV
NOISE ERROR (MEASURED AT S/H OUTPUT) G=1		0.5	1		★	★	mV p-p
DROOP RATE		50	500		★	★	uV/mS
TEMPERATURE COEFFICIENTS — Unipolar Offset			20			15	ppm of FSR/°C
— Bipolar Offset			30			25	ppm of FSR/°C
— Full-scale Calibration			60			35	ppm of FSR/°C
SYSTEM TIMINGS							
ADC CONVERSION TIME		20	25		★	★	μS
S/H APERTURE DELAY		50			★		nS
S/H APERTURE UNCERTAINTY		2			★		nS
TIMING							
ACQUISITION TIME		5			★		μS
(to 0.01% of final value for full scale step)							
THROUGHPUT (SERIAL MODE)			45			★	μS
(OVERLAP MODE)			30			★	μS
OUTPUT							
DIGITAL DATA							
OUTPUT CODES — Unipolar			UNIPOLAR STRAIGHT BINARY (USB)				
— Bipolar			BIPOLAR OFFSET BINARY (BOB)				
LOGIC LEVELS — Logic 0 (sink = 1.6mA)			+0.4			★	V
— Logic 1 (source = 500uA)	+2.4			★			V
LEAKAGE (DATA BITS ONLY), High-Z State	−5	0.1	+5	★	★	★	μA
POWER SUPPLY REQUIREMENTS							
RATED VOLTAGE, Analog (± Vcc)	14.25	15	15.75	★	★	★	VDC
Digital (VDD)	4.75	5	5.25	★	★	★	VDC
SUPPLY DRAIN, +15V		28	40		★	★	mA
−15V		36	45		★	★	mA
+5V		8	15		★	★	mA
POWER DISSIPATION		1	1.4		★	★	WATTS
TEMPERATURE RANGE							
OPERATING TEMPERATURE RANGE							
JH, KH/JL, KL	0		70	★		★	°C
AH, BH/AL, BL	−25		+85	★		★	°C
RH, SH/RL, BL	−55		+125	★		★	°C
STORAGE TEMPERATURE RANGE	−65		+150	★		★	°C

NOTES: [1] Measured at the sample and hold output. [2] Measured with all input channels grounded. [3] The range of voltage on any input with respect to common over which accuracy and leakage current is guaranteed. [4] Applicable over full operating temperature range. [5] Adjustable to zero using external potentiometer or select-on-test resistor. ★ Specification as per SDM862/863 J, A, R. NO MISSING CODES GUARANTEED OVER TEMPERATURE RANGE.

ABSOLUTE MAXIMUM RATINGS

+VCC TO ACOM ..... −0.5V TO +16V	ANALOG INPUT SIGNAL RANGE ..... + VCC + 20V TO − VCC − 20V
− VCC TO A COM ..... +0.5V TO −16V	DIGITAL INPUT SIGNAL ..... − 0.5V TO + VDD
+ VDD TO D COM ..... −0.5V TO +5.5V	ACOM TO DCOM ..... ± 1V

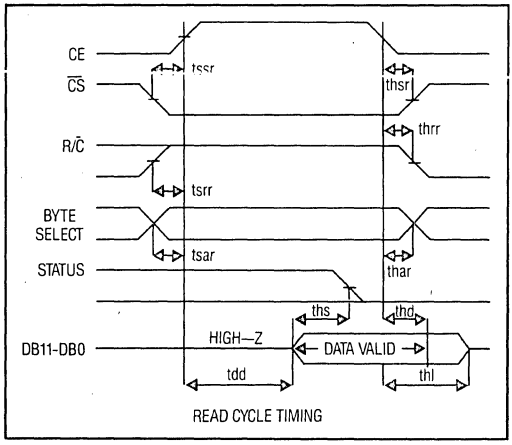
ANALOG TIMING SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
MULTIPLEXER				
Switching time (between channels)		+1.5		µS
Settling time (10V step to 0.02%)		2.5		µS
Enable time 'ON'		1	2	µS
'OFF'		0.25	0.5	µS
INSTRUMENTATION AMPLIFIER				
Settling time to 0.01%				
G=1		5	12.5	µS
G=10		3	7.5	µS
G=100		4	7.5	µS
Slew rate	12	17		V/µS
S/H AMPLIFIER				
Acquisition time (10V step to 0.01%)		5		µS
Aperture delay		50		nS
Hold mode settling time		1.5		µS
Slew rate		10		V/µS

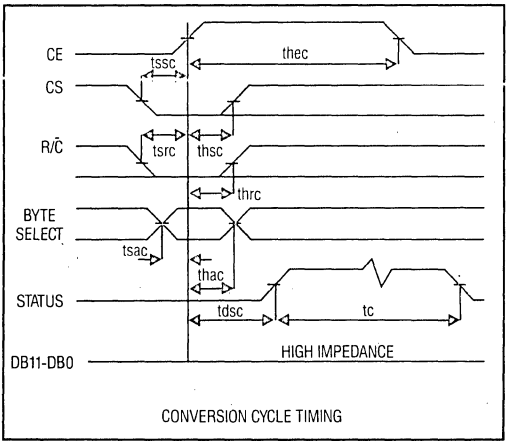
Note: Specifications are at +25°C and measured at 50% level of transition.

DIGITAL TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
tdsc	Status delay from CE		100	200	nS
thec	CE Pulse width	50	30		nS
tssc	$\overline{CS}$ to CE setup	50	20		nS
thsc	$\overline{CS}$ low during CE high	50	20		nS
tsrc	R/$\overline{C}$ to CE setup	50	0		nS
thrc	R/$\overline{C}$ low during CE high	50	20		nS
tsac	Byte select to CE setup	0	0		nS
thac	Byte selected valid during CE high	50	20		nS
tc	Conversion line, 12 bit cycle	15	20	25	µS
	8 bit cycle	10	13	17	µS
READ MODE					
tdd	Access time from CE		75	150	nS
thd	Data valid after CE low	25	35		nS
thl	Output float delay		100	150	nS
tssr	$\overline{CS}$ to CE setup	50	0		nS
tsrr	R/$\overline{C}$ to CE setup	0	0		nS
tsar	Byte select to CE setup	50	25		nS
thsr	$\overline{CS}$ valid after CE low	0	0		nS
thrr	R/$\overline{C}$ high after CE low	0	0		nS
thar	Byte select valid after CE low	50	25		nS
ths	Status delay after data valid	300	500	1000	nS



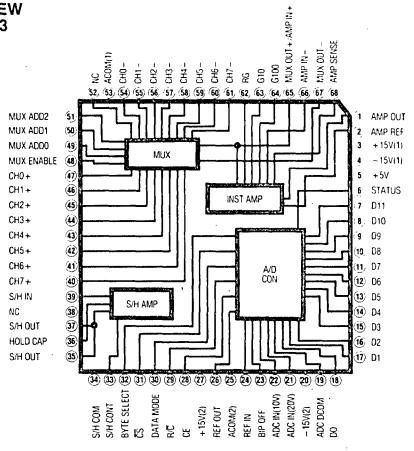
READ CYCLE TIMING



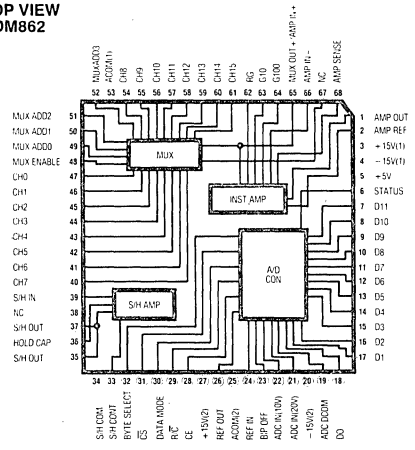
CONVERSION CYCLE TIMING

PIN CONFIGURATIONS

TOP VIEW
SDM863



TOP VIEW
SDM862



PIN DESIGNATION	DEFINITION	COMMENTS
CH0 to CH15 CH0 to CH7 (+,−) (PINS 40 to 47, 54 to 61)	Channel Inputs	Analog Inputs (Total 16) for single-ended and differential operation. Unused inputs must be connected to analog common.
MUX OUT+/AMP IN+ (PIN 65)	MULTIPLEXER "HI" OUTPUT	On the SDM862 this is the multiplexer output. On the SDM 863 it is the output of the positive selected inputs. It is connected internally to the positive input of the instrumentation amplifier.
MUXOUT (PIN 67)	MULTIPLEXER "LO" OUTPUT	This pin is used on the SDM863 only. It should be connected to the negative input of the instrumentation amplifier.
AMPIN (PIN 66)	Negative Input of Instrumentation Amplifier	On the SDM862 this should be connected to analog common. On the SDM863 it should be conencted to Muxout—(Pin 67).
AMPOUT (PIN 1)	Output of instrumentation amplifier	This pin should be connected to the input of the S/H amplifier (Pin 39).
AMP SENSE (PIN 68)	Output sense line of instrumentaiton amplifier	This pin will normally be connected direct to A input (Pin 1)
AMP REF (PIN 2)	Reference for amplifier output	This pin will normally be connected to analog common. Care should be taken to minimise tracking and contact resistance to analog common to optimise system accuracy.
S/H OUT (PINS 35/37)	Output of sample/hold amplifier	Two pins are provided to facilitate a guard ring around the hold capacitor pin. These pins should be connected to either ADC in (20V) or ADC in (10V) depending on the desired range.
HOLD CAP (PIN 36)	Connection for hold capacitor on S/H amplifier	The tracking to the hold capacitor should be as short as possible and a guard ring employed using Pins 35 and 37.
ADC IN (20V) ADC IN (10V) (PINS 21, 22)	Inputs to A/D convertor	Connect to S/H amplifier output. Use appropriate Pin for desired range.
RG, G10, G100 (PINS 62, 63, 64)	Gain setting Pins on instrumentation amplifier	For Gain = 1, no connections For Gain = 10, connect G10 to RG. For Gain = 100, connect G100 to RG.
REF OUT (PIN 26)	10V Reference voltage	This is the reference voltage for the A/D convertor.
REF IN, BIP OFF (PINS 24, 23)	Reference input and offset input to A/D convertor	Connect trim potentiometers (or select-on-test resistors) to these pins for unipolar or biploar operation as shown in figure 4.
S/H IN (PIN 39)	Input to sample/hold amplifier	Connect to amp out (Pin 1).
MUX ENABLE (PIN 48)	Multiplex enable/disable	Logic '1' on this pin will enable a selected channel on the internal multiplexer. Logic '0' de-selects all channels.
MUX ADD0 to MUX ADD3 (PINS 49 to 52)	Address inputs for channel selection	These address lines select a particular channel as specified in figure 2.
S/H CONT (PIN 33)	Track/Hold control on S/H amplifier	Logic '1' holds an analog value for conversion by the A/D convertor. This line may be controlled by the status (Pin 6) of the convertor to simplify external timing control.
S/H COM (PIN 34)	Reference for S/H logic control	Connect to digital common
D0 to D11 (PINS 7 to 18)	3-state digital outputs	The 12 or 8-bit result of a conversion is available as output on these pins (DO-LSB, D11-MSB).
STATUS (PIN 6)	Status of A/D conversion	This output pin is at logic '1' while the internal A/D convertor is carrying out a conversion. This pin may be used to directly control the S/H amplifier.
CE (PIN 28)	Chip enable	This input must be at logic '1' to either initiate a conversion or read output data (see figure 1).
$C\overline{S}$ (PIN 31)	Chip select	This input must be at logic '0' to either initiate a conversion or read output data (see figure 1).
$R/\overline{C}$ (PIN 29)	Read/convert	Data can be read when this Pin is logic '1' or a conversion can be initiated when this Pin is logic '0'. This Pin is typically connected to the $R/\overline{W}$ control line of a microprocessor—bases system (see figure 1).
DATA MODE (PIN 30)	Select 12 or 8 Bit Data	When data mode is at logic '1' all 12 output data bits are enabled simultaneously. When data mode is at logic '0' MSB's AND LSB's are controlled by byte select (Pin 32).
BYTE SELECT (PIN 32)	Byte address, short cycle	When reading output data, byte select at logic '0' enables the 8 MSB's. Byte select at logic '1' enables the 4 LSB's. The 4 LSB's can therefore be connected to four of the MSB lines for inter-connection to an 8-bit bus. In start convert mode, logic '0' enables a 12-bit conversion while logic '1' will short cycle the conversion to 8-bits (see figure 1).
+15V(1), +15V(2) (PINS 3, 27)	Power Supply	Connect to +15V supply using decoupling as indicated in figure 5.
−15V(1), −15V(2) (PINS, 4, 20)	Power Supply	Connect to −15V supply using decoupling as indicated in figure 5.
A COM (1), A COM (2) (PINS 53, 25)	Analog common	Analog common connection. Note that a common (including digital common) should be connected together at one point close to the device.
+5V (PIN 5)	Logic power supply	Connect to +5V digital supply line with decoupling as indicated in figure 5.
ADC DCOM (PIN 19)	Reference for A/D convertor control lines	Connect to S/H commmon at one point close to device.
NC (PIN 38)	No internal connection	

CE	$\overline{CS}$	R/$\overline{C}$	DATA MODE	BYTE SELECT	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	↑	0	0	Ebable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

FIGURE 1. CONTROL INPUT TRUTH TABLE

RANGE	–FS + 1/2 LSB (000 TO 001 TRANSITION)	+FS – 1/2 LSB (FFE TO FFF TRANSITION)	1 LSB EQUALS
0–10V	+0.0012V	+9.9963V	2.44 mV
±5V	–4.9988V	+4.9963V	2.44 mV
±10V	–9.9976V	+9.9927V	4.88 mV

FIGURE 3. CODE TRANSITION RANGES

SDM862						SDM863				
MUX ADD3	MUX ADD2	MUX ADD1	MUX ADD0	MUX ENABLE	CHANNEL SELECTED	MUX ADD2	MUX ADD1	MUX ADD0	MUX ENABLE	CHANNEL PAIR SELECTED
X	X	X	X	L	NONE	X	X	X	L	NONE
L	L	L	L	H	0	L	L	L	H	0
L	L	L	H	H	1	L	L	H	H	1
L	L	H	L	H	2	L	H	L	H	2
L	L	H	H	H	3	L	H	H	H	3
L	H	L	L	H	4	H	L	L	H	4
L	H	L	H	H	5	H	L	H	H	5
L	H	H	L	H	6	H	H	L	H	6
L	H	H	H	H	7	H	H	H	H	7
H	L	L	L	H	8			–		
H	L	L	H	H	9			–		
H	L	H	L	H	10			–		
H	L	H	H	H	11			–		
H	H	L	L	H	12			–		
H	H	L	H	H	13			–		
H	H	H	L	H	14			–		
H	H	H	H	H	15			–		

FIGURE 2. CHANNEL SELECT TRUTH TABLE

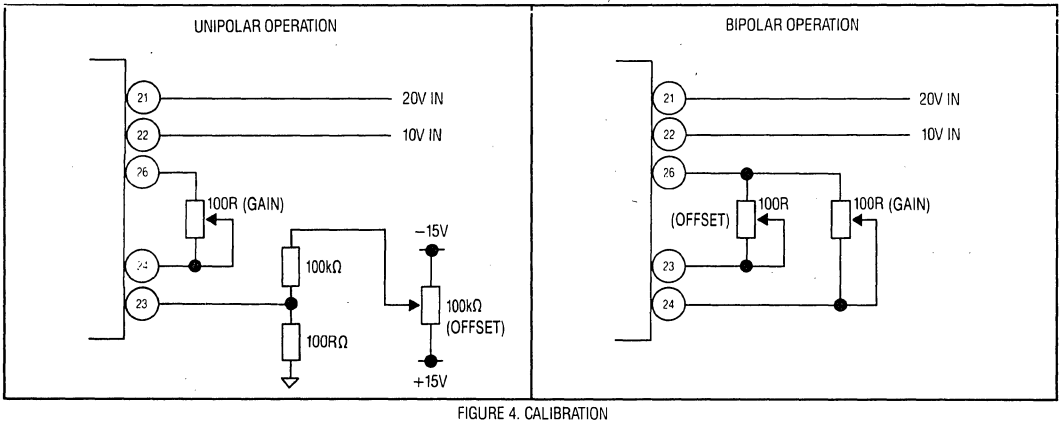


FIGURE 4. CALIBRATION

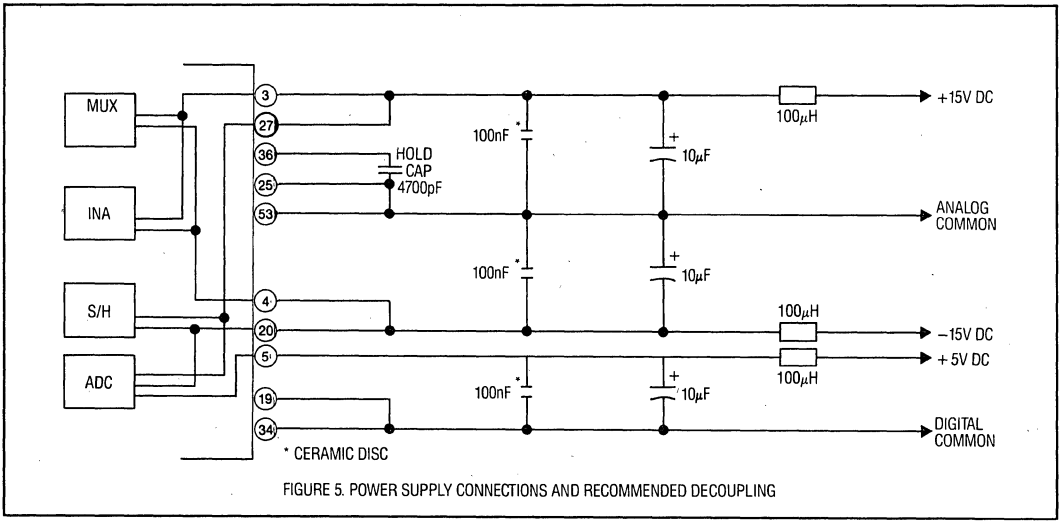
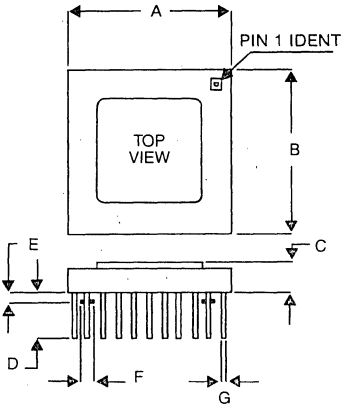


FIGURE 5. POWER SUPPLY CONNECTIONS AND RECOMMENDED DECOUPLING

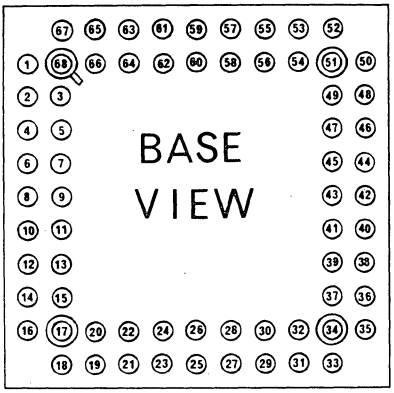
P.G.A. MECHANICAL OUTLINE



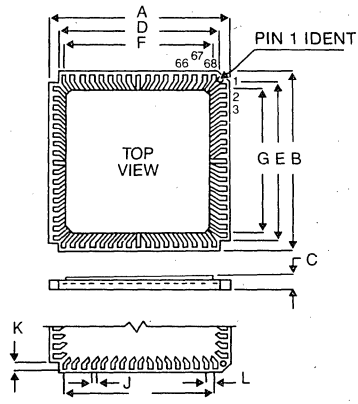
H PACKAGE

Terminations: Gold plated KOVAR.
Case: Black ceramic with gold plated nickel lid.
Hermeticity: Gross leak test.
Weight: 9 grms (0.32oz)

	INCHES		MILLIMETRES	
DIM	MIN	MAX	MIN	MAX
A	1.087	1.109	27.610	28.169
B	1.087	1.109	27.610	28.169
C	.095	.120	2.413	3.048
D	.162	.198	4.115	5.029
E	.045	.055	1.143	1.397
F	.045	.055	1.143	1.397
G	.016	.020	.406	.508
H	.100 BASIC		2.540 BASIC	
J	.100 BASIC		2.540 BASIC	



L.C.C. MECHANICAL OUTLINE



L PACKAGE

Terminations: Gold plated nickel on refractory metallization.
Case: White ceramic with gold plated nickel lid.
Hermeticity: Gross leak test.
Weight: 4.2 grams (0.15oz)

	INCHES		MILLIMETRES	
DIM	MIN	MAX	MIN	MAX
A	.945	.965	24.003	24.511
B	.945	.965	24.003	24.511
C	.076	.094	1.934	2.388
D	.841	.859	21.361	21.819
E	.841	.859	21.361	21.819
F	.755	.785	19.177	19.939
G	.755	.785	19.177	19.939
H	.800 BASIC		20.320 BASIC	
J	.027	.033	.686	.838
K	.045 BASIC		1.143 BASIC	
L	.050 BASIC		1.270 BASIC	

ORDERING INFORMATION*

SDM 862 16 SINGLE ENDED INPUTS					SDM 863 8 DIFFERENTIAL INPUTS				
GRADE	68 PIN PACKAGE		ACCURACY % FSR	TEMP. RANGE (DEG. C)	GRADE	68 PIN PACKAGE		ACCURACY % FSR	TEMP. RANGE (DEG. C)
	LCC	PGA				LCC	PGA		
J	L	H	±0.024	0–70	J	L	H	±0.024	0–70
K	L	H	±0.012	0–70	K	L	H	±0.012	0–70
A	L	H	±0.024	–25 +85	A	L	H	±0.024	–25 +85
B	L	H	±0.012	–25 +85	B	L	H	±0.012	–25 +85
R	L	H	±0.024	–55 +125	R	L	H	±0.024	–55 +125
S	L	H	±0.012	–55 +125	S	L	H	±0.012	–55 +125

*i.e. 16 single ended inputs in LCC with accuracy of 0.024% FSR and Temp Range of 0–70 Deg. C = SDM 862 JL.

NOTES

1. J, K, A, B Grades are burned in AT+85°C for a minimum of 48 hrs.
   R.S. Grades are burned in AT+125°C for a minimum of 48 hrs.
2. All units are supplied serialised and with a printout of their electrical test results (25°C).

SDM 862/863 evaluation board part number: PC 862/863—1
68 Pin L.C.C. Socket Part Number: MC 0068—1

WHY REINVENT AN OPERATOR INTERFACE?

Is your microprocessor-based equipment used or serviced by human beings? If so, you may be interested in a new line of operator interface terminals from Burr-Brown. The operator interface provides the way for an operator to setup and run equipment; it may also provide diagnostic/service access for a repairman.

For most new products, the operator interface is custom designed because no off-the-shelf product has been available which adequately addresses this need. This means that engineering resources are needed, which will place an additional demand on already limited manpower. The availability now of commercial/industrial operator interfaces allows companies to concentrate their resources in the area of their greatest expertise, and therefore, to get the best return on engineering investment.

Operator interfaces are used in a variety of equipment. There are numerous controller applications such as machine controllers, motor controllers, process controllers, HVAC controllers, programmable controllers, and motion controllers. Other applications include operator interface for instruments, test machines, data acquisition systems, weighing systems, imaging systems, and medical equipment.

Consider these issues when looking for an operator interface:

Display—Is it easily readable in your operating environment?

Keyboard—Is the tactile response appropriate for your needs? Can the keys be clearly marked for your application?

Operation—Will the units operate in a mode that is convenient in your application?

Communications—What interface do you need? RS-232C is a good choice for many applications. RS-422 is useful for distances of greater than 50 feet or for electrically noisy environments.

Package—Will the package fit into your equipment, aesthetically and physically? Is it easy to mount? Does the package need to be sealed?

Environment—Under what conditions must the unit operate?

Burr-Brown has recently introduced a line of operator interface terminals, the TM2500 and the TM2700, which uses standard ASCII communications. They are low cost, easy-to-use, easy-to-design-in units. In many applications it is no longer necessary to design an expensive long-lead-time custom operator interface. These units provide a large liquid-crystal display with a wide viewing angle. The terminals go through an automatic self-test every time power is applied. The keyboard offers excellent tactile response, providing a numeric keypad, six user-programmable function keys, and six control keys. The function keys are back-lighted under host computer control. They can also be programmed to transmit any sequence of up to four characters. Each function key has a label area adjoining it so that the user can easily customize each key.

The terminals operate in one of three modes. In character mode, a character is transmitted as each key is pressed. The character may be echoed to the display as defined. In the block mode, all characters are internally buffered and displayed as keys are pressed. The entire line of data is then transmitted when the enter key is pressed. The polled mode is the third way to operate these units. In the polled mode, data is entered as in the block mode; however, the data is not transmitted until the host processor requests it. Another option in this mode is to assign each terminal an address so that a number of terminals may be committed to the same host interface line.

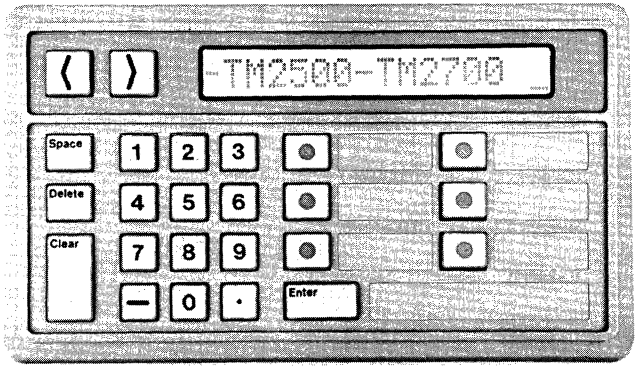
Other options include baud rate, line termination, turnaround delay, display viewing angle, hand check protocol, local echo, key repeat, and key click. All options are user selectable and stored in nonvolatile EEPROM.

The TM2500 is available with an RS-232C interface, while the TM2700 is provided with an RS-422 interface.

These microterminals provide an easy-to-use, off-the-shelf interface in many new equipment designs.

BURR-BROWN®

TM2500
TM2700



OEM MICROTERMINALS

BENEFITS/FEATURES

- MINIMIZES DEVELOPMENT TIME AND EXPENSE
- LARGE, HIGH CONTRAST 16-CHARACTER LCD DISPLAY
- 80-CHARACTER DISPLAY BUFFER
- SIX PROGRAMMABLE BACKLIT FUNCTION KEYS
- POSITIVE TACTILE FEEDBACK KEYBOARD
- EASILY CUSTOMIZED LABELS
- ADJUSTABLE VIEWING ANGLE
- NONVOLATILE CONFIGURATION STORAGE
- POWERUP SELF-TEST
- ALL OPTIONS USER-SELECTABLE

APPLICATIONS

- OPERATOR PANEL
- SERVICE/DIAGNOSTIC DEVICE
- DATA COLLECTION TERMINAL

DESCRIPTION

The TM2500/TM2700 are low cost, compact, industrial data entry and display terminals. They are designed to be used as operator panels, as well as service and diagnostic equipment. The terminals can also be used as a simple keyboard entry data collection terminal. The TM2500 and TM2700 are similar units, differing only in communications interface—RS-232C on the TM2500 and RS-422 on the TM2700.

Both terminals are lightweight, 10.5 ounces, and are enclosed within a 4.102″ × 7.102″ × 1.060″ case. The terminals have six backlit programmable function keys. Space is provided to customize the keyboard and function keys with company logos and function labels. The compact size of the TM2500/TM2700 makes them ideal for applications where space is at a premium.

The TM2700 is recommended for electrically noisy environments, multidrop applications, and where communication distances of more than 50 feet are required. Fifteen command sequences are used by the host to control these terminals. Burr-Brown's 25 years of experience in developing and producing OEM products has ensured that the design of the TM2500/TM2700 is focused on the needs of potential and existing customers.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

KEYBOARD

A numeric keypad with six programmable function keys is provided for operator input. The keys are widely spaced for ease of entry. The silicon rubber keyboard provides environmental sealing with good tactile feedback. A unique characteristic of the keyboard is that each function key is backlit. The backlighting is under host computer control to give maximum flexibility to the operator. The keyboard also features key click and key repeat functions. If an invalid key is pressed, the terminal responds with an audible tone.

DISPLAY

The display is a 16-character LCD with large, easy to read characters. An 80-character display buffer with scroll keys allows the operator to slide the 16-character window across the 80-character line. The high contrast display on the terminals provides sufficient alphanumeric display capability for most panel-mount applications.

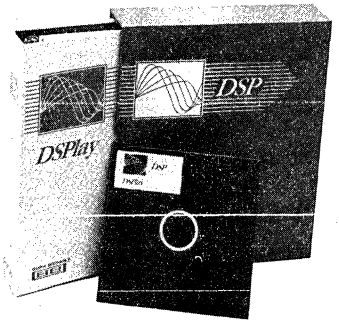
CASE

The case for the TM2500/TM2700 is designed for either surface or recessed mounting. The keyboard and display are sealed in the ABS plastic case so that when properly mounted, the terminal is protected against dust and moisture.

SPECIFICATIONS

Display	16-character alphanumeric LCD with adjustable viewing angle
Character Size	0.38″ (9.66mm) character height
Display Buffer	80 characters
Keyboard	Sealed molded silicon rubber
Scrolling Keys	Two, manual
Keypad	Numeric
Number of Keys	24
Operation Life	1,000,000 operations
Function Keys	Six, programmable, backlit
Indicators	Audible tone, flashing display, 6 LEDs
Communications	TM2500—RS-232C, point-to-point; TM2700—RS-422, multidrop up to 32 terminals
Power	5VDC or 7.5 to 10VDC at 250mA max, TM2500 350mA max, TM2700
Baud Rate	300, 1200, 9600
Modes	Character and block
Operating Temperature	0°C to +50°C (32° F to 122° F)
Storage Temperature	−20°C to +70°C (−4° F to +158° F)
Dimensions	4.102″ × 7.102″ × 1.060″
Weight	10.5 ounces
Mounting	Flush or surface mounted
Case	Dust and moisture sealed ABS plastic

DSPlay™



The *DSPlay* product family is designed to assist those involved in the analysis of real-world signals by simplifying the implementation of digital signal processing (DSP). Typical applications include vibration analysis; process, medical and analytical instrumentation; audio, sonar and voice signal processing; and test or quality control applications.

The *DSPlay* Software Package transforms the IBM® PC/XT/AT or compatible into an easy-to-use DSP workstation, even for the nonexpert. *DSPlay* Software features a menu-driven interface with pull-up lists to process, analyze, and display real-world signals. Built-in editor functions make program development and modification simple; and, the package utilizes a concept familiar to the user for program development—the block diagram approach.

Each block represents a process function such as correlation, signal source, filter or FFT operation. Once the program is developed, *DSPlay* offers three different ways to view the data. The "Windows" display provides an overview of up to six signal windows. The "Active" display allows a concentrated examination of one signal window, and the "Landscape" display offers a comparison of signal frames by presenting a series in 3-D perspective.

DSPlay requires 512k bytes memory, one double-sided floppy drive, and an IBM color graphics board for operation.

The execution time of *DSPlay* Software may be enhanced by implementing *DSPlay* XL™. Using a powerful accelerator board, the software's performance is improved by two orders of magnitude (typically). Even higher performance improvements can be achieved in operations requiring numerous sequential calculations—for example, where large filters or transforms are processed frequently.

DSPlay XL is slated for introduction in the fourth quarter of 1987.

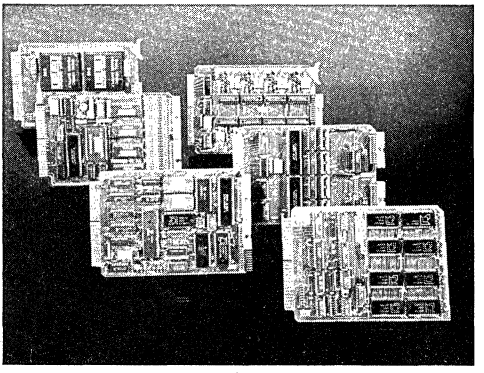
For more information about *DSPlay* products, contact the factory at 602-741-1155 or write DSP Marketing, Burr-Brown Corporation, 6550 S. Bay Colony, Tucson, AZ 85706.

DSPlay™, *DSPlay* XL™, Burr-Brown Corp.; IBM® IBM Corp.

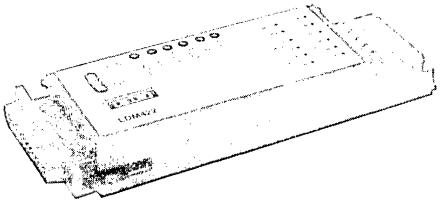
STD BUS INDUSTRIAL I/O PRODUCTS

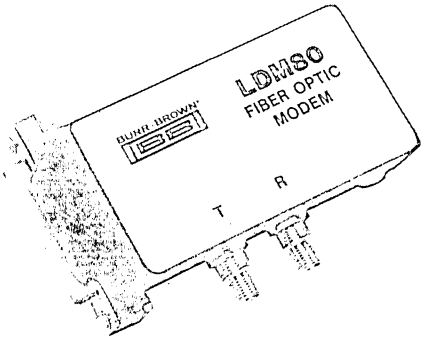
The Burr-Brown STD Bus products provide the most cost-effective tool for solving the application-oriented problems of process control and system integration.

The modularity and simplicity offered by this well-defined standard have led to the development of a complete line of STD Bus products. The line includes a disk controller and operating system, a Z80 CPU with onboard DMA, various memory boards, a 32-channel 12-bit A/D converter, two CRT controllers, an IEEE-488 interface card, and two types of discrete I/O cards.



DATA COMMUNICATIONS PRODUCTS





Burr-Brown Data Communications products provide the most cost-effective tool for solving the local data communications problems for industrial and institutional facilities.

Limited Distance and Fiber Optic Modems provide extension of RS-232 ports up to several miles. In addition, electrical isolation for wire units is provided by transformers and optical couplers, eliminating ground loops, equipment damage, and noise pickup. Surge suppression devices are internally mounted on all field inputs and outputs. The LDM422 serves as a Limited Distance Modem and as an RS-232-to-RS-422 converter with multipoint capability. It has two complete high speed transmit and receive channels for data and handshake. It features 1000V isolation and surge protection.

Fiber optic modems offer the maximum in isolation and EMI/RFI immunity. The LDM80 is signal powered from RS-232 ports and transmits up to 3.5km at 19.2k bits per second. The LDM85 is a unique multipoint-capable modem with data rates to 5M bits per second.

Other products include:

- LDM35—Signal-Powered Limited-Distance Modem
- LDM70—High Speed Ruggedized Industrial Modem
- APA120—Personal-Computer-Based Protocol Analyzer.

NORTH AMERICAN SALES DIRECTORY

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Prices in U.S. dollars | F.O.B. Tucson, Arizona | Quantity discounts available. | Effective June 1, 1987

MODEL	FOOT NOTE	1-24	25-99	100-249
0100MS		14.98	12.74	10.34
0145MC		5.21	4.43	3.78
0546		104.00	99.00	96.00
0548MC		28.00	27.00	26.00
0700		50.00	48.00	46.00
0700M		53.00	51.00	49.00
0700U		44.00	43.00	41.00
0700UM		60.00	58.00	56.00
0710		121.00	117.00	112.00
0722		52.96	40.77	36.23
0722BG		67.59	53.14	47.09
0722MG		60.87	47.03	40.74
0724		73.85	56.86	50.98
0803HS		4.20	3.24	2.84
0803MC		5.75	4.43	4.04
0804HS		5.61	4.32	3.94
0805HS		25.25	19.44	
0807HS		1.54	1.19	1.00
2014MC		17.00	14.00	11.00
2020MC		9.00	7.00	6.00
2026MC		39.00	32.00	26.00
2302MC		9.00	8.60	8.20
2350MC		14.00	13.50	13.00
2525MC		28.00	23.00	19.00
3291/14		125.00	120.00	115.00
3292/14		125.00	120.00	115.00
3293/14		125.00	120.00	115.00
3329/03		43.23	35.64	25.20
3354/25		165.00	159.00	152.00
3355/25		133.00	128.00	123.00
3356/25		125.00	120.00	115.00
3450		280.00	269.00	258.00
3451		228.00	219.00	210.00
3452		240.00	230.00	221.00
3500A		11.54	8.80	6.72
3500B		19.71	15.61	11.39
3500C		25.14	20.14	14.91
3500E		40.60	30.24	23.36
3500MP		40.60	30.24	23.36
3500R		23.80	17.93	13.13
3500R/883B	+	40.00	36.00	34.00
3500RQ		32.40	25.00	18.90
3500S		36.96	27.27	22.26
3500SQ		52.48	38.72	31.60
3500T		59.64	44.28	35.28
3500TQ		82.72	62.87	50.40
3500U/883B	+	30.00	26.00	24.00
3501S		28.56	22.41	17.80
3507J		13.05	10.42	8.72
3507JQ		19.43	15.07	12.97
3508J		11.48	8.91	7.77
3510AM		10.47	8.10	6.25
3510BM		13.27	10.15	7.82
3510CM		20.44	15.39	12.18
3510SM		20.44	15.39	12.18
3510VM/883B	+	70.00	60.00	50.00
3521H		27.65	21.65	16.49
3521J		39.50	28.80	22.31
3521JQ		52.00	38.55	30.87
3521K		59.30	43.20	35.96
3521L		83.50	61.45	49.35
3521R		97.00	76.50	58.49
3521RQ		137.75	105.65	86.78
3522J		20.60	16.00	12.34
3522K		27.00	21.55	16.80
3522L		37.78	28.10	22.16
3522S		53.40	41.50	31.34
3522SQ		71.15	57.80	45.83
3523J		38.50	29.20	22.73
3523JQ		50.75	41.20	33.08
3523K		45.80	36.00	28.93
3523L		54.90	42.00	33.39
3523LQ		73.85	60.65	51.40
3527AM		18.20	13.72	11.50
3527AMQ		24.42	18.52	15.59
3527BM		24.36	17.82	15.38
3527BMQ		29.96	23.81	20.21
3527CM		37.13	28.89	24.47
3528AM		22.68	17.12	13.60
3528AMQ		30.30	23.27	18.32
3528BM		27.83	20.90	18.43
3528BMQ		36.96	28.03	24.78
3528CM		33.88	26.08	23.00
3528CMQ		45.86	36.34	30.45
3550J		34.94	27.00	22.52
3550K		44.52	33.75	26.78
3550S		64.74	50.60	37.49
3550SQ		87.36	69.66	53.55
3551J		35.62	27.27	22.52
3551S		62.89	49.95	37.49
3551SQ		78.40	64.80	51.45
3553AM		40.32	31.21	23.57

CUSTOMER PRICE LIST--COMPONENT PRODUCTS

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MODEL	FOOT NOTE	1-24	25-99	100-249
3553AMQ		63.84	54.00	46.20
3554AM		77.35	60.00	50.09
3554AMQ		95.50	76.96	68.25
3554BM		88.85	73.50	58.96
3554BMQ		111.30	93.60	80.85
3554SM		105.00	88.00	73.50
3554SMQ		145.60	118.80	99.23
3571AM		81.14	58.32	50.40
3571AMQ		109.76	85.32	72.45
3572AM		92.96	69.12	57.23
3572AMQ		125.44	99.36	81.90
3573AM		40.32	28.62	26.25
3573AMQ		54.88	42.12	36.75
3580J		65.72	49.40	42.25
3580JQ		94.35	72.30	60.75
3581J		99.05	72.65	62.85
3582J		107.60	90.90	73.15
3582JQ		143.00	123.75	107.15
3583AM		106.00	88.40	72.10
3583AMQ		148.40	122.75	106.10
3583JM		97.85	83.20	66.95
3584JM		100.00	75.40	67.45
3584JMQ		136.75	113.35	100.95
3606AG		117.60	102.60	91.35
3606BG		153.44	136.62	119.54
3627AM		14.00	10.64	9.61
3627AMQ		28.00	17.55	14.18
3627BM		18.76	13.61	11.81
3627BMQ		36.40	21.60	17.59
3650HG		63.00	46.22	35.44
3650JG		81.93	59.56	49.04
3650KG		99.57	81.38	68.25
3650MG		56.45	39.53	33.60
3652HG		81.93	61.94	49.04
3652JG		99.57	75.28	67.20
3652MG		64.12	51.03	44.94
3656AG		96.71	74.52	60.74
3656BG		119.56	92.18	81.74
3656HG		85.40	65.88	53.55
3656JG		91.06	70.20	57.23
3656KG		111.94	86.35	70.30
4025MC		39.00	32.00	26.00
4085BM		91.84	79.38	61.95
4085KG		79.52	65.50	51.98
4085SM		115.36	102.06	79.28
4115/04		74.26	56.70	51.19
4127JG		56.84	42.55	36.12
4127KG		65.46	53.41	46.10
4203J		43.50	29.15	21.55
4203K		59.58	47.90	38.30
4203S		92.40	66.10	58.30
4203SQ		122.40	91.85	81.40
4204J		76.16	64.75	53.55
4204K		99.40	85.91	67.73
4204S		113.12	101.52	86.10
4204SQ		150.08	139.32	121.80
4205J		35.78	28.08	20.95
4205K		52.08	40.88	31.76
4205S		74.42	56.16	42.00
4205SQ		98.95	77.60	59.48
4206J		54.26	43.15	31.76
4206K		77.06	61.18	44.36
4213AL		34.20	27.10	21.95
4213AL-BS		34.20	27.10	21.95
4213AL-BSS1		112.86	89.43	72.44
4213AL-BSS2		44.46	35.23	28.54
4213AL-BSS3		39.33	31.17	25.24
4213AL-BSS4		37.62	29.81	24.15
4213AM		31.15	24.40	19.50
4213AM-BS		31.15	24.40	19.50
4213AM-BSS1		104.61	81.18	64.19
4213AM-BSS2		40.50	31.72	25.35
4213AM-BSS3		35.82	28.06	22.43
4213AM-BSS4		34.27	26.84	21.45
4213AMQ		38.90	31.85	26.25
4213BL		48.40	37.50	31.65
4213BL-BS		48.40	37.50	31.65
4213BL-BSS1		159.72	123.75	104.45
4213BL-BSS2		62.92	48.75	41.15
4213BL-BSS3		55.66	43.13	36.40
4213BL-BSS4		53.24	41.25	34.82
4213BM		45.05	34.75	29.15
4213BM-BS		45.05	34.75	29.15
4213BM-BSS1		151.47	115.50	96.20
4213BM-BSS2		58.57	45.18	37.90
4213BM-BSS3		51.81	39.96	33.52
4213BM-BSS4		49.56	38.23	32.07
4213SL		61.90	51.75	41.40
4213SL-BS		61.90	51.75	41.40
4213SL-BSS1		204.27	170.78	136.62
4213SL-BSS2		80.47	67.28	53.82
4213SL-BSS3		71.19	59.51	47.61

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4213SL-BSS4		68.09	56.93	45.54
4213SM		58.30	48.80	38.90
4213SM-BS		58.30	48.80	38.90
4213SM-BSS1		196.02	162.53	128.37
4213SM-BSS2		75.79	63.44	50.57
4213SM-BSS3		62.04	56.12	44.74
4213SM-BSS4		64.13	53.68	42.79
4213UM		31.00	26.00	23.00
4213UM/883B	+	43.00	37.00	29.00
4213VM		45.00	39.00	31.00
4213VM/883B	+	60.49	38.00	35.00
4213WM		60.00	60.00	49.00
4213WM/883B	+	75.00	62.00	48.00
4214AP		28.28	22.95	17.64
4214BP		41.94	33.70	28.35
4214RM		34.16	26.95	24.52
4214SM		55.33	45.36	38.59
4302		58.86	42.88	33.76
4340		108.90	79.95	70.65
4341		32.70	25.97	18.85
4423		27.10	21.06	17.48
8300201XC		170.00	163.00	155.00
AD515JH		19.04	14.31	9.98
AD515JL		19.50	15.75	12.00
AD515KH		25.48	19.71	14.54
AD515KL		25.25	20.75	16.35
AD515LH		31.36	24.30	18.90
AD515LL		30.50	25.00	20.50
ADC10HT		577.50	477.75	414.75
ADC574AJH		45.00	36.00	30.00
ADC574AKH		59.00	47.20	39.50
ADC574ASH		124.00	99.00	91.35
ADC574ATH		177.00	141.00	118.50
ADC600B	C		2375.00	2090.00
ADC600K	C		1695.00	1495.00
ADC674AJH		58.50	46.75	39.25
ADC674AKH		75.00	60.00	50.25
ADC674ASH		158.00	126.00	106.00
ADC674ATH		228.00	182.00	153.00
ADC71JG		98.70	86.10	66.15
ADC71KG		122.85	107.10	81.90
ADC72AM		239.40	203.70	156.45
ADC72BM		298.20	254.10	195.30
ADC72JM		199.50	170.10	131.25
ADC72KM		249.90	212.10	162.75
ADC76AM		281.40	224.70	193.20
ADC76BM		330.75	264.60	226.80
ADC76JG		156.45	135.45	103.95
ADC76JM		193.20	154.35	132.30
ADC76KG		179.55	153.30	124.95
ADC76KM		242.55	194.25	165.90
ADC803BM		239.00	199.00	162.00
ADC803BMQ		321.00	256.00	205.00
ADC803CM		292.00	225.00	180.00
ADC803CMQ		369.00	293.00	234.00
ADC803SM		382.00	304.00	243.00
ADC803SMQ		502.00	399.00	319.00
ADC804BH		66.15	47.25	40.95
ADC804BHQ		102.90	72.45	57.75
ADC804SH		124.95	87.15	69.30
ADC804SHQ		156.45	109.20	87.15
ADC80AG-10		83.48	66.15	46.20
ADC80AG-12		85.05	67.20	46.73
ADC80AG-12Q		110.25	88.20	60.90
ADC80AGZ-12		85.05	67.20	46.73
ADC80H-AH-12		85.05	67.20	46.73
ADC80H-AH-12Q		110.25	88.20	60.90
ADC80KD	E,O		33.00	33.00
ADC80MAH-12		52.00	42.00	35.00
ADC80MAH-12/QM		67.00	54.00	45.00
ADC82AG		78.75	54.60	46.20
ADC82AM		113.40	78.75	66.15
ADC82AMQ		153.30	115.50	105.00
ADC84KG-10		92.40	73.50	61.95
ADC84KG-12		97.65	77.70	65.10
ADC85-10		158.55	143.85	103.95
ADC85-12		179.55	144.90	110.25
ADC85H-12		131.25	105.00	88.20
ADC85HQ-12		163.80	131.25	110.25
ADC87		119.00	102.00	94.00
ADC87/883B	+	130.00	113.00	105.00
ADC87H-12		173.25	138.60	115.50
ADC87HQ-12		216.30	173.25	143.85
ADC87U		110.00	94.00	91.00
ADC87U/883B	+	121.00	104.00	96.00
ADC87V		119.00	102.00	94.00
ADC87V/883B	+	130.00	113.00	105.00
DAC10HT		355.95	241.50	178.50
DAC1200KP-V		9.50	9.50	5.95
DAC1201KP-V		11.20	11.20	6.95
DAC1600JP-V		15.10	14.35	8.95
DAC1600KP-V		16.70	15.95	9.95

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DAC60-10		155.00	149.00	143.00
DAC60-12		165.00	159.00	152.00
DAC63BG		121.80	97.65	91.35
DAC63BM		141.75	117.60	107.10
DAC63CG		137.55	109.20	101.85
DAC63CM		160.65	131.25	117.60
DAC63SM		252.00	210.00	192.15
DAC63TM		276.15	234.15	212.10
DAC700BH		60.90	48.30	40.95
DAC700BH/QM		73.50	55.65	47.25
DAC700BL		95.55	72.45	61.95
DAC700BL/QM		109.20	82.95	71.40
DAC700CH		88.20	67.20	56.70
DAC700KH		48.30	36.75	30.45
DAC700LH		71.40	54.60	46.20
DAC700SH		92.40	70.35	58.80
DAC700SH/QM		107.10	80.85	68.25
DAC700SL		154.35	122.85	103.95
DAC700SL/QM		177.45	140.70	119.70
DAC701BH		60.90	48.30	40.95
DAC701BH/QM		73.50	55.65	47.25
DAC701BL		95.55	72.45	61.95
DAC701BL/QM		109.20	82.95	71.40
DAC701CH		88.20	67.20	56.70
DAC701KH		48.30	36.75	30.45
DAC701LH		71.40	54.60	46.20
DAC701SH		92.40	70.35	58.80
DAC701SH/QM		107.10	80.85	68.25
DAC701SL		154.35	122.85	103.95
DAC701SL/QM		177.45	140.70	119.70
DAC702BH		60.90	48.30	40.95
DAC702BH/QM		73.50	55.65	47.25
DAC702BL		95.55	72.45	61.95
DAC702BL/QM		109.20	82.95	71.40
DAC702CH		88.20	67.20	56.70
DAC702JP		23.10	19.58	17.85
DAC702KH		48.30	36.75	30.45
DAC702KP		25.20	21.95	19.95
DAC702LH		71.40	54.60	46.20
DAC702SH		92.40	70.35	58.80
DAC702SH/QM		107.10	80.85	68.25
DAC702SL		154.35	122.85	103.95
DAC702SL/QM		177.45	140.70	119.70
DAC703BH		60.90	48.30	40.95
DAC703BH/QM		73.50	55.65	47.25
DAC703BL		95.55	72.45	61.95
DAC703BL/QM		109.20	82.95	71.40
DAC703CH		88.20	67.20	56.70
DAC703JP		23.10	19.58	17.85
DAC703KH		48.30	36.75	30.45
DAC703KP		25.20	22.03	19.95
DAC703LH		71.40	54.60	46.20
DAC703SH		92.40	70.35	58.80
DAC703SH/QM		107.10	80.85	68.25
DAC703SL		154.35	122.85	103.95
DAC703SL/QM		177.45	140.70	119.70
DAC703VG	I	102.00	77.00	64.50
DAC703VG/883B	I	118.50	89.00	75.00
DAC703VL	I	143.50	108.00	90.00
DAC703VL/883B	I	165.50	125.00	105.00
DAC705BH		76.65	72.45	56.70
DAC705BH/QM		88.20	82.95	65.10
DAC705KH		66.15	53.55	46.20
DAC705SH		99.75	97.65	77.17
DAC705SH/QM		114.45	108.15	89.30
DAC706BH		76.65	72.45	59.54
DAC706BH/QM		88.20	82.95	68.36
DAC706KH		66.15	53.55	48.51
DAC706SH		99.75	93.45	77.17
DAC706SH/QM		114.45	108.15	89.30
DAC707BH		76.65	72.45	59.54
DAC707BH/QM		88.20	82.95	65.10
DAC707JP		27.30	21.53	18.37
DAC707KH		66.15	53.55	46.20
DAC707KP		32.55	25.73	22.05
DAC707SH		99.75	93.45	73.50
DAC707SH/QM		114.45	108.15	85.05
DAC708BH		76.65	72.45	56.70
DAC708BH/QM		88.20	82.95	65.10
DAC708KH		66.15	53.55	46.20
DAC708SH		99.75	93.45	73.50
DAC708SH/QM		114.45	108.15	85.05
DAC709BH		76.65	72.45	56.70
DAC709BH/QM		88.20	82.95	65.10
DAC709KH		66.15	53.55	46.20
DAC709SH		99.75	93.45	73.50
DAC709SH/QM		114.45	108.15	85.05
DAC70BH-COB-I		150.15	113.40	94.50
DAC70BH-CSB-I		150.15	113.40	94.50
DAC71-CCD-I		67.10	52.80	46.20
DAC71-CCD-V		70.40	57.20	52.80
DAC71-COB-I		56.70	44.10	38.85

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DAC71-COB-V		59.85	47.25	40.95
DAC71-CSB-I		56.70	44.10	38.85
DAC71-CSB-V		59.85	47.25	40.95
DAC710KH		42.00	35.70	30.45
DAC711KH		42.00	35.70	30.45
DAC72BH-COB-I		87.15	66.15	53.55
DAC72BH-COB-V		90.30	70.14	55.65
DAC72BH-CSB-I		87.15	66.15	53.55
DAC72BH-CSB-V		90.30	69.30	55.65
DAC736J		375.00	360.00	345.00
DAC736K		415.00	399.00	382.00
DAC73J		373.00	358.00	344.00
DAC73K		412.00	396.00	380.00
DAC7541AAH		13.10	10.75	7.95
DAC7541AAH/QM		16.20	12.70	9.30
DAC7541ABH		14.45	11.85	8.75
DAC7541ABH/QM		17.90	14.10	10.20
DAC7541AJP		11.80	9.70	7.15
DAC7541AJU		14.15	11.65	8.55
DAC7541AKP		13.10	10.75	7.95
DAC7541AKU		15.70	12.90	9.55
DAC7541ASH		38.35	31.35	23.25
DAC7541ASH/QM		57.00	44.70	32.60
DAC7541ATH		44.75	36.60	27.10
DAC7541ATH/QM		66.50	52.20	38.00
DAC7700KD	E		25.20	18.37
DAC7701KD	E		25.20	18.37
DAC80-CBI-I		23.00	18.25	15.25
DAC80-CBI-V		24.00	19.00	16.00
DAC80-CCD-I		42.00	37.50	25.00
DAC80-CCD-V		42.50	38.00	26.00
DAC800-CBI-I		24.15	19.95	15.75
DAC800-CBI-V		28.87	24.15	18.90
DAC800P-CBI-I		21.26	17.01	14.33
DAC800P-CBI-V		26.25	22.05	16.80
DAC80KD-I	E		15.25	9.60
DAC80KD-V	E		15.25	9.60
DAC80P-CBI-I		20.00	16.00	13.25
DAC80P-CBI-V		21.00	16.37	14.00
DAC80Z-CBI-I		23.00	18.25	15.25
DAC80Z-CBI-V		24.00	19.00	16.00
DAC811AH		23.25	18.35	14.90
DAC811AH/QM		29.15	23.00	18.75
DAC811AL		29.25	23.25	19.40
DAC811AL/QM		36.75	29.25	24.25
DAC811BH		28.50	22.50	18.90
DAC811BH/QM		35.75	28.25	23.75
DAC811BL		37.00	29.25	24.60
DAC811BL/QM		46.50	37.00	31.00
DAC811JD	E		15.25	9.60
DAC811JP		18.60	14.90	11.90
DAC811JU		20.50	16.40	13.50
DAC811KP		24.75	19.80	15.85
DAC811KU		26.50	21.20	17.20
DAC811RH		79.00	63.00	53.00
DAC811RH/QM		91.00	73.00	61.00
DAC811RL		103.00	82.00	69.00
DAC811RL/QM		119.00	95.00	80.00
DAC811SH		130.00	106.00	86.00
DAC811SH/QM		150.00	122.00	99.00
DAC811SL		169.00	138.00	112.00
DAC811SL/QM		195.00	159.00	129.00
DAC812BM		137.55	126.00	96.60
DAC812CM		183.75	139.65	127.05
DAC82KG		40.95	28.35	24.15
DAC850-CBI-I		38.12	27.30	23.10
DAC850-CBI-I/QM		47.36	34.12	28.87
DAC850-CBI-V		40.43	29.40	24.68
DAC850-CBI-V/QM		50.82	36.75	30.98
DAC850BL-I		49.35	35.70	30.45
DAC850BL-I/QM		62.37	45.15	38.33
DAC850BL-V		53.03	37.80	32.02
DAC850BL-V/QM		66.99	47.25	40.43
DAC851-CBI-I		56.59	40.95	34.65
DAC851-CBI-I/QM		65.20	47.25	39.90
DAC851-CBI-V		61.21	44.62	37.27
DAC851-CBI-V/QM		70.36	51.45	43.05
DAC851SL-I		74.03	53.55	45.15
DAC851SL-I/QM		85.58	61.95	51.98
DAC851SL-V		79.80	58.80	48.30
DAC851SL-V/QM		91.35	67.20	55.65
DAC85H-CBI-I		36.23	28.87	25.20
DAC85H-CBI-I/QM		44.10	35.18	30.98
DAC85H-CBI-V		37.80	30.45	26.25
DAC85H-CBI-V/QM		46.20	35.18	32.02
DAC87-CBI-I	J			
DAC87-CBI-I/B	J,+			
DAC87-CBI-V		98.00	78.50	70.50
DAC87-CBI-V/B	+	105.00	85.00	76.50
DAC870U		45.00	40.00	35.00
DAC870U/883B	+	65.00	60.00	55.00
DAC870UL		50.00	45.00	40.00

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DAC870UL/883B	+	70.00	65.00	60.00
DAC870V		80.00	75.00	67.00
DAC870V/883B	+	100.00	95.00	80.00
DAC870VL		85.00	80.00	72.00
DAC870VL/883B	+	105.00	100.00	90.00
DAC87H-CBI-V		82.95	66.15	57.75
DAC87H-CBI-V/QM		100.80	80.85	70.35
DAC87U-CBI-I	J			
DAC87U-CBI-I/B	J,+			
DAC87U-CBI-V		58.00	48.80	44.00
DAC87U-CBI-V/B	+	61.00	49.50	47.00
DAC90BG		25.30	20.12	16.96
DAC90SG		35.07	28.06	23.46
DEM102 KIT		75.00		
DEM106 KIT		85.00		
DIV100HP		33.88	26.19	19.06
DIV100JP		47.32	39.15	29.14
DIV100KP		67.59	56.11	41.84
INA101AD			8.90	4.95
INA101AG		17.95	13.50	11.00
INA101AL		16.50	13.00	9.75
INA101AL-BS		16.50	13.00	9.75
INA101AL-BSS1		54.45	42.90	32.18
INA101AL-BSS2		21.45	16.90	12.68
INA101AL-BSS3		18.98	14.95	11.21
INA101AL-BSS4		18.15	14.30	10.73
INA101AM		14.00	10.50	7.25
INA101AM-BS		14.00	10.50	7.25
INA101AM-BSS1		46.20	34.65	23.93
INA101AM-BSS2		18.20	13.65	9.43
INA101AM-BSS3		16.10	12.08	8.34
INA101AM-BSS4		15.40	11.55	7.98
INA101BL		19.50	15.25	11.30
INA101BL-BS		19.50	15.25	11.30
INA101BL-BSS1		64.35	50.33	37.29
INA101BL-BSS2		25.35	19.83	14.69
INA101BL-BSS3		22.43	17.54	13.00
INA101BL-BSS4		21.45	16.78	12.43
INA101BM-BS		18.70	17.00	16.15
INA101BM-BSS1		56.10	42.08	29.04
INA101BM-BSS2		24.31	22.10	21.00
INA101BM-BSS3		21.51	19.55	18.57
INA101BM-BSS4		20.57	18.70	17.77
INA101CG		23.00	17.25	16.35
INA101CL		20.90	16.30	15.35
INA101CL-BS		20.90	16.30	15.35
INA101CL-BSS1		68.97	53.79	50.66
INA101CL-BSS2		27.17	21.19	19.96
INA101CL-BSS3		24.04	18.75	17.65
INA101CL-BSS4		22.99	17.93	16.89
INA101CM		20.61	14.90	13.49
INA101CM-BS		20.61	14.90	13.49
INA101CM-BSS1		60.72	45.54	42.14
INA101CM-BSS2		26.79	19.37	17.54
INA101CM-BSS3		23.70	17.14	15.51
INA101CM-BSS4		22.67	16.39	14.84
INA101HP		7.37	5.67	5.10
INA101KU		8.29	6.26	5.51
INA101SG		27.72	19.98	18.53
INA101SGQ		39.20	29.16	26.25
INA101SL		22.00	17.15	16.45
INA101SL-BS		22.00	17.15	16.45
INA101SL-BSS1		72.60	56.60	54.29
INA101SL-BSS2		28.60	22.30	21.39
INA101SL-BSS3		25.30	19.72	18.92
INA101SL-BSS4		24.20	18.87	18.10
INA101SM		21.84	15.82	14.65
INA101SM-BS		21.84	15.82	14.65
INA101SM-BSS1		64.35	48.35	46.04
INA101SM-BSS2		28.39	20.57	19.05
INA101SM-BSS3		25.12	18.19	16.85
INA101SM-BSS4		24.02	17.40	16.12
INA101SMQ		31.36	22.68	21.00
INA101VG	I	46.00	41.60	39.50
INA101VG/883B	I	49.50	44.75	42.50
INA101VM	I	43.75	39.50	37.50
INA101VM/883B	I	47.25	42.50	40.50
INA102AD			9.35	5.20
INA102AG		13.95	11.15	7.95
INA102AL		16.45	13.65	10.45
INA102CG		20.61	17.12	11.92
INA102CL		20.90	18.35	13.85
INA102KP		7.60	5.95	5.40
INA102SL		26.40	23.10	17.25
INA104AM		27.16	20.79	18.85
INA104BM		32.48	25.11	22.73
INA104CM		41.94	32.24	29.24
INA104HP		21.00	16.15	14.65
INA104JP		25.20	19.39	17.59
INA104KP		32.48	25.11	22.73
INA104SM		44.80	34.29	31.13
INA105AD			4.65	3.50

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MODEL	FOOT NOTE	1-24	25-99	100-249
INA105AL		12.45	9.95	8.45
INA105AM		9.50	7.15	5.75
INA105AM-BS		9.50	7.15	5.75
INA105AM-BSS1		32.84	24.59	19.64
INA105AM-BSS2		12.35	9.30	7.48
INA105AM-BSS3		10.93	8.22	6.61
INA105AM-BSS4		10.45	7.87	6.33
INA105BL		15.25	12.00	10.15
INA105BM		11.85	8.95	7.20
INA105BM-BS		11.85	8.95	7.20
INA105BM-BSS1		42.08	31.35	25.25
INA105BM-BSS2		15.41	11.64	9.36
INA105BM-BSS3		13.63	10.29	8.28
INA105BM-BSS4		13.04	9.85	7.92
INA105KP		6.25	4.65	3.50
INA105KU		7.34	5.35	3.99
INA105SL		19.10	14.85	12.45
INA106AM		10.00	7.50	6.05
INA106BM		12.45	9.40	7.55
INA106KP		6.50	4.89	3.65
INA110AD			9.45	5.25
INA110AG		16.85	12.65	8.85
INA110AL		19.35	15.15	11.35
INA110BG		26.43	19.17	12.97
INA110BL		26.10	20.25	14.85
INA110KP		7.40	5.80	5.50
INA110KU		8.74	6.59	6.09
INA110SG		28.11	20.36	18.85
INA110SL		27.60	21.35	20.45
INA258UG		38.15	36.00	26.50
INA258UG/883B	+	42.40	40.30	29.70
INA258UL		41.35	39.20	28.60
INA258UL/883B	+	45.60	43.50	32.86
INA258VG		49.80	43.45	40.30
INA258VG/883B	+	65.70	58.30	56.20
INA258VL		54.00	47.70	44.50
INA258VL/883B	+	74.20	64.65	61.50
INA258WG		63.60	55.10	51.95
INA258WG/883B	+	84.80	74.20	69.95
INA258WL		69.95	60.40	56.20
INA258WL/883B	+	93.30	81.60	76.30
ISO100AP		36.40	31.05	26.78
ISO100BP		39.65	34.13	30.08
ISO100CP		44.24	39.20	35.28
ISO102		25.50	19.50	16.50
ISO102B		34.45	26.95	22.30
ISO106		34.00	26.60	22.00
ISO106B		45.90	35.95	29.75
LOG100JP		48.16	37.80	31.50
MA51414				
MP22BG		340.20	271.95	227.85
MP32BG		340.20	271.95	227.85
MP32CG		425.25	340.20	285.60
MPC16S		24.37	21.06	17.85
MPC4D		13.62	11.81	9.97
MPC800KG		29.25	24.21	20.18
MPC800SG		58.45	48.37	40.31
MPC801KG		15.23	12.60	10.50
MPC801SG		31.50	26.07	21.72
MPC8D		24.37	21.06	17.85
MPC8S		13.62	11.77	9.97
MPY100AG		15.51	13.94	12.26
MPY100AL		13.85	12.45	10.00
MPY100AL-BS		13.85	12.45	10.00
MPY100AL-BSS1		45.71	41.09	30.00
MPY100AL-BSS2		18.01	16.19	13.00
MPY100AL-BSS3		15.93	14.32	11.50
MPY100AL-BSS4		15.24	13.70	11.00
MPY100AM		11.76	10.58	8.40
MPY100AM-BS		11.76	10.58	8.40
MPY100AM-BSS1		37.46	32.84	24.75
MPY100AM-BSS2		15.29	13.75	10.92
MPY100AM-BSS3		13.52	12.17	9.66
MPY100AM-BSS4		12.94	11.64	9.24
MPY100BG		25.14	22.09	17.22
MPY100BL		20.85	18.75	14.15
MPY100BL-BS		20.85	18.75	14.15
MPY100BL-BSS1		68.81	61.88	46.70
MPY100BL-BSS2		27.11	24.38	18.40
MPY100BL-BSS3		23.98	21.56	16.27
MPY100BL-BSS4		22.94	20.63	15.57
MPY100BM		19.04	16.69	12.23
MPY100BM-BS		19.04	16.69	12.23
MPY100BM-BSS1		60.56	53.63	38.45
MPY100BM-BSS2		24.75	21.70	15.90
MPY100BM-BSS3		21.90	19.19	14.06
MPY100BM-BSS4		20.94	18.36	13.45
MPY100CG		37.74	33.48	27.56
MPY100CL		30.50	27.35	23.00
MPY100CL-BS		30.50	27.35	23.00
MPY100CL-BSS1		100.65	90.26	75.90
MPY100CL-BSS2		39.65	35.56	29.90

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MODEL	FOOT NOTE	1-24	25-99	100-249
MPY100CL-BSS3		35.08	31.45	26.45
MPY100CL-BSS4		33.55	30.09	25.30
MPY100CM		28.56	25.33	20.95
MPY100CM-BS		28.56	25.30	20.95
MPY100CM-BSS1		92.40	82.01	67.65
MPY100CM-BSS2		37.13	32.89	27.24
MPY100CM-BSS3		32.84	29.10	24.09
MPY100CM-BSS4		31.42	27.83	23.05
MPY100SG		56.62	50.22	33.60
MPY100SGQ		77.28	67.50	48.83
MPY100SL		44.50	39.45	30.50
MPY100SL-BS		44.50	39.45	30.50
MPY100SL-BSS1		146.85	130.19	100.65
MPY100SL-BSS2		57.85	51.29	39.65
MPY100SL-BSS3		51.18	45.37	35.08
MPY100SL-BSS4		48.95	43.40	33.55
MPY100SM		42.84	38.02	28.61
MPY100SM-BS		42.84	38.02	28.61
MPY100SM-BSS1		138.60	121.94	92.40
MPY100SM-BSS2		55.69	49.43	37.19
MPY100SM-BSS3		49.27	43.72	32.90
MPY100SM-BSS4		47.12	41.82	31.47
MPY100SMQ		58.24	51.30	43.05
MPY534AD			12.57	9.38
MPY534JD		32.98	27.67	19.77
MPY534JH		25.37	21.18	15.16
MPY534JH-BS		25.37	21.18	15.16
MPY534JH-BSS1		74.42	59.23	42.41
MPY534JH-BSS2		32.98	27.53	19.71
MPY534JH-BSS3		29.18	24.36	17.43
MPY534JH-BSS4		27.91	23.30	16.68
MPY534JL		25.05	20.45	15.35
MPY534JL-BS		25.05	20.45	15.35
MPY534JL-BSS1		82.67	67.49	50.66
MPY534JL-BSS2		32.57	26.59	19.96
MPY534JL-BSS3		28.81	23.52	17.65
MPY534JL-BSS4		27.56	22.50	16.89
MPY534KD		47.14	39.94	29.09
MPY534KH		38.76	32.27	23.42
MPY534KH-BS		38.76	32.27	23.42
MPY534KH-BSS1		113.85	90.26	65.51
MPY534KH-BSS2		50.39	41.95	30.45
MPY534KH-BSS3		44.57	37.11	26.93
MPY534KH-BSS4		42.64	35.50	25.76
MPY534KL		37.00	29.85	22.35
MPY534KL-BS		37.00	29.85	22.35
MPY534KL-BSS1		122.10	98.51	73.76
MPY534KL-BSS2		48.10	38.81	29.06
MPY534KL-BSS3		42.55	34.33	25.70
MPY534KL-BSS4		40.70	32.84	24.59
MPY534LD		70.45	58.23	43.48
MPY534LH		57.23	47.14	34.81
MPY534LH-BS		57.23	47.14	34.81
MPY534LH-BSS1		168.14	131.84	97.35
MPY534LH-BSS2		74.40	61.28	45.25
MPY534LH-BSS3		65.81	54.21	40.03
MPY534LH-BSS4		62.95	51.85	38.29
MPY534LL		53.45	42.45	32.00
MPY534LL-BS		53.45	42.45	32.00
MPY534LL-BSS1		176.39	140.09	105.60
MPY534LL-BSS2		69.49	55.19	41.60
MPY534LL-BSS3		61.47	48.82	36.80
MPY534LL-BSS4		58.80	46.70	35.20
MPY534SD		89.50	74.28	55.46
MPY534SH		76.41	62.95	47.02
MPY534SH-BS		76.41	62.95	47.02
MPY534SH-BSS1		224.24	176.06	131.51
MPY534SH-BSS2		99.33	81.84	61.13
MPY534SH-BSS3		87.87	72.39	54.07
MPY534SH-BSS4		84.05	69.25	51.72
MPY534SL		70.45	55.85	42.35
MPY534SL-BS		70.45	55.85	42.35
MPY534SL-BSS1		232.49	184.31	139.76
MPY534SL-BSS2		91.59	72.61	55.06
MPY534SL-BSS3		81.02	64.23	48.70
MPY534SL-BSS4		77.50	61.44	46.59
MPY534TD		107.40	89.50	64.00
MPY534TH		91.80	76.50	54.50
MPY534TH-BS		91.80	76.50	54.50
MPY534TH-BSS1		317.39	252.45	179.85
MPY534TH-BSS2		119.34	99.45	70.85
MPY534TH-BSS3		105.57	87.98	62.68
MPY534TH-BSS4		100.98	84.15	59.95
MPY534TL		98.68	79.00	57.00
MPY534TL-BS		98.68	79.00	57.00
MPY534TL-BSS1		325.64	260.70	188.10
MPY534TL-BSS2		128.28	102.70	74.10
MPY534TL-BSS3		113.48	90.85	65.55
MPY534TL-BSS4		108.55	86.90	62.70
MPY634AL		20.00	16.35	12.45
MPY634AL-BS		20.00	16.35	12.45
MPY634AL-BSS1		66.00	53.95	41.09

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MODEL	FOOT NOTE	1-24	25-99	100-249
MPY634AL-BSS2		26.00	21.26	16.19
MPY634AL-BSS3		23.00	18.80	14.32
MPY634AL-BSS4		22.00	17.99	13.70
MPY634AM		18.65	14.96	10.45
MPY634AM-BS		18.65	14.96	10.45
MPY634AM-BSS1		57.75	45.71	32.84
MPY634AM-BSS2		24.25	19.45	13.59
MPY634AM-BSS3		21.45	17.20	12.02
MPY634AM-BSS4		20.52	16.45	11.50
MPY634BL		28.45	23.05	17.75
MPY634BL-BS		28.45	23.05	17.75
MPY634BL-BSS1		93.89	76.07	58.58
MPY634BL-BSS2		36.99	29.97	23.08
MPY634BL-BSS3		32.72	26.51	20.41
MPY634BL-BSS4		31.30	25.36	19.53
MPY634BM		27.72	22.19	16.01
MPY634BM-BS		27.72	22.19	16.01
MPY634BM-BSS1		85.64	67.82	50.33
MPY634BM-BSS2		36.04	28.85	20.81
MPY634BM-BSS3		31.88	25.52	18.41
MPY634BM-BSS4		30.49	24.41	17.61
MPY634KP		14.39	11.50	8.35
MPY634SL		65.15	52.35	40.35
MPY634SL-BS		65.15	52.35	40.35
MPY634SL-BSS1		214.99	172.76	133.16
MPY634SL-BSS2		84.70	68.06	52.46
MPY634SL-BSS3		74.92	60.20	46.40
MPY634SL-BSS4		71.67	57.59	44.39
MPY634SM		66.81	53.84	39.74
MPY634SM-BS		66.81	53.84	39.74
MPY634SM-BSS1		206.75	164.51	124.91
MPY634SM-BSS2		86.85	69.99	51.66
MPY634SM-BSS3		76.83	61.92	45.70
MPY634SM-BSS4		73.49	59.22	43.71
0245MC		6.05	5.05	4.85
OPA101AM		42.00	33.45	25.60
OPA101BM		52.20	42.00	36.00
OPA102AM		44.40	35.56	26.70
OPA102BM		54.00	43.30	36.85
OPA103AM		11.76	9.29	7.14
OPA103BM		15.90	12.37	9.40
OPA103CM		20.83	16.04	12.13
OPA103DM		33.43	25.76	19.43
OPA104AM		19.60	15.07	10.76
OPA104BM		26.49	20.47	15.23
OPA104CM		33.04	25.38	19.95

MODEL	FOOT NOTE	1-24	25-99	100-249
OPA105UM		27.00	23.50	22.00
OPA105UM/883B	+	32.00	28.00	25.00
OPA105VM		37.00	32.00	30.00
OPA105VM/883B	+	50.00	44.00	40.00
OPA105WM		47.00	42.00	40.25
OPA105WM/883B	+	68.00	59.00	52.00
OPA106UM		30.00	25.00	22.00
OPA106UM/883B	+	36.00	32.00	28.00
OPA106VM		40.00	35.00	32.00
OPA106VM/883B	+	55.00	49.00	44.00
OPA106WM		52.00	45.00	42.00
OPA106WM/883B	+	72.00	63.00	57.00
OPA111AD			7.29	4.04
OPA111AL		12.25	10.45	7.95
OPA111AL-BS		12.25	10.45	7.95
OPA111AL-BSS1		40.43	34.49	26.24
OPA111AL-BSS2		15.93	13.59	10.34
OPA111AL-BSS3		14.09	12.02	9.14
OPA111AL-BSS4		13.48	11.50	8.75
OPA111AM		10.92	8.59	5.72
OPA111AM-BS		10.92	8.59	5.72
OPA111AM-BSS1		32.18	26.24	17.99
OPA111AM-BSS2		14.20	11.17	7.44
OPA111AM-BSS3		12.56	9.88	6.58
OPA111AM-BSS4		12.01	9.45	6.29
OPA111BL		17.85	14.75	12.45
OPA111BL-BS		17.85	14.75	12.45
OPA111BL-BSS1		58.90	48.68	41.09
OPA111BL-BSS2		23.21	19.18	16.19
OPA111BL-BSS3		20.53	16.96	14.32
OPA111BL-BSS4		19.64	16.23	13.70
OPA111BM		17.19	13.23	10.45
OPA111BM-BS		17.19	13.23	10.45
OPA111BM-BSS1		50.66	40.43	32.84
OPA111BM-BSS2		22.35	17.20	13.59
OPA111BM-BSS3		19.77	15.21	12.02
OPA111BM-BSS4		18.91	14.55	11.50
OPA111HT		63.30	50.70	40.70
OPA111SL		19.35	16.45	14.45
OPA111SL-BS		19.35	16.45	14.45
OPA111SL-BSS1		63.86	54.29	47.69
OPA111SL-BSS2		25.16	21.39	18.79
OPA111SL-BSS3		22.25	18.92	16.62
OPA111SL-BSS4		21.29	18.10	15.90
OPA111SM		20.25	15.65	13.15
OPA111SM-BS		20.25	15.65	13.15

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MODEL	FOOT NOTE	1-24	25-99	100-249
OPA111SM-BSS1		55.61	46.04	39.44
OPA111SM-BSS2		26.33	20.35	17.10
OPA111SM-BSS3		23.29	18.00	15.12
OPA111SM-BSS4		22.28	17.22	14.47
OPA111SMQ		27.30	21.85	17.55
OPA111VM	I	26.00	20.50	17.00
OPA111VM/883B	I	35.00	30.00	27.00
OPA11HT		58.80	52.15	43.15
OPA121KL		9.35	7.00	5.90
OPA121KL-BS		9.35	7.00	5.90
OPA121KL-BSS1		30.86	23.10	19.47
OPA121KL-BSS2		12.16	9.10	7.67
OPA121KL-BSS3		10.75	8.05	6.79
OPA121KL-BSS4		10.29	7.70	6.49
OPA121KM		6.85	4.50	3.40
OPA121KM-BS		6.85	4.50	3.40
OPA121KM-BSS1		22.61	14.85	11.22
OPA121KM-BSS2		8.91	5.85	4.42
OPA121KM-BSS3		7.88	5.18	3.91
OPA121KM-BSS4		7.54	4.95	3.74
OPA121KP		5.65	3.65	2.75
OPA121KU		7.78	4.27	3.20
OPA121SL		15.05	11.55	8.75
OPA121SL-BS		15.05	11.55	8.75
OPA121SL-BSS1		49.67	38.12	28.88
OPA121SL-BSS2		19.57	15.02	11.38
OPA121SL-BSS3		17.31	13.28	10.06
OPA121SL-BSS4		16.56	12.71	9.63
OPA121SM-BS		12.55	9.05	6.25
OPA121SM-BSS1		41.42	29.87	20.63
OPA121SM-BSS2		16.32	11.77	8.13
OPA121SM-BSS3		14.43	10.41	7.19
OPA121SM-BSS4		13.81	9.96	6.88
OPA128JD			14.58	8.66
OPA128JL		20.00	16.45	12.75
OPA128JL-BS		20.00	16.45	12.75
OPA128JL-BSS1		66.00	54.29	42.08
OPA128JL-BSS2		26.00	21.39	16.58
OPA128JL-BSS3		23.00	18.92	14.66
OPA128JL-BSS4		22.00	18.10	14.03
OPA128JM		21.25	16.95	12.50
OPA128JM-BS		21.25	16.95	12.50
OPA128JM-BSS1		57.75	46.04	33.83
OPA128JM-BSS2		27.63	22.04	16.25
OPA128JM-BSS3		24.44	19.49	14.38
OPA128JM-BSS4		23.38	18.65	13.75
OPA128KL		27.50	22.50	18.00
OPA128KL-BS		27.50	22.50	18.00
OPA128KL-BSS1		90.75	74.25	59.40
OPA128KL-BSS2		35.75	29.25	23.40
OPA128KL-BSS3		31.63	25.88	20.70
OPA128KL-BSS4		30.25	24.75	19.80
OPA128KM		32.80	25.75	19.50
OPA128KM-BS		32.80	25.75	19.50
OPA128KM-BSS1		82.50	66.00	51.15
OPA128KM-BSS2		42.64	33.48	25.35
OPA128KM-BSS3		37.72	29.61	22.43
OPA128KM-BSS4		36.08	28.33	21.45
OPA128LL		34.00	27.50	22.50
OPA128LL-BS		34.00	27.50	22.50
OPA128LL-BSS1		112.20	90.75	74.25
OPA128LL-BSS2		44.20	35.75	29.25
OPA128LL-BSS3		39.10	31.63	25.88
OPA128LL-BSS4		37.40	30.25	24.75
OPA128LM		41.38	32.02	25.15
OPA128LM-BS		41.38	32.02	25.15
OPA128LM-BSS1		103.95	82.50	66.00
OPA128LM-BSS2		53.79	41.63	32.70
OPA128LM-BSS3		47.59	36.82	28.92
OPA128LM-BSS4		45.52	35.22	27.67
OPA128SL		56.75	47.45	41.00
OPA128SL-BS		56.75	47.45	41.00
OPA128SL-BSS1		187.28	156.59	135.30
OPA128SL-BSS2		73.78	61.69	53.30
OPA128SL-BSS3		65.26	54.57	47.15
OPA128SL-BSS4		62.43	52.20	45.10
OPA128SM		60.76	48.55	40.43
OPA128SM-BS		60.76	48.55	40.43
OPA128SM-BSS1		179.03	148.34	127.05
OPA128SM-BSS2		78.99	63.12	52.56
OPA128SM-BSS3		69.87	55.83	46.49
OPA128SM-BSS4		66.84	53.41	44.47
OPA156AM		12.60	9.67	7.09
OPA201AG		9.00	6.30	4.35
OPA201BG		14.00	9.80	6.80
OPA201CG		16.75	11.70	8.20
OPA201SG		18.30	12.05	9.00
OPA2111AD			10.75	7.30
OPA2111AL		18.15	14.45	12.45
OPA2111AM		16.24	12.42	10.45
OPA2111BL		29.50	24.20	19.35
OPA2111BM		29.06	22.52	17.33

CUSTOMER PRICE LIST—COMPONENT PRODUCTS

Prices in U.S. dollars | F.O.B. Tucson, Arizona | Quantity discounts available. | Effective June 1, 1987

MODEL	FOOT NOTE	1-24	25-99	100-249
OPA2111KM		9.90	7.90	5.25
OPA2111KP		7.90	5.50	4.25
OPA2111SL		31.15	24.50	19.60
OPA2111SM		29.68	22.90	17.59
OPA21EZ		10.02	7.72	6.25
OPA21GZ		4.98	3.89	3.10
OPA27AJ		19.95	15.65	12.50
OPA27AJ-BS		19.95	15.65	12.50
OPA27AJ-BSS1		70.46	53.63	41.25
OPA27AJ-BSS2		25.94	20.35	16.25
OPA27AJ-BSS3		22.94	18.00	14.38
OPA27AJ-BSS4		21.95	17.22	13.75
OPA27AJQ		32.85	25.00	18.75
OPA27AL		23.85	18.75	15.00
OPA27AL-BS		23.85	18.75	15.00
OPA27AL-BSS1		78.71	61.88	49.50
OPA27AL-BSS2		31.01	24.38	19.50
OPA27AL-BSS3		27.43	21.56	17.25
OPA27AL-BSS4		26.24	20.63	16.50
OPA27AZ		19.95	15.65	12.50
OPA27AZQ		32.85	25.00	18.75
OPA27BJ		12.85	9.65	7.65
OPA27BJ-BS		12.85	9.65	7.65
OPA27BJ-BSS1		45.38	33.00	25.25
OPA27BJ-BSS2		16.71	12.55	9.95
OPA27BJ-BSS3		14.78	11.10	8.80
OPA27BJ-BSS4		14.14	10.62	8.42
OPA27BJQ		21.20	15.45	11.85
OPA27BL		16.25	12.50	10.15
OPA27BL-BS		16.25	12.50	10.15
OPA27BL-BSS1		53.63	41.25	33.50
OPA27BL-BSS2		21.13	16.25	13.20
OPA27BL-BSS3		18.69	14.38	11.67
OPA27BL-BSS4		17.88	13.75	11.17
OPA27BZ		12.85	9.65	7.65
OPA27BZQ		21.20	15.45	11.85
OPA27CD			6.30	4.20
OPA27CJ		9.95	7.50	5.95
OPA27CJ-BS		9.95	7.50	5.95
OPA27CJ-BSS1		35.15	25.74	19.64
OPA27CJ-BSS2		12.94	9.75	7.74
OPA27CJ-BSS3		11.44	8.63	6.84
OPA27CJ-BSS4		10.95	8.25	6.55
OPA27CJQ		16.45	12.00	9.25
OPA27CL		13.15	10.30	8.45
OPA27CL-BS		13.15	10.30	8.45
OPA27CL-BSS1		43.40	33.99	27.89
OPA27CL-BSS2		17.10	13.39	10.99
OPA27CL-BSS3		15.12	11.84	9.72
OPA27CL-BSS4		14.47	11.33	9.30
OPA27CZ		9.95	7.50	5.95
OPA27CZQ		16.45	12.00	9.25
OPA27EJ		11.00	8.35	6.65
OPA27EJ-BS		11.00	8.35	6.65
OPA27EJ-BSS1		38.78	28.71	21.95
OPA27EJ-BSS2		14.30	10.86	8.65
OPA27EJ-BSS3		12.65	9.60	7.65
OPA27EJ-BSS4		12.10	9.19	7.32
OPA27EL		14.25	11.20	9.15
OPA27EL-BS		14.25	11.20	9.15
OPA27EL-BSS1		47.03	36.96	30.20
OPA27EL-BSS2		18.53	14.56	11.90
OPA27EL-BSS3		16.39	12.88	10.52
OPA27EL-BSS4		15.68	12.32	10.07
OPA27EZ		11.00	8.35	6.65
OPA27FJ		8.55	5.95	4.95
OPA27FJ-BS		8.55	5.95	4.95
OPA27FJ-BSS1		30.20	20.46	16.34
OPA27FJ-BSS2		11.12	7.74	6.44
OPA27FJ-BSS3		9.83	6.84	5.69
OPA27FJ-BSS4		9.41	6.55	5.45
OPA27FL		11.65	8.70	7.45
OPA27FL-BS		11.65	8.70	7.45
OPA27FL-BSS1		38.45	28.71	24.59
OPA27FL-BSS2		15.15	11.31	9.69
OPA27FL-BSS3		13.40	10.01	8.57
OPA27FL-BSS4		12.82	9.57	8.20
OPA27FZ		8.55	5.95	4.95
OPA27GD			4.20	2.80
OPA27GJ		6.00	4.95	4.00
OPA27GJ-BS		6.00	4.95	4.00
OPA27GJ-BSS1		21.29	17.00	13.20
OPA27GJ-BSS2		7.80	6.44	5.20
OPA27GJ-BSS3		6.90	5.69	4.60
OPA27GJ-BSS4		6.60	5.45	4.40
OPA27GL		8.95	7.65	6.50
OPA27GL-BS		8.95	7.65	6.50
OPA27GL-BSS1		29.54	25.25	21.45
OPA27GL-BSS2		11.64	9.95	8.45
OPA27GL-BSS3		10.29	8.80	7.48
OPA27GL-BSS4		9.85	8.42	7.15
OPA27GP		5.25	4.15	2.95

CUSTOMER PRICE LIST—COMPONENT PRODUCTS

Prices in U.S. dollars | F.O.B. Tucson, Arizona | Quantity discounts available. | Effective June 1, 1987

MODEL	FOOT NOTE	1-24	25-99	100-249
OPA27GU		5.95	4.45	3.25
OPA27GZ		6.00	4.95	4.00
OPA27HT		67.09	55.46	44.10
OPA356AM		8.12	6.43	4.73
OPA37AJ		19.95	15.65	12.50
OPA37AJ-BS		19.95	15.65	12.50
OPA37AJ-BSS1		70.46	53.63	41.25
OPA37AJ-BSS2		25.94	20.35	16.25
OPA37AJ-BSS3		22.94	18.00	14.38
OPA37AJ-BSS4		21.95	17.22	13.75
OPA37AJQ		32.85	25.00	18.75
OPA37AL		23.85	18.75	15.00
OPA37AL-BS		23.85	18.75	15.00
OPA37AL-BSS1		78.71	61.88	49.50
OPA37AL-BSS2		31.01	24.38	19.50
OPA37AL-BSS3		27.43	21.56	17.25
OPA37AL-BSS4		26.24	20.63	16.50
OPA37AZ		19.95	15.65	12.50
OPA37AZQ		32.85	25.00	18.75
OPA37BJ		12.85	9.65	7.65
OPA37BJ-BS		12.85	9.65	7.65
OPA37BJ-BSS1		45.38	33.00	25.25
OPA37BJ-BSS2		16.71	12.55	9.95
OPA37BJ-BSS3		14.78	11.10	8.80
OPA37BJ-BSS4		14.14	10.62	8.42
OPA37BJQ		21.20	15.45	11.85
OPA37BL		16.25	12.50	10.15
OPA37BL-BS		16.25	12.50	10.15
OPA37BL-BSS1		53.63	41.25	33.50
OPA37BL-BSS2		21.13	16.25	13.20
OPA37BL-BSS3		18.69	14.38	11.67
OPA37BL-BSS4		17.88	13.75	11.17
OPA37BZ		12.85	9.65	7.65
OPA37BZQ		21.20	15.45	11.85
OPA37CD			6.30	4.20
OPA37CJ		9.95	7.50	5.95
OPA37CJ-BS		9.95	7.50	5.95
OPA37CJ-BSS1		35.15	25.74	19.64
OPA37CJ-BSS2		12.94	9.75	7.74
OPA37CJ-BSS3		11.44	8.63	6.84
OPA37CJ-BSS4		10.95	8.25	6.55
OPA37CJQ		16.45	12.00	9.25
OPA37CL		13.15	10.30	8.45
OPA37CL-BS		13.15	10.30	8.45
OPA37CL-BSS1		43.40	33.99	27.89
OPA37CL-BSS2		17.10	13.39	10.99
OPA37CL-BSS3		15.12	11.84	9.72
OPA37CL-BSS4		14.47	11.33	9.30
OPA37CZ		9.95	7.50	5.95
OPA37CZQ		16.45	12.00	9.25
OPA37EJ		11.00	8.35	6.65
OPA37EJ-BS		11.00	8.35	6.65
OPA37EJ-BSS1		38.78	28.71	21.95
OPA37EJ-BSS2		14.30	10.86	8.65
OPA37EJ-BSS3		12.65	9.60	7.65
OPA37EJ-BSS4		12.10	9.12	7.32
OPA37EL		14.25	11.20	9.15
OPA37EL-BS		14.25	11.20	9.15
OPA37EL-BSS1		47.03	36.96	30.20
OPA37EL-BSS2		18.53	14.56	11.90
OPA37EL-BSS3		16.39	12.88	10.52
OPA37EL-BSS4		15.68	12.32	10.07
OPA37EZ		11.00	8.35	6.65
OPA37FJ		8.55	5.95	4.95
OPA37FJ-BS		8.55	5.95	4.95
OPA37FJ-BSS1		30.20	20.46	16.34
OPA37FJ-BSS2		11.12	7.74	6.44
OPA37FJ-BSS3		9.83	6.84	5.69
OPA37FJ-BSS4		9.41	6.55	5.45
OPA37FL		11.65	8.70	7.45
OPA37FL-BS		11.65	8.70	7.45
OPA37FL-BSS1		38.45	28.71	24.59
OPA37FL-BSS2		15.15	11.31	9.69
OPA37FL-BSS3		13.40	10.01	8.57
OPA37FL-BSS4		12.82	9.57	8.20
OPA37FZ		8.55	5.95	4.95
OPA37GD			4.20	2.80
OPA37GJ		6.00	4.95	4.00
OPA37GJ-BS		6.00	4.95	4.00
OPA37GJ-BSS1		21.29	17.00	13.20
OPA37GJ-BSS2		7.80	6.44	5.20
OPA37GJ-BSS3		6.90	5.69	4.60
OPA37GJ-BSS4		6.60	5.45	4.40
OPA37GL		8.95	7.65	6.50
OPA37GL-BS		8.95	7.65	6.50
OPA37GL-BSS1		29.54	25.25	21.45
OPA37GL-BSS2		11.64	9.95	8.45
OPA37GL-BSS3		10.29	8.80	7.48
OPA37GL-BSS4		9.85	8.42	7.15
OPA37GP		5.25	3.95	2.95
OPA37GU		5.95	4.45	3.25
OPA37GZ		6.00	4.95	4.00

CUSTOMER PRICE LIST—COMPONENT PRODUCTS

Prices in U.S. dollars | F.O.B. Tucson, Arizona | Quantity discounts available. | Effective June 1, 1987

MODEL	FOOT NOTE	1-24	25-99	100-249
OPA37HT		67.09	55.46	44.10
OPA404AD			8.59	6.25
OPA404AG		16.74	13.50	9.40
OPA404AL		17.45	15.00	11.45
OPA404BG		22.12	17.01	13.49
OPA404BL		22.25	18.25	15.35
OPA404KP		11.85	9.25	6.95
OPA404SG		32.76	25.11	20.95
OPA404SL		31.75	25.75	22.45
OPA501AM		59.81	43.20	34.13
OPA501BM		70.56	51.68	39.74
OPA501RM		76.72	53.19	44.63
OPA501SM		91.84	64.64	52.45
OPA501SMQ		125.44	93.96	75.60
OPA501UM		86.00	75.75	68.10
OPA501UM/883B	+	94.75	83.40	74.85
OPA501VM		96.00	84.50	76.00
OPA501VM/883B	+	100.00	88.00	79.00
OPA511AM		45.00	38.50	34.50
OPA512BM		63.50	53.95	48.50
OPA512SM		76.50	66.50	61.50
OPA541AM		29.50	21.40	16.85
OPA541BM		34.75	25.20	19.85
OPA541SM		49.90	36.30	28.60
OPA600BM		101.85	85.05	77.70
OPA600CM		124.95	106.05	101.85
OPA600SM		128.10	106.05	101.85
OPA600TM		156.45	141.75	135.45
OPA600UM		143.00	115.00	102.00
OPA600UM/883B	+	165.00	145.00	137.75
OPA600VM		175.00	153.00	143.00
OPA600VM/883B	+	195.00	176.00	163.00
OPA605AM		76.80	61.00	52.80
OPA605CM		106.80	83.45	73.45
OPA605HG		61.80	50.40	44.55
OPA605KG		91.98	75.00	63.25
OPA606KD			3.78	2.42
OPA606KM		6.38	4.70	3.68
OPA606KP		4.20	3.10	2.60
OPA606LM		15.51	10.75	8.65
OPA606SM		15.96	11.07	8.95
OPA633AH		10.95	9.10	7.60
OPA633KP		5.80	4.85	4.00
OPA633SH		24.50	20.35	16.95
OPA8780UM	J			
OPA8780UM/883B	J,+			
OPA8780VM	J			
OPA8780VM/883B	J,+			
PCM53JG-I		50.00	40.63	28.75
PCM53JG-V		50.00	40.63	28.75
PCM53JP-I		22.05	20.48	12.76
PCM53JP-V		22.05	20.48	12.76
PCM53KP-I		24.68	22.31	13.91
PCM53KP-V		24.68	22.31	13.91
PCM54HP		19.43	18.38	11.45
PCM54JP		22.05	20.48	12.76
PCM54KP		24.68	22.31	13.91
PCM55HP		19.43	17.90	11.45
PCM55JP		22.05	20.56	12.76
PCM56P		20.48	19.43	12.60
PCM56P-J		23.10	21.53	13.91
PCM56P-K		25.73	23.36	15.23
PCM75JG		137.55	119.70	91.35
PCM75KG		156.45	135.45	103.95
PGA100AG		72.80	59.40	51.98
PGA100BG		80.64	66.96	56.70
PGA102AD			4.43	3.57
PGA102AG		12.26	9.72	8.03
PGA102BG		22.34	17.55	14.44
PGA102KP		6.66	5.13	4.15
PGA102SG		27.38	21.55	17.59
PGA200AG		57.68	43.15	36.49
PGA200BG		64.79	50.49	43.05
PGA201AG		57.68	43.15	36.49
PGA201BG		64.79	50.49	43.05
PWR 70	K	43.00	37.00	30.10
PWR 71	K	61.00	52.00	42.70
PWR 72	K	49.00	42.00	34.30
PWR 74	K	48.00	41.00	33.60
PWR 1XX	K	33.00	29.00	23.00
PWR 2XX	K	38.00	33.00	27.00
PWR 3XX	K	43.00	37.00	30.00
PWR 4XX	K	49.00	42.00	34.00
PWR 5XX	K	59.00	51.00	41.00
PWR 6XX	K	54.00	46.00	38.00
PWR 7XX	K	81.00	69.00	57.00
PWR 8XX	K	92.00	79.00	65.00
PWR1017	K	76.00	68.00	58.75
PWR5038	K	65.00	50.00	35.00
PWR510X	K	65.00	59.00	51.00
PWS 725	I	36.00	27.70	21.30
PWS 726	I	46.80	36.00	27.70

CUSTOMER PRICE LIST—COMPONENT PRODUCTS

Prices in U.S. dollars | F.O.B. Tucson, Arizona | Quantity discounts available. | Effective June 1, 1987

MODEL	FOOT NOTE	1-24	25-99	100-249
REF101JL		35.85	31.70	25.65
REF101JM		34.61	30.02	23.63
REF101KL		44.10	39.25	32.15
REF101KM		43.12	37.80	30.24
REF101RL		38.95	34.75	28.45
REF101RM		37.80	33.16	26.46
REF101RMQ		53.20	46.44	36.75
REF101SL		48.25	43.40	35.85
REF101SM		47.43	42.07	34.02
REF101SMQ		66.08	58.32	48.30
REF10JL		21.30	18.95	16.25
REF10JM		19.49	16.90	14.02
REF10KL		26.10	23.15	19.75
REF10KM		24.47	21.22	17.59
REF10RL		24.05	21.35	18.30
REF10RM		22.34	19.39	16.12
REF10RMQ		31.36	27.00	22.94
REF10SL		34.25	30.15	25.70
REF10SM		32.93	28.46	23.63
REF10SMQ		45.92	39.42	33.44
RF-500-108		8.95	8.25	7.65
SDM853	G	346.00	333.00	319.00
SDM854AG		241.50	193.20	162.15
SDM854BG		267.95	215.05	179.40
SDM856JG		208.15	166.75	139.15
SDM856KG		251.85	201.25	169.05
SDM857JG		223.10	178.25	149.50
SDM857KG		266.80	213.90	178.25
SDM862AH		154.00	129.00	111.00
SDM862AL	L,M	154.00	129.00	111.00
SDM862BH		178.00	146.00	127.00
SDM862BL	L,M	178.00	146.00	127.00
SDM862JH		128.00	117.00	103.00
SDM862JL	L,M	128.00	117.00	103.00
SDM862KH		145.00	129.00	118.00
SDM862KL	L,M	145.00	129.00	118.00
SDM862RH		239.00	204.00	189.00
SDM862RL	L,M	239.00	204.00	189.00
SDM862SH		298.00	255.00	235.00
SDM862SL	L,M	298.00	255.00	235.00
SDM863AH		154.00	129.00	111.00
SDM863AL	L,M	154.00	129.00	111.00
SDM863BH		178.00	148.00	127.00
SDM863BL	L,M	178.00	148.00	127.00
SDM863JH		128.00	117.00	103.00
SDM863JL	L,M	128.00	117.00	103.00
SDM863KH		145.00	129.00	118.00
SDM863KL	L,M	145.00	129.00	118.00
SDM863RH		239.00	204.00	189.00
SDM863RL	L,M	239.00	204.00	189.00
SDM863SH		298.00	255.00	235.00
SDM863SL	L,M	298.00	255.00	235.00
SHC298AM		8.35	5.78	4.73
SHC5320KH		13.40	11.60	9.80
SHC5320SH		61.00	52.75	44.70
SHC600BH	D		304.50	280.35
SHC76BM		99.00	75.00	63.00
SHC76KM		85.05	65.10	54.60
SHC803BM		182.70	141.75	129.15
SHC803BMQ		234.15	177.45	160.65
SHC803CM		212.10	160.65	147.00
SHC803CMQ		265.65	201.60	182.70
SHC804BM		168.00	127.05	115.50
SHC804BMQ		207.90	158.55	143.85
SHC804CM		183.75	138.60	127.05
SHC804CMQ		229.95	174.30	158.55
SHC80KP		64.05	43.05	35.70
SHC85		112.70	78.20	65.55
SHC85ET		170.20	126.50	121.90
SHC85ETQ		215.25	186.30	178.25
SHC85Q		180.55	126.50	105.80
SHM60		150.00	144.00	138.00
TM25-300HT		320.00	267.00	226.00
TM25-300NT		320.00	267.00	226.00
TM2500		325.00	290.00	195.00
TM27-12		320.00	267.00	226.00
TM2700		350.00	315.00	210.00
TM70		595.00	496.00	402.00
TM71		675.00	582.00	456.00
TM71-IO		790.00	658.00	533.00
TM76		595.00	496.00	402.00
TM76K		705.00	587.00	476.00
TM77		675.00	562.00	456.00
TM77-I/O		790.00	658.00	533.00
TM77K		805.00	671.00	543.00
TM77K-IO		895.00	746.00	604.00
UAF11		64.35	45.60	29.05
UAF21		102.60	88.10	58.69
UAF41		23.35	15.23	12.08
VFC100AG		10.45	8.70	6.95
VFC100AL		12.95	11.20	9.45
VFC100BG		16.40	13.65	10.95

Prices in U.S. dollars F.O.B. Tucson, Arizona Quantity discounts available. Effective June 1, 1987

MODEL	FOOT NOTE	1-24	25-99	100-249
VFC100BL		18.90	16.15	13.45
VFC100SG		18.95	15.95	13.65
VFC100SL		21.45	18.45	16.15
VFC320BG		15.95	11.75	8.95
VFC320BL		19.65	14.45	11.50
VFC320BL-BS		19.65	14.45	11.50
VFC320BL-BSS1		64.85	47.69	37.95
VFC320BL-BSS2		25.25	18.79	14.95
VFC320BL-BSS3		22.60	16.62	13.23
VFC320BL-BSS4		21.62	15.90	12.65
VFC320BM		15.60	11.40	8.75
VFC320BM-BS		15.60	11.40	8.75
VFC320BM-BSS1		56.59	39.44	29.70
VFC320BM-BSS2		20.28	14.82	11.38
VFC320BM-BSS3		17.94	13.11	10.06
VFC320BM-BSS4		17.76	12.55	9.63
VFC320CG		20.72	14.74	12.08
VFC320CL		20.75	15.50	13.25
VFC320CL-BS		20.75	15.50	13.25
VFC320CL-BSS1		68.48	51.15	43.73
VFC320CL-BSS2		26.98	20.15	17.23
VFC320CL-BSS3		23.86	17.83	15.24
VFC320CL-BSS4		22.83	17.05	14.58
VFC320CM		18.59	13.45	10.97
VFC320CM-BS		18.59	13.45	10.97
VFC320CM-BSS1		60.23	42.90	35.48
VFC320CM-BSS2		24.17	17.49	14.26
VFC320CM-BSS3		21.38	15.47	12.62
VFC320CM-BSS4		20.45	14.80	12.07
VFC320SL		25.20	18.90	16.30
VFC320SL-BS		25.20	18.90	16.30
VFC320SL-BSS1		83.16	62.37	53.79
VFC320SL-BSS2		32.76	24.57	21.19
VFC320SL-BSS3		28.98	21.73	18.75
VFC320SL-BSS4		27.72	20.79	17.93
VFC320SM		23.13	16.85	14.07
VFC320SM-BS		23.13	16.85	14.07
VFC320SM-BSS1		74.91	54.12	45.54
VFC320SM-BSS2		30.07	21.91	18.29
VFC320SM-BSS3		26.60	19.38	16.18
VFC320SM-BSS4		25.44	18.54	15.48
VFC32BD			8.45	5.55
VFC32BL		15.65	12.95	10.45
VFC32BL-BS		15.65	12.95	10.45
VFC32BL-BSS1		51.65	42.73	34.49
VFC32BL-BSS2		20.35	16.84	13.59
VFC32BL-BSS3		18.00	14.89	12.02
VFC32BL-BSS4		17.22	14.25	11.50
VFC32BM		11.95	9.95	7.95
VFC32BM-BS		11.95	9.95	7.95
VFC32BM-BSS1		43.40	34.48	26.24
VFC32BM-BSS2		15.54	12.94	10.34
VFC32BM-BSS3		13.75	11.44	9.14
VFC32BM-BSS4		13.15	10.95	8.75
VFC32BMQ		18.87	15.07	12.55
VFC32KP		8.95	7.45	5.95
VFC32SL		21.45	17.65	14.35
VFC32SL-BS		21.45	17.65	14.35
VFC32SL-BSS1		70.79	58.25	47.36
VFC32SL-BSS2		27.69	22.95	18.66
VFC32SL-BSS3		24.67	20.30	16.50
VFC32SL-BSS4		23.60	19.42	15.79
VFC32SM		18.30	14.98	11.85
VFC32SM-BS		18.30	14.98	11.85
VFC32SM-BSS1		62.54	50.00	39.11
VFC32SM-BSS2		23.79	19.47	15.41
VFC32SM-BSS3		21.05	17.23	13.63
VFC32SM-BSS4		20.13	16.48	13.04
VFC32SMQ		24.70	20.25	16.00
VFC32UM		15.00	11.00	10.45
VFC32UM/883B	+	20.00	16.00	15.20
VFC32VM		24.00	19.50	18.50
VFC32VM/883B	+	36.00	28.75	27.25
VFC32WM		30.00	24.00	22.75
VFC32WM/883B	+	34.00	27.50	26.00
VFC42BM		33.21	27.16	23.05
VFC42BP		23.91	18.74	16.49
VFC42SM		40.32	32.40	25.88
VFC52BM		33.21	27.00	23.05
VFC52BP		23.91	18.74	16.49
VFC52SM		40.32	32.40	25.88
VFC62BG		17.86	12.69	9.40
VFC62BL		19.65	14.45	11.50
VFC62BL-BS		19.65	14.45	11.50
VFC62BL-BSS1		64.85	47.69	37.95
VFC62BL-BSS2		25.55	18.79	14.95
VFC62BL-BSS3		22.60	16.62	13.23
VFC62BL-BSS4		21.62	15.90	12.65
VFC62BM		17.47	12.31	9.19
VFC62BM-BS		17.47	12.31	9.19
VFC62BM-BSS1		56.59	39.44	29.70
VFC62BM-BSS2		22.71	16.00	11.95

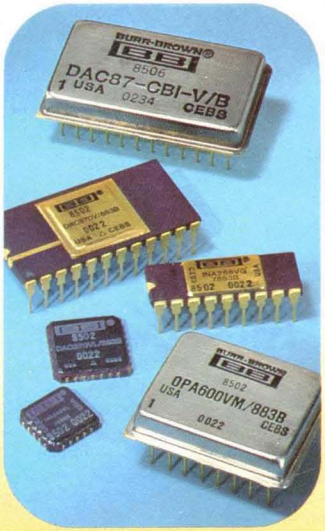
CUSTOMER PRICE LIST—COMPONENT PRODUCTS

Prices in U.S. dollars F.O.B. Tucson, Arizona Quantity discounts available. Effective June 1, 1987

MODEL	FOOT NOTE	1-24	25-99	100-249
VFC62BM-BSS3		20.09	14.16	10.57
VFC62BM-BSS4		19.22	13.54	10.11
VFC62CG		22.20	15.30	12.65
VFC62CL		20.75	15.50	13.25
VFC62CL-BS		20.75	15.50	13.25
VFC62CL-BSS1		68.48	51.15	43.73
VFC62CL-BSS2		26.98	20.15	17.23
VFC62CL-BSS3		23.86	17.83	15.24
VFC62CL-BSS4		22.83	17.05	14.58
VFC62CM		19.95	13.95	11.45
VFC62CM-BS		19.95	13.95	11.45
VFC62CM-BSS1		60.23	42.90	35.48
VFC62CM-BSS2		25.94	18.14	14.89
VFC62CM-BSS3		22.94	16.04	13.17
VFC62CM-BSS4		21.95	15.35	12.60
VFC62SL		25.20	18.90	16.30
VFC62SL-BS		25.20	18.90	16.30
VFC62SL-BSS1		83.16	62.37	53.79
VFC62SL-BSS2		32.76	24.57	21.19
VFC62SL-BSS3		28.98	21.73	18.75
VFC62SL-BSS4		27.72	20.79	17.93
VFC62SM		24.80	17.50	14.75
VFC62SM-BS		24.80	17.50	14.75
VFC62SM-BSS1		74.91	54.12	45.54
VFC62SM-BSS2		32.24	22.75	19.18
VFC62SM-BSS3		28.52	20.13	16.96
VFC62SM-BSS4		27.28	19.25	16.23
XTR100AM		42.56	38.50	30.40
XTR100AP		33.60	30.02	25.04
XTR100BM		51.52	46.82	37.75
XTR100BP		40.32	36.67	30.71
XTR101AD			7.30	5.50
XTR101AG		11.75	9.75	8.25
XTR101AL		14.25	12.25	10.75
XTR101AP		8.50	7.05	5.95
XTR101AU		8.95	7.40	6.25
XTR101BG		17.35	14.45	12.25
XTR101BL		19.85	16.95	14.75
XTR101SL		25.05	21.30	18.45
XTR110AD			7.45	4.95
XTR110AG		10.85	8.75	7.45
XTR110AL		14.25	11.65	10.15
XTR110BG		16.25	13.10	11.10
XTR110BL		20.05	16.15	13.95
XTR110KP		7.45	5.95	4.95
XTR110KU		8.40	6.55	5.40
XTR110SL		25.30	20.25	17.40

A) Not necessarily pin or spec compatible.
B) Expected date of last order 6/30/88.
C) ADC600K pricing: 1-4 $1995; 5-9 $1895; 10-24 $1795; ADC600B; 1-4 $2790; 5-9 $2650; 10-24 $2510.
D) SHC600BH pricing: 1-4 $329; 5-9 $321; 10-24 $314.
E) 25 piece minimum.
F) Minimum order is 10 pieces.
G) Connector supplied with each unit.
H) These products slated to be discontinued June 30, 1987.
I) Prices effective upon introduction.
J) Consult factory.
K) /G level I screening add 25% to pricing above; /T level II screening add 45% to pricing indicated above.
L) Eurocard evaluation PCB part #PC862/863-1 $16.00 each.
M) 68 pin LCC socket (Note N) part #MC0068-1 $14.00.
N) Manufacturer and part # for this socket is "Robinson Nugent" part #ICC-503 68-2-G (It is a U.S. part).
O) ADC80KD must be ordered in multiples of 36.

†Qualification reports $100 each.
Prices subject to change without notice. Minimum order $75.
 MKT-173B Printed in U.S.A. June, 1987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